

The Minicars Research Safety Vehicle Program Phase III

Volume II—Appendices

V. K. Ausherman

A. V. Khadilkar

S. R. Syson

C. E. Strother

D. E. Struble

Minicars, Inc. 55 Depot Road Goleta, California 93117

Contract No. DOT HS-7-01552 Contract Amount \$10,906,954 This document is disseminated under the sponsorship of the Department of Transportation in the interest of information exchange. The United States Government assumes no liability for its contents or use thereof.

1. Report No.	2. Government Accession No.	3. Recipient's Caralog No.
DOT-HS-806 214		İ
4. Title and Subtitle The Minicars Research Sai	Tety Vehicle Program	5. Report Date September 1981
Phase III - Volume II, Appendices		6. Performing Organization Code
7. Author's) V.K. Ausherman, A.V C.E. Strother, D.E. Struble	V. Khadilkar, S.R. Syson	8. Performing Organization Report No. RF-2100-09-81
9. Performing Organization Name and Addr	ess	10. Wark Unit No. (TRAIS)
Minicars, Inc. 55 Depot Road Goleta, California 93117	,	11. Contract or Grant No. DOT-HS-7-01552
12. Spansaring Agency Name and Address U.S. Department of Transp National Highway Traffic 400 Seventh Street, S.W.	13. Type of Report and Period Covered Final Report Jan 1977 to Sep 1981	
Washington, DC 20590		14. Spansaring Agency Code
15 Supelanasan Netes		

seppremental y manual

16. Abstract

The objective of the RSV Program was to provide research and test data applicable to the automobile safety performance requirements for the mid-1980s, and to evaluate the compatibility of these requirements with environmental policies, efficient energy utilization, and consumer economic considerations. The program was designed to answer the question, "Can small fuel-efficient cars be made safe?," and to address such topics as: How safe should cars in general, and small cars in particular, be? What technologies will be required to make them this safe? Are these technologies feasible? Can they be, or have they been, sufficiently developed to justify the promulgation of more stringent safety standards?

The RSV Program has demonstrated that it is possible to make cars much safer than they are presently. It has produced automobile designs that are consistent, at affordable cost, with the national objectives for fuel economy and environmental protection. It has indicated, at least to a limited degree, that the technological findings are applicable, at varying levels, to a variety of car designs. And it has provided evidence that these findings can be wrapped in a package of considerable appeal to the public.

This Final Report is a comprehensive compilation of the findings of the Phase III efforts of Minicars, Inc. It describes the design and testing of the RSV systems, and the performance levels achieved. Specific topics include a vehicle description and performance specification, the structure, occupant restraints, braking and handling, propulsion, the vehicle exterior, driver controls, the radar and electronics, the Large Research Safety Vehicle, and the accident environment analysis.

17. Key Words RSV, Safety, Crashworthiness, Radar, Large RSV, Foam-filling Technology RSV, Occupant Prote Anti-skid Braking, Minicars, A Electronics	through the Na	vailable to the ational Technicangfield, Virgini	1 Information	
19. Security Classif. (of this repart) Unclassified	20. Security Class Unclassifi		21. No. of Pages 301	22, Prico

METRIC CONVERSION FACTORS

	Approximate Con-	versions to Metri	c Measures	
Symbol	When You Know	Multiply by	To find	Symbol
		LENGTH		
sa fs yd ens	inches teet yards miles	*2.5 30 0.9 1.6	Centineles Centineles meters kikmeters	em em m kup
	aniug	AREA	K I I I I I I I I I I I I I I I I I I I	NIO.
in ² ft ² yd ³ mi ²	square inches square feet square yards square mites acres	6.5 0.09 0.8 2.6 0.4	squate centimeters square meters square meters square kilometers hectares	cm² m² m² km² ha
	<u>M</u>	ASS (weight)		
tb tb	ounces points short (ons (2000-16)	28 0.45 0.9	grans kilograns lumes	g kg t
		VOLUME		
tsp Tbsp 11 oz c pt	teaspoors tablespoors fluid ounces cups poots	6 15 30 0.24 0.47	millilaturs milliliters intlilaters laters	mi ml ml I I
gt gai ft ³ yu ³	pints quarts gallons cubic leut cubic yards	0.47 0.96 3.8 0.03 0.76	liters liters (iters Cubic meters Cubic meters	1113 1 1
	TEMP	ERATURE (exact)		
°f	falvenheit temperature	5/9 (alter suburcting 32)	Celsius tuniperature	°c

^{*)} in * 2.54 (exactly). For other match convensions and none detailed tables, see NBS Misc. Publ. 286, Units of Weights and Measures, Price \$2.25, SO Cotatog No. C13.10 286.

 -		=	-
•		=-	2
	=	≣	
_		=	66
	_=	≕	-
		=	
	_=	弄	-
		==	•
(20	_=	=	
		=	Ę
		===	
-	-	≡—	9
	_=	≡ _	9
		=	
		=	
-4	=	≡	÷
		==	
		==	
_		≡	:
		≡	
		=	
		≡	2
		≡	
٠.		=	
		≡	-
	_	=	_
_	==	=	7
	_=	=- -	•
	_=	=	
		₩	
GI .	_ _	≡	٠
		≡	
		=	:
-		==	
	-	≡	
		=	:
		≡	
4		=	
	=	☲	\$
	_=	=	
_	=	==	_ ;
	=	=-	
		≡	
		==	
w		≡	
		=	
		=	
	_=	≡-	
	==	=	
	=	≡ _	- 4
	=	=-	
		≡	
N	_=	\equiv	
		≡	
	- - <u>=</u>	≡	
	<u>=</u>	≡	•
		==	
		==	
	=	≡	•
		=-	
-		≡	
		=	•
		≡	
= -		≡	
ă .	=	■	. •
,	-=	==	Š
-		==	_

Approximate Conversions from Metric Measures

	When You Knew	Multiply by	To Find	Symb
		LENGTH		
anen,	millumters	9.84	inches	i
cm .	cantimeters	0.4	ınches	
മ	meters	3.3	lost	(
en Nom	k i jouetera	1.1 0.6	yaids Miles	1
		AREA		
		AREA		
ew ₅	square centimeters	0.16	square inches	je
au ²	ទាវិកាម្ភាព មានស្រុក	1.2	square yards	y
lun ²	square kilometers	0.4	adnate utjes	a
ha	hectares (19,000 m ²)	2.5	acres	
	<u>M</u>	ASS (weight)		
8	yams	6.035	DUBC 85	1
 ₽9	kilograms	2.2	pounds	
ı	tonnes (1000 kg)	1.1	short tons	
		AOTAWE	<u> </u>	
mJ	milliliters	0.03	fluid ounces	n
1	liters	2.1	pints	pt
l	titurs	1.06	quarts	qt
1	titers	0.26	gallons	ga
Ean	cubic meters	36	cubic feet	ħ.
w ₃	Cubic mulers	1.3	cubic yards	γd
	TEMP	ERATURE (exac	:1)	

APPENDIX A

RCA LABORATORIES FINAL REPORT

ELECTRONIC SUBSYSTEMS FOR THE RESEARCH SAFETY VEHICLE (PHASE III)

ELECTRONIC SUBSYSTEMS FOR THE RESEARCH SAFETY VEHICLE (PHASE III)

RCA Laboratories Princeton, NJ 08540



MARCH 1980

FINAL REPORT

Document is available to the U.S. public through the National Technical Information Service, Springfield, Virginia 22161.

Prepared for Minicars, Inc. 55 Depot Road Goleta, CA 93017 Prepared for the Department of Transportation, National Highway Traffic Safety Administration under Contract No. DOT-HS-01552. The opinions, findings, and conclusions expressed in this publication are those of the authors and not necessarily those of the National Highway Traffic Safety Administration.

The United States Government does not endorse products or manufacturers. Trade or manufacturer's names appear herein solely because they are considered essential to the object of this report.

This document is disseminated under the sponsorship of the Department of Transportation in the interest of information exchange. The United States Government assumes no liability for the contents or use thereof.

1. Report No.	2. Gavernment Accession No.	3. Recipient's Cotalog No.
4. Title and Subtitle		5. Report Date
ELECTRONIC SUBSYSTEMS	FOR THE RESEARCH	March 1980
SAFETY VEHICLE (PHASE	II I)	6. Performing Organization Code
7. Author(s) E. F. Belohoubek, J. J. Rosen, J. M. Cusack, R. E. Mar		8. Performing Organization Report No. PRRL-80-CR-8
9. Performing Organization Name and A RCA Laboratories	ddress	10, Work Unit No.
Princeton, New Jersey	08540	11. Contract or Grant No.
		13. Type of Report and Period Covered
12. Sponsoring Agency Name and Addres	15	Final Report
Minicars, Inc.		3/1/77 to 11/15/79
55 Depot Road		N. C. and A. and C. do
Goleta, California 930	017	14. Sponsoring Agency Code
15. Supplementary Notes		

16. Abstract

This final report covers Phase III of RCA's effort in the DOT sponsored development of the Research Safety Vehicle (RSV) for the mid 80's. Minicars, Inc., is the prime contractor on this program with RCA being responsible for the radar, sensor and display subsystems of the RSV. The radar, an FM/CW system interfaced with a microcomputer, is used to provide: (a) collision-mitigation braking, (b) automatic headway control, and (c) driving-related warning messages.

The collision-mitigation function of the RSV involves the application of antiskid brakes under conditions where, based on radar and other sensor inputs, it is certain that a severe collision will take place. Other objects, not directly in the immediate path of the vehicle, must not trigger the brakes. The optimization of the radar processing hardware and associated computer algorithm for this function was performed with the help of tape recordings (both video and radar IF) for a large variety of road, traffic, and weather conditions. Separate, simulated collision tests were performed with an expendable target (corner reflector) to demonstrate the short reaction time of the system.

The automatic headway-control system has the task to keep a safe distance with respect to the car ahead based on speed and range inputs. Without other vehicles close by, the system functions as a standard cruise control. Successful operation of the headway-control system interfaced with the car throttle was demonstrated on an RCA-owned station wagon. The integration of the system into the RSV is a separate follow-on task.

Driving-related information, such as speed, mileage, fuel economy, fuel level, etc., together with warning messages such as water temperature too high, oil pressure too low, emergency brake on, doors open, etc., are shown on an alphanumeric plasma display which is interfaced through a microcomputer to various sensors.

17. Key Words (Selected by Author(s))		18. Distribution Statement		
Research Safety Vehicl	le	Document	is available	to the U.S.
Collision-mitigation h	public through the National Technical Information Service.			
Automatic headway cont				
Driving-related warning messages			eld, Virginia	•
19. Security Classif. (of this report)	20. Security Classi	f. (of this page)	21. No. of Pages	22. Price
Unclassified Unclass		sified	196	

^{*}For sale by the Clearinghouse for Federal Scientific and Technical Information, Springfield, Virginia 22151.

PREFACE

This Final Report describes work performed at the Microwave Technology Center of RCA Laboratories, Princeton, New Jersey, from March 1, 1977 to November 15, 1979, under subcontract P.O. 5062 from Minicars, Inc., Goleta, California. The prime contract for this effort was DOT-HS-7-01552, with Mr. Jerome Kossar from National Highway Traffic Safety Administration as contracting officer.

The program was carried out under the direction of Dr. Erwin F. Belohoubek, Head of the Microwave Circuits Technology. The following scientists participated in the development effort: John J. Risko, Mordechay Ilovich, Jerome Rosen, and Joseph M. Cusack (part-time consultant). The major portion of the effort on the radar headway control was carried out under separate RCA funding, with William R. Lile as project scientist.

TABLE OF CONTENTS

Secti	on			Page	
I.	INTRODUCTION				
II.	OVE	RALL	SYSTEM LAYOUT	5	
III.	RAD	AR RE	EDESIGN	8	
	A.	Ku-F	Band, Bistatic Noncooperative Radar	8	
		1.	Block Diagram	8	
		2.	System Parameters	10	
			a. RF Frequency Considerations	10	
			b. Bistatic Radar Considerations	12	
			c. Modulation Parameters	13	
		3.	Range and Range-Rate Accuracy	15	
		4.	Antenna Design and Measurement	20	
		5.	Coverage Pattern Measurements	21	
		6.	IF Amplifier Shaping for CMS	26	
	В.	Dua]	l-Mode X-Band Radar	28	
		1.	Block Diagram	28	
		2.	System Parameter Selection	30	
		3.	Coverage Pattern Measurements	33	
	c.	Rado	ome for RSV Installation	37	
IV.	PRO	CESS	OR HARDWARE	46	
	A.	Rada	ar Cards for CMS and Headway Control	46	
		1.	Introduction	46	
		2.	Phase II Radar Card	47	
		3.	Phase III Radar Card	50	
		4.	Revised Phase III Radar Card	52	
		5.	Threshold Circuit	53	
	В.	CPU	and Memory	55	
		1.	Introduction	55	
		2.	Phase III Evaluation-Board System	56	
		3.	CPU and Memory Card Cage for RSV Installation	59	
		4.	Remote-Start Circuit for CPU	60	
	c.	Dist	play and Sensor Interfaces	65	

TABLE OF CONTENTS (Continued)

Sectio	n		Page
V.	CONTROL FUNCTIONS AND SOFTWARE IMPLEMENTATION		
	A.	Collision-Mitigation Braking Considerations	75
	В.	Collision-Mitigation System	78
	C.	Headway/Cruise Control	82
		1. Introduction	82
		2. Design Considerations	83
		3. Algorithm Flow Diagram	89
VI.	PER	FORMANCE TESTS	92
	Α.	Test Van Instrumentation	92
	В.	Collision-Mitigation System Tests	97
	С.	Headway-Control Tests	104
		1. System Optimization	104
		2. Road Tests	105
		3. Headway-Control Demonstration Vehicle	111
VII.	INS	STALLATION OF EQUIPMENT INTO THE RSV	115
	A.	General	115
	В.	Microcomputer and Sensor Installation	115
	C.	Radar Safety Considerations	118
VIII.	cos	ST ESTIMATES	120
IX.	CON	CLUSIONS AND RECOMMENDATIONS	122
APPENI	DIX A	A. COVERAGE PATTERN CALCULATIONS	A-1
APPENI	DIX I	3. SOFTWARE LISTING FOR CMS ALGORITHM	B-1
APPENI	OIX (C. SOFTWARE LISTING FOR ARITHMETIC SUBROUTINE GETRAN	C-1
APPENI	DIX I	O. SOFTWARE LISTING FOR ELECTRONIC DASHBOARD DISPLAY	D-1
nereni	entora		D_1

LIST OF ILLUSTRATIONS

Figu	are	Page
1.	Block Diagram of Electronically Related Functions in RSV	6
2.	Block Diagram of the Ku-Band FM/CW Radar	8
3.	Front and Back View of the Radar Assembly	9
4.	Asymmetric Triangular Modulation	16
5.	Single Cycle of Nonlinear Modulation Waveform	18
6.	Single Cycle of Distorted IF Frequency	20
7.	Exploded View of Antenna	22
8.	Azimuth Ku-Band Pattern	23
9.	Elevation Ku-Band Pattern	23
10.	Typical Radar-Target Configuration for Coverage Pattern	
	Measurements	24
11.	Coverage Pattern Ku-Band Radar - Output of Preamplifier	25
12.	Coverage Pattern Ku-Band Radar - Output of Postamplifier	25
13.	Transfer Characteristic of Ku-Band Preamplifier	26
14.	Transfer Characteristic of CMS Postamplifier	27
15.	Composite of Preamplifier and Postamplifier	27
16.	Block Diagram of Dual-Mode Radar	30
17.	(a) Typical IF Voltage Waveform for 0- to 180-Degree Phase	
	Modulator. (b) Output of Envelope Detector	31
18.	Cooperative Channel of Dual-Mode X-Band Radar	34
19.	Baseband Channel of Dual-Mode X-Band Radar	34
20.	Location of Microwave Tag Mounted on Vehicle	35
21.	X-Band Dual-Mode Radar Mounted on Vehicle	36
22.	Anechoic Chamber for Antenna Measurements	38
23.	Azimuth Antenna Pattern (Nose and Air Scoop)	39
24.	Elevation Antenna Pattern (Nose and Air Scoop)	39
25.	Radome Construction	41
26.	Azimuth Antenna Pattern With Radome	42
27.	Elevation Antenna Pattern With Radome	43
28.	Bistatic Ku-Band Radar with Radome	44
29.	RSV With Radar and Radome in Place	45
30.	Block Diagram of Phase II CMS Card	48

LIST OF ILLUSTRATIONS (Continued)

Figu	re	Page
31.	Waveforms on Radar Interface Card	48
32.	Signal-Processing Time Relations	49
33.	Block Diagram of Phase III CMS Card	51
34.	Revised Phase III CMS Card	53
35.	Threshold Detection Circuits	54
36.	Evaluation Board with Card Cage and Display	58
37.	Evolution From Development Board to Full Card Cage System	59
38.	Block Diagram of CPU Card	60
39.	Photograph of CPU Card	61
40.	Complete CMS Card Cage	62
41.	CMS Card Cage with Cover Removed	63
42.	Size Comparison - Microcomputer and CDS	64
43.	Remote-Start Circuit	65
44.	8-Input Analog/Digital Circuit	67
45.	Trip Odometer Circuit	67
46.	Clock Circuit Diagram (Oscillator and Minute Counter)	69
47.	Clock Circuit Diagram (Hour Advance)	69
48.	Tachometer Interface Circuit	70
49.	Fuel Economy Sensor Circuit	70
50.	Schematic of Display Interface	72
51.	Binary Input Card for Switches	73
52.	Schematic of Airbag Indicator	73
53.	Schematic of Velocity Indicator	74
54.	Distance/Time Relation Between Two Vehicles, One of Which is	
	Being Braked	75
55.	Impact Velocity as Function of Distance Between Radar Car and	
	Collision Object (System Delay 0.2 s; Braking Coefficient	
	$\mu = 0.9$)	76
56.	Energy Reduction as Function of Detection Distance and Closing	
	Rate	77
57.	Flow Chart of GETRAN (Date Acquisition)	79
58.	Flow Chart of Main CMS Program	80
59.	Comparison Between Cruise Control and Radar Headway Control	83

LIST OF ILLUSTRATIONS (Continued)

Figu	re	Page
60.	Block Diagram of Headway-Control System	84
61.	Automatic Cruise/Headway-Control Algorithm	85
62.	State Transition Diagram	87
63.	Capture Mode	88
64.	Headway-Control Flow Chart	91
65.	Test Van for Recording of Video and Radar Information	93
66.	Interior of Test Van	94
67.	View from Test Van During CMS Tests on Airport Runway	95
68.	Block Diagram of Power Distribution in Test Van	96
69.	Test Van During CMS Test with Expendable Target	97
70.	Block Diagram and Waveforms of Recording System	99
71.	Block Diagram of Playback System	101
72.	System for Simultaneous Playback of Radar and Video Information .	102
73.	Headway-Control Computer and Strip Chart Recorder Mounted in	
	Front of RCA Station Wagon	106
74.	Linear Throttle Activator	107
75.	Early Recording of Cooperative Radar Car Following A Target	
	Car Operating in Cruise Control at 45 mph	109
76.	Noncooperative Ku-Band Radar Car Following Standard Passenger	
	Car (Pinto) Using Optimized Algorithm	110
77.	Headway-Control Radar Mounted on RCA Station Wagon	112
78.	Display Format for Headway-Control Demonstration	114
79.	Electromechanical Arrangement for Steering Angle Determinations .	117
80.	Antenna Field Intensities	118
A-1	Calculated Detection Pattern (No Shaping)	132
A-2	Calculated Detection Pattern (High Pass: 1 Section, Cutoff at	
	30.7 m)	133
A-3	Calculated Detection Pattern (Low Pass: 4 Section, $R_c = 32.2 \text{ m}$;	
	High Pass: 1 Section, R _c = 15.4 m)	134
A-4	Cooperative Radar-Tag Geometry for Coverage Pattern Measure-	
	ments	137
A- 5	Detection Pattern for Cooperative Radar (Output of Detector)	139

LIST OF ILLUSTRATIONS (Continued)

Figure		Page
A-6	Detection Pattern of Cooperative Radar (Output of Post-	
	amplifier)	140
A-7	Detection Pattern of Monostatic, X-band, Noncooperative Radar	
	(Output of Preamplifier)	142

SECTION I

INTRODUCTION

This report covers Phase III of the development effort, sponsored by the National Highway Traffic Safety Administraton (NHTSA) under contract No. DOT-HS-7-01552, toward the demonstration of various electronic subsystems for the Research Safety Vehicle (RSV), for the mid-1980s time frame. Specifically, this effort encompassed extensions of the electronic functions that act as driver aids and that maximize the vehicle's collision avoidance and mitigation capabilities, with the final goal of installing these systems in the latest, high technology version of the RSV. This work was conducted by the Microwave Technology Center of RCA Laboratories in Princeton, New Jersey, under subcontract from Minicars, Inc., Goleta, California, during the period from March 1977 to November 1979.

The major effort during Phase III was directed toward the development of an FM/CW radar that, interfaced with a microcomputer, provides the following functions: (a) collision mitigation braking; (b) automatic safe headway control; and (c) driving-related warning messages. These warning messages are flashed on a self-scan alphanumeric plasma display which, driven by another microcomputer, also shows general operating and functional data such as speed, mileage, fuel level, oil pressure, water temperature, etc.

While the provision of safety and warning messages represented merely an extension and refinement of an existing system developed during Phase II, the collision-mitigation and headway-control systems required substantial development efforts to demonstrate their practical potentials in a real traffic environment. Early road tests with the initial radar system during Phase II had clearly shown the need for a more systematic approach to the optimization of the radar system to ensure proper operation and elimination of practically all false alarms under a wide variety of driving conditions. A large portion of Phase III was thus devoted to the tape recording of a wide variety of road, traffic, and weather conditions to permit a thorough optimization of the radar processing hardware and associated computer algorithm.

We also proceeded from initial headway-control experiments during Phase II that provided only speed-up or slow-down messages to a closed-loop system with the throttle of the car tied to the radar system for truly automatic headway

control. The inclusion of proportional braking into the automatic headwaycontrol action, which would further enhance the acceptability of this function to the driver, was not yet included on the present test car.

The specific goals for the Phase III effort as originally formulated are listed below:

- Task 1 Installation of Phase II radar and display into RSV exhibition vehicle.
- Task 2 Radar improvements, including dual-mode operation (cooperative/noncooperative).
- Task 3 Road tests using tape recordings of radar output, together with video information of traffic conditions to optimize signal processing algorithm.
- Task 4 Final system integration and installation in high technology RSV.
- Task 5 Cost effectiveness studies.

During the early portion of the program it became apparent that a shift in the operating frequency of the radar to higher values would be beneficial. We also learned at that time of three major government-sponsored programs in Germany [1,2,3], all directed toward radar warning on high-speed expressways. Consequently, we concentrated our efforts mainly on collision mitigation and headway control, rather than long-range warning that was being explored by German companies very extensively using sophisticated 35-GHz radars. In addition, our program experienced a serious slow-down due to funding shortages that eventually led to a stretch of the program from the originally planned 18 months to 33 months.

^{1.} D. Zur Heiden and H. Oehlen, "Radar Anticollision Warning System for Road Vehicles," Electrical Communications 52(2), 141 (1977).

^{2.} G. Hahlganss and L. Hahn, "Headway Radar Using Pulse Techniques," Int. Conf. on Automobile Electronics, London, July 1976, pp. 132-135.

^{3.} E. Dull and H. Peters, "Collision Avoidance System for Automobiles," Society of Automotive Engineers, Publication #780263, March 1978.

The above factors resulted in a redefinition of the program goals, as outlined in a new work statement dated May 1978 and listed in abbreviated form below:

Task 1 - Demonstration of Radar Functions in RCA-Owned Vehicles

- (a) Headway control using a cooperative X-band radar
- (b) Headway control using the new Ku-band noncooperative radar
- (c) Collision-mitigation function tests with expendable target

Task 2 - Radar Improvements

- (a) Design, fabricate, and test dual-mode (cooperative/noncooperative) radar at X-band
- (b) Develop noncooperative bistatic Ku-band radar
- (c) Improve processor algorithm and reliability of microcomputer system
- (d) Interface throttle and brakes to microprocessor

Task 3 - Road Test Program

- (a) Equip RCA test van with video recorder and synchronized radar IF output recorder
- (b) Perform tape recordings of test rides under a wide variety of traffic, road, and weather conditions
- (c) Optimize radar processing and computer algorithms of collision mitigation and headway-control* functions
- (d) Perform final road tests of both systems in RCA cars under actual traffic conditions

Task 4 - Final System Integration

- (a) Fabricate and install Ku-band noncooperative bistatic radar, display, and associated microcomputers in a high-technology version of RSV
- (b) Calibrate all sensor functions, optimize radar performance and put all algorithms in the programmable read-only memory (PROM)

^{*}The development of a digital cruise control, the headway control, and fuel economy experiments with these systems were performed on RCA cars under separate RCA funding.

Task 5 - Cost Study

Estimate the 1985 cost of individual systems in 1979 dollars using RCA's PRICE program

Practically all of the above tasks have been completed, except that in the present version of the high-technology RSV, the tie-in between the headway microcomputer and the automatic, electronically shifted transmission was not implemented. Due to a series of program delays and the unavailability in time of a properly functioning computer-controlled transmission, the final optimization of the automatic headway control could not be carried out in the RSV. The basic feasibility of this function was demonstrated instead on a separate RCA station wagon, which was refurbished specifically for demonstration purposes.

The final integration of the headway control into the RSV is the objective of a planned follow-up program which will be a joint effort between Dubner Computer Systems,* Minicars, and RCA, and will be performed at RCA Laboratories in Princeton toward the middle of 1980. The results of this final integration will be reported separately.

^{*}Dubner Computer Systems, New York City, NY.

SECTION II

OVERALL SYSTEM LAYOUT

As mentioned before, the use of radars for long-range warning-only purposes has been explored extensively by several companies under government sponsorship in Germany. These radars are geared mainly toward warning the driver of impending dangerous situations and leaving the decision to react to this warning to the driver. Because of the relatively long reaction time of the driver (between 0.6 to 1 s), the warning has to be based on long-range information (typically 100 to 150 m) at the high speeds prevalent on many of Europe's expressways.

The situation in the United States, having a maximum speed limit of 90 km/h (55 mph) throughout, is substantially different. Here we try to effect a societal savings by mitigation of an inevitable collision. The key considerations are elimination of all false alarms and automatic application of antiskid brakes under conditions where, due to human error or mechanical failure, a severe collision is definitely unavoidable. This limits the action range of the radar to 25 to 30 m because for longer distances, the opportunities for false alarms increase rapidly and more importantly, a skilled driver possibly could still perform an avoidance maneuver which could be hampered by the application of antiskid brakes. Thus, the emphasis is on an automatic reaction only where a high-speed collision is unavoidable. This does not exclude the use of the radar for warning purposes over a longer range; the latter subject, however, has been covered extensively by the German radar development efforts and thus was not addressed in this program.

While the collision-mitigation function mentioned above is tailored mainly to safety aspects of the car, the automatic headway control could substantially improve the driver comfort and increase the throughput on high-density highways. Since the collision-mitigation function of the radar would not be used by the average driver so long as he is not involved in an accident, the simultaneous use of the radar for driver convenience is expected to lend a strong sales appeal to the inclusion of a radar in future cars.

In addition to the radar functions, the high-technology version of the RSV includes also a computer-controlled plasma display that provides driving-related information such as speed, mileage, fuel level, water temperature, etc., to the driver in either digital form or as analog bars. The selection

of the type of display format can be made through a switch by the driver. Malfunctions or safety hazards are indicated on the display by temporary flashing of warning messages which interrupt the normal display in 30-second intervals until the particular hazard has been corrected.

A block diagram of all electronically related functions in the RSV is shown in Figure 1. The processed radar signal is fed to two separate microprocessors, one for collision mitigation and one for headway control. A series of other sensor inputs, such as vehicle speed, steering angle, brake pedal position, and cruise control inputs are also interfaced with the respective microprocessors.

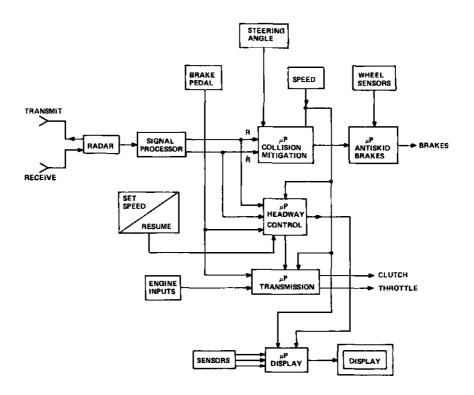


FIGURE 1. BLOCK DIAGRAM OF ELECTRONICALLY RELATED FUNCTIONS IN RSV.

At present, separate microprocessors are used for the collision-mitigation system (CMS), the headway control, the display, the antiskid system,* and the automatic gear shift of the car. The latter function, being developed under subcontract to Minicars by Dubner Computer Systems, Inc., is important for

^{*}An experimental antiskid system, manufactured by Bendix, is used in the RSV.

improved fuel economy and interfaces directly with the commands from the automatic radar headway control. Later versions of the RSV could possibly use only two or three microprocessors, whereby one could perform certain vital functions in case of failure of the others to preserve a limp-home ability. Questions of time sharing between microprocessors and interleaving of programs, however, have not been addressed during this program.

SECTION III

RADAR RF DESIGN

A. Ku-BAND, BISTATIC NONCOOPERATIVE RADAR

1. Block Diagram

The Ku-band radar is a forward-looking, bistatic noncooperative FM/CW radar. A block diagram of the system is shown in Figure 2. The RF section of the radar consists of a transmitter chain and receiver chain; each with its own antenna. The transmitter chain consists of a varactor-tuned oscillator and modulator, power divider, and printed circuit antenna. The receiver chain consists of a printed circuit antenna (same as in the transmit arm), isolator, and mixer. The IF section is made up of a shaped preamplifier and shaped postamplifier. Voltage regulators and ignition noise filters are included in the amplifiers.

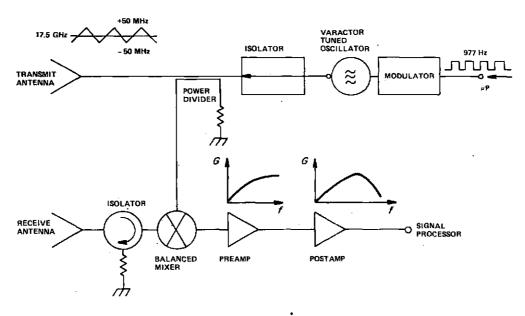


FIGURE 2. BLOCK DIAGRAM OF THE Ku-BAND FM/CW RADAR.

Figure 3 shows front and back views of the radar assembly with the radome removed. Also shown as part of the radar assembly are the radome supports, which serve as the transition members between the radar and the hood of the RSV. The radome conforms to the contour of the RSV and is made up of blocks of polystyrene covered with expanded polyethylene. The radome will be discussed in greater detail in subsection III.C below. The performance features of the radar are given in Table 1.

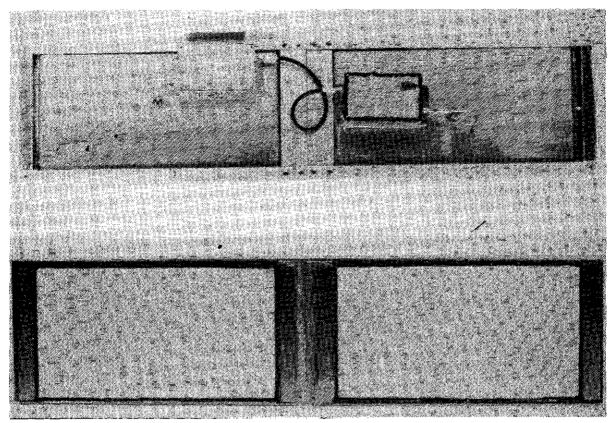


FIGURE 3. FRONT AND BACK VIEW OF THE RADAR ASSEMBLY.

TABLE 1. PERFORMANCE CHARACTERISTICS OF Ku-BAND RADAR

Parameter	Value
Frequency, f	17.5 GHz
Power Output, Po	10 mW
Frequency Deviation, Δf	<u>+</u> 50 MHz
Modulation Rate, f	977 Hz
Beamwidth Horizontal, θ _H	3°
Beamwidth Vertical, $\theta_{ m V}$	5°
Antenna Gain, G	30 dB
Bistatic Antenna Assembly Size	77 cm x 20.5 cm x 2.5 cm
Range	7 to 30 m, collision mitigation 8 to 50 m, headway control
Range-Rate	0-60 m/s

The operation of the radar is as follows: referring to Figure 2, the varactor-tuned oscillator and modulator furnish a 15-mW frequency-modulated carrier to the power divider. The carrier frequency is 17.5 GHz and has triangular modulation of ± 50 MHz deviation. One output of the power divider (11 mW) is directed to the antenna while the other output (2.75 mW) enters the local oscillator port of the mixer via a rigid cable. The power split is 6 dB to compensate for the 1.6-dB loss in the cable. The transmitted signal is reflected back to the radar from a target and coupled to the signal port of the mixer through the antenna and isolator in the receiver chain.

Due to the time delay between transmission and reception, the frequency of the received signal differs from the transmitted signal (local oscillator signal), and a beat frequency signal will be generated at the IF port of the mixer. The beat frequency contains the desired range and range-rate information which is recovered in the processing circuitry. The details of the signal processing are given in Section IV. Range and range-rate accuracy are discussed in subsection III.A.3 below. Range and range-rate information, speed of the radar-equipped vehicle, and steering angle are processed further to determine if a vehicle control action is necessary. The speed and steering angle are derived from transducers coupled to the speedometer and steering column of the vehicle, respectively. The software algorithms used for the control decisions are discussed in Section V.

2. System Parameters

a. RF Frequency Considerations

To avoid false alarms from vehicles in adjacent lanes or roadside objects, a narrow antenna beam is desirable. For a narrow antenna beam, a large radiating surface is required, large with respect to a wavelength. For example, the X-band antenna used during Phase II is 28 x 17 cm (9.9 x 6 wavelengths) and provides a beam 5 degrees wide in azimuth and 10 degrees wide in elevation. Beamwidths are measured at the 3-dB points of the gain pattern. To decrease the beamwidth by a factor of two in azimuth and elevation, the required cross section becomes (19.9 x 12 wavelengths) or 56 x 34 cm at X-band. However, if the RF frequency were doubled, the same antenna area would provide an antenna pattern of half the beamwidths. Thus from both a size and ultimately cost standpoint, it is desirable to increase the RF frequency. The major limitation

to this trend is the availability and cost of RF components at the higher frequencies. The upper end of Ku-band (17.5 GHz) was chosen as a compromise frequency.

At 17.5 GHz, transferred electron oscillators (TEOs) are still state-of-the-art devices, and microstrip technology can be applied cost effectively to the other microwave components. In addition, microwave absorption through the atmosphere is still small, 0.02 dB/nautical mile for 1% water vapor and 6 dB/nautical mile for heavy rain. From the X-band reference of 10.575 GHz, a 40% size reduction is expected. The actual Ku-band antenna is 33 x 19 cm (19 x 11 wavelengths) and has a 3-degree beamwidth in azimuth and a 5-degree beamwidth in elevation.

A 3-degree beamwidth has been found to be a good compromise between beam confinement at far ranges and target acquisition at close range. For example, at 50 m the beam coverage is ±1.31 m. Although the possibility of missing a target off to the side exists at close range, the decreased probability of false alarms in the far field is of greater importance.

For a well designed antenna, reducing the beamwidth will increase the gain. If the same current distribution would exist at X-band and Ku-band, reducing the beamwidths by a factor of two in azimuth and elevation would yield a 6-dB increase in gain. From the range equation the power returned to the radar is proportional to the square of the antenna gain, and square of the wavelength [4]. The net effect of increasing the gain by 6 dB and decreasing the wavelength would be a 8-dB increase in returned power for constant transmitted power. However, for the actual 17.5-GHz antenna, the gain only increased by 5 dB so that the returned power increased by 6 dB.

The location of multipath nulls is also dependent on the RF frequency. The range at which multipath nulls appear is given by, [5]

$$R = \frac{2h_1h_2}{\lambda N}$$
 , $N = 0$, 1, 2, ... (1)

where λ is the wavelength, h_1 is the effective height of the antenna above ground, h_2 is the effective height of the target above ground, and N=0 corresponds to $R=\infty$.

^{4.} F. E. Nathanson, Radar Design Principles, (McGraw-Hill Publishing Company, New York, 1969).

S. A. Hovanessian, <u>Radar Detection and Tracking Systems</u>, (Artech House, Inc., Massachusetts, 1973).

Experimentally it has been found that the farthest null from the radar, corresponding to N = 1, is the most severe. Assuming $h_1 = h_2 = 0.675$ m, the first null occurs at 32 m in X-band. For a headway control system it is desirable to operate out to 50 m. A multipath null at 32 m would result in unstable operation around 32 m. To ensure smooth tracking out to 50 m, the multipath null should be moved beyond 50 m. By increasing the frequency to 17.5 GHz, the first null occurs at 53 m. This has been found to be acceptable.

b. Bistatic Radar Considerations

A shortcoming of CW radars is the lack of complete isolation between the transmitter and receiver. In a monostatic configuration (single antenna for transmit and receive), the antenna mismatch is the basic coupling mechanism between the transmitter and receiver. For example, an antenna with a VSWR of 1.2:1 will reflect 1% of the transmitter power to the receiver. By comparison in Ku-band, a 1-m² target 30 m from the radar returns only -67 dB to the receiver. Causes for the antenna reflection may be a slight mismatch between the feedline and the antenna or also the accumulation of snow or dirt on the front of the antenna radome.

The most serious problem caused by the coupled power, or spillover as it is more commonly called, is distortion of the IF amplifier output. In order to process the radar return and extract range and range-rate accurately, a flat amplifier response is required.

Because of spillover, the amplifier baseline is distorted and processing errors occur. Spillover also causes dynamic range problems when the spillover is orders of magnitude above the minimum detectable signal (MDS). A bistatic radar reduces this problem since separate antennas are used for transmit and receive. The basic coupling between transmitter and receiver for the bistatic system is through radiation from the transmit antenna to the receive antenna. The amount of radiation is a function of the antenna radiation pattern and the geometry of the antennas. For the stripline antennas mounted in the RSV that leakage is approximately -60 dB.

Another mode of spillover, even in bistatic radars, is through the mixer. Due to the finite isolation between the LO and signal port, some of the LO power is coupled to the signal port. An isolator before the receive antenna is used to reduce the effects of this source of spillover.

Although bistatic arrangements are larger and thus somewhat costlier, this configuration was chosen for the Ku-band radar to ensure reliable operation with high sensitivity.

c. Modulation Parameters

The general considerations made in choosing triangular FM modulation were given in the final report of Phase II [6] and will not be repeated here. Only the choice of modulation parameters for the Ku-band radar will be discussed.

Range accuracy is proportional to the bandwidth of the transmitted signal, while the range-rate accuracy is proportional to the processing time. Since the processing time is inversely proportional to the repetition frequency, some tradeoffs must be made between response time and range-rate accuracy. These tradeoffs are different for the CMS and the headway-control system. The CMS requires response times of the order of less than 100 ms while 0.5 s is adequate in the headway-control mode. For these response times, the 1-kHz repetition rate used previously for the X-band radar is adequate. In practice, because of greater stability, the 2-MHz crystal in the microprocessor is divided down to 977 Hz and serves as the repetition frequency.

The choice of the frequency deviation, Δf , about the center frequency is based on the following considerations:

The IF frequency, f_B , during the modulation upsweep, f_{up} , and downsweep, f_{down} , is given by [6]

$$f_{up} = \left| \frac{8\Delta f f_m R}{c} \right| + \left| \frac{2 f_o \dot{R}}{c} \right|$$

$$f_{down} = \left| \frac{8\Delta f f_m R}{c} \right| - \left| \frac{2 f_o \dot{R}}{c} \right|$$
(2)

The first term in equation (2) is often referred to as the range frequency, f_r , and the second term as the doppler frequency, f_d . Since \hat{R} can be positive or negative, depending on whether the target is inbound or outbound, equation (2) holds for an outbound target. For an inbound target, the sign of \hat{R}

^{6.} E. F. Belohoubek et al., "Electronic Subsystems for Research Safety Vehicle (RSV)," Final Report, Phase II, 1976.

is reversed and the beat frequency during upsweep is less than the beat frequency during the downsweep. This allows the determination of the direction of the range-rate during processing. When the range frequency, f_r , is greater then the doppler frequency, f_A , equation (2) becomes

$$f_{up} = |f_r| + |f_d|$$

$$f_{down} = |f_r| - |f_d|$$
(3)

and

$$\left| f_r \right| = \frac{1}{2} (f_{up} + f_{down}) = f_{B AVG}$$

$$\left| f_d \right| = \frac{1}{2} (f_{up} - f_{down})$$
(4)

From equation (4) it is seen that the range is proportional to the beat frequency averaged over a modulation cycle and the range-rate is proportional to the difference between upsweep and downsweep frequencies. When the doppler frequency is greater than the range frequency, the relations are reversed and the average beat frequency is proportional to the range-rate.

To ensure the condition of range frequency being greater than the doppler frequency over the complete set of range and range-rate of interest, the following inequality must hold

$$4\Delta f f_{m} R_{min} > v_{max} f_{o}$$
 (5)

where f_m is the repetition frequency (977 Hz), R_{min} is the minimum range of interest (10 m), v_{max} is the maximum range-rate of interest (60 m/s), and f_o is the carrier frequency (17.5 GHz).

For the given parameters,

$$\Delta f > 27 \text{ MHz}$$
 (6)

Equation (6) imposes one condition on the frequency deviation.

Another restriction arises from the spectral nature of the signal. Since the modulation is periodic in the repetition frequency, \mathbf{f}_{m} , the transmitted signal can be represented as a Fourier series, with period $1/\mathbf{f}_{\mathrm{m}}$. The maximum signal strength occurs at \mathbf{f}_{m} and decreases as the harmonic number increases. Unless filtering is included in the receiver, the receiver will be saturated by strong signal terms at \mathbf{f}_{m} and the first two or three harmonics of \mathbf{f}_{m} . To

simplify the filter problem, the IF frequency, f_B , should be much greater than f_m . Since f_B is proportional to Δf , a large value of Δf is desirable. For example, the minimum value of f_B that the receiver must pass is given by a target at the minimum range, traveling at the maximum velocity. Assuming a maximum velocity of 60 m/s at a range of 10 m and a frequency deviation of 27 MHz, the minimum IF frequency is 3.3 kHz; too close to 3 f_m . A value of 50 MHz for Δf increases the minimum IF frequency to 6.2 kHz. This was considered a reasonable tradeoff between filter requirements and modulator complexity.

3. Range and Range-Rate Accuracy

Implicit in the derivation of equation (2) is the assumption that the modulating signal is a symmetric triangular wave. When the symmetry or the linearity of the triangular wave is perturbed, an error in range and range-rate will occur. To determine these errors, we use the more general equation relating the IF frequency, f_R , to modulation [6]

$$2\pi f_{R} = \Psi \tau + \Psi \dot{\tau} \tag{7}$$

where

$$\Psi(t) = 2\pi \left\{ f_0 t + \Delta f \int_0^t g(x) dx \right\}$$

$$\tau = \frac{2R}{c}$$
(8)

and $\Delta fg(x) = frequency modulation$

In the ideal case,

$$g(x) = 4f_{m}x \tag{9}$$

From equations (7) and (8)

$$f_{R} = \pm 2\Delta f_{g}(t) \frac{R}{c} + (f_{Q} \pm \Delta f_{g}(x)) \frac{2\dot{R}}{c}$$
 (10)

Neglecting second-order terms,

$$f_{B} = \pm \frac{2\Delta f \dot{g}(t)R}{c} + \frac{2\dot{R}f}{c}$$
(11)

As before, the first term is the range frequency and the second term the doppler frequency.

Equation (11) will be used to evaluate the error when the frequency modulation, $\Delta f \dot{g}(t)$, is not ideal.

When there is an asymmetry in the half-periods of the triangular modulation as shown in Figure 4, $\dot{g}(t)$ will differ on the upsweep and downsweep of the modulation cycle. Therefore, a stationary target will exhibit a range-rate from equation (4). From Figure 4 the half-period during the upsweep T_{11} , is

$$T_{u} = \frac{T}{2} - \delta T \tag{12a}$$

and the half-period during the downsweep, \mathbf{T}_d , is

$$T_{d} = \frac{T}{2} + \delta T \tag{12b}$$

Using equations (12a) and (12b) to calculate $\dot{g}(t)$

$$f_{up} \simeq \frac{8\Delta f f_{m}R}{c} \left(1 + \frac{2\delta T}{T}\right)$$

$$f_{down} \simeq \frac{8\Delta f f_{m}R}{c} \left(1 - \frac{2\delta T}{T}\right)$$
(13)

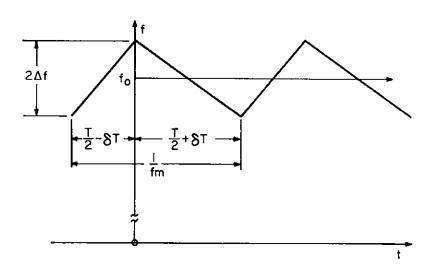


FIGURE 4. ASYMMETRIC TRIANGULAR MODULATION.

From equations (4) and (13), the range error is zero and the apparent doppler frequency, δf_d , is

$$\delta f_{d} = 2 f_{r} \frac{\delta T}{T}$$
 (14)

$$f_{\mathbf{d}} = \frac{2 Rf_{\mathbf{0}}}{c} \tag{15}$$

The apparent range-rate, δR, is

$$oR = \frac{f_r c \delta T}{f_o T}$$
 (16)

For the present modulation parameters and center frequency

$$\delta \dot{R} = 22.33 R \frac{\delta T}{T} m/s$$
 (17)

From equation (17), a 1% modulation asymmetry will cause an apparent range-rate of 6.7 m/s at 30 m. To eliminate this source of error, the repetition rate (and hence symmetry) is derived from the 2-MHz crystal of the microprocessor.

The effect of a nonlinear triangular wave can be derived from the model shown in Figure 5(a). From Figure 5(a), the RF frequency, f(t), is

$$f(t) = f_0 + 4\Delta f f_m t + \varepsilon(t)$$
 (18)

where $\varepsilon(t)$ is the time-dependent nonlinearity

Assuming the target to be stationary,

$$-\frac{T}{2} \le t \le 0$$

$$f_{B} = f_{r} + \frac{2 \dot{\epsilon}(t) R}{c}$$
 (19a)

$$0 \le t \le \frac{T}{2}$$

$$f_{B} = -f_{r} + \frac{1 \hat{\epsilon}(t) R}{c}$$
 (19b)

When f(t) has the form shown in Figure 5(a), the decomposition into $\epsilon(t)$ and $f_0(t)$ is shown in Figures 5(b) and 5(c), respectively. $f_0(t)$ is the ideal

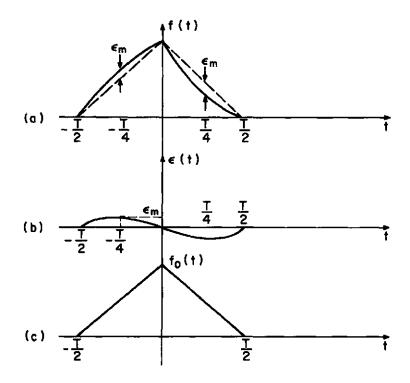


FIGURE 5. SINGLE CYCLE OF NONLINEAR MODULATION WAVEFORM.

linear waveform. If we assume $\epsilon(t)$ to be quadratic about T/4, $\epsilon(t)$ can be written as

$$-\frac{T}{2} \le t \le 0$$

$$\varepsilon(t) = \varepsilon_{m} - \varepsilon_{m} (\frac{4}{T})^{2} (t + \frac{T}{4})^{2}$$
(20a)

$$0 \le t \le \frac{T}{2}$$

$$\varepsilon(t) = -\varepsilon_{\rm m} + \varepsilon_{\rm m} (\frac{4}{T})^2 \left(t - \frac{T}{4}\right)^2 \tag{20b}$$

From equations (20a) and (20b)

-
$$\frac{T}{2} \le t \le 0$$

$$\dot{\varepsilon}(t) = -2\varepsilon_{\rm m}(\frac{4}{T})^2 \left(t + \frac{T}{4}\right) \tag{21a}$$

$$0 \le t \le \frac{T}{2}$$

$$\dot{\varepsilon}(t) = 2\varepsilon_{m} \left(\frac{4}{T}\right)^{2} \left(t - \frac{T}{4}\right)$$
(21b)

Substituting equation (21a) into equation (19a) and equation (21b) into equation (19b), we have

$$-\frac{T}{2} \le t \le 0$$

$$f_{B} = f_{r} - 4\varepsilon_{m} (\frac{4}{T})^{2} \left(t + \frac{T}{4}\right) \frac{R}{c}$$

$$0 \le t \le \frac{T}{2}$$

$$f_{B} = -f_{r} + 4\varepsilon_{m} (\frac{4}{T})^{2} \left(t - \frac{T}{4}\right) \frac{R}{c}$$

Assuming $\boldsymbol{\epsilon}_{m}$ to be small so that \boldsymbol{f}_{r} is the dominant term

$$f_{up} = f_r - 16\varepsilon_m f_m \frac{R}{c} - 64\varepsilon_m f_m^2 \frac{R}{c} t \qquad -\frac{T}{2} \le t \le 0$$

$$f_{down} = -f_r - 16\varepsilon_m f_m \frac{R}{c} - 64\varepsilon_m f_m^2 \frac{R}{c} t \qquad 0 \le t \le \frac{T}{2}$$
(22)

Figure 6 is a plot of equation (22). From the figure it is seen that the IF frequency is frequency modulated. The modulating function is a sawtooth of amplitude $\pm \frac{16\epsilon_m}{c} \frac{f_m}{c} \frac{R}{c}$ about f_r . From the stationary phase one would expect the IF frequency spectrum to be uniform about f_r and extending $\pm \frac{16\epsilon_m}{c} \frac{f_m}{c} \frac{R}{c}$ cycles on either side.

If we let $\frac{\varepsilon_{m}}{2\Delta f}$ be a measure of the nonlinearity, then

$$\frac{16\varepsilon_{\rm m} f_{\rm m} R}{c} = \frac{16\varepsilon_{\rm m}}{2\Delta f} (2\Delta f) f_{\rm m} \frac{R}{c}$$

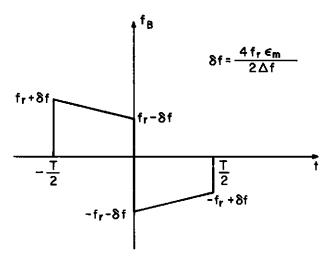


FIGURE 6. SINGLE CYCLE OF DISTORTED IF FREQUENCY.

or
$$\frac{16\varepsilon_{\text{m}} f_{\text{m}} R}{c} = 4f_{\text{r}} \frac{\varepsilon_{\text{m}}}{2\Delta f}$$
 (23)

From equation (23), we see that a 1% nonlinearity will lead to a ±4% frequency spread. This has the net result of causing the IF response to appear noisy and difficult to process. Since the IF frequency is frequency modulated, the frequency between successive cycles will vary. If the variation is great enough, the measurement will be rejected by the signal processor. To avoid these problems a modulator with high linearity is used in conjunction with a linearized voltage-controlled oscillator.

4. Antenna Design and Measurement

From our road test experience with the X-band antenna design from Phase II, improvements in beam definition were considered definitely desirable. The new design goals for beamwidth in azimuth and elevation were set at 3 and 5 degrees, respectively. This appeared to be the best compromise between avoiding interference from adjacent traffic lanes and not becoming so sensitive to beam alignment that slight steering angle corrections would lead to a temporary loss of target.

In addition, the new design was required to have lower side-lobe levels than the original X-band design, since large targets off to the side could otherwise still be detected. A uniformly illuminated rectangular aperture ideally has side-lobe levels of only -13 dB with respect to the main lobe [7]. To further reduce the side-lobe level, a predetermined current distribution

^{7.} S. Silver, Microwave Antenna Theory and Design, Rad. Lab Series, Vol. 12, Boston Tech. Publications, 1964.

was established over the antenna aperture, consistent with the side-lobe level desired. A -30 dB Dolph-Chebyshev distribution was chosen for the azimuth pattern and -20 dB for the elevation pattern.

The new Ku-band antenna, shown in Figure 7, uses a construction similar to the original X-band design. The antenna consists of 512 fan-shaped dipoles printed together with the feed structure on both sides of a Duroid circuit board. A ground plane is located $\lambda/4$ behind the printed board as a reflector. This arrangement provides a high-gain antenna in compact form (33 x 19 x 2 cm). Two identical printed circuit antennas, one for transmit and one for receive located next to each other, were used for the Ku-band bistatic radar.

Pattern measurements on the new antennas were performed in a special anechoic chamber. The azimuth and elevation patterns are shown in Figures 8 and 9, respectively. The measured side-lobe levels close to the main lobe were -22 dB in azimuth and -18 dB in elevation. These lower than theoretical levels are probably due mainly to the perturbing effects of the feed structure which is in the same plane as the radiating dipoles. The resulting side lobes are, however, much lower than for the previously used antenna with uniform excitation and should be adequate for the intended purpose.

The measured antenna beamwidth is close to the 3-degree azimuth and 5-degree elevation objective values. The gain is 30 dB above that of an isotropic radiator. For the 19 x 11 wavelength aperture, this represents an efficiency of 50%. Since a nonuniform current distribution is not as efficient as a uniform current distribution, 50% is a reasonable efficiency. By way of comparison, a parabolic reflector is also about 50% efficient.

5. Coverage Pattern Measurements

A coverage pattern of the radar is a series of equipower contours in the plane containing the radar and the target. A 10-m² corner reflector was used as target, mounted at the same height from the ground as the radar. Neglecting multipath effects for this position of the target, only the azimuth variation of the target and radar affects the power contours. Moreover, since the corner reflector is much less sensitive to azimuth changes than the antennas in the radar, the entire variation can be attributed to the radar. This allows a simpler mathematical model to be used, as discussed in Appendix A, where computer results are presented. A typical radar-target configuration is shown in Figure 10. The transmit and receive antennas are designated by their normals,

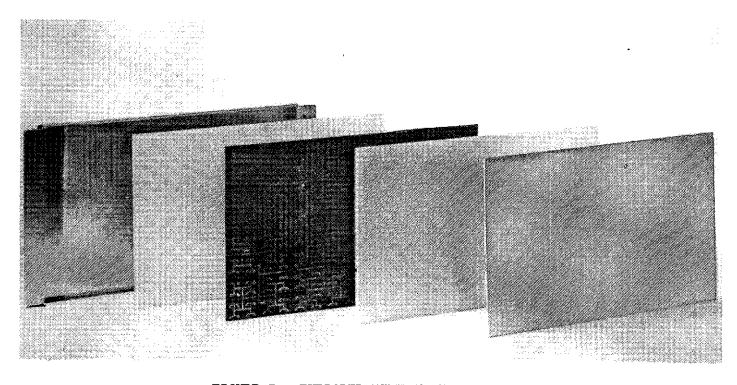


FIGURE 7. EXPLODED VIEW OF ANTENNA.

,

*

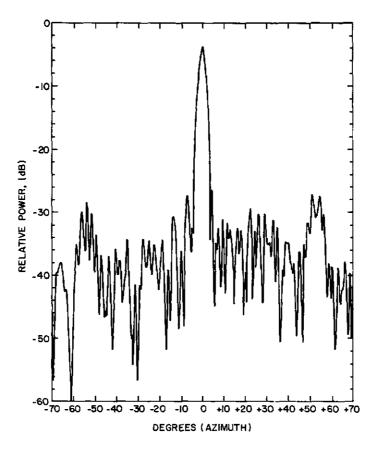


FIGURE 8. AZIMUTH Ku-BAND PATTERN.

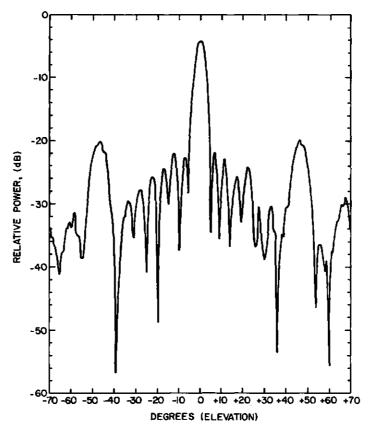


FIGURE 9. ELEVATION Ku-BAND PATTERN.

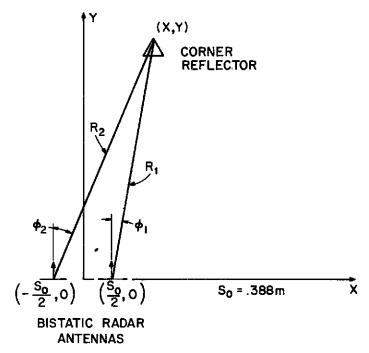


FIGURE 10. TYPICAL RADAR-TARGET CONFIGURATION FOR COVERAGE PATTERN MEASUREMENTS.

which are shown on the x axis at $\pm s_0/2$. The target is designated by the coordinates of the apex of the reflector. For a fixed separation, s_0 , the geometry is completely defined by the coordinates of the corner reflector.

The determination of the equipower contours was made on a premarked range. Range markings consisted of parallel lines spaced 25 cm apart for the first ± 1 m from the center line (x = 0) and 50 cm apart for x = ± 1 m to x = ± 2.5 m. Because of the narrow antenna beam the range markings were finer for the first ± 1 m. A spectrum analyzer was used as the readout device for the radar return. The analyzer has a wide dynamic range and can measure low-level signals, thus making it a natural candidate for this type of measurement.

Figure 11 shows a contour plot, where the radar return was monitored at the output of the preamplifier, shown in Figure 2. To confine the return to approximately 30 m as needed for CMS operation, a shaped postamplifier was designed with the aid of the computer program discussed in Appendix A. Figure 12 shows the power contour at the output of the shaped postamplifier. An inspection of Figure 12 shows that when the threshold level of detection is set for 30 m, the maximum coverage is within -1.0 m and +0.5 m off axis, a sharply defined microwave beam.

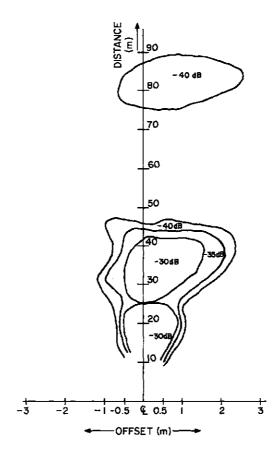


FIGURE 11. COVERAGE PATTERN Ku-BAND RADAR - OUTPUT OF PREAMPLIFIER.

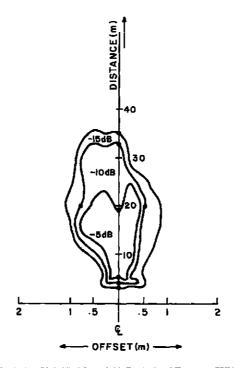


FIGURE 12. COVERAGE PATTERN Ku-BAND RADAR - OUTPUT OF POSTAMPLIFIER.

6. IF Amplifier Shaping for CMS

Two amplifiers are used between the radar receiver and the microprocessor. They are referred to as a preamplifier and a postamplifier. The combination of these amplifiers has three functions:

- (1) To amplify the return signal (f_R) ,
- (2) To minimize unwanted signals, and
- (3) To limit the amplitude of the return signal.

A two-stage preamplifier and a five-stage postamplifier were designed for this purpose. They both use the CA3401 operational amplifier chip as the basic building block.

The preamplifier, located at the mixer output, consists of two stages. Its transfer characteristic is shown in Figure 13. The slope at the low-frequency end of the band is approximately 15 dB/octave, while in the operating band it is 5 dB/octave. The 15 dB/octave is intended to limit low-frequency noise and pickup of the harmonics of the modulating signal at 977 Hz. The 5 dB/octave helps compensate for the 12 dB/octave dropoff of the return signal. The high-frequency end is rolled off slightly to minimize unwanted signals beyond the desired range.

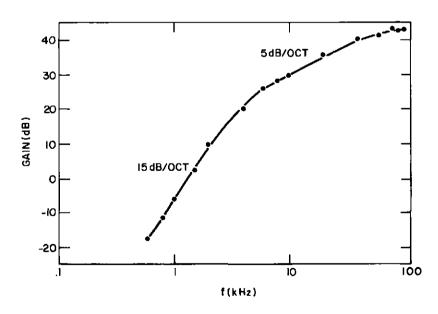


FIGURE 13. TRANSFER CHARACTERISTIC OF Ku-BAND PREAMPLIFIER.

The postamplifier designed for the CMS application has a transfer characteristic as shown in Figure 14. This amplifier consists of five stages. The

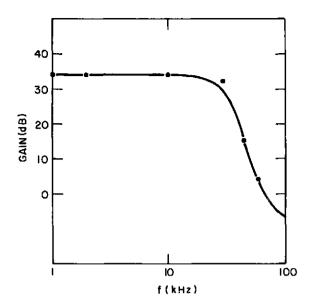


FIGURE 14. TRANSFER CHARACTERISTIC OF CMS POSTAMPLIFIER.

multiple stages are required to sharpen the roll-off at the high-frequency end of the passband to approximately 28 dB/octave. This roll-off minimizes spurious signals from beyond the range of interest.

The composite of the two sections, preamplifier and postamplifier, is shown in Figure 15. This composite band shaping gives us the required characteristics for operation out to a range of approximately 30 m.

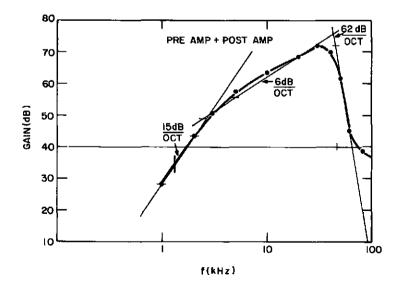


FIGURE 15. COMPOSITE OF PREAMPLIFIER AND POSTAMPLIFIER.

B. DUAL-MODE X-BAND RADAR

1. Block Diagram

As part of this program, the operation of a cooperative radar was to be investigated and compared to the noncooperative radar. Cooperative means targets are identified by a special tag that affects the reflected RF energy in a unique way. The original cooperative radar system [8] demonstrated by RCA in 1973 used frequency doubling in the tag to differentiate the target return from regular backscattering clutter. In a more recent version of the cooperative principle [9], the tag provides phase modulation of the reflected signal.

Two of the major advantages of the cooperative system are the practical elimination of false alarms (only targets provided with a tag are being recognized by the radar) and an accurate, nonambiguous location capability of the target (the tag provides a clean single point of reflection). These characteristics appeared to be especially desirable for the development effort on the headway-control algorithm. Using a cooperative radar at least in the initial development phases has the advantage of eliminating a larger number of possible problem areas and permitting concentration on the actual algorithm development. In this way, the cooperative system would be exposed to a large variety of traffic conditions and its behavior could be conveniently evaluated and optimized. We, therefore, proceeded to modify the existing X-band monostatic radar for cooperative operation using the phase modulated tag principle. A second, higher frequency IF channel was added to the X-band radar to handle the modulated signal. The original baseband response remained unaltered to permit noncooperative operation also. A switch selects the desired mode.

With the cooperative system, alarms are only triggered by 'tagged' targets, so that false alarms due to road signs, bridges, guard rails, or generally any reflecting object in the radar beam are eliminated. Thus the useful warning range can be extended. Also since the radar cross section of the tag is constant, there is no problem with fluctuating returns and the dynamic range is

^{8.} J. Shefer et al., "A New Kind of Radar For Collision Avoidance," SAE Automotive Engineering Congress and Exposition, Detroit, Michigan, February 26, 1974.

^{9.} G. S. Kaplan and F. Sterzer, "Dual-Mode Automobile Collision Avoidance Radar," SAE Automotive Engineering Congress and Exposition, Detroit, Michigan, February 24-28, 1975.

reduced. A tag on a compact car will return as much signal as a tag on a truck. This feature was particularly attractive during the headway-control development. Because of the complex return from a target when a problem arose, it was not clear if the headway-control algorithm was at fault or if the signal had dropped out. With the tag this variable was eliminated. From a long-range view-point, the possibility of encoding other messages also exists. The license number of the car as well as emergency messages could be transmitted from the car via the tag [9].

Potential false-alarm situations which cannot be eliminated with the cooperative radar occur when the tagged vehicle is in the line of sight but is not a collision threat. A car in the adjacent lane rounding a curve is an often-cited example.

A block diagram of the dual-mode radar, including the tag, is shown in Figure 16. The tag consists of an antenna identical to the one used in the radar, terminated in a reflective modulator. The modulator is an inexpensive, low-drain varactor modulator which encodes a 0- to 180-degree phase sequence on the signal received from the radar. This phase-coded signal is reradiated back to the radar where it is preprocessed in the cooperative channel. The resulting baseband signal is processed further in the common processor. The modulation rate of 500 kHz was chosen so that T^2L logic could still be used. Ideally, a large separation between the modulation frequency and the highest expected baseband frequency is desired to eliminate false alarms from massive targets at far distances and to maintain signal fidelity of the modulated wave.

After the phase-coded signal is received by the radar, it is translated to IF via the homodyne mixer. The IF which is at the modulation frequency (500 kHz) is filtered through a bandpass filter. The bandwidth of the filter is twice the baseband frequency. The bandpass filter prevents the target's baseband signal from getting through the cooperative channel and removes harmonics of the modulation frequency. After filtering, the signal is amplified and envelope detected. Figure 17(a) shows the waveshape at the output of the mixer, and Figure 17(b) shows the waveshape at the output of the envelope detector. As seen from Figure 17(b), the output of the envelope detector is at twice the baseband frequency. A low-pass filter at the output of the envelope detector removes the high-frequency components and further conditions the detector output. A shaped postamplifier completes the preprocessing of the cooperative channel.

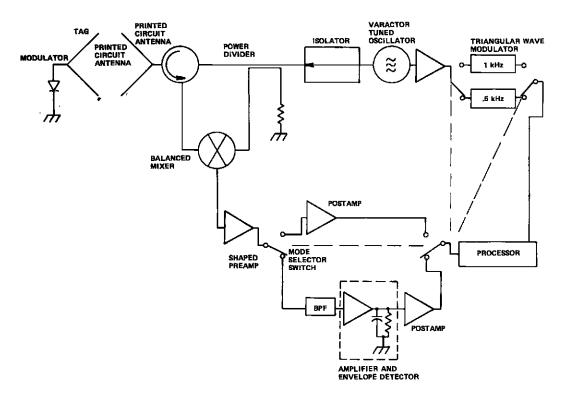
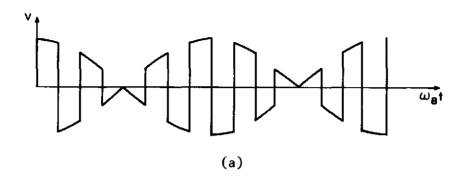


FIGURE 16. BLOCK DIAGRAM OF DUAL-MODE RADAR.

Earlier, it was mentioned that the output of the envelope detector is at twice the baseband frequency. Since it is desirable to use the same signal processor when the cooperative mode is selected, the frequency modulation repetition rate is reduced by a factor of two to 500 Hz to keep the final baseband frequency the same. When the mode of operation is selected by the switch, the modulation rate and the flow path are selected simultaneously.

2. System Parameter Selection

The cooperative channel of the dual-mode radar shares the RF front end with the noncooperative channel and, therefore, the modulation parameters with the exception of the repetition frequency, f_m . Because phase modulation doubles the baseband frequency (see Figure 17), f_m is reduced from 1 kHz to 500 Hz to keep the baseband constant. This permits the use of a single processor for the dual-mode radar. The frequency deviation Δf for the X-band radar remains at 25 MHz.



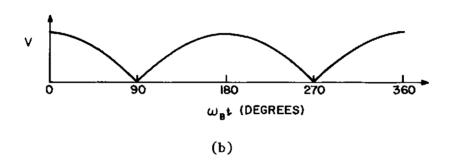


FIGURE 17. (a) TYPICAL IF VOLTAGE WAVEFORM FOR 0- to 180-DEGREE PHASE MODULATOR. (b) OUTPUT OF ENVELOPE DETECTOR.

A key parameter of the cooperative channel is the modulation rate, $\mathbf{f}_{\mathrm{T}}.$ The reflected radar signal when phase modulated from 0 to 180 degrees can be represented as

$$\cos(\Psi(t) + \pi S'(t)) \tag{24}$$

where $\Psi(t) = 2\pi \{f_0't + \Delta f_0 \int^t g(x) dx\}$

and S'(t) = 0 or 1 at the modulation rate

but $cos(\Psi(t) + \pi S'(t)) = cos\Psi(t) cos\pi S'(t)$

and $\cos \pi S^{\dagger}(t) = S(t)$

where S(t) = 1 or -1 at the modulation rate.

therefore,
$$cos(\Psi(t) + \pi S'(t)) = S(t) cos\Psi(t)$$
 (25)

When the modulated signal is translated to IF via a product mixer, the IF can be written as

$$u_{IF} = S(t) \cos[\Psi(t+\tau) - \Psi(t)]$$
 (26)

because
$$\Psi(t+\tau) - \Psi(t) = \dot{\Psi}\tau$$

the IF response, $\mathbf{u}_{\mathbf{IF}}$, becomes

$$u_{TF} = S(t) \cos \dot{\Psi} \tau \tag{27}$$

When the modulation rate f_T is much greater than the range frequency, $\Psi \tau$, equation (27) is the equation of an amplitude-modulated wave. That is, the square wave of amplitude 1 and -1 is amplitude modulated by the slowly varying baseband function $\cos \dot{\Psi} \tau$. Another point of view is that the cosine function is sampled by the square wave and must be at least twice the frequency of the cosine wave. For a range frequency, $\Psi \tau$ per meter of 333 Hz/m corresponding to $\Delta f = 25$ MHz and $f_m = 500$ Hz, the range frequency, f_r , at 100 m = 33.34 kHz. A tag modulation frequency of 500 kHz is 15 times larger than the maximum range frequency and thus is adequate.

In order to remove the baseband envelope, $\cos\mathring{\Psi}\tau$, from the high-frequency carrier, S(t), we make use of the fact that S(t) is periodic at the modulation rate, f_T , and can be represented as a Fourier series. Therefore, u_{IF} can be written as

$$u_{\text{IF}} = \cos \dot{\Psi} \tau \sum_{\kappa=0}^{\infty} A_{\kappa} \cos[2\pi(2\kappa+1) f_{\text{T}} t - \phi_{\kappa}] \qquad (28)$$

$$u_{\text{IF}} = \frac{1}{2} \sum_{\kappa=0}^{\infty} A_{\kappa} \cos[2\pi(2\kappa+1) f_{\text{T}} t + \dot{\Psi} \tau - \phi_{\kappa}] + \frac{1}{2} \sum_{\kappa=0}^{\infty} A_{\kappa}$$

$$\cos\left[2\pi(2\kappa+1) f_{T}t^{-\dot{\psi}}\tau^{-\dot{\phi}}\right] \tag{29}$$

where
$$A_{K} = \frac{4}{(2\kappa+1)\pi}$$
 (30)

From equation (29) we see that each Fourier component is DSB modulated by $\cos\dot{\Psi}\tau$. The bandwidth around each line of the spectrum is $\pm\frac{\Psi\tau}{2\pi}$. To prevent spectral overlap

$$f_{T} > \frac{\ddot{\Psi}_{\tau}}{2\pi} \tag{31}$$

Equation (31) is less restrictive than the condition derived earlier from sampling considerations. When \mathbf{u}_{IF} is passed through a bandpass filter centered at \mathbf{f}_{T} (500 kHz), the result is a DSB-modulated signal centered at 500 kHz.

The bandwidth of the filter must be wide enough to accommodate the highest frequency of $\dot{\Psi}\tau$ or 70 kHz, and selective enough to remove the baseband response at the third harmonic. A three-section Butterworth filter, with a 3-dB bandwidth of 180 kHz was found to be adequate.

After filtering, an envelope detector is required to strip the baseband signal from the carrier. To improve the detector efficiency, the signal is amplified before detection. The signal-to-noise ratio of a linear detector is better than the signal-to-noise ratio of a square law detector in the region of low signal-to-noise [4]. Figure 17(b) shows a sketch of the signal after envelope detection. Because of the 0- to 180-degree modulation, the waveshape corresponds to a full wave rectified sine wave.

To eliminate the harmonics associated with a full wave rectified sine wave, a low pass filter follows the detector. Since the second harmonic of the rectified sine wave is 14 dB below the fundamental [10], a single R-C filter was used. A shaped amplifier provides the final signal conditioning before range and range-rate are derived in the common dual-mode processing circuitry. The shaping is similar to that used for the baseband amplifier of the noncooperative channel, the basic difference being that the bandwidth is increased to accommodate the anticipated range of up to 100 m.

3. Coverage Pattern Measurements

Coverage pattern measurements similar to those described in subsection III.A.5 above were made for both channels of the dual-mode radar. The tagged channel can be seen in Figure 18 and the baseband channel in Figure 19. The targets consisted of an electronic tag, mounted at license plate height (0.385 m), as shown in Figure 20, and a 10-dB corner reflector mounted at the radar height for baseband tests. A photograph of the radar mounted on an RCA vehicle is shown in Figure 21. The height of the target affects the position of the multipath nulls. For example, using equation (1), the first multipath null for the tagged channel should occur at 18.4 m, whereas the baseband channel null should occur at 32.6 m. This is in good agreement with the measured results shown in Figures 18 and 19.

^{10.} A. G. Kandoian et al., Reference Data for Radio Engineers, International Telephone & Telegraph Corp., New York, 1964.

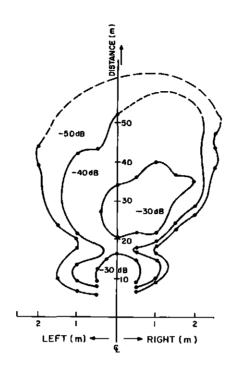


FIGURE 18. COOPERATIVE CHANNEL OF DUAL-MODE X-BAND RADAR.

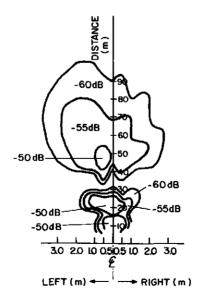


FIGURE 19. BASEBAND CHANNEL OF DUAL-MODE X-BAND RADAR.

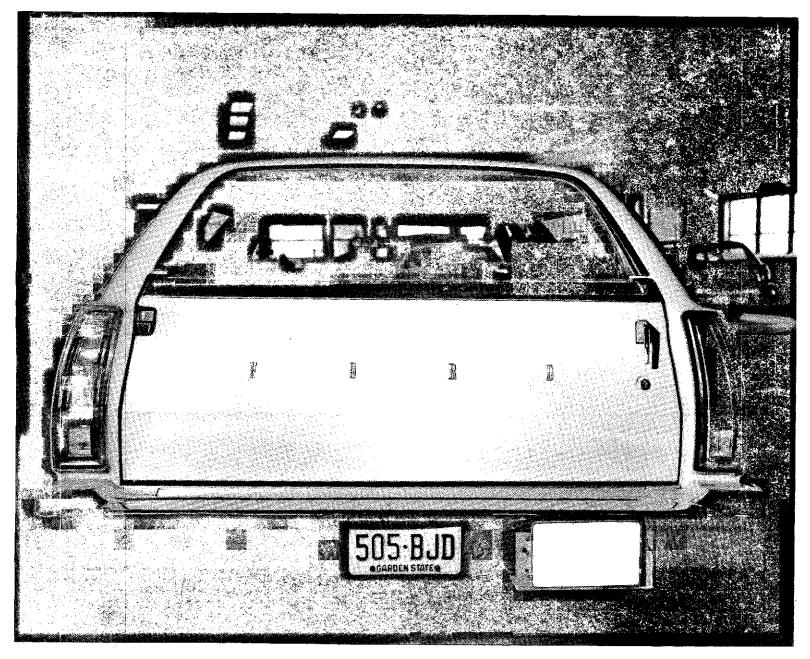


FIGURE 20. LOCATION OF MICROWAVE TAG MOUNTED ON VEHICLE.



FIGURE 21. X-BAND DUAL-MODE RADAR MOUNTED ON VEHICLE.

Although a complete one-to-one comparison between Figures 18 and 19 cannot be made due to the differences in amplifier gains and bandwidths between channels of the dual-mode radar (the tagged channel output was taken at the envelope detector and the preamplifier output was used for the baseband channel), it can be seen that the cooperative mode has no severe signal dropout and has a narrower coverage pattern out to 50 m. A theoretical treatment of coverage pattern is given in Appendix A which also indicates a narrower pattern for the tagged channel.

C. RADOME FOR RSV INSTALLATION

To evaluate the various radome structures, we constructed a fixture that supports the entire nose of the RSV, as well as different radome structures under test. This mount was attached to a pedestal in the microwave anechoic chamber located at RCA's facility in Moorestown, NJ. The chamber, mount, and nose structure are illustrated in Figure 22. The pedestal on which the structure is mounted can be rotated 360° for azimuth measurements. At the top of the pedestal, the head to which the fixture is attached can also be tilted 90° for elevation measurements. The antenna is at the center of rotation so that it remains bore-sighted with the transmitting antenna located at the far end of the chamber.

Antenna patterns were originally taken on an antenna without a radome to be used as a bench mark. These patterns were shown in Figures 8 and 9. At first, an attempt was made to beam directly through the existing structure; that is, the RIM (Reaction Injection Molded outer skin of the RSV) and an ABS plastic air scoop. Due to the different dielectric properties of the two materials directly in the radar beam, the side lobes are degraded as shown in Figures 23 and 24. This is particularly severe in elevation. As can be seen from the illustrations, one of the side lobes comes within 6 dB of the main lobe. This could result in false targets from overhead structures such as bridges and signs. There is also an additional 5-dB insertion loss due to the lossiness of the material. Since the radome loss affects both transmit and receive, a total sensitivity reduction of 10 dB results. We, therefore, decided to investigate the development and fabrication of a separate radome structure.

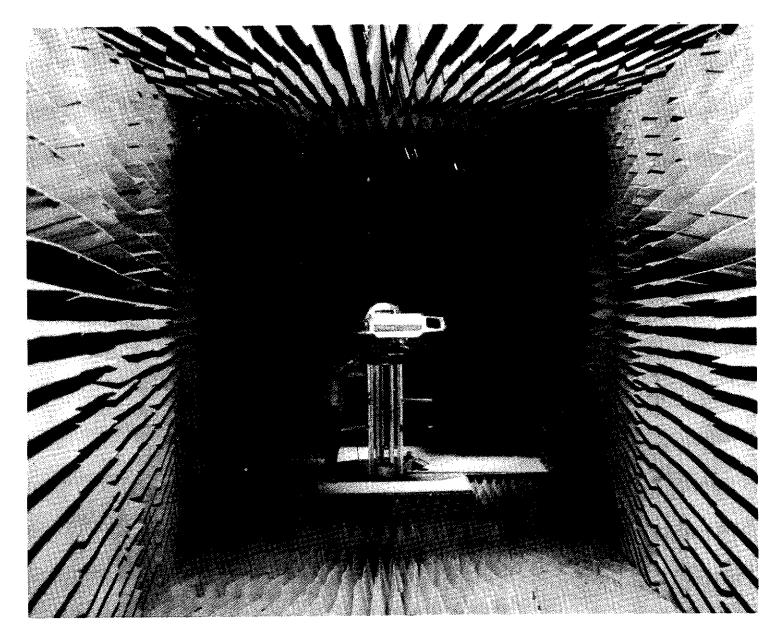


FIGURE 22. ANECHOIC CHAMBER FOR ANTENNA MEASUREMENTS.

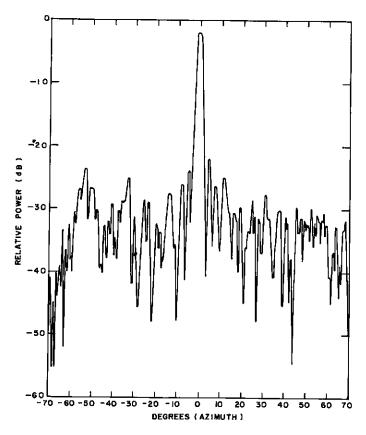


FIGURE 23. AZIMUTH ANTENNA PATTERN (NOSE AND AIR SCOOP).

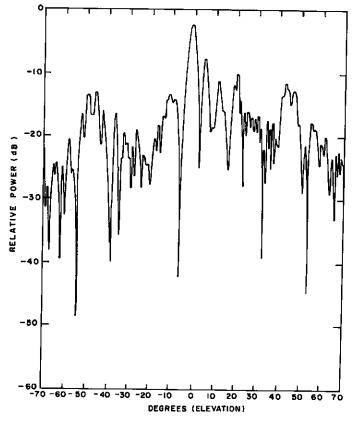


FIGURE 24. ELEVATION ANTENNA PATTERN (NOSE AND AIR SCOOP).

The radome has to conform to several requirements, such as:

- (1) It must have the same shape as the body of the vehicle;
- (2) It must have suitable electrical properties (low dielectric constant and low loss);
- (3) It must be environmentally sound (waterproof and fuel resistant).

Several materials were considered, as shown in Table 2, for this purpose. Early in the program, we approached Emerson & Cuming* to cast a block of low dielectric, low loss, closed cell foam in a mold provided by RCA. After considerable delay, they declined to quote on small production numbers, and they recommended the use of Eccofoam FPH foam-in-place. We were, however, not equipped for handling a structure of this size and complexity by ourselves.

TABLE 2. CHARACTERISTICS OF MATERIALS CONSIDERED FOR RADOME CONSTRUCTION

<u>Material</u>	Constant	Dielectric Loss Factor	Comment
Hardman Epoweld 3672	∿ 3	0.021	Hard/brittle
Foamed Polystyrene	1.03	0.0001	Light/porous
Polyethylene*	2.26	0.0031	Flexible/nonporous
Eccofoam FPH	1.04/1.25	0.001/0.005	Hard to handle
Eccoseal High-Q	2.55	<0.0004	Solvent attacks substrate
Eccocoat FP3	4.40	0.006	Too fluid/absorbed by substrate

^{*}The polyethylene used is expanded approximately 4:1, which reduces the dielectric constant and dissipation factor.

As the next best alternate to a solid block, we chose a laminated structure from standard blocks of foamed polystyrene, shaped to conform to the body contour, and sealed. The sealer is required to prevent moisture absorption into the foamed polystyrene which would deteriorate its electrical properties. Several sealers, listed in Table 2, were tested. The Eccoseal High-Q could not be used because its solvent dissolved the foamed polystyrene substrate.

^{*}Emerson & Cuming, Inc., Canton, MA.

The Eccocoat FP3 was better, but still too thin; it entered the cell structure of the foamed polystyrene, forming an irregular inner surface. The most promising coating was Hardman Epoweld 3672. A mock radome was constructed and tested. Electrically it was satisfactory, but, physically, the epoxy coating was too hard and shattered on minor impact.

The foamed polystyrene seemed the best building block because of its extremely low dielectric constant and dissipation factor. It still, however, required a suitable coating. A sheath of closed cell, cross linked, expanded polyethylene was finally selected as cover. This material does not absorb moisture and is highly resistant to automotive solvents as well as having acceptable electrical properties. A full scale radome was constructed, as shown in Figure 25.

The blocks of foamed polystyrene were shaped to conform to the contour of the RSV. The end and center supports are fastened to the antenna frame. The expanded polyethylene sheet is stretched over the foamed polystyrene and secured to the three solid polystyrene plates with plastic molding and nylon screws. The top and bottom edges are secured with aluminum battens. The natural gasket effect of the expanded polyethylene seals the edges while all other openings are sealed with RTV.

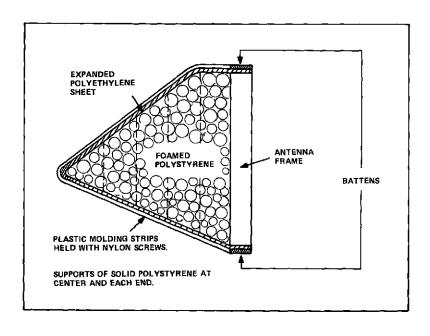


FIGURE 25. RADOME CONSTRUCTION.

The final structure was tested in the anechoic chamber with satisfactory results. Figures 26 and 27 show the resulting azimuth and elevation pattern. The side lobes in the worst case, elevation, are only 11 dB below the main lobe. This, however, occurs at an angle of 40° which is far removed from the general range of interest. The side lobes closer-in are at least 16 dB below the main lobe. There is also a loss of approximately 2 dB over an antenna without radome, but this is within acceptable limits.

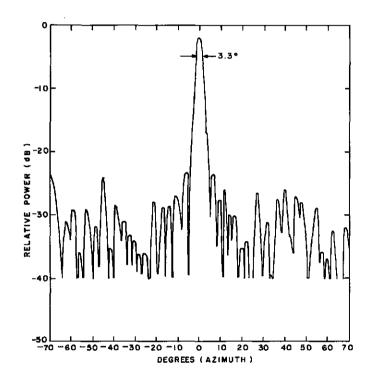


FIGURE 26. AZIMUTH ANTENNA PATTERN WITH RADOME.

The final configuration of the antenna and radome forms a separate unit, as shown in Figure 28, which fits into a cutout in the nose section of the RSV. A photograph of the RSV with the radar and radome inserted but before finishing off the joining areas is shown in Figure 29.

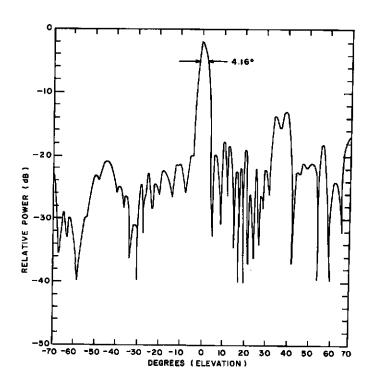


FIGURE 27. ELEVATION ANTENNA PATTERN WITH RADOME.

FIGURE 28. BISTATIC Ku-BAND RADAR WITH RADOME.



FIGURE 29. RSV WITH RADAR AND RADOME IN PLACE.

SECTION IV

PROCESSOR HARDWARE

A. RADAR CARDS FOR CMS AND HEADWAY CONTROL

1. Introduction

The radar card is hardware that converts the analog signal input from the radar system to useable data for the microprocessor. During Phase II and Phase III of the Minicars program, three versions of radar interface cards were constructed. Each of the three cards during the course of their respective programs had minor modifications, as the need arose, to improve performance.

The first radar card, used in Phase II, measured an accumulated count over a predetermined number of periods selected by software within the measurement interval. The square wave that was used to generate the triangular wave for the TEO and blanking at the radar card originated at the radar system. The blanking of the turnaround transient started at the beginning of each turnaround transient for a set time period (hardware-determined). The weakness of this radar card was that it needed eight consecutive modulation cycles with the same number of periods within the measurement interval in order to obtain one processed data output of range and range-rate.

The second radar interface card (Phase III) measured each period individually within the measurement interval. The greater the range from the target to the radar, the greater the number of periods within the measurement interval and, therefore, the greater the number of periods individually measured. The second card was designed to not only measure each period within the measurement interval, but also the periods up to the time of a dropout that may occur. This type of adaptive processing improved the range accuracy and reduced the number of rejected readings. The blanking arrangement for the second radar card was the same as the first radar card, except that the square wave was now derived from the microprocessor by dividing down the 2-MHz clock frequency. This card was used in the headway-control processor to provide range data with high accuracy but slow update rate.

The third card tailored for CMS operation had to provide range and rangerate in very short time intervals. Range-rate was derived directly from the doppler information. To improve the accuracy of the range-rate information, a symmetrical blanking pulse had to be used that overlapped the turnaround points of the triangular wave equally on both sides. The hardware of the card was simplified to accumulate a count through the measurement interval and up to any dropouts within the measurement intervals if they occurred.

The Phase III radar cards achieved increased responsiveness to all targets presented to the radar system. This increased system sensitivity placed the burden of false-alarm rejection in the case of the CMS system heavily on software.

2. Phase II Radar Card

A block diagram of the Phase II CMS radar card is shown in Figure 30. The radar provides a 1-kHz input and a sinusoidal signal input to the radar interface, f_B ; this is shown in Figure 31. The transitions of the 1-kHz square wave correspond to the turnaround points of the triangular modulation waveform. The positive transition of the 1-kHz square wave is the beginning of the positive-going slope of the triangular waveform. The negative-going transition of the square wave corresponds to the beginning of the negative slope of the triangular wave. The signal input into the interface contains both transients occurring at the turnaround points of the triangular waveform and sinusoidal waveforms generated on the upswing and the downswing of the modulation containing range and range-rate information. The greater the range, the larger the number of periods between the transients available for measurement will be. The amplitude of the input signal is a function of the multipath nulls, range, and type of target.

The 1-kHz input signal is applied to a network that generates a 20-µs pulse at each transition of the incoming square wave. The pulses are called the "reset" pulses. The reset pulses, in turn, are applied to a variable-period one-shot multivibrator which generates the blanking pulses. The blanking pulses occur at the transitions of the 1-kHz square wave which corresponds in time to the transient period from the turnaround.

The total signal input consisting of transient pulses and information-carrying sinusoidal waveforms is applied to the threshold circuit. The timing relationships between the triangular wave, blanking, and sinusoidal input from the radar are shown in Figure 32. The function of the threshold circuit is to shut off any input that falls below a preset value either initially or during the time of measurement between the transient pulses. If the input falls below the preset value at any time, the circuit shuts off and is reset by the reset

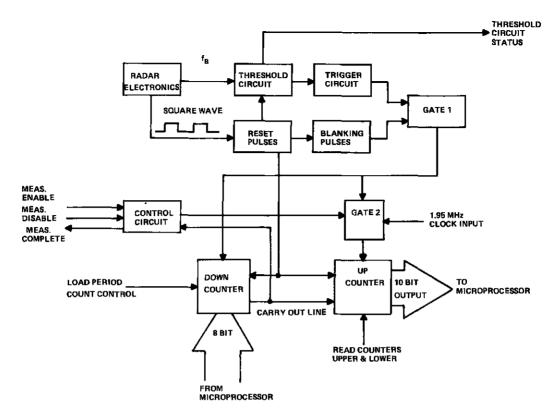


FIGURE 30. BLOCK DIAGRAM OF PHASE II CMS CARD.

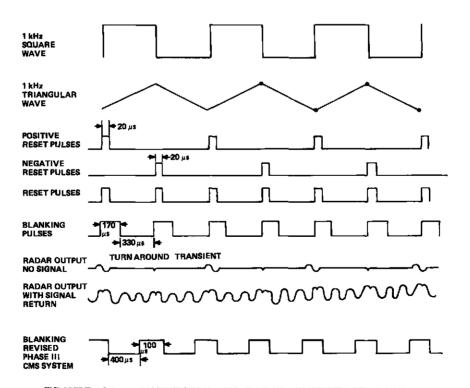


FIGURE 31. WAVEFORMS ON RADAR INTERFACE CARD.

pulse at the beginning of the next modulation cycle. The transient pulse is filtered out and the only pulses passing through to the counter are trigger pulses whose spacing is a function of range.

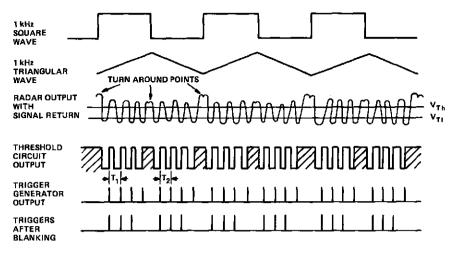


FIGURE 32. SIGNAL-PROCESSING TIME RELATIONS.

Two counters are used in the circuit, a "down" counter and an "up" counter. The down counter is loaded by the microprocessor with the number of periods that would be desirable to measure. When the down counter counts to "0," it generates a "carry out" pulse. The up counter is a high-speed counter which uses 1.95-MHz clock pulses as drivers. The counter is turned on by the first trigger pulse from the input signal and then turned off when the desired number of periods is measured. The reset pulses, which occur during the blanking time, are used to load the down counter with the number of periods to be measured and to reset the up counter to a zero count. Also available at the up counter transmission gate is information as to whether the threshold circuit shuts down during a measurement interval. The blanking pulse is also available at the up counter transmission gate to define the allowed measurement interval. The interface card runs asynchronously with the microprocessor. The control circuit allows the microprocessor to call for a measurement. A flag line is used to indicate that the measurement is complete. Another control line disables the "measurement ready" line.

One of the major problems associated with the use of this particular radar interface card was the possible loss of significant data during consecutive measurements. The Phase II CMS system measured either 1, 2, 3, 4, or 5 periods within a measurement interval. Eight full modulation cycles with the same "set" number of periods must be obtained for a successful measurement. However, during the actual radar measurement process, complex returns from the target cause dropouts during measurement intervals. The dropouts that occurred during the measurement interval would cause the system software to reject readings

until eight consecutive full modulation cycles could be read with the same set period count. This rejection of data during dropouts in the measurement interval makes the overall system seem insensitive to a variety of target situations that should be detected.

Two other problems were associated with the Phase II CMS system. First, selecting the proper period count to be measured within a measurement interval required auto-ranging software which required additional run time for the overall software. The second problem associated with the Phase II CMS system was that at the higher ranges, it is possible to have more than five periods within the measurement interval. An inherent one count error is usually averaged by dividing by the total number of periods; if the number of periods is limited to five, the one count error has a greater effect on the accuracy of the system since one count is a large percentage of the total period count.

3. Phase III Radar Card

A new radar interface card, shown in block diagram form in Figure 33, was constructed for Phase III. A square wave to provide the triangular wave modulation for the radar is generated by dividing down the 2-MHz clock frequency of the CPU to obtain 977 Hz. The square wave is passed on to the radar system, so that the triangular wave can be generated, and to the radar interface card. The 977-Hz square wave, 1 kHz nominal, is used to trigger blanking pulses and it is also used as a system reference for the software by means of the status latch. The blanking pulse output from the blanking pulse generator goes to a gate and the system status latch. If we refer to Figure 31 we see that the square-wave level appearing at the status latch during the blanking interval indicates whether the measurement is on the upswing or downswing of the measurement interval.

The beat frequency output, f_B , of the radar system after passing through the threshold circuit becomes a 5-V pulse train which contains range and range-rate and the turnaround phase discontinuity. A trigger generator generates narrow pulses at the positive transitions of each of the pulses coming from the threshold circuit. The blanking pulse is used to filter out unwanted data for approximately 170 μ s after the turnaround point.

A high-speed clock of 2 MHz from the microprocessor is used to drive a $12\text{-bit}\ T^2L$ counter. The triggers, corresponding to the positive transitions of the beat frequency, are passed to three locations in the radar interface card.

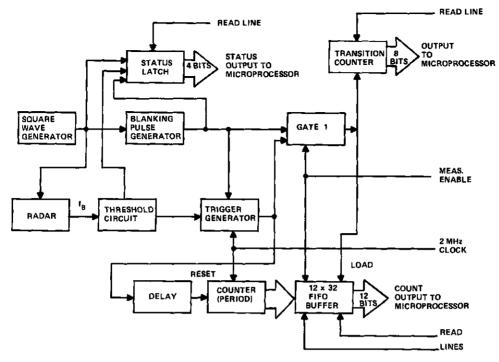


FIGURE 33. BLOCK DIAGRAM OF PHASE III CMS CARD.

When the measurement is enabled by software, the trigger output is passed through the "gate 1" circuit to the transition counter and the buffer. In addition, the first trigger pulse which corresponds to the first positive transition of the beat frequency is fed through a delay to the period counter. This trigger pulse is delayed always by two counts for the reset mode. The reset line initializes the high-speed counter to the count of two. Before the counter is reset, the data from the counter is read into a 12-bit wide x 32-bit deep first-in first-out buffer (FIFO). The measurement enable strobe which allows the measurement also resets the FIFO. The second positive transition of the beat frequency corresponds to the first period. The count corresponding to one period is loaded into the FIFO, and two clock periods later by virtue of a hardware delay, the high-speed clock is reset to a count of two. The two-count delay eliminates the one error usually associated with a high-speed clock measuring technique.

The number of periods in a measurement interval is stored in the FIFO. The square wave and blanking pulse relationship indicates either an up- or downswing of the triangular wave. A dropout that occurs during the measurement interval is noted by reading the threshold circuit condition from the status latch. Software can, therefore, select to accept readings up to the dropout since individual periods are measured and average the partial set of acquired data

in the measurement interval. The new Phase III CMS radar card can, therefore, measure up to 32 periods within a measurement interval. The card will also acquire and use the data up to a dropout in the measurement interval. This particular radar interface card was demonstrated and is used presently with the headway-control system.

4. Revised Phase III Radar Card

Early experiments had shown that the accuracy of the doppler information was not sufficient for proper CMS operation. The problem was traced to the asymmetrical blanking pulse. Since the tuning curve of the TEO in general is not perfectly linear, it is important to operate over the same tuning range of the TEO, both on the upswing of the triangular wave and on the downswing. Referring to Figures 31 and 32, we see that if the blanking starts at the turnaround point, an asymmetric tuning curve results. The beat frequency is read 170 µs after the beginning of the positive slope of the triangular wave up to the peak or turnaround point. Then, 170 µs later, the beat frequency is read back from the peak to the turnaround point or valley of the triangular wave. A nonlinearity of the TEO tuning curve under the described conditions causes only minor range measurement problems because the range readings average. However, an offset in doppler frequency will occur because of the nonlinearities creating a difference in frequencies of the periods on the upswing and downswing.

The revised Phase III radar interface card, which overcomes this difficulty, is shown in Figure 34. Once again, the square-wave generator divides down the 2-MHz microprocessor clock to obtain the 977-Hz square wave. A status latch is used to monitor the level of the square wave with respect to a blanking pulse which originates at the turnaround point. The blanking pulse generator also generates a blanking pulse that overlaps the turnaround points 50 μs on each side, as shown in Figure 31. The symmetrical blanking pulse causes the same part of the TEO tuning curve to be swept through on the upswing and downswing of the triangular wave. The status latch monitors the threshold condition line and a data out ready line from the FIFO. The threshold condition line goes high when the data drops below $V_{\mbox{\scriptsize Th}}$ (Figure 32) anytime during the measurement interval. The data out ready line indicates the FIFO has at least one set of useful data.

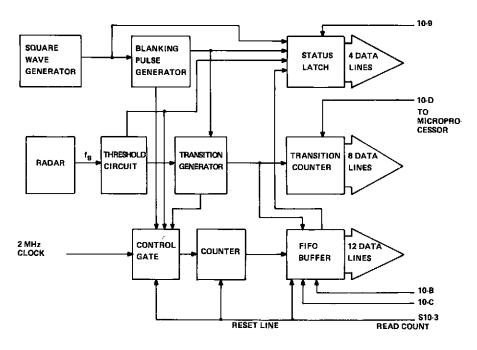


FIGURE 34. REVISED PHASE III CMS CARD.

In order to simplify the hardware, it was decided to accumulate a count across the entire measurement interval and divide out the inherent one count error by averaging the large number of periods. The output of the threshold circuit once again is used to generate narrow trigger pulses within the transition generator. The positive transitions of the beat frequency are counted by a transition counter. The first transition pulse or trigger after blanking turns on the high-speed counter. Each successive transition loads the accumulated count to that respective time in the FIFO. If a dropout occurs during the measurement interval, the count accumulated up to that point is used for the signal processing. The control gate that allows the counter to be initially started is disabled by the blanking pulse or the threshold circuit. A reset line is used to zero the counter initially and to enable the control gate. The data from the status lines, 4 bits, a nibble, is read by a IO-9 The 12-bit-wide FIFO is read twice. An 10-B pulse is used to read the lower eight bits. An IO-C pulse reads the upper four bits (nibble). The revised Phase III card is now used in the CMS algorithm.

5. Threshold Circuit

Figure 35 shows two versions of the threshold circuit used with the radar interface cards of the CMS and headway-control system. The threshold circuits

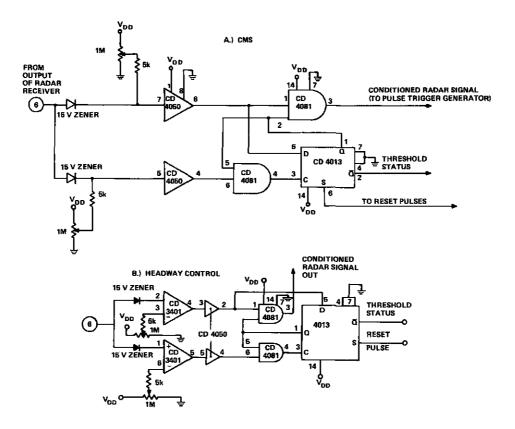


FIGURE 35. THRESHOLD DETECTION CIRCUITS.

differ from each other in the manner in which the analog input, f_B , is converted to a digital pulse train. The threshold circuit used with the CMS biases the inputs of two buffers to provide a low and high threshold value that must be exceeded for the circuit to perform properly. The threshold circuit used with the headway-control system uses two comparators instead of two digital buffers at the input. After passing through the buffers or comparators, both threshold circuits are the same. The two different input circuits were tried to determine if there were any operational differences between the standard comparator using an OP-AMP and reference voltage, and the voltage-biased digital buffer. At this point, no conclusive data indicates that one comparator circuit is better than the other.

Basically, the threshold circuit consists of two buffers or comparators, two AND gates, and a flip-flop. The input signal is split into two paths to their respective buffers or comparators. A diode in the series leg of each of the paths limits the bipolar signal to a positive-going signal only. (A negative-going signal greater than -0.75 V would cause the buffer to clamp a large signal at this level and create problems in setting threshold levels.)

The threshold level of each buffer with $V_{\rm dd}$ = 5 V is 2.5 V; therefore, a DC level is applied to each buffer or comparator to provide an upper- and lower-threshold level. The lower-threshold level setting has a significant voltage applied to the input so that a small signal of only a few tenths of a volt generates an output from the buffer or comparator. The upper-threshold level provides a low-level bias at the input of the second buffer or comparator and a large signal of the order of 2 V is required to generate an output from this stage. The circuit uses an AND gate to control the signal from the threshold circuit into the rest of the doubler circuit. The other AND gate controls the clocking of the flip-flop used to turn the circuit on or off.

Initially, the CD4013 flip-flop is set by the reset pulse of the radar interface. A high level appears at both AND gates, enabling both circuits. The low-level signal threshold generates a pulse out of the buffer or comparator which is used to clock the flip-flop. If the high-level threshold allows a pulse output from the buffer or comparator, then a pulse will be appearing at the "D" or data input to the flip-flop. Since the clock input is delayed by propagation time through the AND gate, the high-logic level at the "D" input corresponding to the signal will be present when the CD4013 is clocked. Clocking it with a high level keeps Q high and maintains the enabled state of both AND gates; therefore, the threshold circuit is "on."

If at any time the upper-level threshold is not exceeded while the lower-level threshold is generating a pulse from the buffer or comparator, the net result is a clock signal to the CD4013 which sees a zero at the "D" input, and, therefore, Q goes low, shutting off both AND gates. No signal is allowed to pass to the doubler, and additional clock pulses are not allowed to pass to the flip-flop. The Q output of the flip-flop goes high, signaling the micro-processor that the threshold circuit is shut down. The reset pulses of the radar interface are then needed to turn the threshold circuit on again.

B. CPU AND MEMORY

1. Introduction

During the initial stages of hardware and software development a flexible microcomputer system for prototyping purposes is required. The RCA COSMAC development system (CDS) has the necessary memory size required for a prototype system in the form of RAM space so that software can be easily loaded

from another storage area or host computer. To aid in this storage and rewriting function, some type of ROM chip continuing a "utility" routine is also included. The utility software enters and retrieves data from the RAM space and, if necessary, can be used to modify the data and then restore the data to any selected location or address.

During Phase II we used exclusively the COSMAC development system for prototyping both hardware and software. The CDS consisted of a card nest, control panel, and a basic set of plug-in modules. The card nest provided user space for the development of interface hardware between external hardware and the control processing unit (CPU) system. A large variety of interface cards was developed for the radar, display, and various sensors on the RSV. Two major problems were, however, noted for the CDS. The plug-in modules that formed the basic microcomputer system were interconnected at the backplane by a printed circuit (PC) structure that connected each card of the module to other modules within the card rack. The continuous insertion and removal of cards during the development period and vibrations from the test vehicle caused the printed circuit connections eventually to deteriorate and some open- and short-circuit conditions on the backplane of the CDS occurred. A second problem was the difficulty in using the system to debug the hardware. A hardware failure in an interface card usually caused one of the plug-in modules of the microcomputer system to fail.

During Phase III, therefore, we switched to the newly released RCA evaluation board, single PC card $(24 \times 36 \text{ cm})$ that contains all of the necessary components for prototyping. The evaluation board was finally replaced by another standard PC board that fit within the normal card cage to form a compact single-enclosure computing system.

2. Phase III Evaluation-Board System

The evaluation board uses an RCA CDP 1802 one-chip microprocessor with a 2-MHz crystal to provide the system clock frequency. Control chips are provided for resetting and starting either a previously loaded program in RAM space or the utility routine located on a ROM chip on the card. Additional chips are provided for addressing the 4K of RAM space on the board and for I/O decoding. Three transistors on the card provide a RS-232 interface which allows communication between the evaluation board, an "execuport" terminal, and the host computer system. A set of LEDs on the card provides a visual

indication of the data address status lines of the microcomputer system. The evaluation board with RAM and ROM operates from a single 5-V supply.

During Phase II, a large number of interface cards had been developed for the radar, display, and sensors of the RSV, using the COSMAC development system. To avoid redesigning the hardware of the interface cards, we designed another card that made the evaluation board look like the CDS to the existing interface hardware; this new card was called the CPU interface card. A card cage was constructed that would hold five standard 11.5 x 16.5 cm cards capable of mating with a 44-pin connector. A picture of the evaluation-board card cage system is shown in Figure 36. The card cage and evaluation board are powered by a single 5-V supply. Connections are made between the card cage via the CPU interface card and the evaluation board by two 16-lead flat ribbon connector cables which mate to standard DIP sockets. Also shown in the photograph is a self-scan display which was found useful for visual readout during testing and debugging.

A typical card cage assembly for CMS testing included the CPU interface card, the radar interface card, and a display interface card. The display was used during testing to indicate range and range-rate data. Early tests of the electronic dashboard display microcomputer also made use of the evaluation-board card cage system. For testing the dashboard display, the card cage assembly contained a CPU interface card, A/D-trip odometer card, clock-fuel economy-tachometer card, and the card which contained the display-binary switches and velocity interface. Both card cage systems were able to use a standard CPU interface card and the evaluation board. As mentioned above, the main purpose of the CPU interface card was to make the evaluation board look like the CDS with regard to I/O functions such as input and output data lines and input and output strobes.

Closer examination of the evaluation board later in the program indicated that the elimination of the circuitry for the utility ROM, two CD 1852 I/O ports, the LEDs with their associated drivers, and the three-transistor RS-232 interface would produce a compact design for a CPU card that could fit within the standard card cage. If the output lines from the CPU card were made the same as the output lines (ribbon cable) from the evaluation board, it would create a system that could be used for initial prototyping and then, with the addition of a CPU card, become a stand-alone microcomputer. This concept is illustrated in Figure 37. The CPU card, CPU interface card, and evaluation board are common to all card cage systems.

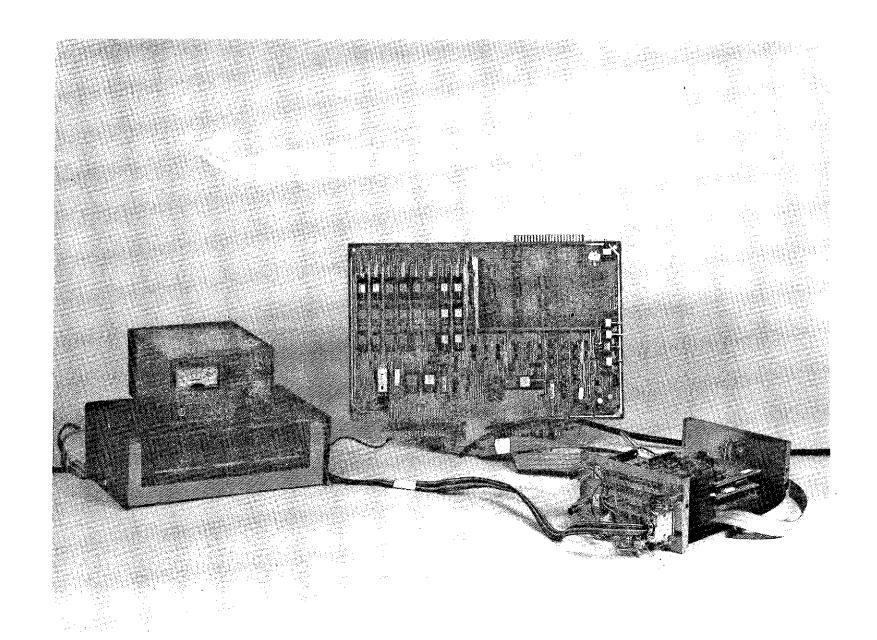


FIGURE 36. EVALUATION BOARD WITH CARD CAGE AND DISPLAY.

t t

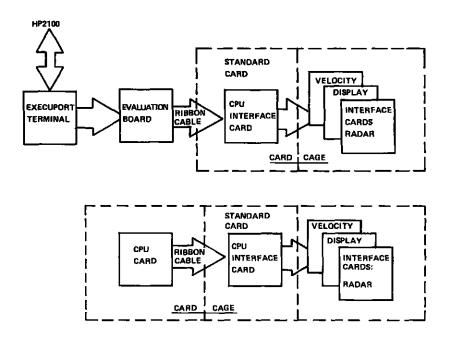


FIGURE 37. EVOLUTION FROM DEVELOPMENT BOARD TO FULL CARD CAGE SYSTEM.

CPU and Memory Card Cage for RSV Installation

A block diagram of the final CPU card is shown in Figure 38. The card consists of a CDP 1802 microprocessor with a 2-MHz crystal for the system clock. Two CDP 1822 RAM chips provide ½K of memory space for available storage. Either 2758 or 2716 EPROMs can be used with the CPU card. The 2758 is a 1K EPROM, and the 2716 is a 2K EPROM. From 1K to 8K of EPROM space is available on the CPU board. Both types of EPROMs are convenient to program and erase, and both operate from a single 5-V supply. An 1852 chip is used as an address latch and a 4555 chip is used for address decoding. A CD4028 is used for I/O decoding. A photograph of the CPU card is shown in Figure 39.

When the EPROM programming is complete, the CPU card, CPU interface card, and hardware interface cards form a stand-alone microcomputer system. A photograph of the complete CMS microcomputer system is shown in Figure 40. Another photograph, Figure 41, shows the CMS with the cover removed. Figure 42 gives a size comparison between the microcomputer system and the CDS. The CMS card cage contains two additional cards intended for the headway-control system in the RSV. The CMS card and headway-control card share the same CPU interface card by means of transmission gates at the connections between the CPU and CPU interface cards. An interrupt throttle controller card is backplane wired to the headway CPU card. A switch is used to select between either the CMS or headway-control system.

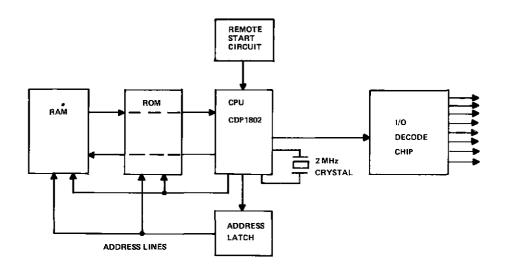


FIGURE 38. BLOCK DIAGRAM OF CPU CARD.

The electronic dashboard microcomputer is the same size as the CMS microcomputer. It consists of a CPU card, CPU interface card, and three additional cards which interface to the hardware and sensors of the RSV. Thus two card cages, each measuring approximately 9 cm x 15 cm x 26 cm contain all computer circuitry for CMS, headway control, and display functions.

4. Remote-Start Circuit for CPU

Both CPU cards contain a special start-up circuit to reset the CPU card and to start the software running at the proper location when the ignition is turned on. A low level on the $\overline{\text{WAIT}}$ line of the CDP 1802 microprocessor will reset all registers of the microprocessor and start the software running at location 00. The $\overline{\text{WAIT}}$ line has to be held low until the crystal oscillator stabilizes after turn on (approximately 50 ms).

Figure 43 shows the remote-start circuit of the CPU card. An R-C network is used as input to an inverter. The transient response when the power is applied to the circuit from t=0 is shown at different points (A, B, C, D) on the figure. The capacitor charges as a function of the R-C time constant. The inverter output B remains high until the charging capacitor exceeds the CMOS threshold level of the inverter. At t_1 , the inverter output at B goes low. Examination of diagram (B) shows that when the power is turned on a spike is generated that can be used for initializing hardware. This particular pulse is used to reset the CD4047 one-shot circuit so that \overline{Q} is high.

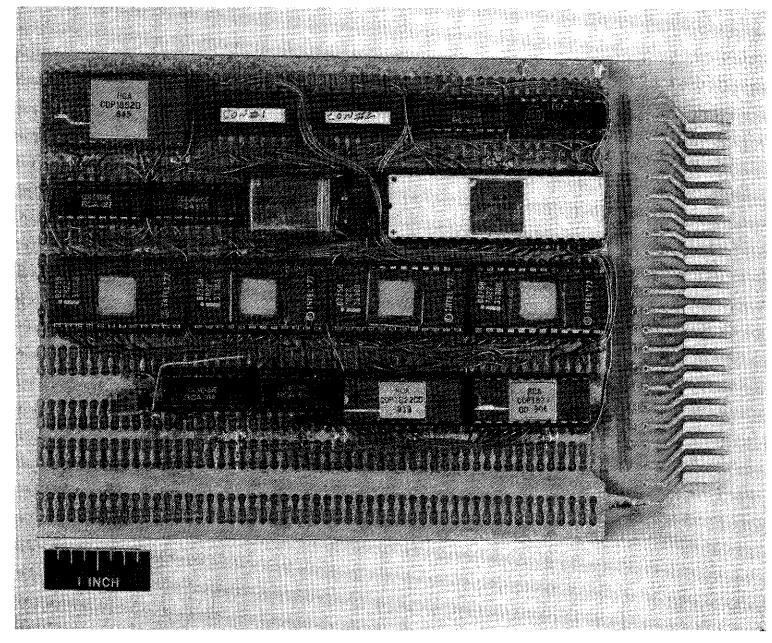


FIGURE 39. PHOTOGRAPH OF CPU CARD.

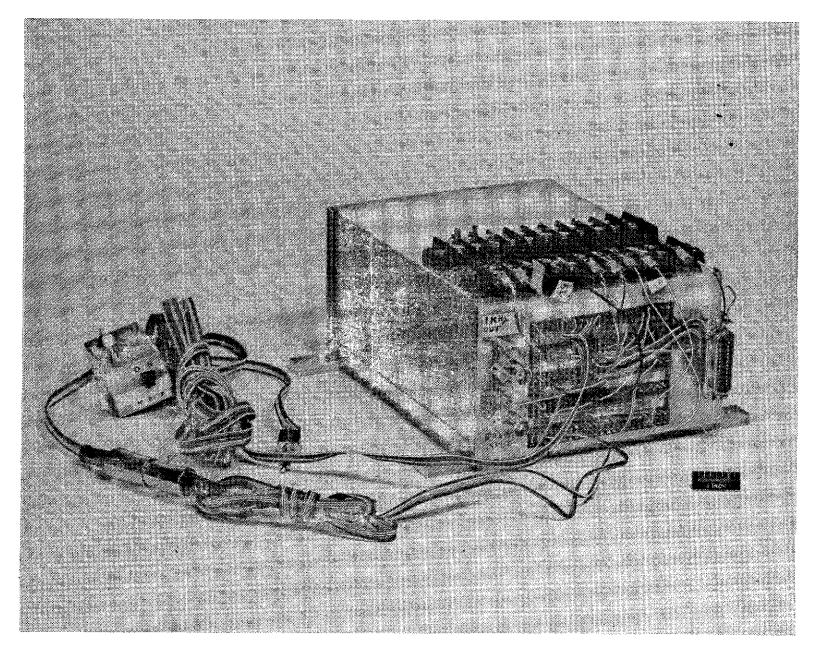


FIGURE 40. COMPLETE CMS CARD CAGE.

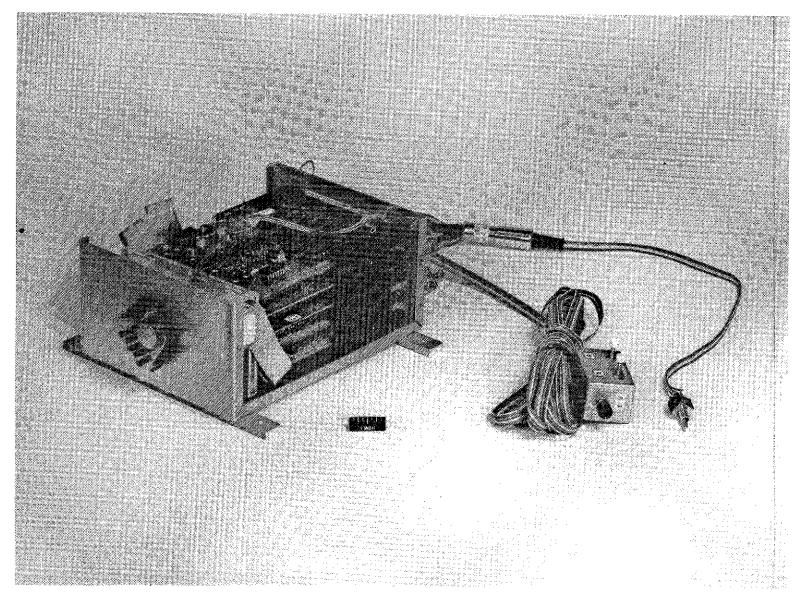


FIGURE 41. CMS CARD CAGE WITH COVER REMOVED.

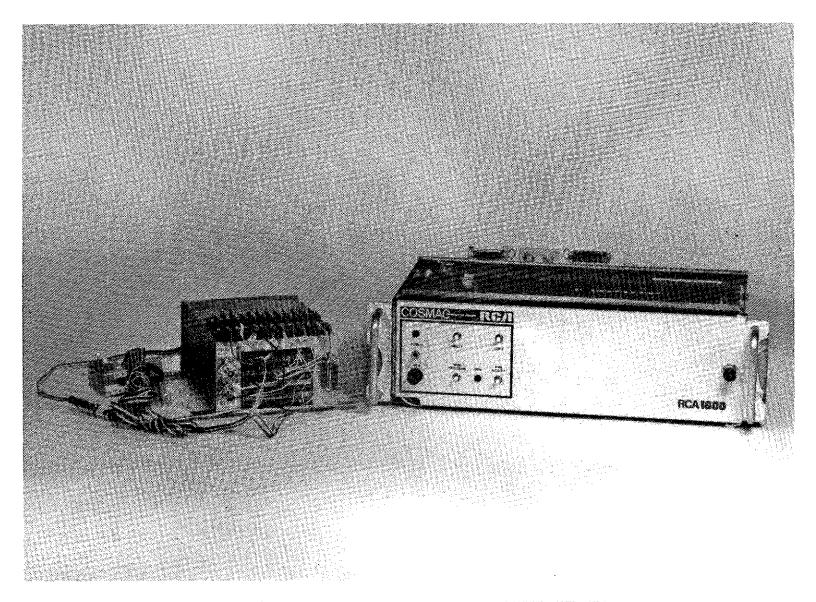


FIGURE 42. SIZE COMPARISON - MICROCOMPUTER AND CDS.

r 4

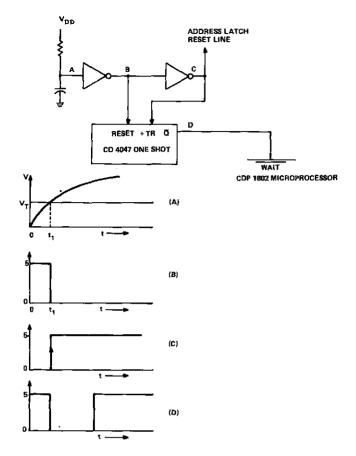


FIGURE 43. REMOTE-START CIRCUIT.

Since point B is high until t_1 and is also the input to another inverter, point C, the output of the second inverter is low until t_1 . This low level is used to reset the address latch to zero. The positive transition shown in diagram (C) is used to generate the pulse to reset and start the microcomputer.

The WAIT pulse is low in diagram (D) for a time determined by an R-C network associated with the CD4047 one-shot. The output of the second inverter (C) cannot be used to restart the microprocessor because of a conflict in timing between resetting the address latch and restarting the microprocessor. The remote-start circuit for the dashboard display microcomputer is the same except for an additional circuit which is used to inhibit interrupt pulses until the microprocessor is running.

C. DISPLAY AND SENSOR INTERFACES

The display and sensor interface hardware that originally had been developed for the COSMAC development system during Phase II was consolidated to fit on three standard cards within the card cage system. The three interface cards,

the CPU interface card and the CPU card, form the electronic dashboard display microcomputer.

The top of the dashboard display card cage has the 8-input analog-to-digital conversion circuit and a trip odometer circuit. The A/D circuit uses three of its inputs to monitor fuel level, water temperature, and oil pressure. A voltage divider is formed between 5 V and ground by a series resistance and the resistance of the respective sensor. The voltage developed across the sensor is converted by the A/D system.

The 8-input analog-to-digital circuit is shown in Figure 44. The heart of the circuit is a Burr-Brown* ADC80AG-10 A/D converter that has a 17-µs conversion time for an 9-bit output. The A/D has a 0- to 10-V input voltage range. The ±15 V necessary to operate the A/D chip is provided by a Datel** DC-DC converter. A CD4051 multiplex chip has 8-channel capability. The 9, 10, 11 pins of the chip are internally decoded to select a channel and connect it to the A/D converter. The multiplex chip is tied to the ±15 V of the DC-DC converter through a voltage-dropping resistor, so that only 10 V actually appears across the chip. The 10 V at the multiplex chip allows 10-V-level signals to be present at the input of the multiplex chip, which can still be switched by 5-V logic levels applied to the channel select pins.

The selection of one of eight channels to be connected to the A/D is accomplished by setting a level at the three binary-coded select pins 9, 10, 11. This level is placed there by the presence or absence of OTD-0, OTD-1, OTD-2 pulses at the "D" input of a CD4013 flip-flop, and is clocked through to the Q outputs (1, 13, 1) by an SIO-4 pulse.

The A/D converter is enabled by an SIO-3 pulse. The completion of the conversion cycle is indicated by the status of the EF-1 flag line. The 8-bit output of the A/D converter is applied to the data bus lines by pulsing a pair of CD4016 transmission gates with a IO-C pulse.

The second circuit located on the top card with the A/D circuit is the trip odometer, shown in Figure 45. The trip odometer must have the capability of retaining distance data when the vehicle is not operating. A connection is made directly to the vehicle battery, and the battery voltage is dropped to the

^{*}Burr-Brown Research Corp., Tucson, AZ.

^{**}Datel Systems, Inc., Canton, MA.

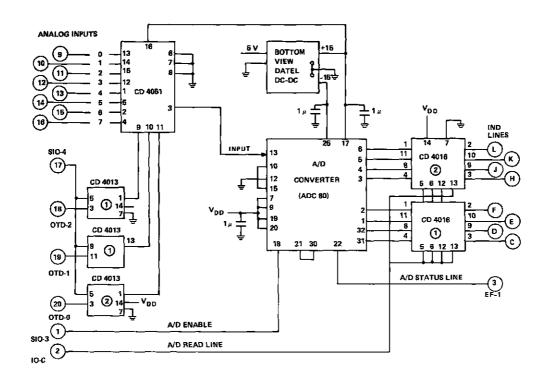


FIGURE 44. 8-INPUT ANALOG/DIGITAL CIRCUIT.

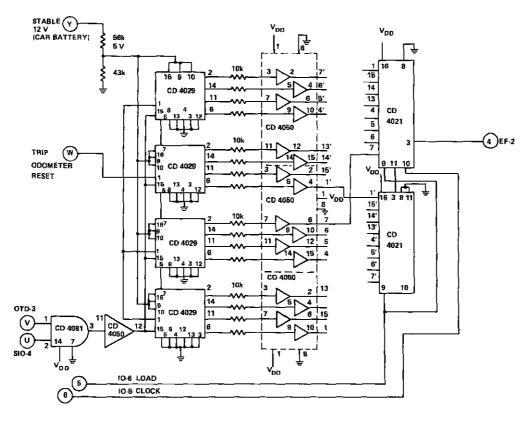


FIGURE 45. TRIP ODOMETER CIRCUIT.

5-V level for operating the CMOS counter by use of a voltage divider. Four CD4029s are used for the trip odometer counters. The counter is updated by a level generated by the simultaneous application of a SIO-4 pulse and an OTD-3 pulse. The 16-bit output of the four counters is connected to 16 buffers through individual $10-k\Omega$ resistors.

The purpose of the $10-k\Omega$ resistors in series with each input to the buffer is to provide protection to the buffer when the computer is in the "off" position. The counters will retain the logic level at their respective outputs because of the stable 12-V supply. During normal operation, the 16-bit output of the buffer is loaded by a IO-6 pulse into two shift registers (CD4021) and the 16 bits are then read serially by the application of a IO-5 clocking pulse onto a flag line EF-2. The trip odometer can be reset by applying a level to reset pin 1 of each of the CD4029 counters. The trip odometer is reset by a debounced switch which provides 5 V for this function.

The second card from the top of the dashboard display card cage is the clock, fuel-economy, tachometer interface. The automobile clock is designed to keep accurate time whether the car's ignition is on or off. The automobile clock circuit is shown in Figure 46. A stable 12 V is applied to the counting circuits by the vehicle battery. The voltage to the respective CMOS chips is reduced to 5 V by a $10\text{-k}\Omega$ voltage-dropping resistor connected in series. An inverter (CD4007) is used for isolation between the oscillator and the four CD4029 counters. The four CD4024 counters are used as dividers, dividing down successively from 32768 to 2048 to 128 to 8 and, finally, to 1 Hz. The 8 Hz is applied to the interrupt circuit section of the remote start. The 1-Hz pulse is applied through a buffer to two CD4017 decade counters which count to 60 and generate a pulse per minute.

Figure 47 shows the pulse-per-minute input applied to two CD4029s, whose function is to count to 59 and then at the next minute reset to 0. The CD4082 at the output lines of the CD4029s provides the logic necessary for the "reset after 59" function. The reset pulse 1 minute after 59 is the hour pulse, which is applied to a single CD4029. This counter counts to 12 and then the next hour resets by jam loading to 1. The CD4073 is used for the "reset to 1" logic function.

The manual minute advance is accomplished by the use of a level derived from a debounced switch and applied to the clock line of the two CD4029s. The incrementing or decrementing of the minute counter is accomplished by use of a CD4049 inverter. A "O" at the input results in a high applied to the up/down

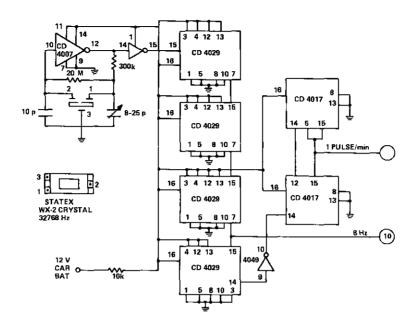


FIGURE 46. CLOCK CIRCUIT DIAGRAM (OSCILLATOR AND MINUTE COUNTER).

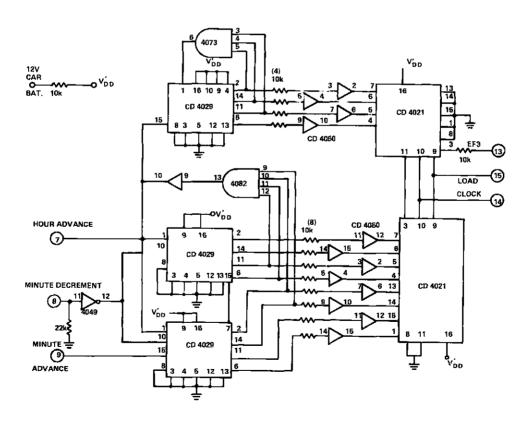


FIGURE 47. CLOCK CIRCUIT DIAGRAM (HOUR ADVANCE).

count pin, which causes the counter to count up. A high level at the input of the inverter makes the inverter output go low, and the counter decrements when a level is applied to the clock line. The hour advance uses a voltage-level from another debounced switch to advance the hour function. The buffer outputs are loaded into two shift registers by a IO-6 pulse and then clocked out serially by IO-5 clock pulses. Note that the load and clock pulses are the same for both the trip odometer and the clock. However, the automobile clock output is read out on flag line EF-3, while the trip odometer is read out on flag line EF-2.

The tachometer interface and the fuel economy interface are also located on the card with the automobile clock. The circuits are shown in Figures 48 and 49. The tachometer interface obtains its input from the point side of the coil. The input is applied through a buffer to a one-shot multivibrator (CD4047). The one-shot multivibrator generates a pulse that is noise-free and free from ringing effects and therefore can be used to drive a counter. The pulse output is applied to a CD4029 counter whose 4-bit output is read by pulsing a transmission gate (CD4016) with a IO-D pulse. The counters are set to "0" initially by the CLEAR-P line.

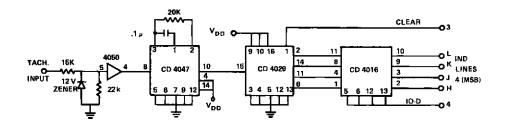


FIGURE 48. TACHOMETER INTERFACE CIRCUIT.

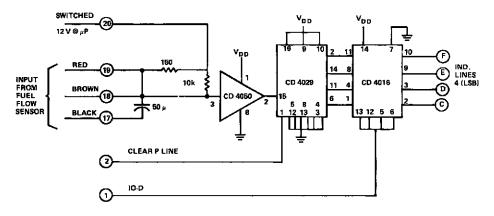


FIGURE 49. FUEL ECONOMY SENSOR CIRCUIT.

The circuitry necessary to operate the Model 261PB-15 flow transducer* is connected at the input to the fuel-economy sensor interface card. The pulse output of the sensor is applied to a CD4050 buffer for logic level conversion from 12 to 5 V. The pulses clock a CD4029 counter which, in turn, is gated on to the transmission bus by the application of an IO-D pulse to a transmission gate. The CLEAR-P line is used to initialize the counter. Note that the IO-D pulse gates simultaneously the tachometer and fuel economy interfaces by gating the upper 4 bits onto the bus for the fuel economy data and the lower 4 bits for the tachometer data.

The third card from the top of the dashboard display card cage contains the display interface, the binary interface, the velocity interface, and a circuit used to check the condition of the restraint system. The display interface circuitry is shown in Figure 50. Eight bits of data are read from the CPU card interface bus lines and stored in CD4042 latches by use of a stretched SIO-1 pulse. Six bits of data are applied to the self-scan unit by use of CD4049 inverters. A "data present" pulse from the latch coincident with the SIO-1 pulse applied to a CD4023 NAND gate provides a logical O which causes the "Data Present" line of the self-scan to go low, thereby permitting the data on the line to enter the memory of the self-scan unit.

Another pulse from the latch is used to clear memory by use of a second CD4023 NAND gate. Pin 14 of the latch is the control bit for "Data Present" or "Clear." Pins 1 and 15 are the latched outputs of the pin 14 input, pin 15 is the complement of pin 1. The two CD4011 NAND gates, the CD4050 buffer, and 1N461 diode and the RC network comprise the pulse stretching network for the SIO-1 pulse. The blank disable line is always tied low so that it is inoperative.

The control function provided by the computer is the same for both the "high brightness" and conventional self-scan display. The conventional self-scan unit makes use of 7 latched data outputs to obtain the 128-character repertoire. The switch located on the clear line of the display is used to stabilize the display from update flicker. If the overall system voltage supply is free from noise, the switch can be left open and the display will not flicker. However, if noise spikes are present on the vehicle's 12-V system,

^{*}Flo Scan Instrument Co., Seattle, WA.

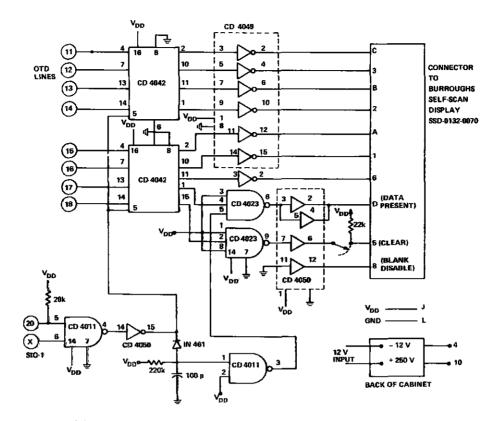


FIGURE 50. SCHEMATIC OF DISPLAY INTERFACE.

the display data will offset because the T²L circuitry of the self-scan unit is affected by noise. Closing of the clear switch will eliminate the data shift on the display but will cause some minor update flicker.

The binary input card of the display microcomputer is shown in Figure 51. It makes use of 9 buffers and 3 transmission gates (CD4050 and CD4016, respectively). The card is broken down into families of buffers and quad-latches. The input of each of the buffers is tied to ground through a 22-k Ω resistor. A 12-V input at the input of any buffer is converted by the buffer to a 5-V logic level at the output. The 12-V inputs are derived from switch sensors. The output of the buffer is read onto the 8-bit data line by gating the proper pair of quad-latches. The quad-latches are selected by IO-9 or IO-A pulses in the display card cage. The binary inputs monitor door switches, service brake switches, brake fluid level switches, battery indication, the selection of the display format, and the airbag or restraint system status.

The circuit used to monitor the voltage from the top of the airbag squib to ground is shown in Figure 52. Two comparator circuits monitor the squib voltage. The voltage from the squib to ground is considered in tolerance if

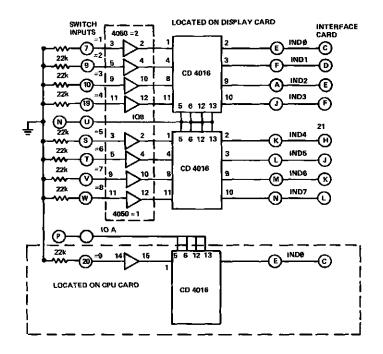


FIGURE 51. BINARY INPUT CARD FOR SWITCHES.

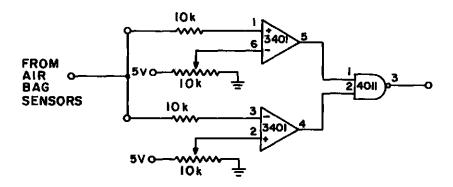


FIGURE 52. SCHEMATIC OF AIRBAG INDICATOR.

it is between 6 and 10 V. Under this condition, the comparator outputs are both high; therefore, the output of the NAND gate is low which in turn is connected to one of the binary input parts. If the voltage from the squib-to-ground should go to 0 or 12 V, one of the comparators will go low; therefore, the NAND gate output will go high thereby causing a 5-V level to appear at a binary input port to trigger the "Restraint System Out" message.

The final circuit on the third card is the velocity sensor interface, shown in Figure 53. A pulse train input is received at the input of the circuit. The pulse frequency is directly proportional to velocity. This pulse

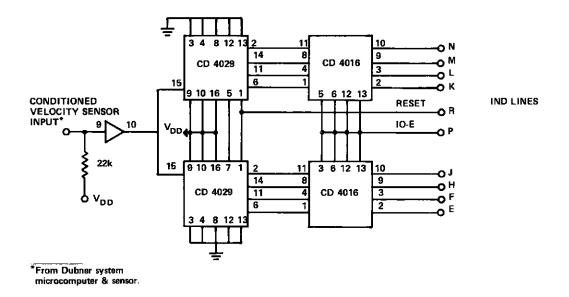


FIGURE 53. SCHEMATIC OF VELOCITY INDICATOR.

train is read by a sensor located on the RSV drive train, buffered by the Dubner system automatic transmission microcomputer, and then passed on via cable to the RCA electronic dashboard display microcomputer. The input circuit is also buffered. The output of the buffer drives a counter which is read through the transmission gates by an 10-E strobe.

SECTION V

CONTROL FUNCTIONS AND SOFTWARE IMPLEMENTATION

A. COLLISION-MITIGATION BRAKING CONSIDERATIONS

The two key features of the collision-mitigation system are (1) the automatic application of antiskid brakes in case a high-speed collision is definitely unavoidable and (2) the complete elimination of false alarms (i.e., no application of brakes in cases where no real collision is imminent or where the driver could have avoided the collision by himself). For a better understanding of the boundaries that guide automatic braking, a simplified summary of braking dynamics is presented.

The general case of two vehicles moving toward each other, with one being braked, is illustrated by the time-distance relationship shown in Figure 54. The following assumptions are made:

 $\mathbf{v_1}$ is the initial velocity of the radar-equipped car

 v_2 is the initial velocity of the target vehicle $(v_2 < 0)$

 \boldsymbol{v}_{T} is the impact velocity of the radar-equipped car

 v_{It} is the total impact velocity $(v_{It} = v_I - v_2)$

µg is the maximum braking deceleration (0.9 g for dry road, antiskid brakes)

 $\boldsymbol{R}_{\!\scriptscriptstyle +}$ is the radar detection range

Δt is the reaction delay (0.1 s for the radar processor and algorithm and 0.1 s for the brake system to reach full braking action)

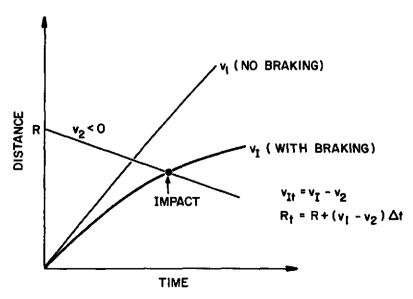


FIGURE 54. DISTANCE/TIME RELATION BETWEEN TWO VEHICLES, ONE OF WHICH IS BEING BRAKED.

The relation between impact velocity, $\mathbf{v}_{\text{It}},$ and the radar detection range, $\mathbf{R}_{\!_{\text{T}}},$ can be expressed as

$$R_{t} = \frac{1}{2\mu g} \left\{ (v_{1} - v_{2})^{2} - v_{1t}^{2} \right\} + (v_{1} - v_{2}) \Delta t$$
 (32)

This equation applies, of course, also for the case of impact with a fixed object by setting $\mathbf{v}_2 = \mathbf{0}$. Since $\mathbf{v}_1 - \mathbf{v}_2$ can be replaced by the measured rangerate, $\dot{\mathbf{R}}$, we obtain the more general relation

$$\mathbf{v_{It}} = \sqrt{\dot{\mathbf{R}}^2 - (\mathbf{R_t} - \dot{\mathbf{R}}\Delta t) \ 2\mu g} \tag{33}$$

The impact velocity as a function of different radar detection ranges, R_t , and initial closing rates, \dot{R} , is shown in Figure 55. For a collision with a fixed object, for example, the impact velocity v_{It} is reduced from an initial speed of 25 m/s (55 mph) to 13.7 m/s (30 mph) if a detection distance of 30 m is maintained. This corresponds to a reduction in impact energy by 70%.

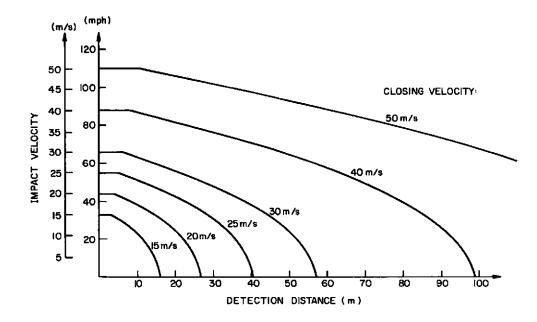


FIGURE 55. IMPACT VELOCITY AS FUNCTION OF DISTANCE BETWEEN RADAR CAR AND COLLISION OBJECT (SYSTEM DELAY 0.2 s; BRAKING COEFFICIENT μ = 0.9).

For head-on collisions where both vehicles are going at a speed of 25 m/s (55 mph), the impact velocity is being reduced by 8.8 m/s (17 mph), provided both cars have CMS braking with a detection range of 30 m. The impact energy

is correspondingly reduced by 30%. Here the energy reduction is not so pronounced, but still significant enough to make a substantial difference in the severity of the injury sustained by the driver. Figure 56 shows the resulting impact velocity, \mathbf{v}_{It} , as a function of closing rate, $\hat{\mathbf{R}}$, for different detection ranges. Also indicated are lines of constant energy reduction.

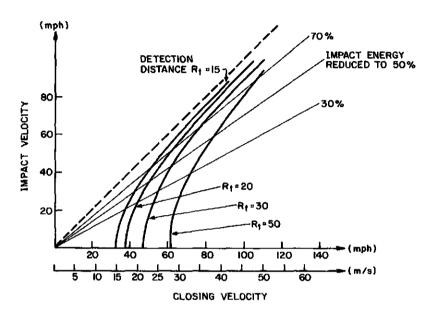


FIGURE 56. ENERGY REDUCTION AS FUNCTION OF DETECTION DISTANCE AND CLOSING RATE.

The above calculations clearly indicate the importance of having a large detection range, $R_{\rm t}$, for the radar and a fast reaction time for the overall system. These requirements are counteracted by the need for keeping all false alarms at an absolute minimum and, equally important, for ensuring that a driver remains in control of the car as long as there is any possibility of avoiding an accident by skillful driving maneuver.

Based on a typical maximum lateral acceleration of 0.3 g (which is rarely exceeded by the average driver), a minimum distance of 32 m is required [11] to avoid an obstacle straight in line with a vehicle driven at 25 m/s (55 mph). We, therefore, selected a maximum detection distance, $R_{\rm t}$, of 30 m for a car driven at 25 m/s. If a driver at this speed approaches an obstacle without

R. Limpert, <u>Motor Vehicle Accident Reconstruction and Course Analysis</u>, Michie Company, Charlesville, VA, December 1978.

steering wheel or brake pedal activation, the automatic antiskid braking should take over. At lower speeds, this distance should obviously be reduced further.

B. COLLISION-MITIGATION SYSTEM

The inputs to the CMS algorithm consist of range, range-rate, steering angle ϕ , brake pedal status indicator, and car velocity. The range-rate is derived directly from the beat counts during the up- and downswing of the frequency modulation cycle, and is not generated by differentiating range with time. Range-rate can, therefore, be used to independently check the validity of range data obtained at different time points.

The entire CMS algorithm (a complete program listing is included in Appendix B) is conveniently subdivided into two parts. The first part includes the acquisition of radar data, calculation of range, range-rate, car velocity, and a check of steering wheel angle and brake pedal position. The second part contains the actual decision subroutine which activates the antiskid brakes if all conditions for two sets of data separated by a time interval, Δt , are fulfilled. Two flags and a status bit, DF, keep track of the decisions made at various points within the algorithm.

chart form in Figure 57. First, the number of transitions within a measurement interval are counted. From the number of transitions within the measurement interval, we can determine the number of periods within the measured interval. If we do not have at least one period within either the upswing or downswing measurement interval, we repeat the entire measurement process. The accumulated count is read for both the upswing and downswing modulation interval. The count in each case is averaged by dividing by the number of periods within the respective measurement interval. A deviation check is performed on each period measurement of the up- and downswing. A failure of the deviation check restarts the entire measurement process. If only one period was measured on the up- and downswing of the modulation cycle because of a close target or dropouts, the periods are compared to each other and, if they exceed a set tolerance, the measurement process is restarted.

If after passing the transition counter check, deviation check, and if necessary the single period check, the data is considered acceptable, range and range-rate values are determined from a table using the up and down count

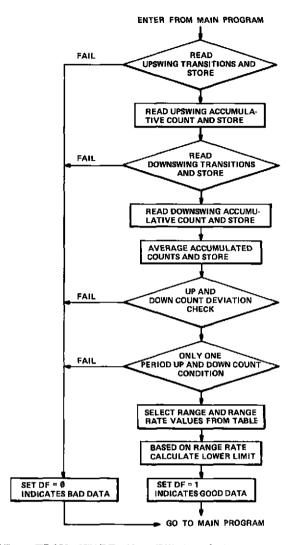


FIGURE 57. FLOW CHART OF GETRAN (DATA ACQUISITION).

readings as a parameter. A 1-bit status indication, DF, is set to indicate good data readings after a lower limit value has been calculated from range-rate data. The good data readings are either taken over a full measurement interval during the full modulation upswing and downswing or over part of a cycle, from the beginning of the interval up to the point of a dropout.

Once range and range-rate data have been computed, the primary purpose of microprocessor software is to sort out real emergency situations from false alarms. This is performed in the main CMS algorithm, shown in Figure 58. A target moving toward a radar-equipped car does not always require automatic braking, as for example in tight turns or parking maneuvers. The speed cutoff eliminates the possibility of emergency braking if the car velocity is less

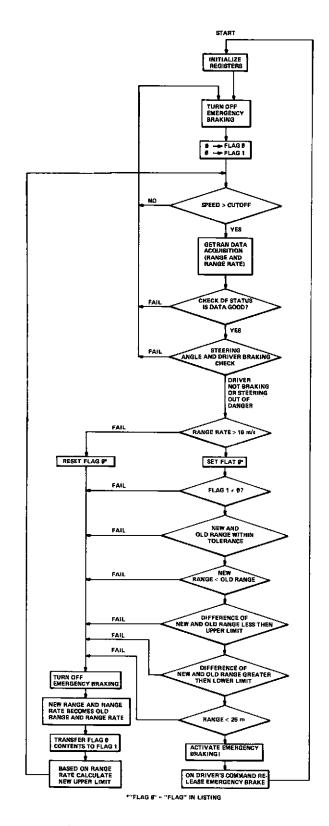


FIGURE 58. FLOW CHART OF MAIN CMS PROGRAM.

than 10 m/s. The velocity cutoff computation is done in the electronic dashboard display software. If the cutoff velocity is exceeded, a flag is set by the dashboard display microcomputer and is read by the CMS algorithm. An indication of bad data acquired by GETRAN is signaled by the status bit DF = 0 and the software restarts the overall measurement process. An indication that a driver is taking action by steering or braking also causes the software to begin again.

If we have reached a point where the vehicle is operating above a set speed and has acquired a target and there is no reaction in the form of braking or steering by the driver, further analysis is then made of the potential threat. If the closing rate between the target and the radar-equipped RSV is less than 16 m/s, the target is not considered a severe threat, emergency braking is prohibited, and the range and range-rate data are stored as a reference. Based on range-rate a new value of range difference is calculated for an upper limit, which is later used in the algorithm. In case the driver is not reacting and the closing rate or range-rate is greater than 16 m/s, a flag is set. Another flag (called flag 1) is checked to see whether this is the first or second test of acquired data. If flag 1 is 0, which corresponds to the first test of acquired data, the range and range-rate data are stored as a reference or "old data" and a new upper limit is computed. The contents of flag 0 which has been set previously are then tranferred to flag 1.

Now the process starts again; once data is acquired a second time, the set speed is exceeded, and there is no reaction by the driver, and the closing rate is above 16 m/s, additional checks are performed by software to verify the presence of a real target. Checks are also made to determine if the difference between the newly acquired range-rate and the old range-rate is within a certain tolerance. The newly acquired range must be less than the first range reading. The difference between the new range reading and the previous one must fall between a lower and upper limit value that is a function of range-rate. Finally, the range measured has to be less than the cutoff range of 25 m. Only if all of these conditions are met is the emergency braking activated.

The automatic activation of the antiskid brakes will be disabled if the driver takes over the braking maneuver. This is considered an indication that the driver is in control. Also, if any of the conditions for range comparison are rejected, automatic emergency braking is prohibited. The newly acquired data then becomes the reference or old data, and a new value is calculated for

the range difference upper limit. A target threat is still considered because a flag is set to indicate the successful acquisition of one set of data. Another consecutive set of data is therefore needed which, if it passes all of the test conditions, will enable the automatic emergency braking condition that applies the antiskid brakes.

The computation and decision making time for the CMS algorithm during Phase II was approximately 160 ms. For the new CMS algorithm, which includes more sophisticated decision making, this time is only approximately 80 ms. The reduction in software processing time can be attributed to two reasons. First, the new RCA CDP 1802 microprocessor has a larger instruction set than the 1801 unit used during Phase II. Secondly, the software is greatly improved together with the use of look-up tables and faster multiplying chips.

C. HEADWAY/CRUISE CONTROL

1. Introduction

A car equipped with a collision-mitigation system has limited sales appeal because under normal conditions, a driver would be totally unaware of the system's presence. As discussed before, emergency braking is to take place only when a severe collision is unavoidable, and a good driver should, hopefully, never find it activated. Public acceptance of the radar could be greatly increased if it were also to provide improvements in convenience and traffic flow. Automatic headway control that governs the safe spacing of successive cars on limited-access highways is such an application.

The difference between regular cruise control and radar headway control is illustrated in Figure 59. In the normal cruise control, a fairly popular option in American cars, the driver can select a particular cruising speed, \mathbf{v}_{set} , and the car will maintain this speed $(\mathbf{v}_1 = \mathbf{v}_{\text{set}})$ until a new speed is set or the brake pedal is tapped. This convenience feature is, unfortunately, not very useful when traffic density increases. Cars ahead, going at only slightly lower speeds, force the temporary disablement of the cruise control or lead to rather dangerous weaving in and out of traffic lanes to avoid having to reset the cruise control.

Under radar headway control, the radar senses the distance and closing rate with respect to the vehicle ahead and controls the throttle to match the speed of the first car $(v_2 = v_1)$ and keep a safe headway. If there is no other vehicle ahead, cruise control takes over and the car resumes the preset speed. In the present implementation, only the throttle is interfaced with the radar;



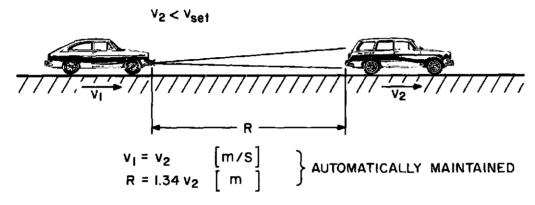


FIGURE 59. COMPARISON BETWEEN CRUISE CONTROL AND RADAR HEADWAY CONTROL.

if the closing rate becomes too high, a warning signal is given on the electronic display and the driver has to take over.

2. Design Considerations

A block diagram of RCA's headway-control system is shown in Figure 60. The driver makes his inputs through switches located on the turn signal stalk. An RCA 1802 based microcomputer monitors ground speed and interprets signals from the radar. Throttle control signals are computed and delivered in the form of variable width pulses to a linear DC motor which is connected to the car's throttle by a chain. The computer has control of the full travel of the throttle, but cannot at present initiate brake activation. Limited deceleration due to air friction and engine drag is achieved when the throttle is fully released. When more rapid deceleration is required the driver must intervene by personally applying the brakes. Whenever the computer senses driver application of the brakes, it responds by fully releasing the throttle and relinquishing control back to the driver until instructed by the driver to resume control.

For diagnostic and demonstration purposes we have interfaced a Burroughs* self-scan single-line display to the computer. Although it is not required for

^{*}Burroughs Corp., Plainfield, NJ.

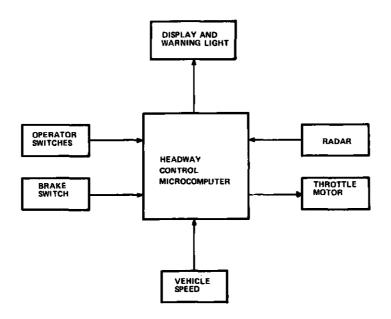


FIGURE 60. BLOCK DIAGRAM OF HEADWAY-CONTROL SYSTEM.

operation of the system, the display is useful for indicating radar-measured range, range-rate, vehicle speed, and other system state information. A yellow warning light on the display is turned on when the closing rate is too high (over 3 m/s) or the following distance is dangerously close (less than 10 m).

Control for the throttle is implemented entirely within microprocessor software as a sequence of discrete-time computations. A diagrammatic representation of these computations is shown in Figure 61. Computed expressions are shown by their z transform equivalents, while events external to the computer are shown as continuous time LaPlace transforms. The fundamental inputs to the computer are range, R, and velocity, v. Range-rate, R, is computed as

$$\dot{R} = \frac{R_1 - R_0}{t_s} \tag{34}$$

where \mathbf{R}_1 is present range, \mathbf{R}_0 is previous range, and \mathbf{t}_s is the sampling time of 0.5 s.

There is some inherent "noise" in range data in headway control because the radar beam looks at different positions on the irregular surface of the target car. Road bounce of the radar and target aggravate the noise. There is also quantization noise of range due to the way the radar signal is processed and to the finite precision of the microprocessor computations. Range measurements are quantized in steps of 5 cm. Velocity is quantized in steps of 0.1 m/s. Input noise is propagated to the throttle control causing annoying jerky motions which can be sensed by passengers.

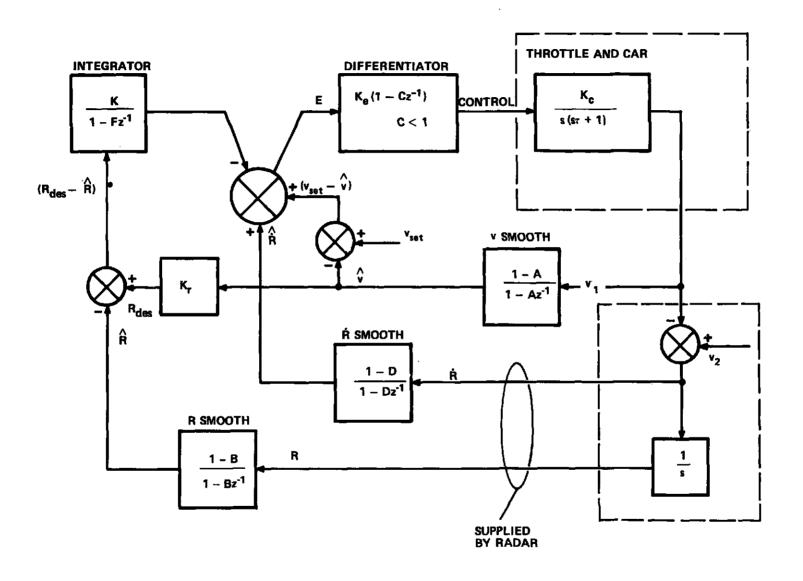


FIGURE 61. AUTOMATIC CRUISE/HEADWAY-CONTROL ALGORITHM.

In an effort to reduce the effects of noise, smoothing functions are used on R, \hat{R} , and v to generate \hat{R} , \hat{R} , and \hat{v} . Heavy smoothing provides the quietest outputs, but there is a decline in responsiveness as smoothing is increased. Since \hat{R} is a time derivation of range it is potentially quite noisy and therefore has heavy smoothing. Care must be taken in choosing the \hat{R} smoothing constant \hat{D} so that sudden changes in closing rate are reflected quickly enough in \hat{R} .

The desired headway distance is computed as

$$R_{des} = K_r v ag{35}$$

This headway distance increases linearly with road speed. Constant K_r is presently 1.5 m per m/s; for example, the desired distance at 25 m/s (55 mph) is 38 m. The difference between $R_{\rm des}$ and \hat{R} constitutes a range error which we attempt to minimize. Similarly, the difference between $v_{\rm set}$, the cruise control set speed, and v constitutes a velocity error which is minimized in a conventional cruise control. Referring again to Figure 61 we see that velocity difference between the two vehicle, \hat{R} , and a term representing an integrated range error are fed into the main summing junction to produce error E. This error is compensated by a differentiating expression $v_{\rm e}$ (1-Cz⁻¹), C < 1, to generate throttle control. The feedback compensation is designed to force $v_{\rm e}$

In general, increasing E will produce more throttle acceleration and decreasing E will cause throttle release. If the radar car is moving at less than \mathbf{v}_{set} , a positive velocity error is present at the summing junction. The range error integrator permits the velocity error to be canceled out at the junction, even as the range error is reduced toward zero. In the present system we were so far not able to implement a perfect integrator (F = 0.9 instead of 1.0 is being used) because of some instability problems. The remaining residual error has the same polarity as the velocity error and has a magnitude of about 1.45 m for each 1 m/s of velocity error.

The residual error results in a headway distance which is smaller than desired, an effect that becomes more pronounced when the set cruising speed is much higher than the actual speed. We believe that this deficiency can definitely be eliminated by properly adjusting the integrator term. However, since any changes also affect other constants of the loop, work priorities and available time restrictions did not permit us to fully optimize these

counter dependent system parameters. In practice, the deviation from the correct headway distance does otherwise not affect the proper operation of the headway control.

As indicated earlier the control output is in the form of a signed number which is converted by digital circuitry to a pulse, the width of which is proportional to the magnitude of the number. The throttle motor is turned on for the duration of the pulse. Thus the microcomputer generates relative position control for the throttle, rather than absolute or direct positioning. For this reason the throttle is modeled as an integral controller (1/s). The car has a response time τ , and the combination of throttle and car are modeled in the diagram as $K_{c}/[s(s\tau+1)]$.

In an ordinary driving situation the radar is constantly acquiring targets and losing them again as they go out of range. At any instant the system can be considered to be in any of the five states, as shown in Figure 62. In addition to "Cruise" and "Resume" found in conventional cruise controls, we also have "Headway," "Capture," and "Lost Targets." The arrows in the diagram show permitted state transitions. "Resume" permits the car to go from present speed to previous set speed after "Cruise" has been disengaged by the brake. "Resume" is implemented as a special form of "Cruise" in which the reference speed to be obtained is gradually raised from present speed to set speed at the rate of 3.3 m/s per second. Thus if set speed were 25 m/s and "Resume" is engaged at

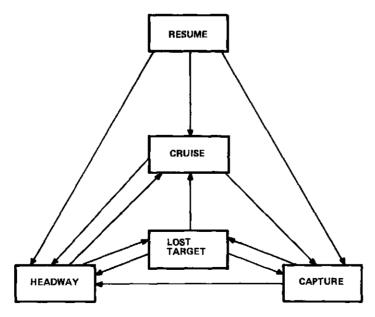


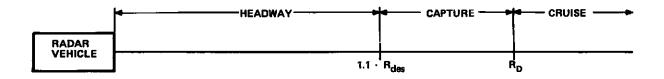
FIGURE 62. STATE TRANSITION DIAGRAM.

15 m/s, the resume state will last approximately 3 seconds. Without a "Resume" state, the car would accelerate very rapidly and overshoot the set speed considerably.

When a target is acquired the system will go from "Resume" or "Cruise" to "Headway" or "Capture." "Capture" is intended as a transition state from "Cruise" to "Headway." "Capture" is implemented as the opposite of "Resume" with "Cruise" reference speed reduced from set speed at the rate of 1.8 m/s. Figure 63 shows how "Capture" begins at range $R_{\rm D}$ and terminates when range is 1.1 $R_{\rm des}$. "Capture" range is computed as

$$R_{D} = K \dot{R}^{2} + R_{des} + 3 m$$
 (36)

Increasing the closing rate increases R_{D} , lengthening the capture distance. If a target is acquired at a range of less than 1.1 R_{des} , or if the closing rate is very low, the "Capture" state is bypassed and we go directly to "Headway."



$$R_D = K \cdot \dot{R}^2 + R_{des} + 3m$$

FIGURE 63. CAPTURE MODE.

The "Lost Target" state is needed because a target may appear to drop out occasionally, due to signal multipath or multiple target detection. It is undesirable to return immediately to "Cruise" because of a momentary signal loss. In the "Lost Target" state, the throttle is held steady for up to 1.5 seconds while the radar tries to reacquire the target. If at the end of this time there is still no target, the system transits from "Lost Target" to "Cruise."

The important transition rules are summarized below:

- (1) From "Resume" or "Cruise" to "Capture" -- Target is acquired and 1.1 \cdot $R_{\rm des}$ < \hat{R} < $R_{\rm D}$
- (2) From "Resume" or "Cruise" to "Headway" -- Target is acquired and $\hat{R} < R_D$ and $R < 1.1 \cdot R_{des}$

- (3) From "Capture" to "Headway" -- \hat{R} < 1.1 R_{des}
- (4) From "Headway" to "Cruise" -- $(v 1.4 \text{ m/s}) > v_{\text{set}}$ or $\hat{R} > 2.3 \text{ m/s}$

Rule 4 inhibits the target car from "towing" the radar car.

3. Algorithm Flow Diagram

The headway-control software is written in RCA Level II Assembly language and is stored in 3K bytes of EPROM. It consists of an interrupt service routine which executes whenever the driver presses a switch or the timer interrupts, and a main program loop, which runs continuously. The interrupt service routine has the following functions:

When a switch is pressed on the driver's stalk, a status bit is set in a microprocessor register, provided the current velocity is above 9 m/s (20 mph). The main program later tests this status bit to determine if the switch has been pressed. For the SET SPEED or SET 55 switches, the interrupt routine will store v as present speed or 55 mph (90 km/h), respectively. When the foot brake is depressed, the interrupt routine will release the throttle completely, giving the fastest possible response. When the timer interrupts, the velocity sensor is read and v is computed. In addition, timer status is used to synchronize the main program so that range measurements are taken at precise intervals.

The main program loop is shown in flowchart form in Figure 64. A description of the basic algorithm using block numbers from the flow chart is given below.

- I Initialize microprocessor registers and memory locations.
- II Release throttle completely (normally not engaged) and erase start-up message from display. This step requires about 2 seconds.
- III Wait for driver to press SET SPEED or SET 55.
- IV Loop synchronization. Wait for timer interrupt indication. Time interrupt occurs every 0.5 second.
- V Input data from radar card. Determine validity of data using deviation check.
- VI, VII If data valid, compute range, R.
 - VII-X If target has been lost for 1.5 seconds, leave headway state; otherwise hold throttle.

- XI-XIII Warning light management. If R < 10 m or there are two consecutive measurements with R < -3 m/s, warning light is turned on; otherwise it is turned off.
- XIV-XVI If this is first valid range measurement, variables must be initialized. Two consecutive valid range measurements are required to compute radar control.
 - XVII Compute smoothed range, range-rate, smoothed range-rate, and summing junction error.
- XVII-XXI If not in HEADWAY state, transition rules are used to see if we should go to CAPTURE.
 - XXI If in CAPTURE state, capture processing is done.
 - XXIII If $v > v_{set}$ or R > 2.3 m/s transition to RESUME or NORMAL is made.
 - XXIV Control is computed using headway control compensation equation.
- XXV-XXVIII If RESUME switch has been pressed, do RESUME state processing until $v_{ref} > v_{set}$; otherwise $v_{ref} = v_{set}$.
 - XXIX Control is computed using normal cruise compensation equations.
- XXX-XXXII If brake has been pressed, we want to avoid sending further control outputs to the throttle since it has been disengaged by the interrupt service routine. Wait until driver releases brake and presses a switch before continuing.
 - XXXIII Control is sent to the throttle pulsing circuitry.
 - XXXIV Self-scan display is formatted according to current state.

 This is not essential to system operation.

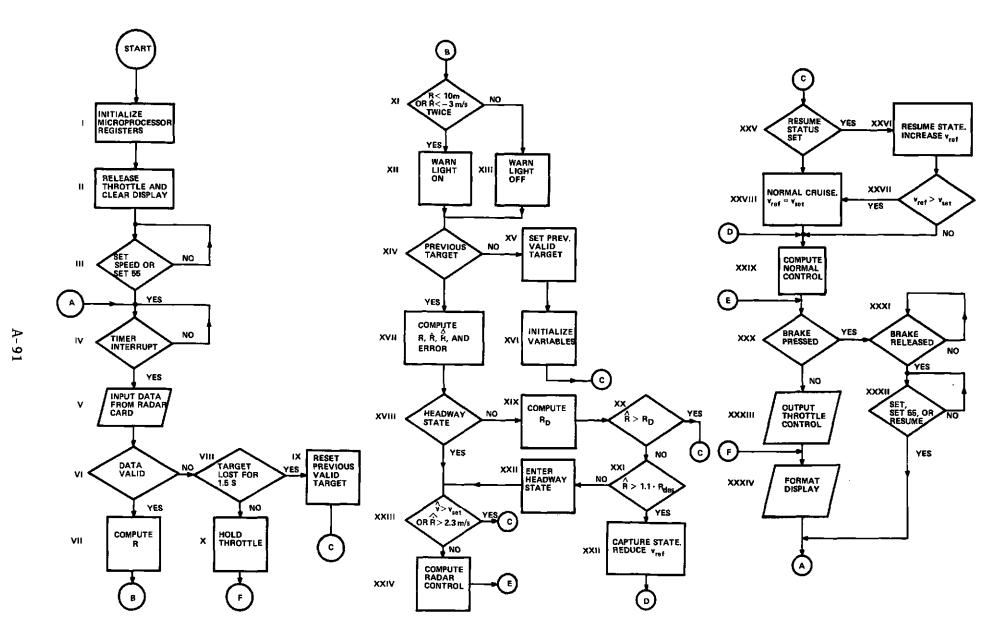


FIGURE 64. HEADWAY-CONTROL FLOW CHART.

SECTION VI

PERFORMANCE TESTS

A. TEST VAN INSTRUMENTATION

A special test vehicle was equipped to permit the recording of radar and video data for optimization of the radar hardware and software. Aside from providing a test platform for the radar, the vehicle is also fully instrumented with recording equipment and other test gear for evaluating the performance of various components of the radar system. A Ford "Econoline" van, shown in Figure 65 houses all of the test equipment and acts as a mobile laboratory. The front of the van is fitted with a support structure that accommodates different antenna configurations. Figure 65 also shows the Ku-band bistatic system radar without radome assembly mounted on the van. The metal plate underneath the radar antenna assembly is covered with an RF absorber material and shaped to simulate the front of the RSV. By use of the absorber material and metal plate, the near-field effects of the nose assembly of the RSV were studied as a function of the positioning of the absorber material relative to the plate and antenna.

The interior of the van is fitted with instrument benches and a seat for the equipment operator. Figure 66 shows the video camera in front and the radar recorder in back of the van with its supporting equipment. The camera is fitted with a wide-angle lens to give a panoramic view of road conditions. It is mounted next to the driver, strapped down on the motor housing. A view of the scene presented to the camera through the windshield is shown in Figure 67.

In addition to the camera, the test van is also equipped with a velocity sensor and steering wheel indicator. The velocity sensor is a generator-type unit attached to the speedometer cable whose output is a frequency directly proportional to velocity. The steering wheel sensor is a potentiometer attached to the front wheel linkage. The resistance of the potentiometer is part of an R-C network of an astable multivibrator whose frequency therefore varies as a function of steering wheel angle. Information from the three sensors, camera, steering wheel, and velocity sensor is recorded by the Panasonic* video tape recorder.

^{*}Panasonic Co., Secaucus, NJ.



FIGURE 65. TEST VAN FOR RECORDING OF VIDEO AND RADAR INFORMATION.

A block diagram of power sources for instrumentation and environmental control is shown in Figure 68. AC power for the instrumentation, especially the video equipment, is provided by a Deltec* static inverter. This unit provides a sinusoidal output of 110 VAC at 60 Hz ±0.15%. The inverter has a power capacity of 1.2 kW. The power input to the inverter is provided by an additional heavy duty 135-A Leece-Neville** alternator with a 250-A/hour battery backup. The AC power for the environmental control and the less frequency-sensitive instruments is provided by a 4-kW Onan motor generator mounted in a separate compartment at the rear of the vehicle. The environmental control for the mobile lab is provided by an Intertherm RV roofmount airconditioner. The unit provides 12,600 BTUH of cooling and 5400 BTUH

^{*}Deltec Corp., San Diego, CA.

^{**}Sheller Globe Corp., Leece Neville Div., Cleveland, OH.

[†]Onan, Huntsville, AL.

^{††}Intertherm, St. Louis, MO.

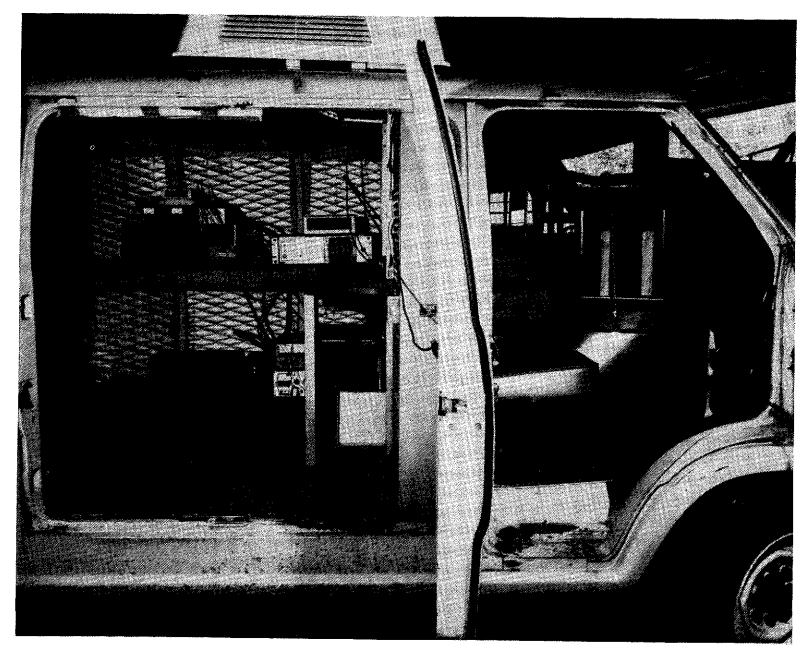


FIGURE 66. INTERIOR OF TEST VAN.

FIGURE 67. VIEW FROM TEST VAN DURING CMS TESTS ON AIRPORT RUNWAY.

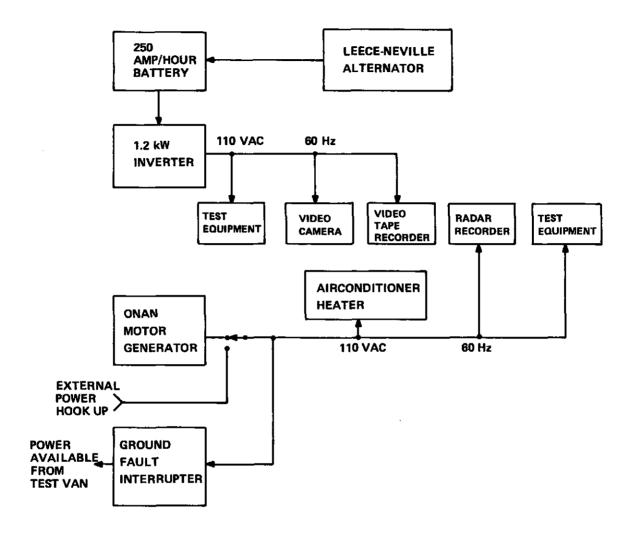


FIGURE 68. BLOCK DIAGRAM OF POWER DISTRIBUTION IN TEST VAN.

of heat. The Intertherm unit has been rewired to operate in a bucking mode to alternately heat and cool so that a relative humidity of 40% maximum could be maintained. The low humidity is necessary for the tape used with the recorders. A switching arrangement is available to power all equipment in the van from an external AC line voltage. In the field, AC voltage is available from the van through a ground fault interruptor protected circuit.

The test van has proved itself extremely valuable in the testing of all X- and Ku-band monostatic and bistatic radar systems. It was also used in simulated crash tests with disposable 1- and 10-m² targets at various speeds, on a runway at a nearby airport, as shown in Figure 69. The most extensive use of the vehicle was for recording radar returns and video representations

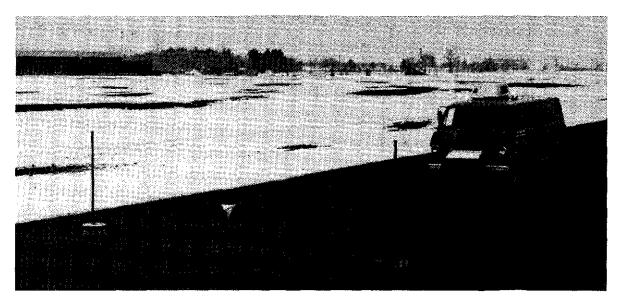


FIGURE 69. TEST VAN DURING CMS TEST WITH EXPENDABLE TARGET.

of actual traffic situations. These radar recordings, which were used for the optimization of the CMS algorithm, were performed during different weather conditions and with a variety of road and traffic scenarios.

B. COLLISION-MITIGATION SYSTEM TESTS

One of the problems encountered during Phase II was the testing and evaluation of hard- and software for the mitigation system. Rather than repeatedly drive a fixed route and possibly tailor a system to operate only for that peculiar case, we found that a better, more true-to-life approach is to drive as much as possible in many different scenarios. However, following the random driving procedure still made system evaluation subjective. For example, an event that occurred in a particular location on a road with a particular traffic pattern and under unique weather conditions might cause a false alarm during testing. Corrective software and/or hardware changes would therefore be made to the system. Returning to the same location where the original false alarm occurred would possibly indicate that we no longer receive a false alarm. The question is, have we really accomplished anything? The answer can only be perhaps. Returning to the same location only partially ensures a repeat of road condition. The traffic pattern and weather condition during the initial test that may have given a false alarm can not easily be repeated.

During Phase III, we resorted, therefore, to a more rigorous approach for testing and algorithm optimization. A system was developed that recorded both the beat frequency return from the radar and the video information from the scene that the radar was illuminating. In addition to the radar and video recording, the audio track of the video recorder was used to read both speed and steering information. By use of this recording system a tape library of a variety of traffic situations was acquired. Playback of the recording system through the microprocessor would thus give perfect repetition of events. Hardand software changes could be made and the effect of these changes could reproducibly be observed when the tapes were played back.

A block diagram of the recording system is shown in Figure 70. The video output from the camera, trace (a) of Figure 70, shows the video format. The camera generates horizontal sync pulses every 63 µs. Between the 10-µs-long sync pulses, the video information is contained which represents a single line (horizontal) on a video monitor. The video system uses random interlace which means a vertical sync pulse moves through the horizontal sync pulse every 1/16 of a second. The horizontal line frequency of the camera was chosen as the system clock.

The video output from the camera feeds into a video tape recorder (VTR), a switch, and a sync stripper circuit. The sync stripper circuit picks up the sync pulses from the video. To eliminate the effect of the vertical sync pulse moving through the horizontal sync pulses, the horizontal sync pulses are fed to a digital phase lock loop (DPLL) which operates at the horizontal line frequency. The output of the DPLL is divided down to give 977 Hz, which corresponds to the repetition frequency of the radar modulation. To further smooth the square wave generated from the horizontal line frequency, the divided-down signal is fed to a DPLL operating at 977 Hz. The output of this circuit, a 977-Hz square wave, goes to three locations. First, the 977-Hz square wave is used to generate the triangular wave to modulate the radar system TEO. The 977-Hz square wave is also used to provide external sync for a radar recorder, thereby electrically synchronizing the video and radar recorder, and finally the 977-Hz square wave goes to the sync pulse generator and combining circuit. The positive and negative transitions of the square wave trigger one-shot circuits.

The relationships between the sync pulse generator and the incoming square wave are shown in diagrams (b) and (c) of Figure 70. The wider sync pulse

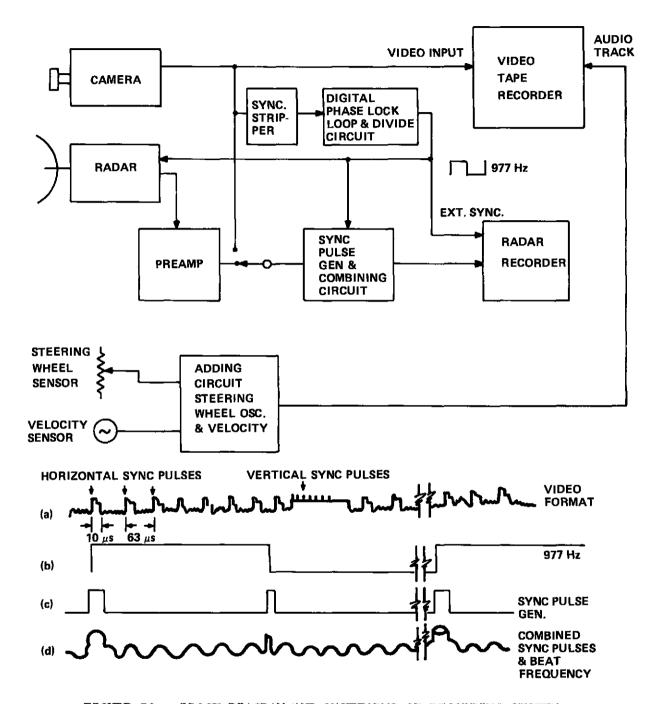


FIGURE 70. BLOCK DIAGRAM AND WAVEFORMS OF RECORDING SYSTEM.

corresponds to the positive transient of the square wave. The sync pulses generated from the square wave are combined with the beat frequency return from the radar preamplifier and recorded. The reason for the simultaneous recording of the sync pulse and the beat frequency is to maintain the proper phase relationship between the beat frequency waveform and the square wave that is used to modulate the TEO.

Two additional sensors on the test van are used to record velocity and steering angle. The pulse train from the steering-wheel angle sensor and the velocity information are combined and both recorded on the audio track of the VTR. The recording system therefore records the beat frequency return from the radar postamplifier in correct phase relationship with respect to the modulating square wave.

The video tape recorder used with the system is a Panasonic NV-5120, a standard consumer type cartridge unit with a recording time of 30 minutes. The radar recorder is a flight test "Star" manufactured by RCA in Camden, NJ for military use. This unit has a 3-MHz bandwidth (modified) and is capable of being synched to an external source (977-Hz square wave). The "Star" recorder uses standard video tape and can record about 20 minutes.

The block diagram of the playback system is shown in Figure 71. The output of the VTR is fed to the TV monitor. The video recorded on the tape recorder is also passed on to a sync stripper circuit and DPLL divider circuit that generates a 977-Hz square wave from the horizontal line frequency of the recorded video. The 977-Hz square wave is used to externally sync the radar recorder. The output from the radar recorder goes to another sync stripper circuit which strips off the pulses corresponding to the transitions of the original waveform. The output of this circuit goes to two locations. first location is a DPLL and square-wave reconstruction circuit which restores the original modulating square wave. A switch is used to determine the positive transition by referring to the wider sync pulse that had been recorded. The second location that receives the stripped sync pulse is a sync canceling circuit. Another input to this particular circuit is the beat frequency which includes the sync pulses from the radar recorder. The sync canceling circuit subtracts the stripped sync pulse from the beat frequency, which then goes through a radar postamplifier to the microprocessor.

The audio track of the VTR is separated by filtering, and velocity information and speed information are fed separately to the microprocessor. The microprocessor thus receives the beat frequency input, a 977-Hz square wave, and the sensor inputs. The microprocessor response is indicated by a self-scan unit or by reading out memory locations from the evaluation board using an execuport terminal. A photograph of the system set up in the playback mode is shown in Figure 72. At the left is the "Star" recorder; next to the "Star" recorder is the Panasonic recorder. The monitors and self-scan display are visible in the photograph as well.

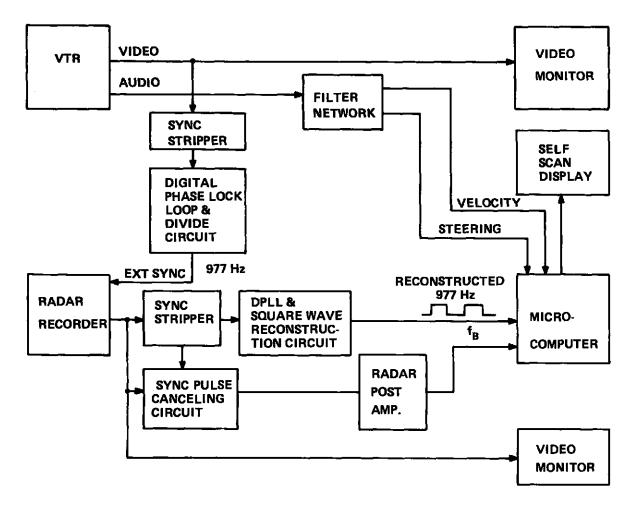


FIGURE 71. BLOCK DIAGRAM OF PLAYBACK SYSTEM.

The purpose for using two video monitors is to synchronize the data recorded by both recorders. The two recorders are always electrically synchronized, but only in multiples of the sync pulses. To sync the two recorders in time, video information is simultaneously recorded on both recorders for a short period of time. During playback, the video recorder is started first, advanced to an easily identifiable scene, and frozen. (The Panasonic VTR has stop-action capability.) The radar recorder then is started and when the video scenes of both monitors match, the Panasonic unit is restarted and both recorders are in time synchronization.

With the recording system loaded in the test van, a large variety of scenarios were taped. Several runs were made on Route 1, a four-lane divided highway with moderate-to-heavy traffic. These runs were made with both the X-band and Ku-band bistatic radar systems. Two tapes were made during light



FIGURE 72. SYSTEM FOR SIMULTANEOUS PLAYBACK OF RADAR AND VIDEO INFORMATION.

e a

and moderate snow conditions on Route 1. An attempt to record data during a severe blizzard failed because only video data was inadvertently recorded on both recorders. Recording runs were also made on Route 206, a heavily travelled two-lane road with a variety of curves. The effect of very hilly terrain was recorded northwest of Princeton.

In order to investigate the effects of bridges and tunnels, several recording runs were made to New York City. A recording run was also made on the NJ Turnpike, a six-lane divided highway with limited access. When it became clear that the Ku-band bistatic system was definitely superior to the X-band system, several of the X-band tapes were erased and recorded over with Ku-band data. Runs through a disposable target at a nearby airport were also recorded. The airport runs were made for 1-m² and 10-m² targets at 20, 30, 40, 50 and 60 mph.

The use of this recording system greatly helped in the systematic evaluation and optimization of the radar system. By playing back the tapes, the early version Phase III CMS radar interface hardware could clearly be identified as more sensitive to a variety of target conditions than the Phase II CMS radar interface card. This was demonstrated to DOT and Minicars personnel in September 1978. Another recorded tape during playback through the microprocessor indicated a constant offset in the range-rate readings. While the tapes were rerun, the microprocessor was halted and memory locations that contained the up and down counts were examined. An analysis of this data showed that the range-rate offset was caused by a nonlinear FM deviation in the TEO of the radar system.

The majority of the tapes had been recorded in situations that had a high probability of giving a false alarm with the CMS system. Two examples of tapes that initially gave us false alarm indications were the bridge and tunnel runs to NYC and the curve-rich part of the Route 206 run. False alarms were generated by one of the towers that supports the suspension cables of the Verrazano Narrows Bridge. Modification of the CMS software, specifically the deviation check constant, eliminated this problem. Once this correction was made to the software, the tapes were rerun to ensure that the correction did not destroy the sensitivity of the system. The deviation check tolerance tightening that eliminated the bridge tower false alarm in the first tape also eliminated the problem in the second tape.

The most informative tapes about the operation of the CMS were the airport tapes. These tapes of runs through the disposable target were considered the standard by which any changes in hardware or software were measured. The runway tapes were particularly useful to determine when a brake signal is given. The reaction time of the braking system was measured by putting a stop in the CMS software when the braking command is given. The memory contents of the evaluation-board card cage system can then be used to measure reaction time. For a given run through a target, the velocity of the vehicle is known. From the data in memory we can determine when the target was acquired (range), and the range-rate when the braking signal was given is also available. From these data the reaction time of the CMS can accurately be determined. The brake signal appeared reproducibly at a distance of at least 23 m from the target for all targets and speeds. Based on a car speed of 25 m/s (55 mph) and a brake system delay of 0.1 s, the automatic application of antiskid brakes with the above system would result in a 45% reduction in crash energy.

C. HEADWAY-CONTROL TESTS

1. System Optimization

The main requirements on a radar headway-control system are safety, driver convenience (smooth control, with minimum action required from driver), and fuel economy. Whereas false alarms are totally unacceptable in the collision-mitigation mode, which limits the active range to below 30 m, the headway control requires range information up to at least 45 m, but permits some false alarms, provided they do not lead to jerky movement of the car. Satisfactory headway control under actual traffic conditions is difficult to realize because it requires low-fluctuation, high-accuracy range and range-rate data that constantly act upon the car's throttle and thus are continuously preceived by the driver.

Since it is very difficult to separate problems caused by the control loops from radar processing problems, the initial optimization and program development for the headway control was performed with a cooperative radar system. An existing X-band FM/CW radar was modified to accept only return signals from tagged targets, as discussed in subsection III.B. By use of the cooperative system, problems with false alarms, signal dropouts, target scintillation, etc., are greatly reduced or totally eliminated. The headway-

control algorithm can thus be investigated and optimized under idealized conditions; this is important for separating the possible causes of erratic or jerky performance and helped greatly in the initial phases of the headway algorithm development.

The tagged target car provided a clean reliable return signal which could be processed to give stable, highly accurate range readings. Tests with two tagged cars simultaneously pointed to the possibility of false alarms, even with the cooperative system. For example, in gradual curves and at great distances, a tagged vehicle in the outer lane may easily be mistaken for a vehicle in the radar car's lane. Thus, although the cooperative system was very instrumental in the headway-control development, it does not represent the complete solution to the false alarm problem when there are many tagged vehicles on the road.

The initial headway-control system optimization was performed using RCA-owned station wagons for the radar car and as tagged target vehicles. The radar-controlled car was equipped, aside from the cooperative X-band radar and its associated computer, with a strip chart recorder and an inverter to permit the use of an execuport terminal in the car for on-the-road program changes of algorithm constants. The strip chart recorder provided accurate readouts of vehicle velocity, range, throttle position, and throttle control voltage as a function of time. For later fuel economy runs the car was also equipped with a highly accurate fuel metering device. A photograph of the experimental computer and recorder installation is shown in Figure 73. The system was mounted in place of one of the front seats which was removed for the testing period. The throttle of one car was activated through a chain by a linear DC motor, which in turn was controlled by the computer. This arrangement is shown in Figure 74. The potentiometer attached to the throttle axis was used only for monitoring and diagnostic purposes.

2. Road Tests

The flow chart algorithm of the headway control shown in Figure 61 is the outgrowth of a series of other algorithms that were tried and step-by-step improved to arrive at a workable control system. Initial tests with a simple vacuum-based throttle controller proved unsatisfactory until a more reproducible and linear DC motor was installed as control element. Single-loop control laws originally tried had to be abandoned in favor of more complex ones to obtain suitable, stable operation under a variety of operating conditions.

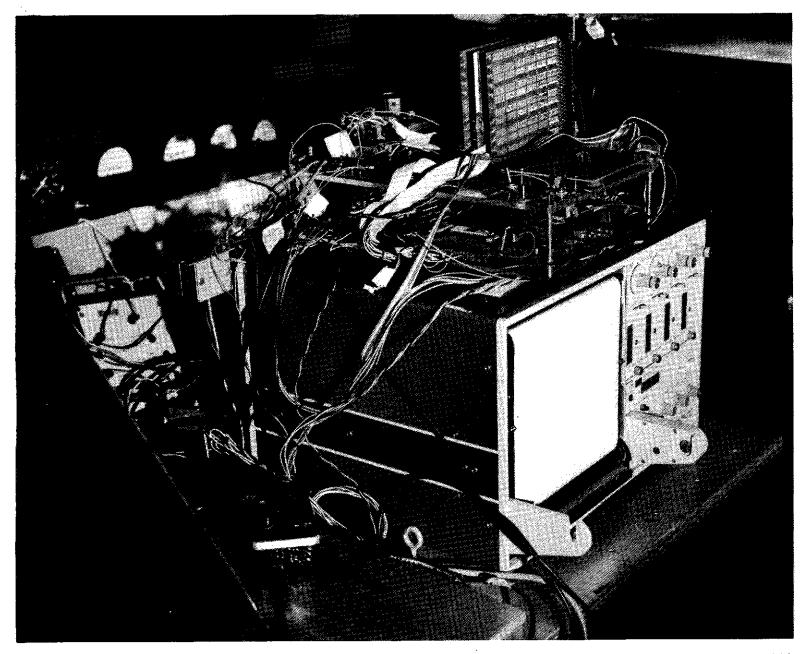


FIGURE 73. HEADWAY-CONTROL COMPUTER AND STRIP CHART RECORDER MOUNTED IN FRONT OF RCA STATION WAGON.

•

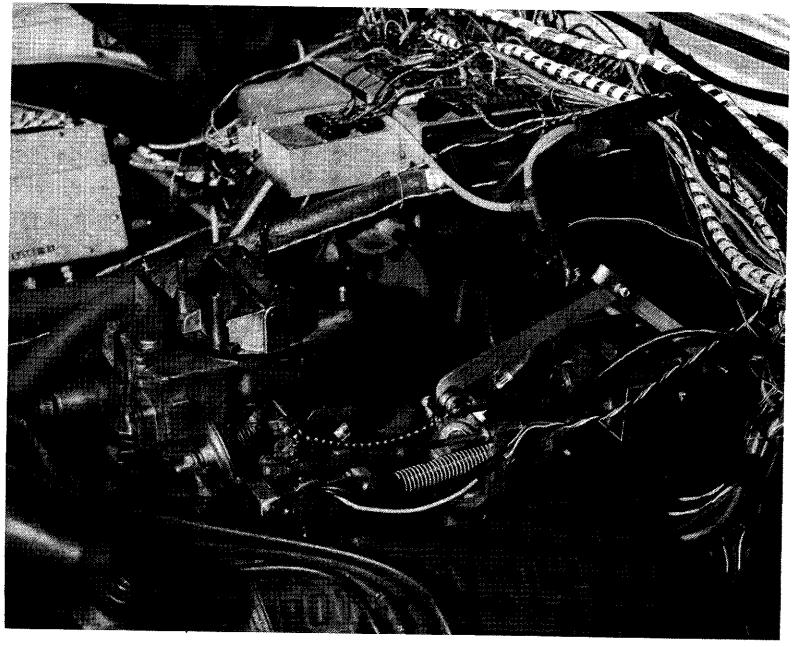


FIGURE 74. LINEAR THROTTLE ACTIVATOR.

Initial values for the constants in the final algorithm shown in Figure 61 were derived from dynamic tests performed on the car with a dynamometer and from certain driving tests. The optimization of these constants was then performed experimentally with the help of the strip chart recorder and by driving with the cooperative radar system over the same stretches of road to ensure reproducibility. The final fine tuning of the algorithm was performed with the noncooperative Ku-band radar in open traffic driving.

Figure 75 shows a typical strip chart recording from early tests. The tick marks on the uppermost line represent 1-minute intervals. The next trace represents the radar car velocity ranging from 13.6 to 25 m/s (30 to 55 mph). The next lower trace shows the range to the tagged target car ahead which in this case was operating under cruise control at 45 mph. The two lowest traces are the actual throttle position, $\theta_{\rm Th}$, and the control voltage, $\rm V_{\rm Th}$, to the throttle. This particular run represents early results on the cooperative system. Although the range and the velocity are kept reasonably constant (range deviations remain within ± 1.5 m), the throttle control voltage fluctuates widely causing a very jerky and erratic driving behavior.

For comparison, Figure 76 shows a run obtained with the noncooperative Kuband radar following a standard passenger car at the final stages of algorithm optimization. Here, in spite of the fact that the radar faces the full road environment in the noncooperative mode, velocity and range variations remain acceptably small while short-term throttle angle fluctuations have decreased to approximately 1 degree, providing a smooth ride free from perceptible jerks.

Aside from headway control, the system is also capable of providing regular cruise control operation and includes special programs for the transition modes of target capture, lost target, and resume speed. All of these functions were finally optimized under actual traffic conditions found on typical high-speed, limited-access freeways.

A series of controlled test runs were performed toward the end of the program to investigate the possibility of cruise and headway control having a beneficial effect on fuel consumption. Contrary to some earlier, not well documented tests which showed a superiority of cruise/headway control, no significant differences could be established within the bounds of run-to-run fluctuations (±2%) between cruise/headway control and average "sensible" driving behavior. Some drivers indeed had the habit of using a "heavy" foot on the gas pedal and, consequently, ended up with poor fuel economy. However, anybody aware

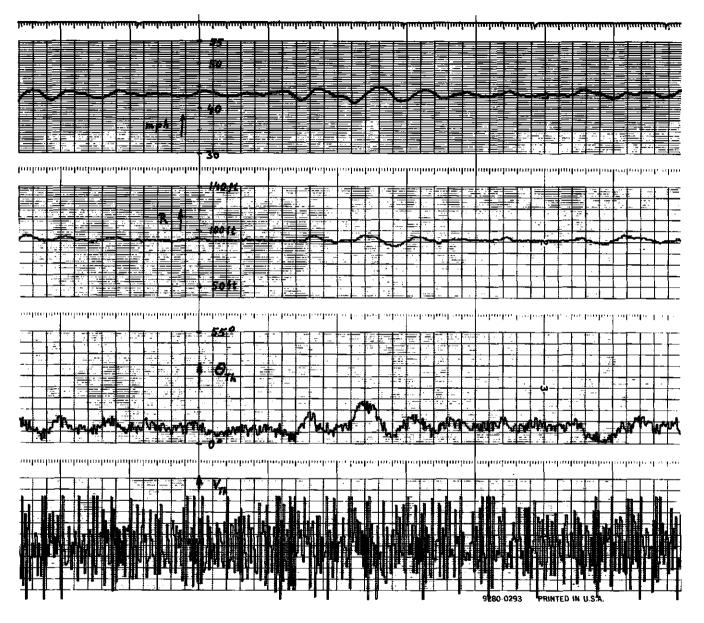


FIGURE 75. EARLY RECORDING OF COOPERATIVE RADAR CAR FOLLOWING A TARGET CAR OPERATING IN CRUISE CONTROL AT 45 mph.

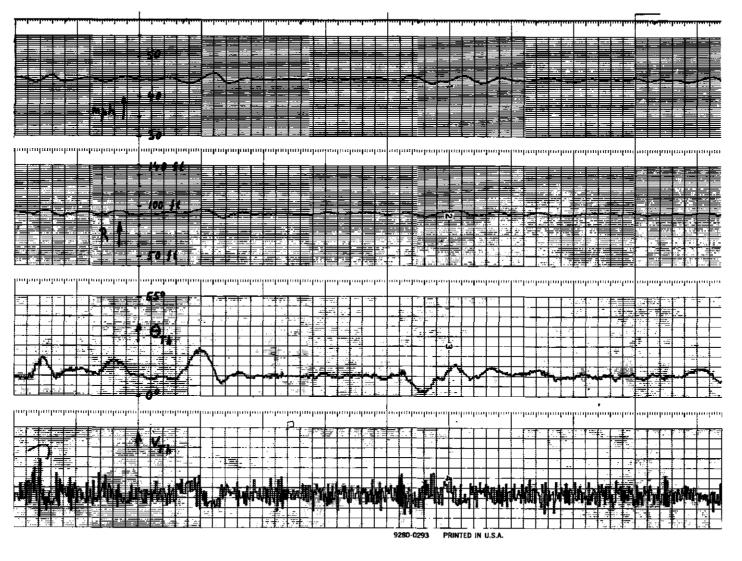


FIGURE 76. NONCOOPERATIVE Ku-BAND RADAR CAR FOLLOWING STANDARD PASSENGER CAR (PINTO) USING OPTIMIZED ALGORITHM.

of what causes poor fuel economy could, without difficulty, duplicate the fuel economy of the cruise control. The tests were performed over a 26-mile stretch of highway in both directions to average wind loading; each type of test consisted of several runs. The fuel consumption was measured by a Fluidyne* fuel flow meter.

The following test runs were taken:

- (a) Driver only (asked to keep reasonably constant speed)
- (b) Cruise control
- (c) Radar car following cruise control car
- (d) Driver asked to keep constant distance after cruise control car
- (e) Driver asked to intentionally accelerate and slow down while keeping average speed equal to cruise-control car ahead.

Tests a, b, and c did not show any significant differences in fuel consumption. Only test e showed clearly poorer performance whereas test d, while demonstrating much poorer performance in keeping a constant distance to the car ahead (± 5 m versus ± 1.5 m for the radar headway control), showed only a slight ($\sim 10\%$) increase in fuel consumption.

Based on these admittedly limited tests, we concluded that no significant claims to better fuel economy could be made. The headway-control system, however, did perform equally to a cruise-control system or the average conscientious driver and is capable of keeping the spacing between cars to much closer values than average drivers can. The latter effect may be quite beneficial in establishing better column stability and higher throughput for high-density "safe" traffic flow. However, these factors require considerably more theoretical and practical studies.

3. Headway-Control Demonstration Vehicle

The unavailability of a suitable RSV for headway-control development made it necessary to use an RCA station wagon for algorithm optimization. For demonstration purposes the car was finally stripped of all the excessive electronic attachments and prepared as a demonstration vehicle. Figure 77 shows the RCA headway/cruise control car with a Ku-band bistatic radar attached to the front.

^{*}Fluidyne Instrumentation, Oakland, CA.



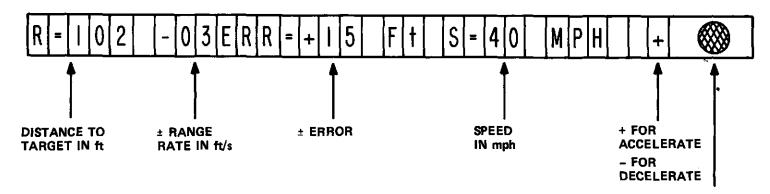
FIGURE 77. HEADWAY-CONTROL RADAR MOUNTED ON RCA STATION WAGON.

The car is also equipped with a display which provides range, range-rage, distance error, and vehicle speed information. This display is used for demonstration purposes only and would not be present in a regular headway-control-equipped car.

Operation of the headway-control system is similar to operation of a conventional cruise control, since the computer makes all decisions concerning how the radar information is to be used. The directional signal control stalk has three momentary contact switches added for "Set," "Set 55 mph," and "Resume." None of the momentary switches can be activated below a speed of 9 m/s (20 mph). The "Set 55 mph" switch is a convenience feature not found on conventional cruise controls, but is easily implemented in software. An on/off toggle switch is used to inhibit control of the throttle, but in the present system the display will be actively updated even in the off position. This is useful for checking the operation of the radar.

In general, drivers adapt quickly to the headway-control system, learning to use it within a few minutes. The major difficulty is learning which circumstances require driver braking, and which can be handled adequately by computer release of the throttle. As a rule the computer can handle closing rates on the order of 2.3 to 4.5 m/s (5 to 10 mph), depending on where the target is acquired. The system has been driven extensively in real traffic, following cars and trucks of various sizes and shapes, and found to perform smoothly in most situations.

Figure 78 shows the format of the Burroughs display when the system is in the headway control state. The values \hat{R} , \hat{R} , $(R_{des} - R)$ and \hat{v} are displayed. The warning light requires two consecutive range-rates smaller than -3 m/s for activation. Nonsmoothed range-rate is used for rapid response. The light goes out when $\hat{R} > -3$ m/s. The light is also activated if range is less than 10 m. If the driver activates the brake, the throttle immediately returns to the closed position and the display information disappears. The car is then fully under the control of the driver.



WARNING LIGHT

R < 10 m

R < - 3 m/s

FUNCTIONS: NORMAL CRUISE CONTROL

CAPTURE

HEADWAY CONTROL

LOST TARGET

RESUME CRUISE CONTROL

CONTROL STALK:

CHOOSE CRUISING SPEED

SET: SET 55: CRUISING SPEED 55 mph RESUME: RETURN TO LAST SET SPEED

ON/OFF: DISABLES THROTTLE CONTROL

FIGURE 78. DISPLAY FORMAT FOR HEADWAY-CONTROL DEMONSTRATION.

SECTION VII

INSTALLATION OF EQUIPMENT INTO THE RSV

A. GENERAL

The original program plan called for the integration of all electronic systems into a high-technology version of the RVS. This includes, aside from the RCA-developed components, an antiskid system, an airbag deployment system and a computer-controlled automatic transmission. Due to delays in getting the RSV to RCA Laboratories for installation of our systems and difficulties with the operation of the automatic transmission, the final integration of the CMS and headway control into the RSV had to be postponed to mid-1980 at which time the car should return to RCA Labs and be equipped with all other electronic systems and be completely operational. In the meantime, the RSV was instrumented with the alphanumeric display and associated microcomputer and sensors. The CMS computer was installed and interconnected for tryouts of the basic functions and then removed again. Also the fitting of the antenna radome into the nose section of the RSV was completed; it awaits final installation after all other body work on the RSV is finished. The performance of the CMS and headway-control system has been demonstrated so far only on RCA-owned vehicles.

B. MICROCOMPUTER AND SENSOR INSTALLATION

The dashboard display and CMS/headway-control microcomputers were installed in the luggage compartment of the RSV. Proper sensor connections to both microcomputers were made with conventional twisted wire pairs. Only the radar was connected via two coaxial lines to avoid spurious pickups on the modulation and IF return lines. A dedicated 12-V and ground line was run from the battery to a terminal strip mounted on the side wall of the front compartment near the two RCA microcomputers. The purpose of running dedicated lines to the microcomputers and radar was to minimize the effects of possible ground loops or excess voltage drops between the battery and the respective systems.

The following sensors were interfaced, calibrated where necessary, and checked for proper operation: hand-brake switch, brake fluid level switch, door switch, water temperature sensor, oil pressure sensor, velocity sensor, fuel flow sensor, fuel level sensor, tachometer, battery status indicator, restraint system status, and brake and steering wheel position switches. All

sensor wires were connected to a terminal strip mounted on the top of the dash-board display microcomputer. In this way, if necessary, each sensor could be tested individually for proper operation. A set of instrument gauges that came with the RSV was used as reference to calibrate the dashboard display microcomputer with respect to water temperature and oil pressure. The sensors that monitored these functions were connected by dashboard mounted switches to either the gauges or the dashboard microcomputer.

Two intra-microcomputer connections were also made. The first connection was between the Dubner system microcomputer and the RCA dashboard display microcomputer. This connection, after buffering, is used to pass on the velocity pulse train monitored by the Dubner microcomputer system. A connection between the dashboard display microcomputer and the CMS microcomputer passes on information when the calculated velocity is above the set speed in the CMS algorithm by setting an appropriate level.

The steering angle microswitch and associated hardware were mounted in an enclosed area adjacent to the luggage compartment that afforded protection from harsh automotive environmental conditions. An illustration of the electromechanical arrangement used to determine when the preset steering wheel angle cutoff is exceeded is shown in Figure 79. The cams and microswitches are adjusted to allow 1-1/2 degrees of steering on either side of center. Exceeding this limit on either side provides a 5-V level to a flag line on the CMS microcomputer. A calibration of the wheel's center alignment was made by following a 40-m-long line on the test range and noting the steering wheel position. Using alignment plates marked in degrees with the front wheels, the microswitches and cams were set to allow 1-1/2 degrees steering on either side of the center position before triggering the flag level. The lock-to-lock steering for the RSV is approximately 30 degrees on either side of the center position. The 1-1/2-degree steering angle was chosen as a compromise between having a good margin against false alarms on one hand, and not being too sensitive on the other hand. The steering wheel angle tolerance can be adjusted independently to have a greater or smaller cutoff angle on either side of the wheel's center line.

The airbag sensor circuit consists of resistances associated with the three impact sensors in series with the two paralleled airbag squibs. The airbag sensor interface (see Figure 52) monitors the voltage drop from the squib to ground. Thus, should any one of the six sensor switches (each impact sensor includes two sensor switches) have accidentally shorted out or more than two

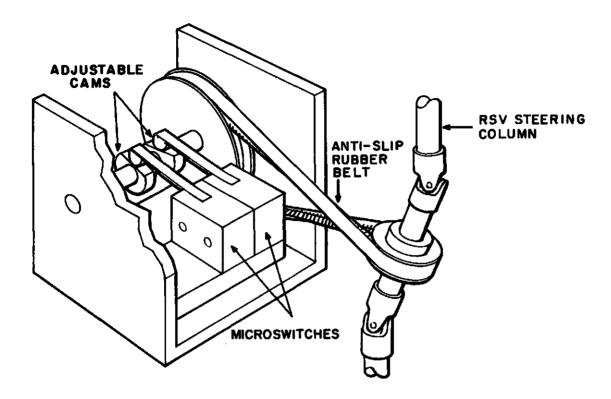


FIGURE 79. ELECTROMECHANICAL ARRANGEMENT FOR STEERING ANGLE DETERMINATIONS.

be open-circuited, the sensor interface will provide a warning message on the display. The problem of determining whether the squibs themselves are possibly either open or short circuited is being addressed separately by Minicars.

A Burroughs high brightness display with two bezels and edge lighting was mounted in the display housing that was delivered with the RSV. The assembly was temporarily mounted by a bracket to the RSV dashboard and interfaced with the dashboard display microcomputer through a set of connectors for ease in installation and servicing. A switch was installed on the dashboard to select either the upper or lower bezel with the corresponding proper display format. A potentiometer permits variation of the intensity of edge lighting of the bezels. The final installation of the display in the proper dashboard location will be made after Minicars replaces the present experimental dashboard with the final version.

C. RADAR SAFETY CONSIDERATIONS

In view of the growing concern on part of the public and the government with nonionizing radiation effects, the microwave power typically radiated from a collision-mitigation/headway-control radar was investigated theoretically as well as practically.

Our present Ku-band radar emits nominally a power of 10 mW from an antenna with a gain of ~ 30 dB. In the far field of the antenna, the power density decreases as $\frac{1}{R^2}$ with R, the distance from the antenna. Closer to the antenna

this law does not hold since we are in the near field or Fresnel region of the antenna. By normalizing the field in the far-field region, we can recalculate the field intensities closer to the antenna, as shown in Figure 80. The field pattern undergoes various spatial maxima and minima due to interference in the near field. Based on a radiation of 10 mW from a 30-dB antenna, the maximum power density is $20~\mu\text{W/cm}^2$ at a distance of 0.6 m.

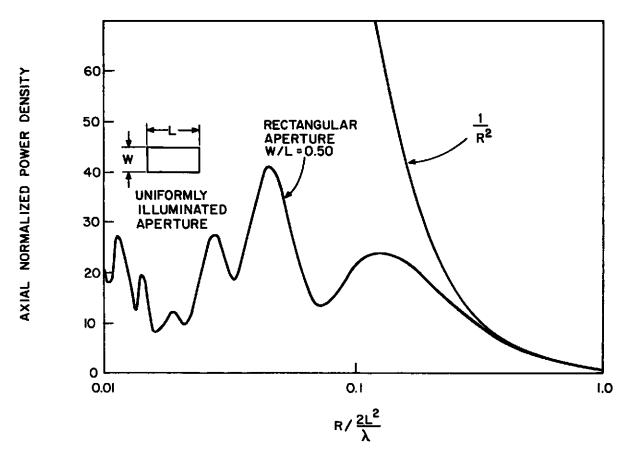


FIGURE 80. ANTENNA FIELD INTENSITIES.

Actual measurements performed with a small waveguide antenna in the near-field area of the antenna showed a maximum power density of 15 $\mu\text{W/cm}^2$ at a distance of approximately 1 m from the antenna. These measurements are not to be considered very accurate since the presence of the waveguide distorts the existing field pattern; however, the measured values give a good order-of-magnitude indication of what fields can be expected in front of the antenna.

At present, the United States microwave radiation limit is 10 mW/cm 2 , which is based on the onset of thermal effects in the human body. The Soviet Union, on the other extreme, maintains a limit for continuous exposure as low as $10~\mu\text{W/cm}^2$ to avoid possible neurological and physiological effects. Substantial controversy exists as to where a realistic safe limit should be drawn. In any case, the amount of nonionizing radiation to which humans may be exposed from CMS/headway radars is very low, and for distances above a few meters is even below Russia's very stringent standards. In addition, the radar could be easily equipped with a solid-state switch that prohibits radiation below a certain critical speed, which would further reduce the radiation exposure of humans in actual traffic.

SECTION VIII

COST ESTIMATES

A production cost analysis of the CMS and headway-control system was prepared using RGA's PRICE program [12]. The system analysed consists of an FM/CW Ku-band bistatic radar and a three-chip microprocessor controller set (since large production quantities are assumed, VLSI would be implemented) in a metallized weather-tight plastic box. The cost of the velocity and steering wheel position sensor, the throttle controller for the cruise control system, integration, and testings are included in the overall production cost figure. The complete CMS and radar cruise control system is estimated to have a production cost figure of \$177. This production cost figure is based on 100,000 units, 1979 dollars and 1985 technology.

The PRICE program gives a range of production costs for each item. The upper value is the worst-case prediction. The actual production cost of an item will be somewhere between the high and low extremes. The cost breakdowns are as follows:

The electronics for the radar and processor are assumed to be contained within a metallized weather-tight plastic box. The box also contains the bistatic radar system consisting of two antennas and associated electronics. The purpose of metallizing the box is to provide a ground plane for the printed circuit antennas. The predicted production cost range of the metallized weather-tight plastic box varies between \$12.92 to \$18.77, with \$15.07 the average cost. The microprocessor system that will provide the CMS and cruise control functions is assumed to require a total of three VLSI chips. The production cost for the three-chip system including the PC board on which the ICs would be mounted ranges from \$7.99 to \$12.98. The average cost of the three-chip microprocessor controller including the necessary ROM and RAM is \$9.58.

The cost evaluation of the radar system, antennas, transmitter and receiver is based on the use of microwave IC technology. The bistatic antennas are fabricated in PC form. The modulating and analog processing circuitry is assumed to be in IC form. The computed cost range low is \$92.67; the maximum cost computed for the Ku-band radar production system is \$144.95 with an average of

^{12.} R. F. Freiman, "PRICE - A Parametric Cost Modeling Methodology," RCA Government and Commercial Systems, Cherry Hill, NJ, May 1978.

\$112.50. An electromechanical solenoid that is used to control the throttle was also estimated by a description of the size and complexity of the device. The PRICE system predicts a cost range between \$18.48 and \$28.31.

The steering and speed sensor were the final components of the CMS/headway-control system that were cost evaluated. The speed sensor is described as a device that outputs a pulse train at logic voltage levels whose frequency is a function of velocity. The steering wheel sensor is a geared potentiometer attached to a steering arm on the front wheel. Based on a description of the function of both sensors and the approximate size of each unit, the sensors have a predicted production cost of \$7.06 to \$10.89. The assembling of the overall systems and testing is computed by PRICE to be \$10.00 per unit.

The production cost of the complete CMS/headway-control system (excluding braking system) ranges from \$147.26 to \$228.51. The average \$177.00 figure is based on a production run of 100,000 units.

SECTION IX

CONCLUSIONS AND RECOMMENDATIONS

The present effort under DOT sponsorship has contributed greatly to establishing the viability of the radar concept for automotive applications. Truly promising results have been obtained with a radar-controlled collision-mitigation system. With the help of tape recordings of a large number of traffic, road, and weather conditions, a systematic approach to the optimization of the hard-and software of the radar-controlled safety system has been made possible. The importance of these tests lies in the recording of raw radar data that permit a thorough comparative study of how different signal-processing techniques affect the false alarm rate while, at the same time, giving valuable information about the minimum detection distance and the speed with which a proper alarm (output to initiate antiskid braking) is being generated from experimental targets of various cross sections.

With the present system adjusted for practically no false alarms, a target as small as 1 m^2 is recognized at a distance of at least 23 m, and braking is initiated if the closing rate is high enough to make a severe collision unavoidable. In a car traveling 25 m/s (55 mph) against a fixed object, this action results in a reduction of crash energy by $\sim45\%$, an amount that can be very significant with respect to the injuries sustained by the car's occupants. Obviously such a system does not provide the full solution to crash survivability but, if combined with other means such as car structures with higher impact tolerance and use of airbags, a substantial societal savings can be achieved.

It also has to be realized that the system discussed here represents only a feasibility demonstration of the present state-of-the-art; further work in radar processing certainly could still increase the minimum detection range to around 30 m while keeping false alarms in check. Some of the desirable improvements that are considered feasible, but were not implemented during this program, are a further reduction in size of the antenna by using higher frequencies and the introduction of range gate processing to reduce weather interference and multiple-target problems. Also, it can be assumed that further progress in signal processing can be made to increase the safety margin against false alarms.

Aside from the collision-mitigation safety aspects, the present DOT program also addressed two other important areas, an electronic display as driver

aid and automatic cruise/headway control. The final high-technology version of the RSV was equipped with an alphanumeric display which presents driving-related data as well as a series of warning messages if a vital part of the car malfunctions. The display system corresponds closely to the one developed originally during Phase II of the program and includes some refinements and additions, among others a conversion to metric readouts of all measured parameters.

The final version of the high-technology RSV was also to have an automatic cruise/headway control using the existing radar. Since a suitable RSV test vehicle was not available in time, the development of this system was carried out exclusively with RCA-owned station wagons. An experimental system was successfully developed and the algorithm optimized for operation on typical limited access highways using a noncooperative Ku-band FM/CW radar identical in design to the one used in the RSV for collision mitigation.

The cruise/headway control operates either in standard cruise control or automatically switches to a safe headway spacing mode when a vehicle in front is driving at a slower speed than the chosen cruising speed. Since the spacing between cars by the radar system can be maintained considerably more accurately than can be achieved by average drivers, such a system holds promise to provide a better throughput on highways while reducing the common safety hazards of bunching and tailgating. In addition, such a system can be expected to add greatly to the overall sales appeal of the radar and enhance the driver's convenience.

Duplicates of the hard- and software of the cruise/headway-control system were prepared for the RSV but could not be included and fully optimized because of time and certain compatibility problems. A proposal is presently being submitted for a subsequent joint effort between Minicars, Dubner Computer Systems, and RCA to solve the compatibility problems and include the headway control in the final RSV. The high-technology RSV will be returned to RCA at a future time after installation of an antiskid brake system, a new dashboard, and an improved electronically controlled transmission for the final incorporation of the radar and the above-mentioned joint effort.

While substantial progress has been made during this program to show the basic feasibility of cruise/headway control under real, every day traffic conditions, it must be realized that a large amount of work still remains to be done before such a system can be implemented in passenger cars. First, low-g

proportional braking should be included to handle most of the frequently occurring situations where a slightly faster deceleration is needed than can be obtained from engine braking alone; second, radar improvements such as recommended above for the collision-mitigation system (smaller antenna and multiple target resolution) would further enhance the system's versatility; and third, the question of the stability of long columns of cars (under study for some time with the driver as part of the feedback loop) will have to be looked at under the special conditions and restrictions of radar headway control.

Finally, we want to suggest that the time has come to take a serious look at the benefits that radar can add to the automotive environment. Plans for fabrication of a limited number of systems should be initiated to permit a more detailed and thorough testing of the concepts discussed here under actual road conditions by average drivers. Extensive road tests on many cars for a prolonged period of time would certainly be required before a radar-based system could be considered by the rule-making body of the government.

APPENDICES

APPENDIX A

COVERAGE PATTERN CALCULATIONS

A. BISTATIC Ku-BAND RADAR

Statement of the Problem

To determine the detection area of the Ku-band radar, contours of constant power were calculated. An ideal bistatic radar above a ground plane was assumed. The target was assumed to be an isotropic point source. Based on the above assumptions, the power, P_r , returned to the radar becomes

$$P_{r} = \frac{P_{T} G_{\phi}(\phi_{1}) G_{\phi}(\phi_{2}) \lambda \sigma P_{m}}{(4\pi)^{3} R_{1}^{2} R_{2}^{2}}$$
(A-1)

where.

 ϕ_1 = Azimuth angle between transmit antenna and target

 ϕ_2 = Azimuth angle between receive antenna and target

 G_{ϕ} = Antenna azimuth gain function

 $\dot{\lambda}$ = Wavelength in free space

P_m = Multipath factor

 R_1 = Distance from transmit antenna to target

 R_2 = Distance from receive antenna to target

A typical configuration defining the coordinate system is shown in Figure 10 in the main body of the report. The transmit and receive antennas are located at $(S_0/2, 0)$ and $(-S_0/2, 0)$, respectively, and the target is located at (x, y). The radar and target are at the same height above ground. From Figure 10, R_1 and R_2 are given by

$$R_{1} = \sqrt{(x - \frac{S_{0}}{2})^{2} + y^{2}}$$

$$R_{2} = \sqrt{(x + \frac{S_{0}}{2})^{2} + y^{2}}$$
(A-2a)

$$\phi_1 = \tan^{-1} \frac{\frac{S_0}{2} - x}{v} \tag{A-2b}$$

$$\phi_2 = \tan^{-1} \frac{\frac{S_0}{2} + x}{y}$$
 (A-2c)

The multipath factor, P_{m} , is given by [6]

$$P_{m} = \left\{ (1-P)^{2} + 4P \sin^{2} - \frac{2\pi h_{1}h_{2}}{\lambda R} \right\}^{2}$$
 (A-3a)

where R = mean

 $R = mean range, (\frac{1}{2}(R_1 + R_2))$

$$P^{2} = \frac{G_{\theta}(\theta_{2})}{G_{\theta}(\theta)} |\Gamma|^{2}$$
 (A-3b)

 $|\Gamma|$ = reflection coefficient of the road ~ 0.5

 h_1 = radar height above ground

 $h_2 = target height above ground$

 $\frac{G_{\theta}(\theta_2)}{G_{\theta}(\theta)}$ = relative gain of multipath component

 $\mathbf{G}_{\boldsymbol{\theta}}$ = antenna elevation gain function

 θ = elevation angle between antenna and target (0 degrees)

 $\boldsymbol{\theta}_2$ = elevation angle between antenna and ground

Assuming the mixer to be linear, the output of the mixer P_r is proportional to P_r . Since only the relative variations in power level are significant and not the absolute power levels, P_r can be written as

$$P_{r}' = \frac{G(\phi_{1}) G(\phi_{2}) P_{m}}{R_{1}^{2} R_{2}^{2}}$$
 (A-4)

Similarly, the output, $P_r^{\ \prime\prime}$ of the preamplifier is

$$P_{r}'' = P_{r}' \left| H_{HP}(f) \right|^{2} \tag{A-5}$$

and the output of the postamplifier $P_r^{\ \prime\prime\prime}$ is

$$P_{r}^{\prime\prime\prime} = P_{r}^{\prime\prime} \left| H_{LP}(f) \right|^{2} \tag{A-6}$$

where $|H_{HP}(f)|^2$ = preamplifier gain function $|H_{LP}(f)|^2$ = postamplifier gain function f = IF frequency

2. Mathematical Models

a. Multipath

The mathematical model of the multipath is given in equations (A-3a) and (A-3b). Since the target and radar are at the same height (h = 0.67 m), θ is zero and θ_2 is

$$\Theta_2 = \tan^{-1} \frac{2h}{R} \tag{A-7}$$

Experimentally, $|\Gamma|$ has been found to be approximately 0.5. Knowing the gain function, G_A , the multipath is also known as a function of distance.

b. Antenna

The gain function of the antenna is modeled as

$$G = G_{H}(\phi, \Theta) G_{V}(\phi, \Theta)$$
 (A-8)

with

 $G_{
m H}$ = gain function corresponding to a horizontal 32-element linear array of dipoles with a Chebyshev illumination function to realize -30-dB side lobes.

 $G_{
m V}$ = gain function corresponding to a vertical 16-element linear array of dipoles with a Chebyshev illumination function to realize -20-dB side lobes.

The array function $\psi_H(x_H)$ or $\psi_V(x_V)$ for a Chebyshev distribution can be written as [7]

$$\psi_{\rm H}(x_{\rm H}) = \frac{T_{\rm nH}^2 (a_{\rm H}^2 x_{\rm H})}{T_{\rm nH}^2 (a_{\rm H}^2)} \tag{A-9}$$

$$T_n(\mu) = \cos(n \cos^{-1}\mu) \quad \mu \le 1$$

 $T_n(\mu) = \cosh(n \cosh^{-1}\mu) \quad \mu \ge 1$ (A-10a)

$$x_{\text{H}} = \cos\left(\frac{\pi S_{\text{H}}}{\lambda} \sin\phi \cos\theta\right)$$
 (A-10b)

 S_{H} = horizontal dipole spacing

$$a_{\rm H} = \cosh \frac{1}{n_{\rm H}} \cosh^{-1} r_{\rm H} \tag{A-10c}$$

r_H = ratio of peak field to side-lobe field for horizontal array (e.g., for 30-dB side lobes r = 31.62).

 $n_{\rm H}$ = number of elements in horizontal array -1

 ψ_{vy} is derived from a parallel development with H replaced by V

and
$$X_V = \cos \left[\frac{\pi S_V}{\lambda} \sin \theta \right]$$

The effect of the ground plane is taken into account by the method of images; the ground plane is replaced by a dipole of negative polarity and spaced a half-wavelength from the given dipole. In effect one has a two element array of out-of-phase current elements $\lambda/2$ apart.

$$G_{H} = D \psi_{H}$$

$$G_V = D \psi_V$$

where D is the element directivity function with ground plane

$$D = \cos \Theta \sin \left[90^{\circ} \cos \Theta \sin \phi\right] \tag{A-11}$$

Equations (A-10) and (A-11) are sufficient to calculate the azimuth and elevation gain functions.

Preamplifier

Since only normalized values of the return power are significant, the magnitude of the gain will be unity and only the shaping will be specified.

A maximally flat high pass filter response, $\left|H_{HP}(f)\right|^2$, was used to represent the shaping. That is,

$$\left| \frac{H}{HP}(f) \right|^2 = 1 + \left(\frac{f_c}{f} \right)^{2N}$$
(A-12)

where $f_c = \text{cut-off frequency}$

f = frequency at which response is measured

N = number of filter sections

For a stationary target, the range is proportional to frequency, so that equation (A-12) can be written as

$$\left| H_{HP}(R) \right|^2 = \left(1 + \frac{R_c}{R} \right)^{2N} \tag{A-13}$$

where

$$R = \frac{f}{1.302} m$$
 (A-14)

d. Postamplifier

The gain of the postamplifier $\left|\mathbb{H}_{LP}(f)\right|^2$ will also be represented by the shaping; a low pass maximally flat response

$$\left| H_{LP}(f) \right|^2 = \left(1 + \frac{f}{f_c} \right)^{2N} \tag{A-15a}$$

As in the preamplifier, the frequency can be expressed in terms of range and equation (A-14) becomes

$$\left| H_{LP}(R) \right|^2 = \left(1 + \frac{R}{R_c} \right)^{2N}$$

3. Calculated Results

Power contours at the output of the mixer P_r ', at the output of the preamplifier P_r '', and at the output of the postamplifier P_r ''' were computed using the above models. The results are shown in Figures A-1 through A-3. Because of reflection symmetry about the y axis, only the results for the positive x axis were computed.

```
FCL,N1,FCH,N2=1,1,1,1,1
                                 DDDDDDDDDD
 100- • EEEEEEEEEEEEEEEEEE
                                             CCC
                                 DDDDDDDDD
                                             CCC
    • EEEEEEEEEEEEEEE
                                 DDDDDDDDDD
                                             CCCC
    • EEEEEEEEEEEEEEEE
                                            CCCCC
                                 DDDDDDDDD
    •EEEEEEEEEEEEEEEE
     • EEEEEEEEEEEEEEEEE
                                 DDDDDDDDD
                                           CCCCC
  90- •EEEEEEEEEEEEEEEE
                                DEEDDEEDD
                                           CCCC
     • EEEEEEEEEEEEEEEEEE
                                DDDDDDDD
                                          CCCC
     • EEEEEEEEEEEEEEEEEE
                               DDDDDDDD
                                         CCCC
    • EEEEEEEEEEEEEEEEE
                               DDDDDDD
                                        CCCC
                                              BB
    •EEEEEEEEEEEEEEEEE
                              DDDDDDD
                                        CCCC
                                             BBB
                              DDDDDDD
  80- • EEEEEEEEEEEEEEEEE
                                       CCCC
                                             BBB
                             DDDDDDD
                                      CCCC
                                            BBB
    • EEEEEEEEEEEEEEEE
                             DDDDDDD
                                     CCCC
                                           BB
    • EEEEEEEEEEEEEEEE
                                              AA
                            DDDDDDD
                                    CCCC
                                          BB
                                             ĤĤĤ
    • EEEEEEEEEEEEEEEEE
                           DDDDDDD
                                   CCC
                                        BBB
                                            AAAA
     · EEEEEEEEEEEEEEE
  70- • EEEEEEEEEEEEEEE
                          DDDDDD
                                  CCC
                                        BB
                                           AAAAAA
                         DDDDDD
                                 CCCC
                                       BB
                                          AAAAAAA
                                CCC
                                     BB
    • EEEEEEEEEEEEE
                        DEDEDE
                                        AAAAAAAAA
                       DDDDDD
                               CCC
                                    BB
                                       AAAAAAAAAA
    • EEEEEEEEEEE
                     DDDDDDD
                             CCC
    *EEEEEEEE
                                  RR
                                     - AAAAAAAAAAAAA
  60- .EEE
                   DDDDDDD
                            CCCE
                                 BBB
                                     AAAAAAAAAAAAAAA
Ε
                 DDDDDDDD
                          CCCC
                                BB
                                   Axial Range,
                         CCC
               DDDDDDDD
                              BB
                                  AAAAAAAAAAAAAAAAAA
             DDDDDDDDDD
                        CCCC
                             BB
                                 DDDDDDDD
                        CCC
                             BB
                                AAAAAAAAAAAAAAAAAAAAAAAA
                DDDDDD
                        CCC
                            BB
                               AAAAAAAAAAAAAAAAAAAAAA
  50-
    *EEEEEEEE
                  DDDDDD
                        CC
                            BB AAAAAAAAAAAAAAAAAAAA
                    DDD
                         CC BB AAAAAAAAAAAAAAAAAAAAAAAA
       EEEEEEEEEE
              EEEEE
                     DDD
                         .FFFFFF
                EEEE
                      DD
                         C
                            Béééééééééééééééé
    .FFFFFFFFF
                  EEE
                      DD
                         C Baaaaaaaaaaaaaaaaaaaaaaa
         FFFFFF
                  EEE
                      DD C BAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA
            FFFF
                  EEE DD C
                          FFFF
                     EE
                  30--
    .FFFFFF
             EE
                 EEE DD СВАААААААААААААААААААА
             .GGGGG
              Ε
                  20- • GGGGG
           FF E
                   ΑΛΑΑΑΑΑΑ ΑΑΑΑΑΑΑ ΑΑΑΑΑΑΑ
          AA B AAAA AA AA AA
       GGG FED
                                    AA
                                       AAA AAA
                                               Ĥ
        G FEAD BABB AA BBAAA BBAAAA B A AA BAA
                                        Ĥ
                                               Ĥ
        GE CB
               AB BAAB BAAABB AA BBAAA BB A A BBA
                                              Ĥ
    .HH BED ACABC ABC A CC A C AA
                                AAB
                                    A AB BA AB BAB
    .HH FEED C
                  CCAC
                      ACC BCC
                             CC A CC
                                     BCCB
    . CF DA DADB CA CCACCC
                          Α
                            CAC CABC
                                     B
                                       C
                                          Б
                                            B
    .DEFFDC
                   C D CD CDDBA
                               ACC B
                                     AB CC
                                           BBAAAA
     0
                               3
                                       Δ
                                                5
                                 Offset, m
```

FIGURE A-1. CALCULATED DETECTION PATTERN (NO SHAPING).

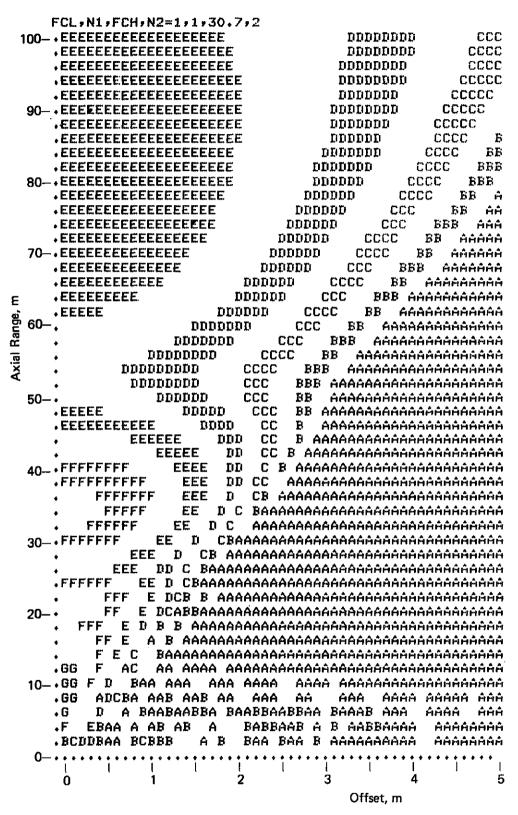


FIGURE A-2. CALCULATED DETECTION PATTERN (HIGH-PASS: 1 SECTION, CUTOFF AT 30.7 m).

```
FCL, N1, FCH, N2=32, 2, 5, 15, 4, 2
100- •
           .BBBBBBB
                90-.BBBBBBBBBBBBB
                 .88888888888888888
                 .BBBBBBBBBBBBBBBBBBB
                  AGGGGGGGGGGGGGGGGGGGGGGGG
  .88888888888888888888
                  AAAAAAAAAAAAAAAAAAAAAAAA
80-
      BBBBBBBBBBBBBBBB
                   BBBBBBBBBBBBB
                   BBBBBBBBBB
                   BBBBBBBBBB
                   BBBBBBBBB
                   70-
           BBBBBBBB
                   AAAAAAAAAAAAAAAAAAAAAAA
            BBBBBBBB
                  AAAAAAAAAAAAAAAAAAAAAAAAAA
            BBBBBBB
                  ARMARARARARARARARARA
Ε
  .CC
                  BBBBBB
Axial Range,
  . CCC
           BBBBBBB
                 60-.ccc
           BBBBBB
                 BBBBBB
                BBBBBB
                .ccccc
          BBBBBB
                .ccccccccc
           BBBB
                50-+CCCCCCCCCCCC
            BBB
                cccccc
              BBB
                .DDDDDDDDDDD
           CCCC
              BB
                 DDDDDDD
            CC
               В
                 · EEEEEEEE
          DDD
             CC
               В
                 CC
     EEEEEEE
           ppp
               40- •
        EEEE
              C
               Bádadadadadadadadadadada
  .FFFFFFF
           DD
              C Béanaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaa
         EEE
  .FFFFFFFF
         EEE
           .FFFFFFFF
          DD C
              30- FFFFFF
        EE
          IJ
           .FFFF
         DD C
            D
           E DDCBA
            + GGG
      20- . GGGG
        FF E
         FF EDAC
          ann.
  . GGG
     F E CC AA
           AAAAA AAAAA
      EA CBA B AAA
             AAAA
                AAAA
                   AAAAAA
  · GGG
 10- · GG
     DD A BAA B AA B AAA BAAAA
                    AAAAA
         BA
           BAABBAA BBAA B AA BBAAA B AAA B A
       ABA
   GFE DCAB AA
           AB
               AA
                 AAB
                    Ĥ
                     BAAABB AAABBAA
              Α
     AACACA BA BBABBB
                A
                 BAB BAA
                      AA BBA
      В
         C CBC BBCA C AAB BA
                        BBB
                  3
                             5
                    Offset, m
```

FIGURE A-3. CALCULATED DETECTION PATTERN (LOW PASS: 4 SECTION, $R_c = 32.2 \text{ m}$; HIGH PASS: 1 SECTION, $R_c = 15.4 \text{ m}$).

The target location varied from 2 to 100 m in the axial direction and 0 to 5 m in the x direction. Letters ranging from A to H are used to represent the relative power received from a target located at that letter position. The power levels increase from A to H in approximately 10-dB steps, and each letter ranges in value about 5 dB.

For the calculation P_r '', the cutoff range was specified as 30.7 m and the slope was 6 dB/octave. For the calculation of P_r ''', the high and low pass filter cutoff frequencies (ranges) were taken from the measured composite preamplifier and postamplifier characteristics. From Figure 15, the high pass filter was modeled as a single-section filter with cutoff at 15.4 m. Similarly, the low pass filter was modeled, as a four-section filter with cutoff at 32.2 m. Using the composite filter characteristic takes into account the interaction when the preamplifier is integrated with the postamplifier.

Comparisons between the calculated and measured contours of P_r '' show good agreement if letter E of Figure A-2 is the -40 dB level, shown in Figure 11. Similarly for P_r ''', when letter F of Figure A-3 is the -15 dB level shown in Figure 12, Figure A-3 demonstrates the range containment that can be achieved by shaping the postamplifier.

B. MONOSTATIC COOPERATIVE X-BAND RADAR

1. Tagged Channel Operation

The detection area of the cooperative X-band radar was also determined from contours of constant power. The power returned to the radar is calculated in a two-step process. First the power received by the tag is formulated and then this power is considered to be reradiated back to the radar. That is

$$P_{TAG} = \frac{P_T G_R G_T \lambda^2}{(4 \pi R)^2} \sqrt{P_m}$$
 (A-16)

$$P_{R} = \frac{L P_{TAG} G_{R} G_{T} \lambda^{2}}{(4 \pi R)^{2}} \sqrt{P_{m}}$$
 (A-17)

From equations (A-16) and (A-17)

$$P_{R} = \frac{L P_{T} G_{R}^{2} G_{T}^{2} \lambda^{4}}{(4 \pi R)^{4}} P_{m}$$
 (A-18)

where

L = loss in modulator

 G_R = antenna gain of radar

 G_{T} = antenna gain of tag

When $G_R = G_T = G$

$$P_{r} = K \left(\frac{G}{R}\right)^{4} P_{m} \tag{A-19}$$

$$K = \frac{L P_T \lambda^4}{(4\pi)^4}$$
 (A-20)

The factor K is normalized to unity for the calculation of the power contours as before and P_{m} is given by equation (A-3). The geometry of the radar and tag for a typical power calculation is shown in Figure A-4. From the figure, the distance to the tag R, is given by

$$R = \sqrt{x^2 + y^2 + (h_1 - h_2)^2}$$
 (A-21a)

The azimuth angle ϕ is given by

$$\phi = \tan^{-1} \frac{x}{y} \tag{A-21b}$$

and the elevation angle θ

$$\theta = \sin^{-1} \sqrt{\frac{h_1 - h_2}{x^2 + y^2 + (h_1 - h_2)^2}}$$
 (A-21c)

The multipath angle θ_2 is

$$\theta_2 = \tan^{-1} \frac{h_1 + h_2}{\sqrt{x^2 + y^2}}$$
 (A-22)

 h_1 = height of radar above ground = 0.675 m

 h_2 = height of tag above ground = 0.385 m

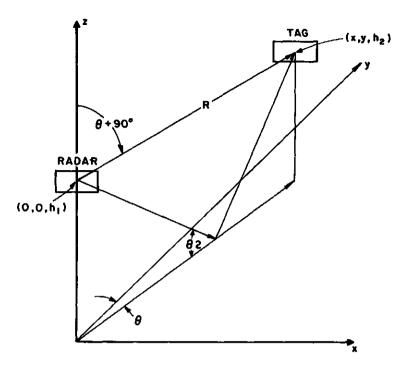


FIGURE A-4. COOPERATIVE RADAR-TAG GEOMETRY FOR COVERAGE PATTERN MEASUREMENTS.

The power contours are calculated at the output of the detector P_r '' and at the output of the postamplifier, P_r '''. (See Figure 16.) The output of the detector P_r '' is given by

$$P_{r}^{\prime\prime} = \left(\frac{G}{R}\right)^{4} P_{m} \tag{A-23}$$

Equation (A-23) assumes a linear detector and a flat response from the preamplifier at the tag modulation frequency. The output of the postamplifier $P_r^{'''}$ is given by

$$P_{r}^{\prime\prime\prime} = \left(\frac{G}{R}\right)^{4} P_{m} \left| H_{LP}(f) \right|^{2}$$
(A-24)

where $|H_{LP}(f)|^2$ = gain function of the postamplifier.

The amplitude of the gain is normalized to unity and the shape is given by a maximally flat filter response as in subsection A.2.c above.

2. Mathematical Models

a. Multipath

The same model is used as in subsection A.2 above with the following changes: θ is given by equation (A-21c) and θ_2 by equation (A-22).

b. Antenna

The gain function of the antenna is modeled as $G = G_H(\phi, \Theta)$ $G_V(\phi, \Theta)$ as before. However, the side lobe-level is only -20 dB in azimuth and elevation, and the number of elements is reduced from 32 x 16 to 16 x 8 to approximate the antenna used at X-band.

The elevation gain G_V (Θ), is taken into account, with Θ given by equation (A-21c).

c. Preamplifier

The preamplifier is modeled as a high pass filter of unit gain. At the tag modulation frequency and over the signal bandwidth, the preamplifier is assumed to be operating in its passband so that $\left|\mathbb{H}_{HP}\right|^2 = 1$.

d. Postamplifier

The postamplifier is modelled as a single-section, low-pass filter with range frequency cutoff at 50 m. For example,

$$|H_{LP}(R)|^2 = \left(1 + \frac{R}{R_c}\right)^2$$

$$R_c = 50 \text{ m}$$
(A-25)

3. Calculated Results

Figure A-5 shows contours of constant power as measured at the output of the detector of the tagged channel; no shaping was used. These results are in good agreement with the measured results shown in Figure 18, when letter E of Figure A-5 is compared with the -50 dB contour of Figure 18.

Figure A-6 shows the beam confinement when a postamplifier with a shape factor corresponding to a single-section, low-pass filter is used. The cutoff range is 50 m. The output is taken at the postamplifier. Even with the simple filter, the maximum range associated with the letter E is reduced from 68 m to 58 m. Measurements were not taken at the output of the postamplifier so that comparisons cannot be made.

A fortunate departure between the measured and calculated results is the extent and depth of the multipath null. The measured results indicate that the null is not as broad or as deep as the calculated results. This may be due to the nonideal nature of the tag; i.e., it is not a perfect reflector

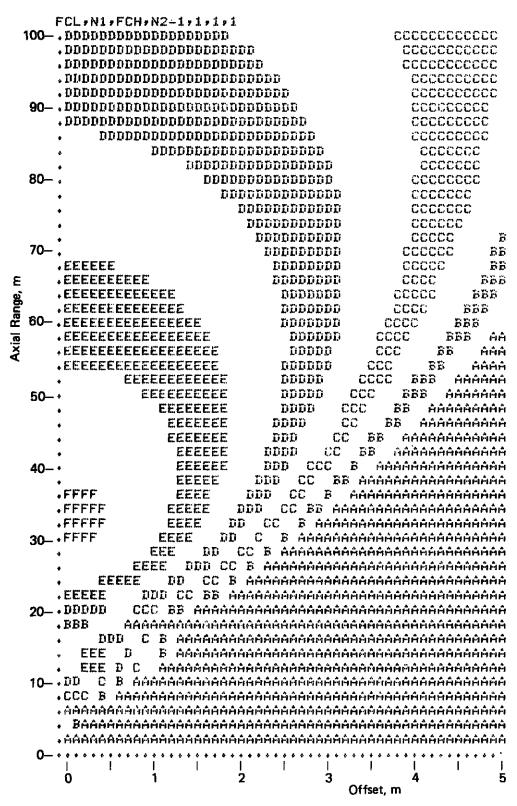


FIGURE A-5. DETECTION PATTERN FOR COOPERATIVE RADAR (OUTPUT OF DETECTOR).

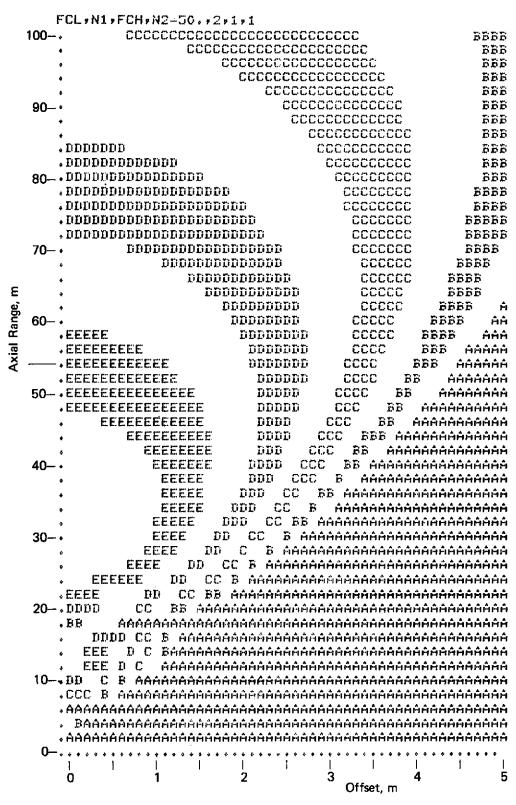


FIGURE A-6. DETECTION PATTERN OF COOPERATIVE RADAR (OUTPUT OF POSTAMPLIFIER).

whose radiation pattern is unaltered by the modulator as a termination. Also, the nonideal nature of the road surface contributes to a flattening of the null.

C. MONOSTATIC NONCOOPERATIVE X-BAND (BASEBAND OPERATION)

The baseband channel of the X-band radar can be treated as a special case of the bistatic radar discussed in Section A, with $S_0=0$. The only other changes required are in the physical constants such as the number of antenna elements and side lobes and the amplifier cutoff ranges. From equation (A-4)

$$P_{r}' = \frac{G^2(\phi) P_{m}}{R^4}$$
 (A-25)

where

$$\phi = \tan^{-1} \frac{x}{y}$$

R = distance from radar to target

Similarly,
$$P_r'' = P_r' \left| H_{HP}(f) \right|^2$$

and $P_r''' = P_r'' \left| H_{LP}(f) \right|^2$

where $|H_{HP}(f)|^2$ is modeled by equations (A-12) and (A-13). The conversion from frequency to range is different at X-band due to the different modulation parameters so that equation (A-14) becomes

$$R = \frac{f}{0.667} m$$
 (A-26)

with f expressed in kHz. Similarly, the postamplifier is given by equations (A-15a) and (A-15b).

Contours of the power out of the preamplifier are shown in Figure A-7. The preamplifier was modeled as a single-section high-pass filter, with cutoff at 50 m. The antenna was modeled as a 20-dB side-lobe Chebyshev array with 16 x 8 elements. The contour represented by the letter E has a maximum range of 80 m and an axial offset of 2.7 m. The multipath null extends from 30 to 36 m. This contour approximates the -60 dB contour shown in Figure 11. The measured results show the maximum range to be about 90 m and the axial offset to be about 3 m. The measured multipath null extends from 31 to 41 m.

If one keeps in mind the large number of approximations and simplifying assumptions that have to be taken in the calculation of these antenna patterns,

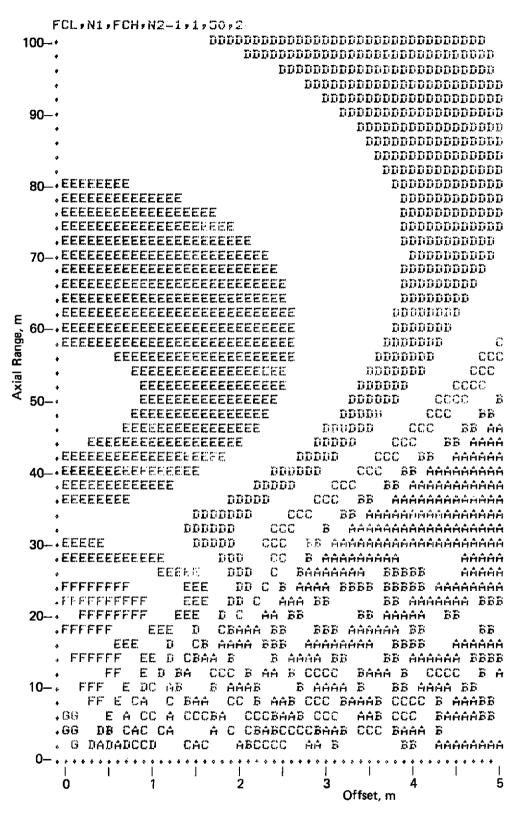


FIGURE A-7. DETECTION PATTERN OF MONOSTATIC, X-BAND, NONCOOPERATIVE RADAR (OUTPUT OF PREAMPLIFIER).

the agreement between theory and measured results is quite good. The computer solution presented here thus can be used to predict with reasonable accuracy other situations not treated here.

APPENDIX B

SOFTWARE LISTING FOR CMS ALGORITHM

```
0000
                                                                          RCA LABS 10:16:79
0000
                                                  > CMS3
                                      2 ...
                                                  CDP1802 MICROPROCESSOR VERSION
FOR RSV CAR
DEVIATION, SPEED, STEERING WHEEL ANGLE
                                      ā ..
0000
                                      4 ...
0000
0000
                                     5 ...
                                     6 ..
7 ..
0000
                                                  CHECK
0000
                                      8 ..
                                                  THIS VERSION IS EQUIVALENT TO CMS1 NO SWITCHES ARE USED
0000
0000
                                      9 ..
                                    10 ...
0000
0000
                                                  STACK=#10FF
0000
                                    12
                                                  UPBUF = #1000
0000
                                    13
                                                  DNBUF=#1030
                                    14 ...
0000
0000
                                    15 ...
0000
                                    16 ...
0000
                                                  VAR=#1060
                                                  V= VAR
UCOUNT= VAR+2
0000
                                     18
0000
                                    19
0000
                                    20
                                                  DCOUNT= VAR+4
0000
                                    \overline{21}
                                                  NUP=VAR+6
                                                  NOP=VAR+0
NDN=VAR+8
TEMP1=VAR+10
TEMP2=VAR+12
                                    22
9999
                                    \overline{23}
0000
                                    \overline{24}
0000
                                    25
                                                  TEMP3= VAR+14
0000
                                    \overline{26}
0000
                                                  DOPRR= VAR+ 16
0000
                                    27
                                                  DOPRR1=VAR+18
0000
                                    28
                                                  DOPRRO = VAR+20
                                                  RRDV2= VAR+22
RANCE= VAR+24
RANCE0= VAR+26
0000
                                    \overline{29}
9999
                                    30
0000
                                    31
                                                  TVAL= VAR+28
AVGUCT= VAR+30
0000
                                    32
0000
                                    33
0000
                                    34
                                                  AVGDCT= VAR+32
0000
                                    35
                                                  FLAC= VAR+34
                                                  FLAG1=VAR+35
FLAG2=VAR+37
0000
                                    36
0000
                                    37
0000
                                    38
                                                  FLAG3=VAR+39
0000
                                    39
                                                  LOLIM= VAR+41
0000
                                    40
                                                  UPLIM= VAR+43
                                    41 ...
0000
                                    42 ...
0000
                                    43 ...
0000
9999
                                    44
                                        . . .
0000
                                                   ORC 0
                                    45
0000
                                    46
                                        . .
0000 F800B3
0003 F800A3
0006 D3
                                    47
                                                  A. 1(NEWPC) -> R3.1
                                    48
                                                  A. 0(NEWPC) -> R3.0
                                    49 GO STATE R3 ..R3 IS PC
50 NEWPC: A.1(STACK) -> SP.1
51 A.0(STACK) -> SP.0
0000 D3
0007 F810B2
000A F8FFA2
000D E2
000E F80FB4
                                    52
                                                  SEX SP
                                    53
                                                  A. 1(CALLS) -> R4. 1
```

```
0011 F85EA4
                                                                          A. 0(CALLS) -> R4. 0
                                                                          A. 1 (RETR) -> R5.1
A. 0 (RETR) -> R5.0
0014 F80FB5
0017 F86EA5
                                                      55
                                                      56
                                                                          OUT 5; DEC SP .. TURN OFF MEAS. CIRCUIT
 001A 6522
                                                      57
 001C
                                                      5Ř
001C F800BA
001F F800AA
0022 D4000
0025 D40F8CFFFF
                                                     58 ...
59 START: A.1(SYSAC)->AR.1
60 A.0(SYSAC)->AR.0
61 CALL DISP
62 CALL DELAY; ,#FFFF
62 CALL DELAY; ,#FFFF
                                                     63 CALL DELAY; , *FFFF ... ABOUT 3 SECS 64 CLEAN: A.1(FLAG3) -> AR.1 65 A.0(FLAG3) -> AR.0
002A D40FBCFFFF
002F F810BA
0032 F887AA
0032 F887AA
0035 4A
0036 3200
0038 F88052
003B 6122
003D F80052
0040 6622
0042 F810BA
0045 F882AA
0048 F800
                                                      66
67
                                                                          LDA AR
BZ CLEN
                                                                          #80->@SP
OUT 1;DEC SP ..CLEAR DISPLAY
                                                      68
                                                      69
70
71
                                                             CLEN: 0->@SP
                                                                          OUT 6; DEC SP ... TURN OFF WARNING A. 1 (FLAG) -> RA. 1
                                                      72
                                                      73
                                                                          A. 0(FLAC) -> RA. 0
                                                                           LDI 0
                                                                            STRA ...FLAC=0
INC AR; STRA ...FLAG1=0
 004A 5A
                                                      75
                                                     75
76
1NC A...
77
78 FIRST: CALL DELAY; , 0, 1
79
A.1(FLAG3) -> AR. 1
A.0(FLAG3) -> AR. 0
-> GAR
EF1
 004B 1A5A
 004D
 004D D40F8C0001
0052 F810BA
0055 F887AA
0055 F867AA
0058 F8005A
005B 3C2F
005D 7B
005E D40000
                                                      82
                                                                          BN1 CLEAN ..EF1=1 SPEED SPEED CUTOFF
                                                      83
                                                                          SEQ
                                                      84
                                                               LOOK: CALL GETRAN
                                                                                                         ...ACQ. DATA, DEVIATION CHECK
0061 3B2F
0063 3D2F
0065 7A
                                                                          RNF CLEAN
                                                      86
                                                                          BN2 CLEAN...EF2=1 S.W. ANGLE>NUM.NG
                                                      87
                                                                          REQ
 0066
                                                      នន
0066
                                                      89
0066 D40E491070
006B D40C2D0000
0070 9FFA80CA0000
0076 FB10BA
                                                              CAON: CALL LOADOP; , A(DOPRR)
CALL SMOP; , A(RRTHR)
AC.1. AND. #80; LBNZ NOALR1
A.1(FLAG) -> AR.1
A.0(FLAG) -> AR.0
                                                      90
                                                      91
                                                                                                                                ... RR> RRTHR
                                                      92
                                                      93
0079 F882AA
007C F8805A
007F 1A4AC20000
                                                                         A.O(FLAG) -> AR.O
LDI #80; STR AR ...FLAC=80
INC AR; LDA AR; LBZ NOALAR ...FLAG1=0-> N
CALL LOADOP; ,A(DOPRR)
CALL SMOP; ,A(DOPRR)
CALL SMOP; ,A(DELRR) ...-DELRR
AC.1.AND.#80; LBZ NOALAR ...DIFF. RR> DE
CALL LOADOP; ,A(RANGEO)
CALL SMOP; ,A(RANGEO)
CALL SMOP; ,A(RANGEO)
...PRESENT R< PREVIO
AC.1.AND.#80; LBNZ NOALAR
AC.1-> RO.1; AC.O-> RO.O
CALL SMOP; ,A(UPLIM) ...DIFF. RANGE
                                                      94
                                                      95
                                                      96
0084 D40E491070
0089 D40C2D1072
008E D40000
                                                      97
                                                      98
                                                      99
0091 D40C2D0000
0096 9FFA80C20000
009C D40E49107A
                                                     100
                                                     101
                                                     102
 00A1 D40C2D1078
                                                     103
00A6 9FFA80CA0000
00AC 9FB08FA0
                                                     104
                                                     105
 00B0 D40C2D108B
                                                     106
00B5 9FFA80C20000
                                                     107
```

```
00BB 90BF80AF
00BF D40C2D1089
                                      108
                                                      RØ.1->AC.1; RØ.0->AC.0
                                                      CALL SMOP; A(LOLIN) ...I
AC. 1. AND. #80; LBNZ NOALAR
                                      109
                                                                                        ..DIFF. RANCE>LOLI
    00C4 9FFA80CA0000
                                      110
                                             CALL LOADOP; A(RANGE)
CALL SMOP; A(RCUTOF)
AC.1.AND.#80; LBZ NOALAR
ALARM:1->@SP; OUT 6; DEC SP
    00CA D40E491078
                                      111
    00CF D40C2D0000
                                                                                           .. RANGE < RCUTOF
                                      112
    00D4
           9FFA80C20000
                                      113
                                                        CALL LOADOP; ,A(RANGE)
    00DA F801526622
                                       114
    OODE
          D40E491078
                                      115
                                                      CALL STOROP; A(RANGEO)
CALL LOADOP; A(DOPRR)
CALL STOROP; A(DOPRR)
A. 1(FLAG) -> AR. 1
    00E4 D40E57107A
                                       116
                                                                                             ... RANGE-> RANGE
    00E9 D40E491070
                                       117
    00EE D40E571072
                                                                                             ... DOPRR-> DOPRR
                                       118
    00F3 FB10BA
                                       119
    00F6 F882AA
                                                        A. 0(FLAG) -> AR. 0
                                       120
                                                       LDA AR; STR AR ...FLAC->FLAG1
CALL RANUP ...CALCULATE UPLIM
CALL STOROP;, A(UPLIM) ...UPLIM=.078*DOP
.... DISPLAY SUBRUTINE
CALL MOVE A/MESAVER
    00F9 4A5A
                                       121
    00FB D40000
                                       122
    00FE D40E57108B
                                       \overline{123}
    0103
                                       124
                                             FORMAT: CALL MOVB, A(MESOUT), A(OUTBF), 32
A.1(OUTBF) -> AR.1
A.0(OUTBF+2) -> AR.0
    0103 D40F7A0000000020
                                      125
    010B F800BA
                                      126
127
    010E F802AA
                                                     CALL LOADOP; , A(RANGE)
CALL CVT; , 4, 1
CALL LOADOP; , A(DOPRR)
A. 0(OUTBF+10) -> AR. 0
    0111 D40E491078
                                      128
    0116 D40FA20401
                                      129
    011B D40E491070
                                       130
    0120 FROAAA
                                       131
                                                     T'+'->@AR
    0123 F82B5A
                                       13\overline{2}
                                                     AC.1.AND.#80; BZ CHSIGN
T'-'->@AR
    0126 9FFA803200
                                      133
    012B F82D5A
                                      134
                                      012E D40000
    0131
           1 A
    0132 D40FA20401
    0137
           D40E491060
    Ø13C
           F813AA
                                                    CALL CVT;,2,0
CALL LOADOP;,A(NUP)
A.0(OUTBF+26)->AR.0
    013F D40FA20200
                                      140
    0144
           D40E491066
                                      141
F
    0149
           F81AAA
                                      142
                                                     CALL CVT; ,3,0
A.O(OUTBF) -> AR. 0
    014C D40FA20300
                                      143
    0151 F800AA
                                      144
    0154 D40000
                                       145
                                                     CALL DISP
                                                      CALL LOADOP; , A(FLAG1)
AC. 1. XOR. #80
LBZ CTD
    0157 C0004D
                                       146
                                                                             TO STORE R, RR PUT 3 NOP
    015A D40E491083
                                      147
                                                 .... TO STORE R, RR PUT NOP (C4)
.... STORE R, RR SUBROUTINE
CALL LOADOP;, A(RANGE)
CLO AC; SDI #40
LBDF ZIP
CLO AC, DIT
    Ø15F
           9FFB80
                                      148
    0162 C20000
                                      149
    0165 C0004D
                                      150
    0168 00
                                               CTD: IDLE
                                      151
    0169
                                      152
    0169 D40E491078
                                       153
    016E 8FFD40
                                      154
    0171 C30000
                                      155
    0174 8FB0
                                      156
                                                      CALL LOADOP; , A( DOPRR) GLO AC; PLO RO
    0176 D40E491070
                                      157
    017B 8FA0
                                      158
                                                        CALL LOADOP; A(FLAG2)
GHI ROSTR ACLINC AC
    017D D40E491085
                                      159
    0182 905F1F
                                      160
    0185 805F1F
                                      161
                                                        GLO RO; STR AC; INC AC
```

```
0188 D40E571085
018D C0004D
0190 00
                                                        CALL STOROP; , A(FLAG2) LBR_FIRST
                                     162
                                     163
                                                  ZIP: IDL
                                     164
0191
                                      165
0191
                                                          TURN OFF ALARM SUBRUTINE
                                      166
0191
                                      167
0191 F810BA
                                     168
                                            NOALR1: A.1(FLAG) -> AR.1
A.0(FLAG) -> AR.0
LDI #0;STR AR
...FLAG=0

NOALAR: 0-> @SP; OUT 6; DEC SP
...T
CALL LOADOP; ,A(RANGE)
CALL STOROP; ,A(RANGE)
...R
CALL LOADOP; ,A(DOPRR)
CALL STOROP; ,A(DOPRR)
A.1(FLAG) -> AR.1
A.0(FLAG) -> AR.0
LDA AR:STR AR ...FLAG-> FI
                                             NOALR1: A.1(FLAG) \rightarrow AR.1
0194 FBB2AA
0197 FB005A
                                     169
                                      170
019A F800526622
019F D40E491078
                                                                                                ...TURN OFF ALA
                                      171
                                      172
01A4 D40E57107A
01A9 D40E491070
01AE D40E571072
                                      173
                                                                                                 ..RANGE->RANGEØ
                                     174
175
                                                                                                 ... DOPRR-> DOPRR
01B3 F810BA
01B6 F882AA
                                     176
177
01B9 4A5A
01BB D40000
01BE D40E57108B
                                                                                     ...FLAG->FLAG1
                                                          LDA AR; STR AR
                                     178
                                                          CALL RANUP ... CALCULATE UPLIM CALL STOROP; , A(UPLIM) .. UPLIM=.078*DO
                                      179
                                      180
01C3 C00103
                                      181
                                                          LBR FORMAT
                                                                                     ... BRANCH TO DISPLAY
                                     182
01C6
                                      183
01C6
                                                  ... RANGE DIFFERENCE UPER LIMIT CALCULATION
                                      184
0106
                                     185
                                                    ... UPLIM=.078*DOPRR
01C6
                                      186
                                                RANUP: CALL LOADOP;, A(DOPRR)
CALL MPYOP;, A(DEC5)
A. 1(DEC40) -> MA. 1
01C6 D40E491070
                                      187
01CB D40C4F0000
                                     188
01D0 F800BD
                                     189
                                                     A.0(DEC40) -> MA.0
CALL DIVQ .. UPLIM=1.25*DOPRR
EXIT
01D3 F800AD
                                     190
01D6 D40D5F
                                     191
01D9 D5
                                     192
01DA
                                     193 ..
                                                     > ABSAC
                                                                       J.M.C.
                                                                                       RCA LABS
                                     194 ..
01DA
01DA
                                      195 ....
                                                        COMPUTE ABS VALUE OF AC
01DA
                                     196
                                             ABSAC: AC.1.AND.#80; LBZ ABSEX
AC.0.XOR.#FF+1->AC.0 ..WAS NEG
AC.1.XOR.#FF ..COMPLEMENT IT
01DA 9FFA80C20000
                                      197
01E0 SFFBFFFC01AF
                                      198
01E6 9FFBFF
01E9 3BEDFC01
                                      199
                                                     BNF *+4; +1
-> AC.1
                                     200
01ED BF
                                     201
01EE D5
                                     202 ABSEX: EXIT
                                     203 ...
Ø1EF
                                     204 ...
01EF
01EF
                                     205
                                                      ... FAST VERSION-- OBTAIN VEHICLE SPEED
01EF
                                     206
01EF
                                     207
                                                     . . .
01EF
                                     208
                                     209 DISP:#80->@SP
210 OUT 1; DEC SP ... CLEAR MEMORY
211 8->CR.0
01EF F88052
01F2 6122
01F4 F808AC
01F7 2C8C3AF7
                                                     DEC CR; CR.0; BNZ CLP 32-> CR.0
                                     212 CLP:
01FB F820AC
01FE EAEAEA
                                     213
                                                     SEX AR; SEX AR; SEX AR .. MORE SEX LDA AR; DEC AR .. STALL A WHILE
                                     214 DGO:
0201 4A2A
```

```
CR.0-1->CR.0 ..SLOW DECREMENT LBNZ DGO; SEX SP 1->@SP
    0203 61
                                      216
    0204 BCFF01AC
                                      217
218
    0208 CA01FEE2
    020C F80152
                                      219
                                                     OUT 2; DEC SP ..MAKE SURE IT IS ON EXIT
    020F 6222
                                      220
    0211 D5
                                      221
    0\overline{2}12
                                      222
                                      223 ...
    0212
    0\overline{2}12
                                      224 ...
    0212
                                      \overline{225}
                                                     W=1; X=3; Y=4; Z=5
                                      \overline{226}
    ŏ212
    0212 69FA03FB03
                                      227
                                               GETRAN: INP W; .AND. 3. XOR. 3
    0217 CA0212
                                      228
                                                      LBNZ GETRAN
                                             LBNZ GETRAN
OUT 3; DEC SP ..PRESE'
GET1: INP W;.AND.3.XOR.1
LBNZ GET11
INP Z;.XOR.#FF-2->AC.0
CLRU:ADI 0;LBZ GETX
AC.0;.AND.#80
LBNZ GETX
0->AC.1
                                                                             PRESET STROBE
    021A 6322
                                      229
    021C 69FA03FB01
                                      230 GET1:
    0221 CA0000
                                      231
    0224 6DFBFFFF02AF
                                      232
F
    022A FC00C20000
                                      \overline{233}
    022F 8FFA80
                                      234
F
    0232 CA0000
                                      235
    0235 F800BF
                                      236
                                                       0-> AC. 1
                                                      CALL STOROP; , A(NUP)
LBR PKUP
    0238 D40E571066
                                      237
    023D C00000
                                      238
    0240 FC0069FA04
                                                GET 11: ADI #0; INP W; . AND . 4
                                      239
    0245
                                                      RSHR
                                      240
           76
                                                     LBNZ CET1
INP Z; .XOR. #FF-2->AC. 0
LBR_CLRU
    0246 CA021C
                                      241
    0249 6DFBFFFF02AF
024F C0022A
                                      242
                                      243
                                             PKUP: A. 1(UPBUF) -> RØ. 1
    0252 F810B0
                                      244
    0255 F800A0
                                      245
                                                     A. 0 ( UPBUF) -> R0. 0
                                                     INC AC
INF ';->@RO
INC '
    0258 1F
                                      246
    0259 6B50
                                                                      ..READ FIFO
                                      247
                                            GET2:
    9259 9550
925B 10
925C 6C50
925E 10
925F 2F8FCA9259
                                      248
                                                     INP Y; -> @RØ
INC RØ
                                      249
                                      250
                                                     DEC AC; AC.0; LBNZ GET2
                                      251
    0264
                                      252
    0264
                                      253
                                            . . .
    0264
                                      254
                                      255 GET3: INP W; . AND . 3 . XOR . 1
    0264 69FA03FB01
                                                     BNZ GET3
OUT 3; DEC SP ...PRESET
INP W; AND 3. XOR 3
LBNZ GET 44
INP Z; XOR #FF-2-> AC .0
    0269 3A64
                                      256
    026B 6322
                                      257
                                                                            ..PRESET STROBE
    026D 69FA03FB03
                                            CET4:
                                      258
    0272 CA0000
                                      259
    0275 6DFBFFFF02AF
                                      260
                                             CLRD: ADI 0; LBZ GETX
AC. 0; AND. #80
LBNZ GETX
0->AC. 1
CALL STOROP; , A(NDN)
LBR PKDN
F
    027B FC00C20000
                                      261
    0280 8FFA80
                                      262
    0283 CA0000
                                      263
    0286 F800BF
                                      264
    0289 D40E571068
028E C00000
    0289
                                      265
                                      266
    0291 FC0069FA04
                                               GET 44: ADI #0; INP W; . AND . 4
                                      267
    0296 76
0297 CA026D
                                      268
                                                     RSHR
                                                   LBNZ GET4
                                      269
```

```
029A 6DFBFFFF02AF
02A0 C0027B
                                                       INP Z; .XOR. #FF-2->AC. 0
LBR CLRD
PKDN: A. 1(DNBUF) -> RO. 1
                                             270
                                             271
272
273
02A3 F810B0
                                                                A.O(DNBUF) -> RO.O
INC AC
INP X; -> @RO ..RI
INC RO
02A6 F830A0
02A9 1F
                                             274
275
02AA 6B50
02AC 10
02AD 6C50
02AF 10
                                                    CET5:
                                                                                          ..READ FIFO
                                             276
                                                                 INP Y; ->@RØ
INC RO
DEC AC; AC.
                                             277
                                             278
02B0 2F8F3AAA
                                                                 DEC AC; AC.0; BNZ GET5
A.1(UPBUF)->R0.1
A.0(UPBUF)->R0.0
                                             \overline{279}
02B4 F810B0
                                             280
02B7 F800A0
                                             281
                                                                A.O(UPBUF) -> RO.O
CALL LOADOP;, A(NUP)
DEC AC
CALL AUPDN
CALL STOROP;, A(UCOUNT)
0-> MQ.O, MQ.1
CALL DIVOP;, A(NUP)
CALL STOROP;, A(AVGUCT)
A.1(DNBUF) -> RO.O
CALL LOADOP;, A(NDN)
02BA D40E491066
02BF 2F
                                             282
                                             283
02C0 D40000
                                             284
02C3 D40E571062
                                             285
02C8 F800AEBE
                                             \overline{2}86
02CC D40CA11066
                                             287
02D1 D40E57107E
                                             288
02D6 F810B0
                                             289
02D9 F830A0
                                             290
02DC D40E491068
                                             \bar{2}91
                                                                 CALL LOADOP; , A(NDN)
                                                                DEC AC
CALL AUPDN
CALL STOROP; AC DCOUNT)
02E1
                                             292
02E2 D40000
                                             293
02E5 D40E571064
                                             294
                                                                 CALL STOROF; ACAUGUST)

CALL STOROP; ACAUGUST)
02EA F800AEBE
                                             295
02EE D40CA11068
02F3 D40E571080
                                             296
                                             297
02F8 F800BC
02FB D40E491066
                                             \overline{298}
                                                                   0-> CR. 1
                                                                   CALL LOADOP; , A(NUP)
                                             299
                                                                    CALL LOADOP; ,A(NUP)
AC.0-> CR.0
CALL LOADOP; ,A(DELRAN)
GHI AC; STXD
CLO AC; STXD
CALL LOADOP; ,A(AVGUCT)
GHI AC; STXD
GLO AC; STXD
A.1(UPBUF)-> R0.1
A.0(UPBUF)-> R0.0
0300 BFAC
                                             300
0302 D40E490000
0307 9F73
                                             301
                                             302
0309 8F73
                                             303
030B D40E49107E
                                             304
0310 9F73
0312 8F73
                                             305
                                             306
0314 F810B0
0317 F800A0
                                             307
                                             308
                                                                        @R0!->AC.0
@R0!->AC.0
GLO AC;STXD;INC SP
@R0!->AC.0
031A 40AF
                                             309
031C 40FA0F73
                                             310
0320 8F7312
                                             311
0323 40AF
0325 F5AA
0327 12
                                                       CHKUP:
                                             312
                                                                       SD; -> AR. 0
INC SP
                                             313
                                             314
0328 40FA0FBF
032C 75BA
                                                                      @R0!.AND.15->AC.1
SDB;->AR.1
INC SP_
                                             315
                                             316
032E 12
032F 8AF5AA
0332 12
0333 9A75BA
                                             317
                                             318
                                                                         AR. 0; SD; -> AR. 0
                                             319
                                                                         INC SP
                                                                      AR. 1; SDB ;-> AR. 1
LBDF AH1
                                             320
0336 C30000
0339 BAFBFFFC01AA
033F 9AFBFFFA0F
                                             321
                                                                      AR. 0. XOR. #FF+1-> AR. 0
AR. 1. XOR. #FF. AND. 15
                                             322
                                             323
```

```
0344 7C00BA
0347 12
                                      324
                                                         ADCI #0; -> AR, 1
INC SP
                                      325
                                             АП1:
    0348 8AF712
034B 9A77
                                                         AR. 0; SM; INC SP
AR. 1; SMB
LBDF GEREX
                                      326
                                      327
    034D C30000
                                      328
                                                          DEC CR;CR.0;LBZ DEVDN
DEC SP;DEC SP;DEC SP
AC.1;STXD;AC.0;STXD;INC SP
LBR CHKUP
    0350 2080020000
                                      329
           22222222
    0355
                                      330
    0359 9F738F7312
                                      331
    035E C00323
                                      222
                                             DEVDN: 0->CR. 1
    0361
           F800BC
                                      333
    0364 D40E491068
                                                      CALL LOADOP; , A(NDN)
                                      334
    0369 8FAC
                                      335
                                                        AC. 0-> CR. 0
    036B D40E490000
                                      336
                                                        CALL LOADOP; , A( DELRAN)
                                                      GHI AC; STXD
GLO AC; STXD
CALL LOADOP; , A(AVGDCT)
GHI AC; STXD
    0370 9F73
                                      337
    0372 8F73
                                      338
    0374 D40E491080
                                      339
    0379 9F73
037B 8F73
                                      340
                                                       GLO AC; STXD
A.1(DNBUF)->R0.1
A.0(DNBUF)->R0.0
                                      341
    037D F810B0
                                      342
    0380 F830A0
                                      343
                                                         @R0!->AC.0
    0383
           40AF
                                      344
                                                       @RO!.AND.15;STXD
GLO AC;STXD;INC SP
@RO!->AC.0
SD;->AR.0
INC SP
    0385
           40FA0F73
                                      345
    0389 8F7312
                                      346
    038C 40AF
                                             CHKDN:
                                      347
    038E F5AA
                                      348
    0390 12
                                      349
    0391
           40FA0FBF
                                                        @R0 ! . AND . 15-> AC . 1
                                      350
    0395 75BA
                                                       SDB ;->AR. 1
INC SP
                                      351
    0397
                                      352
    0398 BAF5AA12
                                      353
                                                        AR. 0; SD; -> AR. 0; INC SP
                                                       AR. 1; SDB; -> AR. 1
LBDF AII2
AR. 0. XOR. #FF+1-> AR. 0
AR. 1. XOR. #FF. AND. 15
    039C
           9A75BA
                                      354
    039F C30000
                                      355
    03A2 BAFBFFFC01AA
                                      356
    03AB 9AFBFFFA0F
                                      357
    03AD 7C00BA
                                                         ADCI #0;->AR.1
                                      358
    03B0 12
                                                AH2:
                                      359
                                                         INC SP
    03B1 8AF712
                                      360
                                                         AR. 0; SM; INC SP
                                                         AR. 1; SMB
LBDF GEREX
    03B4 9A77
                                      361
    03B6 C30000
                                      362
                                                       DEC CR:CR.0; LBZ DEVON
DEC SP; DEC SP; DEC SP; DEC SP
AC. 1; STXD; AC. 0; STXD; INC SP
    03B9
           2C8CC20000
                                      363
    03BE
           2222222
                                      364
    03C2
           9F73BF7312
                                      365
    03C7 C0038C
                                                         LBR ĆHKDN
                                      366
                                                          CALL LOADOP; A(NUP)
GLO AC; SMI 1; LBZ CHK1
CALL LOADOP; A(NDN)
GLO AC; SMI 1; LBZ CHK1
LBR COMPRA
    03CA D40E491066
                                             DEVON:
                                      367
F
    03CF 8FFF01C20000
                                      368
    03D5 D40E491068
                                      369
    03DA 8FFF01C20000
                                      370
                                      371
372
    03E0 C00000
    03E3 D40E49107E
                                                           CHK1: CALL LOADOP; , A(AVGUCT)
    03E8 D40C2D1080
                                      373
                                                                    CALL SMOP; A (AVGDCT)
    03ED D401DA
                                      374
                                                                   CALL ABSAC
                                                                  CALL SMOP; , A(DELRAN)
AC. 1. AND. #80; ADI 0
F
    03F0 D40C2D0000
                                      375
    03F5 9FFA80FC00
                                      376
    03FA C20000
                                                                  LBZ GEREX
                                      377
```

```
COMPRA: CALL LOADOP; A(AVGDCT)
GLO AC; PLO RO
GHI AC; ADI #5; PHI RO
03FD D40E491080
                                           378
0402 8FA0
0404 9FFC05B0
                                           379
                                           380
0408 40AA
040A D40E49107E
040F 8FAO
                                           381
                                                                      @R0!->AR.0
                                                                       CALL LOADOP; A(AVGUCT)
GLO AC; PLO RO
GHI AC; ADI #5; PHI RO
@RO!->@SP; AR.O; ADD; PLO AC
                                           382
                                           383
·0411 9FFC05B0
                                           384
0415 40528AF4AF
                                           385
041A CB0000
                                                                       LBNF DAV
                                           386
041D F801BF
                                           387
                                                                        1-> AC. 1
0420 C00000
0423 F800BF
                                                                       LBR DAV1
                                           388
                                                        DAV:
                                           389
                                                                        0-> AC. 1
                                                                       O-> AC. 1
CALL STOROP; , A(RANGE)
CALL LOADOP; , A(AVGDCT)
GLO AC; SHL; PLO RO
GHI AC; SHLC; ADI #8; PHI RO
@RO!-> AC. 1
@RO!-> AC. 0
0426 D40E571078
042B D40E491080
                                           390
                                                          DAV1:
                                           391
0430 8FFEA0
0433 9F7EFC08B0
                                           392
                                           393
0438 40BF
                                           394
                                                            AG3:
043A 40AF
043C 8FAA9FBA
                                           395
                                                                       AC.0-> AR.0; AC.1-> AR.1
CALL LOADOP; A(AVGUCT)
GLO AC; SHL; PLO MA
GHI AC; SHLC; ADI #8; PHI MA
                                           396
0440 D40E49107E
0445 8FFEAD
                                           397
                                           398
0448 9F7EFC08BD
                                           399
                                                                         AR. 1->AC. 1; AR. 0->AC. 0
CALL SM
044D 9ABF8AAF
                                           400
                                                            AG1:
0451 D40C31
                                            401
                                                                         CALL STOROP;, A(DOPRR)

0-> CR. 1; #5-> CR. 0

GHI AC; SHL; GHI AC; SHRC; PHI AC

GLO AC; SHRC; PLO AC

DEC CR; CR. 0; LBNZ RD2
0454 D40E571070
0459 F800BCF805AC
                                           462
                                           403
045F 9FFE9F76BF
                                                            RD2:
                                           404
0464 8F76AF
                                           405
0467 2C8CCA045F
046C D40E571089
                                           406
                                           407
                                                                           CALL STOROP; , A(LOLIM)
0471 FF00
0473 D5
                                            408
                                                                         SMI 0
                                           409
                                                          GETRX:
                                                                         EXIT
0474 FC00D5
0477 F810BA
047A F887AA
047D F8015A
0480 FC00D5
                                                                         ADI #0: EXIT
A. 1(FLAC3) -> AR. 1
                                                            GEREX:
                                           410
                                           411
                                                              CETX:
                                           412
                                                                         A. 0(FLAG3) -> AR. 0
                                           413
                                                                         #1->@AR
                                           414
                                                                         ADI #0; EXIT
0483
                                           415
                                           416
417
0483
                                                    ... AVERAGE UPAND DOWN COUNT
AUPDN: @RO!->AR.0
@RO!; STXD
0483
0483 40AA
0485 4073
0487 8A7312
048A 10102F
                                           418
                                           419
                                                                AR.0;STXD; INC SP
INC R0; INC R0; DEC AC
AC.0;LBNZ AVE
@R0!;SD;->AC.0; INC SP
@R0!;SDB;.AND.15->AC.1
                                           420
                                           421
422
                                                     AVE:
048D 8FCA048A
0491 40F5AF12
                                           423
0495 4075FA0FBF
                                           424
049A D5
049B
                                           4\overline{25}
                                                                EXIT
                                           426
                                                  .... TABLE FOR RANCE CONSTANTS ....> RTAB 8:27:1979
049B
                                           427
049B
                                           428
049B
                                           429
                                                  • • •
051E
                                           430
                                                              ORG #51E
05 1E
                                           431
```

```
,254,246,239,231,224,218,212,206,201,196,191,159,156,152,149,147,144,141,139,136,134,13,115,114,112,110,109,107,106,104,103,101,1
051E FEF6EFE7E0DAD4CE
                                           432
0530 9F9C989593908D8B
                                           433
0542 7372706E6D6B6A68
                                           434
0556 5857
                                           435
                                                               88.87
0558 5655545453525150
                                           436
                                                           ,86,85,84,84,83,82,81,80,79,78,78,77,76,75,
056F 4444434342414140
0586 3938383737373636
                                           437
                                           438
059D 3030302F2F2F2E2E
                                           439
05B3 2A2A2A2A29292929
                                           440
05CA 2525252525242424
                                           441
05E2 2121212121212020
                                           442
95FA 1E1E1E1E1E1D1D1D
                                           443
9611
         1C1B1B1B1B1B1B1B1B
                                           444
0629
         1919191919191919
                                           445
9641
         1717171717171717
                                           446
0657
         1616161616151515
                                           447
066F
         1414141414141414
                                           448
                                                         0684
         1313131313131313
                                           449
983C
                                           450
                                                          ,2785,2695,2611,2532,2457,2387,2321,2258,219
,1899,1857,1816,1778,1741,1705,1671,1638,16
083C 0AE10A870A3309E4
                                           451
0858 076B0741071806F2
                                           452
                                                            , 1440, 1416, 1392, 1370, 1347, 1326, 1305, 1285, 12
, 1160, 1144, 1129, 1114, 1099, 1085, 1071, 1057, 10
, 971, 960, 949, 938, 928, 918, 908, 898, 889, 879, 87
, 811, 803, 795, 788, 781, 773, 766, 759, 752, 746, 73
0874 05A005880570055A
                                           453
0890 048804780469045A
                                           454
08AC 03CB03C003B503AA
                                           455
08CE 032B0323031B0314
                                           456
08F0 02B802B202AD02A7
                                           457
                                                            ,696,690,685,679,673,668,663,658,652,647,64
                                                           ,610,605,601,596,592,588,584,580,576,572,56,539,535,532,528,525,522,519,515,512,509,50,485,483,480,477,474,472,469,466,464,461,45,439,437,435,433,430,428,426,424,422,419,41,401,399,397,396,394,392,390,388,386,385,38,369,368,366,364,363,361,360,358,357,355,35,343,342,341,339,338,336,335,334,332,331,33
0912 0262025D02590254
                                           458
0936 021B021702140210
                                           459
0958 01E501E301E001DD
                                           460
097C 01B701B501B301B1
                                           461
09A0 019101BF01BD01BC
                                           462
09C4 01710170016E016C
                                           463
09E6 0157015601550153
                                           464
                                                            ,320,318,317,316,315,314,313,311,310,309,30
,299,298,297,296,295,294,293,292,291,290,28
,281,280,279,278,277,276,275,274,274,273,2
0A0A 0140013E013D013C
                                           465
0A2E 012B012A01290128
                                           466
0A52 0119011801170116
                                           467
                                                           , 265
, 264, 263, 262, 261, 261, 260, 259, 258, 257, 257, 25
, 0, 252, 0, 251, 0, 250, 0, 250, 0, 249, 0, 248, 0, 247,
, 0, 244, 0, 243, 0, 242, 0, 241, 0, 240, 0, 240,
, 0, 236, 0, 235, 0, 234, 0, 234, 0, 233, 0, 232, 0, 232,
, 0, 228, 0, 227, 0, 227, 0, 226, 0, 225, 0, 225, 0, 224,
, 0, 221, 0, 220, 0, 219, 0, 219, 0, 218, 0, 218, 0, 217,
, 0, 214, 0, 213, 0, 213, 0, 212, 0, 212, 0, 211, 0, 211,
, 0, 207, 0, 207, 0, 206, 0, 206, 0, 205, 0, 205, 0, 204,
, 0, 201, 0, 201, 0, 200, 0, 199, 0, 199, 0, 198,
, 0, 196, 0, 195, 0, 195, 0, 194, 0, 194, 0, 193, 0, 193,
, 0, 190, 0, 190, 0, 189, 0, 189, 0, 189, 0, 188, 0, 188,
, 0, 185, 0, 185, 0, 184, 0, 184, 0, 184, 0, 183, 0, 183,
, 0, 180, 0, 180, 0, 179, 0, 179, 0, 178, 0, 178,
, 0, 176, 0, 175, 0, 175, 0, 175, 0, 174, 0, 174, 0, 174,
, 0, 171, 0, 171, 0, 171, 0, 170, 0, 170, 0, 166, 0, 165,
0A76 0109
                                           468
                                                               265
9A78 9198919791969195
                                           469
        OOFCOOFBOOFAOOFA
0A96
                                           470
OAAC 00F400F300F200F2
                                           471
        ООЕСООЕВООЕАООЕА
0AC4
                                           472
0ADC 00E400E300E300E2
                                           473
0AF4 00DD00DC00DB00DB
                                           474
0B0C 00D600D500D500D4
                                           475
                                           476
477
0B24
        00CF00CF00CE00CE
OB3C
        00C900C900C800C8
                                           478
479
0B54 00C400C300C300C2
OB6C OOBEOOBEOOBDOORD
0B84 00B900B900B800B8
                                           480
0B9C 00B400B400B400B3
                                           481
OBB4 OOBOOOAFOOAFOOAF
                                           482
OBCC OOABOOABOOAB
                                           483
0BE4 00A700A700A700A6
                                           484
                                                             0, 167, 0, 167, 0, 167, 0, 166, 0, 166, 0, 166, 0, 165,
OBFC 00A300A3
                                           485
                                                            ,0,163,0,163
```

```
0C00
                                                                                486 ...
487 ...
 0C00
 0C00
                                                                                 488
 0000
                                                                                 489
 9C00
9C00
9C00
9700
9790 2920292929
9705 29202029
                                                                                                        OUTBF = # 1090
                                                                                 490
                                                                                 491
                                                                                                ORC #0700

SYSAC: ,32,32,32,32,32

,32,32,32,32

,T'SYSTEM',32

,T'ACTIVE'

,32,32,32,32,32

,32,32,32,32,32
                                                                                 492
                                                                                 493
0705 2020202020

0705 20202020

0709 53595354454D20

0710 414354495645

0716 2020202020

071B 2020202020

0720 523D58582E5820

0727 52523D2B58582E58

0731 533D58582020

073E 202020

0741 00A0

0743 003C

0745 000A

0747 00FA

0749 0010

074B 000D

074B 000D

074F 0028

0751
                                                                                 494
                                                                                 495
                                                                                 496
497
                                                                                 498
                                                                                 499
                                                                                 500
                                                                                                 MESOUT: ,T'R=XX.X',32
,T'RR=+XX.X',32,32
,T'S=XX',32,32
,T'NUP=XXX'
                                                                                 501
                                                                                 502
                                                                                 5\overline{0}\overline{3}
                                                                                504
505
506
507
                                                                                                                           ,32,32,32
                                                                                                                  RRTHR: ,0,160
DELRR: ,0,60
SCUTOF: ,0,10
RCUTOF: ,0,250
DELCNT: ,0,16
DELRAN: ,0,13
DEC5: ,0,5
DEC40: ,0,40
                                                                                 508
                                                                                 509
                                                                                 510
                                                                                 511
512
                                                                                 513
                                                                                 514
                                                                                                            PEND: END
                                                                                 515
```

APPENDIX C

SOFTWARE LISTING FOR ARITHMETIC SUBROUTINE GETRAN

```
FL LOC COSMAC CODE
                                                 LNNO SOURCE LINE
                                                                     ..COPYRIGHT 1976 RCA CORPORATION
.. COSMAC ARITHMETIC SUBROUTINE PACKAGE
ORC #COO ...**FOR RADAR CRUISE CONTROL
      0000
      0000
      0000
      0000
      0000
                                                                     .. VERSION 1.1 FOR CDP1802
      0000
                                                                    EXTRACTED FOR BINARY ARITHMETIC
AND CONVERSIONS FOR DECIMAL
GCCUPIES 1K BYTES
      6000
      0CC0
                                                       a
      0000
      0000
                                                     10
      6C00
                                                                     .. DESIGNED FOR STANDARD CSDP SUBROUTINE CA
      0000
      0000
                                                      13
                                                                    .. FOR STANDARD LINKAGE,
SP= #02 ...IT SHOULD BE THE STACK POINTER.
PC= #03 ...IT IS THE PROGRAM COUNTER
.. USED BY THESE SUBROUTINES.
CALL= #04 ...IT SHOULD POINT TO THE ROUTINE
.. WHICH EFFECTS SUBROUTINE CALLS.
      CC00
      0000
                                                     15
      0000
                                                     16
      0000
      9000
                                                     18
     0000
                                                     19
                                                              RETH= #65 ... IT SHOULD POINT TO THE ROUTINE
.. WHICH EFFECTS SUBROUTINE RETURN.
LINK= #66 ... IT SHOULD POINT TO CALL PARAME
... (USUALLY OPERAND ADDRESSES AND/OR CON
.. THE FOLLOWING REGISTERS MUST BE ASSIGNED
AR= #9A .. (USED FOR RESULT ADDRESS)
NR= #0B .. (USED FOR RESULT DIGIT COUNT)
16-RIT BINARY ARITHMETIC BOUTINES
     0000
                                                     20
     OCCO O
     6000
     OCOG
                                                     23
     OC06
                                                     24
                                                     25
     0000
     4000
                                                     26
                                                              .. 16-BIT BINARY ABITHMETIC ROUTINES
.. THE FOLLOWING REGISTERS MUST BE ASSIGNED
AC =#0F ..16-BIT ACCUMULATOR=RF
MY =#0E ..16-BIT ACCUMULATOR=RE EXTENSION
     0C00
                                                     27
     0000
     0000
                                                     29
     0C00
                                                     \bar{30}
                                                              MA = #0D ...(TEMPORARY) GPERAND MEMORY ADDRESS.
CR = #0C .. (TEMPORARY) SCRATCHPAD AND COUNTER.
     0000
                                                     31
     0000
     ØC00
                                                     3\overline{3}
     00000
                                                     34
                                                            SWAP AC WITH MQ REGISTERS
SWAPAQ: CHI MQ .. SAVE MQ.1
PLO CR .. IN CR.0 (COULD HAVE PUSHED ON STA
CHI AC .. NOW AC.1 TO HQ.1
PHI MQ
     9099
                                                     35
     0C00 9E
                                                     36
     0C01 AC
0C02 9F
                                                     38
     0C03 BE
                                                     39
                                                                    GLO MQ .. SAVE MQ.0
PHI AC .. IN AC.1
GLO AC .. THEN AC.0 TO MQ.0
     0C04 8E
                                                     40
     OCO5 BF
                                                     41
     9C06 8F
9C07 AE
                                                     42
                                                     43
                                                                     PLO MQ
     0008 9F
                                                     44
                                                                     GHI AC .. NOW SAVED MQ.0 TO AC.0
     0009 AF
                                                     45
                                                                     PLO AC
     OCOA 8C
                                                     46
                                                                    GLO CR .. FINALLY SAVED MQ. 1
                                                                    PHI AC .. TO AC.1
SEP RETN
     OCOB RF
                                                     47
     0000 PS
                                                     48
                                                                    .. 16-BIT SUBTRACT AC FROM CONSTANT
.. ****AC= CONSTANT-AC
     ecod
                                                     49
     COD
                                                     50
     0000
                                                            51
     OCOL
                                                     52
     OCOD 86
```

```
OCOF AD
                                                          PLO MA
                                                         GIII LINK
PHI MA
                                           55
OCIO BD
                                           56
                                                         INC LINK
OC11 16
                                           57
0C12 16
                                           58
6C13 3000
                                           59
                                                         BR SD
9C15
                                           60
0C15
                                                          .. 16-BIT SUBTRACT AC FROM OPERAND
0C15
                                                          .. ***AC=OPRN-AC
0C15
                                                          .. ********** (TO CALL, WRITE) *******
0C15
                                                          .. ****CALL SDOP : , ACOPRN)
                                           64
0C (5
                                                  SDOP: LDA LINK .. FETCH OPERAND ADDRESS PHI NA .. TO MA REGISTER
0C15 46
                                           66
67
0C16 BD
0C17 46
                                                         LDA LINK
                                           68
                                                         PLO MA . FALL INTO SD
. 16-BIT SUBSTRACT AC FROM OPERAND.
. CALL HERE IF OPERAND
. ADDRESS IN RECISTER MA
OC18 AD
                                           69
€C19
                                           70
0C19
0C19
0C19
                                           73
                                                          .. ****AC=M(R(MA))-AC
0C19
                                           74
                                                         .. ********* (TO CALL, WRITE) *******
0019
                                           75
                                                          .. ****CALL SD
0C19
                                                         SFX MA .. SET X PTR TO MA
GHI AC ..CHECK SIGN BIT OF AC
XOR ..AND OPERAND & MA
STR SP ..AND STORE ON STACK
INC MA ..POINT TO LOW 8
GLO AC .. FETCH AC 1.0W 8
SD .. SUBTRACT FROM LOW B IN NEMORY
PLO AC .. PUT IT BACK
DEC MA .. NOW HIGH 8
GHI AC
                                                         . .
0C19 ED
0C1A 9F
0C1B F3
0C1C 52
                                           77 SD:
                                           78
                                           80
OCID ID
                                           81
OCIE 8F
                                           82
OCIF F5
                                           83
0C29 AF
0C21 2D
                                           814
                                           25
0C22 9F
                                           86
                                                 GHI AC
SDNB: SDB .. SUBTRACT HICH 8
PHI AC .. PUT IT BACK
LDN SP ..LOAD STORED COMPARING BIT OF OPE
SHL ..CHECK STORED SIGN COMPARISION BIT
BNF SDFF ..IF OPERAND'S SIGNS ARE SAME
GHI AC ..NO OVERFLOW POSSIBLE
XOR ..OTHER WISE CHECK RESULT
SHL ..SET DF=0 IF OK
SDFF: SEP RETN ..RETURN

16-BIT SUBTRACT FROM AC (ADDRESS IN CALL
                                                         CHI AC
CC23 75
CC24 PF
                                           87
0C25 C2
0C26 FE
0C27 3B00
0C29 9F
                                           89
                                           90
                                           91
                                           92
0C2A F3
                                           93
OC2B FE
0C2C D5
0C2D
                                           95 SDFF:
                                                               16-BIT SUBTRACT FROM AC (ADDRESS IN CALL
                                           96
ĕC2b
                                           97
                                                         .. ****AC=AC-OPRN
0C2D
0C2D
                                                         .. #********* (TO CALL, WRITE) ********
.. ****CALL SMOP; , A(OPRN)
                                           93
                                           99
0C2D
                                         100
                                                  SMOP: LDA LINK
0C2D 46
                                         101
0C2E BD
0C2F 46
                                                         PHI NA
LDA LINK
                                         102
                                         103
OC30 AD
                                          104
                                                         PLO MA
9C31
                                          105
                                                               16-BIT SUBTRACT FROM AC (ADDRESS IN MA)
                                                         . .
0C31
                                          166
                                                         .. CALL HERE IF OPERAND
€C31
                                          107
                                                         .. ADDRESS IN RECISTER MA
```

```
0C31
                                             108
                                                              .. ***AC=AC-M(R(MA))
0C3 I
                                             109
                                                              .. ********* (TO CALL, WRITE) *******
0C31
                                             110
                                                              .. ****CALL SM
0C31
                                             111
0C31 ED
                                             112 SM:
                                                                SEX MA .. SET X PTR
                                                              GHI AC ..GET SIGN OF AC AND SHR ..AND STORE IN 7TH BIT OF CR STR SP ..BUT PUT IN (SP) FIRST GHI AC ..AND SEE IF OPERANDS SIGNS ARE THE
0C32 9F
                                             113
0C33 F6
                                             114
0C34 52
                                             115
0C35 9F
                                             116
                                                             XUR
ANI *80 ..TAKE OUT COMPARING SIGN BIT
SEX SP ..NOW STORE THAT BIT IN 8TH OF CR
ADD ..BY ADDING TO IT
STR SP ..AND STORE THESE TWO BITS ON STACK
INC MA ..POINT TO LOW 8
SEX MA ..REMEMBER TO SET X TO OPERANDS
GLO AC .. FETCH AC LOW 8
SN .. SUBTRACT MEMORY FROM IT
PLO AC .. PUT IT BACK.
DEC MA .. NOW HIGH 8
GHI AC
0C36 F3
0C37 FA80
0C39 E2
                                             117
                                             118
                                             119
0C3A F4
                                             120
0C3B 52
                                             121
0C3C 1D
                                             122
OC3D ED
                                             123
OCSE SF
                                             124
OCSF FZ
                                             125
0C40 AF
                                             126
0C41 2D
0C42 9F
                                             127
                                             128
                                            128 CHI AC
129 SMNB: SMB . . HIGH 8 SUBTRACT, NO BORROW ACCROSS
130 PHI AC . . PUT HIGH 8 BACK
131 SEX SP . .NOW CHECK IF UNDERFLOWED
132 LDX . .LOAD THE STORED TWO BITS
133 SHL . .AND TAKE OUT THE COMPARING SIGN BIT
134 BNF SMRT . .THE SAME, UNDERFLOW NOT POSSIBLE
135 STR SP . .PUT IT BACK TO STACK
136 CHI AC . .OTHERWISE HAVE TO COMPARE SIGN O
137 XOR . .SIGN BIT OF AC WAS STORED ON STACK
138 SMRT: SEP RETN . .DF=0 IF SUBTRACTION OK
                                                              GHI AC
0C43 77
0C44 BF
0C45 E2
0C46 F0
0C47 FE
0C48 3B00
0C4A 52
0C4B 9F
0C4C F3
OC4D FE
0C4E D5
0C4F
                                             140
0C4F
                                            141
0C4F
                                             142
                                                             .. 16X16 BIT SIGNED MULTIPLY(2'S COMPLEMENT)
0C4F
                                             143
                                                              ..****AC=AC*OPRN
ØČ4F
                                                              144
ÖČ4F
                                             145
0C4F
                                             146
                                                   MPYOP: LDA LINK ..FETCH MULTIPLICAND ADDRS
PHI MA ..INTO REGISTER A
LDA LINK
OC4F 46
                                             147
0C50 BD
                                            148
ØC51 46
                                            149
0C52 AD
                                                             PLO MA .. FALL INTO MPY ... 16X16 BIT SIGNED MULTIPLY (2'S COMPLEMEN .. CALL HERE IF OPERAND ADDRESS
                                            150
0C53
                                             151
0C53
                                             152
0C53
                                             153
                                                              .. IN REGISTER MA
0C53
                                             154
                                                             .. ****AC=AC*M(R(MA))
0C53
                                             155
                                                              .. ********* (TO CALL, WRITE) *******
0053
                                                              .. ****CALL MPY
                                            156
0C53
                                            157
                                                     MPY: SEX MA .. SET X NOW

GHI AC .. CHECK IS THE SIGN OF MULTICAND

XOR .. THE SAME AS THE SIGN OF MULTIPR
OC53 ED
                                            158
6C54 9F
                                            159
0C55 F3
                                            160
0C56 FA80
                                                              ANI #80 .. AND STORE THAT BIT
                                            161
```

```
PHI CR .. INTO CR. 1
LDI #10 .. SET COUNTER TO 16
 0C58 BC
                                        162
 0C59 F810
                                        163
 OC5B AC
                                        164
                                                       PLO CR
 0C5C F800
                                                       LDI #00 .. INITIALIZE MQ TO 0
PHI MQ ... TO HOLD PRODUCT.
                                        165
 OC5E BE
OC5F AE
                                        166
                                        167
                                                       PLO MQ
 0C60 2C
                                                       DEC CR ... IF NOT, DECREMENT IT. CHI AC .. SHIFT AC (=MULTIPLJER) RIGHT
                                        168 MPL:
 0C61.9F
                                        169
 0C62 F6
                                        170
                                                       SHR
 0C63 BF
                                        171
                                                      PHI AC
                                        172
173
174
 6C64 8F
                                                       CLO AC
                                                       SHRC ...
 9C65 76
                                                                   SHIFT 0 ACCROSS BYTES ...
 0C66 AF
                                                       PLO AC
                                                      BNF MPB ..IF NO BIT OUT, DON'T ADD.
INC MA .. POINT TO LOW 8 OF MULTIPLICAND
GLO CR .. IF NOT LAST ITERATION,
BNZ MPA .. GO ADD.
GLO MQ ... I OAD MO C. ...
 0C67
         9 E
                                        175
 0C68 3B00
                                        176
0C6A 1D
0C6B 8C
                                        177
                                        178
0C6C 3A00
                                        179
0C6E 8E
                                        180
                                                       CLO MQ
                                                                    .. LOAD MQ. Ø INTO D
                                                             MQ ... AND STORE BACK INTO MQ.0
MA .. NOW DO THE HIGH BYTE
 0C6F F7
                                        181
                                                       SM
0C70 AE
0C71 2D
0C72 8E
                                        182
                                                       PLO MQ
                                        183
                                                       DEC MA
                                        184
                                                       CHI MQ
 0C73 77
                                                                    .. REMEMBER THE BORROW BIT
                                        185
                                                      SMR
0C74 BE
0C75 9C
                                                                   ..AND PUT BACK INTO MQ.1
..NOW ARE THE SIGNS OF OPERANDS THE
..TEST FOR SIGN BIT
                                                      PHI MQ
                                        186
                                        187
                                                      CHI CR
9C76 FE
9C77 3093
9C79 BE
9C7A F4
                                        188 MPB:
                                                         SHL
                                                      BR MPS+#03 ..IF NEGATIVE, SIGN EXTEND GLO MQ ..DO MQ+(MA)
                                        189
                                             MPA:
                                       190
                                                            GLO MQ
                                                      ADD ..MQ.0+(MA.0)
PLO MQ ..AND PUT BACK INTO MQ.0
DEC MA ..SAME FOR HIGH BYTE
                                        19 Ï
OC7B AE
                                       192
0C7C 2D
                                        \overline{193}
0C7D 9E
                                       194
                                                      CHI MQ
0C7E 74
0C7F BE
                                       195
                                                      <u>A</u>DĊ
                                                                 ..ADD WITH CARRY
                                                      PILI MQ
                                       196
0C80 CF
0C81 F0
                                             MPS:
                                       197
                                                          LSDF
                                       198
                                                      LDX
0C82 FE
0C83 9E
                                                      SHL..IF GPERAND IS NEGATIVE, THEN CHI MQ ..PUT MQ.1 INTO D SHRC .. SHIFT IN CARRY
                                       199
                                       200
                                                      SHRC .. SHIFT IN CARRY
PHI MQ
GLO MQ .. CONTINUE TO LOW 8 OF MQ
0C84 76
                                       201
0C85 BE
                                       202
9C86 8E
9C87 76
                                       \overline{2}\overline{9}\overline{3}
                                       204
                                                      PLO MQ
BNF MT . IF NO CARRY OUT, ITERATE.
GHI AC . . ADD CARRY OUT INTO AC MSB.
0088 AE
                                       205
0C89 3B00
                                       206
0C8B 9F
                                       207
OCSC F980
OCSE BF
                                                      ORI #80
PHI AC
                                       208
                                       209
0C8F 8C
0C90 3A60
0C92 9F
                                               TF: GLO CR ..CHECK COUNTER
BNZ MPL ..IF COUNTER IS NOT 0, GO BACK FOR
MPX: GUI AC .. FINISHED:
                                       210 MT:
                                       211
                                       212
0C93 FE
                                                      SHL .. CHECK FOR PRODUCT > 15 BITS. GLO MQ
                                       213
0C94 8E
                                       \overline{214}
ØC95 C7
                                       \overline{2}15
                                                      LSNF
                                                               .. THAT'S HIGH 17 BITS
```

```
0096 FBFF
                                                  XRI #FF .. ALL 00 OR FF. BNZ *+#06 .. NAW.
                                    216
CC98 SA9E
                                    217
OC9A 9E
                                    218
                                                  CHI MQ
OCOB C7
OCOC FIVE
OCOE FOFF
                                    \bar{2}1\bar{9}
                                                  LSNF
                                                  XRI #FF
ADI #FF
                                    220
                                                  ADI #FF .. SET DF IF PRODUCT > 15 BITS
SEP RETN .. RETURN.
.. 32/16 BIT SIGNED DIVIDE (2'S COMPLEMENT)
                                    221
CCAG D5
                                    วีวีว
                                    223
OCA1
CCA1
                                    224
                                                       AC=FIQ. AC/OPRN
OCAL
                                    223
                                                       QUOTIENT IN AC
                                                                               . REMAINDER IN MQ.
                                    226
                                                       *********** (TO CALL, WRITE) ******
OCA1
OCAL
                                    227
                                                  .. CALL DIVOP ; , A(OPRN)
OCA1
                                    228
                                           OCAL
                                    229
OCAR BD
                                    230
OCAS
       46
                                    231
OCA4 AD
                                    232
0 CAS
                                    233
OCA5
                                    234
0CA5
                                    235
@CAS
                                    236
                                                  .. ########### (TO CALL, WRITE) **#######
                                           DIVO: SEX MA .. SET X TO POINT TO DIVISOR (0)

CHI AC .. LOOK AT AC SIGN (0)

SHL .. COPY IT TO DF (0)

LDI #00 .. EXTEND #00 IF POSITIVE, (0)

LSNF .. (0)

LDI #FF .. #FF IF NEGATIVE. (0)

PHI MQ .. CIVING +0 OR -0 IN MQ (0)

PIO MQ (0)
0CA5
                                    237
                                                      ****CALL DIVO
OCAS ED
                                    238
OCA6 9F
OCA7 FE
                                    239
                                    240
6CAS FA00
                                    241
OCAA CZ
                                    242
OCAB FSFF
                                    243
OCAD BE
                                    244
OCAE AE
                                    2 15
                                                  PLO MQ .. (0)
OCAF 4D
OCEO F1
OCB1 2D
OCB2 FD00
                                    246
                                                  LDA MA
                                                              . CHECK FOR ZERO DIVISOR (0)
                                                 OR . (0)
DEC MA .. (DON'T FORGET TO FIX POINTER)(0)
SDI #00 .. IF ZERO, CALL IT DIVIDE CHECK(0)
BNF DIV .. CO ON IF NO DIVIDE CHECK ERR
SEP REIN .. AND RETURN WITH DF=1 (0)
... OPTION #2: PERMIT 32-BIT DIVIDEND; (/)
                                    247
                                    248
                                    249
0CB4 3B00
                                    250
0006 D5
                                    251
(ACD)?
                                    252
OCB7
                                    253
OCD?
                                    254
                                                  .. MAKE SURE QUOTIENT DOES NOT EXCEED 16 BIT
ØCB7
                                                  .. ******* (TO CALL, WRITE) ******(/)
.. ***** CALL DIV *****(/)
                                    255
OCB7
                                    256
0CB7 9E
                                    257 DIV:
                                                   GHI MQ .. SAVE PARTIAL DIVIDEND(/)
                                                  PHI CR ..INTO CR. 1(/)
CLO MQ ..(/)
OCBS BC
                                    258
                                                           1 ..(/)
1 ..AND CR.0(/)
OCB9 SE
                                    \overline{2}59
OCBA AC
                                    260
                                                  PLO CR
OCBB FE
                                    264
                                                  SIIL
                                                 PLO MQ ..(/)
GIII MQ ..DO THE SAME FOR HICH BYTE(/)
OCBC AE
                                    262
OCBD 9E
OCBE 7E
OCBF BE
                                    263
                                                            ..REMEMBER CARRY(/)
                                    264
                                    265
                                                  PHI MQ ...(/)
9000 9F
                                    266
                                                              ..ALSO SHIFT IN AC HIGH(/)
                                                  CHI AC
OCCI FE
                                    267
                                                 SHL ..(/)
BDF D2-#01
                                                  SHL
OCC2 CSFF
                                                   3DF D2-#01 ..(/)
GLO CR ..SEE IF MQ.0 =0(/)
                                    268
0CC4 8C
                                   269
```

```
BNZ D2 ...IF NOT GO THROUGH CHECKING STEPS
GHI CR ..SEE IF MQ.1 IS #40(/)
XRI #40 ...WHICH SHOULD RESULT 0 IF TRUE(/)
BZ D4 ...IF TRUE, SKIP NORMAL CHECKING(/)
0005 3A00
                                                                   270
                                                                   \frac{271}{272}
 0CC7 9C
 OCCB FB40
0CCA 3200
0CCC 38
                                                                   273
                                                                   274
                                                                                                #38
                                                                                             ,#38
INC MQ ..IF 1, SHIFT INTO MQ(/)
CHI CR ..CHECK IF HICH 2 BITS OF MQ AR
ANI #CO ..TAKE OUT 2 HICH BITS(/)
SDI #00 ..SEE IF THEY ARE THE SAME(/)
SHL ..SHIFT OUT COMPARISION (/)
LBOF DVXX ..SET DF AND RETURN(/)
GUI CR ..LOOK AT THE SIGNS OF DIVND AND D
SEX MA ..POINT X TO DIVISOR(/)
YOR (/)
 OCCD 1E
                                                                    275
                                                                    276 D2:
277
 OCCE 9C
 OCCF FACO
OCD1 FDGO
                                                                   278
279
 OCD3 FE
0CD4 C30000
0CD7 9C
                                                                    280
                                                                    281 D4:
 OCDS ED
                                                                    282
 OCD9 F3
                                                                                            SHL ..SET DF IF THE SAME(/)

INC MA ..MQ.0-(MA)(/)

GLO MQ ..MQ.0 TO D(/)

BDF DVA ..IF FLAG ,MQ.0+(MA)(/)

SM ..MQ.0-(MA.0)(/)

PLO MQ ..AND STORE BACK INTO MQ.0(/)

DEC MA ..DO THE SAME FOR HIGH BYTE(/)

GHI MQ ..LOAD MQ.1 INTO D(/)

SMB ..MQ.1-(MA.1) WITH CARRY(/)

BR DVB ..SKIP OVER ADD STEP(/)

ADD ..MQ+(MA)(/)

PLO MQ ..STORE BACK TO MQ.0(/)

DEC MA ..SAME FOR HIGH BYTE(/)

GHI MQ ..MQ.1+(MA.1)(/)

ADC ..ADD MQ.1 AND (MA.1) WITH CARRY(/)
                                                                    283
                                                                                                           ..(/)
                                                                                              XOR
 OCDA FE
                                                                   284
 OCDB 1D
                                                                    285
 OCDC 8E
                                                                    286
 0CDD 3300
                                                                    287
 OCDF F7
                                                                    288
 CCEO AE
                                                                   289
0CE1 2D
                                                                    290
0CE2 9E
0CE3 77
                                                                   291
                                                                   2)2
0CE4 2G00
0CE6 F4
                                                                   293
                                                                   294 DVA:
6CE?
                                                                   \overline{295}
OCES 2D
                                                                   296
 6CE9 9E
                                                                   297
                                                                                             GHI MQ ..MQ.1+(MA.1)(/)
ADC ..ADD MQ.1 AND (MA.1) WITH CARRY(/)
PHI MQ ..AND STORE BACK INTO MQ.1(/)
GHI CR ..LOOK AT THE SIGN OF DIVIND(/)
SHL ..SET DF IF DIVIND IS NE@@ATIVE
LUNF DV2 ..IF NOT, DON'T COMPLEMENT DIFF(/
GHI MQ ..COMPLEMENT MQ(/)
XRI #FF ..BY XOR TO #FF(/)
PHI MG (/)
OCEA 74
                                                                   298
OCEB BE
                                                                   299 DVB:
OCEC 9C
OCED FE
                                                                   300
                                                                   30 i
6CEE CB0000
                                                                   302
9CF1 9E
                                                                   303
OCF2 FBFF
                                                                   394
ØCF4 BE
                                                                   305
                                                                                             PIII MQ
                                                                                             CLO MQ ..(DO THE SAME FOR LOW BYTE)(/)
XRI #FF ..(/)
OCF5 8E
                                                                   306
 OCF6 FBFF
                                                                                                                  ..(/)
                                                                   307
 OCFS AE
                                                                                           PLO MQ ..(/)
INC MQ ..REMEMBER TO ADD 1 (/)
CHI MQ ..NOW LOOK AT THE DIFF OF MQ8(M
LBZ D10 ..IF 0,CHECK MQ=0(/)
SHL ..CHECK IF MQ IS NEGATIVE(/)
BDF DDQ ..IF YES, NO PROBLEM(/)
BR D9 ..IF NOT 0 NOR NEC, DIVND IS TOO LARG
CLO MQ ..HERE WE CHECK DIFF=0 CASES(/)
ADI #FE ..IF MQ.0 IS NOT EITHER 0 OR 1(/)
BDF DVXX ..THEN DIVND IS STILL TOO LARGE(
XRI #FF ..RESULT 0 IF MQ.0 WAS 1(/)
BNZ DVH ..IF NOT, MUST BE 0, CO TO DVII(/)
CIII CR ..SEE IF DIVND IS NEGATIVE(/)
ANI #80 ..RESULT 80 IF YES(/)
BZ D9 ..IF DIVND POSITIVE, IT CANNOT DIV
ADD ..SEE IF DIVISOR IS POSITIVE(/)
                                                                   308
                                                                                              PLO MQ
OCF9 1E
                                                                   309
OCFÁ 9E
                                                                             DV2:
                                                                   310
OCFE FE
                                                                   311
                                                                   312
OCFF 3300
                                                                   313
OD91 3000
                                                                   314
0003 8E
                                                                   315 D10:
ODO4 FCFE
                                                                   316
0D06 3300
                                                                   317
ODOS FREE
                                                                   318
ород Здоо
                                                                   319
ODOC 9C
                                                                   320
ODOD FA80
                                                                   321
0D0F 3200
                                                                   322
0D11 F4
                                                                   323
                                                                                                           .. SEE IF DIVISOR IS POSITIVE(/)
                                                                                             ADD
```

```
BDF DVXX .. IF NEGATIVE, DIVND CANNOT DIVI
INC MA .. AC+(MA) TO MQ(/)
CLO AC .. DO AC LOW FIRST(/)
ADD ..(/)
0D12 3300
                                                                     324
0D14 1D
0D15 8F
                                                                     325
                                                                     326
0D16 F4
0D17 AE
                                                                                                PLO MQ ..STORE BACK TO LOW MQ(/)@
DEC MA ..DO THE SAME FOR HIGH BYTE(/)
GHI AC ...(/)
                                                                      327
                                                                      328
0D18 2D
                                                                      \tilde{3}\tilde{2}\tilde{9}
0D19 9F
                                                                      \overline{330}
                                                                                                GHI AC ..(/)
ADC ..ADD WITH CARRY(/)
PHI MQ ..(/)
INC MA ..LEAVE MA POINTING TO LOW DIVISOR(/
LDX ..NOW HECK LOW BIT (MA) IS 0 OR 1(/)
SHR ..SHIFT THAT LOW BIT OUT(/)
DEC MA ..REMEMBER TO RESET MA(/)
CHI MQ ..READY TO ADD #80(/)
LSNF ..IF LOW BIT OF AC IS 1(/)
ADI #80 ..TO MQ.1(/)
PHI MQ ..STORE STATUS(/)
SHL ..SEE IF MQ >0(/)
0D1A 74
                                                                      33 i
ODIB BE
                                                                      352
ODIC ID
                                                                      333
ODID FO
                                                                     334
6D1E F6
                                                                      335
ØD1F 2D
                                                                      336
0D20 9E
                                                                      337
ØD21 C7
                                                                      338
0D22 FC80
0D24 BE
                                                                      339
                                                                      \bar{3}\bar{4}\acute{0}
                                                                                                SHL ..SEE IF MQ >0(/)
CHI CR ..SEE IF DIVND POSTIVE(/)
ANI #80 ..BY TAKE OUT SIGN(/)
BNZ *+#06 ..(/)
0D25 FE
                                                                      34 ī
0D26 9C
                                                                     342
0D27 FA80
0D29 3A2F
                                                                     343
                                                                                                BNZ *+#06 ..(/)
BNF D9 ..EXIT WITH DF=1(/)
                                                                                              BNZ **#06 ..(/)
BNF D9 ..EXIT WITH DF=1(/)
BR DDQ ..OK(/)
BDF DVXX ..IF NEGATIVE, THEN OUT(/)
CHI MQ ..SEE IF MQ=0?(/)
BNZ DDQ ..IF NOT, THEN NO PROBLEM(/)
CLO MQ ..MAKE SURE MQ.0 IS 0 TOO(/)
BZ D9 ..IF YES, THEN RETURN WITH DF=1(/)
BR DDQ ..OR ELSE CO TO DIVIDE(/)
CHI CR ..SEE IF THE OPERANDS SIGNS DIF
XOR ..BY COMPARING SIGN BITS(/)
SHL ..AND TAKE OUT THAT BIT(/)
BDF D10+#11 ..IF SINGS DIFF, IT'S OK(/)
CHI CR ..OTHERWISE TEST SIGN OF DIVND(/)
SIL ..IF POSITIVE, RETURN WITH DF=1(/)
BNF D9 ..RETURN WITH DF=1(/)
INC MA ..SEE IF LOW BIT OF AC IS 0 OR 1(/
LDX ..LOAD THAT IN D(/)
DEC MA ..REMEMBER TO RESET MA(/)
SHR ..SHIFT THAT BIT OUT(/)
CLO AC ..IF AC IS NOT 0 ,NOT PROBLEM(/)
BNZ DDQ ..GO TO DIVIDE(/)
CHI AC ..READY TO CHECK #80 IF LOW BIT AC
BDF **#06 ..(/)
BZ D9 .NO GOOD, RETURN WITH DF=1(/)
BR DDQ ..ANY THING ELSE IS OK(/)
XRI #80 ..IF AC.1 IS NT #80(/)
BNZ DDQ ..IT'S OK(/)
SMI #00 ..DF IS SET TO 1(/)
: GHI CR ..PUT ORGINAL DIVND(/)
PHI MQ ..INTO MQ(/)
CLO CR ..(/)
PLO MQ ..(/)
SEP RETN ..AND RETURN WITH DF=1(/)
                                                                      344
0D2B 3B00
                                                                     345
0D2D 3000
                                                                      346
9D2F 3399
                                                                      347
ØD31 9E
                                                                     348
0D32 3A00
                                                                     349
                                                                     356
0D34 8E
0D35 3200
                                                                     251
9D37 3000

9D39 9C
                                                                     352
                                                                     353 DVH:
 OD3A F3
                                                                     354
 OD3B FE
                                                                     355
0D3C 3314
                                                                      356
0D3E 9C
                                                                      357
 ODSF FE
                                                                      358
0D40 3B90
                                                                     359
0D42 1D
                                                                     360
ОД43 ГО
                                                                     361
6D44 2D
                                                                     362
6D45 F6
                                                                      363
0D46 8F
0D47 3A00
0D49 9F
                                                                      364
                                                                     365
                                                                     366
OD4A
              3350
                                                                      367
0D4C 3200
                                                                     368
0D4E 3000
                                                                     369
0D50
              FB89
                                                                     370
0D52 3A00
                                                                     371
0D54 FF00
                                                                     372 D9:
eD56 9C
                                                                     373 DVXX:
OD57 BE
                                                                     374
0D58 8C
                                                                     375
                                                                                                SEP RETN
0D59 AE
                                                                     376
                                                                                                                               .. AND RETURN WITH DF=1(/)
0D5A D5
```

```
0D5B 9C
                                                                             ..PUT ORGINAL DIVND(/)
                                         378 DDQ:
                                                            CHI CR
                                                         PHI MQ ..BACK INTO MQ(/)
GLO CR ..(/)
ODSC BE
                                         379
ODSD &C
                                         380
ODSE AE
                                         381
                                                       PLO MQ
OD5F
                                                         382
OD5F
                                         383
                                                         .. ****CALL DIVQ
OD5F
                                         384
                                                        CHI MQ . LOOK AT DIVIDEND SIGN
SHL . IF POSITIVE,
LDI #90 . PLAN TO BEGIN WITH SUBTRACT,
LSNF . (ALSO SAVE SIGN OF DIVIDEND)
LDI #50 . OTHER WISF BEGIN WITH ADD.
PLO CR . SET ITERATION COUNT IN CR.0
0D5F 9E
                                         385 DIVQ:
0D60 FE
                                         386
0D61 F890
                                         387
0D63 C7
                                         388
0064 F850
                                         389
0D66 AC
0D67 8E
                                         390
                                                                  MQ ... SHIFT MQ LEFT 1 BIT ... SHIFT LEFT MQ.0
                                         391
                                               DVL:
                                                           GLO MQ
OD68 FE
OD69 AE
                                         392
                                                         SHL
                                                        PLO MQ
CHI MQ
SHLC
                                         393
0D6A 9E
                                                                   O ... SAME FOR HIGH BYTE ... SHIFT LEFT WITH CARRY
                                         394
0D6B
        7E
                                         395
OD6C BE
                                                         PHI MQ ..
                                         396
                                                        SHL ..SHIFT AC.0
PLO AC ..
GHI AC ..
SHLC ..SHIFT
PHI AC
OD6D 8F
OD6E FE
                                         397
                                                                         .SHIFT AC LEFT 1 BIT
                                         398
0D6F AF
0D70 9F
                                         399
                                         400
                                                        SHLC ...SHIFT WITH CARRY
PHI AC
BNF *+#03 .. BIT SHIFTED OUT OF AC.1,
INC MQ .. GOES INTO MQ.0
0D71 7E
                                         401
0D72 BF
                                         402
0D73 3B76
                                         403
0D75 1E
                                         404
9D76 ED
9D77 8C
9D78 F3
9D79 FE
9D7A 1D
                                         405
                                                         SEX MA ..
                                                                  R .. NOW, WAS THAT ADD, OR SUBTRACT?
. IT DEPENDS ON SAVED FLAG,
...AND SIGN OF DIVISOR
                                         406
                                                         GLO CR
                                                         XOR ..
                                         407
                                         408
                                                         SHL
                                                                      ..MQ.0-(MA.0)
                                         409
                                                         INC MA
OD7B SE
                                                         GLO MQ
                                         410
6D7C 3B00
                                                       DEC MA ...FIX X PTR
CHI MQ ..DO THE SAME FOR HIGH BYTE
SMB ..REMEMBER THAT BORROW BIT
BR DSM ...SKIP OVER ADD STEPS
ADD ..MQ+(MA)
PLO MQ
DEC MA ...DO ...
                                         411
                                                         BNF DSA
                                                                       .. IF NO FLAC, MQ. 0+(MA. 0)
9D7E F7
                                         412
6D7F AE
6D80 2D
                                         413
9D81 9E
                                         415
0D82 77
                                         416
0D83 3000
                                         417
0D85 F4
                                         418 DSA:
0D86 AE
                                         419
                                                        DEC MA .. DO THE SAME FOR HIGH BYTE CHI MQ ..
0D87 2D
                                         420
                                                        ADC ..ADD WITH CARRY
PHI MQ ..STORE BACK TO MQ.1
DEC CR .. COUNT DOWN ITERATION COUNTER
GLO CR
ANI #75
6D88 9E
                                         421
0D89 74
                                         422
ODSA BE
                                         423
                                               DSM:
0D8B 2C
ODSC SC
                                         425
0D8D FA7F
0D8F 3B94
0D91 1F
                                         426
                                                         ANI #7F
                                                        BNF *+#05 .. TEST CARRY OUT OF ADD/SUBTRACT INC AC .. IF 1, SHIFT INTO QUOTIENT, ORI #80 .. AND FLAG NEXT OP AS SUBTRACT. PLO CR .. OTHERWISE IT'S ADD. ANI #3F .. LOOK AT COUNTER:
                                         427
                                         428
0D92 F980
                                         429
OD92 TO00
OD94 AC
OD95 FA3F
                                         430
                                         431
```

```
BNZ DVL .. IF NOT 0, LOOP BACK; BDF_DVR .. AT END, CHECK REMAINDER ADJUST.
0D97 3A67
                                      432
0D99 3300
                                       433
                                               DVC: INC AC
0D9B 38
                                       434
                                                     INC AC .. (FINAL DIVIDE STEP)
XOR .. BE SURE TO GET POLARITY
SHL .. OF ADJUSTMENT RIGHT...
OD9C 1F
                                       435
OPOD F3
ODOE FE
ODOF 1D
                                      436
                                       437
                                                    INC MA .. YES, ADD DIVISOR BACK ON,
GLO MQ .. TO CORRECT FOR FINAL SUBTRACT,
BPF DVM .. (ADDING NEGATIVE IS SUBT.)
                                       438
ODÁO SE
                                       439
ODA1 3300
ODA3 F4
                                      440
                                                      ADD .. WHICH SHOULDN'T HAVE.
                                       441
ODA4 AE
ODA5 2D
                                                     PLO MQ
DEC MA
                                       442
                                      443
ODA6 9E
                                                     CHI MQ
                                       444
                                                     ADC .. ADD WITH CARRY
BR DVR-#01
ODAZ 74
ODAS 20FF
                                      445
                                      446
                                              DVM: SM .. SAME THING,
PLO MQ .. EXCEPT, FOR NEGATIVE DIVISOR.
DEC MA
ODAA F7
                                       447
ODAE AE
ODAC 2D
ODAD 9E
                                       448
                                       449
                                                     CHI NQ
                                       450
ODAE 77
ODAF BE
                                       451
                                                     SMB
                                       452
                                                     PHI MQ
6DE0 9E

0DB1 3AB6

0DB3 8E

0DB4 3200

0DE6 8C
                                              DVR: CHI MQ .. IF REMAINDER IS NOT ZERO,
BNZ *+#05
GLO MQ
                                       453
                                      454
                                       455
                                                     BZ DVN .. BUT IT IS; NO PROBLEM. GLO CR .. IF NOT ZERO, SHL .. IT SHOULD BE SAME SIGN
                                       456
                                       457
ODB7 FE
                                       458
                                                     SHL ...
ODB8 FE
                                                             .. AS ORIGINAL DIVIDEND.
                                       459
ODE9 9E
                                       460
ODBA CF
ODBB FB80
                                                      LSDF
                                       461
                                      462
                                                      XRI #89
ODBD FCGO
ODEF 3B9C
                                               ADI #80 .. IF NOT, WE NEED BNF DVC .. ONE MORE DIVIDE ITERATION. DVN: LDX .. FINALLY, IF DIVISOR NEGATIVE,
                                       463
                                       464
ODC1 FO
                                       465
                                                     SHL
BNF DVX ..(IT'S NOT; WE ARE
GLO AC .. COMPLEMENT QUOTIENT,
XRI #FF .. BY INVERFING IT,
ODC2 FE
                                       466
ODC3 3B00
                                       467
                                                                        .(IT'S NOT: WE ARE DONE)
ODC5 8F
ODC6 FBFF
                                      468
                                      469
ODCO AF
ODCO OF
ODCA FEFF
ODCC OF
                                       470
                                       471
                                                     GHI AC
                                                      XRI ≠FF
                                       472
                                              PHI AC
INC AC . THEN INCREMENTING
ADI #00 . ALSO CLEAR DF.
DVX: SEP RETN . DF=0 IF DIVIDE SUCCESSFUL.
                                       473
ODCD 1F
                                       474
ODCE FC00
ODDO D5
                                      175
                                      476
477
ODD1
                                                     ODD 1
                                       478
ODD 1
                                       479
ODD 1
                                       480
ODD 1
                                       481
ODD1
                                       482
ODD1
                                       483
                                               ADDOP: LDA LINK .. FETCH OPERAND ADDRESS PHI MA .. TO REGISTER MA
ODD1 46
                                       484
ODD2 ED
                                       485
```

```
LDA LINK
PLO MA . FALL INTO ADD
. 16-BIT ADD TO AC, OPERAND ADDRESS IN REG
. CALL HERE IF OPRN ADDRESS
. IS IN REGISTER MA
 ODD3 46
                                       486
 ODD4 AD
                                       487
 eDD5
                                       488
 ODD5
                                        489
 ODD5
                                       490
 ODD5
                                       491
                                                       .. ***AC=AC+M(R(MA))
 ODD5
                                       492
                                                       .. ******** (TO CALL, WRITE) *******
ODD5
                                       493
                                                       .. ****CALL ADD
ODD5
                                       494
                                               ADD: SEX MA
ODDS LD
                                                      SEX MA ...CHECK SIGN BIT OF AC GHI AC ..GET THE OPERAND XOR .. AND OPERAND @MA
                                       495
0DD6 -9F
0DD7 F3
0DD8 FB80
                                       496
                                       497
                                                      XOR ..AND OPERAND @MA
XRI #80 ..RESULT A 1 IF DIFF
STR SP ..STORE ON STACK
INC MA ..POINT TO LOW 8 BITS
GLO AC .. FETCH AC LOW 8
ADD .. ADD LOW 8 FROM MEMORY
PLO AC .. PUT IT BACK
DEC MA .. POINT TO HIGH 8 MEMORY LOCATION
CHI AC
                                       498
ODDA 52
                                       499
 ODDE 1D
                                       500
 ODDC 2F
                                       501
 ODDD F4
                                       502
ODDE AF
                                       503
        2D
                                       504
ODEO OF
                                       505
                                                       GHI AC
                                                      ADC ..ADD HIGH BYTE WITH CARRY
PHI AC .. PUT IN AC.
LDN SP ..LOAD THE STORED COMPARING SIGN BI
SHL ..RESET STACK PTR
BNF ADDRT+#01 ..NOT POSSIBLE
GHI AC ..OTHERWISE SEE IF SUM IS RIGHT
XOR ..BY COMPARING SIGN BITS
TO SHL ..SHIFT OUT 0 INTO DE
ODE1 74
                                       596
ODE2 BF
                                       507
ODE3 62
                                       508
ODE4 FE
                                       509
0DE5 3B01
0DE7 9F
                                       510
                                       511
0DE8 F3
                                       512
ODE9 FE
                                       513 ADDRT:
ODEA D5
                                       514
                                                      SEP RETN
                                                                       . RETURN TO MAIN
ODEB
                                       515
ODEB
                                       516
                                                      .. 16-BIT CONSTANT ADD TO AC.
.. CALL HERE FOR ADD CONSTANT TO AC
ODEB
ODEB
                                       517
                                       518
                                                       .. ****AC=AC+CONSTANT
ODEB
                                                      519
ODEB
                                       520
ODEB
                                       521
522
                                            ADDCON: GLO LINK .. COPY LINK TO MA PLO MA GHI LINK
ODEB 86
ODEC AD
                                       523
ODED 96
ODEE BD
                                       524
                                                     PHI MA
INC LINK .. INCREMENT PAST DATUM
INC LINK
                                       525
                                       526
ODEF 16
0DF0
                                       527
ÖDF1 30D5
ODF3
                                       528
529
                                              ADDST: CHI SP .. COPY STACK POINTER PHI MA .. TO MA REGISTER GLO SP
ODF3
                                       530
0DF3 92
0DF4 BD
                                       531
                                       532
ODF5 82
ODF6 AD
                                       533
                                                      PLO MA
INC MA .. ADVANCE TO SUB-TOP (@)
                                       534
ODF7 1D
                                       535
ODF8 1D
                                       536
ODF9 1D
                                       537
                                                      INC MA
                                                                       (@)
                                                      INC MA .. (@)
BR ADD .. GO DO IT
ODFA 30D5
                                       538
ODFC
                                       539
```

```
ODEC
                                  540
ODFC
                                   541
                                                . .
                                                    PUSH AC INTO STACK
STACK POINTER = SP
ODFC
                                   542
                                                . .
ODEC
                                  543
                                                . .
OPEC
                                                    ******** (TO CALL, WRITE) ******
                                  544
                                         .. ****CALL PUSHAC
.. PUSH AC (UNDER TOP OF STACK)
PUSHAC: GHI SP .. COPY STACK POINTER TO MA
PHI MA
GDFC
                                  545
ODEC
                                  546
                                  547
548
ODFC
ODFD BD
ODFE 82
ODFF AD
OEGO 1D
                                  549
                                                GLO SP
                                   550
                                                PLO MA
                                   551
                                                INC MA .. NOW SLICE OFF TOP 2 BYTES,
0E01
0E62
        1D
                                   552
                                                INC MA
                                   553
                                                SEX SP
                                                SEX SP
LDN MA .. TO MAKE A 2-BYTE HOLE.
STXD
DEC MA
LDN MA
OEO3 OD
                                   554
0E94
       73
                                   555
0E05 2D
                                   556
CEO6 OD
                                  557
0E07 73
0E08 9F
                                  558
                                                STXD
                                                GHI AC .. NOW STUFF AC INTO THE HOLE. STR MA
                                  559
0E99 5D
                                  560
                                                CLO AC
INC MA
GEGA SF
                                   561
OEOB ID
                                  562
CECC 5D
                                  563
                                                STR MA
                                         DEC MA .. LEAVE MA POINTING TO IT.
SEP RETN .. (AC UNCHANGED)
.. PUSH CR, MA, MQ (UNDER TOP OF STACK)
PUSHCQ: GLO MA .. FIRST PUSH MA ONTO TOP
OEOD 2D
                                  564
OEOE D5
                                  565
OFOF
                                  566
0E9F 8D
0E10 E2
                                  567
                                  568
                                                SEX SP
CE11 73
OE12 9D
                                  569
                                                STXD
                                  570
571
572
                                                GHI MA
STR SP
0E13 52
0E14 92
                                                CHI SP .. NOW COPY SP TO MA
0E15 BD
                                  573
                                                PIII MA
0E16 62
0E17 AD
                                  574
                                                GLO SP
                                  575
                                                PLO MA
0E18 22
                                  576
                                                DEC SP
                                                INC MA .. THEN ADJUST IT
                                               INC MA .. TO POINT INTO OLD TOP CLO MQ .. CONTINUE PUSHING, MQ STXD GHI MQ STXD LDN M.
0E19 1D
                                  577
OE 1A
                                  578
                                  579
580
0E1B
       1D
OEIC EE
0E1D 73
                                  581
ØE1E 9E
                                  582
0E1F 73
0E20 0D
                                  583
                                                LDN MA
                                  584
0E20 0B
0E21 73
0E22 2D
0E23 0D
                                  585
                                                STXD
                                                DEC MA
LDN MA
                                  586
                                  587
0E24
       73
                                  588
                                                STXD
0E25 9C
                                  589
                                                GHI CR .. FINALY INSERT CR IN HOLE
0E26 5D
                                  590
                                                STR MA
0E27 11
                                  591
                                                INC MA
0E28 8C
0E29 5D
                                  592
                                                GLO CR
                                  593
                                                STR MA
```

```
0E2A D5
0E2B
                              594
                                          SEP RETN .. (MA IS CARBAGE OUT)
                              595
0E2B
0E2B
0E2C 92
0E2D BD
                              596
                                           .. POP STACK INTO MQ, MA, CR (UNDER TOP OF
                                    POPCQ: INC SP
GHI SP .. COPY STACK POINTER TO MA
                              597
                              598
                              599
                                          PHI MA
0E2E 62
0E2F AD
0E30 1D
                              600
                                          GLO SP
                                          PI.O MA
INC MA .. ADJUST POINTER TO CR DATUM
                              601
                              602
6E31 1D
6E32 1D
                                          INC MA
                              603
                              604
ÕESS ÎD
                              605
                                          INC MA
ÖESÄ ID
                              606
                                          INC
                                               MA
ÖE35 1D
                              607
                                          INC MA
0E36 4D
                              608
                                          LDA NA .. FETCH IT
OEST BC
                                          PHI CR
                              609
@E38 @D
                              610
                                          LDN MA
OES9 AC
                                          PLO CR
DEC MA .. COPY TOP OF STACK INTO GAP
                              611
OESA 2D
                              612
0E3B 42
                                          LDA SP
                              613
OESC 5D
                                          STR MA
                              614
GESD 1D
GESE 42
GESF 5D
                              615
                                          INC MA
                              616
                                          LDA SP
                                          STR MA
0E40 42
0E41 BE
                                                   .. THEN POP MQ
                              618
                                          LDA SP
                                          PIII MQ
                              619
0E42 42
                              620
                                          LDA SP
                                          PLO NO.
LDA SP .. FINALLY POP MA
PHI MA
OE43 AE
                              621
0E44 $2
                              6\overline{2}\overline{2}
0E45 BD
0E46 02
0E47 AD
0E48 D5
                              \tilde{6}\tilde{2}\tilde{3}
                              \begin{array}{c} 624 \\ 625 \end{array}
                                          LDN SP
                                          PLO MA
                              626
                                          SEP RETN
0E49
                              627
                                          .. 16-BIT ACCUMULATOR LOAD (ADDRESS IN CALL
0E49
                                          .. ****AC=OPRN
                              628
0E49
                                          .. ******** (TO CALL, WRITE) ******
                              629
0E49
                              630
                                          .. ****CALL LOADOP ; ,A(OPRN)
0E49
                              631
                                    LOADOP: LDA LINK .. FETCH ADDRESS PHI MA .. TO MA REGISTER LDA LINK
0E49 46
                              632
OE4A BD
                              633
0E4B 46
0E4C AD
                              634
                                          635
0E4D
0E4D
0E4D
                              636
                              637
                              638
0E4D
                              639
OE4D
                              640
                                             ********** (TO CALL, WRITE) *******
                              641
0E4D
                                             ***CALL LOAD
CE4D
                              642
                                    LOAD: LDA MA .. FETCH HIGH 8
PHI AC
0E4D 4D
                              643
OF4E BF
                              644
0E4F 4D
0E50 AF
0E51 D5
                              645
                                          LDA MA .. NOW LOW 8
                                          PLO AC .. LEAVE MA AT NEXT DOUBLE-BYTE SEP RETN .. GEE, THAT WAS QUICK.
                              646
```

```
0E52
                              648
0E52
                                         .. 16-BIT ACCUMULATOR LOAD FROM CONSTANT IN
                              649
                                         0E52
                              650
0E52
                              651
0E52
                              652
                                         .. ****CALL LODCON : , CONSTANT
0E52
                              653
                                    LODCON: LDA LINK .. FEICH HIGH 8
PHI AC
LDA LINK .. THEN LOW 8
 6E52
                              654
655
 0E53 BF
0E54 46
0E55 AF
                             656
                                         PLO AC
SEP RETN
                              657
0E56 D5
                              658
0E57
                              659
                                         .. 16-BIT ACCUMULATOR STORE (ADDRESS IN CAL
0E57
                              660
0E57
                                         .. ****OPRN=AC
                              661
                                         .. ********* (TO CALL, WRITE) *******
0E57
                             662
0E57
                                         .. ****CALL STOROP ; , A(OPRN)
                             663
0E57
                              664
0E57 46
                                    STOROP: LDA LINK .. FETCH ADDRESS INTO MA
                              665
OE53 ED
                                         PHI MA
LDA LINK
                             666
0E59 46
                             667
GESA AD
                                         PLO MA .. THEN FALL INTO STORE
.. 16-BIT ACCUMULATOR STORE (ADDRESS IN MA)
                             668
0E5B
                             669
                             679
671
672
ØE5B
                                         .. ****M(R(MA))=AC
ØE5B
                                         .. ********* (TO CALL, WRITE) *******
ØE5B
                                         .. ****CALL STORE
@E5B
                             673
0E5B 9F
                             674
                                    STORE: CHI AC .. FIRST HIGH 8
                             675
676
677
678
679
                                         STR MA
INC MA .. INCREMENT MA, SINCE STR DOESN'T
0E5C 5D
0E5D 1D
ØESE 8F
                                         GLO AC .. NOW LOW 8
STR MA
0E5F 5D
0E60 1D
                                         INC MA .. LEAVE MA POINTING TO NEXT WORD SEP RETN .. QUIT
0E61 D5
@E62
                             681
0E6\overline{2}
                             682
                                         0E62
                             683
0E62
                             684
ØE62
                             685
0E62
                             686
                                         .. ****CALL COMOP ; , A(OPRN)
0E62
                             687
                                   COMPOP: LDA LINK .. FETCH ADDRESS PHI MA .. TO MA REGISTER LDA LINK
0E62
      46
                             688
0E63 BD
                             689
0E64 46
0E65 AD
                             690
                             69 i
                                         PLO MA
0E66
                             692
                                            16-BIT COMPARE, OPERAND ADDRESS IN REGIS
                                      .. CALL HERE IF OPERAND
.. ADDRESS IN REGISTER MA
.. ****AC-M(R(MA)) (DF SET IF 0 OR +)
.. ****************
.. *****CALL COMP
0E66
                             693
0E66
                             694
0E66
                             695
0E66
                             696
0E66
                             697
0E66
                             698
0E66 ED
0E67 9F
                                   COMP: SEX NA .. COMPARE HIGH 8 FRST
GHI AC ..CHECK IF SIGN OF OPERANDS ARE SA
XOR ..BY LOOKING AT THE HICHEST SIGN BIT
                             699
                             700
0E68 F3
                             701
```

```
0E69 FAS0
                                702
                                            ANI #80 ..RESULT A '1' IF NEGATIVE BNZ CNE ..IF NOT, THEN GO TO CNE
                                           BNZ CNE
GIII AC
CE6B 3A00
                                703
OE6D 9F
                                704
0E6E F7
0E6F 3A00
                                705
                                            SM
                                            BNZ CMPX .. NOT EQUAL QUITS
INC MA .. TRY LOW 8
                                706
0E71 1D
0E72 BF
                                707
                                768
                                            GLO AC
0E73 F7
0E74 2D
0E75 38
                                709
                                            SM
                                710
                                            DEC MA .. LEAVE MA POINTING TO IT
                                            ,#38
                                711
0E76 F4
0E77 DS
                                                  ADD
                                712
                                     CNE:
                                                          .SEE IF OPERAND IS NEGATIVE
                                                   SEP RETN ..DF=1 IF AC>=(MA)
                                713
                                     CM'X:
0E78
0E78
                                714
715
716
717
0E78
QE78
0E78
0E78 16
                                           .. TEST 16-BIT ACCUMULATOR SIGN/ZERO
                                718
                                            INC LINK ..SKIP OVER NON ZERO RETURN INC LINK ..
                                719
0E79 16
0E7A D5
                                720
                                           r: CHI AC .. FIRST LOOK AT SIGN SHL ..SET DF IF MINUS GIII AC .. NOW CHECK FOR 6 BNZ TEST-#03 .. NO. GLO AC BZ TEST-
                                721
                                722
                                       TEST: CHI AC
OFTB 9F
0E7B 9F
0E7C FE
0E7D 9F
0E7E 3A78
0E80 8F
0E81 327A
0E83 3078
                                723
724
                                725
                                7\overline{2}_{0}
                                            727
                                \frac{728}{729}
0E85
OE85
                                730
0E85
                                731
0E85
                                732
                                               ****CALL POPAC
0E85 FF00
0E87 C8
0E88 FC00
                                      POPAC: SMI #00 .. SET DF TO REMEMBER THIS ENTRY
                                733
                                      LSKP
POP: ADI #00 .. CLEAR DF FOR THIS ENTRY
INC SP
                                734
                                735
0E8A 12
CE8B 92
                                736
                                            CHI SP .. COPY SP TO MA
                                737
OESC BD
OESD 82
OESE AD
                                738
                                            PHI MA
                                739
                                            GLO SP
                                740
                                            PLO MA
                                741
                                            INC MA .. ADJUST TO SUB-TOP OF STACK INC MA
6E8F
      1D
0E90 1D
                                742
0E91 3B98
                                743
                                            BNF *+#07
0E93 4D
                                744
                                            LDA MA .. POPPING INTO AC. GET DATUM
0E94 BF
                                745
                                            PIII AC
0E95 ØD
                                746
                                            LDN
                                                 MA
0E96 AF
0E97 2D
                                747
                                            PLO
                                                 AC
                                748
                                            DEC
                                                 MA
0E98 42
                                749
                                            LDA
                                                 SP
                                                     .. NOW CLOSE UP THE GAP
                                            STR MA
INC MA
0E99 5D
                                750
OE9A 1D
                                751
                                            LDN
STR
0E9B 02
                                732
                                                 SP
GE9C 5D
                                753
                                                 MA
0E9D
      1 D
                                754
                                            INC
                                                  MΔ
őÉ9É D5
                                                 RETN .. MA POINTS TO NEW SUB-TOP
                                755
                                            SEP
```

```
0E9F
                                   756
                                                     DECIMAL TO BINARY CONVERSION

***** AC=DECIMAL NUMBER OF N BYTES
0E9F
                                   757
0E9F
                                   758
OFOF
                                   759
                                                     .. DECIMAL NUMBER = SIGN, NN, ...., N1, NO
OFOF
                                   760
                                                         SIGN=#0B +
                                                     . .
                                                .. SIGN=#0D -
.. NO=10**0 DIGIT
.. NI=10**1 DIGIT
.. ********************************
.. **** CALL CDB; ,A(NUMBER); ,LENGTH
LDA LINK ..GET NUM ADDRESS
PHI AR ..AND STORE IN RA.
LPA LINK
PLO AB
OFOR
                                   761
OLOF
                                   762
0E9F
                                   763
                                  764
765
OE9F
0E9F
CEOF.
        46
                                   766 CDB:
OEAO BA
                                   767
0EA1 46
                                   768
                                                PLO AR
LDA LINK
GEA2 AA
                                   769
                                                               ..GET LENGTH
CEAS 46
                                   773
                                                              .. MINUS SIGN BYTE .. AND STORE IN RB.
                                                SMI #01
PLO NR
CEA4 FF01
                                   771
                                  772
773
774
OEA6 AB
OEA7 PSOO
OEA9 AF
                                                LDI #00
PLO AC
                                                              ..CLEAR RF
OEAA BF
                                   775
                                                PIII AC
OFAB OA
CEAC FBOD
CEAE BB
                                   776
                                                LDN AR
                                                                .. CHECK SIGN BYTE
                                   777
                                                 RRI #OD
                                                                .. MINUS?
                                                PHI NR ..INTO NR.1

INC AR ..GRAB THE FIRST DIGIT
SEX SP ..FIX X PNTR
LDN AR ..CLEAR HIGH BYTE (FOR ASCII)
                                   778
OEAF IA
                                   779 LOOP:
                                   789
OEDI GA
                                   781
732
783
GEB2 FAOF
                                                ANI #0F
0EB4 52
                                                            ..PUT IT BACK
..ADD THAT DIGIT TO ACCUM
                                                STR SP
OEBS OF
                                                GLO AC
                                   784
GEB6 F4
                                   785
                                                ADD
                                                PLO AC
GIH AC
ADGI #00 ..REMEMBER CARRY OVER
OEBZ
       \Lambda F
                                   786
GEBS 9F
                                   787
6ED9 7C00
                                   788
                                                PHI AC
BDF OVFLW
OEBB BF
                                   789
OEDC 3300
                                   790
                                                                    .EXECTEDS ACCUM LIMIT?
OEBE 2B
OEBF 8B
                                                DEC NR . DEC DIGIT COUNTER
GLO NR . SEE IF IT IS 0?
BZ FINAL . YES, THEN DONE
                                   791
                                   792
OECO 3200
                                   79\overline{3}
OEG2 SF
OEG3 FE
                                   794
                                                GLO AC
                                                            ..OTHERWISE MULTIPLTY THE ACC BY 10
                                   795
                                                SIII.
OEC4
       73
                                   796
                                                STXD
0EC5 9F
                                                GHI AC
SHLC
                                   797
OEC6
                                                           .. CARRY OVER
       7E
                                  798
       73
                                   799
                                                STXD
OECS SSFE
OECA F802
                                  800
                                                 BDF OVFLW-#02 .. EXCEEDED ACC LIMIT
                                              LDI #02
S: STR SP ..LOOP COUNT
                                  891
0ECC 52
                                  802 MPY3:
OECD 8F
OECE FE
OECF AF
                                                SHL ... NOW SHIFT AC OVER 4 TIMES MORE PLO AC
                                                GLO AC
                                  £03
                                  804
                                   805
GEDO OF
                                                GIII AC
                                   806
                                                              .. SAME FOR AC. 1
0ED1 7E
                                                SIILC
                                   807
OED2 BF
                                  808
                                                PHI AC
0E93 33FE
                                  800
                                                BDF OVFLW-#02 ... IF OVFLOW, RESET STACK
```

```
LDN SP ..CHECK LOOP COUNT
BZ MPY10 ..AFTER MULPLY BY 8
SMI #01 ..OR ELSE DEC LOOP COUNT
BR MPY3 ..BACK FOR MORE ADDITION
10: INC SP ..RECOVER LOOP COUNT
GHI AC ..ADD HIGH BYTE
ADD ACC TO ACC
0ED5 02
0ED6 3200
                                     810
                                     811
OEDS FF01
                                     812
OEDA 30CC
OEDC 12
                                     813
                                     814
                                           MPY10:
OEDD 9F
                                     815
OEDF F4
                                                   ADD ..ADD BACC TO 2ACC PHI AC
                                     816
CEDF BF
                                     817
                                                               LW-#01 ..RESULT DF IF OVFLOW
..RESET STACK PNTR
..SAME FOR AC.O
                                                   BDF OVFLW-#01
INC SP ..RES
OEEØ 33FF
                                     818
0EE2 12
                                     819
OEE3 SF
                                                   GLO AC
                                     820
ÖEE4 F4
                                     821
                                                    ADD
ØEE5 AF
                                     822
                                                   PLO AC
OEE6 9F
OEE7 7COO
OEE9 BF
                                                                .. FOR CARRY OUT
                                                   GHI AC
                                     823
                                                   ADCI #00
                                     824
                                                   PHI AC
BNF LOOP
                                     825
                                                             OP ...IF NOT OVELW, CO BACK FOR MORE
...SKIP STACK RESET
...RESET STACK PTR
PEEA SBAF
OEEC C8
                                     826
                                     827
                                                   LSKP
ØEEB 12
                                     328
                                                   INC SP
ØEEE
       12
                                                   INC SP
                                     829
                                                         SEP RETN ..DF=1
GHI AC ..CHECK IF EXCEED MAX POS NUM L
OEEF D5
                                     830 OVFLW:
GEFO 9F
                                     831 FINAL:
CEF1 FC80
                                                   ADI #80
                                     832
                                                  BNZ CP ... IF NOT, GO TO COMP
GHI NR ... SEE IF IT IS POSITIVE
ADI #FF ... SET DF ACCORDINGLY
SEP RETN
BDF *-#01 ... OVERFICE
GHI NR
9EF3 3A99
9EF5 8F
                                     833
                                     834
ØEF6 3A00
                                     835
OEFS 9B
                                     836
ÖEF9 FCFF
OEFB D5
OEFC 33FB
                                     837
                                     838
                                                   BDF *-#01 ..OVERFLOWED!
GHI NR ..TEST FOR SIGN
BNZ EXIT ..IF POS, DONE
GLO AC ..IF NEC, SUBTRACT FROM 0
                                     839 CP:
OEFE 9B
OEFF CAOO
                                     840
                                     841
0F01 8F
0F02 FD00
                                     842
                                     843
                                                   SDI #00
0F04 AF
0F05 9F
                                     844
                                                   PLO AC
                                                   GHI AC
SDBI #00
                                     845
0F06 7D00
0F08 BF
0F09
                                     846
                                                   PHI AC
                                     847
                                     848
0F09
0F09
                                                        849
                                     850
0F09
                                     85 1
6F09
                                     852
                                                            SIGN=#0B +
0F09
                                     853
                                                            S1CN=#0D -
                                                        0F09
                                     854
oFo9
                                     855
0F09
                                     856
0F02
                                     857
                                                    SÉP BETN
LDA LINK
0F09 D5
                                     858 EXIT:
                                                   LDA LINK ..GET THE ADDRESS
PHI AR ..AND STORE IN RA
LDA LINK ..SAME FOR LOW BYTE
0F0A 46
                                     859 CBD:
OFOB BA
                                     860
0F0C 46
                                     86 t
OFOD AA
                                     862
OFOE 46
                                     863
                                                   LDA LINK
                                                                  .. GET LENGTH
```

```
OFOF FF01
                                                                     ..SUBTRAC FOR SIGN BYTE ..STORE IN NR.0
                                       864
                                                      SMI #01
 OF11 AP
                                       865
                                                      PLO NR
 0F12 BB
                                       866
                                                                     . AND NR. 1
                                                      PHI NR
 9F13 F89F
                                                                     .. NUM OF ITERATIONS .. STORE IN MA. 0
                                       86.7
                                                      LDI #0F
 OF15 AD
                                       868
                                                      PLO MA
0F16 9F
0F17 FE
0F13 F80B
                                       869
                                                      GHI AC
                                                                     .. TEST FOR SIGN
                                       879
                                                    SHL
                                       871
                                                      LD1 #0B
                                                                     .. IF DF=0, IT IS POS
0F1A 3B00
0F1C 8F
                                       872
                                                      BNF POS
                                                       GLO AC
SD1 #00
                                       873
                                                                     ..OTHERWISE CONVERT IT TO POS
OFID FD00
                                       1174
 OFIF AF
                                       875
                                                       PLO AC
GIII AC
 0F20 9F
                                       876
0F21 7D00
0F23 BF
                                       877
                                                       SDBI #00
                                                     PIII AC
LDI #OD
                                       878
0F24 F80D
0F26 C8
                                       879
                                                                    .. MINUS SIGN
                                       889
                                                      LSKP
 0F27 F800
                                       881
                                                      LDI #00
                                                     STR AR ... PUT IT IN SIGN BYT
GLO NR ... CHECK DIGIT COUNTER
BZ LOOP1-#02 ... GO BACK FOR MORE ITERATION
INC AR ... GO TO NEXT DIGIT
DEC HR ... DEC DIGIT CNTR
 0F29 5A
                                       882 POS:
 OF2A 8B
                                       883
ÖF2B 32FE
                                       884
OF2D 1A
OF2E 2B
                                       885
                                       886
0F2F 3627
                                       887
                                                      BR P08-#02
                                                                          ..GO BACK FOR MORE CLEAR
OFOI E2
                                                    SEX SP
GHI NR
PLO NR
                                       888
0F32 9B
                                       889
                                                                  .. RESET DIGIT CNTR
OF33 AB
                                       890
OF34 SF
                                                             CLO AC .. SHIFT BIT OF AC OUT
                                      891 L00P1:
OF35 FE
                                                     SIIL
                                       892
0F36 AF
0F37 9F
0F38 7E
                                                     PLO AC
                                      89\bar{3}
                                      894
                                                     GHI AC
                                                     SHLU .. SAME FOR AC.1
PHI AC
LDN AR
ADCI #60 ..ADD TO L
                                       895
OF39 BF
                                       896
0F3A 0A
0F3B 7C00
                                      397
                                       898
                                                                        .. ADD TO LOWEST DIGIT
0F3D 5A
                                                     STR AR
                                       899
OFSE CD
OFSF SA42
                                                                   ..FOR MORE ITERATION?
__..CONTINUE IF MORE ITERATION
                                       900
                                                     CLO MA
                                                    BNZ *+#03
SEP RETN
                                      901
0F3F 3A42
0F41 B5
0F42 6A
0F43 7E
0F44 5A
0F45 FF0A
0F47 3B4A
                                              END:
                                      902
                                                   F: LDN AR ..LOAD DIGIT'
SHLC ..SHIFT LEFT OVER ONCE
STR AR ..PUT IT BACK
SMI #0A ..NEED TO INC NEXT DIGIT?
BNF *+#03 ..SKIP IF NOT>10
STR AR ..ELSE UPDATE DIGIT
DEC AR ..GO TO NEXT DIGIT
DEC NR ..DEC DIGIT COUNT
GLO FIR ..CHECK IF 62
                                      903 NEXT:
                                      904
                                      905
                                      906
                                      907
0F49 5A
                                      908
OF4A 2A
                                      909
6F4B 2B
                                      910
OF4C SB
                                                                   ..CHECK IF 0?
..IF NOT, DO THE SAME FOR NEXT DI
..OVERFLOWED
                                      911
                                                    GLO NR
ŏF4ñ 3<u>442</u>
                                                            NEXT
                                      912
                                                    BNZ
0F4F 3341
0F51 2D
                                      913
                                                           END
                                                    DEC MA ..DEC NO OF SHIFTS
GHI JIR ..RESET ADDRESS PTR
0F52 9B
                                      915
                                                     STR SP
CLO AR
0F53 52
                                      916
                                                                   .. PUT DIGIT ON STACK
0F54 8A
                                      917
```

```
0F55 F4
                                 918
                                             ADD
0F56 AA
0F57 9A
                                  919
                                              PLO AR
                                             GHI AR
ADCI #00
                                  920
0F58 7C00
                                  921
                                             PIII AR
BR LOOP1-#62
OF5A BA
                                  922
0F5B C032
                                  923
0F5D
                                  924
OF5D
                                  9\overline{25}
                                              .. *****SUBROUTINE CALL (CDP1802 VERSION)***
                                  \tilde{92}6
OF5D
OF5D P3
OF5E E2
                                  927
                                         CALLR:
                                                A: SEP PC ..TO SUBROUTINE...
S: SEX SP ..POINT TO STACK
GHI LINK ..SAVE LINK ON STACK.
                                 928
929
                                         CALLS:
0F5F 96
0F60 73
                                  930
                                                STXD
0F61 86
                                  931
                                                GLO LINK
                                               STXD
GII PC
PHI LINK
GIO PC
PLO LINK
LDA LINK
0F62 73
                                  932
0F63 93
                                  933
                                  9\overline{34}
0F64 B6
0F65 83
                                  935
0F66 A6
0F67 46
                                  936
                                  937
0F68 B3
                                 938
                                                PHI PC
0F69 46
0F6A A3
                                 939
                                                LDA LINK
                                 940
                                                PLO PC
0F6B 305D
                                 941
                                                BR CALLR
                                                              ...JUMP TO SUBROUTINE.
OF6D
                                 942
                                              .. ****SUBROUTINE RETURN (CDP1802 VERSION)*
0F6D
                                 943
OF6D
                                 944
                                        RETUR: SEP PC ..RETURN TO MAIN ...
RETR: CHI LINK ..RESTORE RETURN ADDRESS
PHI PC ..INTO PC.
CLO LINK
cred D3
                                 945
0F6E 96
                                 946
0F6F B3
0F70 &6
0F71 A3
0F72 E2
0F73 12
0F74 72
                                 947
                                 948
                                 949
                                                PLO PC
SEX SP
                                 950
                                 951
                                                INC SP
                                                            ..ON STACK INTO LINK.
                                 952
                                                LDXA
OF75 A6
                                 953
                                                PLO LINK
0F76 F0
0F77 B6
                                 954
                                                LDX
                                 955
                                                PHI LINK
ØF78 306D
                                 956
                                                                 .. RETURN.
                                                BR RETNR
OF7A
                                 957
OF7A
OF7A
                                                ...ADDITIONS BY J.M.C.
...NOT SUPPORTED!!!!!
                                 958
                                 959
OF7A
OF7A
                                 960
                                                MOVB -- ROUTINE TO MOVE N BYTES
OF MEMORY FROM ONE LOCATION TO ANOTHER
..CALLING SEQUENCE:
                                 961
OF 7A
                                 962 ..
OF7A
                                 963
OF7A
                                                CALL MOVB; , A(SOURCE) , A(DEST) , NBYTES
                                 964
OF7A
                                 965
OF7A 46BD
                                 966 MOVB: @R6!->MA.1
0F7C 46AD
                                                @R6!->MA.0
                                 967
OF71: 46BA
                                 968
                                                @R6!->AR.1
0F80 46ΛΛ
0F82 46ΛΒ
                                                @R6!-> AR. 0
                                 969
                                 970
                                                @R6!->NR.0
0F84 4D5A1A
                                 971 MOVB01: @MA!->@AR: INC AR
```

```
972
973
0F87 2B8B3A84
                                              DEC NR; NR.0; BNZ MOVB01
OF8B D5
                                                                  . . DONE
                                              EXIT
                                974 ...
975 ...
976 ...
of8c
0F8C
OF8C
                                977 .. CALLING SEQ.: CALL DELAY; DCON
978 .. WHERE DCON IS A 2 BYTE CONSTANT.
979 .. DCON=(TIME-400)/24
OFSC
6F8C
ersc
0F8C
                                980 ..
                                              TIME IN MICROSECONDS
ØF8C
                                981
6F8C
      8C5222
                                982 DELAY: CR. 0-> @SP; DEC SP
                                              CR. 1-> @SP
@R6!-> CR. 1
@R6!-> CR. 0
6F8F 9C52
                                983
                                                                  .. COPY CR TO STACK
0F91 46BC
                                984
6F93 46AC
                                985
0F95 38
0F96 2C8C3A96
0F9A 9C3A96
                                986
                                              SKIP
                                              DEC CR; CR.0; BNZ DEL1
CR.1; BNZ DEL1
@SP!->CR.1
                                987 DEL1: DEC CR;
                                988
GF9D 42BC
                                989
OF9F FØAC
                                              @-> CR. 0
                                990
                                                                  .. RESTORE CR
OFA1 D5
                                991
                                              EXIT
OFA2
                                992
OFA2
                                993 ... >CVT
                                                     CONVERT BINARY (16 BIT)
                                                                                        TO ASCII
OFA2
                                              ... CALL CVT; , (NO. CHARS) . (CHARS AFTER ".")
                                994
OFA2
                                995
0F42
       46BC52
                                996 CVT:
                                              @LINK!->CR. I, @SP
OFA5
                                              @LINK!->CR. 0
      46AC
                                997
                                              AB. 0+@-> AR. 0
ENF *+6
AR. 1+1-> AR. 1
DEC AR
OFA7 SAF4AA
                                998
OFAC 9AFC01BA
                                999
                                                                 ..ADJUST AR
                               1000
OFBO 2A
                               1001
GFB1 F800BEAE
                               1002 DIV10: 0-> M9.1, MQ.0
1003 DLOOP: AC.0-10-> AC.0
OFBS SFFFØAAF
                                              INC MQ
BDF DLOOP
OFB9 1E
                               1004
                                                                  .. BUMP QUOTIEN'T COUNTER
OFBA 33B5
                               1005
OFBC 9FFF01BF
                                              AC. 1-1-> AC. 1 .. PROCESS HI BYTE BORROW
                               1006
OFCO 23B5
6FC2 2E
                                              BDF DLOOP
DEC NQ
                               1007
                                              DEC NO ... AR HAS ROLLED OVER NEG AC.0+#3A->@AR ... CONVERT REMAIN TO ASCII
                               1008
OFC3 SFFC3A5A
OFC7 2A
OFC8 9EBF
                               1009
                               1010
                                              DEC AR
                               1011
                                              MQ. 1-> AC. 1
                                                                  .. COPY MQ TO AC
OFCA PEAF
                               1012
                                              MQ.0 \rightarrow AC.0
ÖFCC ECFF01AC
OFD0 3A00
                                              CR. 0-1-> CR. 0
                               1013
                                              IF > 0 COTO CVT01
T'.'->@AR ...
                               1014
                                                                  ..OUTPUT DEC POINT
OFD2 F82E5A
                               1015
                                              DEC AR
OFD5
                               1016
ÖFD6 9CFF01BC
                                              CR. 1-1-> CR. 1
1F > 0 GOTO CVT01
GOTO CVT03
                               1017
OFDC 3000
                               1018
                               1019
                               1026 CVT01: CR. 1-1-> CR. 1
1021 IF >0 G0TO DIV10
OFDE SCFF01BC
OFE2 SAB1
OFE4 1A
                               1022 CVT03: INC AR
0FE5 D5
                               1023
                                                                  .. DONE
                                              EXIT
OFE6
                               1024
OFE6
                               1025
                                                 END
```

APPENDIX D

SOFTWARE LISTING FOR ELECTRONIC DASHBOARD DISPLAY

```
0600
                                              1 ...
                                                             > DASH
                                                                              J.M.C. RCA LABS 9:3:76
0000
                                              2 ...
OANĀ
                                              3 ..
                                                                 REGISTER ALLOCATION
0000
                                                  . . .
                                                           SP = R2 ...IT SHOULD BE THE STACK POINTER.
PC = R3 ...IT IS THE PROGRAM COUNTER
.. USED BY TRESE SUBROUTINES.
0000
                                              6
7
0000
0000
                                                           CALL = R4 ... IT SHOULD POINT TO THE ROUTINE
.. WHICH EFFECTS SUBROUTINE CALLS.
RETN = R5 ... IT SHOULD POINT TO THE ROUTINE
.. WHICH EFFECTS SUBROUTINE RETURN.
LINK=R6 ... USED FOR SUBROUTINE PARAM
0000
                                              8
0000
0000
                                             10
0000
0000
0000
                                             13
                                                      MS=R9 ... (MESSAGE POINTER/COUNTER)
AR=RA ... (USED FOR RESULT ADDRESS)
AC=RF ... 16-BIT ACCUMULATOR=RF.
MQ=RE ... 16-BIT ACCUMULATOR=RE EXTENSION.
0000
                                             14
0000
                                             15
0000
                                             16
0000
                                             17
                                                      MA=RD . (TEMPORARY) OPERAND MEMORY ADDRESS. CR=RC . (TEMPORARY) SCRATCHPAD AND COUNTER.
0000
0000
0000
                                             \bar{20}
0000
                                             \bar{2}\bar{1}
                                                               MESSL=#10FE; STACK=#1080
0000
                                             22
0000
                                            23
                                                                       INPUT--OUTPUT INSTRUCTION ALLOCATION
                                            24
0000
                                                         OUT 1
OUT 2
0000
                                            25 ...
                                                                       ENTER DATA IN DISPLAY MEMORY
                                                                      ENTER DATA IN DISPLAY INFORT
TURN DISPLAY ON OR OFF
STROBE FOR A TO D CONVERSION
CROUP SELECT FOR A TO D CONVERSION
CLOCK SHIFT RECISTERS
SHIFT REGISTER LOAD (STROBE)
                                            26 ...
0000
                                            27 ...
28 ...
                                                         OUT 3
OUT 4
0000
0000
                                                         OUT 5
OUT 6
OUT 7
                                            29 ..
0000
0000
                                            30 ..
0000
                                            31 ..
                                                                       FREE
0000
                                             32
                                                  • •
                                                                       READ BINARY DEVICES (CHANNEL 1)
READ BINARY DEVICES (CHANNEL 2)
READ BINARY DEVICES (CHANNEL 3)
0000
                                            33
                                                          INP
                                                  . .
                                                          INP 2
INP 3
0000
                                             34
                                            34 · · · 35 · · ·
0000
                                                                       READ 8 BIT A TO D CONVERTED DATA READ TACH(4-7)/FUEL(0-3) COUNTERS READ SPEED COUNTER
0000
                                                          INP 4
                                            36 ..
0000
                                                          INP 5
                                            37
                                                  . .
                                                          INP 6
0000
                                             38
                                                  . .
0000
                                             39
                                                          INP
                                                                       FREE
                                                 • •
0000
                                             40
                                            41 ..
0000
                                                                       A TO D CONVERSION COMPLETE
                                                          EF 1
                                                                       ODOMETER SERIAL INPUT
0000
                                             42 ..
                                                          EF2
                                                                       CLOCK SERIAL INPUT
READ TELEPRINTER (UT2 UTILITY)
0000
                                             43 ..
                                                          EF3
0000
                                             44 ..
                                                          EF4
0000
                                            45 ...
0000
                                             46 ...
                                                              IMMEDIATE BYTE DATA VALUES
0000
                                            47
                                                 . . .
                                                       ACT1=#7F; ACT2=0 ; ACT3=0
INV1=#FE; INV2=#FF; INV3=#FF ..12V -> DANCER!
OV2=237; OV3=217; OV4=196 ..OIL PRESSURE DATA
OV5=176; OV6=156; OV7=135
0000
                                            48
0000
                                            49
0000
                                            50
0000
                                            51
റററദ
                                            52 ...
                                            53 ...
0000
```

```
0000
                                           54
                                                         ORC 0
                                                         SEX O
    0000 E0
                                           55
    0001 E0
0002 7100
                                                         SEX 0
                                           56
                                                                                 ..TURN INTERRUPTS OFF!
                                          57
                                                         DISABLE; , 0
    0004 F800B3
0007 F800A3
                                                         A.1(PC3) -> R3.1
                                           58
                                                         A.0(PC3) \rightarrow R3.0
                                           59
                                                         A.0(PC3)->R3.0

GO STATE R3 ..FREE R0
A.1(STACK)->SP.1; A.0(STACK)->SP.0
A.1(MESSL)->MA.1; A.0(MESSL)->MA.0,MS.I

#FO->GMA; DEC MA; #FF->GMA ..SET MESS ARE
240->MS.0 ..MESSACE COUNTER
0->R0.0 ..INTERRUPT COUNTER
14->CR.0 ..ZERO RAM CONSTANT AREA
A.1(RAM)->MA.1; A.0(RAM)->MA.0
    000A D3
                                           60
    000B F810B2F880A2
                                           61 PC3:
    0011 F8IOBDF8FEADB9
                                           62
    0018 F8F05D2DF8FF5D
001F F8F0A9
                                           63
                                           64
    0022 F800A0
0025 F80EAC
                                           65
                                           66
    0028 F800BDF800AD
002E F800SD1D
F
                                               ZLOOP: 0-> @MA; INC MA

DEC CR; CR.0; BNZ ZLOOP

A.1(CALLS) -> R4.1; A.0(CALLS) -> R4.0

A.1(RET) -> R5.1; A.0(RET) -> R5.0
    0032 2C8C3A2E
    0036 FP00B4F800A4
                                          70
    003C F800B5F800A5
                                           71
    0042 F800B1
                                           72
                                                         A. 1(INTCD) -> R1.1 .. PREPARE FOR 'INTERRUPTS
    0045 F800A1
                                           73
                                                         A. 0(INTCD) -> R1.0
    0048 E37023
004B
                                           74
                                                         SEX R3; RETURN; , #23 .. ENABLE INTERRUPTS
                                           75
    004B
                                           76
    004B
                                           77
                                                            WAIT FOR INTERRUPT
                                               . .
    004B
                                           78
                                               INTWT: GO TO INTWT
    004B 304B
                                           79
    004D
                                           80
    004D F800B3F84BA3
                                               EXIT: A.1(INTWT)->R3.1; A.0(INTWT)->R3.0
                                           81
    0053 70
                                           82
                                                         RETURN
    0054
                                           83
    0054
                                                            INTERRUPT SERVICE STARTS HERE
                                           84
    0054
                                           85
    0054 2278
0056 22
                                               INTCD: DEC SP; SAVE
                                           86
                                                         DEC SP
A. I(NEWPC) -> R3. 1
                                                                               .. POINT TO FREE
                                           87
    0057 FB00B3
                                           88
                                                         A. 0( NEWPC) -> R3.0
    005A F800A3
                                           89
                                          96 GO STATE R3 ..R3 IS PC
91 NEWPC: INC R0; R0.0.XOR.8 ..CHECK FOR RESET
92 BNZ *+3; -> R0.0
    005D D3
    005E 1080FB08
0062 3A65A0
                                                         32-> CR. 0
A. 1 (OUTBF+#400) -> AR. 1
    0065 F820AC
                                          9\overline{3}
    0068 F800BA
                                          94
                                          95 A.0(OUTBF+#400)->AR.0
96 CLEAN: 32->@AR; INC AR ..PUT SPACES IN
97 DEC CR; CR.0; BNZ CLEAN ..DISPLAY BUFFER
    006B F800AA
    006E F8205A1A
    0072 2C8C3A6E
                                          98 ...
    0076
    0076
                                           99
                                                            UPDATE ECONOMY/TACH RAW VALUES
                                               . .
    0076
                                         100
                                         100 ...
101 ECOTAC: INP 5; DEC SP
102 INP 5; LDX; INC SP; XOR ..READ AND COMPAR
103 BNZ ECOTAC ..SHOULD BE SAME OR REPEAT
    0076 6D22
    0078 6DF012F3
007C 3A76
    007E FOFBFFA7
    0082
                                         105 ...
    0082
                                                            UPDATE FUEL COUNTER
                                         106
    0082
                                         107 ...
```

```
0082 D400000400
0087 8752
                                                   CALL LOADOP; , A(FCNT+#400)
                                   108
                                    109
                                                   R7.0->@SP
0089 9BF5FA0FA852
                                    110
                                                   RB. 1-+@. AND. #F->R8.0, @SP .. NEW MINUS OLD
008F 8FF4AF3B98
0094 9FFC01BF
                                                   AC.0+@->AC.0; BNF *+6
AC.1+1->AC.1 ..ADD W
                                    111
                                                                        .. ADD WITH CARRY
0098 0400000400
                                                   CALL STOROP; , A(FCNT+#400)
                                    113
deoo
                                    114
009 n
                                    115 ..
                                                      UPDATE TACH COUNTER
009D
                                    116 ...
009D F800BDF800AD
                                    117
                                                   A. 1(TCNT+#400) -> MA. 1; A. 0(TCNT+#400) -> MA. 0
00A3 4DAF2D
00A6 87FAF052
                                                   @MA!->AC.0; DEC MA
R7.0.AND.#F0->@SP
                                    118
                                    119
                                                   RB.1.AND.#F0-+@.AND.#F0->R8.1 ..NEW-OLD /2/2/2/2->@SP
OOAA 9BFAF0F5FAF0B8
                                    120
00B1 F6F6F6F652
                                    121
                                   122
123
                                                   AC.0+@->@MA ..CUMULATIVE TCNT
R7.0->RB.1 . NEW PREVIOUS VALUE
R0.0.AND.7 ..LOOK FOR 3 LSB-0
00B6 8FF45D
00B9 87BB
00BB 80FA07
                                    124
                                   124 R0.0.AND.? ..LUUK FOR 3
125 BNZ EPAG1 ..=>POWER OF 8
126 0->AC.1,AC.0,MQ.1,MQ.0
127 6->CR.0; SEX MA ..COMPUTE
128 MPY6: AC.0+@->AC.0; BNF **+6
129 AC.1+1->AC.1
130 DEC CR; CR.0; BNZ MPY6
131 SEX SP; 0->@MA ..ZERO TCNT
132 DIVTEN:AC.0-19->AC.0
133 LNC MQ. BDE DIVTEN
00BE 3A00
                                                                    ..=>POWER OF 8 (EVERY SECOND)
OOCO F800BFAFBEAE
                                                                               ..COMPUTE R.P.M.
00C6 F806ACED
00CA 8FF4AF3BD3
OOCF 9FFC01BF
00D3 2C8C3ACA
00D7 E2F8005D
OODB 8FFF13AF
                                                   INC MQ; BDF DIVTEN
AC.1-1->AC.1 ..SUBTRACT WITH BORROW
BDF DIVTEN; DEC MQ
A.1(RPM+#400)->MA.1; A.0(RPM+#400)->I
MQ.0->@MA ..SAVE RPM
00DF 1E33DB
                                    133
00E2 9FFF01BF
                                    134
00E6 33DB2E
                                    135
00E9 F800BDF800AD
00EF 8E5D
                                    136
                                                                                  A.O(RPM+#400)->MA.O
                                    137
00F1 D400000000
                                    138 EPAG1: CALL JUMP: , A(PAGE1)
00F6
                                    139
                                                   PAGE
0100
                                    140
0100
                                   141
142
143
0100
                                                      READ VELOCITY -- CONVERT TO KM/H.
0100
0100
                                    144
0100 80F63300
                                    145 PAGE1: RO. 0/2; BDF SPEED
                                                                               ..EVERY OTHER TIME
0104 D400000000
                                                   CALL JUMP; , A(PML)
                                    146
0109
                                    147
                                   148 SPEED: INP 6; DEC SP ..READ A BYTE
149 INP 6; LDX; INC SP; XOR ..READ AND COMPARE
150 BNZ SPEED ..SHOULD BE SAME OR REPEAT
151 @.XOR.#FF->@SP
0109 6E22
010B 6EF012F3
010F 3A09
0111 F0FBFF52
                                                   RB.0-+@-> R7.0. NEW MINUS OLD

@-> RB.0 . NEW BECOMES OLD

A.1(KPH+#400)-> MA.1; A.0(KPH+#400)-> MA.0
0115 8BF5A7
                                    152
0118 FOAB
                                    153
011A F800BDF800AD
                                    154
0120 875D
                                                    R7.0->@MA
                                    155
                                    156 ...
157 ..
0122
0122
                                                      UPDATE ODOMETER COUNT AND REGISTER
0122
                                    158 ...
                                                   CALL LOADOP; , A(OCNT+#400)
0122 D400000400
                                    159
0127 8752
                                                   R7.0->@SP
                                                                         .. SPEED DIFFERENCE
                                    160
                                                   R7.0->@SP ..SPEED
AC.0+@->AC.0; BNF *+6
0129 8FF4AF3B32
                                    161
```

```
AC.1+1->AC.1 ..ADD WITH CARRY CALL STOROP; A(OCNT+#400) CALL SMOP; A(TENTH) AC.1.AND.#80; BZ ODO2
                                      162
012E 9FFC01BF
0132 0400000400
                                      163
0137 D400000000
013C 9FFAB03200
                                      164
                                      165
                                                      CALL JUMP; A(PML)
0->AC.1,AC.0
CALL STOROP; A(OCNT+#400)
8.XOR.#FF->@SP ..HAVE GONE 0.1 KM.
OUT 4; DEC SP ..STROBE ODOMETER REGISTER
0141 D400000000
                                      166
                                      167 ODO2:
0146 F800BFAF
014A D400000400
                                      168
014F F808FBFF52
                                      169
0154 6422
                                      170
                                      171 ...
0156
                                                          COMPUTE FUEL ECONOMY EVERY 0.1 KM.
                                      172
0156
                                            • •
                                      173 ...
174
0156
0156 F800AE
                                                      0-> MQ. 0
                                                      CALL LOADOP; A(FCNT+#400) ...DIVIDE BY ZER AC.0; BNZ KP; AC.1; BNZ KP ..FCNT=0?
A.1(KMPL+#400)->MA.1; A.0(KMPL+#400)->MA.0
0159 D400000400
                                      175
                                      176
177
015E 8F3A009F3A00
0164 F800BDF800AD
                                                      GO TO KPLEX
                                       178
016A 8F5D
016C 3000
                                       179
016E D40000000
0173 D400000400
                                      180 KP: CALL LOADOP; A(KPLCON)
181 KPLDIV: CALL SMOP, A(FCNT+#400)
0178 1E
0179 9FFA803273
                                                       INC MQ
                                       182
                                                       AC.1.AND.#80; BZ KPLDIV
                                       183
017E 2E
017F F800BDF800AD
                                                       DEC MQ ..ROLLED NEGATIVE
A.1(KMPL+#400)->MA.1; A.0(KMPL+#400)->MA.0
                                                                              .. ROLLED NEGATIVE
                                       184
                                       185
                                      186 MQ.0->@MA

187 0->AC.1,AC.0

188 KPLEX: CALL STOROP;,A(OCNT+#400) ..ZERO ODOMETER

189 CALL STOROP;,A(FCNT+#400) ..FUEL COUNTERS

190 CALL JUMP;,A(PML)
0185 8E5D
0187 F800BFAF
018B D40000400
0190 D400000400
0195 D400000000
019A
                                       191
                                       192
019A
                                       199 ...
019A
                                                          PROCESS MESSAGE LIST
                                       194 ..
019A
                                       195 ...
019A
                                                      ...MESSAGE PROCESSING STATUS IS MAINTAINED ...LIST AREA OF MEMORY WHICH HAS THE ...FOLLOWING FORMAT:
019A
                                       196
019A
                                       197
019A
                                       198
                                       199
019A
                                                       . . .
                                                                    #FF ..END OF LIST MARKER
(MESSAGE #) ..2ND MESSAGE OUTPUT
(MESSAGE #) ..1ST MESSAGE OUTPUT
019A
                                      200
                                                       . . .
019A
                                      201
                                                       . . .
019A
                                      202
                                                                                 ... DOING A 30 SECOND WAIT
                                                       ...MESSL: #F0
019A
                                       203
019A
                                      204
                                                       MS.1->MA.0; A.1(MESSL)->MA.1 ..LIST POINT
DEC MS; MS.0 ..DECREMENT MESSAGE COUNTER
BNZ MSTAT ..COUNTER AT ZERO?
DEC MA; R9.1-1->R9.1 ..DECR LIST POINTER
                                                                                                         .LIST POINT
019A 99ADF810BD
                                       205 PML:
                                      206
019F
        2989
                                       207
01A1 3A00
 01A3 2D99FF01B9
                                       208
                                                       @MA!->@SP; DEC MA; .XOR.#FF ..END OF LIST?
BNZ NOTEOL
 01A8 4D522DFBFF
                                       209
                                       210
01AD 3A00
                                                       A.O(MESSL)->NA.O,NS.1 ..MESS ALL OUTPUT
240->MS.0 ..SET UP 30 SEC WAIT
                                       211
        F8FEADB9
 Ø1AF
 01B3 F8F0A9
                                       212
                                      213 GO TO MSTAT
214 NOTEOL: 0-> AR. 1; 5-> CR. 0; @-> AR. 0 .. NEXT MESSAC
215 SHL5: AR. 1-> @SP; &+@-> AR. 1 .. COMPUTE MESS ADDR
 01B6 3000
                                                                                                      ..NEXT MESSAGE
 01B8 F800BAF805ACF0AA
 01C0 9A52F4BA
```

```
01CB 3BCE
                                       217
                                                       BNF *+6
                                                                      ... 16 BIT SHIFT LEFT
                                       217 BNF *+6 ..16 BIT SHIFT LEFT
218 AR.1+1->AR.1 ..PROCESS CARRY
219 DEC CR; CR.0; BNZ SHL5
220 AR.1+A.1(MES0)->AR.1 ..ADD OFFSET
221 CALL DISP ..OUTPUT THE MESSAGE
222 24->MS.0 ..SET UP 3 SEC WAIT
223 MSTAT: @MA!.XOR.*F0; BZ BIP ..NOW ON DISPLAY?
224 CALL JUMP; ,A(1NTEX)
    01CA 9AFC01BA
    OICE 2C8C3AC0
    01D2 9AFCO7BA
    01D6 D40000
    01D9 F81BA9
01DC 4DFBF03200
    01E1 D40000000
                                       225
    01E6
                                       226 ...
    01E6
                                                         LOOK FOR NEW BINARY PROBLEMS
    01E6
                                        227
    01E6 B0F63B00
                                       228 BIP:
                                                      RO.0/2; BNF BEZEL ..ODD COUNTS ONLY
    01EA D40000
                                                      CALL BSCAN
                                        229
    01ED
                                       230
                                       231
    01ED
                                                          UPPER OR LOWER BEZEL ACTIVE?
    OIED
                                       232
    01ED 69F0FA803200
                                       233 BEZEL: INP 1; @. AND. #80; BZ LOBEZ
234 CALL JUMP; , A(UPBEZ)
    01F3 D400000000
     01F8
                                        235
     01F8
                                        236
                                                      LOWER BEZEL PROCESSING:
    01F8
                                        237
                                       238 .... RØ. Ø. AND. 3 ... LOOK FOR 2 LSB= Ø
239 LBZ TANK .. => POWER OF 4 (EVERY Ø.5 SEC)
240 CALL JUMP; , A (INTEX) ... SKIP DISPLAY
    01FB 80FA03
    01FB C20000
    01FE D40000000
    0203
                                       241
                                                          FORMAT DISPLAY IN 1/6 TANK INCREMENTS
    0203
                                        242
                                             . .
    0203
                                        243
    0203 F801FBFF52
                                             TANK: 1.XOR.#FF->@SP
                                        244
                                                      OUT 4; DEC SP ... GROUP SELECT
OUT 3; DEC SP ... CONVERT
    0208 6422
                                       245
    020A 6322
020C 3C0C
020E 6CF0FF05AF
                                       246
                                                       BN1 * ..WAIT FOR CONVERSION INP 4; @-5-> AC.O ..ACCOUNT FOR OFF
                                        247
                                                       BN1 *
                                                      INP 4; @-5->AC.0 ..ACCOUNT FOR OFFSET A.1(OUTBF+#400)->AR.1; A.0(OUTBF+#400)->AR
                                       248
F
    0213 F800BAF800AA
                                       249
    0219
                                       250
                                       251 7-> CR.0 ..MAX 6 BARS ON FUEL DISPLAY
252 FUEL: AC.0-16-> AC.0
253 T'@'-> @AR; INC AR ..FILL IN FUEL BAR
    0219 F807AC
    021C 8FFF10AF
0220 F8405A1A
                                       254 DEC CR; CR.0; BZ FUEL1
255 BDF FUEL
256 FUEL1: DEC AR; 32->@AR ..BLANK ROLLOVER
    0224 2C8C3200
    0228 331C
    022A 2AF8205A
    022E
                                        257
    022E
                                                         FORMAT DISPLAY IN TACH REVS (TWO DIGITS)
                                        258
    022E
                                        259
    022E F800BDF800AD
                                        260 TACH: A.1(RPM+#400)->MA.1; A.0(RPM+#400)->MA.0
    0234 4DAF
0236 D400000407
                                        26 1
                                                      @MA!-> AC. 0
                                                      CALL FMT2;,A(OUTBF+#400+7)
@AR!.XOR.#30; BNZ *+6 ..LEADING ZERO?
DEC AR; 32->@AR ..BLANK IT
                                       262
    023B 4AFB303A44
                                       263
    0240 2AF8205A
                                        264
    0244
                                       265
    0244
                                       266
                                                         FORMAT DISPLAY IN KM/H (SPEED)
    0244
                                       267
    0244 F800A7B7
                                       268
                                                           0-> R7.0, R7.1
    0248 F800BDF800AD
                                       269
                                                      A. 1(KPH+#400)->MA. 1; A. 0(KPH+#400)->MA. 0
```

```
024E 4DAF
                                 270
                                               @MA!->AC.0
                                               A. 0( OUTBF+#400+10) -> AR. 0
                                 271
272
0250 F80AAA
                                         DIV11: AC.0-7->AC.0 ..DIVIDE BY 7
T'@'->@AR; INC AR ..AND FILL IN SPEED BAR
INC R7: R7.0->@SP
0253 8FFF07AF
0257 FB405A1A
                                 273
                                 274
275
025B 178752
                                               BDF DIVII ..POSITIVE REMAINDER?
DEC AR; 32->@AR ..BLANK IT
9;SD;BDF RESQL
025E 3353
0260 2AF8205A
                                 276
0264 F809F53300
                                 277
0269 7B38
                                 278
                                                 SEQ; SKP
026B
                                 279
                                        RESQL: REQ
026C D400000000
                                 280
                                               CALL JUMP; A(DISALL)
0271
                                 281
0300
                                 282
                                               PAGE
0300
                                 283
0300
                                 284
                                               UPPER BEZEL PROCESSING:
0300
                                 285
                                 286
0300
                                     UPBEZ: R0.0; BZ TIME ..ONCE A SEC
CALL JUMP; , A(INTEX) ..ELSE WE ARE DONE.
TIME: 0-> R7.0, R7.1, AC.1
A.1(KPII+#400)-> MA.1; A.0(KPH+#400)-> MA.0
0300 803200
                                 287
0303 D400000000
                                 288
0308 F800A7B7BF
                                 289
030D F800BDF800AD
                                 290
                                                @MA!->AC.0
0313 4DAF
                                 291
                                           DIV8: AC. 0-7-> AC. 0
INC R7; R7.0-> @SP
0315 8FFF07AF
                                 292
0319
      178752
                                 293
                                               BDF DIVS
031C 3315
                                 294
031E F809F53300
                                 295
                                                 9:SD:BDF RESQ1
0323 7B38
                                 296
                                                SEQ SKP
0325 7A
                                 297
                                         RESQ1: REQ
0326
                                 298
                                 299 . .
                                                    READ IN SERIAL TIME AND CONVERT
0326
0326
                                 300 ...
                                 0326 F800B7A7F810AC
032D 6622
032F 87F6A7
0332 97F63638F980B7
0339 3B3F87F980A7
033F 6522
0341 2C8C3A2F
0345
                                 308
                                               ... BIT 15 IS MSB. BIT 0 IS ... BITS 15-8 CONTAIN MINUTES ... BITS 7-4 CONTAIN HOURS
                                                                            BIT Ø IS LSB.
0345
                                 309
0345
                                 310
0345
                                 311
0345
                                 312
                                                0-> AC. 1
0345 F800BF
                                 313
                                               G-AG.1

R7.0/2/2/2/2->AC.0 .SHIFT RIGHT 4

CALL FMT2;,A(OUTBF+#400) ..FORMAT HOURS

@AR!; DEC AR; .XOR.T'0'; BNZ *+5

32->@AR ..SUPPRESS LEADING ZERO
0348 B7F6F6F6F6AF
                                 314
034E D400000400
                                 315
                                 316
0353 4A2AFB303A5C
0359 F8205A
                                 317
                                               A.0(OUTBF+#400+2)->AR.0
T':'->@AR .PUT OUT A COLON
R7.1->AC.0 ..CET MINUTES
035C F802AA
035F F83A5A
                                 318
                                 319
                                                R7.1->AC.0 ..CET MINUTES
CALL FMT2;, A(OUTBF+#400+3)
0362 97AF
                                 320
0364 D400000403
                                 321
0369
                                 322
                                 323 ...
0369
```

```
324 ...
325 ...
    0369
                                                       READ IN SERIAL ODOMETER AND CONVERT
    0369
                                    0369 F800BFAFF810AC
                                                                        .. LOAD SHIFT REGISTER
    0370 6622
                                                                       ..SHIFT LO BYTE
    0372 8FF6AF
    0375 9FF6357BF980BF
                                                   AC. 1/2; B2*+4;
                                     329
                                                  BNF*+6; AC.0.OR.#80->AC.0
OUT 5; DEC SP..CLOCK SHIFT REGISTER
DEC CR; CR.0; BNZ ODOSH
    037C 3BB28FF980AF
                                     330
    0382 6522
                                     331
    0384 2C8C3A72
                                     \tilde{3}\tilde{3}\tilde{2}
                                     333 ...
    0388
                                                         ODOMETER RANGE IS 0 TO 999.9 KM.
    0388
                                     334
                                     335
                                                        REGISTER AC CONTAINS 4 BCD DIGITS.
    0388
                                     336
    0388
                                                   A. 0(OUTBF+#400+6)->AR. 0
    0388 F806AA
                                     337
                                                  A. 0 (001BF+#400+6)->AR. 0
AC. 1/2/2/2/2+#30->&AR; INC AR ...1ST DIGI'
AC. 1. AND. #F+#30->&AR; INC AR ...2ND DIGIT
AC. 0/2/2/2/2+#30->&AR; INC AR ...3RD DIGIT
T'.'->&AR; INC AR ...DECIMAL POINT
AC. 0. AND. #F+#30->&AR ...4TII DIGIT
                                                                                                 . 1ST DIGIT
    038B 9FF6F6F6F6FC305A
                                     338
    0394 9FFA0FFC305A1A
                                     339
    039B 8FF6F6F6F6FC305A
                                     340
    03A4 F82E5A1A
                                     341
    03A8 SFFA0FFC305A
                                     342
                                     343 ...
    OBAE
                                                      SUPPRESS LEADING ZEROES
    ÖBAE
                                     344 ...
    GRAE
                                     345 ...
                                                  A.0(OUTBF+#400+6)->AR.0; SEX AR @.XOR.#30; BNZ ESUP
    OBAE F806AAEA
                                     346
    03B2 F0FB303A00
03B7 F8205A1A
                                     347
                                                   #20-> @AR; INC AR
                                     348
                                                   @.XOR.#30; BNZ ESUP
F
    OSBB FOFBSOSAGO
                                     349
    03CO F8205A1A
                                     350
                                                   #20->@AR; INC AR
    03C4 F0FB303A00
                                     351
                                                   @.XOR.#30; BNZ ESUP
    03C9 F8205A
03CC E2
                                                   #20->@AR
                                     352
                                     353 ESUP: SEX SP
                                     354 ...
    03CD
                                                      DO A TO D ON WATER TEMPERATURE.
                                                                                                     FORMAT.
    03CD
                                     355 ...
                                     356 ...
    03CD
    03CD F802FBFF52
                                     357
                                                   2. XOR. #FF->@SP
                                                   OUT 4; DEC SP .. GROUP SELECT
OUT 3; DEC SP .. CONVERT
    0302 6422
                                     358
    0304 6322
                                     359
                                                                       .. WAIT FOR CONVERSION
    03D6 3CD6
                                     360
                                                   BN1 * ..WAI
INP 4; @->AC.0
CALL JUMP;,A(SCALW)
    OSDS 6CFOAF
                                     361
    03DB D40000000
                                     362
    03E0
                                     363
    0400
                                     364
                                                   PACE
    0400
                                     365
                                                   . . .
                                    366 ...
367 ...
    0400
                                                   SCALE THRU 0-99
    0400
    0400
                                     368
                                     369 SCALW: A.O(OUTBF+#400+15)->AR.O
370 T'O'->@AR; INC AR ...PUT IN OK
371 T'K'->@AR
    0400 F80FAA
    0403
           F84F5A1A
    0407 F84B5A
                                     372
                                                   AC.0/2-> @SP .. USE LINEAR APPROX.
182-@-> AC.0, R7.0 ... TO COMPUTE
                                                   AC.0-244; BCE FLW
                                                                                .TEMP < 60?
    040A 8FFFF43300
    040F 8FF652
                                     373
                                                   182-@-> AC.0, R7.0 ... TO COMPUTE TEMP
CALL FMT2;, A(OUTBF+#400+12) ... NO. FO
R7.0-97; IF LESS GO TO FLW
0-> CR.1; 7-> CR.0 .. MESSAGE #7
    0412 F8B6F7AFA7
                                     374
                                                                                           .. NO. FORMAT
    0417 I;40000040C
                                     375
    041C 87FF613B00
                                     376
    0421 F800BCF807AC
                                     377
```

```
CALL MESADD .. "WATER TEMP HIGH" A.0(OUTBF+#400+15)->AR.0
T'H'->@AR; INC AR .. IT IS HIGH
T'I'->@AR
                                       378
    0427 D40000
                                        379
    042A F80FAA
Ē
                                        380
    042D F8485A1A
    0431 F8495A
                                        381
                                                      CO TO OIL.
0->CR.1; 7->CR.0 ..MESSAGE #7
CALL MESSUB
                                        382
    0434 3000
    0436 F800BCF807AC
                                        383 FLW:
                                        384
    043C D40C00
                                        385 ...
    043F
                                                          DO A TO D ON OIL PRESSURE. FORMAT.
                                        386
    043F
    043F
                                        387
                                        388 ÖİL:
                                                       3. XOR. #FF->@SP
    043F F803FBFF52
                                                       OUT 4; DEC SP ... GROUP SELECT
OUT 3; DEC SP ... CONVERT
    0444 6422
                                        389
    0446 6322
0448 3C48
                                        390
                                                                             .. WAIT FOR CONVERSION
                                        391
                                                       RN1 *
                                                       INP 4;@->AC.0
                                        392
     044A 6CFOAF
                                        393
     044D
                                        394 ...
                                                       SCALE 0-7
     044D
                                        395
     044D
                                                        2-> MQ. 0
                                                       AC.0-OV2; IF CE GO TO OILEX
INC MQ; AC.0-OV3; IF GE GO TO OILEX
INC MQ; AC.0-OV4; IF GE GO TO OILEX
INC MQ; AC.0-OV5; IF GE GO TO OILEX
INC MQ; AC.0-OV6; IF GE GO TO OILEX
INC MQ; AC.0-OV6; IF GE GO TO OILEX
                                        396
     044D F802AE
     0450 8FFFED3300
                                        297
            1E8FFFD93300
                                        398
     0455
     045B 1E8FFFC43300
                                        399
            1E8FFFB03300
                                        400
     0461
     0467 1E8FFF9C3300
                                        401
                                                       INC MQ; AC.O-OV7; IF GE GO TO OILEX INC MQ ... MQ NOW UP TO 7
     046D 1E8FFF873300
                                        402
                                        403
     0473 1E
                                                   OILEX: A. O(OUTBF+#400+19) -> AR. O
                                        404
     0474 F813AA
                                                         MQ.0; SHR; -> AC.0; +#30-> @AR
     0477 BEF6AFFC305A
                                        405
                                                       B-> CR. 1; O-> CR. 0 . MESSAGE #8
INC AR; INC AR
AC. 0-2; IF GE GO TO OILOK
T'L'-> @AR; INC AR
T'O'-> @AR
     047D F808BCF800AC
                                        406
     0483 1A1
                                        407
     0485 8FFF023300
                                        408
     048A F84C5A1A
048E F84F5A
0491 D40000
0494 3000
                                        409
                                        411 CALL MESADD .. "OIL PRESSURE LOW"
412 GO TO FUELEC
413 OILOK: T'O'->@AR; INC AR
414 T'K'->@AR
                                        410
     0496 FB4F5A1A
     049A F84B5A
                                                        CALL MESSUB
                                        415
     049D D40000
     0440
                                        416
                                                           FORMAT FUEL ECONOMY
                                        417
     04A0
     0440
                                        418
                                        419
     04A0
                                        420 FUELEC: A.1(KMPL+#400)->MA.1; A.0(KMPL+#400)->MA
     04A0 F800BDF800AD
F
                                                        @MA!->AC.0
AC.0->R7.0; BZ AMPS1
                                         421
     04A6 4DAF
04A8 8FA73200
                                         422
                                                        AC.0->R7.0; BZ AD ST
CALL FMT2; A(OUTBF+#400+24)
@ART.XOR.#30; BNZ *+6 ..LEADING ZERO?
DEC AR; 32->@AR ..BLANK IT
                                         423
     04AC D400000418
                                         424
      04B1 4AFB303ABA
                                                        DEC AR; 32->@AR
R7.0->AC.0
                                         425
     04B6 2AFB205A
     04BA &7AF
                                         426
                                                        A. 0(OUTBF+#400+27) -> AR. 0
     04BC F81BAA
                                         427
                                                        AC. 0-9; IF GE CO TO TRYOK
      04BF 8FFF393300
                                         428
                                                        T'L'->@AR; INC AR
T'O'->@AR
      04C4 F84C5A1A
                                         429
                                         430
      04C8 F84F5A
                                                        GO TO AMPS 1
                                         431
     04CB 3000
```

```
04CD EFFF0D3300
                               432 TRYOK: AC. 0-13; IF GE GO TO TRYHI
                                             T'O'->@AR; INC AR
T'K'->@AR
04D2 F84F5A1A
                               433
0406 Ft 4B5A
                               434
04D9 3000 .
04DB F8485A1A
04DF F8495A
                               435 GO TO AMPS1
436 TRYHI: T'H'->@AR; INC AR
437 T'I'->@AR
04E2
                               438
04E2 D400000000
                               439 AMPS1: CALL JUMP; , A(AMPS)
0500
                               440
                                             PAGE
0500
                               441
0500
                               442
0500
                               443 ...
                                               DO "LO" OR "OK" INDICATION FOR AMPS
0500
                               444
0500 F81EAA
                               445 AMPS: A.0(OUTBF+#400+30)->AR.0
446 T'O'->@AR; INC AR
447 T'K'->@AR
0503 F84F5A1A
0507 F84B5A
                                             INP 2;@.AND.1;BZ DISALL..UNUSED BINARY DEC AR; T'L'->@AR; INC AR T'O'->@AR
050A 6AF0FA013200
                               448
0510 2AF84C5A1A
                               449
0515 F84F5A
                               450
0518
                               451
0518
                               452
                               453 DISALL: A.1(OUTBF+#400)->AR.1; A.0(OUTBF+#400)->
454 CALL DISP
0518 F800BAF800AA
051E D40000
0521
                               455
0521
                                             EXIT FROM INTERRUPT
                               456
0521
                               457
0521 12
0522 F800B1
                               458 INTEX: INC SP
459 A.1(EXIT)->R1.1
9525 F84DA1
9528 D1
                               460
                                             A. 0(EXIT) -> R1. 0
                               461
                                             GO STATE R1
0529
                               462
05\bar{2}9
                               463
0529
                                               SCAN AND PROCESS ALL BINARY INPUTS
                               464
05\bar{29}
                               465
0529 F800BDF800AD
                               466 BSCAN: A. 1(OST1+#400) -> MA. 1; A. 0(OST1+#400) -> MA. 0
052F 4DAF
                               467
                                             @MA! \rightarrow AC.0
0531 8F5222
                                             AC.0->@SP; DEC SP
                               468
0534 69
0535 FOFBFEFA7F
                                                             LEAST SIGNIF. (DEV 7-0)
                                             INP 1
                               469
                               470
471
                                             @. XOR. INVI. AND. ACT1
053A 52AF
                                             ->@SP,AC.0
INC SP; XOR
->R7.0
053C 12F3
053E A7
053F 22
                               472
473
                                                                .XOR OLD, NEW STATUS
                                                            .. SAVE FOR LATER
.. POINT BACK TO NEW STATUS
                               474
                                             DEC SP
                                             AND; -> R7.1 ..DETECT 0-> 1 TRANSITION
A.1(OST1+#400)-> MA.1; A.0(OST1+#400)-> MA.0
AC.0-> @MA ..STORE IT
0540 F2B7
                               475
0542 F800BDF800AD
                               476
                               477
478
0548 8F5D
054A F800BC
                                             0-> CR. 1
                                             0->CR. 1 ..DEVICE OFFSET CALL BINDET; INC SP
054D D4000012
                               479
                                             A.1(0ST2+#400)->MA.1; A.0(0ST2+#400)->MA.0
0551 F800BDF800AD
                               480
0557 4DAF
                               481
                                             @MA!->AC.0
                                             AC.0->@SP; DEC SP
0559 8F5222
                               482
055C 6A
055D FØFBFFFA00
                                             INP 2 ..DEVICES 15-8
@.XOR.INV2.AND.ACT2 ..PROCESS SAME WAY
                               483
                               484
0562 52AF
                               485
                                             ->@SP,AC.0
```

```
INC SP; XOR; ->R7.0
DEC SP; AND; ->R7.1
A.1(OST2+#400)->MA.1; A.0(OST2+#400)->MA.0
    0564 12F3A7
0567 22F2B7
                                       486
                                       487
    056A F200BDF800AD
                                       4RR
                                                      AC.0->@MA
    0570 8F5D
                                       489
                                                      8-> CR. 1 .. DEVICE OFFSET
CALL BINDET; INC SP
A.1(OST3+#400)-> MA.1; A.0(OST3+#400)-> MA.0
    0572 F808BC
                                       490
    0575 D4000012
0579 1'800BDF800AD
057F 4DAF
0581 8F5222
                                       491
                                       492
                                       493
                                                      @MA!->AC.0
                                       494
                                                      AC.0->@SP; DEC SP
                                                                       ..DEVICES 23-16
                                                      INP 3
    0584 6B
0585 FOFBFFFA00
                                       495
                                                      INF 3

... NOR. INV3. AND. ACT3

-> @SP, AC.0

INC SP; XOR; -> R7.0

DEC SP; AND; -> R7.1

A.1(OST3+#400)-> MA.1; A.0(OST3+#400)-> MA.0
                                       496
                                       497
    058A 52AF
    058C 12F3A7
058F 22F2B7
                                       498
                                       499
    0592 F800BDF800AD
0598 8F5D
                                       500
F
                                                      AC. 0->@MA
                                       501
                                                                             . DEVICE OFFSET
    059A F810BC
059D D4000012
                                                       16-> CR. 1
                                       502
                                                       CALL BINDET; INC SP
                                       503
                                                                            . . DONE
                                                       EXIT
    05A1 D5
                                        504
    05A2
                                        505
    05A2
                                        506
    05A2
                                        507
                                                          DETECT DEVICE TRANSITIONS
    05A2
                                        508 ..
                                       509
    05A2
    05A2 F800ACAF
    05A6 97F6B7
05A9 3B00
    05AB D40000
    05AE 1C8CFB083AA6
    05B4 F800AC
05B7 121212
05BA 87F2B7
    05BA B772B7
05BD 222222
05C0 97F6B7
05C3 3B00
05C5 D40000
    05C8 1C8CFB083AC0
05CE D5
     05CF
                                        524
     0600
                                        525
                                                       PAGE
                                        526
     0600
                                                       . . .
                                        527 ...
     0600
                                        528 ...
     0600
                                        529 ..
                                                          ADD MESSAGE TO DISPLAY LIST
     0600
                                        530
     0600
                                        531 MESADD: CR. 1->@SP; CR. 0+@->RB. 0
532 A. 1(MESSL) -> MA. 1 .. ADD M
533 A. 0(MESSL) -> MA. 0
                                                                                              ..DEVICE NUM
     0600 9C528CF4A8
0605 F810BD
0608 F8FEAD
                                                                                 ..ADD MESSAGE
     060B ED
060C 88F3
060E 3A00
0610 3000
0612 F0FBFF
                                        534
                                                       SEX MA
                                                                              ..ITEM TO BE ADDED?
                                        535 MESA01: R8.0; XOR
                                                       BNZ MESA02
BR MESA99
                                        536
                                                                             ..REJECT
                                        537
                                        538 MESA02: @; XRI *FF ..EOL MARKER?
539 DEC MA
     0615 2D
```

```
0616 3A0C
0618 1D885D
061B 2D
                                                                                                                      BNZ MESA01
INC MA; R8.0->@MA
DEC MA
                                                                                   540
                                                                                   541
542
                                                                                                                                                                                          ... PUSH ON MESSAGE STAC
061C F8FF5D
061F F810BD99AD
0624 4DFBF03A00
                                                                                                                       #FF->@MA
                                                                                                                                                                           .. MARK NEW EOL
                                                                                    543
                                                                                   543 **FF-ZMA ...MARK NEW EOL

544 A.1(MESSL)->MA.1; MS.1->MA.0

545 @MA!.XOR.#FO; BNZ MESA99 ..MESS ON DISPLAY

546 1->MS.0 ..FORCE DISPLAY OF MESSAGES

547 MESA99: SEX SP; EXIT ...GOOD RETURN
0629 F801A9
062C E2D5
                                                                                    548 ...
062E
062E
                                                                                                                              REMOVE MESSAGE FROM DISPLAY LIST
                                                                                    549
062E
                                                                                    550
                                                                                   551 MESSUB: CR.1->@SP; CR.0+@->R8.0 ..DEVICE NUM

552 A.1(MESSL)->MA.1; A.0(MESSL)->MA.0; SEX MA

553 0->R0.1 ..CLEAR FOUND FLAC

554 MESS01: @->@SP ..PUSH MESSACE LIST ON SP
062E 9C528CF4A8
 0633 F810BDF8FEADED
063A F800B0
 063D F052
063F 88F3
                                                                                                                       R8.0; XOR ...ITEM TO REMOVE?

BNZ NOTIT

INC SP; 1->R0.1 ...KNOCK IT OFF SP

@. XOR. #FF ...EOL?

DEC MA; DEC SP

BNZ MESS01

INC SP; INC MA

R0.1; BZ MESS02

LIC MA

LIC MA

LIC MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

RO MA

R
                                                                                     555
 0641 3A00
                                                                                    556
 0643 12F801B0
0647 F0FBFF
                                                                                     557
                                                                                     558 NOTITE
0644 2D22
064C 3A3D
064E 121D
0650 903200
                                                                                    559
                                                                                    560
                                                                                    561
                                                                                     562
                                                                                    563 INC MA ... COMPRESS LIST IF FOUND

564 MESSO2: 6SP!->@MA; INC MA .. PUT BACK MESSAGE LIST

565 XRI #FO ... FRAME MARKER?
0653 1D
0654 425D1D
0657 FBF0
0659 3A54
065B 22E2D5
                                                                                                                       XRI #F0 ..FR
BNZ MESSO2
DEC SP;SEX SP;EXIT
                                                                                     566
                                                                                     567
 065E
                                                                                     568
 065E F88052
                                                                                     569 DISP: #80->@SP
                                                                                                                        OUT 1; DEC SP ... CLEAR MEMORY
8->CR.0
 0661 6122
0663 F808AC
                                                                                    570
571
                                                                                                                        DEC CR; CR.0; BNZ CLP 32-> CR.0
                                                                                     572 CLP:
 0666 2C8C3A66
 066A F820AC
                                                                                     573
                                                                                                                        SEX AR; SEX AR; SEX AR .. MORE SEX LDA AR; DEC AR .. STALL A WHILE OUT 1 .. ZING IT
                                                                                     574 DCO:
 066D EAEAEA
 0670 4A2A
0672 61
0673 8CFF01AC
0677 3A6DE2
067A F80152
                                                                                     575
                                                                                                                                                                         ..ZING IT
                                                                                    576
577
578
                                                                                                                         ČŘ.0-1-> CR.0 ... SLOW DECREMENT
BNZ DCO; SEX SP
                                                                                                                         1->@SP
OUT 2; DEC SP ..MAKE SURE IT IS ON
                                                                                     579
 067D 6222
067F D5
                                                                                     580
                                                                                     581
  0680
                                                                                     582
                                                                                     583 FMT2: @R6!->AR.1
584 @R6!->AR.0
                                                                                                                                                                  .. FORMAT 2 DIGIT ASCII
  0680 46BA
 0680 468A
0682 46AA
0684 F800AE
0687 8FFF0AAF
068B 1E3387
068E 2E8EFC305A
0693 1A8FFC3A5A2A
                                                                                                                                                                   ..CET DESTINATION ADDRESS
                                                                                     585 D10:
                                                                                                                         0-> MQ. 0
                                                                                     586 DLP:
                                                                                                                         AC. 0-10-> AC. 0
                                                                                                                         AC. 0-10-7 AC. 0
INC MQ; BDF DLP
DEC MQ; MQ.0+#30->@AR
INC AR; AC.0+#3A->@AR; DEC AR
EXIT ..REGISTER AR IS UNCHANGED
                                                                                     587
                                                                                     588
                                                                                     589
  0699 D5
                                                                                     590
  069A
                                                                                     591
                                                                                     592 JUMP: SEX SP
                                                                                                                                                                                . MAKE SURE
  069A E2
                                                                                                                         @R6!->@SP .. SAVE HICH BYTE
  069B 4652
```

```
069D 46A6
                                                      @R6!->R6.0 ..PUT IN LOW @->R6.1 ..PUT IN HIGH
                                       594
     069F FOB6
                                       595
     06A1 D5
                                       596
                                                                           ..RETURN ADJUSTED
     06A2
                                       597
                                       598 LOADOP: LDA LINK .. FETCH ADDRESS
599 PHI MA .. TO MA REGISTER
600 LDA LINK
     06A2
     06A3 BD
     06A4 46
     06A5 AD
                                                     PLO MA .. FALL INTO LOAD
                                       601
     06A6 4D
                                               LOAD: LDA MA .. FETCH HIGH 8
                                       602
     06Λ7 BF
06Α8 4D
                                       603
                                                     PIII AC
                                                     LDA MA .. NOW LOW 8
PLO AC .. LEAVE MA AT NEXT DOUBLE-BYTE
SEP RETN .. CEE, THAT WAS QUICK.
                                       604
     06A9 AF
                                       605
     06AA D5
                                       606
     06AB
                                       607
                                       608 STOROP: LDA LINK .. FETCH ADDRESS INTO MA
609 PHI MA
     06AB
            46
     06AC BD
                                               LDA LINK
PLO MA .. THEN FALL INTO STORE
STORE: CHI AC .. FIRST HIGH 8
     06AD 46
06AE AD
                                       610
                                       611
     06AF 9F
                                       612
                                                     STR MA
INC MA .. INCREMENT MA, SINCE STR DOESN'T
     06B0 5D
                                       613
     96B1 1D
                                       614
     06B2 BF
                                       615
     06B3 5D
                                       616
                                                     STR MA
    06B4 1D
06B5 D5
                                                     INC MA .. LEAVE MA POINTING TO NEXT WORD SEP RETN .. QUIT
                                       617
                                       618
    06B6
                                       619
                                       619
620 SMOP: LDA LINK
621 PHI MA
     06B6
     06B7 BD
                                       6\overline{2}
     06B8 46
                                                     LDA LINK
    06B9 AD
                                              PLO MA .. POINT TO LOW 8
                                       623
    06BA 1D
                                       624
                                                    GLO AC .. FETCH AC LOW 8
SM .. SUBTRACT MEMORY FROM IT
PLO AC .. PUT IT BACK.
DEC MA .. NOW HIGH 8
GHI AC
BDF SMNB
SMI #1 .. PROPAGATE BORROW OF LOW 8
BDF SMNB
XOR .. SECOND DODOGO
                                                     SEX MA .. SET X TO MA GLO AC .. FETCH AC LOW B
    06BB ED
                                       625
     06BC 8F
                                       626
     06BD F7
                                       627
    06BE AF
                                       628
    06BF 2D
                                       629
    06CO 9F
                                       630
F
    06C1 3300
                                       631
     06C3 FF01
                                       632
    06C5 3300
                                       633
                                              XOR .. SECOND BORROW; FORCE BORROW OUT,
,#38 .. WHILE SUBTRACTING HIGH 8.

SMNB: SM .. HIGH 8 SUBTRACT, NO BORROW ACCROSS.
PHI AC .. PUT HIGH 8 BACK
SEX SP
    06C7 F3
                                       634
    06CB 38
                                       635
    06C9 F7
                                       636
    06CA BF
                                       637
    06CB E2
                                       638
    06CC D5
                                                     SEP RETN .. RETURN. DF=NO BORROW OUT
                                       639
    06CD
                                       640
    06CD D3
06CE 9652
                                                                           ... RETURN TO MAIN
                                       641
                                                      SEP R3
                                       642 CALLS: R6.1->@R2
643 DEC R2
    06D0 22
                                                                            ... STACK LEFT POINTING AT
                                                      R6.0->@R2
DEC R2
    06D1 8652
                                       644
                                                                           ... NEXT FREE LOCATION
    06D3 22
                                       645
    06D4 93B6
                                       646
                                                      R3.1->R6.1
                                                                           ... COPY R3 TO R6
    06D6 83A6
                                       647
                                                      R3.0->R6.0
```

```
06D8 46B3
                                                  @R6!->R3.1
@R6!->R3.0
                                   648
06DA 46A3
06DC 30CD
                                   649
                                   650
                                                   COTO CALLS-1
06DE
                                   651
                                                  SEP R3
R6.1->R3.1
R6.0->R3.0
INC R2
GR2!->R6.0
GR2!->R6.1
DEC R2
GOTO RET-1
06DE D3
06DF 96B3
06E1 86A3
06E3 12
06E4 42A6
                                                                        ... RETURN TO MAIN ... COPY R6 TO R3
                                   652
                                   653 RET:
                                   654
                                   655
                                                                        ... POP R6 FROM STACK
                                   656
06E6 42B6
06E8 22
                                   657
                                   658
06E9 30DE
                                   659
                                   660 ...
06EB
06EB
                                   661 ..
                                                     ROM CONSTANTS
                                   662 ...
06EB
                                              ORC #6F0
KPLCON: ,3000 ... TO COMPUTE KM/LITER
TENTH: ,3918 .. TENTH OF A KILOMETER
06F0
                                   663
06F0 0BB8
06F2 0F4E
                                   664
                                   665
06F4
                                   666
06F4
                                   667
                                                   .. RAM STORAGE REQUIRED
06F4
                                   668
                                   669 ...
06F4
                                   670
671
672 RAM:
673 KPII:
674 RPM:
0C00
                                                  ORG #C00
0C00
                                                   0C00
0C00 00
0C01 00
                                                  , 0
                                                                   .. PROPORTIONAL TO KM. PER HR.
                                   675 OST1:,0
0C02 00
0C03 00
                                   676 OST2:,0
677 OST3:,0
678 OCNT:,0,0
679 TCNT:,0
0C04 00
0C05 0000
0C07 00
                                                                        .. ODOMETER COUNT
0C08 0000
0C0A 00
                                   680 FCNT: ,0,0
681 KMPL: ,0
                                                                         .. FUEL COUNT
                                                                         ... CURRENT FUEL ECONOMY
0C0B
                                   682
                                   683 OUTBF: ... WORKING RAM BUFFER FOR DISPLAY
OCOB
OCOB
                                   684
OCOB
                                   685
OCOB
                                   686 END:
                                                  END
```

```
COSMAC CODE
FL LOC
                                    LNNO SOURCE LINE
FL LOC
                                    LNNO SOURCE LINE
    0000
                                                               J.M.C. RCA LABS
                                                  > MESS
                                                                                           8:16:76
    0000
                                          . . .
                                        3 ..
                                                       ELECTRONIC DASHBOARD NESSAGES
    0000
    0000
                                        4
                                           . . .
    0700
                                        5
                                                    ORG #700
    0700
                                        6
                                                   0700
           2020202020202020
                                          MESO:
                                        7
    0708 5345325649434520
                                        B
    0710 4252414B45204F4E
                                        9
    0718 2020202020202020
                                       10
    0720
                                       11
                                                    0720
            2020202020202020
                                          MES1:
    0728 202020444F4F5253
                                       13
    0730 204F50454E20
0736 2020202020202020
073E 2020
                                       14
                                       15
                                                    ,32,32
                                       16
    0740
                                       17
                                       18 MES2: .32,32,32,32,32,32,32,32
19 .32,32,32,32,32
20 .T'HAZARD'
21 .32,32,32,32,32,32,32,32
22 .32,32,32,32,32
    0740 2020202020202020
    0748 2020202020
074D 48415A415244
    0753 2020202020202020
075B 2020202020
                                       \overline{23}
    0760
                                       24 MES9: .32,92,32,32,32,32,32,32
25 ,T'BRAKE',32
26 ,T'FLUID',32
27 ,T'LOW',32
28 ,32,32,32,32,32,32,32,32
    0760 2020202020202020
    0768 4252414B4520
    076E 464C55494420
    0774 4C4F5720
    0778 2020202020202020
    0780
                                       29
    0780 202020202020
0786 2020
                                       30 MES4: ,32,32,32,32,32,32
                                                     .32,32,32,33
,32,32
,T'DANGER',32
,T'SLOW',32
,T'DOWN'
                                       31
    0788 44414E47455220
078F 534C4F5720
                                       32
                                       33
    0794 444F574E
0798 2020
079A 202020202020
                                       34
                                                    ,32,32
,32,32,32,32,32
                                       35
                                       36
    07/10
                                       37
    07A0 202020202020
                                       38 MES5: ,32,32,32,32,32,32
                                                    T'RESTRAIN'
T'T', 32, T'SYSTEM'
32, T'OUT'
    07A6 524553545241494E
                                       39
    07AE 542053595354454D
                                       40
    07B6 204F5554
                                       41
    07BA 202020202020
                                       \overline{42}
                                                    (32,32,32,32,32,32,32)
    07CQ
                                       43
                                       44 MES6: ,32,32,32,32,32,32,32,32

45 ,32,T'ANTI-'

46 ,T'SKID',32

47 ,T'OUT',32,32,32

48 ,32,32,32,32,32,32,32
    07C0 2020202020202020
07CB 20414E54492D
    07CE 534B494420
    0703 4F5554202020
0709 20202020202020
    07E0
                                       49
    07E0
                                       50
                                                       ANALOG SENSORS
    07E0
                                       51
    07E0 2020202020
                                       52 MES7: ,32,32,32,32,32
```

REFERENCES

- 1. D. Zur Heiden and H. Oehlen, "Radar Anticollision Warning System for Road Vehicles," Electrical Communications 52(2), 141 (1977).
- 2. G. Hahlganss and L. Hahn, "Headway Radar Using Pulse Techniques," Int. Conf. on Automobile Electronics, London, July 1976, pp. 132-135.
- 3. E. Dull and H. Peters, "Collision Avoidance System for Automobiles," Society of Automotive Engineers, Publication #780263, March 1978.
- 4. F. E. Nathanson, Radar Design Principles, (McGraw-Hill Publishing Company, New York, 1969).
- 5. S. A. Hovanessian, <u>Radar Detection and Tracking Systems</u>, (Artech House, Inc., Massachusetts, 1973).
- 6. E. F. Belohoubek et al., "Electronic Subsystems for Research Safety Vehicle (RSV)," Final Report, Phase II, 1976.
- 7. S. Silver, Microwave Antenna Theory and Design, Rad. Lab Series, Vol. 12, Boston Tech. Publications, 1964.
- 8. J. Shefer et al., "A New Kind of Radar For Collision Avoidance," SAE Automotive Engineering Congress and Exposition, Detroit, Michigan, February 26, 1974.
- 9. G. S. Kaplan and F. Sterzer, "Dual-Mode Automobile Collision Avoidance Radar," SAE Automotive Engineering Congress and Exposition, Detroit, Michigan, February 24-28, 1975.
- 10. A. G. Kandoian et al., <u>Reference Data for Radio Engineers</u>, International Telephone & Telegraph Corp., New York, 1964.
- 11. R. Limpert, Motor Vehicle Accident Reconstruction and Course Analysis, Michie Company, Charlesville, VA, December 1978.
- 12. R. F. Freiman, "PRICE A Parametric Cost Modeling Methodology," RCA Government and Commercial Systems, Cherry Hill, NJ, May 1978.

APPENDIX B

VOLVO OF AMERICA CORPORATION FINAL REPORT

LARGE RESEARCH SAFETY VEHICLE (LRSV) ENGINE DEVELOPMENT

LARGE RESEARCH SAFETY VEHICLE (LRSV)

ENGINE DEVELOPMENT FINAL REPORT

February, 1981

Minicars, Inc. Subcontract Purchase Order #5185

Prepared by:

Product Planning & Development Department Volvo of America Corporation Rockleigh, New Jersey 07647

Volvo of America Corporation, Rockleigh, New Jersey 07647

ABSTRACT:

The intent of the Large Research Safety Vehicle (LRSV) program is to research passenger car technology for the purpose of meeting the discussed safety, fuel economy and emission standards for the mid 1980s. It is also the goal of that program to be able to meet these standards while still retaining the comfort and size of an automobile typical to the U.S. motoring public.

Volvo of America Corp., (VAC) under contract to Minicars, Inc. of Goleta, California, and subcontract to the LRSV program, agreed to provide an engine capable of meeting the defined fuel economy, performance and emission goals of that program.

This report describes the procedure and results by which a refined spark ignition engine was developed, constructed, tested and provided for that program.

TABLE OF CONTENTS

TITLE		PAGE
INTRODU	JCTION AND SUMMARY	1
PROCED	URE	4
RESULTS		8
APPENDI	x	
Α.	General Specifications and Performance Objectives	20
в.	General Description of the Lambda-Sond Air Fuel Control System	23
C.	Development Test Equipment Description	28
D.	FTP Results	32
E.	Task Results	35
F.	Observed and Calculated Data Recorded During Dynamometer Study	47
G.	Steady State Emission Data	52

LIST OF FIGURES

FIGURE	TITLE	PAGE
1	Manifold Vacuum vs. Time (1978 FTP)	13
2	Engine Break In Schedule Manifold Vacuum vs. Time	14
3	Engine Break In Schedule Engine Speed vs. Time	14
4	BSFC vs. Rpm B-21 and B-19 at WOT	15
5	BSFC vs. Rpm B-19 at 13" Hg	15
6	Exhaust Emissions B-19 at 13" Hg	16
7	BSFC vs. Rpm with Synthetic Oil at 13" Hg	16
8	BSFC vs. Rpm with Reduced Accessory Drive at 13" Hg	17
9	BSFC vs. Rpm with MSD Ignition at 13" Hg	17
10	Max. Hp Production B-19 and Turbo B-19	18
11	Boost Retard System	18
12	Crankcase Pressure vs. Rpm at 13" Hg	19
13	Engine Performance Measurement System	30
14	Engine Dynamometer Fuel Measurement System	30
15	Engine Dynamometer Exhaust Emission Measurement	31
16	LRSV Engine Performance Turbo, Normally Aspirated	35

17	Predicted LRSV Performance	37
18	Predicted Acceleration Curve	38
19	Actual Acceleration Times LRSV - Volvo - Chassis	44
20	Predicted Emission Levels and Fuel Economy at 50,000 Miles	45
21	Zero Mile Test Data	46

INTRODUCTION AND SUMMARY:

The need for clean running and fuel efficient vehicles combined with passenger comfort and safety are major concerns for car manufacturers.

Aware of the need to research such technology, the U.S. Government through U.S. DOT/NHTSA implemented the Large Research Safety Vehicle (LRSV) program.

Volvo of America Corp. (VAC), under contract to Minicars, Inc. of Goleta, California, and subcontract to the LRSV program, agreed to supply a refined spark ignition engine capable of meeting the program objectives. The program commenced with Issuance of Subcontract January 20, 1978 and was concluded Summer, 1979.

The program's intentions, as set by NHTSA, specified development of technology which may be translated into a feasible, affordable, mass-produced product for the mid-eighties but did not necessarily require the provided engine to be an actual production engine.

The engine program had the following goals to be met:

EXHAUST EMISSIONS

Objective	Maximum Acceptable	
HC41 g/mi	HC41 g/mi	
CO - 3.4 g/mi	CO - 3.4 g/mi	
NOx4 g/mi	NOx - 1.0 g/mi	

FUEL ECONOMY

Objective

27.5 mi/gal. combined EPA cycle

ACCELERATION

Objective	Maximum Acceptable
0-60 mph - 13.5 secs.	0-60 mph - 20.0 secs.

The general specification and performance objectives are further detailed in Appendix A.

To this end, DM Engineering, Inc. of Brookfield, Conn., under VAC direction, was contracted to complete the hardware development and construction of the LRSV engine.

With their assistance, a methodology was developed for considering what technical features would be incorporated and the means by which they would be tested.

As an overview, technical modifications to be developed would be centered around: improving cycle and thermal efficiency, reducing internal frictional losses and rotational mass, and improving combustion characteristics within established emission levels.

The basic engine selected for the program was the Volvo B-21F 2.1 inline 4 cylinder engine. To stay within the intent of the program, a serious effort was made to retain as much of the present engine as possible. It was further realized that the Lambda-Sond feedback control system, would form a vital part of the program. A detailed description of the system is presented in Appendix B.

The program for the engine was out. ned to follow this course of development: initially candidate technical modifications were to be evaluated with the engine on a dynamometer and run under a predetermined steady state condition. All the modifications which were found to improve either the fuel efficiency or emission characteristics would be explored further with the aim to be incorporated into the final refined engine. Subsequently, the refined engine would be installed in a Volvo 244 DL with over-drive transmission and developed on DM's chassis dynamometer. Once completed, the LRSV-Volvo chassis would undergo final development and fine-tuning at an approved EPA lab. Results would then be verified on the FTP cycle.

During the approved EPA lab testing the dyno horsepower would be set to the PAU (Power Absorption Unit) setting for the actual LRSV chassis, as determined by Minicars. Upon completion of this course of development, a duplicate EPA test cycle would be run to verify the repeatability of the results. The Volvo test chassis would serve the dual purpose of investigating and determining specific gear ratios and proving acceleration times and driveability.

From this work the following refinements were found to be beneficial: reduced engine displacement, elevated coolant temperature, synthetic engine lubricants, reduction of accessory drive speed, multi-spark capacitive discharge system, reduced rotational mass, and matched fuel injectors.

As a result of these technical features and tuning the program goals were met. They account for an approximate 15% increase in fuel economy over the stock production engine while remaining within the emission and acceleration objectives.

* The name Lambda-Sond is a registered trademark of A.B. Volvo.

It should be noted that the engine, including turbocharger as developed in the program and tested in the Volvo chassis, met the test goals. However, when the engine was fitted to the LRSV the turbo was removed to ease installation. It was found that all the program goals could be met with the engine in its normally aspirated version, and therefore this vehicle configuration was pursued.

Following January, 1980, the initial LRSV program was extended to facilitate replacement of original engine and further fitting and testing. For this, DM Engineering was named as the prime contractor with Volvo of America Corporation, again, named as a subcontractor.

The final results stated below were acquired with DM as the prime contractor.

To clarify and conclude, this is a special research engine that was carefully prepared for the needs of this program. Therefore, it should be realized that application of all the refinements would not necessarily yield the same results in a production car or in a production environment. Rather, it should be concluded that gains in fuel economy can be attained with the utilization of a similar engine development program.

Results:	<u>LRSV</u>
Emissions:	
HC CO NOx	0.19 gpm 2.38 gpm 0.57 gpm
MPG:	
EPA City (Est.) EPA Highway EPA Combined	22.8 mpg 36.5 mpg 27.43 mpg

Dyno Setting: 10.8 hp @ 50 mph Inertia Weight: 3250 lbs.

PROCEDURE:

The goal of the LRSV engine development program was to arrive at a Volvo B-21 based power plant which would meet established emissions and fuel economy levels as measured by the 1978 FTP emission/fuel economy cycle and 0-60 mph acceleration times.

To expedite development, a modeling "tool" was devised to approximate the transient conditions of the FTP test cycle. Therefore, it was desired to find a steady state condition which would, on a "first cut" basis, resemble the driving cycle. In this way, the effect of technical features or modifications could be assessed to determine the contribution to the program. The exact effect of all the technical additions would later be verified by the testing on the FTP cycle.

To determine this steady state condition, a 1978 B-21F Lambda-Sond engine was fitted with a vacuum transducer to monitor intake manifold pressure. The obtained vacuum trace, along with a speed trace of the driving cycle, allowed an average engine load schedule to be developed.

Calculating the N/V ratio (engine RPM in 4th. gear/mph) of the test Volvo led to an rpm range which the engine operated during the EPA cycle. This rpm range was later corrected for the actual LRSV drivetrain N/V ratio. Subsequently, an engine dynamometer testing schedule was structured to record various engine performance and operating conditions under partial and wide-open throttle.

These recorded engine parameters are:

- 1. Engine RPM
- 2. Engine Torque
- 3. Engine Air-inlet Temperature, Dry Bulb
- 4. Engine Air-inlet Temperature, Wet Bulb
- 5. Barometric Pressure
- 6. Engine Oil Pressure
- 7. Engine Water Temperature

- 8. Engine Inlet Oil Temperature
- 9. Engine Fuel Flow Rate, Pounds per Hour
- 10. Exhaust gas %CO
- 11. Exhaust gas HC, ppm
- 12. Exhaust gas NOx, ppm
- 13. Manifold Vacuum/pressure
- 14. Ignition Patterns/RPM

For reference, a description of equipment used and its application is presented in Appendix C.

A list of technical modifications were compiled for evaluation and, as stated earlier, these modifications include:

- 1. Reduction in displacement (2.1 liter to 2.0 liter)
- 2. Substitution of synthetic engine oil
- 3. Reduction of accessory drive speed
- 4. Addition of a multi-spark capacitive discharge ignition system
- 5. Elevated engine coolant temperature
- 6. Turbocharging
- 7. Reduction of engine lubricant pumping losses
- 8. Reduction of crankcase pressure

It was anticipated, from the onset, that a reduction in engine displacement from 2.1 L to 2.0 L would be beneficial to the program. This would be accomplished by utilizing a B-19 engine block with a B-21 Lambda-Sond cylinder head. Therefore, initial break-in and running would be done with a B-19 block.

Engine development began with three B-19 engines being broken in and baselined. The engine break-in was accomplished by operating these engines on the engine dynamometer over a predetermined vacuum and RPM schedule. The schedule was arrived through the use of factory recommended break-in schedules. (The total break-in time for each engine was 30 hours.) All three engines, at completion of their break-in, were baselined to determine their relative horsepower, torque and brake specific fuel consumption (BSFC).

The third engine remained on the dynamometer to begin evaluation of the candidate modifications previously mentioned.

Simultaneously, engines #1 and #2 were disassembled to determine their dimensional consistency. After measuring, #1 engine was blueprinted and balanced. It should be noted that the machining of these internal engine parts were maintained within production tolerances but brought to a finer degree of precision than normally found in factory production.

For reference, the following describes some of the tolerances incorporated into the LRSV engine:

	<u>B-21</u>	LRSV
Cylinder Bores	+/0004"	+/0001"
Piston Diameter	+/002'	+0/002"
Piston Weight Variation	+/220 oz.	+0/010 oz.
Connecting Rod Weight	+/180 oz.	+0/004 oz.

Engine #1 was reassembled according to recommended Volvo procedure and subsequently broken in and baselined.

Concurrently, engine #2 was reassembled to serve as an installation mock-up for the turbocharging system. This turbocharging layout was then re-installed on engine number one.

The turbo air delivery pressure capability of the turbocharging system was matched according to operational requirements of the B-19 engine. Similarly, boost levels and knock suppression system (water injection) were matched and installed.

At conclusion of the testing program those modifications which were significant or necessary were incorporated onto #1. This engine was then installed into a 1978 244DL Volvo for final testing.

In addition to the engine modifications, a series of power train modifications were assessed and included into the final test chassis. These modifications include:

- 1. Reduction of engine rotating mass by reducing the flywheel, clutch and pressure plate size and weight.
- 2. Addition of synthetic lubricants in the transmission and rear axle.
- 3. Optimization of transmission and rear axle ratios with available ratio.

This engine and chassis were then tested at New York City Department of Environmental Protection, Air Resources Lab in Brooklyn, New York to optimize and confirm results on the EPA cycle.

To facilitate the final stages of development and tuning a series of hot starts, using the 1972 Federal Driving Cycle, were run. During these tests, the performance of the Lambda-Sond system, catalytic converter and engine were monitored by continuous reading of the HC and CO reading before the catalyst and HC, CO, CO₂ and NOx levels at the tailpipe. Analysis of these results returned sufficient data to reasonably predict performance of both emission and fuel economy on the FTP composite and highway cycle.

Final test verification was run on the 1978 EPA Test Procedure which required a 12 hour cold soak prior to the city and highway cycle.

RESULTS:

(All figures referenced are included immediately following the result section of this report).

As stated from the Procedure Section of this report, it was desired to establish a steady state condition which could serve as a "modeling tool" to expedite technical trend analysis during initial stages of development.

The installed manifold vacuum transducer yielded a trace, a section of which is described on Figure 1, which when integrated manually, indicated a load corresponding to 13" Hg would approximate the transient conditions of the test cycle. Further, a speed trace of engine speed range yielded a test range of 1600 to 2800 Rpm.

Engines were broken in and baselined according to the "break-in" schedule described on Figures 2 and 3. The total break-in time was 30 hours each engine.

Using this modeling "tool", it was possible to evaluate a number of anticipated modifications in a fairly rapid manner. As stated in the previous section, the list of test modifications included:

- 1. Reduction in displacement (2.1 liter to 2.0 liter)
- 2. Addition of synthetic engine oil
- Reduction of accessory drive speed
- 4. Addition of a multi-spark capacitive discharge ignition system
- 5. Elevated engine coolant temperature

The below modifications were tested but for reasons noted later in the report were not included into the final engine.

- Turbocharging
- 2. Reduction of engine lubricant pumping losses
- 3. Reduction of crankcase pressure

Using the stated procedure in evaluating the above items, the following results were obtained:

Before continuing it should be emphasized that each candidate modification was in turn evaluated and compared against the baseline data from the stock B-19 engine. It should be understood that the results

of all the tests are <u>not</u> additive and the presence or effect of one modification will, in most circumstances, influence the results of the other modifications. Therefore, the combined effect of all these modifications will be diminished by the effect or change of engine operating characteristics caused by the other modifications.

To determine the effect of reduction of displacement from 2.1 L to 2.0 L under wide open throttle conditions (WOT), BSFC curves were generated for both engines. From these curves, Figure 4, it can be seen that there is a decrease in fuel consumption that varies from 3% at 1700 rpm to a maximum decrease of 8% at 4000 rpm.

The baselined B-19 BSFC curve is depicted in Figure 5; this curve is provided as a reference for comparison of following modifications.

Figure 6 is a graphical representation of the B-19 Lambda Sond engine emissions before and after the catalyst. For the remainder of this section, if emission levels are discussed, only emission levels before the catalyst will be considered.

The effect of the substitution of low viscosity synthetic lubricants was studied. Figure 7 shows the results of this test at 13" Hg manifold pressure. From the graph it can be seen that there was reduction in BSFC with a maximum decrease of 4% at 2200 rpm. This effect has been attributed to the reduced pumping loss from a lower viscosity oil and to a lesser extent, reduced friction in the main bearing, rod bearings and cylinder wall surfaces.

The alternator and water pump constituted the only engine driven accessories. Customarily, during the FTP cycle, the alternator would be driving no accessories and, therefore, at low load. However, it was anticipated that there would be a decrease in BSFC if the accessory drive speed was reduced.

This was accomplished with the installation of 3.75' diameter crank pulley as opposed to the stock pulley diameter of 5.50" diameter. This accounted for a 30% reduction of accessory drive speed. The largest decrease in BSFC, as shown on Figure 8, was 7% at 2200 rpm.

A commercially available multi-spark ignition system was installed and tested. This system is designed to spark repetitively over 30° of crank-shaft rotation. Referring to Figure 9, there was a decrease in BSFC over the range of 1600 to 2500 rpm.

It was believed that emissions could be attenuated particularly during certain parts of the FTP (Bag 1), if the cooling system was modified to raise the coolant temperature above the standard 195°F. The two test temperatures were selected at 210°F and 220°F. The cooling system was modified by: removing the engine driven fan and replacing it with an electric fan activated by a temperature switch sensing coolant temperature, and the installation of a thermostat of the correct opening temperature.

By increasing the coolant temperature, it was speculated that there would also be a simultaneous improvement in cycle efficiency which would return correspondingly lower BSFC. However, only when the 220°F coolant temperature was used was there a noticed decrease in BSFC over the test range of 1600 to 2800 Rpm. Due to the risk of thermal degradation to the engine, the lower test temperature of 210°F was used. When evaluating the 210°F coolant temperature over the same test range, the change in fuel efficiency was only marginal.

The final system, as installed on the LRSV, utilized the mentioned electric fan with a thermostatic temperature setpoint of 210°F on, 200°F off.

Finally, fuel injectors were flowed to obtain matched sets of injectors ensuring consistent cylinder to cylinder A/F ratios. Eight sets of nozzles were flowed at A/F meter control arm openings of 1/4, 1/2, 3/4 and full open to determine flow rate consistency. Of all eight sets, one set would flow to within 2% variation up to a 1/2 control arm opening, and one more set would hold up to 3% variation in flow rates up to 3/4 A/F ratio control arm opening. In the other cases, variations of up to 4% were encountered.

Earlier exploration of BSFC curves and engine maps revealed that there would be a need to decrease the N/V ratio. It was further speculated that reduced rotational mass would reduce inertial losses and enhance fuel economy. This was accomplished via the following methods:

N/V ratio was lowered by utilization of overdrive ratio on 1st, 2nd as well as engaged 5th overdrive ratio on the highway cycle above 45 mph. The rear axle ratio was lower (numerically) to a 3.54 ratio as opposed to the standard 3.91 axle. Utilizing this, the N/V ratio was lowered to 51.8 at 4th. or 41.3 in 5th. (O.D.) compared to the stock N/V ratio of 57.2 in 4th. and 45.5 in 5th. (O.D.).

Inertial losses were reduced during acceleration through utilization of a lighten flywheel, clutch and pressure plate. To accomplish this, the stock flywheel was machined to reduce the flywheel weight to 11 lbs. A Borg Beck pressure plate and clutch was added, bringing the entire installed weight of the assembly to 23lbs. This compares to a stock flywheel, clutch, and pressure plate weight of 34 lbs.

As mentioned earlier, special attention was given to the control of the Lambda-Sond system. Before continuing, it is necessary to briefly describe the system. The system centers itself around controlling the HC, CO, NOx levels from the engine to a degree of accuracy so as to accommodate the very narrow operating conditions needed for the three-way catalyst to be effective in reducing the three pollutants. This is accomplished by sensing the oxygen present in the exhaust system and altering air/fuel ratio to make the appropriate change. A more detailed description of the system operation is presented in Appendix B.

During the EPA testing, it became evident that tighter and better control of the Lambda-Sond controller would be necessary for this application.

Initial findings indicated that it would be advantageous for emission reduction to lean the mixture during the cold start portion of the composite cycle.

To accommodate this, the sensor voltage was lowered according to coolant temperature. This was accomplished with a thermostat set to the correct temperature level making the appropriate change in the controller internally. The best results were achieved with a 400 mv sensor voltage during cold condition changing to 550 mv as coolant temperature reached 180°F.

During testing it was found helpful in reducing exhaust emission to insulate the exhaust header and catalytic converter. The insulation required a thermal conductivity of .55 BTU/hr/sqft/OF/in. and thickness of i/2".

The specific results of the FTP testing which commenced 9/18/78 and was concluded on 8/2/79 are presented in Appendix D. The development program was concluded with a repeated cycle for verification of results.

As noted earlier, certain modifications were tested but for reasons described below were not included into the final engine. As these modifications were part of the initial program, the results obtained are discussed below.

When the program was initially proposed, it was felt that the additional hp and torque provided by turbocharge boosting would be necessary for meeting acceleration objectives. As stated previously, it was later found that the naturally aspirated version would meet the program objectives.

Initially when the turbocharger was fitted, it was fitted to an exhaust manifold with similar primaries, but no secondary exhaust head pipe.

The turbo and manifold were then installed and tested, but provided actually lower hp. at high manifold vacuum than the stock engine. The manifold was then redesigned to include the secondary exhaust head pipe. After investigation of the manifolding system, the best configuration was found to be the stock exhaust head pipe coupled with a fabricated "J" pipe which duplicates the secondaries of the stock engine.

The turbo was then matched to the engine such that positive pressure boost from the compressor was not utilized below 2500 rpm. This was accomplished by testing of various capacity exhaust housings. The engine was then dynamometer tested under load to determine the knock limited boost, which under these circumstances is 4 PSIG boost.

The maximum horsepower output was then tested and recorded under WOT conditions. The results are shown on Figure 11. Referring to this figure, maximum boosted turbo power is 122 hp. at 5000 rpm compared to the naturally aspirated version with 100 hp at 5000 rpm.

Knocking was suppressed via a modulated water injection system which would introduce water into the turbo compressor inlet according to engine load as determined by manifold pressure. Additionally, an independent manifold fuel injector was installed to both deter knocking and introduce additional fuel required for boost conditions.

Knocking was further deterred by a vacuum ignition retard system as described on Figure 12. Under boost conditions, the in-line check valve closes and supplies positive pressure to the diaphragm retarding the system. At a maximum boost of 4 PSIG, ignition can be retarded up to 8°.

Reducing engine lubricant pumping losses was next investigated. Most engine oil pressure levels are somewhat higher than necessary to maintain bearing life. Therefore, it was felt that if the oil pressure could be lowered to a level somewhat above a critical level, the oil pumping horsepower could be reduced increasing BSFC. This was accomplished by modifying the existing oil pump to output 35 PSI instead of 65 PSI.

After evaluation of oil pressure reduction, it was found there was only a marginal improvement in horsepower output and in lieu of the possible reduced bearing life, it was felt that this modification did not warrant installation onto the final LRSV engine.

Positive crankcase pressure increases the pumping losses induced by the piston movement. In certain instances, output horsepower increases if this pressure is reduced. This reduction in crankcase pressure is usually accomplished by "syphoning" the engine's crankcase into the intake manifold. In most cases, this type of system is working well if zero crankcase pressure is maintained. Referring to the Figure 12 which correlates crankcase pressure of a production Volvo B-19, operating at 13.0 inches Hg manifold vacuum and at wide open throttle full load, it can be seen that the production system functions extremely well. Therefore, crankcase pressure reduction was considered of marginal benefit and not included in the final engine.

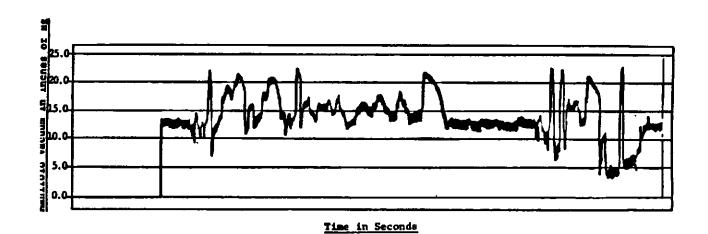


Figure No. 1. Manifold Vacuum vs. Time - 1978 B-21 Volvo Manifold

Vacuum During 1978 FTP Driving Cycle

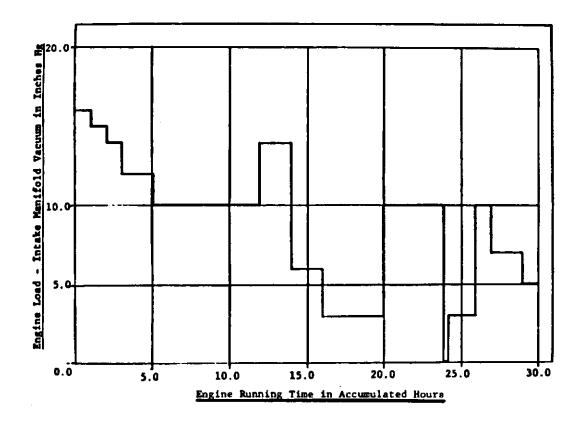


Figure No. 2. Engine break-in Schedule - Manifold Vacuum vs. Total Time

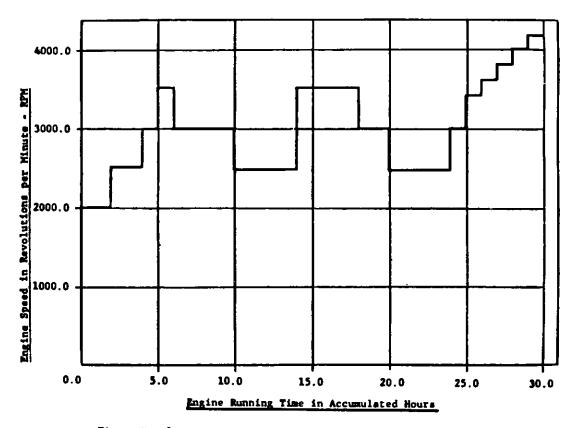
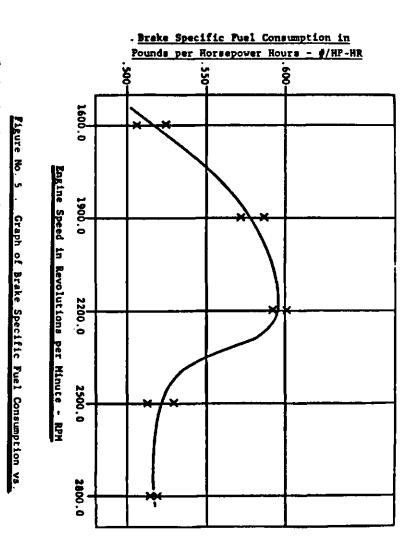
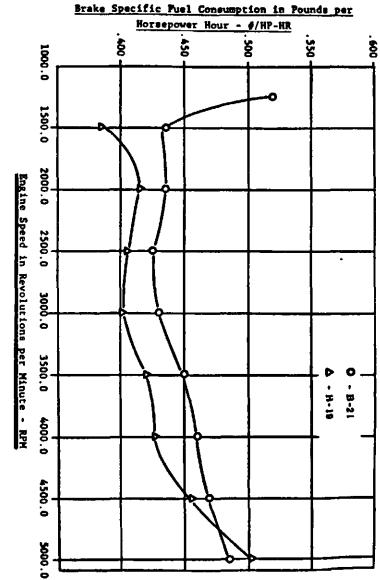


Figure No. 3. Engine Break-in Schedule - Engine Speed vs. Total Time

Volvo B-19 Operated at 13.0 Inches (Hg) Intake Manifold Vacuum B-15.



for Volvo B-21 & B-19 Engines Evaluated at Wide Open Throttle Graph of Brake Specific Fuel Consumption vs. Engine Speed



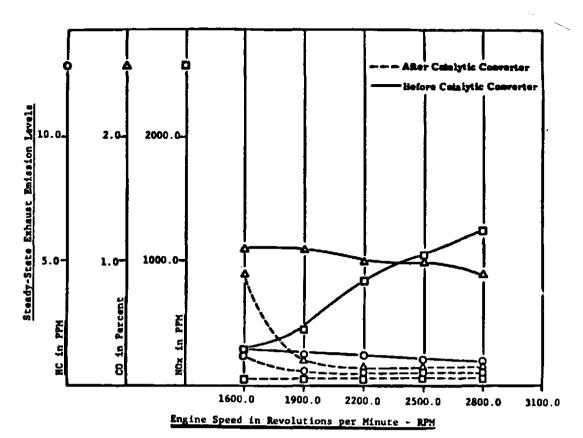


Figure No. 6 . Graph of Steady-State Exhaust Emission Levels vs. Engine Speed -Volvo B-19 Engine Operated at 13.0 Inches Hg Intake Manifold Vacuum

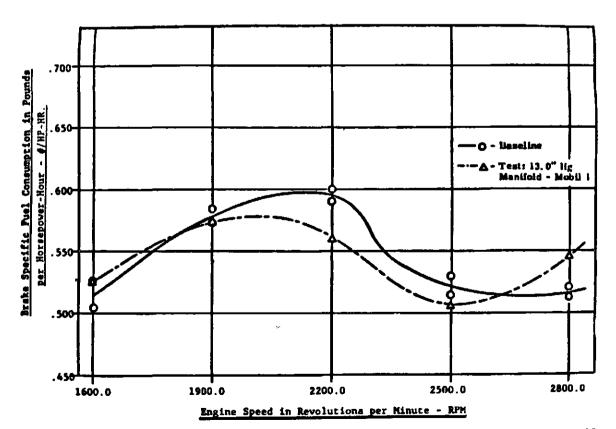


Figure No. 7. Graph of Brake Specific Fuel Consumption vs. Engine Speed - Volvo B-19
Engine Operated at 13.0 Inches Hg Intake Manifold Vacuum with Synthetic Engine Oil

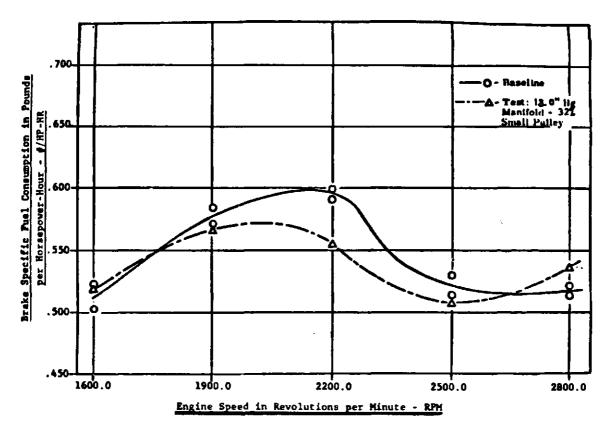
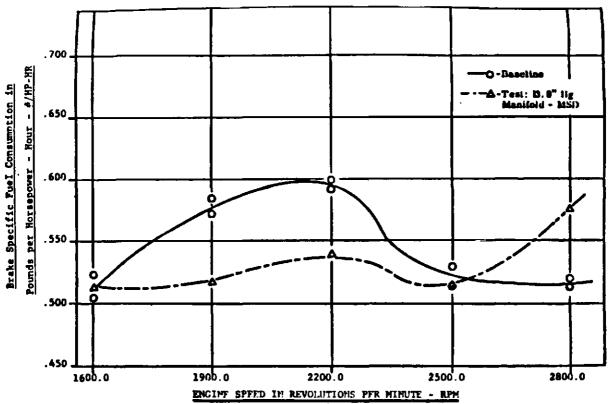


Figure No. B Graph of Brake Specific Fuel Consumption vs. Engine Speed - Volvo B-19

Operated at 13.0 Inches Hg Intake Manifold Vacuum with a 30% Reduced Diameter Crankshaft Pulley



YIGURE NO. 9 Graph of Brake Specific Fuel Consumption vs. Engine Speed

Volvo B-19 Operated at 13.0 Inches Intake Manifold Vacuum With Multi-Spark

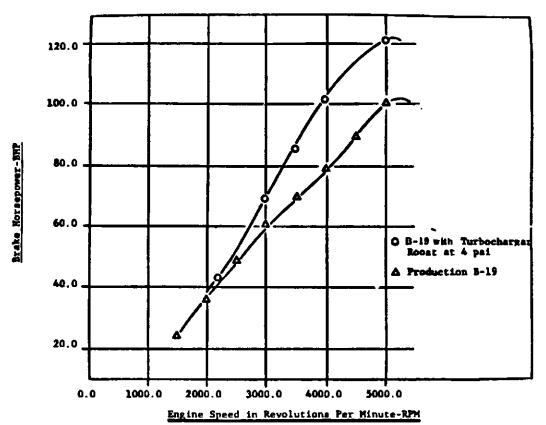


Figure No. 10 Graph of Brake Horsepower vs. Engine Speed - Production Volvo B19 and Balanced-Blueprinted- Turbocharged Volvo B-19

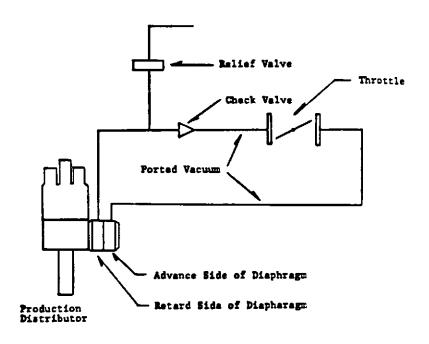


Figure No. 11 Boost Pressure Retard System

Figure 12 Crankcase Pressure as Recorded Against Engine Speed at 13" Manifold Vacuum and Wide Open Throttle

Engine Speed-RPM	Load-Speed	Crankcase Pressure
1600.0	13.0 in. Hg	0.0 in H ₂ O
1900.0	п	n
2200.0	п	n
2500.0	п	n
2800.0	IT	2 in
1500.0	WOT	1.2 in
2000.0	11	1.0 in
2500.0	11	.8 in
3000.0	11	.3 in
3500.0	n	.2 in
4000.0	n	0.0 in
5000.0	71	0.0 in

APPENDIX A GENERAL SPECIFICATIONS AND PERFORMANCE OBJECTIVES

This section defines 1) the preliminary design specifications for the LRSV; 2) the performance specification for the LRSV when powered by the Engine to be furnished by VAC, and 3) the general specifications for that Engine when it is configured for installation and operation in the large RSV.

I. LRSV SPECIFICATIONS

The specifications that follow describe the preliminary configuration of the LRSV. These specifications will be updated as the engine/vehicle interface and LRSV designs evolve into their final forms.

Vehicle Type

4-door, 6-passenger sedan; front engine, front wheel drive

Inertia Weight Class: 3,000 lbs.

Weight Distribution 52/48

Front/Rear (with driver)

Wheelbase: 115.0" Width 76.0"

Length: 213.0" Height 59.3"

Track, Front/Rear: 63'/63'

Ground Clearance: 6.0"

Fuel Capacity: 10 U.S. gallons

II. LRSV PROGRAM GOALS

The LRSV Engine shall provide the following performance:

Exhaust Emissions

As an objective, the levels of exhaust emissions shall be:

HC 0.41g/mi; CO 3.4g/mi; NOx 0.4g/mi. The maximum acceptable emissions levels shall be: HC .41g/mi; CO 3.4g/mi; NOx 1.0g/mi. Exhaust emissions performance is to be determined according to test procedures used for 1978 EPA Certification. Data based on sound engineering practice shall be provided to show that the LRSV can be reasonable expected at low emissions levels throughout a projected 50,000 miles of normal use.

Fuel Economy

The minimum acceptable fuel economy of the LRSV shall be 27.5 miles/gallon for combined EPA city and highway driving. The fuel economy performance is to be determined according to 1978 EPA Fuel Economy Test Procedures.

Acceleration

As an objective, the LRSV shall accelerate from 0 to 60 mph in not more than 13.5 seconds. The maximum acceptable time for this acceleration shall not exceed 20.0 seconds.

III. ENGINE SPECIFICATIONS

The Engine to be furnished for the LRSV shall be based on a modified design of the 1977 Volvo B21 engine. The specifications that follow describe the preliminary Volvo B21 engine configuration revised for LRSV use.

Type

Liquid cooled 4 cylinder in-line
with cast iron block, light-alloy
cylinder head of cross flow design;

belt driven overhead camshaft

Displacement 2017cc

Bore 3.53" (89 mm)

Stroke 3.15" (80 mm)

Compression Ratio 10.4:1

Maximum Output Estimated SAE net H.P.: 122

@ 5,000 rpm

Fuel Requirements 91 RON unleaded gasoline

Fuel Induction Bosch K Jetronic continuously

manifold injected system with exhaust oxygen sensing mixture correction and three-way catalyst

Ignition System Autotronic Controls Corporation

High energy multi spark capacitive

Discharge system

Standard engine driven accessory equipment

770 watt (55 amp) alternator

Starter

810 watt, 1.1 HP

Cooling system

Positive pressure, closed system with cross flow radiator and separate expansion tank. Radiator fan and fan drive to be supplied by Minicars. System capacity: 10 qts. (9.5 liters) 50% water/glycol

solution

Temperature activated electric

fan, set point 210°F

380 lbs. max.

Clutch

Borg and Beck pressure plate and flywheel with lighter flywheel. Cable operated Borg and Beck dry plate type

Miscellaneous

Lubrication system adopted to synthetic oil plus other friction reduction modifications.

A three-way catalytic converter and an appropriately configured exhaust head pipe to connect it to the turbo charger discharge connection shall be provided.

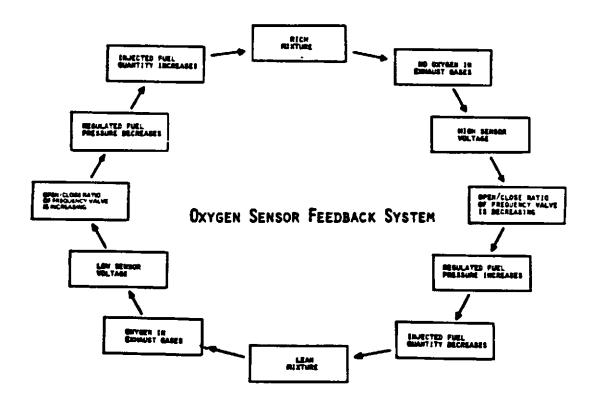
Engine Weight

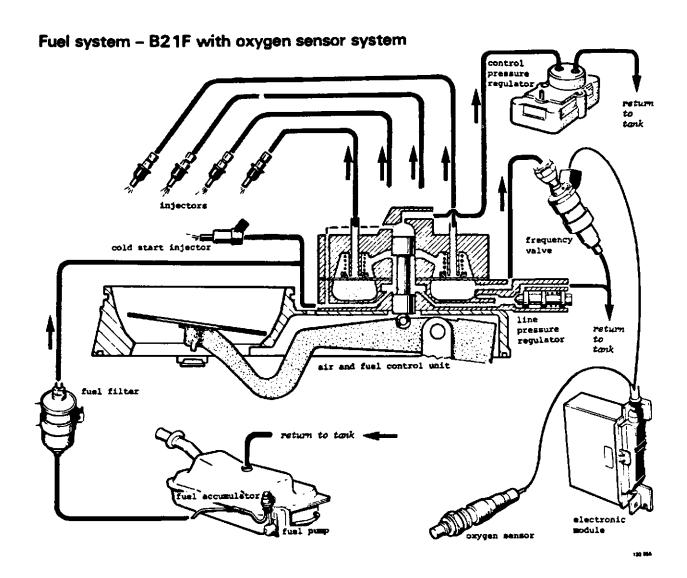
Estimated net, including engine mounted accessories and components as indicated excluding fluids,

APPENDIX B-GENERAL DESCRIPTION LAMBDA-SOND AIR FUEL CONTROL SYSTEM

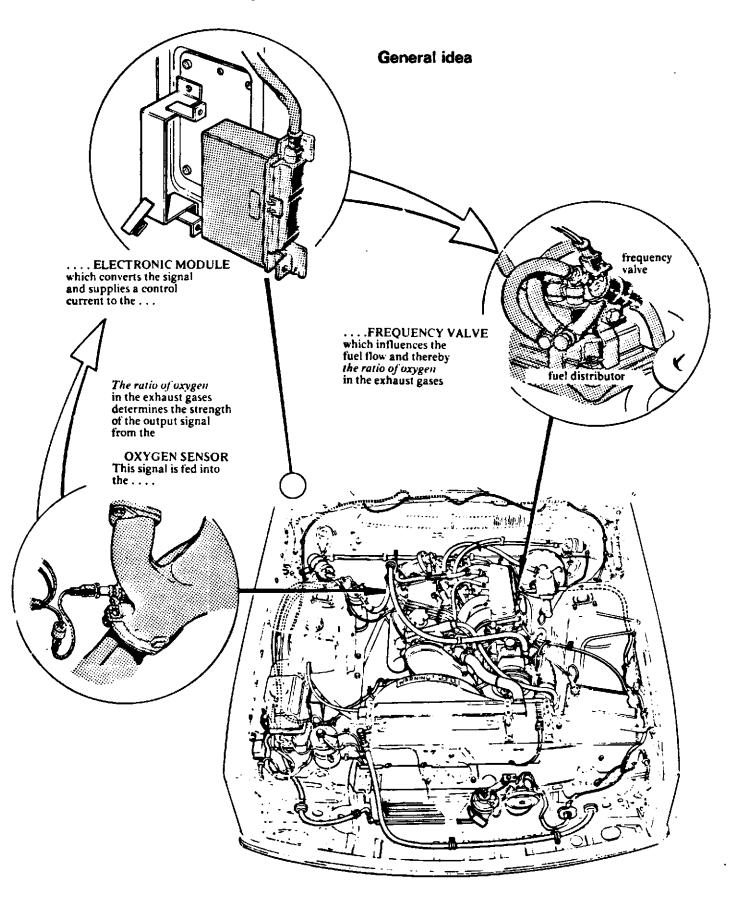
The following description has been excerpted from a Volvo Publication:

The Lambda-Sond oxygen sensor feedback system, described in the flow chart below, is a self-tuning engine control system designed to reduce emissions and improve fuel economy. An exhaust gas sensor, (oxygen sensor, also called Lambda Sensor) monitors the composition of the exhaust gases leaving the engine. The exhaust gas analysis is fed into a closed loop feedback system. This continuously adjusts the air/fuel ratio to provide optimum conditions for combustion and efficient elimination of all three of the major pollutants (HC, CO, NOx) by a 3-way catalytic converter.





Description of Oxygen Sensor Feedback System

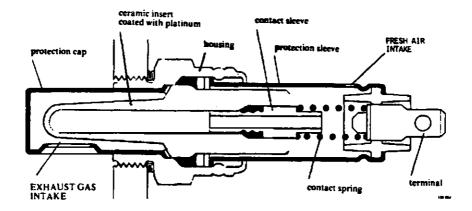


OXYGEN SENSOR

The exhaust gas sensor, called oxygen sensor, is located in the exhaust manifold. It consists of a platinum coated ceramic tube. The inside is connected to atmosphere, while the outside extends into the exhaust gases.

An electrical potential is built up according to air/fuel ratio. There is a steep transition just at the point where the air/fuel ratio is ideal.

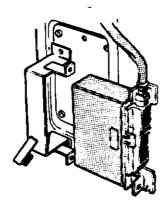
The electrical potential is high (approx. 1 volt) with low content of oxygen in the exhaust gases (= rich mixture) and low (approaching 0 volt) when the mixture is lean (= oxygen surplus).



ELECTRONIC MODULE

The output from the oxygen sensor is fed into an electronic unit, called the electronic module. This device supplies a control current to the frequency valve. The control current has a set frequency and operates by varying the duty cycle.

The electronic module is located inside the vehicle, at the right side in front of the right door. In this position it is protected and is close to the oxygen sensor and the electrical system.

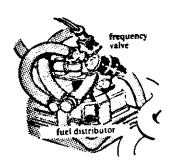


FREQUENCY VALVE

This device influences the fuel flow by influencing the pressure on the underside of the diaphragm in the pressure regulating valves in the C1 System.

It is located on a bracket behind the fuel distributor on the left side of the engine.

The frequency valve operates on a set frequency and by varying the duty cycle (ratio of closed/open circuit).



APPENDIX C DESCRIPTION ENGINE DEVELOPMENT APPARATUS

The testing apparatus as used in the engine dynamometer engine development can be divided into three basic systems:

- 1. Engine performance measurement
- 2. Engine fuel consumption measurement, and
- 3. Engine emission measurement.

Because direct correlation between FTP cycle results and engine dynamometer fuel economy and emission data is very difficult to obtain, the engine dynamometer measurement systems were used only for trend analysis of the effects of select modifications. This offered the ability to weigh the relative value of each modification. Considering the preceding, the following is a partial description of the test apparatus for information purposes.

The engine performance measuring system is shown in diagrammatic form in Figure No. 13. The engine parameters measured in this system are as follows:

- 1. Engine rpm
- 2. Engine torque
- 3. Engine air inlet temperature, dry bulb
- 4. Engine air inlet temperature, wet bulb
- 5. Barometric pressure
- 6. Engine oil pressure
- 7. Engine water temperature
- 8. Engine inlet oil temperature
- 9. Manifold vacuum/pressure

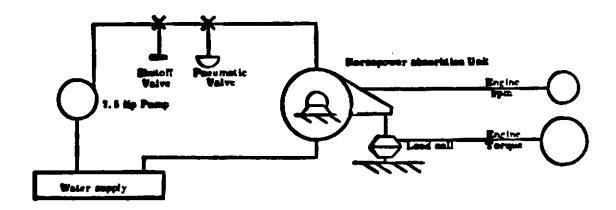
This system centers around a water absorption type dynamometer unit and is controlled by varying the flow of water through the unit using an analog pneumatic valve arriving at the engine's output horsepower. The absorption dynamometer's water supply consists of a 3,000 gallon capacity reservoir. The water is maintained at a constant temperature using an external water cooling tower. Engine torque was measured using a pressure transducer as a load cell. The torque measurement system was calibrated daily using a detachable arm and calibrated weights. Engine rpm was measured using a mechanical tachometer calibrated in place.

Oil pressure, manifold vacuum, and fuel pressure were measured using Bourdon Tube mechanical gauges. Oil and water temperatures were measured using resistance type electric gauges. Air inlet wet and dry bulb temperatures were continuously monitored throughout the testing series using thermistors. Finally, barometric pressure was measured using a temperature compensated Taylor aneroid barometer.

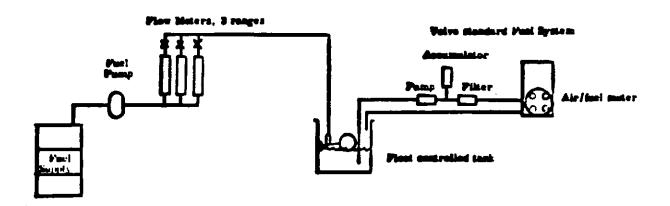
The fuel measurement system, shown in Figure No. 14, is calibrated to read engine fuel flow rate in pounds per hour. The system consisted of the following: An aircraft type fuel pump supplying fuel to one of three Rotometer type flow meters ranging: 3-30 lbs/hr, 20-190 lbs/hr and 50-350 lbs/hr. The use of any one of the flow meters was determined by opening and closing the appropriate valves. Fuel continues into a level controlled tank which acts as the fuel reservoir for the Volvo system.

The exhaust emission measurement system equipment was chosen to be of the infrared type. This measurement system, shown in Figure No. 15 is explained as follows: Exhaust gas, sampled from before and after the catalytic converter enters discreet stainless steel lines into an ice bath cooler. From the cooler the gases enter two inline 0.6 micron filters and into the systems' pump. From the pump, gases flow into two discreet flow meters and one line enters a NOx oven and the NOx cell, while the other enters a condenser, a HC cell, and CO cell.

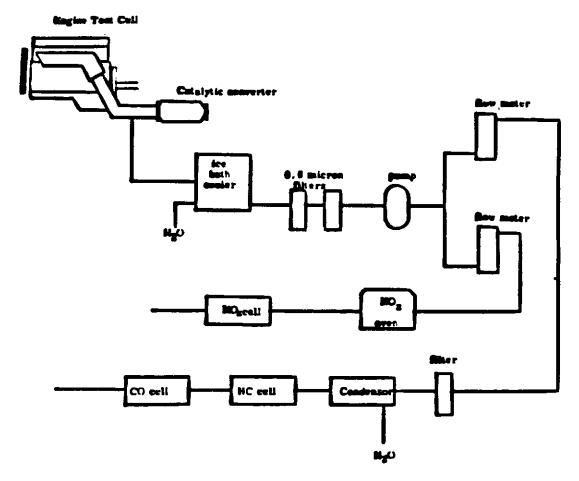
This type of measurement allowed direct comparison of emission being produced from a Volvo engine with a select modification to the production Volvo engine.



Pigure No. 13 Engine Performance Measurement System



Pigure No. 14 Engine Synamometer Fuel Measurement System



Pisure No. 15 Engine Ernenceter Exhaust Paissions Messurement

APPENDIX D
VOLVO B19 LRS.

Brooklyn Air Resources Lab Test Results

Date	Run #	HC	co	CO ₂	NO _x	MPG	Notea
9/18	2871c	. 56	11, 16	437.	. 12	19. 3	As delivered
	2971c	. 37	8. 98	259, 1	. 10	32.0	
9/18	2872c	, 39	9. 27	366, 4	. 01	23. 0	Trans & rear end
·	2 87 2h	. 44	9, 75	251, 4	. 10	32. 8	lube installed
9/19	2873c	. 51	10. 63	375. 3	. 10	22. 3	Run leans r
9/19	2874c	. 53	4. 79	373, 5	. 12	23. 0	Lambda Sond
·	2874h	. 28	6. 17	241.9	. 06	34.8	Problems
	2974h	. 35	8. 43	231. 8	. 14	35.8	Overdrive used
9/29	Englehard	1, 48	11, 50	462, 8	1. 86	18,4	
10/23	2883c	. 48	8, 48	365, 7	1. 05	23. 3	New cat. Engine
·	2883h	, 20	4, 29	214, 2	1. 01	39. 7	ss per Engirhard
	2884c	. 24	3, 69	364.4	. 07	23.7	Remove warm-up
	2884h	. 20	2,56	214.0	. 06	40, 2	regulator/install of
	2885c	, 53	7, 17	364. 5	, 26	23. 3	cat. Fuel meter wi large air meter
10/30	2891c	. 37	4,47	373, 2	. 20	23. 1	•
55,55	2891h	. 20	2,27	222.4	, 04	38. 8	CO high-repeat hot
	2892c	. 24	3, 68	373, 2	. 07	23. 2	•
	2892h	. 16	2, 53	218.6	. 03	39.4	
	2893c	. 22	3, 98	373.4	. 07	23. l	
	2893h	. 14	2, 28	219, 0	. 02	39. 4	
10/31	2894comp	, 57	6, 42	392. 0	. 44	21. 8	Cold start
•	2894i	1, 67	16, 14		1,22	•••	
	2894il	. 19	3, 67	•••	. 05		Average 27.22
	2894ii l	. 45	4, 30		. 58		
	2894c	. 32	3. 97	387. 1	. 30	22. 3	
	2894h	, 17	1.99	221.4	, 12	30 , 1	

VOLVO BIR LRSV Brooklyn Air Resources Lab Test Results Continued

Date	Run #	нС	co	co ₂	NO _x	MPG	Notes
11/20	2902c	. 20	2, 11	394, 0	. 34	22.1	Weighted fuel meter
	2902h	. 13	1, 04	225.9	. 06	38.6	
	2903c	. 5 6	9, 34	384.8	. 49	21, 9	Rich sensor/retard
	2904c	. 51	5, 43	369. 5	. 96	23, 2	Rich sensor no retard
	2905c	. 36	4, 09	382. 9	. 73	22, 5	Good sensor/retard
11/21	2906comp	. 68	3, 56	425. 6	. 32	20, 3	Cold start test/
	29061	2. 39	8, 56		1, 14		raised air meter disc.
	290611	. 15	2.21		. 08		Too lean on start.
	2906ill	. 31	2. 42		. 15	~	Average 25, 83
	2906h	, 09	. 64	225. 8	. 12	38. 7	_
12/18	2910c	. 14	2. 80	370, 5	. 71	23. 4	New Lambda Sond
	2911c	. 24	3, 77	364. 6	, 49	23.7	computer set lower
	2912c	. 12	2, 61	364.8	, 20	23, 8	500mv nom. added
	2913c	. 19	3, 38	364. 4	, 51	23.7	2 oz wgt. fuel meter
	2913h	. 04	. 62	214.0	, 09	40, 8	_
	2914	. 10	2. 99	385. 7	. 07	22.5	#2913 same as 2916
12/19	2915comp	. 47	4.77	396. 5	. 44	21. 8	Set volt richer/800my
	2915i	1. 50	13, 08		1, 44	•••	500mv
	291511	. 13	2.72		, 14		
	2915414	. 33	2.41		. 25		
	2915h	. 08	1, 11	218.0	. 08	40, 0	
	291 6c	. 46	3.84	371.5	. 09	23. 2	Same as 2915/fuel
	2917e	. 12	2.29	377.8	. 31	23. 0	shutoff hookup \$00mv
	2918c	, 10	2.67	365, 6	. 12	23.8	OD in all gears
	2919c	. 12	3. 45	377. 6	. 05	22. 9	No OD 550my 50ms
12/20	2920comp	. 45	5, 22	383.2	. 37	22.3	550 my 10ms
	2920i	1, 53	12.75		1, 33		OD all gears
	2920i1	. 13	3, 69		. 08		
	2920ill	. 25	2.44		. 19		
	2920h	. 07	1, 14	230. 5	. 08	37.8	

VOLVO H 19 Brooklyn Air Resources Lab Test Results Continued

Date	Run	HC	CO	CO ₂	NO _x	MPG	Notes
12/27	SATRA comp	. 27	4, 33		. 36	22, 51	400 - 4 min.
	SATRA ih	. 29	4, 75		. 49	21, 62	
	lih	. 29	4, 46		. 55	22. 35	
	tiih	. 27	4, 34	•	. 46	22. 0 6	
	tvh	. 28	4, 23		. 40	21. 90	
1/10	2921соп р	. 28	1, 78	361, 5	. 55	24.1	Turbo charger
	2 921i	1.14	7.44		. 89		removed
	292111	. 04	. 23		. 26		
	29211il	. 08	. 36		. 83	•••	
	2921h	.06	. 37	225. 8	. 15	38. 8	
1/15	2924c	. 05	. 51	360	. 11	24, 4	Vac. retard
0,00	3925c	. 09	1.19	350, 7	. ii	24, 9	No vac. retard
	2926c	. 05	. 51	366, 1	, 09	24, 0	3250 Inertia wheel
1/16	2927comp	. 28	2.42	367. 8	. 17	23. 8	
	2927i	1. 07	10, 08		. 51	•	
	2927il	. 04	. 38		. 04		
	2927iii	. 08	. 53		. 17		
	2927h	. 06	. 26	222.8	. 04	39. 4	

APPENDIX E--TASK RESULTS:

TASK 1 - Predict performance of an LRSV powered by the engine and an estimate of the maintenance required to preserve the performance levels over 50,000 miles.

A) <u>LRSV engine output</u> (Based on actual dynamometer data)

Engine: B-19 derived Lambda-sond emission

control system

Displacement: 2017 cc

Compression Ratio: 10.4:1

Max Turbo Boost: 4 Psig

Figure 16

<u>RPM</u>	LRS	V Turbo	LRS	SV (N.A.)
	<u>hp</u>	Torque (ftlbs.)	<u>hp</u>	Torque (ftlbs.)
1000	15.0	78.8	15.0	78.8
1500	25.4	88.9	25.4	88.9
2000	35.9	94.3	37.3	98.1
2500	52.0	109.2	49.0	102.9
3000	70.2	122.9	62.3	109.1
3500	86.2	129.3	71.5	107.2
4000	103.3	135.7	81.3	106.7
4500	115.0	134.2	91.9	107.2
5000	122.1	128.2	102.6	107.7

TASK 1 (cont'd)

B) LRSV Preliminary Performance Prediction Determined from following data:

- 1 Engine torque: turbo and normally aspirated from figure 16.
- 2 Maximum engine rpm 5000
- 3 Gear Box Ratio:

lst.	3.53
2nd.	1.45
3rd.	1.24
4th.	0.81
Final Drive	3.34

- 4 Assume transmission efficiency 96%
- 5 Wheel dimension P175/14 tire

Rolling radius 11.5 in.

6 Coefficient of Drag = .42

Frontal Area = 25 ft.²

- 7 Rolling Resistance = 36 lbs.
- 8 Curb weight = 3004 lbs.

Test weight = 3304 lbs.

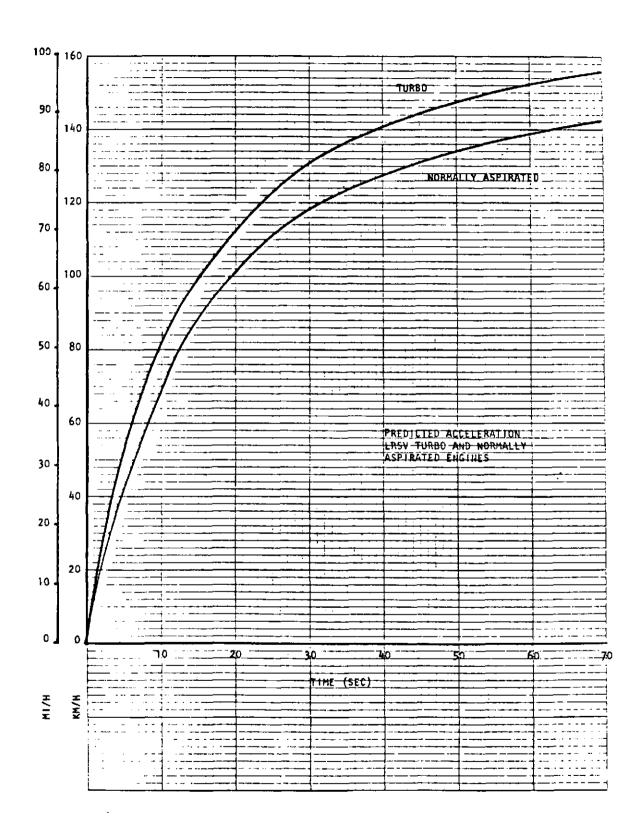
TASK 1 (cont'd)

Figure 17 LRSV Acceleration Prediction

Turbocharged engine:

<u>MPH</u>	TIME (Sec.)	DISTANCE (Ft.)
10	1.20	6.01
20	2.46	36.20
30	4.25	115.73
40	7.50	246.70
50	9.50	417.48
60	13.80	793.74
70	19.75	1280.64
80	28.00	2302.26
90	44.50	5024.16
Normally asp	irated engine:	
10	1.50	11.30
20	3.30	47.52
30	6.00	137.54
40	9.00	300.79
50	12.40	521.57
60	17.75	1003.24
70	25.50	1702.02
80	40.50	3964.56
90		

Figure 18 Predicted Acceleration Curve



TASK 1 (cont'd)

C) LRSV Maintenance Schedule

Replace	Initially (miles)	Interval (miles)
Engine oil and oil filter Oxygen sensor Spark plug	600-1200	3,750 30,000 30,000
Transmission oil	600-1200 600-1200	50, 551
Rear axle oil Air cleaner filter Engine coolant Camshaft belt (if required)	600-1200	30,000 30,000 45,000
Adjust		
Engine drive belts	600-1200 600-1200	
Torque manifold bolts Camshaft drive belt	600-1200	
Oxygen sensor Catalytic converter mounting bolts	600-1200 600-1200	10,000
Inspect		
Cooling system and connection Engine drive belts Valve clearance	600-1200	30,000 30,000 30,000
Vacuum fitting	600-1200	30,000
Idle rpm Fuel system cap, tank, lines and connections	600-1200 600-1200	10,000 30,000

TASK 2 Furnish a description of procedure that will be followed in the tests and the type of test data to be acquired. Fabricate engine according to this procedure.

Test Procedure for LRSV Engine

- 1) a) outfit 1978 244DL with vacuum transducer
 - b) run a 1978 FTP
 - c) determine steady state "modelling tool"
- 2) a) construct B-19 Lambda-Sond engine
 - b) break in (three engines) 30 hours each according to load/engine speed schedule
 - c) baseline engine WOT test B-19 and production B-21
- 3) a) test engine at steady state modelling tool conditions
 - b) record engine parameters for following:
 - 1) synthetic oil
 - 2) reduced accessory drive speed
 - 3) multi-spark capacitive discharge ignition system
 - 4) reduced oil pump pressure
 - 5) reduced crankcase pressure
 - 6) elevated coolant temperature
 - c) determine BSFC's of above modifications
- 4) a) blueprint and balance engine
 - b) break in on dyno
 - c) baseline engine
- 5) a) install turbocharging system from mock-up
 - b) break in, baseline
 - c) WOT test turbo engine
 - d) install boost retard system
 - e) match and install injectors

- 6) a) assemble final engine with selected modifications from above test
 - b) install in 244DL test chassis
- 7) a) test on FTP
 - b) drivetrain modifications
 - c) Lambda-Sond modifications

TASK 3 Engine specifications shall be revised by the findings of TASK 2. Where revisions influence performance, trade off studies shall be conducted to assure that revisions do not unnecessarily compromise performance objectives.

Updated Engine Specifications - None at TASK 3, as actual dynamometer values were utilized for performance predictions, the need to revise the engine specifications are at TASK 3 not necessary. This is evidenced by the satisfactory acceleration data computed during TASK 1, Page 37, Figure 17.

TASK 4 Follow up testing, tests shall be conducted to determine acceleration performance of TASK 3 engine.

Actual Acceleration Times for LRSV - Volvo Chassis

A Data:

- Engine torque: turbo and normally aspirated torque, see Figure 16 Page 35
- 2 Maximum engine speed 5,000
- 3 Gear Box Ratio

lst.	3.17
2nd.	2.16
3rd.	1.37
4th.	1.00
5th.	0.80
Final drive	3.54

- 4 Transmission efficiency 96%
- 5 Wheel dimensions 185/70 SR14 Rolling radius 11.1 in.
- 6 Coefficient of drag = 0.51 Frontal area = 22.6 ft.
- 7 Rolling resistance = 37 lbs.
- 8 Curb weight = 3040 lbs. Test weight = 3340 lbs. (assumed)

Note: 1980 GL acceleration times are provided for comparison.

TASK 4 (cont'd)

Figure 19

Actual acceleration times:

Engine: LRSV-turbo

Chassis: Volvo 1978 244DL

Zero to mph	Time to Speed LRSV-turbo	1980 Volvo GL
20	2.23	2.15
30	3.40	3.56
40	5.09	5.60
50	6.80	8.10
60	9.50	12.03
70	13.00	16.46
80	16.60	24.03
90	22.10	

Note: This data reprinted with permission from Motor Trend Magazine, April 1980, Petersen Publishing Co., Los Angeles, California

TASK 5 The durability of the engine in maintaining the specified emission and fuel economy levels shall be extrapolated to 50,000 miles, using actual data and appropriate engineering data.

Figure 20

Predicted Emission Levels and Fuel Economy at 50,000 Miles

	I nitia	, Initial Level		Predicted Levels 50,000 miles		
	Turbo	Non-turbo	Turbo ¹	Non-turbo ²		
Emission Da	ta:					
НС	0.37	0.19	0.49	0.19		
СО	2.96	2.38	4.80	2.54		
NOx	0.48	0.57	0.56	0.57		
Fuel Economy (Combined):						
MPG	29.65	27.43	30.1	28.04		

1) Based on "deterioration factors" for 1980 GLT Turbo,

Chassis: Volvo LRSV

Transmission: Volvo 5 Sp. Manual

2) Based on "deterioration factors" for 1978 244 DL Lambda-Sond engine, Chassis: LRSV

Transmission: GM X-body 4 Sp. Manual

TASK 6 Zero mile test, final drawing, final maintenance schedule, and raw data collected during dynamometer.

A) Zero mile test:

1976 Federal Urban Driving Cycle conducted at Air Resources Lab, Brooklyn, N.Y., August 2, 1979

Test #3021

Figure 21

	<u>HC</u>	<u>co</u>	<u>co</u> 2	<u>NOx</u>	<u>MPG</u>
Bag 1	1.24	10.08		1.93	
Bag 2	0.13	1.23		0.06	
Bag 3	0.18	0.94	***	0.22	
Composite	0.37	2.96	363.2	0.48	24.0
Highway	0.06	0.32	225.8	0.17	39.1

Inertia weight: 3,000 lbs.

Dyno setting: 10.3 hp @ 50 mph.

Chassis: LRSV-Volvo

- B) Final drawing see separate General Arrangement Drawing
- C) Final maintenance schedule unchanged from preliminary specification, Page 39
- D) Raw data see Appendix F, G

Appendix F. Observed and Calculated Data Recorded During Dynamometer Study

VAC. = in. Hg Torque = lbs.-ft. Temp. = Dry Bulb, ^oF Fuel Flow = lbs./hr.

Test 1: Baseline VAC: WOT

	<u>RPM</u>	TORQUE	FUEL FLOW	TEMP.	<u>Нр</u>	CORRECTED Hp	<u>BSFC</u>
•	1600	82.72	9.10	84	23.62	24.38	0.385
	2000	91.91	14.60	84	35.00	36.12	0.417
	2500	97.68	18.90	85	46.50	48.03	0.406
	3000	100.05	22.80	86	57.15	59.09	0.399
	3500	99.79	28.00	85	66.50	68.69	0.421 0.427
	4000	98.46	32.00	86	75.00	77.55	0.427
	4500	99.79	39.00	87	85.50	88.49	0.505
	5000	99.79	48.00	86	95.00	98.23	0.483
	5 2 00	98.21	47.00	87	97.20	100.64	0.465
	Test 2:	Baseline					
	VAC:	13.0"					
	Baro:	30.27"					
	1600	29.15	4.50	83	8.80	9.21	0.507
	1900	30.46	6.30	83	11.02	11.02	0.572
	2200	28.68	8.40	83	14.19	14.72	0.592
	2500	34.14	8.60	83	16.25	16.86	0.529
	2800	35.45	9.80	84	18.90	19.63	0.519
		D 11					
	Test 3:	Baseline					
_	VAC:	13"					
-	Baro:	30.28					
	1600	31.25	5.00	86	9.52	9.90	0.525
	1900	29.67	6.30	86	10.73	11.16	0.587
•	2200	33.35	8.40	86	13.97	14.52	0.601
	2500	35.19	8.60	86	16.75	17.42	0.513 0.515
	2800	35.71	9.80	86	19.04	19.80	0.515

Multi-Spark Ignition 13" 30.4

Test 4: VAC: Baro:

<u>RPM</u>	TORQUE	FUEL FLOW	TEMP.	<u>Hp</u>	CORRECTED Hp	BSFC
1600 1900 2200 2500 2800	31.25 32.56 35.45 35.19 36.50	4.90 6.10 8.00 8.60 11.20	83 83 84 84	9.52 11.78 14.85 16.75 19.46	9.81 12.23 15.29 17.26 20.06	0.515 0.518 0.539 0.513 0.576
Test 5: VAC: Baro:	Reduced Diam 13" 30.45	neter Crank Pulley	,			
1600 1900 2200 2500 2800	32.03 33.09 35.19 35.98 36.76	5.10 6.80 8.20 8.70 10.50	81 81 80 80	9.76 11.97 14.74 17.12 19.60	10.01 12.28 18.12 17.55 20.09	0.523 0.568 0.556 0.508 0.536
Test 6: VAC: Baro:	Synthetic Lub 13" 30.43"	ricant				
1600 1900 2200 2500 2800	32.03 32.83 35.71 35.97 36.87	5.10 6.80 8.40 8.70 10.80	91 91 91 91 91	9.76 11.87 14.96 17.12 19.65	10.15 12.35 15.55 17.81 20.44	0.523 0.573 0.561 0.508 0.549
Test 7: VAC: Baro:	Elevated Coo 13" 30.80"	lant 210 ⁰ F Temp.				
1600 1900 2200 2500 2800	28.36 29.15 34.14 34.40 35.19	4.70 5.40 6.80 10.20 10.50	82 82 82 82 82	8.64 10.54 14.08 16.37 18.76	8.85 10.79 14.41 16.76 19.21	0.544 0.512 0.438 0.623 0.560

Elevated Coolant 220°F Temp. 13" 30.8

Test 8: VAC: Baro:

<u>RPM</u>	TORQUE	FUEL FLOW	TEMP.	<u>Hp</u>	CORRECTED Hp	BSFC
1600 1900 2200 2500 2800	29.94 29.94 33.09 34.14 35.45	4.20 5.80 7.80 8.60 11.00	83 83 83 83	9.12 10.83 13.86 16.25 18.90	9.34 11.10 14.20 16.65 19.37	0.461 0.536 0.563 0.529 0.582
Test 9: VAC:	Turbocharged					
1600 1900 2200 2500 2800	26.19 29.41 30.99 34.66 37.29	5.30 6.30 7.80 8.50 11.09	 - - -	7.68 10.64 12.98 16.50 19.88	7.77 10.77 13.13 16.70 20.12	0.690 0.592 0.601 0.515 0.558
Test 10: VAC:	Turbocharged WOT (positive	pressure)				
2000 2200 2400 3000 3500 4000	93.49 101.70 105.04 121.85 128.15 134.45	15.59 17.97 19.68 28.81 36.04 25.60	- - - - -	35.60 42.60 48.00 69.60 85.40 102.40	35.92 43.06 48.43 70.22 86.17 103.32	0.435 0.422 0.410 0.414 0.422 0.250
Test 11: VAC:	Blueprinted E 13"	ngine				
1600 1900 2200 2500 2800	21.00 25.72 30.46 32.81 35.19	5.00 6.50 7.90 9.40 11.11	- - - -	6.40 9.31 12.76 15.62 18.76	6.56 9.55 13.09 16.03 19.24	0.781 0.698 0.619 0.602 0.592

Test 12: Blueprinted Engine VAC: WOT

<u>RPM</u>	TORQUE	FUEL FLOW	TEMP.	<u>Hp</u>	CORRECTED HP	BSFC
1500 2000 2500 3000 3500 4000 4500 5000 5200	86.67 95.59 102.41 106.35 104.97 103.99 104.51 105.04 101.10	9.99 14.60 19.80 24.00 28.12 38.42 38.00 44.00 45.04	- - - - - -	24.75 36.40 48.75 60.75 69.95 79.20 89.55 100.00 100.10	25.39 37.34 38.31 62.33 71.46 81.26 91.87 102.60 102.70	0.404 0.401 0.406 0.395 0.402 0.429 0.424 0.440
Test 13: VAC:	13" Hg					
1600 1900 2200 2500 2800	24.94 28.08 31.25 32.56 35.71	6.75 7.00 8.19 9.60 11.25	- - - -	7.60 10.16 13.09 15.50 19.04	7.78 10.40 13.40 15.87 19.49	0.888 0.689 0.626 0.619 0.591
Test 14: VAC:	Blueprinted E WOT	ingine				
1500 2000 2500 3000 3500 4000 4500 5000	87.18 96.37 103.72 105.04 105.56 104.78 103.20 99.79 102.94	10.51 14.68 19.70 22.02 36.02 33.99 38.02 45.03 44.03	- - - - - -	24.90 36.70 49.37 60.00 70.35 79.80 88.42 95.00 101.92	25.49 37.58 50.56 61.44 72.03 81.71 90.54 97.28 104.36	0.422 0.409 0.399 0.367 0.512 0.426 0.430 0.474 0.432

Test 15: Blueprinted Engine VAC: 13"

	<u>RPM</u>	TORQUE	FUEL FLOW	TEMP.	<u>Hp</u>	CORRECTED Hp	BSFC
	1600 1900	19.95 24.93	4.90 6.59	-	6.08 9.02	6.28 9.32	0.806 0.731
,	2200	29.41	8.30	-	12.32	12.72	0.674
	2500	32.46	9.30	•	15.45	15.96	0.602
	2800	35.19	11.34	-	18.76	19.38	0.605
	Test 16:	Blueprinted E	ingine				
	VAC:	WOT					
	1500	86.38	11.20	_	24.67	25.48	0.454
	2000	96.11	15.48	_	36.60	37.80	0.423
	2500	102.14	19.59	-	48.62	50.23	0.403
	3000	103.99	22.99	-	59.40	61.36	0.387
	3500	103.99	28.00	_	69.30	71.58	0.404
	4000	104.51	32.00	-	79.60	82.83	0.402
	4500	103.46	38.03	_	88.65	91.57	0.429
	5000	102.41	43.00	_	97.50	100.71	0.441
	5200	100.05	45.96	_	99.06	102.32	0.464

Appendix G Steady State Emission Data Recorded During Dynamometer Study

VAC 13" Hg

Test 1: Baseline Before Catalytic Converter

<u>RPM</u>	<u>% CO</u>	PPM/HC	PPM/NOx
1600 1900 2200 2500 2800	1.10 1.10 0.98 1.00 0.90	1.55 1.30 1.39 1.35 1.18	300 400 840 1020 1220
Test 2:	Baseline After Catalytic C	Converter	
1600 1900 2200 2500 2800	0.90 0.20 0.17 0.15 0.13	1.30 0.63 0.65 0.62 0.61	75 65 80 80 20
Test 3:	Reduced Diameter Cranks	haft Pulley Before Catalytic	Converter
1600 1900 2200 2500 2800	2.13 1.60 1.30 1.05 0.90	1.53 1.10 1.10 1.00 0.80	320 520 840 1160 1400
Test 4:	Elevated Coolant Temp	210 ⁰ F Before Catalytic Conv	/erter
1600 1900 2200	0.72 0.70	0.8 <i>5</i> 0.60	380 560

Test 5: Elevated Coolant Temp. - 220°F Before Catalytic Converter

RPM	% CO	PPM/HC	PPM/NOx
1600	1.23	1.15	430
1900	0.80	0.75	460
2200	0.65	0.79	940
2500	0.73	0.72	1240
2800	0.79	0.65	1380
Test 6:	Multi-Spark Ignition System	n Before Catalytic Convert	er
1600	2,23	1.80	320
1900	1.85	1.50	500
2200	1.70	1.55	740
2500	1.40	1.40	1020
2800	1.27	1.29	1300

APPENDIX C

BENDIX AUTOMOTIVE CONTROL SYSTEMS GROUP FINAL REP	ORT
BENDIX ADAPTIVE BRAKING SYSTEM INSTALLATIONS ON MINICARS' RESEARCH SAFETY VEHICLE	C-1
and	
ADAPTIVE BRAKING SYSTEM FOR MINICARS' HIGH TECHNOLOGY RESEARCH SAFETY VEHICLE: DESCRIPTION AND OPERATING INSTRUCTIONS	C-21

Final Test Report

Bendix Adaptive Braking System Installations on

Minicars' Research Safety Vehicles

March 1980

Final Test Report

Bendix Adaptive Braking System
Installations on
Minicars' Research Safety Vehicles

SUMMARY

This report summarizes test activities associated with the installation of four-wheel adaptive braking system (ABS) on Minicars' Ride and Handling Test Bed and High Technology Research Safety Vehicle (RSV). A recurring problem associated with insufficient front brake pressure consumed an inordinate amount of activity. However, this problem did not prevent the acquisition of substantial data and satisfactory demonstration of major test objectives.

Briefly, the Ride and Handling Test Bed was initially tested to a portion of MVSS-105 procedures; then, the ABS was installed and system function verified on a number of test surfaces. The system was then transferred to the High Technology RSV which was fitted with new Dunlop run-flat tire / wheel assemblies. Pre-and-post burnish effectiveness data was obtained. System function was verified and demonstrated via an eight-to-ten minute color movie. The balance of this report will discuss testing, results, and related events in more detail. Appendix "A" discusses the brake pressure problem.

DISCUSSION

Ride and Handling Test Bed

Prior to any vehicle testing, the four Chapman / McPherson strut assemblies were replaced with Minicars' supplied items to accommodate a higher GVW. The vehicle front and rear axles were realigned by a local chassis specialist. New brake pads (procured from local Fiat dealer) were installed with thermocouples per SAE J-46. The vehicle was equipped with a fifth wheel and instrumentation to monitor rear brake pressure, pedal effort, and vehicle deceleration.

The vehicle was loaded to GVW and MVSS-105 test procedures were followed through the second effectiveness portion. Figures 1 and 2 show results of these tests. As requested, a measurement of vehicle deceleration versus brake pressure was then conducted. Figure 3 shows the results.

DISCUSSION

(Continued)

Ride and Handling Test Bed (Continued)

The four-wheel adaptive braking system was then installed. In preparation for initial system tests, difficulties were experienced in obtaining sufficiently high front brake pressure to assure wheel lock prior to primary master cylinder runout. Many different solutions were attempted with only fair success. Appendix "A" (attached) will provide more details on these efforts.

In order to demonstrate ABS performance, all ballast was removed from the vehicle to reduce high brake pressure requirements. The vehicle was then tested periodically over a six week period at curb weight, plus two occupants, plus approximately 100 pounds of instrumentation.

In a typical test sequence, several alternate system ON and system OFF stops are made under the same test surface / speed condition. SAE J-46 procedures were used including rapid brake application to a high level of effort. Initial speed (0.1 ft./sec. resolution) and stopping distance (0.1 ft. resolution) were recorded. The data was reduced by correcting stopping distance for minor initial speed variations, and then averaging the groups of system ON and system OFF stops. Figure 4 summarizes the results of these ABS performance measurements. Please note the test surfaces changed over the time period due to wear, climate, and, in some cases, resurfacing; thus, no attempt should be made to dwell on absolute distances. In fact, it is for this type of reason that J-46 seeks to compare the system equipped vehicle only with itself in a locked wheel stop at the same surface / speed condition.

High Technology RSV

With satisfactory system function demonstrable on the Ride and Handling Test Bed, transfer to the High Technology RSV was accomplished. The vehicle was also equipped with new brake pads and thermocouples, instrumentation, and weighed with the following results:

	Weight (Lbs.)	
	Front	Rear
Left	576	765
Right	560	760
Totals	1,136	1,525

2,661

High Technology (RSV) (Continued)

Pre-burnish effectiveness was measured at 30 and 60 mph (two occupants) and the results are plotted in Figures 5 and 6. The vehicle was then subjected to the 200 stop burnish schedule of SAE J-46 and 30 and 60 mph brake effectiveness again measured. See Figures 7 and 8.

A short movie was made of the High Technology RSV on a variety of surfaces. The movie sought to visually demonstrate the ABS contribution to vehicle performance, much like SAE J-46, by comparing vehicle behavior with and without the system in operation.

Attachments

Figure 1 Ride and Handling Test Bed MVSS-105 Test Results

Conditions:

- Fuel tank 75 100% full. Tire inflation pressure correct. Weight: Front Axle 1,440 Lbs. Rear Axle 1,782 Lbs.

First Effectiveness - 30 MPH

Stop Number	Maximum Line Pressure (psi)	(1) Corrected Distance <u>(Ft.)</u>	Maximum Pedal Effort (Lbs.)
1	1,470	41.7	128
2	1,510	41.0	137
3	1,550	40.7	142
4	1,440	42.1	139
5	1,500	40.1	137
6	1,470	42.7	135
	(1) Corrected dist	tance, $D_c = D_A \left(\begin{array}{c} V_0 \\ V_b \end{array} \right)^2$	}

{ VA 2 }

 D_A = actual distance, feet. Where:

V_A = actual velocity, feet/second.

V = desired velocity, feet/second.

First Effectiveness - 60 MPH

Stop Number	Maximum Line Pressure (psi)	Corrected Distance (Ft.)	Maximum Pedal Effort (Lbs.)
1	1,400	184.9	128
2	1,500	171.5	131
3	1,300	176.4	125
4	1,460	182.4	128
5	1,470	176.0	128
6	1,490	183.6	125

FIGURE 2
Ride and Handling Test Bed
MVSS-105 Test Results

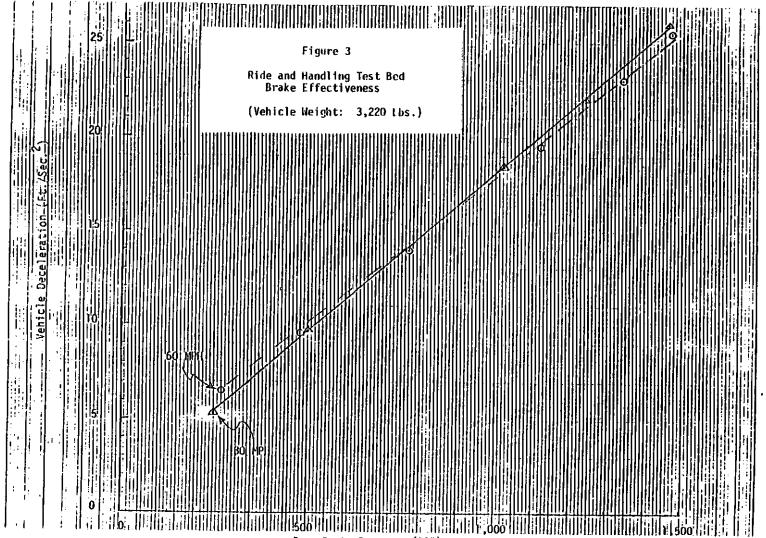
Second Effectiveness - 30 MPH

Stop <u>Number</u>	Maximum Line Pressure (psi)	Corrected Distance (Ft.)	Maximum Pedal Effort (Lbs.)
1	1,550	44 6	133
2	1,580	41.5	136
3	1,600	40.6	142
4 *			
5	1,500	46.3	135
6	1,525	44.6	140

Both front wheels slide, midway.

Second Effectiveness - 60 MPH

Stop Number	Maximum Line Pressure (psi)	Corrected Distance (Ft.)	Maximum Pedal Effort (Lbs.)
1	1,560	176.0	133
2	1,650	170.1	145
3	1,600	174.9	132
4	1,510	175.5	115
5	1,530	181.3	107
6	1,550	179.5	102



Rear Brake Pressure (PSI)

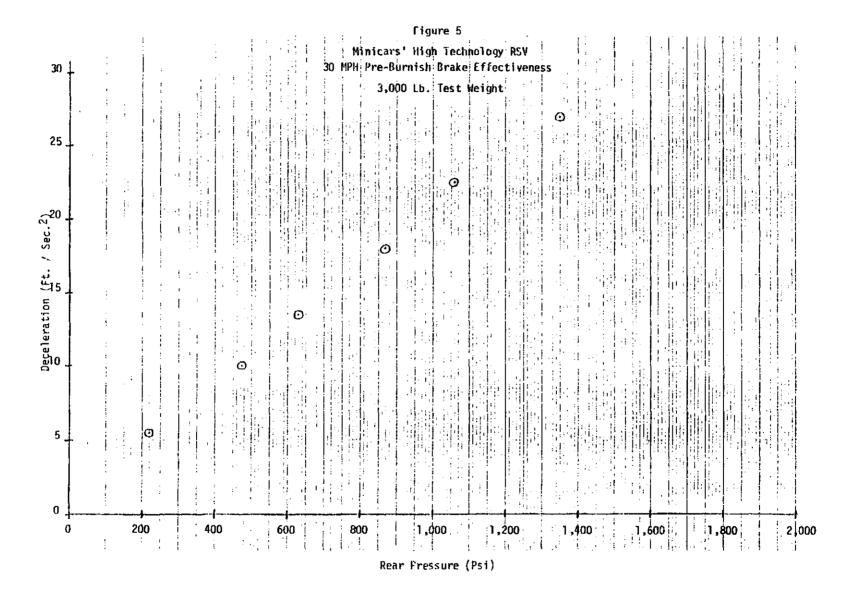
Figure 4

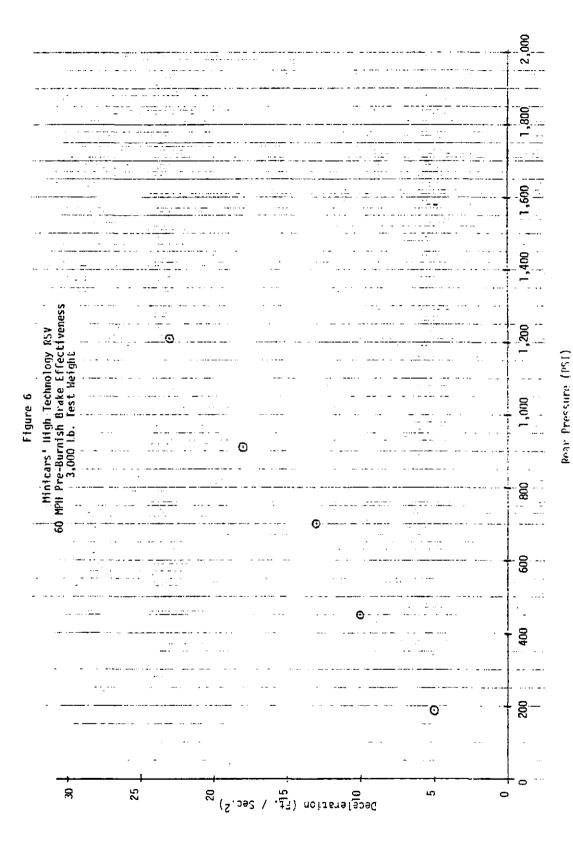
Ride and Handling Test Bed
ABS Performance Summary

Surface (Skid Number Range)	Speed (MPH)	Corrected Stop System ON (Ft.)	pping Distance System OFF (Ft.)	Improvement (Percent)
Wet X-10 (18 - 35)	30	76.1	92.6	+18.0
(10 - 35)	30 30 30	76.8 75.3 117.8	90.6 90.6 1 158.7	+15.2 +16.9 +25.8
Wet Jennite (28 - 48)	30	73.5	90.0	+15.3
	30	68.3	85.6	+20.2
	40	137.9	177.9	+22.6
	45	118.7	150.6	+21.2
Wet Asphalt (55 - 65)	30	52.0	 49.4 	- 5.3
Dry Asphalt ⁽²⁾ (70 - 85)	30	41.0	 	- 6.5
	60	159.9	1 156.0 	- 2.1

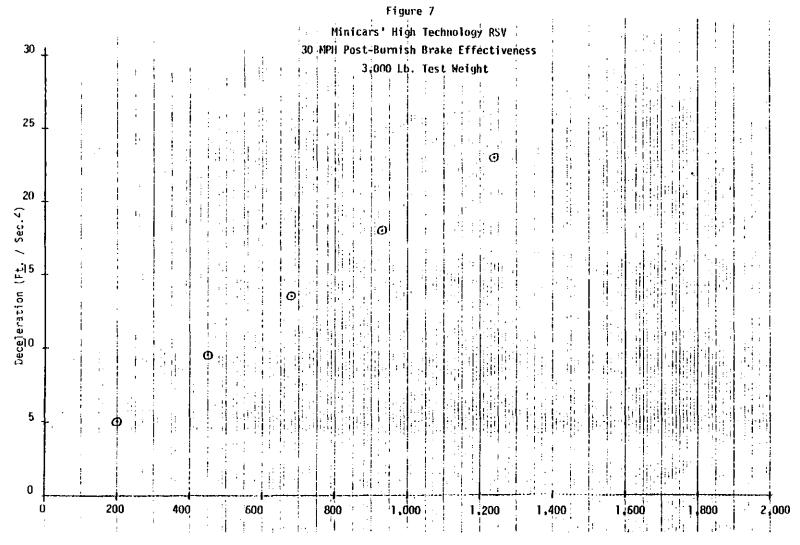
^{1.} Percent improvement of system ON over system OFF.

^{2.} Locking of both front wheels sometimes erratic.



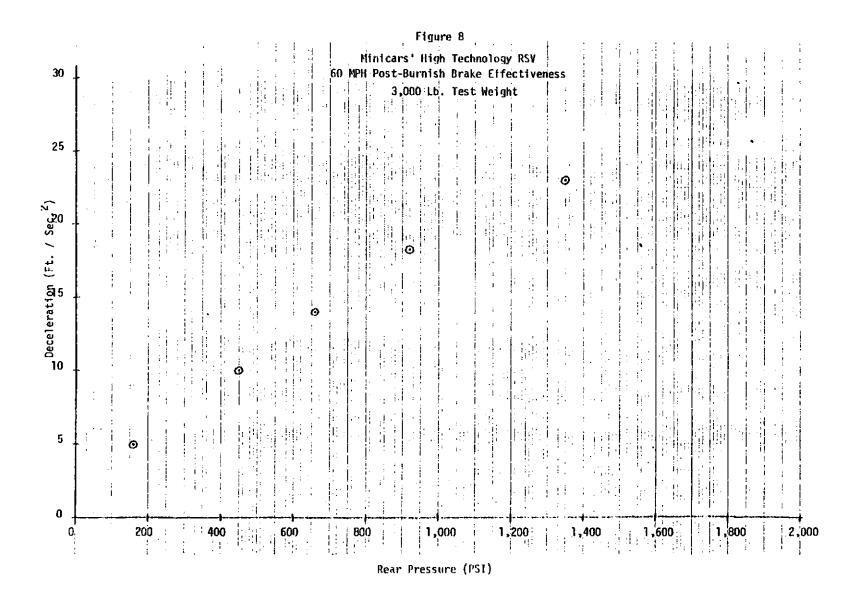


C-11



Rear Pressure (PSI)

· ·



Appendix A

High Brake Pressure Limitation

SUMMARY

The ability to develop a given level of brake pressure in the foundation brake system for a given pedal stroke diminished in both vehicles. Thus, for full pedal stroke, peak brake pressure available diminished. No conclusive reason was identified although some attempted changes were helpful in mitigating the problem. This Appendix summarizes activities associated with this phenomena.

DISCUSSION

Figures A-1 and A-2 illustrate the changes observed in the stroke / pressure relationship. Figure A-1 demonstrates the relationship of travel and pressure versus pedal effort before any test activity had been conducted on the High Technology RSV. Note that with a pedal travel of four inches, both front and rear pressures in excess of 2,000 psi were demonstrable. Figure A-2 represents data from the same vehicle at a later time. Note here that pedal travel of almost five inches provides pressures of 1,500 psi or less. This reduced maximum pressure produced two effects:

- A. On high coefficients, sufficient torque to quickly lock the front wheels was marginal; thus, a meaningful comparison of OFF versus ON stopping distances was difficult.
- B. With the pedal fully stroked, the primary master cylinder piston (front axle) was also fully stroked. In ABS operation, desired pressure balance in the front regulator was uncertain since even minute motion of the regulator piston could have a substantial effect on front master cylinder pressure in the full stroked situation.

Examination of Figures A-1 and A-2 reveal a difference which suggested an insight into cause of the phenomena. Note on Figure A-1, the initial knee of the pedal stroke application curve occurs at around 0.9" of stroke with an application force of around 12 pounds. By contrast, Figure A-2 shows that 12 pounds of force results in approximately two inches of pedal travel. Thus, this "loss" of an inch of stroke is thought to be a direct casual factor of the diminished high pressure capability.

Although the bulk of activity investigating this phenomena was directed at the Ride and Handling Test Bed, both vehicles demonstrated quite similar behavior; therefore, it is concluded that differences between the two vehicles were insignificant. (This dispells the earlier hypothesis that the pressure differential switch, which was only present on the Ride and Handling Test Bed, was a major contributor.)

Presence of ABS was widely examined as a factor on the Ride and Handling Test Bed even though the same system had been installed on several earlier vehicles without incident. However, this hypothesis was ruled out when the phenomena continued to manifest itself on the Ride and Handling Test Bed after the vehicle was returned to standard in preparation for return.

Speculations on the principle cause and subsequent investigations can be grouped broadly into two categories: air in the brake system and some added source of hydraulic compliance.

Air

Various bleeding techniques were utilized on many different occasions including those suggested by the local Fiat Service Manager and those used by Minicars during vehicle assembly. None of these techniques proved superior. In all cases, pumping the brakes rapidly produced higher peak pressure. The following summarizes these techniques:

Standard Pressure Bleeding - This technique is widely used by Bendix test vehicle support personnel and with only minor variations was suggested by both Minicars and the local Fiat representative. A source of brake fluid, under pressure of 30 - 50 psi, is connected to the master cylinder remote reservoir or to the reservoir lines. A transparent tube is attached to the individual caliper bleed screws; the screw is turned and flow out of the caliper is continued until the flow is free of bubbles or foam. An alternative was used on many occasions where, during the time that flow was under way, the pedal was exercised to promote higher flow rates, intended to dislodge air in the lines which might be stationary due to high surface adhesion.

Reverse Pressure Bleeding - In this technique, flow through the brake system is reversed by connecting the brake fluid pressure source to the caliper bleed screw port and monitoring flow out of the reservoir lines.

<u>Vacuum Bleeding</u> - In this technique, a vacuum pump capable of producing approximately 29 In. Hg. is connected to the master cylinder reservoir. After the brake system is thoroughly evacuated, reservoir pressure is returned toward atmospheric. By intent, air removed during evacuation is replaced by fluid from the reservoir.

Manual Bleeding - Mild pressure is applied to the pedal and maintained while the caliper bleed screw is opened and closed. The pedal is then released allowing the master cylinder to be recharged with fluid from the reservoir. The process is continued until the flow out of the bleed screw port is free of bubbles or foam.

Service Bleeding - This technique from the Fiat X-1/9 Service Manual is a variation of manual bleeding. A transparent hose is attached to the bleed screw and the other end is immersed in clean brake fluid. After the bleed screw is opened, the brake pedal is rapidly depressed, then allowed to return slowly. This process is continued until bubble and foam-free fluid is obrained; then, while the pedal is depressed, the bleed screw is tightened.

Other - The master cylinder has two outlet ports in the primary bore, which normally are connected to individual front brake lines. Because only one line was necessary from the master cylinder to the front regulator / modulators assembly, one of the primary ports was plugged. During activities directed at the High Technology RSV, the master cylinder was removed and the two primary outlet ports were plumbed together. The master cylinder was bled in the laboratory and reinstalled. This change made no detectable difference in high pressure capability.

As installed, the master cylinder bore axis is not horizontal; the outlet ports are higher than the reservoir ports. To test the hypothesis that air could be trapped in the top of the master cylinder bore, the front of the High Technology RSV was raised to reverse the inclination of the bore axis with the horizontal. The brake pedal was actuated repeatedly in an effort to flow any air trapped in the master cylinder back into the reservoir. No benefits were detected from this exercise.

Additional Hydraulic Compliance

This hypothesis came into being because of the apparent diminishment of high pressure capability after the vehicles had been exercised and was strengthened when bypassing of the ABS showed no improvement in pressure capability.

Master Cylinder Replacement - From vehicle instrumentation, it was sometimes observed that the master cylinder front piston would reach a limiting pressure before the pedal had full stroked. This situation allowed rear master cylinder pressure to continue to increase with stroke. This phenomena was not visible during the initial testing (MVSS-105) of the Ride and Handling Test Bed since only rear pressure was monitored. Thus, it was hypothesized that an anomoly might exist with the primary piston seal and / or compensating arrangement. Disassembly of the master cylinder did not reveal any problems. A new master cylinder was procured and installed with no benefits detectable.

<u>Pedal Linkage Hinge Pin</u> - After noting that the hinge pin was made of Delrin tubing, it was hypothesized that high stresses had caused it to yield. A new solid pin was fabricated from aluminum. However, no improvements were noted after installation on the High Technology RSV.

Caliper Mounting Influence - Since the calipers had been removed during speed sensor installation, it was suggested that they had been remounted in a fashion that caused the pads to not be parallel with the contact surface of the new rotors. The calipers were removed from the High Technology RSV hub assemblies and pie shaped sections of a spare rotor were inserted between the pads. However, no change in high pressure capability was observed.

Front Brake Hoses - Under pressure, a slight swelling of the front brake hoses was observed. New hoses were provided by Minicars. However, after installation, no significant improvement was detected.

Master Cylinder Modification - The Fiat X-1/9 brake system includes 48mm front calipers and 34mm rear calipers, meaning that the fronts require essentially twice the fluid displacement as the rears for a given amount of piston travel. The X-1/9 master cylinder has a 50 / 50 split, i.e., front and rear sections displace the same amount of fluid, which is measured as 0.186 cubic inches on the original master cylinder from the Ride and Handling Test Bed. Data from another program indicated that a pair of 48mm calipers would require 0.223 cubic inches at 2,000 psi. As an experiment, the primary piston stroke on the Ride and Handling Test Bed was increased by cutting .122 inches off the piston snout. Thic change provided an increase in maximum pressure on the front axle sufficient to reliably lock the front wheels. However, this change was not pursued on the High Technology RSV because of MVSS-105 split system implications.

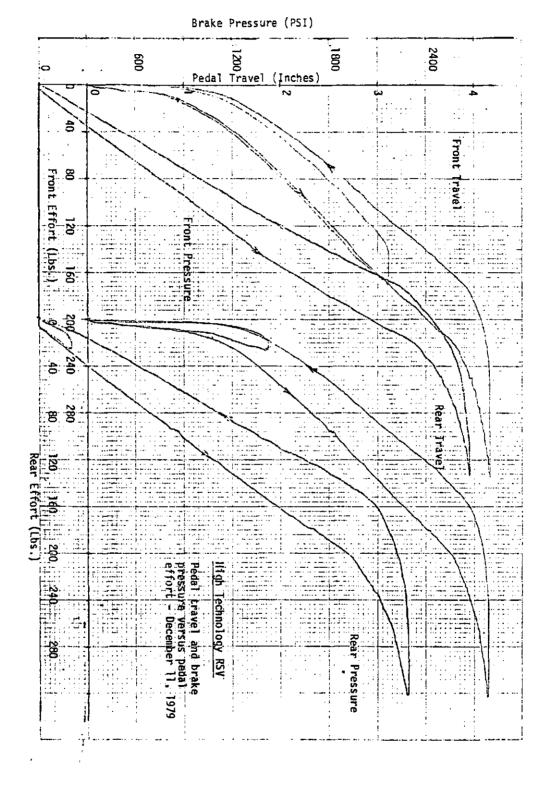


Figure A-1

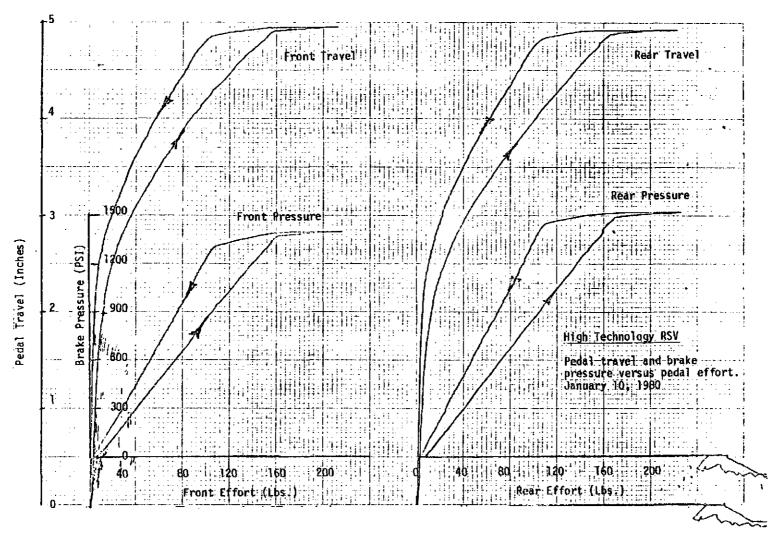


Figure A-2

•

Adaptive Braking System

for

MINICARS HIGH TECHNOLOGY RESEARCH SAFETY VEHICLE

Description

and

Operating Instructions

March, 1980

INTRODUCTION

- This booklet provides operating instructions and describes the four-wheel Adaptive Braking System (ABS) installed in Minicars' High Technology Research Safety Vehicle, DOT License Number 80141. The system is quite similar to other systems installed by Bendix Automotive Control Systems Group (ACSG) in an earlier feasibility program for commercial application, and is also similar to the system utilized in another RSV application.
- Briefly, the system consists of wheel speed sensors in each wheel, an electronic control unit, a brake pressure modulator for each front wheel and the rear axle, and a hydraulic power supply which consists of an electric motor driven brake fluid pump and two brake fluid accumulators. Except for the speed sensors, Figure 1, all components are mounted on a common bracket in the right rear corner of the trunk, Figure 2.

The system has no effect on routine braking and requires no participative action by the operator. However, because of the prototype nature of this system and, as well, to allow vehicle evaluation without the system, an ON / OFF switch has been provided. In the OFF position, electrical power to the system pump and solenoid valves is denied by a specially installed relay. When the switch is in the ON position, it is internally illuminated while the ignition key is ON. With the system switch in the ON position and with a brake light signal present, the system continuously monitors for imminent wheel lock. Should this be detected, brake pressure to the affected wheel(s) is decreased and reapplied in order to maximize braking performance and avoidance of wheel lockup at all speeds above approximately five miles per hour. Avoidance of wheel lockup allows for significant vehicle steerability and stability characteristics not otherwise possible.

A red warning light on the instrument panel is connected to the system. This light will illuminate (with the ignition key ON) should the system detect any of several undesirable conditions or if the system switch is in the OFF position. When the warning light is illuminated, the system is inoperable.

- Since the system does not require any servicing or periodic maintance, no special tools or equipment are necessary for support.
- The remaining sections of this booklet will describe the system components and function in greater detail.

General

The four-wheel Adaptive Braking System (ABS) is designed to prevent any wheel from locking due to excessive brake pressure above a speed of approximately five miles per hour. The system reduces the skid potential of a locked wheel but still maintains brake pressure for maximum stopping effort available with the existing tire / road condition. The end result is to improve the directional control and steerability of the vehicle and, in many cases, to reduce the distance required to bring the vehicle to a stop.

The major components of the ABS are:

- 1. A speed sensor at each front and rear wheel.
- 2. An electronic control unit (ECU) located inside the trunk right side adjacent to the fuse panel.
- 3. An electric motor driven brake fluid pump located in the trunk below the ECU.
- 4. Two accumulators which are located on the forward side of the ABS mounting bracket inside the right side of the trunk, along the firewall.
- 5. Two regulators which are attached to the modulators inside the right rear of the vehicle trunk.
- 6. Three pressure modulators mounted inside the right rear of the vehicle trunk. They are attached to the aft side of the ABS mounting bracket.

Figure 3 illustrates the basic plumbing arrangement of the ABS components.

Speed Sensors

Each wheel speed sensor consists of a variable reluctance pickup placed in close proximity to a rotating toothed wheel. The pickup includes a permanent magnet and coil in a case which is attached to the mounting bracket. In this installation, the toothed wheel is formed by teeth cut on the outside diameter of the brake rotor. Clearance between the pickup and toothed wheel is adjustable and is nominally set for .020-inch air gap.

Electronic Control Unit

The electronic control unit (ECU) is essentially a small computer and contains various electronic components. The unit is encased in a container and includes the necessary cables and connectors. Electronically, the ECU contains three channels, one for each of the three pressure modulators, as well as failure detection logic.

Wiring System

The wiring system consists of one major wiring harness plus the leads from the speed sensors and the pressure modulators. Figure 4 shows a schematic of the harness and the other electrical leads that make up the wiring system.

Brake Fluid Pump

This assembly is an electric motor driven single piston pump. The motor is activated by the pump relay. The pump relay coil is powered by ignition voltage; coil current flows when the pump switch provides a ground (low pressure). The pump accepts fluid from the master cylinder reservoir and provides brake fluid under pressure to the two system accumulators. The accumulators are maintained at about 1,700 psi by the pressure sensitive pump switch which turns the pump motor ON and OFF via the pump relay.

Accumulators

The two accumulators are spring loaded devices which store pump output fluid under pressure for replenishment of caliper fluid during ABS function. One accumulator is provided for each half of the brake system to preserve the hydraulically split brake system. The accumulators have a check valve at their pump inlets and a filter is provided at their output to the regulators. Also, internal to the accumulators is a relief valve which vents the accumulator to master cylinder reservoir, should the internal pressure exceed approximately 2,700 psi. Attached to the top of the accumulators are low pressure switches which provide an electrical signal (ground) to the ECU when stored pressure is greater than 1,000 psi. This signal is used for failsafe purposes described later.

Regulators

The regulators receive fluid from the accumulators and provide the modulators with a fluid pressure source equivalent to master cylinder pressure for use during ABS cycling. There are two regulators, a front and a rear, to maintain the brake system split.

Pressure Modulators

The system includes three pressure modulators. There is a pressure modulator for each front brake and one pressure modulator for the two rear brakes.

The hydraulic brake tubes are routed as follows: (See Figure 3.)

- a. <u>Front Wheels</u> From the master cylinder primary outlet port to both front brake modulators; from each modulator to an individual front disc brake caliper.
- b. Rear Wheels From the master cylinder secondary outlet port to the rear brake modulator; from the modulator to the disc brake calipers of both rear brakes.

Pressure Modulators (Continued)

The pressure modulators are simply an assembly of two two-way electrically operated solenoids and two flow rate control orifices. The two valves are called "isolation" and "decay" and function as follows: (Refer to Figure 5.)

Isolation Valve - As the name implies, this valve can, when energized, isolate the master cylinder from communicating with the wheel caliper. Normally, the valve is de-energized and master cylinder pressure comes in and passes the open ball seat and passes on to the decay valve. The regulator supply pressure is sealed off by the closed ball seat of this valve.

Decay Valve - Again, as the name implies, this valve can, when energized, allow wheel caliper fluid to bleed to reservoir, decreasing caliper fluid pressure. Normally, the valve is de-energized and master cylinder pressure comes in the top center of the valve seat, passes the open ball seat, and out to the caliper.

The two orifices, build and decay, control the flow rate of the brake fluid during pressure build and decay. Their function will be described in the ABS Function section of this document.

Speed sensor layout drawings, AEXD-10540 and 10541, were provided earlier. Remaining major packaging drawings are attached.

Warning
System
(Continued)

If the ABS OFF / ON switch is illuminated and the ABS failure lamp is illuminated, then a failure is being detected by the ECU. The conditions under which the ECU will cause the ABS failure lamp to illuminate are as follows:

- No low I (e.g. fuse blown) five millisecond delay non-latching.*
- Low pressure switch open (e.g. low accumulator pressure) -35 millisecond delay - non-latching.
- Any isolation or decay valve continuously energized (e.g. solenoid driver transistor shorted) - 6.8 seconds delay - latching.** Fail only if no brake signal present.
- 4. Any isolation or decay valve or its conductive path to the ECU open (e.g. connector unplugged) 6.8 second delay latching.** Fail only if no brake signal present.
- 5. Any processed speed sensor signal 15 MPH less than other speed sensor signals (e.g. connector unplugged) - differential must exist for 7.0 seconds - latching.** Fail only if no brake signal present.
- Non-latching: ABS warning lamp lit only for duration of failure.
- ** <u>Latching</u>: If failure is detected, ABS warning lamp is lit continuously until ignition switch is turned off.

Ignition OFF

With the ignition switch in the OFF position, the system relay is de-energized and, therefore, no voltage is supplied to the motor / pump or to the ECU for powering solenoids. If the brakes are applied, master cylinder pressure is applied to the calipers as shown in Figure 5, passed the two normally open ports of the solenoid valves.

Ignition ON

When the ignition is turned ON and the system OFF / ON switch is in the ON position, the system relay is energized providing voltage to the ECU for solenoid power and to the motor / pump. If the vehicle has been sitting for any length of time, the accumulators may have lost some fluid charge; therefore, the ABS warning lamp may be lit, due to low pressure, and the motor will run to charge the accumulators. Within approximately ten seconds, the pump motor will normally have recharged the accumulators, causing the ABS warning lamp to extinguish.

Engine Running - Vehicle Stationary

The speed sensors do not generate any signals while the vehicle is stationary. In the absence of speed signals, the ECU does not send any commands to the pressure modulators.

If the brake pedal is depressed, master cylinder pressure is applied to the calipers as shown in Figure 5, passed the two normally open solenoid valve ports in each modulator.

Engine Running -Vehicle in Motion

When the vehicle is in motion, an alternating voltage (AC) is generated at each speed sensor and is sent to the ECU. The frequency of the AC voltage is directly proportional to the speed of the wheel.

The ECU converts the signals received from the speed sensors to a DC voltage which is proportional to wheel speed. If the brakes are not applied, or if they are applied lightly, the ECU sends no commands to the pressure modulators.

Engine Running - Vehicle in Motion (Continued)

When the brakes are applied with greater force, the ECU, based on the signals received from the speed sensors, determines the rate at which each wheel is decelerating. If the rate of deceleration is great enough to produce excess wheel slippage or wheel lockup and a brake light signal is present, the ECU sends commands to the pressure modulator of the slipping wheel(s).

The command from the ECU initially performs two functions at the pressure modulators: (Refer to Figure 6.)

- 1. It energizes the isolation valve. This shuts off the fluid communication path from the master cylinder to wheel caliper.
- 2. It energizes the decay valve. This provides a path for now trapped wheel caliper fluid to flow to master cylinder reservoir. The rate of pressure drop is controlled by the decay orifice.

As the caliper pressure decreases, and brake torque consequently reduces, the wheel speed stops decreasing and starts to increase back toward vehicle speed. The ECU, which is continuously monitoring wheel speeds, detects the increase in wheel speed. At the appropriate time, the ECU de-energizes the decay valve. The isolation valve is maintained in an energized condition for a predetermined fixed period of time. This action results in the following:

- 1. <u>Isolation Valve Energized</u> Communication is denied to master cylinder. However, a path is now provided across the lower isolation valve seat to regulator supply. Regulator fluid is supplied from the accumulator at master cylinder pressure.
- 2. Decay Valve De-energized Regulator supply is now communicated to the wheel caliper (see Figure 7). The rate of flow from the regulator supply, and therefore the rate of pressure increase at the caliper, is controlled by the build orifice.

Engine Running Vehicle in Motion
(Continued)

This controlled resupply of brake fluid to the caliper increases hydraulic pressure to reapply the brakes at a controlled rate.

The cycle described above is repeated during a hard brake application until the vehicle has stopped or the driver reduces force on the brake pedal below a level which will cause wheel(s) lock. Pressure decay may not occur below five miles per hour due to wheel speed signal resolution.

Under some conditions, the ECU timed isolation valve command, which is set by a decay command, may expire causing the isolation valve to de-energize. If this happens, the driver may notice a slight drop in the brake pedal as the master cylinder is again able to provide fluid to the caliper.

After the ABS stop, when the isolation valve timer in the ECU times out, the isolation valve will de-energize. When this happens, the brake pedal may drop slightly as noted above.

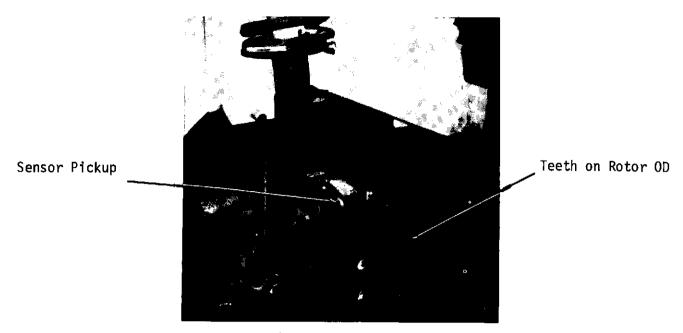
If either accumulator pressure drops below approximately 1,500 psi during ABS cycling, the pump switch will detect this event and provide a ground to the pump relay, causing the electric motor to start and continue to run until the low accumulator is replenished.

Warning System

The ABS includes a warning sub-system to warn the driver of certain types of failures or undesired conditions in the system. The warning system illuminates the ABS warning lamp to warn the driver that an anomaly exists and inhibits system cycling for the duration of the warning.

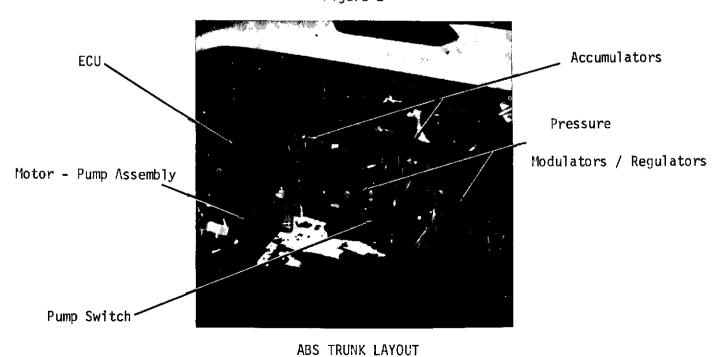
Note that on the wiring diagram, Figure 4, there is an ABS OFF / ON switch. When the switch is ON, the switch's internal lamp is illuminated and the ABS is active. When the switch is OFF, the switch's internal lamp is extinguished and the ABS warning lamp is illuminated. Also when the switch is OFF, the system relay is de-energized, which denies power to the electric motor driven pump and all power required to energize solenoid valves in the pressure modulators (Hi I conductor).

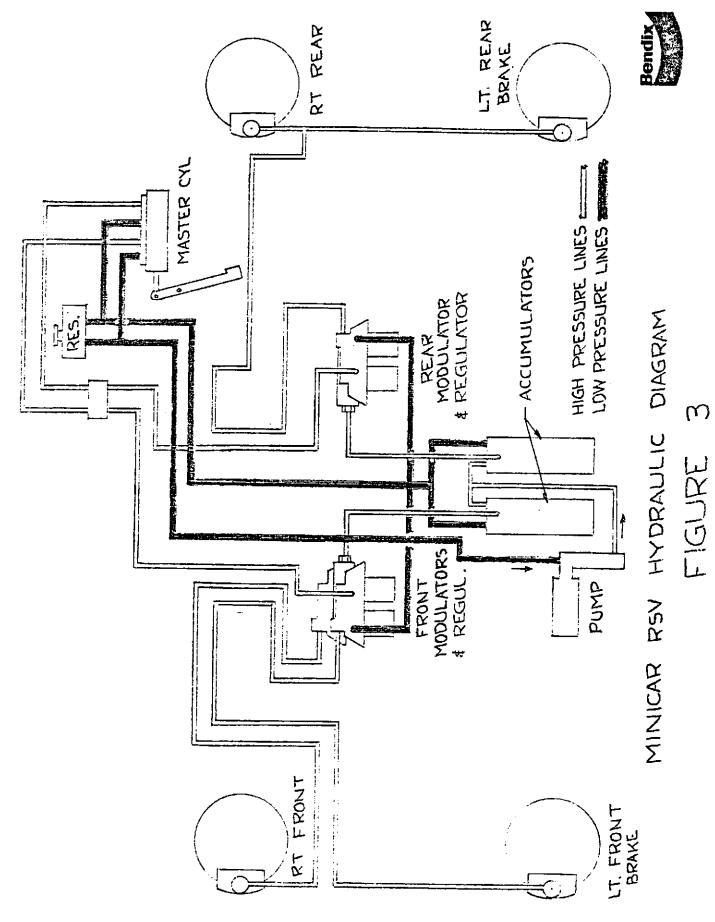
Figure 1

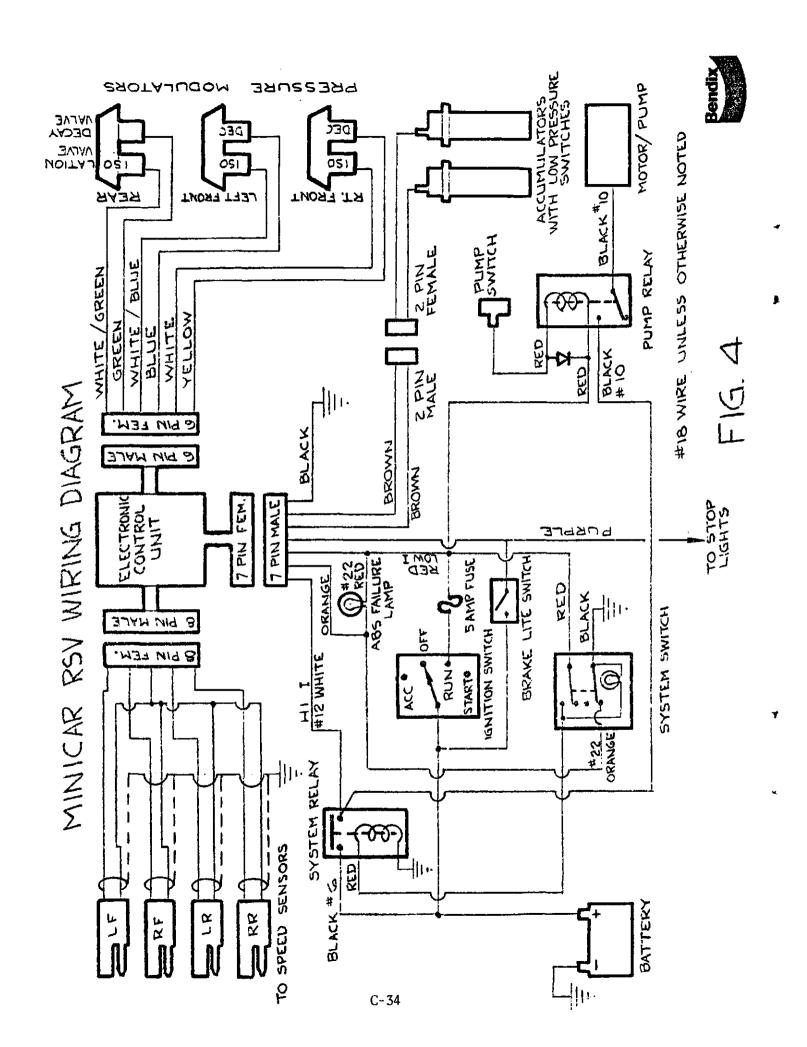


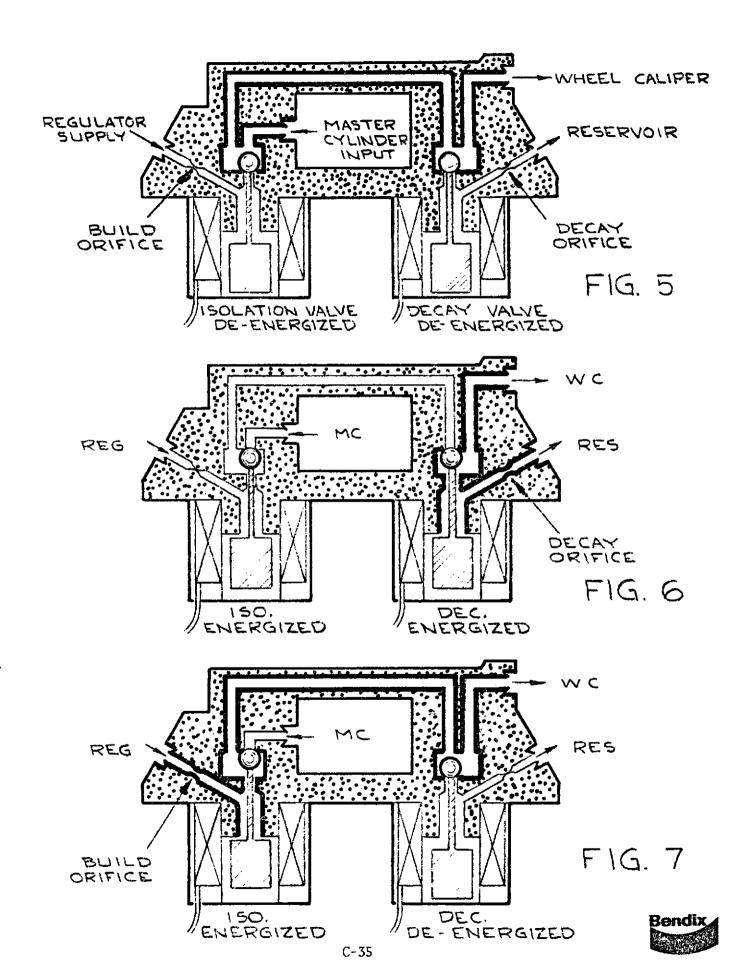
TYPICAL WHEEL SPEED SENSOR

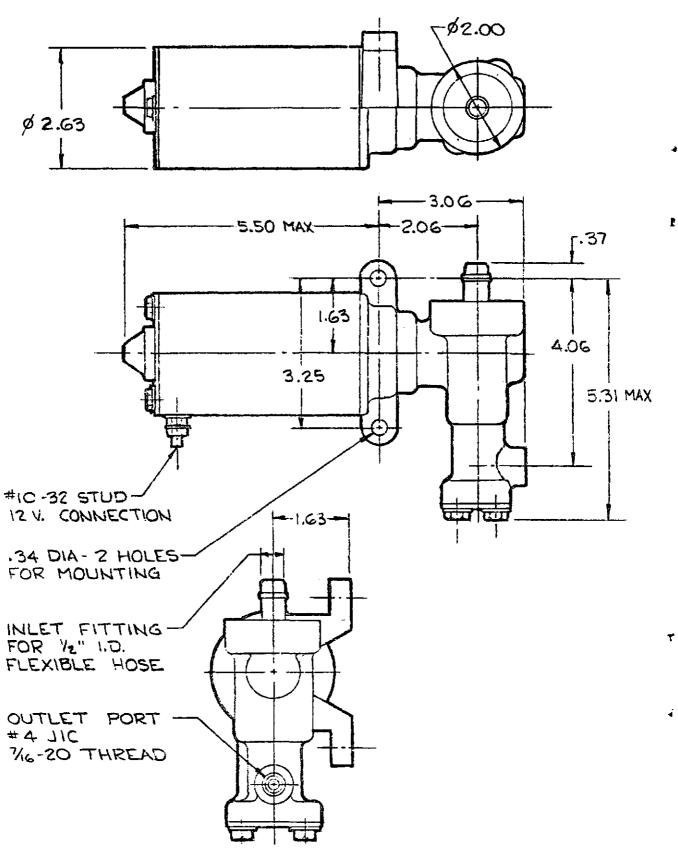
Figure 2





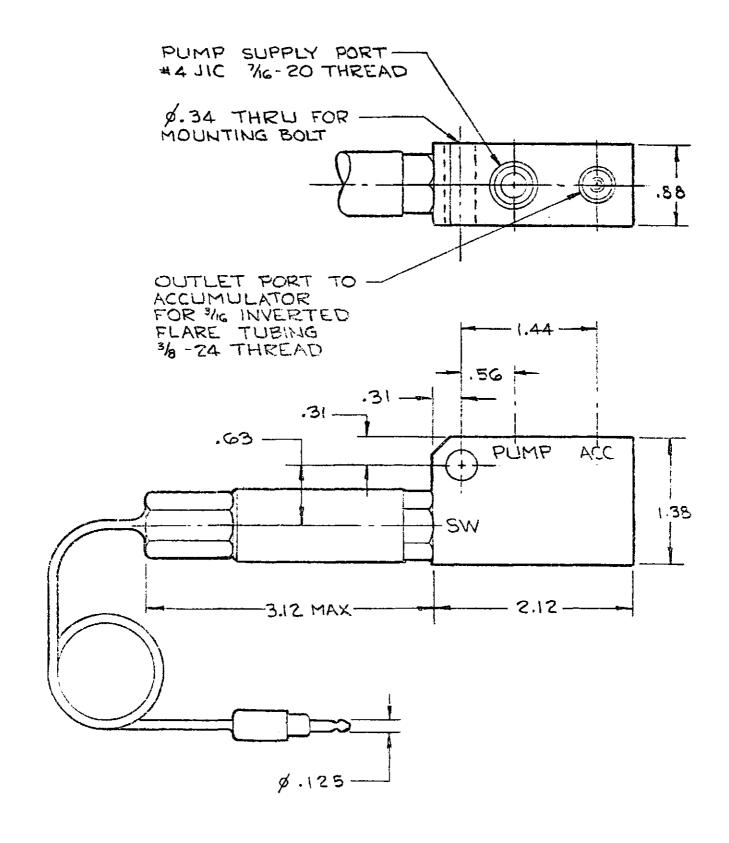






ABS MOTOR/PUMP ASSEMBLY





ABS PUMP SWITCH ASSEMBLY



.5

