The Design of High Speed Data Acquisition System Based on JESD204B

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Abstract. Recently, various acquisition systems require data converters to provide higher resolution and sampling rates. The physical layout of parallel interfaces and the bit rate limitations of serial LVDS methods pose technical hurdles for designers. The design is based on the classical architecture of FPGA+DSP+ADC of data acquisition system. The High speed ADC is based on JESD204B interface with four slices and two channels, it can meet the requirements of high-speed acquisition, and high-speed sampling of eight channels. It provides a good method for the design and application of various high-speed acquisition systems, and it effectively solves all kinds of problems in parallel transmission of traditional data acquisition, and brings great engineering application value.

1. Introduction

In our era, the increasing of demand for high data rate application is never stop. This trend leads to the development of high resolution and high sample rate ADC devices. As early as 1991, the United States Navy studied and designed a high-performance programmable signal processor, the architecture of FPGA+DSP had been widely used. Many universities and institutes in China have also developed their own signal processing systems under the FPGA+DSP architecture [1]. Combined with ADC chip, the high-speed acquisition system has also been implemented, but it is difficult for the data transmission to meet the needs of multi-channel, high bandwidth and small size when the traditional data acquisition system adopts parallel transmission mode of multiplex data wires. As a result, the JEDEC international organization has launched a new AD/DA sampling data transmission standard JESD204. So that, the development of the high-speed acquisition system can develop continuously [2].

2. The overall hardware design

The design is based on JESD204B interface, designed to achieve high-speed data acquisition system. The design is based on the classical FPGA+DSP+ADC data acquisition system architecture. The FPGA chip uses the XC7VX485T from the Xilinx Virtex-7 series. GTX, its maximum serial speed transceiver, supports the maximum line speed of 12.5Gbps. The DSP chip uses the TMS320C6678 from TI, it integrates 8 arithmetic cores, and the highest processing speed of single core can reach 1.25Gbps. The ADC chip uses the ADC32RF45 from TI, its data is output based on JESD204B interface. As shown in Fig 1, the eight channels sampling signal enters the ADC chip firstly, and then the serial high-speed transceiver GTX is transmitted to the FPGA by the JESD204B interface, then the data is sent to the DSP through SRIO for signal processing operations.

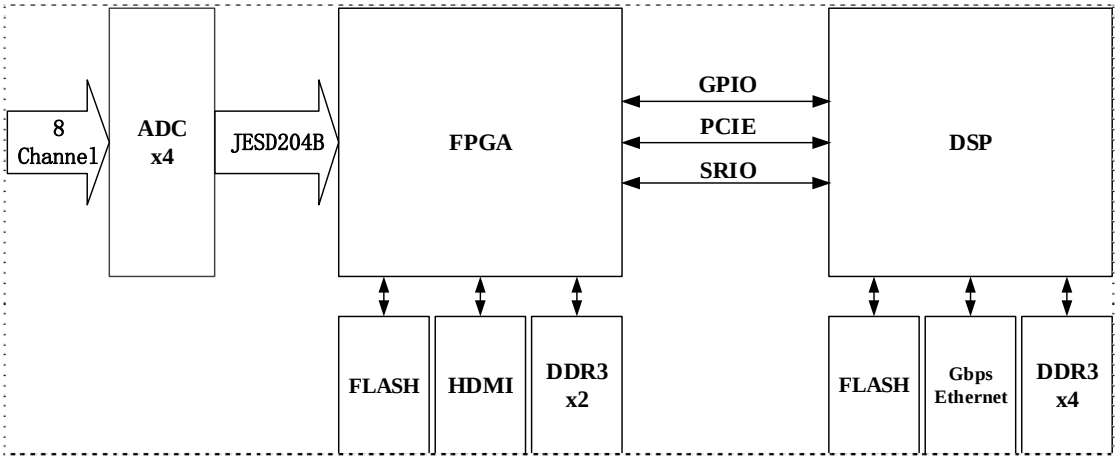

Fig.1 System overall structure diagram

In the design of the data acquisition system, the FPGA's external interface HDMI, a 19 pin high-speed data interface, is used for data's communication with external memory. On the board, we connect the four differential signal line of the FPGA's high speed serial transceiver (GTX) to the HDMI interface. The external high-speed interface of DSP adopts Gigabit Ethernet to realize high-speed data transmission. Both the FPGA and the DSP have an external 256MB Flash memory, In addition, the FPGA has two DDR3 external memory to form the storage space of the 1GB, DSP has four DDR3 memory external to form the storage space of 2GB.

3. JESD204B Interface

In the field of PC and embedded systems, it has been an empty talk that the method for improving bus bandwidth by raising bus operating frequency under the condition of a parallel bus data width. It cannot be realized at all because of the influence of technology and environment in the actual implementation. Therefore, the communication structure of the serial bus is changed from parallel bus communication. Typically, the ADC is 12~16 bit data lines, and strictly required to be aligned on one edge of the clock. The higher frequency the ADC operating, the greater data offset between the data lines, and then synchronization between data is becoming more difficult. The JEDEC international organizations have fully learned the advantages of PCIE/SRIO and other serial bus communication protocols based on data packet (frame format). The JESD204 protocol was introduced in 2006, it is the a differential pair adopted the CML level, instead of the 12~16 bit parallel data line, realizing serial communication interface and supporting the highest 3.125Gbps data transmission rate of ADC device. In January 2012, the JESD204 bus protocol has been upgraded to the JESD204 B.01 version, the maximum transmission rate of each pair of differential lines is supported by 12.5Gbps [3,4].

Table 1 Comparison of JESD204 with other interfaces

Number of Channels	Resolution	CMOS Pin Count	LVDS Pins Count (DDR)	CML Pin Count (JESD204B)
1	14	13	14	4
2	14	26	28	4
4	14	52	56	6
8	14	104	112	6

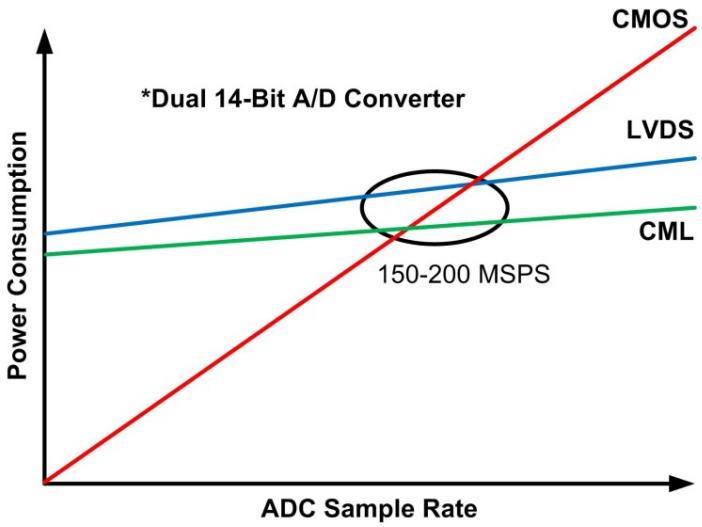

Fig.2 CMOS, LVDS, and CML Driver Power Comparison

In summary, the advantages of JESD204B include the following three points:

(1) Decreased in pin number, simplified system design, greatly simplified the wiring between ADC and FPGA

(2) Because wiring is simpler and pin number is less, using JESD204B will make the package smaller and simpler.

(3) High speed ADC devices consume less power per unit after adopting CML level.

At present, the TI, the ADI and other companies have their latest high-speed ADC chip based on the JESD204B interface. ADC32RF45 released by TI, AD9625 released by ADI, and the latest AD9208 released by ADI Company in April 2017, these all belong to the new ADC series adopted with JESD204B interface. In respect of Field Programmable logic device (FPGA), the company, such as Xilinx and Altera, also supports the JESD204B interface. In addition there are JESD204B dedicated clock chip, such as LMK042828, HMC7044 and so on.

4. The Key of ADC design interface

We can implement the JESD204B protocol by FPGA's GTX interface, to parse the data emitted by ADC correctly. The hardware uses the FPGA's GTX interface directly, and the GTX is connected with the data-in pin of the ADC. ADC data-out pin as the sending end, FPGA GTX port as the receiving end, to achieve data transmission on the line [5]. The software uses the 8B/10B codec module and the control character detection module which are embedded in the GTX interface. Among them, there are clock configuration and the analysis of data frames.

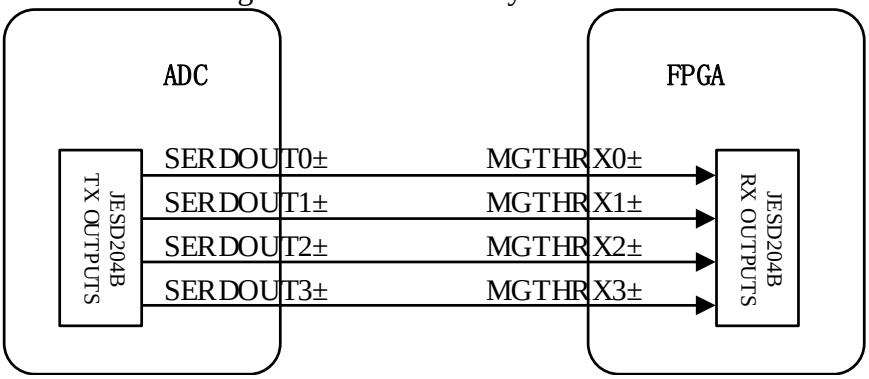

Fig.3 Interface design between ADC and FPGA

The ADC device ADC32RF45 is a 14 bit precision AD chip. The 14 bit AD sampling data and 0 in low two bit make up a frame with 16bit data. After framing, the data is encoded by 8B/10B, then it becomes 20 bit. Sending to Serial high-speed transceiver GTX of FPGA, FPGA complete the operation of the 8B/10B decoding and the analysis of JESD204B protocol. Setting the ADC32RF45 sample clock to 2.5GHz, the rate corresponding to the encoding at all levels is shown below.

Table 2 Comparison of JESD204B

	Clock/GHz	**Data-width/bit**	**Rate/Gbps**	**Remark**
Original data	2.5	14	8.4	ADC Sampled Data
Framing	2.5	16	10	Zero-padding
Coding	2.5	20	12.5	8B/10B

The ADC is dual channel, each channels has 4 lanes, that is, 4 pairs of CML data lines. As can be seen from the chart above, ADC eventually sends the sampled data at a rate of 12.5Gbps, GTX, the receiving rate of the FPGA side should also be set to 12.5Gbps.

5. Clock design

JESD204B begins with the edge of the clock signal to identify synchronization. And through a certain handshake signal, the sender and receiver can correctly recognize the frame length and boundaries. Therefore, the clock signal and its timing relation are extremely important to JESD204B. The following is a multi-device synchronization solution for the JESD204B system, the Device Clock is the main clock for the device operation. A clock that is usually sampled in a digital to analog converter or a clock with integer multiples. The frame and multi frame clock of the protocol itself are also based on Device Clock. SYSREF is the edge of the Device Clock used to indicate different converters or logic, or the reference delay between different devices.

In the JESD204B system, the synchronization of data converters can be broken down into four basic requirements. These requirements are vividly depicted in Fig.4.

(1) The phase alignment of the device clock is implemented on each data converter;

(2) The setting and holding time of the SYSREF (relative to the device clock) are met on each data converter and logic element;

(3) An appropriate resilient buffer release point is selected in the JESD204B receiver to ensure deterministic delay;

(4) Need to meet the SYNC signal timing requirements when necessary.

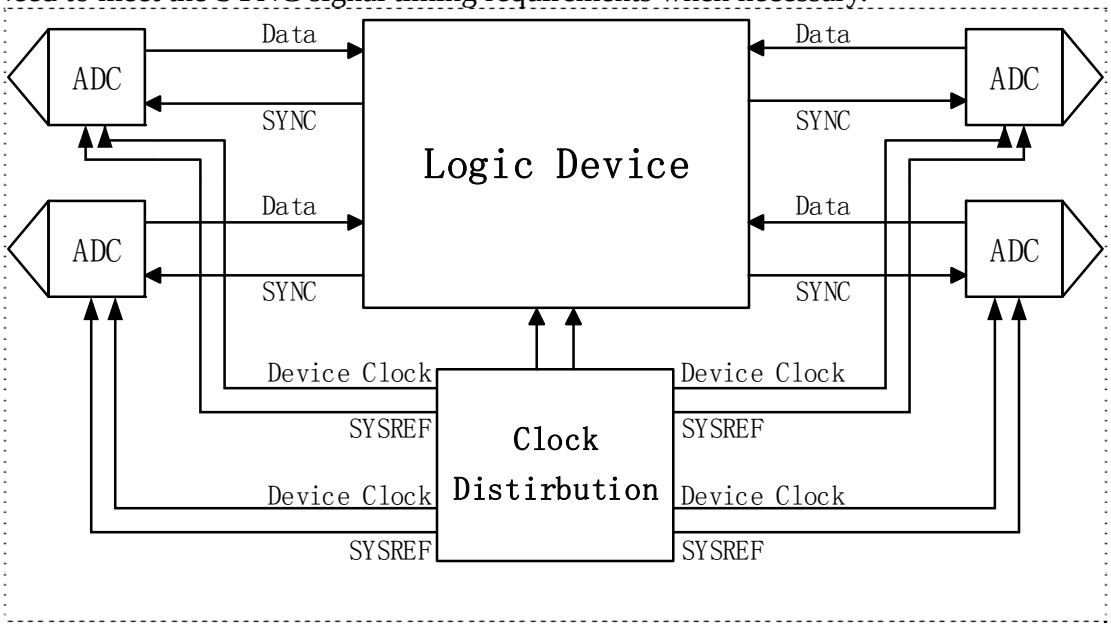

Fig.4 Multi device synchronization solution for JESD204B system

ADI and TI have high performance clock jitter attenuator with JESD204B, such as HMC7044, LMK04828 and so on. Their Device Clock, and SYSREF are paired output, its output timing meets its timing requirements, and its application is relatively simple.

6. Conclusion

This paper utilizes the advanced high-speed ADC with JESD204B interface, combine the latest ADC chip and Xilinx 7 Series resources, and proposes the design of high-speed data acquisition system based on JESD204B. This paper first describes the overall design of the system, and then we detailed for each module design. We first solve the core processing module of FPGA+DSP. Both of FPGA and DSP communicate with each other through SRIO, FPGA pretreatment data is sent to the DSP for signal processing. Utilizing existing technology and hardware, a high-speed data acquisition system is designed with the JESD204B interface ADC which has higher resolution and higher sampling rate (3Gbps or so). It can be well suited to eight channel high-speed sampling, the design is miniaturized and the wiring is simpler. FPGA resource consumption is reduced by about half of resources compared to traditional parallel data lines, it has great prospect of engineering application.

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