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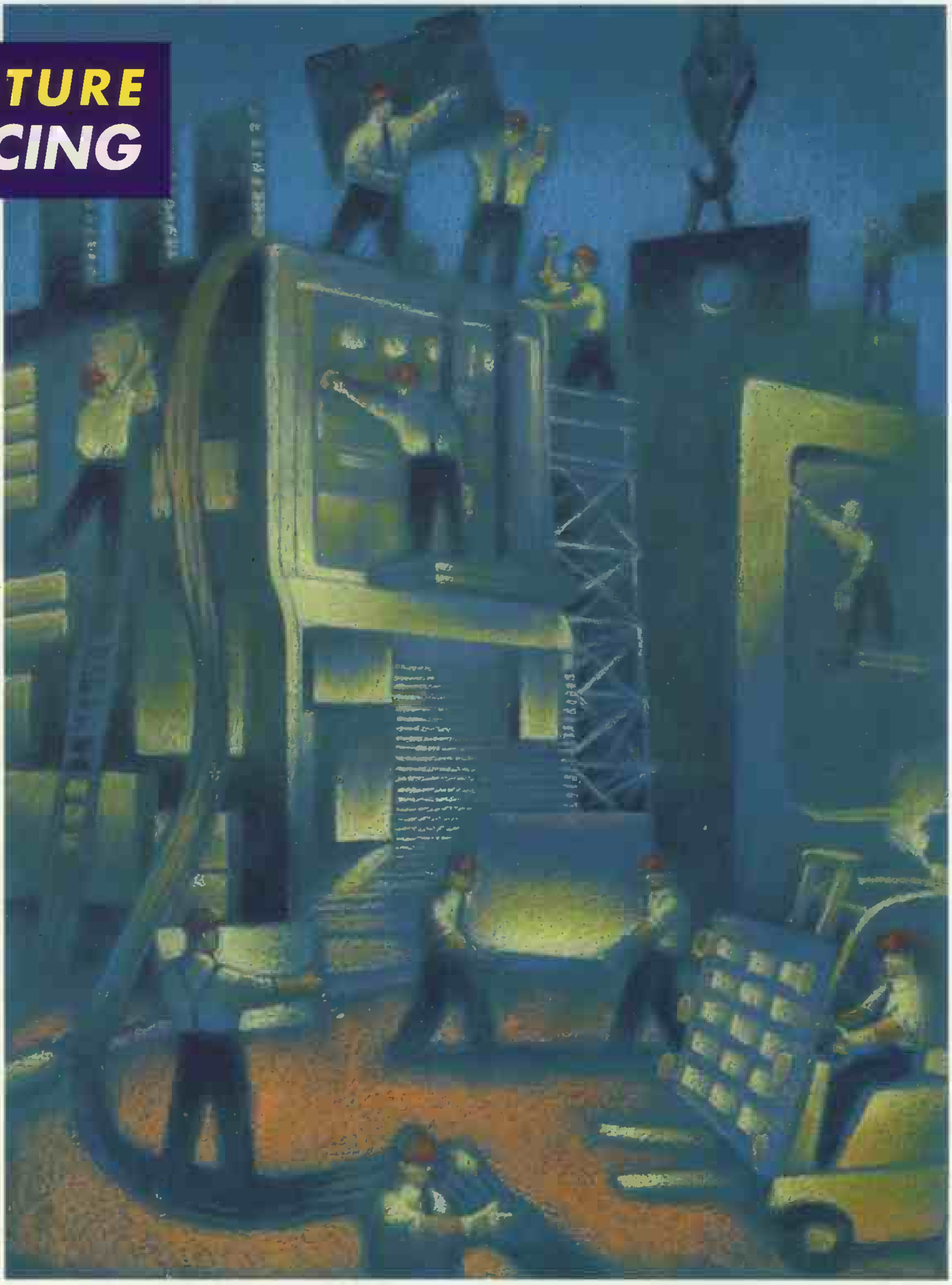

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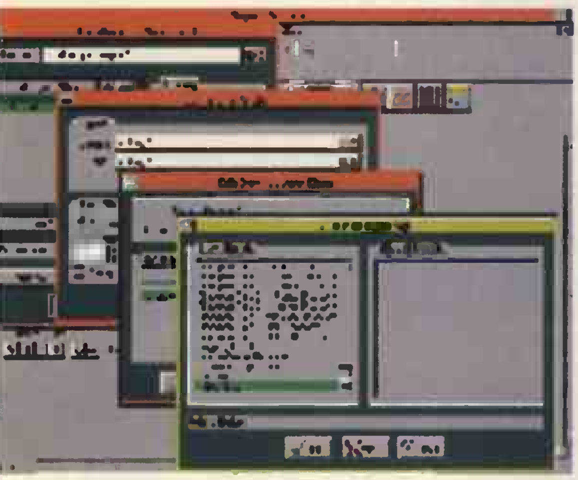
CONTENTS



Want to acquire data on a pc and analyse it? See page 567.

REGULARS

Next month:

Active subwoofer design, GPS, 24cm antenna.

AUGUST ISSUE – ON SALE 27 JULY

Cover illustration – Hashim Akib

Andy Emmerson has been looking at apparatus that was invented long before the world was ready for it. See page 562

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REED BUSINESS PUBLISHING

Jobs for the boys

The Government currently has the future of British broadcasting under review through the debate on the BBC's Royal Charter. Like Peacock and Annan before, the result will probably support the status quo and be of little significance to the average viewer.

It shouldn't be thus. Technology has placed all aspects of broadcasting into the melting pot. The old duopoly of BBC and IBA no longer exists yet both the Corporation and the successors to the IBA act as if it does.

Technology can send us programmes and services any way we want... via terrestrial broadcast, through satellite or by cable. Any house, any business, anywhere in the country could soon receive hundreds of broadcast quality tv channels when the digital satellites start flying early next year. Everyone from Lands End to John O'Groats will shortly be able to receive what they want, when they want – if the existing terrestrial broadcasters were prepared to embrace it.

NTL, the independent transmission company responsible for ITV terrestrial broadcasts, is currently banging on about the unfairness of allowing the BBC to retain its engineering and transmission service. It sees it as wrong to allow a public body to compete openly with private companies such as itself using public money. It says that either the BBC should run autonomously, with a specific prohibition on the selling of its engineering facilities externally, or that the BBC's engineering should be privatised to compete openly with other suppliers.

We invite a plague on both their houses.

The BBC and NTL want to create digital broadcast systems using a terrestrial network. While we accept totally that digital transmission should give the nation's viewers unparalleled choice of viewing, and offer excellent retailing and setmaking opportunities, all new digital tv services should go on satellite.

From a technical point of view, there is absolutely no reason to run digital tv from land based transmitters. The new technology will provide so many extra channels that the one remaining argument for terrestrial tv – regional programmes – completely loses significance. Satellite transponders cost far less than equivalent terrestrial networks yet the all-satellite option doesn't even enter discussion by the BBC or NTL.

Terrestrial television broadcasting occupies nearly half the available spectrum up to one gigahertz, a valuable and irreplaceable resource which could be freed up when analogue tv eventually closes down. Examples of the new applications for these frequencies include portable telephone and communications systems.

The NTL and BBC have a vested interest in maintaining terrestrial services. Satellite services make the organisations' terrestrial digital plans redundant. The Government should take this into account in submissions.

Frank Ogden.

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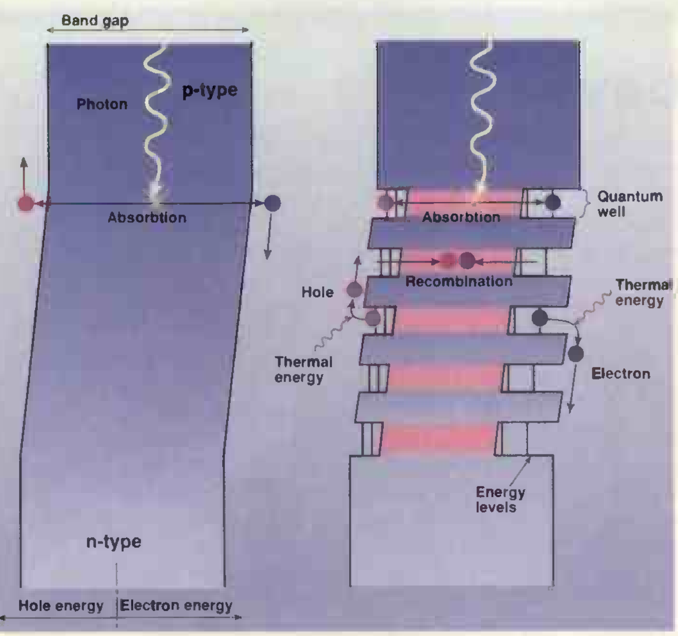
Solar cell eficiency boost

Energy diagram of conventional (left) and quantum well p-n junctions compared. Photons of lower energy are absorbed by the right hand junction even though both band gaps are the same.



What will we do when the oil runs out? No one knows yet, few people are thinking about it and fewer are doing anything about it.

One man who is making his contribution is Dr Keith Barnham, Reader in Physics at Imperial College London. He and his colleagues, with a little help from industry, are working on ways to improve solar cell efficiency.

Semiconductor solar cells reduce electricity by absorbing photons in, or near, a p-n junction. The photons create electron-hole pairs which, once they are established, drift across the junction under the influence of the electric field from the doping of the p and n type semiconductors, resulting in current flow in an external circuit.

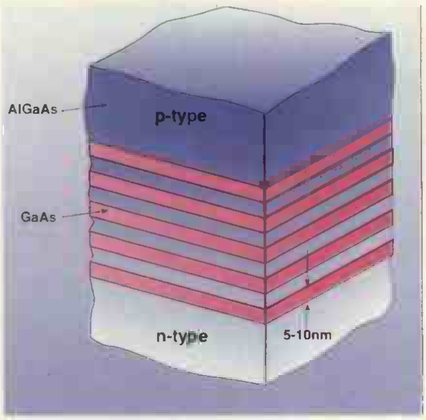
One of the features of sunlight that makes it so difficult to catch is that it has a spectrum. That is, it consists of light at a variety wavelengths, or, has photons of varying energies.

A 'normal' solar cell has a fixed band gap and can only usefully absorb photons of sufficient energy to boost electron-hole pairs across the semiconductor's band gap.

Photons with less energy than the band gap are not absorbed at all. Higher energy photons give the pairs far more energy than is required to push them across the band gap. Any superfluous energy above the band gap is wasted as heat when the pair fall back to the band gap level.

All this means that conventional solar cells absorb light at one wavelength very well, but less effectively over the range of wavelengths in the solar spectrum.

The choice of band gap becomes a compromise. A narrow band gap



Quantum wells are introduced into a p-n junction by interspersing very thin layers of lower band gap semiconductor with the bulk material.

material will capture a lot of photons and will produce a lot of current. But the narrow gap means low cell voltage. The cell voltage can be increased by using a wider band gap, but less photons will be usefully absorbed, so the current will be lower. The most effective band gap is the one whose energy corresponds with that of the amplitude peak of the incident spectrum.

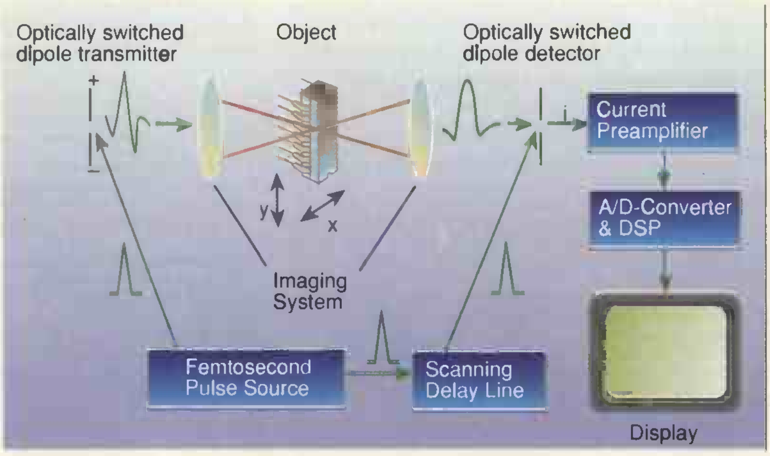
Dr Barnham's group has introduced thin layers of material, called

Terahertz analyser on the cards

Researchers at AT&T's Bell Labs in the US have developed a one terahertz time domain spectroscopy – tds – analyser that can be developed into a commercial product. The device can be used to measure the chemical composition of organic materials and gasses and to x-ray integrated circuits.

Currently, analysers using tds techniques are bulky and expensive but Martin Nuss and Binbin Hu, researchers at the Advanced Photonics Research Department at Bell Labs, are said to have a commercially viable device using compact lasers and advanced integrated circuits.

A tds map of a leaf, showing the reduction of water content over 48 hours. The leaf was visibly unchanged.



Tds is a technique for determining the absorption spectrum of a sample by sending an energy pulse of known shape through it and measuring the shape of the pulse after it has been distorted by the sample. Fourier analysis of the incident and resultant pulses reveal the absorption spectrum.

The absorption spectrum of materials at frequencies around one terahertz gives information about the water content of organic materials, the fat content of meat and the chemical composition of gases. Since metals are opaque and plastics transparent at 1THz, the technique can also be used to x-ray integrated circuits.

quantum wells, into the semiconductor junction.

These thin layers, only a few nanometers thick, are interspersed between layers of the native semiconductor and have a lower band gap.

Extremely thin layers of semiconductor behave differently than the same material in bulk. The distinct energy levels that electrons occupy theoretically are 'blurred' in mass material but exist in thin layers.

Photons of insufficient energy to push pairs over the band gap of the host may still have sufficient energy to create useful pairs in the quantum well material.

The Imperial College group as shown that the electron-hole pairs last long enough, a few nanoseconds, to escape from the wells. They escape because thermal energy in the semiconductor is often enough to raise the energy in the electron or hole high enough to move it into the band gap of the adjoining native layer. It then drifts through this, falls into the next well and the process is repeated.

The native material can be chosen with a high band gap to give a high cell voltage, but the current remains high because a large number of photons are absorbed.

But there are problems. So far all the work has been done with expensive gallium arsenide (GaAs), rather than cheaper silicon. There are two related reasons for this. Silicon absorbs photons by a more complex, 'indirect', route that does not lend it self to this kind of process. And quantum well technology in silicon is still in its infancy.

Dr Barnham said: "Our work is still in an early experimental stage. We have taken a simple, conventional solar cell material with a sunlight efficiency of eight percent and boosted it to 14 percent using quantum wells."

Although he realises that GaAs has cost limitations, Barnham said: "GaAs has two advantages. It needs 100 times less material than silicon to absorb the same number of photons and its theoretical efficiency is higher than that of silicon." He also noted that the increasing demand for GaAs for optical computing and lasers is bringing the price down.

Quantum well solar cells have the potential to extract more usable energy from sunlight than conventional cells. This is because they can absorb a wide range of photons but retain a high cell voltage. They can only be made in gallium arsenide and aluminium gallium arsenide at this time but the concepts may transfer to silicon as silicon quantum well technology improves. Dr Barnham had a final word to about the potential efficiency of this kind of cell: "The very best conventional GaAs solar cells are 25 per cent efficient, the theoretical limit is about 30 per cent. Whether quantum wells will allow the GaAs to exceed this upper limit is open to question but they seem to be a better way to approach the maximum."

Toshiba finds dvds ally

Time Warner says it will manufacture super density digital video discs (dvds) to be used by supporters of the Toshiba video disc standard to record and play digital films.

The company has formed a new subsidiary called Advanced Media Operations. The discs will be capable of storing as much as 270 minutes of mpeg-2 compressed digital video. The range of discs includes SD-5 with 5Gbytes storage capacity for digital films and multiple language soundtracks; SD-9, a double layer single-sided disc with 9Gbytes storage; SD-10, a double-sided disc with 5Gbytes storage on each side for double feature films or a digital movie plus a related video game; SD-R a recordable format with 3.2Gbytes storage on each side; and SD Rewriteable with 2.6Gbytes storage on each side.

Time Warner says that it has already produced more than 300,000 high density discs. The move is a further boost for the supporters of the Toshiba digital video disc standard which is competing with the Sony-Philips standard.

The digital video discs to be made by Time Warner can store 270 minutes of compressed digital video.

Generating short energy pulses at 1THz has hitherto been difficult and expensive.

Nuss and Hu's analyser uses novel laser switched micro dipoles to transmit and detect the 1THz, single cycle, measurement pulse. The primary source of energy and timing in the Bell Labs set-up is a self-mode-locked Ti:sapphire laser. This type of laser inherently produces a stream of very short energy pulses. In this case the chosen laser produces a 100fs pulse of 800nm wavelength light at a repetition rate of 100MHz.

The laser output is split into transmit and receive beams. The transmit beam is used to trigger a photoconductive switch in the centre of a microscopic dipole.

The dipole is a conductive line 50[?u]m long on a GaAs substrate. A bias voltage, between 10 and 100V, is connected across the length of the line but current cannot flow due to a narrow gap in the middle. The laser pulse is directed at this gap and generates electron-hole pairs that briefly connect the gap edges.

The resulting brief current flow causes the dipole to 'ring' and act as a transmitting antenna. The rf pulse that is generated is approximately 1ps long with a spectrum centred at 1THz. An 'optical' system, consisting of mirrors, focuses the spectral pulse onto the material under test. This pulse passes through (or is reflected by) the material which may be up to 1mm thick, and is shaped by the material's time domain response.

A second mirror focuses the resultant distorted spectral pulse onto a second, detector, dipole. This dipole has to be very fast and has been fabricated using silicon on sapphire technology. The electrical (e) field of the distorted spectral pulse creates a bias voltage across the detector dipole. The field, and therefore the bias voltage, changes with time as the spectral pulse passes the dipole.

The receive part of the original 100fs laser pulse is directed at the centre of the detector dipole. This laser pulse turns on the dipole briefly, converting the instantaneous e field derived bias voltage into a current pulse.

The whole process repeats at the 100MHz rate and the average of the current pulses represents the e field of the spectral pulse as the receive laser pulse samples it.

Varying a delay in the second laser path (using a moving mirror) allows a complete profile of the distorted spectral pulse to be obtained.

Fourier analysis of the original and distorted spectral pulses allow the transmission (or reflection) characteristics of the material under test to be derived.

The experimental rig measures two feet square but Nuss suggests a purpose built TDS would be considerably smaller.

The Bell Labs team has shown that the cost and size of this kind of TDS can be reduced enough to make commercial exploitation possible.

Smallest, fastest 256Mbyte DRAM announced

IBM, Siemens and Toshiba have claimed success in the development of a fully-functional 256Mbyte dynamic ram chip, the smallest and fastest yet developed.

The dynamic random access memory chip – less than half an inch in size – is the culmination of two and half years' research by leading scientists from the three companies at IBM's advanced Semiconductor Research and Development Centre in New York. A spokesman claimed that it was at least 13 per cent smaller and has an access time nearly twice as fast as any chip on the market. At the moment the chip is only available in sample quantities, and only for internal evaluation. No indication has been given as to when production quantities will be available.

Said to be the smallest and fastest yet developed, this 256Mbtye d-ram is a joint development by IBM, Siemens and Toshiba.

D-rams are pervasive, fingernail-sized silicon devices that store electronic data in all manner of products ranging from mainframe computers to home appliances. A single 256Mbyte d-ram can hold more than 25,000 pages of double-spaced typewritten text.

The smaller size and faster speed of the device will be required by the memory-hungry systems of the future such as high-definition digital video, multimedia pcs and telecommunications systems. For manufacturers and developers a smaller, faster chip means improved overall system performance and a reduced footprint for memory on printed circuit boards.

"This remarkable breakthrough in advanced research shows what can be achieved by a dedicated alliance of companies that brings leading-edge capabilities to a highly motivated program with clear aims," said Manaobu Ohyama, senior vice president of Toshiba and group executive of its semiconductor group. "The project and its achievements are clearly in the forefront of many international projects for advanced semiconductors."

Dr Michael J Attardo, general manager of IBM's Microelectronics Division declared: "This is only the beginning. The best is yet to come."

The device uses 0.25 micron cmos process technology and is designed to support any proposed Joint Electron Device Engineering Council (JEDEC) standard for 256Mbyte DRAMs.

Details of the performance and technology aspects of the chip will be presented at the 1995 Symposium on VLSI Technology, and at the 1995 Symposium on VLSI Circuits, both held in June in Kyoto, Japan.

The 256Mbyte d-ram project is not the only area in which the three companies are willing to co-operate to share cost and expertise. IBM and Siemens currently work together in 16Mbyte d-ram manufacturing. IBM, Siemens and Toshiba are partners in 64Mbyte d-ram development, and a joint venture between IBM Japan and Toshiba manufactures advanced colour flat panel computer displays. Toshiba and Siemens have been collaborating in various semiconductor areas, including 1Mbit dynamic rams, standard cells and gate arrays.

Personal point-to-point satellite comms

Video-on-demand (vod) developer Online Media says it is involved in research which could lead to personalised point-to-point satellite communications services delivering 2Mbit/s channels to the home within three years.

Online Media is working with parent company Olivetti on a technique to use highly directional spot beam satellite transmissions to turn today's point-to-multipoint satellite tv broadcasts into point-to-point services. The company is using Olivetti's satellite hardware joint venture with Hughes to adapt spot beam technology for interactive tv services. The return channel would be provided over a telephone line.

According to Online Media chief executive Malcom Bird, the cable TV companies' window of opportunity for interactive tv is between three and five years. "Once the satellite boys can point-to-point download data they will knock the cable companies for six," he said.

Online Media's is currently conducting a vod trial with Cambridge Cable which have 200 users by the end of the year.

Emi analysis goes 3D

Quad Designs, a Viewlogic Systems subsidiary, has introduced an electromagnetic interference analysis tool that includes a three-dimensional simulation engine.

Quiet Version 2 has been designed to predict electric and magnetic field intensities radiated from backplanes, motherboards and mcms.

The package is claimed to be capable of allowing for cable radiation, enclosure resonances and multi-board screening.

Quiet uses a mixture of finite difference time domain analysis and what it describes as a full-wave simulation technique which solves Maxwell's equations for the whole structure.

Quiet 2 will be available before the end of the year.

Draft interface standard for sensor connect

The National Institute of Standards and Technology (NIST) have unveiled a draft of their sensor interface standard. The specification seeks to standardise output range – likely to be 0.5V to 4.5V – and supply voltage, probably at 5V. It also proposes a format for transducer electronic data sheet (teds) and a sensor model to be used in teds. A spokesman for NIST said that it aims to produce a definitive draft by the end of this year.

Broadcasters soon to get disk option

International test and measurement giant Tektronix is developing disk-based storage products aimed at the television broadcast community. The professional video storage market – currently dominated by tape-based vcrs using the Betamax format – is worth £30bn and is dominated by electronics giants such as Sony and Panasonic.

Farnell buys CPC

Components and spares distributor CPC has been sold to Farnell Electronics for £30m. The company will be extending its product offerings and looking to expand into Europe, something it has been "looking at for quite some time", according to CPC managing director Chris Haworth. Farnell Group chief executive Howard Poulson said the move into Europe will be "sooner rather than later". He takes over as chairman of CPC from outgoing founder Keith Duckett. ■

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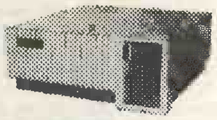

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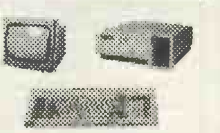

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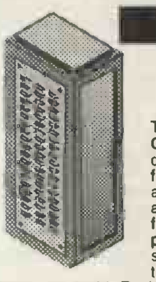

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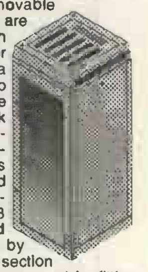

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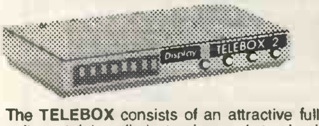

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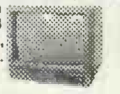

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CIRCLE NO. 108 ON REPLY CARD

RESEARCH NOTES

Jonathan Campbell

Analogue mics begin to sound a little creaky

In the increasingly digital domain of modern audio recording, the tried and tested microphone still stands out as an obvious link to our past. But a new digital design could break that link forever, enabling microphones to deliver digital output directly to mixing desks.

Conventionally, analogue microphones produce an output, proportional to incident sound pressure, which is converted to digital form for processing. But they can suffer noise, which a digital design should not. They also have outputs that are not so easy to filter and they can not be directly linked to digital recording systems.

Now F A Ghelmansarai, a Umist researcher in the Department of Electrical Engineering & Electronics, looks to have overcome those shortcomings with a design incorporating several innovative ideas.

In Ghelmansarai's mic ("Digital optical microphone and digital transducer, *IEE Proc Circuits Devices Syst*, Vol 142, No 2, pp.135-139), a diode laser beam is directed through an optical scanner onto a photoconductive detector. The detector is designed to deliver a number of pulses, depending on the movement of the beam, and so provides a direct measure of the microphone membrane deflection. Pulses are converted to logic pulses and counted, to produce a representation of the amplitude of sound pressure in binary.

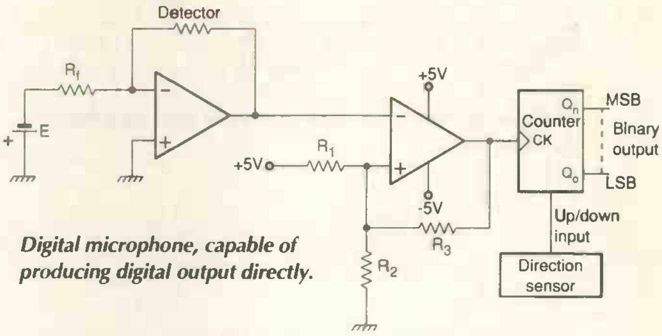
Key to operation is design of the interdigital photoconductive detector (idpc) itself. In it, two metallic electrodes are deposited as a series of separated interlocking fingers onto the surface of a conducting layer of InGaAs.

The electrodes are connected to a power supply, and conductivity of the semiconductor is greater when a conducting section is illuminated than when a *non*-conducting aluminium section is illuminated. So scanning the laser beam over the structure generates a series of pulses, which can be converted to logic pulses. In this way the design provides a precise indication of the position of the laser beam on the detector, generating a digital audio output.

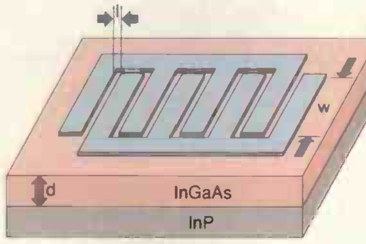
Successful operation has only been made possible through simultaneous development of a novel method of scanning the detector – making use of a multi-reflecting scanner – a beam expander and a lens to scan the idpc without calling for any analogue driving voltage while also magnifying the angular movement of the membrane.

Using a 20V dc bias voltage and charge amplifier producing 250mV/pC, Ghelmansarai says a ten-bit microphone can provide a sensitivity of 0.09mV/nm and a bandwidth of 5MHz.

The principle of the idpc could also be applied to a digital transducer.



Digital microphone, capable of producing digital output directly.



Laser beam from the optical scanner generates pulses as it moves across the photoconductive detector.

Robotic ants on the march

They're small, identical, hard workers and operate cooperatively in a group for the benefit of their community. But these insects don't have six legs and antennas, but rather rubber tracks and electronic sensors. Robot ants are here, crawling (still rather chaotically) out of the labs at MIT in Massachusetts, and Virginia Polytechnic, Virginia.

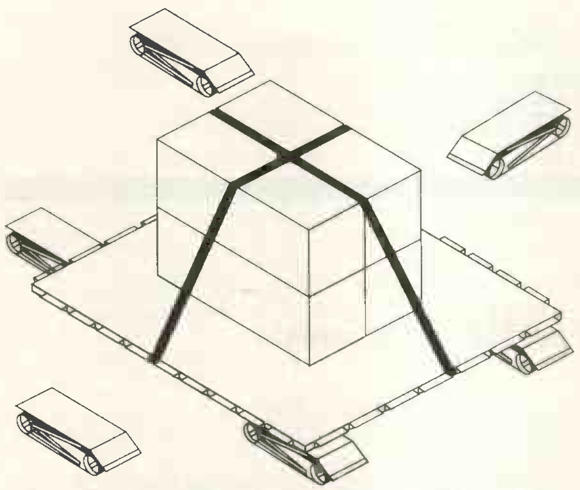
MIT's James McLurkin, a senior in electrical engineering and computer science there, has been concentrating on building colonies of robots using micro-robots developed as a basis for a remote-controlled colon surgery.

His robots are guided away from objects they hit and toward illumination sources by antennae and light sensors, and also have mandibles powered by a third motor to pick up bits of "food" – so far they have been feeding on quarter-inch balls of crumpled brass. Each has a pair of tiny treads powered by a battery and two motors taken from vibrating beepers.

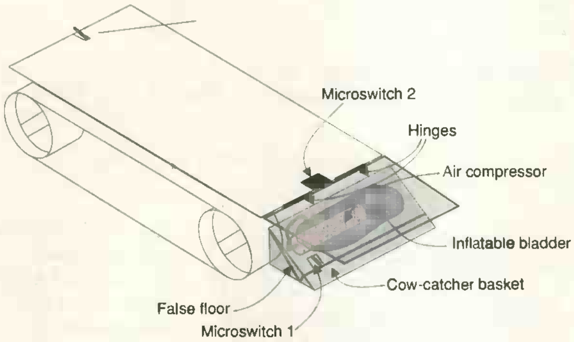
McLurkin and colleagues have built six robot ants up to now, eventually aiming to have 21, which would be the largest robot community in the world.

The goal is to have the robots behave cooperatively like an ant colony, seeking food and communicating with each other about where to find it. They do this with the aid of infrared transmitters and receivers. If one robot finds food, it sends out the message "I found food;"

MIT's McLurkin is looking to create the largest robot ant colony in the world. The CIA is watching carefully.



Multiple robotic ants could be used as the basis for a flexible handling system.



First attempts at a Virginia robot that can crawl in and out from under loads.

others in the vicinity respond by heading toward the sender and signalling "I found a robot that found food," eventually spreading the word to the entire group. The robots also check once a second for the proximity of other ants to help avoid collisions.

In practice, the robots tend to get confused if they receive signals from more than four other robots at once. It's impossible to get robots to act exactly like ants because of the sophistication of ant behaviour, and because "nature solves a lot of problems differently from the way people think they should be solved," says McLurkin.

However, his task is made easier by the fact that individuals (either real ants or robots) can fail and yet the group as a whole can still succeed.

Potential applications for the MIT ants include groups of disposable micro-robots to inspect pipes in nuclear power plants, while the CIA is also said to be interested in equipping the micro-robots with cameras and microphones for staking out buildings.

John Bay at Bradley Department of Electrical Engineering, Virginia Polytechnic, has been working with much bigger ants. His aim is to develop an "army ant" approach to flexible handling problems, with small identical robots working together to move materials.

Unlike conventional handling solutions, his ants can deal with non-standard containers, and will handle loads heavier and more costly than themselves.

Bay and his team have been concentrating on design of the robots themselves, with the main aim to produce a robot with a low profile able to crawl in and out from under a load ("Design of the army-ant cooperative lifting robot", *IEEE Robotics & Automation*, pp.36-43).

Sensors include infrared monitors for beacon-/direction-finding and obstacle detection, ultrasonic for range finding, and a whisker contact for collision detection.

Materials handling use requires that the ants must be able to detect the range and direction to a stationary beacon attached to a payload and must also be able to locate each other. In use they must be able to work together perhaps in a hierarchy of leaders and followers, to lift and move a load. They must also be able to share the load equally amongst themselves.

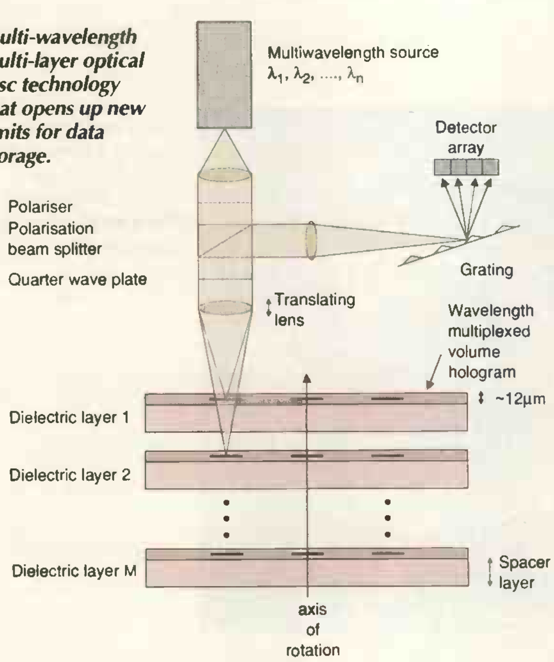
Robots so far constructed are costing £2000 in materials (plus a huge amount of goodwill from student teams). That could still add up to a sizeable sum for a complete robot ant handling system, but Bay points out that the ants can be acquired in a modular fashion, with each robot contributing to the overall solution, but with the system still operating if an individual unit fails.

Presumably the CIA is at this moment planning how it can use these ants too, to put the skids under Fidel

Getting (a lot) more out of optical storage

Optical disk system hardware manufacturers are already facing up to do battle with competing technologies looking to squeeze the latest Shwarznegger or Demi Moore onto digital video. The problem is that Arnie's bulging biceps can soak up anything up to 5Gbytes of capacity, stretching to the limit current optical disk storage techniques. But two electrical engineers from the University of California have proposed a system that can double at a stroke the current capacity limits, on a single side of an optical disk, and can offer much higher capacities in the future.

Multi-wavelength multi-layer optical disc technology that opens up new limits for data storage.



Storing 5Gbytes of video is already possible – just. Philips-Sony technology can compress it onto a 3.7Gbyte disk; or a 5Gbyte disk system is being developed by Matsushita-Toshiba and others, in alliance with major film studios.

But S Homa and AE Wilner are proposing a technology (*Electronics Letters*, Vol 31, No 8, pp.621-623) that offers 9.7Gbytes as a starting figure, with far higher levels possible in the future.

The technique depends on combining two separate methods for reading and storing data – a multi-layer method that allows data to be stored and read in three-dimensions in the disk, and wavelength-multiplexing where each layer contains different data channels accessible using different wavelengths.

Use of a multi-wavelength source allows the various channels to be read from the same location in the same layer, with the wavelength dependent reflected signal being spatially separated and recovered by a detector.

Other layers are read by the same wavelength source, by mechanically translating the lens up and down to focus the source on each layer in turn.

Using this technique, a six wavelength source and six layer disk could store anything up to 40Gbytes – if the laser spot size were small enough and channel separation large enough.

But even with a 25nm channel separation and a 2μm spot size a total capacity of 9.7Gbyte has been achieved, a figure that will be improved upon with optimised manufacturing techniques, say the researchers.

Spark of genius?

Automotive engineers have long been searching for a simple technique to enable continuous monitoring of combustion parameters inside a petrol engine. Now H Zhao and N Collings, at the University of Cambridge, and T Ma of Ford Motor Company, seem to have come up with a simple answer: use the spark plug itself as the probe.

In fact, using the spark to find out more about what is happening inside the engine is not in itself new. Previous workers have used the spark plug to detect engine knock and even to investigate plug fouling. But where the new system differs is that it needs no expensive and unreliable high voltage diodes. Instead it builds on the recent appearance of one-coil-per-plug ignition systems, with circuitry integrated into the secondary winding of an ignition coil ('Engine performance monitoring by means of the spark plug', *Proc Instn Mech Engrs*, Vol 209, pp.143-146).

Inside a conventional engine, the spark plug ionisation current can be broken down into two stages. Stage 1 reflects the performance of the plug itself in terms of plug fouling, pre-spark ignition and spark plug voltage/resistance. An earlier team has already shown that the leakage current prior to spark is inversely proportional to the plug leakage resistance and so indicates any spark plug fouling. Any leakage peaks before sparking also identify pre-ignition, while the spark voltage spike, slope and duration can be used to provide information on spark plug gaps, open plug wires, shorted coils and other problems.

But it is stage 2 of the cycle that the researchers have now been concentrating on, where the ionic current flowing relates to the combustion processes. In the new system, the positive end of the secondary winding is connected to a 1µF capacitor in parallel to a 1MΩ resistor and an isolated 370V transient suppresser – a combination that puts +400V bias across the spark plug.

Ionic current flowing through the plug is then measured as a voltage appearing across a resistor, with a 4.7V zener diode in parallel to limit output voltage in the range –4.7 to 0.7V.

As the researchers point out, because the ionisation detection circuit is on the secondary winding, greater sensitivity can be obtained than by using the primary windings. More importantly, high voltage diodes are not necessary.

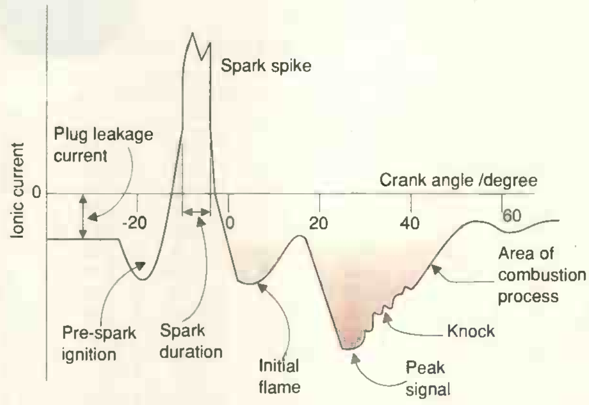
Testing the system using a single-cylinder engine with a pressure transducer mounted in it, enabled pressure and spark plug ionisation signals (spi) to be compared directly.

Results show a very good correlation between pressure and spi, suggesting the system would be a reliable and cheap way to detect knock. Similarly, tests showed that the maximum values of spi showed good indication of engine cyclic variations.

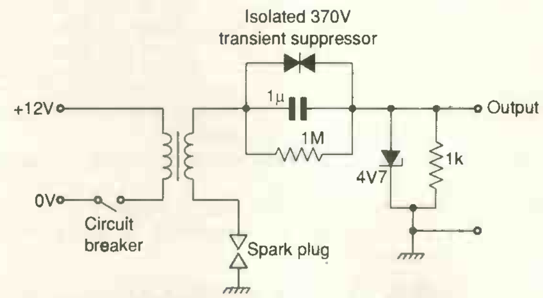
Plainly the system provides a practical way to enable spark plug monitoring to be applied directly to a one-coil-per-plug system without any engine modification or mapping.

If car makers were to make full use of the system's potential, this simple approach could be used to supply information on everything from mis-firing and pre-spark ignition to changes in overall combustion performance.

Not bad for a spark of an idea.



Ionisation current can reveal a surprising amount about the workings of a car engine.



Spark plug ionisation probe built into the secondary winding on a one-coil-per plug ignition system.

LF noise is a real problem – sometimes

Complaints about low frequency environmental noise repeatedly surface (some in the letters column of *EW+WW*). But frequently complainants are frustrated that they are not taken seriously. Whether that situation will improve following a study carried out by the Building Research Establishment and Sound Research Laboratories is not clear. In most instances no noise was detected: in the few others it is mains hum. But in one case...

Some 500 people a year complain about low level noise. In the vast majority of instances, according to John Sargent of the BRE ('A study of environmental low frequency noise', *Acoustics Bulletin*), no sound can be measured.

In fact of the 31 cases investigated in detail as part of the study there were only three where noise could be detected. In two, the noise was consistent with the 100Hz noise emitted by electrical sub-stations.

But in the other there was a narrow band of measured noise centred on 104Hz, which, though low level, was audible. Sargent reports the noise was still present when the local electricity board switched off the nearby sub station. The noise was not audible or detectable outside the house, yet no-one could identify its source.

In another seven cases there was some evidence to suggest that a low level of noise may occasionally have been present.

Part of the difficulty with low frequency noise is that the extent of the problem is dependent on the perception of the individual. Mostly, the study, speculates, the problem is down to tinnitus or hypersensitivity to all sounds.

In one case a husband and wife both complained of hearing low frequency noise, a noise that was subsequently measured in a particular room in their house.

But it became apparent that the woman was also able to register the sound in a sound-proof room, while her husband could not.

The conclusion was that the she had tinnitus, but that her drawing attention to the noise had sensitised her husband so that he began to experience the real noise. Amazingly this complex state of events was not unique in the study, says Sargent.

The survey advises that investigators looking into lf noise complaints should be armed with a frequency analyser, operable in real time with a narrow $^{1}/_{24}$th octave bandwidth. If they don't find anything, any "opinions about the complainants hearing should be avoided". ■

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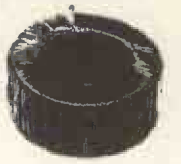

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80	17.98	12.60	9.49	7.02	6.81	6.60
100	21.07	14.74	11.11	8.21	7.96	7.72
120	21.54	15.08	11.35	8.39	8.15	7.89
150	25.98	18.19	13.70	10.12	9.82	9.53
160	23.83	16.68	12.56	9.28	9.00	8.73
225	30.10	21.07	15.87	11.73	11.39	11.04
300	34.32	24.02	18.09	13.38	12.98	12.58
400	46.19	32.32	24.35	17.99	17.47	16.94
500	50.48	35.34	26.61	19.67	19.09	18.51
625	53.09	41.36	31.14	23.02	21.24	20.57
750	58.39	44.23	33.30	24.62	23.89	23.17
1000	78.80	55.16	41.54	30.70	29.80	28.89
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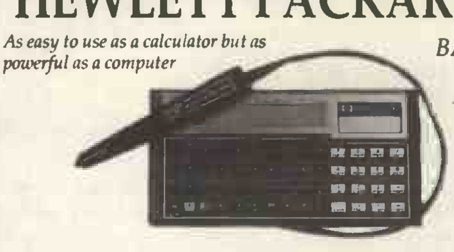

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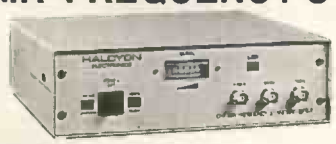

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I/O processing *made easy*

Hamid Mustafa's i/o interface simplifies sensing and load switching by using a PIC microcontroller to respond to brief Ascii commands keyed in on a pc or terminal. Hamid's simple terminal emulator is also useful as a general-purpose RS232 receiver and generator.

My universal i/o processor is based on the Microchip *PIC16C55* single-chip computer. It provides eight inputs and eight outputs.

The interface is driven from any RS232 device capable of sending and receiving Ascii characters. This can be an Ascii terminal or a pc comms port.

I designed the circuit to provide digital i/o capabilities via a Psion Organiser. This i/o was used to monitor the frequency and time of the day that a conveyor was stopped and re-started by operators on a production line. The i/o processor provides the status of three stop and two start buttons while the Psion organinser time stamps the event.

In another application the interface operates pneumatic cylinders to separate and apply labels to envelopes, printed by a label printer. The printer is driven by a pc via the parallel

Commands from the keyboard are translated into i/o functions.

Output commands:
O=A3 sets the output port to byte A316
O2=1 turns output 2 on, O2=0 turns output 2 off
O2=I toggles output 2

Input commands:
Ox=1 and Ox=I where x is 0-7. I=?? gets the input port status in ascii hexadecimal form, e.g. 5F in ascii
I4=? gets the status of input 4, e.g. 1 in ascii

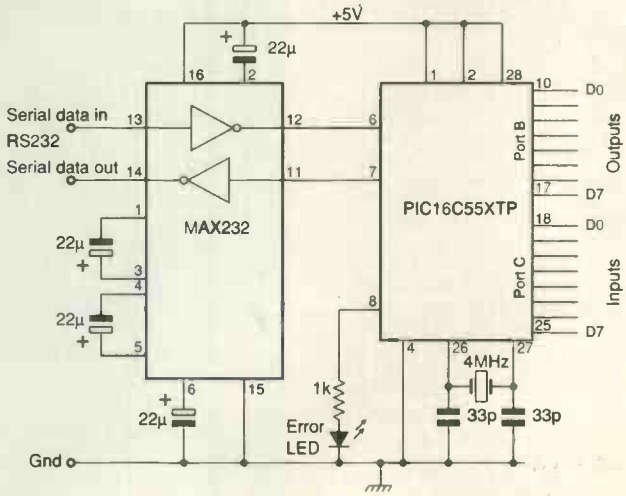

Fig. 1. PIC microcontroller and serial buffers produce a versatile i/o interface. Controlling relays, lamps and mains loads is achieved by simply buffering the micros' output and typing Ascii characters on a keyboard. Sensing switch contacts is even easier.

port, and the pneumatic solenoids are switched by the i/o processor via a serial port. This arrangement eliminates the need for i/o boards plugged into the pc when eight inputs and eight outputs are sufficient and speed is not critical.

Input and output commands are received by the i/o processor receives via the serial port, interfaced as shown in **Fig. 1**. Commands are made up of four Ascii characters. For example O=5A will put $5A_{16}$ (01011010_2) on the output port, while O=00 will switch off all eight outputs. Input commands grab the status of the input port. For example, I=?? returns two Ascii hexadecimal characters such as $E4_{16}$ (11100100_2). Commands may be in upper or lower case, see Commands panel.

Communications parameters are fixed at 9600 baud, 7 data bits, no parity 2 stop bits, no handshake. The i/o processor is fast enough to work without the need for hardware handshake. At 9600 baud, a character is sent in 1ms. Therefore response time of the processor is 4ms. If inputs are to be checked and outputs updated, the update will take 8ms, 4 to read inputs and 4 to write outputs, plus processing time by the host.

The total time should be less than 10ms. To keep the speed as high as possible, no acknowledgement is returned to the host from the i/o processor. All the work is done by the *PI16C55* microprocessor. The processor acts only on valid commands, and recovers automatically when a valid sequence is detected, therefore no reset button is needed. Any errors in transmission or invalid command sequence will switch on the error led. The error led will go off when a valid character is received.

RS232 receive and transmit signals are converted to ttl level by the *MAX232*, which needs a single 5V supply. All inputs and outputs are ttl or 5V c-mos compatible. To drive outputs at a higher voltage, one of the driver circuits may be used, **Fig. 2**.

Inputs may be via opto isolators, volt-free contacts, or voltage sources connected to input terminals through current limiting resistors, **Fig. 3**.

The i/o processor can be controlled by any device capable of sending and receiving ascii characters in RS232 format at 9600, 7, N, 2. To send output commands from a pc, at the dos prompt, type *mode com1 9600,e,7,2* and press enter. Then type *copy con com1* and press enter. Next type one of the i/o processor output commands, eg *o=5a*, then press function key F6 followed by the enter key. As a result $5A_{16}$ will be written to the outputs. Function key F6 terminates the dos copy command.

The C program below can be used to communicate with the i/o processor. It sets COM1 parameters to 9600,7,N,2 and sends anything typed to the serial port, and displays anything received from the serial port.

When used with a pc with nine-pin serial

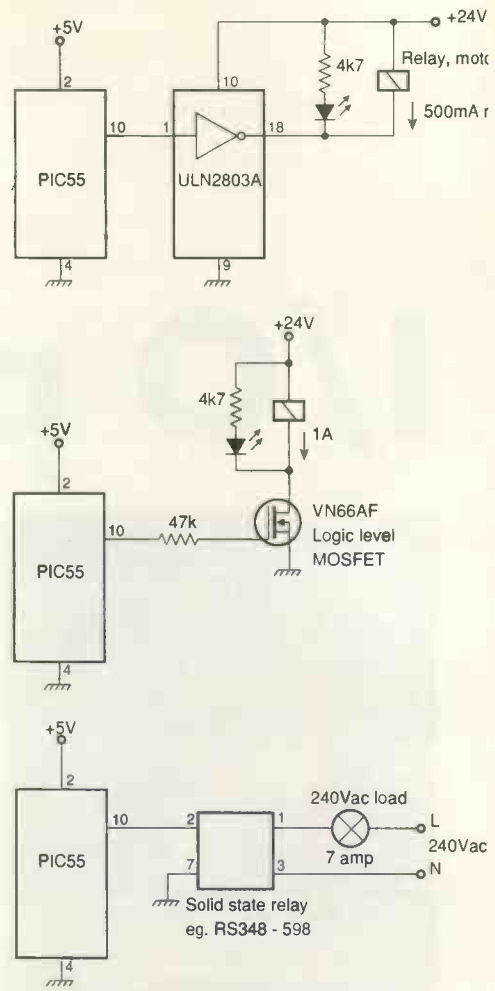

Fig. 2. All inputs and outputs are ttl or 5V c-mos compatible. To drive outputs at a higher voltage, one of these driver circuits may be used.

Object code for the PIC universal RS232 i/o processor.

```
:080000000C09000505250C00000600660CFF00072A
:0800080000680800 0C0E0A0E0C1D0A0E002B02EBF5
:08001000 0A0F080000300C47009006030A230C4131
:0800180000900603 0A250C3A009006030A230C30D0
:0800200000900603 0A250503080004030800 0C30B5
:080028000B00C0A009007030A300C0700B008006B
:080030000800 0C0A009007030A370C0701F00C308F
:080038001F0080000300C61009006030A4105033E
:080040000800040308000C07002A0425090C0329FA
:0800480007030A4C05250A4D0425090C02EA0A4754
:0800500005250 90C090C080009000A5705450C0C80
:08005800024070 50A5906050A5B090A06050A591C
:080060000 90A090A0C07002A04030605050 30328F0
:0800680009 0C02EA0A64040303280C4F01880643C2
:08007000 0AAB0C6F018807430A780C2000A80AAB7A
:08007800 0C49018806430AAB0C69018807430A83CF
:08008000 0C2000A80AAB0C3D018806430A990C2104
:0800880001880643 0A990C3F018806430A99020831
:08009000093A06030A950C2000A8020809120 6037B
:08009800 0A56044502080020 02A40C100DE0018459
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:0800A8000 6430B130A5604450C0C00240208 0020DA
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:0800C800020F003009270210002F020E0030040337
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:0800D800 0C38008D06030A560C30008D07030A56B3
:0800E000 0C30018F06430AEC0C31018F06430AEC01
:0800E800 0C21018F07430A560C3000AD02AD0C30D5
:0800F000018F06430B090C31018F06430B000503F2
:0800F800007003700 0ED07430AF9021001A60A57C9
:08010000050300700370 00ED07430B02021001268F
:08010800 0A5704030CFF00300370 00ED07430B0C8B
:0801100002100166 0A570C3D018D06430B1C0C3D7D
:08011800018E06430B3B0A560C3F018E07430A56DD
:08012000 0C3F018F07430A5602070031003004 03E1
:0801280003300330033003300C0F0170093102102B
:0801300002909430211003 00C0F017009310 21037
:080138000290943 0A570C3F018F07430A560C3820
:08014000 08D06030A560C30008D07030A560C3052
:0801480000AD02AD020700310 33102ED0B4C060396
:07015000 0B530C300B540C3100290943 0A579C
:0101FF000A54A1
:00000001FF
```

Simple terminal emulation program written in Turbo C. It sets up COM1 for 9600, 7,N,2,sends typed characters to COM1 and displays received characters.

```
#include <bios.h>
#include <stdio.h>
#include <conio.h>

#define DATA_READY 0x100
#define ESC '\x1b'
#define SETTINGS ( 0xe0 | 0x02 | 0x00 | 0x04)        // 9600, 7, N, 2

void main(void)
{
    int char_in, key, status;

    bioscom(0, SETTINGS, 0);
    printf("TERMINAL EMULATION AT 9600, 7, N, 2. [ESC] to exit ...\n");

    while (1) {                          // Loop forever
        status = bioscom(3, 0, 0);
        if (status & DATA_READY)         // Check for character in
            if ((char_in = bioscom(2, 0, 0) & 0x7F) != 0)
                putch(char_in);          // Display it

        if (kbhit()) {                   // Any key pressed ?
            if ((key = getch()) == ESC) exit();    // ESC = Exit to DOS
                bioscom(1, key, 0);      // Send it out
        }
    }
```

Software and programming services

Assembly-language listings for the RS232 universal i/o processor can be obtained on a pc formatted disk by sending £11.50 including postage and vat to *EW+WW* Editorial, Quadrant House, The Quadrant, Sutton, Surrey SM2 5AS. Please make cheques payable to Reed Business Publishing and mark your envelope 'RS232 processor'. Don't forget to include your address.

Hamid is supplying programmed PIC controllers for £12 each fully inclusive. Send a postal order or cheque payable to Hamid Mustafa at Rosslare Strand, Co. Wexford, Ireland.

connector, link pins 7-8 and 4-6, connect pin 3 (Tx) to pin 13 of *MAX232*, pin 2 (Rx) to pin 14 of MAX232 and pin 5 to ground.

If the pc has a 25-pin serial connector, link pins 4-5, 6-20, and connect pin 2 (Tx) to pin 13 of *MAX232*, pin 3 (Rx) to pin 14 of *MAX232*, and pin 7 to ground. ■

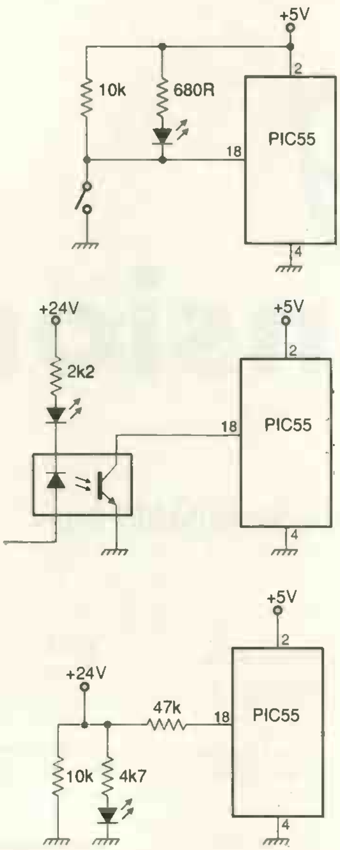


Fig. 3. Inputs may be via opto isolators, galvanically-isolated contacts, or voltage sources connected to input terminals through current limiting resistors.

Designing pc expansion

Dave Robinson runs through the steps needed to design a programmable-logic based interface for controlling i/o via a pc expansion slot.

Here, I outline how to design a general purpose segment of a board, concentrating on the way the unit interfaces into the ISA bus. The interesting bit of the circuit design – turning the control signals into useful i/o – I leave to you.

When designing add on boards, you have two options for interfacing them – memory mapping or i/o mapping. Memory mapping makes the board appear as a segment of system memory. With some processors, such as the Motorola 68 series, this is the only option available.

While memory mapping is fine when you have total control of how the memory resource is distributed – as in the case of designing an embedded system – it is more difficult to accomplish safely in a computing system like the pc. If the software you are running expects to find memory in locations that you have allocated to your function card, then all kinds of problems can occur. My advice is, unless you have a good reason for using memory mapping in this context – don't do it.

Input/output mapping is the recommended method of interfacing to function cards. Whenever an i/o instruction is issued by the pc processor chip, it places a 16bit address on the address bus. This may be qualified by the i/o read signal going active if the cpu wants the peripheral to supply the data. Alternatively, if the processor is giving data to the peripheral then the processor activates the i/o write signal.

The peripheral must monitor both the address and i/o control lines continuously. If it recognises that the transaction is aimed at it – i.e. it recognises its own address – then it must respond. The pc has a number of i/o mapped peripherals built into the mother board, such as RS232 interfaces; dma controllers and printer ports. To allow the system to differentiate between these internal peripherals and peripherals plugged into the ISA bus, IBM defined the following protocol.

If an i/o instruction is issued by the cpu that has the tenth address bit, A_9, set to a zero then no card on the ISA bus may claim it. When low, A_9 specifies that the peripheral being addressed is mounted on the motherboard, and not to any add-in peripheral. Conversely if an i/o instruction is issued with A_9 high then it is aimed at an add-on card plugged into the expansion facilities.

In **Table 1**, the first row indicates the state of the address bus whenever an internal peripheral is accessed. The second indicates that a peripheral card in an ISA slot is expected to respond. Normally address bits A_{10} upward are unused, while $A_{0\text{-}8}$ define the card and its register.

It is necessary to be able to uniquely define your function board from any other plugged into the ISA bus. Failure to do so results in bus contention – reading from or writing to two cards at once – and the computer will probably behave unpredictably.

To avoided contention, it is good practice to provide your function card with a modifiable address. I almost always define address lines $A_{5\text{-}8}$ to be the board identification address. The address that the board responds to can then be determined by a set of four switches or links.

Address lines $A_{0\text{-}4}$ provide local identification of up to 32 registers on the card. If this isn't enough then the upper address lines $A_{10\text{-}15}$ can be called into action.

Power precautions

Modern pcs are equipped with large power supplies, capable of supplying 20A or more at 5V. Wiring a short circuit between a power line and ground, or even a solder splash across the power lines, could cause a catastrophic failure.

Chances are the wire you use to connect your circuitry is going to have a greater current carrying capacity than the pc traces on the mother board. The result will almost certainly be a pc-track burn out, and your pc may well be ruined. Similarly, polarised capacitors have a nasty habit of catching fire when inserted back to front.

However, if you follow this tried and tested procedure, such problems are highly unlikely.

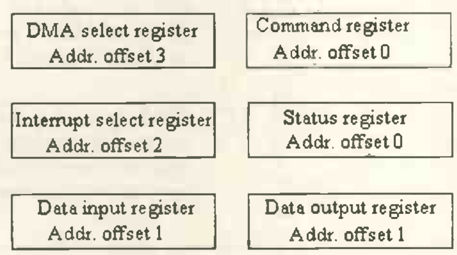


Fig. 1. Programmer's model of a pc interface card helps visualisation of the card's functions when writing the control software.

Board specification

The example described comprises of an 8bit i/o-mapped peripheral consisting of nothing more than an 8bit input first in first out memory, fifo, and a similar output fifo. Whether you are building a data acquisition system or a communication controller, all you need to do is connect any

Table 1. First row indicates state of the address bus when an internal peripheral is accessed. Second indicates that a peripheral card in an ISA slot is expected to respond.

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
x	x	x	x	x	x	0	?	?	?	?	?	?	?	?	?
x	x	x	x	x	x	1	?	?	?	?	?	?	?	?	?

input into one fifo and to extract any output from the other.

In order to explain how to handle interrupts, I will design the board so that the fifos will create an interrupt when they are half full. To help explain how to control a direct-memory-access, dma, channel, I will construct the system so that data can be deposited into, or extracted from the fifos under dma control.

Interrupt and dma channels will be software selectable at initialisation, and the interrupt operation will be configured to be optional. Data can also be extracted/deposited into the fifos by either dma or via straight forward i/o instructions. The i/o address of the board will be selected by means of four switches for the reasons mentioned earlier.

Now define what the board is going to look like with respect to the software, i.e. specifying the user interface, **Fig. 1**. This diagram shows that the programmer has access to six registers. In my design they are either read only or write only. You may prefer to use read back registers. If you do, you will not be able to use the same address for read and write only registers in the way that I have.

The address is specified in terms of an offset. This is because at this stage, the address that will be assigned to the board is not usually defined. Suppose the DIP switches are used to select address $0x300_{16}$. Writing to i/o port $0x300_{16}$ will deposit a value into the command register. Similarly reading i/o port $0x300_{16}$ will result in the board status being read. Reading port $0x301_{16}$ will pop a value from the input fifo. Writing to the same address pushes a value into the output fifo.

One of the two remaining registers holds the channel that the board is to use when operating under interrupt mode. The other holds information regarding which dma channel the input and output channels will use when operating in direct memory access mode. Note that these cannot share an address since they are both write only.

Having allocated the addresses to the overall functional registers, contents of the individual registers must defined, **Table 2**.

Reset 1 is an active low signal. Writing a zero to it causes contents of the input fifo to be dumped, even though they have not been read by the pc. You must write a one back into this position in order that your circuitry can start to deposit data into the fifo.

Reset 2 is active low. Writing a zero to this position causes contents of the output fifo to be dumped, even though they have not been read by your circuitry. You must write a one back into this position so that the pc can start to deposit data into the FIFO.

Intr 1 is an active-high interrupt enable for the input signal. If a zero is written into this location then no interrupt will be given when the input fifo reaches half full. If a one is written, then the interrupt will be presented to the pc. on the software selected channel.

Intr 2 is the same as Intr 1, except that it operates on the output fifo.

Intr 3 allows the board to monitor the state of the pc dma controllers terminal count. If the pc has either received the required number of bytes or transmitted the required number of byte, then it activates the terminal count signal. If Intr 3 is set to zero nothing happens; if it is set to 1 then the board will produce an interrupt.

Note that all three sources of interrupt activate the same selected interrupt line. It is the job of the interrupt handler to identify which situation caused the interrupt by reading the status register.

DMA 1 is an active high signal that activates a dma request on the situation where space is available in the output fifo. If DMA 1 is set to zero nothing happens, if it is set to one then the board will produce an dma request.

Seven of the eight bits in this register have now been allocated. If your application needs more bits – for example you may have an input multiplexer that needs setting, or a programmable gain amplifier that needs to be configured – then all you have to do is include another command register, by modifying the programmer's model.

Table 2. PC command register bit definitions.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused	DMA 2	DMA 1	Intr 3	Intr 2	Intr 1	Reset 2	Reset 1

Table 3. Status register bit functions.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T.C. 2	T.C. 1	Full 2	Halffull 2	Empty 2	Full 1	Halffull 1	Empty 1

Status register requirements

Table 3 shows bit functions of the status register.

Empty 1 is an active low flag indicating that there is no data in the input fifo. If this bit read a 1 on interrogating this register it indicates that the fifo contains at least one byte of data.

Halffull 1 is an active low signal that indicates that the input fifo is full to half or more of its capacity.

Full 1 is an active low signal that indicates that the input fifo has been filled to capacity. This situation should be avoided, as it could mean that data has been actually lost.

The next three bits are identical flags belonging to the output fifo.

TC 1 reflects the state of the pc terminal count state, corresponding to the input fifo. It goes to a logic one when the pc has received all of the data that it is expecting from the input fifo.

TC 2 reflects the state of the pc terminal count state, corresponding to the output fifo. It goes to a logic one when the pc has transmitted all of the data that it is expecting from the input fifo.

Note that the TC signals are generated by the dma controller in this case by logically combining the TC signal from the ISA bus together with the relevant dma acknowledge signal.

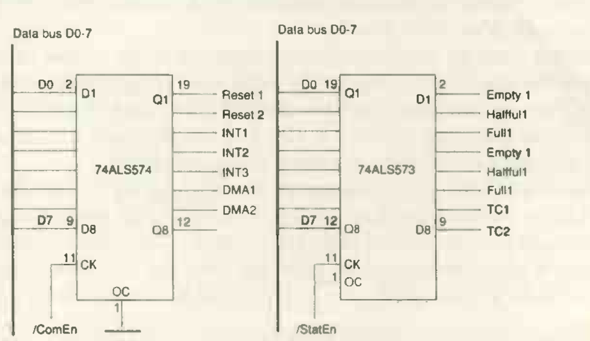
The status register has three primary purposes, these are:-

- Enables the board to be used without interrupts or dma.
- Allows the interrupt handler to recognise the interrupt source.

- The interrupt handler reading this port causes the board to remove its interrupt request.

The first option allows the board to be used in an entirely software polled mode. The control program can be written so that all interrupts and dma transfers are disabled by writing the required bit pattern into the control register. The software then sits in a software loop reading the status register. If the empty flag on the input fifo goes inactive (i.e. there is data available), then the software reads it. Similarly if the full flag on the output fifo goes inactive then it is safe to put data in the fifo.

The second and third option are tied in with the way that the ISA bus implements its interrupt control. Whenever a ISA bus peripheral requires servicing, it pulls its interrupt line active. However there is no mechanism to indicate that the interrupt is being serviced, so it is essential that the hardware designer includes some software mechanism that can be instigated from the interrupt handler that will remove the inter-



Implementing command and status registers is simply a matter of connecting LS series ICs to the data bus and applying enables.

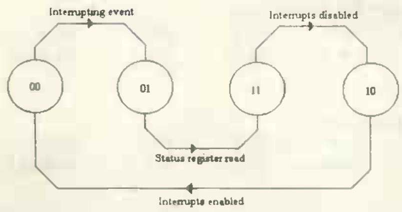


Fig. 3. State-machine structure adopted for the . Binary numbers within the circles represent the state variables

Table 4. Interrupt-select register bits. This register allows the programmer to select the desired interrupt channel via software.

Bit 2	Bit 1	Bit 0	Int. ch. selected
0	0	0	None
0	0	1	None
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Table 5. DMA select register functions. This register allows software selection of the required DMA channel.

Bit 3	Bit 2	Bit 1	Bit 0	DMA channel
x	x	0	0	None
x	x	0	1	Channel 1
x	x	1	0	Channel 2
x	x	1	1	Channel 3
0	0	x	x	None
0	1	x	x	Channel 1
1	0	x	x	Channel 2
1	1	x	x	Channel 3

rupt request flag.

I have chosen a read from the status register to accomplish this task. Note that it is necessary for the software to take into account that there may be two or more interrupts pending, and the interrupt request will vanish when the status register is read. This is because all the interrupting sources produce the same interrupt. As a result, reading the status register could indicate that the input fifo had reached half full *and* that the output fifo dma transfer had terminated. Both situations should be dealt with from the one interrupt request.

Input data register. This is a simple 8bit data port. A read from this location, or a single byte dma transfer will result in the output value in the fifo being read into the pc and replaced by any subsequent value.

Output data register. This is a simple 8bit wide data port. A write to this location, or a single byte dma transfer, will result in another value being pushed into the output fifo. Note that if the output fifo is already full when this operation is undertaken, will lead to the data simply being lost. *It is not possible to deposit data into a full FIFO.*

Interrupt-select register. The interrupt-select register allows the programmer to select whatever interrupt channel to use via a software command. Note that this is not the only way of achieving interrupt-channel selection. Many boards accomplish the same task by using either a hardware DIP switch or link option to route the required interrupt channel. Both methods work superbly; you must decide whether mechanical setting or software selection is the better option for your own application, **Table 4**.

Note that interrupts on the first two channels are used by the pc system itself. If you experiment with them, your computer will become unstable. Consequently there is no access to these interrupts via the ISA bus. Selecting these forbidden channels is identical to disabling interrupts via the command register; which is the preferred way of doing it.

When allocating interrupt channels it is up to you to select a vacant channel that is not being used by any other hardware in your system.

DMA select register. The dma select register allows the programmer to select a dma channel via a software command. Note that this is not the only way of achieving dma channel selection.

Many boards accomplish the same task by using either a hardware DIP switch or link option to route the required dma channel. Both methods work superbly; you must decide whether mechanical setting or software selection is the better option for your application, **Table 5**.

At this stage, you have control of the dma channels required for both the input and output fifos. These are totally independent. However there are two things to note. You cannot use channel 0, as this is used by the pc in connection with ram refreshing. Indeed although the dma acknowledge signal is distributed to the ISA bus, the corresponding request line is not accessible. Consequently selecting that channel is equivalent to disabling the dma transfer via the command register – the preferred method.

Secondly, you cannot use the same channel on both the input and output fifo simultaneously. The dma controller is configured to transfer a given number of bytes in a specified direction, so cannot be used to read and write.

When allocating dma channels it is up to you to select a vacant channel that is not being used by any other of your hardware in your system.

Designing decoding logic

Design of the board decoding logic is the first step. At the top level, the

Anatomy of an 8bit expansion card

The eight bit expansion card was the first type available. You have around 12.5in by 3.5in of usable area on which to construct your circuit. Power and processor interface signals are provided by the 62 contact gold-plated edge connector at the edge of the board.

In many cases the connector used to interface with the outside world can be used as the mounting structure for the metal fixing plate. Various types of blank fixing plates are available. These are standard plates, some of which are already punched to take stock connectors. Others come equipped with pc mounting lugs, and some are ideal for mounting via the connector.

The signals to the edge connector are as in the table on the right. Signals prefixed by an exclamation mark are active low while the remainder are active high. Power lines are marked in quotation marks. Note that the sense of the signal type is with reference to your expansion card. The signal Osc is supplied by the computer to your board, whereas Irq3 is supplied by your board to the computer.

Data lines are of course bi-directional, and can source and sink data.

Signals to the edge connector are as follows.

Solder side		Access Sig.type	Panel Sig.type	Component side	
B1	Gnd	Power	Output	!IO chck	A1
B2	RESET	Input	I/O	D7	A2
B3	'+5V'	Power	I/O	D6	A3
B4	Irq2	Output	I/O	D5	A4
B5	'–5V'	Power	I/O	D4	A5
B6	Drq2	Output	I/O	D3	A6
B7	'–12V	Power	I/O	D2	A7
B8	Reserved		I/O	D1	A8
B9	'+12V'	Power	I/O	D0	A9
B10	Gnd	Power	Output	IO chrdy	A10
B11	!Memw	Input	Input	AEN	A11
B12	!Memr	Input	Input	A19	A12
B13	!IOw	Input	Input	A18	A13
B14	!IOr	Input	Input	A17	A14
B15	!DAck3	Input	Input	A16	A15
B16	Drq3	Output	Input	A15	A16
B17	!DAck1	Input	Input	A14	A17
B18	Drq1	Output	Input	A13	A18
B19	!DAck0	Input	Input	A12	A19
B20	Clock	Input	Input	A11	A20
B21	Irq7	Output	Input	A10	A21
B22	Irq6	Output	Input	A9	A22
B23	Irq5	Output	Input	A8	A23
B24	Irq4	Output	Input	A7	A24
B25	Irq3	Output	Input	A6	A25
B26	!DAck2	Input	Input	A5	A26
B27	T/C	Input	Input	A4	A27
B28	Ale	Input	Input	A3	A28
B29	'+5V'	Power	Input	A2	A29
B30	Osc	Input	Input	A1	A30
B31	Gnd	Power	Input	A0	A31

decoder is simply a logic block which takes in the address bus from $A_{0\text{-}9}$ and the two i/o strobes !IORd and !IOWr. It also requires the four address switch inputs which change the allocated board address; and vitally important is the signal AEN which is provided on the ISA bus. This signal becomes active during a dma cycle, as does the i/o strobes.

During this phase however the address on the address bus relates to the memory location in which the data to/from the i/o board is to be deposited. Hence decoding during this phase can lead to problems. *The decoder must be disabled while the AEN signal is active.*

The simplest way to implement the decoder is via an epld. This way the complete decoder can be implemented on one chip. An AMD *MACH110* costing around £8 is suitable; Electromail supplies these, together with the Palasm software needed to compile the Boolean equations, and also offers a programming service.

Software is shown in **List 1**. Just a few words of explanation are needed. Signals beginning with a lower case 'n' are active low signals. the forward slash (/) is a logical inversion, the asterisk (*) is equivalent to an 'AND' gate, and the plus (+) is the logical OR operator. If you don't have access to the relevant epld programmers, or want to do it using standard ttl or cmos chips, converting the equations into a circuit diagram is relatively trivial Make sure that your gate delays do not become excessive.

Command register design

Designing the command register is easy. All you need is an octal latch, connected directly to the ISA data bus. One of the *74HC574* or *HCT574* type will suffice here, as there is no real timing problem.

Output enable of the chip should be tied active, **Fig. 2**, as there is never any situation where the command register needs to be tristated off. The command register enable signal can be used directly as the chip clock signal. The device clocks on a low-to-high transition, which will occur as the !IOWr signal from the ISA bus deactivates. The chip itself has a zero hold time so the timing pans out correctly.

Status-register considerations

The status register can be implemented as simply as the command register, using just one chip. However this time use a *74x573* transparent octal latch.

Outputs of the chip connect to the ISA bus data lines, and both the latch enable and the tri-state control are connected directly to the status latch enable signal. Normally in an un enabled state the output of the latch will be in a high impedance state, but the latches themselves will be 'transparent'.

Immediately after status register is accessed the inputs get latched. This ensures that the outputs remain stable during the duration of the read process, and that outputs of the latch get enabled onto the data bus allowing the pc to read the status of the board. Once the access is over the latch resumes its high impedance transparent mode again waiting for the next access.

Interrupt controller design

From a hardware point of view, handling interrupts is slightly odd – especially if you are used to designing much closer to your cpu.

The first thing you will notice when scanning down the signals on the ISA bus connector is the absence of any form of interrupt acknowledge signal. Within the interrupt handler, the software must access an i/o port that the interrupting board will recognise as an 'interrupt acknowledge'. In response, the hardware removes the interrupt request.

In this example, one obvious choice is to use the status register read for this purpose. Because we have several sources of potential interrupt coming from our board, the interrupt handler will need to know which is the active source(s). It does this by interrogating the status register.

So arranging this read to also be interpreted as the interrupt acknowledge we can substantially increase the efficiency of our board and its associated interrupt handler.

There is a slight complication with this design example, that may not be present with any future board you may be designing. Consider that during the interrupt latency period – which could be many milliseconds if you are running under Windows – the fifo receives a very fast burst of data, virtually filling it up. As soon as the software exits the interrupt

Listing 1. Pal assembly code for logic needed to produce a pc address decoding chip.

```
;PALASM Design Description
;———————— Declaration Segment ————
TITLE ISA Board decoding PAL
PATTERN DCODE1
REVISION 0.0
AUTHOR Dave Robinson
COMPANY
DATE 03/05/95
CHIP_dcode1 MACH110
;———————— PIN Declarations ————
PIN     1     Gnd       ;
PIN     2     A0        ;INPUT
PIN     3     A1        ;INPUT
PIN     4     A2        ;INPUT
PIN     5     A3        ;INPUT
PIN     6     A4        ;INPUT
PIN     7     A5        ;INPUT
PIN     8     A6        ;INPUT
PIN     9     A7        ;INPUT
PIN     10    A8        ;INPUT
PIN     11    A9        ;INPUT
PIN     12    Gnd       ;
PIN     13    NC        ;
PIN     14    Switch0   ;INPUT
PIN     15    Switch1   ;INPUT
PIN     16    Switch2   ;INPUT
PIN     17    Switch3   ;INPUT
PIN     18    AEN       ;INPUT
PIN     19    nIORd     ;INPUT
PIN     20    nIOWr     ;INPUT
PIN     21    NC        ;
PIN     22    Vcc       ;
PIN     23    Gnd       ;
PIN     24    nComEn    ;OUTPUT
PIN     25    nStatEn   ;OUTPUT
PIN     26    nPOPEn    ;OUTPUT
PIN     27    nPUSHEn   ; OUTPUT
PIN     28    nIntrEn   ;OUTPUT
PIN     29    nDMAEn    ;OUTPUT
PIN     34    Gnd       ;
PIN     36    nISME     ;OUTPUT
PIN     40    Dummy0    ;OUTPUT
PIN     41    Dummy1    ;OUTPUT
PIN     42    Dummy2    ;OUTPUT
PIN     43    Dummy3    ;OUTPUT
PIN     44    Vcc       ;
;————————PLD Description————————
; This PLD provides the main decode logic for use with the demonstration ISA board. It takes in from ;the ISA BUS the address signals A0 –> A9 and logically combines them with a valid !IORd and ;!IOWr signal to form the correct enable signals.
; The decoding is done in two stages. First the address bits A5 –> A8 are compared with the switch ;settings to insure that the i/o instruction is targeted at this board. (Note that the comparison ;generates some intermediate logic values called Dummyi. These are never used on the outside of the ;PLD but do not represent spare capacity). An address match during a valid i/o instruction leads to ;the generation of an active low 'ISME' signal. Subsequent decoding takes the valid ISME signal, and ;combines this with the lower parts of the address A0 –> A4 and the data direction, obtained from ;!IORd and !IOWr to form the active; low register enable signals
;———— Boolean Equation Segment ————
EQUATIONS
; Checks if A5 and Switch0 are both equal
        Dummy0   =        Switch0 * A5   ;Address and switch both high
        + /Switch0 */A5                  ;Address and switch both low
; Checks if A6 and Switch1 are both equal
        Dummy1 =    Switch1 * A6   ;Address and switch both high
        + /Switch1 */A6   ;Address and switch both low
; Checks if A7 and Switch2 are both equal
        Dummy2 =    Switch2 * A7   ;Address and switch both high
        + /Switch2 */A7   ;Address and switch both low
; Checks if A8 and Switch3 are both equal
        Dummy3 =    Switch3 * A8   ;Address and switch both high
        + /Switch3 */A8   ;Address and switch both low
; Now forms the board address recognition signal nISME
        /nISME =    A9               ;Must be high for valid ISA transfer
                    * Dummy0         ;Switch0 matches A5
                    * Dummy1         ;Switch1 matches A6
                    * Dummy2         ;Switch2 matches A7
                    * Dummy3         ;Switch3 matches A8
                    * (/nIORd+/nIOWr)   ;Valid IO Instruction recognised
                    * /AEN           ;Not a DMA transfer
; Now forms the individual enable signals
;1) Command register Enable at offset &000 write only
        /nComEn =   /nISME                     ;This board recognised
                    * /A4*/A3*/A2*/A1*/A0      ;Offset &000
                    * /nIOWr                   ;ISA bus supplying data
;2) Status register Enable at offset &000 read only
        /nStatEn =  /nISME                     ;This board recognised
                    * /A4*/A3*/A2*/A1*/A0      ;Offset &000
                    * /nIORd                   ; ISA bus requesting data
;3) Push data into the output fifo at offset &001 write only
        /nPUSHEn =  /nISME                     ;This board recognised
                    * /A4*/A3*/A2*/A1* A0      ;Offset &001
                    * /nIOWr                   ;ISA bus supplying data
;4) Pop data from the output fifo at offset &001 read only
        /nPOPEn =   /nISME                     ;This board recognised
                    * /A4*/A3*/A2*/A1* A0      ;Offset &001
                    * /nIORd                   ;ISA bus requesting data
;5) Interrupt selection register Enable at offset &002 write only
        /nIntrEn =  /nISME                     ;This board recognised
                    * /A4*/A3*/A2* A1*/A0      ;Offset &002
                    * /nIOWr                   ;ISA bus supplying data
;6) DMA selection register Enable at offset &003 write only
        /nDMAEn =   /nISME                     ;This board recognised
                    * /A4*/A3*/A2* A1* A0      ;Offset &003
                    * /nIOWr                   ;ISA bus supplying data
;————————————————————————————
```

Listing 2. Design specification for the interrupt controller PAL.

```
;PALASM Design Description
;————— Declaration Segment —————
TITLE    interrupt controller
PATTERN  INTCON1.PDS
REVISION 0.0
AUTHOR   Dave Robinson
COMPANY
DATE     03/12/95
CHIP  _intcon1  PALCE26V12
;————— PIN Declarations —————
PIN    1    nIntrEn                ;INPUT
PIN    2    D2                     ;INPUT
PIN    3    D1                     ;INPUT
PIN    4    D0                     ;INPUT
PIN    5    Intr3                  ;INPUT
PIN    6    Intr2                  ;INPUT
PIN    7    Vcc
PIN    8    Intr1                  ;INPUT
PIN    9    Halffull2              ;INPUT
PIN    10   Halffull1              ;INPUT
PIN    11   TC2                    ;INPUT
PIN    12   TC1                    ;INPUT
PIN    13   nStatEn                ;INPUT
PIN    27   Intr_Pending           COMBINATORIAL
;OUTPUT
PIN    26   A          COMBINATORIAL    ;OUTPUT
PIN    25   B          COMBINATORIAL    ;OUTPUT
PIN    24   IntSel2    REGISTERED       ;OUTPUT
PIN    23   IntSel1    REGISTERED       ;OUTPUT
PIN    22   IntSel0    REGISTERED       ;OUTPUT
PIN    21   Gnd
PIN    20   Intreq7    COMBINATORIAL    ;OUTPUT
PIN    19   Intreq6    COMBINATORIAL    ;OUTPUT
PIN    18   Intreq5    COMBINATORIAL    ;OUTPUT
PIN    17   Intreq4    COMBINATORIAL    ;OUTPUT
PIN    16   Intreq3    COMBINATORIAL    ;OUTPUT
PIN    15   Intreq2    COMBINATORIAL    ;OUTPUT
;————— PLD Description —————
;This PAL provides all of the interrupt control logic for use with
;demonstration ISA BUS board. It takes the signals D0 -> D2 from
;the ISA BUS, and the decode signals nStatEn and nIntrEn from the
;decoding PLD (DCODE 1). The terminal count signals TC1 and TC2 are
;generated by the DMA controller, whilst the half full flags are obtained
;from the fifo's. The interrupt enables are obtained from the command
;register.
;The PLD registers the three data bits on the rising edge of nIntrEn
;when these bits contain the required interrupt request pin to be used.
;It generates the interrupt pending flag whenever any of the interrupting
;states are true and enabled.
;It provides a simple four state state machine to handle the interrupt
;request generation as described in the text.
;All unselected interrupt channels are tristated off.
;————— Boolean Equation Segment —————
EQUATIONS
; Forms the interrupt register
IntSel2 :=        D2
IntSel1 :=        D1
IntSel0 :=        D0
; Generates the Interrupt pending flag
        Intr_Pending = Halffull1 * Intr1
                     + Halffull2 * Intr2
                     + TC2      * Intr3
                     + TC1      * Intr3
; Implements the state machine for interrupt generation
        A            = /A*/B*Intr_Pending
                     + A*/B
                     + A* Intr1
                     + A* Intr2
                     + A* Intr3
        B            = A*/B*/nStatEn
                     + A* B*/Intr1*/Intr2*/Intr3
; Generate interrupt request signals
        Intreq7      = IntSel2 * IntSel1 * IntSel0 * A */B
        Intreq7.trst = IntSel2 * IntSel1 * IntSel0
        Intreq6      = IntSel2 * IntSel1 */IntSel0 * A */B
        Intreq6.trst = IntSel2 * IntSel1 */IntSel0
        Intreq5      = IntSel2 */IntSel1 * IntSel0 * A */B
        Intreq5.trst = IntSel2 */IntSel1 * IntSel0
        Intreq4      = IntSel2 */IntSel1 */IntSel0 * A */B
        Intreq4.trst = IntSel2 */IntSel1 */IntSel0
        Intreq3      =/IntSel2 * IntSel1 * IntSel0 * A */B
        Intreq3.trst =/IntSel2 * IntSel1 * IntSel0
        Intreq2      =/IntSel2 * IntSel1 */IntSel0 * A * /B
        Intreq2.trst =/IntSel2 * IntSel1 */IntSel0
;—————————————————
```

handler, it would receive another interrupt. Bear in mind that the he fifo is still more than half full. The pc would essentially become interrupt bound, spending all its time dealing with the interrupts being sent to it.

To overcome this potential problem it can be arranged that reading the status register effectively turns off the interrupt-enable signals within the command register. After receiving confirmation that the first interrupt from the board is recognised, the interrupts from the board are automatically disabled and need re-enabling to resume.

This is a problem with many solutions. You could, for example, arrange the status read enable signal to clear the actual command register bits corresponding to the interrupt enables. However this requires a more complex command register structure than the one previously described, as not all of the command register positions need to be cleared. This is a viable solution, but the one that I have adopted makes use of a state machine structure, shown in **Fig. 3**.

Binary numbers within the circles represent the state variables, and as we have four states we need two of them. Note that they are grey coded – as opposed to being binary. As a result, only one bit is altered from each state to the next. This avoids the problem of any timing glitches. The interrupt request signal is obtained simply by forming the logic signal A*/B. Immediately after a valid interrupting event has occurred the interrupt request occurs. Then when the status register is read, the interrupt request is removed. It remains inactive until the software firstly disables the interrupt enables, and then reestablishes them.

As with the decoder, you can either build the interrupt controller from discrete ttl or programmable logic. The device I have chosen is the *PALCE26V12* from AMD. This is a stretched body *PAL22V10*, in which the controller logic fits comfortably. Should you have trouble obtaining it, then the logic equations can easily be transferred into one of the smaller *MACH* devices. The only thing to be wary of when using the *26V12* is the odd pin positions that the manufacturers have placed the power rails. (V_{cc} on pin 7, Gnd on pin 21).

Listing 2 is the design specification for the interrupt controller pal. An important aspect to note in this design is the Intreqi.trst signals. These control whether the interrupt request lines which connect directly onto the ISA BUS are operational, viz if the channel has been selected, then the driver for that request line is enabled, all others are tristated off. If you are not using interrupts then selecting channel 0 or channel 1 will ensure that all interrupt request lines are in a safe state.

DMA controller design

DMA on the pc ISA bus is slightly idiosyncratic. However its use for transferring data from an ISA peripheral device to pc memory at high speed can sometimes be invaluable. The protocol is as follows. The peripheral requires access to the pc memory – either to extract or deposit data. It does this by enabling the relevant dma request signal.

When the processor has relinquished control of the bus the peripheral receives the following indication:-

- /DACKi goes active
- AEN goes active
- /IORd or /IOWr goes active depending on data-flow direction.

Note that the address on the address bus is that of the memory location within the pc memory that is being serviced. It bears no relationship to any i/o port number on the i/o card requesting the service.

As soon as the peripheral recognises that the /DACKi matches the request line it has activated it can remove the request line. If the ISA bus is sourcing the data, then the peripheral must latch the data bus with the rising edge of /IOWr

If the ISA bus is receiving data, the peripheral tristate drivers must be enabled via /IORd. If your software has been set up to transfer a fixed size record from the peripheral, then the dma controller tells the peripheral that the transfer is complete by activating the terminal count signal.

Note that there is only one terminal count signal shared amongst all dma channels. You tell that it is 'yours' by qualifying it with the /DACKi signal. Also, there is no direct connection between the terminal count signal and the cpu in the pc. It is therefore the responsibility of the ISA bus board designer to essentially take the correctly qualified terminal count signal, and cause a processor interrupt. ■

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Frequency counting interface

On its own, even a fast pc or microprocessor is not fast enough to measure frequencies much outside the audio range. Interfacing a few ttl ics combined with a little software however increases the frequency measuring range to 25MHz and beyond, as Tony Fisher explains.

This frequency counter add on suits almost any type of computer or microcontroller. The prototype incorporates readily available and inexpensive ttl and requires only three input and three output signals to the computer or controller. Using 74LS series ttl, the minimum guaranteed operating frequency is 25MHz, but my prototype worked up to at least 30MHz –. the top of the short wave band.

A 16-stage divider produces a maximum output frequency of around 460Hz at an input of 30MHz. This 460Hz output can easily monitored by the computer. A pulse with a precise duration is needed to gate the input signal to the counter. Because of unknown quantities, such as interrupt timings and memory wait states, the computer cannot produce such a pulse.

The solution is to use the computer to generate a gate of the approximate duration and to synchronise it to a crystal controlled clock of 1kHz to give a possible gate duration of any multiple of a millisecond.

Another requirement was to keep the number of i/o pins used to a minimum so a novel method of reading the 16bit counter was required. This was easily resolved by adding a single OR gate, **Fig. 1**.

Gate timing is derived from the crystal oscillator. Its frequency is divided down to 1kHz so the gate period can be any multiple of 1ms. The 1kHz clock feeds an input pin of the computer for monitoring.

To produce a precise 1ms pulse the computer waits for the 1kHz input to go from low to high and then sets the latch-in high within the next millisecond. This is then latched on the next positive transition of the 1kHz clock. After the positive transition the latch-in is set low and synchronised with the next positive transition of the clock. A pulse with a width of any multiple of 1ms can be produced by counting a number of positive transitions of the clock before setting the latch-in low.

The frequency to be measured is passed through by the and gate and the input to the OR gate is set low during the counting phase. The lower 16 bits of the frequency is counted by hardware counters while the higher bits are kept in the computer by detecting the high to low transitions of the most significant bit of the hardware counter.

Once counting has finished, the 16 bits of the hardware counter have to be read out and reset to zero ready for the next count. This is done by taking the clock input high and low repeatedly until the most significant bit of the counter changes from high to low. The contents of the counter are then 65536 minus the number of clocks provided by the clock input.

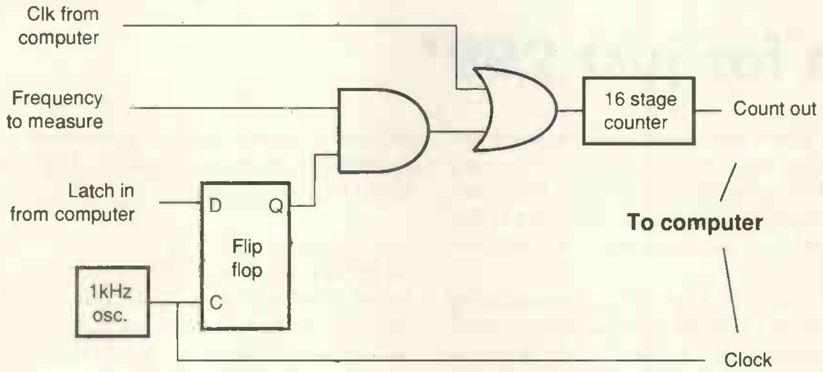


Fig. 1. Block circuitry needed for counting frequency via a pc or microcontroller. Although this configuration works, clocking the result out serially takes a long time.

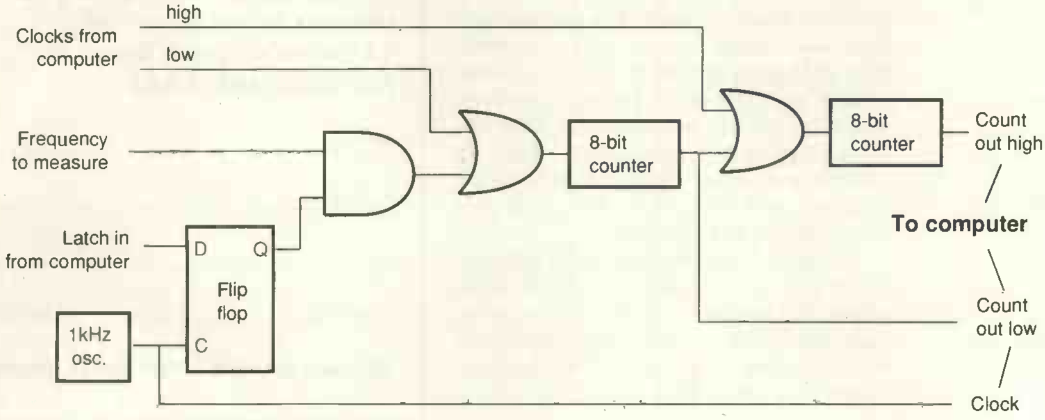


Fig. 2. Dividing the frequency count into two eight-bit chunks makes clocking the result out much quicker, at the expense of a couple of extra control lines.

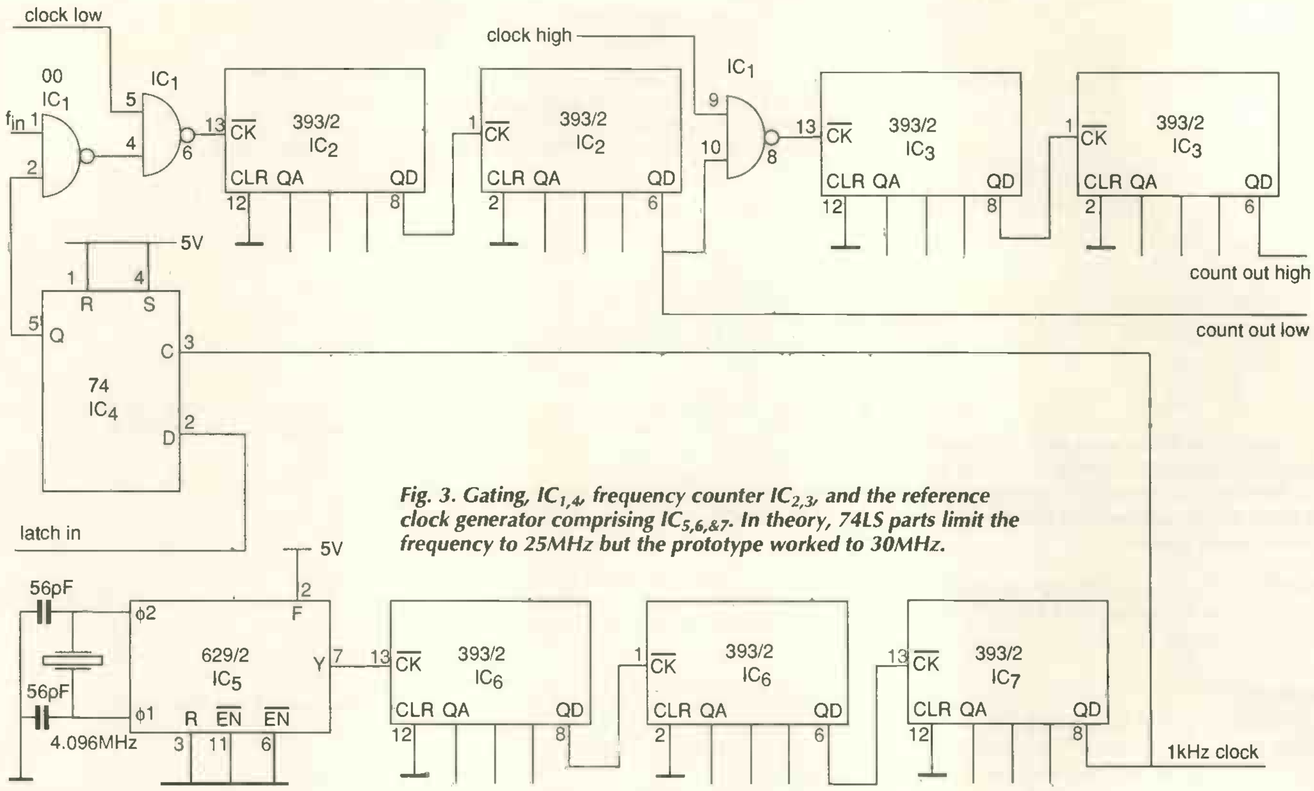


Fig. 3. Gating, $IC_{1,4}$, frequency counter $IC_{2,3}$, and the reference clock generator comprising $IC_{5,6,\&7}$. In theory, 74LS parts limit the frequency to 25MHz but the prototype worked to 30MHz.

This has the side-effect of resetting the counter to zero. For example if the counter contained 1 then 65535 pulses would be required on the clock input before the most-significant bit of the counter goes from high to low so the counter must have contained 65536–65535. A count of zero would require 65536 clock pulses. However I was felt that clocking up to 65536 times would take too long so the counter is split into two eight-bit stages. Each half can be read out independently so the number of clocks required is reduced from 65536 to 512, **Fig. 2**.

Frequency is easily determined by,

$$f(\text{in hertz}) = \frac{counter \times 1000}{gate\ time\ (\text{in milliseconds})}$$

Any frequency offset or other adjustment can be done at this stage in software, making the system versatile.

Circuitry

All the ICs are 74LS types, **Fig. 3**. In theory, the ttl parts limit the frequency to 25MHz, but in practice the circuit worked up to 30MHz. By replacing $IC_{1,2}$ with faster components higher speeds may be achievable.

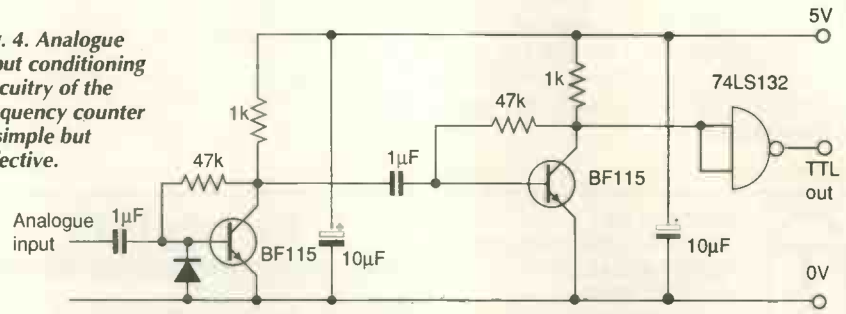
Component choice for the circuit was based on what was to hand so a reduction in component count may be possible.

Software

On reset both clock inputs are set high and the latch-in set low. The computer then waits for the clock to go from low to high. This ensures that any counting has stopped.

Contents of the counters are read back and the result discarded, this is to reset the counters so that the first frequency read is not

Fig. 4. Analogue input conditioning circuitry of the frequency counter is simple but effective.



List 1. C-like pseudo code for controlling the frequency counter interface via a pc, processor or controller.

```
/* this takes the gate period as a parameter and repeatedly
reads frequencies */
void counter(int gate)
{
/* stop counting */
clock_lo = HIGH;
clock_hi = HIGH;
latch_in = LOW;
/* wait for stop counting to take effect */
while (clock == HIGH); /* do nothing */
while (clock == LOW); /* do nothing */
/* clear contents of counter */
junk = readback_count();
while (1==1) /* do forever */
    {
    software_count = 0; /* counter bits above 16 = 0 */
    gate_remain = gate; /* number of 1 ms periods remaining */
    last_count_out_hi = count_out_hi;
    last_clock = clock;
    do
        {
        /* part to control gate timing */
        if (last_clock == LOW && clock == HIGH)
            {
            if (gate_remain > 0)
              latch_in = HIGH;
            else
              latch_in = LOW;
            gate_remain = gate_remain - 1;
            }
        last_clock = clock;
```

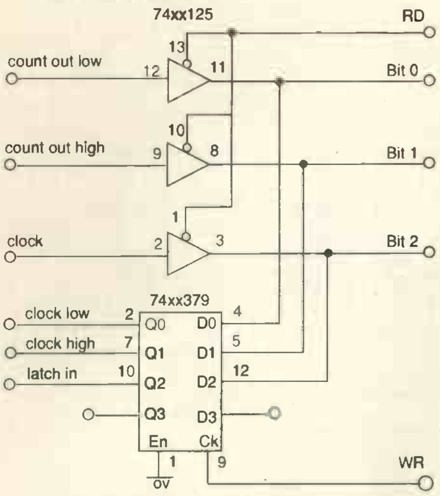


Fig. 5. Interfacing the counter to the pc needs only two gate ICs. If the counter is read by a microcontroller, the interface is even simpler since these ICs are only needed to cope with the bidirectional signals.

dependent on how the counters powered up.

Operation can be summarised by the C-like pseudo-code of **List 1**.

Interfacing

The analogue front end is standard, **Fig. 4**. To interface the meter to my pc, I used an 8-bit parallel i/o port with separate read and write signals. As you need separate input and output lines, the circuit in **Fig. 5** is required. If you use a microcontroller with dedicated i/o pins, such as the *PIC165x* or *8032*, then interfacing can be simply done by dedicating three inputs and three outputs. ■

```
            /* part to monitor counter output */
            /* if a low to high transition of the counter
            output then increment the software clock */
            if (last_count_out_hi == LOW && count_out_hi == HIGH)
                 software_count = software_count + 1;
            last_count_out_hi = count_out_hi;
            }
        while (gate_remain >= 0);
        /* combine hardware and software counts */
        readback = readback_count | (software_count << 16);
        /* now printout the readback or do something with it */
        }
}
int readback_count( void )
{
clock_hi = LOW;
clock_lo = LOW;
/* read back low 8 bits */
count_lo = 0;
last_count_out_lo = count_out_lo;
do
    {
    clock_lo = HIGH;
    finish = last_count_out_lo == LOW && count_out_lo == HIGH;
    if (!finish)
        clock_lo = LOW;
    count_lo = count_lo + 1;
    last_count_out_lo = count_out_lo;
    }
while (!finish);
/* read back high 8 bits */
count_hi = 0;
last_count_out_hi = count_out_hi;
do
    {
    clock_hi = HIGH;
    finish = last_count_out_hi == LOW && count_out_hi == HIGH;
    if (!finish)
        clock_hi = LOW;
    count_hi = count_hi + 1;
    last_count_out_hi = count_out_hi;
    }
while (!finish);

/* make a 16 bit result from two 8 bits */
return (count_hi<<8) | count_lo;
}
```

Best rf article '95

Following the success of 1994's Writers Award, ***Electronics World*** and **Hewlett-Packard** are launching a new scheme to run from January to December 1995.

Only articles which have an element of rf design will be eligible for consideration by the judging panel. It is hoped that this year's award will focus writer interest on rf engineering in line with the growing importance of radio frequency systems to an increasingly cordless world.

The aim of the award scheme is to locate freelance authors who can bring applied electronics design alive for other people.

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Technology Lag

Not all of today's electronic wizardry is as new as we think – an anomalous factor called technology lag often comes into play. Andrew Emmerson has been combing the archives with some prophetic results.

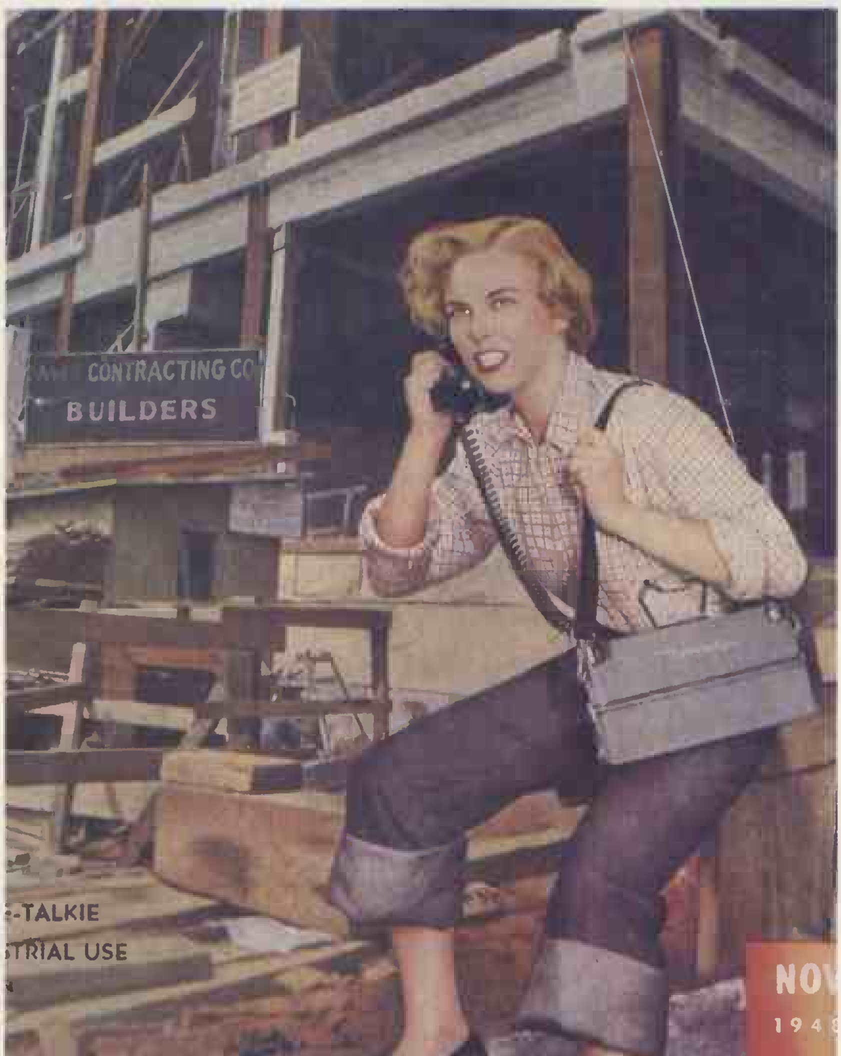
"It is conceivable that cables of telephone wires could be laid underground, or suspended overhead, communicating by branch wires with private dwellings, country houses, shops, manufactories etc., etc., uniting them through the main cable with a central office where wires could be connected as desired establishing direct communication between any two places in the city.

Such a plan as this, though impracticable at the present moment will, I firmly believe, be the outcome of the introduction of the telephone to the public. Not only so, but I believe, in the future, wires will unite the head offices of the Telephone Company in different cities, and a man in one part of the country may communicate by word of mouth with another in a distant place.

I am aware that such ideas may appear to you Utopian... Believing, however, as I do that such a scheme will be the ultimate result of the telephone to the public, I will impress upon you all the advisability of keeping this end in view, that all present arrangements of the telephone may be eventually realised in this grand system." These words are now sufficiently well known to become almost a cliche but when they were first uttered they must have sounded fanciful in the extreme. They were spoken in 1878 by Alexander Graham Bell some two years after he had invented the telephone.

"HDTV saw its first serious exploitation fifty years ago..."

Conventional wisdom of course knew better. After all back in 1865 the Boston Post had written solemnly: "Well-informed people know it is impossible to transmit the voice over wires. Even if it were, it would be of no practical value." A memo attributed to the Western Union telegraph company in 1877 took an equally prosaic attitude. "This 'telephone' has too many shortcomings to be seriously consid-



Poserphones are not new. This Motorola 'Handie-Talkie for Industrial Use' was the business back in November 1948.

Five years before the Handie-Talkie, the original Walkie Talkie was introduced – a much more cumbersome affair weighing 35 pounds.

ered as a means of communication. The device is inherently of no value to us." A similar opinion is said to have been given by someone in the British Post Office.

There is no doubt, however, that competent engineers were not afraid of forecasting their view of the future; in November 1911, A.A. Campbell Swinton, addressing the Röntgen Society in London, proposed a fully electronic television system and back in 1897 an electrical engineer by the name of Ayrton addressed the Imperial Institute in London as follows. 'There is no doubt that the day will come, maybe when you and I are forgotten, when copper wires, gutta-percha coverings, and iron sheathings will be relegated to the Museum of Antiquities. Then, when a person wants to telegraph to a friend, he knows not where, he will call an electromagnetic voice, which will be heard loud by him who has the electromagnetic ear, but will be silent to everyone else. He will call "Where are you?" and the reply will come, "I am at the bottom of the coal- mine" or "Crossing the Andes" or "In the middle of the Pacific"; or perhaps no reply will come at all, and he may then conclude that his friend is dead.'

This is all excellent stuff but it is, we must also concede, highly speculative. It is also ancient history – what about the miracles of today, such as the cellphone, high-definition television and digital techniques for interleaving several programmes on the same TV channel?

Remarkably, they are not as new as you might think and they all developed from practical work – not fanciful postulating – carried out during the second world war. That they are only reaching commercial exploitation some forty or fifty years later can be put down to technology lag.

Let's take the cellphone first: all the basic technologies were in place by the end of the war, even the concept of frequency re-use. Here is a quote from a British book of 1946, 'The Miracle of Wireless' by Miles Henslow.

Maybe it will sound a far-fetched idea today, but the time is surely approaching when everyone will be able to carry about with him a small radio telephone. War-time development of apparatus to work on very short wavelengths has opened up many entrancing possibilities. Hundred of thousands of 'radio-telephone channels' can be used over short distances without interference; and the installation of a network of automatic telephone exchanges might well be utilized for handling the calls from a multitude of pedestrian or automobile telephone subscribers, to sort them out and pass them by line – or by radio link – to main exchanges. Certainly it is but a matter of time before the railway traveller is able to pick up the phone and dial his office or his home.

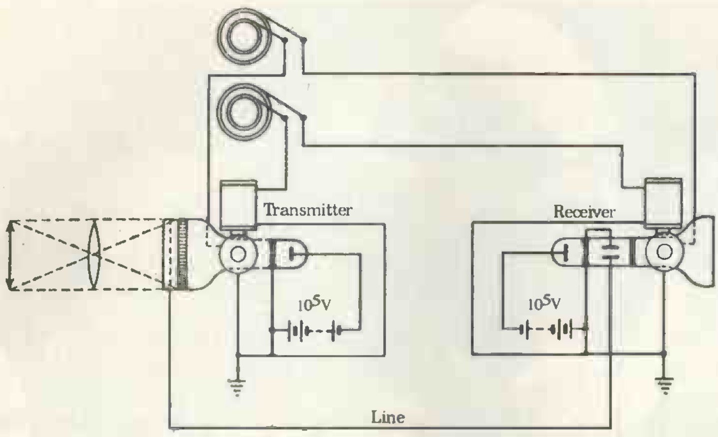
Indeed, but a matter of time – just a little under fifty years to be precise. But what were those war-time developments? Mobile radio was by no means new then: already in 1939 three vhf bands in the vicinity of 100MHz had been allocated by the Home Office to the police and fire services and tests had proved that 'two-way radiotelephone service of a good standard and reliability' was possible in built-up areas. The mobile equipment was extremely bulky and in no way a 'personal phone'; even the Walkie-Talkie portable fm two-way radio introduced by Motorola for US forces in 1943 was a hefty back-pack affair weighing 35lb. But there was a much more portable two-way radio operating on uhf frequencies (450MHz) known as S-Phone.

Developed in 1941 by Capt. Bert Lane and Major Hobday, both of Royal Signals, S-Phone became standard operational equipment in 138 and 161 Squadrons of the RAF for covert air-to-ground communication. A similar short-range radio was developed in 1944 by the Americans for OSS agents working in Germany under the cover-name Joan-Eleanor; this set worked on 260MHz. Highly-directional vhf beam antenna systems were also developed for gun-laying radar and other purposes, so it can be argued that the key elements of the technology required for cellular radio were in place by 1946. The only elements missing were the finance and commercial pressure to turn concept into reality.

The same applies to the concept of multi-channel digital television – or something very close to it. This, as far as I can trace, was first revealed in print the same year, 1946. The author was Kenneth Ullyett in the long defunct publication *Courier*, a sort of all-British version of *Reader's Digest*. Just read this.

"euphoria for cellular radio, multi-channel television and high-definition pictures at the end of the war was fated to subside..."

Radio experts have been disclosing the secrets of frequency modulation broadcasting, but this system is already out-dated by a new British discovery... The BBC Television section is very enthusiastic because the pulse sys-



Campbell Swinton had already devised all the elements of electronic television in 1911, only the technology to realise his project was missing.

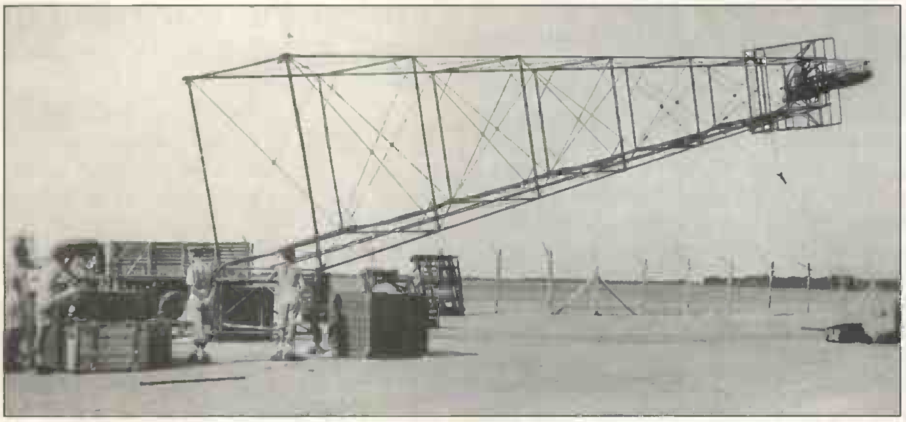
"Well-informed people know it is impossible to transmit the voice over wires..."

tem offers a very special advantage to television. Sight and vision can be broadcast on the same wavelength. In fact, a choice of television programmes, both sight and sound, could be put out on the same wave-length lane, leaving receiver pulse selectors to sort them out.

In his article Ullyett describes both pulse width and pulse time modulation and put his money on pulse time. He had witnessed tests, he said, which showed it was possible to get better sound definition and tonal quality by varying the timing of the pulses rather than their shape. Today we would call the technique pulse-position modulation and the alternative pulse width system which he refers to had recently been exploited during the war to best advantage in the Wireless Set No. 10, a somewhat prosaic designation that in fact conceals a fully mobile multi-channel radiotelephone system operating on a 6GHz carrier.

Entirely British in design and conception, this was undoubtedly the world's first multi-channel communication system and was yet another engineering achievement that helped 'save our bacon' in those dark days half a century ago. The 'Ten Set' as it is also known used pulse-width modulation and after early trials in 1942 was first used to link the Isle of Wight to Cherbourg, just after D-Day. Subsequently it provided vital speech links, within the advancing forces and back to the War Office in London. It was flexible and secure, whilst there is no evidence that the Germans even knew of its existence, let alone that they succeeded in intercepting it.

More than fifty years ago Britain successfully exploited the Wireless Set 10 – an eight-channel microwave radio systems for secure communication in the battlefield; at the end of the war the same technique was proposed for broadcasting multi-channel to the home. Here we see the mobile equipment of the Ten Set as a tower carrying dishes is raised. Photo courtesy Chris Hilton.



Ullyett described the pulse system as being equally valid for sound broadcasting as for television although he conceded it would not see the light of day in the immediate future. 'The present position is that all radio manufacturers in Britain are committed for at least 18 months to a programme of over 60 per cent for export, and they could not possibly make home receivers for the pulse system.'

High-definition television, that is with more than 1000 lines, also saw its first serious exploitation fifty years ago as part of war efforts.

"digital television was revealed in print in 1946..."

In Paris the Compagnie Française de Télévision maintained development work on television throughout the period of German occupation, producing a 1050-line system, described by an Allied Combined Intelligence Objectives Committee report compiled in October 1944.

A demonstration of a 1050-line system was seen on a cathode ray tube of 15in diameter. The picture was extremely good, definition and contrast were very good, even up to the corners of the picture. At a distance of eight feet the quality was comparable with that of an ordinary cinema. During the demonstration, films and a live scene from the studio were shown on both the 450 and the 1050-line systems. The improvement in the increase in entertainment value of the 1050-line picture was most marked. The same type of iconoscope [camera tube] was used in the 1050 and 450-line systems.

The report continues that although the 1050-line transmissions are well ahead, they were not yet ready to be put into service and that if television started again in the next two years, it would surely start with the 450-line transmissions. History proved the author of the report entirely right.

Whereas the French were devising high definition television for broadcast entertainment purposes, the Germans had a different purpose in mind. In mid-1940 Fernseh technical experts developed and demonstrated a complete 1029-line television system, the purpose of which was said to be transmitting maps for military purposes.

Employing a slide-scanner as pickup device the apparatus gave exceptional results, exceeding 16mm film in resolution. Despite this apparent success, the authorities were apparently unconvinced of the system's strategic value and given its need for 15MHz transmission bandwidth, it is difficult to see how these pictures could have been transmitted with security over long distances.

What became of this work in France and Germany? In the latter case, not a lot. After the war German researchers remaining in the Russian Zone were spirited off to Leningrad, whilst the two installations which had been moved out into Sudetenland (then a part of Germany and now in the Czech Republic) to avoid Allied bombardment formed the nucleus of Czechoslovakia's television development scheme. In the western zones of Germany the Allies initially prohibited any further research into television and thus any momentum was lost. In any case it was now considered that 625 lines were a more practical compromise for entertainment television.

That was not the thinking in France, however, and television was a field in which France intended to excel in the new era of peace. Again, however, a compromise was called for since their 1050-line system would occupy too much bandwidth over the air. So by 1948 an 819-line system, demonstrably superior to the existing British, American and new German systems, was devised and this remained in use for nearly 40 years. As well as demonstrating Gallic achievement, there was a notion that the unique 819-line system would discourage foreign manufacturers from entering the French market, a strategy that no longer succeeded when Sony and other Far Eastern manufacturers brought out transistor portable sets which included the 819-line standard in the late 1960s.

What lessons can be learned from each of these demonstrations of premature technical achievement? Certainly that given the correct environment and resources, the timescale for new development can be compressed considerably, and the pride in achievement and the enthusiasm to take this further are hard to suppress at the time.

Technical virtuosity is of little value, however, if there is no commercial market for it and no means to apply it to mass production. For this reason it was sadly inevitable that the euphoria for cellular radio, multi-channel television and high definition pictures at the end of the war was fated to subside and not surprising that fifty years on we are only now really starting to enjoy the benefits of those predictions.

For technology to create a mass market it must offer something the broad public both desires and can afford, and back in 1946 most people's minds were on matters more prosaic than advanced home entertainment or convenience in communication. In those days even a normal telephone in the home was a luxury, whilst television was exclusively for the well-off. Times change. ■

Software that plays cards

Software can help get the most out of data-acquisition expansion cards. *Signal Centre* can help more than most, says Allen Brown

Data acquisition and processing used to be the preserve of engineering and physical science laboratories. Now pcs are routinely found in biology, chemistry and even psychology departments, with many machines dedicated to data acquisition applications.

Converting a pc into a data acquisition platform is simply a matter of inserting a suitable card, with analogue and i/o facilities. But software is needed to drive the card too, and this is where packages such as *Signal Centre* come in, automatically recognising the expansion card and providing all the processing features likely to be needed.

Signal Centre, version 2 from Computer Park Software – a British company for a change – runs under Microsoft *Windows* and can be used either for data acquisition, or as control software as it has the ability to output digital i/o and analogue signals.

No programming skills are called for since everything is performed using dialogue boxes, and the user should feel at home with familiar 'viewports' such as an oscilloscope, chart recorder, meter, led display, rotary control, thermometer and other display and control items.

The heart of *Signal Centre* is a large 'processor' library containing all the operations and functions likely to be needed. Each processor (or range of processors) is used to feed information into the display items.

Designing a system is intrinsically quite straightforward, with the user working backwards from the final display.

For example, to show an oscilloscope displaying a square wave contaminated by noise (**Fig. 1**), the first step is to generate an oscilloscope by clicking on the appropriate icon. Clicking on the scope brings up a dialogue box that allows the `multisig add` processor to be included and generates another dialogue box, enabling an input to the adder to be selected. This in turn generates a processor dialogue box, so that `square wave generator` can be selected from a list.

Once that dialogue box is closed a second input can be chosen. The processor list again appears and this time `White Noise` is chosen.

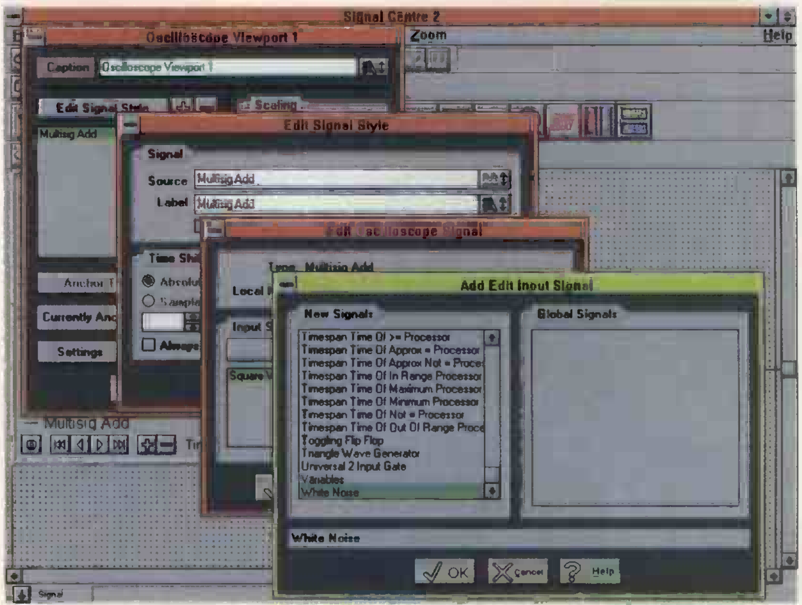


Fig. 1. To construct a design in Signal Centre, the user works backwards through a series of dialogue boxes. Each processor has a dialogue box attached to it and the user configures it by changing the settings in the box.

When all the dialogue boxes are closed, a noise-contaminated square wave appears on the oscilloscope screen, **Fig. 2**. Various parameters can be adjusted for each processor before it is accepted.

Initially the procedure appears somewhat awkward, but after a little practice it becomes surprisingly easy to generate and customise a design layout. However, real proficiency only comes through practice, as operation of the software is far from intuitive.

Expansion card drivers

A large range of device drivers is supplied for the popular analogue i/o cards, and this is an attractive feature. Drivers are included for the Amplicon PC range, ComputerBoard's CIO range and for Datel and IOTech expansion cards.

Many cards have multiple analogue channels. When the driver for the input card is selected the card can be configured, via its dialogue box, for the appropriate mode. So, with an eight-input analogue card the user can show all eight input channels on the chart recorder viewport (**Fig. 3**). Adjustments can also be made to the gain and sampling frequency of the channels by choosing appropriate options in the dialogue box.

Configuring an analogue i/o card in this way, with little fuss, is very effective and is one of the best selling points of the package. Signals from the i/o cards are then available to any processor the user selects.

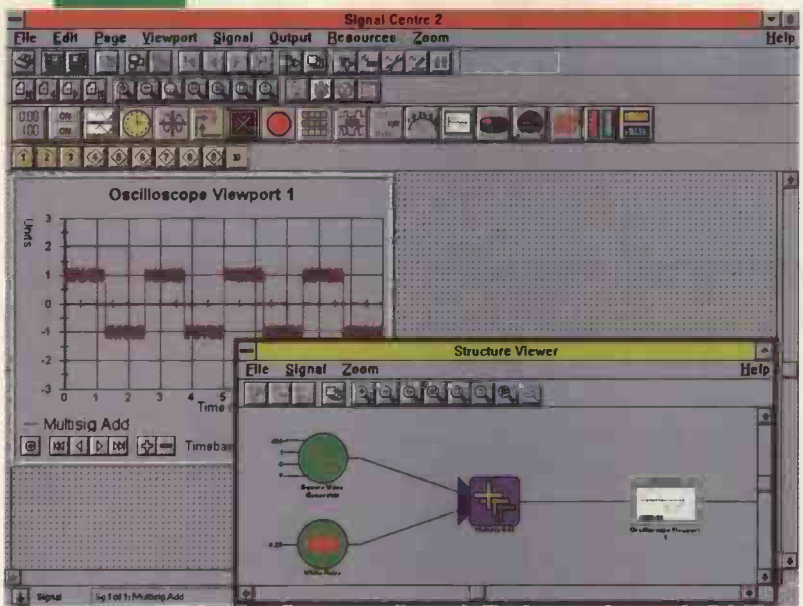


Fig. 2. A design completed, the oscilloscope viewport can be used to show output signals. In this case we see a noise-contaminated square waveform, the schematic of the processors and connections needed for its construction.

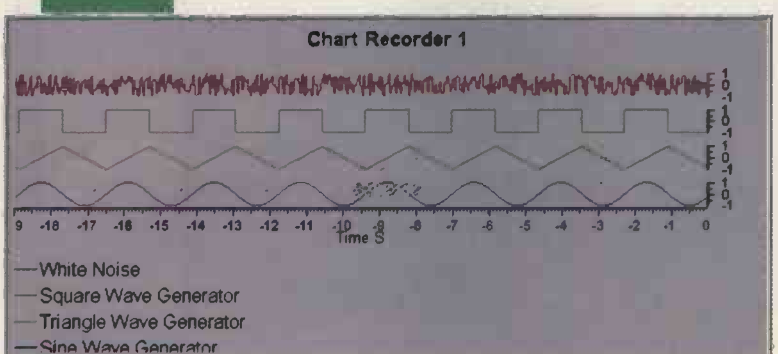


Fig. 3. One of the most useful viewports, the chart recorder, can be linked directly to an analogue i/o expansion card to give real-time signal monitoring.

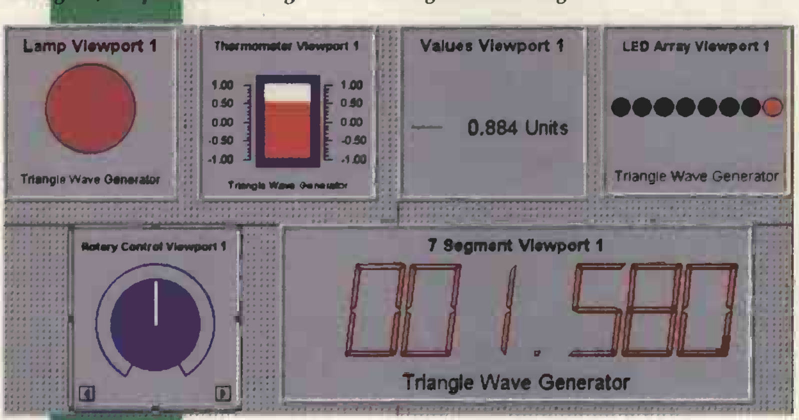


Fig. 4. Several viewports can be useful for monitoring a small scale system. Each viewport can have conditional settings attached to it.

Viewport visualisation

Visual aspects of *Signal Centre* are handled by viewports. Some serve only as quantitative devices – the thermometer and bulb for example – and various voltage thresholds can be set to give different colour displays (**Fig. 4**). If the pc has a sound card, audio (voice) outputs can be triggered when threshold or condition events occur.

When monitoring small-scale industrial processes these viewports and the audio warning features could prove to be quite useful. Should a record of the data displayed by each viewport be needed, a disk file can be attached to store the data for future analysis. Or real-time statistics can be performed on the data by constructing an array of processors from the processor library.

Controlling events

'Events' are important to *Signal Centre* and act in a similar way to interrupts. They are evoked once certain conditions are satisfied.

Typical events include buttons in a button-box viewport, pressing keys on the keyboard, threshold values from viewport thermometers and checkers (conditional comparisons). Determining these conditions is accomplished by means of more processors.

Events can also be triggered sequentially by using a timer, with each event added to an event list and evoked when the appropriate time has lapsed – so events can be scheduled at predetermined times.

Once they have been added to the event list with their respective start and reset times the sequence is started with the `play` button from the menu bar.

`Fast-forward`, `rewind`, `pause` and the all-important `stop` button are a nice idea if you want to automate a sequence of measurements and control outputs over a long time – certainly quite appealing in a laboratory environment for long-duration testing.

Processors

The impressive number of processors within the library is accessed by a drop-down menu Simple examples range from a moving average (**Fig. 5**) to curve fitting following input data (**Fig. 6**).

Polynomials up to order twenty can be demonstrated. But computational time starts to become noticeable for high order curve fitting, even on a fast *486*-PC.

A viewport for dealing with image allows pictures to be imported to improve the layout of a display. Appearance of images can be conditionally controlled with a suitable processor – which looks like a good idea for reminding the user pictorially of the origin of signals.

User manuals

Signal Centre's four manuals – Reference, Guide to Processors , User Guide and Guide to Drivers – are well laid out with a pleasing presentation. But certain aspects are acutely lacking, and the Guide to Processors is of questionable value in several respects. For example, it provides a discussion on all the processors but fails to explain how many of the processors can be used. Consequently several processors appear quite enigmatic in operation. Lack of examples illustrating processor application is also very irritating.

The Reference manual describes overall operation of the software in general terms, with particular attention focused on the viewports. But what is really needed in the User's manual are tutorials and actual examples showing how to use the processors.

Many *Signal Centre* operations are not intuitive and their operation is far from obvious, and some new users simply will not have the time to learn by trial and error.

Minimum system requirements
486-DX PC
SVGA colour monitor
8Mbyte ram
10Mbyte hard disk
Recognised analogue i/o expansion card

Availability
Computer Park Software, Broughton Grange, Headlands, Kettering, Northants NN15 6XA. Tel: 01536 417955 Fax: 01536 417466. Prices, professional version £795, standard £295. Multi-user and educational discounts are available.

But the tool is only suitable for small images. Moving a large memory image takes several seconds and is unacceptable in practice. So caution must be exercised when using this feature.

A variety of other data sources (and destinations) can be accessed by using the dynamic data exchange (dde) processors.

Spectral analysis
Discrete Fourier transform (dft) and fast Fourier transform (fft) processors are available in the library (**Fig. 7**).

Spectral outputs are displayed on an oscilloscope viewport. At first this can be rather confusing as the X axis is displayed as time (seconds). In a messy procedure, it is left to the user to make all the necessary changes to display frequency. .

As potential users of the software are likely to place a high importance on frequency measurements, future versions could really do with a separate spectrum analyser viewport.

Another puzzling oversight is the default number of input data points into the dft or fft processors – not 512 or 256 or even 128 but only one!

Needless to say nothing happens when you first use these processors unless you spot the appropriate data button. Even the reference manual does not caution against using the default value.

Window functions to profile the data before using the dft or fft processors are also lacking. But, with these reservations, on the whole the package is pretty good.

Once you have acquired the technique of working backwards from display to source, you should be able construct a design for data acquisition within a couple of hours. The manufacturers must be complimented on the ease of configuring the i/o cards, and this must be a major selling point for the package.

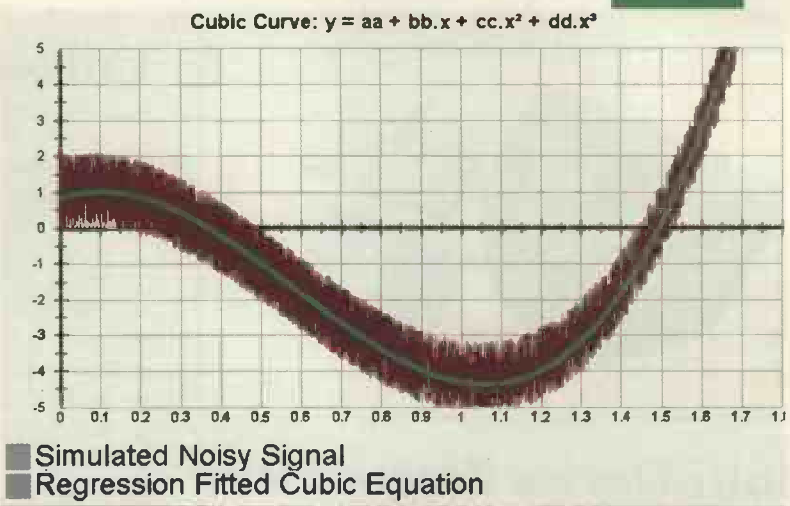


Fig. 6. Curve fitting can be performed and polynomials up to order 20 can be used. But processing time is much extended as the order is increased.

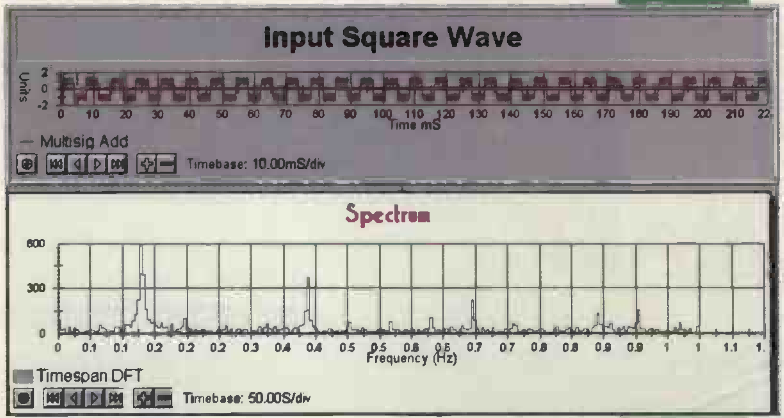


Fig. 7. The spectrum (bottom trace) you would expect from a square wave (top trace) after a fast Fourier transform.

Visual impact of the software is good and the instant access of the viewports is attractive.

For small scale control applications *Signal Centre* would probably serve quite adequately, provided real-time advanced signal processing techniques are not required.

Overall, for data acquisition, storage and display purposes *Signal Centre* is easy to use and is highly recommended. ■

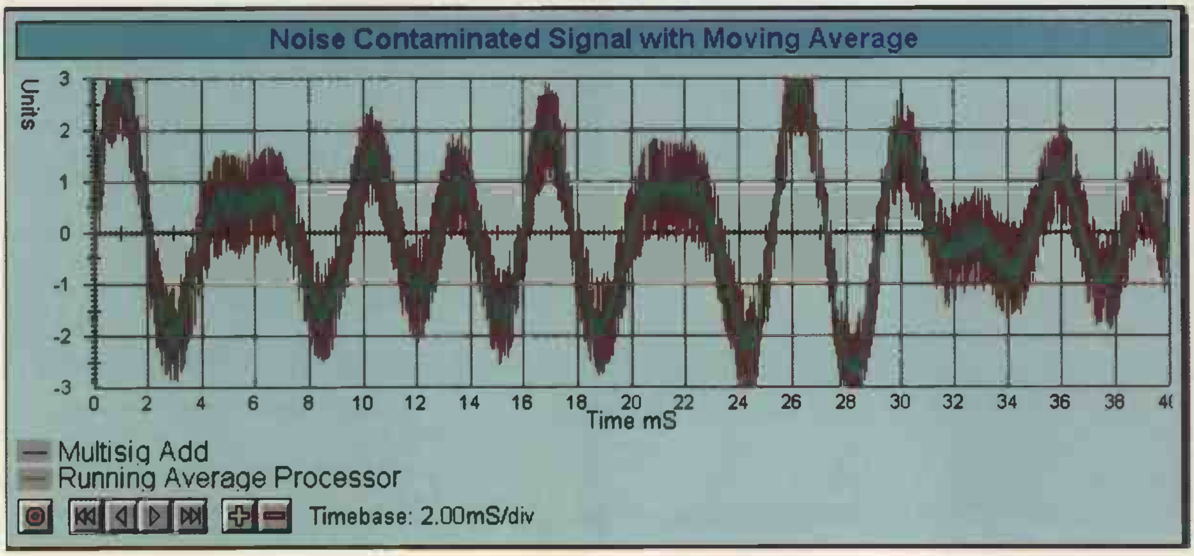


Fig. 5. When dealing with noisy signals it is sometimes convenient to use a running average processor to show the trend movement. In Signal Centre, *this can be implemented in real time.*

DOUBLE MIRRORS REFLECT HIGHER SPEED

Boosting the gain of a power amplifier's long-tail pair can reduce distortion, increase speed. But will gain boosting cause instability? Not necessarily says Bengt Olsson.

Input stages of most power amplifiers are long-tailed pair, Fig. 1. They have a high output impedance, and are loaded by Miller capacitor C_3, via the dotted line.

A frequent problem is that the open loop gain is too small to produce enough negative feedback*. As a result, thd is increased.

This current mirror booster replaces an extra stage. It acts as a buffer amplifier, preventing loading of the long-tail pair and supplying plenty of current to the next stage, Tr_9. The high gain increases output slew-rate and gain-bandwidth product, reduces intermodulation and thd, and increases power bandwidth.

The circuit was first applied to my 'super-symmetrical' mosfet amplifier, but it is also applicable to bipolar voltage amplifier transistors, since Tr_9 can be a bipolar device.

Design details

A typical long-tail pair has a current mirror $Tr_{5,6}$, $R_{5,6}$, which assures that i_1 and i_2 are equal and in opposite phase. Adding Tr_7 and R_7 produces another output current i, which may be N times higher than i (since $R_5/R_7=N$). The output voltage of Tr_6 has low output impedance – approximately equal to R_6 – and is able to drive both Tr_5 and Tr_7 since gate current of Tr_7 is small.

The same voltage appearing on the three transistors $Tr_{5\text{-}7}$ produces more current in Tr_7 since R_7 is smaller than R_5 by a factor of N. This means that Tr_7 works as a current booster without phase delay and with a high output impedance.

Adding Tr_8 provides a complementary current in opposite phase to that of Tr_7. At low slew-rate, Tr_8 works in a linear mode around the idling current of Tr_7. If the feedback signal tries to turn Tr_8 off, it also starts to turn Tr_7 on, pulling current negatively.

If Tr_8 sees a positive signal, it again has the idling current of Tr_7 as a high impedance source, but is also free to supply current. It will eventually be limited in some way. When limiting takes place, Tr_7 current falls to zero. Transistor Tr_8 now conducts twice the idling current – in Class A – and can supply even more. This only takes place if maximum signal output slew-rate is exceeded, and never with ordinary program material.

Note that Tr_8 normally conducts almost constant current, supplied by Tr_7. Gain of the long-tail pair is thus extremely high, resulting in very low thd. This is true for increasing current modulation in Tr_8, caused by increasing frequency. This is true until current amplitude in Tr_8 reaches the steady-state current in Tr_7, which still is held almost constant. Output current is the difference between the currents in Tr_8 and Tr_7, each being driven in its own way.

Output slew rate now reaches 50% of its maximum value, which may give a power bandwidth of, say, 50kHz. With further increasing frequency, still in Class A, the current may be twice this value. Current in either Tr_7 or Tr_8 on the other hand switches to zero as the signal approaches typically 100kHz at full amplitude.

The high current is justifiable if large gate-capacitance mosfets are used, or if maximum usable current in the capacitance C_2 can not normally be obtained from the long tail pair. This may be for example because the pair would need to supply too much Δi_1 current,

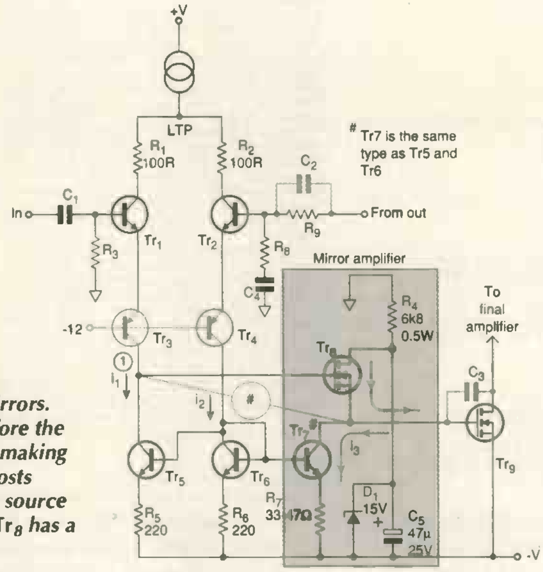


Fig. 1. Implementing dual current mirrors. Placing the dual mirror amplifier before the second voltage amplifying stage and making use of the existing current mirror boosts output current. This is a true current source since Tr_7 *is a current generator and* Tr_8 *has a very high impedence driver.*

*Above approx. 1kHz, open loop gain of the amplifier is half of $g_m/\omega C_3$, where g_m is transconductance of Tr_1 in series with R_1 and $\omega=2f$. Increasing the g_m of the long-tail pair would help, but may involve much higher current in the input transistors, of the order of 10-20mA – an impossible solution.

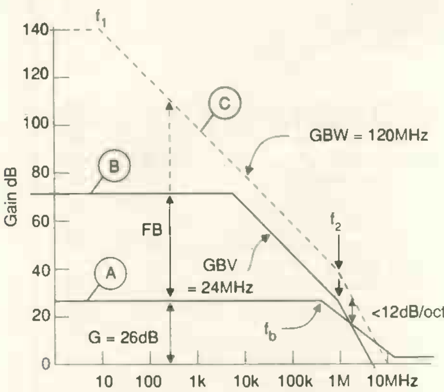


Fig. 2. Gain versus frequency for the dual current mirror. Curve A is closed-loop gain, typically 20×, while B is open-loop gain for a typical bipolar-transistor power amplifier. Curve C shows open-loop gain with a dual current booster.

Note that a higher gain-bandwidth product reduces the so-called tim-spike and improves the THD in general – especially at the sensitive lower frequencies. Curve A must cut the open loop curves B or C at less than 12dB/octave (<180°) for stability. A minor pole, f_2, is in reality unavoidable. It reduces stability. In the super-symmetrical design, f_2 is generated at the output stage, but it is relatively easily dealt with. Note that the selection of C_2 is critical – a fact that every designer has experienced.

resulting in high thd – a frequent problem.

Push-pull action is advantageous since idling Class-A current is only 50% of the peak current. More current in C_3 means faster output slew-rate and other benefits relating to thd etc. as indicated above.

6dB/octave roll-off down to 10Hz

As a bonus, with Tr_8 a mosfet, the gain-bandwidth product will increase at all frequencies, down to a few hertz. In this case, local gain between the non-inverting input and Tr_8 is more than 10^5. This will not cause oscillation, since the roll-off is 6dB/oct, but it will render thd at frequencies under 1kHz insignificant.

Transistor Tr_8 could also be bipoplar. Any small 200MHz f_t device will do. Bipolar types have a smaller input capacitance than the *2N7000* mosfet. Even so, the mosfet performs well when used as a source follower. Loading on i_1 is around 10pF. This comprises feedback capacitance of the *2N7000* in a grounded-drain configuration of 5pF, plus the input capacitance reduced by the source-follower efficiency. It is difficult to measure any difference between the bjt and the mosfet, except at low frequencies, due to the number of zeros in the thd figure.

Gain improvers

This circuit is an example of a gain improver – a device, which increases the gain towards the low frequency end, without lowering the gain-bandwidth product.

It is a popular misconception that any increase of absolute gain has to be accompanied by an increase of the compensating capacitor C_3.

The key to this design is that increasing the gain avoids increasing C_3 and in turn reducing the gain-bandwidth product†. The problem is to maximize gain-bandwidth product, without causing oscillation.

One way to improve gain is to use a current source as a collector load followed by another high input impedance mosfet, as in node 1 of Fig. 1. Bootstrapping and emitter followers can also improve gain.

These techniques for improving the gain of a stage can avoid additional stages of amplification. Any new stage introduces an additional 90° phase shift, increasing the chance of oscillation.

Ideally, there should only be one gain stage – the long-tail pair – and it should never be necessary to have more than two.

In this way, phase shift stays 180° or lower, allowing a high gain-bandwidth product since the minor poles are high in frequency. ■

†I assure readers concerned about intermodulation caused by high feedback that it is possible to use unlimited amounts of feedback without the slightest risk for tim – provided that the feedback is properly implemented. The common notion of tim has as much substance as other popular myths. It would be interesting to discuss these questions sometime in this paper.

COAXIAL cable tester

Although less complicated than some reflectometers, this experimental instrument by Dmitry Malinovsky provides a digital indication of reflection index, from which vswr and power loss are easily obtained.

In time, even well designed coaxial signal distribution systems can need maintenance. The instrument described is an experimental cable tester that has been used under real conditions when installing and maintaining private cable tv networks.

As its block diagram in **Fig.1** shows, it consists of an hf oscillator, broadband amplifier, directional coupler and reflectometer, forming an 'active' reflectometer with its own oscillator and working into 75Ω. It is smoothly tunable in three bands – 40-70MHz, 70-125MHz and 125-225MHz – to ensure the overlapping of the tv bands I and III, the cable tv band, the 144-146MHz amateur band and the communications frequencies. Amplifier output at 15mW goes to the directional coupler, which detects and separates the forward and reflected signals and feeds the results to the reflection index meter to give a digital indication of the ratio V_{ref}/V_{for}.

Oscillator

Figure 2 shows that the hf oscillator section consists of separate circuits for each band, using three *J309* jfets, each Varicap-tuned oscillator covering one band. Diodes $D_{4,5}$ in the jfet gates help to stabilise the oscillator output amplitude at about 0.6Vpk-pk; there is no need for a diode in the highest-frequency oscillator since its output does not exceed 0.6V. Potentiometer P_1 tunes all the oscillators and is calibrated in frequency to within about 5%. Non-working oscillators are switched off to save power.

Directional coupler

Output from the wide-band amplifier goes to the input of the directional coupler, the circuit of which I 'borrowed' from Ref.1 and modernised slightly to simplify the design. Coupling coefficient in my version is –10dB; I know from experience that one should choose the largest possible signal level at the input of the directional coupler and use the maximum coupling coefficient, so that signals proportional to forward and reflected waves are fed to the measuring detectors at maximum possible amplitude.

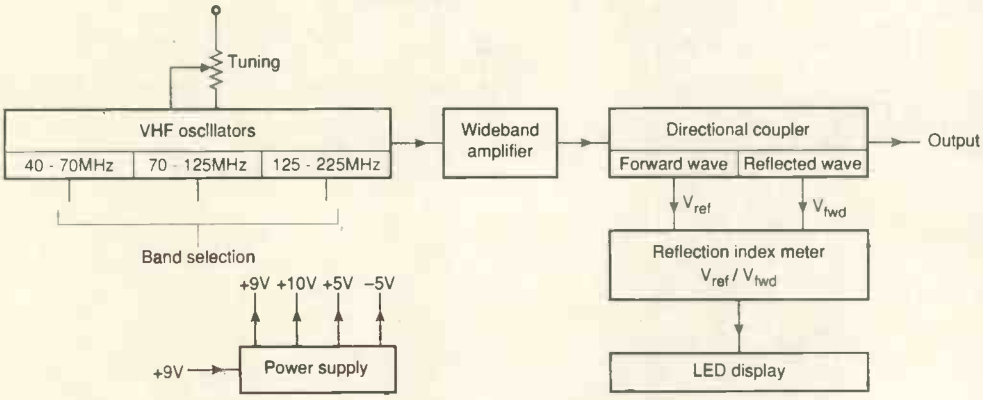
Semiconductor diodes work well as linear detectors when the hf signal amplitude is greater than 100-200mV for germanium diodes and more than 200-400mV for silicon types. If the directional coupler is connected to a matched feeder, the amplitude of the reflected wave can be less than 5% or 10% of the forward wave amplitude. Taking into account the –20dB gain of the directional coupler, one can see that when the signal level in the feeder is 2Vpk-pk and the reflection index is equal to 0.1 (a well matched feeder), there is 0.2Vpk-pk at the 'forward' coupler output and 0.02Vpk-pk at the "reflected wave" output.

It is not easy to detect such signals linearly and the use of the usual diode detectors will lead to errors of up to 50% and perhaps more; the -10dB coupling coefficient and the use of logarithmic-amplifier detectors give an accuracy of better than ±5%%. I used germanium diodes, selected in pairs; methods of diode selection are described in the appendix.

Detection

Two *741* op-amps are used as logarithmic amplifiers, the type having a moderate thermal drift. Both are balanced by potentiometers P_2 and P_3 to obtain zero voltage at the their outputs with no hf input and potentiometers R_{adj} trim for best detection linearity, particularly when working with hf inputs in the range 30-800mVpk-pk. It turned out to be possible to measure a reflection coefficient of 0.06 to

Fig. 1. Block diagram of reflectometer coaxial-cable tester, working in the 40-225MHz frequency range. The instrument will measure a reflection coefficient of 0.06 to within ±10%.



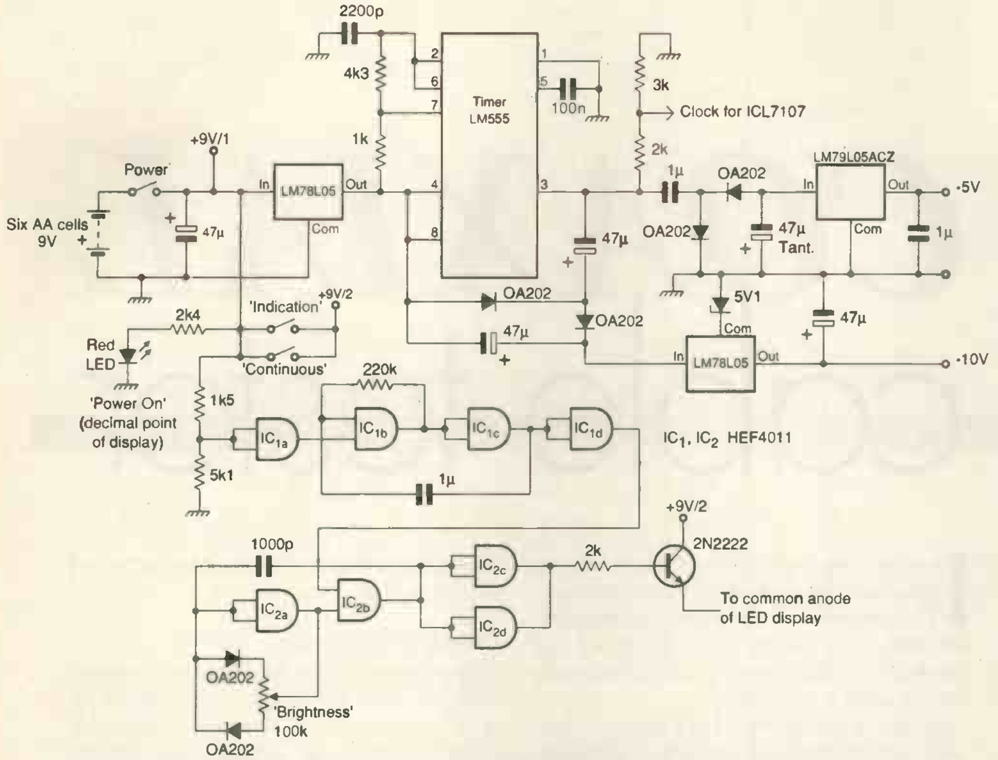
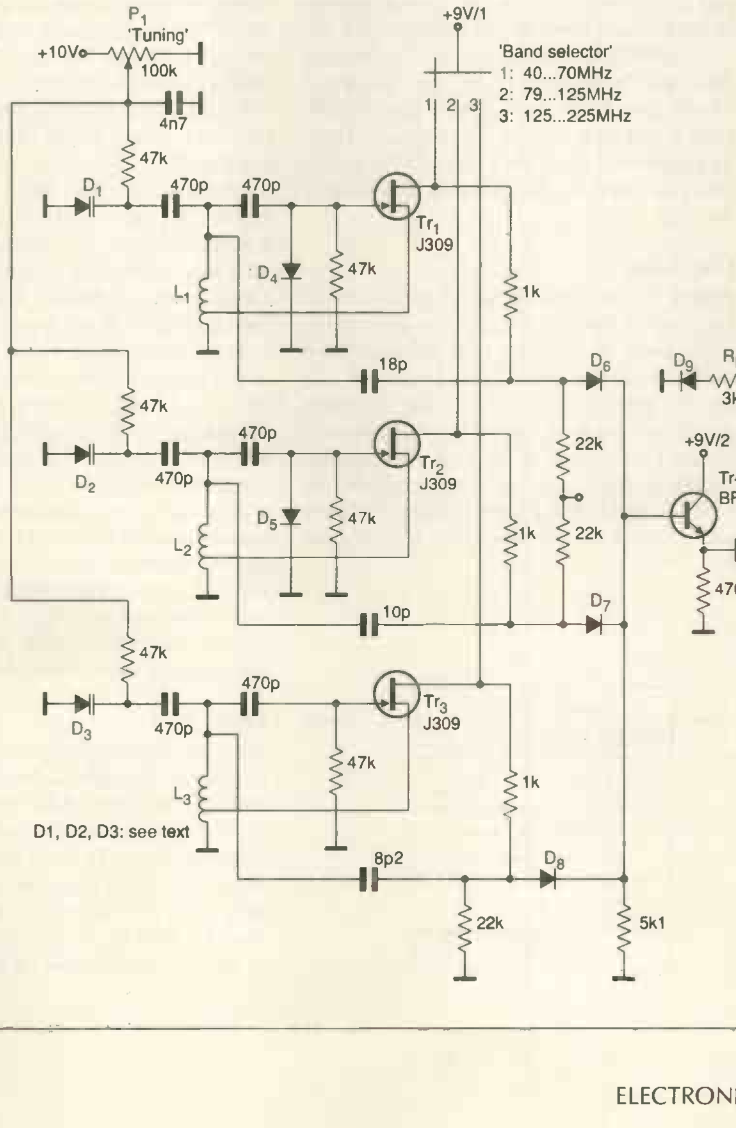


Fig. 2. Three frequency bands covered by three separate oscillators. Analogue-to digital converter acts as analogue voltage divider with digital output, since output n is proportional to V_{in}/V_{ref}.



an accuracy of about 10%.

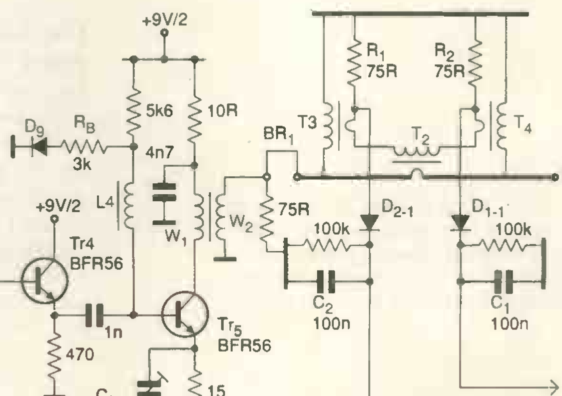
An *ICL7107* a-to-d converter fulfils two functions: it divides the two analogue signals, by virtue of the fact that the reference voltage is varied, and indicates the result in digital form; it helps to simplify this part of the circuit immeasurably and the accuracy of the ratio meter itself is better than 0.1% – negligible in comparison with the accuracy of the rest of the circuit.

Only two digits are used for the indication of tenths and hundredths of the value of the reflection coefficient; the thousandths are more or less irrelevant, bearing in mind the overall accuracy, and the indication of the permanent "zero" is an extravagance from the power point of view. Optimum display is in the form ".XX", the decimal point being a power-on indicator.

Selecting diodes

I use an ordinary analogue ohmmeter for this. When measuring resistances in the sub-bands 1, 10 and 100kΩ, the currents flowing differ according to the logarithmic law. Every selected diode is connected to the ohmmeter and its forward resistance in three sub-bands is measured. Two diodes are considered to have been selected in a pair if their forward resistances coincide in three points (in the three sub-bands) to within 5%. Usually, two pairs with the necessary accuracy can be selected from 20-30 diodes.

Fig. 3. Power supply giving four outputs from one 9V input. Logic circuitry forms a battery-management arrangement.



Power supply

This is rather complicated because it is intended for a portable device demanding several supply voltages. I calculated on the use of six AA-cells in the tester. **Figure 3** shows the circuitry of the power supply with a *555* timer working as a multivibrator to drive the voltage converter to give –5V for the op-amps and a-to-d converter, regulated by the *LM79LO5ACZ*; it also drives the voltage doubler to provide, via the *LM78LO5* fixed voltage regulator, +lOV for the varicaps and op-amps. A positive 5V for the *ICL7107* comes straight from the battery via an *LM78LO5* fixed regulator. Clock signals for the *ICL7107* also come from the *555* oscillator.

Multivibrator $IC_{1.2}$ and $IC_{1.3}$ constitute a battery-management circuit; when battery voltage falls below 6.5V, the multivibrator starts up and the display flashes at about 1Hz. To extend battery life, display power comes from the brightness regulator, which is pulse-width modulator $IC_{2.1}$-$IC_{2.4}$.

An additional power economiser is the 'indicate/continuous' switch which, in the indicate position, turns on the power amplifier and indicators only during measurements, reducing power consumption between activities; it can be blocked by switching to 'continuous'.

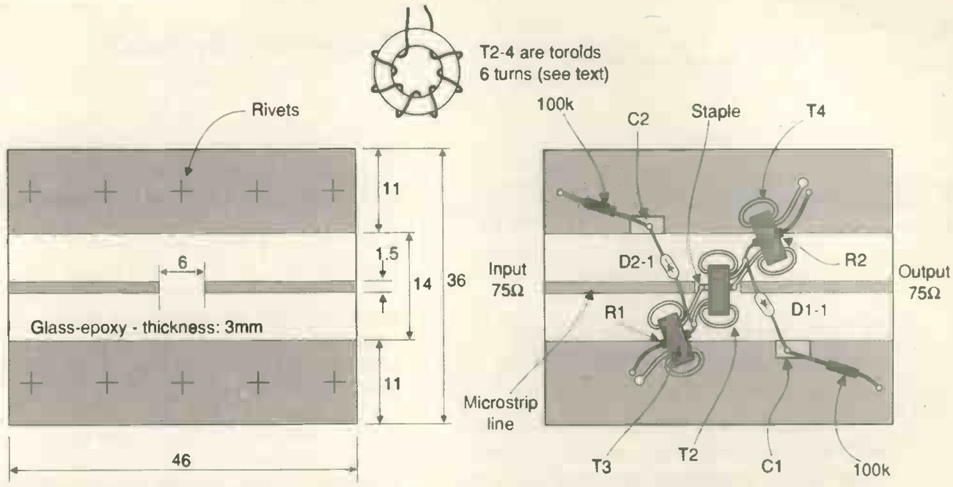


Fig. 4. Both sides of the directional coupler built on a stripline, part of the main board. Close adherence to this layout is advised.

Reflection index	0.05	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0
VSWR	1.10	1.2	1.5	1.9	2.3	3.0	4.0	5.7	9.0	19	∞
Power losses, %	<1	1	4	9	16	25	36	49	64	81	100

The kind of losses caused by mismatching the transmission line with the source load.

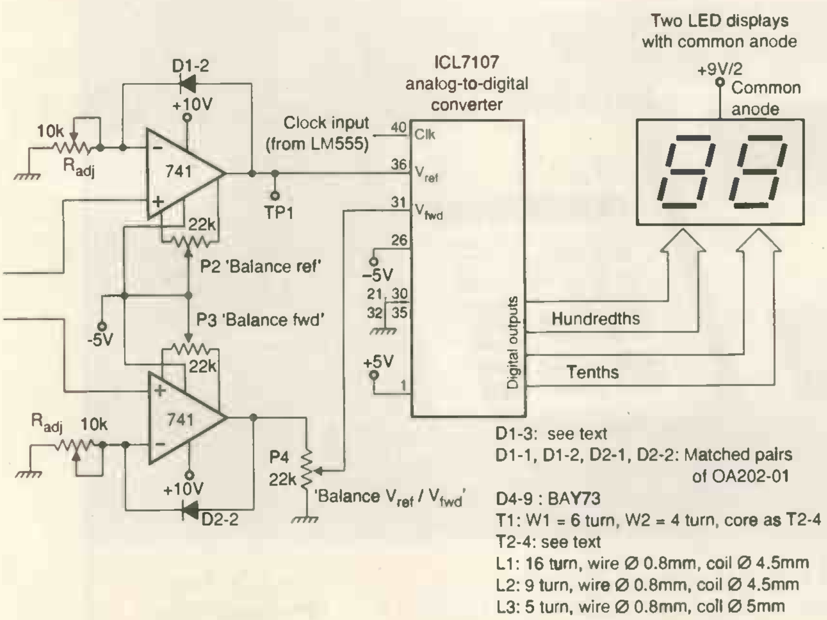
Coupler details

Figure 4 shows the construction of the directional coupler, which consists of a pc board with a microstrip line and three current transformers wound on ferrite cores with an outside diameter of 7mm, inside diameter 4mm and 2mm thick; permeability is 400. One can use any cores of a suitable size and permeability from 400 to 1500.

Each transformer has a six-turn secondary of 0.2mm solid, Teflon-insulated conductor (it is easier to solder), all three cores being wound in the same direction. Transformer Tr_2 in Fig. 2 is held in the gap of the microstrip line, with its contacts up, by a staple that represents the primary coil of Tr_2. Transformers Tr_3 and Tr_4 are soldered with their contacts down – one contact to the staple and microstrip line and the other to ground.

Resistors R_1 and R_2, both 75Ω, 1/8W, are pushed through the cores of the transformers Tr_3 and Tr_4 and soldered to ground at one end and to the corresponding contact of the Tr_2 at the other. Leads of resistors and transformers should be cut as short as possible. Diodes $D_{1\text{-}1}$ and $D_{2\text{-}1}$ should have their anode ends soldered close up to resistors R_1 and R_2 and the contacts of Tr_2. Capacitors C_1 and C_2, are used as mounting contacts, soldered to ground by one leg and supporting a diode cathode with the other.

Note that the directional coupler is part of the pc board on which all other elements of the tester are assembled. A bnc connector, having an adaptor on the microstrip line, is soldered to the board. As regards general construction, my tester is in a 0.8mm sheet-steel case, measuring 180 by 100 by 60mm.



Setting up

Tuning the tester is not difficult. First, the three hf oscillators should be adjusted to their sub-bands by varying the spacing of the turns. Using the set of three identical Varicaps of the type used in broadcast fm receivers or tv channel selectors gives a 1.8:1 tuning ratio in all three sub-bands.

Then set the collector current of the transistor T_5 to 15mA by adjusting the resistor R_b. Connect a 75Ω hf signal generator equipped with a calibrated attenuator to the directional coupler input (remove the bridge Br_1 first) and load the directional coupler output by a 75Ω resistor. Set the output voltage of the generator equal to 2Vp/p and measure the direct voltage at the detector output on TP_1; it should be 300mV ±15%. Decrease the hf level by 10dB and check the voltage on TP_1, which should decrease linearly with the decrease of hf input. Tune the potentiometer R_{adj} in such way that the detector nonlinearity is less than ±7% when the hf signal changes from 70 to 2000mVpk-pk.

Tuning of the second detector is carried out in the same way, but the signal is fed to the directional coupler output and the input is loaded by a 75Ω resistor. Now check the frequency response of the tester's hf oscillators

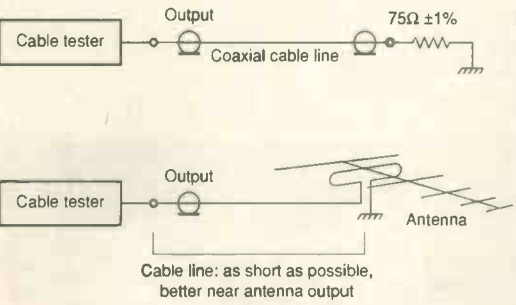


Fig. 5. Ways of using cable tester, checking coaxial cable, top, and an antenna, bottom.

by loading the tester output with 75Ω and watching the direct voltage on TP_1. Frequency response is adjustable by trimming capacitor C_f, but a little unevenness up to about 3dB in all bands is quite admissible.

Applying the tester

Figure 5 shows methods of connecting the tester for checking coaxial cable line and antenna. The only universal rule is: when checking any hf devices, one should make the connection between tester and tested as short as possible. ■

Reference

1. R.Lewallen. A Simple and Accurate QRP Directional Wattmeter. *QST*, February 1990, pp.19-23.

Processing the results

When a signal propagates in a transmission line there can be three cases:

(a) the impedance of the signal source is equal to the characteristic impedance of the transmission line (W), and the line is loaded by a resistance $R = W$. This is the matched mode and signals in the transmission line propagate only from the signal source to the load;

(b) impedance of the signal source is equal to the characteristic impedance of the transmission line, but the line is broken or shorted at the end. In this case, standing waves are formed in the line;

(c) impedance of the signal source is not equal to the characteristic impedance of the transmission line or the line is loaded by an impedance $Z \neq W$, ($Z=r+jx$). This is a mixed-wave mode, in which the line simultaneously carries signal that propagates from the source to the load and that from load to source.

How well the signal source matches with the line or the line with the load is characterised by the voltage standing wave ratio (vswr), which is the ratio of characteristic impedance to load impedance (or the signal source impedance): vswr = R/W when R is more than W or vswr = W/R when W is more than R.

With a device that can measure the amplitudes of the forward wave (propagating from signal source to the load) and of the reflected wave (propagating from the load to the source), you can measure the so-called reflection index:

$$\Gamma = V_{ref}/V_{fwd} = |R-W|/|R+W|,$$

there being a simple correlation between Γ and vswr:

$$\Gamma = (vswr-1)/(vswr+1) \text{ or } vswr = (1+\Gamma)/1-\Gamma).$$

Knowing reflection index or vswr, one always can define the power gain when the signal propagating in an unmatched transmission line

$$M = 4/(2 + vswr + 1/vswr) \text{ in absolute units or}$$
$$M = \log(4/(2 + vswr + 1/vswr)) \text{ in decibels.}$$

When power losses arise, the line resistance is irrelevant – it can be equal to zero but the losses can make up 100% of the signal power if the matching is wrong. The table shows the kind of losses caused by mismatching the transmission line with the source or the load.

The application of the transmission line dictates what matching we can consider satisfactory. For vhf-fm broadcast transmitters, a vswr of up to 1.2 is usually permissible and it is undesirable to have a vswr of more than 1.5-2 in tv receiving antennae. A mismatch in long tv coaxial lines causes not only energy losses but also a very unpleasant double or ghost image that can be seen when light objects are on a dark background.

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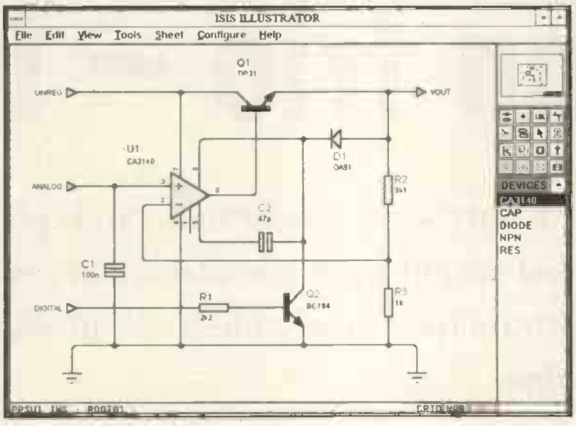

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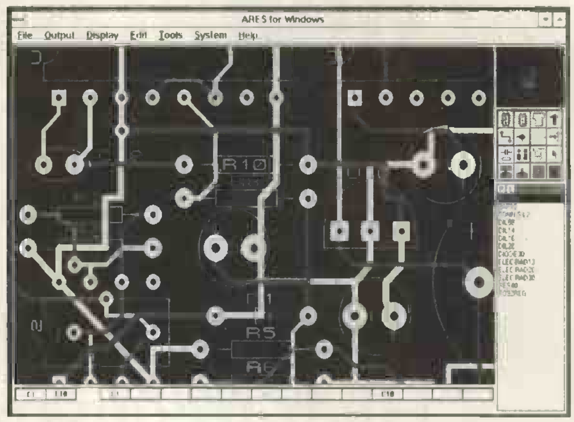

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Waveform generation trio – II

Oscillators based on saw filters: handy 4046 circuit that varies phase shift; and low distortion high-level output from a fundamental crystal oscillator. Three circuits demonstrate how simple ideas can produce useful effects. From *EDN* magazine.

High-frequency vcos top 100MHz

Surface-acoustic-wave (saw) filters are available from US, European and Japanese manufacturers in an increasing range of frequencies and styles. They permit the direct implementation of vhf and uhf high-stability oscillators without the doublers or triplers needed with crystals, and with a wider pulling range.

VCOs that use saw filters have higher operating frequencies and higher pull ranges than circuits using crystal oscillators.

Two examples (see circuits) show how practical realisations of saw-filter-based vcos can have different operating frequencies – 140 and 181MHz – because of that fact that two types of saw filters are available. The first circuit uses a saw filter that has 180° of phase shift, while the second has a phase shift of 0°. Both circuits draw about 20mA and operate from a 5V supply. Operating frequency is solely dependent on the saw filter's pass-band centre frequency, which can be higher than 1000MHz.

The saw filters have a pull range near 500ppm when the *BBY31* varactor diode's control voltage $V_{control}$ varies by 4V. Typical pk-pk voltage of the circuits when driving a 50Ω load is 600mV, and the spectrum of the output signals is such that all the harmonics are below 25dB with respect to the carrier. Variation with temperature when the circuits run in the free-running mode is 100ppm – a typical value for saw filters.

Crystal oscillators tend to be more stable over their operational frequency range than saw-based oscillators. But that range is limited compared with the range of saw-based oscillators. SAW filters are available with centre frequencies starting at 120MHz.

Component cost of both circuits, without the saw filter, is about £0.80 with the saw filters costing about £20.

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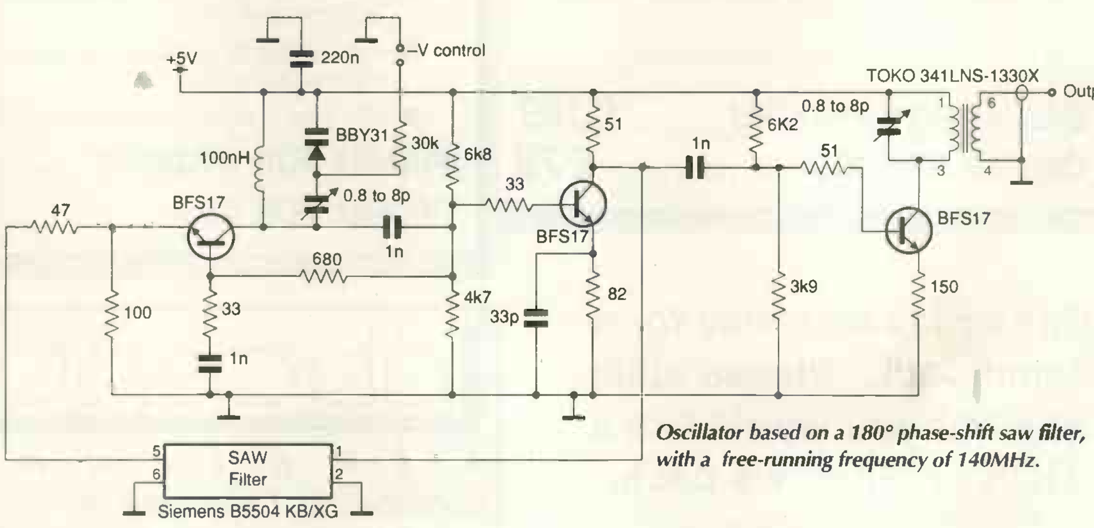

Oscillator based on a 180° phase-shift saw filter, with a free-running frequency of 140MHz.

Offset varies pll's phase shift

Deliberately introducing a dc offset into the error-signal path of a phase-locked loop (pll), allows phase shift to be added between the input reference and the feedback signal driving the phase detector.

This circuit has a phase-shift range of ±160° over a reference-signal range of 1-10kHz: if the signals applied to pins 3 and 14 of the *CD4046* are both divided by 2^N first, the available phase-shift range becomes 2^N times 320°. Because the loop uses an integrator, once set, the phase shift remains constant over the entire frequency range.

The positive-edge-triggered frequency/phase detector inside the *CD4046B* compares the frequency and phase of the input reference signal with the feedback signal from the *74HC193* counter. Since this phase detector is edge-triggered, the duty cycle of the reference can be arbitrary.

IC_{1A} level shifts the three-state output of the phase detector. When in lock, if the positive edge of the reference leads the positive edge of the feedback signal, the output of IC_{1A} swings to its lower rail for the time interval between the two edges.

The output then returns to 2.5 V until the next positive edge of the reference occurs.

If the positive edge of the reference lags the positive edge of the feedback, IC_{1A} output remains at the upper rail for the time interval between the two edges. It then returns to 2.5V until the next positive edge of the feedback occurs.

Using the quad *LMC660C* cmos op-amp for IC_{1A} permits dynamic-loop, error-voltage variations over almost the entire range of 0 to 5V. Adjusting the 20kΩ potentiometer causes the phase shift to change because the average voltage of the pulses at the output of IC_{1A} must change to maintain the constant-feedback-forced value of 2.5V at the inverting input of IC_{1B}. A unity-dc-gain lead network stabilises the loop.

Output of the vco is divided by 16 before applying it to the phase-detector input.

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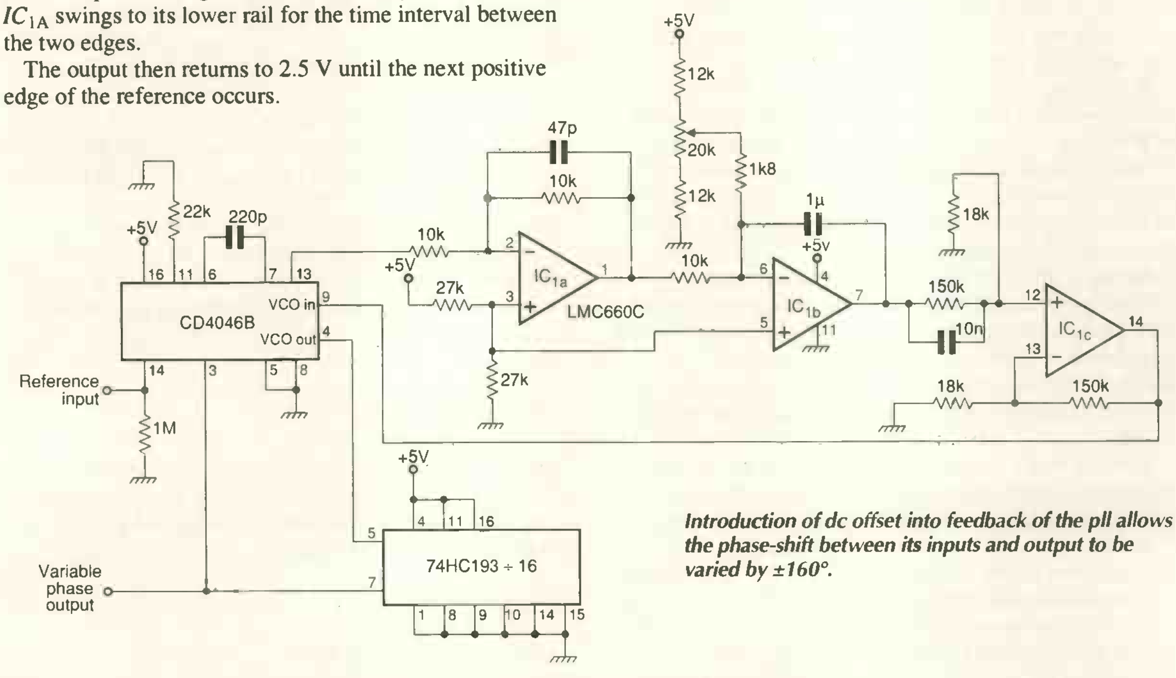


Introduction of dc offset into feedback of the pll allows the phase-shift between its inputs and output to be varied by ±160°.

Servo loop controls oscillator amplitude

It may not provide the ultimate in low noise crystal oscillator design, but we can design a circuit that offers sufficient output level (combined with a good waveform having a low harmonic content) to drive a double balanced mixer directly. Crystal drive level may be set to optimise either long term or short term stability, as required,

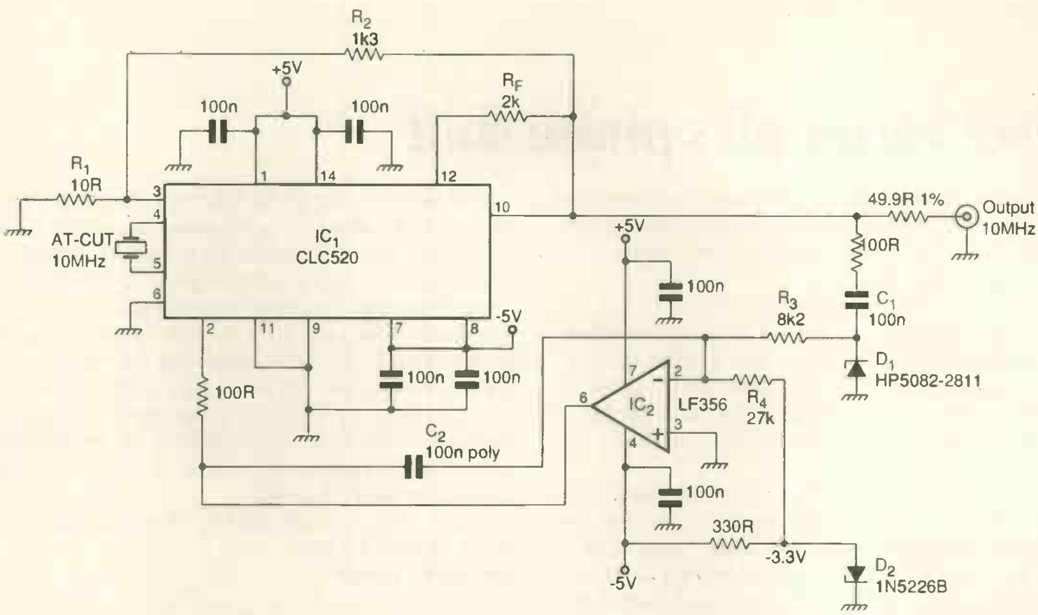
The high-performance, fundamental-mode crystal oscillator uses an agc amplifier and a crystal to form a very-narrow-band filter at the crystal's series-resonant frequency. Phase noise and jitter are reasonably low because the design places the crystal between two low-impedance points of the *CLC520* agc amplifier IC_1. The oscillator can drive a 50Ω load easily and has a well-controlled output impedance, while the design exhibits low distortion and is adaptable to a variety of fundamental-mode crystals.

Unlike most oscillators, which use limiting to set the amplitude, this design uses a servo loop to control amplitude. D_1 and C_l are the key components of a clamping circuit that produces an average voltage proportional to the pk-pk oscillator amplitude. The larger the amplitude, the more positive the dc component.

The *LF356* (IC_2) is as an integrator that compares the dc signal against the reference voltage of D_2. If the oscillator's amplitude is too high, the integrator's output voltage drops, as does the gain of IC_1 and the loop gain of the oscillator.

When the loop gain drops below unity, the oscillator output amplitude begins to drop until it reaches the desired amplitude of the loop. If the amplitude is too low, the integrator output voltage increases, increasing the loop gain and increasing the amplitude to the desired value of the loop.

When the oscillator amplitude is stable, the average



Unlike most oscillators, which use limiting to set the amplitude, this 10MHz oscillator uses a servo loop to control amplitude. Six steps are necessary to tailor the design to individual requirements.

current flowing into the integrator capacitor (C_2) is zero. The average current through R_3 is equal in magnitude and opposite in sign to the current flowing through R_4 (assuming that bias currents for IC_2 are negligible) and the oscillator loop gain is exactly equal to one.

A levelling loop, not circuit limiting, sets the amplitude of this oscillator design, so distortion is low. The amount of distortion is mostly set by IC_1 and as its band-width (typically 140MHz for large signals) is approximately four to five times higher than the highest oscillation frequency of most fundamental mode AT-cut crystals, the effect of IC_1 band-width is negligible.

Design of the oscillator requires six major steps.

First step is to determine the range of equivalent series resistance for the crystal. – it should be consistent with the distribution of crystals to be used. If the range is to be tuned, the equivalent resistance of the crystal and tuning network at the new series-resonant frequency should be found.

In the case of a crystal and a tuning capacitor in series, the highest overall series resistance exists at the lowest tuning capacitance and highest crystal series resistance.

Second step is to choose the output amplitude. To determine the output voltage at pin 10 of IC_1, dBm should be converted to watts using $P_{out} = 10^{(0.1\mathrm{dBm}-3)}$ where P_{out} is the power delivered to the load in watts, and dBm is the power delivered to the load in dBm. RMS voltage delivered to the load is $V_{OL}=(R_{load}\times P_{out})^{0.5}$. For a doubly terminated load, the equation is,

$$V_{opamp}=2\times V_{OL}=(4R_{load}\times P_{out})^{0.5}$$

where V_{opamp} is in volts rms.

Third step is to select the crystal drive level. Drive levels should be 1 to 20μW for good long-term stability, or between 100 and 500μW for good short-term stability.

Equivalent series resistance of the crystal affects the drive level, so the drive level must be reasonable for all expected values of the resistance.

One way to start is to choose the maximum crystal drive level (D_{max}) and see if the minimum drive level is acceptable using:

$$D_{min} = D_{max}\left(\frac{R_{s(max)}}{R_{s(min)}}\right)\left[\frac{R_{s(min)}+3}{R_{s(max)}+3}\right]^2$$

where $R_{s(max)}$ and $R_{s(min)}$ are the maximum and minimum series resistances, respectively. If this calculated value of D_{min} is acceptable, whether or not IC_1 can deliver D_{max} needs to be determined.

IC_1 will be most limited at the minimum series resistance, as $D_{limit}=(0.9113\times10^{-6})R_{s(min)}$, where D_{limit} is the maximum drive available from IC_1 in W, and $R_{s(min)}$ is the minimum crystal series resistance in ohms.

If D_{limit} is greater than D_{max}, IC_1 can deliver the targeted maximum drive level. If not, substitute D_{limit} in place of D_{max} in the above equation for D_{min} to determine the lowest drive that will occur.

D_{limit} and the new D_{min} set the new drive-level range.

Step four is to set the forward gain of the oscillator.

Input voltage to IC_1 pin 3 must be determined at the maximum series resistance as follows (with D_{min} in W and V_{in} in V rms):

$$V_{in} = \left(R_{s(max)}+3\right)\left(\frac{D_{min}}{R_{s(max)}}\right)^{0.5}$$

The equation accounts for the crystal's loading of the buffers of IC_1 (pins four and five). Now the voltage gain of IC_1 at the highest series resistance and highest gain-control voltage (A_v) can be determined:

$$A_V = \frac{V_{op\ amp}}{V_{in}}$$

To achieve this gain, set R_F as:

$$R_F = \frac{A_V\left(R_{s(max)}+3\right)}{1.85}$$

In general, the value of R_F should be between 1 and 2kΩ.

Somewhat higher values are acceptable if the oscillator is running below 10MHz. If R_F needs to be lower than 1kΩ, refer to the data sheet for the output-amplifier loop-gain reduction techniques for IC_1.

The penultimate step is to calculate values of the feedback network R_1 and R_2. To keep the noise low at IC_1 input and provide reasonable resistor values, $R_1 \geq 10\Omega$ and $\leq 1\mathrm{k}\Omega$.

Loss in the network should be set equal to $B = 1/A_v$, which means that $R_2 = R_1\,(A_v-1)$.

The sixth and final step requires setting up the levelling loop. Average voltage from the clamping circuit is (where V_{pk} is the peak output voltage of IC_1, and V_D is the forward voltage drop for D_1):

$$V_{DC} = V_{pk} - V_d = 1.414V_{op\ amp} - V_D.$$

Six steps to servo amplitude control

1. The crystal has a measured equivalent series resistance of approximately 7.3Ω. Range of R_S is 5-25Ω.
2. Output-power requirement is 7dBm into 50Ω so that the oscillator can drive a double-balanced mixer directly. The requirement translates into an output voltage at the op-amp of approximately 1V rms.
3. For a 5Ω minimum equivalent series resistance, IC_1 limits crystal drive level to 4.56μW. At R_S of 25Ω, the drive level falls to 1.86μW. These numbers produce good long-term stability.
4. Input voltage at IC_1 pin 3 is 7.64mV rms. Voltage gain is 131, so R_F must equal 1.98kΩ (use 2kΩ).
5. R_1 is set to 10Ω, so R_2 must equal 1301kΩ.
6. Assuming a forward drop of 0.4V for D_1 yields approximately 1V dc from the clamping circuit. R_3 must then be approximately 8.3kΩ (use 8.2kΩ). C_1 is set to 0.1μF because this design is for 10MHz oscillator.

Once the amplitude of the oscillator is stable, the current flowing through R_3 and R_4 must cancel at C_2. For this condition to be met,

$$R_4 = R_3\left(\frac{V_{D2}}{V_{DC}}\right)$$

where V_{D2} is the zener voltage of D_2. To ensure stability of the amplitude-control loop, C_2 should be made equal to 0.01 x F, where C_2 is in μF and F is in MHz. ■

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Trimodal Audio power part 2

Douglas Self has already shown how the low-impedance negative feedback network integrated into his trimodal amp reduces noise. Here he demonstrates how low-Z nfb improves output dc offset performance too. He also details the amplifier's mode-switching and bias control systems and looks at overall performance.

The same components that dominate amplifier noise performance also determine the output dc offset; if R_9 is reduced to minimise the source resistance seen by Tr_3, then the value of R_8 is scaled to preserve the same closed-loop gain, and this reduces the voltage drops caused by input transistor base currents.

My previous amplifier designs assumed that a ±50mV output dc offset is acceptable. This allowed dc trimming, offset servos, etc to be gratefully dispensed with. However, it is not in my nature to leave well enough alone, and it could be argued that ±50mV is on the high side for a top-flight amplifier. For this reason, I have reduced this range as much as possible without resorting to a servo; the required changes were already made when impedance of the feedback network was reduced to minimise Johnson noise. There were details on this in last month's issue.

With the usual range of component values, the dc offset is determined not so much by input transistor V_{be} mismatch, which tends to be only 5mV or so, but more by a second mechanism-imbalance in beta. This causes imbalance of base currents, I_b, drawn thorough input bias resistor R_1 and feedback resistor R_8. Cancellation of the voltage-drops across these components is therefore compromised.

A third source of dc offset is non-ideal matching of input degeneration resistors $R_{2,3}$. Here they are 100Ω, with 300mV dropped across each, so two 1% components at opposite ends of their tolerance bands could give a maximum offset of 6mV. In practice, it is unlikely that the error from this source will exceed 2mV.

There are several ways to reduce dc offset. Firstly, a Class-A amplifier with a single output pair must be run from modest ht rails, so the requirement for high-V_{ce} input transistors is relaxed. This allows higher beta devices to be used, directly reducing I_b. The *2SA970* devices used in this design have a beta range of 350 to 700, compared with 100 or less for *MPSA06/56*. Note the pinout is *not* the same.

In the first half of this article, we reduced the impedance of the feedback network by a factor of 4.5, and the offset component due to I_b imbalance is reduced by the same ratio. We might therefore hope to keep the dc output offset for the improved amplifier to within ±15mV without trimming or servos. Using high-beta input devices, the I_b errors did not exceed ±15mV for ten sample pairs – *not* all from the same batch – and only three pairs exceeded ±10mV. Errors in I_b are now reduced to the same order of magnitude as V_{be} mismatches, and so no great improvement can be expected from further reduction of circuit resistances. Drift over time was measured at less than 1mV, and this seems to be entirely a function of temperature equality in the input pair.

Figure 1 shows the ideal dc conditions in a perfectly-balanced input stage, assuming a ß of 400, compared with a set of real voltages and currents from the prototype amplifier. In the latter case, there is a typical partial cancellation of offsets from the three different mechanisms, resulting in a creditable output offset of –2.6mV.

Biasing for three modes

Figure 2 shows a simplified rendering of the Trimodal biasing system; the full version appears in **Fig. 3**. The voltage between points A and B is determined by one of two controller systems, only one of which can be in command at a time. Since both are basically shunt voltage regulators sitting between A and B, the result is that the lowest voltage wins. The novel Class-A current-controller introduced in the original article[1] is used here adapted for 0.1Ω emitter resistors, mainly by reducing the reference voltage to 300mV, which gives a quiescent current (I_q) of 1.5A when established across the total emitter resistance of 0.2Ω.

In parallel with the current-controller is the V_{be}-multiplier Tr_{13}. In Class-B mode, the current-controller is disabled, and critical biasing for minimal crossover distortion is provided in the usual way by adjusting preset Pr_1 to set the voltage across Tr_{13}. In Class-A/AB mode, the voltage Tr_{13} attempts to establish is increased (by shorting out Pr_1) to a value greater than that required for Class-A. The current-controller therefore takes charge of the voltage between X and Y, and unless it fails Tr_{13} does not conduct. Points A B X Y are the same circuit nodes as in reference 1.

Class A/AB mode

In Class-A/AB mode, the current-controller, comprising $Tr_{14,15,16}$ in Fig. 2, is active and Tr_{13} is off, as Tr_{20} has shorted out Pr_1. Transistors $Tr_{15,16}$ form a simple differential amplifier that compares the reference voltage across R_{31} with the V_{bias} voltage across output emitter resistors R_{16} and R_{17}; as explained in reference 1, for Class-A this voltage remains constant despite delivery of current into the load. If the voltage across $R_{16,17}$ tends to rise, then Tr_{16} conducts more, turning Tr_{14} more on and reducing the voltage between A and B. $Tr_{14,15,16}$ all move up and down with the amplifier output, and so a tail current-source Tr_{17} is used.

I am aware that the current-controller is more complex than the simple V_{be}-multiplier used in most Class-B designs. There is an obvious risk that an assembly error could cause a massive current that would prompt the output devices to lay down their lives to save the rail fuses. The tail-source Tr_{17} is particularly vulnerable because any fault that extinguishes the tail current removes the drive to Tr_{14}, the controller is disabled, and the current in the output stage will be very large. In Fig. 2 the V_{be}-multiplier Tr_{13} acts as a safety-circuit which limits V_{bias} to about 600mV rather than the normal 300mV, even if the current-controller is completely non-functional and Tr_{14} fully off. This gives a 'quiescent' of 3A, and I can testify this is a survivable experience for the output devices in the short-term; however they may eventually fail from overheating if the condition is allowed to persist.

There are important points about the current-controller. The entire tail-current for the error-amplifier, determined by Tr_{17}, is syphoned off from the voltage amplifier stage current source Tr_5. This must be taken into account when ensuring that the upper output half gets enough drive current.

There must be enough tail current available to turn on Tr_{14}, remembering that most of Tr_{16} collector-current flows through R_{15}, to keep the pair roughly balanced. If you feel moved to alter the voltage-amplifier stage current, remember also that the base current for driver Tr_6 is higher in Class-A than Class-B, so the positive slew-rate is slightly reduced in going from Class-B to A.

I must admit that the details of the voltage reference were rather glossed over in reference 1, because space was running out fast. The original amplifier shown last month used a National *LM385/1.2*, its output voltage fixed at 1.223V nominal; this was reduced to approx 0.6V by a 1kΩ/1kΩ divider.

The circuit also worked well with V_{ref} provided by a silicon diode, 0.6V being an appropriate bias voltage drop across two 0.22Ω output emitter resistors. This is simple, and retains the immunity of I_q to heatsink and output device temperatures, but it does sacrifice the total immunity to ambient temperature that a band-gap reference gives.

The *LM385/1.2* is the lowest voltage band-gap reference commonly available; however, the voltages shown in Fig. 2 reveal a difficulty with the new lower V_{bias} value and the complementary feedback pair stage; points A & Y are now only 960mV apart, which does not give the reference room to work in if powered from node A, as in the original circuit.

The solution is to power the reference from the positive rail, via $R_{42,43}$. The midpoint of these two resistors is bootstrapped from the amplifier output rail by C_5, keeping the voltage across R_{43} effectively constant. Alternatively, a current-source could be used, but this might reduce positive headroom. Since there is no longer a strict upper limit on the reference voltage, a more easily obtainable 2.56V device could be used providing R_{30} is suitably increased to 5kΩ to maintain V_{ref} at 300mV across R_{31}.

In practice, stability of I_q is very good, staying within 1% for long periods. The most obvious limitation on stability is differential heating of $Tr_{15,16}$ due to the main heatsink. Transistor Tr_{14} should also be sited with this in mind, as heating it will increase its beta and slightly imbalance $Tr_{15,16}$.

Class-B mode

In Class-B mode, the current-controller is disabled, by turn-

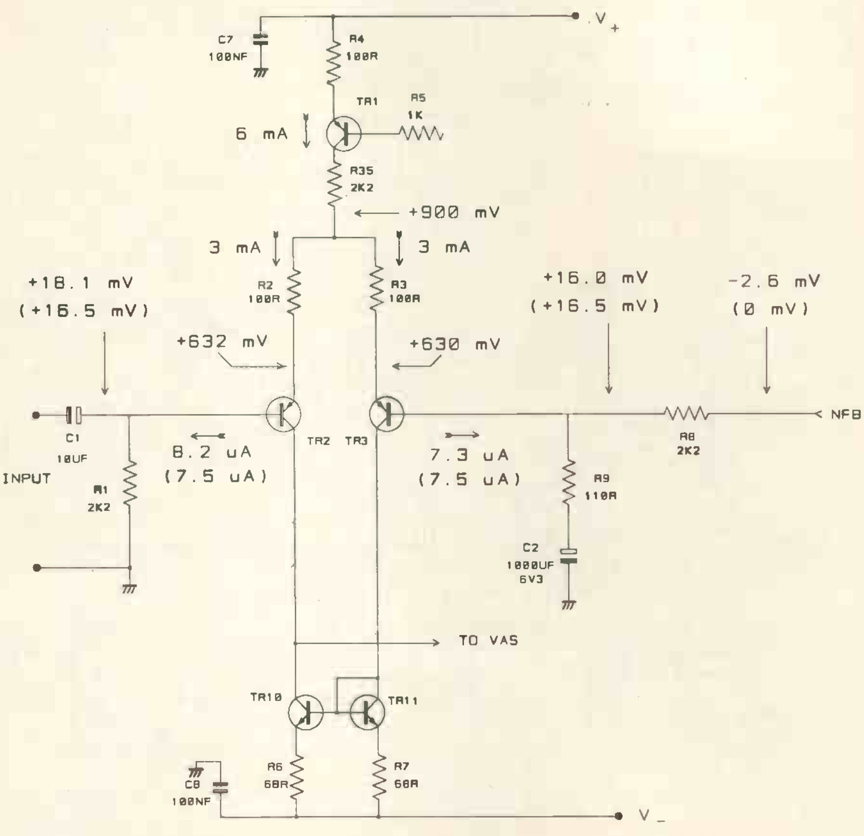

Fig. 1. A close look at input stage balance. Circuit conditions shown here are a real example. Ideal conditions for ß = 400 are shown in brackets. All voltages measured to ground.

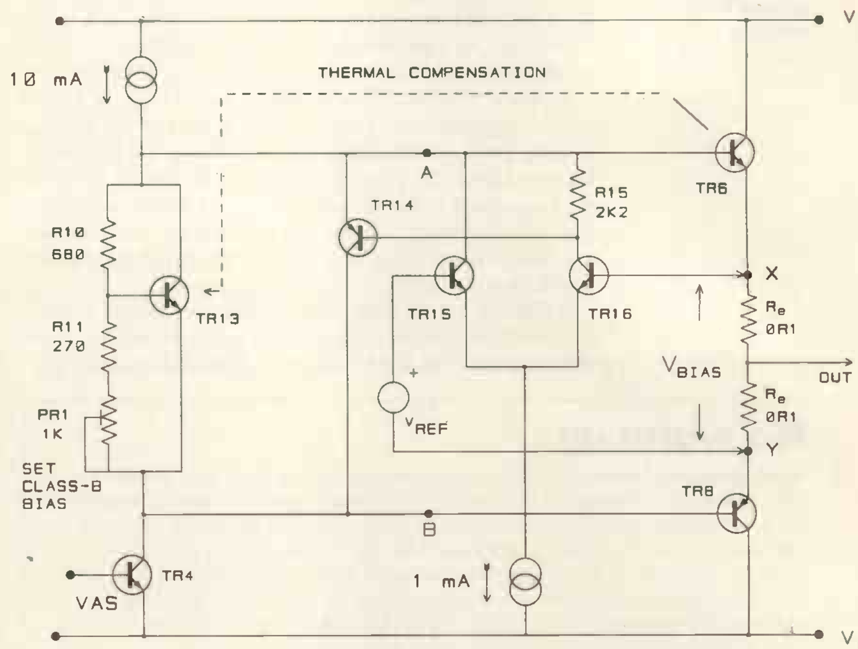

Fig. 2. Simplified current-controller in action, showing typical dc voltages in class-A. Points A, B, X and Y are the same as in the original class-A article. The grey panel on the left is the V_{be} multiplier, Class-B biasing and Class-A safety circuit. Panel in the middle is the Class-A current regulator. Voltage over points A,B is 1.5V while over X,Y, i.e. V_{bias}, there is 300mV.

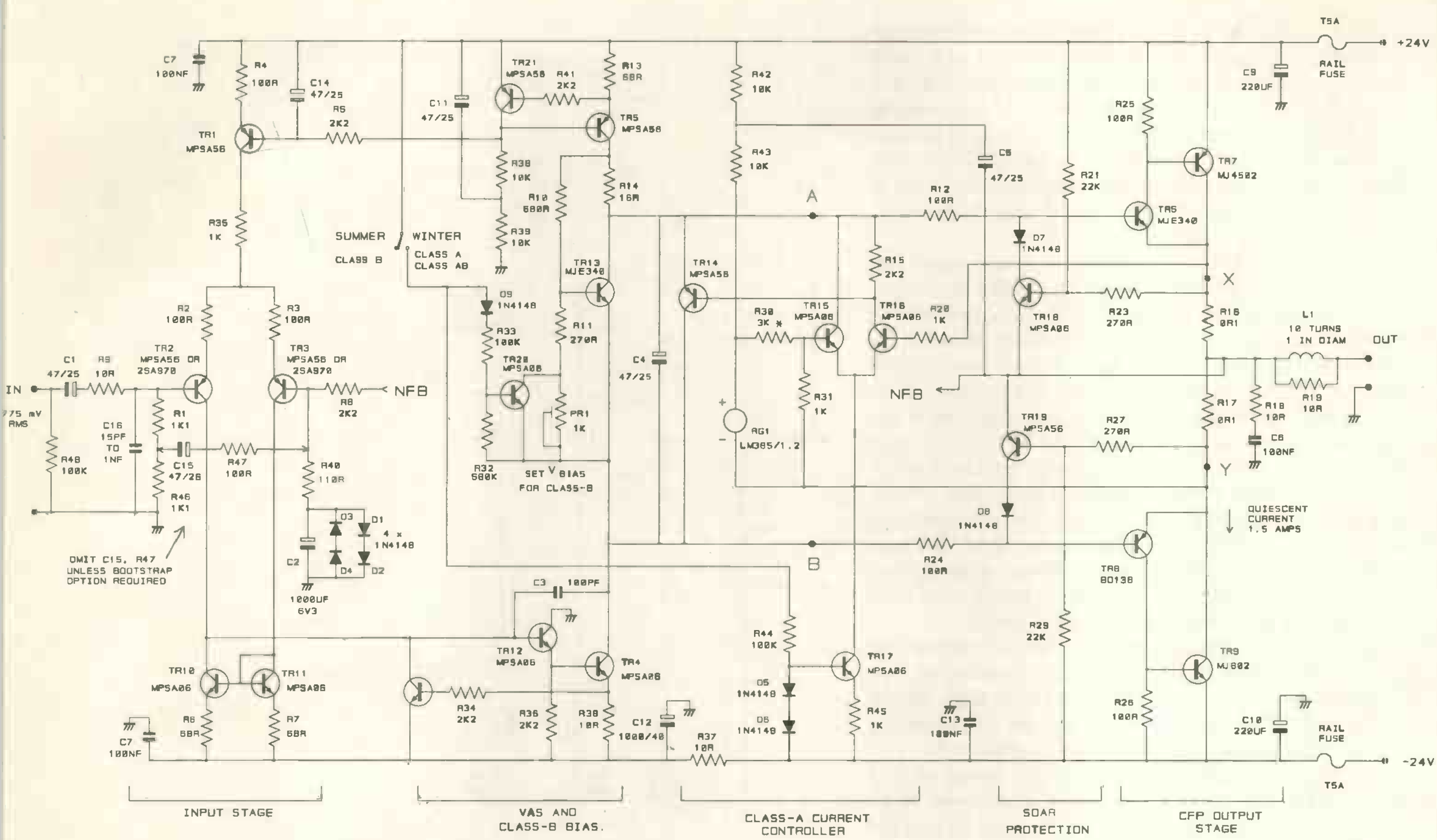

Fig. 3. Complete circuit diagram of class-A amplifier, including the optional boot-strapping components, R_{47} and C_{15}.

ing off tail-source Tr_{17} so Tr_{14} is firmly off, and critical biasing for minimal crossover distortion is provided as usual by V_{be}-multiplier Tr_{13}. With 0.1Ω emitter resistors V_{bias} (between X and Y) is approx 10 mV. I would emphasise that in Class-B this design, if constructed correctly, will be as 'blameless' as a purpose-built Class-B amplifier. No compromises have been made in adding the mode-switching.

As in the previous Class-B design, the addition of R_{14} to the V_{be}-multiplier compensates against drift of the voltage amplfier stage current-source Tr_5. To make an old but much-neglected point, the preset potentiometer should always be in the bottom arm of the V_{be} divider $R_{10,11}$, because when presets fail it is usually by the wiper going open; in the bottom arm this gives minimum bias voltage, but in the upper arm it would give maximum.

In Class-B, temperature compensation for changes in driver dissipation remains vital. Thermal runaway with the complementary feedback pair is most unlikely, but accurate quiescent setting is the only away to minimise cross-over distortion. Tr_{13} is therefore mounted on the same small heatsink as driver Tr_6. This is often called thermal feedback, but it is no such thing as Tr_{13} in no way controls the temperature of Tr_6; 'thermal feedforward' would be a more accurate term.

Switching modes

The dual nature of the biasing system means Class-A/Class-B switching is easily implemented, as in Fig. 3. A Class-A amplifier is an uneasy companion in hot weather, and so I was unable to resist the temptation to sub-title the mode switch 'Summer/Winter', by analogy with a car air intake.

Switchover is dc-controlled, as it is not desirable to have more signal than necessary running around inside the box, possibly compromising interchannel crosstalk. In Class-A/AB mode, S_1 is closed, so Tr_{17} is biased normally by $D_{5,6}$, and Tr_{20} is held on via R_{33}, shorting out preset Pr_1 and setting Tr_{13} to safety mode, maintaining a maximum V_{bias} limit of 600mV. For Class-B, S_1 is opened, turning off Tr_{17} and therefore $Tr_{15,16}$ and Tr_{14}. Transistor Tr_{20} also ceases to conduct, protected against reverse-bias by D_9, and reduces the voltage set by Tr_{13} to a suitable level for Class-B. The two control pins of a stereo amplifier can be connected together, and the switching performed with a single-pole switch, without interaction or increased crosstalk.

Mode-switching affects the current flowing in the output devices, but the output voltage is controlled by the global feedback loop, and switching is completely silent in operation. The mode is switchable while the amplifier is handling audio, allowing some interesting 'A/B' listening tests.

It may be questioned why it is necessary to explicitly disable the current-controller in Class-B; Tr_{13} is establishing a lower voltage than the current-controller which latter subsystem will therefore turn Tr_{14} off as it strives futilely to increase V_{bias}. This is true for 8Ω loads, but 4Ω impedances increase the currents flowing in $R_{16,17}$ so they are transient-

No warm up

Audio magazines often state that semiconductor amplifiers sound better after hours of warm-up. If this is true – in most cased it almost certainly isn't – the admission represents truly spectacular design incompetence. Accusations of this type are applied with particular venom to class-A designs, because it is obvious that the large heat sinks required take time to reach final temperature. So it is important to record that in class-A operation this design stabilises its electrical operating conditions in less than a second, giving the full intended performance.

No "warm-up time" beyond this is required.

Obviously the heat sinks take time to reach thermal equilibrium. But as already described, measures have been taken to ensure that component temperature has no significant effect on operating conditions or performance.

Supplying power

Regulated supplies are quite unnecessary, and are virtually certain to do more harm than a good unregulated power supply (**Fig. 4**).

The supply must be designed for continuous operation at maximum current, so the bridge rectifier should be properly heat-sunk, and careful consideration given to the ripple-current ratings of the reservoirs. This is one reason why reservoir capacitance has been doubled to 20,000μF per rail: the ripple voltage is halved, improving voltage efficiency as it is the ripple troughs that determine clipping onset. But the ripple current, although unchanged in total value, is now split between two components. (The capacitance was *not* increased to reduce ripple injection. This is dealt with far more efficiently and economically by making amplifier psrr high[3].)

Do not omit the secondary fuses. Even in these modern times rectifiers do fail, and transformers are horribly expensive...

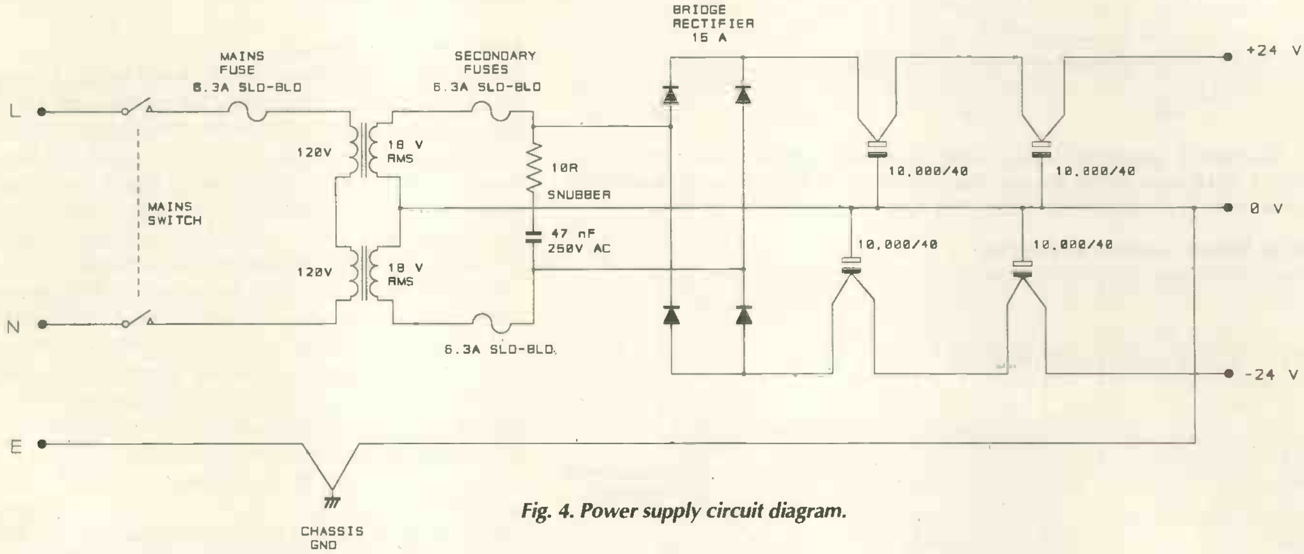

Fig. 4. Power supply circuit diagram.

ly greater than the Class-A I_q, and the controller will therefore intermittently take control in an attempt to reduce the average current to 1.5A. Disabling the controller by turning off Tr_{17} via R_{44} prevents this.

Test mode

If the Class-A controller is enabled, but preset Pr_1 is left in circuit, (eg by shorting Tr_{20} base-emitter) we have a test mode which allows suitably cautious testing; current I_q is zero with the preset fully down, as Tr_{13} over-rides the current-controller, but increases steadily as Pr_1 is advanced, until it suddenly locks at the desired quiescent current. If the current-controller is faulty then I_q continues to increase to the defined maximum of 3A.

Thermal design

Class-A amplifiers are hot almost by definition, and careful thermal design is needed if they are to be reliable, and not take the varnish off the Sheraton. Since the internal dissipation of the amplifier is maximal with no signal, simply turning on the prototype and leaving it to idle for several hours will give an excellent idea of worst-case component temperatures. In Class-B the power dissipation is very programme-dependant, and estimates of actual device temperatures in realistic use are notoriously difficult.

Table 1 shows the output power available in the various modes, with typical transformer regulation, etc; the output mode diagram in Part 1, Fig. 1, showed exactly how the

Table 1. Power capabilityof the trimodal power amplifier.

	W	W	W	Distortion
Load resistance	8Ω	6Ω	4Ω	
Class A	20	27	15	low
Class AB	n/a	n/a	39	high
Class B	21	28	39	medium

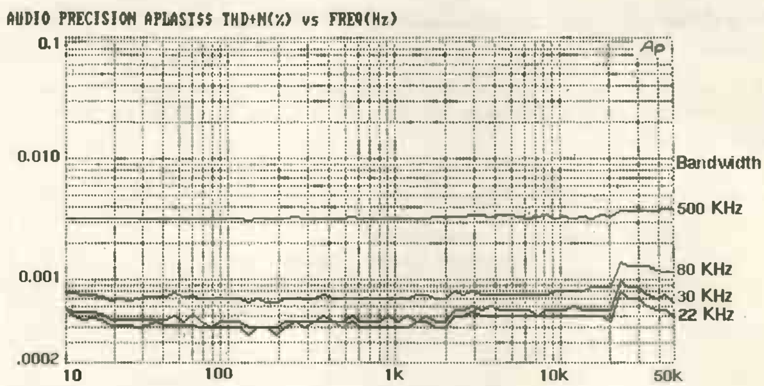

Fig. 5. Distortion plot of the Audio Precision oscillator/analyser combination alone, for measurement bandwidths of 500, 80, 30 and 22kHz. The saw-teeth below 1kHz are artefacts. The residual appears to be pure noise.

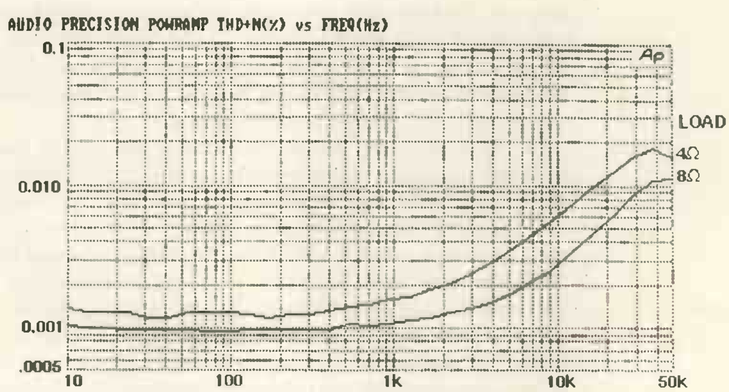

Fig. 6. Distortion in class-B (summer) mode. Distortion into 4Ω is always worse. Power was 20W in 8Ω and 40W in 4Ω, bandwidth 80kHz.

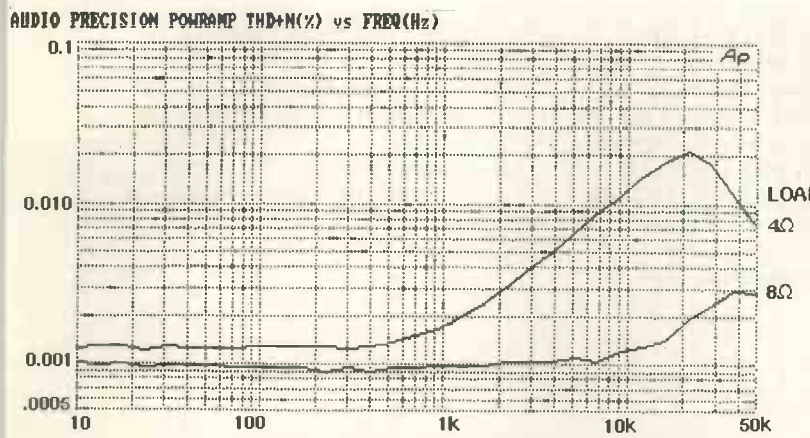

Fig. 7. Distortion in class-A/AB (winter) mode, same power and bandwidth. The amplifier is in AB mode for the 4Ω case, and so distortion is higher than for class-B8Ω. At 80kHz bandwidth, the class-A plot below 10kHz merely shows the noise floor.

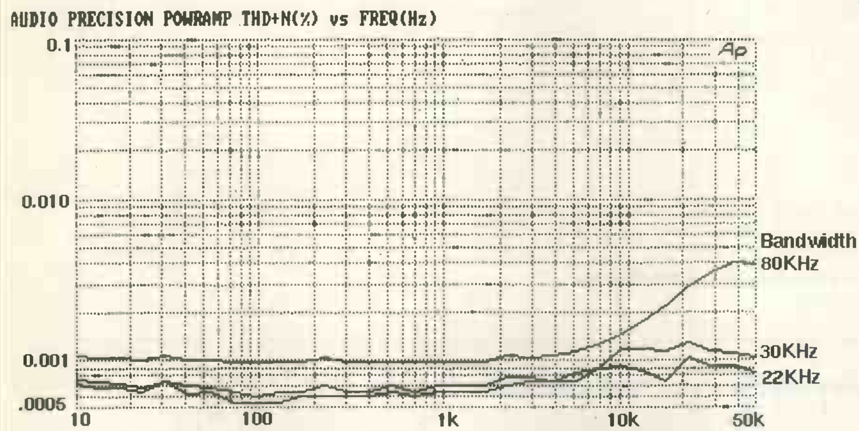

Fig. 8. Distortion in class-A only (20W/8Ω) for varying measurement bandwidths. The lower bandwidths ignore hf distortion, but give a much clearer view of the excellent linearity below 10kHz.

Table 2. Temperature considerations.

	Thermal resist °C/W	heat flow W	temp rise °C	temp °C
				100 junction
Juncn to to3 case	0.7	36	25	75 TO3 case
Case to sink	0.23	36	8	67 heatsink
Sink to air	0.65	72	47	20 ambient
Total			80	

amplifier changes mode from A to AB with decreasing load resistance. Remember that in this context 'high distortion' means 0.002% at 1kHz. This diagram was produced in the analysis section of *PSpice* simply by typing in equations, and without actually simulating anything at all.

The most important thermal decision is the size of the heatsink; it is going to be expensive, so there is a powerful incentive to make it no bigger than necessary. I have ruled out fan cooling as it tends to make concern for ultra-low electrical noise look rather foolish; let us rather spend the cost of the fan on extra cooling fins and convect in ghostly silence. The exact thermal design calculations are simple but tedious, with many parameters to enter; the perfect job for a spreadsheet. The final answer is the margin between the predicted junction temperatures and the rated maximum.

Once power output and impedance range is decided, the heatsink thermal resistance to ambient is the main variable to manipulate; and this is a compromise between coolness and cost, for high junction temperatures always reduce semiconductor reliability, **Table 2.**

This shows that the transistor junctions will be 80°C above ambient, ie at around 100°C; the rated junction maximum is 200°C, but it isn't wise to get anywhere close to this very real limit. Note the *Case-Sink* thermal washers are made from high-efficiency material. Standard versions have a slightly higher thermal resistance.

The heatsinks used in the prototype had a thermal resistance of 0.65°C/W per channel. This is a substantial piece of metal, and is expensive.

The complete circuit

The complete Class-A amplifier is shown in Fig. 3, complete with optional input bootstrapping but omitting any balanced-line input amplifier or gain control. The circuitry may look a little complex at first, but we have only added four low-cost transistors to realise a high-accuracy Class-A quiescent controller, and one more to implement mode-switching. Since the biasing system has been described above, only the remaining amplifier subsystems are dealt with here.

The input stage follows my design methodology in running at a high tail current to maximise transconductance, and then linearising it by adding input degeneration resistors $R_{2,3}$. These reduce the final transconductance to a suitable level. Current-mirror $Tr_{10,11}$ forces the collector currents of the two input devices $Tr_{2,3}$ to be equal, balancing the input stage to prevent the generation of second-harmonic distortion. The mirror is degenerated by $R_{6,7}$ to eliminate the effects of V_{be} mismatches in $Tr_{10,11}$.

With some misgivings I added the input network R_9, C_{15}, which is definitely *not* intended to define the system bandwidth, unless fed from a buffer stage; with practical values the hf rolloff could vary widely with the source impedance driving the amplifier. It is intended rather to give the possibility of dealing with rf interference without having to cut tracks. Resistor R_9 could be increased for bandwidth definition if the source impedance is known, fixed, and taken into account when choosing R_9; bear in mind that any value over 47Ω will measurably degrade the noise performance. The values given roll off above 150MHz to keep out uhf.

As a result of insights gained while studying the slewing behaviour of the generic/Lin configuration, I have increased the input-stage tail current from 4 to 6mA, and increased the voltage amplifier stage standing current from 6 to 10mA over the original circuit. This increases the maximum positive and negative slew rates from the basic +21, –48V/µs of reference 4 to +37, –52V/µs; as described elsewhere[2] this amplifier architecture is always assymetrical in slew rate. One reason is feedthrough in the voltage amplifier current source; in the original circuit an unexpected slew-rate limit was set by fast edges coupling through the current source c-b capacitance to reduce the bias voltage during positive slewing. This effect is minimised here by using the negative-feedback type of current source bias generator, with voltage amplifier collector current chosen as the controlled variable.

Transistor Tr_{21} senses the voltage across R_{13}, and if it attempts to exceed V_{be}, turns on further to pull up the bases of Tr_1 and Tr_5. Capacitor C_{11} filters the dc supply to this circuit and prevents ripple injection from the positive rail. Capacitor C_{14}, with R_5, provides decoupling. Increasing input tail-current also mildly improves input-stage linearity, as it raises the basic transistor g_m and allows $R_{2,3}$ to apply more local feedback.

The voltage amplifier stage is linearised by beta-enhancing stage Tr_{12}, which increases the amount of local feedback through Miller dominant-pole capacitor C_3, often referred to as C_{dom}. Resistor R_{36} has been increased to 2.2kΩ to minimise power dissipation, as there seems to be no significant effect on linearity or slewing. Do not, however, attempt to omit it altogether, or linearity *will* be affected and slewing much compromised.

As described in reference 3, the simplest way to prevent ripple from entering the voltage amplifier via the negative rail is old-fashioned *RC* decoupling, with a small *R* and a big *C*. We have some 200mV in hand (see Part 1) in the negative direction, compared with the positive, and expending this as the voltage-drop through the *RC* decoupling will give symmetrical clipping. R_{37} and C_{12} perform this function; the low rail voltages in this design allow the 1000µF capacitor C_{12} to be a fairly compact component.

The output stage is of the complementary feedback pair, or CFP, type. As described in Part 1, this gives the best linearity and quiescent stability, due to the two local negative feedback loops around driver and output device. Quiescent stability is particularly important with $R_{16,17}$ as low as 0.1Ω, and this low value would probably be rather dicey in a double emitter-follower output stage.

Voltage efficiency of the copmplementary feedback pair is also higher than the emitter follower version. Resistor $R_{25,26}$ define a suitable quiescent collector current for the drivers $Tr_{6,8}$, and pull charge carriers from the output device bases when they are turning off. The lower driver is now a *BD136*; this has a higher f_T than the *MJE350*, and seems to be more immune to odd parasitics at negative clipping.

The new lower values for the output emitter resistors $R_{16,17}$ halve the distortion in Class-AB. This is equally effective when in Class-A with too low a load impedance, or in Class-B but with I_q maladjusted too high. It is now true in the latter case that too much I_q really is better than too little – but not much better, and AB still comes a poor third in linearity to Classes A and B.

Safe operating area protection is given by the networks around $Tr_{18,19}$. This is a single-slope safe operating area system that is simpler than two-slope safe area, and therefore somewhat less efficient in terms of snuggling the limiting characteristic up to the true safe operating area of the output transistor. However, in this application, with low rail voltages, maximum utilisation of the transistor safe area is not really an issue; the important thing is to observe maximum junction temperatures in the A/AB mode.

An adaptive trimodal design?

One interesting extension of the ideas presented here is the adaptive trimodal amplifier. This would switch into class-B on detecting device or heat-sink over-temperature, and would be a unique example of an amplifier that changed mode to suit the operating conditions.

Thermal protection would need to be latching as flipping from class-A to class-B every few minutes would subject the output devices to unnecessary thermal cycling.

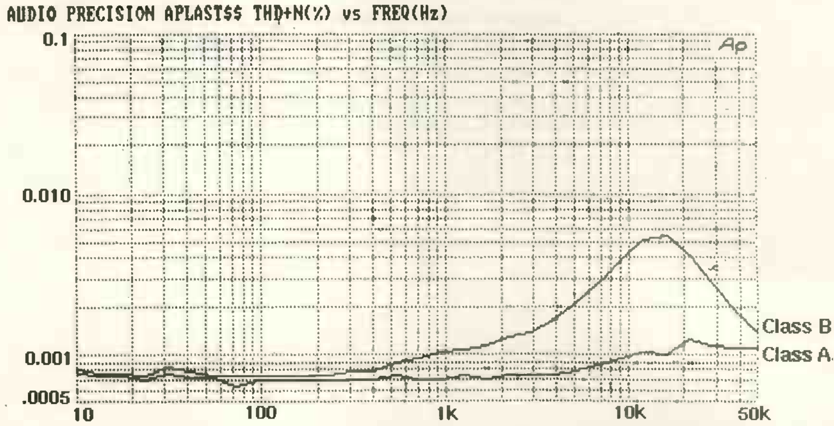

Fig. 9. Direct comparison of classes A and B (20W/8Ω) at 30kHz bandwidth. The hf rise for B is due to the inability of negative feedback that falls with frequency to linearise the high-order crossover distortion in the output stage..

The global negative-feedback factor is 32dB at 20kHz, and this should give a good margin of safety against Nyquist-type oscillation. Global negative feedback increases at 6dB/octave with decreasing frequency to a plateau of around 64dB, the corner being at a rather ill-defined 300Hz; this is then maintained down to 10Hz. It is fortunate that magnitude and frequency here are non-critical, as they depend on transistor beta and other doubtful parameters.

Performance

The performance of a properly-designed Class-A amplifier challenges the ability of even the Audio Precision measurement system. To give some perspective on this, Fig. 5 shows the distortion of the AP oscillator driving the analyser section directly for various bandwidths. There appear to be internal mode changes at 2kHz and 20kHz, causing step increases in oscillator distortion content; these are just visible in the thd plots for Class-A mode.

Figure 6 shows Class-B distortion for 20W into 8 and 4Ω, while **Fig.** 7 shows the same in Class-A/AB.

I would like to acknowledge the invaluable help and encouragement of Gareth Connor. Credit goes to him for the tricky task of pcb layout – and not me, as previous adverts have implied. ■

References

1. Self, D, "Distortion In Power Amplifiers; Part 8" *Electronics World & Wireless World*, March 94, p 225.
2. Self, D, "High Speed Audio Power", *Electronics World & Wireless World*, Sept 1994, p760.
3. Self, D, "Off the Rails" *Electronics World & Wireless World*, March 1995, p201.
4. Self, D, "Distortion In Power Amplifiers; Part 7." *Electronics World & Wireless World*, Feb 1994, p 139.

Notes on part 1

Regrettably, a couple of errors crept into the original article on Class-A[1]. On page 229, second column: "$Tr_{15,16}$ then compares the reference voltage with that at point Y" should read "at point X". On page 229, third column: "This comes to the same thing as maintaining a constant V_{bias} across Tr_5" should read "across Tr_{13}". This is nobody's fault but mine, and I humbly apologise as it cannot have made understanding the current-controller action any easier. ***D.S.***

591 TVA

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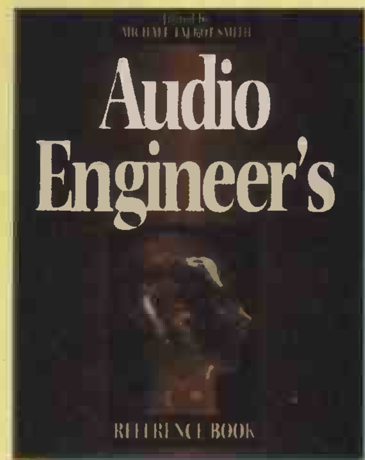

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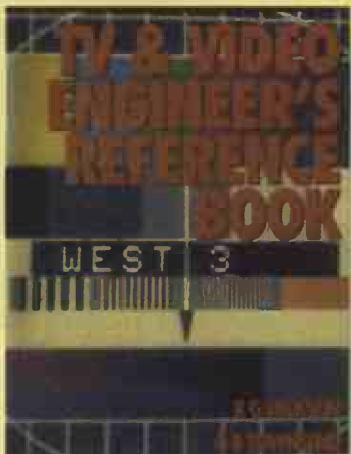

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LETTERS

Letters to *"Electronics World + Wireless World"* Quadrant House, The Quadrant, Sutton, Surrey SM2 5AS.

Emi still not understood

Laptop computers plunge planes into mid-air danger! In April the *Sunday Times* published a front page article with the above title suggesting that electromagnetic interference from personal computers and other electronic equipment used by passengers could interfere with the control and navigation equipment of modern aircraft. I think the issues raised warrant public debate.

I am a physicist and throughout my career have been involved with issues in the reliability of digital hardware and software. In the late 1970s I was working with CAM Consultants on the reliability of fast computer hardware. At that time we realised that interference problems – generally know as electromagnetic compatibility (emc) – were very poorly understood.

We were concerned that digital systems were finding increasing use in real time control applications where they would be vulnerable to catastrophic, though infrequent, failure. We were able to lay down guidelines which were propagated through our seminars and which, to some extent, helped to improve the situation.

Sadly, as emc standards were drawn up by bodies such as the Federal Communication Commission (and later incorporated into European emc standards), they failed to incorporate the sound principles we had developed and indeed are based on misconceptions of the nature of electromagnetic interference. A number of issues now arise:

1. The standards bodies need to explain why there is a need to ban computers etc from aircraft when they are compliant with the published standards designed to ensure compatibility.

2. The aircraft manufacturers should explain why we should have any confidence in the integrity of aircraft control systems which can be so easily affected. As an aside: how much electromagnetic energy is released by a thunderstorm and how can we be sure that the control and navigation systems are immune to this emi 'explosion' when they are clearly susceptible to the electronic 'whispers' emanating from in-cabin passenger equipment?

3. Will the CAA and other relevant government bodies please reassure us that they have given due consideration to the possible exposure to terrorist attack resulting from such vulnerable electronic systems?

Finally, if we can be sure that in-cabin passenger equipment is the source of the interference we must not make the mistake of simply banning it. Rather, we need to understand the problems and design reliable real-time systems. So, let us have some properly refereed tests carried out (on the ground!) to see whether the interference sources can be confirmed.

Dr David S Walton
Tyne and Wear

The right to ask questions

Reading your May Letters page, I was very pleased to see a missive from Ivor Catt. He comments on censorship, "publishable" material and other suppressed theories. He is, of course, right; as he always was. Way back when, in the real *Wireless World*, he outlined conundrums and puzzles which sat me back on my haunches, as he was clearly right and his thinking and reasoning was obviously on the right track. Questioning my night school tutors, I was never given answers, but told to read my text books; I never got reasoning a-la-Catt.

We now face a situation in the UK electronics industry which mimics textiles; the era of mass production is rapidly progressing to mainland China and will leave the West behind with only a waste disposal problem. Software experts are all well and good, but if you don't make 'something to sell, that the people want' you'll starve; and you can't eat microchips or software. Service industry is all well and good while someone is actually making the base product; but you can't service 'nowt'.

Your leader spells out a vision of a flagging, failing and faltering UK semiconductor industry; you are only just touching the truth with such comments. The real, live situation is a mass production industry on its knees, facing a challenge from labour exploitable nations worldwide. Useless, disconnected and unprofitable 'academics' supply the government with information. From that they generate decisions to propagate the future. Such bombastic, 'jobs-for-the boys' jerrymandering and fake wage generation can only bleed dry the industry that feeds them.

Ivor, for god's sake, start writing letters to *EW+WW* again; I miss your openness and frankness.

Peter Thornton G6NGR
Oldham, Lancashire

False assumption on mains changes?

Nigel Cook (Letters, May) has considered the problem caused by the Cenelec harmonisation document HD 472 S1:1988 from the point of view of an engineer. As a result he has made a false assumption with regard to the power supplied to consumers of mains electricity.

In fact the reduction of the low voltage electricity supply from a nominal 240V to a nominal 230V in this county has been carried out solely by legislators. Such people can change voltage without changing transformer taps or reducing delivered power. The Electricity Supply (Amendment) (No 2) Regulations 1994 [SI 1994 No 3021] alter the low voltage supply tolerances set in the Electricity SuppLy Regulations 1988. Previously the permitted 240V supply variation was plus or minus six per cent; now the 230V supply variations are plus ten per cent or minus six per cent. It will be noticed that ten per cent on 230V is the same as six per cent on 240V

Plus ca change, plus ca meme chose (as they say in Bruxelles).

Guy Selby-Lowndes
Billingshurst, West Sussex

...or not?

Nigel Cook's letter in the *EW+WW*, May, rightly points out some of the domestic consequences of reducing standard mains voltage from nominal 240V to 230V. However, the effects are more significant than he suggests. At the moment the supply may vary some seven per cent up and down from nominal 240V giving a voltage range between 223 and 256. A shift to 230V nominal will give a range of 214 to 246.

I monitor the mains voltage here continuously, and find that it stays in the narrow band of 235 to 242. This has not always been so. Some years ago we found 240V light bulbs lasted only a few days, because the voltage seemed always over 250. The MEB put a voltage recorder on our domestic supply for a week. This showed a minimum of 250 and a maximum of 285!

The problem was caused by domestic users in this rural area taking less electric power for heating and cooking by changing to lpg and oil-fired systems, which dramatically reduced the voltage drop on the overhead 240V supply system. Needless to say, the local distribution transformer tappings were quickly altered.

Although 230V is the new Euro-standard, inspection will show that many pieces of imported equipment like fridge and freezer compressors are already wound to 220V to cut copper costs. I'm told by service engineers that most of the motors they replace are 220V types where the wattage effect of the extra 20V causes early burnout in hot summer weather.

The only short term consumer benefit I can see from lowering the voltage will be the increased life of incandescent lamps (albeit at reduced emission) – a drop of 10 per cent in voltage doubles filament life – that is until the 240V bulb becomes a thing of the past in the rush to save tungsten...Time to stock up!

Anthony Hopwood
Worcestershire

The right to provide answers

At the risk of being still further misinterpreted, I would like to clarify a central point that appears to have been overlooked in discussions concerning the Establishment's 'suppression' of non-orthodox ideas and theories.

It is simply this: orthodox science is not, and does not claim to be 'Right' with a capital R. To paraphrase Arthur C Clarke, the universe is not only stranger than we imagine, it is probably stranger than we can imagine, and the best that we can do is to formulate workable approximations to reality (whatever it may be).

Pete Davies
Birmingham

Newtonian trap

I fear that Mr Lerwill (*EW+WW*, April) has fallen into the well-worn trap that catches out so many of us from time to time – that of trying to apply Newtonian thinking to a non-Newtonian situation.

Newton's second law is in essence the law of conservation of momentum. Only in the situation where one assumes, as Newton does, that mass is invariant does this result in the velocity remaining unchanged. Thus to assume as Mr Lerwill has done that the velocity remaining unchanged is directly contrary to what he says about the electron.

In order to obey the conservation of momentum, as the mass increases, the velocity has to decrease – as the text-books say it does. Perhaps they could have explained it better.

Alan Watson
Mallorca, Spain

Absence of proof

Mr Wheeler's response in your May issue to the question I posed in your April issue seems to have missed the point on several counts.

No scientific laws are provable; there are only those which we have been unable to disprove. While it would be unproductive to question the validity of well-established laws in familiar circumstances, when any new circumstance arises which might have implications for the assumptions behind the workings of a law, its validity in these new circumstances cannot be inferred by its demonstrated reliability in the old circumstances. It has to be tested.

Mr Wheeler does not say which particular laws he thinks my proposition would violate, but I am assuming they are Newton's laws of motion. Central to Newton's laws of motion is the concept of the conservation of mass. Newton defines force both as rate of change of momentum and as mass times acceleration. These two quantities are only the same if mass is assumed to be constant. This assumption has been called into question by Relativity. In fact anyone who has studied and accepted Special Relativity will know that Newton's equations of motion can only be an approximation, valid when relative velocities are low.

Contrary to what he says, the effect described would not be very small compared to others occurring at the same time. Even in the oscilloscope set-up I described, it would amount to several per cent of the electron's upwards momentum. The reason the measurable effect is so small is because the electron's momentum is so small to start with.

There may be a flaw in my proposition, but I am sure it is not the one described. To start with, the question I am posing concerns all bodies with a velocity in a y axis that are accelerated along an x axis. They do not have to be charged. I am only suggesting the use of charged particles like electrons because it is easy to accelerate them to the required velocities and so be able to carry out experiments. It should in any case be clear that electrodynamic effects cannot balance the relativistic increase in upwards momentum because momentum depends on the mass of the charged particle whereas electrodynamic forces do not.

Finally, may I point out that while I am interested in theoretical views on this subject, the purpose of my letter was to ask whether any experimental work had been or could be applied to this question.

R Lerwill
Castle Mills, Chirk Clwyd

Hostile elements

In answer to your correspondent Nicolas Holliman (*EW+WW*, May, p 435). Yes, it's not surprising that "some components such as LEDs corroded and broke down after being exposed to the elements for a period of five weeks", especially after being left by a busy London road and in quite a lot of rain.

Seriously though, acid rain or no, the outside world is exceedingly hostile to the proper working of electronic apparatus, a fact first forcibly brought home through the failure of equipment in harsh climates during the Second World War. The subject has received extensive attention since then, as a trawl through the INSPEC/IEE abstracts would show.

Outside installations need to be fully encased in suitable enclosures, with gaskets on lids and windows, 'O' rings and rubber boots on switches and with suitable splashproof or waterproof connectors. Water will even find a way into good enclosures by diffusion and through atmospheric pressure change, and reserves of 'drierite' or other proprietary drying agent may be obligatory. As a last resort, pressurising with dry nitrogen or total 'potting' in suitable compounds may offer a solution. On an everyday level, the use of generous clearances including air-space insulation and PTFE 'stand-offs' help with high-impedance signals, as do insulating lacquers. Batteries can pose problems in sealed containers, releasing corrosive gasses which cause havoc with contacts – they are best isolated in separate compartments.

Temperature is of vital importance – will the casework be white or black? Will it need to be shaded from the sun? Battery performance is drastically affected, particularly at low temperatures – will extra capacitive decoupling help with pulsed loads? Will individual temperature coefficients balance out, add, or multiply to cause disaster? Semiconductor gain is badly reduced at low temperatures. Many years ago, my father found that his pukka electrocardiograph would not work in the morning after being left in the boot of the car over a cold winter night.

What else can go wrong? Watch out for large slugs walking over the photovoltaics. Oh yes, and piles of bird droppings. I think I prefer the acid rain.

Dr T C H Going
Southend

Looking to build a better dynamo

I am a keen cyclist and have spent some time trying to make a decent dynamo-based lighting system. Dynamos that you can buy over the counter are designed to produce 3W into a 12Ω load over a wide speed range and are, unfortunately, good at this. Why unfortunately? Well, 3W is enough to give you a bright front or rear light but not both. I have found, through experience, that 5 – 6W at the front and 2 – 3W at the back reduces the occurrence of those "I didn't see you" incidents to reasonable limits. The other thing about bikes dynamos is that output is regulated by making them lossy. This makes them inefficient – hard work – at high speed. Is there a way to extract more power? Do you know of another type of small electrical machine that I could use as a generator? I can design and build any number of electrical circuits, but could write all I know about electromagnetic machines on a postage stamp.

Steve Bush
Epsom

Regarding mosfets

Reading recent articles it seems opinions are divided on the verdict on mosfets. Here are some of the characteristics of mosfets:

The obvious disadvantage is the linearity compared to bipolar transistors. However, there are mosfets that feature linearity as good as conventional bjt_1. The Hitachi *2SK213*, although not suitable for output stages, makes very good driver stages due to its good linearity, bandwidth and high V_{ds}. Price also seems to be a drawback. (Pity I haven't got the V_{gs}–I_d curves)

The main advantage of mosfets must be the negative temperature coefficient. If used at drain currents above the Q point, there is no need to apply thermal coupling or feedback. This reduces complications involved in designing a suitable bias network.

Output impedance for mosfets will be $1/g_m$ if used as source followers. This means there is no need to drive the output stage with a low impedance. Usually input stages and drive stages give output impedance around 2kΩ or higher. As most output devices have low g_m, around 40, the open loop output impedance would be too high to control the speaker. Using mosfets avoids this problem – this only needs concern when designing zero global feedback amplifiers.

In Japan there are people who prefer the sound of mosfets used in the output stages. Such people acknowledge the linearity problem and such like, but still prefer the 'mosfet sound'. This is pretty much up to individuals and is purely subjective.

If you look at the recent Technics hi-fi brochures, they state that mosfets are used for driving the bipolar output stages. They claim to combine the linearity of the mosfets with the current capacity of the bpt. If this is true, they must be using very good mosfets indeed – maybe the *2SK213* mentioned above.

Why doesn't Mr Self use J-fets for the input stage? By using J-fets instead of transistors, the input capacitor can be removed. There are various devices, such as the *2SK117* which offer very low noise and high enough gain. How about trying current feedback amplifiers? The current feedback amplifier is supposed to offer constant bandwidth regardless of gain/feedback levels. Also, if you look through *Hi-fi World* magazine, it offers a pair of very linear output bipolar transistors. Apparently these were designed for audio purposes and out perform anything on the market.

From the hi-fi magazines I have been reading for five years in the UK, Japan and the US it seems that the type of distortion is very important. They say that even order harmonics are benign, whereas the odd ones may add a shrillness and sharpness to the sound. There are large numbers of people who support the sound of valve amps. The better sounding ones seem to employ single-ended output stages and do not use a differential input stage. Push/pull operation and differential amplifiers, if used correctly, cancel second order harmonics, but double third order harmonics. This may be the reason why so many modern transistor amplifiers sound sharp and shrill compared to the valve counterparts. Modern valve amps can sustain the full 20–20kHz, so bandwidth is probably not the reason for the valve smoothness.

During a two hour session at a hi-fi shop with two friends, I could only detect small differences between three amplifiers. The three are competently designed; which raises the question of what caused the differences in sound. Is it due to the three amplifiers having different capabilities, or was I hearing the differences in the amplifier/loudspeaker interface? Output impedance and the ability to drive low impedance differ from one amp to another, independent of distortion levels. Surely these affect the amplifier/speaker interface more than the distortion content?

I admire the articles written by Mr Self. The designs do not use exotic and expensive devices that are hard to source. They are all sound engineering practices not always pursued by manufacturers. Please keep up the good work.

Koji Kiyokawa
Derby

Douglas Self replies

I thank Mr Kiyokawa for his kind comments. Since he raises many points I hope he will not mind if I only answer a selected few of them.

I do not see why the negative temperature coefficient of V_{gs}/I_d in mosfets should be an advantage; it may give more security against thermal runaway, but this really should not be a problem in modern times. The use of silicon bjts, particularly in the CFP output configuration, makes thermal runaway virtually impossible in a competently designed amplifier

My understanding is that a typical mosfet only has a negative temperature coefficient at reasonably high drain currents, and at low currents it goes positive. Since the positive coefficient only manifests itself at these low currents,thermal runaway is still guarded against, but surely this variable-sign coefficient must make thermal compensation of the biasing extremely difficult?

Perhaps the point here is that a bjt output stage has not only a consistent temperature coefficient, but also a very well-defined and clearly visible bias which gives minimal crossover distortion. A fet output stage has much more latitude in bias simply because there is no such optimal point – just a range of varying shapes of crossover non-linearity. No bias value is obviously right. This means that there is no point in worrying over getting the thermal compensation exact.

I feel there is every need to drive an output stage from a reasonably low impedance, so the non-linear input impedance of the output stage does not cause distortion in the previous stage (Distortion 4 on my list). In the case of bjts it is the base currents that cause the trouble – with fets it seems to be the large and signal-dependent gate-input capacitances

There may well be individuals that prefer 'the mosfet sound', if such a thing really exists, as there are those who clam to prefer 'the valve sound' or the 1922 directly-heated triode sound. The latter two are perhaps explicable, as second-harmonic distortion has been claimed to make things sound nicer, but it is hard to see the subjective attraction in crossover distortion; I would have thought that the 'mosfet sound' could only manifest itself in this way. I have always considered that audible crossover distortion was about the worst fault an amplifier could suffer from.

Single-ended stages tend to be inefficient, non-linear, and generally bad news. If generating lots of second harmonic distortion is felt to be a good thing, why not do it at low-level, (with a diode or two) where the exercise is going to be much cheaper? Personally I have no use for an amplifier that generates audible distortion of any kind.

I do accept that the nature of harmonic distortion can be important if it is audible, and that, for example, second harmonic is benign compared with third. However, to extrapolate from that and say that high-order even harmonics are more acceptable than high-order odd harmonics is very questionable; and this is of course the sort of distortion that amplifier crossover non-linearities generate. There has also been speculation that the exact rate at which the various types of harmonic fall off with increasing frequency has a complex significance beyond the generally accepted rule that higher order is worse. The only harmonic-weighting scheme that has received anything like acceptance is the n^2 approach, which says that the third harmonic is $^9/_4$ times worse than the second, and that the fourth is $^{16}/_9$ times worse than the third, and so on, presumably until our hearing gives out. This is hard to reconcile with the statement that high-order even harmonics are always nicer than high-order odd harmonics, and shows that this is one area that really could benefit from a good deal more psychoacoustical research.

However, my design approach is to avoid these questions altogether. Rather than worry about the nature of the distortion, I have aimed to reduce it in total amplitude to such an extent that no matter what its composition is, it cannot plausibly be said to be audible. This approach may be thought to lack finesse or sonic correctness, but it is difficult to deny its effectiveness in making an accurate amplifier.

Impossible curves

In the May issue of *EW+WW* (p387) Mr Self suggests "that it is an established fact that mosfets...are a good deal less linear than bjts". His proof: the "wingspread" curves of his ref 2.

I do not know where these curves originate, but one thing is clear: they do not agree with presently known physical reality. Maybe they are the result of some technical blunder, perhaps from a less than perfect PSpice macro.

Evidence for my claim is provided by Mr Self's own Fig. 3. The curve 'g_m' shows a remarkable linearity up to: V_g=3V and I_d=10A. Thus, the mosfet has a square-law characteristic, say $I_d=K_1\,(\Delta V_g)^2$ giving

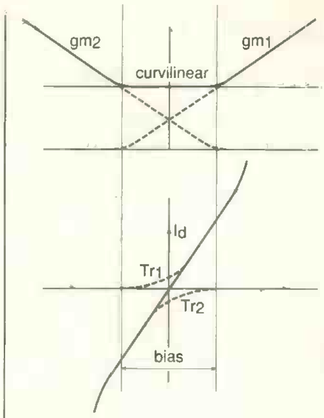
$$g_m = \frac{dI_d}{dV_g} = 2k_1 x\Delta V_g$$

Consequently the square-law for that transistor is accurate to 10A! Note that in Fig. 3 the g_m curve is ever increasing, with no down-fall. The is typical for all kinds of fets.

The Fig. 13 curves reflect the gain of the output stage, which is $g_m \times R_{load}$ (slightly reduced by emitter degeneration). Then it is impossible for these curves to have the shape they are supposed to have in Fig. 13. A peak in the middle, with dips on both sides, cannot be in agreement with g_m from Fig. 3. Qualitatively speaking, g_m is proportional to the wingspread gain, (see above) and g_m shows no dip.

Fig. 13 is definitely non-existent as described. A better argument for the superiority of the bjt is needed.

Again, Mr Self has given a clue to the real wing-shape. It is a horizontal line, flanked by tilted straight lines, as jotted down by me. Directions: for a mosfet pair, draw the two g_m curves from Fig. 3, one reversed, with overlap equal to bias voltage, and you will find the "curvilinear" straight cross-over characteristic with constant g_m. This curve is by no means as complicated as the wingspread, but it has the advantage of being in agreement with reality.



Top - linear g_m curves have constant cross-over gain. Source output impedance is linear, equal to $1/(g_{m1}+g_{m2})$ in this range, corresponding to the 'Curvilinear' characteristic in the second digram. The single mosfet gain increase (the wings) is also linear. Bottom – mosfet characteristics are the integral of those above. Current is shared between $Tr_{1,2}$ in a way that produces linear output current.

A consequence of this is that there is no "best linearity" bias. The linear cross-over range is ever increasing with the bias current. Choosing a specific idling current is a matter of taste, where distortion can be traded for power dissipation, up to Class A.

But there is more to it, which I discovered when I was developing a set of design formulae for mosfet amplifiers. I calculate distortion products with a current sources – a natural way to drive the high impedance gates. Surprisingly enough the non-linear square-law area produced less distortion than did the linear cross-over – just the opposite of what one would expect. This, rather natural, property will have an impact on the ideas in mosfet design. The current driver will produce a very high gain, approaching infinity at low frequencies and makes a very low distortion level possible, which is confirmed by tests.

Regarding my super-symmetric design, I will not make any comments. It has to prove itself on its own merits. I just want to state, that in this design, like in any mosfet amplifier, the g_m change is entirely dependent on the amount of bias used. My amplifier is a pure embodiment of a typical mosfet stage, since the transistors are identical square-law types, which are directly acting on the output, with no load feedback (direct drive).

I think we ought to discuss amplifier design in a more unbiased way, and I invite Mr Self to do this, which most likely will forward the audio science.

Bengt G Olsson
Saltsjo-Boo, Sweden

Douglas Self replies

Readers may perhaps know that I have written an article analysing Mr Olsson's allegedly "super-symmetric" output stage, which will hopefully be appearing later this year, and I don't really want to anticipate this by discussing it in detail at this stage. Suffice it to say that my wingspread diagrams seem to match those of Robert Cordell, and I think they are correct. You can certainly get a nice flat centre-section if the bias is sufficiently advanced, but this is because you are now running in class A in that part of the plot.

My point is that the bjt output stage not only has about ten times better general linearity, but an obvious position of optimal Class-B bias that can be clearly seen to minimise the crossover distortion in the thd residual. However, in a Class-B or AB fet amplifier there is no such minimum, and as Mr Olsson says "choosing a specific idling current is a matter of taste"; this is not an approach that has much appeal to me.

I have several points of disagreement with other parts of the letter, but these are all fully dealt with in my article, and so I would ask readers to be patient until it appears.

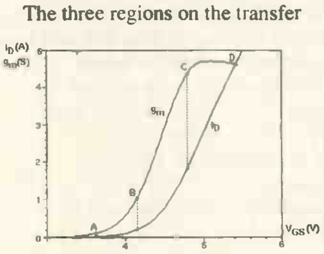
more mosfets

With reference to Douglas Self's recent article in your magazine – Fets versus bjts, May – I would like to point out that some of his statements about the characteristics of power mosfets seem to contradict various manufacturers' data books.

Douglas Self acquired his results by using computer simulation of electronic devices. In one of his figures (Fig 3, page 388) he shows the forward transconductance of a fet and states that "there is no question that fet transconductance increases in a beautifully linear manner". And, in accordance with this statement, the graph shows a perfectly linear relationship between g_m and V_{GS}. So much so that one becomes suspicious whether this perfect linearity is only an assumption of the program modelling the device. And in fact, if we examine the transfer characteristics of power mosfets, we see a very different picture.

Measured I_D (V_{GS}) and g_m (V_{GS}) Characteristics of an IRF 530 mosfet

The three regions on the transfer



characteristic curve of a power mosfet [1].This Figure shows the typical $I_D - V_{GS}$ and $g_m - V_{GS}$ relationship of a power mosfet. Here I would refer to [1], which discusses the transfer characteristics of power mosfets in detail. The book distinguishes between three major regions on the characteristics of power mosfets. Region A to B is the sub-threshold region, where the relationship between V_{GS} and I_D is exponential. Region B to C is where the well-known square-law relationship is valid. The book states: "One can see that the transconductance increases linearly with V_{GS} in the square-law region, but then levels off to a constant value in the velocity saturated region" (Region C to D). In addition, it should be noted that above a certain drain current the transconductance droops off again. Douglas Self's graphs do not show region C to D at all. Nor do they show the behaviour in the initial sub-threshold region, where the $V_{GS} - I_D$ relationship also does not follow the square-law.

Data books from other manufacturers seem to confirm the validity of the above described model. For example, [2] contains the forward transconductance characteristic of several hundred power mosfets and none of them seem to have a "beautifully linear" $g_m - V_{GS}$ relationship.

Furthermore, Douglas Self writes: "the PSpice simulation shown was checked against manufacturers' curves for the devices, and the agreement was very good – almost unnervingly so". I wonder if any physical device is really capable of showing such perfect square-law characteristics as Douglas Self's IRF 240 – the majority of them seem to follow a much more complicated relationship.

Laszlo Gaspar
Nottingham Trent University

References:
1. MOSPOWER Applications Handbook. Siliconix Ltd, 1984. (ISBN 0-930519-00-0), p 3-3.
2. PowerMOS Transistors. Philips Semiconductors (Data Book SC13), 1991.

Douglas Self Replies

As Mr Gaspar says, I did indeed check the simulation output against manufacturers' published data, and found very good correspondence: in this case the source was Harris Semiconductors. I thought it not unreasonable to assume that the manufacturer knew how his own devices worked. In particular, the manufacturer's graphs for I_{drain} versus Vgs look very much like my Fig. 2 up to 20A, which is actually just outside the continuous current maximum rating for the real device.

For the record, the PSpice simulation model here is a Level-4 bsim model that includes body effect, transverse-field mobility degradation, and velocity saturation sensitivity, and is widely accepted as accurate enough for use when millions of dollars of IC investment are based on the outcome. However, I do not claim to be an expert on simulator fet models, and so I had better leave it there.

The real question is: would acceptance of Mr Gaspar's alternative gm curve make the fet look more linear than the bjt? As far as I can see it makes it less linear if anything, and so I stand by my conclusion that a bjt – with a little emitter degeneration to bring down its g_m to fet levels – will always be the more linear device.

Feedback on feedforward

I would like to thank Mr Self for his appreciation and comments on my recent article on a feed-forward error-correction audio power amplifier technique[1].

I am grateful to him for his constructive criticism which gives me the opportunity to provide some additional considerations to the content of my paper.

Mr Self is right in noting that the practical circuitry ends up being more complex than conventional amplifiers. This, on the other hand, was clearly stated in my paper (see paragraph "Feed-forward more promising?"), although the very aim of my work was to demonstrate that the improvement achievable from this technique can be worth the extra circuit complexity and cost. However, the main point to stress is that 'feed-forward' is not proposed as an alternative to 'feedback'. On the contrary, it is intended to be applied to audio power amplifiers as a complement to feedback in order to achieve – when required – levels of distortion probably unattainable with feedback only, mainly in class B/AB amplifiers.

As for the main power amplifier circuit configuration (Fig 8 in the article), it is not to be considered my suggested choice for a true low distortion feed-forward amplifier.

I agree with Mr Self that better results in terms of distortion can be achieved by using, for instance, some of the techniques and suggestions given by himself in his comprehensive series of articles about distortion in power amplifiers[2], and others proposed by E M Cherry in well known articles and recently in *EW+WW*[3].

However, it has to be pointed out that the demonstration prototypes were conceived and assembled (1988-1991) with the aim to prove – first of all to myself – the effectiveness and viability of the feed-forward error correction technique in a wide range of both different output stage bias current and load conditions.

Therefore I decided to make use of a class B power amplifier configuration capable of providing good phase margin and overall stability over the whole output voltage/current range and on the following conditions:

- output stage bias current setting range: from 0mA to 300mA
- load impedance *(R//C)* range: (2 to 10)Ω//(0 to 2)μF.

Fig. 8 has the above characteristics and was chosen for this purpose.

However, some degree of frequency over-compensation turned out to be needed to reach the goal. As a result, C_0 was set to 100pF, leading to a distortion performance of the main amplifier which is not excellent, as properly noted by Mr Self, especially at high frequency.

Lower distortion can be achieved by the same configuration via optimised frequency compensation (C_0= 60pF) for a fixed output stage total bias currently of about 300mA and a load impedance of 8Ω in parallel with no more than 0.33μF, and, eventually, incorporating suggestions from E M Cherry[3].

This would lead to a complete feed-forward amplifier with proportionally lower distortion than 0.004% at 20kHz, as reported in the article – actually 10 to 20dB better.

Providing an optimised feed-forward amplifier design was not the aim of my paper, but I have been working on such a task.

I would also like to provide some explanation for why a cascoded jfet input stage was used in the schematic of Fig. 8 instead of a standard bjt stage, despite the worse matching characteristics of jfet pairs.

Apart from the results provided by R R Cordell in his well known article[4], and by other authors, which prove the benefits associated with jfet input stages, as well as of mosfet output stages, there is one more reason why I have a tendency to employ a differential jfet input stage in some amplifiers: it eliminates the distortion induced by non-linearities in the base current of bjts due to the following causes:

- β dependence on the operating conditions of transistors (I_c and V_{ce})
- the Early effect.

Bipolar transistor base-current induced distortion is often overlooked, while, in my opinion, it can constitute an important source of distortion in amplifiers (it should be considered a root cause of distortion to be added to the seven examined by Mr Self[2]. This is mainly true when bjts are operated at relatively low emitter current densities, for which β variations are usually larger, and when the dynamic

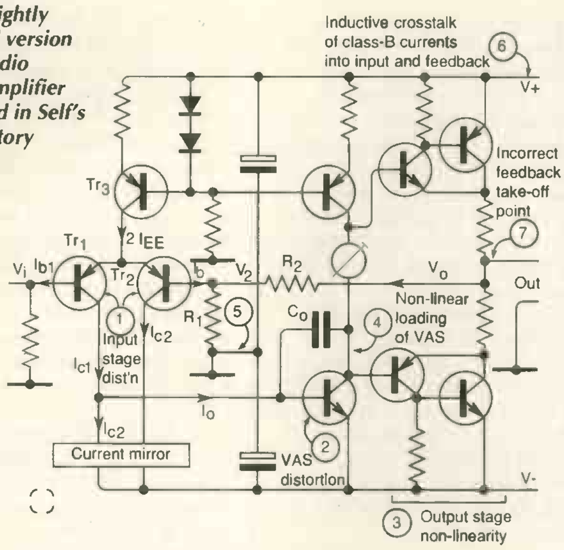


Fig. 1. Slightly modified version of the audio power amplifier presented in Self's introductory article.

variations of the collector or current are a large fraction of the bias current. Both the above conditions normally apply to standard bipolar input stages.

There are effective techniques to counteract this kind of distortion. Among them:

- the use of low impedance level both in the input signal sources and in the feedback network, or the use of buffers in front of Tr_1 and Tr_2.
- the reduction of the input stage transconductance g_m (g_m V_T/I_{EE} in Fig. 1, where V_T=25mV @ 290K is the thermal voltage).
- use of appropriate bias current compensation, mainly in ICs.
- the use of specifically designed differential bjt input stages[5];
- the use of a differential jfet cascoded input stage (eventually boot-strapped to reduce the Early effect-induced distortion).

To the best of my knowledge, the influence of input stage bias current on amplifier distortion was dealt with and worked out to any extent in only a few works [5,6].

The influence of the base current non-linearities on the closed loop voltage gain A_{Cl} of the amplifier, can be evaluated by determining its sensitivity to the incremental current gain $A_C = \Delta V_0/\Delta I_b$.
Its formal expression is

$$S_{A_c}^{A_{cl}} = \frac{A_c}{A_{cl}} x \frac{\partial A_{cl}}{\partial A_c}.$$

Referring to Fig. 1, which represents a slightly modified version of Fig. 2 of Self's introductory article[1], the source of V_1 is supposed to have zero internal impedance, so we can ignore the effects due to I_{b1} and take into account in our analysis Tr_2 base current I_b only.

Assume the following: $\Delta I_b/\Delta I_0/2\beta$, $A_V=\Delta V_0/\Delta(V_1-V_2)=f_T/f=g_m/(2\pi f C_0)$. This is a good approximation for an amplifier with a dominant pole (f_T is the unity gain frequency), and $A_C=A_v\beta/g_m$. The above sensitivity can then be calculated as,

$$S_{A_c}^{A_{cl}} = \frac{f}{f_T} \times \frac{g_m R_2}{\beta(1+R_1/R_2)} = \frac{2\pi f C_0 R_2}{\beta(1+R_1/R_2)}$$

Let us consider, as an example, the following case: β=200, C_0=100pF, R_1=0.5kΩ and R_2=10kΩ.

For f=20kHz the sensitivity of A_{cl} to the amplifier incremental current gain variation turns out to be 6.10^{-4}. This means that a change of 10% in β will produce a corresponding variation in A_{cl} of 0.006%.

If we now inspect the circuit of Fig. 1, where Tr_1 and Tr_2 are normally biased at a low current density (I_{EE}=1-2mA), we see that I_0 is mainly used to drive the compensation capacitance C_0. That means that at the upper side of the audio frequency range, where the ratio $\Delta I_o/I_{EE}$ can be as high as 0.5 even in well designed amplifiers, you can expect β variations higher than 10%, depending on the bjt types used. As a consequence, higher values of deviation from linearity can be expected.

The amplifier deviation from linearity discussed so far does not translate directly into figures of the thd of the same amount.

Nevertheless it throws some light on the importance of base current-induced distortion in bjt input stages, and accounts for the benefits of using j-fets (preferably cascoded and boot-strapped).

As for the input-injected technique, I think that Mr Self refers to the techniques which were first proposed by Klaassen[7] and Hawksford[8], and subsequently applied by Cordel[14] to correct the distortion of the output stage of class AB power amplifiers. I think that these techniques can really prove effective in reducing the distortion in feedback amplifiers. However, both entail the incorporation of additional negative and/or positive feedback loops – to be carefully balanced. This could lead again to the well known limitation of feedback, namely dynamic instability problems.

True feed-forward techniques, on the other hand, do not suffer from such problems, because they operate outside the feedback loop of the main power amplifier. This fact offers the designer the possibility of an iterative application, as shown in Fig. 2, for confining distortion below measurable level. Distortion reduction ranging from 50 to 70dB could be theoretically attained by a two step iteration, even for distortion components a high as 1MHz. Similar results are theoretically possible with feedback only, yet almost insurmountable stability problems, I think, have to be faced and worked out.

Finally, the remaining problem to be clarified, in order to understand the real potentiality of the proposed feed-forward technique, is the order of magnitude of the lowest achievable residual distortion (ie with $V_e \geq 0$ at the input of the auxiliary amplifier) due to cross-modulation between the main and the auxiliary amplifiers under high load current conditions.

Personally I am convinced that this residual distortion should be less than 0.0001% in the full audio frequency range. This conviction is based on the following considerations. Referring to the figure in the box 'Magnetic flux concellation' of my article[1], consider the maximum output peak current $I_p=V_p/R_0$, which is flowing into the secondary winding of the transformer, while V_2 is coerced to zero by feedback. The auxiliary amplifier, in order to neutralise the flux in the transformer has to force a current $I_p=I_p/n$ into the primary winding and, consequently, produce an output-voltage $V_1 = RI_p/n$, where $n=N_1/N_2$. Practical values are R=5Ω and n=30, so we can expect values of V_1 less than $1.6V_{peak}$ for I_p<10A.

Now consider that amplifier A_2 is operated in class A and drives an equivalent load equal to $R_{eq}=R_0 n^2$ in parallel with the primary inductance L_1. In the prototypes L_1=400mH and n=30, so that R_{eq}>1.8kΩ for R_0>2Ω which is high enough to allow low distortion operation. Problems can only arise at very low frequency, where the reactance of L_1 is as low as 50Ω at 20Hz. However, the available open loop gain of the auxiliary amplifier is so high at low frequency that driving L_1 without producing distortion should not represent a major task. Therefore, even assuming a conservative distortion component V_{1d} not better than $0.1\%V_1$ (=1.6mVpeak in the above worst case conditions), this would entail a distortion voltage at the secondary winding V_{2d} equal to $V_{1d}/n=0.05mV_{peak}$. This value, if compared with a corresponding peak output voltage V_{0peak}=40V across a 4Ω load, yields a peak distortion of about 0.000125%. ■

Giovanni Stochino
Italy

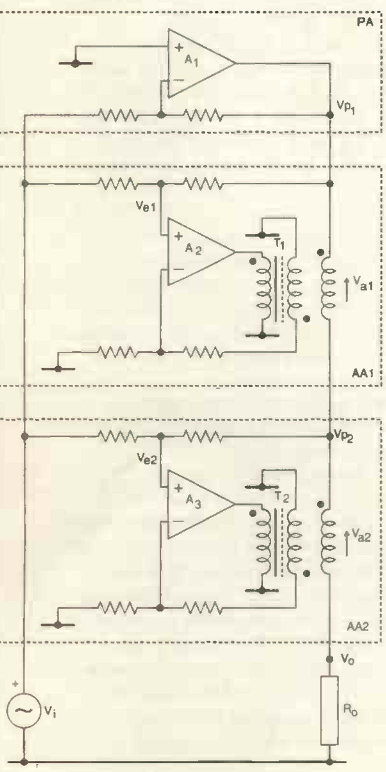


Fig. 2. Operating outside the feedback loop of the main power amplifier, true feed-forward offers designers the possibility confining distortion to unmeasurable levels.

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8. M J Hawksford 'Distortion Correction in Audio Power Amplifiers', *JAES* Jan/Feb 1981, p27-30.

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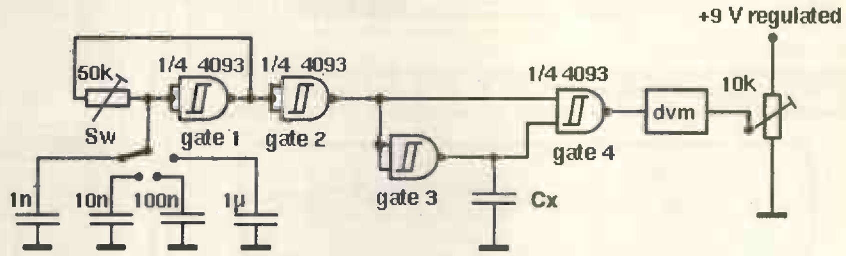
Capacitance meter for a DMM

In conjunction with a voltmeter, this circuit gives a direct reading of capacitance.

Two of the four gates in a *4093* Schmitt Nand form an oscillator and buffer, the frequency being set by the 50kΩ trimmer. Output goes to gate 4, one of whose inputs is inverted and delayed by the unknown component by time proportional to its value. At the output of gate 4, normally high, a negative-going pulse with a width proportional to the capacitance appears, the duty cycle of the output and, therefore, the average voltage indicating the value of capacitance.

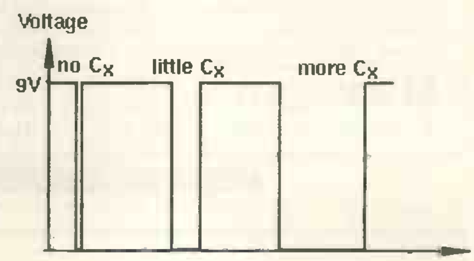
To calibrate, set the dvm to its 2V range and remove C_x, adjusting the 10kΩ trimmer for a zero reading (a very narrow pulse is present in this condition due to the inherent delay of gate 3). Connect a known capacitor in the C_x position, set the frequency switch and adjust the 50kΩ trimmer for the correct value.



Single-chip capacitance meter measures values in the pF-μF range.

Range is from a few picofarads to several microfarads. Supply voltage stability is required for accuracy and the oscillator capacitors must be exactly in the ratio 1:10:100:1000.

Rae Perälä
Helsinki
Finland



Zero-crossing detector copes with varying line voltage

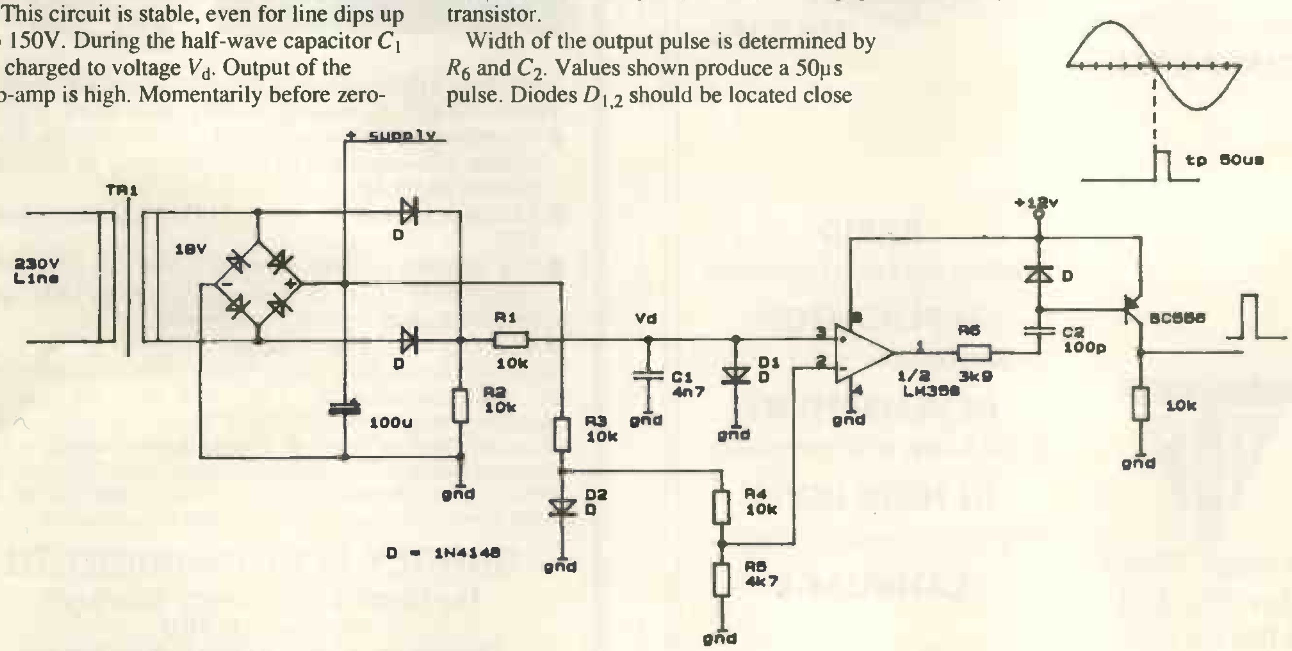
Most power-line zero-crossing detectors show phase shift if mains voltage is not constant. For synchronising an audio tape-recorder to the mains, I needed a zero crossing-pulse that was independent of any mains voltage fluctuations and distortion.

This circuit is stable, even for line dips up to 150V. During the half-wave capacitor C_1 is charged to voltage V_d. Output of the op-amp is high. Momentarily before zero-crossing takes place, C_1 starts to discharge through $R_{1,2}$.

After time $T=C_1(R_1+R_2)$, V_d falls below the voltage of pin 2 of the *LM358*. Now the output swings down and creates a base current pulse, through R_6 and C_2 for the pnp transistor.

Width of the output pulse is determined by R_6 and C_2. Values shown produce a 50μs pulse. Diodes $D_{1,2}$ should be located close together so that they will have the same temperature. This avoids thermal drift of the zero-crossing pulse.

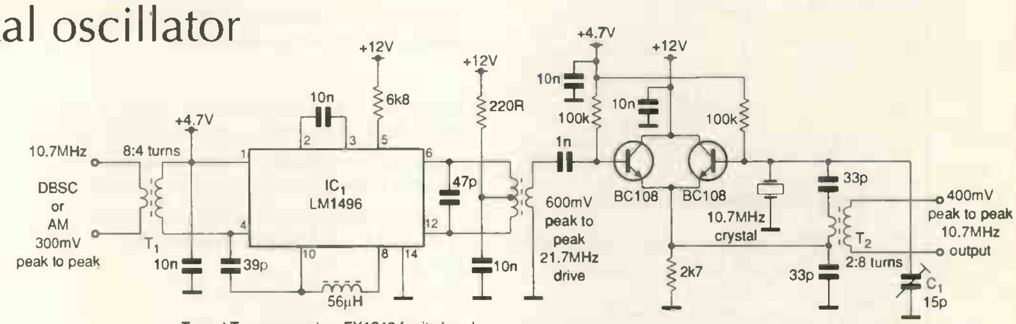
Ernst Schmid
Munich
Germany



Synchronising a crystal oscillator

It is possible to synchronise a crystal oscillator – in phase – to an amplitude modulated signal near to its resonant frequency. The IC doubles frequency of the incoming modulated signal. This is then injected into the crystal oscillator to provide synchronisation drive.

I use the oscillator output in a further circuit, not shown here, to demodulate the signal using another *LM1496* double-balanced modulator. With a 600mV 21.4MHz peak-to-peak drive to the oscillator from the doubler, the circuit provides a lock-in range of ±500Hz. This proved useful for demodulating both DSBSC and AM digital signals – provided that their carrier frequencies didn't drift beyond the lock range of the oscillator.



T_1 and T_4 are wound on FX1242 ferrite beads
The output from the oscillator is taken by sampling the crystal current to reduce the harmonic content

The inherent frequency stability of the crystal-controlled oscillator enables it to be locked easily by adjustment of C_1.

Colin Bamforth
Altrincham
Cheshire

Using a frequency doubler, it is possible to lock a crystal – in phase – to an amplitude-modulated signal.

Simple current transmitter for thermometry

Temperature measurement often requires remote reading indication, the sensor output being transmitted in the form of a 4-20mA current. Commercial current transmitters can be expensive; this circuit is simple and costs much less.

An *LM3911* IC contains a 10mV/°C voltage source, a 6.8V reference and an accessible op-amp; with the addition of a few passives and one transistor, the circuit becomes a temperature-controlled current source.

Resistor R_1 in series with the parallel combination of R_a and R_b, and $R_{2,3}$ set the current gain to give a 16mA span for temperatures between –20°C and 80°C, R_5 allowing zero setting with negligible effect on sensitivity. Resistor R_L, at the indicator end of the line, converts the current to voltage, any differences between the two grounds having no effect on the reading while Tr_1 is conducting.

A 24V supply and R_4 limit supply current to 1mA to minimise local heating; in still air, the circuit takes a few minutes to respond to changes. Accuracy after a single-point calibration is around ±1°C.

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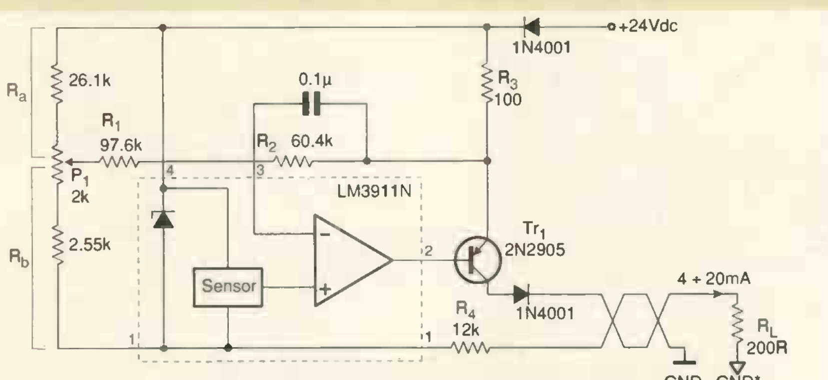
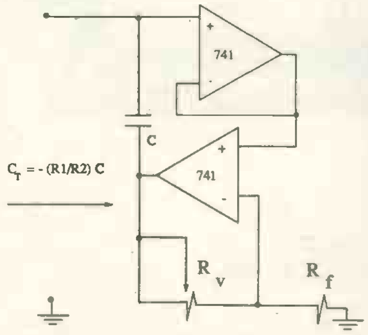


Current transmitter provides remote reading of temperature simply, at low cost and at ±1°C accuracy in the –20°C to 80°C range.

Bipolar programmable capacitor

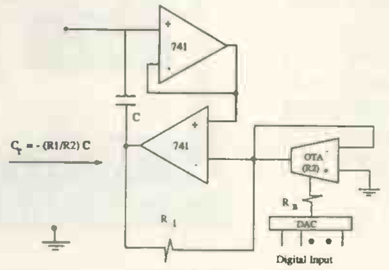
Development of an idea by Dunn* produces a digitally programmable positive/negative capacitor.

Originally as shown in **Fig.1**, the circuit becomes the arrangement of **Fig.2**, in which R_v is replaced by a fixed R_1 and R_f by the active resistor circuit composed of the operational transconductance amplifier. For example, R_1 is 25kΩ and



Original programmable capacitor.

R_2, the OTA resistance $1/g_m$, is variable between 50Ω and 50kΩ. Capacitance is found from,
$C_T=C[1-(R_1/R_1+R_2)]=-C(R_1/R_2)$
and C_T is inversely proportional to R_2. The conductance of the OTA is $g_m=I_B/2V_T$, in which V_T is the thermal voltage of 25mV, and $C_T=-C(I_b/2V_T)R_1$. Total negative capacitance is therefore controllable by I_B. If digital programming is



New digitally programmable featuring positive or negative capacitance.

required, a d-to-a converter adjusts the OTA tranconductance and therefore the capacitance. Adding a positive capacitor in parallel with the circuit produces a digitally programmed positive/negative capacitor.

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Saudi Arabia

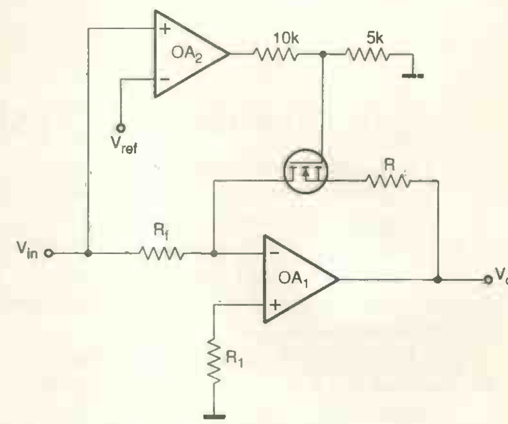
Reference
Dunn. *Electronic Design*. December 5, 1991.

Linear/non-linear amplifier

A control voltage determines whether this amplifier operates in a linear manner with a gain of about R/R_f or in a non-linear mode with open-loop gain.

If Vref is greater than Vin, the comparator OA2 switches the mosfet off and the circuit is non-linear; a smaller Vref turns the mosfet on, whereupon the amplifier receives feedback and is linear. Changing the input polarities of OA_2 reverses the effect of V_{ref}.

K N Sunil Kumar
Visakhapatnam
India



Amplifier behaves as a high-gain, non-linear circuit or as a lower-gain, linear type, depending on control voltage.

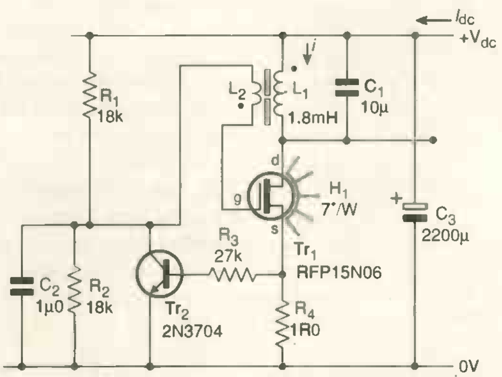
Amplified autobias

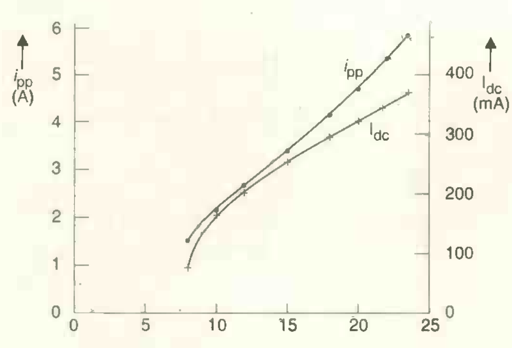
While similar in principle to automatic valve bias using a decoupled resistor, this bias loop for a low-frequency mosfet oscillator provides gain in the loop and a low reference voltage at the base/emitter junction of Tr_2. Increase in current through R_4 causes Tr_2 to take more current and pull down the junction of $R_{1,2}$, the mosfet gate.

Oscillator transistor Tr_1 operates stably and efficiently with the tank connected as shown at a frequency of 1.1kHz and with an output of 58V pk-pk on a 24V supply. Voltage waveform at Tr_1 drain is as would be expected from a Class C circuit: rounded during cut-off and flat during conduction. However, the tuned circuit provides a relatively clean output current waveform. With a turns ratio of 10:1, oscillation starts when the supply is around 7.5V, and the amplitude of the output current waveform is proportional to supply voltage.

As the diagram shows, at 24V supply, supply current I_{dc} is about one sixteenth of the oscillation current I_{pp}. Mount the transistors close together for best dc stability.

CJD Catto
Cambridge

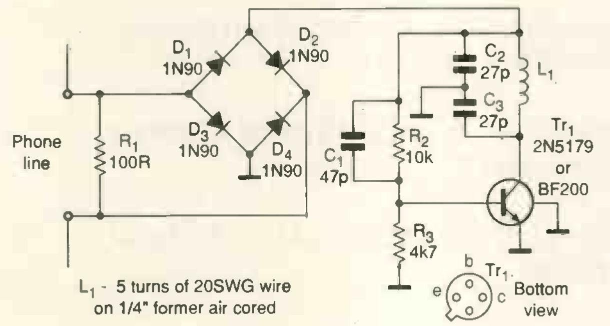




Gain in the source bias loop provides stable operation and efficiency in this low-frequency power oscillator.

Remote monitor for private exchange lines

Telephone conversations can be heard on an fm receiver via this simple transmitter. The circuit comprises a Colpitts oscillator, based on 2N5179 or BF200, that derives its power from the telephone line.



A 100Ω resistor stops the circuit interfering with the telephone line. Performance is low and the range is about five to ten metres, but no antenna is required.

Diodes $D_{1\text{-}4}$ form a bridge rectifier to produce a varying dc voltage according to audio signal on the line. Oscillation is at the resonant frequency of L_1, C_2 and C_3 which should be 92 to 95MHz.

It may be necessary to increase or decrease the inductance of L_1 slightly to bring the frequency of oscillation in the range of fm receiver. This may be done by squeezing the turns of L_1 closer or pulling them apart.

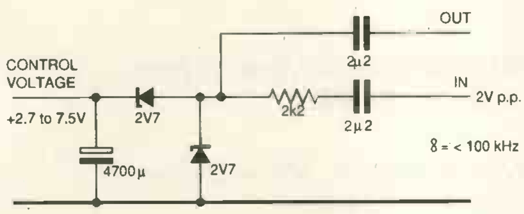
Raj Krishna Gorkhali
Asian Commercial Enterprises, Nepal

Electronic attenuator

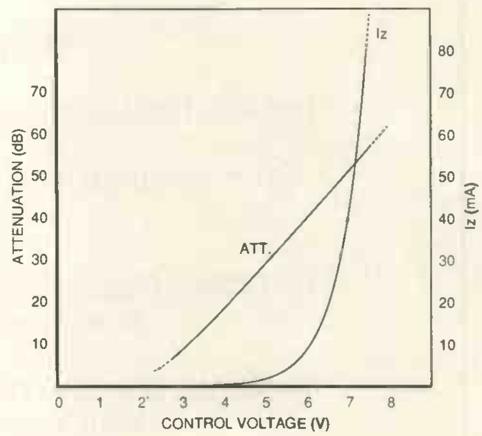
Although 2-3V zener diodes make inefficient voltage stabilisers, they can work well as attenuators.

In the circuit shown, attenuation is from 6dB to 58dB as control voltage varies from 2.7V to 7.5V, with a zener current between 42μA to 77mA. If the control voltage is to exceed 7.5V, a current-limiting resistor is needed.

D Di Mario
Milan
Italy



Zener attenuator controls signals of up to 100kHz over a 50dB range. Injecting signal at mid-point of two zeners reduces distortion.



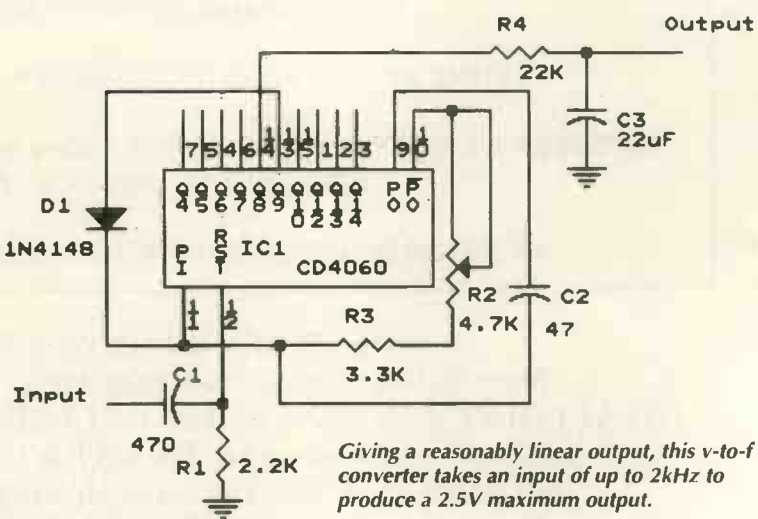
Single-chip voltage-to-frequency converter

Offering an input range of a few Hz to 2kHz, this v-to-f converter uses a single IC, the *CD4060* cmos 14-bit binary counter.

An internal oscillator in the *4060* takes a signal from the Q_9 binary output, which switches the oscillator on and off. Input signals are differentiated by R_1C_1 to allow a very narrow reset pulse to start the oscillator, so that there is only one pulse from Q_8 during an input signal period.

If the width of the pulse on Q_8 is t_1 and the input signal period $1/f_{in}$, the duty cycle of the Q_8 pulse is t_1f_{in}, a supply of 5V giving an output voltage of $5t_1f_{in}$V, and since t_1 is constant, output is proportional to frequency. Resistor R_2 adjusts the span; 1V/kHz is obtainable.

Yongping Xia
Torrance
California
USA



Giving a reasonably linear output, this v-to-f converter takes an input of up to 2kHz to produce a 2.5V maximum output.

Monitoring heartbeat

Worried about your heart? Baki Koyuncu* brings you a cheap monitor that puts an ecg in your pocket.

*Baki Koyuncu is in the Elec Eng Dept, King Fahd University, Dhahran, Saudi Arabia.

Many heart rate monitors on the market today are able to display heart pulse rates. Unfortunately they are not cheap. But it is possible to design an inexpensive monitor that can be as efficient as any of the commercial monitor units, with a PC interface that allows heart rhythm wave-forms to be stored and later analysed.

The system consists (**Fig. 1**) of a pair of probes and their differential amplifier, filters to clear the received probe signals and a frequency-to-voltage converter to convert the pulse rate frequency to a dc voltage. For displaying heart pulse rates, an lcd unit and its interface ic is also used.

Circuit description

Two pressure-sensitive miniature circular transducers are used as probes. One probe is attached to the upper part of the chest on the left hand side, and the other to the lower part. Each probe is placed in a circular adhesive contact pad, with electrical contact to the skin maximised by a jelly lubricant placed between the skin and the probe contact surface.

Both probes are connected to an instrumentation amplifier formed around three ics, IC_1, IC_2 and IC_3 (**Figs. 2a and 2b**). Probe one is also connected to an astable oscillator – the test signal generator – through spdt switch *SW*.

Amplification of the heart-beat signals is through the instrumentation amplifier circuit which also inhibits the noise picked up by the probes. All amplifiers are biased by +4.5V.

Amplified output signal of IC_3 is passed to capacitor filter *LMF*10, the first half of which is configured as a notch filter to attenuate 50Hz mains. Other frequencies are amplified by around a factor of ten.

Second half of the filter is configured as a low pass circuit, enabling frequencies below 50Hz to be used because of the low frequency of heart-beat signals. The filter's signal frequency mode is adjusted for 50Hz operation with an external 5kHz astable oscillator built around a *555*.

Following *LMF*10, a variable gain amplifier is formed by IC_5, to vary the signal gain between 10 and 500.

Two series diodes and a 1μF capacitor rectify the incoming signal and feed it to comparator circuit, IC_6. Every time the heart beat signal is above the +4.5V reference voltage at IC_6 input, the comparator output goes high corresponding to a heart beat, and a led is included at IC_6 output to display the beats.

Individual pulse lengths vary from patient to patient at different heart beats so a monostable *4538* is used as a pulse shaper. Its effect is to act as a pulse-length standardiser and produce equal pulse lengths for every patient.

Output from IC_6 triggers the *4538* and makes its output go high for a fixed duration set by 1M and 100nF. The monostable is not retriggered again during this period..

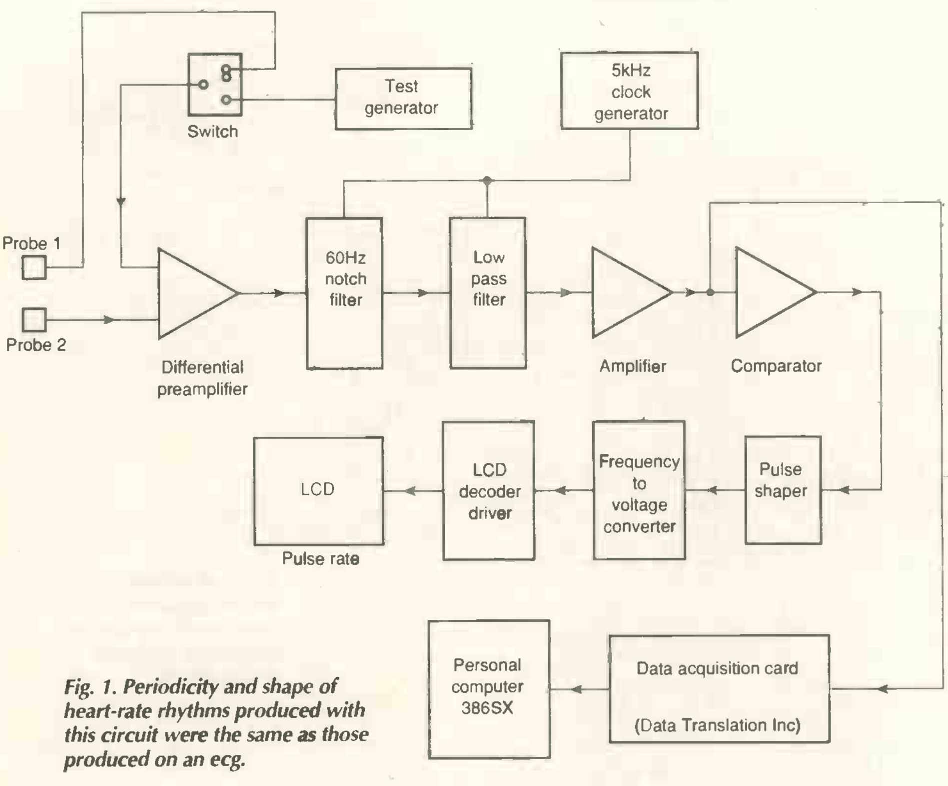


Fig. 1. Periodicity and shape of heart-rate rhythms produced with this circuit were the same as those produced on an ecg.

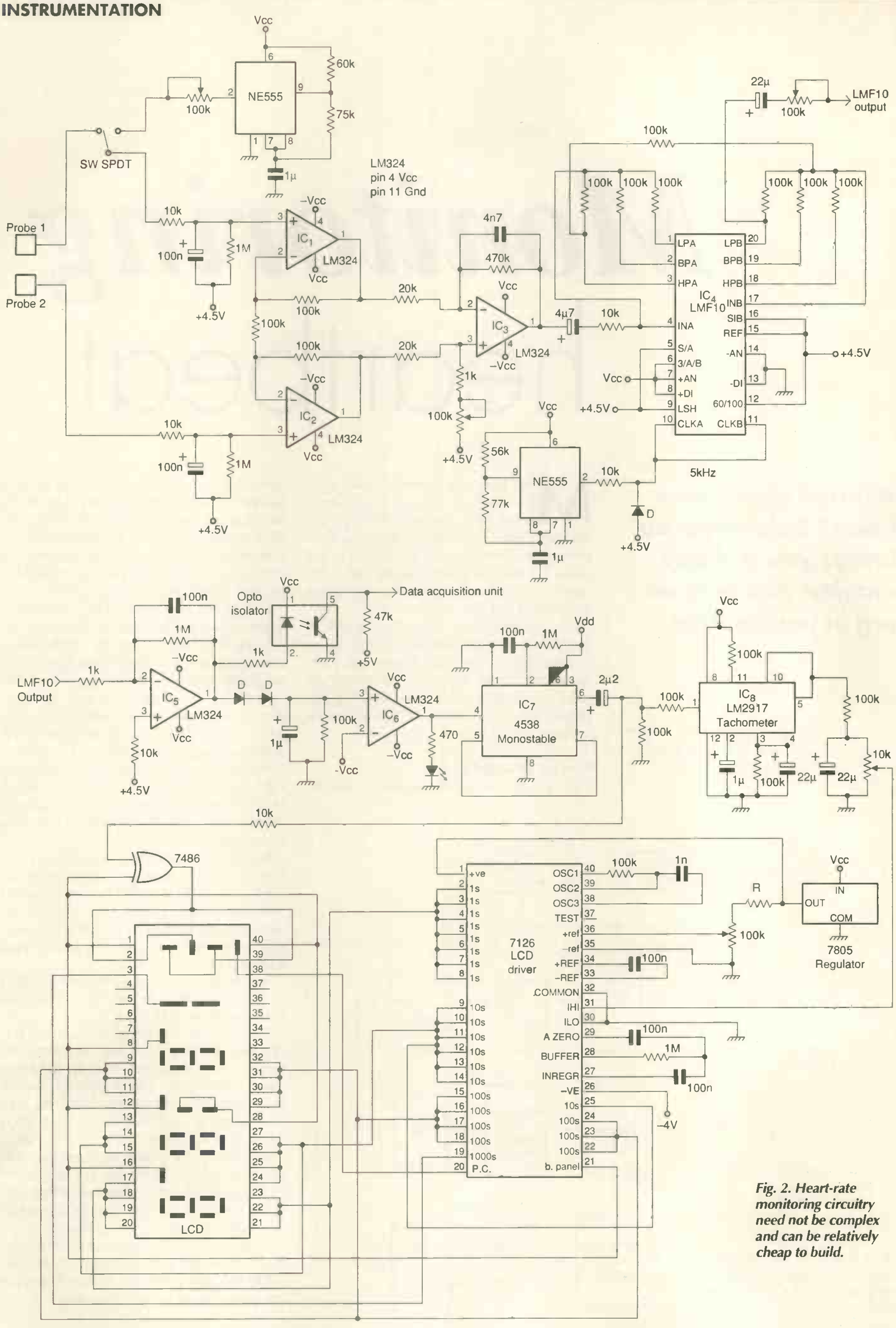


Fig. 2. Heart-rate monitoring circuitry need not be complex and can be relatively cheap to build.

Equal length pulses at the *4538* output are applied to an *LM2917* frequency-to-voltage converter which turns the input pulse rates into a dc voltage. This is fed to lcd driver *7126*, a digital panel meter *IC*, to decode the dc voltage from the *LM2917* into an equivalent digital output format to drive a 3.5 digit lcd.

The dc voltage representing the heart pulse is compared to a reference voltage of 1V at the +ref pin of *7126*, producing a calibration factor of 1mV input voltage/digit increment. Digital panel meter IC contains an internal clk generator with its frequency subdivided by internal counters to produce a signal sampling rate of one sample per 2s.

Heart rate uniformity

Patient's pulse rates are numerically displayed by the lcd in terms of pulse beats per minute and each pulse beat also triggers a plus symbol on the lcd, monitoring the uniformity of the heart rate.

On/off state of the plus symbol is determined by phase of the signal applied to it, a signal generated by X-or gating the *4538* output and the lcd's backplane clk When 4538 output is high, the X-or gate inverts its output signal phase with respect to the lcd's backplane clk and turns on the symbol.

An additional low-frequency square-wave oscillator test circuit is built around a *555* to check operation of the heart rate monitor (Fig. 2a). Oscillation frequency is preset between 20pulses and 200pulses/min, and the oscillator output is applied to IC_1 input through spdt switch *SW*, instead of probe one.

In this mode, the signal is only amplified through the IC_1 path, the other path through IC_2 being held at reference level of +4.5V. The test circuit is used to check the lcd readout against the pulse rate of the test circuit. A match between the oscillator generated pulse rate and the lcd read out verifies correct operation of the circuit.

Operation is from a V_{cc} = 9V supply provided by a 9V battery with a 20 mA supply current, making the monitor portable, though a mains adaptor can be used instead*.

PC interface

To observe the heart rhythm wave forms and compare them with the standard ecg wave forms, we use a PC interface. DC output voltage of the IC_5 amplifier is interfaced to an a-to-d channel of a data acquisition card using an opto-isolator circuit (Fig. 2b). The opto-isolator provides the computer with further noise isolation from the system, and the *DT2801* card from Data Translation is placed into one of the PC i/o ports.

Output voltage from IC_5 is converted into digital form by a 12bit a-to-d converter on the card and stored in a data file in ascii form in PC memory.

Lotus *123* can make use of this file to display heart rhythm wave forms on the PC.

Measured pulse widths with the heart rate monitor are around 0.85s, producing a nominal pulse rate of 71beats/min.

Comparing heart rhythm wave-forms, **Fig. 3**, with those taken via ecg devices shows that the periodicity and shape of the heart rhythm wave forms are the same for both ecg recordings and the heart monitor. ■

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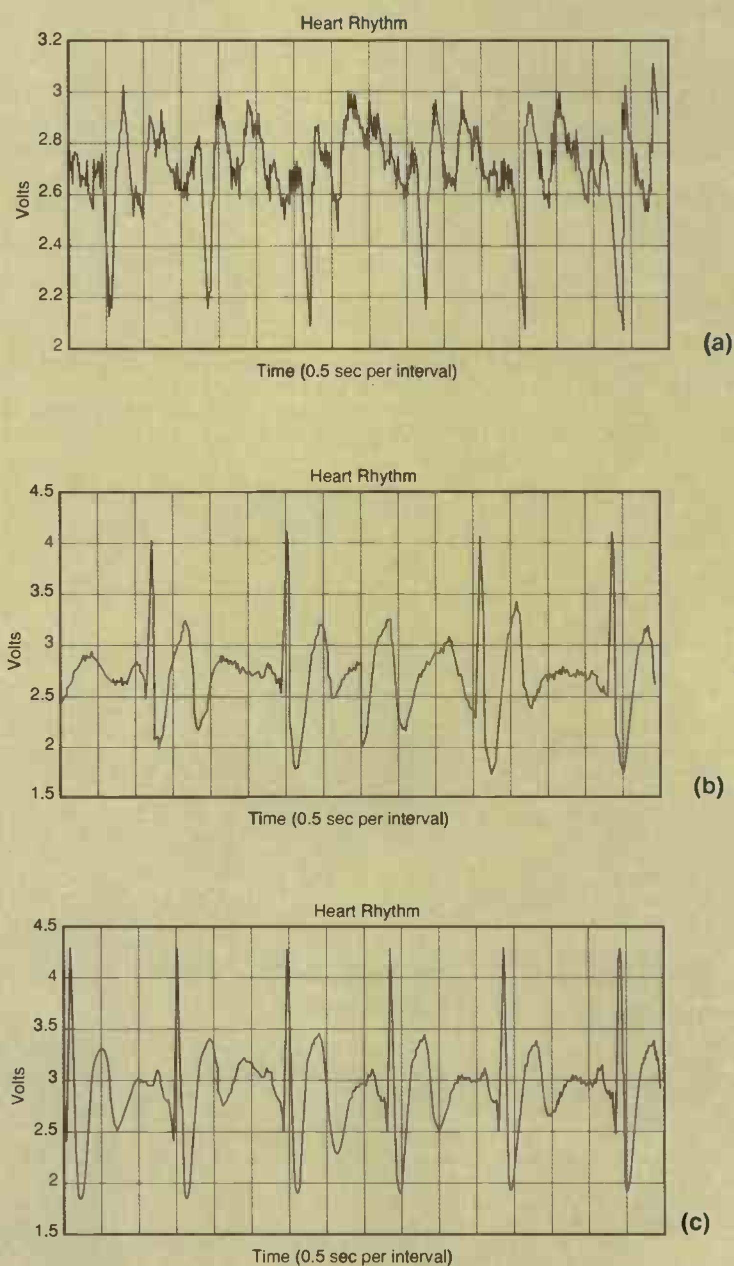
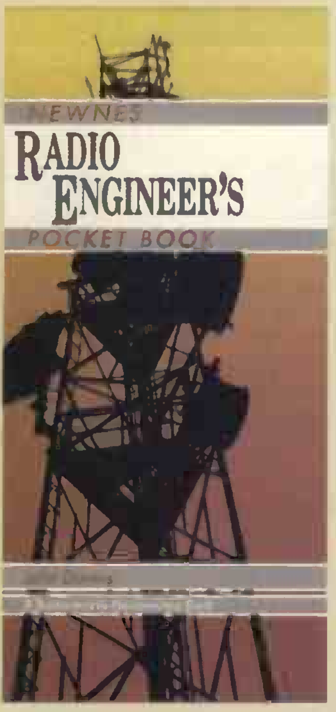
2. Moris Mano, *Digital Design*, Prentice Hall.
3. Sedra and Smith, *Microelectronic Circuits*, HRW Saunders, International Edition.

*In this application, any mains adaptor used must meet the medical safety requirements apropriate to your country – Ed.

Fig. 3. Sample heart rhythms from the heart rate monitor.





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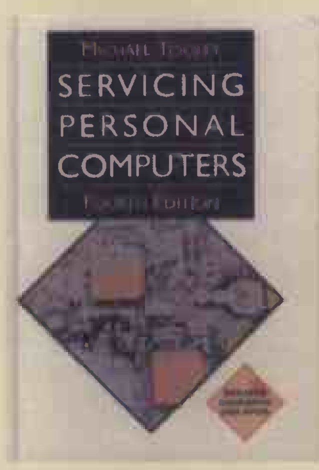

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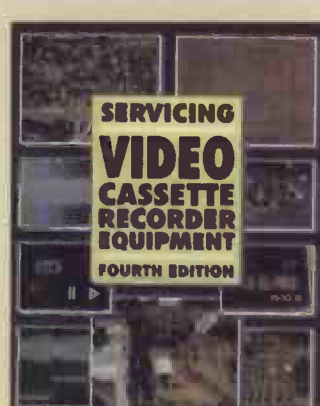

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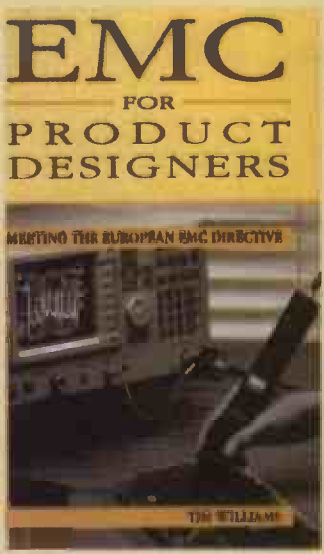

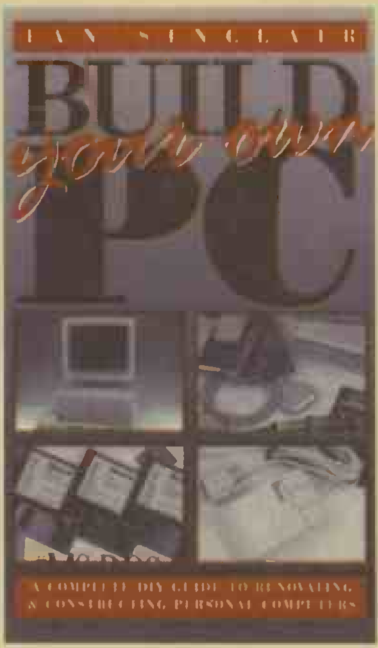

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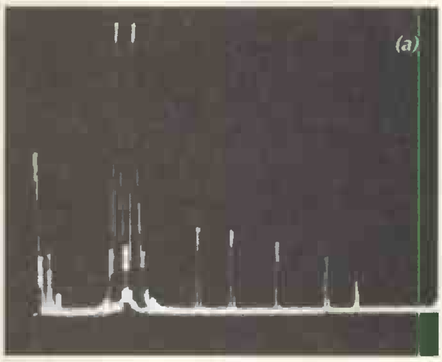
Modulating *linearly*

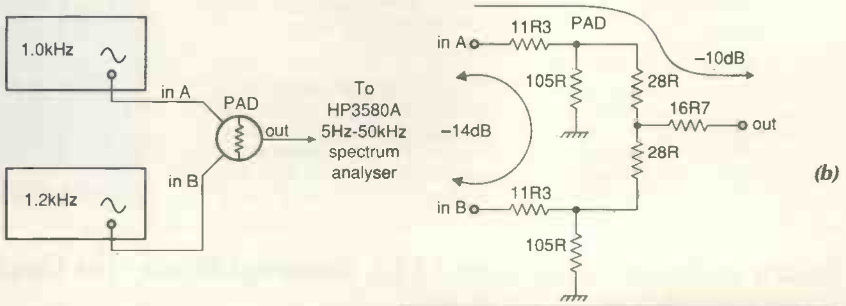
Due to crowding in the radio spectrum, it is vital to reduce third-order intermodulation in rf modulators to an absolute minimum. Ian Hickman looks at a technique that promises significant benefits in terms of linearising modulation.

Receiving a given radio signal may be commercially important. It may even be a matter of life and death. But the ether is a crowded place, and a weak signal – even though it be in an otherwise unoccupied channel – may be drowned by the spillover of energy from a higher powered transmission in an adjacent channel. This is particularly the case on the crowded hf bands. There have been persistent rumours of an impending tightening of the specifications for the level of transmitter third order intermodulation products. Since I drafted an amendment to these, incorporated in the current issue of CCIR Recommendation 326, time has passed but the rumours persist.

In an hf ssb transmitter, it is likely to be the transmitter power amplifier output stage that is principally responsible for third order – and possibly even higher odd-order – intermodulation products. But problems can also arise in the modulator stage, especially if poorly designed, while for test and measurement purposes, as clean a test signal as possible is desirable.

This reminded me of an article published





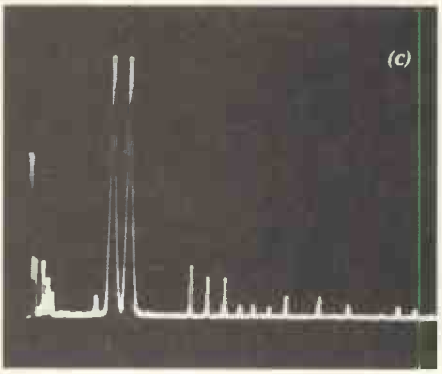
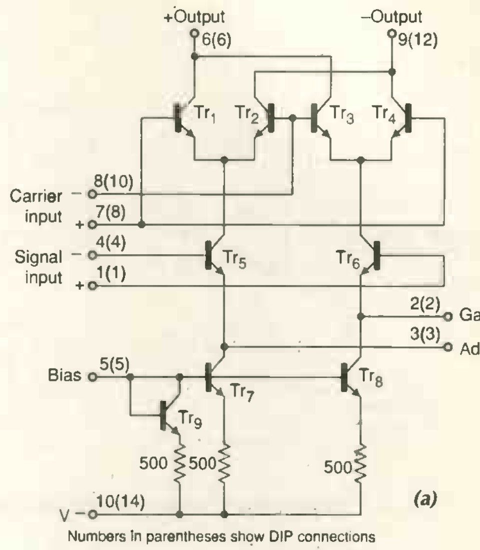


Fig. 1a). Spectra of the two oscillators used to provide the two-tone test signal. Span 0-5kHz, resolution bandwidth 10Hz, post detector smoothing off, reference level (top of screen) +10dBV, noise floor –90dBref.
b) 50Ω resistive combining pad providing 10dB attenuation from each input to the output and 14dB isolation between inputs when terminated in 50Ω. (Nearest E24 values used.)
c) Using the combining pad (unterminated), a third order intermod is visible at 800Hz, as well as sum and difference products. Spectrum analyser settings as a).

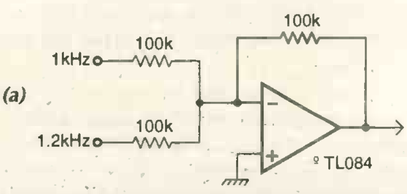


many years ago, concerning the linearisation of an active double balanced modulator, using op-amps. I failed to find it so I am unable to quote the reference, but the scheme is certainly attractive and well worth another look.

Since it was the principle of the scheme that was of interest, I decided to investigate it at very low frequencies. This would enable the investigation to be undertaken without needing careful and eleborate construction to avoid problems with parasitics.

To provide a two-tone test signal to the modulator, two video oscillators were used, one set to 1kHz and the other to 1.2kHz. Each was separately connected into a 5Hz to 50kHz spectrum analyser and its spectrum stored, both traces being shown in **Fig. 1a)**. The two tones just reach up to the reference level (top of screen) which is at +10dBV. At the left of the display, adjacent to the 0Hz marker, low levels of 50, 150 and 250Hz can be seen, being odd multiples of the mains frequency and doubtless due to stray field from a mains transformer.

Also visible are 100Hz sidebands either side of each tone, at about 70dB down. Unfortunately the scale does not show up because the *HP3580A* used does not feature graticule illumination, and I have not yet added this facility to the camera. The second harmonic of each tone at 2kHz and 2.4kHz is also visible at over 60dB down, while higher harmonics are lower still.



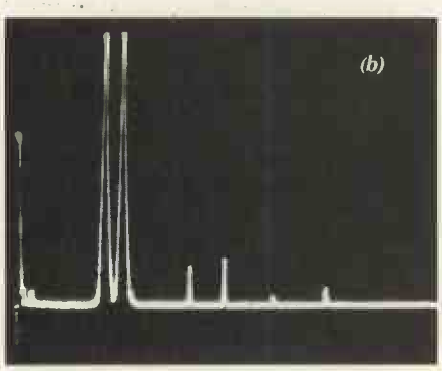
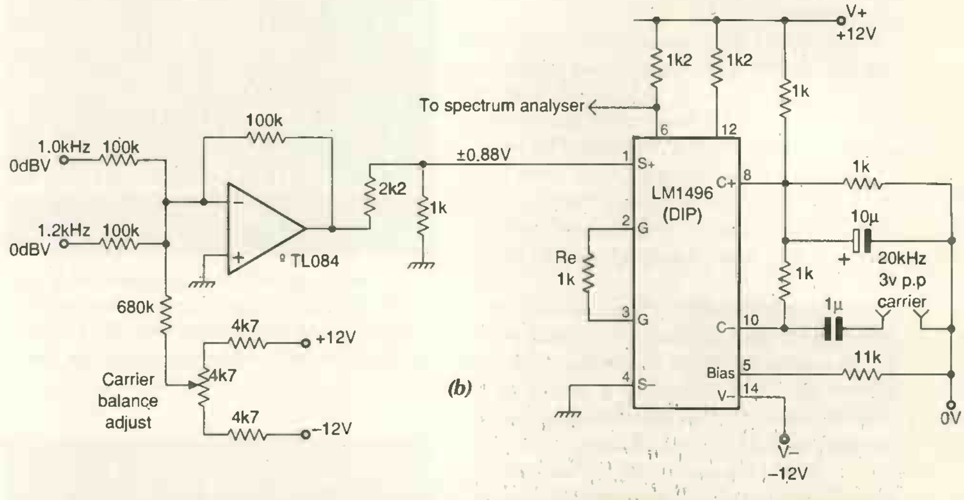


Fig. 2a). Combining the two tones at a virtual earth point provides near perfect isolation between sources, as the spectrum analysis, b), shows. Settings as Fig. 1a). Generator outputs reduced to ca. +7dBm in 50Ω, to give 0dBV unloaded.

When testing a modulator, it is obviously essential that the two-tone test signal is itself free of intermodulation products. This is not as straightforward as it sounds, requiring isolation between the outputs. The 50Ω outputs of the two video oscillators were therefore combined using a special resistive pad designed for this purpose, Fig. **1b)**. It is basically a three-port 6dB resistive combiner with an extra 4dB pad in series with two of the ports. Thus the attenuation from each input to the output is 10dB, while the isolation (attenuation) between inputs is 14dB.



The two tones were combined using this pad and the output connected to the spectrum analyser, Fig. **1c)**. Due to the attenuation of the pad, the two tones are now 10dB down on the reference level. The spectrum analyser's sensitivity is unchanged, and all the other products are similarly 10dB lower. It is of course not permissible to increase the analyser's sensitivity to set the two tones back to the reference level. Their combined value when in phase – their PEP, or peak envelope power – is 6dB greater than either tone alone. This is enough to cause intermodulation products within the analyser itself, due to overload.

Isolation between the oscillators is evidently insufficient, as a number of products are visible. These include the difference frequency, visible as an additional 200Hz line at the left of the trace between the 150Hz and 250Hz lines of Fig. 1a), and the sum frequency at 2200Hz, between the two second harmonics.

More importantly, there is a third order intermodulation product at 200Hz below the 1kHz tone. Third-order intermods usually come in pairs, but there is only the barest hint of a product at 200Hz above the 1.2kHz tone. The reason may be that the output of each oscillator, feeding back into the output circuit of the other, is producing upper and lower

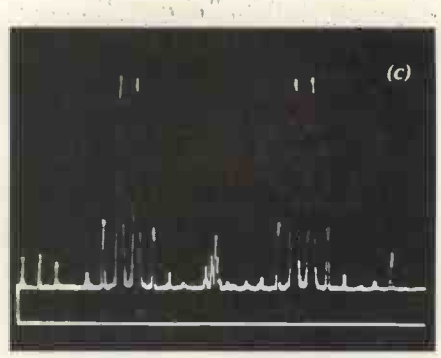


Fig. 3a). National's LM1496 double-balanced modulator internal circuit diagram.
b) LM1496 connected as a double balanced modulator, with a two-tone test signal applied, modulating the 1mA standing current in Tr_5 and Tr_6 by ±90%.
c) Resultant output spectrum, showing the (largely) suppressed carrier at centre screen, the two tones in the upper sideband with third order intermods either side, and a similar picture in the lower sideband. Third-order intermodulation products at 20.8kHz and 21.4kHz are 44dB down on either tone, i.e. 50dB down on PEP (and similarly in the lower sideband). Centre frequency 20kHz, span 5kHz, resolution bandwidth 10Hz, post detector smoothing off.

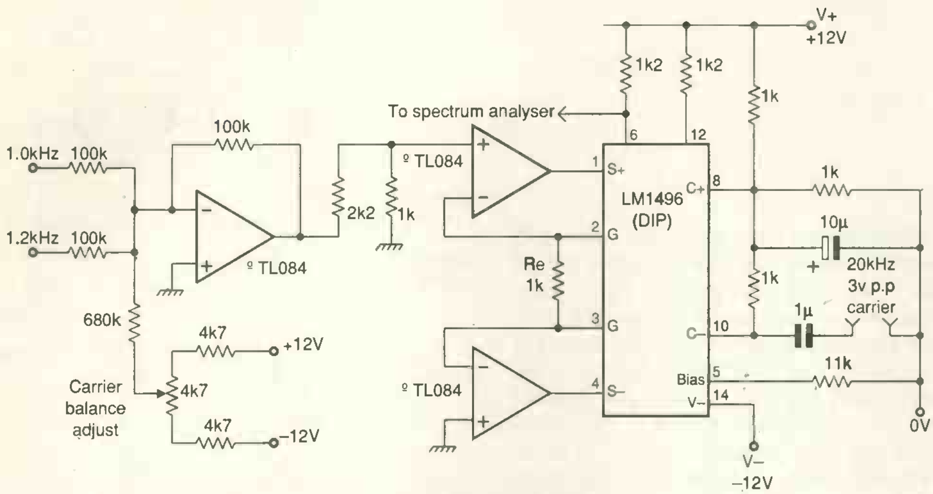


Fig. 4a). Modulator circuit with additional linearising opamps.

third order intermodulations, with the phasing such that they add on the lower side but cancel on the upper.

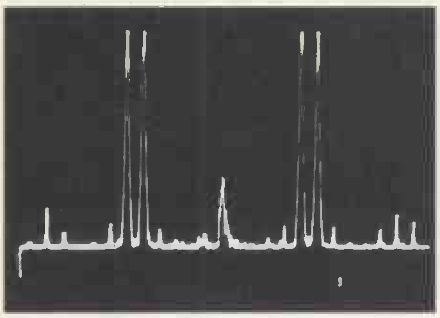
In search of a better arrangement, the special combining pad was removed and the output level of each oscillator reduced by 10dB to compensate. The two tones were then added at a virtual earth point, as in **Fig. 2a)**. This resulted in the two tones appearing at the same level as in Fig. **1c)**. However there were no third order intermodulations visible above the noise floor of 80dB below either tone, 86dB below PEP, Fig. **2b)**.

With a clean two-tone test signal avaiable, it was time to look at the performance of an active double balanced modulator. The one chosen was the popular and widely second-sourced *LM1496*, **Fig. 3a)**. Standing current through each of the signal input transistors $Tr_{5,6}$ is set by the associated current sources $Tr_{7,8}$.

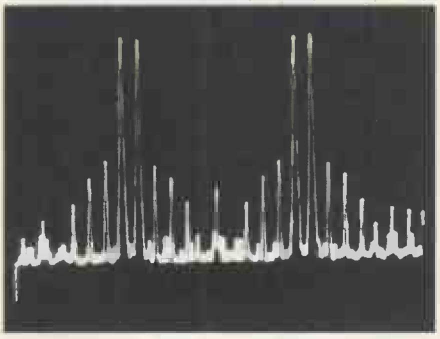
The standing currents are modified by signal current through the gain defining resistor, which is connected between pins 2 and 3. The current through this resistor will of course be zero when when the differential signal voltage between pins 1 and 4 is zero. Standing currents through $Tr_{7,8}$ mirror the current injected into Tr_9 via the bias terminal.

Current through Tr_5 is steered by the switching cell Tr_{1-4} to the positive or negative output at the same time as that through Tr_6 is steered to the negative output or the positive output, by the carrier input. Thus if the currents in Tr_5 and Tr_6 are equal, the current in the positive output is independent of the instantaneous polarity of the carrier, and similarly for the negative output: i.e. both outputs are balanced as far as the carrier is concerned. With signal present, when current through Tr_5 increases and that through Tr_6 decreases, rf current appears at the positive output in phase with the carrier, or in antiphase when the current through Tr_6 exceeds that through Tr_5. The situation at the negative output is the exact reverse. However, the baseband signal itself does not appear at either output. The circuit is thus also balanced as far as the signal is concerned, or 'double balanced'.

I connected the mixer as in Fig. **3b)**. This is



4b) With the same input signal level as in Fig. 3, the third order intermods are now about 65dB down on PEP and the fifth order barely discernable. Spectrum analyser settings as in Fig. 3c).



4c) With both tones increased in level by 3dB, the signal input is overloaded by about 2dB, and a mass of higher order products appear.

generally similar to the published typical application circuit, but using ±12V supplies instead of +12V and –8V. I applied a 20kHz squarewave of ±1.5V peak to the carrier input.

Since switching stages Tr_{1-4} have no emitter degeneration resistors, a small swing of 100mV or so is enough to switch the current from one path to the other. The 10% to 90% rise and fall times of the 3V pk-pk squarewave carrier were just 1.5μs. As a result, the effective switching time was less than 100ns, or very small indeed compared to the period of the carrier.

A high degree of linearity at the signal port is ensured by the comparatively large value of resistance between pins 2 and 3, namely 1kΩ. Very much greater sensitivity to the input at the signal port is possible by reducing the value of this resistor, but only at the expense of linearity, as discussed in the panel.

The signal was applied to pin 1 only, pin 4 being grounded, i.e. as an unbalanced input. But the effect is almost exactly the same as using a balanced drive, in view of the near-perfect current-source 'long tails' supplying Tr_{5-6} emitters. Similarly, an unbalanced drive was used for the carrier input.

As the voltage swing at the signal input modulates the two tail currents nearer and nearer to ±100% of their standing value, s-shaped or third-order distortion will eventually set in, regardless of the value of the gain-defining resistor between pins 2 and 3. Third-harmonic distortion of the signal current fed to the switching section Tr_{1-4} results. This appears not only as third-harmonic distortion of the two tones. It also appears as third-order intermodulation products either side of the two tones, in exactly the same way as in an audio frequency amplifier.

These products are at frequencies $2f_1–f_2$ and $2f_2–f_1$, in the present case 800Hz and 1400Hz. However, rather than appearing at baseband as in an audio amplifier, here the intermodulations are translated along with the two tones to the upper and lower sideband outputs of the mixer.

I applied one of the mixer-circuit outputs to the input of the spectrum analyser, as in Fig. 3 b), the resultant spectrum being as in Fig. 3 c). It shows the largely suppressed carrier at centre screen, the two tones in the upper sideband with third order intermods either side, and a similar picture in the lower sideband.

Each of the two tone inputs to the mixer was –10dBV, and the third order intermod products were 50dB down on PEP (44B down on either tone). Fifth order products at 600Hz and 1600Hz above and below the carrier are also just visible.

With 1mA tail current in each of Tr_5 and Tr_6, the maximum possible linear current modulation is ±1mA, via the gain-defining resistor R_e. This corresponds approximately to 2V pk-pk at the signal input. With two tones at –10dBv, the peak envelope voltage is ±0.88V, or barely 1dB below that theoretical maximum! Clearly, the high value of gain defining resistor is very effective at linearising the modulation.

A reduction in the drive level, so that the signal was not just 1dB below overload level, but 3dB, 6dB or more below, would improve the linearity, driving the intermods even further below PEP But the noise level remains unchanged. As a result, the circuit's dynamic range would be reduced. However, a substantial reduction in intermod levels is possible without reducing the input signal level at all, by using op-amps to linearise the transconductance of the $Tr_{5,6}$ pair.

The arrangement is simplicity itself, **Fig. 4a)**. Connected as unity gain followers, the two opamps drive the bases of Tr_5 and Tr_6 so as to force the voltages at their emitters to

Linearity issues

Long-tailed pair $Tr_{5,6}$ in Fig. 3 operates very linearly, provided the signal input swing is not too large. This is due to the emitter degeneration provided by the gain setting resistor R_e. But the transistors themselves contribute some additional resistance, dependent on the emitter current. When a grounded-emitter transistor is driven from a very high impedance source, i.e. a constant current generator, the collector current is determined principally by the base current and the device's current gain. When driven from a very low impedance source however (a constant voltage generator), a different model is appropriate. Often, a very simple model, such as shown at a) in Fig. 5, suffices to give an understanding of how a circuit works, and of its limitations.

The diagram shows a transistor with infinite mutual conductance, g_m, so that as far as small changes of signal voltage are concerned, its internal emitter voltage follows exactly the base voltage. But between this notional internal emitter and the outside world, there is a resistance r_e The value of this resistor depends on the emitter current and hence also on the signal-voltage.

Resistance r_e is inversely proportional to emitter current. In fact at room temperature the value of the resistance is given by,

$$r_e=25/I_e\Omega$$

where I_e is in milliamps.

Imagine that the transistor is biased so that the standing dc is 1mA. When a ±250μV ac signal is applied to the base, the current swing will be almost exactly ±10μA.

But not quite. For when the emitter current rises to 1.01mA, r_e will fall to 25/1.01Ω, and likewise will rise by 1% when the current falls to 0.99mA. So the increase in current at the positive peak will be slightly greater than the decrease at the negative peak.

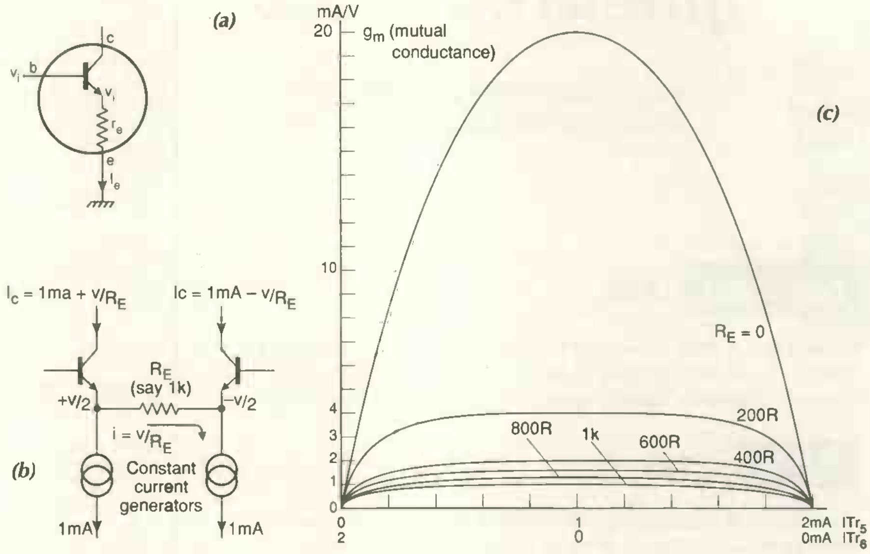


Fig. 5a) Simple model of a transistor driven from a constant voltage source.
b) In a long-tailed pair with ideal 'tails', the increase in current through one transistor must exactly match the decrease through the other.
c) Additional resistance R_E between the emitters linearises the stage, permitting a much larger percentage current swing for a given acceptable degree of distortion, at the expense of needing a much larger voltage swing at the input (reduced stage gain).

The disparity becomes greater as the fractional modulation of the emitter current is increased. This leads to significant second harmonic distortion unless some measure, such as negative feedback is used to control it.

In a balanced circuit, such as b) in the Figure, the internal emitter resistance r_e of each transistor must be added to any external resistance R_E connected between the transistors. With constant tail currents as shown, as the current through one transistor increases, that through the other must fall by the same amount.

If the current through Tr_5 decreases by 10% its r_e will rise to 25/0.9, which is 27.78Ω while the r_e of Tr_6 will fall to 22.72Ω. Thus the effective emitter to emitter resistance is (R_E+50.5)Ω.

This differs from (R_E+50)Ω, the value when both emitter currents are 1mA, by only 10% even if R_E is 0, and a mere 0.05% if R_E is 1kΩ. If the current variation is not ±1% but, say, ±90%, then even when R_E is 1kΩ, significant peak crushing (third-harmonic distortion) will result, due to the variation of the effective emitter-emitter resistance. For when the current through one transistor doubles to 2mA, its r_e drops only to 12.5Ω, whereas for the other, when I_e falls to 0mA, r_e rises to infinity. The effect of different values of emitter-emitter resistance R_E in linearising the mutual conductance g[m] of a long-tailed pair is illustrated in c) in the Figure.

equal the signal input at the op-amp non-inverting inputs.

Falling differential transconductance of the $Tr_{5,6}$ pair as one or other nears cutoff is within the loop feedback, and thus largely overcome. This is shown in Fig. **4b)**, where the analyser settings are as those in Fig. 3c). Now, the third order intermods are 65dB down on PEP, even with the input within 1dB of overload.

With both tones increased by 3dB, the signal input circuit is overdriven and a mass of odd-order intermod products of higher orders appear, Figure **4c)**. Thus the linearisation allows the circuit to operate in an extremely linear manner, right up to just below the theoretical overload point. And although, for convenience, the results presented here were obtained when operating the *LM1496* at very low frequencies, the scheme doubtless operates at much higher frequencies.

Data book typical performance curves for the *LM1496* show its performance to 50MHz and beyond. Op-amps are now available with gain-bandwidth products of many hundreds of megahertz. As a result, it should be easy to implement the linearisation scheme at, say, 10.7MHz, or even higher frequencies. This would provide a super-linear modulator for test and measurement purposes, or for use in transmitters of exceptional linearity, using perhaps class A output stages. ■

NEW PRODUCTS CLASSIFIED

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ACTIVE

A-to-d and d-to-a converters

Serial-output a-to-d. Harris has the *HI5816* 12-bit, sampling a-to-d converter with serial output, which takes only 3.5mA from 5V and allows direct digital input to microcontroller serial ports. Conversion time is 20μs and sampling rate 50ksample/s. Data is output either as the conversion proceeds or when it is completed, the mode being pin-selected. The in-built t/h amplifier has a 1MHz bandwidth. Harris Semiconductor UK. Tel., 01276 686886; fax, 01276 682323.

Dual delta-sigma a-to-d. Crystal's *CS5504* is a dual-channel delta-sigma converter allowing perfect differential non-linearity with no missing codes to 20 bits, with fast, on-chip calibration circuitry. It samples at up to 200sample/s and both 50Hz and 60Hz noise is rejected by built-in filtering. There is no need for the usual external integrating capacitor and control logic and the device uses a cheap crystal as used in watches as the clock. The family includes single, dual and four-channel versions, all with direct interfacing to low-power microcontrollers, since these devices operate with supplies down to 3.3V. Crystal Semiconductor Corporation. Tel., (USA) 00 512 442 7555; fax, 00 512 445 7581.

'Fastest' a-to-d. Made by Signal Processing Technologies, the *SPT7760* is a full parallel flash converter with a guaranteed sample rate of 1000Msample/s and an analogue bandwidth of 900MHz. Input capacitance is 15pF, stabilised by the inclusion of 256 buffers, and output is in Gray code. Single-ended 5.2V is needed. Ambar Cascom Ltd. Tel., 01296 434141; fax, 01296 29670.

Little a-to-d. Said by Analog Devices to be the smallest 12-bit a-to-d converter to give 100ksample/s from one 2.7-5.5V supply, the *AD7896* is in an 8-pin SOIC or mini-dip. Input range matches the supply voltage and consumption from 3V is 9mW or 15μW in power-down, which is automatically timed to occur after a conversion and 6ns before the next one. Track-and-hold and a serial interface are on-chip. Analog Devices Ltd. Tel, 01932 266000; fax, 01932 247401.

Microprocessors and controllers

Fastest Pentium. Intel has introduced a new version of the *Pentium* processor, which is in 3.3V, 0.35μm cmos/bipolar technology, operates at 120MHz, gives 140 SPECint92 and 103 SPECfp92 and is now available. Die size is about half that of earlier 0.6μm, 75, 90 and 100MHz Pentiums. Intel Corporation UK Ltd. Tel., 01793 696000; fax, 01793 430763.

Discrete active devices

Uhf silicon fet. *MHW916* from Motorola is a laterally diffused mosfet designed for European extended GSM base-station use, working in the 925-960MHz range. It operates from 26V and takes 15.5dBm of rf input, giving a gain of 26.5dB minimum, harmonics being 35dBc down. Input and output are both 50Ω. Motorola Inc. Tel., 01908 614614; fax, 01908 618650.

240V mosfet. Zetex's *ZVP4424G* SOT223 mosfet has a maximum on resistance of 12Ω at 100mA and 2V maximum V_{GS}. Rise and fall times are 8ns and 20ns at a 100mA drain current and the device controls a continuous 480mA drain current pulsed to 1A. Input capacitance is 100pF. Zetex plc. Tel., 0161-627 5105; fax, 0161-627 5467.

Low-voltage mosfets. Four power mosfets from Siliconix, in the company's *TSSOP Lite Foot* family turn on fully on 4.5V and operate down to 2.5V. The *Si6xxxDQ* series includes a single n-channel device, double n-channel and p-channel types and a complementary version, breakdown for n-channel devices being 20V and 12V for the p-channel types, with a 35mΩ on resistance in the single n-channel unit (100mΩ for the dual p-channel type). Siliconix/Temic Marketing. Tel., 01344 485757; fax, 01344 427371.

Digital signal processors

DSP56002 evaluator. Motorola offers an evaluation module for the *DSP56002* 24-bit audio dsp chip. The *EVM*, combined with 32Kword of on-board sram and a stereo codec, carries out a range of audio processing algorithms. It comes with the *DSP5600X* cross-assembler and debug software running under dos. Macro Group. Tel., 01628 604383; fax, 01628 666873/668071.

Linear integrated circuits

Rail-to-rail op-amp. Linear's *LT1366* dual precision op-amp offers rail-to-rail input and output, input voltage offset of 150μV and input bias current of 10nA over the whole input range. Common-mode rejection is 90dB and loop gain 10^6 into 2kΩ. Linear Technology (UK) Ltd. Tel., 01276 677676; fax, 01276 64851.

Optical devices

Coaxial 1550nm laser. NEC says its NDL7701P is the first 1550nm distributed-feedback laser to go into a coaxial package. It and the 1350nm equivalent, the 7601P, use NEC's multiple-quantum well laser diode, the dfb technique exhibiting very narrow spectra for long transmission distance. Output is 5mW and the devices are suitable for external modulation at up to 10Gbit/s. NEC Electronics (UK) Ltd. Tel., 01908 691133; fax, 01908 670290.

Displays

Colour tft. Colour displays from Hitachi are now obtainable from Eiger, including the model tersely known as the *TX26D60VC1CAB*, which is a 640 by 480 type weighing only 600g and having a thickness of 10mm. Backlighting is built in. Other colour and mono types offered include the *LM9520RPCC*, an 8mm thick unit with 320 by 240 resolution, and the *LMG4320* mono type, measuring 5.8mm thick and weighing 200g. Eiger Technologies Ltd. Tel., 01928 579009; fax, 01928 579123.

SM GaAs mmics. Anglia is handling the Samsung *SMP* range of plastic-packaged, low-cost, gallium arsenide, monolithic microwave ics, including a 0-8GHz voltage-variable attenuator (30dB/1GHz), the *SMP 10008-1*; the *SMP 10008-2* two-stage type giving 35dB at 1GHz; a 1.8-3GHz low-noise amplifier, the *SMP 22203* with a typical noise figure of 2.2dB; the *SMP 11206* 1.8-6GHz medium-power/driver amplifier; and the SMP-13203 low-noise amplifier offering 2.5dB noise figure and 15.5dB gain at 2.4GHz. Anglia Microwaves Ltd. Tel., 01277 630000; fax, 01277 631111.

Mixed-signal ICs

Conferencing. Mitel's *MT8924* provides conference call capability in digital switching systems, allowing up to ten independent conferences of three parties or one of thirty parties to be set up using a 32 pcm voice channel supporting 2.048, 1.536 and 1.544Mb/s data rates. It converts pcm a-law or μ-law data to linear form, processes it and reconverts the result to companded form, sending it to the

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pcm output port. There is programmable noise suppression and individual channel gain. Mitel Semiconductor. Tel., 01291 430000; fax, 01291 436389.

Fast, low-noise plls. *MB1516A* and *MB1517A* from Fujitsu operate at 1.1GHz and 2GHz for GSM and DECT mobile work. Both have a pulse-swallow function to form a fast dual-modulus prescaler with selectable 64/65 and 128/129 ratios. In DECT tests, spurious noise levels are 72dB and phase noise 80dBc/Hz. Power needed is 6.5mA and 14mA respectively from single 3V supplies. Fujitsu Microelectronics Ltd. Tel., 01628 76100; fax, 01628 781484.

Pll for 'phones. Murata's *HFQ351/361* series of miniature pll modules for E-AMPS and E-TACS radiophones are surface-mounted devices containing a low-pass filter, microstrip line resonator vco and a pll. They work on 3V and take a maximum of 18mA, providing an s:n ratio of over 45dB and carrier:noise of 72dB. Murata Electronics (UK) Ltd. Tel., 01252 811666; fax, 01252 811777.

Cameras

Video imaging terminal. Harris's high-definition *Compact Video Imaging Terminal* weighs 12lb, is battery-powered and captures colour and monochrome images from analogue cameras, still and live video cameras and digital cameras, including the Associated Press *NC2000* and Kodak's *DCS 420* series, as well as images from infrared and radar sensors. Results are stored, manipulated, annotated, compressed and transmitted on hf, vhf or uhf channels, satellite links or landlines. There is a built-in 4in screen and an internal memory is enough to store 20 images, with room for a removable memory card. Harris Corporation. Tel., 00 1 716 244-5830.

PASSIVE

Passive components

Thin-film capacitor. In values of 0.1pF to 24pF at between 50V and 100V, AVX's *ACCU-P* range of thin-film rf/microwave capacitors are now available in 0603 size packages. Cover and substrate are alumina rather than glass for improved thermal matching, smaller size or better current handling. AVX Ltd. Tel., 01252 770000; fax, 01252 770001.

SM carbon trimmer. Murata's *POZ3* series of surface-mounted trimmer potentiometers are constructed in two parts to give lower cost and better reliability. Special plating provides good solderability and the substrate used prevents flux wicking. Resistance range is 200Ω-2MΩ at 0.1W. Murata Electronics (UK) Ltd. Tel., 01252 811666; fax, 01252 811777.

Connectors and cabling

Smart-card connector. Made by Jin Kwang, the *JCR* series of smart-card reader connectors have dual tension points to ensure stable card insertion and are designed to avoid damage to the pcb when the housing cover is opened. They are available with eight or sixteen gold-plated contacts and can be supplied with blade or sealed detection options. Pedoka Ltd. Tel., 01462 422433; fax, 01462 422233.

Low-power smps. *LCS25* from Gardners is a 25W switched-mode power supply possessing a range of industry approvals and interchangeable with many existing units; it has standard pinout and fixing centres on single, double and treble output units, the range covering several combinations of 5V, 12V and 15V in seven open-frame or cased models accepting 85-265V ac or 12V, 24V or 48V dc at the input. Gardners Ltd. Tel., 01202 482284; fax, 01202 470805.

Insulated BNCs. Multi-Contact has the *HCK* range of insulated BNC connector accessories, including test leads, connectors and adaptors for a range of hf needs in both male and female form in red, black or blue. The connectors are designed to handle 1kV to earth, with a maximum of 500V between inner and outer. Attachment to the lead is by solder or crimping. Multi-Contact UK Ltd. Tel., 01908 265544; fax, 01908 262080.

PC card connectors. Light-weight connectors from Fujitsu, the *FCN-560H* series, conform to both JEIDA and types I, II and III PCMCIA standards and are meant for completely automatic assembly. The ejector mechanism is assembled separately to allow the connector to be mounted using a pick and place machine. Special pins and solderable flanges prevent subsequent mounting stress and movement during soldering. Fujitsu Microelectronics Ltd. Tel., 01628 76100; fax, 01628 781484.

Crystals

Sm crystals. *CMX 5000* crystals by C-MAC cover the 10-250MHz frequency range, with fundamentals up to 100MHz using a plasma etching technique and overtones above that. From –10°C to 60°C, stability is ±5ppm; ±50ppm in the –55°C to 105°C range. Surface-mounted packages are in ceramic and have an overall height of 2.7mm. C-MAC Quartz Crystals Ltd. Tel., 01279 626626; fax, 01279 454825.

Eight-led packages. New in Dialight's *Series 567* circuit board indicator range is a two-level type containing two rows of four rectangular-window leds in yellow, green and other combinations in UL94V-0 black housings. Dialight. Tel., 01638 662317; fax, 01638 560455.

Printers and controllers

Thermal printers. Static head thermal printer mechanisms and interface boards by Panasonic are quiet and fast and are meant for use in instrumentation and data terminals. Six models in the *EPL1100* range use paper 60, 80 and 112mm wide at print speeds of eight and 16 lines/second, the number of dots being in the 448-832 per line, depending on width, or up to 80 characters per line. They all handle graphics and can be fitted with an end-of-paper sensor. Able Systems Ltd. Tel., 01606 48621; fax, 01606 44903.

Colour vga lcd. *LDH102T-10* is an active-matrix lcd module by FPD, which is a joint Philips, Thomson, Sagem and Merck concern, that provides vga resolution on a 10.4in diagonal screen. With its 24-bit driver, there are 16.7 million colours and performance is applicable to multi-media computing on notebook types. Although pixel drive is by way of diodes, rather than by transistors, drive electronics for tft displays are compatible and the smaller diodes allow more light to pass to give brighter presentation. Philips Components. Tel., 00 31 40 722790; fax, 00 31 40 724547.

Filters

Card-based filter system. Multi-channel electronic filters systems by Kemo take the form of cards, assembled in cases to users' requirements and allowing a wide range of frequency, gain and characteristic to be configured. The *21ST* range, which is manually switched, offers filters from the simple fourth-order, 15:1 cut-off adjustment type to the 2555:1 cut-off model with a choice of four, six or eight poles. In the computer-controlled *21CC* range of units, choices are one or two channels per card, differential input, jumper-selected gain and gain/offset trim. Versions with programmable gain and adjustable frequency are available. Kemo Ltd. Tel., 0181 658 3838; fax, 0181 658 4084.

Instrumentation

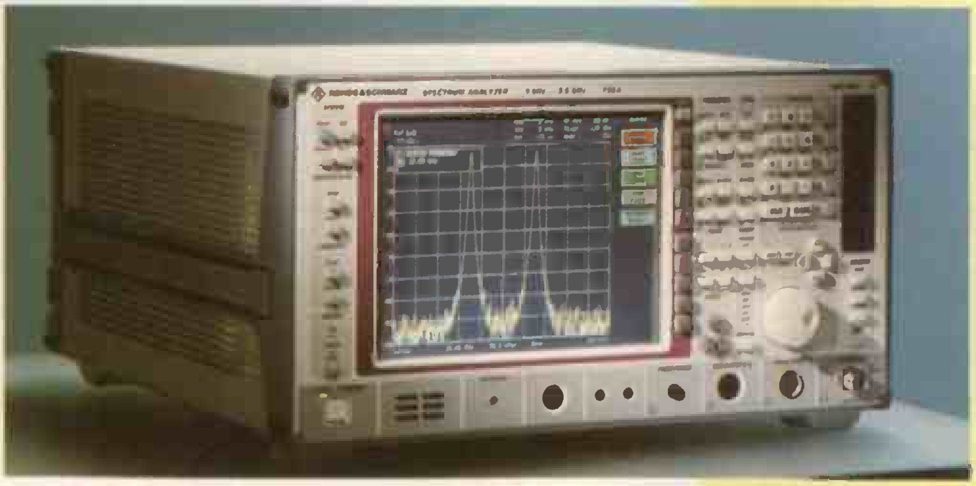
Bright panel meters. *DMS-30PC-RL* panel meters made by Datel use the newest, brightest, 0.56in red leds and take a mere 10mA from 5V. They are said to be readable from 20ft. The internal a-to-d converter is an autozero type, accurate to within ±1 count. Three standard ranges are ±200mV, ±2V and ±20V, all having 1GΩ input impedance, protected to ±250V, with autopolarity and over-range indication. Datel (UK) Ltd. Tel., 01256 880444; fax, 01256 880706.

Satellite terminal tester. Racal's *6121* is said to be the world's first commercial test set for satellite mobile terminals and is meant for maintenance, servicing and production test of mobiles for geostationary satellites Optus, AMSC, TMI, Inmarsat-M and miniM, and the future low-earth orbit types such as Iridium and Globalstar. Tests carried out include call setup, call termination, voice loopback, data, facsimile, log-on, acquisition and transmission disable, with a number of transmitter tests. Racal Instruments Ltd. Tel., 01734 669969; fax, 01734 262121.

40GHz signal generator. Extending the coverage of the R&S *SME* and *SMT* range of signal generators is the *SMP 04* 40GHz instrument, which is available with am, fm, phase, ask and fsk modulation, with an optional internal pulse generator. Frequency coverage is 2GHz-40GHz, with the low end starting at 10MHz as an option, to 0.1Hz resolution. There is also frequency and level sweep and a list mode for fast frequency hopping. Rohde & Schwarz UK Ltd. Tel., 01252 811377; fax, 01252 811447.

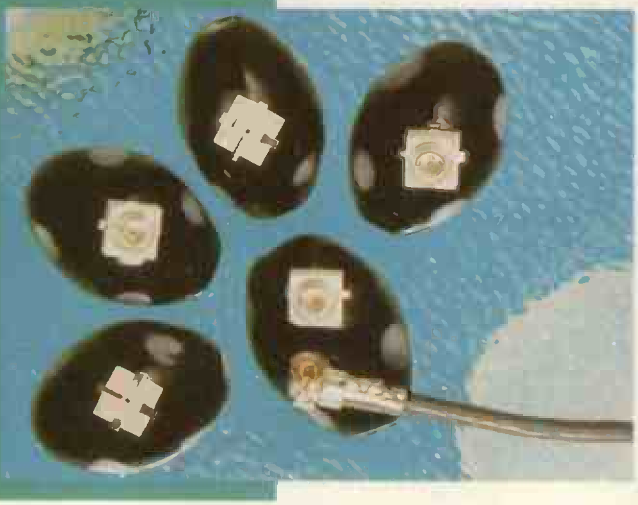
Fibre tester. Using time-domain reflectometry, a new version of Tektronix's *Fibremaster*, the *TFP2A/FM* resolves faults in optical fibres at 850nm and 1310nm down to less than 20cm, with a very short dead zone. The instrument supports two optical modules with four wavelengths, allowing exact configuration without damage to the modules. Both multi-mode lans and single-mode wans can be tested, results being produced in hard copy and on floppy disk. Tektronix UK Ltd. Tel., 01628 486000; fax, 01628 474799.

Digital clampmeter. *DL 235* is a clamp meter combining conventional operation with dmm versatility. It gives 4-digit readout of true rms current to 1000Apk, with an analogue display for transient capture and frequency measurement. Accuracy is 2% at 400A from 0.5Hz to 10kHz. Its features include detection and measurement of harmonics in neutral currents, alternating and direct voltage and resistance and continuity, a display hold facility assisting in difficult conditions. Di-loG Instruments. Tel., 01942 222657; fax, 01942 227735.



Sound-level meter. B&K's *Type 2236* sound-level meter is intended for use in measurements concerned with the Noise at Work legislation, containing no more than is necessary for this work. It measures noise levels and can be upgraded by built-in octave filters for frequency analysis to allow remedial measures to be determined. The instrument has standard international parameters for industrial noise measurement, and is provided with a serial interface to down-load results to a pc. Bruel & Kjaer (UK) Ltd. Tel., 0181 954 2366; fax, 0181 954 9504.

Sm rf connectors. An rf connector for 50Ω application, the *Hirose JAE CV10* has a 3GHz bandwidth with vswr of 1:3 and measures 3mm off the board with the right-angle plug inserted. Other versions are available: the *S.F2-R-SMT* is a 50Ω type on tape for automated production, offering a vswr of 1.2 at 2GHz with a profile of 4.7mm after mating. Flint Distribution. Tel., 01530 510333; fax, 01530 510275.



Literature

Enclosures. Vero's full range of plastic and metal enclosures and accessories is described in a new colour catalogue, with guides based on printed-board sizes and templates to help cost and specification of modifications that may be needed. Vero Electronics Ltd. Tel., 01703 266300; fax, 01703 265126

Esd. Baystat make bags to protect components against the effects of electrostatic discharge and now offer a free booklet on esd, its associated problems and how to prevent it. Teknis Ltd. Tel., 01823 481248; fax, 01823 481120.

Production equipment

Pcb miller. If you have a pc, you can mill printed-circuit boards using the German LPKF system, the *Protomat*. For around half the cost of some other systems, the package includes board design software and connects directly to the pc. Bed size is 420 by 375mm and repetition accuracy ±0.02mm. All standard materials can be handled, both single and double sided. Tracks CAD Systems Ltd. Tel., 01344 55046; fax, 01344 860547.

Spectrum analysers. Intended, in the main, for the communications industry, the *FSE* range of spectrum analysers by R&S covers the 20Hz-7GHz range and could therefore be said to be universal in application. Speed is one of its claims to fame: it carries out 25 sweeps/s and synchronised tuning at sweep times of 5ms provide accuracy at every display point. Gap sweep and a resolution of 200ns/division for time domain analysis allow simultaneous measurement of pulse rise and fall times at high resolution. A phase noise of around –128dBc/Hz at 10kHz eliminates the need for extra phase noise testing. Test functions include eight different markers, adjacent-channel power and occupied bandwidth measurement and a selectable-resolution counter. Hard and soft keys make for ease of operation, as does the large colour monitor, and output is provided for a range of printers and plotters and all Windows file formats. Rohde & Schwarz UK Ltd. Tel., 01252 811377; fax, 01252 811447.

Power supplies

Fast-response regulator. Linear's *LT1585* 4.6A, 3-5V linear regulator is claimed to have the best combination of low drop-out and fast transient response. Input is a maximum of 7V and fixed and adjustable versions are made. Thermal limiting is provided. Micro Call Ltd. Tel., 01844 261939; fax, 01844 261678.

Intelligent smps. Vero has a 300W single-voltage version of the *ISI-Power* switched-mode power supply, which is said to be the first 19-in rack pluggable psu to have an intelligent controller to allow programming, control and interrogation from a standard pc by way of an RS-232 link. Its 800kHz converter is over 80% efficient and the unit is in a 6U by 8HP module. Outputs currently

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available are 3.3V, 5V, 12V and 24V, with autoranging input from 115V ac to 230V ac. Vero Electronics Ltd. Tel., 01489 780078; fax, 01489 780798

Three-output dc-to-dc converters. Interpoint's *MHF* family of mil. spec. dc converters now includes the *MHF+28515T*, which provides both ±5V and ±15V (±12V from the *28512T*) outputs at a total power of 15W. The units are in the same package as the single and dual models, which measures 1.45 by 1.12 by 0.325in. Normal operation is obtained for inputs of 16-48V, coping with 80V surges without damage. Output noise is 30mV pk. Interpoint UK Ltd. Tel., 01252 815511; fax, 01252 815577.

Low-voltage converter. Operating from power supplied by alkaline, lithium, nickel-metal-hydride or nickel-cadmium battery packs, Micro Linear's *ML4863* converter chip still works when battery voltage is down to 3.15V for a 5V±3% output, so extending by up to 10% the time available to the user of a notebook. In addition to the 5V output, the device produces 3.3V and 12V for lcds. A 200kHz switching frequency reduces the size of the output transformer. Ambar Components Ltd. Tel., 01844 261144; fax, 01844 261789.

Power for 3V micros. Micrel's *MIC29150/MIC29300* series of 3V and 3.6V supplies provide up to 1.5A/3A, with a full-load drop-out of under 300mV. They are protected against overcurrent, reversed polarity and leads, over temperature and transients and have logic-level on/off control or an error flag to signify drop-out. Hawke Components Ltd. Tel., 01256 880800; fax, 01256 880325.

Radio communications products

Receiver protection. Broadband limiters by Anglia in the *ACLM-4553* series consist of pin diode limiters and passive hybrid circuits in a 50Ω line structure, and are meant for use in radar, communications and ecm. They come in either stripline or coaxial mountings in eight models, the whole series covering 500MHz-18GHz, at a peak input-power capability of 100W (1-2W continuous). An internal dc return is provided to minimise vswr. Anglia Microwaves Ltd. Tel., 01277 630000; fax, 01277 631111.

Protection devices

S-m fuses. *SupraFuse* by Schurter is a range of miniature surface-mounted fuses that are laser-trimmed from metal-clad foil to allow special ratings in addition to a standard range, coverage being 63mA-6.3A. Main areas of usage are transient suppression, interface protection and conventional overcurrent protection. Packages measure 2.6 by 4.5 by 1.9mm. Radiatron Components Ltd. Tel., 01784 439393; fax, 01784 477333.

Transducers and sensors

Absolute shaft encoder. *Model AD* encoder by Control Transducers is a non-contacting device able to network up to 15 encoders on one six-wire telephone cable in a 330m cable run, interfaced to an RS-232 port, the interface being included. Models available have 2-65536 codes/rev. at up to 115.2kbaud with 9 or 12 bit accuracy. Maximum shaft speed is 10,000rev/min. Being an absolute encoder, rather than the incremental type, means that it always shows the correct position and needs no home pulse. Control Transducers. Tel., 01234 217704; fax, 01234 217083.

Pressure transmitter. From HBM, the *P19* pressure transmitter is robust both mechanically and electrically, having a welded steel diaphragm contained in a stainless steel case and an emc specification of 10V/m – to IEC803-2. Full-scale ranges of 10-500bar are available and there are twenty different connection threads to ease the problems of installation into existing equipment. HBM United Kingdom Ltd. Tel., 0181-420 7170; fax, 0181-420 7336.

Silicon accelerometer. Known, for some inscrutable reason, as 'Yoda', IC Sensors's *Model 3255* is a dual-chip device incorporating a silicon accelerometer die in the same case as the signal-conditioning asic. The device was originally meant for use in ±50g automotive airbag activation and is now available for general use. Sensitivity is ±40mV/g about 2.5V dc and response extends to zero frequency. Shocks and vibration up to 2000g do not degrade performance. Eurosensor. Tel., 0171 405 6060; fax, 0171 405 2040.

Vision systems

Scan converter. Astrodesign's *SC-2020* scan converter converts computer graphics to television format for use with video recorders, projectors and monitors in real time. It automatically synchronises to horizontal scan rates from 15kHz to 80kHz and includes the hdtv frequency. Features include pan and zoom facilities, NTSC and PAL output, RS-232 control for remote operation and programming and Y, R-Y, B-Y, Y/C and Betacam output. Ginsbury (UK) Ltd. Tel., 01634 290903; fax, 01634 290904.

COMPUTER

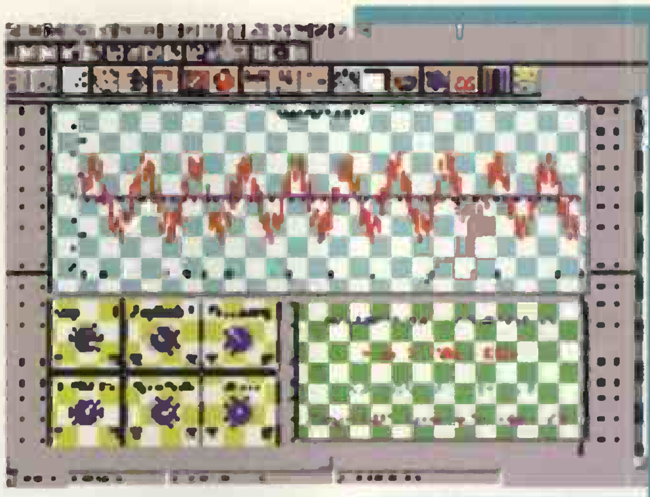
Computer board-level products

Single-board computer. A 386/486 board from Blue Chip, the *Apex II*, conforms to the new A5 board size standard. It is suited to a variety of embedded and industrial applications, providing processing, video and peripheral control on a single 5V board. processors from a 386DX40 to a 486DX4 can be specified and standard 72-pin simms give a maximum of 32Mbyte, with solid-state disk memory by way of 1Mbyte of flash memory, with sockets allowing more flash and sram to be added. The board supports 640 by 480 pixel lcds and 1024 by 768 on crts. There is one ISA slot for pc AT cards and two serial ports, a controller providing 24 lines of programmable digital i/o. A watchdog timer and real-time clock are backed by a 3.7V lithium battery, with external battery input provided. Blue Chip Technology. Tel., 01244 520222; fax, 01244 531043.

STEbus I/o. Arcom has an STEbus board with memory-backed a-to-d and d-to-a i/o, controlled by a 16-bit processor. It is supported by 32Kbyte of ram dual-ported to the bus and is capable of continuous data handling at sample rates to 9kHz. There are eight multiplexed, differential a-to-d channels and two 12-bit d-to-a outputs, 12 16-bit timers, three interrupt sources and two byte-wide latches to give ttl output. The Analog Devices *SP2105* dsp is programmed to control a-to-d trigger, memory storage and memory arbitration. Arcom Control Systems Ltd. Tel., 01223 411200; fax, 01223 410457.

Multi-function card. In the form of a short card with a D-type connector, Blue Chip's *ADC-44d* provides a pc with a combination of input, output and conversion functions. Sixteen analogue inputs with selectable ranges from ±50mV to ±10V can be used singly or doubled up to give a-to-d conversion to 12 bits at 3μs. Programmable gain is 1-100. Four analogue voltage or current-loop outputs are available and there are 24 programmable digital input/output lines at ttl level. Analogue conversions are programmable under i/o control, interrupt control or by dma. Blue Chip Technology. Tel., 01244 520222; fax, 01244 531043.

PC/104 modules. Cards to the PC/104 standard by Advantech are PC-compatible and connect straight to an AT-bus. Those available include cpu core modules, PCMCIA controllers, super i/o modules, Ethernet controllers, solid-state disk modules, flat-panel/vga types and data converters. Fairchild Ltd. Tel., 01703 559090; fax, 01703 5559100.



Signal processing. *Signal Centre v.2*, which runs under Windows, is a data acquisition and analysis program providing DDE link to other software, sound for verbal commands and warnings and process control. Signals are monitored, created, recorded, displayed and processed without programming and data is saved in ASCII with automatic time and date to provide a record. Presentation is in the form of virtual instruments with all the relevant controls and indicators, including oscilloscope displays, all under the user's control; several displays can be used with mouse switching between them. There is a state machine interface for control applications with digital and analog output for motor or servo control. Discrete Fourier transforms and FFTs are incorporated and inputs for a range of thermocouples, while processing includes statistics, integration, differentiation, linearisation and signal generation. The package has been designed in co-operation with Amplicon Liveline with Amplicon's boards in mind. Amplicon Liveline Ltd. Tel., 0800 525 335 (free); fax, 01273 570215.

Computer systems

Industrial PC. *Panecon-PC* by Contec is a PC/AT in which is combined a 10-in touch-panel display, programmable membrane switches and i/o expansion slots in one panel-mounted unit. Tft, lcd, el and stn colour displays are available and the silicon disk emulates a floppy drive to run dos, Windows and other operating systems. There are eight full-size expansion slots, six of them free. The processor is a 33/66MHz 486DX2, with 64Mbyte of dram. 256Kbyte cache, a 1.44Mbyte disk and two hard disk bays. Gothic Crellon Ltd. Tel., 01734 776161; fax, 01734 776095.

Data communications

Ir ic for IrDA. Conforming to the new Infra-red Data Association standard for cordless, 2400b/s-115.2kb/s communication between laptops, notebooks, desk-tops and all the other tops, Crystal Semiconductor's *CS8130* multi-standard IR chip handles communications between equipment from different manufacturers. It connects to a standard uart, output being to standard led and pin diodes. An evaluation kit is on offer. Sequoia Technology Ltd. Tel., 01734 258000; fax, 01734 258020.

Mass storage systems

PCMCIA disk drive. A 260Mbyte hard disk drive on a type III PCMCIA card allows data transfer between mobile and desk-top computers and to remove sensitive data for security, which is further enhanced by means of a two-level password. To increase battery life, the card automatically goes into idle mode if no access request is present. It is compatible with either PCMCIA-ATA or with 68-pin ATA (IDE) interfaces, configuring itself to the relevant type. Premier Electronics Ltd. Tel., 01922 700261; fax, 01922 787422.

Software

Emc guidance. Although it is less than a year to the effective start of the European Directive on Electromagnetic Compatibility, it appears that some manufacturers are unclear about its exact requirements. With this in mind, Seaward has produced *Expert Consultant*, a Windows-based package that gives the required standards for any product and offers a guide on how to achieve them, showing how to effect countermeasures in a design. Emc tests defined by the program can then be carried out by the manufacturer if required as a preliminary to full compliance certification. All necessary paperwork is produced by the software, which runs on a 386SX or higher with Dos 5 and Windows 3.1, with an 800 by 60-pixel graphics card and 10Mbyte or more of hard disk space. An update service keeps the program current. Seaward Electronic Ltd. Tel., 0191 586 3511; fax, 0191 586 0227.

Fpga design. Actel's *Designer Series 3.0* is a set of tools to simplify the design of field-programmable gate arrays, while maintaining performance. It uses a graphical user interface and is, says Actel, very easy to learn. The tools produce fully deterministic fpga designs to meet timing requirements in one pass, in contrast to other software that requires multiple iterations; the *DirectTime* option allows specification of the design frequency and timing of important signals, the program then ensuring that the specification is met. A spreadsheet-type timing analyser shows performance results, which can be compared with those specified, taking into account temperature and voltage. *PinEdit* shows an fpga package graphically and allows signals to be placed on selected pins. All versions of Windows after 3.1 are supported. Actel Europe Ltd. Tel., 01256 29209; fax, 01256 55420.

Pcb design. Now in the pcb design market, MicroSim announce two packages: *PCBoards for Windows* and *PCBoards with Autorouter for Windows*, both currently being offered at low prices as an introduction. There is no limit to the number of devices the packages or number of pins or layers that the packages can cope with, and even basic features of board design, such as board size, shape or number of layers, can be changed at any time. In many other respects, the software is equivalent to many other professional programs. MicroSim Corporation. Tel., 00 1 714 770-3022; fax, 00 1 714 455-0554.

Data acquisition. Version 4.6.1 of National's *NI-DAQ* driver software for the company's pc-based data acquisition equipment is available. Running under dos or Windows, the software allows users of E series boards to perform equivalent time sampling on boards with analogue trigger, change sampling rates without reprogramming delays and execute new counter-timer operations. It also works with any card and socket services software at v2.0 or higher. Upgrade from older versions is offered free and the package is included with the company's boards. National Instruments UK. Tel., 01635 523545; fax, 01635 523154.

System modelling. SB Technology's *ModelMaker* for Windows is a mathematical modelling program simulating experiments and both event-driven and continuous processes in life sciences, engineering and commerce. Although it is said to be easy to use, it offers powerful tools for analysis, including optimisation, confidence intervals, minimisation, sensitivity and stochastic analysis. The package contains tutorials and examples. Models are built up using a screen diagram. Cherwell Scientific Publishing Ltd. Tel., 01865 784800; fax, 01865 784801. ■

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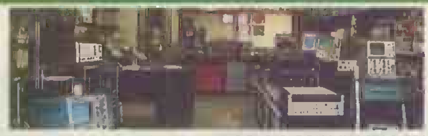

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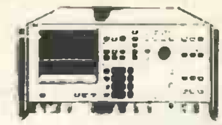

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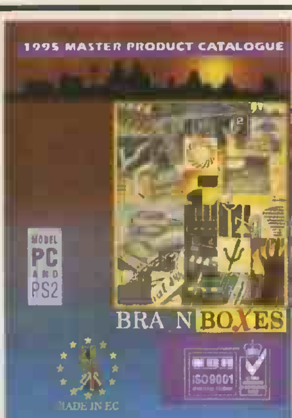

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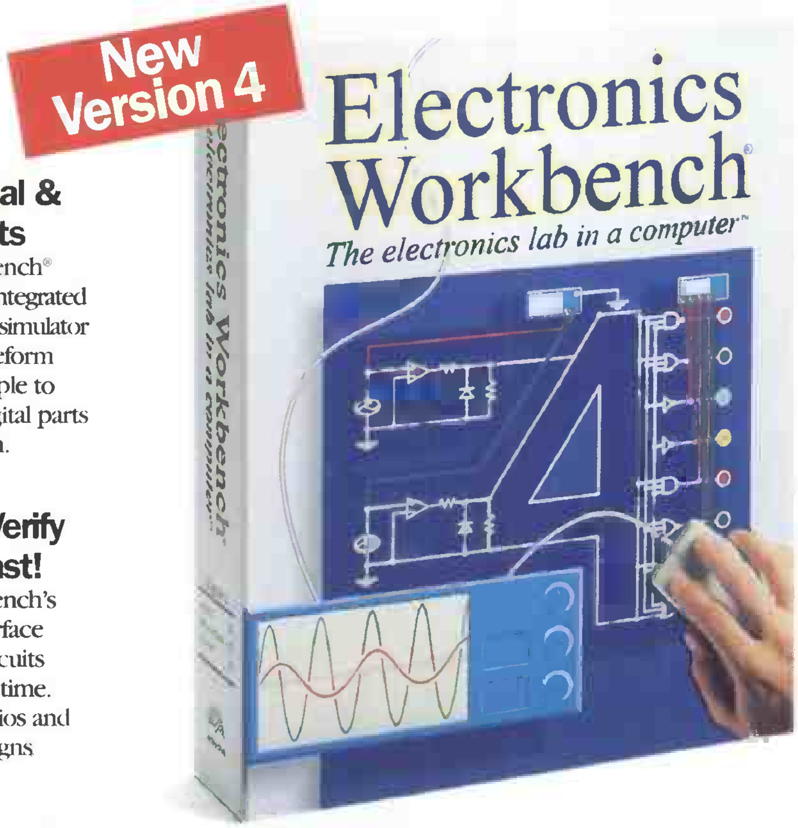

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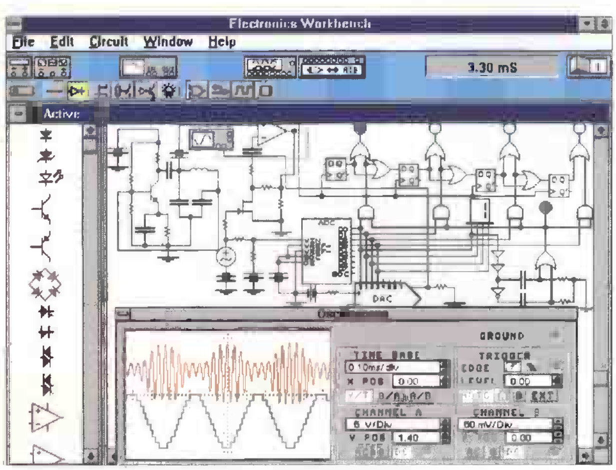

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