The month's top new products – page 39

ELECTRONICS WORLD

MAY 2002 £2.95

Cable fault locator

Making your own PCBs

Setting LC oscillators

Super-regen applied

VHDL primer

Win a Hitachi Worldspace radio worth £149

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Circuit ideas:

Circuit ideas: motorbike gear display, three-component voltage doubler and more...

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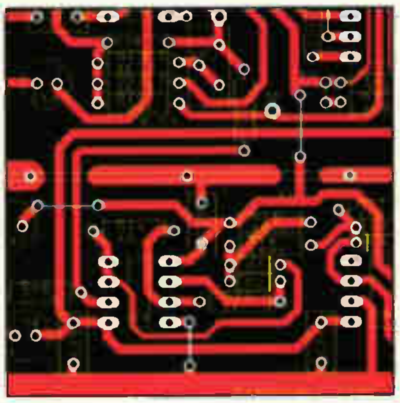

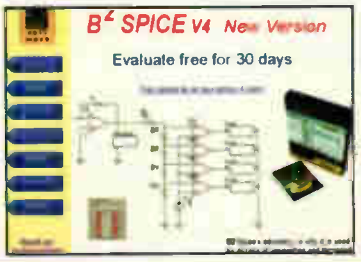

Turn to page 28 to find out how to win this Hitachi WorldSpace radio worth £149. It receives terrestrial broadcast bands as well as WorldSpace satellite transmissions.

Find out at a glance which gear your motor bike's in with Pekka Ritamaki's gear indicator – Circuit Ideas, page 32.

This cable-fault locater allows you to locate faults in coaxial cables using time-domain reflectometry – page 12.

June issue on sale 2 May

EDITOR
Martin Eccles

CONSULTANT
Ian Hickman

EDITORIAL ADMINISTRATION
Jackie Lowe
020 8722 6054

EDITORIAL E-MAILS
J.lowe@cumulusmedia.co.uk

GROUP SALES
020 8722 6028

ADVERTISEMENT E-MAILS
j.thorpe@cumulusmedia.co.uk

EDITORIAL FAX
020 8722 6098

CLASSIFIED FAX
020 8770 2016

NEWSTRADE ENQUIRIES
020 7907 7777

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SUBSCRIPTION HOTLINE
Tel (0) 1444 475662
Fax (0) 1444 445447

SUBSCRIPTION QUERIES
rbp.subscriptions@rbi.co.uk
Tel (0) 1444 445566
Fax (0) 1444 445447

Genesis of a Digital Utopia

What a piece of work is man, how noble in reason, how infinite in faculties, In form and moving how express and admirable, in action how like an angel, in apprehension, how like a god;

-Hamlet, II, 2

Not in Eden was the tree of knowledge found, though its fruit may yet give us pause for thought. When in 1945, ENIAC was revealed to the world, few understood the profound changes that the electronic digital computer would have on almost every aspect of our daily lives. Similarly, although the announcement on 26 June 2000 giving notice of the first rough draft of the human genome made headline news, it was soon drowned out amidst the clamour of other world events all competing for media attention. But these two developments will not go away, and despite the apparent dissimilitude of their origins, the principle that unites them and makes them vitally different from every technological advancement that has gone before, is that of digital information.

Most of us are familiar, at least in principle, with the idea of the digital computer; its fundamental unit of information is the binary digit, or bit, and by combining bits in appropriate patterns we can represent code, data or information in any form we like. The possible combinations are infinite, and so too the possible applications of the technology.

At first sight, it might appear as if genetics does not fall into the realm of the digital, but indeed it does, although the basic unit of information here has one of four, rather than two, representations. To understand how this works, we need to review the rudiments of genetic science.

Each human being has 23 pairs of chromosomes, found within the nucleus of every cell. Each chromosome is made of a very long DNA (deoxyribonucleic acid) molecule, in the now familiar shape of the double helix. If we think of this double helix as a twisted ladder, then the rungs are made up from one of four possible *bases*: adenine, guanine, cytosine or thymine. These are normally referred to as AGC or T for short. Sequences of these bases, from a few thousand to a few hundred thousand, go to make up each gene. The human genome has approximately one hundred thousand genes, and there are about 3 billion bases within the total cellular DNA.

Genes determine almost everything about us, from the exact length of our ear lobes to the dexterity of our right hands. Geneticists will also tell you that they strongly influence such things as intelligence, character, susceptibility to disease and a host of other traits that were once very hard to define in terms of their biological origins.

It comes as little surprise to learn therefore, that vast amounts of money were spent in sequencing the human genome, under a united and international programme called the Human Genome Project, formally initiated in 1990 by the US Department of Energy and the National Institutes of Health. In a twist of fate that is no coincidence, its success would simply not have been possible without the involvement of automated, computerised sequencers. But the links between these two scientific achievements do not end here.

When ENIAC was first completed, it contained 18 000 valves, consumed 150 kilowatts of power and performed 5000 additions or 357 multiplications per second. Recently, Motorola announced its latest *Starcore* DSP chip – little bigger than a 50p piece, and capable of nearly *five billion multiplications and additions per second;* all this, in the space of 57 years.

This degree of digital power represents not merely a quantitative, but a qualitative change in our relationships with scientific problems, enabling us to unlock the quantum secrets hidden within the very heart of our universe. Just as the currency of our brains is thought, so too the currency of digital computers is number.

So now we can effectively rewrite certainty, altering information in a way that was possible only conceptually forty years ago; an engineer or scientist from this time would be struck dumb by the feats we can now achieve. Despite all this, the digital computing revolution is still in its infancy.

And what of the science of genetics? We know that the sequence of bases on a gene is the code that instructs a cell how to manufacture a single protein; by altering this *digital code* of AGCT, we can alter the gene and change the organism, subtly or, if we wish, radically. We have indeed become as God. Mice have already been genetically modified with enhanced memory and problem-solving skills, and human medical applications are simply too numerous to list.

Make no mistake, this is just the start. The computer revolution has been with us for less than sixty years, and it has seen a billion-fold increase in power since it began. We can probably not even conceive of the advances that will be made in the science of human genomics over such a span; the idea of human immortality is no longer a wild and ridiculous fantasy.

Three things are however clear. First, both these digital revolutions represent a paradigm shift in our relationships with the physical world, for by altering code sequences, we can restructure our very reality. Second, developments in computing and genetics will continue exponentially and fuel the advances in almost all other sciences during the 21st century. Finally, and worryingly, our global political systems have not moved forward at a rate commensurate with the enormous leaps in these areas.

Hamlet correctly observed that in action, man can be as a god but he omitted to mention that he could also be the very Devil. The benefits or curses these things will bring us very much depend on our systems of government, which too often across our globe, are underpinned by greed and an all-consuming lust for power. It is up to us whether we create a hell, or sow a new Eden, and it is high time we gave this some thought.

Patrick Gaydecki

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New multiplier algorithm is twice as fast

A multiplier algorithm developed by Oxford start-up Automatic Parallel Designs is twice as fast as existing designs, the company claims.

AutoPD also has a floating-point multiplier that is currently being evaluated by "one of the largest CPU companies", and algorithms under test at two other "major" CPU manufacturers.

According to its chief technology officer Sunil Talwar, the firm's efficient arithmetic building blocks are based on "mathematics dating back to the Indians in 1000AD, developed by the Chinese in 1303, and coming together with Pascal's Triangle in 1709".

"People currently only know how to add three numbers efficiently in a column," said Talwar. "If they want to add more numbers they build [adders] out of these basic count-up-to-three building blocks. It's very slow, lots of logic levels, plus very bad wiring." AutoPD's multiplier designs enable customers to choose between a one and-a-half times reduction in area or increased speed, versus existing multiplication schemes. The modular designs are optimised for silicon and available as either reference RTL or licensable IP.

"We are negotiating with one large FPGA company – they're chasing the DSP market at the moment," explained Talwar. "We're under evaluation at all the major DSP companies, but we've just seen a real slowdown in the industry there." As well as the arithmetical building blocks, the company has also devised an encryption algorithm, for which it has a licensee. "Things are nice," mused Talwar.

A mathematician, Talwar founded AutoPD in 1998 with Tony Curzon Smith, an economist. Initially funded by a SMART award, last year they raised £2.5m from venture capital firm Quester, with a further £500 000 from the seed backers and £200 000 in DTI awards.

With 12 full-time staff, the company has a sales office in Austin, Texas, and does all its business in the US. Dr Earl Swartzlander, a leading authority on computer architecture, has recently been appointed as a technical adviser.

Mini speakers have low resonant frequency

Nothing escapes scrutiny in the effort to make mobiles smaller and better. With this in mind, Matsushita has announced a range of mini-loudspeakers for 3G phones.

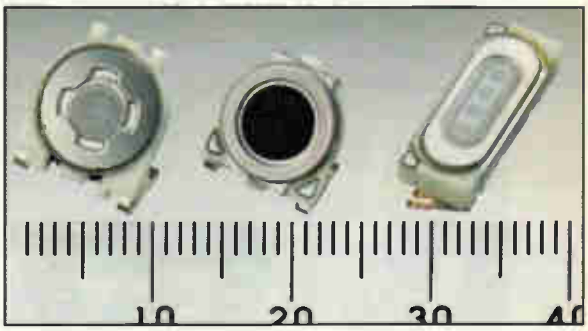
The problem with existing designs, says the company, is the air gap between speaker and ear that ruins low-frequency reproduction.

Countering this, the new speakers do not rely on a seal between phone and user, but have an inherently low resonant frequency on their own.

The key is a new diaphragm material, a special amorphous polymer with a low elastic modulus and high internal loss.

Three types are available, the best one achieving a 380Hz resonant frequency – close to the bottom of the spoken range.

The largest one in the picture is 10mm in diameter and 2.6mm thick. Mass is 0.52g. Production should begin this July.



Specifically designed for tracking plastic packaging assets, magnetic tagging company Flying Null has introduced a toughened tag. They can be "boiled, frozen, even run over by a forklift truck," said Flying Null. The new device is launched following life-cycle testing at Demes Logistics.

Get a Master's degree on the Web

Scotland's Institute for System Level Integration (ISLI) has extended its groundbreaking Master's degree in system level integration to Web users.

The online version of the degree will be aimed at part time students already working in the industry and those from overseas.

"We had a lot of interest in flexible learning from industry," said Professor Steve Beaumont, director of the ISLI. "We also have a lot of interest from overseas."

Beaumont expects that most students would complete the course in around three years.

"We're going to provide a lot of e-mail, telephone and online support plus online library facilities," he said. Like many Open University courses, the ISLI degree will still have a residential element for some of the lab work.

Eventually the concept could be extended to the Institute's four year long Engineering Doctorate, which took its first students in October 2000.

Located at the Alba Centre Campus in Livingston, the ISLI is an academic collaboration of four Scottish universities: Edinburgh, Glasgow, Heriot-Watt and Strathclyde. It opened its doors to students in March 1999 and offer both full and part time MSc degrees.

www.sli-institute.ac.uk

One-stop PCB prototyping

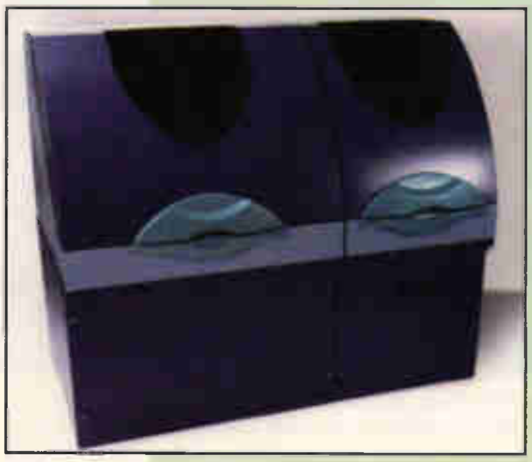
The Kwikboard division of Sigtronics, the Scottish PCB machine company, is launching its nation-wide UK network of one-stop prototyping outlets.

"The company is doing deals with PCB manufacturers around the country, leasing Kwikboard machines to them so they can offer rapid PCB prototyping," said a spokesman for the company. "Four have already signed up and we are looking to sign up 15 by the end of the year."

Kwikboard claims that a finished PCB can be produced in less than three hours.

The prototyping system is additive, rather than subtractive with a copper polymer being printed onto the PCB. "You can still do all the normal soldering operations that you can do on conventional PCBs," said the spokesman.

Its printer is made up of four stations: micro engraving, polymer application, curing and laminating. Unlike the conventional PCB process, no acids or etchants are used said Kwikboard.



1.3Tbit/s over an 8400km optical fibre

In a test using a single optical fibre and 65 signals of 20Gbit/s each, Mitsubishi has succeeded in sending 1.3Tbit/s down 8400km of optical fibre.

"This is the highest transoceanic class transmission capacity achieved to date," said Takashi Mizuochi, head researcher at Mitsubishi.

The record required four developments, said the company: effective fibre area management, symmetrically-collided transmission, 20Gbit/s equipment and hybrid optical repeaters.

With distributed Raman amplification, effective fibre area – A_{eff} in **Fig. 1** – is an important parameter as amplification efficiency is proportional to the power density in the fibre core. Previous type of fibre design, Fig. **1a)**, arranges the smaller Aeff fibre in the final section. Raman gain is concentrated in the final section.

Mitsubishi shifted the smaller Aeff fibre to the middle section, Fig. **1b)**. The company says this improves the optical signal-to-noise ratio, because the smaller A_{eff} fibre provides the major part of the Raman gain in the middle section, light amplification becomes more closely ideal distributed amplification.

Symmetrically-collided transmission is important as higher bit-rate signals are easily degraded by fibre non-linearity induced by pulse collision between the different wavelength channels.

Once optical pulses having different wavelength collide with each other, **Fig. 2a)**, fibre non-linearity causes significant signal distortion.

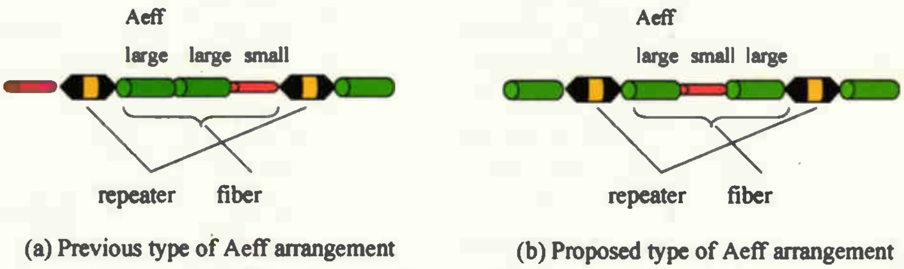


Fig. 1. With distributed Raman amplification, effective fibre area – A_{eff} – is an important parameter as amplification efficiency is proportional to the power density in the fibre core.

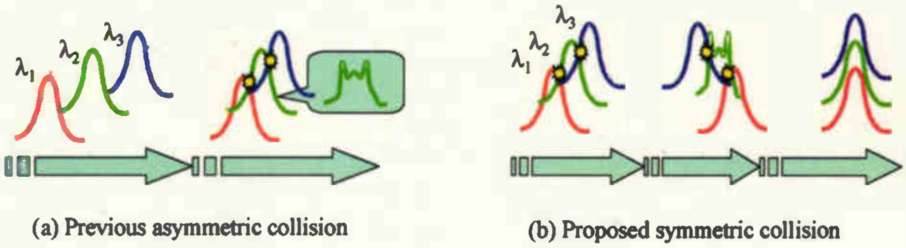


Fig. 2. Once optical pulses having different wavelength collide with each other, a), fibre non-linearity causes significant signal distortion. If collisions are intentionally made again, signal distortion is cancelled out, b).

If collisions are intentionally made again, signal distortion is cancelled out as shown in Fig. **2b)**.

Asymmetric collisions are the rule because the variations in fibre loss, dispersion and repeater gain along the transmission path combine to destroy the symmetry. Mitsubishi makes symmetric collisions by optimising the dispersion map and the ratio of distributed Raman amplifier to Erbium doped fibre amplifier gain. The resulting controlled pulse collisions reduce the pulse distortion said the company.

'Fully engineered' 20Gbit/s optical sender and receiver equipment was used, including newly developed SiGe integrated circuits. Using multiplexing technology, the equipment is usable at 40Gbit/s said the firm.

The hybrid repeaters use distributed Raman amplification followed by an erbium-doped fibre amplifier (EDFA). Mitsubishi has started submarine grade reliability qualification.

NXT launches disposable cardboard speakers

Cheap, cardboard loudspeakers from Cambridge audio technology firm NXT perform as well as conventional models costing "three to four times" as much, according to the company.

The £30 'SoundpaX' speakers are delivered flat-packed, and fold into 700mm tall pyramids. NXT's marketing director Andrew Williams said the new speakers would be ideal for parties and barbeques: "if they have to be thrown away afterwards, it's no big deal."

Using the firm's SurfaceSound technology, an electromagnetic exciter coil on the inside of one face forces vibrations across the whole structure. The 8Ω units can be produced with any pattern, although the first models have a picture of a traditional-looking speaker cone on the front. Eventually they will be supplied with their own 15W amplifier. Low-range frequency response, seen by some as the weakness of the NXT technology, is around 60Hz.

Rad-hard processor has hardware error protection

A French design firm has created a radiation-hardened processor that uses extra hardware to prevent errors occurring in logic and memory. Moreover, iRoC Technologies claims to have proven the extra circuitry does not impact performance.

iRoC designed error detection and correction circuits for memories and logic circuits to avoid single-event upsets (SEUs) caused by cosmic radiation.

The shift to more advanced processes means SEUs and other soft errors, such as logic races and glitches, are appearing not just in space-borne equipment, but also in earth bound electronics.

"Today our solutions can eliminate the vulnerability of electronic systems to transient errors which affect their availability and reliability," said Eric Dupont, president and CEO of iRoC.

The firm built 0.25μm test chips of both its ROC S81 design and LEON, the Sparc V8 32-bit Risc processor on which it based its design.

Both devices were stressed by a cyclotron to stimulate soft errors, which were observed in LEON, but not in the S81 device. Moreover the extra circuits, around 17 per cent extra, needed to detect the transient pulses did not slow the chip, said Dupont.

"I've reviewed the test results and am convinced that this approach offers designers the ability to achieve cost savings while bringing a protected system to market much faster," said Joseph Borel, a VLSI expert and formerly director of design automation at STMicroelectronics.

At 0.13μm, iRoC reckons SEUs and other soft errors, such as glitches, races, crosstalk and ground bounce, can come at the rate a one every few hours. While other error correction systems concentrate on memory, iRoC claims logic is just as vulnerable. Memory can be checked through standard error correction schemes, logic has no such fallback. The aerospace solution of replicating logic several times over is unsuitable for modern electronics, especially in the price sensitive consumer world.

Processor works in highly radioactive environments

If you happen to be building a satellite, you may want to get hold of RAD750 – claimed by maker BAE Systems to be the most powerful radiation-hardened general purpose microprocessor ever developed for space.

"The processor has successfully passed manufacturing and environmental testing and is ready for civil, military and commercial satellite applications," said Dale Hutchinson, executive v-p at BAE.

Clock rate is 133MHz for this toughened version of the PowerPC 750, and at 240 million instructions per second, BAE said it has nearly ten times the processing capability of current space processors.

Radiation in a geostationary orbit should only cause one upset every 10 years.

A companion Asic, dubbed Power PCI, has been developed to provide a bridge between the CPU, main memory and a PCI bus.

Ultra-bright electroluminescent displays

Alternating current thin-film electroluminescent displays, demonstrated by Sharp as early as 1974 and subsequently forgotten by industry, are getting a new lease of life at Nottingham Trent University.

Together with the Rutherford Appleton Labs in Oxfordshire, the University has made a super-bright head-up display demonstrator.

The displays, called ACTFEL and shortened to TFEL, fell by the wayside as emphasis on full-colour side-lined this predominantly yellow-emitting technology.

The Nottingham researchers decided have taken another look – forgetting full-colour and pushing the technology for what it is really good at: high-intensity.

Essentially a sandwich of two conductors with a insulated phosphor between, TFEL displays rely on exciting phosphors with capacitively-isolated AC fields - typically 250V 5kHz.

Dr Wayne Cranton of Nottingham said a problem with conventional TFELs is the high refractive index of the phosphor, which tends to trap light – up to 90 per cent – in the phosphor layer.

Light escape can be boosted by surface treatments, but Cranton has turned the problem of trapping on its head and made a virtue of it. He increase's entrapment and uses the phosphor layer to guide emitted light to an angled micromirror. The mirror bounces light out of the display at right angles.

Intensities of 17 000cd/m^2 at 580nm have been demonstrated – compared with around 400cd/m^2 for a TV turned up to full brightness – using zinc sulphide doped with manganese (ZnS:Mn). This is the most efficient TFEL thin-film phosphor and 68 000cd/m^2 has been squeezed out of an array of mirrors and phosphor.

Light is piped sideways to a mirror by a high refractive index emissive phosphor film between 0.5 and 1µm thick. Phosphor planes 100µm wide make the most effective use of light. For narrower angles of emission, lenses can be made in the passivation layer.

A laterally emitting thin film electroluminescent (LETFEL) chip 4mm across. Each line is an aperture with a mirror running down the centre. It is aimed at head-mounted displays where it appears to hang in space.

IoW firm wins second Government SMART award

Signal processing specialist RF Engines, based on the Isle of Wight, has won a second Government SMART award.

The company's first grant was used to develop a pipelined frequency transform (PFT) architecture, which the firm has now patented. The PFT can perform broadband filtering and Fourier transformation in standard programmable logic chips.

The money from the latest SMART award will be used to develop a tuneable version of the transform.

"We qualified for the maximum award which is £45 000," said John Summers, sales and business development director at the firm. "The standard PFT operates by creating a filter bank, and filters are spread evenly across the bandwidth," he said.

"In the tuneable PFT the user can focus down on frequencies of interest. The user can create the shape and type of filter needed."

This enables Fourier analysis to concentrate on specific frequencies, throwing away unwanted data prior to processing.

The company said a tuneable PFT has applications in defence and communications. "It would apply in certain 3G applications but also in 4G," said Summer.

It could be useful in pulling signals out of low-power spread-spectrum comms, with implications for defence and security.

The firm also develops intellectual property for Fourier transforms particularly in complex front-end designs, where real time analysis is important. The standard cores include wide and narrow band designs.

RF Engines' chief executive John Lillington with the firm's second SMART award.

New FM radio chips remove the need for trimming

You can make an FM radio without having to trim it at all, following the release of two new chips from Philips.

The hi-tech radio devices are specifically aimed at adding FM reception to portable electronic devices including phones, MP3 players and PDAs. As such, they do need a host processor to operate.

"We have made a significant cut in the number of external components needed to build radio function into a cell phone," said Keef Joosse of Philips.

A complete radio from aerial signal in to line level audio out, according to Joosse, can be built onto a 9 by 9mm patch of PCB if both sides are used. "Only 15 to 17 external components are needed," he said, and despite none of them being precision components no adjustment whatever is needed to make an FM radio.

The BiCMOS chip is a low-IF design, using an intermediate frequency somewhere between 100 and 200kHz. Quadrature mixing is used in the frequency conversion stages. The on-chip synthesiser gets its reference from the host processor, several frequencies are supported including watch-chip crystals and 13MHz.

The new chip includes a fair amount of intelligence and will automatically scan up or down on command from the host processor. It includes station presets and all control it through a serial bus. One version of the chip is purely I^2C, the other also includes a three-wire control bus.

The price is around $3 in 10 000 quantities. The TEA5767 is due out very soon, the TEA5768 slightly later.

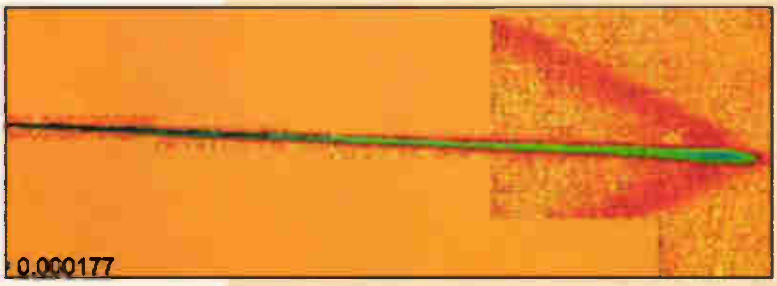
This is fuel injection in action. The nozzle is 178μm across and the fuel is moving at 345m/s.

Normally this photo would be impossible because of a dense fog of fuel particles that precludes normal photography.

To take it a special one-off X-ray camera was developed by researchers at Cornell University in New York capable of capturing a succession of microsecond.

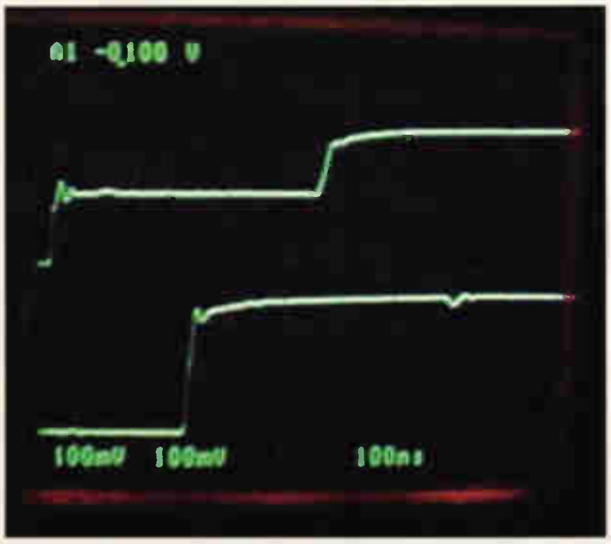
The light sensor is a 9200 pixel two-layer custom chip. On top is a layer of 150μm X-ray conversion pixels. One solder bump per pixel connects signals to the second layer were the image is captured.

Eight images can be stored before the device has to be read. The university has now moved on to designed sensors with 45 000 pixels and experiments are under way to bump-bond four chips together to build larger area detectors with as many as 726 000 pixels.



Cable Fault locater

David Huddart's first fault locater, presented a few months ago, was remarkable in that it allowed you to pinpoint faults along the length of coaxial cable at very low cost. David's first reflectometer relied on a fairly fast oscilloscope for displaying its output. His latest version is stand-alone...



This cable-fault locater allows you to locate faults in coaxial cables using time-domain reflectometry. It is low cost, very portable and yet easy to use and reasonably accurate.

The design was developed from a previous time-domain reflectometry design[1] which, while very simple, needed access to a fast oscilloscope to use it – a little inconvenient in dusty loft spaces!

Background

A time-domain reflectometer sends a very fast-edged pulse into a cable and then looks for reflections. If the cable isn't correctly terminated by its characteristic impedance, a return echo will be observed that is delayed by twice the transit time of the cable (go and return).

If the cable is accurately terminated, no return echo will be seen. The extremes of cable faults are of course open or short circuit.

When a fast edge pulse enters a transmission line, the initial impedance is the characteristic impedance of the line. This is logical as, at that time, the electrons have no way of knowing what lies ahead of them at the end of the transmission line. Energy is therefore entering the line from t = 0 according to:

$$\frac{V}{I} = Z_0$$

Once the pulse reaches the end of the line an open or short circuit termination will dissipate no power so the energy stored in the line must now return to the start and be dissipated in the signal generator output impedance.

Fig. 1. Reflections in an open-circuit line. Upper trace is the transmitted signal. Lower trace is the pulse at the far end of cable. Note how the voltage at the far end is twice the initial transmit voltage to the line.

In the case of an open circuit, this is seen as a doubling of the applied voltage. Energy is stored in the line capacitance to be returned to the signal source on the falling edge of the pulse, **Fig. 1**. In the case of a short circuit the transmit voltage drops to 0V, **Fig. 2**, and energy is stored in the line inductance until the falling edge of the pulse.

As no cable is totally without loss, the actual values may be reduced especially on long cable runs and for short-circuited lines.

How the TDR meter performs

This TDR meter generates the fast pulses needed, then measures the echo time delay and calculates the distance. It is capable of resolving distance to an accuracy of approximately 5%, if carefully calibrated. It has a maximum range of 200m and is usable down to about 5m.

The idea for the design came from comments made about my previous article and set me thinking of a low cost but self-contained solution. My initial thoughts centred on fast digital counters to measure time delay, with some form of high-speed sampling device such as a very fast comparator. After a few sums though, followed by a search for

Circuit boards

Details of double-sided PTH circuit boards can be obtained by sending an SAE to 'Reflectometer', Electronics World, Cumulus Business Media, Anne Boleyn House, 9-13 Ewell Road, Cheam, Surrey SM3 8BZ.

available fast CMOS logic devices, I decided that any resultant device would be expensice and possibly not as portable as I had in mind.

I then started to think how my oscilloscope measures time. Its time base consists of a linear ramp generator and trigger circuit. Some hours of contemplation later and I was on the track of a device that would generate a square-wave with fast edges and would sample the line voltage at an adjustable time period after the positive-going edge.

By adjusting the time delay, I could look for the sudden change in voltage on the line indicating a return echo. Once the echo point was located manually using a meter to display the sampled voltage, it was just a matter of displaying the time interval, or better still, the distance to the cable fault.

The final solution is a simple design that has performed well in the field. It is not the most accurate of instruments, but it is perfectly adequate for the intended application of locating cable faults to the nearest couple of metres.

In my experience, by the time you are in the correct room, the source of the problem is usually only too obvious. In any case, if you knew the distance to the nearest 10cm, would you then use a tape measure to trace the path of the cable exactly anyway?

How it works

Figure 3 is a block diagram of the unit. An oscillator, V_1, generates a square wave with fast edges of less than 3ns. These edges are coupled to the line via a buffer and 50Ω coupling network.

Sampling gate S_2 is switched on when the positive going pulse is transmitted to line and so allows the parasitic capacitance of a FET input buffer amplifier to charge to the actual line voltage.

A timing circuit comprising C_1, RV_1 and IC_2 switches the sampling gate off. This timing circuit is varied from 0 to 3µs by RV_1. When the gate turns off, the instantaneous voltage on C_2 is held. Capacitor C_1 is discharged every cycle by S_1.

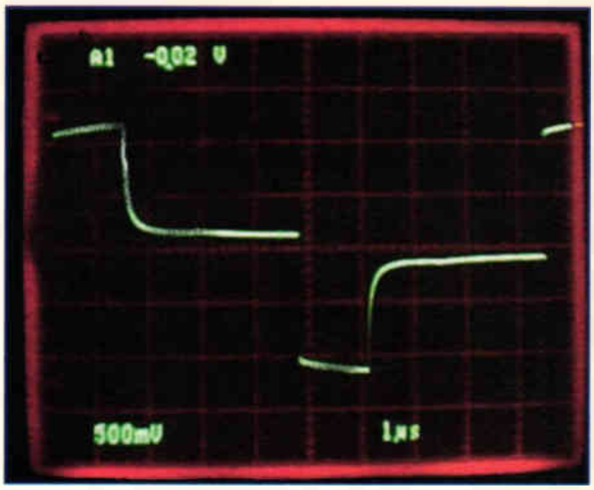


Fig. 2. Reflections in a short-circuit line.

In the final design the on duty cycle for the sample gate is very low – less than 1% – and so the average voltage across C_2 is very close to the sampled voltage.

To measure the distance to an echo, RV_1 is adjusted while observing the return echo voltage on the meter until a sudden drop or increase is seen. This will be the echo.

TABLE 1. Circuit operating conditions

Dielectric type	Velocity coefficient	$V_{full\text{-}scale}$ at C_{11} (mV)	10m range		25m range		50m range		100m range		200m range	
			t_{max}	F	t_{max}	F	t_{max}	F	t_{max}	F	t_{max}	F
Polyethylene	0.66	50.51	101.01ns	100kHz	252.53ns	40kHz	505.05ns	20kHz	1010.10ns	10kHz	2020.20ns	5kHz
Foamed polyethylene	0.78	42.74	85.47ns	100kHz	213.68ns	40kHz	427.35ns	20kHz	854.70ns	10kHz	1709.4ns	5kHz
Air-spaced polyethylene	0.84	39.68	79.37ns	100kHz	198.41ns	40kHz	396.83ns	20kHz	793.65ns	10kHz	1587.3ns	5kHz

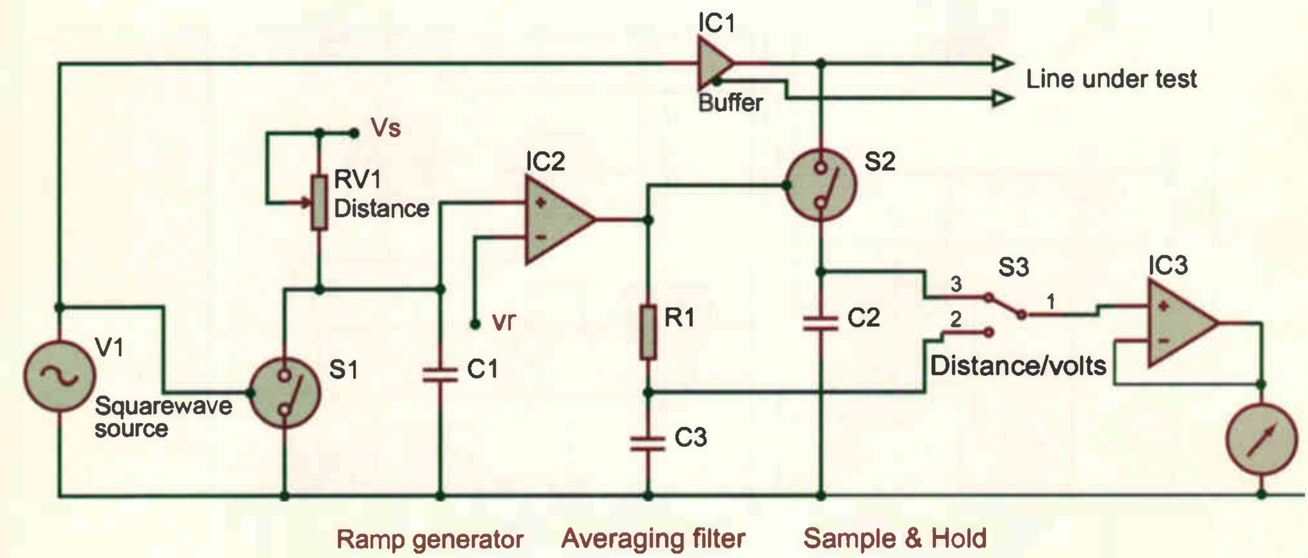


Fig. 3. Fast-edged square waves from V_1 are coupled to the line under test via buffer, IC_1. Remaining circuitry samples and displays the reflection.

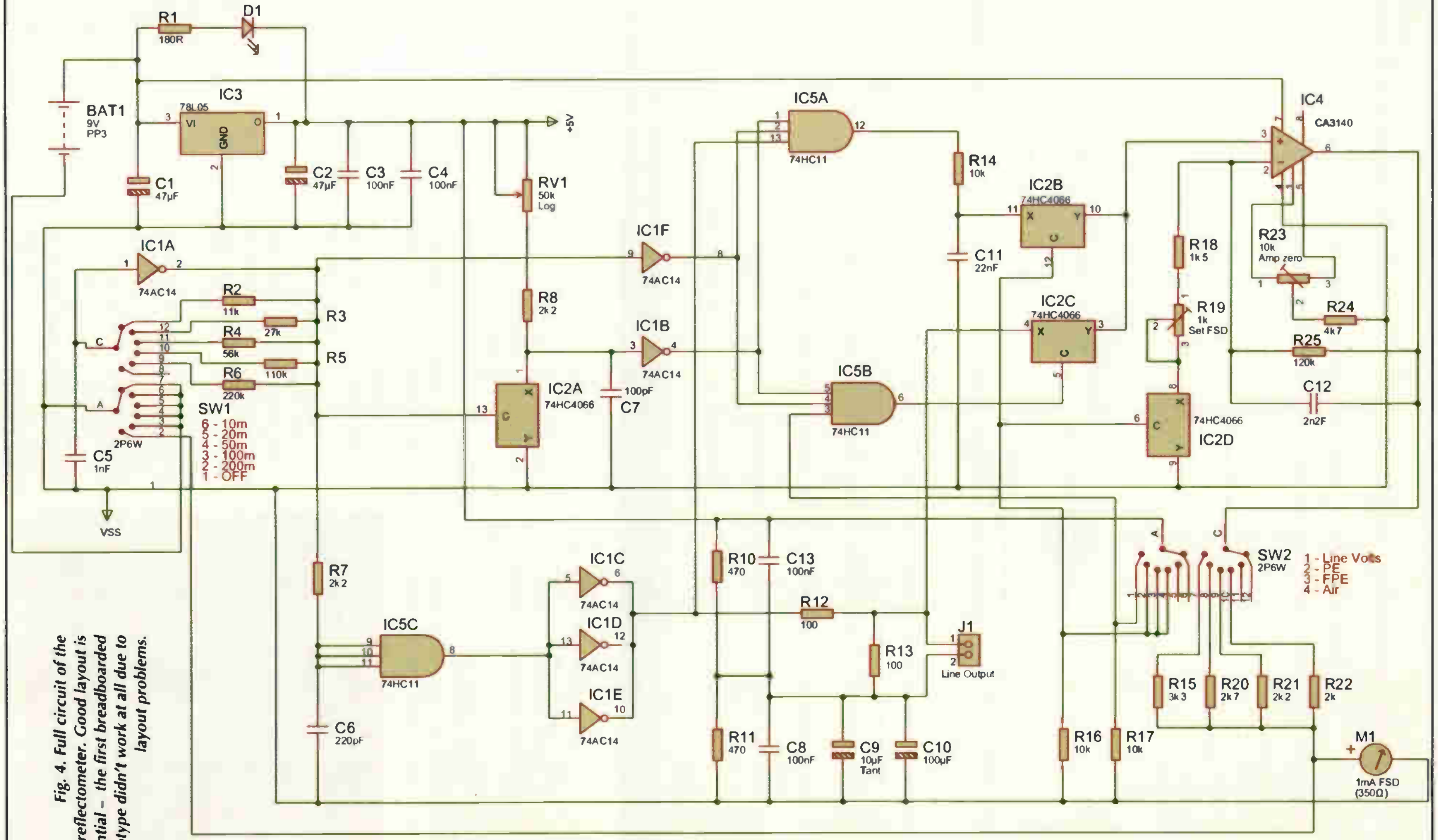


Fig. 4. Full circuit of the reflectometer. Good layout is essential – the first breadboarded prototype didn't work at all due to layout problems.

Switching S_3 to 'measure', i.e. position 2, allows the distance to be read off. Distance is proportional to the echo time but also depends on the velocity coefficient of the cable (more of this later).

The duration of the sample gate pulse is therefore proportional to distance. Provided voltage levels are stable, the DC derived from the filter, R_1, C_3, will also be proportional to distance. With S_3 in the 'measure' position, the distance setting of RV_1 is displayed on the meter.

In the final design, range is changed by switching the clock frequency. As the pulse width from IC_2 is controlled only by the echo delay, but the voltage across C_2 is a function of the pulse width and frequency, it is possible to change range by changing the clock frequency.

To compensate for the differing velocity coefficients of cable types, the gain of IC_3 is switched to give accurate distance measurements. Details of this are given in **Table 1**.

Circuit details

This section is a little hard going and may be safely skipped unless you wish to understand the finer details of how the reflectometer works.

Figure 4 shows the full circuit. The clock signal is generated by IC_{1A}, R_{5-6}, and C_5. Buffer IC_1 is a Schmitt trigger. Switch SW_1 controls the clock frequency and hence range indicated on the meter. Approximate clock frequencies for each range are given in Table 1.

The pulse stream, delayed by approximately 300ns, is transmitted to line via $IC_{1C,D\&E}$. Paralleled buffers provide a low-impedance and fast-rise-time edge to the network R_{10-13}, $C_{8-10,13}$. This network adjusts the drive impedance to 50Ω, to attenuate the signal to 2.5V pk-pk and to raise the logic-zero level to approximately 1.25V.

Matching at 50Ω is desirable to reduce the effects of returned echoes 'bouncing off' the cable locater due to mismatch and in effect causing an additional erroneous pulse. Having said that, the unit has been used with 75Ω cables very effectively as the mismatch is not too severe.

If you are considering using the meter with vastly different impedances – 120Ω for example – $R_{12,13}$ should be adjusted to equal twice the cable impedance.

The reason why the logic 0 level signal needs to be above ground is that the sampling gate IC_{2C} will only accept signal levels between 0 and 5V. Any ringing in the cable under test may exceed these limits unless precautions are taken. It is important to appreciate that the coaxial connector earth is *not* connected to the circuit 0V though.

Turning now to the variable delay circuit, IC_{2A} holds C_7 shorted to ground while the transmitted pulse is at logic zero. Some 300ns before the pulse goes to logic one, IC_{2A} is turned off and C_7 is allowed to charge via RV_1 and R_8. After 0.2-3μs, the threshold of IC_{1B} is reached its output drops to logic zero.

Note that as the pulse to line is delayed by 300ns, this will occur between –0.1 and +2.9μs after the rising edge of the transmitted pulse. This pulse is now gated with the clock from IC_{1A} such that IC_{5B} is only at logic one from the time the positive pulse is sent to line, until C_7 times out. This gives it a duty cycle of 0 – 1%.

This signal is used to switch off the sample gate – S_2 in Fig. 3 and IC_{2C} in Fig. 4. Voltage to line is frozen on the input capacitance of IC_4. This voltage is displayed on the meter when SW_2 is in position 1.

In use, RV_1 is adjusted from 0 – noting the positive transmit pulse transition – until the echo is noted when there's a sudden rise or fall. Switch SW_2 is then turned to measure and the distance is read from the meter.

The range is measured by taking the average of the signal used to operate the sample gate. The off time is set to at least 99% by the frequency of the clock generator. The on time is set by the echo time as set above.

In Fig. 4, the averaging circuit is R_{14}, C_{11} or R_1, C_3 in Fig. 3. When SW_2 is in the measure positions, namely 2, 3 or 4, IC_{2B} gates the voltage from C_{11} to be amplified by IC_4 and displayed on the meter.

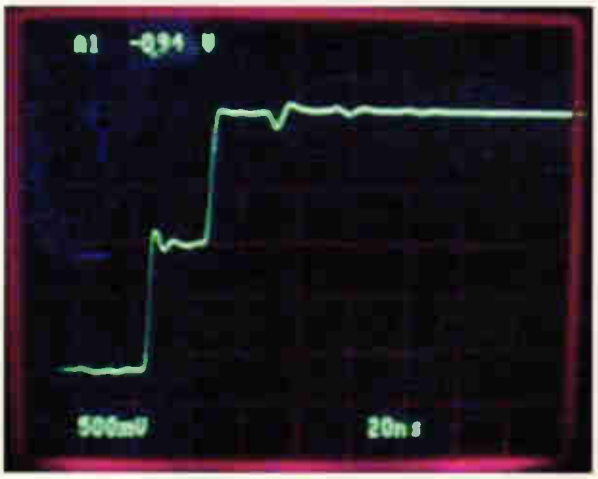
Scaling for differing dielectrics is catered for by R_{20-22}. Range is set by SW_1 switching the frequency of the clock. The effect of this is to multiply the filtered DC voltage, V_{C3} in Fig. 3, by the ratio of the p.r.f.

For example, if the pulse-repetition frequency were 10kHz, on the 100m range, and the full-scale deflection direct voltage across C_{11} were 50mV, it would become 100mV if the frequency were switched to 20kHz. Capacitor C_{11} is the equivalent of C_2 in Fig. 3.

In order to display range in metres and not nanoseconds, it is necessary to take into account the velocity

Parts List

Qty	Part ref.	Value
Resistors (all fixed value are 1/4W 2%)		
1	R_1	180R
1	R_2	11k
1	R_3	27k
1	R_4	56k
1	R_5	110k
1	R_6	220k
3	$R_{7,8,21}$	2.2k
2	$R_{10,11}$	470
2	$R_{12,13}$	100
4	$R_{14,16,17}$	10k
1	R_{23}	10k preset RS 187-113
1	R_{15}	3.3k
1	R_{18}	1.5k
1	R_{19}	1k preset RS 187-084
1	R_{20}	2.7k
1	R_{22}	2k
1	R_{24}	4.7k
1	R_{25}	120k
Capacitors		
2	$C_{1,2}$	47µF 16V elec.
4	$C_{3,4,8,13}$	100nF multi-layer ceramic
1	C_5	1nF ceramic NPO
1	C_6	220pF ceramic NPO
1	C_7	100pF ceramic NPO
1	C_9	10µF 10V tant. bead
1	C_{10}	100µF 10 V elec.
1	C_{11}	22nF ceramic multi-layer
1	C_{12}	2.2nF ceramic NPO
Integrated Circuits		
1	IC_1	74AC14 RS 169-0036
1	IC2	74HC4066
1	IC3	78L05
1	IC4	CA3140
1	IC5	74HC11
Diodes		
1	D_1	LED 5mm
Miscellaneous		
1	BAT_1	9V PP9
1		Battery connector RS 489-021
1	RV_1	50K log. RS 263-3236
2	$SW_{1,2}$	2P6W RS 665-196
1	M_1	1mA FSD (350/400Ω) Maplin RW94C
1	J_1	50Ω BNC socket
PCB, knobs etc.		
Case RS 343-9372		



Reflections into a mismatched 75Ω open-circuit cable show that measurements can still be made.

Table 2. Coaxial cable characteristics

Cable type	Manufacturer	Impedance	Velocity coefficient	Dielectric
RG8	Belden 9913	50	0.84	ASPE
RG59B	Belden 8263	75	0.66	PE
RG11	Belden 8213	75	0.78	FPE
RG58A	Belden 8219	50	0.78	FPE
RG58C	Belden 8262	50	0.66	PE
RG174	Belden 8216	50	0.66	PE
RG213	Belden 8267	50	0.66	PE
RG214	Belden 8268	50	0.66	PE
RG223	Belden 9273	50	0.66	PE

PE represents polyethylene, ASPE represents air-spaced polyethylene and FPE represents foamed polyethylene.

Velocity coefficient

The following formula gives the relationship between factors involved in measuring cable length using time-domain reflectometer.

$$l = \frac{t \times V_c \times C}{2}$$

Here, l is the length of cable in metres, t is the time from transmit pulse to echo in seconds, C is the speed of light and V_c is the cable's velocity coefficient. The speed of light is 3×10^8 m/s.

The velocity coefficient is the ratio of the speed of signals through cable to the speed of light. It varies depending on the dielectric used in the cable but is usually between 0.6 and 0.8.

coefficient of the cable being measured.

Table 2 gives specified velocity coefficients for different types of cable. Values are in the range 0.6 and 0.8. For coaxial cables, the controlling factor is the dielectric material used. On that basis, only three settings are available for velocity coefficients covering the common dielectrics used. The effect of changing setting on SW_2 is to adjust the DC gain of IC_4 so that the meter reads in metres.

One final point: in the off position, the meter is deliberately short-circuited. This is an age-old trick to provide mechanical shock protection to the meter movement. The theory is that any movement of the needle will cause an emf to be generated by the meter coil cutting the magnetic field (the reverse of normal operation of a moving-coil meter).

If the coil is shorted current flows and sets up an opposing magnetic field. This resists movement and so prevents damage to the mechanism. As an apprentice, this was drummed into me as essential good practice so I can't resist passing it on.

Finished cable tester.

Putting it together

It is necessary to use good quality multi-layer ceramic capacitors for $C_{8,13,3,\&4}$ to reduce spurious ringing and use good high frequency layout practice. Any common impedance in power or signal rails increases ringing and this in turn will limit the range and accuracy of the unit. I have found to my cost that it is a false economy to use 'economy' grade single-plate capacitors for decoupling in fast logic circuits.

The effect of unwanted ringing would be to blur return the echo somewhat. In use the echo is very clearly seen as an almost instantaneous rise – or fall – in voltage as RV_1 is adjusted. This is possible only because of the very fast and clean edges generated by $IC_{1C,D,E}$.

I have used an AC rather than HC version of the 7414 for better performance. This performance increase will not be realised though unless good decoupling and layout are used. The breadboard version built on Vero board just would not work. A second breadboard built on a piece of copper-clad PCB performed well.

To assist those of you interested in building this design, I have designed and tested a double-sided plated-through hole PCB. Details on this are given separately.

Setting-up

Assuming that the circuit has been assembled correctly and is functioning, only calibration is necessary.

Firstly the offset voltage of IC_4 must be zeroed. Set SW_2 to position 2, RV_1 to minimum. Check that the voltage across C_{11} is less than 1mV. Now adjust R_{23} until a reading is obtained on the meter. Carefully adjust this to 0V but stop immediately when 0V is reached: as this is a single rail system, negative values cannot be displayed.

To calibrate the range, measure 50m of a known dielectric cable using the correct dielectric position on SW_2 and adjust R_{19} for FSD on the 50m range.

Alternatively, set the unit for 50m and poly dielectric, monitor pin 12 of IC_5 with an oscilloscope and adjust RV_1 to make the positive pulse width 505ns. Now set R_{19} for FSD.

All other ranges and dielectric settings should now be calibrated, but using Table 2, it is possible to check every range and dielectric setting.

Using the meter

Polarity of the echo indicates open or short circuit (> or < Z_0) in the cable. Positive echoes indicate high impedance and *vice versa*. The time delay can be used to estimate the distance down the cable where a fault is. The unit will indicate the distance to any echo caused by cable faults or poor joints.

Connect the cable under test and switch to the 100m range and measure volts. Turn RV_1 to zero and observe the reading. This is '0V' to line. Turn RV_1 clockwise and the reading will jump to a new level. This is the 1V to line signal at t=0.

Continue to turn RV_1 till the voltage doubles, representing an open circuit, or returns to 0V representing a short circuit. If this is the distance required to be measured, switch SW_2 to the appropriate dielectric position and SW_1 to obtain a reading.

The TDR has given good service in locating faults in coaxial cable runs, detecting dubious coaxial connections. It even allows you to measure the characteristic impedance of an unknown line by adjusting the termination impedance of a length until minimum reflections are observed.

As I mentioned earlier, it may be modified for use on other impedances by scaling $R_{12\&13}$. In practice, this has not been found necessary for use on 75Ω systems. ■

Reference

1. David Huddart, Cable Fault locater, Electronics World March 2001.

Applications for super-regeneration

Complementing last month's article on how super-regenerative receivers work, Eddie Insam now discusses how you can apply the technique, and presents some practical examples.

At the end of last month's article, I mentioned that many tricks have been used to improve detector performance and that the general aim is to keep loop gain as small as possible at the onset of oscillations.

Most well known, standard oscillator configurations can be adapted to provide self quenching. **Figure 1** shows a simple circuit with two transistors back to back. Feedback is provided by connecting the collectors directly to each other's bases, ensuring a low amplitude limited signal. This results in low power consumption and low radiation.

Designing a receiver

If you want to develop your own circuit, start with a standard oscillator configuration. You can find many examples in the literature mentioned at the end of this article. Choose a circuit where you can understand the purpose of each of the components. This is not so easy with many of the circuits.

Next, you must identify how the components control loop gain. You can do this by arranging the oscillator to be switched on and off from a square wave source: think of this as external quenching.

While switching is taking place, watch the rise and decay of the self-oscillations on an oscilloscope as you adjust components or bias values. The slower the rate of rise, the lower the loop gain, and the better the resulting receiver. Do not worry about self quenching until you have a reliable and efficient externally quenched design.

Feel free to use CAD programs to emulate the operation, but be aware that the step time of the emulation must be at the radio frequency. Some CAD programs cannot handle slow events (quenching) riding on top of fast ones (RF oscillations).

Figure 2 shows an interesting variation. A CMOS 4069 inverter is used as a gated oscillator with a ceramic resonator. This can be used in a simple radio control receiver or MSF time code receiver.

The external quenching action is provided by a microprocessor – the same one that may be used for processing the signal. The microprocessor starts the oscillator, and by sensing its Schmitt trigger input, measures the time period at which the oscillations have reached a threshold of about 1.5 volts. Then the micro resets the oscillator, and after a suitable delay period, starts again. This circuit could also be used with a crystal but the quench frequency will be too low for other than very low speed data recovery.

Figure 3 Shows a typical receiver circuit using a SAW delay line. I have not shown any component values, as these will strongly depend on layout and parts used. A SAW delay line has a much lower Q than a SAW resonator. I have found it quite difficult (although it is possible) to modify a standard key fob type SAW transmitter to act as a super regenerator receiver. The loop

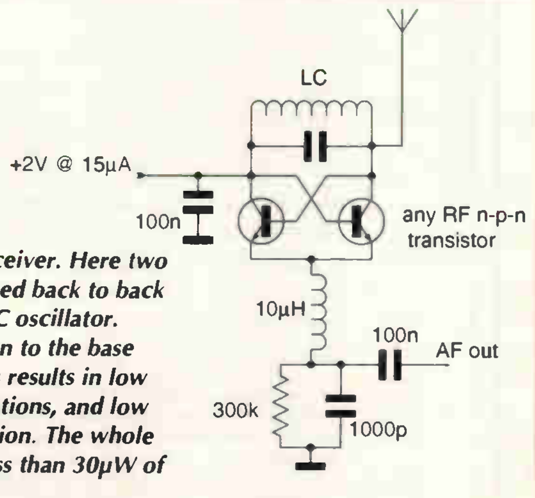


Fig. 1. Simple receiver. Here two transistors are used back to back in an inverting LC oscillator. Direct connection to the base emitter junctions results in low amplitude oscillations, and low power consumption. The whole radio requires less than 30µW of power.

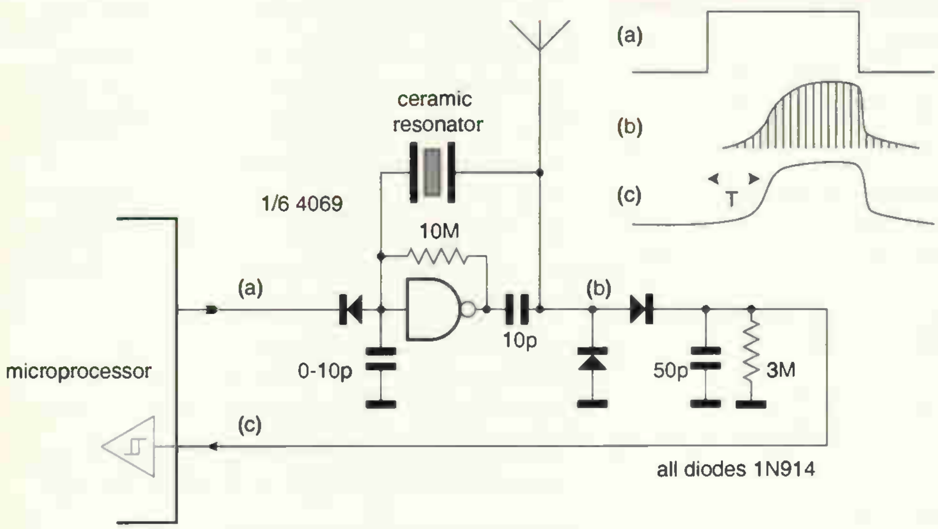


Fig. 2. Unconventional MSF receiver. A CMOS inverter can be used, together with a 60kHz ceramic resonator in an unorthodox, but rather simple time-code receiver. Here a microcontroller is used to control the quenching action by gating a CMOS inverter to enter the linear state. The gate will start oscillating after a time depending on input RF excitation at the antenna. Oscillations are rectified and fed back to the micro as pulse widths for detection. The circuit can work up to 30MHz with suitable components. A crystal could also be used in this design, but with a rather limited quench rate. See text.

gain of these devices is fairly high, and access to the SMD components is rather tricky.

Interesting applications

In theory, any active component that has negative resistance can oscillate. Therefore, there is no reason why such active component should not work in the super-regenerative mode.

Gunn diodes exhibit negative resistance characteristics, and can be used as the basis for receivers in the gigahertz range. The easiest way to get started is by commandeering an old domestic radar-intrusion detector. A popular model is the Mullard CL8960, although most modern types are very similar **Fig 4a**). This unit consists of a microwave cavity with two side by side internal sections; one with the Gunn diode, and the other with a mixer diode used for detecting the combined Doppler signal.

The cavities are designed to resonate at about 10.69GHz. By operating the Gunn diode in the negative resistance region, continuous wave oscillations are generated Fig **4b)**.

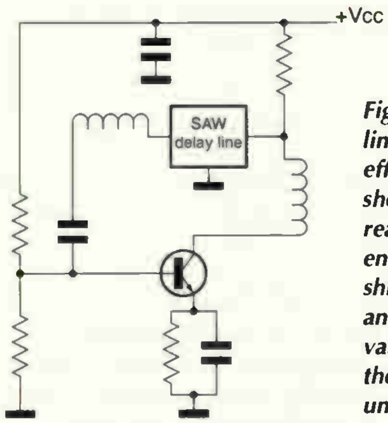


Fig. 3. A SAW delay line can be used to effect in the circuit shown. The various reactive components ensure a 180° phase shift between input and output. No part values are given, as these depend on actual unit used and layout.

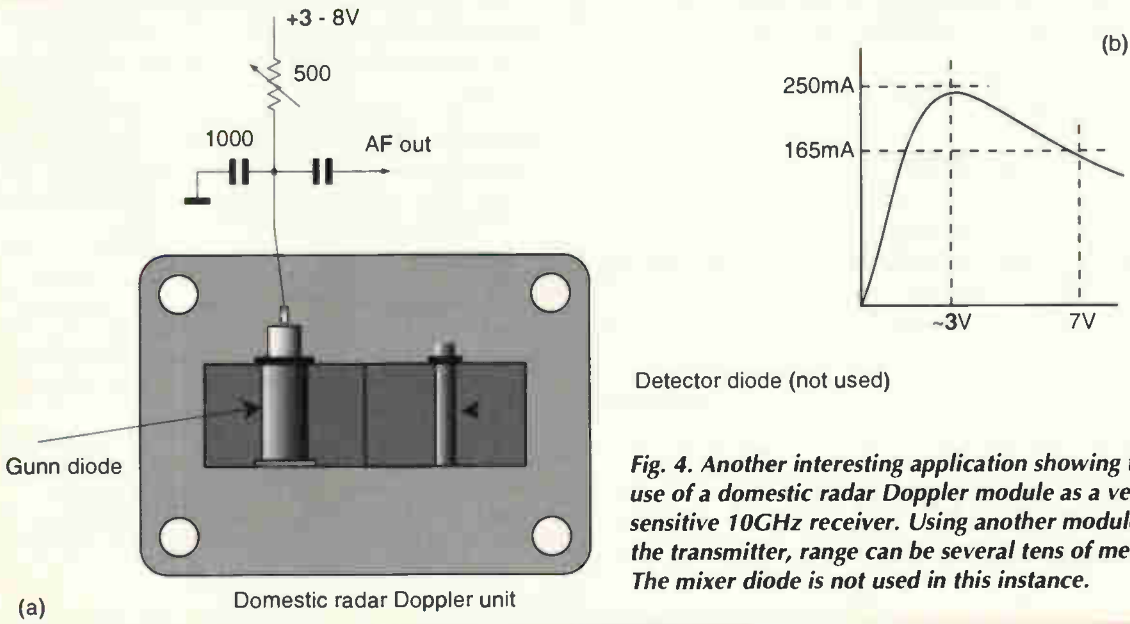


Fig. 4. Another interesting application showing the use of a domestic radar Doppler module as a very sensitive 10GHz receiver. Using another module as the transmitter, range can be several tens of metres. The mixer diode is not used in this instance.

Further reading

Most of the original work on super regenerative receivers was done in the early forties and during WW2. To my knowledge, there has been amazingly little published in terms of in depth coverage since then. The most interesting articles are:

Frink, F., 'The Basic Principles of Super-Regenerative Reception', *Proceedings of the IRE*, Vol. 26, No 1, January 1938.

Bradley W.E., 'Super-regenerative Detection Theory', *Electronics*, Vol 21, September 1948.

Strafford F.R.W., 'The super-regenerative detector: an analytical and experimental investigation', *Proceedings of the IRE*, September 1948.

MacFarlane G.G, and Whitehead J.R., 'The theory of the super-regenerative receiver in the linear mode', *Journal IEE*, Vol. 95, pt III, pp. 143-157, May 1946.

Recent articles and relevant literature on oscillators and associated components:

Ian Hickman, 'Practical RF Handbook' 2nd Edition, 1997. Newnes Publications ISBN 0 7506 34472

Ian Hickman, 'Superregen or superreplacement', *Electronics World*, February 1999. A recent article on receiver design that mentions super-regenerative receivers.

Staff feature, 'Low Noise Microwave Oscillators', *Electronics World*, November 1990. A short note on the design of low noise oscillators.

Martin Eccles, 'Applying Crystals', *Electronics World*, August 1994. Useful information on the workings of crystals and associated oscillator circuits.

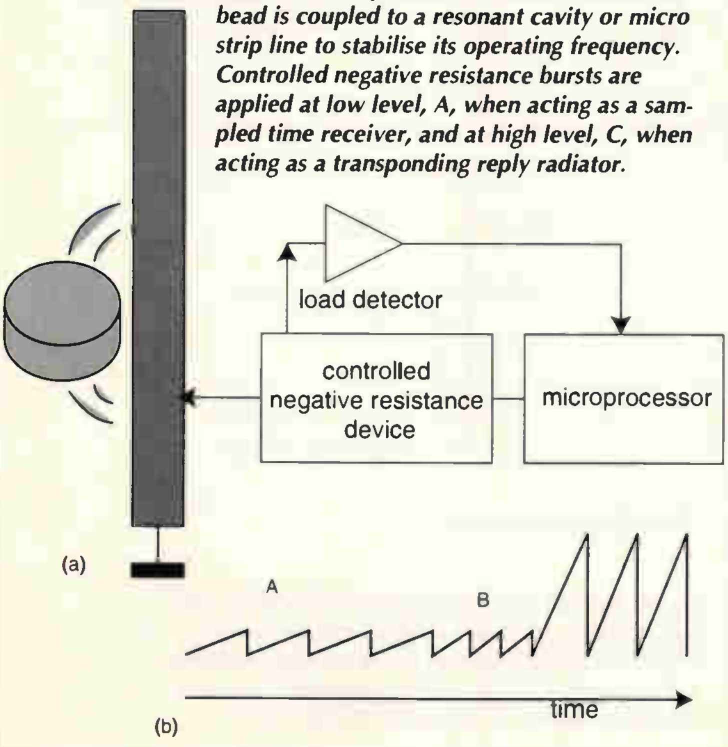


Fig. 5. A concept for a micro-miniature code device or transponder. A dielectric resonator bead is coupled to a resonant cavity or micro strip line to stabilise its operating frequency. Controlled negative resistance bursts are applied at low level, A, when acting as a sampled time receiver, and at high level, C, when acting as a transponding reply radiator.

Self quenching can be obtained by starving the supply with a series resistor and storage capacitor to ground. Simply connect the device as shown in the figure. You may need to experiment with the values as different modules may have different characteristics. You should hear a loud 'hiss' from the amplifier and loudspeaker.

You will need another Gunn unit as the transmitter. The range can be quite impressive, especially if you attach antenna horns to the flanges. You can arrange for external quenching if the unit refuses to self-quench. Just switch the supply on and off at the desired quench rate. You may need a hefty switching transistor as the Gunn device can take up to 200mA.

One thing you cannot use this circuit for is as a Doppler radar module. The receiver only samples incoming radiation at the quench rate. It also radiates pulses at the same rate, but just after the detector was active, so the two signals do not meet.

Having said that, here is a simple experiment you might like to carry out. I have not tried it by the way.

An electronic tape measure?

You will only need one Gunn device for this test. Arrange for the quench rate to be around 10MHz or more. You may need to use a very small value for the quench capacitor *C*. Alternatively, use external quenching, and arrange to measure the current into the Gunn diode, say by measuring the voltage drop across a series resistor in the supply line.

Feed the two signals into an oscilloscope. The delay between the application of power and the current blip will indicate the oscillation trigger point.

Point the unit at a wall or solid object about 15 meters away. This distance should be such that a quench RF pulse will have enough time to travel to the wall and back to coincide with the exact time when the next RF quench pulse starts.

The echoed signal will then react with the detector at the exact points when the next oscillations start, and produce some kind of output on the oscilloscope. What we have here is a quite accurate distance measuring device. Again, I have not tried this, but it would be interesting to see how sensitive it can be.

Long-range transponder

Lastly, Fig. 5a) shows a concept for a long-range miniature key fob transponder device. A resonant 1/4-wave strip line is used as both receiving and transmitting antenna.

An active device source is used to sense incoming radiation by applying short duration, controlled negative conductance loads to the strip. This active source will have to be a very accurate, programmable device, such as a combined gyrator-controller in a chip.

The sense rate can be very slow to conserve power; say once every second. When radiation is detected – from a transponder enquiry source – sense ramps are applied more often to increase the sampling rate, and to decode any incoming addressing codes. When the unit is ready to reply, a much larger negative load is placed on the strip to provide power for radiation.

The diagram shows a dielectric resonator placed close to the micro strip. Such resonators are effectively stable, high-Q RF cavities constructed from solid dielectric material, and can be used to stabilise the frequency characteristics of the strip. Such a unit may work at a range of 30-50 meters. ■

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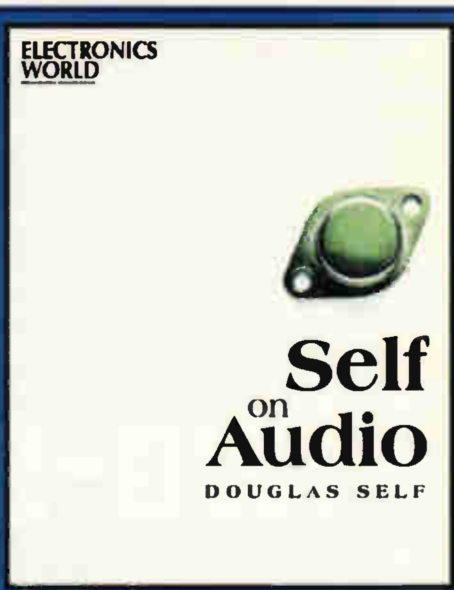

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Two-step LC tuning

Peter Fry explains his method for simplifying the tuning of LC oscillators.

If, like me, you set up an *LC* oscillator by adjusting the *L* and *C* trimmers until the calibration is about right then you might find the following method not only saves time but also gives a better understanding into the processes involved.

At the outset, my aim was purely academic. I was taking frequency measurements from an out of calibration oscillator and then using these values to calculate the exact setting for the final *C* and *L* adjustments.

The results were worth the effort though in that I now have a method that is very satisfying to use. It also proves, before final calibration, that the capacitor values will produce the desired frequency maximum to minimum range. In addition, it minimises the times you have to touch the dust iron cores, which is always a good thing.

In the industrial instrumentation world, my background, we would normally expect to find non-interactive 'zero' and 'span' calibration adjustments rather than the highly interactive *L* and *C* trimmers on a typical *LC* oscillator.

With a few simple frequency checks and a pocket calculator, it is possible to break the interaction between the *L* and *C* trimmers. The final calibration then consists of a single adjustment of the *C* trimmer to a calculated frequency and then a single set of the inductor to achieve a close calibration of the radio or oscillator.

This method does assume that the instrument or radio has been correctly designed such that the variable capacitor characteristics match the printed scale.

The method

Most *LC* oscillators can be simplified to the basic circuit as in **Fig. 1**. Here, calibration is achieved by setting C_T, the trimmer, and *L* the inductor, which is assumed to be variable. Other circuit capacitances, designated as 'stray' will always modify the actual

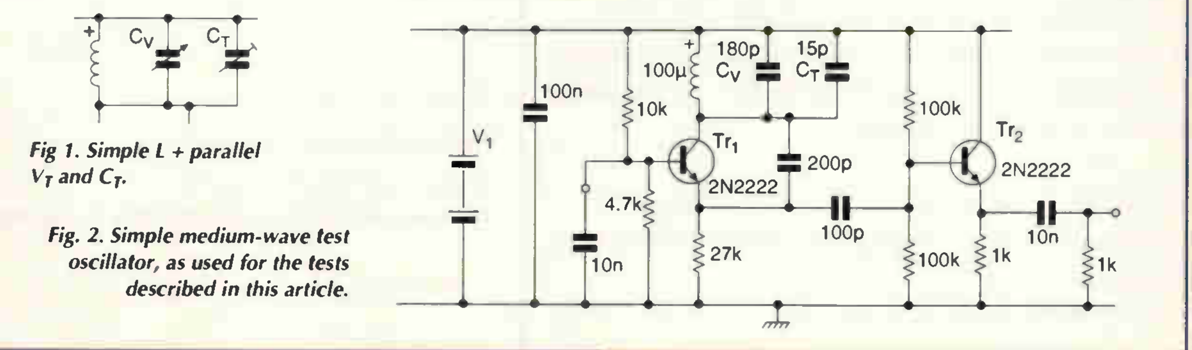


Fig 1. Simple L + parallel V_T and C_T.

Fig. 2. Simple medium-wave test oscillator, as used for the tests described in this article.

frequency downward from the theoretical values.

The frequency ratio of maximum f over minimum f is set by:

$$\sqrt{\frac{C_{V\,max} + C_T + C_{stray}}{C_{V\,min} + C_T + C_{stray}}}$$

The inductor controls the frequency with the capacitor but it plays no part in the max:min frequency ratio. This is fundamental to the calculations that follow. But first, take look at the actual circuit used in the practical tests, **Fig. 2**.

The circuit is from a simple AM signal generator that was used to check the calculations in this article. This schematic and traces were taken from a Micro Cap 5 simulation. The waveform in **Fig. 3** is close to the actual generator signals, which gives good confidence.

I have not however included the modulation on the schematic. In the commercial generator, this is applied to the base of Tr_1. This is not good practice as it modulates both the aptitude and the frequency however for 10-15% AM modulation. Considering that the generator was to be used for bench testing AM broadcast radios, then this is just about acceptable.

In order to cover 400kHz to 1600kHz, the generator had a waveband switch that brought in a second section on the variable capacitor and a second inductor. The section shown is the 925kHz to 1600kHz range. For clarity this is not shown.

Calibrating the oscillator

What needs to be done is to test the limits of the oscillator in its *uncalibrated* state and then determine if it will be possible to calibrate it without adding or subtracting extra capacitors. It is also necessary to determine a setting for C_T that will give a one off setting. Final calibration is by a single adjustment of the inductor, assuming that it can be varied in some way.

Step 1. The first step is to ensure that *all* mechanical parts of the tuning mechanism are in good order. Check that the scale pointer moves from end to end as the capacitor vanes fully mesh and un-mesh and that all shaft screws are tight. Any problems here must be solved first or the whole process will be invalidated. Be careful with any string and pulley type pointers as they can be very difficult if not impossible to re-string!

Step 2. Set up a frequency counter or calibrated receiver to measure the oscillator frequency. Counters should always be coupled via a buffer stage. Alternatively, they should be coupled as loosely as possible using a pick up coil of a few turns connected to the end of a probe or a x10 probe connected to a low impedance part of the oscillator.

Step 3. Choose two calibration points, near, but not right at the ends of the tuning scale. Depending on the quality of the oscillator there can be inaccuracies right at the extremities of the range.

Also remember that if this a a radio local oscillator then the IF frequency will need to be added or subtracted. Assuming a normal broadcast receiver that is basically functioning, this frequency can be determined by measuring at the detector stage with a strong broadcast or injected if signal peaked for max amplitude.

Step 4. Draw up or copy the table as **Table 1**.

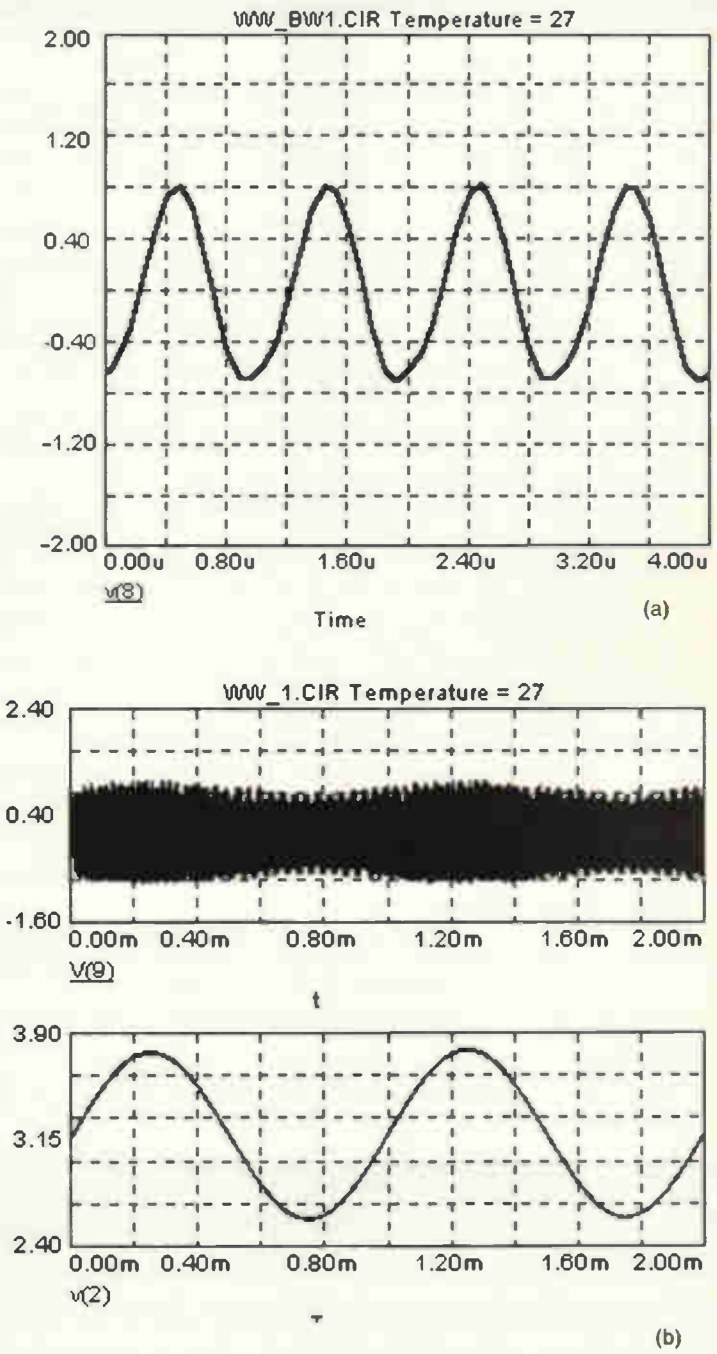


Fig 3. Output from the oscillator, a) and modulated signal, b). Y scales are volts X scales microseconds in a) and milliseconds in b).

Table 1. Use this table as an aid to calibrating your oscillator. See Table 2 for clarification.

	Chosen dial setting	±IF if applicable	Frequency at C_{Tmin}	Frequency at C_{Tmax}
F_{max}				
F_{min}				
Ratio				

Table 2. Setting-up table including values from a simple test oscillator.

	Chosen dial setting	±IF if applicable	Frequency at C_{Tmin}	Frequency at C_{Tmax}
F_{max}	1.400MHz		1.567MHz	1.3771MHz (FB)
F_{min}	0.950MHz		1.0274MHz	0.9674MHz
Ratio	1.4737 (Z)		1.525 (X)	1.4235 (Y)

Next set the dial to your upper chosen setting and with the trimmer capacitor set to minimum, i.e. if it's a compression type, slacken the compression screw or if small vane type, unmesh it. Measure the frequency and enter the value in the table at the maximum dial C_{Tmin} location (1.567 in the example).

Leaving the trimmer alone, set the dial to the chosen low point and enter the frequency into the minimum-dial C_{Tmin} location (1.0274 in the example).

Leaving the dial at the chosen low point, adjust the trimmer for maximum capacity. If it is a compression type nip the screw up, but not too tightly. If it's a vane type fully mesh it. Now measure the frequency and enter the value in the chosen low point C_{Tmax} position.

Set the main dial to the high chosen point and enter the value into the table in the remaining high-dial point and C_{Tmax} location.

Now divide each column highest frequency by the lowest to reveal the actual frequency ratios.

This bit is important. The actual ratio of minimum to maximum tuning range is set by the square root of the capacitor minimum to maximum values regardless of actual frequency. If you are designing the circuit yourself, this is of concern and is dealt with in basic *LC* theory.

In this example though, we are measuring frequency ratios. As a result, we do not need to be concerned with the mathematics of the *LC* oscillator.

If the ratio under the chosen dial settings is *not* within the range of ratios in the Max and Min C_{Tmin} and C_{Tmin}, columns, then it will *not* be possible to calibrate the oscillator without some change to the pad capacitors.

You may be able to squeeze a bit more out of the adjustment if you pull up the trimmer a bit harder and repeat the C_{Tmax} calculations but take care!

The values shown in Table 2 are those from my simple bench test oscillator. All that now remains is to set the dial to the high chosen value and to calculate the spot frequency that will be set by C_T. This will *not* be the dial setting frequency but will be a frequency that gives the precise frequency ratio, value *Z* in the table.

If the figures you entered into the table were accurate, you may not need to touch C_T again in this calibration. Referring to the table for the variable identifiers calculate the spot frequency using:

$$f_{spot} = \frac{z-y}{x-y} \times (f_A - f_B) + f_B$$

For my example this gives

$$f_{spot} = \frac{1.4737 - 1.4235}{1.525 - 1.4235} \times (1.567 - 1.377) + 1.377$$
$$= 1.471\text{MHz}$$

Using my example, set the dial to 1.400 and use the C_T trimmer to set the oscillator to 1.471MHz.

All that now remains is to set the inductor to give 1.400MHz precisely. This setting could equally be done at any point on the scale as it brings the whole scale calibration in line.

Providing that the dial scale matches the variable capacitor characteristics and the calculations were done accurately, then you should find the scale setting to be reasonably accurate and no further trimming may be required.

It is quite easy to set up a simple spread sheet to further simplify the procedure. Doing it this way also removes any chance for calculation errors. ■

Reducing flyback stand-by power

Jonathan Adams of International Rectifier looks at how to wind down the stand-by losses of flyback power supply circuits using the IRIS40 range of integrated switchers.

There is an increasing amount of emphasis on the stand-by or no-load consumption of electrical equipment. This is being driven by various environmental agencies, which are focussing there efforts on reducing the losses and power wastage of electrical equipment.

These efforts include programmes and initiatives that define criteria for appliances and equipment. Examples are the Energystar program in the USA and the Blue Angel Program in Germany. These are both being adopted worldwide.

Meeting the criteria for these programmes allows manufacturers to place marking like the Blue Angel and the Energystar Logo on their equipment, signifying the environmental saving measures the devices incorporate.

These programmes and initiatives are becoming universally adopted. Soon, they'll apply to all electrical equipment. As a result of this it is important the Power supplies for these pieces of equipment are energy efficient and consume very low power in the Standby or off states.

This design tip shows you how to implement a circuit to reduce the no-load/stand-by losses of a flyback

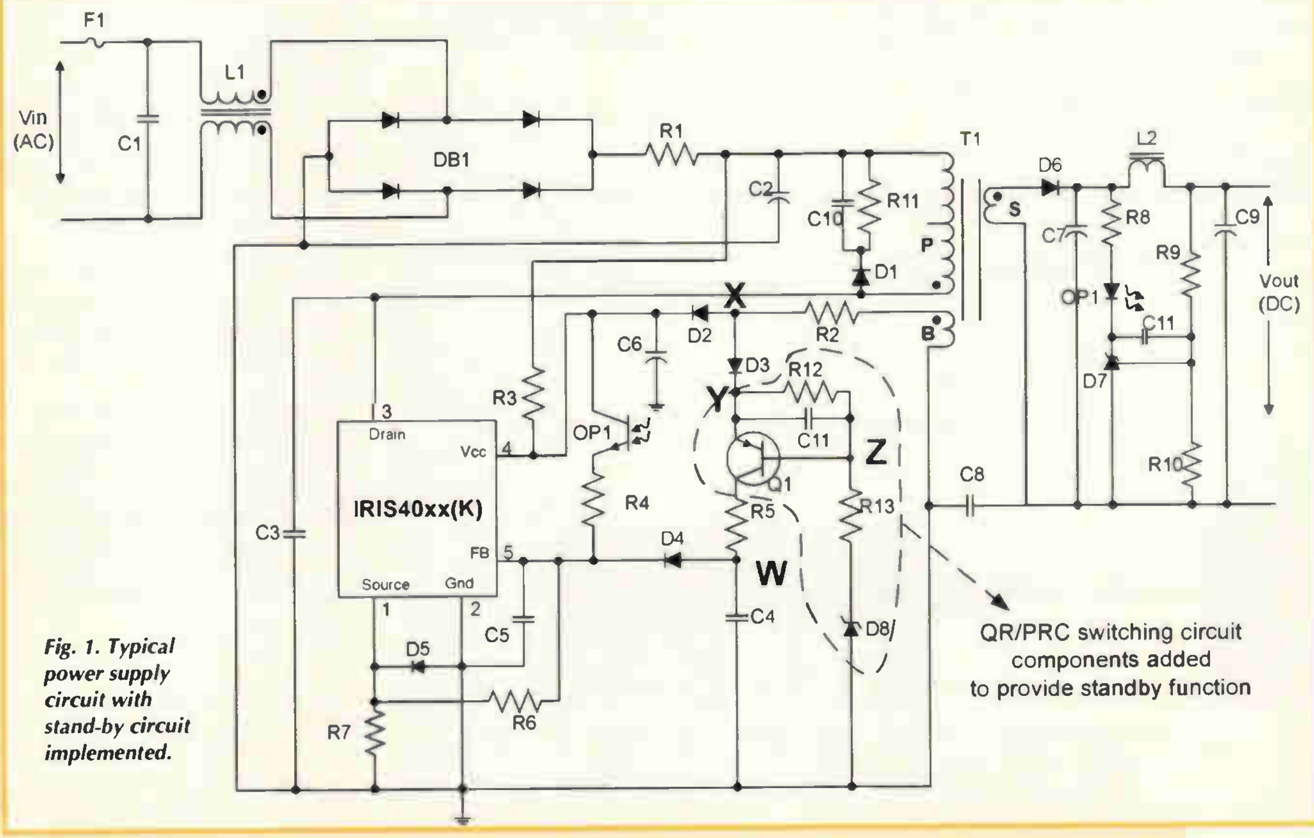


Fig. 1. Typical power supply circuit with stand-by circuit implemented.

power supply using IRIS40xx series integrated switchers. It involves using a circuit to change the mode of operation of the IRIS device depending on the load. quasi-resonant mode for higher loads. and pulse-ratio control. or PRC. mode for light load and no-load conditions.

Changing to PRC for light or no load conditions would set the circuit to operate in a frequency range of 15-20kHz. This would drop the no-load losses from a typical 2.5W with a 230V AC input to about 0.8W. Quasi-resonant mode at no-load though would cause the circuit to operate around 300-350kHz. which leads to higher switching losses.

Stand-by circuit operation

The circuit on the next page in **Fig. 1** shows a typical single output flyback power supply using the IRIS40xx integrated switcher. It is different from the circuits in the other application notes in that circuitry has been added to facilitate lower-power operation at no-load and standby conditions.

This additional circuitry consists of $Q_1/R_{12}/R_{13}/C_{11}/D_8$. These five components form a switching circuit to either pass or disable the feedback of the quasi-resonant signal from the bias winding B to the feedback pin of the IRIS40xx.

Operation of the circuit in stand-by mode is fairly simple and will be explained here. Components $D_3/R_5/C_4/D_4$ form the delay circuit which feeds back the quasi resonant information from the bias winding to the feedback pin. This allows the IRIS40xx to detect when all the energy has been transferred from the primary to the secondary. and detect when the drain voltage is at its lowest point for softer switching.

Transistor Tr_1 is placed in the path to act as a switch to enable or disable the feedback. This effectively changes the mode of operation of the IRIS40xx from quasi-resonant mode – when the feedback is enabled – to the lower-frequency pulse-ratio control mode – when the feedback is disabled.

The circuit monitors the bias winding voltage to determine when to switch between modes. At normal load. the bias winding voltage would be higher. Also. the mode-switching circuit would have its level set so that under these conditions Q_1 is on and the quasi-resonant feedback/delay circuit is enabled. When the circuit drops to a no load or light load condition the bias winding voltage will drop below the set level and disable the feedback/delay circuit.

Components $R_{12}/R_{13}/D_8$ form a voltage divider to set the switching level of the standby-mode switching circuit. The switching level is determined by the voltage across R_{13} and D_8.

When the bias winding voltage is high enough current will pass through $D_3/R_{12}/R_{13}$ and D_8. This causes a voltage drop across R_{12}, which in turn is seen across the emitter-base junction of the p-n-p transistor. Tr_1. As this voltage starts to rise above 0.6V. current is injected into the emitter-base junction of Tr_1 and it will turn on.

If the voltage across R_{12} – and in turn the emitter-base of Q_1 – is less than 0.6V due to a lower voltage at the bias winding. less or no current flows through R_{12}. As a result. Q_1's collector-base junction is not sufficiently forward biased. so Q_1 cannot turn on and the feedback/delay signal is disabled.

Design procedure

I'll present an example to show how you can design and implement this part of the circuit. I'll assume that the rest of the circuit has already been designed using the other application notes.

First. take an example where the normal designed V_{cc} is 17V. If the rectifier for the bias winding is something like a 1N4148. then the bias winding voltage would have been designed to be 18V. So under normal load conditions there is 18V at point X. during the energy transfer cycle.

Now it's time to select the voltage at point X to change the mode of operation. This will obviously be below 18V. Consequently. select a voltage that's a few volts below the expected bias voltage to ensure it will switch at light load. but can also start up into quasi-resonant mode when there is a full load condition. Let's select 15V. The bias winding voltage drops at light or no load. due to the higher feedback current from the output control circuit.

If there's 15V at point X. then the voltage at the emitter of Q_1 – point Y – will be 1V below this due to the forward voltage of D_3. So at Y. there's 14V.

Transistor Tr_1 will turn on at the point when there is 0.6V across the emitter/base junction. Therefore set R_{12} to 620Ω. Now. Q_1 will turn on when there is 968μA through R_{12}. So if you want Q_1 to switch on when point Y is at 14V. you can set a zener voltage for D_8 and calculate R_{13} from:

$$R_{13} = \frac{V_y - (V_{D8} + 0.6)}{I}$$

Here. V_y is 14V in this example. and I is 968μA. If you make D_8 an 11V Zener diode. then R_{13} will be 2.4k. The circuit shown will be able to change modes to the low power

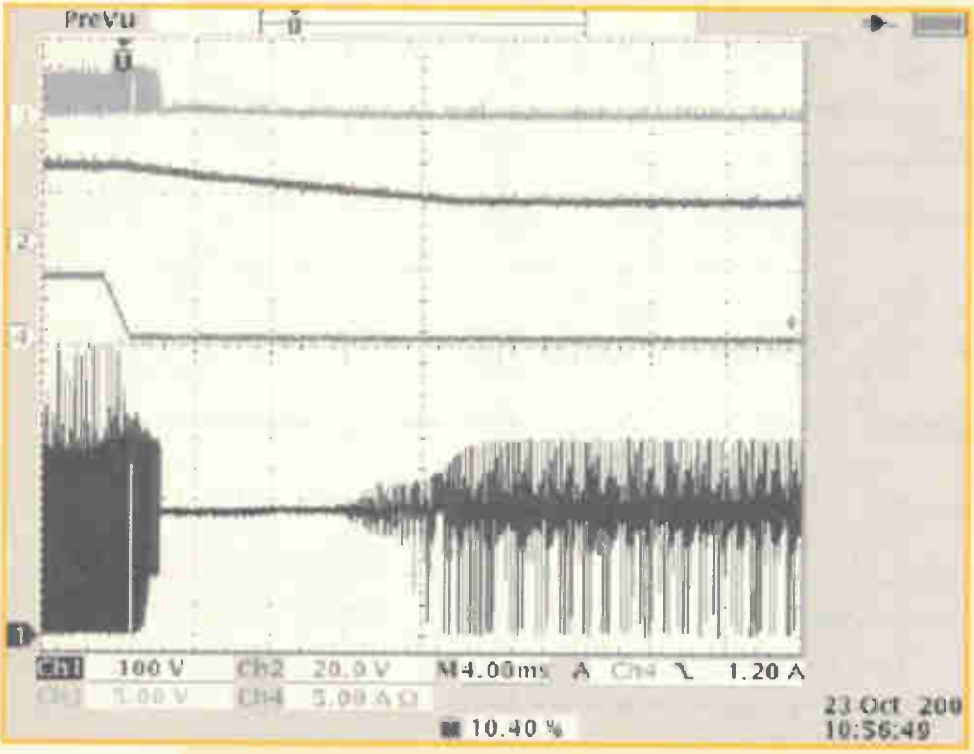


Fig. 2. Waveforms of drain (CH1)/Vcc(CH 2)/FB (CH3) and load current (CH4) as the circuit changes from quasi-resonant mode to pulse-ratio control mode.

standby with a load change from any load above 1A to a load of 0.05A or less.

Circuit waveforms

In **Fig.** 2, the waveform plots show what happens as the circuit changes from operating in the quasi-resonant mode to pulse-ratio control mode as a result of a load change.

When the load current changes from full load to no-load, as shown on CH4, the feedback level increases as the output voltage increases to try and move the energy stored. Eventually, under this condition, the feedback level increases to a point where the FET stops switching as shown by the flat part of the drain waveform on CH1. At the same time the FB pin (CH3) no longer sees the quasi-resonant information. Also, the V_{cc} voltage, CH2, will fall as the bias winding is now not supplying energy.

After about 5ms, the circuit feedback level stabilises. The FET starts to switch again, but this time it is operating in the pulse-ratio control mode. This results in a reduced V_{cc}. Also, there is no quasi-resonant signal at the FB pin, shown by the reduced voltage on CH3.

During operation under these conditions, there is still a high feedback level. This is due to the no-load condition at the output. As a result, the circuit only needs to transfer a very small amount of energy from the primary to the bias and output to keep the circuit in equilibrium until there is another load change.

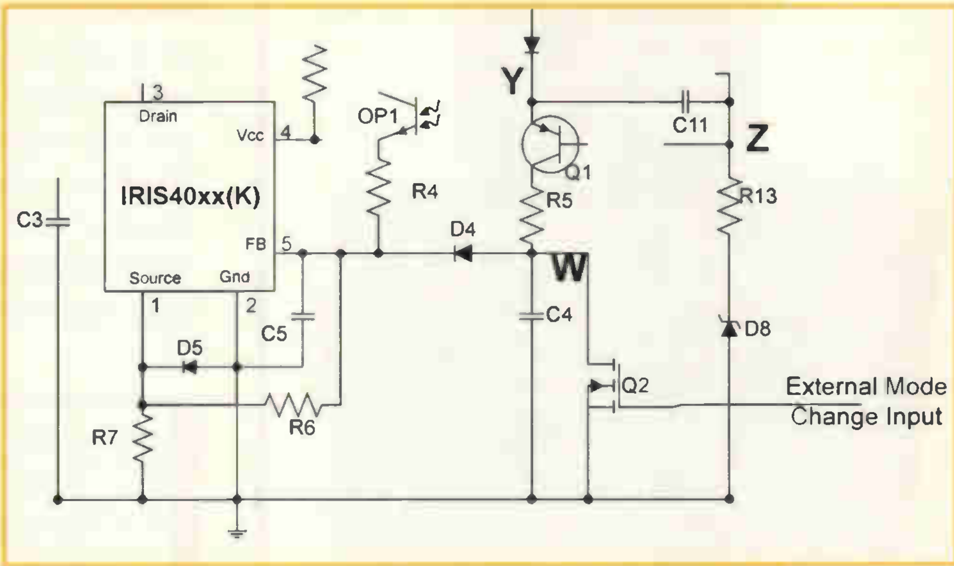


Fig. 3. Part of an IRIS power supply circuit showing Q_2 added for mode-override circuit.

Optional external override circuit

Figure 3 shows how an external override signal can be used to make the circuit go into the pulse-ratio control mode. FET Q_2 could be a logic-level FET, which would allow a driving signal from a microcontroller or other source.

The implementation of this circuit is very simple. Transistor Q_2 is usually off, which allows the circuit to operate as normal where the mode of operation is determined by the load current. When Q_2 is turned on. point W is tied to ground which shorts out the quasi-resonant signal and prevents it from reaching the FB pin. Therefore the circuit will default to operating in the PRC mode. ■

Gang your own pots

A very low-cost method for ganging multiple potentiometers.

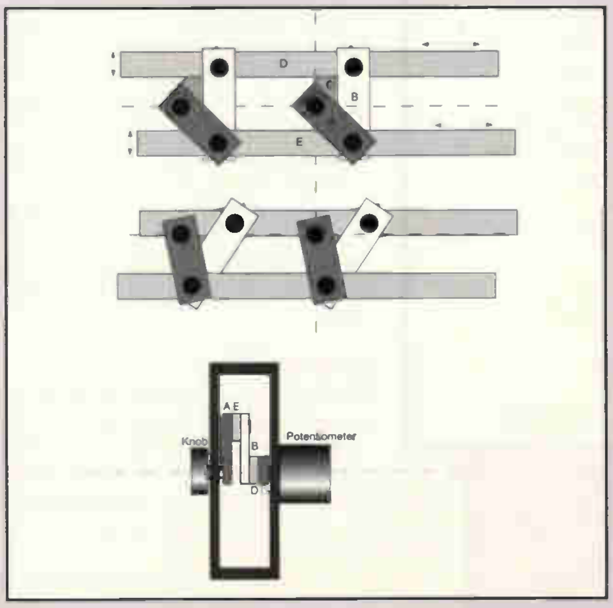
It is possible to gang potentiometers using just hardboard, a few strips of wood and some lengths of spindle. John Farbrother kindly sent a contraption to *Electronics World* to illustrate the point.

Strips A and C are identical. They're about 5mm thick on the prototype. Strip B is similar, but a little longer. Strips A and C are linkage arms from hardboard.

The drawning only shows the mechanism for two pots. Strip A is fixed to the potentiometer shaft at one end and to one of the linkage strip at the other. The potentiometer is fixed. Similarly, the knob fixes to one end of strip C, the other end of which connects to the other linkage strip.

Although the knob and potentiometer aren't directly linked, as you can see from the side view, the pot turns when the knob is turned due to the action of strip B and the linkage strips. The linkage strips cause any other A, B, C combinations connected to it to turn by the same amount.

Further pots can be added along the linkage strip. We couldn't detect any play in the prototype triple-ganged version by the way.



Want to win it? Simply send us the answer to the question, "How many WorldSpace satellites are operational?" on a postcard together with your name and address and your entry will go into the hat. Address the postcard to Electronics World, Cumulus Business Media, 9-13 Ewell Road, Cheam, Surrey SM3 8BZ. Please read the competition rules first though.

This competition is sponsored by Nevada Communications, UK distributor of the Worldspace radio. You can telephone Nevada 02392 313090 or visit www.worldspaceradios.co.uk for more information on the radio. Nevada Communications, Unit 1, Fitzherbert Spur, Farlington, Portsmouth PO6 1TT.

Win an Hitachi WorldSpace radio worth £149

What is a WorldSpace receiver?
Listen to over 40 channels of crystal clear, fade-free digital audio programming direct from geostationary satellites around the world with the Hitachi KH-WS1 WorldSpace Digital Receiver. In addition to the satellite WorldSpace programming, it receives regular terrestrial AM, FM and SW broadcasts.

Personalising available programs
The Hitachi KH-WS1 WorldSpace receiver displays a scrollable menu of available channels. You can then customise the types of channels the receiver shows by preselecting preferred language and program types.

For example, an Arabic speaking user who wants to receive a wide variety of global news can preset the receiver to display only the WorldSpace array of Arabic language news channels.

Fade-free WorldSpace programs include:
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The WorldSpace satellites
When complete the WorldSpace network will consist of three geostationary satellites. Afristar™ was successfully launched in late 1998 followed by Asiastar™ in early 2000. Ameristar™ is scheduled for launch in 2001.

WorldSpace satellites are located more than 35 000 kilometers above the equator. Using powerful spot beams, each of which can support more than 50 services, the satellites transmit to three overlapping coverage areas approximately 14 million square kilometers each!

Earth Stations
WorldSpace satellites use on-board processing to enable program reception from many stations. Content providers on the WorldSpace system can uplink their programs via the traditional hub method, sending broadcast signals to a central location for processing before transmitting them to the transparent part of the satellite.

A second mode enables use of a smaller, more mobile feeder link uplink stations. Onboard processing technology converts these multiple signals at the satellite, combining them into a single downlink signal before transmitting them back to earth.

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  MW: 522 - 1620kHz (9/10kHz)
  SW1: 2.3 - 7.3MHz
  SW2: 9.5 - 26.1MHz
- Memory: 10 WorldSpace
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  Last station memory
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- Stereo line out connectors for integration with your stereo or home theatre system
- Built-in easy to aim antenna
- Decryption and narrowcast capability
- Program selection by language and category
- Clock display/timer function
- 1-line 8 character LC display
- Port for easy attachment to the WorldSpace PC card to enjoy multimedia services – not yet available in Europe
- Easy to set up and operate
- 246.5 x 162.5 x 93mm (9.7 x 6.4 x 3.6in) including antenna and handle
- Weighs 1.5kg (4.1lbs) without batteries

Competition rules
No purchase is necessary. Strictly one entry only per household. Competition closing date 12 July 2002. No entries will be accepted after that date. The draw will be made within the next working week following 12 July and the winner announced as soon as possible thereafter. The prize is not negotiable.No correspondence will be entered into regarding this competition. No employee of Cumulus Business Media or Nevada of Hitachi may enter the competition.

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Letters to the editor

Letters to "Electronics World" Cumulus Business Media, Anne Boleyn House, 9-13 Ewell Road, Cheam Road, Surrey SM3 8BZ
e-mail j.lowe@cumulusmedia.co.uk using subject heading 'Letters'.

Doctor, Doctor!

I was heartened at the start of Lawrence Jones' editorial† giving support to female graduate engineers. However the piece soon deteriorates, bemoaning the lot of postgraduate engineers generally and how poorly he feels society perceives their worth.

Though I have sympathy for his view, the engineering profession is ill served by castigating GPs with fashionable cheap shots and spiteful invective, with among other ludicrous implications, the well rehearsed arguments about the title doctor.

Crossing the Atlantic aboard a 747, I am certain that when the steward requests a doctor that Dr Jones will not be arguing issues of title ownership and to everyone's relief, including his own, will remain firmly in his seat.

Brian Judd
Paediatric Nephrologist
St Helens
Merseyside

† Editorial, *Electronics World* 108;1791 March 2001

Referring to Lawrence Jones' editorial, I have been an electronics hobbyist for nearly 30 years but I work as a GP. Having spent many years studying and working to become a GP, I generally appreciate the work that the author must have done to obtain his PhD but I was taken aback by the disrespect he showed to my profession.

As a scientist, I would have thought that he would have researched the validity of the headline figures released by the government before using them to denigrate the medical profession.

Firstly, we would not have the current recruitment and retention crisis in medicine if we did indeed earn an average of £84.5k. Unfortunately, the government spin doctors forgot to mention that £20-25k of this is for business expenses such as staff, premises costs, equipment costs etc.

Also the real pay rise will be more like 4% in real terms, not really compensating for more than ten years of significantly below inflation pay rises. The 'bully boy' tactics of the BMA are more an act of desperation to move the government to rid us of Dickensian working conditions the likes of which cannot be fully appreciated by anyone outside medicine.

Finally, a cursory look at the definition of 'doctor' clearly gives both medicine and PhD equal validity to use the term and suggests the author may have a 'chip on his shoulder'.

The results of the reality of the above, which can be verified by a cursory glance at any of the medical press – '*Medeconomics*' for example – are interesting and ironic. The only people interested in becoming GPs are women, who want to work part-time as a second income to their partners working outside the public sector.

Dr R A Wilkins MBCHB MRCGP
Via e-mail

Superhet communication...

I have a minor correction to make to an otherwise excellent article: 'The Invention of the Superhet', by Ian Poole, in the March 2002 issue.

R. A. Fessenden, although working in America at the time, was Canadian born, and should probably be referred to as a 'Canadian engineer' rather than an 'American engineer'.

American writers tend to co-opt Alexander Graham Bell in the same way.

http://www.rcc.ryerson.ca/ccf/personal/hof/fessen_r.html

Michael Drolet
National Film Board of Canada
Montreal
Canada

Misleading?

I read Mr Chung's comment on my article about train safety. I am a bit disappointed that he thinks that I have unintentionally misled your readers by what I wrote.

I obtained much of the information from American sources on the internet. Nearly all the ones I used were official web sites dealing with accident reports produced by the railway safety authorities in several American states.

One or two sites I looked at were university sites. A quick search with Yahoo would give the impression that it is only the Americans who have railway accidents. I did not see any comparable reports about British railway accidents when I did my research for the article.

As American passenger trains are not so different from British trains, I used American data. I stated that I had used American data in the article so there can be nothing misleading about that.

Wilf James
Via e-mail

RMS converter chip

In his fine series of articles concerning RF probes, which I am trying to duplicate, Mr Bateman used the AD8361 RF 'True-power' RMS converter. I tried to locate this chip in the catalogues of major suppliers – RS and Farnell – but it is not listed.

Thanos Baxevanis
Athens
Greece

Farnell has kindly offered to stock this chip. The sales desk number is 0113 263 6311, fax 0113 263 3404, web www.farnell.co.uk. Ed.

Improved Outlook

Referring to Letters in the April issue, Mr Wiltshire does not say what version of Outlook he is using. My version (2000) does have an audible waring of an upcoming meeting. I would suggest that upgrading would be his quickest option.

Alternatively, Outlook does have an 'OLE' interface. This is a programmer's interface visible from Visual Basic, for instance.

It might be possible to detect appointment events from this interface, and then use VB to play a .WAV file or send a USB/RS232 message.

Andrew Malcolm CEng MIEE
Synchronous Designs Ltd
Camberley Surrey

Motorcycle gear display

£100 winner

Many motorcycles have six gears – some models even have reverse – but they rarely, if ever, have a gear-position displays.

At first, making a display seems to be simple matter; on closer inspection, the problem turns out to be quite complicated for motorcycles that use mechanical levers. Using electronics and microprocessor logic though, this problem is easy to solve.

The problem and the sensors needed to solve it

My friend bought an old motorcycle with six gears. He wanted to be able to know which gear is selected via a seven segment display.

A motorcycle's gearbox is controlled using a rocker-type foot pedal. Pushing it down from its original neutral position selects first gear; pulling it up or pushing other end down toggles the gear box first back into neutral, then to second gear, then third, fourth, fifth and sixth position.

For position sensors, we decided to use three micro switches: one for neutral, one for up and one for down. The gear lever operates these switches according to the sequence described above.

Microprocessor and display

A 25mm-high seven segment display is more than adequate for most motorcyclists in daylight and at night.

A Kingsbright SC10-21 display has seven segments and a decimal-point LED with its own anode. This display has common-anode connection. Its common-cathode counterpart requires a small modification for microprocessor program. The modification is explained later.

A flash PIC16F84A with 13 i/o pins is enough for eight display outputs and three micro switch inputs. Port B connects to the display the through a resistor network. Port A is used for micro switch inputs.

The processor and display use a 5V power supply. A standard 7805 regulator drops 12V battery input to 5V. Power supply wires should go through HF filters to the ignition switch and ground.

PIC microcontroller program

Although the logic might seem simple, the real-world interface adds complications. Switch bounces, possible overlapping timing and a special conditions like starting or stopping while the bike is in gear all have to be taken care of.

A program is a state machine in which the only way to get to the next state is to fulfil the right switch combination with the right amount of debouncing time.

After reset, the program goes to the zero state and shows a zero digit at the display. Between each state there must be a 50ms debounce time.

Each switch has also a hardware debounce timer involving an *RC* circuit. This precaution prevents problems from interference caused by the ignition system.

A seven-segment display is decoded directly by segment table that contains the values to turn the right combination of leds on. A CCS PIC-C compiler is used for the software. The software size is about 300 compiled words, List 1.

Because the program doesn't not use any interrupts, timers or any special PIC peripheral, it is easy to implement the code with any microcontroller, including Intel's 80C51 compatible processor.

Using an 80C51 would require a driver though in order to produce a bright display, so the PIC is right selection for this application.

An even better solution might be the PIC16F628. It has internal *RC*-oscillator, which removes one component. This part is not yet so readily available as the 'F84 or 'F84A though.

Putting the idea together

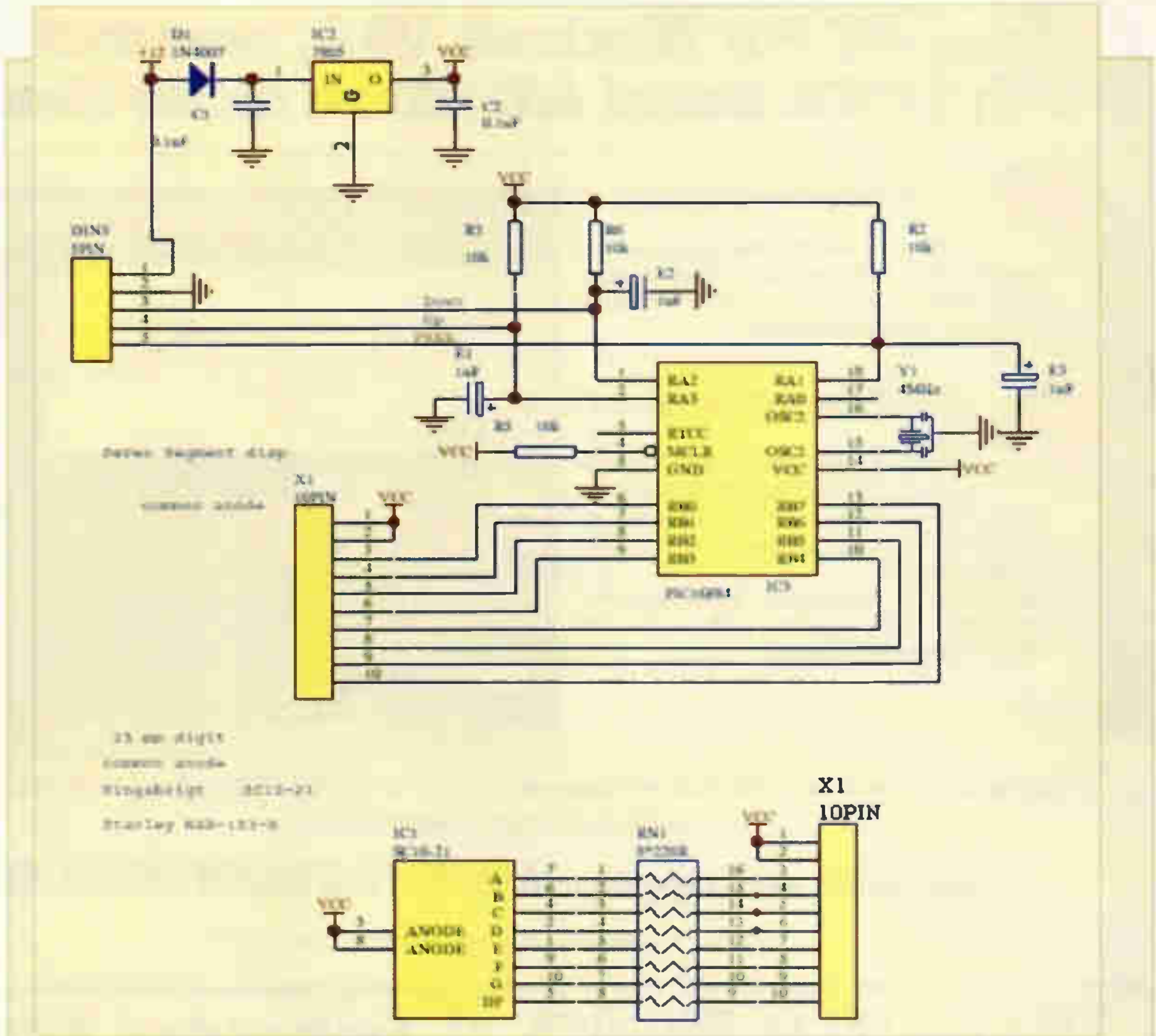
It is possible to make the whole unit on one double-sided circuit board. Because this was a spare-

List 1. A seven-segment display table with some test combinations together with a code snippet for using the table based on a PIC 'c' compiler.

```
const byte seg[25]={0x3f,6, 0x5b,0x5b, 0x4f,0x66,0x6D ,0x7c};
====== a code snippet for using a table
#include <16F84A.h>          // select the right PIC
#use delay(clock=4000000, restart_wdt) // select right oscillator
#fuses HS,NOPROTECT,WDT,PUT          // use watchdog
#byte PORTA = 5              // define IO-port address
#byte PORTB = 6
#bit  UP = PORTA.3           // and  IO-bits
#bit  DOWN = PORTA.2
#bit  FREE = PORTA.1
char dat,state,pre_state;        // declare some variables
void set_display( void) {
 dat = seg[state];// fetch a display bits according state table
 PORTB = ~dat;  // Common anode display requires a inverted (~) bits,
                // common cathode display only PORTB = dat;
}
==== a pseudo program for first state ===
void main (void) {
 set_tris_a (0x3F);   // set data direction register for PORTA, all in
 set_tris_b (0x00);   // set data direction register for PORTB, all out

 test_display_digits( ); // go through each digit for testing
 state=0;                    // set the initial state
while (1) {                          // forever loop
  restart_wdt();                             // keep watchdog alive
  switch ( state) {
         case 0: if( !DOWN )     // if DOWN switch on and state is 0
                     state =1;    // goto to mode 1 i.e.  gear one
                     pre_state =0;         // previous state for direction ops
           break;
         state 1:
      ...
         state 6:                            // each state has some combination
                                             // of pre_state and inputs
   }                                         // end switch()
wait_debounce_delay();    // display the dot led during debounce wait time
set_display();                    // set state to decoded display
 }  // end while ()
}  // end main
==================== end of snippet ======
```

Complete circuit for the motorcycle gear-selection indicator.



time project for a friend though, a two-sided circuit board would have been too expensive. Besides, back-to-back connected single-sided circuit boards are easily made without too many compromises.

Thanks to the microcontroller, the number of parts needed is so low that hand wiring can be carried out in half a hour or so. The boards can be connected together by 0.1in pins, but I used just a flat cable to make testing easier.

The switches and power supply are connected by a five-pin audio DIN-connector. Such a connector is easily obtained from the keyboard connector of an old PC mother board. Making the unit removable ensures that it won't get stolen.

The led display could be smaller, but you would need to modify the circuit board according to the display wiring. The unit fits into almost any small case.

Use twisted wires for switches and power supply. Turn power supply wires around a 12mm ferrite ring to reduce possible interference from the ignition circuitry.

Testing

Before you attach a new gear display to your motorcycle, test the display logic with three push button switches and a 12V power supply.

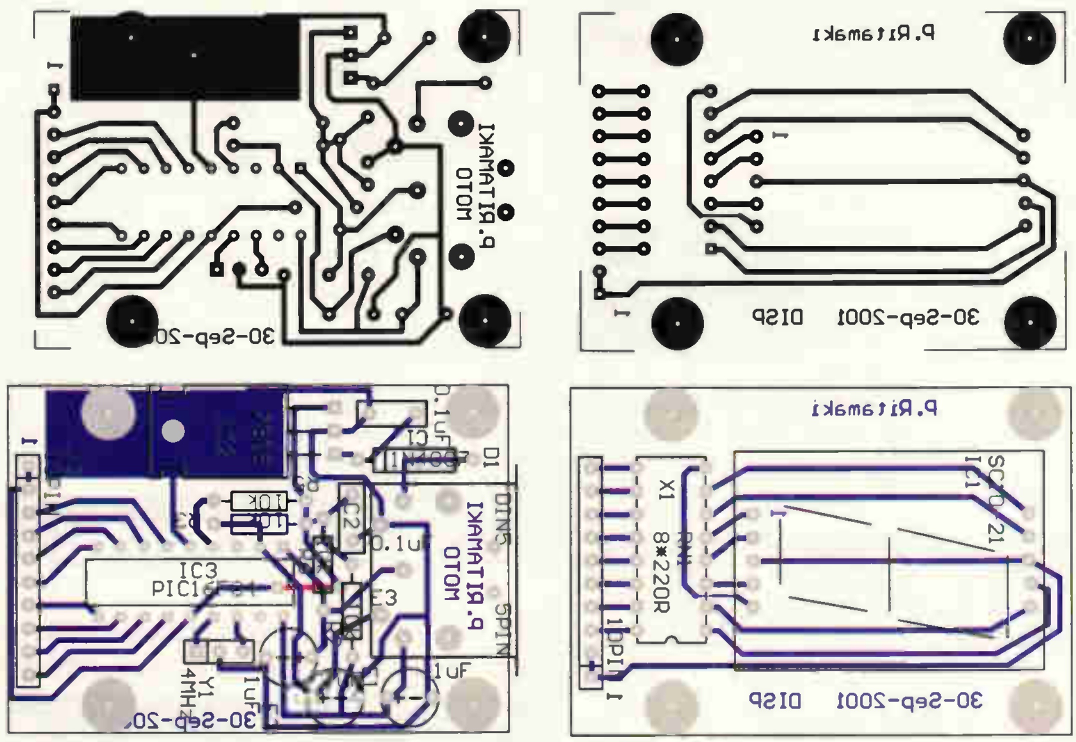
First, make sure that all digits are displayed in sequence. A zero digit represents neutral.

Push the down button and digit one comes on. Push the free button and then the up button and digit two should be displayed. Push the up again until the display shows digit six.

Now push the down button until digit two is shown. Push the free

Hex code for the PIC16F84A controller

```
:1000000000308A00A42800000A108A100A11820712
:100010003F34063406345B345B344F3466346D341D
:100020007C340134023403340434053406340734 98
:10003000FF34FF34FF34FF340034003400340034 24
:10004000003413308400000803193728013 08D0074
:10005000BF308C0064008C0B2A288D0B28284A3076
:100060008C008C0B312800006400800B26280034A3
:10007000C830930021203F30900010088600860988
:10008000C830930021200630900010088600 8609B1
:10009000C830930021200630900010088600 8609A1
:1000A000C830930021205B309000100886008609 3C
:1000B000C830930021205B309000100886008609 2C
:1000C000C830930021204F309000100886008609 28
:1000D000C830930021206630900010088600860901
:1000E000C830930021206D30900010088600 8609EA
:1000F000C830930021207C30900010088600 8609CB
:1001000002309200FA3093002120920B8228B1280D
:100110003230920011 08FF3A7F39860012089203AC
:10012000003803 19A32805080E398C000E300C0284
:100130003199C2832309200013093002120110 8CD
:1001400086008609 8E28282984011F3083056500D2
:10015000003066008601643093002120 8E018F01FB
:1001600038280E0804208D00910011088600 8609A9
:1001700005080E398C000E300C02031928290E08D0
:100180008C000319E42801300C020319EA2802301C
:100190000C020319F82803300C020319F828043064
:1001A0000C020319F82805300C020319F828063050
:1001B0000C020319F82807300C020319F82808303C
:1001C0000C020319F8281A290519E82801308E00B5
:1001D0008F011A298518F1288F08031DF128023094
:1001E0008E008518F72801300F0203198E011A2995
:1001F0002300E02031D0129851801290130 8E00ED
:100200001729851D8E0A051D8E0303300E02031C5F
:10021000B29851C8E0102300E02031D17290519BA
:10022000172901300F02031D172901308E000130FC
:100230008F001A2909300E02031C202908308E0075
:10024000E0804208D0091001108860086098828 78
:04025000B828630067
:02400E000200AE
:0840000002000900000000900A4
:0A4200000100000001000000000100B1
:00000001FF
;PIC16F84A
```



Parts list for motorcycle gear display.

Description	Quantity	Component ref.
Capacitor 0.1µF 50V	2	C_1,C_2
Diode 1N4007	1	D_1
Tantal capacitor 1µF 35V	3	E_1,E_2,E_3
4MHz resonator, 3-wire	1	Y_1
Connector DIN5 180, female	1	DIN5
Straight pins 10-row, 0.1in	1	X_1
Resistor 10k	4	R_2,R_3,R_5,R_6
Regulator 7805 TO-220	1	IC_2
PIC16F84A-04/P Microchip	1	IC_3
Resistor network 8x220R	1	RN_1
Common anode SC10-21	1	IC_1
7-seg LED display Kingbright 25mm or Stanley NAR-1R3-B		

button and then the down button again and digit one should be shown. Push the free button. The display should now show digit zero.

If the free switch is pushed during states 2... 6, the program forces the zero state. This prevents any lockout of different start ups and stop conditions with gear on.

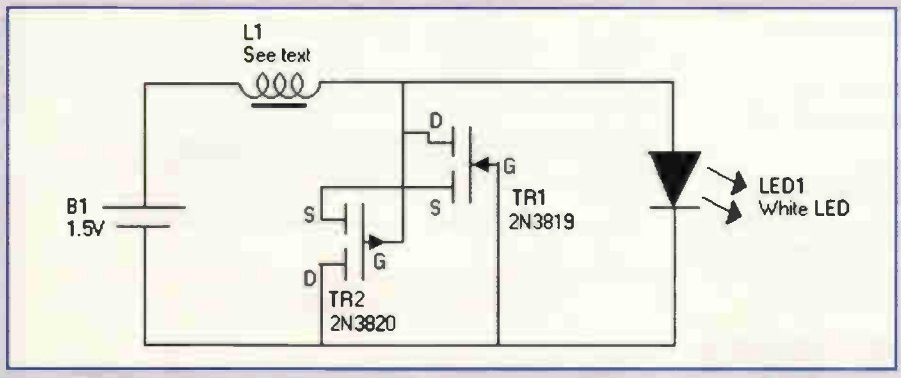
If everything went well you can attach the unit to your motorcycle and show it to your friends.

Pekka Ritamaki
Nirvankatu
Tampere
Finland

Frugal pilot light – three-component voltage step up

This circuit uses the negative-resistance effect from a pair of JFETs to voltage double a 1.5V supply in order to light a LED. Output voltage is 2.9V given a 1.5V supply.

The unusual feature of this oscillator is its extremely low power consumption. I measured this at 250µA. If the LED is removed the circuit draws 60µA.



If a piezo transducer is added across L_1, it will produce a tone dependent on the series-resonant frequency of the inductor used.

Inductor L_1 should be as large a value as possible to get a low frequency output.

Note that this circuit will also detect shorted turns in an inductor as it will not work if one is present.

One possible use of this circuit is a fishing float light for night fishing.

André de Guérin
Vale
Guernsey
G61

£50 winner

Switching EHT generator for ES loudspeakers

Originally developed to power an electrostatic loudspeaker, this circuit replaces the original 600V, 50Hz transformer.

A single-transistor ringing-choke oscilltor forms the heart of the converter. This oscillator drives a pot core. Network R3/C7 forces the oscillator to start at power up. Resistor R_6 limits base current to a safe value.

The transformer feeds a voltage multiplier to produce a final output of around 5200V. This voltage is divided by R_4-R_7 and compared to the reference, D_7, by IC_1.

Output from IC_1 drives power transistor Q_2, hence altering the supply to the converter. To allow for supply regulation, the converter should give its maximum required output at a supply of 10V.

Components C_7, C_9 and R_{10} are there to keep the control loop stable.

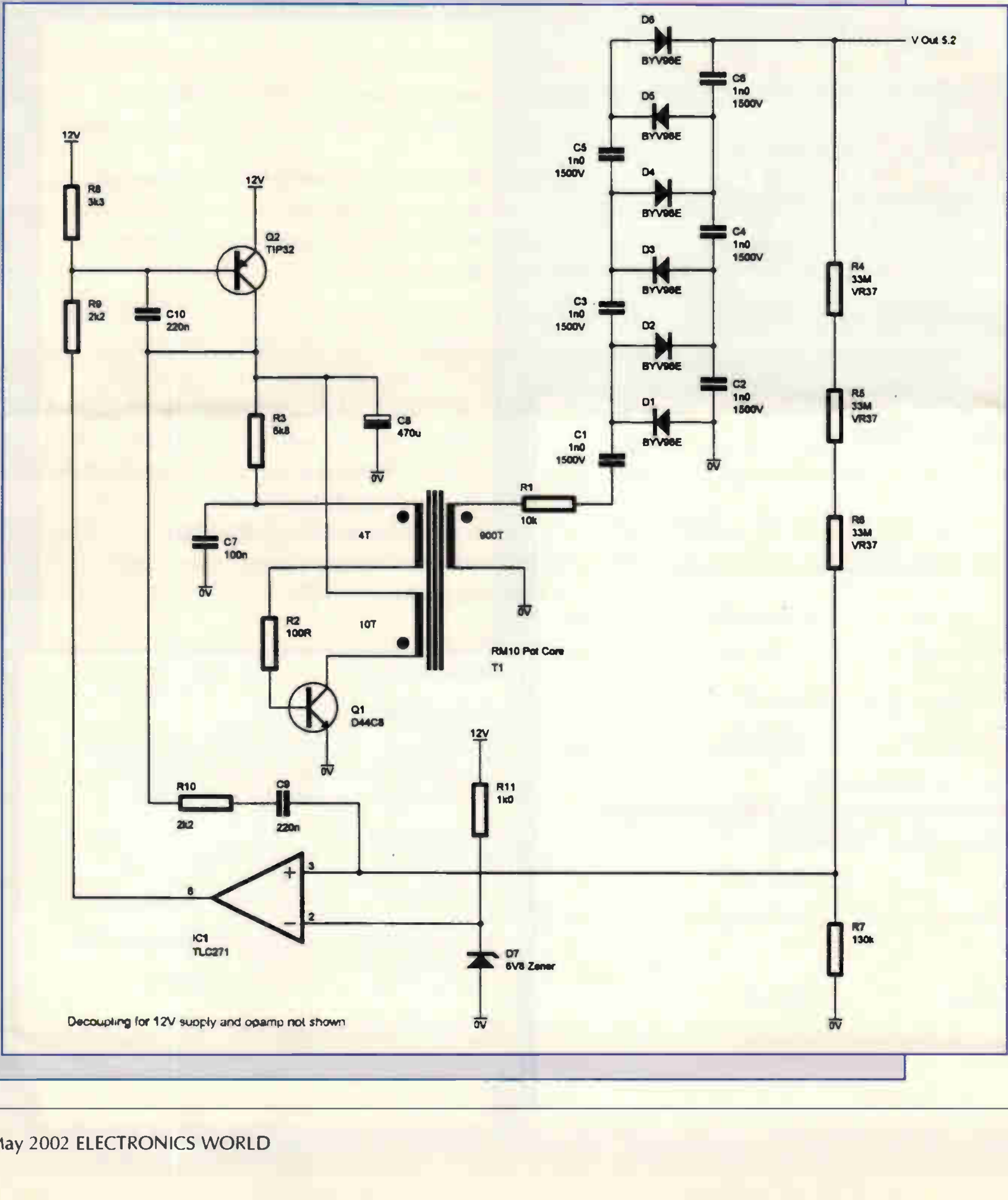
I altered the core gap experimentally to achive maximum efficicency. On the prototype, a gap of 0.1mm gave the best efficiency, with an operating frequency of about 30kHz. This gap was betwen the two halves of the pot core, giving a total air gap of 0.2mm.

Due to the high reflected capacitance, the waveform at the collector of Q_1 was a near sinusoid. Because of this, the usual suppression components around the power transistor were not required.

Resistor R1 reduces the effect of this capacitance on Q_1. ■

John Vincent
Caterham
Surrey
G9

£50 winner



Electronics World reader offer:

x1, x10 switchable oscilloscope probes, only £21.74 a pair, fully inclusive*

*Additional pairs as part of the same order, only £19.24 each pair.

Seen on sale for £20 *each*, these high-quality oscilloscope probe sets comprise:

- two x1, x10 switchable probe bodies
- two insulating tips
- two IC tips and two sprung hooks
- trimming tools

There's also two BNC adaptors for using the cables as 1.5m-long BNC-to-BNC links. Each probe has its own storage wallet.

To order your pair of probes, send the coupon together with £21.74 UK/Europe to Probe Offer, Jackie Lowe, Cumulus Business Media, Anne Boleyn House, 9-13 Ewell Road, Cheam, Surrey, SM3 8BZ

Readers outside Europe, please add £2.50 to your order.

Please supply the following:

Probes

Total__________

Name____

Address______________________________________

____

____

Postcode____________ Telephone________________

Method of payment *(please circle)*

Cheques should be made payable to ELECTRONICS WORLD

Access/Mastercard/Visa/Cheque/PO

Credit card no____________________________________

Card expiry date Signed

Please allow up to 28 days for delivery

Specifications

Switch position 1	
Bandwidth	DC to 10MHz
Input resistance	1MΩ – i.e. oscilloscope i/p
Input capacitance	40pF+oscilloscope capacitance
Working voltage	600V DC or pk-pk AC
Switch position 2	
Bandwidth	DC to 150MHz
Rise time	2.4ns
Input resistance	10MΩ ±1% if oscilloscope i/p is 1MΩ
Input capacitance	12pF if oscilloscope i/p is 20pF
Compensation range	10-60pF
Working voltage	600V DC or pk-pk AC
Switch position 'Ref'	
Probe tip grounded via 9MΩ, scope i/p grounded	

NEWPRODUCTS

Please quote *Electronics World* when seeking further information

PIII card networks four 100 Ethernet ports

Advantech's PCM-9576 is a Socket 370 single-board computer which supports Pentium III/Celeron processors running at up to 850MHz and will supply 2, 3 or 4 10/100 Mbit/s Ethernet ports. The card is designed to be used as a dual Ethernet firewall device, triple Ethernet firewall/DMZ device or through its PCI expansion slot, a four Ethernet port device that allows centralised management of a Secure Virtual Network, including firewall security and VPNs or PCI add-on cards for encryption acceleration. With networking applications in mind the VGA/LCD controller is optional. It has two 144-pin SO DIMM sockets to support 256Mbyte SDRAM and 256KByte of flash memory.

Advantech
Tel: 01908 304800
www.advantech.com

3G transceiver chips eliminates IF devices

Qualcomm has introduced its latest 3G mobile CDMA2000 IX transceiver chip set based on a zero intermediate frequency (zero IF) architecture. Called radioOne, the chip set consists of the RFT6100, RFR6000 chips. They are quad-mode devices, supporting CDMA and GPS-based position location technologies. They are designed to interface with the firm's existing MSM6000, MSM6050 and MSM6100 baseband processors. According to the supplier, the zero-IF architecture can reduce component count by eliminating the need for IF devices, IF surface acoustic wave (SAW) filters, or IF voltage controlled oscillators. One external ultra high frequency (UHF) single-band VCO is required for all CDMA frequency bands.

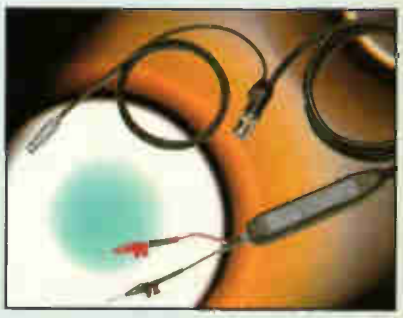
Qualcomm
Tel: 01844 260707
www.qualcomm.com

Quad-band GSM/GPRS transceiver blocks unwanted signals

Sony Semiconductor has announced its first Quad-band GSM/GPRS/Edge transceiver, the DuettoDC. It supports the four GSM frequency bands 850/900/1800/1900MHz and is GPRS/Edge compatible. Incorporating a direct conversion receiver and direct modulator on transmit, the device supports GPRS class 12 and both Edge receive and transmit. The chip includes a fast hopping sigma-delta PLL enabling GPRS class 12. The low PLL spurious and phase noise result in improved receive blocking performance. Traditional direct conversion problems of static and dynamic DC offsets are minimised through a combination of high IP2 RF mixers and a programmable/automated DC offset correction routine. The latter stores the offsets digitally and corrects them through D-to-A converters for low drift.

Sony
Tel: 01932 817502
www.sde.eu.sony.com

Differential probe with 500MHz bandwidth



The new differential probe from Yokogawa Martron is capable of transforming a single-ended oscilloscope input into a balanced differential input with a bandwidth of 500MHz and very high common-mode rejection (typical CMRR is 60dB)
The probe is designed to overcome the limitations of traditional single-ended inputs in accurately capturing high-speed signals at low power-supply voltages, particularly when isolated probing is required to capture noise-resistant differential signals in leading-edge designs.
The probe is powered with a ±12V signal, which can be supplied independently but is available as standard on the latest oscilloscope in the Yokogawa range.

Yokogawa Martron Ltd
Tel: 01494 459200
www.martron.co.uk

ICs drive 12.5dBm for full-rate ADSL

Maxim's 4361/2/3 ADSL drivers and driver/receivers have rail-to-rail outputs and have a 280mA minimum peak output current and deliver up to 12.5dBm average line power for DMT modulated signals, meeting the requirement for full-rate ADSL. SFDR at 100kHz is a low

Flat-panel monitors with rotating screens

Planar Systems has launched a range of 15-inch and 17.4 inch flat-panel monitors that feature the ability to rotate the display from landscape to portrait viewing, providing users with a choice to fit their specific desktop application.
Designed to appeal to both the business and consumer markets, the new models offer crisp, high-contrast images, large format viewing areas, USB hubs and built-in speakers. The units can be ordered in a range of exterior colours, including translucent red, blue and clear, as well as classic white or professional black.
With rotating screens, users can easily switch from landscape to portrait viewing with a simple twist of the display, allowing them to see an entire Web page, PDF, e-mail or word processing document without the need to scroll down. Software provided with the monitors easily switches the orientation of the displayed information with just a click of the mouse.

Planar Systems Ltd
Tel: 01844 276 900
www.planar.com

Please quote *Electronics World* when seeking further information

76dBc. The MAX4361 fixed-gain ADSL driver is available in 8-pin microMAX and SO packages. The Max4362 externally set gain ADSL driver with shutdown is available in 10-pin microMAX and 14-pin SO packages. The MAX4363 ADSL driver/receiver is available in 20-pin TSSOP and SO packages.
Maxim
Tel: 0800 585048
www.maxim-ic.com

16-bit flash micro lowers cost of debugging

Hitachi's latest flash micro-controller offers 128kbyte flash and 4kbyte RAM and features an on-chip debug interface that the company claims will enable low cost debugging in a target system. There is also a low cost E10T emulation option. The H8/3048BF is based on the H8/300H core with an 80ns minimum instruction cycle at 25MHz. It features an integrated timer unit (ITU) for motor control and a well-balanced peripheral set. The E10T emulator connects to the device via the on-chip debug interface and is available as a PCI or PCMCIA version. The emulator's features include hardware breakpoint on address and data, software trace, single stepping at C and assembly level, and the ability to download applications and program on-chip flash. The H8/3048BF is available in a 100-pin QFP/TQFP (Quad Flat Pack) package. The H8/3048BF, E10T, EVB-3052F evaluation board and E63052 emulator support are all available.
Hitachi
www.hitachi-eu.com

In-system programmer for STAPL diet

Actel has teamed up with First Silicon Solutions to offer a programmer for in-system programming of its flash-based ProASIC field-programmable gate arrays (FPGAs), including the recently announced ProASIC Plus family.
The in-system programmability feature uses the IEEE standard 1149.1 JTAG interface, which permits devices to be programmed after they are mounted on the PCB.
Called Flash Pro the programming system also supports the Standard Test and Programming Language (STAPL), which makes the programmer independent of any specific programming algorithms. According to the firms, it will also support new devices immediately upon release with a new STAPL file. The portable programmer is currently available for use with Actel's flash-based ProASIC 500k and ProASIC Plus families.
Actel
Tel: 01276 401462
www.actel.com

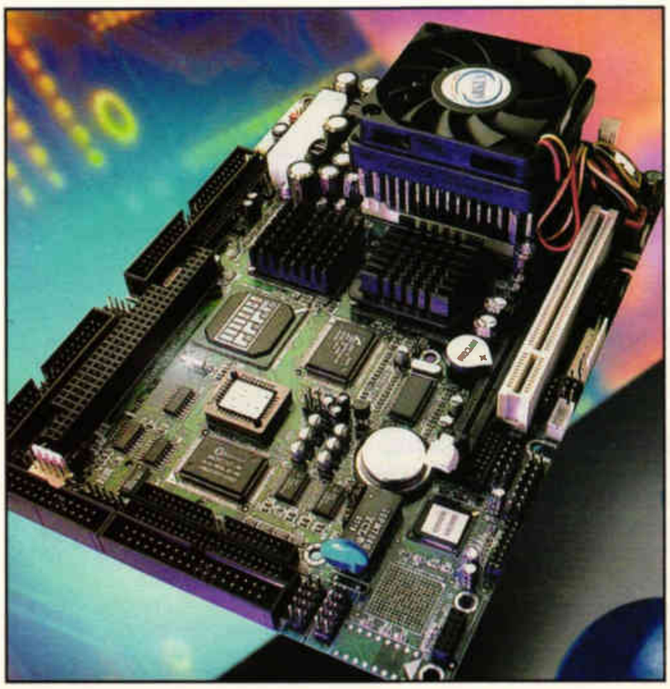
PCI card for multifunction measurement

Measurement Computing's PCIM-DAS 1602/16 board is a multi-function measurement and control board designed to operate in computers with PCI Bus accessory slots, and it retains the same connector type and pin output of the established CIO-DAS 1602/16, making it suitable to migrate designs from ISA to PCI without being forced to change connected hardware or cabling. It uses a standard 37-way D-type connector.
Available form Adept Scientific, the board features 8 differential / 16 single-ended 16-bit inputs 160kHz sample rate, burst mode, two 12-bit analogue outputs, 3 counters and 32 digital I/O.

A software library provides a common set of functions that can be called from C, visual Basic, Delphi and Labview. The library also means full software compatibility with the CIO-DAS1602/16. UL provides a common set of functions that can be called from C, VB, Delphi or Labview.
Adept Scientific
Tel: 01462 480055
www.adeptstore.co.uk

Dual-View dual-LAN board for industrial applications

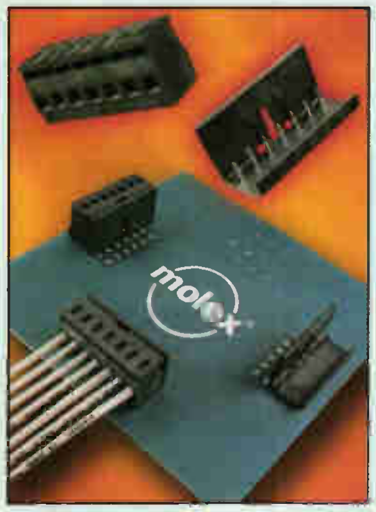
A feature-rich single-board computer (SBC), able to support two independent displays in various combinations of CRT, LCD and TV, is now available from Anders Electronics. Supporting Intel Socket 370, Coppermine Pentium-III and Celeron CPUs, the 5.25in board is ideal for a wide range of industrial applications. Featuring single and optionally dual-LAN (10/100M) as well as dual-view capability, the NC-640 offers a highly flexible display configuration, supporting simultaneous images and refresh rates on LCD/CRT, LCD/TV and CRT/TV. The product will drive 128-bit 3D CRT/LCDs with 8Mb SGRAM and support CRTs to 1200 x 1600 true colour and TFT/DSTN LCD panels up to 1280 x 1024 resolution. It also includes an integrated single-channel 110MHz LVDS transmitter, allowing connection to displays up to 10 metres away or to displays with an integral LVDS interface. Incorporating TV-out with Macrovision, CGMS-A and WSS for DVD copy protection, the NC-640 also offers MPEG-2 video textures and motion compensation for full-speed DVD playback. The product has advanced 3D audio capability and a wide range of connectivity options, including on-board USB (x2) and IrDA interfaces, 4COM ports, RS-232/422/485 (5V and 12V), PCI, PC/104, IDE and a bi-directional parallel port. GPS and touch-panel interfaces are available as options.
Anders Electronics
Tel: 020 7388 7171
www.anders.co.uk



Please quote *Electronics World* when seeking further information

Eurostyle terminal block is highly sprung

The Eurostyle plug terminal block from Molex incorporates a spring clamp which means it can be unplugged without un-wiring for replacement of faulty or damaged electronics.
Applications include automation, motion and process controls as well as telecommunications equipment, HVAC systems and power supplies.
A pre-loaded stainless steel spring clamp enables installers to secure terminations reliably and securely. With horizontal and perpendicular spring actuation slots, termination may be accomplished for many orientations.



Available in two to 24 circuits, these terminal blocks have 5.08mm (.200in) pitch and use 14 to 24 AWG. Field service rated at 300V for 10A with 14AWG wire, operating temperatures are –40°C to 140°C. The system uses phosphor bronze contacts and hot tin dip plating (also available in gold).
The insulator is also surface mount compatible (SMC), made of high temperature polyamide polymer with a 94 V-O high flammability rating, eliminating wave soldering.
Molex
Tel: 01252 720751
www.molex.com

Single-chip modem with caller ID

TDK Semiconductor has introduced a 3.3V single chip modem that combines all the controller (DTE) and data pump functions necessary to implement a V.22bis data modem. The 73M2901CL includes functions like caller ID, blacklisting, parallel phone detect (Line-In-Use and Parallel-Pick-Up/Line-Seize), long space disconnect, inactivity timeout and programmable call progress.
The device is based on an 8032 microcontroller core with a proprietary multiply and accumulate (MAC) co-processor, analogue front end, Sigma Delta A/D and D/A. The ROM and RAM necessary to operate the modem are contained on the device.
It is capable of data transmission and reception at 2400bit/s and power consumption is 9.5mA.
The modem is available in a 32-pin PLCC, 32-pin TQFP or a 44-pin LQFP package.
TDK Semiconductor
Tel: 001 714 508 98821
www.tdksemiconductor.com

Current switch has 1.75A limit for cards

Maxim has introduced the MAX1922 high-side Mosfet current-limited $70m\Omega$ power switch with built-in fault blanking. It has a preset 1.75A current limit (±20 per cent maximum over the operating temperature range), which protects power distribution systems in PC cards, USBs and other hot-swap plug-in applications. The narrow current limit (1.4 to 2.1A) allows for the use of smaller and lower cost power-supply components that can be sized to accommodate lower over-current fault conditions. Input voltage ranges from 2.7 to 5.5V. The device comes in an eight-pin SO package.
Maxim
dbserv.maxim.com

CAN transceiver survives loss of ground

Linear Technology has introduced the LT1796, a transceiver for controller-area network (CAN) bus applications. It is designed to withstand ±15kV ESD strikes and faults up to ±60V in automotive applications. In these applications, the loss of ground connection or cross-wiring faults can force DC voltages in excess of 24V in either polarity onto the bus pins. The device is designed

High-current bench power supplies

The newly upgraded TSX range of bench DC power supply units from TTi offers very high performance at significantly lower cost than other PSUs of comparable performance.
Models currently available include 35V, 10A and 18V, 20A units in both standard and programmable versions. The standard versions incorporate conventional analogue controls, while the programmable versions offer keyboard control along with RS-232 and IEEE-488 interfaces.
The heart of the TSX series PSUs is an advanced regulator design which combines switch-mode pre-regulation with linear post-regulation. The pre-regulator uses specially developed techniques to dramatically reduce the capacitance between input and output, thus eliminating the high levels of common-mode noise normally associated with switch mode PSUs. The linear post-regulator combines very low levels of output noise with excellent load regulation and transient response, resulting in performance comparable with that of a pure linear design
The hybrid regulator design provides a PSU which is both smaller and lighter than competitive products. The high thermal efficiency also means that the PSUs are silent in operation, since fan cooling is unnecessary.
All TSX series PSUs can operate in both constant-voltage and constant-current modes, with automatic crossover and automatic mode indication. They incorporate high-resolution digital meters for both voltage and current. Voltage and current levels can be set to high accuracy prior to connection to the load, and the limit settings can be checked at any time.
Thurlby Thandar Instruments
Tel: 01480 412451
www.tti-test.com

Please quote *Electronics World* when seeking further information

to survive these faults without the need for external protection circuitry, said the company. The device matches the industry standard footprint in the SO-8 package including a combined slew rate control/standby pin. In standby, the supply current is reduced to 800μA. The slew rate control allows a maximum data rate of 500kbit/s or can be programmed for slower rates to minimise EMI and reduce reflections due to long stubs or improper termination. It is offered in the 8-pin SO and PDIP screened for both the commercial and industrial temperature ranges.
Linear Technology
Tel: 01276 677676
www.linear-tech.com

LCR meter is one touch for strays

Available from Vann Draper, the RLC100 is a microprocessor controlled LCR meter capable of making four line measurements of R, L, C, QR, QL, DC and d using series or parallel connection. The unit can display deviations of measured values from reference components either absolutely or relatively in terms of percentage. Also included is an automatic self-diagnosis and one-touch stray capacitance compensation. The design of the instrument has reduced the number of front panel controls to four, plus a mains on-off, which enables the instrument to be set or operated with little adjustment. A group of LEDs indicates control selection and a 16 x 1 alphanumeric backlit LCD provides enunciators and readout of the measured values.
Vann Draper
Tel: 01283 704706
www.vanndraper.co.uk

Precision resistors on a budget

The RE 0207 and RE 0204 from VTM are two ranges of precision metal-film resistors in 0207 and 0204 (0.25 and 0.125W) body sizes. According to the supplier, they are intended as a lower cost alternative to traditional precision resistors. The RE 0207 is available in a resistance range of 10Ω to 2MΩ, while the RE 0204 is available between 10Ω and 1MΩ, both with a standard resistance tolerance of ±0.1% and a temperature coefficient of resistance of +15ppm/°C, although other tolerances and TCRs are available. The resistance element in these devices is a precisely controlled thin film of metal alloy deposited on a high quality alumina substrate. Plated caps are force-fitted before the assembly is trimmed using laser techniques.
VTM
Tel: 01494 738608
www.vtm.co.uk

Miniature joystick for movement in five directions

A five-direction miniature joystick from Tyco Electronics measures 10.4 x 12.0 x 5mm. A single pole, five throw configuration, the switch is rated at 1 to 50mA at 24V DC. It also provides a select function and scanning functions: Up/Down/Left/ Right. Contact resistance is 200mΩ maximum and insulation resistance is a minimum of 100MΩ at 100V DC. Travel is 0.25 ±0.15mm for the select function with an operating force of 360 ±80g and a minimum release force of 100g. For the four scanning functions, travel is 0.35 ±0.15mm with an operating force of 110 ±45g and a minimum release force of 10g.
Tyco Electronics
Tel: 020 8954 2356
www.tycoelectronics.com

Capacitor array in 0612 package

The GNM314 capacitor array from Murata contains four individual capacitors, all of the same dielectric material, tolerance, capacitance value and voltage rating, in a single 0612 package. It includes temperature compensated arrays available from 10pF to 360pF, dielectric constant types from 220pF to 100nF (X7R) and 2.2nF to 150nF (Y5V). Rated voltages are from 16 to 100V.
Murata
Tel: 01252 811666
www.murata.co.uk

Polarity controller for EMC antennas

Hursley EMC Services has introduced a mast polarity controller for EMC testing in automated anechoic chambers. The controller has GPIB and RS232 interfaces with a manual over-ride facility. The MC4090 mast controller is suitable for all pneumatic masts, said the supplier. And at £4,500 + VAT

Fast LVDs for 3G backplanes

National Semiconductor has announced a 10-bit bus low voltage differential signalling (LVDS) serialiser/deserialiser chip set for high-speed data transfer over a single differential pair. The SCAN921025 and SCAN921226 are designed to meet the high speed data transfer rates of third-generation wireless base station, video, and medical instrumentation markets, said the company. The chip sets were developed to address clock speeds over 66MHz, specifically 78.8MHz for telecom and 74.25MHz for video applications. The serialiser input accepts as many as 10 parallel bits with the associated transmit clock to latch the parallel bits into the device. It serialises them and embeds the clock for serial transport. The deserialiser accepts the serial stream, recovers the clock and data, and delivers both to the receiver parallel interface.
The company has also introduced the SCAN921260UJB, which incorporates six 1:10 deserialisers with IEEE 1149.1 test capability and built-in-self-test mode that supports data rates up to 66MHz. The 10:1 (TTL to LVDS) serialiser has a frequency operation of 30MHz to 80MHz. The deserialiser has a random lock and frequency operation also of 30MHz to 80MHz.
National Semiconductor
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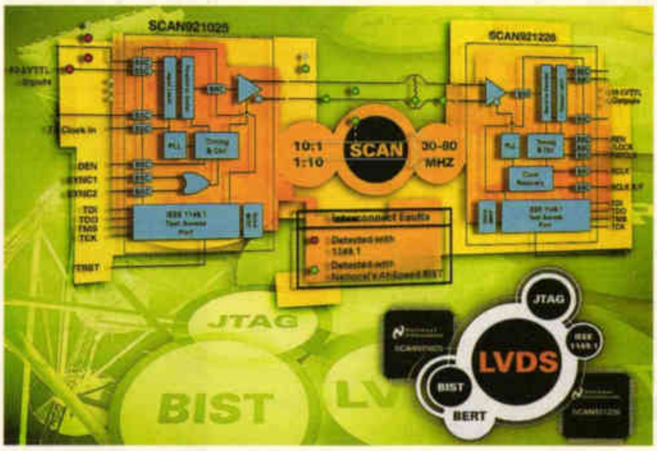

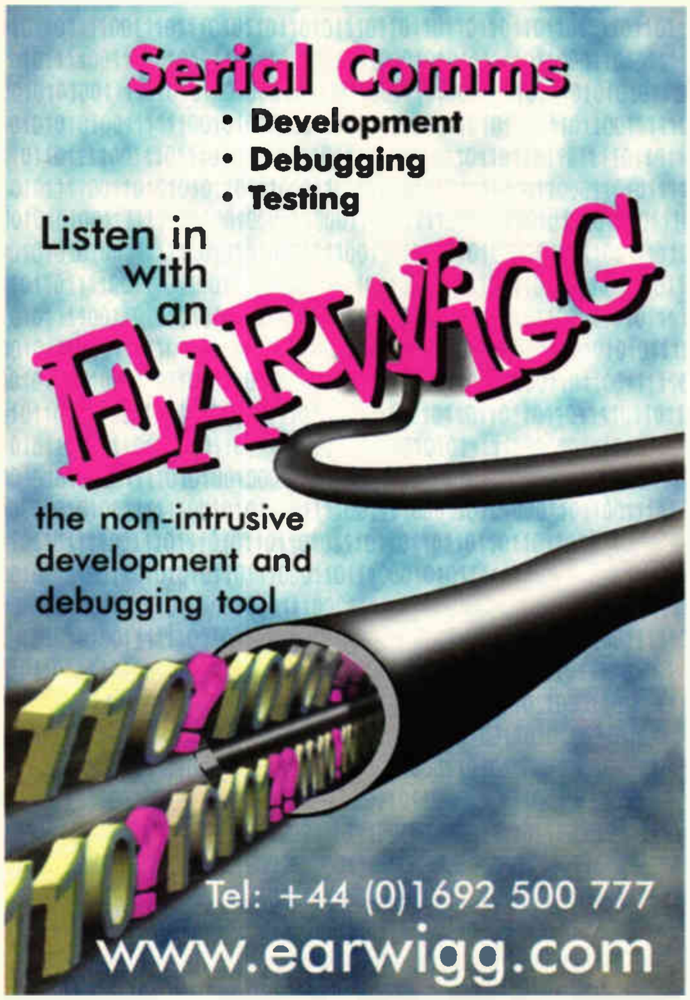

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CTL Components

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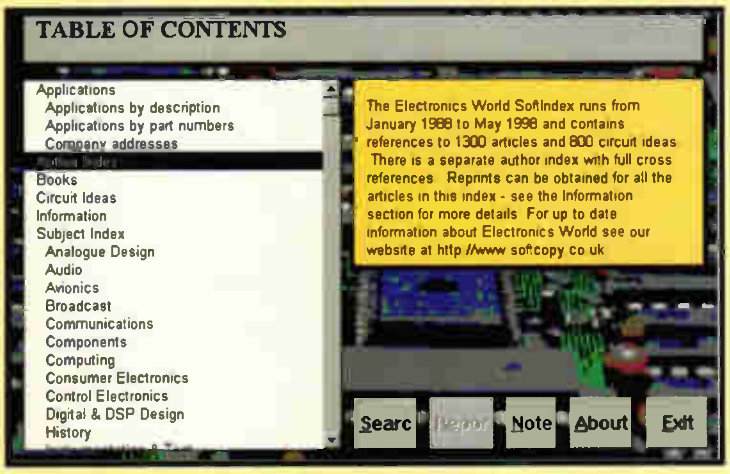

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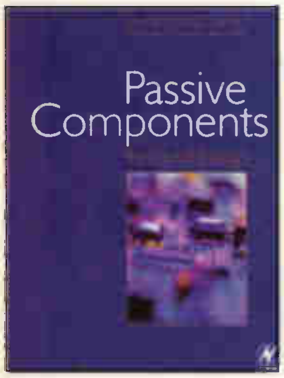

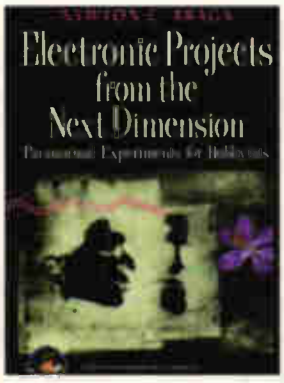

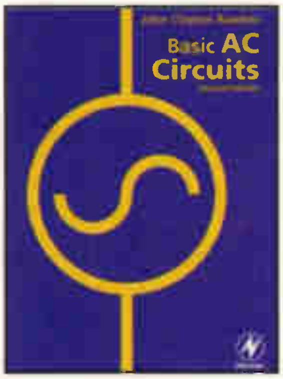

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In this second article on programmable logic, Andrew Malcolm looks at the standard language used for defining programmable devices.

Designing with VHDL

In my last article I looked at the history of programmable logic devices, from their first, simple forms to the multi-million gate forms of today.

In those early days, programming these devices was more or less manual, using modified PROM programmers to write directly to the device's fuse-map. Device complexity increased and software support for other parts of the design cycle became available, including schematic capture and CAD layout programs. As a result, the tools available to programmable logic designers became more sophisticated.

Inevitably, device vendors implemented their own software to support their own devices. Soon there was a variety of incompatible packages, each with their own standard. Moving a design from one vendor's device to another often meant a complete redesign, and so designers became locked in to a particular vendor.

At the same time, the chip design industry was struggling with the growing complexity of fixed-logic devices, from microprocessors to LAN chips. A software industry grew up to support these design activities. Again, many proprietary languages and techniques came into being.

In the early 1980s, the IEEE – America's equivalent to our IEE – realised that standardisation across the industry would bring benefits by allowing all logic design concepts to be expressed in a common language. As part of the 'Very High Speed Integrated Circuit', or VHSIC, initiative, VHDL was born.

VHDL – an acronym for VHSIC Hardware Definition Language – is used for many purposes today. These range from specification to simulation, on device architectures from simple PAL devices to multi-million gate FPGAs. The key to VHDL's success here is its ability to express designs at many different levels of abstraction, and its modular approach to design.

Many vendors, both device vendors and independent design-tool companies, provide VHDL compilers and fitters. They also provide tools that generate device constants from schematics. These use VHDL internally. Some tools are prohibitively expensive, and can be dauntingly complex to set up and use.

There are simpler tools available however, and some of them can be downloaded from the Internet for limited-time use. A list of starting points is presented in a separate panel article.

Intellectual property

VHDL and its associated software tools have enabled a whole new industry: that of intellectual property.

Companies can write and sell device definitions from simple libraries that mimic TTL families and other MSI devices up to complete processor cores, complex peripherals and specialist memory arrays. OEMs can use this 'IP' to quickly assemble a product, using CPLDs and FPGAs as the target devices.

Alternatively, they can pass on their design to a silicon foundry for ASIC production. In this way, companies can take advantage of the high level of integration offered by FPGAs and ASIC technology, without having to design from scratch. They don't need to have the specialist knowledge required to produce the IP for some types of design either.

A good example might be a JPEG codec (encoder/decoder). A digital camera manufacturer may not have the mathematical expertise to implement a codec in hardware. However, that manufacturer could buy the IP as a 'black box', and would have the expertise to employ it.

Elements of the language-combinatorial logic

Lets take a look at a simple example: describing an AND gate. **Fig. 1.** in VHDL.


```
library ieee;
use IEEE.STD_LOGIC_1164.ALL;

entity and_gate is
  port ( a,b     : in std_logic;
         c       : out std_logic );
end entity;

architecture arch of and_gate is

begin
        c<=a and b;
end architecture;
```

An AND gate is described in the above VHDL extract. Taking the file line by line, I'll explain the what language features show here.

The first two lines a declare a reference to an external library. In this case, it's a standard type library defined by the IEEE. The types it defines are the `std_logic` types, which I'll be discussing later.

The next four lines declare the entity. This is analogous to a schematic symbol, as it defines the inputs and outputs to a unit of functionality.

Note that these inputs and outputs may or may not correspond to physical pins on a device: This entity may be part of a larger hierarchical design, much in the way a TTL IC might form part of a larger board performing a more complex function.

In this case, the entity has two inputs, `a` and `b`. The entity has a single output, `c`. The entity is named `and_gate`, and this name is used to refer to the entity when it is incorporated into a larger design.

The remainder of the file describes the architecture of the entity. This is in effect, its desired functionality. In this case, the AND gate is fully describable in terms of simple Boolean algebra, and so the single line `c<=a and b` expresses the required functionality.

Port declarations

Returning to the entity description, let's look at the port declarations. Both input and output are declared as `std_logic`. This is an IEEE defined type from the IEEE library.

The type defines the legal states of the port. Although we think of logic pins as having only two states, 0 or 1, the reality is somewhat different: what about three-state or open collector outputs?

The `std_logic` type defines all the legal states of a port, and comes into play when entities are placed on a bus. It is also useful in describing unknown initialisation states in entities with bistable devices. These extra states make in possible for synthesis and simulation tools to detect conditions such as bus conflicts – i.e. two drivers driving a common line simultaneously – and floating, undriven inputs.

From the above example, and a few extra keywords such as `or`, `nor` and `nand`, you should now be able to write entities describing many of the standard TTL combinatorial functions. For example, by simply by adding extra input ports and extending the architecture like this: `c<= a and b and c and d…` etc;' an N-input AND gate is easily described.

It is possible for an entity to have internal signals, those that are not visible from the entity declaration. In this way, the architecture may describe an arbitrarily complex logic function of *N* inputs:

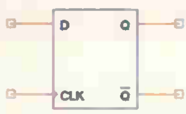
```
library ieee;
use IEEE.STD_LOGIC_1164.ALL;

entity and_nor_func is
   port  ( a,b,c : in std_logic;
           d     : out std_logic );
end entity;

architecture arch of and_nor_func is
signal e : std_logic;
begin
       e<=a and b;
       d<=c nor e;
end architecture;
```

Elements of the language-sequential logic

In the last section I showed that it is possible to describe arbitrary combinatorial functions and package them within an entity. Later I will describe how it is possible to combine those entities into a larger system, in much the same way that you might build a system from TTL gates.

Combinatorial systems alone are of limited use. The TTL designer is soon reaching for bistable devices and registers to create systems that have *state*, that is they remember the value of their inputs over time.

VHDL has constructs that allow the designer to describe sequential logic:




```
library ieee;
use IEEE.STD_LOGIC_1164.ALL;

entity d_type is
    port ( clk    : in std_logic;
           d      : in std_logic;
           q      : out std_logic );
end entity;

architecture arch of d_type is
begin
process(clk)
begin
       if rising_edge(clk) then
             q<=d;
       end if;
end process;
end architecture;
```

As before, the entity describes the inputs and outputs to the function, in this case a simple bistable device. Inside the architecture block however, we encounter some new syntax.

The 'process' block describes an activity that takes place only when a signal or signals change state. These signals are described in a *sensitivity list* following the 'process' keyword, in this case `clk`.

So in this instance, new values only appear on the output port 'q' when the `clk` signal changes state. Within the 'process' block, it is possible to detect rising or falling edges of sensitivity list signals and act only on rising or falling edges. So in the current example, the `q` output is assigned the value at the `d` input on the rising edge of the `clk` input.

A more complete implementation of a bistable device might have a reset input, a clock enable and a q-bar output:

```
library ieee;
use IEEE.STD_LOGIC_1164.ALL;

entity d_type_full is
    port ( clk   : in std_logic;
           rst   : in std_logic;
```

Internet resources

Major device vendors:

http://www.latticesemi.com

Lattice produces CPLDs and has a tool set called ispExpert. It supports design and programming with their 'isp' family of devices. An limited-use form or this tool is available for download. (Be warned, the files are large, more than 30Mbytes and will take a long time to download).

http://www.xilinx.com

Xilinx produces arguably the largest and most versatile FPGAs

http://www.altera.com

Altera are close behind Xilinx, and indeed have the edge in terms of device clock speed.

```
          clken   : in std_logic;
            d     : in std_logic;
            q     : out std_logic;
            q_bar : out std_logic );
end entity;

architecture arch of d_type_full is
begin
process(clk,rst)
begin
        if rst='1' then
                q<='0';
                q_bar<='1';
        elsif rising_edge(clk) then
                if clken='1' then
                        q<=d;
                        q_bar<=not d;
                end if;
        end if;
end process;
end architecture;
```

Note that the reset signal appears in the sensitivity list. This is to ensure that it operates asynchronously of the clock signal: remember, the process only 'runs' when signals in the sensitivity list change.

Note also that it is the *state* of the reset signal, and not an edge, that resets the `q` outputs. The clock-enable signal on the other hand, does not appear in the sensitivity list since it only modifies the operation of the clock input.

The state of `clken` is used to qualify assignment of new `d` values to the `q` outputs. Finally, the `q_bar` output is simply assigned to the inverse of the d input. This last statement shows that combinatorial logic – in this case a simple 'not' – can be employed within a process. If a more complex function were required, combinatorial logic could be used to achieve it.

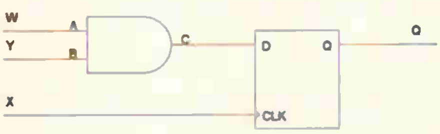
Elements of the language-structural VHDL

So far. I have shown how to generate descriptions for combinatorial and sequential logic functions. Later, I will illustrate how, simply by changing the input and output declarations, you can change a single bistable device into a 32-bit register – greatly extending the power of out functional block.

First though, I will discuss how structural VHDL allows you to interconnect blocks. Returning to the TTL analogy, structural VHDL provides the wires and PCB traces that interconnect gates in a traditional design. A structural block will of course have its own input and output ports, so it must contain an entity declaration.

Each design will have a master entity that corresponds to an actual CPLD or FPGA. This entity is used by 'fitter' software to assign physical pins to logical ports. Complete designs are built up as hierarchies of structural VHDL and functional blocks.

The next part of a structural block is a declaration of subcomponents described elsewhere. These declarations mirror the entity declarations of those subcomponents, but are called components, and are inserted, like `signal` declarations, after the `architecture` statement but before the `begin`:




```
library ieee;
use IEEE.STD_LOGIC_1164.ALL;

entity gated_flip_flop is
    port ( w     : in std_logic;
           x     : in std_logic;
           y     : in std_logic;
           z     : out std_logic );
end entity;

architecture arch of gated_flip_flop is

component d_type is
    port ( clk    : in std_logic;
           d      : in std_logic;
           q      : out std_logic );
end component;

component and_gate is
    port ( a,b    : in std_logic;
           c      : out std_logic );

end component;

signal p : std_logic;
begin

        U1: and_gate port map(x,y,p);
        U2: d_type  port map(w,p,z);
end architecture;
```

The architecture block itself consists of `port map` statements, one per functional block. These, as their name suggests, map the ports of the contained components to the ports of the containing entity.

Each element within brackets maps a single port from the component to a port or signal in the outer entity. Reading from left to right, these ports correspond with posts from first to last in the component declaration.

The functional blocks are given a reference, in the same way as on a circuit diagram – IC_1, IC_2 – and the required block name follows that. So in this case the `w` and `y` inputs of the outer entity are mapped (connected) to an `and_gate` block, inputs `a` and `b`. Similarly, IC_2, a `d_type`, is connected to input `x` and output `q`.

Internally, the connection between the output of the AND gate and the `d` input of the bistable device is achieved via the signal `p`, as `p` appears in the `port map` statement for the `and_gate` and the `port map` statement for the `d_type`.

Glossary

FPGA	field programmable gate array
CPLD	complex programmable logic device
PAL	programmable array logic
VHDL	VHSIC hardware definition language
VHSIC	very high speed integrated circuit
IEE	Institution of Electrical Engineers (UK)
IEEE	Institution of Electrical and Electronic Engineering (US)
LAN	local-area network
CAD	computer-aided design
TTL	transistor-transistor logic
IC	integrated circuit
PROM	programmable read-only memory
PCB	printed circuit board
CPU	central processing unit
RAM	random access memory
PCI	personal computer interconnect
LED	light emitting diode

Elements of the language-vectors

So far, we have dealt with single signals only. In many systems – including microprocessor-based systems – data flows around on busses. These are simply groups of signals that have a collective meaning, and often share common timing characteristics.

Examples are a data bus between a CPU and a RAM array, an address bus in the same system, or a multiplexed bus carrying address, data and control signals in different time slots, such as a PCI bus. In all these cases, it would be tedious and error-prone to handle each signal separately. Also, circuit diagrams and VHDL listings alike would be unwieldy in this circumstance.

Circuit designers have become accustomed to collecting signals into busses to simplify the schematics, and VHDL has a powerful syntax that mirrors this technique. It defines a number of different signal vector types. One of them is:

```
signal data_bus: std_logic_vector(31 downto 0);
```

This statement declares a vector of 32 data signals that can be treated as a unit. The real power of this syntax becomes clear if we redefine the d-type bistable device as a 32-bit register simply by changing the q and d port declarations to be vectors:

```
library ieee;
use IEEE.STD_LOGIC_1164.ALL;

entity register_32 is
  port ( clk  : in std_logic;
         d    : in std_logic_vector(31 downto 0);
         q    : out std_logic_vector(31 downto 0) );
end entity;

architecture arch of register_32 is
begin
process(clk)
begin
       if rising_edge(clk) then
           q<=d;
       end if;
end process;
end architecture;
```

About the author

Andrew Malcolm is a Chartered Engineer with more than 20 years experience in the electronics, industrial control and software industries. He runs his own consultancy company, Synchronous Designs Ltd. www.synchronousdesigns.co.uk
He may be contacted at info@synchronousdesigns.co.uk

Now you have a 32-bit register – without changing the architecture. As the `clk` signal was not declared as a vector, it will be used to clock all the registers – 32 of them – generated by the `process` block. This technique could equally be applied to our `d_type_full` block, giving a 32-bit register with reset, clock enable and q-bar signals.

Using a further technique, known as generics, it is also possible to parameterise the bus width in order to produce a register whose width may be determined by the user. Of course, when you compile this code in order to program a device, this register will take up precisely 32-bit bistable-device cells. As a result, it must be borne in mind that large structures will take up correspondingly large parts of the target device. This is a shorthand, like the schematic bus, but it doesn't magically save device space!

Once designed using this technique, bus-based subsystems like this can be connected with structural VHDL as before. Again, the vector syntax means a single `port map...` statement can deal with many signals at once.

What next?

In the next article on this topic, I will show how to apply the VHDL presented here to a practical application. This application is a high-speed frequency counter with LED display. I will also introduce a few more language constructs.

On the practical side, I will be looking at one vendor's tool set and at mapping a design into a particular device, along with programming tools and techniques.■

Further reading

VHDL for Designers: Sjoholm and Lindh. Prentice Hall, 1997 ISBN 0134734149. This is an excellent book for newcomers and experienced users alike. It is very easy to read, covering all the topics touched on here in much greater depth.

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Track

1 Washington Post March, Band, 1909
2 Good Old Summertime, The American Quartet 1904
3 Marriage Bells, Bells & xylophone duet, Burckhardt & Daab with orchestra, 1913
4. The Volunteer Organist, Peter Dawson, 1913
5. Dialogue For Three, Flute, Oboe and Clarinet, 1913
6. The Toymaker's Dream, Foxtrot, vocal, B.A. Rolfe and his orchestra, 1929
7 As I Sat Upon My Dear Old Mother's Knee, Will Oakland, 1913
8 Light As A Feather, Bells solo, Charles Daab with orchestra, 1912
9 On Her Pic-Pic-Piccolo, Billy Williams, 1913
10 Polka Des English's, Artist unknown, 1900
11 Somebody's Coming To My House, Walter Van Brunt, 1913
12 Bonny Scotland Medley, Xylophone solo, Charles Daab with orchestra, 1914
13 Doin' the Raccoon, Billy Murray, 1929
14 Luce Mia! Francesco Daddi, 1913
15 The Olio Minstrel, 2nd part, 1913
16 Peg 0' My Heart, Walter Van Brunt, 1913
17 Auf Dem Mississippi, Johann Strauss orchestra, 1913
18 I'm Looking For A Sweetheart And I Think You'll Do, Ada Jones & Billy Murray, 1913
19 Intermezzo, Violin solo, Stroud Haxton, 1910
20 A Juanita, Abrego and Picazo, 1913
21 All Alone, Ada Jones, 1911

Total playing time 72.09

21 tracks – 72 minutes of music.
Published by *Electronics World*. All recordings reproduced by Joe Pengelly.

Make single-side PCBs

Cyril Bateman runs through a multitude of tips and tricks for making your own printed circuit boards.

One of the great attractions of *Electronics World* is the number and variety of desirable electronic circuits it publishes. Perhaps like me you have frequently said, "I would like to build this, if only a circuit board was available".

Many articles do include details and drawings of the printed circuit board used to build the prototype design. Because of the tooling and minimum order costs involved though, commercially produced circuit boards may simply not be viable. Yet for little equipment cost it is feasible to etch and drill your own PCB.

This article is not intended as a council of perfection. Instead it recounts various methods I have found to work – or not – for producing prototype PCBs.

A minimal-cost DIY approach

While it is nice to build a circuit on a solder resist and component legended printed circuit board, it is not essential. Reduced to the minimum, it is only necessary to etch the tracks, drill the holes and trim the board outline to size.

I produced my very first home-made PCB almost forty years ago. It was destined for the pulse counting FM tuner, then published in *Wireless World*.

In those days photo-sensitive PCB materials were not readily available. Using carbon paper, adhesive tapes and etch-resistant transfers or etch resist pens, the artwork was often prepared directly on the copper surface. When

Commercial methods

The actions needed to provide commercially produced PCBs can be broken down into:

- Artwork design
- Preparation of suitable Gerber and NC drill files
- Photoplotting
- Board etching and drilling
- Solder resist and legend applications
- Sawing or routing to size
- Inspection and test

Of these stages, the board designer is responsible for the artwork design, Gerber and drill file preparation and accuracy. Checking the accuracy of the artwork design is relatively easy. Validating the Gerber and drill files can prove extremely difficult. Most low-cost PCB design software systems can output the required files, but do not provide any means to 'read back' for verification, prior to committing to production costs.

Gerber files are used to photoplot the masters used to etch circuit tracks. They are also used to produce the solder resist patterns and component legends. They must be in a format accepted by the photoplotter and error free.

Particular care is needed to avoid including extraneous, duplicated or broken lines or tracks. Photo plotters do not recognise a track as such, but are simply triggered 'on' when crossing one light dark transition and 'off' when crossing the next.

Some of the smaller commercial PCB suppliers will agree to pre-vet these files for you before your costs escalate. For this they need your full drawing set, the same software package you used and copies of your design files.

I well recall feeling extremely nervous about the quality of the Gerber files for my tanδ meter boards. Fortunately my supplier[6] had a copy of my software and would check my Gerber files.

In the event, while they did query one intentionally unterminated guard track, the first-off boards had one essential track missing. My boards had to be re-tooled and re-made, doubling costs.

Tooling charges vary, but typically each photoplot and drill file will cost some £15. Expect to pay £60 plus to production tool a single sided board, doubling these costs for two-sided boards.

Board manufacture and delivery costs are additional. All charges escalate rapidly if narrow track widths and spacings are used, so do check first before committing.

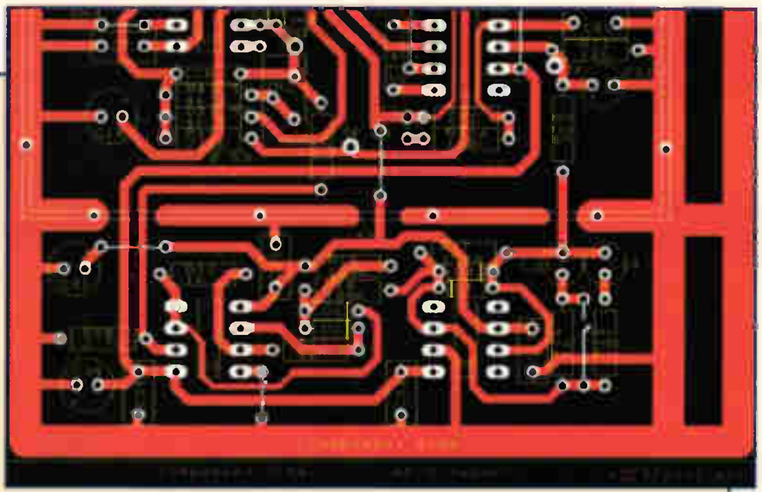

Fig. 1. When exposing a film to ultra-violet light, clear labelling as to the film's correct orientation will help to avoid making board wasting, reversed images.

duplicate boards were needed they were screen printed, using artwork made from Reeves two part 'Profilm' stencil paper, affixed onto a silk screen using a hot iron.

Covering a board-sized polystyrene tile with 1in graph paper facilitated layout. The required components were easily pressed into position. With components positioned, the tracks were drawn on a duplicate piece of paper.

Alfac or Seno pre-printed, rub-down, etch resistant transfers for most IC types and component pads can still be bought for a few pounds. Self-adhesive, flexible, black crepe track tape is available in small reels. Two or three reels provide sufficient choice of track widths for most circuits.

Some designs were printed to scale in magazines' others had clearly identified board dimensions. For these I used overhead projector transparency foils in a dry toner photocopier to make a true-size foil. Any track that lacked density was easily overlaid using transfers or tape.

Needing no special equipment, the Seno GS 'etch in a bag'[1] method provides a clean, economical and safe method of etching a few boards. The supplied neutraliser converts exhausted etchant into an easily disposed of solid mass. Etching, washing and drying a PCB can be completed in less than thirty minutes.

Use plastic containers for developers and etchants. While glass is also suitable, accidental breakage presents an unnecessary hazard. Do not use metal tools or containers.

These low-equipment-cost methods are still valid today. However many alternatives have since been developed, most of which I have used at one time or another.

Other artwork options and methods

Assuming you have a laser printer available, you may find that it gives an adequate image on laser transparency film using just one print pass. However you may produce better images using Laserstar film, specially developed for printing PCB artwork.

Laserstar 100062 film[3] is available direct from Mega in packs of 10 A4 sheets for about £6. Suitable for any laser printer it produces a good dense image. This film is also usable in many dry toner photocopiers, allowing artwork production from a pre-printed original.

Some readers have reported great success using the press-n-peel transfer system. This film is printable using a laser printer or suitable photocopier. The resulting image is transferred to your PCB laminate using heat from a domestic 'iron'. However I prefer re-usable artwork so this is one method I have not tried for myself.

The very best artwork is produced using a photoplotter and Lith photographic film. This is the method most used professionally even for small production runs. Provided you can output the appropriate Gerber file, an artwork photoplot can be received in three or four working days, for around £20. This may prove too expensive however when only a single PCB is required.

There's an even simpler method using the same Gerber and matching NC drill file. A number of PCB makers will provide a complete one-off prototype single-sided PCB complete with component legends and solder side resist for some £65. Of course for these last two routes, you must accept responsibility for any errors your files contribute.

Perhaps the safest route for one-off PCBs is to purchase a suitable flat-bed pen plotter, with pens and ink to match your film. This can provide excellent quality and low-cost art work, but don't forget to clean your plotter pens properly when their work is finished.

Using etch resist ink, a flat-bed plotter can be used to plot direct onto the copper laminate, completely bypassing the artwork film, UV exposure and developing stages.

While I print most of my artwork, occasionally for test jigs or RF strip line circuits I find the quickest method is to use stripping film and UV-proof red Sellotape. This method was used extensively 30 years ago to produce times ten master artwork. The large art work was reduced to size with a camera and used to manufacture precision thick-film circuits.

Called Autotype Ruby Automask film [4], this film comprises a transparent red UV proof film, laminated to a clear base film. A sharp model knife cuts through this red film around any unwanted area. Unwanted red film is then easily peeled away. I still use this method to quickly produce artwork for jigs or ground planes. Being UV and etch resistant, the red Sellotape can be used for artwork as well as for direct etching.

In my pre-computer years – especially when a printed drawing had to be re-scaled – I cut short lengths from black and white high contrast 35mm document film. Loaded with five or six exposures, my 35mm camera produced excellent quality negatives. A correct sized positive enlargement onto 'Lith' cut film was then used as the final artwork.

Document and Lith films are orthochromatic, or insensitive to red light. They are easily handled using a bright red safelight. Development can be by time and temperature, or more usually by inspection in a dish, as used to develop a black and white photographic print.

This method is valid today and is still used commercially. 'Lith' film is a very high contrast material that produces a sharp and extremely dense, archival quality image. I have some films I made more than twenty years ago that are still usable.

All materials can be obtained mail order from the Silverprint Company.[5]

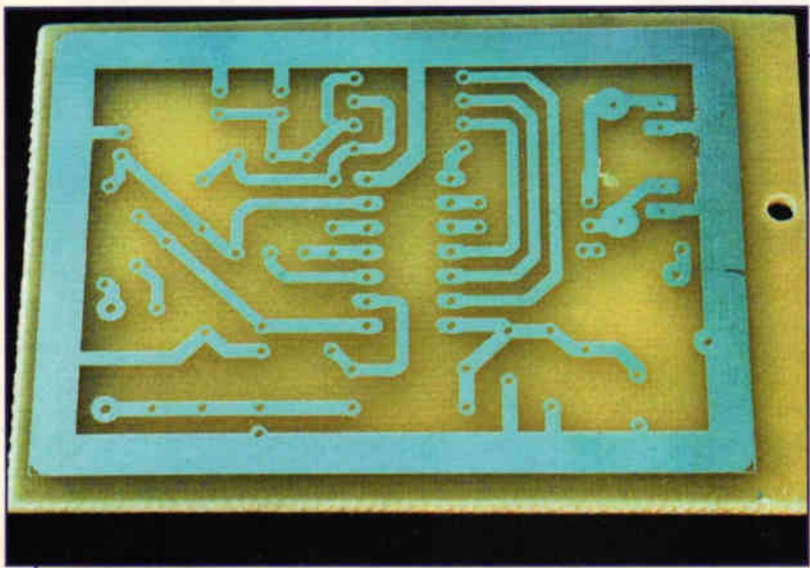

Fig. 2. Photograph of a small etched board made using triple printed artwork, shows ink jet printers can produce usable artwork images.

The following section assumes the use of photo-resist coated printed circuit boards with positive artwork on transparent film. Artwork will be produced using an ink jet or laser printer. A suitable UV light source is then used to expose the photo-resist.

Artwork preparation

Today, most PCB designs are originated using computer software. This provides the possibility of cross-linking both schematic and PCB layout files to flag up and minimise differences between them.

Take care to add text for 'component side' and reversed text for 'copper side'. It should be placed just off the board and form part of the copper layer print. It is also useful to add 'component side' text to the legend print, **Fig. 1**.

Once your PCB design has been completed the copper layer should be printed onto UV transparent film. This master will be used to expose the photosensitive-coated PCB material.

I hand write in capitals 'Copper Side' as appropriate, on the artwork film, ensuring it can easily be seen when registering PCB and artwork, for the exposure.

For many years, I used a Hewlett Packard Deskjet 500C ink jet printer with overhead-projector transparency foils. Using '3M CG3460' transparencies with this printer produces a very good image, provided the foil was overprinted three times, **Fig. 2.**

I have seen artwork produced using an unknown Epson ink jet printer and Epson film that looked sufficiently dense with a single printing. However many, like me, who need a PCL capable printer, will use HP ink jet printers. In this case, my methods may prove useful.

When I first started using surface-mount components, I evaluated a number of film/ink combinations. I changed to Hewlett Packard transparency film C3832A, used with re-manufactured ink cartridges. I bought these from 'System Insight'[2]. This combination worked better, usually providing sufficient density after two print passes.

Both the 3M and HP foils include a white end label, clearly indicating the print side. This is essential when multiple print passes are needed.

Most recently I tried some Jetstar ink jet film, intended for Epson printers and bought from Mega Electronics[3]. This lacked any indication at all as to which side should be printed. However as with many photographic print papers, the print or emulsion side drags if a moistened thumb is applied to one corner.

Once identified I cut away a small portion of the bottom right-hand corner while the film was placed correctly in the printer to indicate how re- insert the film. Provided it is kept dry by storing in a warm location, this film with my ink produces excellent and dense images, using just one or at most two passes.

Double/triple printing

To accept ink from an ink jet printer, the overhead-projector transparency film has to be pre-treated on one side in manufacture. Some makers clearly indicate which side is supposed to take ink. If not, usually this side will exhibit either a softer finish which 'drags' a moistened finger. Alternately, one surface will feel much rougher to the touch.

Most films print with adequate density for text, but PCB designs require dense coverage of larger areas. When fully dried and held close to a light for inspection, variations in print density may be seen, requiring another print pass to become acceptable.

The UV light used to expose photosensitive resist, easily penetrates any location not covered by visibly opaque ink. Such locations are most noticeable at the peaks of a roughened film surface. At best this results in many tiny pinholes in the etched copper tracks.

Provided you are consistent when inserting your film into the printer you will find most ink jet printers are remarkably repeatable. While great care reinserting the film is needed, provided the ink is fully dried, three print passes can be used with negligible blurring of the final artwork, Fig. 2.

My printer needs some help with paper handling. It has a spring-loaded sideways locating guide bar for the left top third of the film only. However a judiciously added spring clip, to control the left bottom third of the film, proves sufficient to triple print down to micro-SOIC size pads.

To fully dry the ink, I suspend the printed film over the warm air emerging from my monitor for at least 15 minutes before re-printing.

In the winter months, to avoid film shrinkage when drying the ink for a second pass, the pack of unprinted film is stored overnight in a warm location. If the film is not properly pre-dried, you can find tiny errors, negligible at the top but increasing toward the bottom of the page. These are sufficient to spoil the artwork when double or triple printing.

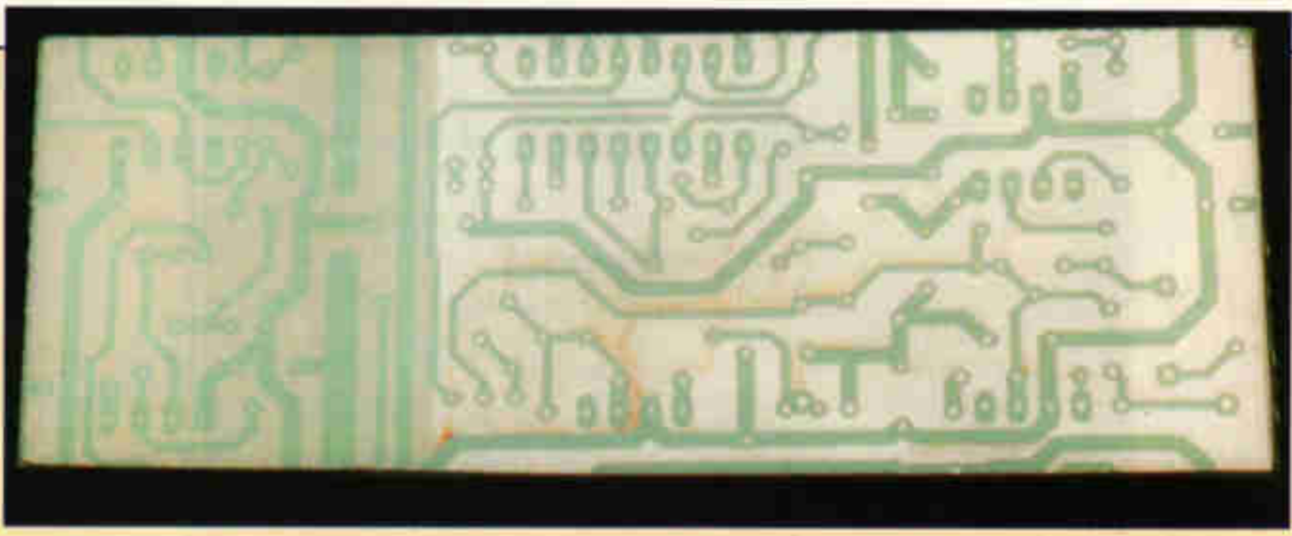

Fig. 3. Test strip made using 4, 8 and 12 minute exposures was developed but not etched. At 4 minutes (left) the resist was not properly exposed. Examining the original board with a times six magnifying glass, almost no difference between the 8 minutes (centre) and 12 minutes (right) exposures was visible.

Photoresist exposure

Most component distributors supply ultra-violet-exposure units, with prices starting from £90. Essentially these are just a small box containing two or more UV tubes, a timer, a glass window and padded lid.

With these, the artwork is pre-registered over the photosensitive PCB material then both are placed together, artwork down, onto the glass window. The closed lid retains their position and constrains the UV light.

More expensive UV units reverse this arrangement by having their tubes in the lid and a padded base. This makes for easier alignment of PCB material and artwork. These types usually provide a larger working area and prices start around £400.

More elaborate models are also available. These use a vacuum hold down method for artwork and PCB, which enables very narrow tracks to be printed. Some versions provide simultaneous exposure for double-sided boards.

Assuming a suitable light source that produces UV-A is available and you only occasionally make a PCB, a variation of the contact printing method is possible. This method has long been used for photographic prints.

The lamp is mounted downwards facing, above your work, in a desk stand. The artwork and photosensitive PCB are maintained in close contact, in a photographic contact print frame.

I prefer this method to using a conventional light box. It allows flexible working – especially when exposing two sided boards and test strips.

Most easily-obtained glass attenuates ultra violet light, but some plastics, e.g. UV transmitting Acrylic or Perspex attenuates much less. But take care, most easily-obtained Acrylic plastic sheets incorporate UV stabilisers. These attenuate UV even more than does window glass, extending your exposure time.

If you have a suitable UV light source, this method costs almost nothing to arrange, but do take proper care. Because the light source emits strong UV at around 400 nanometre, appropriate safety precautions are essential. I always vacate the room while my light is on.

If you do not already have a lamp, obtaining a suitable light source may prove more difficult. Problems resulting from using the original halogen 'white-light' desk lamps resulted in legislation prohibiting almost all lamps from emitting UV light. You will find most lamps are now marked as 'UV Blocked'.

For a one-off trial, even simpler methods can be used. Some years ago, when no UV source was available and the work could not wait, I recall making a satisfactory exposure using sunlight. The sensitised PCB and artwork were simply left under a piece of glass for a few minutes outdoors on a sunny day.

Test exposures

Whichever method is used to expose your artwork, the exposure used should be determined experimentally.

Compared to photographic materials, photo-resist has a wide latitude. Because developing can be done in normal room lighting, under or overexposure is easily compensated by increasing or decreasing developing time. Remove the board when visibly fully developed.

This is not difficult. Once a ball-park exposure has been decided for a batch of PCB materials, that exposure can be used with little change for that batch. Although warnings are printed on each pack about storage and shelf life, I have used similar exposures on a batch of material after a year in storage.

When making a trial exposure for a new delivery it is important to use your 'standard' conditions for the UV light source and development. Standard time for many developers is two minutes at 20°C, but some need less time.

Depending on your UV unit and the glass window used, typical exposure times will range from some four to twelve minutes. For a new delivery of Fotoboard from Mega[3], I made a test strip using four, eight and twelve minutes, **Fig. 3.**

Using spare material cut from one board, I removed the protective film and exposed for four minutes using scrap artwork. After four minutes one third of this material was covered by a piece of thin black card and the remainder exposed for a second four minutes. The card was moved to now cover two thirds and exposed for the final four minutes.

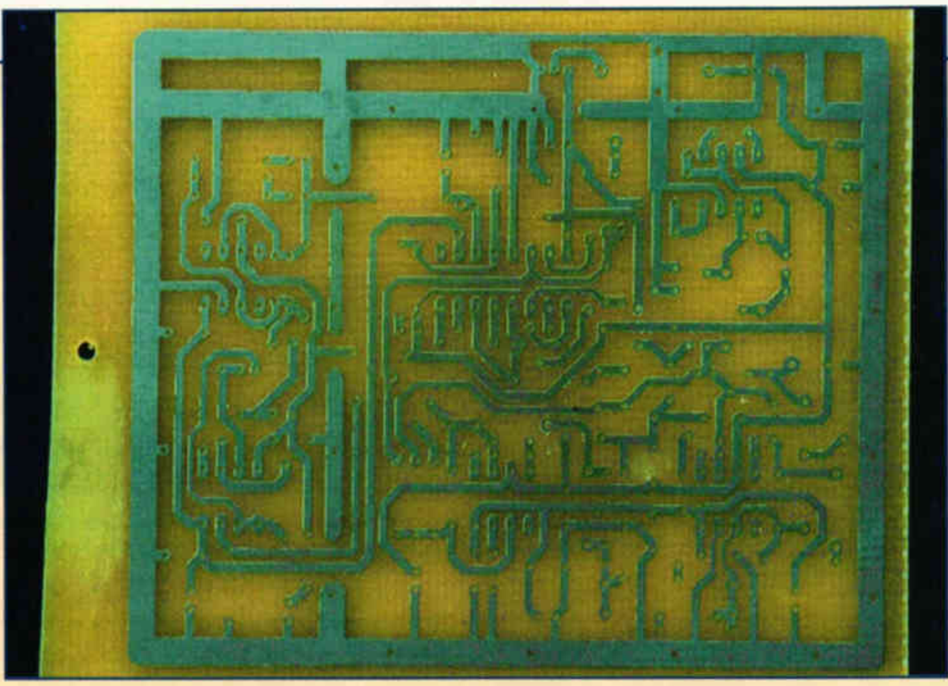

Fig. 4. This final circuit board was made from the board that provided the material for my test strip. It was exposed for 8 minutes.

Developed for exactly two minutes at 20°C then washed under cold running water, the board was dried and examined. If it is underexposed, an image may be seen but the copper will remain coated with a thin layer of resist. If overexposed too much resist will have been removed so the image will appear thin and washed out.

Correctly exposed, the image should show good contrast, with a visibly dense resist covering the wanted tracks, but no resist remaining elsewhere.

With all copper still covered by a thin layer of resist, the four minutes exposure clearly was not sufficient. Eight minutes looked perfect and the twelve-minute exposure was not too long. This batch of boards was then exposed for eight minutes.**Fig. 4.**

Developing the board

PCB development is extremely simple. The material has a wide latitude both for time and temperature. Because development can be done safely by inspection under normal room lighting, slightly longer or shorter time can be used to compensate for exposure time and developer temperature.

For occasional use, Seno supplies a universal PCB developer, SN110, contained in an applicator. The applicator sponge is simply wiped across the surface of your PCB. This combines a safe working method and a two-year shelf life.

Most materials and developers have standardised on two minutes and 20°C. Recently though, some much quicker developing PCB resist has been supplied. For this, the company Mega recommends diluting its developer with an equal volume of water.

Do not use metal containers. To develop a board I use a small A5 size plastic photographic developer tray. This floats in a larger tray containing water, as a water bath. This water bath can be used to raise developer temperature in the winter or lower its temperature in the summer, as required.

As part of my standard routine, I apply gentle developer agitation by rocking the developer tray in its water bath. This agitation ensures a constant supply of fresh developer to the work, minimising uneven development of any large exposed areas.

Some commercial developers are based on a weak solution of caustic soda. Regardless of make, for safety, wear protective gloves and use plastic tongs to immerse and remove your board from the developer tray.

A PCB developer works by dissolving or removing the exposed, unwanted areas. If no agitation is used these areas become covered in stale developer, prolonging the required developing time.

With some PCB resists/developers, you may find it preferable to remove the board for a pre-wash under cold running water, when two thirds of the developing time has elapsed. Then return the pre-washed board to complete its development.

Etching

Etching is perhaps the simplest process for the amateur board maker. The etchants used are corrosive, can stain your hands or your clothes. Wear plastic gloves, handle with care and follow your supplier's precautions.

The most easily available etchant is a solution of ferric chloride in water. This produces an acid solution. When supplied full strength at 45 Baumé or a specific gravity around 1.43, it should be diluted by adding 30% water, before use.

Ferric-hydroxide liquid is initially a red brown and its etching efficiency improves after initial use. The etchant then changes to a muddy brown mixture of ferric and ferrous hydroxide.

When completely, exhausted it changes to a dark green solution with a black precipitate at the bottom. Before disposal, any remaining acid can be neutralised by slowly adding household washing soda crystals. When effervescence ceases, the etchant has been neutralised.

For best results, most etchant should be used at 40°C. With minimal agitation, etching then takes some twelve to fifteen minutes.

The Seno 'etch in a bag' provides all needed equipment and instructions for safe usage. Other methods will need more care.

Proprietary 'bubble-etch' tanks are designed to provide safe handling and economic etching. Injecting air into the etchant provides both agitation and the free oxygen needed to etch copper. These bubble tanks work well but may be too expensive for occasional use.

A minimal cost method – one that I have used for many years – involves a high-density plastic breakfast cereal storage container from a supermarket. Its securely fitting lid ensures freedom from handling splashes and safe storage of etchant.

Two ex ice-cream containers, one inside the other, provide an insulated water bath in which to use and store the cereal container of etchant.

I find my cereal container holds etchant sufficient for boards up to 160 by 120mm, with the board suspended vertically in the solution. I drill a 3mm hole along one longer side and use a short length of 2mm enamelled-copper wire as a hook.

To ensure initial 'wetting' of the board surface, I raise and lower the board a few times. This agitates and drags air into the etchant.

Use only plastic containers and tools when using or storing etchant. For safety avoid using metal or glass. The only exception is my enamelled copper wire PCB supporting hook.

Suspending the board vertically in the etchant provides good etching with acceptable undercut except when using very fine track widths. Bubble agitation would reduce undercut, but tracks down to 0.5mm do not need bubbles.

If bubbles are desired, a small fish tank pump with plastic piping connecting to an air diffusing stone submerged in the etchant, could be used.

With the etchant container in position I fill the water bath with hot but not boiling water. This heats the etchant and maintains working temperature sufficient to etch a few boards.

Washing

When the board is fully etched, I hold is by its copper wire hook then pre-wash it by dipping it in another ex ice-cream container, half filled with clean cold water. This removes sufficient etchant to permit a visual inspection, followed by a final wash in cold running water.

When dry the board is ready to be drilled and trimmed to size.

Trimming a board to size

Almost any convenient hack saw and file will suffice. All edges can be finished by hand linishing the board on a 100 grit abrasive-paper covered flat surface.

Drilling your PCB

Most component holes are best drilled 0.8mm. In principle any drilling method can be used but small drills are easily broken using a power drill or stand-drilling machine.

High-speed steel drills blunt extremely quickly when drilling FR4 fibreglass PCBs. The more expensive – and more easily broken – tungsten carbide drills seem to stay sharp forever*. To reduce drill breakage, your PCB should be supported on a scrap of plywood or PCB material.

Small hand-held drill motors are much easier to use than is a large power drill. For many years I regularly used a low cost 12V 'Reliant' drill[1], powered from 8V to reduce its speed. This allows time for the drill to almost self-centre itself in the etched pad, before drilling the hole.

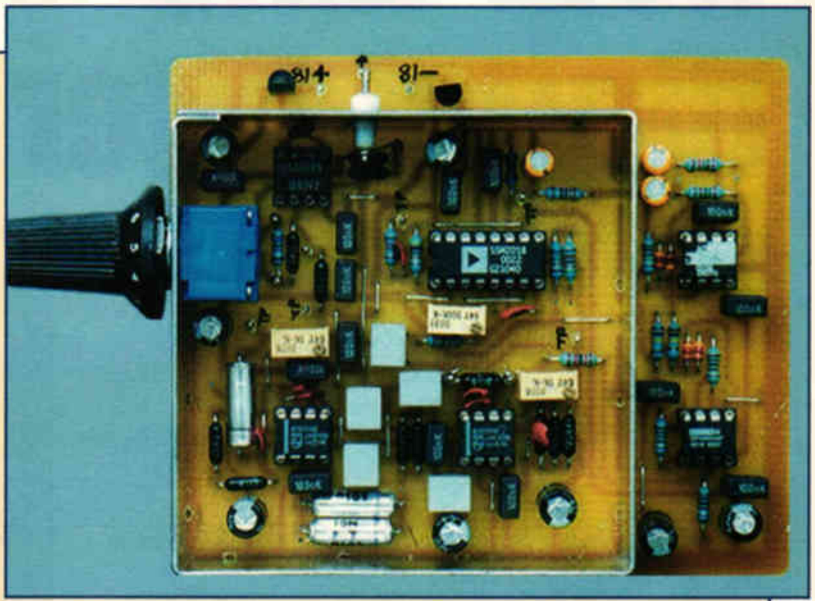

Fig. 5. Circuit assembled using the Fig. 4 printed board. This very low distortion 1kHz oscillator was specially developed to measure sound distortions caused by capacitors. Full design and construction details, together with capacitor test results, will be featured in future articles.

Resist removal

The resist is best left in place until the board is to be assembled. It does not have to be removed. Left in place it helps to 'flux' the copper, **Fig. 5.**

However I prefer to remove this resist, to facilitate board inspection. Commercial resist removers can be used, but I use methylated spirits applied with a rag. The board is then finally cleaned and polished using water with a dab of household abrasive pumice cleaning powder, thoroughly washed and left to dry.

Double sided boards

This article has deliberately avoided discussing two sided PCBs. These – together with a much improved, very low cost, drilling method – will be covered in my next article. ■

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4. Art Supplies, http://www.artsuppliesonline.com
5. Silverprint Company, http://www.silverprint.co.uk
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*They do seem to go on forever, but I find that after about 50 holes, although not blunt, tungsten carbide drills start to push the copper slightly around the edges of the hole. There's a special green whet stone for carbide drills. Normally, the rake of a drill is curved, but such small drills work effectively with a flat rake. Just make sure that you keep the point in the middle, i.e. make the two flats identical. Ed.

Real-time digital filter

RTDF – a unique, integrated hardware and software system for designing, downloading and running very high performance filters in real time. Available only from *Electronics World.*

The RTDF 1.5 is a unique real-time audio-bandwidth digital filter with infinitely adjustable characteristics – all available at the click of a button. Filter design and execution is accomplished in two easy steps. In fact, you can have a no-compromise filter up and running within seconds.

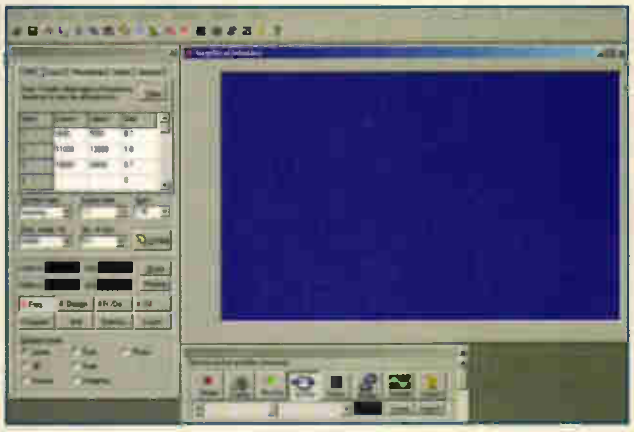
If you want to change the filter completely – low-pass, band-pass, high-pass or arbitrary – just repeat the two steps.

The RTDF filter system includes hardware based on an advanced digital signal processor, low-level firmware that implements the filtering operations, and a high-level PC-based software interface that designs the filter according to your requirements. Once a filter is designed, the software interface is used to download the filter to the hardware system via a serial link, where it is executed on demand.

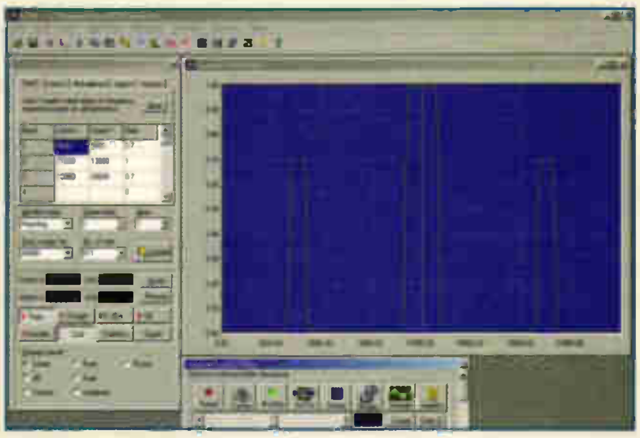
You don't need to know about digital signal processing theory or the mathematics associated with digital-filter design. But if you're a filter expert, you won't find yourself restricted by

RTDF - key features

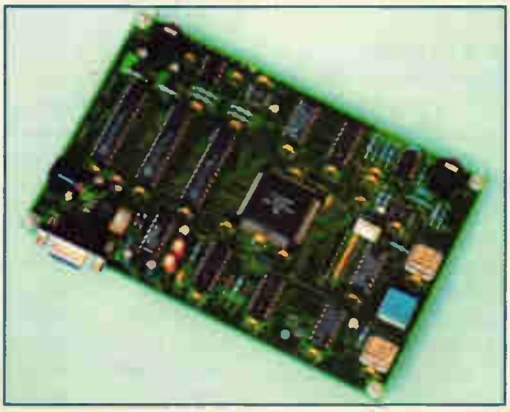
- Runs under Windows 95, 98 or ME
- Generates FIR filters with a maximum of 1024 coefficients.
- Multiple pass, stop or arbitrary filters.
- Lower –3dB frequency 3.7Hz at 48kHz sample rate and 1.2Hz at 12kHz sample rate.
- Filter operates in single or dual channel modes.
- Import mode – ASCII import of any frequency response.
- Hardware module holds up to 16 filters, instantly selectable with one mouse click.
- Zero-phase distortion in the pass, transition and stop bands, ignoring input and output coupling.
- Choice of rectangular, Bartlett, Hamming, Hanning, Blackman or Kaiser Windows.
- Virtual control panel allowing run-time changes to filter gain and sampling rate.
- Includes frequency and time domain plots of filter performance.
- Frequency response plotted as linear, dB, square, root, real, imaginary or phase.
- Impulse, frequency and phase response exportable in a variety of formats (dB, power etc) as ASCII files for incorporation into standard spreadsheets.
- 18-bit resolution in single, 16-bit in dual-channel mode.
- Normal or turbo speed, software selectable.
- User selectable sample rates of 48kHz, 24kHz, 16kHz, 12kHz, 9.6kHz, 8kHz, 6kHz, 4.8kHz, 4kHz, 3.2kHz or 3kHz.
- Maximum input and output level 4V pk-pk



Step 1 – Enter the characteristics of your filter, such as cut-off points and sharpness, in the Filter Design Interface Window on the left of the display.



Step 2 – Click on the Update button to view your result in graphical form, download it to the hardware module and run the filter from the hardware control panel – done!



Filter hardware: a DSP56002 board with RAM and 16/18bit oversampling analogue converters for stereo i/o at up to 48kHz sampling.

For more information, visit: http://www.umist.ac.uk/dias/pag/rtdf.htm

the easy-to-use interface. If you want to do it the hard way, you can even design your filter in long-hand then download the filter's frequency response as an ASCII file to the RTDF's control program!

The RTDF is a total filter solution. Due to its flexibility, it is particularly well suited to processing audio signals in real time. High-quality analogue signal conditioning and a dual-channel 16/18-bit resolution analogue-to-digital converter and digital-to-analogue converter provide a resolution sufficient for the most demanding applications.

In short, the RTDF brings the power of digital signal processing to any audio-bandwidth domain that requires high-performance electronic signal filtering. Applications include sensor linearisation, audio signal processing, signal analysis, vibration analysis, education and research in electrical, electronic and other physical sciences.

Low-pass, high-pass, multiple band-stop / band-pass filters may be combined to produce very complex filters for frequencies up to 24kHz.

The software can accept measured responses to define a filter template. This can be used for measurement equalisation or to search out signal signatures in noisy environments.

Since the filters are implemented using a symmetrical finite impulse response (FIR) method, no phase distortion occurs in the filtered signal – no matter how sharp the filter is. Because the processing module is so fast, it is possible to design filters with responses far beyond what is possible with traditional analogue techniques.

Windows software

The control program runs under Windows and provides a user-friendly filter-design tool that de-mystifies the process of specifying the filter. The filter design process simply becomes one of describing the desired frequency response.

The design package indicates the response that will be produced and any deviations from that specified. User designs may be stored for re-use and actual responses may be entered from measurements for simulation or equalisation purposes. Once designed, filters are calculated and downloaded to the hardware within seconds.

The software designs the filter according to the user's specifications. The filter is expressed as a set of FIR, zero-phase distortion coefficients or taps. Collectively, the coefficients of a filter are known as the *impulse response*.

The system's gain and sampling rate can be adjusted while the filter is running and you can switch instantaneously between a filtered or non-filtered signal.

Most importantly, the software includes a flexible filter design section. A window displays the frequency or impulse response of the realised filter in various formats. A hardware control section downloads a filter and provides for general communication with the filter module.

The DSP module

The hardware DSP module connects to the PC via a standard COM port using the cable supplied.

The 16/18-bit over-sampling dual-channel sigma-delta a-to-d and d-to-a conversion system can easily be set to any one of eleven sample rates, ranging from 48kHz down to 3kHz.

So how fast can the filter operate, and how many filter coefficients can it practically employ? The maximum number of taps at the highest frequency range of 24kHz, in single channel mode, is 527. At this range, the system is sampling at 48kHz. This represents a very sharp filter indeed.

Using a frequency range of 12kHz – sample rate of 24kHz – in single-channel mode, the system can operate a filter with a maximum of 937 taps. At any range below this, it can operate a filter with a maximum of 1024 taps. The performance of a 1024-tap filter is so extremely sharp that it is quite unlikely that you would ever need to use it.

In dual-channel mode, the maximum number of taps permissable at the highest frequency range of 24kHz is 191. With a frequency range of 12kHz , it is 397. Full details concerning tap numbers, frequency ranges and operating modes are provided with the on-line documentation. ■

Minimum system requirements

100 MHz PC running Windows' 95, 98 orME
SVGA display (800X600 pixels) or higher
CD ROM drive
10 Mbytes of free hard disc space
Serial port, capable of 19200 bit/s

System includes:

- Filter DSP board
- Windows filter design software on CD plus demonstration-filters
- Fully-worked help files – featuring tutorial
- Installation instructions
- Analogue i/o cables
- RS232 COM port download cable
- Power supply

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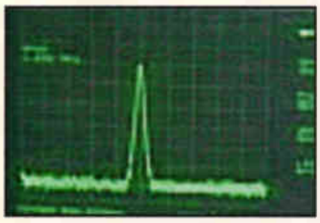

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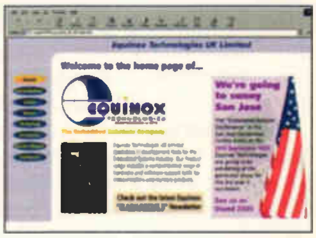

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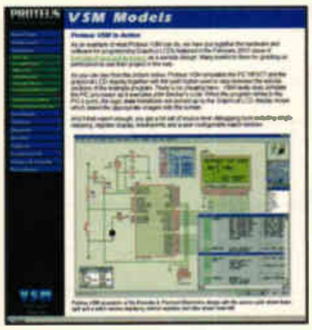

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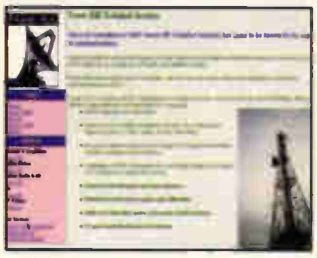

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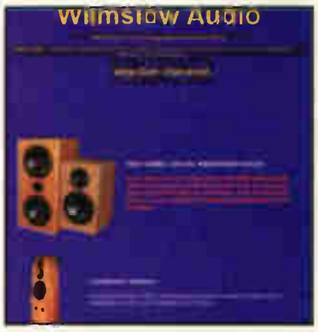

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HP Network Analyser type 8407A + 8412A + 8601A - 100Kc/s - 110Mc/s - £500 - £1000.
HP 8410-A-B-C Network Analyser 110Mc/s to 12 GHz or 18 GHz - plus most other units and displays used in this set-up - 8411a-8412-8413-8414-8418-8740-8741-8742-8743-8746-8650. From £1k.
Racal/Dana 9301A-9302 RF millivoltmeter 1.5-2GHz - qty in stock £250-£400.
Racal/Dana Modulation Meter Type 9008 9009 8Mc/s - 1.5GHz - £150/£250 - 9009A £350.
Marconi Microwave 6600A 1 sweep osc., mainframe with 6650PI - 18-26.5 GHz or 6651 PI - 26.5-40GHz-£750 or PI only £600. MF only £250.
Gould J3B test oscillator + manual - £150.
Barr & Stroud Variable filter EF3 0.1Hz-100Kc/s + High Pass + Low Pass - £150 other makes in stock.
Racal/Dana 9300 RMS voltmeter - £250.
HP 8750A storage normalizer - £400 with lead + S.A. or N/A
Marconi mod meters type TF2304 - £250 - TF2305 - £1,000.
Racal/Dana counters-99904-9905-9906-9915-9916-9917-9921-50Mc/s-3GHz - £100 - £400 - all fitted with FX standards.
HP180TR. HP181T, HP182T mainframes £300 - £500
HP432A-435A or B-436A power meters + powerheads to 60GHz - £150 - £1750 - spare heads available.
HP3586A or C selective level meter - £500.
HP86222A+B Sweep PI-.01-2.4GHz + ATT £1000-£1250
HP86290A+B Sweep PI-2-18GHz - £1000 - £1250.
HP8620C Mainframe - £250. IEEE £350.
HP8165A Programmable signal source - 1MHz - 50Mc/s - £1k.
HP3455/3456A Digital voltmeter - £400.
HP5370A Universal time interval counter - £1k.
HP5335A Universal counter - 200Mc/s-£1000.
TEKTRONIX 577 Curve tracer + adaptors - £900.
TEKTRONIX 1502/1503 TDR cable test set - £400.
HP8699B Sweep PI YIG oscillator .01 - 4GHz - £300. 8690B MF-£250. Both £500.
Dummy Loads & Power att up to 2.5 kw. FX up to 18GHz - microwave parts new and ex equip. - relays - attenuators - switches - waveguides - Yigs - SMA - APC7 plugs - adaptors etc. qty. in stock.
B&K Items in stock - ask for list.
Power Supplies Heavy duty + bench in stock - Farnell - HP - Weir - Thurlby - Racal etc. Ask for list. Large quantity in stock, all types to 400 amp - 100Kv.
HP8405A Vector voltmeter - late colour - £400.
HP8508A Vector voltmeter - £2500.

LIGHT AND OPTICAL EQUIPMENT

Anritsu ML93A & Optical Lead Power Meter - £450.
Anritsu ML93B & Optical Lead Power Meter - £500.
Power Sensors for above MA96A - MA98A - MA914
Battery Pack MZ95A.
Anritsu MW97A Pulse Echo Tester
PI available - MH914C 1.3 - MH915B 1.3 - MH913B 0.85 - MH925A 1.3 - MH929A 1.55 - MH925A 1.3GI - MH914C 1.3SM - £500 + one P.I.
Anritsu MW98A Time Domain Reflector.
PI available - MH914C 1.3 - MH915B 1.3 - MH913B 0.85 - MH925A 1.3 - MH929A 1.55 - MH925A 1.3GI - MH914C 1.3SM - £500 + one P.I.
Anritsu MZ100A E/O Converter.
+ MG912B (LD 1.35) Light Source + MG92B (LD 0.85) Light Source £350.
Anritsu MZ118A O/E Converter.
+MH922A 0.8 O/E unit + MH923 A1.3 O/E unit £350.
Anritsu ML96B Power Meter & Charger £450.

Anritsu MN95B Variable Att. 1300 £100.
Photo Dyne 1950 XR Continuous Att. 1300 - 1500 £100.
Photo Dyne 1800 FA. Att £100.
Cossor-Raytheon 108L Optical Cable Fault Locator 0-1000M 0-10kM £200.
TEK P6701 Optical Converter 700 MC/S-850 £250.
TEK OF150 Fibre Optic TDR – £750.
HP81512A Head 150MC/S 950-1700 £250.
HP84801A Fibre Power Sensor 600-1200 £250.
HP8158B ATT OPT 002+011 1300-1550 £300.
HP81519A RX DC-400MC/S 550-950 £250.
STC OFR10 Reflectometer – £250.
STC OFSK15 Machine jointing + eye magnifier – £250.

MISCELLANEOUS ITEMS

HP 4261 LCR meter – £650.
HP 4274 FX LCR meter – £1,500.
HP 3488 Switch Control Unit + PI Boards – £500.
HP 75000 VXI Bus Controllers + E1326B-DVM-quantity.
HP 83220A-GSM DCS/PCS 1800-1990MC/S convertor for use with 8922A – £2,000.
HP 1630-1631-1650 Logic ANZ's in stock.
HP 8754A Network ANZ 4-1300MC/S + 8502A + cables – £1,500.
HP 8754A Network ANZ H26 4-2600MC/S + 8502A + Cables – £2,000.
HP 8350A Sweeper MF + 83540A PI 2-8.4GHz + 83545A PI 5.9-12.4GHz PI 3 – £3,500.
HP MICROWAVE TWT AMPLIFIER 489A 1-2GHz-30DB – £400.
HP PREAMPLIFIER 8447A 0.1-400MC/S – £200. Dual – £300.
HP PREAMPLIFIER 8447D 0.01-1.3GHz – £400.
HP POWER AMPLIFIER 8447E 0.01-1.3GHz – £400.
HP PRE + POWER AMPLIFIER 8447F 0.01-1.3GHz – £500.
HP 3574 Gain Phase Meter 1Hz-13MC/S OPT 001 Dual – £400
MARCONI 2305 Modulation Meter-50kHz-2.3 GHz – £1,200.
MARCONI 2610 True RMS Meter – £450.
MARCONI 893B AF Power Meter opt Sinad filter – £250-£350.
MARCONI 6950-6960B Power Meters + Heads – £400-£800.
MARCONI SIGNAL SOURCE-6055-6056-6057-6058-6059 – FX Range 4-18GHz – £250-£600.
RACAL 1792 COMMUNICATION RX – £500 early – £1,000 – late model with back lighting and both test.
RACAL 1772 COMMUNICATION RX – £400-£600.
TEK MODULE MAINFRAMES – TM501-502-503-504-506-TM5003-5006.
TEK PI 5010-M1 – Prog Multi Interface – £250. FG Prog 20MC/S Function Gen – £400 – S1 Prog Scanner – £250 – DM Prog DMM – £400.
TEK 7000 OSCILLOSCOPE MAINFRAMES – 7603-7623-7633-7834-7854-7904-7904A-7104 – £150-£1,000.
TEK 7000 PI's – 7A11-7A12-7A13-7A18-7A19-7A22-7A24-7A26-7A29-7A42-7B10-7B15-7B53A-7B80-7B85-7B92A-7D15-7D20.
TEK 7000 – 7S11-7S12-7S14-7M11-S1-S2-S3A-S4-S5-S6-S51-S53-S54.
HP POWER SUPPLIES – 6621A-6623A-6624A-6632A-6652A. Qty available. Also 6000 types £POA.
WE KEEP IN STOCK HP and other makes of RF Frequency doublers which when fitted to the RF output socket of a S/Generator doubles the output frequency EG.50-1300MC/S to 50-2600MC/S price from £250 – £450 each.

SPECTRUM ANALYZERS

HP 3580A 5Hz-50kHz – £750.
HP 3582A Dual 0.2Hz-25.5kHz – £1,500.
HP 3585A 20Hz-40MC/S – £3,500.
HP 3588A 10Hz-150MC/S – £7,500.
HP 8568A 100Hz-1.5GHz – £3,500.
HP 8568B 100Hz-1.5GHz – £4,500.
HP 8590B 9KC/S-1.8GHz – £4,500.
HP 8569B 10MC/S-0.01-22GHz) – £3,500.
HP 3561A Signal Analyzer 15Hz-50kHz – £400.
TEK492 50kHz-21GHz OPT 2 – £2,500.
TEK492P 50kHz-21GHz OPT 1-2-3 – £3,500.
TEK492AP 50kHz-21GHz OPT 1-2-3 – £4,000.
TEK492BP 50kHz-21GHz – £3,000-£4,000.
TEK495 100kHz-1.8GHz – £2,000.
HP 8557A 0.01MC/S-350MC/S – £500 + MF180T or 180C – £150 – 182T – £500.
HP 8558B 0.01-1500MC/S – £750 – MF180T or 180C – £150 – 182T – £500.
HP 8559A 0.01-21GHz – £1,000 – MF180T or 180C – £150 – 182T – £500.
HP 8901A AM FM Modulation ANZ Meter – £800.
HP 8901B AM FM Modulation ANZ Meter – £1,750.
HP 8903A Audio Analyzer – £1,000.
HP 8903B Audio Analyzer – £1,500.

MARCONI 2370 SPECTRUM ANALYZERS – HIGH QUALITY – DIGITAL STORAGE – 30Hz-110MC/S Large qty to clear as received from Gov – all sold as is from bulk complete or add £100 for basic testing and adjustment – callers preferred – pick your own from over 40 units – discount on qtys of five.
A EARLY MODEL GREY – horizontal alloy cooling fins – £200.
B LATE MODEL GREY – vertical alloy cooling fins – £300.
C LATE MODEL BROWN – as above (few only) – £500.

OSCILLOSCOPES

TEK 465-465B 100MC/S + 2 probes – £250-£300.
TEK 466 100MC/S storage + 2 probes – £200.
TEK 475-475A 200MC/S-250MC/S + 2 probes – £300-£350.
TEK 2213-2213A-2215-2215A-2224-2225-2235-2236-2245-60-100MC/S – £250-£400.
TEK 2445 4ch 150MC/S + 2 probes – £450.
TEK 2445A 4ch 150MC/S + 2 probes – £600.
TEK 2445B 4ch 150MC/S + 2 probes – £750.
TEK 468 D.S.O. 100MC/S + 2 probes – £500.
TEK 485 350MC/S + 2 probes – £550.
TEK 2465 4ch-300MC/S – £1,150.
TEK 2465A 4ch-350MC/S – £1,550.
TEK D.S.O. 2430A -150MC/S + 2 probes – £1,750.
TEK D.S.O. 2440 -300MC/S + 2 probes – £2,000.
TEK TAS 475-485 -100MC/S-20MC/S-4 ch + 2 probes – £900-£1.1K.
HP1740A – 100MC/S + 2 probes – £250.
HP1741A – 100MC/S storage + 2 probes – £200.
HP1720A – 1722A - 1725A – 275MC/S + 2 probes – £300-£400.
HP1744A – 100MC/S storage large screen – £250.
HP1745A – 1746A – 100MC/S – large screen – £350.
HP54100A – 1GHz digitizing – £500.
HP54200A – 50MC/S digitizing – £500.
HP54201A – 300MC/S digitizing – £500.
HP54111D – 1GHz digitizing – £1,000.

MICROWAVE COUNTERS – ALL LED READOUT

EIP 351D Autohet 20Hz-18GHz – £750.
EIP 371 Micro Source Locking – 20Hz-18GHz – £850.
EIP 451 Micro Pulse Counter – 300MC/S-18GHz – £1K.
EIP 545 Microwave Frequency Counter – 10Hz-18GHz – £1.2K.
EIP 548A Microwave Frequency Counter – 10Hz-26.5GHz – £1.6K.
EIP 575 Microwave Source Locking – 10Hz-18GHz – £1.2K.
EIP 588 Microwave Pulse Counter – 300MC/S-26.5GHz – £1.4K.
SD 6054B Micro Counter – 20Hz-24GHz – SMA Socket – £800.
SD 6054D Micro Counter 20Hz-18GHz – N Socket – £700.
SD 6054D Micro Counter 800MC/S-18GHz – £600.
SD 6246A Micro Counter 20Hz-26GHz – £1.2K.
SD 6244A Micro Counter 20Hz-4.5GHz – £400.
HP5352B Micro Counter OPT 010-005-46GHz – new in box – £8K.
HP5340A Micro Counter 10Hz-18GHz – Nixey – £500.
HP5342A Micro Counter 10Hz-18-24GHz – £800-£1K – OPTS 001-002-003-005-011 available.
HP5342A + 5344S Source Synchronizer – £1.5K.
HP5345A 500MC/S 11 Digit LED Readout – £400.
HP5345A + 5354A Plugin – 4GHz – £700.
HP5345A + 5355A Plugin with 5356A 18GHz Head – £1K.
HP5385A 1GHz 5386A-5386A 3GHz Counter – £1K-£2K.
Racal/Dana Counter 1991-160MC/S – £200.
Racal/Dana Counter 1992-1.3GHz – £600.
Racal/Dana Counter 9921-3GHz – £350.

SIGNAL GENERATORS

HP8640A – AM-FM 0.5-512-1024MC/S – £200-£400.
HP8640B – Phase locked – AM-FM-0.5-512-1024MC/S – £500-£1.2K. Opts 1-2-3 available.
HP8654A – B AM-FM 10MC/S-520MC/S – £300.
HP8656A SYN AM-FM 0.1-990MC/S – £900.
HP8656B SYN AM-FM 0.1-990MC/S – £1.5K.
HP8657A SYN AM-FM 0.1-1040MC/S – £2K.
HP8660C SYN AM-FM-PM-0.01-1300MC/S-2600MC/S – £2K.
HP8660D SYN AM-FM-PM-0.01-1300MC/S-2600MC/S – £3K.
HP8673D SYN AM-FM-PM-0.01-26.5 GHz – £12K.
HP3312A Function Generator AM-FM 13MC/S-Dual – £300.
HP3314A Function Generator AM-FM-VCO-20MC/S – £600.
HP3325A SYN Function Generator 21MC/S – £800.
HP3326A SYN 2CH Function Generator 13MC/S-IEEE – £1.4K.
HP3336A-B-C SYN Func/Level Gen 21MC/S – £400-£300-£500.
Racal/Dana 9081 SYN S/G AM-FM-PH-5-520MC/S – £300.
Racal/Dana 9082 SYN S/G AM-FM-PH-1.5-520MC/S – £400.
Racal/Dana 9084 SYN S/G AM-FM-PH-.001-104MC/S – £300.

SPECIAL OFFERS

MARCONI 2019A SYNTHESIZED SIGNAL GENERATORS – 80KC/S-1040MC/S – AM-FM – £400 inc. instruction book – tested.
MARCONI 2022E SYNTHESIZED SIGNAL GENERATOR – 10KC/S-1.01GHz AM-FM – £500 inc. instruction book – tested.
R&S APN 62 LF Sig Gen 0.1Hz – 260 kHz c/w book – £250.

MARCONI 2383 S.ANZ 100Hz – 4.2 GHz. £2K
H.P RF AMP 8349A 2-20 GHz microwave. £2K.
H.P. RF AMP 8347A 100 kHz - 3GHz £1,500.
H.P. 8922 radio communication test sets.
G – H – M. options various. £2,000 - £3,000 each.
H.P. 4193A VECTOR IMPEDANCE METER + probe kit. 400 kHz. To 110 ML/S. £3,500.

H.P. 83220A – E GMS UNITS for above. £1,000 - £1,500.
WAVETECK SCLUMBERGER 4031 RADIO COMMUNICATION TEST SET. Internal Spectrum ANZ. £1,800 - £2,000.
ANRITSU MS555A2 RADIO COMM ANZ. To 1000MC/S. No C.R. tube in this model. £450.
TEK 2445A – 4CH – 150MLS SCOPE + New X1 + X10- probe. Instruction book. £500 each.

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