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DIRECT
INJECT,
COMPRESSION
UNIT AND
NOISE GATE



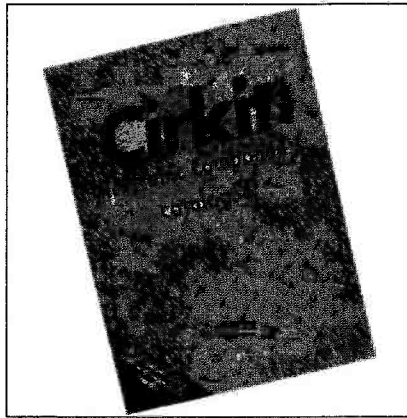
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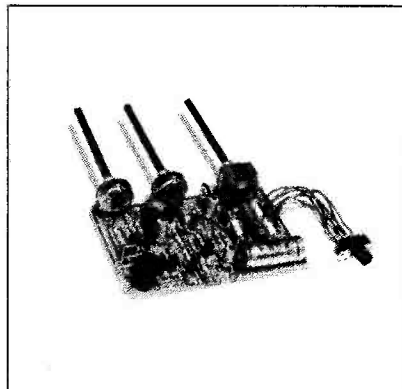
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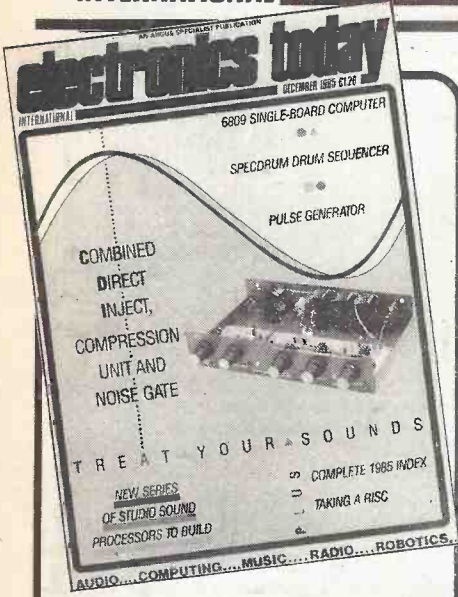
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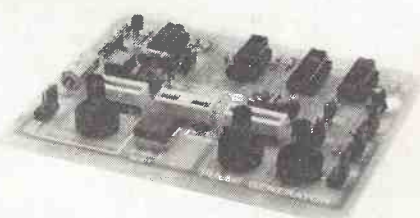
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We apologise for having to hold over the scheduled part of the Digital Sound Sampler. This has been due to circumstances beyond our control. We hope to bring you full constructional details next month.

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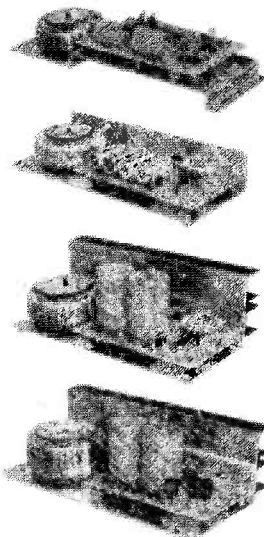
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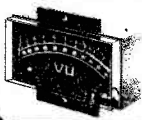
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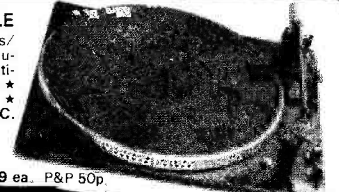
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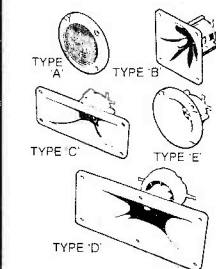


ADC Q4 mag. cartridge for above. Price £4.99 ea. P&P 50p

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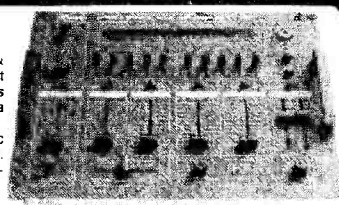
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DIGEST

'Electronic weapons being used against us', Greenham women claim

Women peace campers at Greenham Common claim they are being attacked with electronic weapons from within the base.

They believe that some form of electromagnetic wave or other signal is being directed at them and is responsible for a series of illnesses they have suffered over the past year.

Symptoms range from mild headaches and drowsiness to bouts of temporary paralysis and, in one case, an apparent circulatory failure which required emergency treatment. Women have also complained of sharp pains and problems with speech coordination. A team of doctors from the Medical Campaign Against Nuclear Weapons are compiling a report on the condition of the women affected.

The women first noticed a pattern of illnesses emerging late last year. They discounted food or water poisoning as a cause and started to suspect interference from inside the base. They found that women at different points around the camp appeared to have experienced similar symptoms at the same time, even when they were not in contact with one another.

They believe there is a deliberate intent to make life difficult for them and so drive them away. Some of the worst affected women now find it impossible to stay around Greenham for more than a short period of time.

Electronic weapons are known to have been used by security forces on a number of occasions. The Americans are reported to have used ultrasound to disorient and demoralise their enemies during the Vietnam war and a number of American police forces are believed to have carried out trials with infra-sound generators mounted on the back of trucks. The high intensity, low frequency pressure waves these produce are said to cause vomiting, nausea and a range of other disturbances and to induce fits in those who are subject to them. American medical groups have

protested against the proposed use of these weapons for urban riot control.

Microwave radiation is also believed to have been used as a weapon at various times. The most celebrated instance was the irradiation of the US Embassy in Moscow during the 1950s, '60s and '70s. It has never been made clear whether the Russians used the signal as a weapon or for surveillance, but a television documentary screened last year reported a high incidence of cancer amongst ex-Embassy staff and suggested that disorders of the blood and nervous system could also have been caused by the signal.

The women at Greenham Common suspect that more than one type or frequency of radiation is being used against them. They say that the symptoms vary from time to time and seem to reflect what takes place on the base. Large numbers of women have complained of sudden feelings of extreme tiredness shortly before major events such as the departure of a cruise missile convoy and on other occasions when their activities might have proved particularly awkward for the forces using the base.

ETI has carried out a number of tests around the base in cooperation with journalists from other organisations. Readings taken with a wide range signal strength meter showed marked increases in the background signal level near one of the womens' camps at a time when they claimed to be experiencing ill effects.

On another occasion previously low signal levels near the camp rose sharply when the women created a disturbance just outside the perimeter fence of the base. Whether this indicated an attempt to subdue the women by electronic means or merely the use of a radar surveillance system it is impossible to say.

The signal levels measured were well above normal background levels but still within official safety limits. However, there is evidence from a number of sources that low levels of electromagnetic radiation can have harmful effects, especially where exposure takes place over a long period of time.

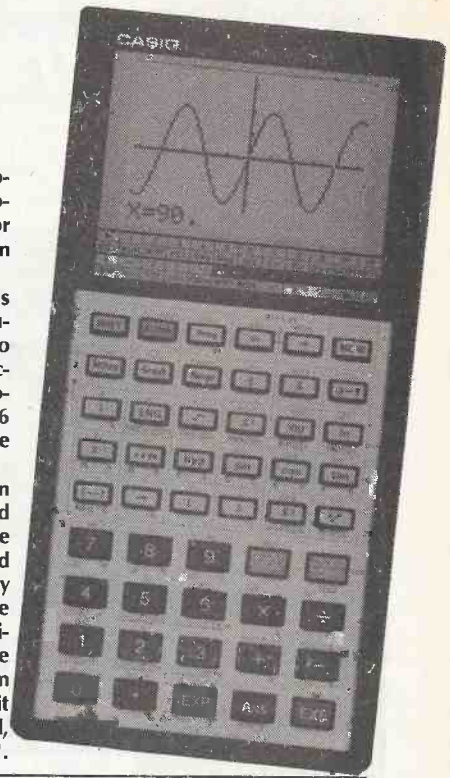
Ministry of Defence officials have denied that any form of electronic signal is being used against the women. Tests at the base are continuing.

A Graphic Display

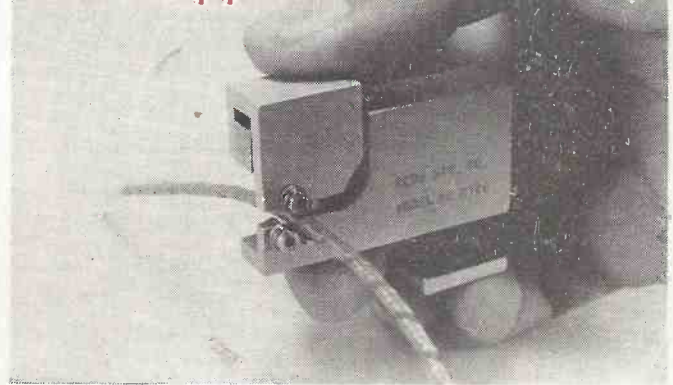
Casio Electronics have introduced a full-function programmable scientific calculator which draws graphs and charts on an integral LCD screen.

The hand-held FX7000G features a 35x52mm screen with a resolution of 63x95 pixels. It can also display up to 8 lines of 16 characters. It is capable of up to 422 programming steps, utilising 26 memories and up to 10 separate program areas.

Twenty algorithms are built-in to draw graphs of standard mathematical functions and the FX7000G can draw bar charts and plot points. The calculator, say Casio, will be 'unbeatable' for the correlation of experimental variables. The RRP is £99.95 and the FX7000G is obtainable from Casio Electronics Co Ltd, Unit Six, 1000 North Circular Road, London NW27JD, tel 01-450 9131.



Versatile Wire Strippers



From the US company Reon Manufacturing comes a new range of wire stripping tools designed for a variety of different types and thicknesses of equipment cable.

All the units are housed in the same casing and different wire diameters and sleeving materials are catered for by changing the cutters. Cutters will handle wire in diameters down to 0.025" and can also cope with extruded, high-temperature sleeving up to 9/32" in diameter.

The tools are designed for ease of use, a rotating blade being used to cut sleeving to a controlled depth and a gripper anvil removing the cut sleeve. Priced at around £42, further details should be obtained from Kern Electrical Components Ltd., 2 Albury Close, Battle Farm Industrial Estate, Reading, Berks RF3 1BD (0734-596368).

ETI Printed Circuit Board Service

Readers tiring of the apparently never-ending saga of the PCB service may console themselves with the thought that the magazine staff are exhausted by it too.

The lack of a PCB Service page this month will not go unnoticed. Our humblest apologies. The situation, is quite simply, that legal complications have delayed the start-up of the service. As anyone who has ever bought or sold a house will know, the law takes not only its course but its time. We are assured that the service will be on-stream within a matter of days. Please write to us for further information or wait until our next issue.

Dial M For Money

The figure in the stripes and spots is not, contrary to appearance, Spiderman with a dose of the measles. Nor is it Superman after emerging from an ultra-modern phone booth. It is (short pause for the intake of breath) — Digital Man, dubbed 'the dots-and-dashes figure' and currently parading as 'the star of British Telecom's nationwide Faraday Lecture tour, "Beyond the Telephone — Or Intelligent Network".' Or so it says in BT's publicity material.

Shown being cosseted by a bevy of lovely schoolgirls, Digital Man — although singularly lacking in eyes, ears, mouth or nostrils — is accompanying BT's Chief Executive of Technology, Mr. Bill Jones, as he makes his way about the country giving the 1985-86 series of Faraday Lectures.

The Faraday Lectures were inaugurated in 1924 by the Institute of Electrical Engineers to promote interest in their field. The IEE invites a major organisation each year to lecture on one aspect of the work of electrical engineers to an audience largely composed of school and college students. And jolly good fun they are, too (although not quite as fascinating as the annual Royal Society lectures).

For BT, only recently privatised and now threatened by the entry of Cable & Wireless offshoot, Mercury Communications, into the Telecoms' game, the Faraday Lectures are a heaven-sent opportunity for public relations and recruitment. 'Young people, who may be about to choose a career, will be a particularly important part of the audience,' says Bill Jones, noting that BT's aim is to 'stimulate a lasting interest in electronics and telecommunications'. Hence Digital Man, the NAND-gate incarnate. And hence BT's budget of £750,000 for the exercise.

This may look like a small fortune, but it's a trifling amount compared to BT's recently announced first quarter profit of £443 million before tax. With that



number of coins, you might think BT would start giving local calls away, like they do in a number of other countries.

But BT want more. In early October, they increased phone charges. In mid-October, they talked of putting them up again for domestic and small business users while reducing charges to the corporate users.

In between times it was revealed that they had introduced hidden price rises. In the shape, for example, of a charge to all those receiving consolidated bills who want to see a call-by-call analysis. Digital Man could provide such an analysis with one hand tied behind his back. But I guess he's too busy telling the world how wonderful BT are.

BT's future may be with Intelligent Networks, but the company itself seems like a most unintelligent network. It may need to look 'beyond the telephone' when Mercury flies on to the scene, happily connecting up its

'independent' network to BT's.

Could it be that the Oftel report (which has given Mercury the go-ahead to link-up with the existing telephone network) is the writing on the VDU for BT? Will Digital Man save them in the face of the looming Mercury monster? Or will they settle for the protection afforded by vast profits in the short time before the Mercury monster arrives? What does lie beyond the telephone?

Faraday lecture dates: November 6th: St. David's Hall, Cardiff; 13th: City Hall, Sheffield; 17th: Free Trade Hall, Manchester; December 4th: The Dome, Brighton; 11th: The Conference Centre, Harrogate; January 22nd: The Guildhall, Portsmouth; 30th: The Philharmonic Hall, Liverpool; February 4th-6th: Logan Hall, London; 12th: The Town Hall, Birmingham; 26th: Sir William Whitlaw Hall, Belfast; March 5th: The University Great Hall, Exeter; 12th: Colston Hall, Bristol; 19th: The Assembly Rooms, Derby.

● Philips have announced their intention to develop an add-on adaptor for TV sets enabling them to pick up MAC standard signals from satellites via a parabolic aerial. It should be on the market by early 1987 and is designed to handle any changes in TV picture aspect ratio which may be introduced. The MAC standard has been formulated to improve picture definition by separating chrominance and luminance signals. Better sound fidelity and multi-channel sound will also be achieved. Philips see the move as a commitment to 'future high-definition TV'.

● Castle Associates have set-up a hire division specialising in acoustic test instruments. Among the instruments available on short-term rental are sound level meters, environmental noise analysers, dosimeters and vibration meters. Customers may take up the option of purchasing a new instrument at 'a generous allowance'. Details from Castle Associates Ltd., Slater Road, Scarborough YO11 3UZ, tel 0723-584250.

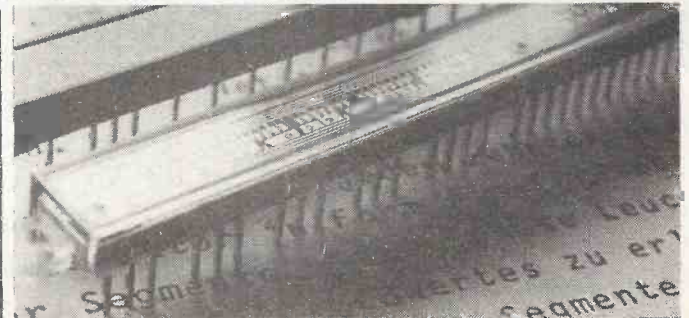
Called To The Bar

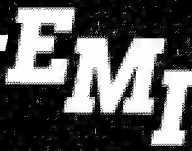
New 101 segment LED bargraph displays from Siemens and Hewlett Packard provide precision alternatives to mechanical meters.

The Siemens range (illustrated) features LEDs combined in groups of ten with common cathodes. One version of the display includes a yellow luminous dot after every tenth segment for ease of reading. The HP range has been extended to include high efficiency red and high performance green devices, in addition to the standard red display. For details contact Siemens Ltd., Siemens House, Windmill Road, Sunbury-on-Thames, Middlesex TW16 7HS (09327-85691) and Hewlett-Packard Ltd., Miller House, The Ring, Bracknell, Berks RG12 1XN, 0344-424898.

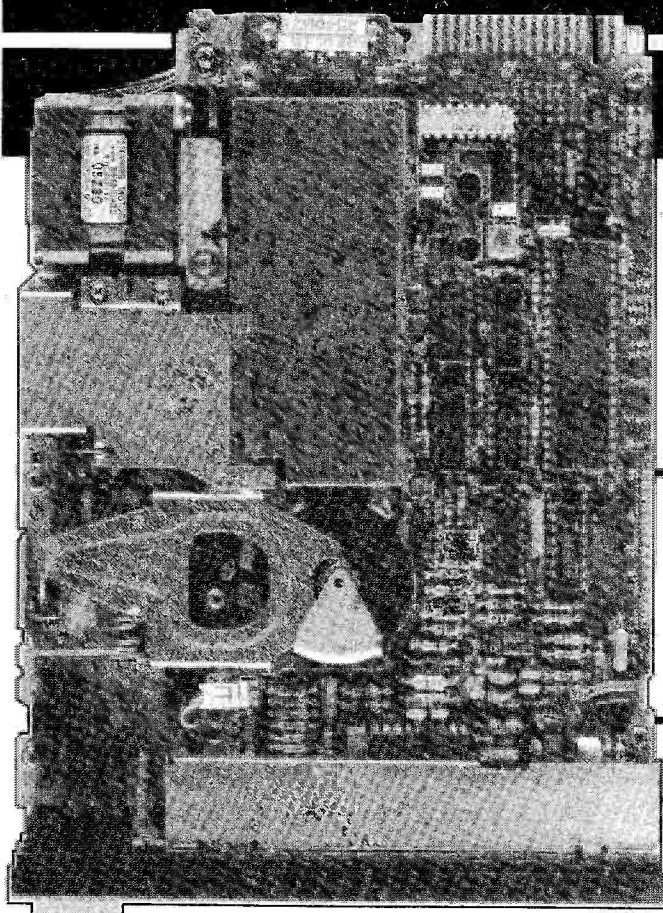
● Texas Instruments have published a European edition of volume 3 of the TTL Data Book series covering bipolar programmable logic and memory devices, including PAL (programmable array logic) FPLAs (field programmable logic arrays) and Schottky TTL memories. The volume is available from Texas Instruments Ltd., PO Box 50, Market Harborough, Leicestershire, at £6.50 plus £1.50 p&p.

● ERA Technology have produced a report titled 'Zinc Carbon and Alkaline Primary Batteries' which investigates the product range of the four leading UK suppliers: Duracell, Ever Ready, Varta and Vidor. Value-for-money comparisons are based on actual discharge rates. The report costs £65 (£55 to members) from Publication Sales, ERA Technology Ltd, Cleeve Road, Leatherhead, Surrey KT22 7SA.





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74LS20		0.13	6116-4	2.00	I.C. SOCKETS - STD	68	11K	3.6M			IMF35V	0.10
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74LS30		0.13	81256-15	5.00	24 PIN	81	15K	5.1M			22MF16V	0.18
74LS32		0.13			28 PIN	91	16K	5.6M				
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74LS125		0.45	9216	8.00		160	30K	10M			PHONO SOCKET -	0.14
74LS138		0.25	6301-1N	1.00	MODULATORS -						NUT FIXING	0.14
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74LS193		0.50	SY6551A	2.50	TRANSISTORS	2.7	470	91K			BNC SOCKET -	0.40
74LS241		0.50	TMS9928	5.00	2N3904	3.0	510	100K			20 x 5MM PCB MTG	0.10
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74LS245		0.75	Z80ACPU	1.50	TLO81CP	4.3	750	150K			QUICK BLOW FUSE	0.10
74LS257		0.75	Z80ACTC	1.40		4.7	820	160K			6 PIN DIN R/A PCB	0.35
74LS273		0.30			DIODES	5.1	910	180K			MTG SOCKET	0.35
74LS365		0.50			IN4004	5.6	1K	200K			7 PIN DIN R/A PCB	0.35
74LS367		0.50			IN4148	6.2	1KMF	220K			MTG SOCKET	0.35
74LS373		0.45			IN5402	6.8	1.1K	240K			9 WAY 'D' TYPE R/A	0.25
74LS374		0.45	47MH	0.05	AXIAL	7.5	1.2K	270K			PLUG	0.25
74LS393		0.50	22MH	0.05		8.2	1.3K	300K				
74LS465		0.75	33MH	0.05		9.1	1.5K	350K				
74S04		2.00	100MH	0.05		10	1.8K	390K				
74S734		2.00			CRYSTALS	11	2K	430K				
			1.8432MHz	2.00	BZX79C4V7	12	2K	430K				
C MOS			3.579645MHz	0.50	BZX79C5V1	13	2.2K	470K				
4013		0.25	4.00MHz	0.50	BZX79C5V6	15	2.4K	470K V/W				
4016		0.25	4.433619MHz	0.50	BZX79C12	16	2.7K	510K				
4049		0.25	10.6875MHz	0.50	BZX79C7V5	18	3K	560K				
4066		0.30			POTENTIOMETERS	20	3.3K	620K				
					1K HOR PRESET	22	3.6K	680K				
					1K CERMET	24	3.9K	750K				
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NEWS:NEWS:NEWS

DIARY

Cellular Communications International — November 5-7th
Wembley Conference Centre, London. For details see September '85 ETI or contact Online at the address below.

Electronics for Peace: London Group Meeting — November 7th
London New Technology Network, Camden, London, 7.30 p.m. Discussion entitled 'Are nuclear weapons a deterrent?'. For details contact Louis Barman on 01-541 1825.

Comex '85 — November 12/13th
Chesford Grange Hotel, Kenilworth, Warwickshire. Conference and exhibition devoted to mobile communication products. Conference topics include the development of radiopaging, the various issues surrounding the future of cellular radio and the re-allocation of the bands used until recently for 405 line television. For details contact Sarah Welch-Hawksby, Federation of Communication Services, PO Box 442, London SE19 3LT, tel 01-653 2657.

Programming In Ada: A Hands-On Workshop — November 12-15th
London. For details see November '85 ETI or contact ICS at the address below.

Compec '85 — November 12-25th
Olympia, London. For details contact Reed Exhibitions, Surrey House, 1 Throwley Way, Sutton, Surrey SM1 4QQ, tel 01-643 8040.

Electronic Component Quality — November 22nd
Institution of Electrical Engineers, London, 10.00 a.m. Discussion meeting at which six papers will be presented. For details contact the Secretary at the address below.

Acorn User Christmas Show — November 22/23rd
Central Hall, Westminster, London. Tickets cost £3.00 (adults) and £2.00 (under 16s) at the door or £2.00 and £1.00 in advance. Contact Edition Scheme Ltd at the address below.

6809 Show — November 23/24th
Royal Horticultural Halls, London. Tickets £3.00 (adults) and £2.00 (under 16s) at the door or £2.00 and £1.00 in advance. Contact Edition Scheme Ltd at the address below.

International Test And Measurement Exhibition — November 27-29th
Olympia 2, London. For details see February '85 ETI or contact Network Events Ltd, Printers Mews, Market Hill, Buckingham MK18 1JX, tel 0280-815226.

Satellite Communications — December 3/4th
Tara Hotel, London. For details see November '85 ETI or contact Online at the address below.

The History of Sound Broadcasting — December 5th
IEE, London. Lecture by Dr. G.J. Phillips, formerly of the BBC. For details contact the Secretary at the address below.

The Which Computer? Show — January 14-17th
NEC, Birmingham. For details contact Cahners at address below.

Electronics In Oil And Gas — February 4-6th
Barbican, London. For details see November '85 ETI or contact Cahners at the address below.

Electronic Production Efficiency Exposition — March 11-13th
Olympia, London. For details see November '85 ETI or contact Cahners at the address below.

Addresses:
Cahners Exhibitions Ltd, Chatsworth House, 59 London Road, Twickenham, Middlesex TW1 3SZ, tel 01-891 5051.
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ICS Publishing Co (UK) Ltd, 3 Swan Court, Leatherhead, Surrey KT22 8AD, tel 0372-379211.
Institution of Electrical Engineers, Savoy Place, London WC2R 0BL, tel 01-240 1871.
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FX/RX/MX100 £10 (d)
FX/FX80 Dust Cover £4.50 (d)

KAGA TAXAN

RS232 with 2K Buffer £85 (c)
KP810/910 Ribbon £6.00 (d)

JUKI 6100

RS232 with 2K Buffer £65 (c)
Ribbon £2.50 (d)

Tractor Attachment £129 (a)
Sheet Feeder £180 (a)
BBC Parallel Lead £7 (d)
Serial Lead £7 (d)

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Sheet Feeder £199 (a)
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Ask for details on WS3000

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Serial Cable switchable at both ends allowing pin options to be re-routed or linked at either end - making it possible to produce almost any cable configuration on site.
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Allows an easy method to reconfigure pin functions without rewiring the cable assembly.
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2764-25.....	£2.40
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CONNECTOR SYSTEMS

I.D. CONNECTORS

No of ways	(Speedblock Type)		Edge Conn.
	Header Plug	Recep-tacle	
10	90p	85p	120p
20	145p	125p	195p
26	175p	150p	240p
34	200p	160p	320p
40	220p	190p	340p
50	235p	200p	390p

D CONNECTORS

No of Ways			
9	15	25	37
MALE:			
Ang.Pins	120	180	230 350
Solder	60	85	125 170
IDC	175	275	325 -
FEMALE:			
St Pin	100	140	210 380
Ang.pins	160	210	275 440
Solder	90	130	195 290
IDC	195	325	375 -
St Hood	90	95	100 120
Screw	130	150	175 -
Lock			

TEXTTOOL ZIF

SOCKETS		
28-pin	£9.00	24-pin £7.50
		40-pin £12

EDGE CONNECTORS

	0.1"	0.156"
2 x 6-way (commodore)	—	300p
2 x 10-way	150p	—
2 x 12-way (vic 20)	—	350p
2 x 18-way	—	140p
2 x 23-way (ZX81)	175p	220p
2 x 25-way	225p	220p
2 x 25-way (Spectrum)	200p	—
2 x 36-way	250p	—
1 x 43-way	260p	—
2 x 22-way	190p	—
2 x 43-way	395p	—
2 x 47-way	400p	500p
1 x 77-way	400p	—
2 x 50-way (S100conn)	600p	—

EURO CONNECTORS

DIN 41612	Plug	Socket
2 x 32 way St Pin	230p	275p
2 x 32 way Ang Pin	275p	320p
3 x 32 way St Pin	260p	300p
3 x 32 way Ang Pin	375p	400p
IDC Skt A + B	400p	—
IDC Skt A + C	400p	—
For 2 x 32 way please specify spacing (A + B, A + C).		

MISC CONNS

21 pin Scart Connector.200p
8 pin Video Connector.200p

AMPHENOL CONNECTORS

	Solder	ZDC
36 way plug	500p	475p
36 way skt	550p	500p
24 way plug	—	—
IEEE	475p	475p
24 way skt	—	—
IEEE	500p	500p
24 way 700p	36way 750p	—

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24" Female Female.....	£10.00
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8-way 120p 10-way 150p

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(grey/metre)
10-way 40p 34-way 160p
18-way 60p 40-way 180p
20-way 85p 50-way 200p
26-way 120p 64-way 280p

DIL HEADERS

	Solder	IDC
14 pin	40p	100p
16 pin	50p	110p
18 pin	60p	—
20 pin	75p	—
24 pin	100p	150p
28 pin	160p	200p
40 pin	200p	225p

TECHNOLINE VIEWDATA SYSTEM

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READ/WRITE

Oldrad?

Dear Sir,

I am grateful for the opportunity to make known the devastating frustration I experienced in my dealings with Newrad in the matter of the Linsley Hood amplifier.

I sent the firm my cheque for £49.49 from London on 10 September, 1984, for MA2 and MA3 kits plus air postage to South Africa. Delivery was to be six weeks from 21 September. I sent reminders in November and again in January 1985. I received an air parcel in mid-February.

The kits were incomplete in many respects. Some items were ridiculously unsuitable and others of very poor quality. As a result of further correspondence, I received a supplementary parcel, the contents of which were still incomplete and inappropriate. A third parcel attempted and failed to restore the order to specification.

At my instigation the firm sent me a cheque 'to cover interest on the money held for eight weeks.' The actual total delivery period in the end proved to be 22 weeks.

The contents of the parcels gave me the impression of an organization unsuited to its undertaking and woefully lacking in quality control. My attempts at assembly have been unsuccessful as a result. I have over 55 years experience in this field backed by full instrumentation and I am extremely angry and frustrated as a result.

I am determined to bring the project to completion. It seems I was supplied with primitive prototype PCBs and unsuitable components. As I am not prepared to repeat this distressing experience, please tell me where I can find a competent supplier of kits or assembled power amp PCBs.

Yours faithfully,
Dr. A.H. Barzilay
South Africa.

Dear Sir,

In the June to September 1984 editions of your magazine, you printed a series of articles on the construction of an amplifier by John Linsley Hood, which was

called 'Audio Design'.

In this article it was stated that a kit was available from a company called Newrad Instrument Cases Ltd. I tried to contact them by post without success and when I phoned them I was given all sorts of strange stories and excuses but precious little information.

In the end, I decided to build the design from scratch — but I cannot get two types of component which are specified.

These are a small MOSFET (VN1210M) and the low ESR electrolytic capacitors of which there are quite a few.

I would be most grateful if you could send me the names of companies which supply these.

Yours faithfully,
R.D. Wren
Bristol.

Oh dear! I'm afraid the staff at ETI Towers are as distressed and frustrated as our correspondents over the matter of Newrad (tired and emotional, some would say). And we haven't even been constructing the kit! I am glad to say that things are looking up. First, for those of you interested in building the JLH system who have heard that Newrad have made changes to the PCBs, we are about to reprint the series with all necessary revisions in our sister magazine, *Electronics Digest*. This is a quarterly and the relevant issue will be appearing towards the end of the year.

As far as the companies are concerned: the VN1210M transistor (in fact, all the transistor types) are stocked by Hart Electronic Kits Ltd., Penylan Mill, Oswestry, Shropshire, SY10 9AF. Hart may also be able to supply the low ESR electrolytics, but — to avoid disappointment — they suggest that any potential customers write to them first to check the stock situation.

I trust that this will be the end of correspondence on this unhappy affair. — Ed.

Artificial Intelligence

Dear Sir,

I am about to start an association for those interested in building robots. I would like you to help me through your magazine to get in touch with other associations in other countries.

I know of one association in Sweden:

Stockholm Robot Sällskab
Leif E.K. Wikstrom
Bjorkhyttevagen 93a
711 00 Lindesberg
SWEDEN

Yours faithfully,
Dansk Robot Forening
Hans Ostergaard
Saekedammen 5
DK-3460 Birkerød
DENMARK.

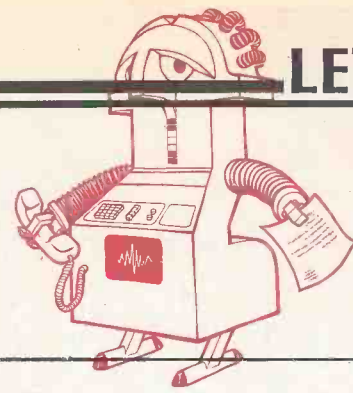
Come on now, all you robots. Drop Hans a line. — Ed.

We are pleased to note that a number of readers responded to the letter from Rodney Dulce of the Philippines which appeared in October, 1985, issue of ETI. We will be able to provide a subscription to Rodney as soon as the paperwork is sorted out. And we will be replying to those of you who wrote to us individually. Just give us a bit of time.

We have also received a letter from an S. Davies of Leeds recommending what appears to be an audio repair company called KIA. We would like to be able to pass on their address to our readers — unfortunately S. Davies failed to supply it. Any chance of another letter?

ETI welcomes all queries, letters and contributions large or small. Any letter we receive is liable to be published unless marked 'Not For Publication'. We reserve the right to edit letters for reasons of space.

In general, please type your contributions using double-spacing and wide margins. Any diagrams should be neatly drawn in ink on plain paper and PCB foil patterns (if enclosed) should be at 2:1 scale. Please print any program listings at 4½ inch column width or (if more suitable to the listing) we may accept listings at 9 inches column width. The specifications for listings are meant to facilitate layout and avoid errors that may creep in if listings have to be re-typed. As a guideline, 4½ inches is most suitable for BASIC or other high-level language listings while 9 inches would suit hex-dumps or annotated assembly language listings. Please send any letters and contributions to ETI, ASP Ltd., 1 Golden Square, London W1R 3AB.



AUNTIE STATIC'S PROBLEM CORNER

Dear Auntie,

Can you please tell me why there are so many different types of capacitors? What is the difference between ceramics, polyester, polystyrene, mica and all the rest?

S. Reed,
Exeter.

In an ideal world, capacitors would be capacitors and there would be nothing to choose between them. In the real world there is no such thing as a capacitor, in the sense of a device which obeys all the text book rules, and we can only hope that our assemblies of insulating and conducting sheets will behave more or less like one.

What we end up with is something like that shown in Fig. 1, where L , R_s and R_p are extra circuit elements that arise because of the way the capacitor is constructed.

You couldn't cut the capacitor open and find them inside, but they are very real because the circuit you've soldered your capacitor into sees all the extra components and behaves accordingly. The effects can be minimised by making L and R_s as small as possible and R_p as large as possible, partly by paying attention to the construction of the capacitor and partly by the choice of dielectric material. The value of L depends on whether the capacitor is wound internally or constructed in flat layers, and R_s results from dielectric losses as well as any physical resistances inside the capacitor. The different compromises that can be reached give rise to a variety of different types of capacitor, some of which are more suited to certain types of circuits than others.

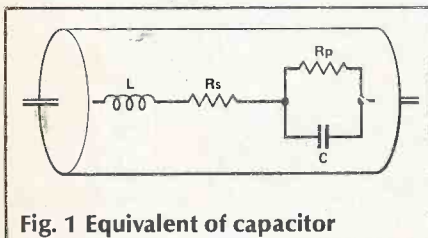


Fig. 1 Equivalent of capacitor

The fact that capacitors are not entirely capacitors is just the beginning of the problem. Another little hiccup is that the value of any capacitor you use will keep changing. Take ceramics for instance. How long do you think it would take for the value of a high K ceramic capacitor to drop by 5%, just through the normal ageing process? Months? Years? I'm afraid not. A high K

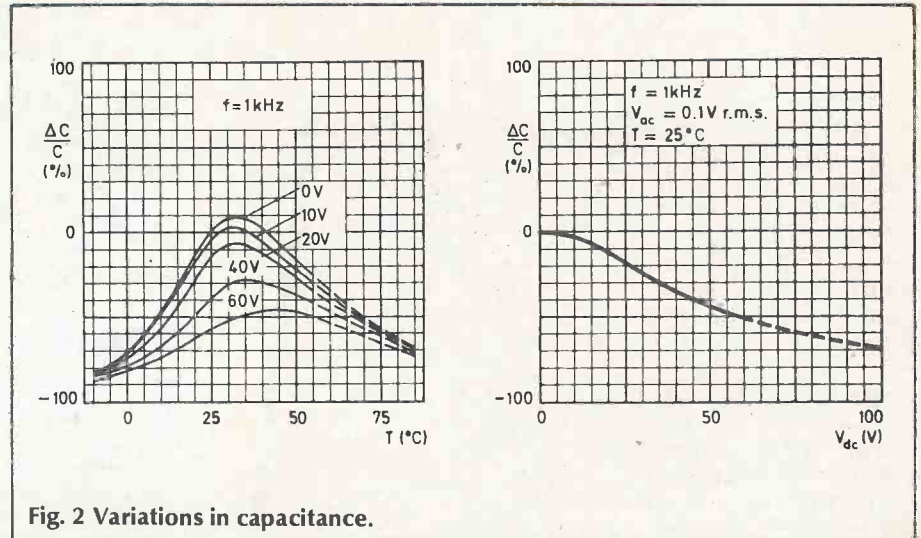


Fig. 2 Variations in capacitance.

ceramic can change in value by 5% between 6 minutes and an hour after being manufactured, and will continue to decline logarithmically thereafter, so that in 10 hours it will be another 5% down, after 100 hours (not much over four days) another 5% is lost, and so on. No wonder they are not recommended for use in tuned circuits and oscillators!

An even greater change in value occurs if the temperature changes. Take a look at the graphs in Fig. 2, taken from a manufacturers data sheet. A ceramic of this type (Mullard 629 series) will drop in value by 70% from its marked value at 25°C if the temperature drops to freezing point. Your 1n0 capacitor now has a value of 300p! Perhaps you don't freeze your circuits, but marked variations occur for quite normal household temperature variations, as you can see. If you have the audacity to wire the capacitor into a circuit, the value can change yet again. With a DC voltage of 60V applied, you've got less than half the capacitance you thought!

We all know that ceramics are notoriously bad in many respects, but other types exhibit similar characteristics to a lesser extent. Capacitance will change with time, temperature and frequency. Losses and insulation resistance will vary and so on. The type you choose will depend on the kind of demand your circuit makes on it.

Ceramics, as we have seen, would be reserved for circuits where the value is not critical. (Having said that, there are fairly stable brands of ceramics made for circuits which make use of some of their more desirable characteristics.) For applications

requiring high stability — oscillators, tuned circuits, filters, etc — mica or polystyrene are particularly good. Polycarbonates are useful when a high insulation resistance is needed.

In some applications a low ESR or low equivalent series resistance capacitor (that is one having a low value of R_s) can be important. The resistance itself can directly dissipate heat (this is the reason for the maximum ripple current rating on electrolytics for use in power supplies) and will cause a shift in the ideal 90° phase relationship between voltage and current. The losses increase with frequency, so careful choice is needed for high frequency applications.

In pulse circuits the series inductions can be a prime consideration. This depends mostly on the way the capacitor is constructed. In sample and hold circuits, dielectric absorption will cause certain types of capacitor to fall in voltage as soon as the input is removed (this is quite distinct from any leakage that may occur), so low hysteresis dielectrics such as polystyrene or polypropylene would be used. And so it continues.

The study of materials used for capacitor dielectrics, or Dielectric Materialism as Marx called it, is a very involved subject. As with my earlier advice about transistors, it's a case of using general purpose types in non-critical applications, using general rules and your own experience in choosing components for more exacting needs, and resorting to manufacturers data sheets on the odd occasion when the right choice will make all the difference to your circuit.

— Auntie.

ETI

NEXT
MONTH

AN ARGUS SPECIALIST PUBLICATION

electronics today

INTERNATIONAL

Etienne Scrooge, known to his friends as Eti for short (he stood less than five feet in his woollen socks) looked out of his window. People scurried about the streets in the swirling snow, collars up to defend themselves against the biting wind. Everywhere the sound of Carols could be heard — Carole King, Carol Bayer-Sager, J. Carroll Nash, Carroll Leavis, Cary Chessman, Carole Lombard., O. Carol (after whom Neil Sedaka had once written a song). It was a glorious sound. Eti had just invented the world's first dyslexic transistor (it was an NNP type), Christmas was coming, the goose was getting fat — and, happily, had not yet been told about Christmas — and he felt good! He gave vent to his emotions:

'Humbug!' he cried. 'Humbug! Bah! Humbug!'

He felt even better for that, and went off to read the Christmas edition of ETI — a magazine he felt a strange kinship to — over a generous breakfast of cornflakes and kidneys. Eti turned to the ETI ACTIVATOR, but soon realised that it wasn't one of his inventions. Then he turned to the ETI AUTOWIPER, but once again they had used his name for no good reason and without his permission or any sort of explanation. He decided to sue the publishers, but first dashed off a note explaining the principles of operation behind the NNP transistor. Suddenly, he was confronted by the ghost of Lee de Forrest.

'It'll never work,' said de Forrest. 'Why don't you read the new Barry Porter article, or find out about Gallium Arsenide. Or you could settle down to a short story by John Linsley Hood.'

'A short story by John Linsley Hood!' snorted Etienne. 'Humbug!'

'No,' said de Forrest, 'but it's not Brighton Rock, either.'

And it wasn't...

The ETI Activator

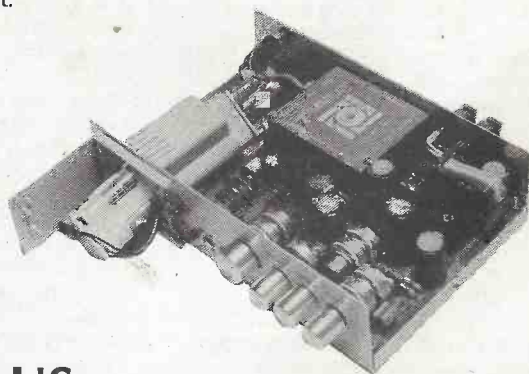
The second in our series of sound processing units, this exciting device adds brilliance to your sounds. High fidelity buffs may murmur disapprovingly, but similar units to this one are all the rage in recording studios and those who've heard the Activator say that it reaches parts of the audio spectrum that even ultra-fi can't!

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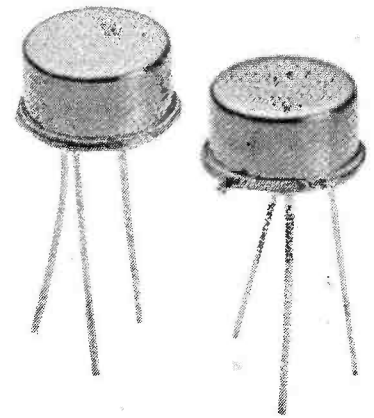


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DESIGNING TRANSISTOR STAGES



Les Sage looks at some variations on a common theme.

Having introduced the practical techniques involved in designing a common emitter transistor stage (ETI, November 1985), this month we'll concentrate on more general consideration of different configurations. Each circuit has been fully tested and its basic characteristics are given in the appropriate diagram. Component values have been calculated using similar techniques to those dealt with last month, involving emitter, collector and base voltages and currents and transistor gain. Two gain figures are used, one for signals (AC) and the other for notional DC levels (notional because most of the circuits are AC coupled). The DC gain figure, however, is an indication of circuit stability.

Bootstraps And Feedback

The main problem with the standard stabilized common emitter stage of last month (ETI, November 1985) is the rather low input impedance resulting largely from the base bias resistors shunting the input signal. A way round this problem is to use three bias resistors and include an extra 'bootstrapping' capacitor (Fig. 2). The principle of operation is that any input signal present at the transistor's base will, by emitter follower action, appear at much the same magnitude at the emitter. Since C2 (the bootstrap capacitor) is relatively large, it will act as a short circuit to the AC signal at the emitter and couple it without any attenuation to the junction of R1 and R2. Resistor R3 will have more-or-less the same AC signal at both ends, so there cannot be any AC current flowing through it and all the signal input goes into the transistor.

The input impedance is then that of the transistor stage and is not shunted by the bias chain. The DC bias conditions have not been altered significantly by the presence of R3 although, in practice, emitter follower action is not 100% and the junction of R1 and R2 is at a slightly lower potential than the input signal, meaning that a very small current still flows into the bias chain.

A second benefit of this configuration — and one not often realised — is that any noise on the supply lines will now be decoupled to the emitter through C2 instead of being fed down the bias chain into the transistor's base. Since the emitter circuit has a very low impedance, it will remove the noise.

The un-bypassed emitter resistor, R5, adds to the input impedance of this circuit by introducing current feedback. The input impedance is approximately equal

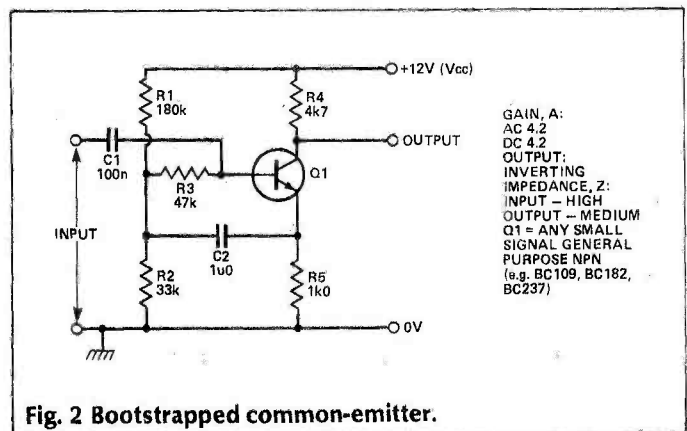


Fig. 2 Bootstrapped common-emitter.

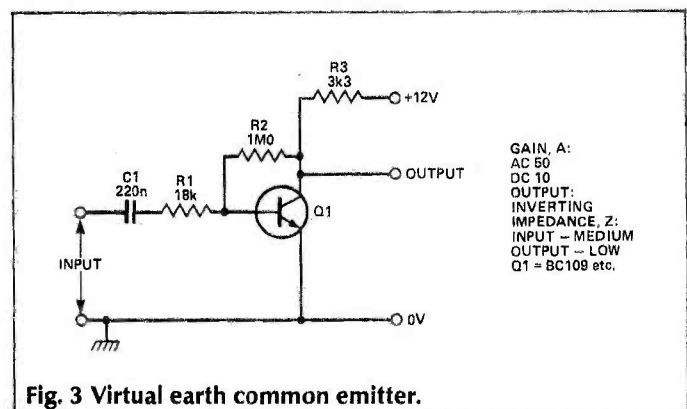


Fig. 3 Virtual earth common emitter.

to the $h_{ie} \times R5$ (typically greater than 100k). The output impedance is also quite high. This can be reduced — at the expense of also reducing input impedance — by a voltage feedback arrangement as in Fig. 3. In this circuit, a current proportional to output voltage is fed back to the input through R2, so that any tendency for the collector current to change is counteracted by an opposite tendency in the feedback current. This is a very economic arrangement, giving good stability at low cost and complexity. The circuit is probably most familiar for its DC stabilization characteristics, but among single transistor stages it is the closest thing to a virtual earth amplifier.

Ideally, the transistor should have a very high current gain, h_{fe} , which is not too difficult with contemporary silicon devices. If R1 is large compared to the source

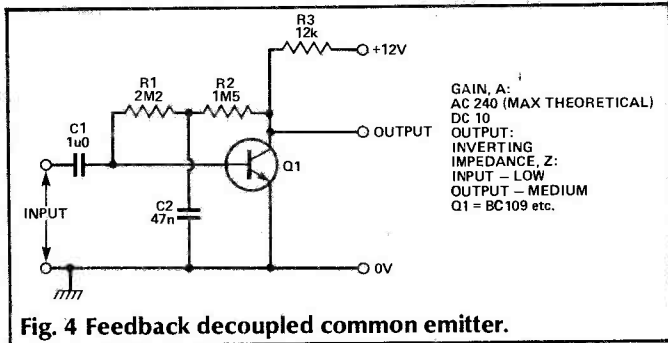


Fig. 4 Feedback decoupled common emitter.

resistance and the transistor input resistance (it's in the order of ten times Q1's input resistance as it stands), then the circuit input impedance will be roughly equal to R1 and the gain roughly equal to the ratio of R2 to R1. The output impedance is reduced by the ratio of closed-loop gain to open-loop gain. In an actual circuit, this worked out to be about three quarters, giving an output impedance of about 2k5 (0.75xR3).

For high gains (and it is only with high gains that the approximate values are really reliable, R1 must be quite low. Reducing R1, however, is also liable to upset the calculations and, in practice, a compromise is required. The circuit makes a good current-to-voltage converter, with output voltage equal to input current multiplied by feedback resistance.

Figure 4 shows how to obtain a higher input impedance at high gains. Two feedback resistors — R1 and R2 — are used, their junction being decoupled to earth through C2. This gives a moderate input impedance (which can be increased by the addition of an input resistor as in Fig. 3) and high gain but at the cost of increasing output impedance against the Fig. 3 circuit. The effect is due to the action of C2 in shunting signal frequencies to earth and avoiding AC feedback. The circuit may be considered the voltage feedback equivalent of the current

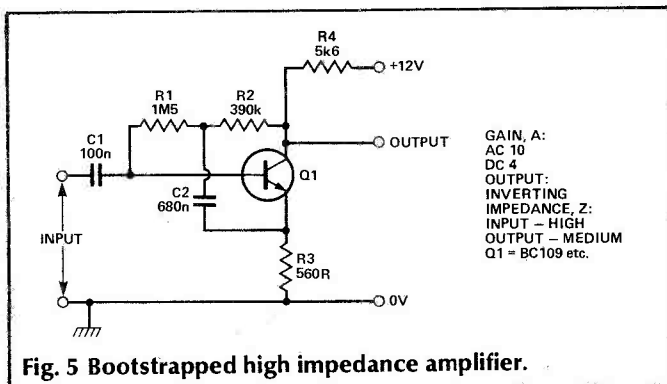


Fig. 5 Bootstrapped high impedance amplifier.

feedback common emitter with a bypass capacitor across the emitter resistor (Fig. 1, ETI November 1985, with R5 shorted out).

A refinement to Fig. 4 can be seen in the circuit shown in Fig. 5. Capacitor C2 now shunts signal frequencies to the transistor emitter. By bootstrap action, R1 is now effectively an open circuit to AC signals, giving high input impedance and an associated reduction in gain. This configuration combines good DC stability with reasonable gain and high input impedance. The output impedance remains fairly high, due to the absence of direct parallel-derived AC voltage feedback. The circuit, however, finds an ideal use as a ceramic cartridge input stage where a high input impedance is required with not much gain.

Because of its high input impedance and very low

output impedance, the emitter follower (or, common collector) circuit (Fig. 6) makes an ideal buffer between stages. The low output impedance (in the order of 10R) means that it will drive almost anything current-wise. The circuit also has an input impedance which is higher than that of all the previous circuits we've seen, even though the emitter circuit impedance of around 500k is shunted by the bias resistors. It therefore presents a very small load to any preceding stage. Add to this the fact that voltage gain is practically unity and it is clear why many engineers — unable or unwilling to design circuits for a particular purpose — just stick an emitter follower at the input and the output of some conventional amplification stages.

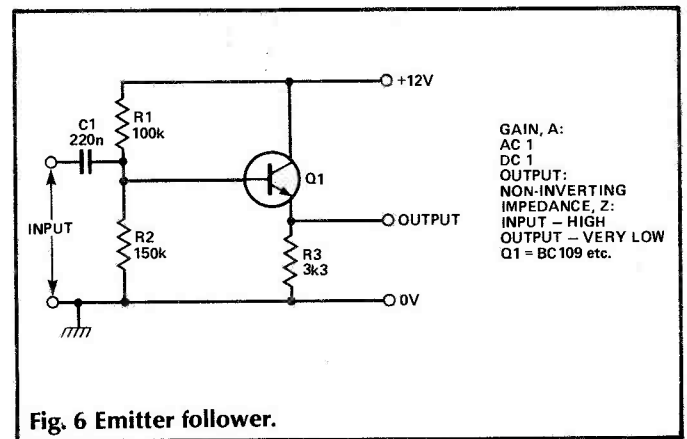


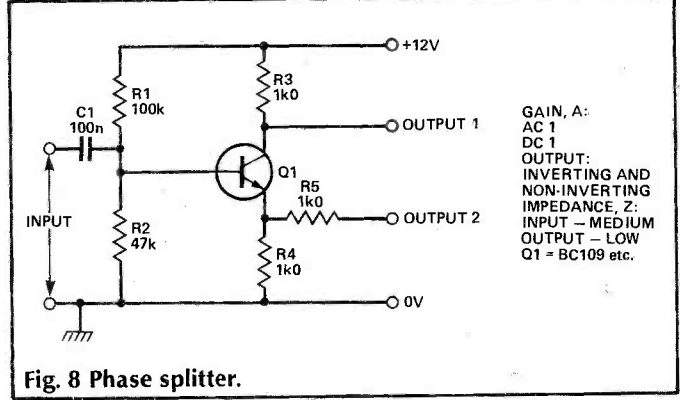
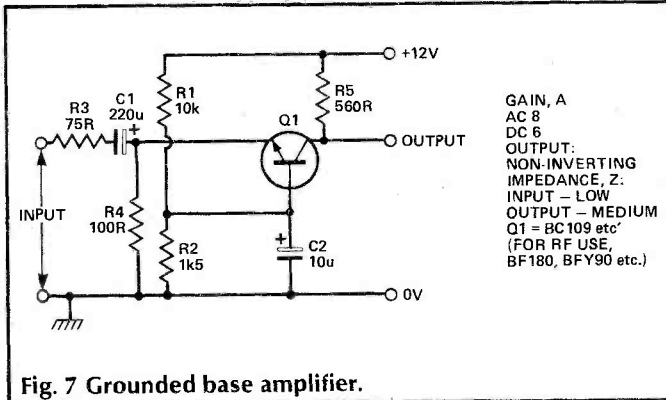
Fig. 6 Emitter follower.

In practice, many emitter followers can be omitted altogether — especially if circuits are custom-designed. Nevertheless, it remains a useful addition to the designer's armoury.

Ground To Base

So far, all the circuits described have been for low frequency applications. At the higher frequencies characteristic of radio and video, they will all show a distinct lack of gain. The responsibility largely belongs to the Miller capacitance effect. All transistors display a certain amount of capacitance between junctions. The capacitance between the base and collector is small and would not seem to be a cause for concern. However, the Miller effect says otherwise. A capacitance between the input and output of an inverting amplifier (for example, between the base and collector in a common emitter stage) appears to the input signal as having a value equal to the actual capacitance multiplied by the voltage gain. This is a form of negative feedback. What's more, the capacitance appears to shunt the signal to earth, so that base-collector capacitance multiplied by voltage gain is added to base-emitter capacitance. This produces a considerable reduction of input impedance at high frequencies and, in conjunction with input source resistance and the transistor's base layer resistance, a loss of signal amplitude and therefore of effective gain. For somewhat different reasons, emitter follower performance (which is dependent on current gain) also falls off at high frequencies.

One way of overcoming such effects is to operate the transistor in grounded (or, common) base mode. The transistor conducts DC as normal and component values are calculated as with a common emitter, but the signal is injected into the emitter and the base is held at ground potential to AC by a large-value capacitor. Any feedback signal due to internal transistor junction capacitance between collector and base is now shorted to ground by



the external capacitor (C2 in Fig. 7). In fact, the base-collector capacitance is no longer directly connected between input and output since the base itself acts as a screen. There is no Miller-amplified feedback capacitance, and the input signal feeds into the already low emitter impedance. Thus, voltage gain remains useful even at very high frequencies (up to the transition frequency f_T).

One characteristic worth noting is that the grounded base configuration is non-inverting since the signal is injected into the emitter and the output is taken from the collector. This is useful for video applications, as is the low input impedance of the circuit (suitable for terminating aerial feeder cables).

Non-inversion can also be achieved with a common emitter stage by taking an output from the emitter itself.

Figure 8 shows a circuit commonly known as a phase splitter, since output 1 and 2 are in antiphase — the first being equal in amplitude to the input but inverted in phase, the second being equal in amplitude and phase to the input. The amplifier has unity voltage gain. Strictly speaking, it only works as a phase splitter for a sine wave, since other waveforms may be degenerated. The main uses of this circuit are for driving balanced lines or as a means of obtaining variable phase for musical effects. R4 is included to ensure that both outputs are of equal impedance.

In the final part of this series we'll be dealing with some useful two-transistor stages. These will show how many of the compromises necessary in designing single transistor stages can be avoided.

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REDUCED INSTRUCTION SET COMPUTERS

Carefully avoiding some of the obvious puns, Mike Bedford takes a look at RISC chips.

The most visible trend in the development of microprocessor technology since the release of 4-bit processors in the early 1970's is a continual increase in the width of the data bus, a factor which is commonly used as a broad classification of processors. Today 8-bit is the accepted type for home computers, 16-bit tends to be used for small business machines and 32-bit is found in scientific machines.

Hand in hand with this development has been an increase in the complexity of the instruction set. The earlier 4 and 6-bit devices could only carry out simple logic and arithmetic functions such as AND, OR, ADD and SUBTRACT, various branches and subroutine calls and limited memory access consisting of LOAD and STORE instructions. As 8-bit development continued, the number of addressing modes increased as did the complexity of the arithmetic functions. Multiply is included on the 6809, for example, this being an 8-bit processor which also offers some limited 16-bit instructions. With 16 and 32-bit processors multiply and divide are the accepted norm and many other advanced instructions such as loop constructions and

block moves are to be found. It goes without saying that increasing execution speeds accompanied the foregoing trends.

A few figures will help to illustrate these trends. The number of basic instruction types on the 8080, the first popular 8-bit processor launched in the mid 1970's, is 30. The later 6502, also an 8-bit device and extensively used in home computers, has a similar

It has been suggested that by the end of the decade, virtually all computers for engineering applications will employ some degree of RISC architecture.

number, whereas the 6809, one of the latest and most advanced 8-bit micros released about 1979, has 43. The 68000, a typical 16-bit processor, has 61. Comparing numbers of instructions between processors is not easy as one processor may have as different instructions what are merely different addressing modes of the same instruction on another device. The numbers above are not necessarily the numbers of instructions claimed by the manufacturers but would, for example, class all conditional branches as a single instruction.

What probably gives a more accurate picture of the complexity of the chip is a count of all the op-codes, a figure which gives a measure of the number of combinations of instructions and addressing modes. When these numbers are considered we see about 200 for the 8080, 266 for the 6809 and over 1,000 for the 68000. Comparing performance numerically is once again difficult but it is quite clear that the 6809 is considerably faster than the 8080 or the 6502 and that the 68000 probably gives a 3 fold speed increase over the 6809.

Even a quick glance at the above figures would lead to the conclusion that complicated instruction sets are

This is the one we use, and this is the one that works out the instructions!



necessary to achieve high processing speeds, and indeed this has traditionally been the point of view throughout the development of computer architecture. The argument for this link is that if a particular function is not available as a processor instruction it will have to be replaced by a series of simpler instructions. For example, if multiply is not available it has to be replaced by a routine carrying out multiple additions and/or shifts, a process which

The Pyramid 90x is claimed by its manufacturers to give 8-10 times the performance of a similar machine with conventional architecture.

will usually be much more time consuming than a hardware implementation of the function.

Recent developments suggest that this trend of increasing complexity in microprocessors may be reversed. The RISC or Reduced Instruction Set Computer offers the possibility of very high speeds coupled with an extremely simple yet innovative architecture.

Development Of RISC

It has been suggested^{1,2} that by the end of the decade virtually all computers for engineering applications, from PCs to multi-user mini-computers, will employ some degree of RISC architecture. Some advocates of RISC would indeed go as far as to suggest that all computers of the late 1980's will include RISC processors. Before going on to describe such a processor and how a simple approach can achieve impressive speeds, it will be useful to outline the development of this type of architecture.

The project which is generally considered to represent the first work carried out on a RISC type architecture is the IBM-801, the design of a simplified instruction set being a result of statistical indications that the most commonly encountered instructions are simple ones such as LOAD, STORE, branches and simple arithmetic. Although this project has not, as yet, yielded a commercial product, preliminary results suggest that it has a performance comparable to the IBM 370/168 mainframe at almost 2 MIPS (million instruction per second) while other reports have claimed speeds as high as 10 MIPS. In view of the fact that the 801 is essentially a mini computer rather than a mainframe, this is a very impressive figure.

Another large company engaged in RISC research is DEC who are reported to have two such projects, code-named Nautilus and Titan. Once again, no commercial product has yet evolved and few details have been published. From those snippets of information that are available, we can say that Nautilus is intended as a general purpose machine which fits somewhere between the VAX and the System 10/20 machines and has a speed of about 10 MIPS, whereas Titan is an engineering workstation with some degree of VAX compatibility which should yield speeds in the region of 2 MIPS.

Other large computer companies are known to be carrying out research in this field but so far only two RISC machines are on the market, both manufactured

We have the promise of microprocessors with a much increased speed-to-cost ratio in the not too distant future.

by smaller companies. The Pyramid 90x is a general purpose machine intended for both commercial and engineering applications. It is clearly intended to compete with the DEC VAX 11/780 and is claimed by its manufacturers to give 8-10 times the performance of a similar machine with conventional architecture. The Ridge 32, on the other hand, brings the power of a VAX to an engineering workstation for applications such as CAD and solid modelling. The claims for this machine are that it executes I/O faster than the VAX 780 and can execute linear equations faster than a VAX 750 with a floating point accelerator.

Although it is interesting to see the impact made by RISC in the realm of mini computers, the area which will be of most interest to readers of this article will be the development of RISC microprocessors. The first such device, RISC I, was completed in 1982 by a team of staff and graduate students at the University of California in Berkley.³ The team, led by Professor David A. Patterson, designed the chip from initial discussion to first silicon in a near record time of only 19 months. The fact that such timescales could be achieved and speeds in excess of those of commercial devices such as the 68000 could be demonstrated by a team with little previous knowledge of VLSI design can be attributed primarily to the simplicity of the architecture. Since impressive performance is possible with minimal design effort, we have the promise of microprocessors with a much increased speed to cost ratio in the not too distant future. In the following

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INSTRUCTION	OPERANDS	DEFINITION	DESCRIPTION
ADD		$Rd \leftarrow Rs + S2$	Integer add
ADDC	Rs, S2, Rd	$Rd \leftarrow Rs + S2 + \text{carry}$	Add with carry
SUB	Rs, S2, Rd	$Rd \leftarrow Rs - S2$	Integer subtract
SUBC	Rs, S2, Rd	$Rd \leftarrow Rs - S2 - \text{carry}$	Subtract with carry
SUBR	Rs, S2, Rd	$Rd \leftarrow S2 - Rs$	Integer subtract
SUBCR	Rs, S2, Rd	$Rd \leftarrow S2 - Rs - \text{carry}$	Subtract with carry
AND	Rs, S2, Rd	$Rd \leftarrow Rs \& S2$	Logical AND
OR	Rs, S2, Rd	$Rd \leftarrow Rs S2$	Logical OR
XOR	Rs, S2, Rd	$Rd \leftarrow Rs \oplus S2$	Logical exclusive OR
SLL	Rs, S2, Rd	$Rd \leftarrow Rs \ll S2$	Shift left
SRL	Rs, S2, Rd	$Rd \leftarrow Rs \gg S2$	Shift right logical
SRA	Rs, S2, Rd	$Rd \leftarrow Rs \ggg S2$	Shift right arithmetic
LDL	(Rx)S2, Rd	$Rd \leftarrow M[Rx + S2]$	Load long
LDSU	(Rx)S2, Rd	$Rd \leftarrow M[Rx + S2]$	Load short unsigned
LDSS	(Rx)S2, Rd	$Rd \leftarrow M[Rx + S2]$	Load short signed
LDBU	(Rx)S2, Rd	$Rd \leftarrow M[Rx + S2]$	Load byte unsigned
LDBS	(Rx)S2, Rd	$Rd \leftarrow M[Rx + S2]$	Load byte signed
STL	(Rx)S2, Rd	$M[Rx + S2] \leftarrow Rm$	Store long
STS	(Rx)S2, Rd	$M[Rx + S2] \leftarrow Rm$	Store short
STB	(Rx)S2, Rd	$M[Rx + S2] \leftarrow Rm$	Store byte
JMP	COND, S2(Rx)	$PC \leftarrow Rx + S2$	Conditional jump
JMPR	COND, Y	$PC \leftarrow PC + Y$	Conditional relative
CALL	Rd, S2(Rx)	$Pd \leftarrow PC \text{ next}$ $PC \leftarrow Rx + S2$ $CWP \leftarrow CWP - 1$	Subroutine call and change window
CALLR	Rd, Y	$Rd \leftarrow PC \text{ next}$ $PC \leftarrow PC + Y$ $CWP \leftarrow CWP - 1$	Call relative and change window
RET	Rm, S2	$PC \leftarrow Rm + S2$ $CWP \leftarrow CWP + 1$	Return and change window
CALLINT	Rd	$Pd \leftarrow \text{last PC}$ $\text{next CWP} \leftarrow CWP - 1$	Disable interrupts
RETINT	Rm, S2	$PC \leftarrow Rm + S2$ $\text{next CWP} \leftarrow CWP + 1$	Enable interrupts
LDHI	Rd, Y	$Rd(31:13) \leftarrow Y$ $Rd(12:0) \leftarrow 0$	Load immediate high
GTLP	Rd	$Rd \leftarrow \text{last PC}$	Restart delayed jump
GETPSW	Rd	$Rd \leftarrow PSW$	Load status word
PUTPSW	Rm	$PSW \leftarrow Rm$	Set status word

Rs = Source register 1
Rd = Destination register
Rm = Register for store
PSW = Status register
Y = Offset

S2 = Source register 2
Rx = Index register
CWP = Register window pointer
PC = Program counter
M = Memory

Table 1. The instruction set for the RISC 1 Microprocessor.

description of RISC architecture the discussion will be based on the Berkeley RISC I and later RISC II chips, although most of what is said could be applied to any machine using RISC philosophy.

Minimal RISC

The most obvious question to tackle first is how a simplified instruction set can lead to high processing speeds. To put this another way, where is the fallacy in the usual argument that incorporating increasingly complex functions into the hardware decreases execution time by removing software overheads?

One problem with this conventional argument is that very often a single advanced processor function of a modern microprocessor may not be all it seems. Instead of a complex instruction being implemented fully in hardware, the situation is that such features are

actually translated to a series of micro-instructions, these being a low level of instruction within the device.

An implication of this is that single instructions on modern microprocessors can often take many cycles to execute. For example, on the 68000, the signed multiply instruction can take up to 42 cycles, 122 cycles are required for signed divide and even a commonly encountered instruction such as return from exception (interrupt return) can take 110 cycles. A closely related point is that, even for simple instructions, if a processor has a number of different variants and/or addressing modes the internal circuitry must be configured to suit each different requirement. This switching of gates is once again carried out by micro-coded instructions with the inevitable speed reduction.

The RISC I and RISC II processors are not micro-programmed and, with a couple of exceptions, are

FEATURE: RISC Chips

able to execute all instructions in a single cycle. Table 1 shows the RISC I instruction set. It will be noticed that there are only 31 instructions and, in contrast to most modern 16 and 32-bit micro-processors, the device is totally devoid of the more esoteric instructions. Coupled with the fact that there are only two addressing modes, it is not difficult to see how all functions can be hardwired, hence obviating the need for micro-coding.

The RISC philosophy is that memory should only be accessed by LOAD and STORE instructions (these being the exceptions which take two machine cycles to execute) all processing being carried out from register to register internally. This limited memory access means, for example, that in order to add two memory locations together into a third, the processor would need to load the contents of the first two memory locations into registers, add the two registers together and finally carry out a store from the register containing the result into the third location.

An implication of this approach is that a large number of internal registers is essential. In fact, the register organisation is quite innovative and will be described shortly. Conveniently, it is because of the simplicity of the processor ALU and control logic (about 6% of RISC I compared to about 50% on many commercial processors) that it is feasible to devote a large area of the chip to the registers required by RISC architecture.

One possible argument against the approach outlined above is that, although it appears able to provide impressive speeds at a reasonable cost, the limited instruction set means that a much greater programming effort will be required. Since the programming time generally represents the greatest part of the cost of a system containing both hardware

and software, this could be a considerable disadvantage. It would undoubtedly limit the attractiveness of RISC processors if programming had to be carried out in assembler language, but RISC I is designed to be programmed in a high level language. Under these circumstances the limited instruction set is quite transparent to the applications programmer, being of concern only to the writers of the compilers.

The use of high level languages does not merely mask a possible disadvantage: indeed, the RISC I

Single instructions on modern microprocessors can often take many cycles to execute. On the 68000, 122 cycles are required for signed divide...

processor was designed with high level languages very much in mind, PASCAL and C being the languages considered. As part of the initial design, statistical data on the frequency of occurrence of various constructions together with the corresponding numbers of machine instructions were analysed. The results led the Berkley team to the conclusion that the most time consuming parts of high level language programmes are concerned with subroutine calls and handling of local variables. As we shall see, the RISC register architecture addressed both these points, reducing their execution times considerably.

Registers

It has already been stated that the RISC I processor offers a large number of general purpose registers. The organisation of these registers and the way in which they greatly contribute to the fast execution of subroutine calls will now be described.

A conventional microprocessor has a relatively small number of internal registers. For example, the 6809 has only two general purpose data registers and two index registers; even the more advanced 68000 has only eight data registers and seven address registers. This means that, on entering a subroutine, all registers which are going to be used by that routine for its internal working must be saved on entry and restored on return to the calling code. This saving and restoring is carried out by means of a stack in memory, this also being the method used for passing parameters to and from the subroutine. It is the need for these PUSH and PULL instructions which so much slows down subroutine calls on conventional processors.

RISC I obviates the need for this time consuming process by using 137 registers which are arranged as a number of overlapping register windows. This scheme is illustrated in Figure 1. The left hand bank shows the internal numbering of the registers in the processor whereas the three banks on the right represent three separate register windows which map physically onto the total pool of 137 registers. Any subroutine has access to one window of 32 registers which are always referred to as R0-R31 irrespective of which physical registers they are mapped onto.

It will be noticed that each register window is split into four segments referred to as global, low, local and high. The global registers are used for values which are

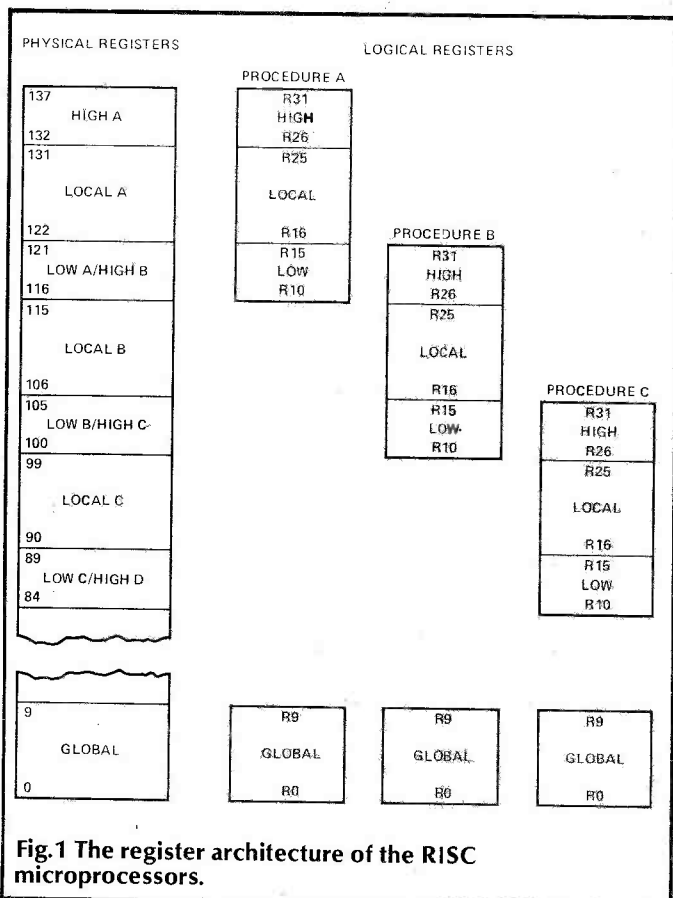
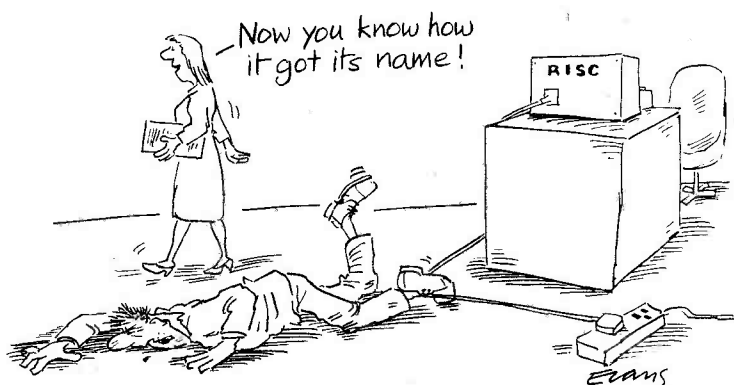


Fig.1 The register architecture of the RISC microprocessors.



team's lack of experience in VLSI design. In spite of this poor circuit speed, RISC I showed up very favourably when compared with a number of commercial 16 and 32-bit processors. Comparisons were made with the Intel 8086, Intel 432 and Motorola 68000, running benchmark tests in high level languages. Of the 4 programs, RISC I proved to be the fastest of the four processors for 3 of the tests and faster than the average for the fourth. The tests are not conclusive because different high level languages were used on the different micros, but the initial results were clearly encouraging.

The RISC II processor ran at 12MHz, giving a cycle time of 330nS which also implies an execution time of 330nS for all but LOAD and STORE instructions. At the time of writing, the RISC II processor has not been built into a microcomputer system and the performance figures are therefore based on simulations. However, it is claimed that for C programs, an 8 MHz RISC II can outperform the 8 MHz iAPX 286, 10 MHz NS 16032, 12 MHz 68000 and 18 MHz HP 9000. Simulated comparisons have

likely to be accessed by a number of different procedures since these are common to all windows. The local registers are used for local working within a particular routine. Whenever a subroutine call or a return is executed, a new window is automatically selected and the local registers used by the calling routine became accessible, thereby obviating the need to save their contents on a stack.

As far as the passing of parameters is concerned, this is where the low and high registers are used. Since the low registers of one window overlap the high registers of a neighbouring window, the means of passing parameters to a procedure is to place them in low registers prior to issuing the call. Conversely, the called procedure will pick up the parameters passed to it in its high register area - once again removing the need for a stack.

Clearly this philosophy places a limit on the depth of subroutine calls which may be nested since there are only a finite number of registers from which to create new windows. To cope with this problem, the RISC I processor recognises overflow and underflow conditions. Under these circumstances a trap takes place to a software routine which stacks the registers in memory in the conventional manner. If this condition were to happen frequently, the performance would clearly suffer. Research has shown that in average programmes, such conditions occur relatively infrequently - if 8 windows are available it is suggested that overflows only happen on about 1% of subroutine calls.

Running The RISC

To conclude this introduction to RISC and to wet the appetite for what could be just round the corner, a comparison of the RISC I and RISC II processors against common 16-bit microprocessors of today will be made. Throughout this section it should be borne in mind that we are talking about a VLSI chip with 44,000 transistors. This compares to 68,000 for the Motorola 68000, and only 5% of the RISC chip is devoted to control functions (that is, the actual processing) compared to 30%-50% on most 16 bit processors.

The RISC I processor achieved a clock frequency of only 1.5 MHz compared to its design frequency of 7.5 MHz, a factor attributable mainly to the development

RISC 1 proved to be the fastest of the four processors for three of the tests and faster than the average on the fourth.

also been made against the DEC VAX 11/780 mini computer. Although this is not comparing like with like because the VAX is a multi user virtual memory machine, it is nevertheless impressive to report that a RISC II running at 12 MHz is able to compile C programs 2 to 2.5 times faster than such a machine.

Conclusions

It is difficult to know how to conclude an article on an aspect of micro electronics which is still in its infancy. Clearly the 'keep it simple' approach to microprocessor design has much to commend it, offering high speed processing at a potentially low cost. RISC advocates predict a rosy future for this type of processor and there is no reason to question the basis for their optimism. Nothing is certain in the electronics industry, however, as a look at the predictions made in the late 1970's regarding bubble memories makes clear. So, is the reduced instruction set computer another dream that will never come to fruition or will it be a major factor shaping the future? Only time will tell!

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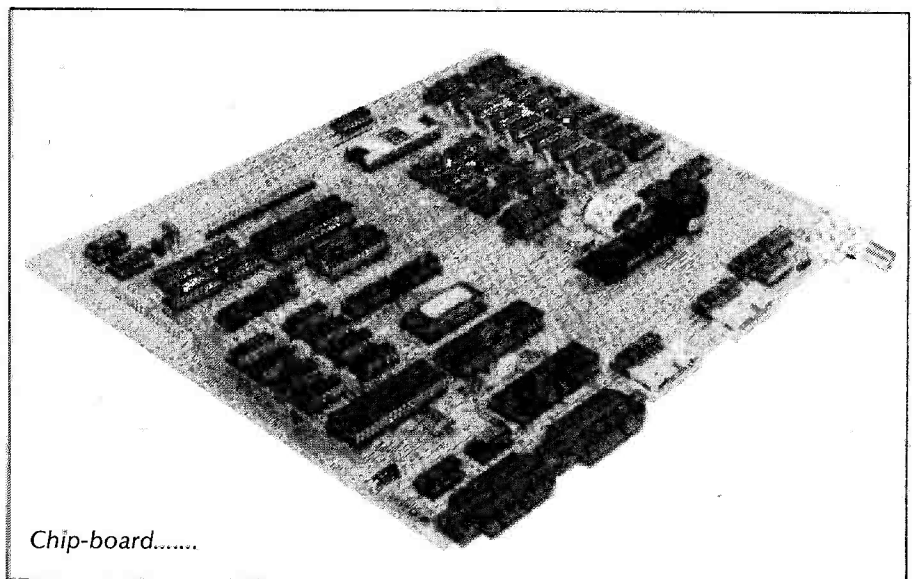
6809-BASED MICROCOMPUTER

In this, the first of a series of articles, G. Mills of Micro Concepts describes a new single-board microcomputer designed by Dave Rumball.

This article describes a single board, 6809-based microcomputer which incorporates a state-of-the-art graphics processor and other advanced features. It can be built at very low cost and is also available from Micro Concepts as a kit.

One of its features is the ability to appear as a Flex standard machine to the wide range of Flex software. This would be of interest to those who are involved in writing software for microprocessor controlled equipment, allowing the board to be used as an inexpensive but sophisticated software development system. In case you aren't aware, the Flex operating system has a wide range of cross assemblers and an elegant command set, and is widely used for this type of work. British companies currently using Flex based development systems for microprocessor software development include Dacom, Racal, and Westwood. Because of its advanced features, this board offers a more congenial environment for software development than many more expensive systems. Companies currently using the Micro Concepts kit (known as the Microbox II) for software development include Thorn EMI and British Telecom.

The design should also be of interest to those who want a really useful computer for very little money. It runs serious wordprocessing and data base software, has beautiful graphics, superb resolution, a completely soft character set and the prototype cost around £450 to build including discs, video monitor, keyboard, power supply and operating system (and the price is coming down).



Chip-board.....

By way of introduction, the following is a partial description of the hardware:

Central processor
— Motorola 68B09E.

64K of dynamic RAM for the central processor. When running the board in the monitor mode, 8K of this is mapped out by the monitor EPROM. When running the Flex operating system, only 4K of the monitor EPROM is retained. This 4K contains driver routines for the discs, serial ports and parallel ports, as well as interface routines for the graphics chip and terminal emulator.

A floppy disc controller that will support up to two 3½ or 5¼ inch floppy disc drives, single or double density, single or double sided, 40 or 80 track.

One parallel keyboard port.

Two independent bi-directional RS232 ports with software programmable baud rates (50 to 19.2k baud), parity, stopbits, etc.

One Centronics standard parallel printer port.

A buffered, fifty pin expansion bus.

All of the above will be familiar to anyone who has experience with run-of-the-mill Flex machines available from a number of manufacturers. The following features are unique to this design:

An additional 128K of dynamic RAM partitioned into alphanumeric video RAM, graphic video RAM, and RAMdisk.

An alphanumeric display format of 108 columns by 24 lines when using the terminal emulator resident in the monitor EPROM. The terminal

emulator and the associated character set are in software and therefore can be redefined if desired. Alternate memory resident emulators come with the kit. One gives a format of 84 by 24 and another 128 columns by 56 lines.

Exceptional monochrome graphics facilities generated by an NEC 7220A graphic display controller. The resolution of the display is 768 pixels by 576 pixels. By way of comparison, this is a resolution 2.7 times greater than the BBC Model B in its highest resolution mode. Graphics primitives (for example the Bresenham algorithm for arc and line drawing) are built into the 7220A, resulting in very fast drawing speeds.

A RAMdisc facility, using a variable amount of the 128K RAM. This RAMdisc looks exactly like a floppy disc to the operating system. The capacity of the disc can vary between 170 sectors (42.5K) when

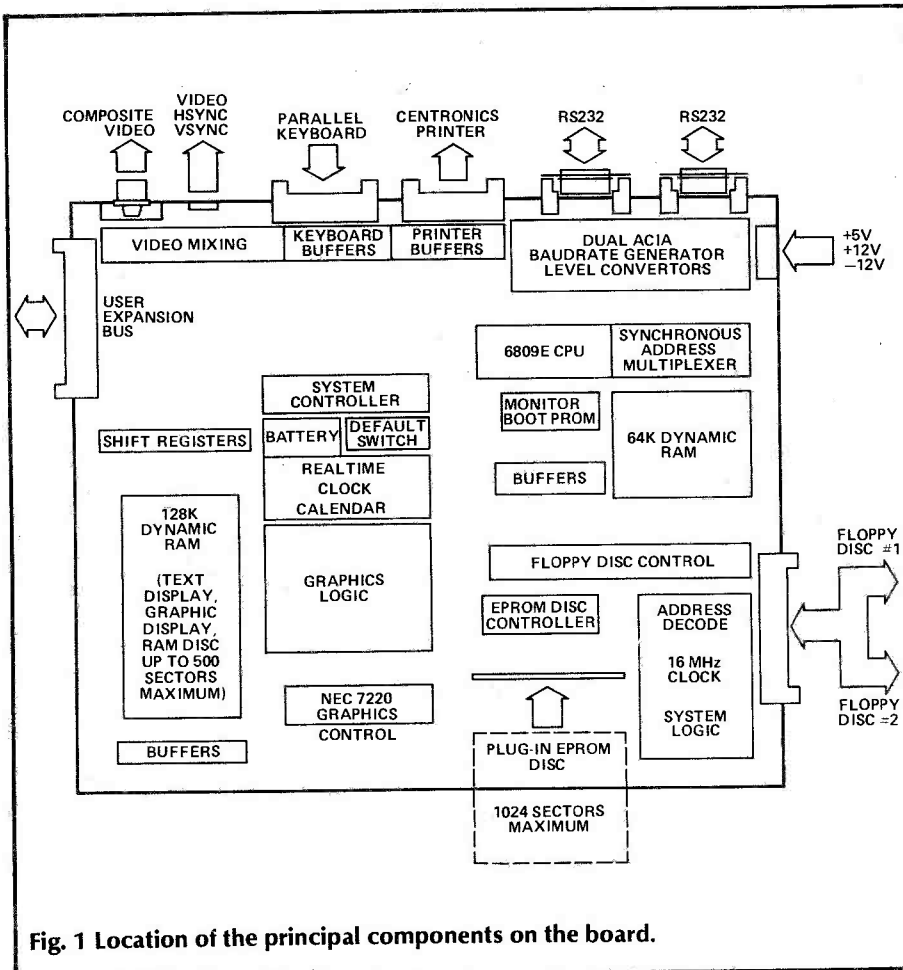
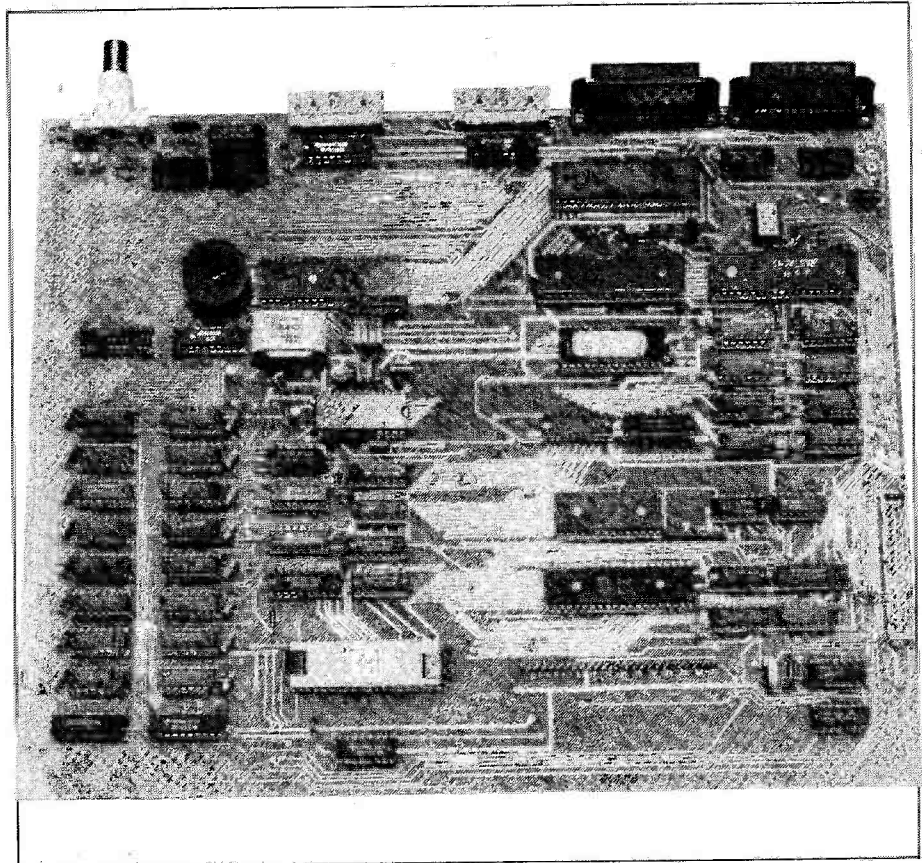


Fig. 1 Location of the principal components on the board.

using the full graphics capabilities of the machine, and 500 sectors (125K) when the machine is being used with a serial terminal and no graphics output. Its mid capacity, when using the terminal capacities of the 7220A, is exactly the size of a single density, single sided 40 track Flex disc. This enables the user to perform fast disc to disc copying with only one disc drive.

An EPROM based silicon disc which again looks to the DOS exactly like a floppy disc, but this time write protected. The EPROM disc is fabricated on its own small PCB which plugs into the main board. This allows the user to keep a number of these discs programmed for different applications. The capacity of this board is 4 EPROMS which can be 27128's, 27256's, or 27512's. These will give 64K, 128K, or 256K bytes of disc space respectively.

An on-board EPROM programmer requiring only a programming power source (for 21V EPROMS three 9 volt batteries stabilized by a zener diode can be used).

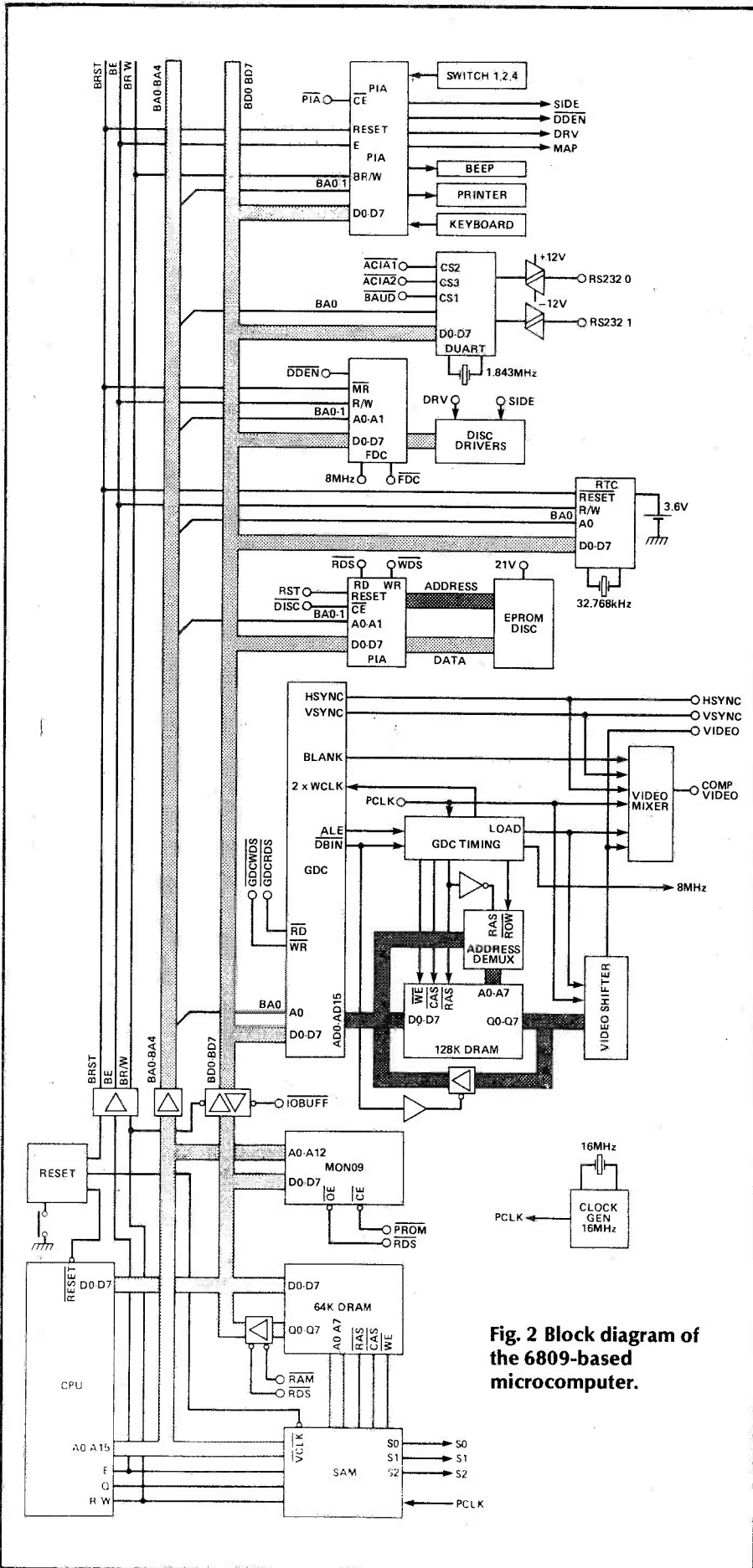


Fig. 2 Block diagram of the 6809-based microcomputer.

A battery backed-up real time clock and calendar. This is used by Flex to date stamp files. The clock chip also contains 50 bytes of non-volatile RAM, some of which is used to maintain system parameters such as baud rates, floppy disc step rates, physical to logical mapping of disc drives and start-up parameters for the graphics device.

It should be apparent by now that the board has been designed with some thought. The combination of EPROM disc and RAM disk makes it very fast indeed and in most cases disc access time is not even noticeable.

The effect of the silicon discs and the fast graphics hardware is to make the machine compare favourably with the graphics on much larger machines (in one incarnation it was used by Imperial College as a graphics terminal for a VAX). Further, the terminal emulation software and the handling of the ROM and RAM discs so that they look like floppy discs enables the system to run Flex software with no more modification than would be necessary with any other Flex computer. In fact, it will boot any Flex operating system. It is in effect a superset of existing Flex computers, not an entirely new departure that leaves the software developers years behind.

Another interesting feature of the design is the low chip count. Fully populated, and including the EPROM disk, the board has only 68 chips of which 24 are memory and five are EPROM.

We hope this brief introduction has whetted your appetite! Next month Dave Rumball will describe the design of the board and the reasoning behind his choice of chips and facilities. Succeeding articles will cover construction and use and will include a list of available software. For those who can't wait that long, the kit is available from Micro Concepts at the address below and includes full construction details. Contact them for information on prices, etc.

Micro Concepts, 2 St. Stephens Road, Cheltenham, Gloucestershire GL51 5AA, tel 0242 - 510 525.

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AUTOMATIC TEST EQUIPMENT

The writing's on the wall for signature analysis, says W.P. Bond.

The increasing predominance of VLSI, microprocessors and large memories has made the use of advanced techniques of automatic testing essential. Signature Analysis (SA) is such a technique and, although first developed over a decade ago, it plays an important part in modern ATE.

SA is a data-compression technique, introduced by Hewlett-Packard in 1970 as a field-service aid for fault-finding in microprocessor-based equipment, but with unexpected applications in functional testing. The theory is fairly complex — at least, if the maths is not taken on trust. If we accept the mathematical foundations as sturdy, the process is reasonably easy to understand.

Figure 18 shows a typical SA set-up. It is, in effect, a pseudo-random sequence generator with an external input connected to the circuit node at which system data is being monitored. The heart of the device is a 16-bit shift register whose contents can be read out on a hex display. On successive clock pulses, the register will shift, producing a binary sequence at the output, X, and an associated sequence of hex numbers on the display. Assuming for the moment that the data input, W, is held low (that is, no data is entering the shift register), the device acts just like a pseudo-random sequence generator. The feedback loop through the exclusive-OR gate, XOR2, ensures that the shift register will cycle through all its possible states (with the exception of all bits zero) whatever the initial state (as long as it was not all bits zero). The proof of this derives from the theory of binary sequences and is connected with the fact the feedback loop is effectively generating a polynomial function whose value is determined by the state of the

shift register at any given time. The state of the shift register at a particular time can, in turn, be specified by reference to preceding stages. In the simplified diagram of Fig. 19 (which shows the Fig. 18 set-up with the data input and associated OR gate removed), the input at time r, X_r , is given by the expression:

$$X_{r-16} \text{ XOR } X_{r-12} \text{ XOR } X_{r-9} \text{ XOR } X_{r-7}$$

This expression can also be written using what's called D-notation. This uses a particular operator, D (something like the differential operator of analytical calculus), to represent the effect of a delay of one clock cycle. The above expression becomes:

$$D^{16}(X) \text{ XOR } D^{12}(X) \text{ XOR } D^9(X) \text{ XOR } D^7(X),$$

where $D^n(X)$ represents n successive operations on X.

If we wanted to generate the sequence of inputs

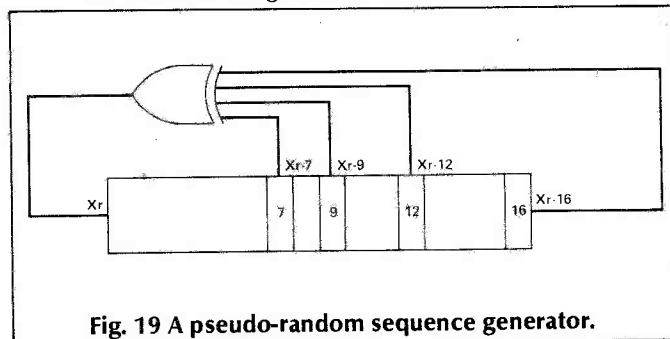


Fig. 19 A pseudo-random sequence generator.

into the Fig. 19 circuit, we could simply take any initial state of the shift register (except for all bits zero, which will never change) and work out successive values of the polynomial. We would get a sequence of ones and zeroes which would, eventually, start repeating. Starting from any single digit in the sequence and taking the next 15 digits (cycling round the sequence, if necessary) will produce states of the shift register.

It can be shown that the above polynomial will generate a sequence of 65535 digits before it starts repeating. Any device with n-stages which generates a sequence of $2^n - 1$ ones and zeroes before repetition is called, for obvious reasons, a maximum length sequence generator. In the case of the circuit shown in Fig. 19, we talk of a maximum length sequence (or m-sequence) of period $2^{16} - 1$. Using the technique of starting from one digit within the sequence and taking a string of 16 consecutive digits, we arrive at $2^{16} - 1$ smaller sequences of 16 bits each. Since there can only be 2^{16} possible sequences of 16 bits (this time including the all bits zero option), and since the m-sequence doesn't start repeating until the 65536th bit,

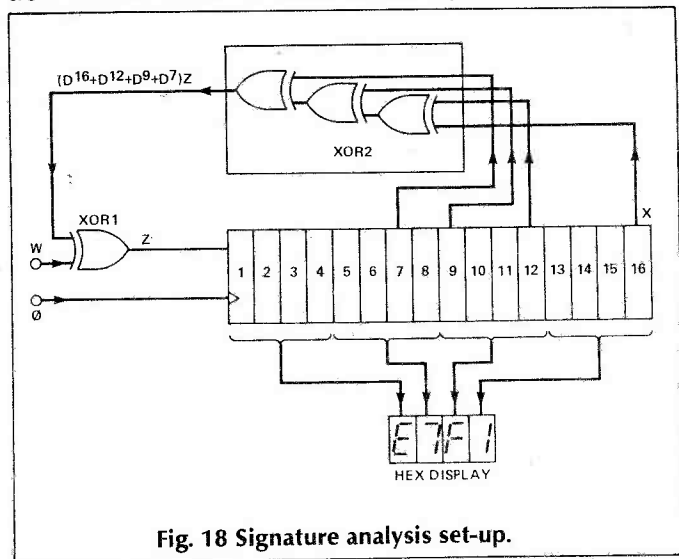


Fig. 18 Signature analysis set-up.

the m-sequence clearly gives rise to every possible state of the 16-stage shift register (with the familiar exception).

The useful thing about the m-sequence is that there is no evident structure to it. It appears to be random, although it is in fact rigidly determined by the initial state of the shift-register and the feedback (or transition) polynomial. By converting each of the states of the shift register into a decimal or hex number we can give another useful expression to this pseudo-random sequence. Table 1 shows the different ways of expressing the sequence for a 3-stage generator (Fig. 20):

CLOCK	I/P	A	B	C	HEX/DEC	O/P
1	1	0	0	1	1	1
2	1	1	0	0	4	0
3	1	1	1	0	6	0
4	0	1	1	1	7	1
5	1	0	1	1	3	1
6	0	1	0	1	5	1
7	0	0	1	0	2	0

Table 1.
Three stage shift register pseudo-random sequences.

Check for yourself that the sequence now repeats.

In the above example, the decimal/hex sequence 1,4,6,7,3,5,2 can be simply read out of the shift-register as with the Fig. 18 circuit. Whatever the number that comes up, we know exactly which number will follow it.

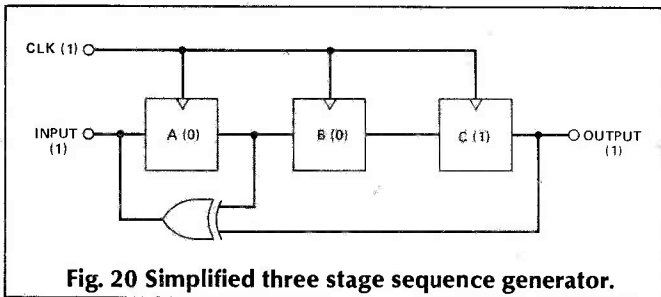


Fig. 20 Simplified three stage sequence generator.

If we now go back to Fig. 18 and start feeding data in on W input, what will happen? Left to its own devices, the shift register will cycle through its sequence of 65535 numbers, one for every clock pulse. But as soon as the W input goes high (in other words, as soon as a data bit 1 arrives on the input), XOR1 will invert the bit on the feedback line. The shift register jumps out of its pre-ordained sequence. Since this sequence includes every possible number between 1 and 65535 already, all that will happen will be that the shift register lands somewhere else in its sequence and will carry on from there. Every data high will cause the shift register to jump to a different part of the sequence, so that a given sequence of data bits will generate a new sequence of numbers in the shift register. After a precise number of clock signals — enough to cover all states of the unit under test — the shift register is stopped and a final number can be read out. This is the signature of the input sequence (also known as the cyclic redundancy code, or CRC). Assuming all the circuits concerned are properly initialised and the time window does not deviate, the signature will be the same each time the SA device sees the same data input. Clearly, any single bit error is certain to be detected, since such an error will cause one and only different jump in the sequence. Multiple bit errors will cause the sequence to jump several times, and it may end up where it would have been if no error had occurred. The chances of this

happening are very small — with a 16-bit shift register, they amount to one in $2^{16}-2$. There is an approximate 99.998% chance that a multiple bit error will result in a wrong signature and so be detected. This near certainty is possible because the original sequence is, in effect, random.

The main advantage of the signature analysis technique is that it is capable of detecting time related errors and can be used to test microprocessor-based systems, for example, or large memory configurations at full system speed. SA procedures require access to a test point for data input, access to a clock signal and the provision of start and stop signals to determine the time window (Fig. 21). The UUT's own clock is often used although it may be more convenient to use other bus signals (RD and WR), for example. Start and stop signals are often provided by a stimulus program built-in to UUT hardware.

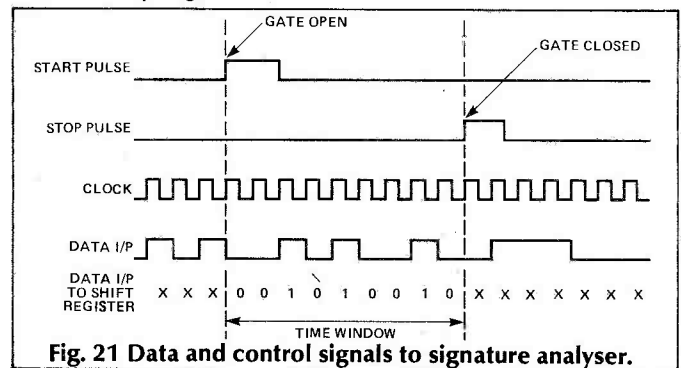


Fig. 21 Data and control signals to signature analyser.

Figure 22 shows how SA can be applied to test an n-bit ROM. A counter is used to cycle through the ROM's address range and the outputs are monitored using the system clock as the SA clock. Start and stop signals are both taken from the MSB of the counter and therefore need to trigger on opposite edges. Using this method, there is no real limit to the size of memory that can be tested, which is particularly important with regard to newer devices and technologies like bubble memory with sizes upwards of one megabit.

The same principle can be used to test RAM, although a method of loading the memory with known data is required. In this case, the stimulus program which initializes the system, provides start and stop pulses and exercises all the test nodes may utilise RD and WR signals as clock inputs. Signatures arrived at when writing data to RAM using WR as a clock signal could simply be compared with signatures arrived at when reading data back using RD as a clock input. This is a less complicated procedure than one using the system clock of the UUT.

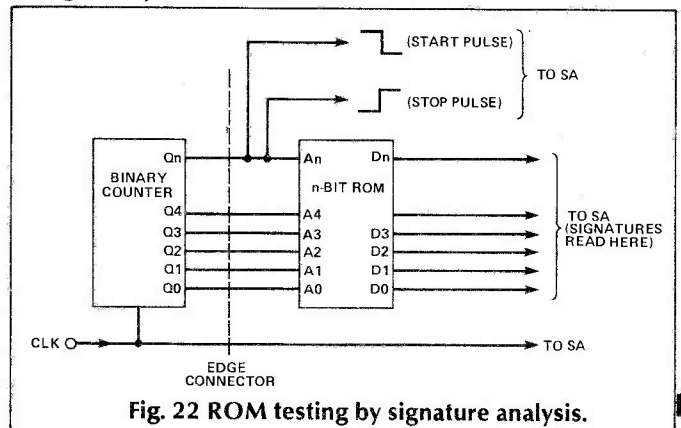


Fig. 22 ROM testing by signature analysis.

One difficulty in testing microprocessor-based bus systems is the presence of feedback loops. A bad signature may be propagated around the loop, for example on a data bus. In such a case, the presence of a fault could be detected but not isolated to component level. In the mpu system of Fig. 23, interrupts must first be disabled or masked if any meaningful and repeatable signatures are to be derived. The data bus must be broken by means of jumpers, switches or buffers and the processor should be allowed to free-run, cycling through its address range. This last can be achieved by putting an instruction on the mpu's now disconnected data inputs causing the program counter to increment and repeat as long as the instruction is present. Normally a no-operation (NOP) instruction will do the trick.

Signatures can be taken from the address bus. If these are wrong, either the micro is not free-running, or there is an address fault. Then the ROMs, RAM and I/O can be enabled in turn and their outputs verified on the data bus. Once again, the RAM must be loaded with known data. If the data bus cannot be isolated, one can often utilise tri-state buffers to isolate the mpu and then force an instruction on to it, vectoring it to a particular address in ROM containing an analysis routine. But such complications are enough to ensure that ATE only uses signature analysis to test large memories, circuits without feedback and easily controllable mpus.

Bus Emulation

There are other options for testing mpu and bus-structured boards, of course. Bus Timing Emulation is a technique developed by Columbia Automation (now Zehntel) for use on their Columbia 2000ATE model. This is currently being used by Smiths Industries for testing complex modules.

Emulation is, in effect, a form of real-time simulation, originally designed as a microprocessor development tool. Unlike simulation testing, emulation is perfectly suited to the uncovering of dynamic faults — even with the UUT being run at full system speed.

To use emulation to test mpu-based bus-structured we must know the timing specifications and protocol of the bus — which are, of course, determined by the controlling mpu and are largely independent of any particular devices attached to the mpu bus. The timing emulator in the ATE is used to replace the mpu. It can be synchronized with the UUT clock and itself produces synchronous timing signals to different isolated areas of the bus.

Bus structure allows the functional grouping of sub-circuits into blocks like RAM, ROM and PIO so that the ATE can apply and measure data within each block simultaneously. For stimulation and monitoring to work, the ATE software needs to be able to manipulate data, check it instantaneously and during a time window and tri-state circuit blocks and components — all in real-time.

Bus timing emulation may be combined with static (step-time) testing of read, write, buffer and control functions and with signature analysis of the UUT with the mpu installed. In this way, static faults, component dynamic faults and microprocessor faults can all be detected — the main drawback being the need to remove or tri-state mpus.

Memory emulation eliminates the need for processor removal. The technique was developed by Genrad Inc. and approaches the problem of dynamic real-time testing from the other end. The UUT pro-

cessor is clipped with a header, allowing it to remain resident while being controlled by the ATE.

The ATE can selectively overdrive test signals and force a processor to redirect its activity from memory resident on the UUT to ATE-supplied memory, thus creating a memory overlay. On reset, the micro will go through its reset routine. Where an OPCODE FETCH is generated (as with the Z80 and 8085), the program counter is reset to 0000h — where the first instruction following reset will be stored. Other micros (such as the 6800 and 6502) load the contents of FFFeh and FFFFh into the program counter as the vector address of the reset routine.

If the mpu control signals (ALE on the 8085, VMA on the 6800 or MREQ on the Z80, for example) have been overdriven by the ATE, the micro will — after reset — address ATE memory as though it was its own. This stage is known as 'capture mode' and the UUT memory is masked from the mpu.

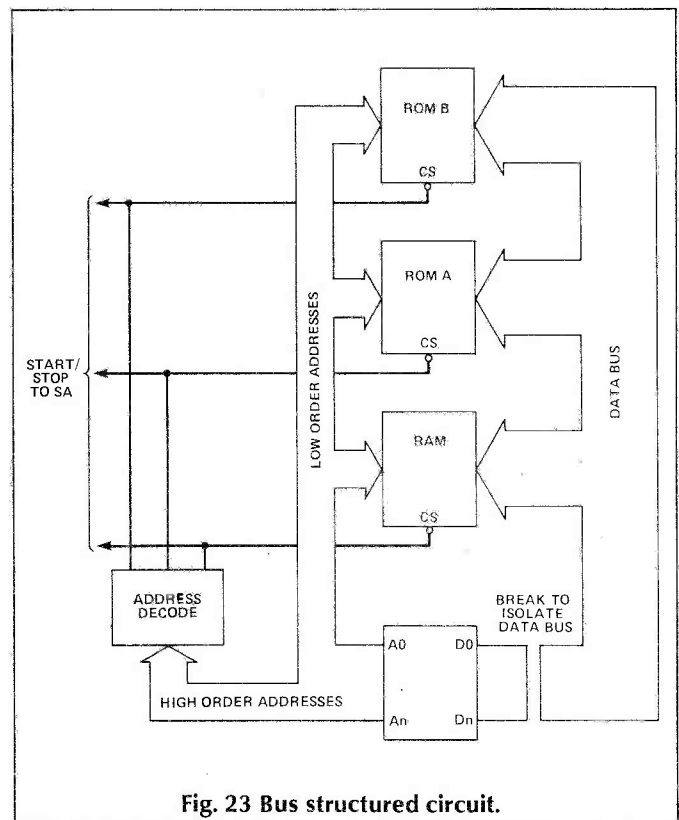


Fig. 23 Bus structured circuit.

In the next stage of the process, the UUT can be tested by using 'target routines' stored in ATE memory. These are of two main types: the diagnostic test routine (DTR) and the idle routine. Tester memory is partitioned into segments which can be placed anywhere in the UUT processor address map, so that the mpu may still have access to parts of its memory or to talkable devices on the bus. DTRs are used to test functional blocks of the UUT, while an idle routine keeps the micro in a known condition under tester control during changeover from one to another test procedure.

In this way, the micro retains access to the system as a whole, while allowing selective real-time testing at full system speed. Stimulus and test measurements can be synchronized and the whole process closely duplicates the actual performance of the UUT, allowing the detection of interactive and component dynamic faults which might otherwise be hidden from a test procedure.

ETI

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1985 PROJECT/ FEATURE INDEX

Listed below are all the major articles we have published in the last 12 months, including those appearing in this issue. We have not listed regular features such as News Digest, Read/Write and the various columns in the Etcetera section but we have included Tech Tips and Reviews and put each of them under separate headings. These sections are quite short so we have not bothered to cross-reference any of the entries, but articles under the main Projects and Features headings are listed twice or even three times in some cases to make them as easy to find as possible. We have also listed corrections to projects where necessary.

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PULSE GENERATOR

Mike Meakin describes another of his low-cost test equipment modules, a versatile pulse generator board.

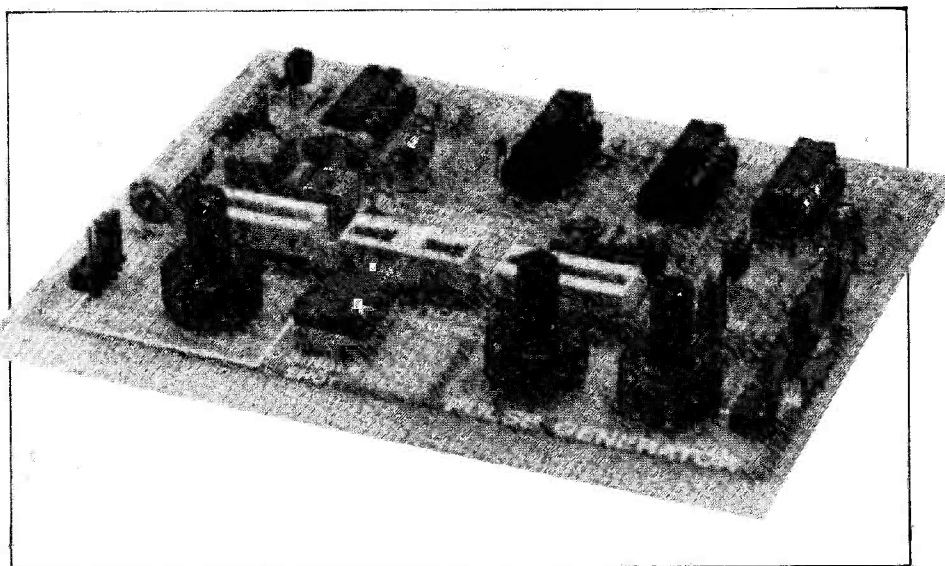
This instrument has been designed as one of a series of test gear modules and complements the power supply which was presented in our October issue and the waveform generator which appeared in the November issue. Each module is assembled entirely on one PCB, complete with all switches, potentiometers, sockets, and so on. This removes the need for cases and other hardware and so reduces the cost.

Further expense is avoided by using the power supply module to provide the operating voltages for the other modules, thus eliminating the duplication involved in providing separate power supplies. Ideally, therefore, the power supply module should be built and used to drive the pulse generator, but in practice there is no reason why another supply should not be used if you don't need all the facilities of the main PSU module.

The pulse generator provides output pulses with widths variable from 1us to 1s at repetition rates from 1Hz to 1MHz. CMOS, TTL and open collector outputs are provided together with a sync output. The internal clock can be switched out when not required and the generator can then be driven from an external clock or operated in single shot mode. The design is inevitably a compromise between complexity and cost but it is felt that most of the facilities the average hobbyist is likely to require are provided.

The heart of any pulse generator is the monostable timing circuit, and a large number of IC devices are available to provide this function. However, obtaining a very wide timing range with sensible values of R and C limits the field.

The 555 timer would seem well suited to this application but the



practical minimum pulse width obtainable from this device is about 10us. The 74121 series of TTL monostables require large values of timing capacitors and behave erratically at high duty cycles. The 74C221 chosen for this circuit is a CMOS device with a performance which is superior to that of both the 4528 and 4538 monostables from the 400 series. A six decade timing range can be achieved with changes of capacitance only and it behaves well at high duty cycles.

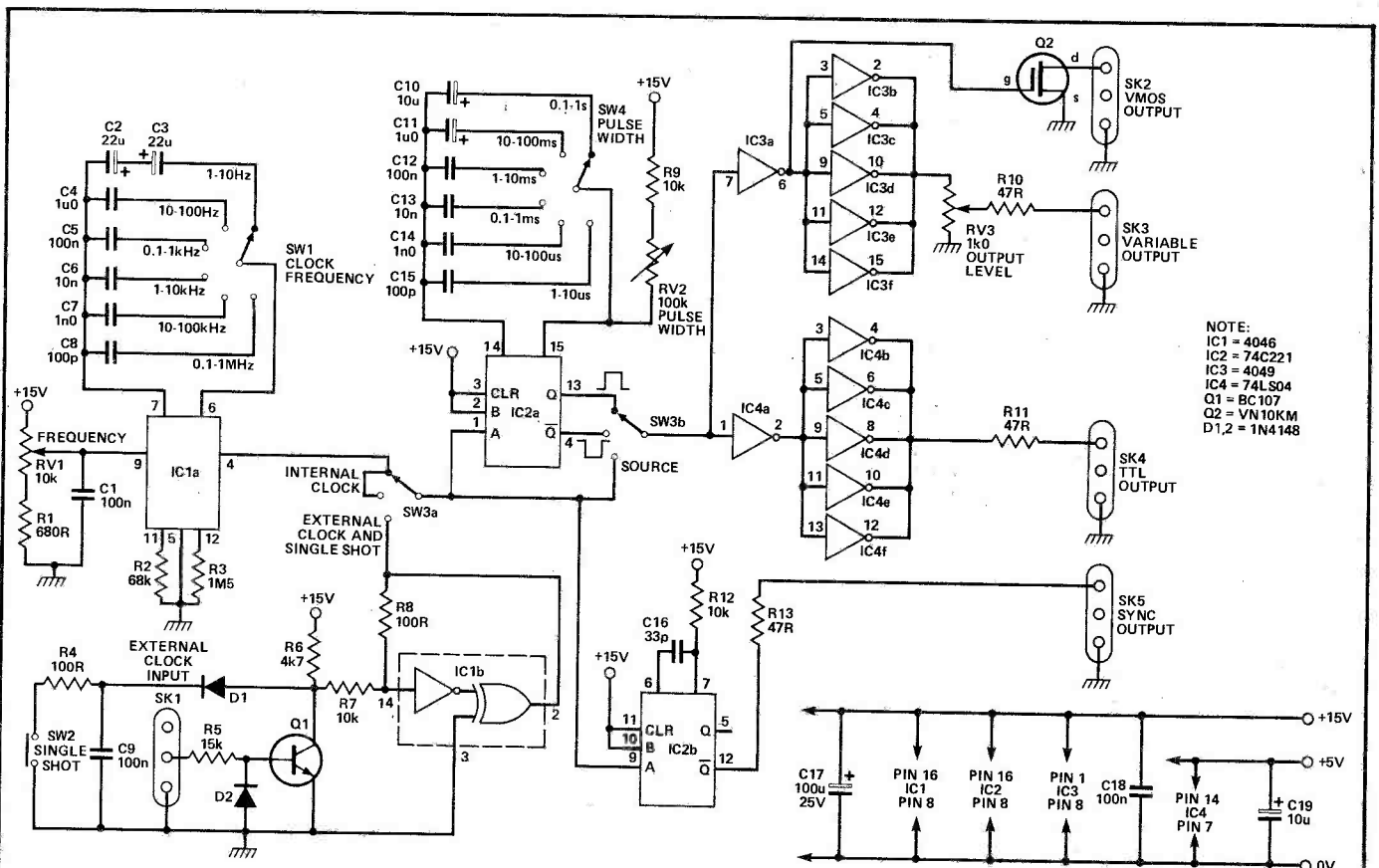
Three outputs are available on the board. The TTL output is provided by five inverters in parallel and is capable of driving ten standard TTL loads. The input is driven from a 15V CMOS output but protection is given by an internal diode. A Schottky device must be used in this position. The 0 to 15V variable output is obtained from five paralleled CMOS buffers and a potential divider, giving a maximum source impedance of about 300R. Some protection is provided by the 47R series resistor. Finally a VMOS transistor provides an 'open

collector' or more correctly an open drain output. This sturdy device can sink up to 500mA and withstand 60V. It is ideal for use as a relay or LED driver.

Construction

Because the switches and potentiometers are all mounted directly onto the PCB, any labelling of functions and switch positions will also have to be done on the board itself. Various methods of doing this were described in the Waveform Generator article in last month's issue and will not be repeated here. However, if you want a particularly neat end result you will have to either screen print the board or use rub-down lettering, and both of these processes must be undertaken before any other constructional work on the board is started.

Installation of the components should begin with the wire links and progress in the normal fashion through hardware devices (switches, sockets, etc), passive



NOTE:
 IC1 = 4046
 IC2 = 74C221
 IC3 = 4049
 IC4 = 74LS04
 Q1 = BC107
 Q2 = VN10KM
 D1,2 = 1N4148

Fig. 1 Complete circuit diagram of the pulse generator. The board is intended for use with our earlier power supply module so no PSU circuitry is shown here.

HOW IT WORKS

The VCO section of a 4046 phase lock loop IC is used as a clock. This circuit gives a 50% duty cycle square wave output at pin 4 of IC1. The six decade timing capacitors are selected by SW1. For the lowest frequency range two 22u tantalum capacitors are connected back to back to give a non-polarized capacitor whose value should ideally be 10u. The timing resistors R2 and R3 in conjunction with the voltage obtained from RV1 set a 1:10 frequency range.

SW3a selects either the VCO output or the external and single shot inputs. The section of the 4046 normally used

as a phase comparator is connected as a Schmitt trigger to clean up the input pulses. These are obtained from an external clock via a transistor buffer whose input is protected by a series current limit resistor R5 and reverse polarity protection diode D2. The external clock input will operate either from a pulse source or an AC signal as long as it crosses the 0.6V turn-on potential of the transistor. The single shot or manual pulse is obtained by shorting the Schmitt trigger input to 0V with SW2. It is de-bounced by the R6, C9 time constant.

Half of the 74C221 is connected as a

negative-edge non-retriggerable monostable. SW4 selects the timing capacitor and RV2, R9 alter the time period over a 1:10 range. The input pulse also triggers the other half of IC2 to give a negative going sync pulse of about 500ns at SK5. This is coincident with the leading edge of the output pulse and can be used to trigger an oscilloscope. SW3B directs either a positive going pulse, a negative going pulse or the source signal to the output stage. The VCO square wave signal, the external clock or manual pulses can thus be sent directly to the output.

BUYLINES

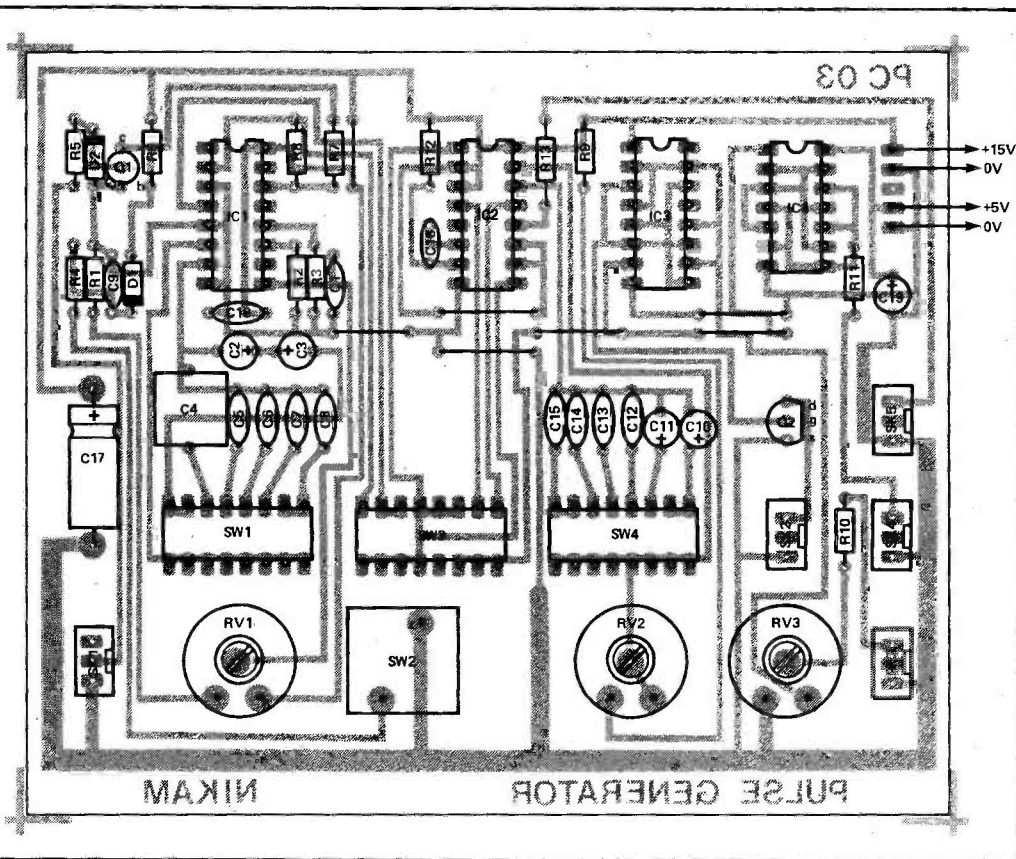
The fixed resistors, the capacitors and the semiconductors are all widely available with the possible exception of the 74C221 which can be obtained from Cricklewood. The only supplier we know of for the carbon track presets is RS Components who will only accept orders from trade and professional customers. However, Crewe Allen & Co of 51 Scrutton Street, London EC2 will obtain parts from them on payment of a small handling charge. The stock numbers are 184-350 for the 10k preset, 184-388 for the 100k preset and 184-322 for the 1k0 preset.

The DIL switches used on the prototype were an ERG DS16D 1-6 for SW1 and SW4 and an ERG DS16D 1-3+1-3 for SW3. ERG will not handle small orders but electronics clubs, schools and others prepared to order reasonable quantities could try contacting them at Luton Road, Dunstable, Bedfordshire LU5 4LJ, tel 0582 - 62241. Unfortunately, we do not know of anybody who stocks similar switches or will supply the ERG switches in small quantities. The board has been laid out to accept eight position switches as well as six position ones and this would permit an

RS stock number 337-532 DIL switch to be used in the SW1 and SW4 positions. The extra switch positions would simply be ignored in use. RS do stock a two-pole DIL switch but the sections are ganged, making it unsuitable for use as SW3. A standard eight way DIL switch could be used but the operator would always have to make sure that only one switch in each group of four was selected at any one time. The only other alternative we can think of is to use standard rotary or slide switches and glue or bolt them to the board.

PROJECT: Pulse Generator

Fig. 2 The component overlay for the pulse generator PCB.



PARTS LIST

RESISTORS

R1	680R
R2	68k
R3	1M5
R4	100R
R5	15k
R6	4k7
R7, 9, 12	10k
R8	100k
R10, 11, 13	47R
RV1	10k carbon track preset with integral knob
RV2	100k carbon track preset with integral knob
RV3	1k0 carbon track preset with integral knob

CAPACITORS

C1, 5, 9, 12, 18	100n polyester
C2, 3	22u 16V tantalum
C4	1u0 polyester
C6, 13	10n polyester
C7, 14	1n0 polyester
C8, 15	100p polystyrene
C10, 19	10u 16V tantalum
C11	1u0 35V tantalum
C16	33p ceramic plate
C17	100u 25V axial electrolytic

SEMICONDUCTORS

IC1	4046
IC2	74C221
IC3	4049
IC4	74LS04

Q1

Q2

D1, 2

BC107

VN10KM

1N4148

MISCELLANEOUS

SK1-5	3-way Molex PCB plug with polarising post
SW1, 4	1-pole 6-way DIL slide switch
SW2	PCB mounting keyboard switch
SW3	2-pole 3-way DIL slide switch

PCB; IC sockets if desired, 3 off 16 pin and 1 off 14 pin DIL.

components (resistors and capacitors) and finally the active components (the ICs, transistors and diodes). Take care that tantalum and electrolytic capacitors and the various active components are all inserted into the board the right way around. It is best to use sockets for the ICs but there is no reason why they should not be soldered directly into the board if you prefer and are careful. Since the DIL switches may suffer slight movement when operated, it is best to avoid sockets and solder them directly into place.

When the board is complete, connect up the +5V and +15V rails from the power supply module or from another regulated power supply. The current drawn from the main supply rail, the +15V one, will be about 25mA. Set SW3a to internal clock, the frequency control potentiometer to mid position and the frequency range to 0.1-1kHz. Select source and then apply power to the board.

Both the variable and the TTL outputs can be monitored either with an audio amplifier or a piezo sounder. The positive and negative

going pulses should be checked with the width switch set to 0.1-1ms to confirm that the monostable is operating. Finally, a LED in series with a 1k0 resistor should be connected between the VMOS output and the plus 15V supply, observing the correct polarity of the LED. Select negative going output pulse, external clock and pulse width range 0.1-1s. If the single shot switch is pressed the LED should momentarily illuminate. Those who have access to a scope can of course test the board more comprehensively.

ETI

SPECDRUM DRUM SEQUENCER

Use a Spectrum to control your kit of drum synths — it's the only way to beat time, courtesy of Digisound.

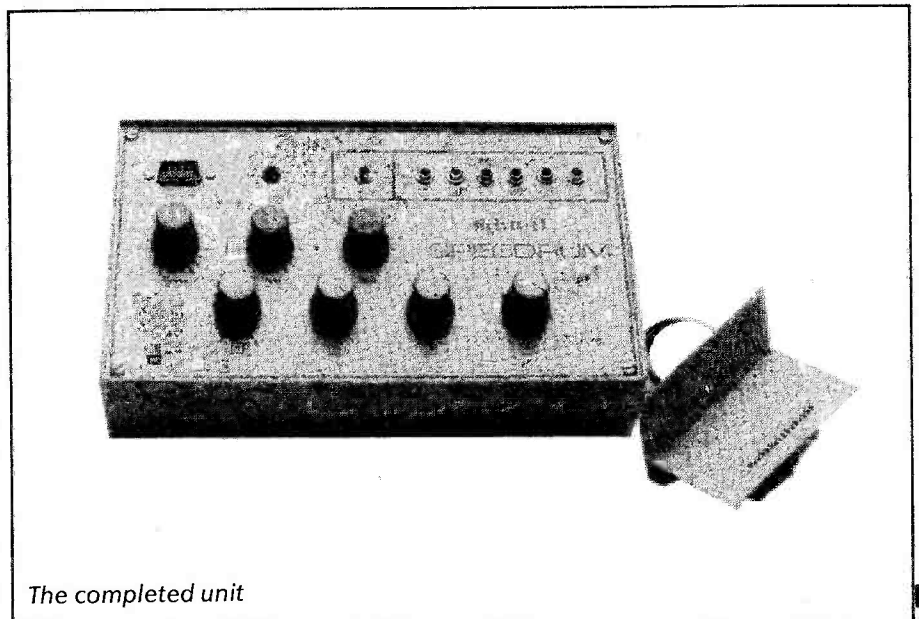
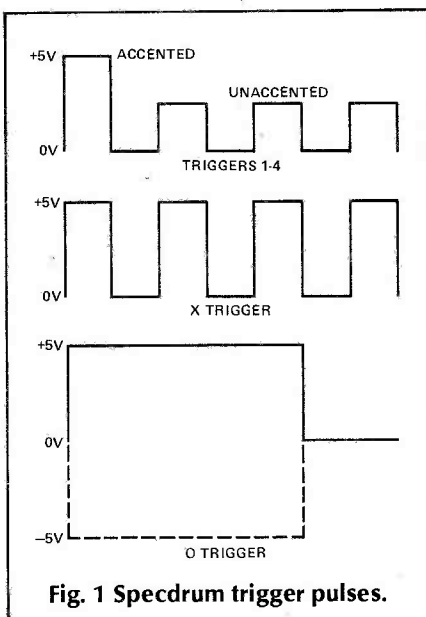
The Specdrum drum sequencing package is a cost-effective and highly flexible method of generating rhythmic structures using a Spectrum or Spectrum + computer, a simple interface and cassette software running to about 15K of machine code. An external clock input is provided to allow synchronisation with tape machines or other devices and the hardware can also be used as a conventional joystick interface when not running the Specdrum software. It uses the Spectrum PSU and is compatible with Interface 1, microdrives and Sinclair-type printers.

The software incorporates a pattern editor (16 patterns of up to 32 events each), a chain editor (eight chains of up to eight patterns each), a sequence editor

(eight sequences of up to 12 chains each with or without repeats) and a track editor (two tracks of 24 combined sequences, chains, patterns and repeats). There is real-time pattern modification and the facility for interfacing microdrives and tape. The external sync operates on a 10V p-p max. level. The interface allows around 60 events per second to be programmed and can store more than 70,000 events per track.

The events are trigger pulses intended to be sent to drum synthesizers under the control of the sequencer. There are four accented triggers and two unaccented triggers. Accenting affects the quality of the output of most drum synths. Data lines D0-D3 produce trigger pulses whose

level (from 0V to 5V) can be controlled by four individual pots. All these pulses may be simultaneously accented by means of data line D6 — an accent effectively overriding the potentiometer setting and producing a 5V pulse at the output whenever it occurs (Fig. 1). Data lines D4 and D5 generate unaccented triggers called O and X, respectively. The O trigger consists of an uninterrupted output at either +5V or -5V (hardware selectable) between two or more consecutive events. This allows the unit to provide open/closed hi-hat control — an inverted, -5V, pulse being necessary to the hi-hat facility offered by the Digisound 'El-Cymb' unit (one of a series of Digisound Digi-Drum units which



HOW IT WORKS

The complete circuit diagram for the interface is shown in Fig. 2. It may be divided up into a number of circuit blocks: address decoding; trigger generation and accenting; joystick interface; and a master clock.

Memory address decoding is performed by IC4 and IC5a, d, e and f, which generate two hardware control signals, WRSEL and RDSEL. The decoding checks for A5, so that the hardware appears at addresses 1F, 5F, 9F and DF (hex). This simplified I/O decoding is quite adequate in this application and does not conflict with other Sinclair hardware. In fact, the software is designed to make full use of micro-drives if they are available.

The decoded RDSEL signal directly controls the two enable pins of an octal buffer (IC2), which is responsible for reading in the appropriate switch status from a standard Kempston joystick. With a logic 0 on the enable pins, the joystick position is passed to D₀-D₅ of the data bus. Data bit D₇ is used to transfer the hardware clock which is responsible for timing duties, synchronization of the display and memory latching. This clock is built

around IC6, a 555 configured for astable operation. Potentiometers RV5 and RV6 provide, respectively, fine and coarse speed/tempo control. The output of the 555 is taken to the break connection of jack socket J1. This allows an external clock to be used for synchronization. Any incoming clock signal is cut down by the resistor/zener diode network connected to the J1 'make' connection. The +5V signal is buffered and inverted by IC5b and reinverted to generate CLK and $\overline{\text{CLK}}$ signals, switchable at S1. This feature is included so that clock signals with extreme duty cycles may still be used. With such signals, inversion may be necessary to allow the software enough time to carry out the display routines. When there is insufficient time for the software, the display is drawn in stages. The third position of S1 grounds the clock, so that the hardware may be used as a conventional joystick interface. If this was not done, games software might mistake the ungrounded incoming clock signal for the fire button! The normal address location of joysticks in games software is 1Fh, making them compatible with this unit.

The remaining hardware is concerned with generating the six trigger pulses. With a logic 1 on WRSEL, IC1 (an octal D-type latch) is enabled and data lines D₀-D₆ pass valid trigger information to the rest of the circuitry. D₀-D₃ are the four channel triggers to which an accent control may be added. This information is generated by D₆ and accents all triggers simultaneously by ANDing the accent pulse with the outputs on D₀-D₃. It is possible to individually regulate the level from 0 to 5V on each trigger by means of potentiometers RV1-4, which control the amount of feedback from the output to the individual channel inputs. The presence of an accent pulse takes all levels to 5V. The trigger outputs are taken off the potentiometer wipers and each is buffered by one of IC8's four op-amps.

The O and X triggers are treated in a different manner in software and are not provided with an accenting facility. The X trigger on D₅ is treated like a fully accented trigger, providing a positive-going 5V pulse which returns to 0V between two adjacent events. The O trigger on D₄ is used to generate an uninterrupted output bet-

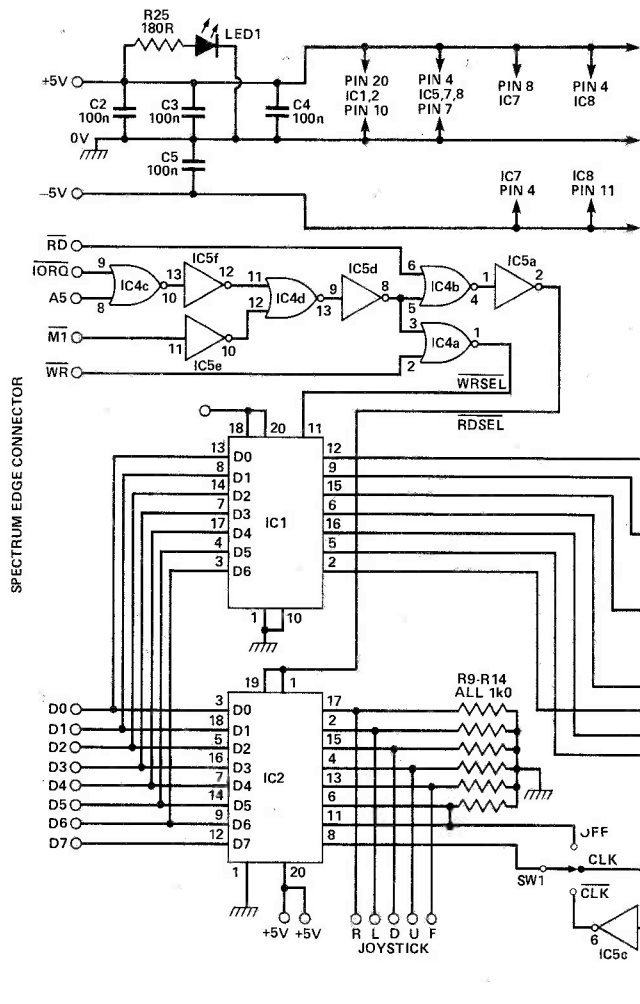


Fig. 2 Complete circuit diagram (positive 0 trigger)

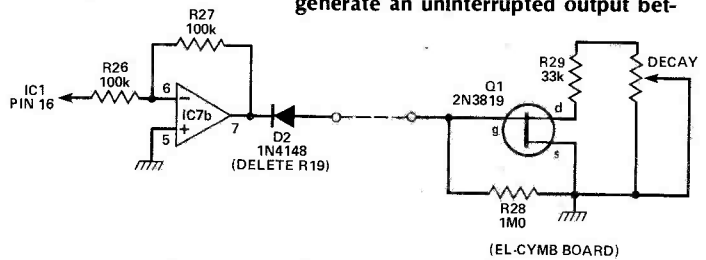
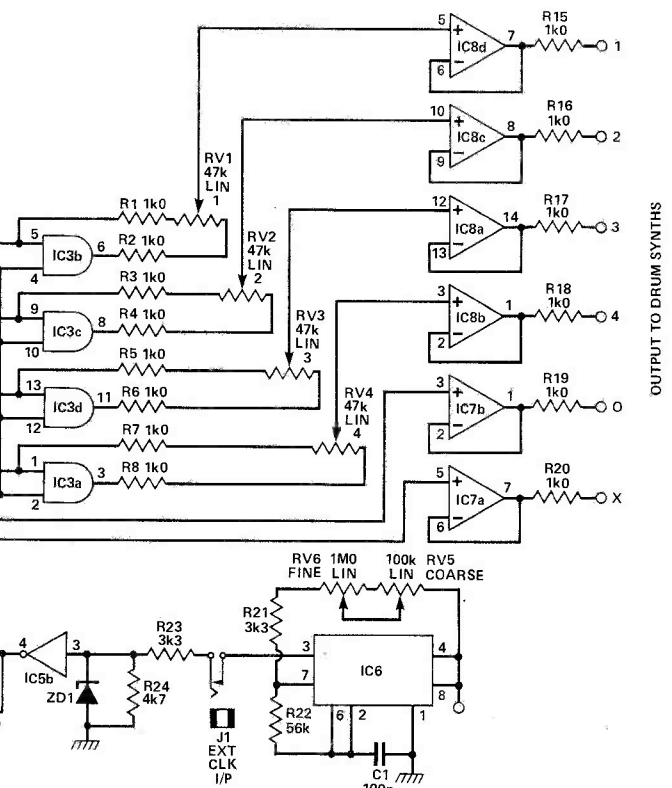


Fig. 2a Modification for use with El-cymb or other negative trigger device



ween two or more consecutive events. The O and X signals pass directly to output buffers configured around the two halves of IC 7. The O trigger buffer may be arranged to invert the incoming 0 to +5V pulse, generating a 0 to -5V signal. A negative voltage can be used to open and close the signal path between the drain and source pins of a 2N 3819 FET in order to control certain units, like the El-Cymb. R29, the resistor between the drain pin and the decay pot, is responsible for setting the difference in decay characteristics and may be altered. The modification for the El-Cymb is shown in Fig. 2a. The diode that replaces R19 is included to block any positive voltages which if they occurred would probably result in the destruction of the FET.

The unit is powered by +5V from the Spectrum PSU and draws around 80mA on the positive rail. The Spectrum can withstand this for long periods of time even with Interface 2 and microdrives attached. Capacitors C2-C5 are for decoupling purposes and LED1 provides a power-on indication.

PARTS LIST

RESISTORS (5%, 1/4 W carbon film)

R1-20	1k0
R21, 23	3k3
R22	56k
R24	4k7
R25	180R
R26, 27	100k
RV1-4	47k lin.
RV5	100k lin
RV6	1M0

CAPACITORS

C1-5	100n polyester
------	----------------

SEMICONDUCTORS

IC1	74LS373
IC2	74LS244
IC3	74LS08
IC4	74LS02
IC5	74LS04
IC6	NE 555
IC7	MC 1458
IC8	LM 348
D1	5mm Red LED
D2	1N 4148
ZD1	5V6 400mW zener

MISCELLANEOUS

J1-7 3.5mm mono jack sockets, 9-way D-Plug, Spectrum edge connector, 8-way Molex sets (2 off), 16-way ribbon cable (1m), case with printed and punched panel, K9 control knobs and caps (7 off), SW1 1 pole, 3-way rotary switch, PCBs.

BUYLINES

The complete kit of parts, including software but excluding ordinary wire and solder, is available from Digisound Ltd., 14-16 Queen St., Blackpool, Lancs. FY1 1PQ. The cost is £43.47 inclusive of p&p and VAT. Digisound are also making available a set of PCBs and the software on cassette for £18.40 inclusive.

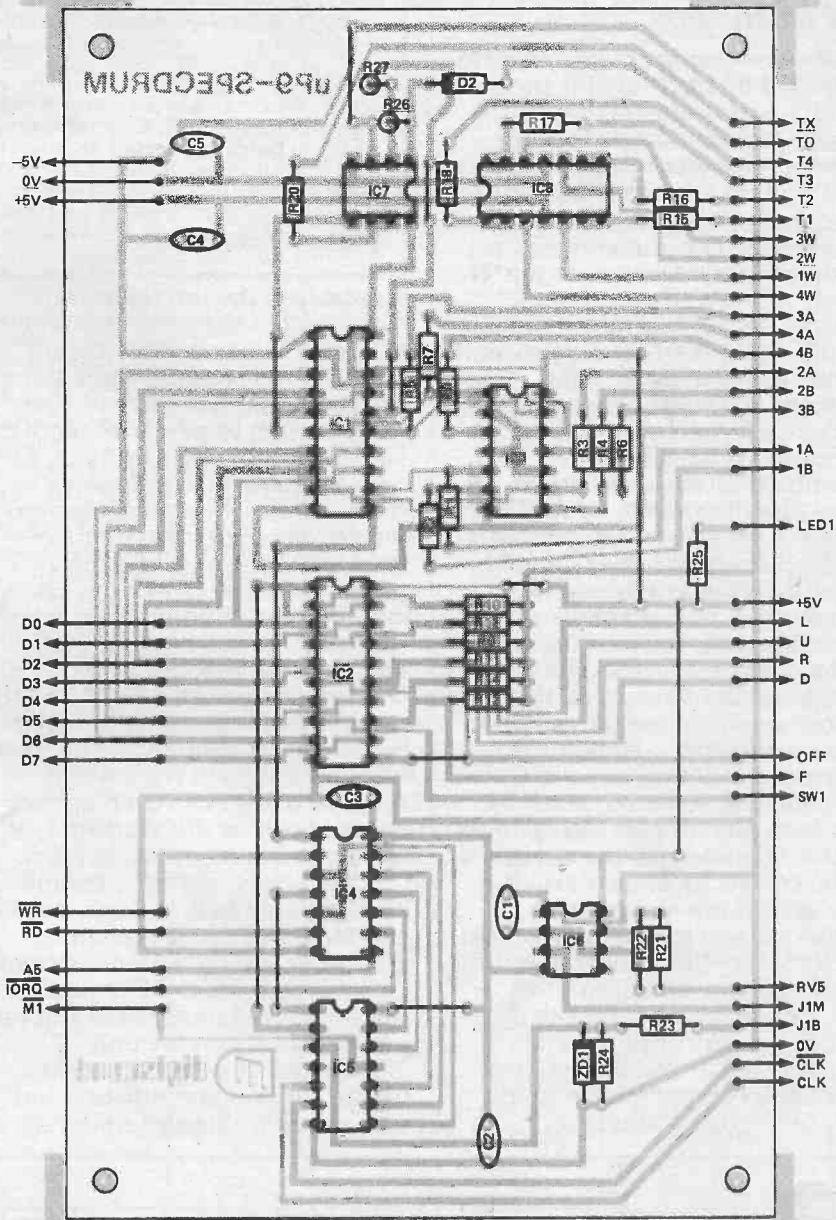


Fig. 3 Component overlay for main board.

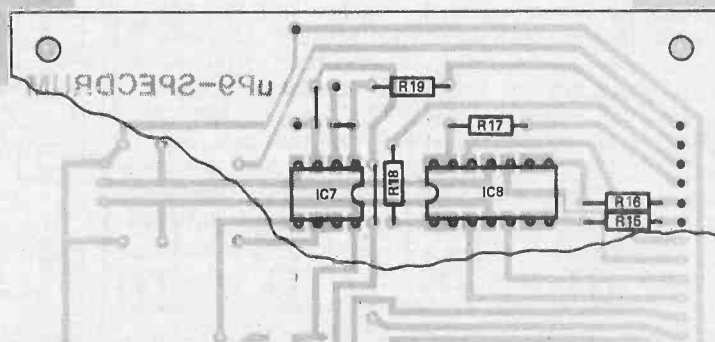


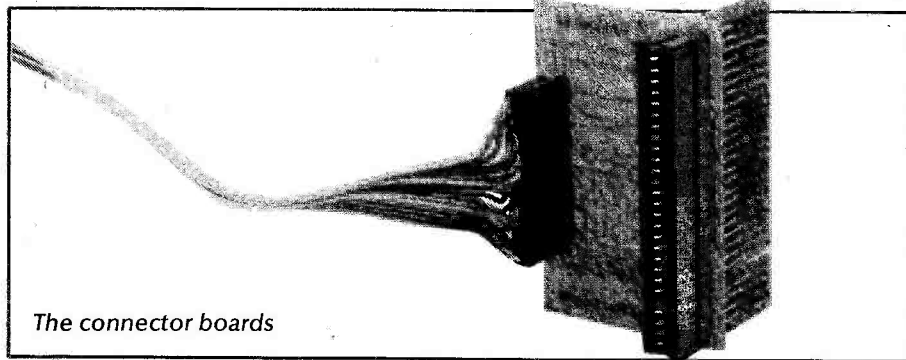
Fig. 4 Changes to overlay for positive 0 trigger generation.

can be operated with this sequencer).

Construction

The component overlay for the main PCB (marked uP9) is shown in Fig. 3 — this arrangement generates an inverted O trigger. The changes needed to generate a positive O trigger are shown in Fig. 4, Figure 2a shows the circuit of the inverted O output and the modifications necessary to the 'El-Cymb' module to produce a variable decay. Assembly is a fairly simple matter and should proceed in the normal manner: links, resistors, IC sockets, capacitors and so on. When all of the components have been assembled on the main board, it should be thoroughly treated with a solvent cleaner and inspected for dry joints and solder bridges. Insert the 28-way edge connector into the PCB marked uP8 and with the PCB evenly towards the body of the connector solder the two parts together. Then bend the exposed ends of the pins so that they meet evenly. Slide the edge connector PCB (marked uP2) between the two rows, ensuring that each pin lines up with a finger on this PCB and that the cut-out is in the correct location. Push the PCB against the rear of the connector and solder in place. Do not let solder flow closer than 1 cm from the exposed edge of this PCB, or it may interfere with the proper location of peripherals.

Using the available case and panel, the connections from the Spectrum edge connector



assembly to the interface are hardwired to the main PCB and made via Molex connectors on uP8. This necessitates the cutting of a small slot in the plastic case wide enough to pass the length of 16-way ribbon cable through. Be sure not to reverse the Molex connections when plugging onto the edge connector assembly — the easiest way to avoid this is probably to find (and if necessary mark) the earth connection on uP8 (two pads joined near the slot). Then, ensure that this is connected to earth on uP9 and the rest of the connections will follow in the correct sequence. The panel wiring is shown in Fig. 5 and is simply a matter of matching the connections on this diagram with the connections shown in Fig. 3.

Once construction is complete and fully checked, the unit may be connected to the Spectrum computer and the latter switched on. At switch-on, the TV/monitor display should be as usual and the power-on LED on the unit illuminated. If anything seems wrong, turn off immediately and recheck all wiring and soldering

until the error is located.

In Use

The users' manual which accompanies this package provides comprehensive information on how to use it. The unit will function with most analogue or digital percussion sound generators currently available. The sound generators may be connected to the triggers in any desired manner, bearing in mind the open/closed hi-hat function. As an example of the system's flexibility, it is possible to trigger two drum modules from a single output, adjusting the dynamic sensitivity of the modules so that one is triggered by an unaccented (low level) trigger and both by an accented (high level) trigger.

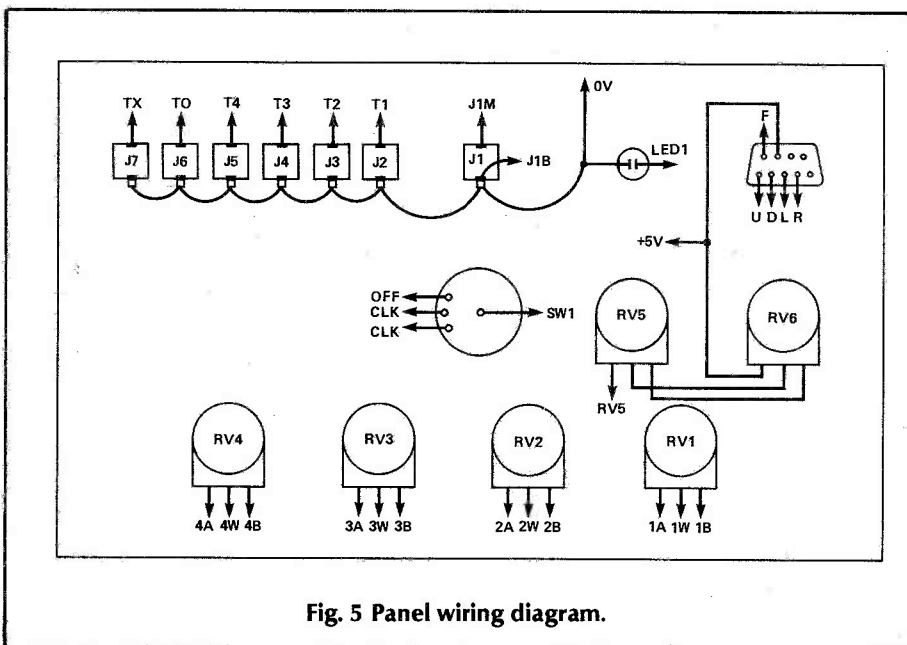


Fig. 5 Panel wiring diagram.

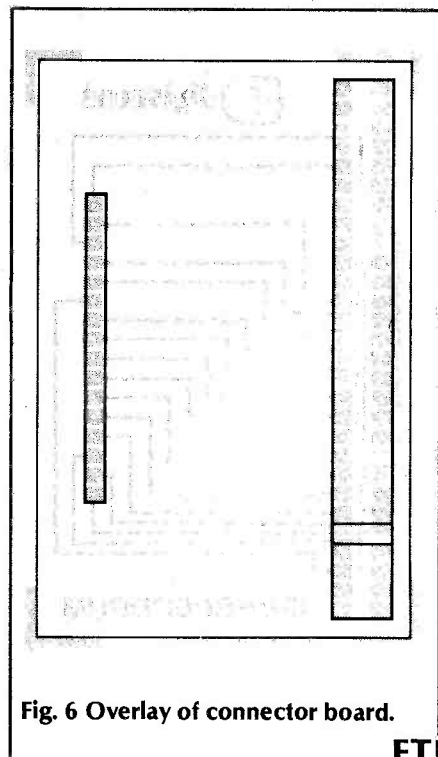
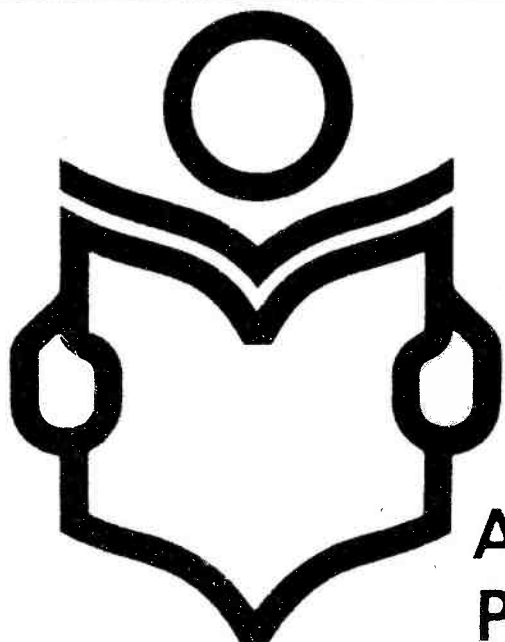


Fig. 6 Overlay of connector board.

For help with Reading and Writing

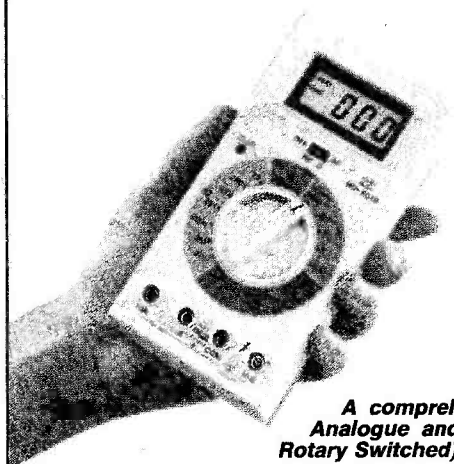
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ETI

DI COMPRESSION GATE

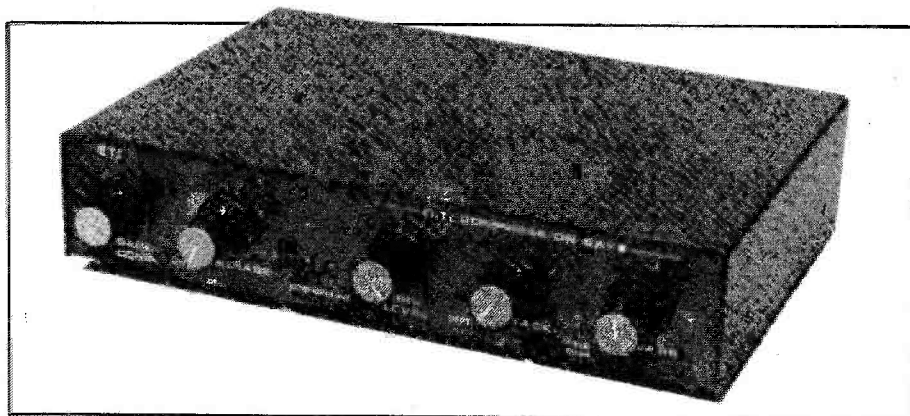
The first ETI Sound Processor is a unit combining compressor, noise gate and direct inject box, designed by Allan Bradford of Time Machine Sound Engineering.

The combination of compressor and noise gate is a useful one. The 'pumping' noise associated with high levels of compression can be eliminated by the gate, while the 'topping and tailing' facility afforded by the compressor makes the gate an excellent feedback-killer for PA systems. Comprehensive envelope shaping of sounds for special effects is also possible.

The compressor has a wide range exponential control characteristic which produces a smooth response in the management of 'peaky' signals, with full control over release or recovery time. Attack time is preset for general use, but a front panel screwdriver adjustment enables it to be slowed to allow 'punch-through' effects. Subsequent stages in the audio chain are still protected from overload by an independent fast limiter riding 12 dB above the compression threshold. Gain reduction and limiting are displayed on four LEDs.

The Noise Gate has an attack fast enough for drum kits (but can be slowed right down for 'violating' sounds) and release time is fully variable to suit the program material. An internal time constant eliminates modulation of the signal due to individual waveforms when short release times are employed. The depth of noise-gating is preset at -60 dB but again a front panel screwdriver adjustment permits this to be softened.

Side-chain inputs are provided both for control of compression (for voice-over effects and 'de-essing' and for triggering the noise gate. Two compression gates can be cross-linked for stereo operation.



Inputs are low impedance microphone level and outputs are line level. Inputs and outputs can be balanced or unbalanced via jack or XLR sockets. The unit uses an external power supply for reasons both of economy and hum prevention. Inputs are also provided for direct injection of instruments and of amplifier loudspeaker outputs. The latter will be of particular interest to guitarists wishing to exploit the sound of valve amplifiers while maintaining complete isolation from other instruments. At 1M Ω impedance the DI inputs place negligible load on any instruments plugged into them — particularly important if a guitar is to be plugged into the line input, in order to preserve the natural sustain of the instrument. A parallel line jack is provided in order simultaneously to connect the instrument to a monitor amplifier.

A switch is provided to reduce the overall sensitivity of the unit by 10 dB. With the compressor RELEASE knob pushed in the compression gate is matched to -10 dBm line and mic level signals. With it pulled out the unit is

matched to 0 dBm line and mic levels.

Two parallel output jack sockets are provided, allowing simultaneous connection to more than one piece of equipment without the need for splitters. These outputs are line level and are unbalanced. A balanced XLR line level output is also provided.

Cold Compressor

The compressor controls the maximum signal level by reducing gain progressively above a certain fixed level known as the threshold. Most sounds fluctuate in amplitude and the effect of compression is to reduce the size of signal peaks and to boost average signal level relative to the peaks (Fig. 1). The dynamic range of the signal is therefore reduced, and this can have several important applications.

LIMITING: This means protection from overload by suppression of unacceptable transients. The ATTACK preset is usually set not quite fully anticlockwise (around 1 ms) — but for maximum overload protection in critical applications it may be turned fully anticlockwise,

PROJECT: DI Compression Gate

running the risk of LF distortion. The GAIN/COMP control is advanced so that one or two green LEDs flicker on with the peaks of the music. The RELEASE control should be set about one quarter turn clockwise (about 0.25s). Avoid simultaneous short attack and release times. Release time should be sufficiently long to avoid individual peaks modulating the signal as a whole, with a resultant rasping distortion.

LIFTING VOCALS: Human voices can have a very wide dynamic range and the average level may be substantially below the peak level. By compressing vocals the average level may be boosted so that they become audible in a mix. Compression should be applied to vocals subtly (around 10dB). Too much can make them flat and lifeless.

RECORDING: The human ear can happily accommodate sounds with a dynamic range of 120dB, while the dynamic range of tape recordings is often only 60dB or so. To make maximum use of tape, without quiet sounds being lost in noise and loud sounds saturating the tape and distorting, some compression of signals with a large dynamic range is desirable.

'Thin' or 'peaky' sounding recordings can be salvaged, percussion, for example, often sounding more solid. 'Mix thickening' can be used to increase the average sound level and obtain the sort of impact demanded in modern commercial sound record-

ing. It's used particularly in recording advertising jingles and disco music.

SUSTAIN: The compressor may be used to add artificial sustain to instruments (Fig. 2). The gain is wound right up but the compressor clamps the output signal at compression thresholds. Only when the amplified signal falls below this level of the compression threshold will the signal resume its natural decay. RELEASE should be kept short and the GAIN/COMP control advanced to give the required degree of sustain.

It is also possible to combine sustain with a 'punch-through' attack by allowing the amplified signal to pass unattenuated for a short time before compression takes over. Set the ATTACK preset and RELEASE control to around mid-position. The fast limiter will prevent excessive excursions of the signal but 12dB of punch-through is still available to preserve naturally percussive sounds or add percussion to softer sounds.

Other Features

The four LEDs form a reverse driven bargraph. The right hand LED indicates up to 10 dB of gain reduction. With this LED on and the next LED flickering, gain reduction is in the region of 10 to 20dB. Two green LEDs on and the yellow LED flickering indicate up to 30dB of gain reduction. The leftmost

red LED shows that the fast limiter is working, handling transients too fast to be controlled by the compressor (Fig. 3).

A two-pole jack socket is wired with the tip as a control input and the ring as a signal output for external connections to the compressor. A standard mono jack may be used. The socket may be used either as a control input or as an insert point. A line level signal fed to the EXT COMP socket will cause a reduction in the level of a music signal passing through the

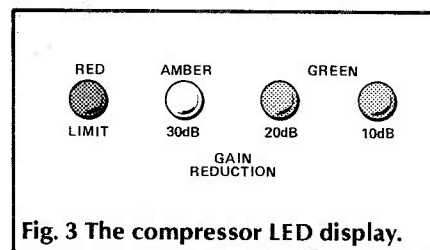


Fig. 3 The compressor LED display.

compression gate ordinarily. This allows voice-overs or 'ducking' effects to be achieved easily — one signal controlling the level of one or more others.

As an insert point, the EXT COMP socket can be used to introduce equalisation into the control path for 'de-essing' and 'de-popping', which are dealt with below.

Noises off

A common hazard of recording and public address work is the inclusion of unwanted sounds in the mix, such as guitar amplifier noise, hum from keyboards, tape hiss, low level RF pick up or 'spillage' of sound from one microphone into other microphones. The problem is aggravated by the high gains associated with large amounts of compression.

BUYLINES

A complete kit of parts including the fully finished steel case and associated hardware is available from TIME MACHINE Sound Engineering for £68.00 including VAT, postage and packing. The double sided, legended PCB is available separately at £9.00 and the case at £14.00. The ready built power supply in a plug costs £24.00. A stereo pair with dual power supply and a cross-linking lead costs £154.00 in kit form. All prices include VAT, postage and packing. Contact: TIME MACHINE Sound Engineering, Abbotsford, Deer Park Avenue, Teignmouth, Devon TQ14 9LJ. Telephone 06267 2353.

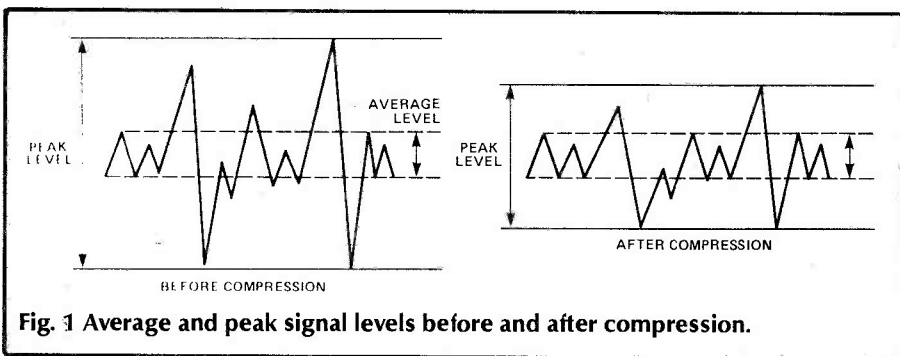


Fig. 1 Average and peak signal levels before and after compression.

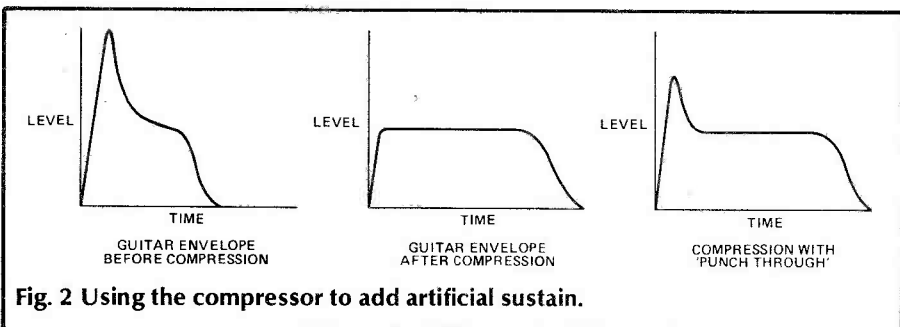
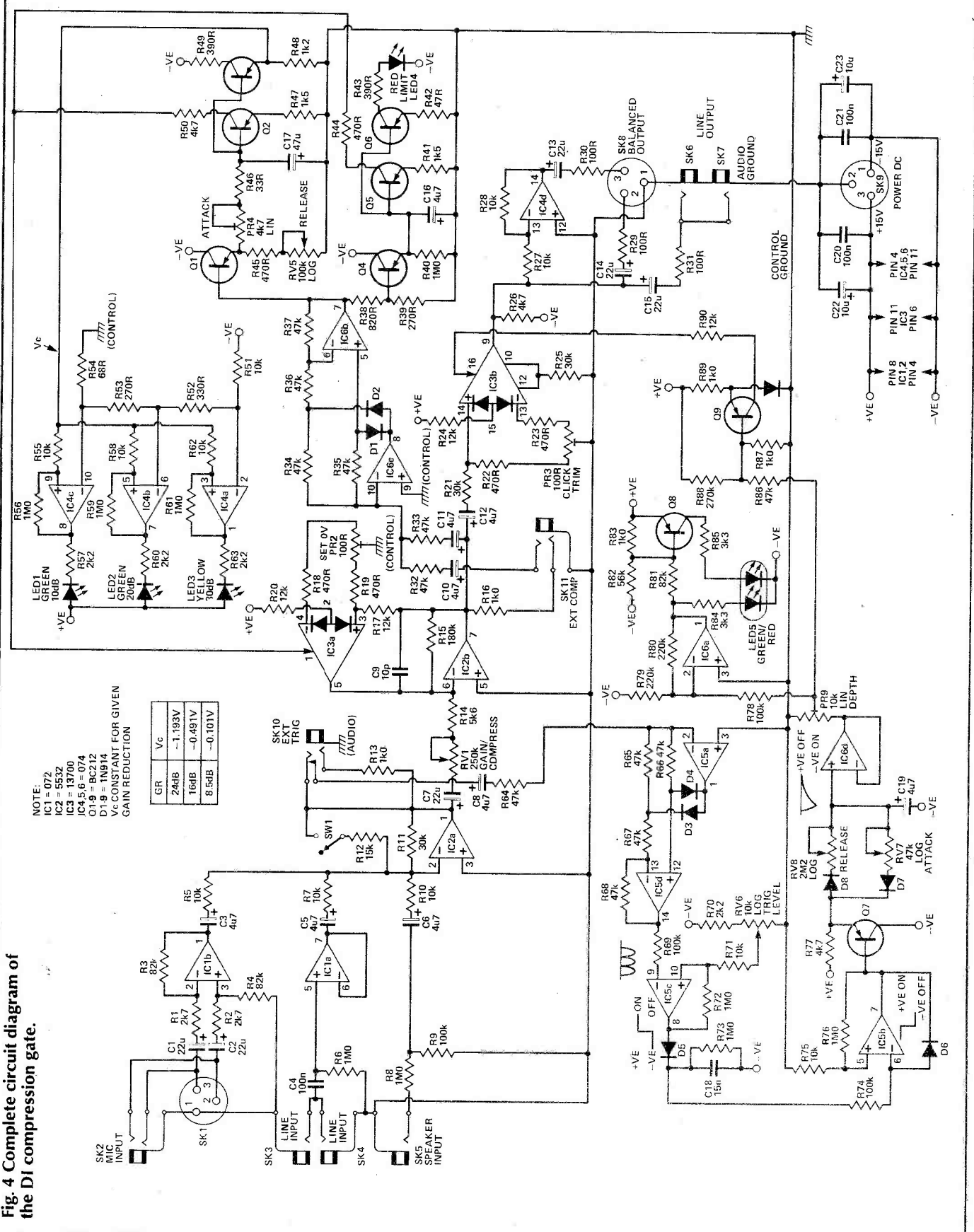
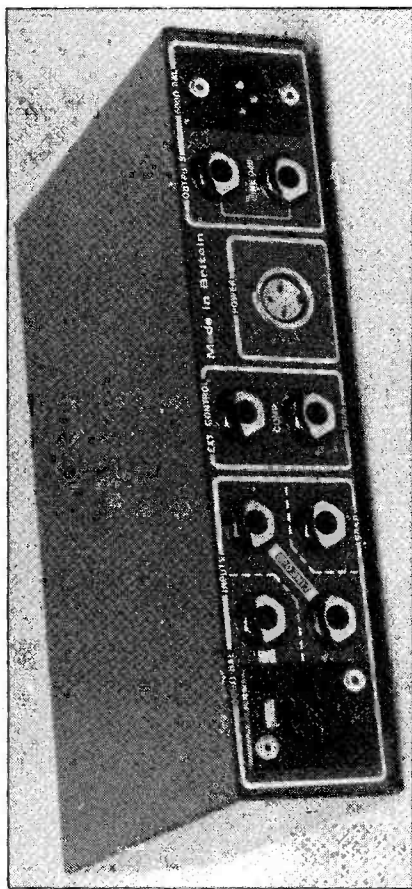


Fig. 2 Using the compressor to add artificial sustain.

Fig. 4 Complete circuit diagram of the DI compression gate.



PROJECT: DI Compression Gate



HOW IT WORKS

Microphone inputs are debalanced by differential amplifier IC1B which has a gain of 30 dB, while line level signals are buffered by high impedance follower IC1a and loudspeaker level signals are attenuated by 20dB by R8 and R9. The resulting matched signal levels are summed by IC2a, the gain of which is switched between 0 dB and +10 dB by SW1.

The compressor is centered on IC2b and OTA IC3a which together form a voltage controlled amplifier, the quiescent gain of which is set by RV1. Current flowing into IC3 pin 1 increases the negative feedback around IC2b and so reduces the overall gain of the system. From here the signal passes through the noise gate VCA constructed around the other half of IC3 (unless this is bypassed by SW2) and thence to the outputs, where IC4d provides an antiphase signal for the other half of the balanced output. PR2 and PR3 are used to minimise control breakthrough in the two VCAs.

The signal at the output of the compressor VCA (IC2 pin 7) is full wave rectified by IC6b and c. If this rectified signal is larger than the voltage drops associated with Q1 and Q2 then current flows into the control pin of IC3a to reduce the gain, and it is this voltage drop which constitutes a threshold above which the signal is compressed. The bigger the signal tries to get, the harder Q2 is turned on, the more current flows and the more the gain is reduced. The closed loop system thus formed makes for very stable control of level which is unaffected by temperature. The exponential control characteristic of Q2 means that the compression ratio (change-in-input-dB/change-in-output-dB), nominally 5:1, actually increases with compression giving a very 'musical' operation over a wide 30dB range of compression. The response and recovery times are set by PR4 and RV5. Q3, R48 and R49 generate a control voltage Vc proportional to the control current and therefore to the amount of gain reduction, and this feeds the bargraph driver built around

IC4a, b and c.

A second side chain with fixed time constants is built around Q4 and Q5. With its input subject to a 12dB attenuation (R38 and R39) it provides the limiter function and responds very quickly to transients, dumping large currents into IC3a pin 1. Q6 drives LED 4 to indicate operation. SK11 allows external signals to control the compressor, or equalisation to be introduced into the side chain.

The signal from IC2a (prior to the compressor) is full wave rectified by IC5a and d and then compared with a reference voltage set by the TRIG LEVEL pot RV6. If the signal exceeds this level the output of Schmitt trigger IC5c goes high and the output of IC5b goes low. The time constant introduced by D5, C18 and R72 prevents IC5b being toggled by individual cycles of the signal waveform. Q7 is included to increase the current output of IC5b in order to achieve attack times as short as 40µsec. The low leakage capacitor C19 is discharged by the ATTACK pot RV7; once the signal falls below the level set by RV6 and IC5b goes high again, C19 charges back up towards 0V via RELEASE pot RV8 and R77. The resulting envelope, buffered by follower IC6d and at a level set by the DEPTH preset PR9, controls the noise gate VCA IC3b, via current source Q9. IC6a and Q8 drive the green and red halves of the tricolour LED in opposite senses to provide indication of gate status. SK10 allows an external signal to be substituted into the noise gate side chain, or for the internal signal to be looped through an external processor.

By careful attention to maximum signal levels at the input to IC3b as determined by the compression threshold, an optimum trade off ratio is achieved, as shown in the specification.

Signal grounds and ground lines in which control currents flow are kept separate on the PCB, joining only where the power supply arrives on the board and is decoupled.

A noise gate discriminates between 'signal' and 'background', shutting down the audio channel in the absence of a useful signal. The level at which the gate opens is set by the Trig Level control. With a useful signal present, turn the control anti-clockwise from fully on until the gate opens. The sound will become audible and the LED indicator will turn from red to green.

The speed with which the gate opens when a signal exceeds the threshold is set by the ATTACK pot. When this is fully anti-clockwise the gate will open within one half-cycle at 10 kHz — fast enough for the sharp transients of drum kits. For vocals, the ATTACK control should be advanced to about one quarter turn clockwise, slowing the attack slightly and avoiding a faint click as the gate opens. The speed with which the gate closes is set by the RELEASE control. This may be set fully anti-clockwise for a sharp cut-off, or advanced clockwise to provide a fade-out which complements the natural decay of the signal. Depth is preset to give 60dB attenuation when the gate is closed, but may be adjusted with a screwdriver down to zero.

Softening the attenuation makes the effect of gating more subtle and also allows the noise gate to be used as a 'two-level device' for controlling monitoring levels during recording.

Other Features

A tri-colour LED shows red for closed, green for open and varying shades of amber in between these states. It also responds to the DEPTH preset, turning slowly from amber to green as this preset is turned anti-clockwise.

A two-pole jack socket is wired with the tip as a trigger input and the ring as a signal output for external connections to the noise gate. A standard mono jack plug may be used. This socket can be used as a straightforward trigger input in which an external signal turns on the gate or as an 'insert point' — for example, to introduce equalisation into the control path so that the gate only opens to signals of the desired frequencies. This latter technique will improve the ability of the noise gate to discriminate between wanted and unwanted signals.

A signal passing through the compression gate may have its envelope substantially modified as

outlined above. The noise gate controls can be used to further modify envelopes. Slowing the gate ATTACK gives a gradual start to sounds while a fast RELEASE gives an abrupt finish to sounds. This latter technique is often used to cut off the 'flap' or reverbera-

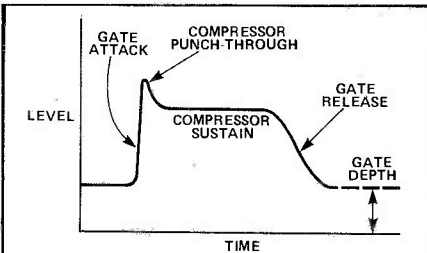


Fig. 5 The parameters defining the shape of the sound envelope.

tion of drums, giving greater impact to the sound.

The parameters available are shown in Fig. 5 and resemble those of ADSR envelope shapers found on sound synthesizers.

Feedback Suppresion

If the overall gain of a PA system exceeds a critical level, the criteria for oscillation are met and

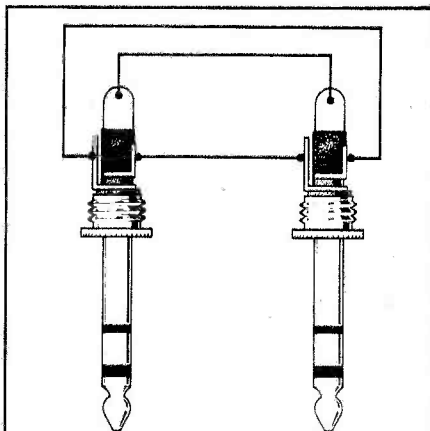


Fig. 6 Wiring of the lead required for stereo operation using two compression gates.

a loud tone is generated. PAs are often used in frequency-selective environments and the feedback generally occurs at a discrete pitch — the resonant frequency at which system gain is highest.

Compression can help by getting rid of large pulses of sound pressure which would shock the system into oscillation. In the absence of a useful signal, however, the gain of a compressor rises and feedback can 'creep up', resulting in howl-round even during periods of apparent silence. The noise gate overcomes this

PARTS LIST

RESISTORS (1% metal oxide)

R1, 2	2k7
R3, 4, 81	82k
R5, 7, 10, 27, 28,	10k
51, 55, 58, 62,	
71, 75	
R6, 8, 40, 56,	1M0
59, 61, 72, 73, 76	
R9, 69, 74, 78	100k
R11, 21, 25	30k
R12	15k
R13, 16, 83, 87, 89	1k0
R14	5k6
R15	180k
R17, 20, 24, 90	12k
R18, 19, 22, 23,	470R
44, 45	
R26, 50, 77	4k7
R29, 30, 31	100R
R32, 33, 34, 35, 36	47k
37, 64, 65, 66,	
67, 68, 86	
R38	820R
R39	270R
R41, 47	1k5
R42	47R
R43, 49	390R
R46	33R
R48	1k2
R52	330R
R53	270R
R54	68R
R57, 60, 63, 70	2k2
R79, 80	220k
R84, 85	3k3
R88	270k
RV1	250k lin pot
PR2, 3	100R min horiz preset
PR4	4k7 vert cermet preset
RV5	100k log pot with push/pull SPST switch
RV6	10k log pot with DPDT switch
RV7	47k log pot
RV8	2M2 log pot
RV9	10k vert cermet preset

CAPACITORS

C1, 2, 7, 13, 14, 15	22u 16V minelect
C3, 5, 6, 8, 10, 11,	4u7 40V minelect
12	
C4, 20, 21	100n polyester
C9	10p ceramic
C16, 19	47u 16V tantalum
C17	47u 16V minelect
C18	15n polyester
C22, 23	10u 40v minelect

SEMICONDUCTORS

IC1	TL072
IC2	NE5532
IC3	LM13700N
IC4, 5, 6	TL074
Q1-9	BC212L
D1-9	1N914
LED1, 2	Green standard LED
LED3	yellow standard LED
LED4	red standard LED
LED5	Tricolour round LED

MISCELLANEOUS

SK1	Female panel mounting XLR
SK2, 10, 11	Stereo break ¼" jack socket
SK3, 4, 5, 6, 7	Mono ¼" jack socket
SK8	Male panel mounting XLR
SK9	Prof 3-pin DIN panel socket
SW1	see RV5
SW2	see RV6

Knobs (collet or grub screw, 5off); PCB; case; stick-on cabinet feet (4 off); PCB pillars (tapped and studded plus nuts, bolts and locking washers, 4 off); PCB linking pins (63 off); Veropins (35 off), self tap screw (no 4 x 6 mm, 4 off); 6BA nuts, bolts and locking washers (4 off); power supply ±15V at 120 mA per rail regulated.

problem and microphones may be operated with between 6 and 10dB more gain than otherwise.

Special Patches

STEREO OPERATION: A pair of compression gates may be cross-linked for stereo operation using a stereo jack to jack lead wired as

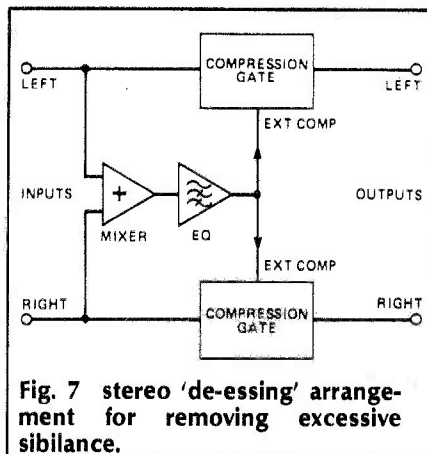


Fig. 7 stereo 'de-essing' arrangement for removing excessive sibilance.

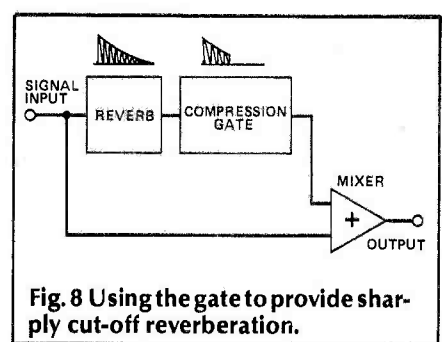
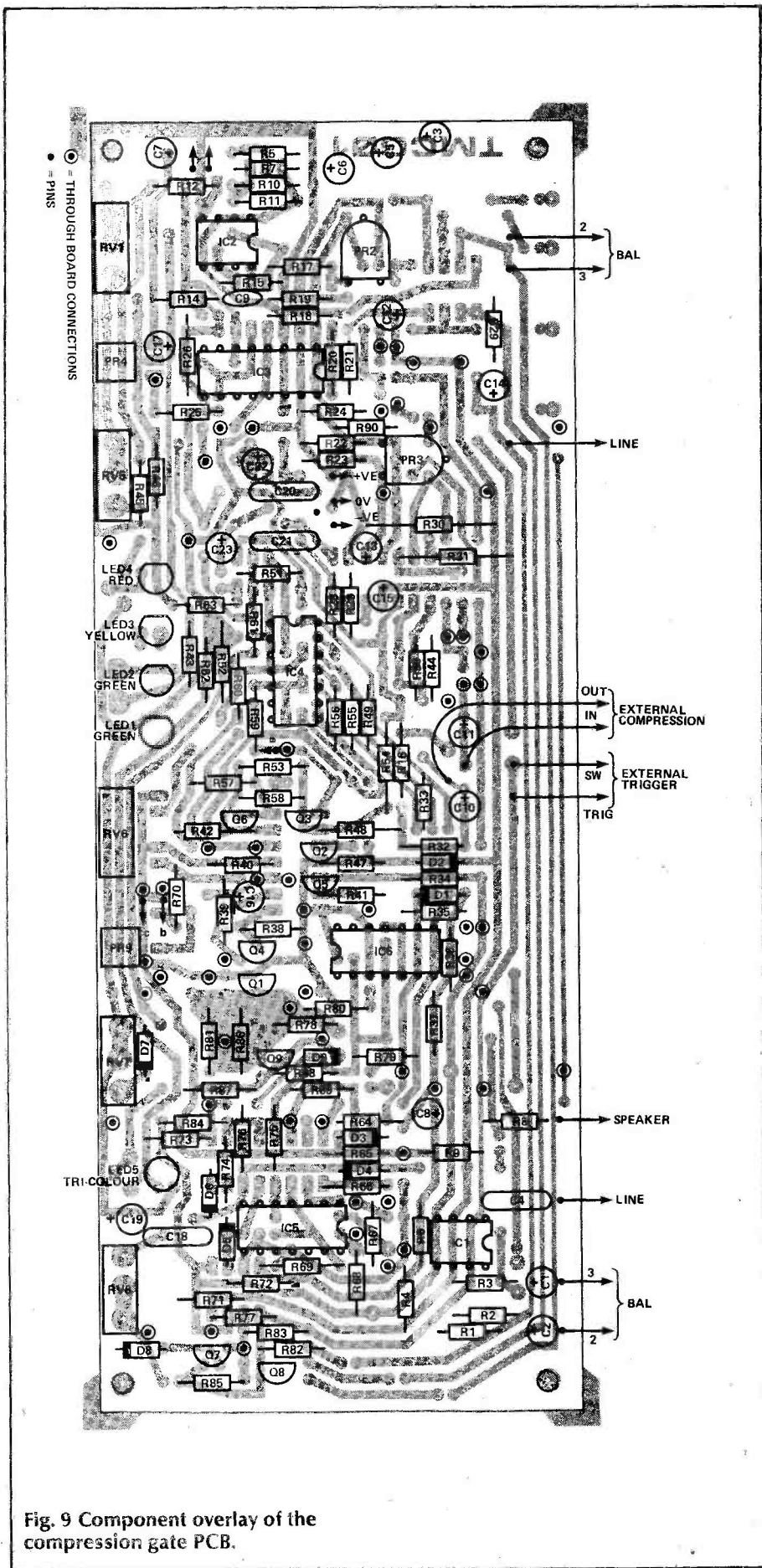


Fig. 8 Using the gate to provide sharply cut-off reverberation.

shown in Fig. 6, with one end being plugged into each EXT COMP socket.

STEREO DE-ESSING: Incoming left and right signals should be mixed and then passed through an equaliser. This equalised signal is fed into the EXT COMP input of each compression gate. A treble boost will cause low frequency components to be compressed most for suppressing 'rumble' or microphone 'popping'. In each case adjust the GAIN/COMP con-

PROJECT: DI Compression Gate



control for the best results, keeping the compressor RELEASE time short so as not to compress the section following the offending sibilant.

GATED REVERB: With the gate RELEASE fully anti-clockwise, adjust the gate Trig Level so that the reverberation cuts off prematurely and abruptly. This is particularly effective on drums (Fig. 8).

EXTERNAL GATE: Sending a signal into the EXT TRIG socket enables that signal to trigger

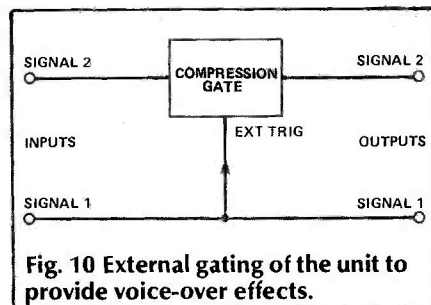


Fig. 10 External gating of the unit to provide voice-over effects.

whatever sound is passing through the compression gate. Softening the gate DEPTH by turning the preset anti-clockwise makes the noise gate a 'two-level device'. This is the complement of the compressor voice-over patch, in which the presence of a signal at the EXT TRIG input switches the signal passing through the compression gate from attenuated to full (Fig. 9).

Construction

The PCB is double sided and linking pins are used to make the through-board connections, their positions being marked by stars printed on the component side of the board. Great care should be taken to ensure that every pin is soldered on both sides of the board — work systematically and check thoroughly as nine out of ten faults will be found to be due to a pin not being soldered somewhere, usually on the underside of the PCB.

Solder components in order of height: resistors, diodes, IC sockets, presets, transistors, capacitors, LEDs and pots. Take care to observe polarity of diodes and capacitors as marked. It helps if the LEDs are the correct way round, too. The LED leads should be bent at 90°, 5mm behind the plastic package and soldered so that the bends are 5 mm above the PCB.

Note that the Alps pots supplied with the kits solder to

PROJECT: DI Compression Gate

pins in order to be the correct height above the board. Solder Veropins in the pot positions and attach the PCB mounting pillars to the board corners using the studded ends and nuts, then fix the PCB inside the case by passing four bolts through the mounting holes in the bottom of the case. Next cut the pot spindles to length (10 mm) and mount them on the front panel. The pot tags can now be soldered to their respective pins and perfect alignment is ensured. The whole assembly may

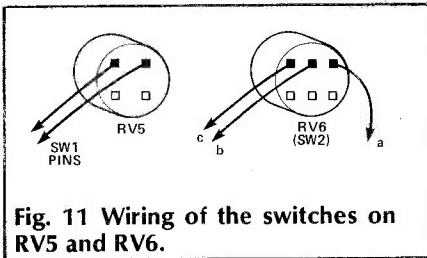


Fig. 11 Wiring of the switches on RV5 and RV6.

now be removed from the case for testing.

Pins should also be used for the off-board connections as well as the connections to the switches on RV5 and RV6 (Fig. 10). Con-

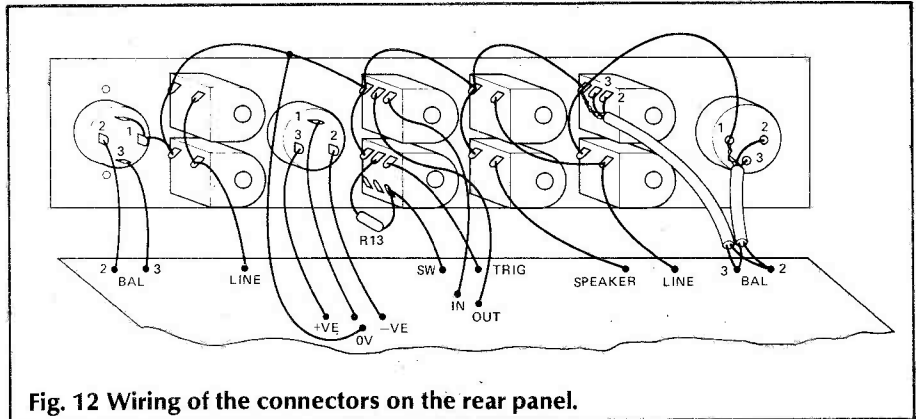


Fig. 12 Wiring of the connectors on the rear panel.

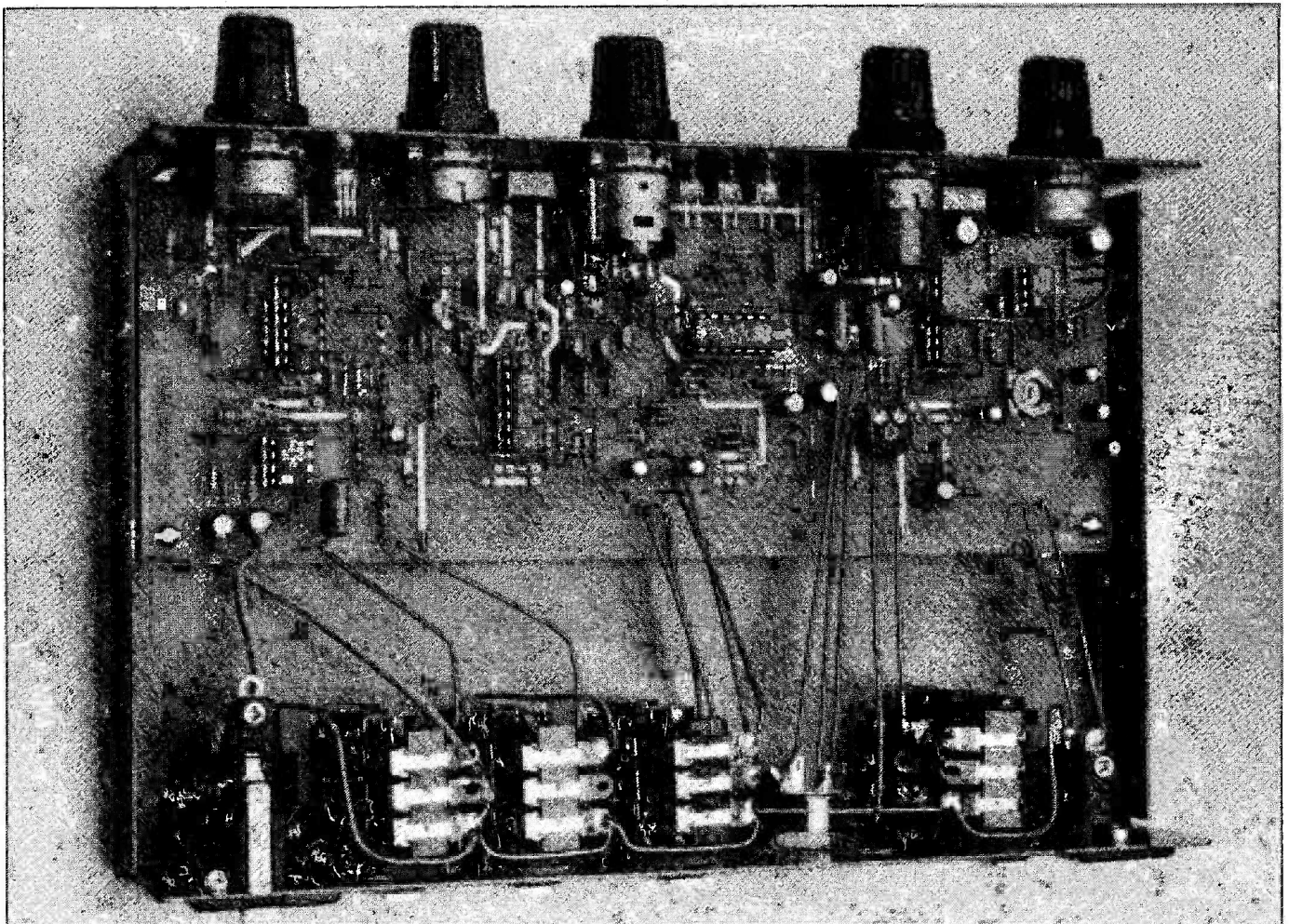
nections to the sockets are shown in Fig. 11 but it is probably wise to complete the setting up and to bench test the completed board prior to wiring it into the case.

The DI compression gate is designed to run from any regulated power supply providing $\pm 15V$ at up to 120mA per rail. A custom power supply built into a mains plug case and with a 2metre lead terminated in a 3-pin DIN plug is available from the kit manufacturers.

The only setting up required is of the two presets RV2 and RV3.

Using a voltmeter on its most sensitive range, adjust RV2 to set IC2 pin 7 to precisely 0V. Next set gate ATTACK and RELEASE at minimum and the DEPTH preset fully clockwise, then either feed a sine wave into a line input or use a microphone in order to trigger the Noise Gate — adjust the THRESHOLD control so that the gate opens and closes as the incoming signal goes up and down in volume. A click will be heard as the gate opens and closes and RV3 should be adjusted until this is minimized.

ETI





FOR FRIENDSHIP, LOVE OR MARRIAGE **Dateline** *is the way to meet*

'She just kissed me and that was it!'

Ron Watt toyed for ages with the idea of joining Dateline.

'One or two of my friends suggested it would be a good idea,' said Ron, a House Sales Officer from Kidcaldor, West Lothian. At 29, most of his friends were married. 'It's very hard to meet people because you don't really want to go to a disco or for a drink on your own — always assuming that you will meet the sort of people that you want to go out with. Dateline gets you through the first hurdle of asking people out because you can write to them.'

Coincidentally, Ron joined Dateline on the very same day as Fiona Martin, a pretty 25 year old from Penicuik, Midlothian. Widowed at a tragically young age, Fiona found that, with a small daughter, it was very difficult for her to set out to meet people. In Fiona's case it was her sister who pushed her into joining Dateline.

In spite of joining on the same day, Fiona received her results before Ron and, having made up her mind to make full use of her membership, she wasted no time in writing to three of the names on her list — one of which was Ron's. 'I got three replies back — including Ron's — and I went out with the first two but they didn't really appeal to me. Then I met Ron.'

Ron in the meantime, had received his first list of names from Dateline but he was destined never to use it. 'Before I got the list I got the letter from Fiona. I thought I would wait and see how that turned out before I met anyone else.'

Ron had written such a nice letter to Fiona, asking her to write again or to phone him, that she decided, 'being very brave,' to ring up. 'She sounded nervous,' said Ron, 'but I was impressed by the voice — she had a nice voice.'

Fiona too liked the sound of Ron and after sorting out a babysitter for Jacqueline, Fiona's daughter, the couple arranged to meet. Ron picked Fiona up from her house and took her for a drink. Initially that first meeting didn't go particularly well. 'I wasn't disappointed when I met her — I liked her,' explained Ron, 'but communication was very difficult because we

were both nervous and I did most of the talking. I got the initial impression that she didn't like me very much!'

'And I didn't think he liked me either,' laughed Fiona.

After a couple of hours Ron took her home but he had already decided not to ask her for another date. Fortunately, Scottish hospitality saved the day because Fiona invited him in for coffee and cheese toasties! Once inside her own home, Fiona became much more confident and relaxed. 'She was just as nice,' said Ron, 'but easier to talk to.'

The couple sat and talked until after midnight. 'I liked him very much,' confessed Fiona, 'and he ended up staying the night. On the couch downstairs,' she added hastily.

Ron was still not convinced that Fiona liked him enough to go out with him a second time and was happily surprised the next morning when she agreed to see him again. From then on their relationship snowballed and the couple spent every available moment together.

'From the second time I met her I realised that she was terrific,' said Ron. 'When I was driving her home I knew then I really wanted to make a go of this.'

Fiona too quickly began to feel that this was something special. 'I don't know why I was so attracted to him — it was just the sort of person he was. He's very kind and gentle.'

Of course, Ron didn't only have to convince Fiona. Jacqueline also had to be won over. Not an easy matter, perhaps, for a single man with a limited experience of children. But Ron was a great success! My daughter took to him like...well, she can twist him round her little finger!' said Fiona.

'To be honest I never really expected to meet a girl with a baby,' said Ron, 'but I must admit I really enjoy Jacqueline's company and it makes me feel...fulfilled. I had no second thoughts about it because she's really a very nice little girl.'

Five weeks after they met, Ron skated warily around the subject of marriage. 'The night before we were engaged I just casually said that if I was to ask her to marry me one day, what would she say? She said she would think about it for a second and then say yes. So I left it at that!'

Less than 24 hours later, however, Ron returned to the subject. 'I simply said how would it be if this time next year we were married and she just kissed me and that was it!'

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<input type="checkbox"/> Family type	<input type="checkbox"/> Practical
<input type="checkbox"/> Clothes-conscious	<input type="checkbox"/> Intellectual

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<input type="checkbox"/> Fashion	<input type="checkbox"/> Classical music
<input type="checkbox"/> Pubs	<input type="checkbox"/> Art/Literature
<input type="checkbox"/> Sport	<input type="checkbox"/> 'Live' theatre
<input type="checkbox"/> Pets	<input type="checkbox"/> Science or technology
<input type="checkbox"/> Folk music	<input type="checkbox"/> Creative writing/painting
<input type="checkbox"/> Jazz	<input type="checkbox"/> Poetry
<input type="checkbox"/> Travelling	<input type="checkbox"/> Philosophy/Psychology/Sociology
<input type="checkbox"/> Cinema	<input type="checkbox"/> History/Archaeology
<input type="checkbox"/> Good food	<input type="checkbox"/> Conversation

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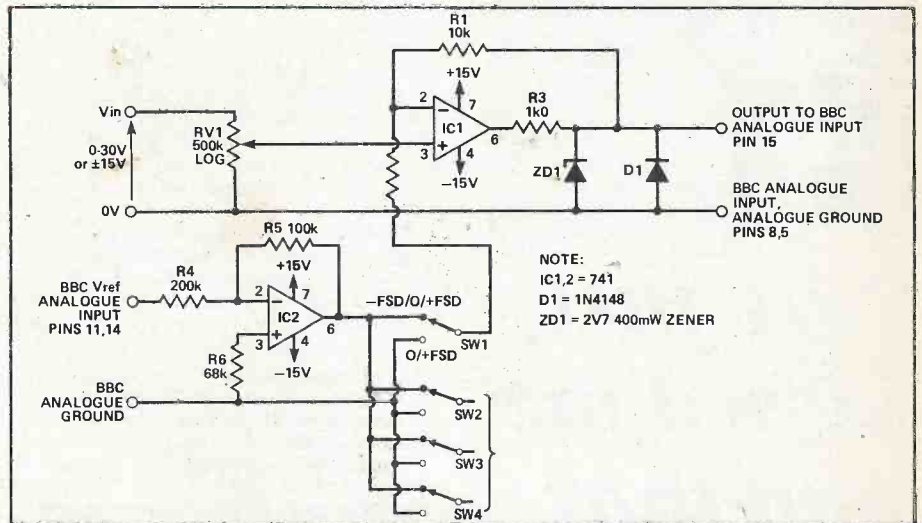
TECH TIPS

Buffer Amplifier For The BBC Microcomputer

D. Bush,
Leamington Spa.

The four channel A to D converter on the BBC micro is limited in use by its fixed input range of 0 to +1.8V, its temperature drift and its susceptibility to damage by input voltages outside the range -1 to +5V. The variable gain buffer amplifier shown here was designed to minimise these problems and allow school children to incorporate the BBC micro into their electronics and technology projects without difficulty.

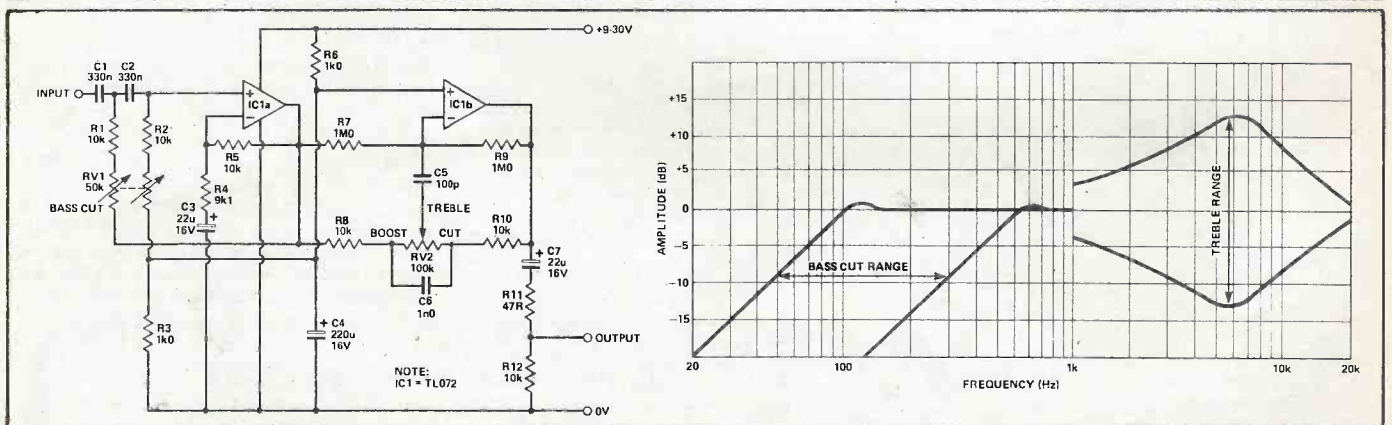
IC1 is a non-inverting amplifier with a gain of x2, the output being limited by D1, ZD1 and R3 so that it cannot exceed the limits -0.7 to +2.1V. These limiting components are placed within the feedback loop so as to maintain linearity over the output range. Input attenuation is



provided by RV1 which can be calibrated for an input range of up to 30V depending upon the potentiometer used. This circuit is repeated for the other three channels.

IC2 is configured as an inverting amplifier with a gain of 0.5x. It takes its input from the Vref line on the BBC and provides an output of one half of this voltage which can be

used to offset the buffer amplifiers. By switching this voltage in or out, the buffers can be set to accept inputs which range from either -FSD through 0V to +FSD or from 0V to +FSD only. In the - FSD to +FSD position, the buffer can be used to process input data for presentation in graphical form, with the graph axis remaining visually coincident with the 0V input.



PA Tone Control

R. Eggleton,
Catworth

Hi-fi tone controls commonly consist of the Baxandall circuit which provides maximum boost and cut at the frequency extremes; public address (PA) tone controls have different requirements.

For PA use only cut is required at the bass end to remove the proximity effect of close-up microphones

and to protect horn loudspeakers which have a limited response below about 200Hz and may easily be damaged. At the treble end boost or cut may be required. However, this must be limited at very high frequencies to avoid speaker damage and amplifier overload.

The circuit shown provides the ideal response as can be seen from the accompanying frequency response graph. It uses a dual op-amp powered from 9-30V DC and consuming approximately 25mA. The first stage provides the bass cut at 12dB/octave, the turnover fre-

quency being adjustable from 80Hz to 500Hz by means of the 50k dual linear potentiometer. The second stage provides ± 13 dB of treble boost or cut at 6kHz and is adjusted by means of the 100k linear potentiometer.

To alter the frequency turnover points the two 330n capacitors may be increased to lower the bass frequency or reduced to raise it. Similarly, capacitors C5 and C6 should be increased to lower the treble peaking frequency or reduced to raise it, maintaining the ratio $C2 = 10 \times C1$.

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- Be brief and to the point in your enquiries. Much as we enjoy reading your opinions on world affairs, the state of the electronics industry, and so on, it doesn't help our already overloaded enquiries service to have to plough through several pages to find exactly what information you want.

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We are a member of the mail order protection scheme, and this means that, subject to certain conditions, if a supplier goes bankrupt or into liquidation between cashing your cheque and supplying the goods for which you have paid, then it may be possible for you to obtain compensation. From time to time, we publish details of the scheme near our classified ads, and you should look there for further details.

OOPS!

Corrections to projects are listed below and normally appear for several months. Large corrections are published just once, after which a note will be inserted to say that a correction exists and that copies can be obtained by sending in an SAE.

Single Board Controller (March 1985)

There were a number of errors in the parts list. RP2 is listed as a 10k SIL pack but is actually four separate resistors, and the same applies to RP3. RP4 is also listed as a SIL pack but should consist of seven commoned resistors. R13 is always required, not just when a cassette interface is used as stated.

The Real Components (May 1985)

In Fig. 1 on page 20, the connections for the Texas L and 2N transistors are incorrectly shown. They should read B, C and E from the top.

Heat Pen (June 1985)

The instruction in the penultimate paragraph on page 49 should read "... adjust RV2 for 2.73V ...", not 2.37V as stated.

Low Cost Audio Mixer (June 1985)

In Fig. 6 on page 39, the PCB foil pattern has been incorrectly shown as though from the copper side. The board is shown correctly from the copper side in the foil pattern pages. In Fig. 10 on page 40, the positive power rail at lower left should be shown connected to pin 8 of the TL072s, IC1-5).

Noise About Noise (July 1985)

In Fig. 5 on page 24, no connection should be shown between the cathode of the diode and the negative side of the 470uF capacitor.

Printer Buffer (July 1985)

The case specified is actually larger than the one used for the prototype. It will, of course, work perfectly well, but if you want to a compact unit use a Verocase 202-21038H (180 x 120 x 65mm) rather than a Verocase 202-21035. The regulator IC17 should be bolted to the back of the case to provide heatsinking or, alternatively, fitted with a TO220 heatsink.

Please note that the designer, Nick Sawyer, has been in touch to inform us that the refresh problem we mentioned in September ETI is dealt with in the printer buffer software. In this case there is no need to replace the TMS 4416 dynamic RAMs, although as far as we know the replacement parts mentioned (Hitachi HM48416 DRAMs) will cause no problems. The full text of Nick Sawyer's letter will appear next month. Meanwhile, our apologies for any confusion caused.

Intel 8294 Data Encryption Unit (September 1985)

It should be apparent from the text, page 35, that an actual program has been omitted. This program is for use with the SDK 8085 kit only, and copies may be obtained from us on receipt of a stamped addressed envelope.

Tech Tips — Novel Input Stage (October 1985)

The caption against the lower figure should read "Low noise output at minimum gain", not maximum gain.

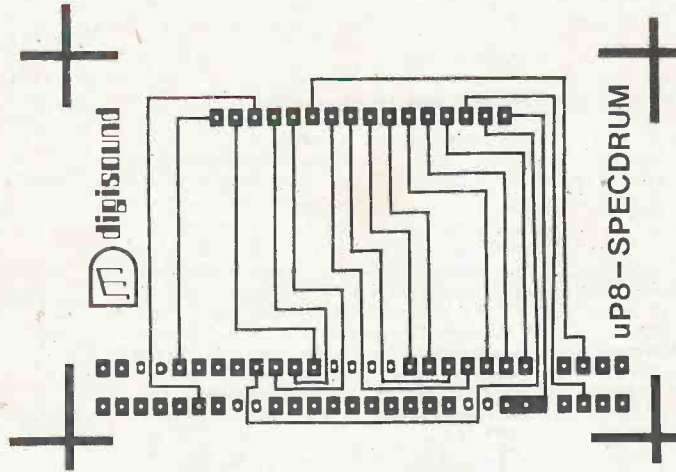
Chorus Unit (November 1985)

IC3 is shown on the circuit diagram on page 49 connected to the 9V supply. It should be connected to the 5V supply. The foil pattern connection to this IC are correct.

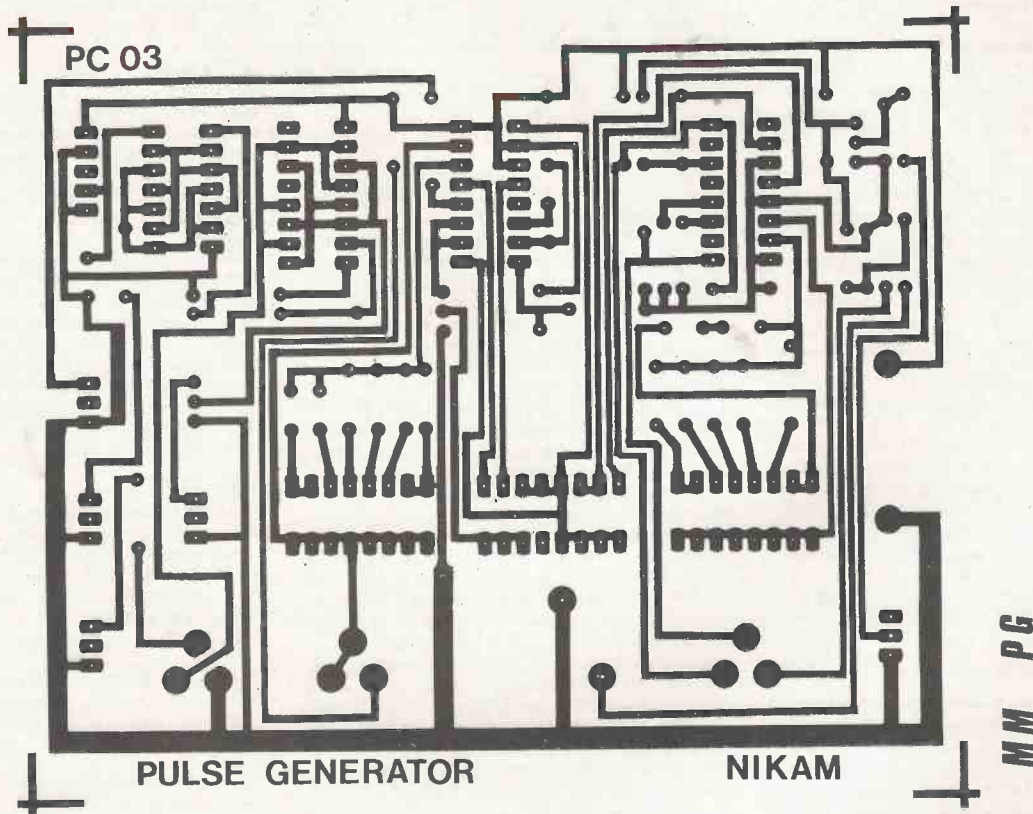
Foil Patterns (November 1985)

The foil patterns for the Modular Test Equipment Waveform Generator and the Chorus Unit are shown from the component side rather than the copper side.

PCB FOIL PATTERNS



The foil pattern for the Spectrum connector board.



The Modular Test Equipment pulse generator board.

Page 57

Missing

Page 58

Missing

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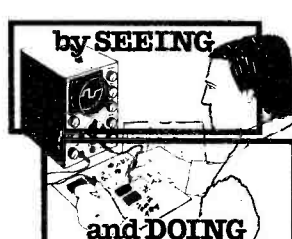
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TRAINS OF THOUGHT

Those of us who model railways for nostalgic reasons know full well that the sounds of full-size railways, especially those of the steam era, were a major component of the atmosphere that we seek to recreate. The addition of sound effects therefore provides an immediate boost to the realism.

There are dozens of ways in which sound can be added to a model railway, and some demand no electronic skills at all. Hidden speakers can reproduce disc or cassette recordings of full-size railways, while a miniature speaker in a station building can broadcast station announcements recorded on cassette. Computer buffs can generate quite convincing train sounds using the complex sound facilities of the BBC Micro or Commodore 64.

But if looking primarily at electronic hardware applications, train sound systems divide into two sorts: off-train and on-train reproduction.

In off-train reproduction the sound is reproduced away from the train, although it may be related to it. For example, the chuff rate of a steam train can be made proportional to the train speed as measured by a speedometer unit.

Many circuits for electronic chuffers and whistles have been published, some using discrete semiconductors and some using ICs. Some of the complex sound generator chips offer some useful facilities. The NS76477 and its 16-pin relative, the SN94281, offer hours of noisy experimentation. Sadly the SN94281 is hard to find nowadays — if any reader knows a source please let me know.

It is also possible to reproduce the sound on board the train. In O-gauge and larger scales it is usually easy to mount a small moving-coil speaker in a locomotive or tender — in HO and OO scales piezo-electric transducers of 20 to 25 mm diameter can provide reasonable reproduction. On-train systems divide into those where the sound is actually generated on board the train and those where it is generated remotely and transmitted to the train. On-train generation poses prob-

blems of space for the circuitry and of an adequate smoothed power supply. The track voltage can be monitored for a measure of train speed if needed.

Off-train generation solves the problems of space and power supply but leaves the questions of sound transmission to the train. The simplest method is through the rails, but this has its limitations. The controller must be a pure DC type or buzzes and hums will drown your sound, and the transducer must have a series capacitor to protect it from the controller voltage. Superimposing the audio on the traction voltage has its own special pitfalls for the unwary. I have used a special controller with complementary VMOS output which acted simultaneously as a DC power amplifier (controller) and audio power amplifier. Audio inputs were provided from both a cassette recorder and an SN94281-based electronic sound generator.

But beware the practical joker who swaps cassettes. You may find that, instead of chuffing and whistling, your 1930s' vintage GWR branch train delivers the latest 1980s' chart-busting hit!

Roger Amos

individual point-to-point communication, merely by dividing the total communications spectrum available in the network up into a number of channels. Each channel is then used to transmit an individual communication between source and receiver. The principle I'm talking about is known as multiplexing, and has been acknowledged and used in various forms since the early days of radio communications.

There is little to stop the CEGB using the national grid purely as a communications network, if the multiplexed channels can be piggy-backed on top of the mains supply voltages. In a very simple way, an example can be seen in the proliferation of mains-powered, cordless intercoms now available, which only need to be plugged in at each required position in a building to allow efficient and good quality communications. ETI itself has published a number of project designs which use a building's mains wiring in this way.

On a larger scale, the whole national grid could be used similarly, but is presently under-utilised. The techniques and principles are all there and have been for many years. The only drawback remains the CEGB itself and its seemingly slow progress.

This Is The BBC

At the end of September BBC radio commenced using its first completely digital sound mixing desk. Reputed to be capable of the sort of tricks with sound that video paintbox-type machines can do with television pictures, the desk is computer controlled and 'totally' portable — it fits onto an outside broadcast trailer and so can be used around the country. No doubt, if you want it to, the desk will allow cricket matches on Radio 3 to sound that much more realistic in pure digital surreal sound, but are we talking of any significant advantage?

The digital desk will presumably make better recordings of concerts, operas and other musical extravaganzas, but is that of any benefit to the listener? Face it, quality of reception on either AM or FM is limited by the transmission system, not by the equipment. Existing mixing desks are every bit as good as they need to be to allow excellent sound reception. Even the UK FM transmission method doesn't allow the large signal-to-noise ratio which the digital desk will afford. The BBC might say they are taking the hiss out of radio broadcasts, but perhaps they are trying to take the hiss out of the licence payer.

Keith Brindley

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OPEN CHANNEL

I'm constantly amazed at the time it takes organizations — particularly larger ones — to take in and adapt to a new technology. Take, for example, the Central Electricity Generating Board. The CEGB's national grid is a wonderful thing: it provides a source of electrical power to every household and business in the land. But it really has more potential (pun intended) than just that. In effect it is a cable network which reaches every building throughout the nation. Think about it.

To date, this network is only capable of providing one-way transmission, the distribution of electrical power from power stations to users. But true transmission networks must be more powerful (yeuch, another pun) than this. They should allow two-way transmissions.

Let's look at the national grid in another way. It can be simplified, at least for this illustration, and thought of as a length of wire which reaches every consumer. Now any length of wire is a transmission medium, and any transmission medium can be used to transmit more than one

ALF'S PUZZLE

Alf's dream

Alf is always keen to improve his education and over the last year he has been attending evening classes at the local Tech. He chose the United Education Guild combined diploma in circuit theory and basket weaving, with which you are no doubt all familiar. Last week, on the night before the final exams, he had a horrible nightmare.

In his dream, Alf entered the examination room and was confronted by a mass of resistors all woven together. The resistor tangle didn't stop at the bench, it trailed across the floor out of the

window and far into the distance. There was only one question on the exam paper: Find the resistance at the terminals of this INFINITE resistor network.

Alf couldn't use the ohm meter the examiners had supplied because the electricity would take an infinite amount of time to travel around all the resistors. Nor did the idea of doing an infinite number of calculations appeal to him very much. What could he do? What IS the resistance of the network? The answer to last month's puzzle:

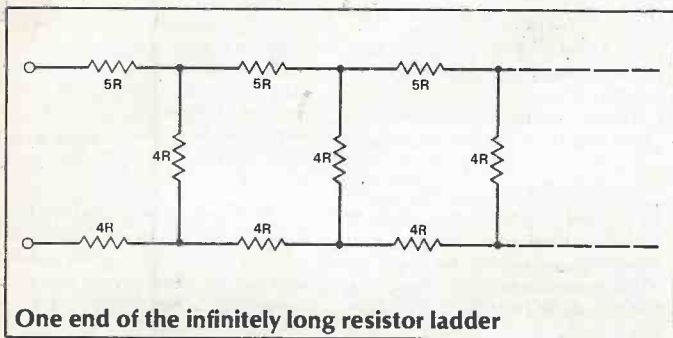
Alf cheated a bit in describing the second waveform as a distorted 2kHz square wave. If you look at it closely you'll find it repeats itself exactly every two cycles of the 2kHz square wave

above, so it really has a frequency of 1kHz. I think it's fairly obvious by inspection that the waves do, in fact, add up to give a 1kHz sine wave. From a mathematical point of view, without going into details, the situation would look something like this:

- sine wave components of 2kHz square wave
- PLUS
- sine wave components of 180° phase-shifted square wave
- PLUS
- the extra 1kHz sine wave
- EQUALS
- a 1kHz sine wave by itself

The frequency components of the two square waves would cancel as they are 180° out of phase, leaving only the 1kHz sine wave.

The 'distorted' square wave could not, in fact, have been produced by feeding the square wave through any kind of linear circuit (in circuit theory, a linear circuit includes such things as filters and tuned circuits, which an amplifier designer would not think of as being very linear!) and could only have been produced by a sine wave being injected from somewhere else. Alf was leading you astray by describing it as a 'distorted square wave'.



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SCRATCHPAD

by Flea-byte

I confess that I find the game of international espionage as mystifying as Ian Botham's haircut. Despite its high profile, I can't for the life of me figure out how it works or why it exists in the first place.

No doubt, as the news media remind us from time to time, spying is dastardly wickedness which endangers the fabric of society in the free world. (So much for the tempting offer to join GCHQ that I saw in 'another electronics magazine' recently. Disabled people, the ad said, were welcome to apply — although if your disability consisted of being a trade union member, forget it!)

It must be just as true that we don't have any spies on our side of the pitch. At least we don't have any now. We used to have some during the war and in John Le Carre books, but most of them worked for the Russians, and the ones that didn't weren't terribly keen on spying so they gave themselves silly, endearing names like Mole and Smiley and The Third Man. Now they're all retired or dead, which makes the game distinctly unfair, because with them on our team the Russians are

bound to win.

What disturbs this cosy little picture is the fact that nobody seems to win or lose at all. In fact, I've never been able to work out what earthly difference all this spying business makes to anything. Spies exist, occasionally they're forced to take early retirement, a lot of hot air is emitted from the seats of power and things carry on much the same as before — with us knowing that they know that we know that they know that we know . . .

To take a case in point, there was the recent affair of Oleg Gordievsky's defection and the resulting poker game with 'undesirables' between Moscow and London. Apparently, Gordievsky had been what I believe is called a double-agent for some years. He would have been well able to tell his Western paymasters all about about the Soviet spies ferreting around among our secrets. Only the most cynical among you will have asked why the British government waited for so long to expel these spies and how it managed to feign such convincing shock when Gordievsky came in from the cold. (There I go again with the jargon.)

Among our boys to be thrown out of Moscow after the faeces hit the ventilating machine was the local office chief of Quest Automation — a company that repre-

sents the interest of firms like the Apricot computer manufacturers, ACT, in the Soviet Union. His employers categorically deny the charge, but then (in the immortal words of Mandy Rice-Davis) they would, wouldn't they? What I do know is that everybody says his expulsion will make no difference whatsoever to anything except the address on his headed notepaper. What I also know is that the government is apparently panic-stricken at the thought of British high technology finding its way to the Eastern bloc. The Customs and Excise have a thing called Operation Arrow going in order to bust the sanctions busters — the sanctions in question being embargoes on the sale of Western high-tech goods behind the Iron Curtain. And the Americans (from whom our government takes most of its cues) are really hot on the high-tech exports front. So, how come Quest Automation was in Moscow at all?

The kerfuffle is made even more pointed by a revelation, at around the time of the big spy-swap, that Operation Arrow had trawled the waters for sanctions busters and had arrested a number of people whose courtroom defence was that they couldn't be security risks because, while setting-up illicit high tech deals in Moscow, they were supplying the low-down on the Russians to MI5 or

MI6 back in London. Gives a new meaning to the concept of information technology, doesn't it? The serious point remains, however: what are we after — information to feed the already bloated and unaccountable security services or trade to protect and build industry and people's jobs? In case you need reminding, it was Mrs Thatcher who described Mikhail Gorbachov as 'a man I can do business with'.

Export System

It might be worth reflecting on a piece of news that was quietly announced earlier this year, in the light of my previous item. The Soviet Computer Import Corporation said recently that it intended to import one million personal computer systems for use in technical training programmes in schools. The first 10,000 units will be supplied by Nippon Gakki (better known as Yamaha in this country) and, yes, they will be MSX machines. Another Japanese company, Star Micronics, hope to export 100,000 MSX-based systems, packaged with their own VDUs, printers and disk drives, at a unit price of around £250. The Soviet electronic products import company, V/O Electronorgtechnica, has already agreed to take 4000 systems. Meanwhile, we were expelling Viktor Logush of Electronorgtechnica's British office.

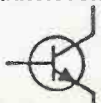
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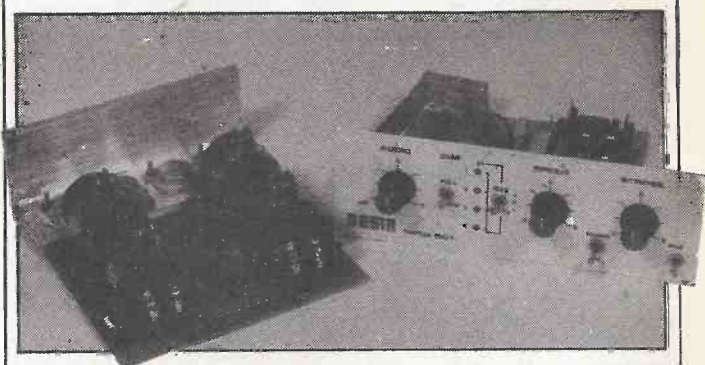
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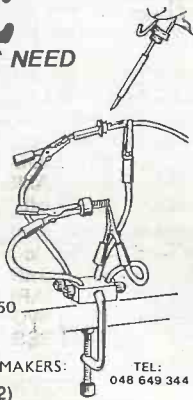
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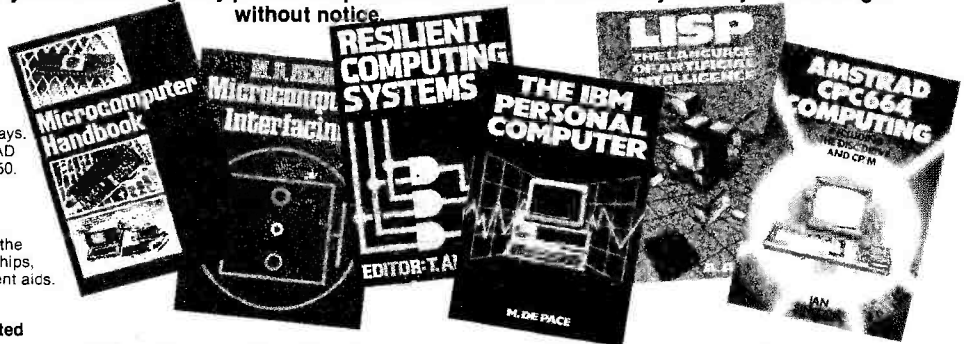
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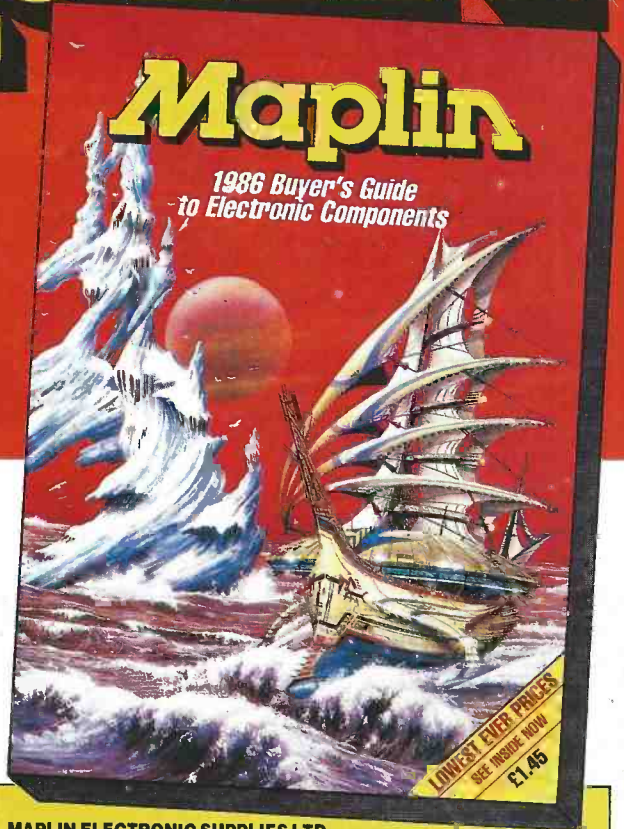
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