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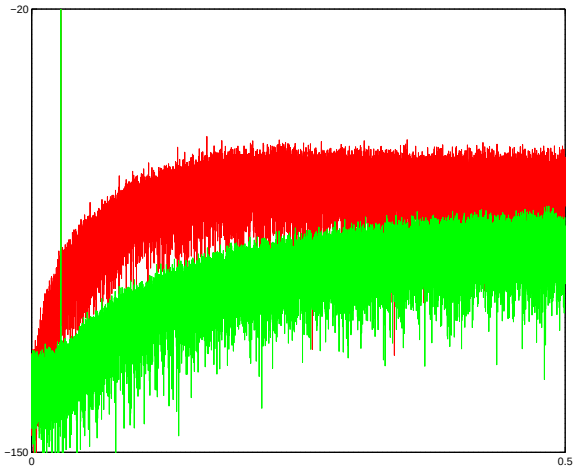
Adaptive Digital Compensation of Analog Circuit Imperfections for Cascaded Delta-Sigma Analog-to-Digital Converters

Technical Report



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Abstract

Cascaded delta-sigma (MASH) analog-to-digital converters offer a good compromise between high accuracy, robust stability and speed. However, they are very sensitive to analog circuit imperfections.

In this thesis, a cascaded 2-0 delta-sigma ADC architecture with 1–1.5-bit first stage and 10–12-bit second stage was investigated. It uses an adaptive digital FIR filter to reduce the noise leakage due to the imperfect error cancellation. For online adaptation, a pseudo-random test signal was injected into the first stage and a simplified block-LMS algorithm, the sign-sign-block-least-mean-square algorithm, was used to update the coefficients of the adaptation filter.

The basic theory and some design considerations were developed under a previous work. However, the reported effective results (signal-to-noise+distortion ratio $SNDR$=75 dB @ f_B=62.5-kHz signal bandwidth) validated only the principle of adaptive noise-leakage compensation, leaving open the question of how to improve this initial performance.

The current thesis deals with the improvements to this technique, and its application to a very fast (sampling frequency f_S=100 MHz, oversampling ratio OSR=8–16, signal bandwidth f_B=3–6 MHz) and high-accuracy (signal-to-noise ratio SNR=13–15-bit) implementation. Such converters have wide applications in high-speed instrumentation, high-definition video, imaging, radar and digital communications. Available behavioral and circuit-level simulation results have confirmed an achievable 13-bit @ 6-MHz ADC, which is a useful performance for a state-of-the-art data converter.

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Chapter 1

Introduction

The title of the thesis is explained first.

This thesis presents an efficient method to design high-resolution and large-bandwidth *analog-to-digital converters*. In order to achieve this goal, the popular *delta-sigma* architecture was used, which provides a high accuracy ($>$13 bits) even in the basic digital CMOS technology implementation, because it features lower sensitivity to the nonidealities of the analog circuitry than "classical" (Nyquist-rate) converters do — a consequence of the time averaging and filtering inherent to the oversampled converter operation. Achieving high resolution and large bandwidth can be accomplished by using higher-order delta-sigma modulators. In addition, to guarantee stable operation even for a higher-order architecture for any input signal and/or initial conditions, the higher-order noise-shaping function was realized using *cascaded* topology. However, cascaded delta-sigma modulators are sensitive to *analog circuit imperfections*, because they rely on the perfect matching between an analog filter (affected by analog circuit imperfections) and its digital counterpart (which can be built with very high accuracy). Even small mismatch causes significant performance degradation. However, this mismatch, which has a random nature, can be estimated by an *adaptive* algorithm, and it can be corrected by a *digital compensation* adaptive filter. In this thesis it is shown that the *adaptive digital compensation of analog circuit imperfections* is an effective method by which the performance of a practical *cascaded delta-sigma analog-to-digital converter* closely approaches its ideal value.

1.1 State-of-the-Art Nyquist-Rate and Delta-Sigma ADCs

Nowadays, the trend in designing analog-to-digital data converters is to obtain high-resolution and large-bandwidth quantization with low-cost fabrication process, which requires low power consumption from a low-voltage supply. For example, a sub-, or deep sub-micron ($0.25 \ldots 0.5$ μm) standard CMOS technology with a single $3.0 \ldots 3.3$ V power supply is widely used in designing ADCs for the above mentioned reasons. However, it is a great challenge to maintain, and

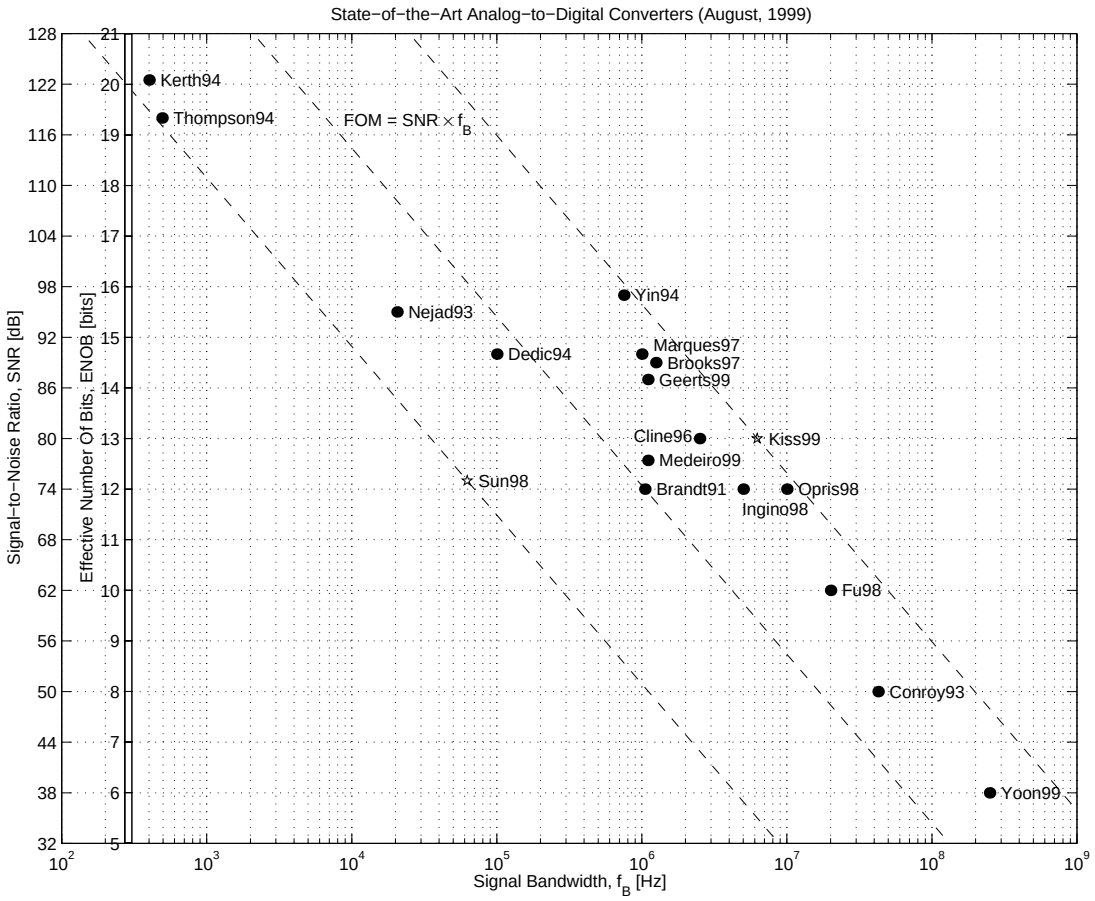

Figure 1.1: State-of-the-art ADCs (August, 1999)

even to improve, the performance level in this low-voltage environment. Due to the trade-off between resolution and signal bandwidth in (mainly) standard CMOS technology there is a large variety of ADCs available, as is illustrated by a selected sample of reported circuits in Tab. 1.1 and Fig. 1.1[1].

Although the power consumption and the chip area of integrated circuits are important characteristics, if these do not have values beyond reasonable limits (e.g. $\sim$500 mW and $\sim$50 mm^2), than one can define a figure of merit FOM as the exclusive product of the signal-to-noise ratio SNR and the signal bandwidth f_B of the ADC:

$$FOM = SNR \times f_B \quad [\text{V/V} \times \text{Hz}]. \tag{1.1}$$

Therefore, Fig. 1.2 provides a one-dimensional, so a more simple-to-read but a more subjective (given by the definition of the FOM by (1.1)) comparison between the selected ADCs.

The medium (>1-MHz) and high (>100-MHz) frequencies are populated by "classical", Nyquist-rate high-speed converters. The achievable accuracy of these converters is limited by the analog circuit imperfections as offset, gain, capacitor-ratio and apperture mismatches. To overcome these nonidealities, especially at

[1]The definition of the effective number of bits $ENOB$ is given by (2.14) on page 15.

Author	SNR @ f_B	f_S / OSR	Architecture	Process / Supply	Power
Nyquist-Rate ADCs					
Yoon99, [1]	6 bits @ 250 MHz	500 MS/s / 1	flash	0.6 μm CMOS / 3 V	330 mW
Conroy93, [2]	8 bits @ 42.5 MHz	85 MS/s / 1	parallel pipelined	1 μm CMOS / 5 V	1100 mW
Fu98, [3]	10 bits @ 20 MHz	40 MS/s / 1	parallel pipelined	1 μm CMOS / 5 V	565 mW
Opris98, [4]	12 bits @ 10 MHz	20 MS/s / 1	digital-calibrated pipelined	0.7 μm CMOS / 5 V	250 mW
Ingino98, [5]	12 bits @ 5 MHz	10 MS/s / 1	analog-calibrated pipelined	0.5 μm CMOS / 3.3 V	338 mW
Cline96, [6]	13 bits @ 2.5 MHz	5 MS/s / 1	digital-calibrated pipelined	1.2 μm CMOS / 5 V	166 mW
Delta-Sigma ADCs					
Kerth94, [7]	122.5 dB @ 400 Hz	256 kHz / 256	4th-order, 1b $\Delta\Sigma$	3 μm CMOS / $\pm$5 V	50 mW
Thompson94, [8]	118 dB @ 492 Hz	126 kHz / 128	5th-order, 1.5b $\Delta\Sigma$	2 μm CMOS / $\pm$5 V	45 mW
Nejad93, [9]	95 dB @ 20.5 kHz	5.25 MHz / 128	2nd-order, 4b $\Delta\Sigma$	2 μm CMOS / 5 V	—
Dedic94, [10]	90 dB @ 100 kHz	3.25 MHz / 16	2-2-2 MASH, 1.5-1.5-1.5b $\Delta\Sigma$	1.2 μm CMOS / 5 V	40 mW
Yin94, [11]	97 dB @ 750 kHz	48 MHz / 32	2-1-1 MASH, 1-1-1b $\Delta\Sigma$	2 μm BiCMOS / $\pm$2 V	180 mW
Brooks97, [12]	89 dB @ 1.25 MHz	20 MHz / 8	2-0 MASH, 5-12b $\Delta\Sigma$	0.6 μm CMOS / 5a-3d V	550 mW
Medeiro99, [13]	77.4 dB @ 1.1 MHz	35.2 MHz / 16	2-1-1 MASH, 1-1-3b $\Delta\Sigma$	0.7 μm CMOS / $\pm$2 V	55 mW
Marques97, [14]	90 dB @ 1 MHz	48 MHz / 24	2-1-1 MASH, 1-1-1b $\Delta\Sigma$	1 μm CMOS / 5 V	230 mW
Geerts99, [15]	87 dB @ 1.1 MHz	52.8 MHz / 24	2-1-1 MASH, 1-1-1b $\Delta\Sigma$	0.5 μm CMOS / 3.3 V	200 mW
Brandt91, [16]	74 dB @ 1.05 MHz	50 MHz / 24	2-1 MASH, 1-3b $\Delta\Sigma$	1 μm CMOS / 5 V	41 mW
Sun98, [17]	75 dB @ 62.5 kHz	1 MHz / 8	2-0 MASH, 1-12b $\Delta\Sigma$	1.2 μm CMOS / 5 V	—
Kiss99, [18]	$\approx$80 dB @ 6.25 MHz	100 MHz / 8	2-0 MASH, 1.5-10b $\Delta\Sigma$	0.25 μm CMOS / 3.3 V	$\approx$300 mW

Legend: SNR – signal-to-noise ratio; f_B – signal bandwidth; f_S – sampling frequency; $OSR = f_S/(2\,f_B)$ – oversampling ratio.

Table 1.1: State-of-the-Art ADCs (August, 1999)

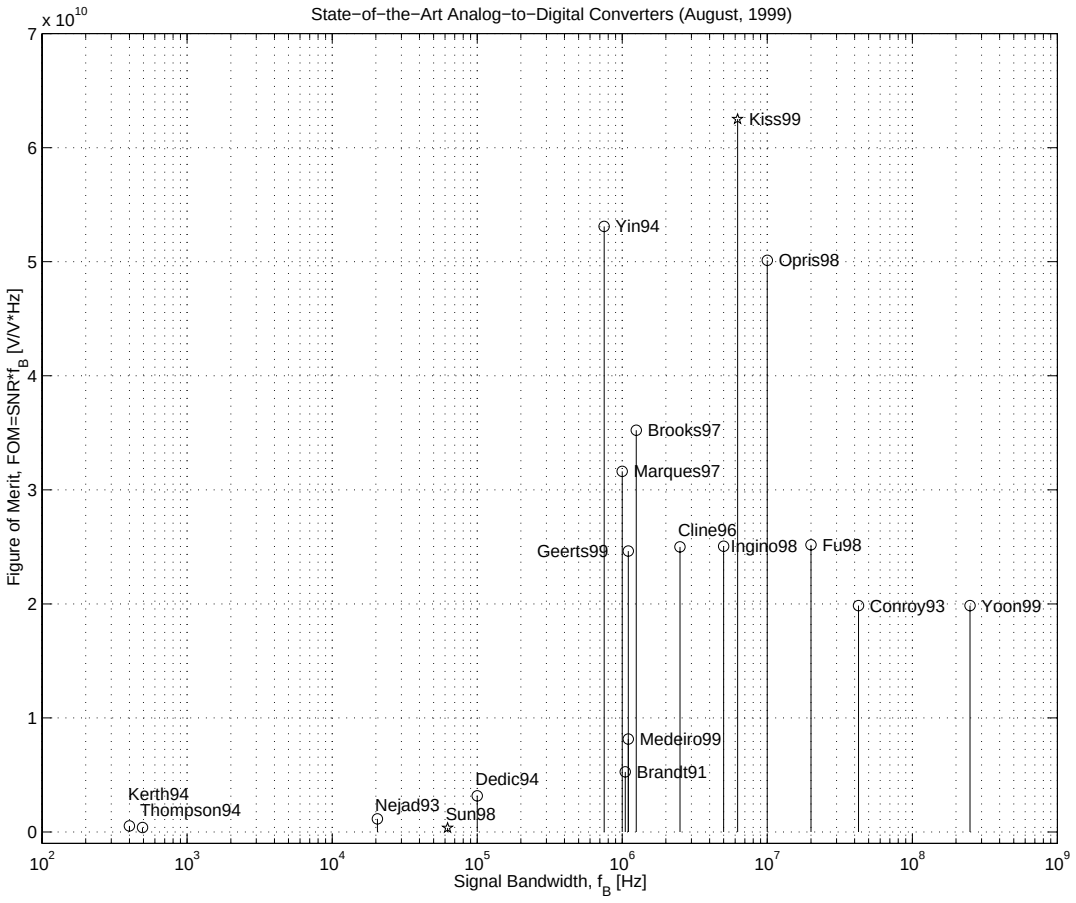

Figure 1.2: Figure of merit for state-of-the-art ADCs

higher resolution than 10 bits, calibrating circuits are often used. Recently, a 6-bit 500-MSamples/s full-flash ADC was reported, which was implemented in 0.4-μm CMOS technology and dissipated 400-mW from a 3.3-V supply [1]. For better resolution but less bandwidth (8-b @ 85-MS/s), a time-interleaved (or parallel) pipelined ADC was built [2]. A digital background calibration was used in another time-interleaved pipelined ADC to trade higher resolution for lower bandwidth (10-b @ 40-MS/s) [3]. Also, a 5-V, 12-b @ 20-MS/s, digital background calibrated [4], and a 3-V, 12-b @ 10-MS/s, analog continuously calibrated [5] pipelined ADCs were reported.

The 12-bit resolution seems to be the upper limit for Nyquist-rate converters implemented in low-cost process even if analog or digital correction circuitry is used. However, a number of high-speed pipelined converter implementations have been reported with resolutions in excess of 12 bits, e.g. [6], [19], [20]. A low-power digital-calibrated pipelined ADC with 13-bits @ 2.5-MHz performance is presented in [6]. In order to achieve a resolution of 16 bits at 500-kHz signal bandwidth a 32-bits on-chip microcontroller was used for self calibrating a pipelined ADC [19]. Laser-trimming techniques can also adjust the accuracy of the pipelined ADCs, e.g. for a 13-bit @ 1.25-MHz performance [20].

Unfortunately, on-chip calibration tends to significantly increase the complexity of pipelined converters. Moreover, one-time calibration schemes (usually at power-up) cannot compensate for the effects of supply and temperature variations. Especially the last two cited circuits [19], [20] require large chip area (e.g. 150×240 mm^2 in [19]) and expensive fabrication costs, so they could not be included into the list of selected ADC samples from Tab. 1.1 and Fig. 1.1.

Above 13-bit linearity essentially different converters, the so-called delta-sigma data converters can satisfy the high-accuracy and low-cost need in many applications, by using oversampling and noise-shaping techniques to suppress the out-of-band quantization noise. The first and most obvious applications of delta-sigma converters are in instrumentation, e.g. 122.5 dB @ 400 Hz [7] and 118 dB @ 492 Hz [8], and in digital audio, e.g. 96 dB @ 20.5 kHz [9]. In the last few years, successful attempts have been made to use the delta-sigma architecture for medium frequencies ($>$1-MHz) as well, and recently published papers (Tab.1.1 and Fig. 1.1) sustain the trend of extending the signal bandwidth while preserving the high accuracy ($>$13 bits).

For such a large signal bandwidth it seems that the cascaded delta-sigma (MASH[2]) topology is suitable, and, therefore is preferred by the researchers. However, it is well-known that this architecture, as in general every cancellation-based architecture, is sensitive to analog circuit imperfections, because they rely on the perfect matching of the transfer functions of the two internal signal paths, one predominantly analog, and the other predominantly digital. This causes quantization noise leakage, and in turn performance degradation. To prevent this, in [12] a multibit (5-bit) quantizer was used in the first stage, which reduces the power of the noise leakage, but which needs a mismatch-shaping digital-to-analog converter in the feedback path. In addition, the second stage was built from a multibit (12-bit) pipelined ADC. Therefore, this high-performance converter (89 dB @ 1.25 MHz !) ended up with a relatively high power consumption (550 mW). Another approach was analyzed and implemented, but which did not necessitate digital correction by using (claimed) optimized architecture and coefficients for a fourth-order cascaded (2-1-1 topology) modulator instead [13]. Therefore, very low power consumption (55-mW) was achieved. Two similar 2-1-1 cascaded but single-bit topologies with (claimed) optimized coefficients were successfully implemented with 5-V [14] and 3-V [15] power supplies. A remarkable design and implementation of 2-1 cascaded delta-sigma ADC was published in 1991 [16] which achieved an impressive (considering the year of publication also) 74-dB @ 10.5-MHz performance.

In the previous cascaded delta-sigma ADC designs [10], [11], [12], [13], [14], [15], [16], the quantization noise leakage was considered as an intrinsic drawback of the topology. Indeed, the noise leakage can be reduced in the analog domain by careful analog circuit design [13], [14], [15], [16] or by the use of multibit

[2]The notation n_1-n_2-n_3-... used in Tab. 1.1 indicates the number of cascaded stages, n_i is the order of the ith delta-sigma loop, and $n_1 + n_2 + n_3$ is the effective order of the MASH. For example, 2-1-1 [14] was built from 3 stages, a second-order modulator is followed by 2 first-order loops, so the effective order of the MASH ADC is 4.

first stage [12], but only to a limited degree, especially if low-cost fabrication must be used. However, if the noise leakage was handled somehow, the performance would be further increased. On the other hand, several digital domain solutions have been developed including off-line calibration [21] and on-line correction [22], [23], [24], [25].

A robust cascaded delta-sigma structure to analog circuit imperfections was proposed in [26]. The so-called indirectly residue-compensated delta-sigma quantizers estimate differently the quantization error of the first stage, which is quantized by a multibit second stage. If the residue quantizer (second stage) has 10-bit resolution and linearity, and the first stage has also a 5-bit quantizer, than an oversampling ratio of $OSR = 10$ provides an SNR performance of 105 dB. However, this modulator also requires mismatch-shaping digital-to-analog converter in the first stage, which means larger chip-area and bigger power consumption.

1.2 The Proposed ADC

An on-line digital-correction method is presented in this thesis. Based on the present work, one can use simple structure and avoid mismatch-shaping digital-to-analog converter in the first stage, and one can allow noise leakage in the output using more relaxed requirements for the integrators, because a simple and effective method can digitally compensate for the analog circuit imperfections in cascaded delta-sigma ADCs.

In this thesis a cascaded 2-0 delta-sigma ADC architecture with 1–1.5-bit first stage and 10–12-bit second stage was investigated, which uses an adaptive digital FIR filter to reduce the noise leakage due to the imperfect error cancellation. For adaptation, a pseudo-random test signal was injected into the first stage and a simplified block-LMS algorithm, the sign-sign-BLMS, was used to update the coefficients of the adaptation filter. The basic theory and some design considerations were developed under a previous work [27], [28], [29], [30]; also, a working prototype of the integrated ADC was successfully fabricated and tested [17], [31]. However, the reported effective results (signal-to-noise+distortion ratio $SNDR$=75 dB @ f_B=62.5-kHz signal bandwidth [17]) validated only the principle of adaptive noise-leakage compensation, leaving a considerably large room to improve this initial performance.

The current thesis deals with the optimization to this technique, and its application in a very fast (sampling frequency f_S=100 MHz, oversampling ratio OSR=8–16, signal bandwidth f_B=3–6 MHz) and high-accuracy (signal-to-noise ratio SNR=13–15-bit) implementation [18], [32], [33], [34]. Such converters may have wide applications in high-speed instrumentation, high-definition video, imaging, radar and digital communications. Available behavioral and circuit-level simulation results has confirmed an achievable 13-bit @ 6-MHz ADC, which is a useful performance for a state-of-the-art data converter (Tab. 1.1 and Fig. 1.1). Moreover, Fig. 1.2 shows that the proposed ADC has the highest figure of merit FOM, (1.1), among these high-performance data converters.

1.3 Thesis Structure

This thesis tries to guide the reader gradually through the main issues of the adaptive cascaded delta-sigma modulators. Many figures and selected simulation results show, explain and illustrate the presented topic.

Following this Introduction, Chapter 2 begins by presenting the basics of quantization, and two key features of delta-sigma modulators: oversampling and quantization noise shaping. To keep a logical and progressive order, the first-order delta-sigma ADCs are briefly described next. Because the first stage of our cascaded delta-sigma ADC was chosen to be a second-order delta-sigma modulator, this subject is detailed in the next section. The possibility of using a tri-level quantizer is also investigated, which is a key element in optimizing the cascaded delta-sigma structure. Detailed design clues are presented for the second-order delta-sigma ADC, supported by simulation results, which are only briefly marked in the available bibliography (e.g. coefficient calculus, internal voltage swing, the gain of a single-bit/multibit quantizer). Higher-order delta-sigma modulators are briefly described next. A short selection guide of single-loop delta-sigma modulators concludes this chapter.

Chapter 3 first presents a comparative analysis between cascaded 2-0 delta-sigma ADC structures. In order to achieve maximum peak-SNR performance, the use of bi-level and tri-level first-stage quantizer, and different interstage coefficients are investigated. The high sensitivity of the cascaded structure to analog circuit imperfections is studied next. Simulation results are coherent with the theoretical assumptions about the quantization noise leakage.

Chapter 4 deals with the adaptive digital correction of the noise leakage. The possibility of using a test signal for on-line compensation is investigated first. The hardware complexity of the adaptive digital compensation filter is studied in order to being reduced. Next, the optimization of the adaptation process is presented. In order to improve the performance of the adaptive MASH, the parameters of the adaptive compensation process, and the properties of the test signal are analyzed.

Chapter 5 presents a high-frequency (sampling frequency $f_S = 100$ -MHz) switched-capacitor implementation[3] of the cascaded 2-0 delta-sigma modulator designed at system level in the previous chapters.

Finally, Chapter 6 summarizes the original achievements and conclusions, and gives a few suggestion for future work.

[3]The prototype chip design, as well Chapter 5, were contributed by my colleague at Oregon State University, José Silva (`silva@ece.orst.edu`).

Chapter 2

Single-Loop Delta-Sigma ADCs

Delta-sigma data converters have been known for nearly fifty years, since 1954 [35, Introduction], but only in the last two decades has the technology, namely the high-density digital VLSI, matured sufficiently to manufacture them as inexpensive monolithic integrated circuits. They are now used in many applications where a low-cost, low to medium signal bandwidth, low-power and high-resolution data converters are required.

The heart of any analog-to-digital converter (ADC) is a quantizer. Therefore, we begin our discussion by describing some basic principles of the quantization. Next, two key features of delta-sigma data modulators: oversampling and noise shaping are presented, which are followed by a detailed system-level analysis of first-order and second-order delta-sigma analog-to-digital converters. Also, some properties of higher-order modulators are presented in the end of this chapter.

2.1 Quantization

Analog-to-digital conversion of a signal is traditionally described in terms of two separate operations: uniform sampling (or quantization, discretization) in time, and quantization (or discretization) in amplitude [36, Section 3.0], [37].

Ideal periodic sampling of a continuous-time signal $u(t)$ at rates f_S more than twice the signal bandwidth f_B need not introduce distortion. In other words, the discretization or quantization in time, as a result of sampling, is completely invertible operation, because according to the Nyquist sampling theorem for $f_S \geq 2\, f_B$, the original continuous-time signal $u(t)$ can be perfectly reconstructed from its discrete-time samples $u[n] = u(nT_S)$, without any loss of signal information. In practice, to assure that the Nyquist sampling theorem is indeed satisfied, and to avoid aliasing, the continuous-time input signal $u_{in}(t)$ is filtered by an anti-aliasing filter before sampling, and, therefore, its bandwidth f_B is surely limited to $\frac{f_S}{2}$ (Fig. 2.1). If $f_S \geq 2\, f_B$, than the spectrum $U(f)$ of the sampled discrete-time sequence $u[n]$ is a periodic replica of the initial, continuous-time input signal's $u_{in}(t)$ spectrum $U_{in}(f)$ with a period of $T_S = \frac{1}{f_S}$ (Fig. 2.1).

On the other hand, quantization is non-invertible process, since an infinite number of input amplitude values of the discrete-time analog signal $u[n]$ are

mapped into a finite number of output amplitude values of the (discrete-time) digital signal $v[n]$ (Fig. 2.1) [36, Section 3.2.0], [37]. In other words, even an ideal quantization process inherently introduces distortion, and our primary objective in designing analog-to-digital converters is to limit this distortion [38, Section 1.2.1].

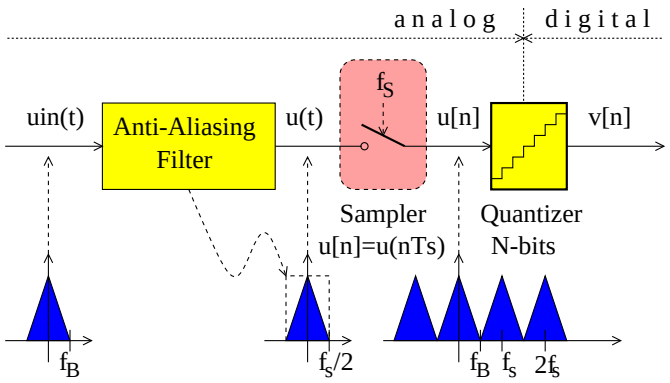

Figure 2.1: General analog-to-digital converter

A N-bit ideal quantizer is presented in Fig. 2.2.a, where $v[n]$ is the digital output word stream while $u[n]$ and V_{ref} are the sampled analog input signal and the reference voltage, respectively. If the digital output $v[n]$ is converted back into an analog discrete-time signal $v_a[n]$ from which the sampled analog input signal $u[n]$ is subtracted, the result will be the quantization error sequence $q[n]$ (Fig. 2.2.b):

$$q[n] = v_a[n] - u[n]. \tag{2.1}$$

In addition, if the sampled analog input $u[n]$ is a ramp signal, than the quantized output $v_a[n]$ appears as a staircase, and the quantization error sequence $q[n]$ has a sawtooth form (Fig. 2.3.a). In Fig. 2.3.a the resolution of the quantizer is $N = 3$ bits, the full-scale range of the input is $FSR = 2\,A_{max}$, and, therefore, its step size Δ, or its 1 LSB (least significant bit), is given by

$$\Delta = 1LSB = \frac{2\,A_{max}}{2^N - 1} = \frac{2}{7} = 0.28 \text{ V}. \tag{2.2}$$

Note that the amplitude of the quantization error $q[n]$ is limited to $\pm\frac{\Delta}{2}$ as far as the analog input signal satisfies the condition:

$$|u[n]| \leq A_{max} + \frac{\Delta}{2} \quad \Longrightarrow \quad |q[n]| \leq \frac{\Delta}{2} \tag{2.3}$$

Under these circumstances the quantizer is said to be not overloaded or saturated. On the other hand, for $|u[n_0]| > A_{max} + \frac{\Delta}{2}$, and hence $|q[n_0]| > \frac{\Delta}{2}$, the quantizer is said to be overloaded [37]. Note that this statement is true for all input signals, not just for ramps.

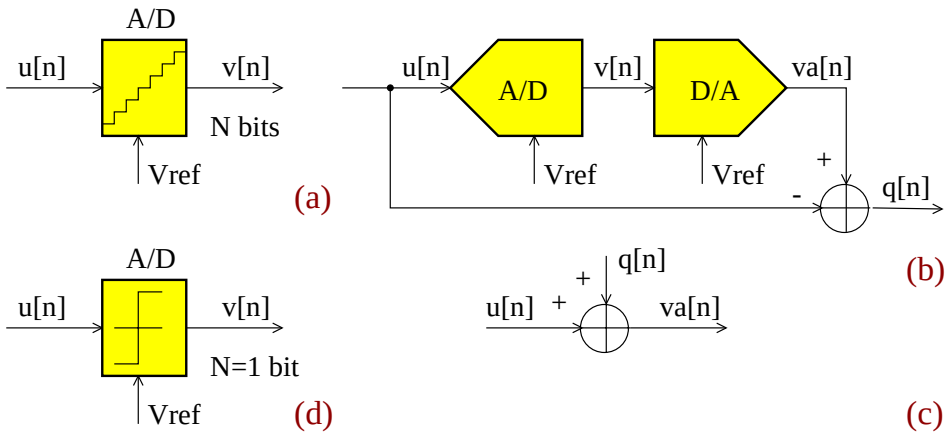

Figure 2.2: (a) Ideal N-bit quantizer; (b) quantization error generation: $q[n] = v_a[n] - u[n]$; (c) discrete-time domain modeling of the quantization process: $v_a[n] = u[n] + q[n]$; (d) ideal single-bit quantizer

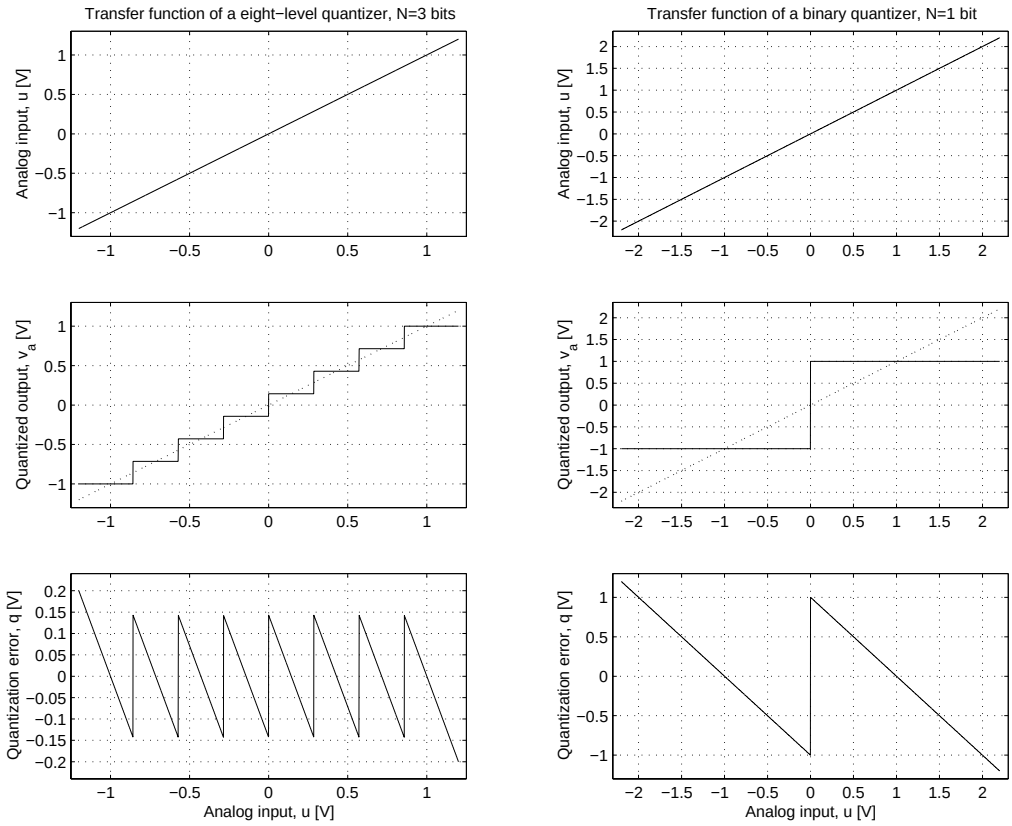

Figure 2.3: Transfer function of an ideal N-bit quantizer for (a) $N = 3$ bits and (b) $N = 1$ bit

2.1.1 Quantization Error

According to (2.1), the quantization error $q[n]$ is completely defined by the input signal $u[n]$. However, if the input signal $u[n]$ changes rapidly from sample to

sample by amounts comparable with or greater than Δ without causing saturation, then the quantization error $q[n]$ is largely uncorrelated from sample to sample and has equal probability of lying anywhere in the range $[-\frac{\Delta}{2}; +\frac{\Delta}{2}]$. Therefore, it seems to be plausible to assume that the quantization error $q[n]$ has statistical properties that are independent of the input signal $u[n]$, so it can be represented by a random variable, which behaves as a noise, namely, as a "quantization noise"[1] [38, Section 1.2.1].

The equation (2.1) can be rearranged [39] as

$$v_a[n] = u[n] + q[n]. \tag{2.4}$$

Although the equation (2.4) is exact for every time instance, it can express also an intuitive link between the statistical properties of the sampled analog input $u[n]$, the quantized output $v_a[n]$ and the quantization error $q[n]$.

A rigorous analysis of a nonlinear system, such a quantizer, is a difficult and complicated task. To further simplify the analysis of the quantization noise, the following assumptions about the noise process and its statistics are traditionally made, which are called the "input-independent additive white-noise approximation" (weak version) [38, Section 2.3], [37]:

Property 1. The quantization error sequence $q[n]$ is a sample sequence of a stationary random process.

Property 2. The quantization error sequence $q[n]$ is uncorrelated with the input sequence $u[n]$.

Property 3. The probability density function of the quantization error process $PDF(q[n])$ is uniform over the range $[-\frac{\Delta}{2}; +\frac{\Delta}{2}]$ (Fig. 2.4.a).

Property 4. The power spectral density of the quantization error process $PSD_Q(\omega)$ is flat (Fig. 2.4.b). (The quantization error is a white noise process.)

These approximations simplify the system analysis because they replace a deterministic nonlinearity by a stochastic linear system, thereby permitting the use of linear system methods to analyze a nonlinear system containing a quantizer [38, Section 2.3]. Also, under certain conditions, namely the Bennett's conditions:

Condition 1. The input signal $u[n]$ is not in the overloaded region.

Condition 2. The resolution N of the quantizer is asymptotically large.

Condition 3. The step size Δ of the quantizer is asymptotically small.

Condition 4. The joint probability density function of the input signal $u[n]$ at different sample times is smooth.

[1] In this thesis the concepts of "quantization error" and "quantization noise" will be used interchangeably. However, "quantization error" is a more descriptive and precise term, and it specifically refers to the time-domain signal $q[n] = v_a[n] - u[n]$, and "quantization noise" will emphasize its assumed white noise properties — detailed later in this section [38, Section 3.1.0].

these assumptions (Properties 1–4) are reasonable [38, Section 2.3], [37].

In conclusion, under these certain conditions (Conditions 1–4) the quantizer can be modeled as an input-independent additive white-noise source, so the equation (2.4) is valid in the frequency domain also, that is, the digital output $V(z)$ (or the quantized output $V_a(z)$ — if the gain of the DAC is assumed to be equal to unity) can be calculated as the sum of the analog input $U(z)$ and the quantization noise $Q(z)$:

$$V(z) = V_a(z) = U(z) + Q(z). \tag{2.5}$$

The relation (2.5) can be intuitively verified on Fig. 2.5, where the spectrum of the quantization error seems to be flat (white noise) and completely uncorrelated with the input signal. In this example a full-scale analog input sinewave $A_u = A_{max}$ with a frequency of $f = 0.03 f_S$ was applied to a $N = 10$-bit quantizer, so the Bennett's conditions were satisfied with a good approximation. Note, however, that the probability density function of the quantization error is not quite uniformly distributed over the range $[-\frac{\Delta}{2}; +\frac{\Delta}{2}]$. If the input was a more "busy" signal, for example a sum of sinewaves, than $PDF(q)$ would be more uniform.

A mathematical analysis of the quantization process is given in [36, Section 3.2]. It has been demonstrated that as the step size Δ of the quantizer decreases, the quantization error sequence $q[n]$ can be considered less correlated (the autocorrelation of $q[n]$ is low) even if the input sequence $u[n]$ is highly correlated (the autocorrelation of $u[n]$ is high) [36, Section 3.2.3]. In addition, it was shown that for small values of the step size Δ, the quantization error sequence $q[n]$ is in fact uncorrelated with the input sequence $u[n]$, although the quantization error $q[n]$ is completely determined by the input sequence $u[n]$, shown by (2.1) [36, Section 3.2.4].

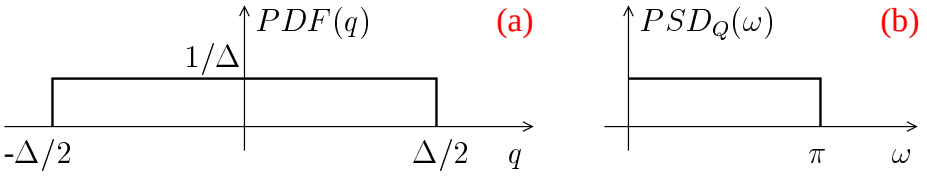

Figure 2.4: Statistical properties of the quantization error as input-independent additive white noise: (a) probability density function $PDF(q)$ and (b) power spectral density $PSD_Q(\omega)$

2.1.2 Performance Modeling

Next, based on the input-independent additive white-noise approximation for the quantization error, one can derive the signal-to-noise ratio SNR performance of a N-bit ideal analog-to-digital converter or quantizer. According to this approximation (Properties 1 and 3), the quantization error $q[n]$ is a uniformly distributed random variable ($PDF(q[n]) =$ constant) over the range $[-\frac{\Delta}{2}; +\frac{\Delta}{2}]$ (Fig. 2.4.a).

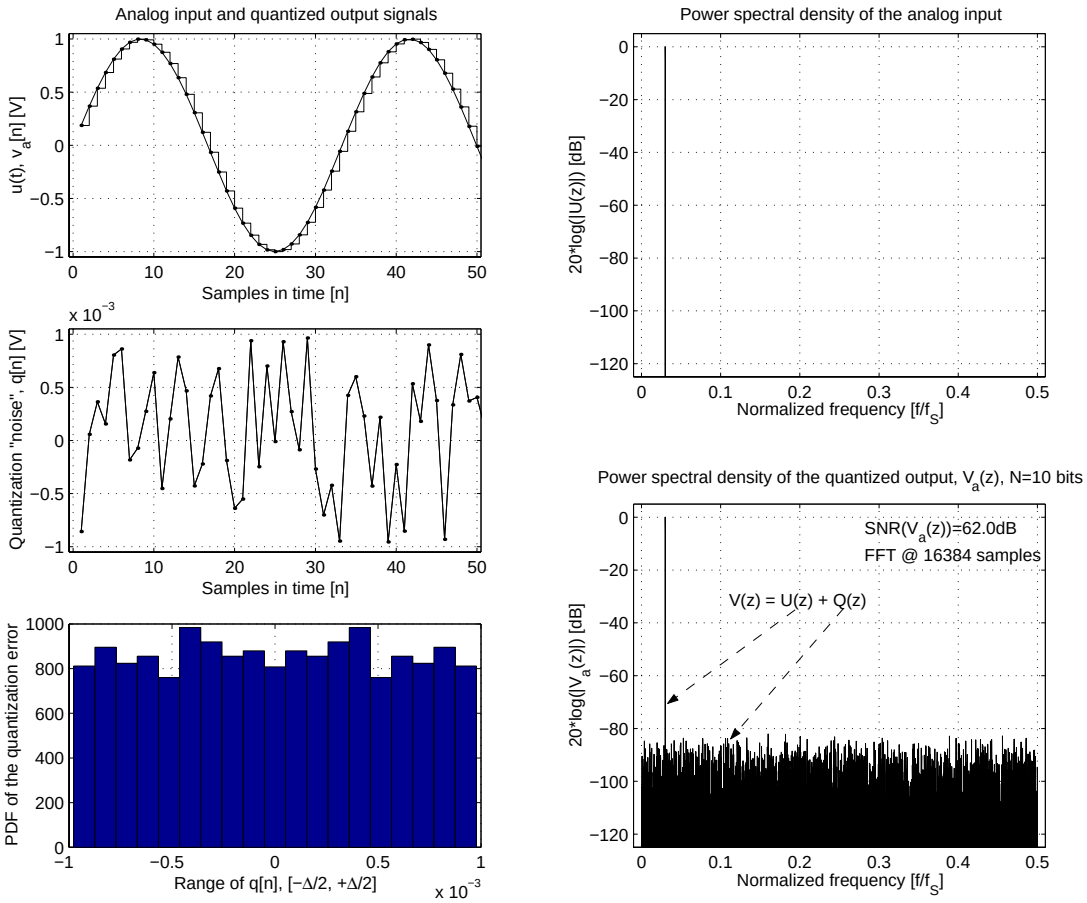

Figure 2.5: The spectrum of a quantized sinewave for N=10 bits

Therefore,

$$\int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} PDF(q[n])\,\mathrm{d}q = 1 \Longrightarrow PDF(q[n]) = \frac{1}{\Delta}, \forall q[n] \in \left[-\frac{\Delta}{2}; +\frac{\Delta}{2}\right] \qquad (2.6)$$

For a zero mean $q[n]$

$$\bar{q} = \int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} PDF(q[n])\, q\,\mathrm{d}q = \frac{1}{\Delta}\int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} q\,\mathrm{d}q = 0, \qquad (2.7)$$

its variance or power is [40, Section 4.4]

$$\sigma_q^2 = P_q = \int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} PDF(q[n])\, q^2\,\mathrm{d}q = \frac{1}{\Delta}\int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} q^2\,\mathrm{d}q = \frac{\Delta^2}{12}. \qquad (2.8)$$

According to Property 4, the spectrum of the quantization error is uniformly distributed ($PSD_Q(\omega) = \text{constant}$) over the digital frequency domain $[0;\pi]$ (Fig. 2.4.b), so its power spectral density can be calculated by

$$P_q = \int_0^{\pi} PSD_Q(\omega)\,\mathrm{d}\omega = \sigma_q^2 \quad \Longrightarrow \quad PSD_Q(\omega) = \frac{\sigma_q^2}{\pi}. \qquad (2.9)$$

In conclusion, the signal-to-noise ratio $SNR_{Nyquist}$ of a Nyquist-rate converter for a sinewave input with amplitude A_u is given by

$$SNR_{Nyquist} = 10\log_{10}\frac{P_u}{P_q} = 10\log_{10}\left(\frac{A_u^2}{2}\frac{12}{\Delta^2}\right) \quad (2.10)$$

$$= 10\log_{10}\left(6\,A_u^2\left(\frac{2^N-1}{2\,A_{max}}\right)^2\right) \quad (2.11)$$

$$= 20\log_{10}\frac{A_u}{A_{max}} + 6.02\,N + 1.76 \quad [\text{dB}], \quad (2.12)$$

and for a full-scale sinewave input

$$SNR_{Nyquist_{max}} = 6.02\,N + 1.76 \quad [\text{dB}]. \quad (2.13)$$

Note that for each extra bit of resolution in the ADC, i.e. for every increment in N, there is about a 6 dB improvement in the SNR. Thus, there is a direct relationship between the resolution of an ADC in bits and its SNR performance in dB-s, and it is common to equate differences in SNR in dB to bits, by dividing the dB value by 6 [37]. More precisely, one can define the effective number of bits $ENOB$ of a converter from its SNR performance by [41, Section 6.2], [42]:

$$ENOB = \frac{SNR\,[\text{dB}] - 1.76\ \text{dB}}{6.02\ \text{dB}}\,[\text{bits}]. \quad (2.14)$$

For example, a $N = 10$-bit converter has an $SNR = 61.86$ dB based on (2.13). This theoretical value matches well with the $SNR = 62.0$ dB obtained by simulations (Fig. 2.5).

2.2 Oversampling Converters

Consider first a band-limited signal with a spectrum which lies in the frequency-band $[0;\, f_B]$, or equivalently in $[0;\omega_B]$. Oversampling is a technique that improves the resolution obtained from a conventional Nyquist-rate converter by sampling the signal at a rate considerably faster ($f_{S_{OS}} = 2\,OSR\,f_B$, $OSR \gg 1$) than the required Nyquist rate ($f_{S_{Nyquist}} = 2\,f_B$) (Fig. 2.6). Typical values for the oversampling ratio (for normalized sampling frequency $f_S = \frac{\omega_S}{2\pi} = 1$)

$$OSR = \left.\frac{f_S}{2\,f_B}\right|_{f_S=1} = \frac{\pi}{\omega_B} \quad (2.15)$$

are between 8 and 512, and usually it can be represented as a power of 2, i.e. $OSR = 2^r$, to facilitate the digital decimating filter.

Because the maximum available sampling frequency is limited by the state-of-the art VLSI technology (e.g. for CMOS switched-capacitor circuits is around $f_S = 100$ MHz), the oversampling technique reduces the available signal bandwidth f_B. In other words, oversampling converters trade signal bandwidth for higher resolution.

By using oversampling, the power spectral density of the quantization error is stretched over the whole band $[0;\pi]$, so its power in the signal band of interest $[0;\omega_B]$ will be reduced proportionally with OSR (Fig. 2.7) [36, Section 3.2.7], [39, Section 14.1]. Therefore, the so-called in-band quantization noise power P_0 is given by:

$$P_{0_{OS}} = \int_0^{\omega_B} PSD_Q(\omega)\,\mathrm{d}\omega = \frac{\sigma_q^2}{\pi}\int_0^{\frac{\pi}{OSR}} \mathrm{d}\omega = \frac{\sigma_q^2}{OSR} \tag{2.16}$$

The power of the out-of-band ($\omega > \omega_B$) quantization noise will be reduced significantly, in ideal case: it will be eliminated, by a digital low-pass filter, and the oversampled digital sequence will be processed by a decimator, which downsamples it to the Nyquist rate ω_B (Fig. 2.6). It turns out that the signal-to-noise ratio SNR_{OS} for an oversampling converter is given by

$$\begin{aligned} SNR_{OS} &= 10\log_{10}\frac{P_u}{P_{0_{OS}}} \\ &= 20\log_{10}\frac{A_u}{A_{max}} + 6.02\,N + 10\log_{10} OSR + 1.76 \quad [\mathrm{dB}]. \end{aligned} \tag{2.17}$$

If we consider the oversampling ratio being $OSR = 2^r$, than $10\log_{10} OSR = 3.01\,r$ [dB], so every doubling of the oversampling ratio, i.e. for every increment in r, the SNR_{OS} improves by about 3 dB, or the resolution improves by $\frac{1}{2}$ bit. In other words, the oversampling converter has a 3-dB/octave or 0.5-bit/octave SNR improvement [39, Section 14.1], [37].

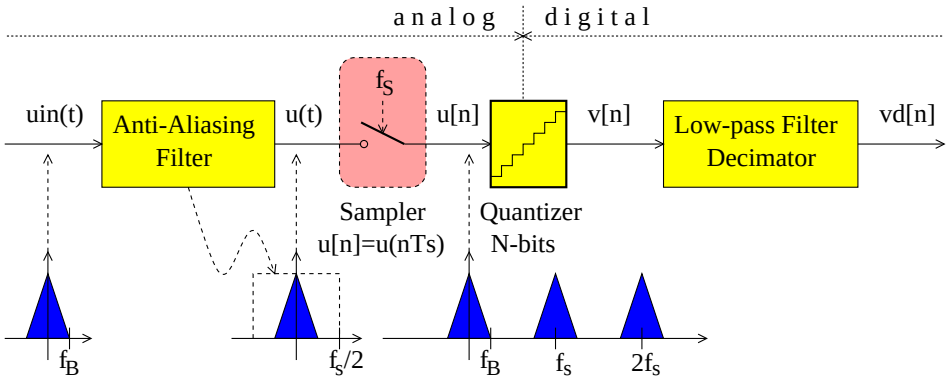

Figure 2.6: General oversampling analog-to-digital converter ($OSR = 2$)

2.3 Noise-Shaping Converters

The in-band quantization noise power can be further suppressed by using quantization noise shaping in addition to oversampling. Nowadays, the most popular noise-shaping converters are the so-called delta-sigma converters or delta-sigma modulators. The general block-structure of a delta-sigma ADC is presented in

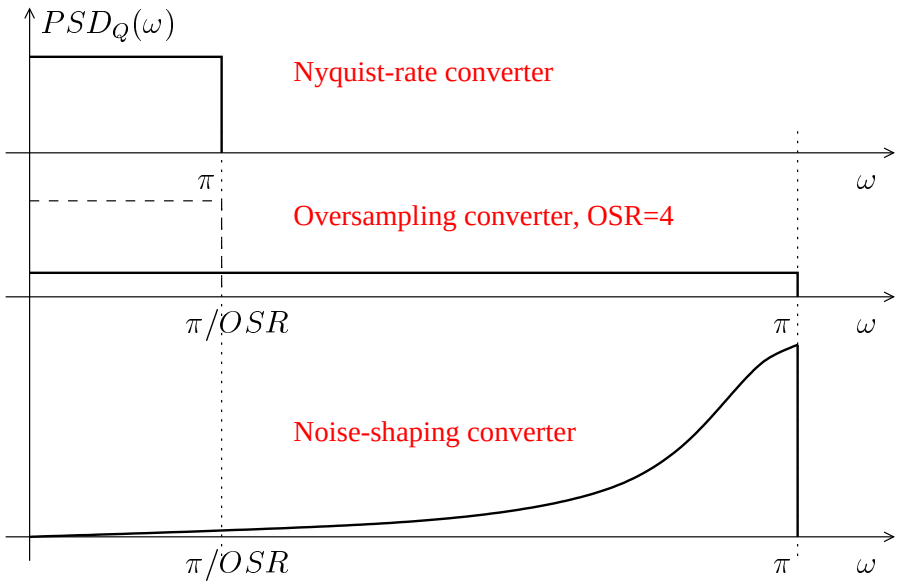

Figure 2.7: The power spectral density of the quantization noise $PSD_Q(\omega)$ for different converters

Fig. 2.8.a, which consists of an analog loop filter $H(z)$ and a coarse N-bit quantizer enclosed in a feedback loop.

Since this system usually contains one integrator or cascade of integrators as the analog loop filter, its name is "delta-sigma" modulator, where the "delta" (Δ) denotes the difference operation ($e[n] = u[n] - v_a[n]$) made in the input node, and where the "sigma" (Σ) denotes the summation (accumulation) performed by the integrators [38, Introduction].

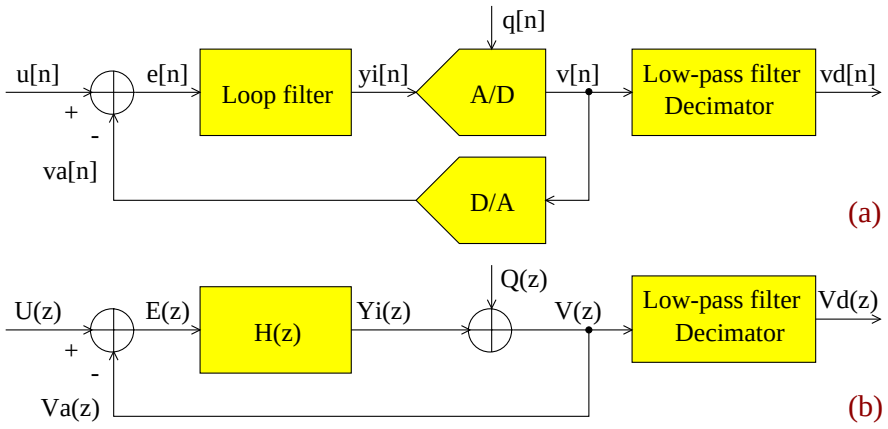

Figure 2.8: (a) General structure of a noise-shaping ADC and (b) its linearized model (for the DAC a unity gain was assumed)

2.3.1 Basic Operation

To rigorously analyze this delta-sigma converter in the frequency domain is a difficult task due to the presence of the nonlinear quantizer. To simplify this analysis, under certain conditions (Conditions 1–4, Section 2.1.1) one can use the input-independent additive white-noise approximation for the quantization error and analyze the delta-sigma modulator as a linear system. The linearized model is presented in Fig. 2.8.b. Therefore, the calculations became trivial:

$$V(z) = (U(z) - V(z))\, H(z) + Q(z) \tag{2.18}$$

$$\Longrightarrow V(z) = \frac{H(z)}{1+H(z)}\, U(z) + \frac{1}{1+H(z)}\, Q(z) \tag{2.19}$$

From (2.19) it turns out that the delta-sigma converter processes independently the signal and the noise components. Therefore, it can be defined its signal transfer function $STF(z)$ and noise transfer function $NTF(z)$:

$$STF(z) = \left.\frac{V(z)}{U(z)}\right|_{Q(z)=0} = \frac{H(z)}{1+H(z)} \tag{2.20}$$

$$NTF(z) = \left.\frac{V(z)}{Q(z)}\right|_{U(z)=0} = \frac{1}{1+H(z)} \tag{2.21}$$

and one can also write the output signal $V(z)$ as the combination of the input signal $U(z)$ and the quantization noise signal $Q(z)$, with each being filtered by the corresponding transfer function:

$$V(z) = STF(z)\, U(z) + NTF(z)\, Q(z). \tag{2.22}$$

If one chooses a low-pass loop filter $H(z)$, which have large magnitude over low frequencies, i.e. over the frequency-band of interest $[0;\omega_B]$, and small magnitude over high frequencies, than the magnitude of the signal transfer function $|STF(z)|$ will approximate unity over the frequency-band of interest $[0;\omega_B]$, hence it will not distort the signal, but the magnitude of the noise transfer function $|NTF(z)|$ will approximate zero over the same band, hence the quantization noise power will be reduced accordingly. The power spectral density of a shaped quantization noise is presented in Fig. 2.7. By doing so, the signal-band spectral composition of the analog input $u[n]$ and digital output $v[n]$ signals will be linearly related, but outside the signal band the spectral composition will differ substantially [26]. Therefore, a digital low-pass filter is used to suppress the out-of-band quantization noise, and a decimator to downsample the filtered but oversampled digital sequence to the Nyquist rate ω_B (Fig. 2.8).

In other words, due to the large loop gain given by $H(z)$ over low frequencies, the output sequence $v[n]$ will track with high accuracy the low-frequency input sequence $u[n]$, and the delta-sigma loop keeps the error $e[n]$ very low over low frequencies. However, in order to compare the digital output $v[n]$ with the analog input $u[n]$ and to preserve the high performance of the modulator, it has to be

converted back into an analog signal $v_a[n]$ by a highly linear digital-to-analog converter.

The linearity of the DAC in the feedback loop has to be as good as the overall linearity of the modulator. Because it is difficult to achieve this high linearity in actually available DACs due to analog circuit imperfections (e.g. limited capacitor-ratio accuracy, typical value: 0.1%), inherently linear single-bit DACs are widely used in delta-sigma converters. However, multibit delta-sigma modulators were successfully implemented by using a so-called mismatch-shaping multibit DAC in the feedback path which provides the required high linearity [26], [38, Section 8.3.3]. Moreover, analog [43], [44] and digital [45], [9], [38, Section 8.4] correction techniques are available for multibit delta-sigma ADCs. Unfortunately, multibit delta-sigma ADCs require more complex circuitry, larger chip area and bigger power consumption.

Note that this thesis focuses exclusively on *low-pass* delta-sigma modulators, but the delta-sigma technique is widely applied for *band-pass* signals also. Band-pass delta-sigma modulation allows high-resolution conversion of band-pass signals, if f_S is much greater than the signal bandwidth f_B, rather than the highest signal frequency. Band-pass sigma-delta modulators can be used in AM digital radios or receivers for digital cellular mobile radios [37], [38, Chapter 9].

In conclusion, the key-words in delta-sigma converters are: oversampling, noise shaping and single-bit[2] quantization.

2.3.2 Circuit-Level Considerations

According to what was presented so far, a delta-sigma modulator usually contains one or several integrators, a simple comparator and a single-bit DAC included in a feedback loop. The key points in its functioning are to oversample the input analog signal and to high-pass shape the quantization noise using a large loop gain at low frequencies provided by the integrators, and to filter out digitally the out-of-band noise.

Because of oversampling, both the analog and digital circuits should work at high speeds, usually near to the state-of-the-art clock frequency. On the other hand, the requirements for analog continuous-time anti-aliasing filter are relaxed, which is a great advantage of oversampling converters over Nyquist-rate converters.

The analog loop filter should provide a large gain at low frequencies, but this gain can have large fluctuations once it exceeded the required minimum value. Generally speaking, the requirements for the analog circuits are reasonably relaxed due to this large gain in the signal band and using a feedback architecture. On the other hand, the digital signal processing, which includes the low-pass filtering and decimation, raises the digital circuit complexity. However, as the layout

[2]The key-word *single-bit* emphasizes on the high-linearity requirement for the feedback DAC, but it does not exclude the possibility of implementing highly-linear *multibit* delta-sigma converters.

density has increased and the power consumption of digital circuits has been reduced over time, this requirement is acceptable nowadays.

In conclusion, delta-sigma converters trade signal bandwidth and very fast circuit operations for higher resolution, and trade analog circuit accuracy for digital circuit complexity. Using standard CMOS technology, the achievable performance is mainly limited by device noise, clock jitter, and other unavoidable effects [26]. Hence, these data converters are the state-of-the art.

2.3.3 Single-Bit Quantizer

One should note that if the delta-sigma modulator uses a single-bit quantizer, that is, a simple comparator, in its internal structure, than Bennett's second and third conditions are not fulfilled (Section 2.1.1), namely the resolution of the quantizer is not asymptotically large, but it is only $N = 1$ bit, and, in addition, the step size Δ is not asymptotically small, but it is as large as $\Delta = FSR$. It turns out that the quantization error of a single-bit quantizer cannot be considered mathematically, based on the Bennett's conditions, as an input-independent white noise. Simulation results are presented on Fig. 2.9 for the same full-scale sinewave with a frequency $0.03\ f_S$ as it was considered in Fig. 2.5. It is clear that the quantization error can be hardly considered as an input-independent white noise.

In addition, the gain of a single-bit quantizer is not equal to one, as it was considered correctly for a multibit quantizer. Actually, the gain of a comparator is input-signal dependent, so it is no longer a constant. This can also be intuitively verified in Fig. 2.3.b: for every input $u[n] \geq 0$V, the quantized output $v_a[n] = 1$V, and for every $u[n] < 0$V, the quantized output $v_a[n] = -1$V, so the instantaneous gain $\frac{v_a[n]}{u[n]}$ depends on the input signal $u[n]$ values.

However, we can still define a linearized model for the single-bit delta-sigma converter, assuming a white and uniformly distributed additive noise source model, preceded by a gain stage with a gain factor of k, even for the comparator. Surprisingly, the simulation results generally match well with those predicted by the linearized model. The desire for an analytical model to supplement simulations is, of course, motivated by the design insight such a model provides.

In practice, delta-sigma modulators use one or more cascaded integrators for building the low-pass loop filter $H(z)$. Depending on the order of the loop filter one can find first-, second- or higher-order delta-sigma modulators. In the next sections single-loop low-order delta-sigma ADCs will be analyzed.

2.4 First-Order Delta-Sigma ADCs

The simplest delta-sigma analog-to-digital converter is the first-order one, whose block diagram is presented in Fig. 2.10.a. The loop filter is built from a single integrator, which is usually implemented by a simple delayed switched-capacitor

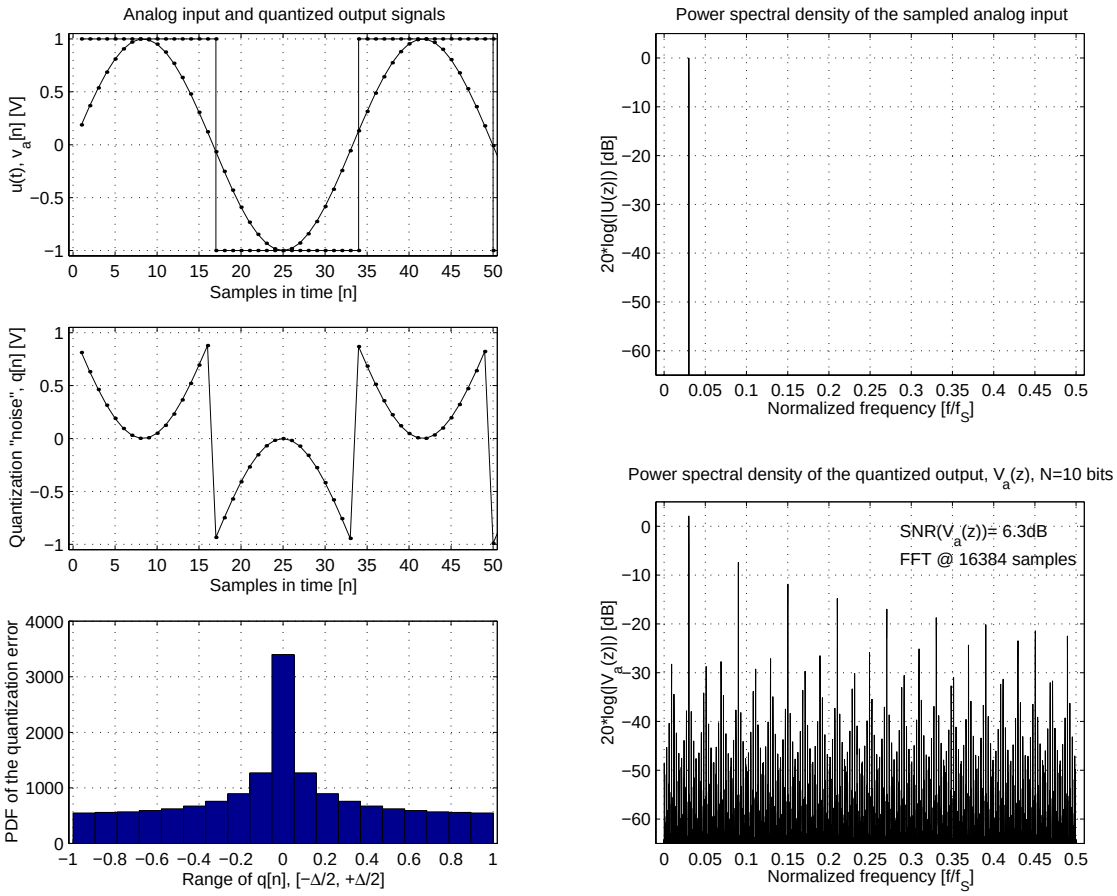

Figure 2.9: The spectrum of a quantized sinewave for N=1 bit

integrator, so

$$H(z) = \frac{z^{-1}}{1 - z^{-1}}. \tag{2.23}$$

2.4.1 Performance Modeling

Based on the linearized model of the first-order delta-sigma modulator presented in Fig. 2.10.b, (2.22) becomes

$$V(z) = z^{-1}\,U(z) + (1 - z^{-1})\,Q(z). \tag{2.24}$$

Hence, the signal transfer function $STF_{1\text{st}}(z)$ and its magnitude are given by

$$STF_{1\text{st}}(z) = z^{-1} \tag{2.25}$$

$$|STF_{1\text{st}}(z)|^2 = |z^{-1}|^2 = 1 \tag{2.26}$$

Also, the noise transfer function $NTF_{1\text{st}}(z)$ and its magnitude are given by

$$NTF_{1\text{st}}(z) = 1 - z^{-1} \tag{2.27}$$

$$|NTF_{1\text{st}}(z)|^2 = |1 - z^{-1}|^2 = \frac{|z-1|^2}{|z|^2} = |z-1|^2 \tag{2.28}$$

$$= \left| \cos \omega T_S - 1 + j \sin \omega T_S \right|^2 \Big|_{f_S=1} \tag{2.29}$$

$$= 4 \sin^2 \frac{\omega}{2} \Big|_{OSR \gg 1} \cong 4 \left(\frac{\omega}{2} \right)^2 = \omega^2 \tag{2.30}$$

So, the magnitude of the noise transfer function for normalized frequency $f_S = \frac{\omega_S}{2\pi} = 1$ and for high oversampling ratios, e.g. $OSR > 8$, which are usual, is simply given by $|NTF_{1\text{st}}(z)| \cong \omega$. Therefore, the in-band quantization noise power is given by

$$P_{0_{1\text{st}}} = \int_0^{\omega_B} |NTF_{1\text{st}}(z)|^2 \, PSD_Q(\omega) \, \mathrm{d}\omega \cong \frac{\sigma_q^2}{\pi} \int_0^{\frac{\pi}{OSR}} \omega^2 \, \mathrm{d}\omega = \frac{\pi^2 \, \sigma_q^2}{3 \, OSR^3} \tag{2.31}$$

Hence, the signal-to-noise ratio $SNR_{1\text{st}}$ can be calculated as

$$SNR_{1\text{st}} = 10 \log_{10} \frac{P_u}{P_{0_{1\text{st}}}} \tag{2.32}$$

$$\cong 20 \log_{10} \frac{A_u}{A_{max}} + 6.02\,N + 30 \log_{10} OSR + 1.76 - 5.17 \quad [\text{dB}].$$

If we consider the oversampling ratio being $OSR = 2^r$, than $30 \log_{10} OSR = 9.03 \, r$ [dB], so every doubling of the oversampling ratio, i.e. for every increment in r, the $SNR_{1\text{st}}$ improves by about 9 dB, or the resolution improves by $1\frac{1}{2}$ bits. In other words, the first-order delta-sigma converter has a 9-dB/octave or 1.5-bit/octave SNR improvement [39, Section 14.2], [37].

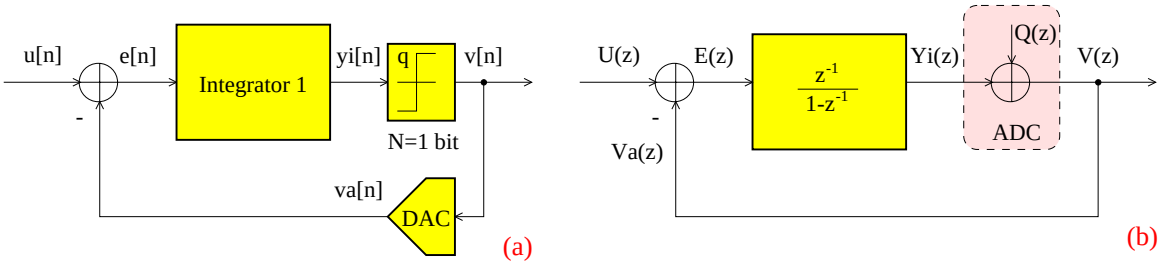

Figure 2.10: (a) First-order delta-sigma ADC and (b) its linearized model

2.4.2 Circuit-Level Implementation

A possible switched-capacitor implementation of the modulator is shown in Fig. 2.11. The analog circuit complexity is clearly quite trivial: it uses 1 switched-capacitor integrator, a single-bit quantizer built from a simple comparator and a D flip-flop, and a single-bit digital-to-analog converter built from 2 reference voltages and 2 switches [17].

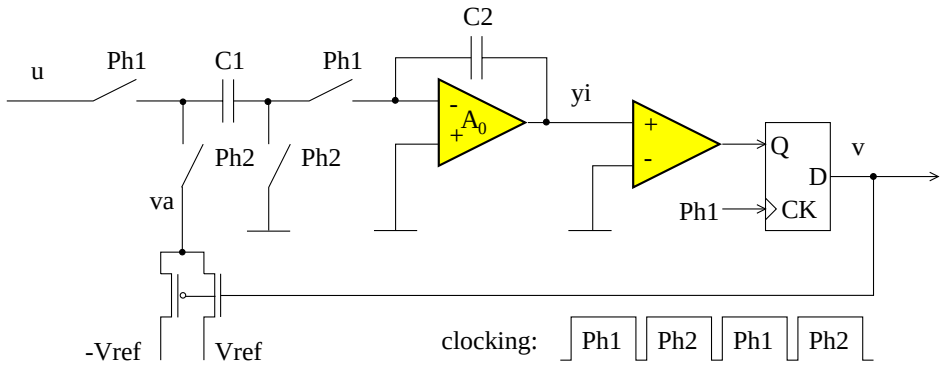

Figure 2.11: Switched-capacitor first-order delta-sigma ADC

2.4.3 Time-Domain Analysis

In order to get a deeper insight into the operation of the delta-sigma modulator, a time-domain analysis is required. The time-domain model of a first-order delta-sigma analog-to-digital converter is presented in Fig. 2.12. Note that this is an exact model and there are no underlying assumptions about the statistical properties of the quantization error. In Fig. 2.12 the single-bit quantizer (comparator) is modeled as a true nonlinear element. Hence, one can write the following difference equations:

$$\begin{cases} y_i[n] &= y_i[n-1] + e[n-1] \\ v[n] &= \begin{cases} 1 & \text{if } y_i[n] \geq 0 \\ -1 & \text{if } y_i[n] < 0 \end{cases} \\ e[n] &= u[n] - v[n] \\ q[n] &= v[n] - y_i[n] \end{cases} \tag{2.33}$$

The exact system-level modeling by using difference equations was used in simulations also, which were performed using Matlab 5.3 and Richard Schreier's Delta-Sigma Toolbox [46][3], [47].

The evolution in time of the modulator's internal and external signals is exemplified in Fig. 2.13, for a half-scale ($A_u = \frac{A_{max}}{2} = \frac{1}{2}$ V) in-band ($f \leq f_B = \frac{f_S}{2OSR}$, $OSR = 32$) sinewave input. The output $v[n]$ is a stream of ± 1 V ('0' logic and '1' logic). By averaging this output over a period of time, one can approximate the input sinewave. This averaging operation represents the low-pass filter block in Fig. 2.8.a, since averaging is a crude low-pass filtering operation [37].

2.4.4 Performance Limitations

Although the first-order delta-sigma modulator is extremely simple to implement, it requires very high OSR in order to achieve high resolution, e.g. the OSR should

[3]The scaling between the digital single-bit output $v[n]$ and its analog counterpart $v_a[n]$, was neglected for simplification, so $v[n] = v_a[n]$ is considered in the time-domain analysis.

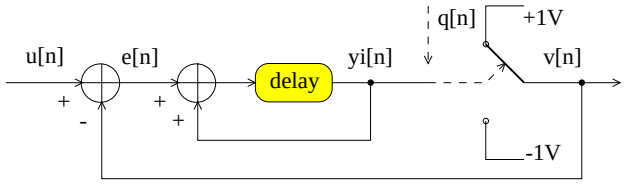

Figure 2.12: Time-domain model of the first-order delta-sigma ADC

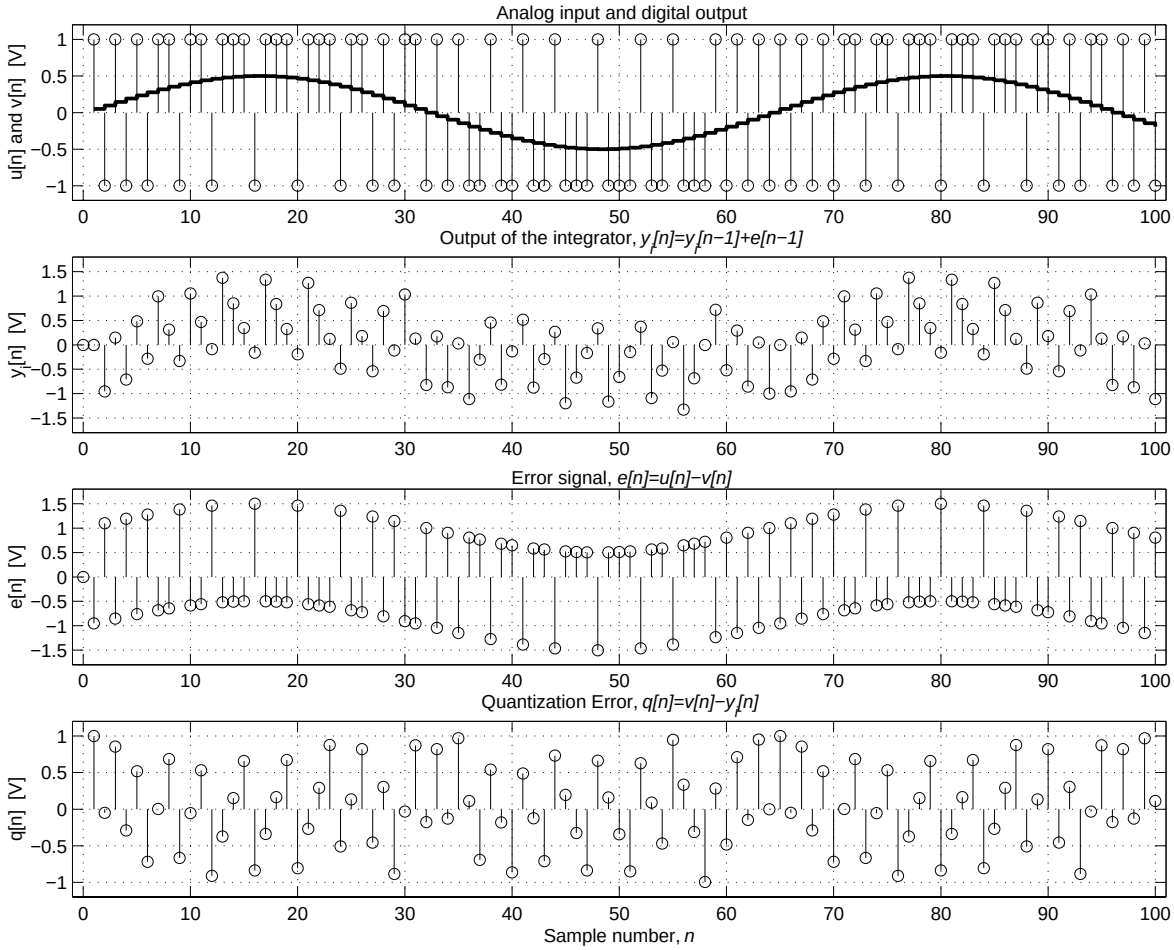

Figure 2.13: First-order delta-sigma ADC response in time to a half-scale in-band sinewave input ($OSR = 32$)

be over 1000 for 16-bit accuracy. In addition, in the first-order delta-sigma modulator's output periodic (tone) components could be present, which make it unusable for several applications, such as digital audio.

2.5 Second-Order Delta-Sigma ADCs

A more practical converter can be implemented by using a second-order delta-sigma converter, which uses 2 cascaded integrators in the forward path (Fig. 2.14). In addition, 2 feedback paths are necessary, because otherwise the modulator would be unstable. The coefficients a_1, a_2, b_1 and b_2 allow to scale the internal input and output signals of the integrators and, also, to realize a convenient signal and noise transfer function for the modulator. The second-order delta-sigma converter is less affected by idle tones and pattern noise, and its signal-to-noise ratio performance is good enough for a wide range of applications, hence it will be studied in more detail in this section.

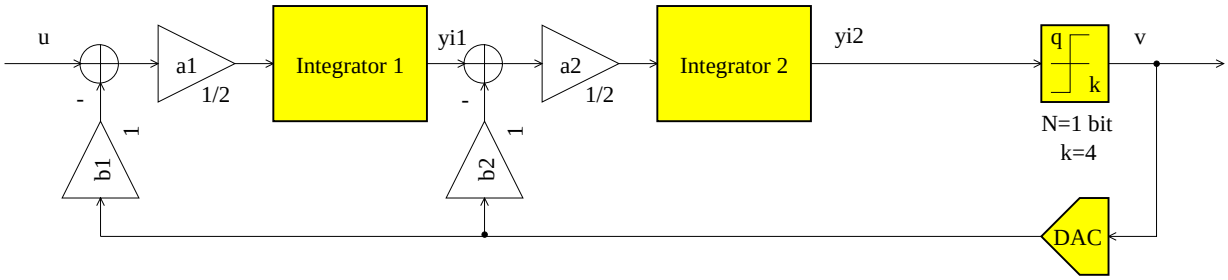

Figure 2.14: Second-order single-bit delta-sigma ADC

2.5.1 Performance Modeling

Before calculating the expected SNR performance, one should note that our delta-sigma modulators use a single-bit quantizer, that is, a simple comparator, in its internal structure. However, we still define a linearized model for the second-order modulator, assuming a white and uniformly distributed additive noise source for the comparator, preceded by a gain stage with a gain factor of k (Fig. 2.15) [48]. Therefore, the output of the modulator based on the linearized model is given by

$$\begin{aligned} V(z) &= k\,Y_{i2}(z) + Q(z) \qquad (2.34)\\ &= k\,a_2\,\frac{z^{-1}}{1-z^{-1}}\left(-b_2\,V(z) + a_1\,\frac{z^{-1}}{1-z^{-1}}(-b_1 V(z) + U(z))\right) + Q(z) \end{aligned}$$

$$\Longrightarrow V(z) = \frac{a_1 a_2 k z^{-2}\,U(z) + (1-z^{-1})^2\,Q(z)}{1 + (a_2 b_2 k - 2)z^{-1} + (1 - a_2 b_2 k + a_1 a_2 b_1 k)z^{-2}} \qquad (2.35)$$

To achieve the desired transfer function for the second-order modulator, namely

$$V(z) = z^{-2}\,U(z) + (1-z^{-1})^2\,Q(z), \qquad (2.36)$$

the gain factors should satisfy:

$$\begin{cases} 1 - a_2\, b_2\, k + a_1\, a_2\, b_1\, k &= 0 \\ a_2\, b_2\, k - 2 &= 0 \\ a_1\, a_2\, k &= 1 \end{cases} \tag{2.37}$$

In conclusion, solving (2.37), one can derive the following relations between the coefficients of the second-order delta-sigma analog-to-digital converter:

$$\begin{cases} k &= \frac{1}{a_1\, a_2\, b_1} \\ b_2 &= 2\, a_1\, b_1 \\ b_1 &= 1 \end{cases} \tag{2.38}$$

Note that $a_1\, a_2\, k = 1$ and hence $b_1 = 1$ in (2.37) and (2.38) respectively, are sufficient but not necessary conditions (details in Section 2.5.6).

Also note that the gain of the single-bit quantizer in the linearized model is considered an input-signal independent constant given by $k = \frac{1}{a_1 a_2 b_1}$, based on the assumption that the product of the loop-gain factors of the modulator are forced to be 1 by the feedback loop [48]. In other words, the delta-sigma loop acts as an automated gain control system over most of the input range (e.g. $A_u = -120 \ldots -10$ dB) maintaining the product of the loop-gain factors at unity [38, Section 6.2.2], so the condition $k = \frac{1}{a_1 a_2 b_1}$ to achieve the desired transfer function is fulfilled for any coefficient values. Its only justification is that the analytical results subsequently obtained compare well with computer simulations that model the true quantization function [48].

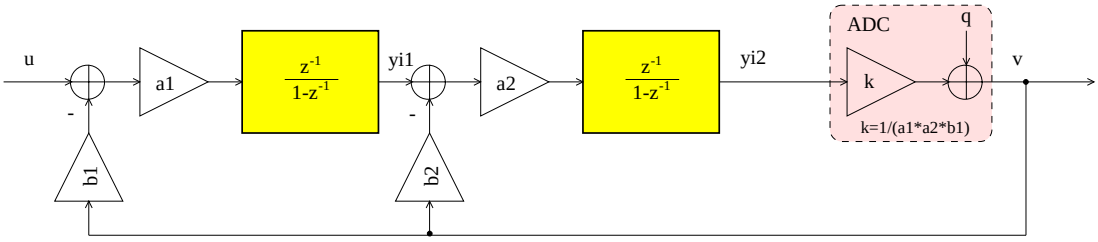

Figure 2.15: Linearized model of the second-order delta-sigma ADC

Choosing appropriate coefficients for the modulator (a_1, a_2, b_1 and b_2), is not trivial, and it needs a careful analysis. Following the objective to find the combination of coefficients that provides second-order noise shaping: $NTF_{2\mathrm{nd}}(z) = (1 - z^{-1})^2$, and ensures the maximum dynamic range, it was found that $a_1 = \frac{1}{2}$, $a_2 = \frac{1}{2}$, $b_1 = 1$ and $b_2 = 1$ are the optimal values for the second-order single-bit delta-sigma modulator [49]. (An earlier paper proposes the same coefficient values [50].)

For the coefficients chosen above, the linearized model indicates the desired transfer function (2.36), which contains a unity-gain signal transfer function

$$STF_{2\mathrm{nd}}(z) = z^{-2} \tag{2.39}$$

$$|STF_{2\mathrm{nd}}(z)|^2 = |z^{-2}|^2 = 1, \tag{2.40}$$

and second-order quantization noise shaping with

$$NTF_{2\mathrm{nd}}(z) = (1 - z^{-1})^2. \tag{2.41}$$

The frequency response and the z-plane representation of this noise transfer function are presented in Fig. 2.16. It can be observed that the quantization noise is filtered ("shaped") by a second-order high-pass filter, by which the low-frequency in-band quantization noise is considerably reduced. The magnitude of the noise transfer function $NTF_{2\mathrm{nd}}(z)$ can be calculated as follows

$$\begin{aligned} |NTF_{2\mathrm{nd}}(z)|^2 &= |(1 - z^{-1})^2|^2 = \frac{|z-1|^4}{|z|^4} && (2.42)\\ &= |\cos\omega T_S - 1 + j\sin\omega T_S|^4 \Big|_{f_S=1} && (2.43)\\ &= 2\,(3 - 4\cos\omega + \cos 2\omega) && (2.44) \end{aligned}$$

Therefore, the in-band quantization noise power is given by

$$\begin{aligned} P_{0_{2\mathrm{nd}}} &= \int_0^{\omega_B} |NTF_{2\mathrm{nd}}(z)|^2\, PSD_Q(\omega)\,\mathrm{d}\omega && (2.45)\\ &= \frac{2\,\sigma_q^2}{\pi}\int_0^{\frac{\pi}{OSR}} (3 - 4\cos\omega + \cos 2\omega)\,\mathrm{d}\omega && (2.46)\\ &= \frac{2\,\sigma_q^2}{\pi}\left(\frac{3\,\pi}{OSR} - 4\sin\frac{\pi}{OSR} + \frac{1}{2}\sin\frac{2\,\pi}{OSR}\right) && (2.47) \end{aligned}$$

Note that by using the approximation $|1 - z^{-1}| \cong \omega$, (2.30), for "high" oversampling ratios (2.47) becomes

$$P_{0_{2\mathrm{nd}}} \cong \frac{\pi^4\,\sigma_q^2}{5\,OSR^5} \tag{2.48}$$

Therefore, the signal-to-noise ratio $SNR_{2\mathrm{nd}}$ is given by

$$\begin{aligned} SNR_{2\mathrm{nd}} &= 10\log_{10}\frac{P_u}{P_{0_{2\mathrm{nd}}}} && (2.49)\\ &\cong 20\,\log_{10}\frac{A_u}{A_{max}} + 6.02\,N + 50\,\log_{10} OSR + 1.76 - 12.9 \quad [\mathrm{dB}] \end{aligned}$$

If we consider the oversampling ratio being $OSR = 2^r$, than $50\log_{10} OSR = 15.05\,r$ [dB], so every doubling of the oversampling ratio, i.e. for every increment in r, the $SNR_{2\mathrm{nd}}$ improves by about 15 dB, or the resolution improves by $2\frac{1}{2}$ bits. In other words, the second-order delta-sigma converter has a 15-dB/octave or 2.5-bit/octave SNR improvement [39, Section 14.2], [37].

Because the simplified relation (2.48) is widely used, it is interesting to compare it with its exact[4] version (2.47) for different oversampling ratios. Based on simulation results presented in Fig. 2.17, $\Delta SNR_{2\mathrm{nd}}|_{OSR=4} = 0.3$ dB and $\Delta SNR_{2\mathrm{nd}}|_{OSR=8} < 0.1$ dB (0.2%), so the relation (2.48) provides a good approximation especially for $OSR \geq 8$.

[4]The relation (2.47) was obtained by *exact* calculation of the integral from (2.45). However, (2.45) itself was based on the input-independent additive white-noise approximation (Section 2.1.1), so (2.45) is *not exact* in a broad sense.

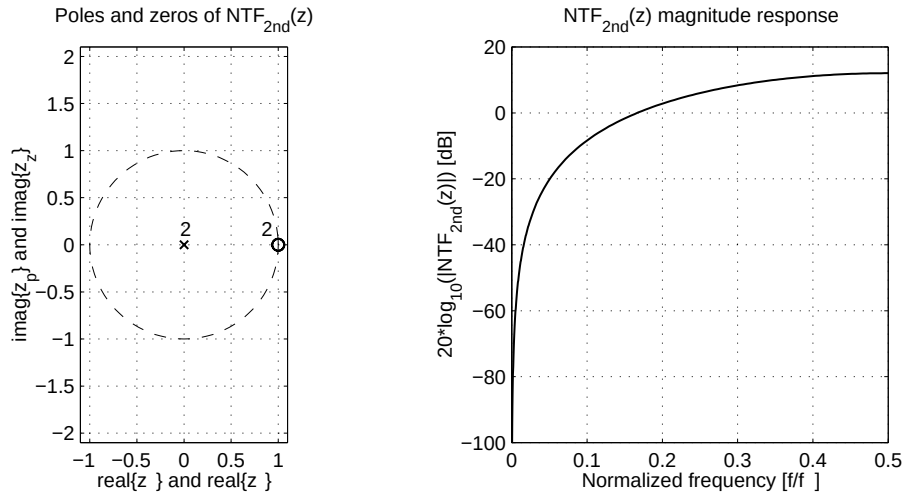

Figure 2.16: Noise transfer function of the second-order delta-sigma ADC

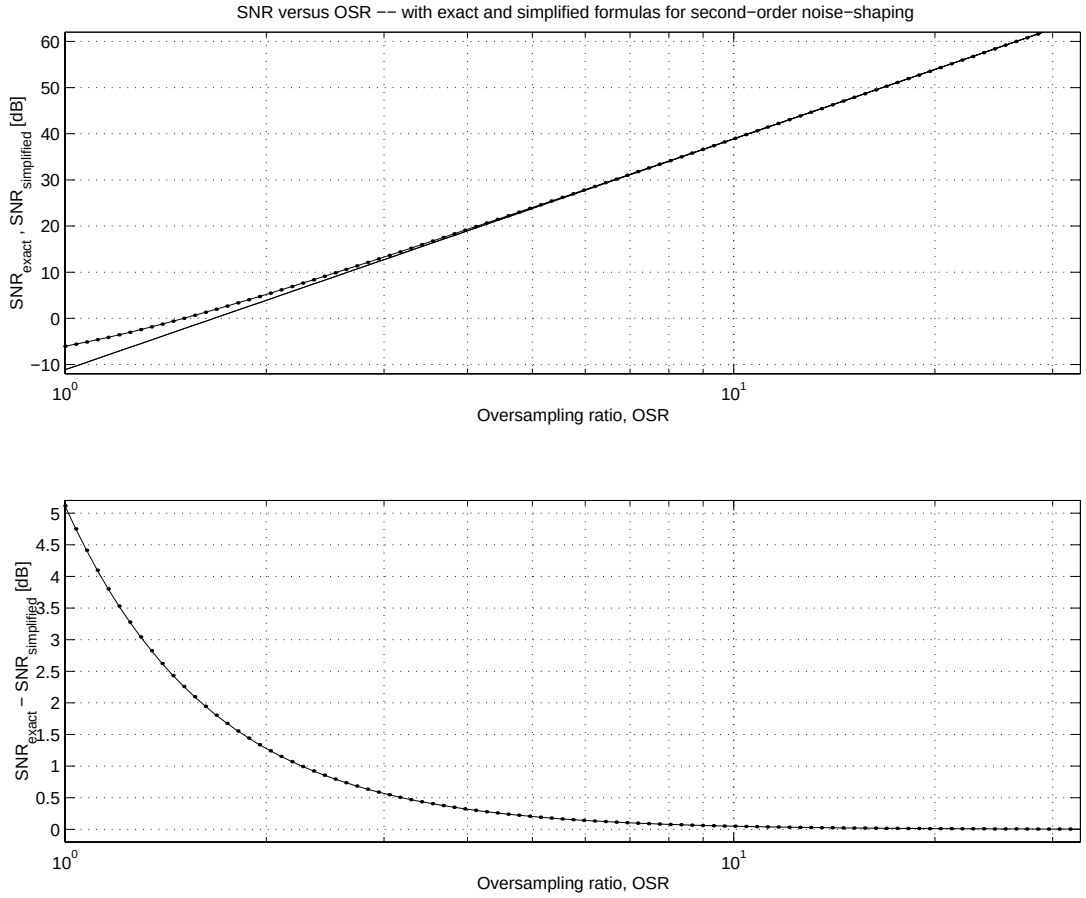

Figure 2.17: Signal-to-noise ratio SNR versus oversampling ratio OSR

2.5.2 Performance Criteria

In order to characterize the performance of the modulators, some performance criteria are usually defined:

Signal-to-noise ratio (SNR), which is defined for a nonoverloading sinusoidal input signal amplitude as the ratio of the output signal power to the uncorrelated in-band noise, used to observe the performance degradation due to linear effects only [49]; the SNR accounts only for uncorrelated noise and not harmonic distortion [50];

Maximum signal-to-noise ratio (SNR_{max} or SNR_{peak} or SM), which is defined as the biggest SNR achievable with the topology; this way, the performance degradation due to nonlinear overload effects can be observed [49];

Overload level (OL), which is defined as the maximum input signal amplitude for which the structure still operates correctly; it is considered that the structure still operates well for amplitudes such that the SNR degrades no more than 6 dB[5] from the SNR_{peak} value [49];

Dynamic range (DR)[6], which is defined as the ratio of the rms value of the maximum amplitude input sinusoidal signal, for which the structure still operates correctly, to the rms value of that small input sinusoidal signal for which the SNR is unity (SNR=0 dB) [39, Section 11.5], [37]; it is considered that the structure still operates well for amplitudes such that the SNR degrades no more than 6 dB from the SNR_{peak} value [49];

Signal-to-(noise-and-distortion) ratio ($SNDR$ or $TSNR$), which is defined as the ratio of the output signal power to the total in-band noise; the $SNDR$ takes into account the effects of harmonic distortion also [50].

2.5.3 Circuit-Level Implementation

Since delta-sigma modulators are usually sampled-data (discrete-time) systems, they are readily implemented in CMOS technology with switched-capacitor circuits. A possible topology is presented in Fig. 2.18 [50]. A fully-differential configuration has been adopted in order to ensure high power supply rejection, reduced clock feedthrough and switched charge injection errors, improved linearity, and increased dynamic range. The two integrators each consist of an amplifier, two sampling capacitors C_1, and two integrating capacitors C_2. The ratio of C_1 to C_2 is chosen so as to realize the gains $a_1 = a_2 = \frac{1}{2}$ that precedes each integrator in the architecture presented in Fig. 2.14. Note that the coefficients a_1

[5] In this thesis we used this definition for the overload level according to [49], but one might consider a 3-dB SNR degradation a more suitable value.

[6] Note that in [50] the dynamic range is defined for sinusoidal inputs as the ratio of the *output* power at the frequency of the input sinusoid for a full-scale input to the *output* signal power for a small sinusoidal input for which the $TSNR$ is unity.

and a_2 are equal, and b_1 and b_2 are equal to 1 in this particular switched-capacitor implementation.

The operation of the modulator is controlled by a nonoverlapping 2-phase clock. During $Phase$-1 all of the switches labeled S_1 and S_3 are open, while those labeled S_2 and S_4 are closed, and the input to each integrator is sampled onto the capacitors C_1. In $Phase$-2, switches S_1 and S_3 open, while S_2 and S_4 close, and charge stored on C_1 is transferred to C_2. During this phase, the closing of switches S_2 has the effect of subtracting the output of the bi-level D/A network from the input to each integrator. The comparison of the outputs from the second integrator is performed during $Phase$-1, and the comparator reset during $Phase$-2. With this clocking arrangement, the time available for the integration and the time for the comparison are both one-half a clock cycle [50].

More advanced circuit-level design issues and simulation results are presented in Chapter 5.

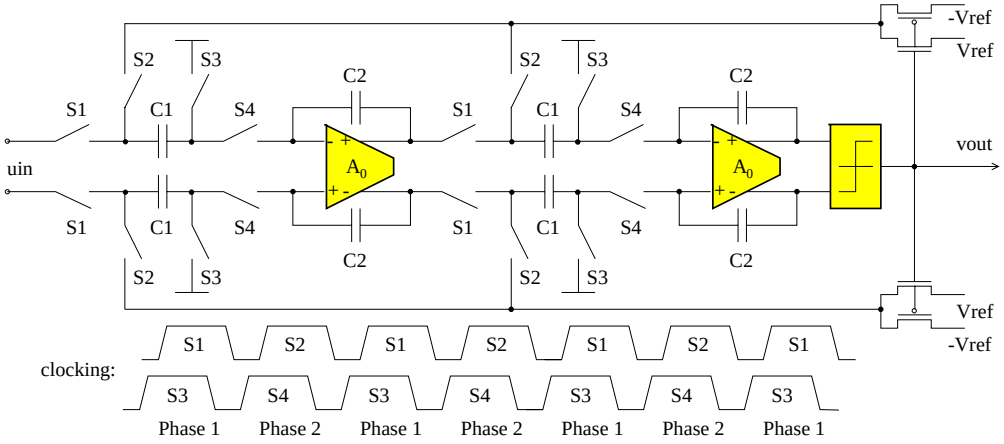

Figure 2.18: Switched-capacitor second-order delta-sigma ADC

2.5.4 Time-Domain Analysis

The linearized model is based on some weakly-verified assumptions, so there is a need to derive the exact model and to verify the second-order modulator's behavior using extensive simulations.

The time-domain model of a second-order delta-sigma analog-to-digital converter is presented in Fig. 2.19. Note that this is an exact model and there are no underlying assumptions about the statistical properties of the quantization error. In Fig. 2.19 the single-bit quantizer (comparator) is modeled as a true nonlinear

element. Hence, one can write the following difference equations:

$$\begin{cases} y_{i1}[n] &= y_{i1}[n-1] + a_1\, e_1[n-1] \\ y_{i2}[n] &= y_{i2}[n-1] + a_2\, e_2[n-1] \\ v[n] &= \begin{cases} 1 & \text{if } y_{i2}[n] \geq 0 \\ -1 & \text{if } y_{i2}[n] < 0 \end{cases} \\ e_1[n] &= u[n] - b_1\, v[n] \\ e_2[n] &= y_{i2}[n] - b_2\, v[n] \\ q[n] &= v[n] - y_{i2}[n] \end{cases} \tag{2.50}$$

Obviously, one must take care of the initial conditions, i.e. the integrators output signals at n=0 time instance also, which usually are all set to zero at power up, because the capacitors are discharged: $y_{i1}[0] = 0$, $y_{i2}[0] = 0$, $e_1[0] = 0$ and $e_2[0] = 0$.

The evolution in time of the modulator's internal and external signals are exemplified in Fig. 2.20, for the same conditions as in Fig. 2.13: half-scale ($A_u = \frac{A_{max}}{2} = \frac{1}{2}$ V) in-band ($f \leq f_B = \frac{f_S}{2OSR}$, $OSR = 32$) sinewave input and for $a_1 = \frac{1}{2}$, $a_2 = \frac{1}{2}$, $b_1 = 1$ and $b_2 = 1$. If one compares the output $v[n]$ from Fig. 2.20 with $v[n]$ from Fig. 2.13, the key point is that the distribution of '1'-s and '-1'-s in the second-order modulator's output is such their average provides a more accurate representation of the input than the corresponding average of the first-order modulator's output. In other words, for a given block of output samples, the second-order modulator uses its allocation of samples more efficiently to represent the input [37].

2.5.5 Linearized Model Limitations

The performance of the specified second-order modulator is usually evaluated using the signal-to-noise ratio SNR versus the amplitude of the input sinewave A_u [50]. Both simulation and theoretical calculation results are presented in Fig. 2.21. The modulator was simulated at system level, described by its difference equations (2.50), and the quantizer was modeled by an ideal single-bit comparator, that is, a nonlinear element.

In addition, the $SNR_{2\text{nd}}$, (2.49), predicted by the linearized model (Fig. 2.15) matched the simulation results to within a few dB-s (Fig. 2.21). However, when the input signal approaches its full-scale range, the simulated SNR drops. One weakness of the linearized model is that it does not account for this phenomena. Beyond this, most of the difference between the linearized model and the simulation is a consequence of the spectral content of the quantization noise $Q(z)$, that is, the quantization noise is not input signal independent, it is not white and uniformly distributed [37], [48] as it was assumed for the linearized model.

The SNR drop due to the large input signals can be viewed as a stability issue of the modulator, that is, for large input signals the second-order delta-sigma loop becomes unstable. By "unstable" we mean that the modulator exhibits large, although not necessarily unbounded, states and a poor SNR compared with that predicted by its linearized model [38, Section 4.1], [51]. If the last integrator's

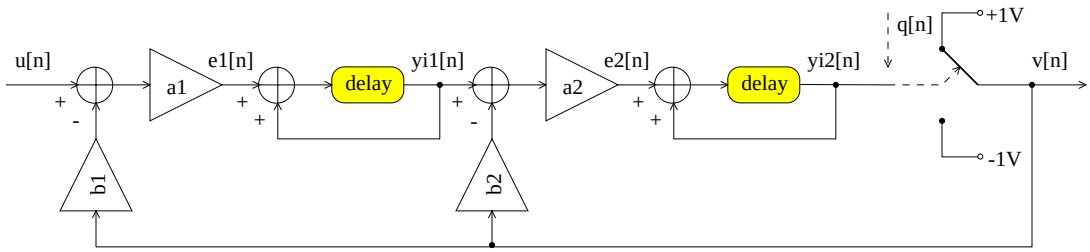

Figure 2.19: Time-domain model of the second-order delta-sigma ADC

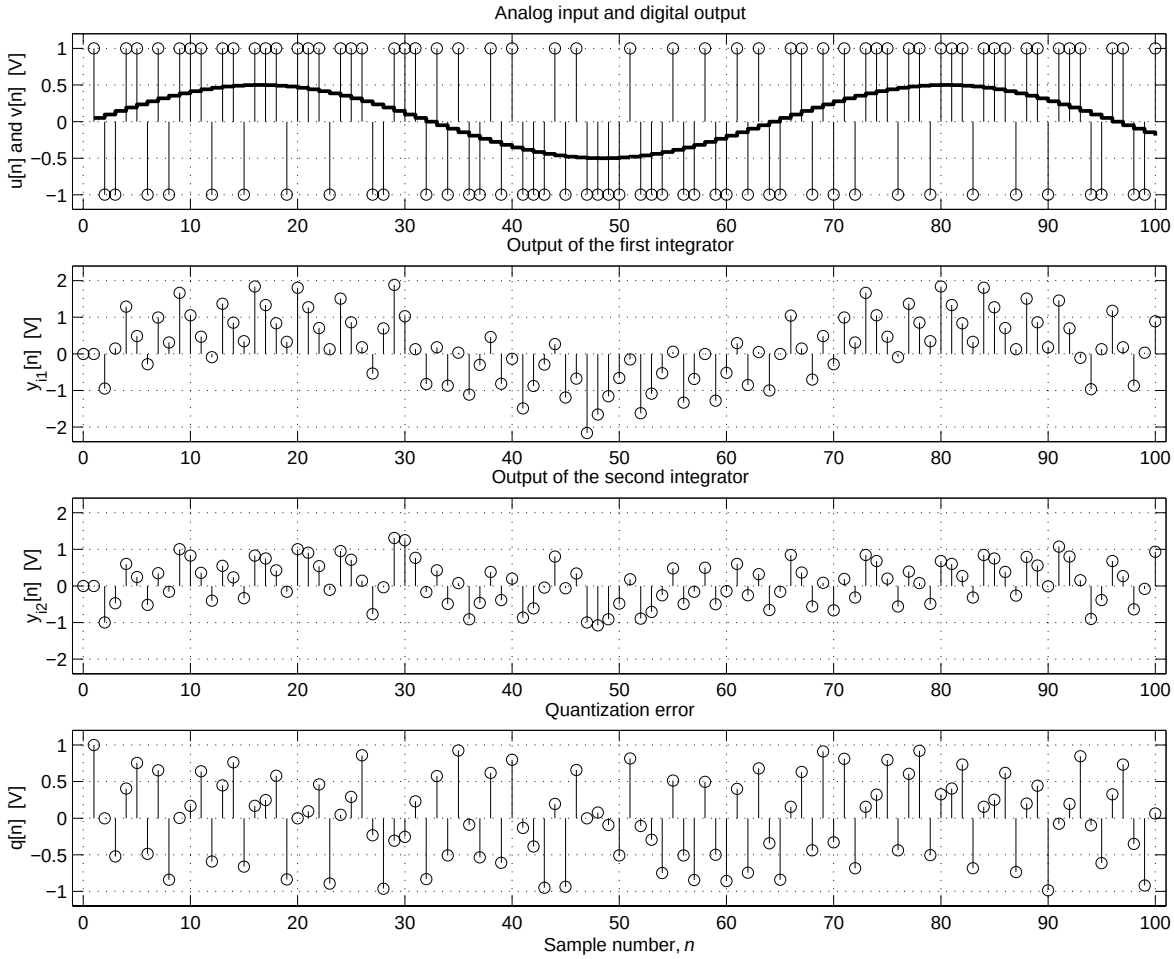

Figure 2.20: Second-order delta-sigma ADC response in time to a half-scale in-band sinewave input ($a_1 = \frac{1}{2}$, $a_2 = \frac{1}{2}$, $b_1 = 1$, $b_2 = 1$)

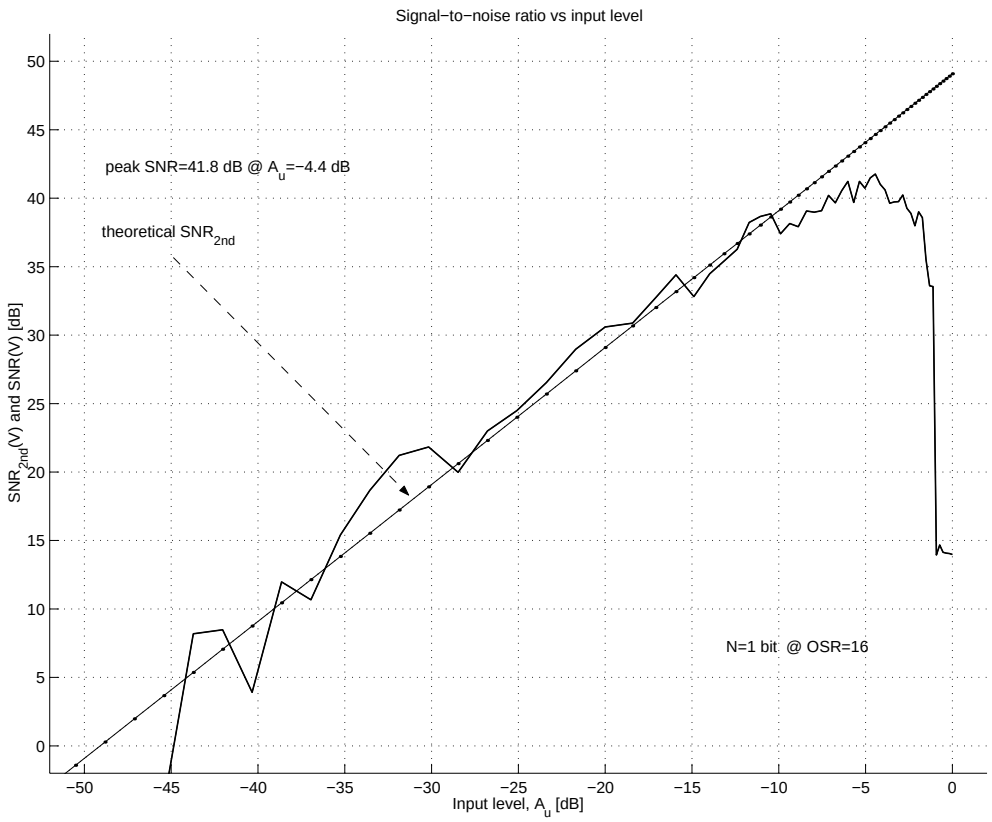

Figure 2.21: Performance of the second-order single-bit delta-sigma ADC

output signal becomes larger than what the quantizer can normally handle, the quantizer overloads, and therefore the quantization error becomes larger than $\pm\frac{\Delta}{2}$, which causes the SNR performance to drop. In addition, at larger internal signals than what the opamps from the integrators can handle, the opamps' outputs will saturate, so the modulator looses signal information and its performance drops.

Exactly when (for which A_u value) does this SNR drop occur? What are the stability criteria for a delta-sigma modulator? The exact stability analysis of a nonlinear system, e.g. a delta-sigma loop, is a difficult task. The delta-sigma design community is still awaiting an effective and general method for proving the stability of an arbitrary high-order modulator with an arbitrary input [51]. In the present work only a simplified analysis is presented, but which gives a good insight into the problem itself.

Let us define a more realistic, input-signal dependent gain k_S for the quantizer, by the ratio of the root-mean-square (rms) value of its quantized output and analog input:

$$k_S = \frac{\text{rms}(v_a)}{\text{rms}(y_{i2})} = \lim_{N\to\infty} \sqrt{\frac{\sum_{n=1}^{N} v_a^2[n]}{\sum_{n=1}^{N} y_{i2}^2[n]}} \tag{2.51}$$

Note that this definition of the quantizer gain is meaningful only, if the reference voltages of the feedback DAC are taken into account also, that is, considering the ratio between $\text{rms}(v_a)$ and $\text{rms}(y_{i2})$, and not between $\text{rms}(v)$ and $\text{rms}(y_{i2})$.

Using the linearized model (Fig. 2.15) with this simulated gain k_S, one can derive the noise transfer function $NTF(z)$ of the modulator from (2.34). The locations of the $NTF(z)$ poles determine the stability of the loop. Simulation results are presented in Fig. 2.22. It can be easily observed that at large input signals ($A_u > 0.1$ V) the simulated gain k_S gradually decreases and suddenly drops. In addition, the SNR values are highly correlated with the simulated gain values and the SNR drop occurs when the simulated gain becomes smaller than a certain value, e.g. $\frac{1}{2}$. For such an input signal amplitude the poles of the $NTF(z)$ are only barely inside of the unit circle, what can generate unstable operation. Note however that the whole concept of noise transfer function is only an approximation which lies on very weakly verified conditions, especially for a single-bit internal quantizer, so the above presented method should be used carefully. On the other hand, there is no doubt about its utility as far as its results match well with the reality, even if the underlying mathematics does not validate the method itself.

In conclusion, the variability of the simulated gain k_S of the quantizer can be viewed as being a cause of instability of delta-sigma modulators [38, Section 4.2.1]. Note that the NTF's root locus method used above, is a powerful and a relatively simple tool for analyzing the stability of higher-order modulators beyond extensive simulations [38, Section 4.2.2].

2.5.6 Non-Unity-Gain Signal Transfer Function

So far, the desired signal transfer functions $STF(z)$ of the delta-sigma modulators (e.g. (2.20), (2.25), (2.39)) were considered with unity gain at low frequencies [50]. The same underlying assumption gave the relation $a_1\, a_2\, k = 1$ in (2.37), which forced $b_1 = 1$ in (2.38). However, if the signal transfer function could amplify the input signal while maintaining the same quantization noise power, than the signal-to-noise ratio SNR of the whole system would increase as well.

A signal transfer function with a low-frequency gain of 2 can be achieved by choosing different coefficients than those proposed in [50], e.g. $a_1 = 1$, $a_2 = 1$, $b_1 = \frac{1}{2}$, $b_2 = 1$ [52]. Similarly, a gain of 4 results for $a_1 = 1$, $a_2 = 1$, $b_1 = \frac{1}{4}$, $b_2 = \frac{1}{2}$. However, simulation results (Fig. 2.23) show very close peak-SNR values for these three different configurations. Although $|STF(z)| = 2$ (Fig. 2.23.b) and $|STF(z)| = 4$ (Fig. 2.23.c) amplify the signal and improves the SNR accordingly, the quantizer overloads at very similar peak-SNR values.

In conclusion, there is no significant benefits of using non-unity DC-gain signal transfer functions [53]. Therefore, (2.38) was correctly derived and we will design the delta-sigma ADCs accordingly.

2.5.7 Tri-Level Quantizer

It can be observed from (2.49) that the SNR of the second-order delta-sigma modulator can be increased by increasing the number of bits N of the quantizer. However, the nonlinearity errors of a multibit DAC in the feedback loop would destroy this performance gain, if advanced techniques, such mismatch shaping

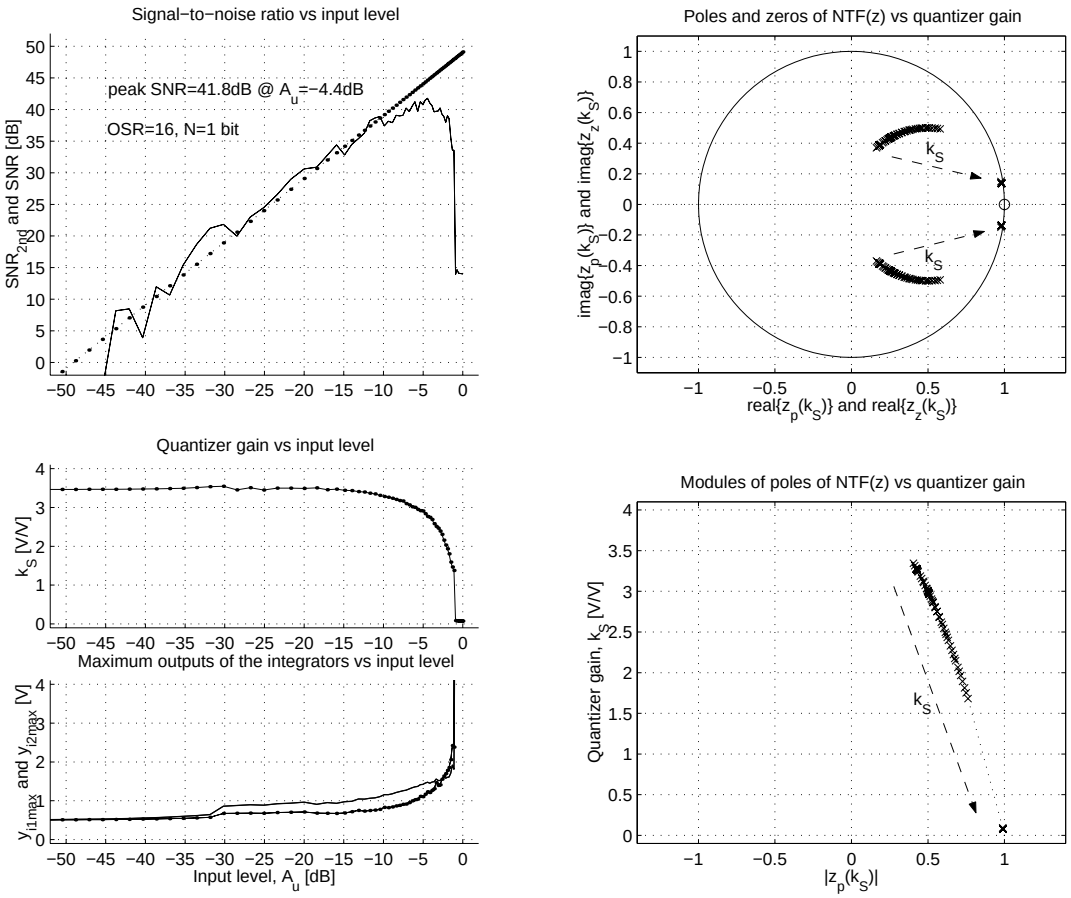

Figure 2.22: Stability analysis of the second-order delta-sigma ADC ($a_1 = \frac{1}{2}$, $a_2 = \frac{1}{2}$, $b_1 = 1$, $b_2 = 1$ and $k = 4$)

or other correction methods (details in Section 2.3.1) did not take care of this introduced nonlinearity.

The simplest multibit quantizer is the tri-level quantizer, proposed in [54]. This tri-level quantizer offers a good trade-off between SNR performance and circuit complexity, especially if one wants to avoid a multibit mismatch-shaping DAC [38, Section 8.3.3] in order to reduce the chip area. The linearity of the tri-level feedback DAC is still critical, but a highly-accurate tri-level DAC was recently described [55] which used extra switches and simple circuitry to insure linearity.

Choosing appropriate coefficients for this modified delta-sigma modulator will be presented next. The objectives of the design are: to provide a second-order noise shaping by an $NTF_{2\mathrm{nd}}(z) = (1 - z^{-1})^2$, while the output signals of the integrators $y_{i1}[n]$ and $y_{i2}[n]$ remain bounded to avoid the saturation of the opamps and of the quantizer even for reasonably large input signal amplitudes. In other words, the coefficients of the modulator should provide the most aggressive noise suppression (in this specific case) and should also maximize the dynamic range.

A good starting point in this design is to draw the linearized model of the

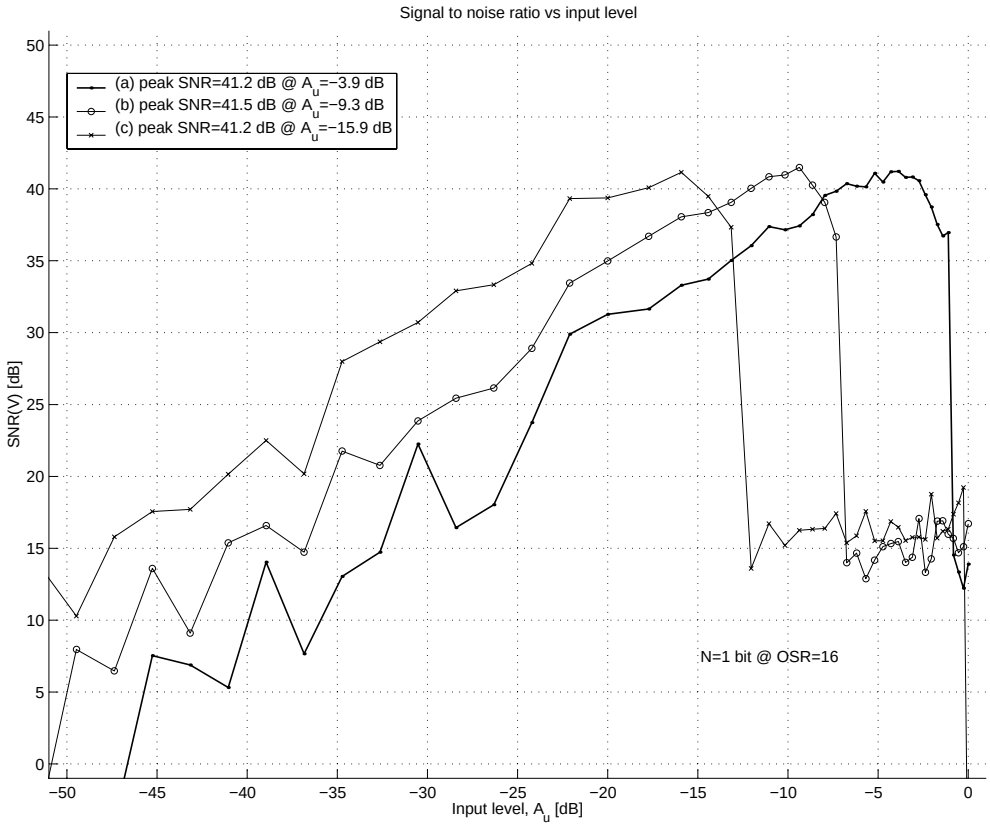

Figure 2.23: SNR performance of second-order single-bit delta-sigma ADCs for (a) $|STF(z)| = 1$, $a_1 = \frac{1}{2}$, $a_2 = \frac{1}{2}$, $b_1 = 1$, $b_2 = 1$ [50], (b) $|STF(z)| = 2$, $a_1 = 1$, $a_2 = 1$, $b_1 = \frac{1}{2}$, $b_2 = 1$ [52], (c) $|STF(z)| = 4$, $a_1 = 1$, $a_2 = 1$, $b_1 = \frac{1}{4}$, $b_2 = \frac{1}{4}$.

modulator (Fig. 2.15) and to follow (2.38). However, the gain of the tri-level quantizer is not controlled by the negative feedback loop, and the product of the loop-gain factors cannot be forced to be unity — as it was the case of a bi-level quantizer —, but the gain of the tri-level quantizer is given by the placement of its 2 threshold voltages. So, the gain k is independent of the coefficients, and in order to obtain $NTF_{2\mathrm{nd}}(z) = (1 - z^{-1})^2$, this gain k should match with $\frac{1}{a_1 a_2 b_1}$. If one chooses the threshold voltages at $\{-0.5; +0.5\}$ V while the reference voltages of the tri-level DAC are $\{-1.0; 0; +1.0\}$ V, than the gain of the quantizer will be $k = 1$ (Fig. 2.25). In conclusion, if $k = 1$, the simplest architecture, which provides the desired $NTF(z)$, (2.38), would have $a_1 = 1$, $a_2 = 1$, $b_1 = 1$ and $b_2 = 2$. Simulation results are presented in Fig. 2.25, where a bi-level (Fig. 2.14) and a tri-level (Fig. 2.24) second-order delta-sigma modulators were compared. The simulated SNR curves show the expected 6-dB improvement.

However, for this configuration the signal swings at the outputs of the two integrators are too wide (Fig. 2.27):

$$y_{i1_{max}}[n]|_{A_u=-1.4\mathrm{dB}} = 2.55\mathrm{V} \text{ and } y_{i2_{max}}[n]|_{A_u=-1.4\mathrm{dB}} = 3.31\mathrm{V}$$

for $B_S = 2^{14}$ samples. To constrain these voltage swings to $[-1; +1]$ V, which can

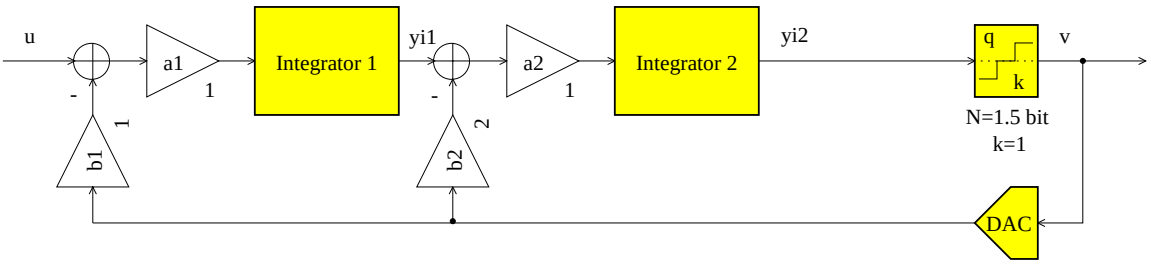

Figure 2.24: Second-order tri-level delta-sigma ADC

be handled by the opamps and the tri-level quantizer, node-voltage scaling should be applied to the modulator. It turns out that $a_1 = \frac{1}{4}$, $a_2 = \frac{1}{2}$, $b_1 = 1$, $b_2 = \frac{1}{2}$ and $k = 8$ provides the same SNR performance, that is, the same $NTF(z)$, but the internal signal swings are well bounded in $[-1; +1]$ V even for large input signals (Fig. 2.28). Apparently, the signals are scaled down too drastically, but we do need additional room for a dither signal, called "test" signal in Chapter 4, which will be injected before the quantizer. Note, that $k = 8$ was obtained by placing the threshold voltages at $\{-0.125; +0.125\}$ V. The simulated gain was also $k_S \approx 8$ for $A_u = -30 \ldots -10$ dB.

Finally, it is interesting to analyze the SNR curve for a second-order modulator which uses a multibit quantizer in a "balanced" ($k = \frac{1}{a_1 a_2 b_1}$) and in an "unbalanced" ($k \neq \frac{1}{a_1 a_2 b_1}$) configuration. In Fig. 2.26 some simulation results are presented for a multibit quantizer with 100 levels ($N \cong 6.64$ bits, midriser quantizer [37]) and different coefficients which satisfy $b_2 = 2a_1 b_1$ and $b_1 = 1$, but $k = \frac{1}{a_1 a_2 b_1}$ is satisfied only in one case. The theoretical $SNR_{2\text{nd}}$, calculated according to (2.49), is also plotted on the same figure. It can be observed that if the modulator is balanced, than the simulation results closely approximate the theoretical $SNR_{2\text{nd}}$ curve. If the modulator is unbalanced, than there is a significant performance drop around $A_u = -40$ dB. However, in both cases, for input signals smaller than about $A_u = -40$ dB, the theoretical and the simulated performances run together, so the unbalanced modulator behaved similarly with the balanced one. So, what happened at about $A_u = -40$ dB?

If one analyzes the transfer function of a multi-level quantizer (Fig. 2.3) with even number of quantization levels, it can be observed that the multilevel quantizer behaves as a bi-level quantizer for small inputs, that is, for $|u[n]| < \Delta$. So, if the input signal range of the multibit quantizer in the second-order delta-sigma modulator remains bounded $|y_{i2}[n]| < \Delta$, than the multibit delta-sigma modulator will behave as a bi-level delta-sigma modulator, and it turns out that the gain of the quantizer will not be anymore $k = 1$, but it will be forced by the feedback loop to satisfy $k = \frac{1}{a_1 a_2 b_1}$ (However, in particular for Fig. 2.26.a it will be still 1!). Simulations validated that this happens for input signals of $A_u = -42.3$ dB if 100 quantization levels are used. Obviously, for an odd number of quantization levels (midtread quantizer [37]) this will never happen.

In addition, if $A_u > -40$ dB, the output of the multibit quantizer will be truly multibit word-sequence, so its gain becomes $k = 1$, and, therefore, its noise trans-

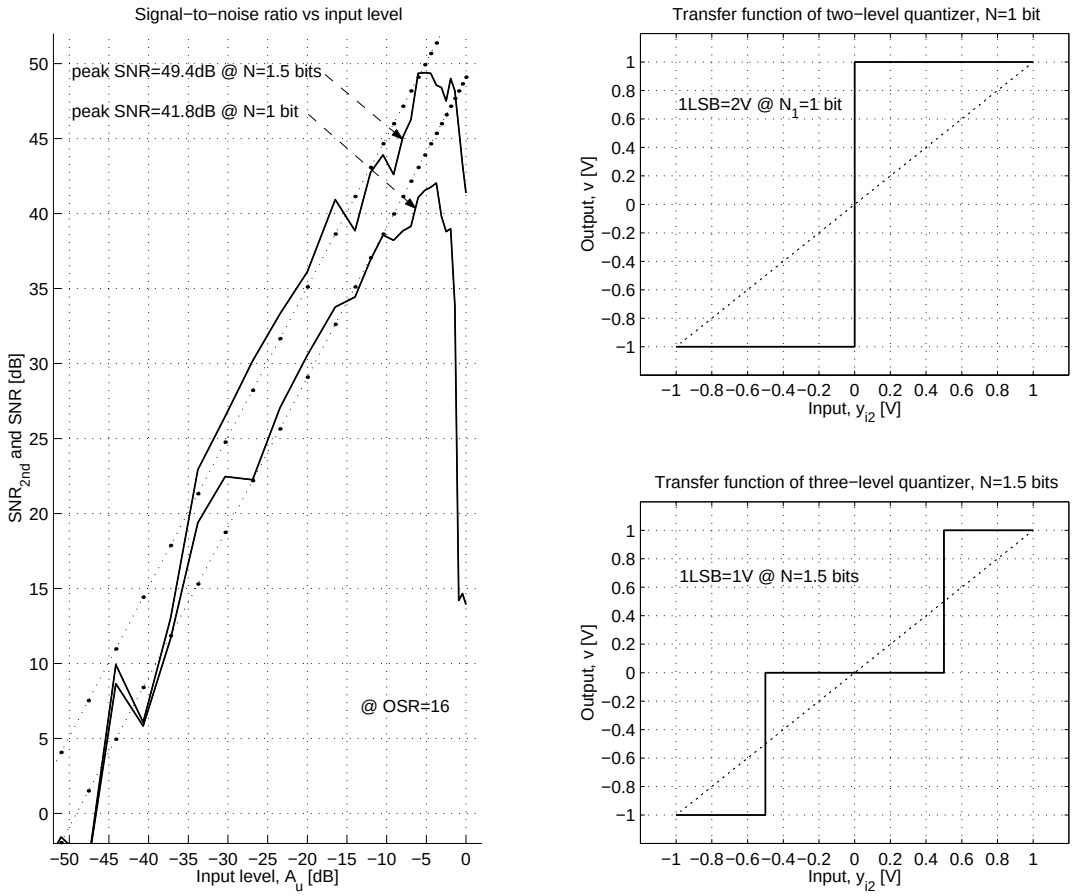

Figure 2.25: Comparative performance of bi- and tri-level modulators

fer function calculated from (2.34) will be $NTF(z) = (1 - z^{-1})^2$ only if the modulator is balanced (Fig. 2.26.a). Otherwise, if the modulator is unbalanced (Fig. 2.26.b–d), its noise transfer function calculated from (2.34) will not be anymore $NTF(z) = (1 - z^{-1})^2$, so its quantization noise suppression will not be so effective, and its SNR performance will be more modest.

This example illustrated again that the gain of a multibit quantizer is defined by the position of its threshold voltages if its output is also a digital sequence of multibit words, and, on the other hand, the gain of a single-bit quantizer is controlled by the feedback loop in such a way that the product of gain factors becomes unity ($a_1 a_2 b_1 k = 1$). These are the rule of thumb what gain should one use in the linearized model of the delta-sigma converter.

2.5.8 Performance Limitations

The second-order delta-sigma modulator is a more practical converter than its first-order counterpart. The second integrator randomizes more the output of the first integrator, and hence the idle tones and pattern noise is considerably reduced, but it is not completely eliminated. However, adding a small ($(1 \ldots 10\%)\, A_{max}$)

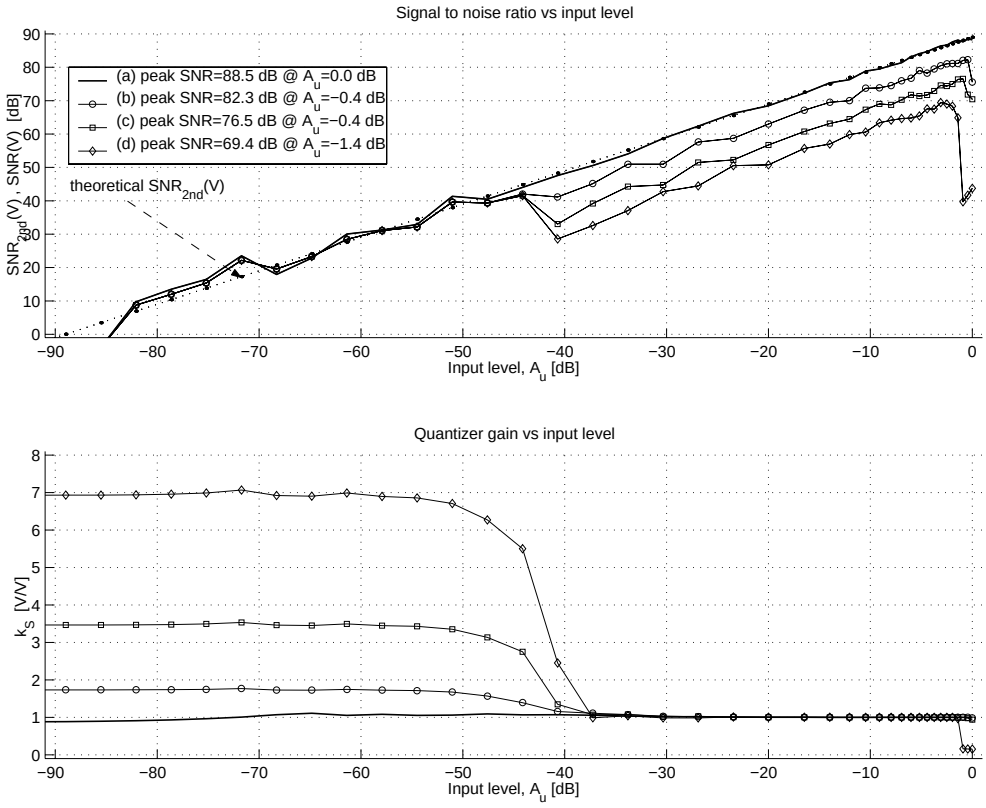

Figure 2.26: Second-order multibit (100 levels, gain $k = 1$) delta-sigma ADC's SNR and quantizer gain curves for $b_2 = 2a_1b_1$ and (a) $\frac{1}{a_1a_2b_1} = 1$, (b) $\frac{1}{a_1a_2b_1} = 2$, (c) $\frac{1}{a_1a_2b_1} = 4$ and (d) $\frac{1}{a_1a_2b_1} = 8$

dither signal [36, Section 3.2.7] improves more this performance. We did not analyze in detail the idle-tone issue, described in detail for example in [38, Chapter 3], but the reader can get a good feeling of this by simply comparing the spectra of $Q_1(z)$ and $V_{m_{real}}(z)$ in undithered (Fig. 3.12) and dithered (Fig. 4.7) case. Note that the output of the (cascaded) delta-sigma modulator got smoother by injecting a small white noise with amplitude $A_t = 0.05$ V before the quantizer (Fig. 4.1.b). Some more details are provided in Sections 3.2.2 and 4.2.1.

Although the second-order modulator provides a good quantization noise suppression in the signal band, it requires high oversampling ratios to achieve high SNR performance. Therefore, in actual applications its performance is improved by interconnecting it with one or two extra stages, or by using a multibit quantizer in the forward path and a linearized multibit DAC in the feedback path.

2.5.9 Adding a Forward Path

So far, we did not consider the influence of the nonidealities introduced by the real circuits which implement the delta-sigma modulator. It was mentioned in Section 2.3.2 that the delta-sigma modulator is a very robust structure, and it is

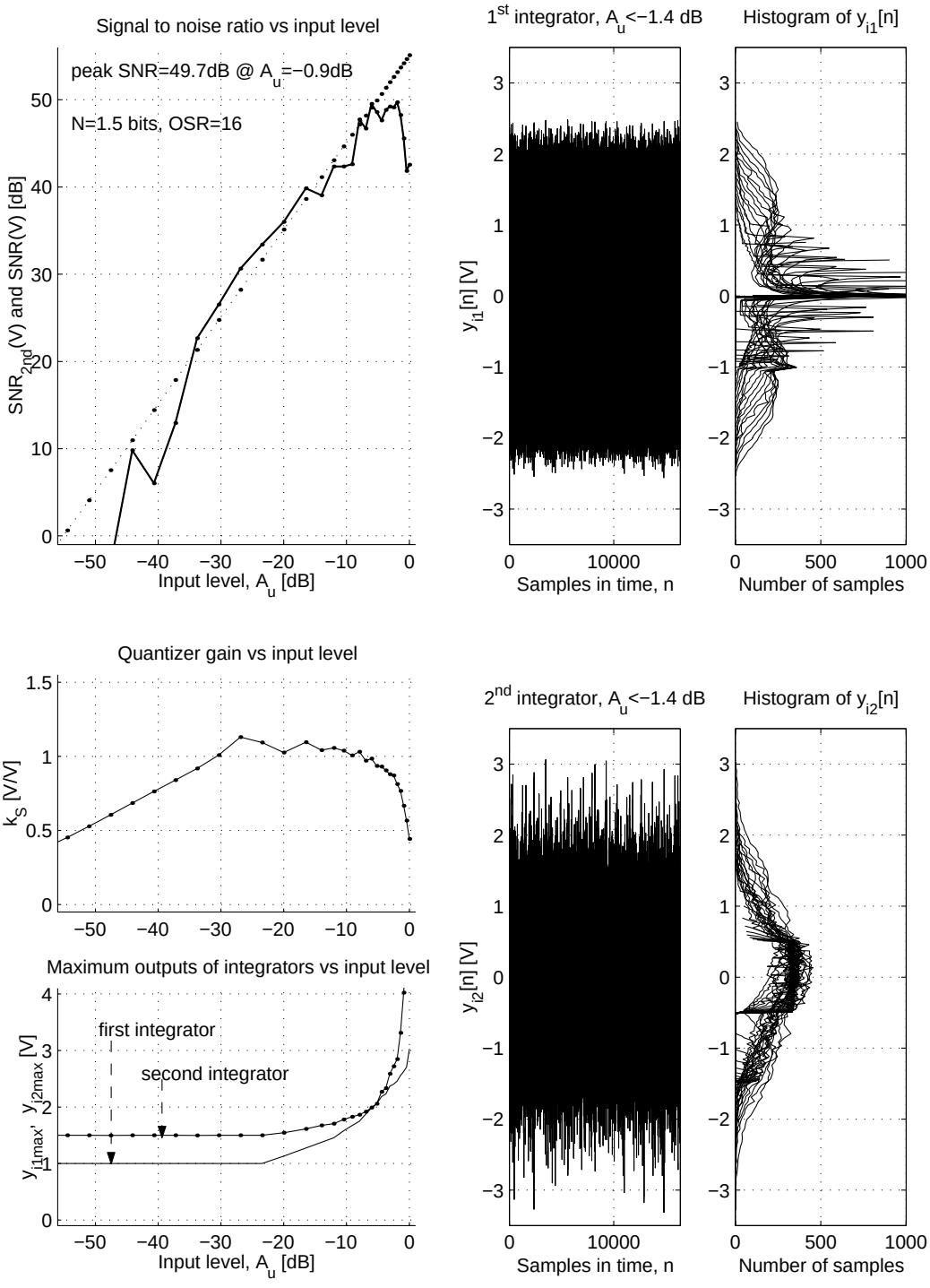

Figure 2.27: Internal voltage swings for $a_1 = 1$, $a_2 = 1$, $b_1 = 1$, $b_2 = 2$, $k = 1$

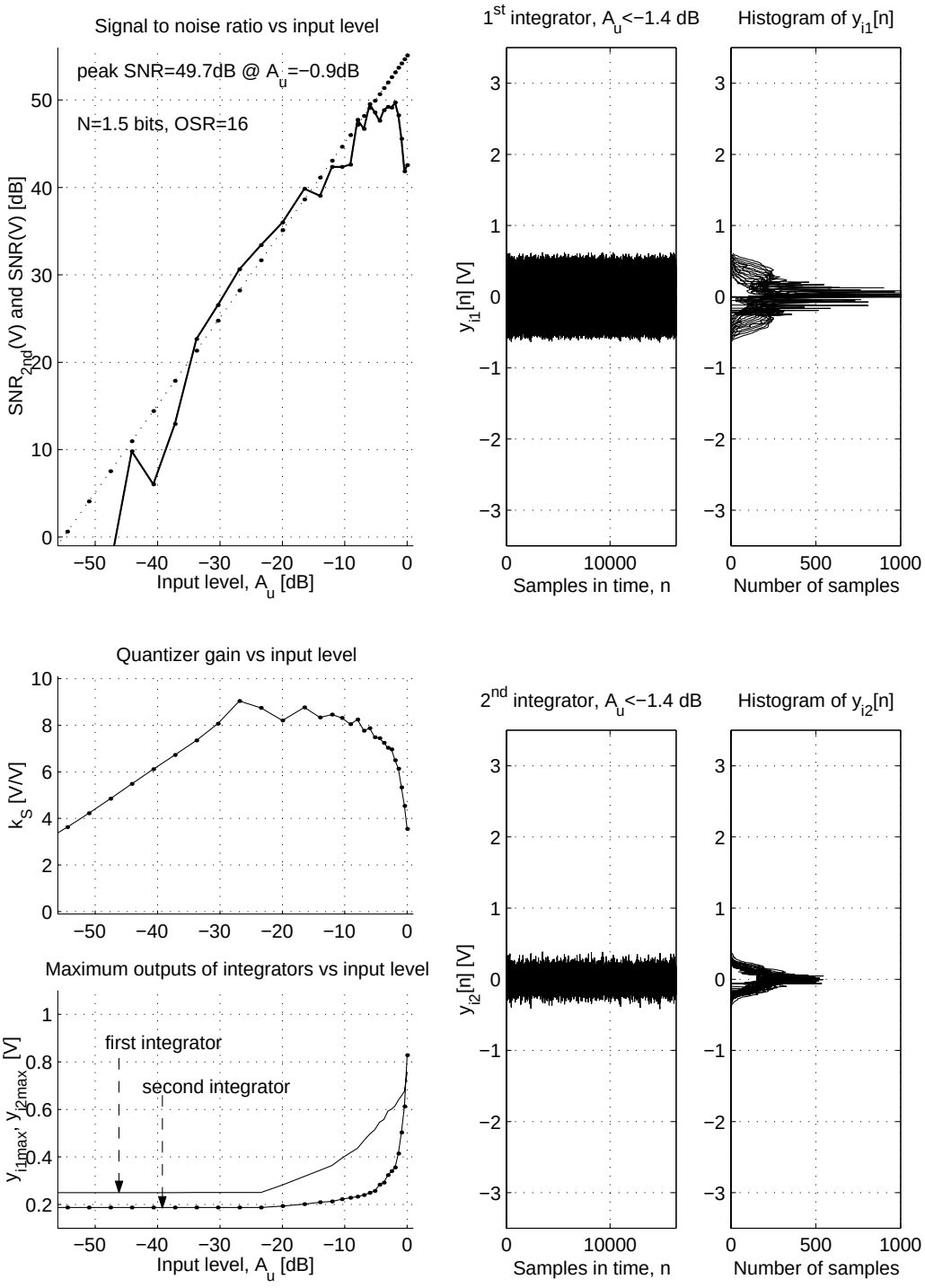

Figure 2.28: Internal voltage swings for $a_1 = \frac{1}{4}$, $a_2 = \frac{1}{2}$, $b_1 = 1$, $b_2 = \frac{1}{2}$, $k = 8$

insensitive to the errors introduced by nonideal analog circuits. However, the technologies are continuously being scaled and the supply voltage lowered. In addition, high-speed technologies offer high operating rates (e.g. f_S=100 MHz in switched-capacitor circuits). It turns out that due to the low supply voltage and high sampling frequency, the achievable gain of the opamps from the integrators might be quite low and nonlinear. These low and nonlinear gains of the opamps will cause harmonic distortions of the input signal, with errors which may dominate both the total harmonic distortion (THD) and the noise performance (SNR) of the delta-sigma modulator [56].

The basic idea in delta-sigma modulators (Fig. 2.8) is to keep the error voltage $e[n]$ as small as possible in the signal band. Therefore, the input node, which performs the "delta" operation $e[n] = u[n] - v_a[n]$, is the most sensitive node. In the popular design of delta-sigma converters (Fig. 2.8), the input signal $u[n]$, which appears in the output $v[n]$, has to go through the loop filter $H(z)$, so the nonlinearities of the loop filter $H(z)$ might introduce distortion into the output image $v[n]$ of the input signal. Because the input node is the most sensitive node in the delta-sigma architecture, the nonlinearity of the first integrator from the loop filter is the most critical issue in the design.

This problem can be simply balanced by adding a forward path over the loop filter $H(z)$ [56], as is presented in Fig. 2.29. The improvement is obtained by directly feeding the input signal $u[n]$ to the quantizer, so that it can be taken into account immediately [26], and the loop filter will process only the quantization noise instead [38, Section 5.6].

The second-order delta-sigma ADC was simulated at behavior-level with and without the forward path. Adding the forward path increased the signal swing of the output of the integrators y_{i1} and y_{i2} with about 10%, which is critical from dynamic range point of view. In conclusion, in the prototype chip design (Chapter 5) we included the forward path as an optional choice and we will study its real effects by measurements as soon as the integrated circuit is available.

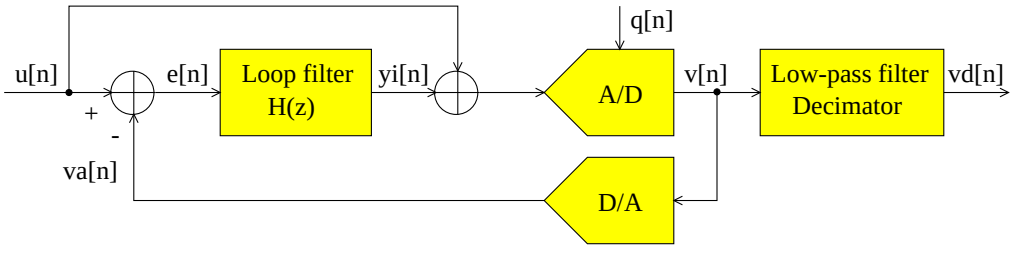

Figure 2.29: General delta-sigma modulator with a forward path

2.6 Higher-Order Delta-Sigma ADCs

Based on the basic operation of a delta-sigma modulator presented in Section 2.3.1, it is obvious that the quantization noise can be further suppressed in the baseband, and hence gaining more SNR performance, by simply using a more aggressive

noise transfer function provided by a higher-order loop filter $H(z)$, which leads in turn to a higher-order delta-sigma modulator. In general, an L^{th} order delta-sigma modulator would have $NTF(z) = (1 - z^{-1})^L$, and its SNR_{Lth} would be given by

$$\begin{aligned} SNR_{\mathrm{Lth}} &= 20\,\log_{10}\frac{A_u}{A_{max}} + 6.02\,N + (20\,L + 10)\,\log_{10} OSR \\ &\quad -10\,\log_{10}\frac{\pi^{2\,L}}{2\,L+1} + 1.76 \quad [\mathrm{dB}] \end{aligned} \tag{2.52}$$

which corresponds to a $(6\,L + 3)$-dB/octave or $(L + \frac{1}{2})$-bit/octave improvement. Unfortunately, using a higher-order delta-sigma modulator with $NTF(z) = (1 - z^{-1})^L$, $L > 2$, would lead to unstable operation for large input signals. However, there has been found, and first stated by Lee, an empirical rule for designing stable higher-order single-bit modulators [38, Section 4.4.1]. Lee claimed that a single-bit delta-sigma modulator will remain stable even for large input signals, if its noise transfer function has a maximum gain of less than 1.5:

$$\max\{|NTF(z)|\} < 1.5 \tag{2.53}$$

Based on this empirical rule several stable high-order single-bit modulators has been designed e.g. [7], [8], but the rule should be used only with caution [26].

In general, to improve the performance of a single-loop delta-sigma modulator, one would have several choices based on (2.52), which can be applied separately or simultaneously, depending on the application:

1. **Increase OSR** (to use a higher oversampling ratio)
   - ◇ *performance gain:* $(6\,L + 3)$-dB improvement for every doubling of the OSR;
   - ◇ *limitation:* the signal bandwidth will be reduced;
   - ◇ *solution:* increasing L, or increasing N, or choosing different architecture.
2. **Increase L** (to use a higher-order modulator)
   - ◇ *performance gains:* 6-dB improvement for every increment in L and, in addition, $(6\,L+3)$-dB improvement for every doubling of the OSR;
   - ◇ *limitation:* the modulator can become unstable;
   - ◇ *solution:* reducing $\max\{|NTF(z)|\}$ according to Lee's rule and verifying the stability by extensive simulations.
3. **Increase N** (to use a multibit modulator)
   - ◇ *performance gain:* 6-dB improvement for every increment in N;
   - ◇ *limitation:* the nonlinearity of the multibit DAC in the feedback path is critical;

- ◇ *solution:* using mismatch-shaping, or analog or digital correction methods for highly-linear DACs.

4. Looking for other **architecture**, such as cascaded modulators...

In the following chapters cascaded 2-0 delta-sigma analog-to-digital converters will be studied in detail.

2.7 Conclusions

In this chapter we presented a large spectrum of basic and more advanced issues of the analysis and the design of single-loop delta-sigma ADCs. Delta-sigma modulators trade signal bandwidth and very fast circuit operations for higher resolution, and trade analog circuit accuracy for digital circuit complexity.

The basic operation of a delta-sigma modulator is usually described by its linearized model, and by the concepts of signal transfer function and noise transfer function. The linearized model, which replace a deterministic nonlinearity by a stochastic linear system, however, lies on weakly verified assumptions, so it should be used only as a first-order approximation, and the final conclusions must be validated by extensive simulations.

In the linearized model, the gain of a single-bit quantizer is controlled by the feedback loop in such a way that the product of loop-gain factors becomes unity, but the gain of a multibit quantizer is given by the position of its threshold voltages, if its output is also a digital sequence of multibit words.

A detailed design of a second-order delta-sigma ADC was presented also. The designed converter will be used for the first stage of our adaptive compensated cascaded 2-0 delta-sigma ADC.

Chapter 3

Cascaded Delta-Sigma ADCs

Cascaded delta-sigma converters offer a good compromise between high accuracy, robust stability and speed. However, their sensitivity to analog circuit imperfections is much higher than that of their single-loop counterpart, because they rely on the perfect matching of the transfer functions of two internal signal paths, one predominantly analog and the other predominantly digital [34].

The general structure of a cascaded delta-sigma or Multi-stAge noiSe-sHaping (MASH)[1] [57], [58], [59] modulator is presented in Fig. 3.1 [29]. The cascaded modulator can be obtained by interconnecting two delta-sigma modulators with signal transfer functions STF_1 and STF_2, and noise transfer functions NTF_1 and NTF_2. The digital outputs of the two delta-sigma modulators v_1 and v_2, are filtered by two digital filters STF_{2d} and NTF_{1d}, respectively. The quantization error q_1 of the first-stage quantizer is estimated by u_2, is quantized by the second stage, is filtered by a digital compensation filter NTF_{1d} which imitates the NTF_1, and the result is subtracted from STF_{2d}(z)V_1(z) [26]. The quantization error of the second stage is q_2. One can write the following equations:

$$\begin{aligned}
V_1(z) &= STF_1(z)\,U_1(z) + NTF_1(z)\,Q_1(z) && (3.1)\\
V_2(z) &= STF_2(z)\,U_2(z) + NTF_2(z)\,Q_2(z) && (3.2)\\
U_2(z) &= Q_1(z) && (3.3)\\
V_m(z) &= STF_{2d}(z)\,V_1(z) - NTF_{1d}(z)\,V_2(z) && (3.4)\\
\Longrightarrow V_m(z) &= STF_1(z)\,STF_{2d}(z)\,U_1(z) - NTF_{1d}(z)\,NTF_2(z)\,Q_2(z) \\
&\quad +(NTF_1(z) - NTF_{1d}(z))\,Q_1(z) && (3.5)
\end{aligned}$$

Because in the ideal case $NTF_1(z) = NTF_{1d}(z)$, the output of the modulator is given by

$$V_m(z) = STF_1(z)\,STF_2(z)\,U_1(z) - NTF_{1d}(z)\,NTF_2(z)\,Q_2(z) \qquad (3.6)$$

which means that one can obtain a noise transfer function of an ideal $(n_1 + n_2)$ order single-loop modulator, which remains stable as long as the individual modulators are stable, so it is desirable to design for $n_{1,2} \leq 2$, where n_1 and n_2

[1]The name "MASH" was probably chosen from a popular Robert Altman movie (1970), and its following TV-show version, both called also MASH, where the title stands for "Mobile Army Surgical Hospital."

are the orders of the first and second stage, respectively. However, the condition $NTF_1(z) = NTF_{1d}(z)$ cannot be exactly fulfilled due to the analog circuit imperfections. In other words, the analog noise transfer function NTF_1 does not match exactly its digital counterpart NTF_{1d}, so the quantization noise $Q_1(z)$ of the first stage is not eliminated completely from the cascaded modulator output $V_m(z)$, (3.5), which leads to significant performance deterioration [29].

In the present work 2-stage 2-0 modulators [60], [61], [38, Section 8.5.1] were investigated, which are built from a second-order delta-sigma modulator and a multibit "plain" (zero-order) analog-to-digital converter with N_2 bits of resolution (see the footnote 2 on page 5).

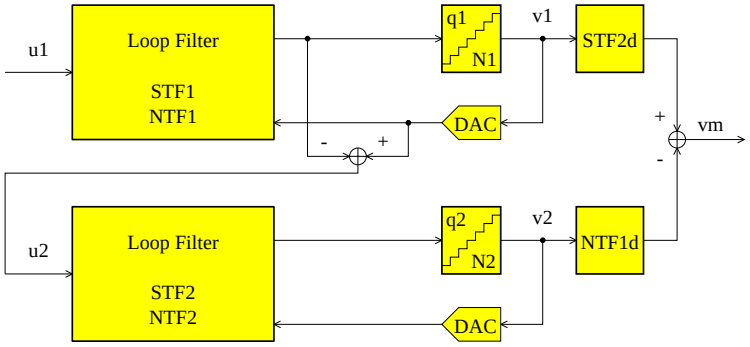

Figure 3.1: General structure of a cascaded delta-sigma modulator

3.1 Cascaded 2-0 Delta-Sigma ADC Structures

A 2-stage 2-0 delta-sigma ADC is built from a second-order delta-sigma N_1-bit ADC and a multibit ADC with N_2 bits of resolution [60], [61], [38, Section 8.5.1]. The standard structure is presented in Fig. 3.2. However, the second stage overloads, that is, $|q_2| > \frac{1}{2}\frac{FSR}{2^{N_2}-1}$, even for small input values of u_1, so this modulator is impractical [32].

The improved standard structure, presented in Fig. 3.3, uses a supplementary gain stage[2] in front of the second stage with a subunity gain factor m_0, which provides an extra degree of freedom to trade peak-SNR value for usable input signal range. In order to simplify the analog circuit, the subtraction branch with the gain factor β can be shifted into the digital domain (Fig. 3.4). This simplified structure was investigated in the previous work [17], [31], [32]. However, by simply combining the last two cascaded modulators discussed above, one can design a general cascaded 2-0 delta-sigma ADC (Fig. 3.5), which can lead to better performance with a 6-dB SNR improvement [33].

[2]Note that the improved standard structure (Fig. 3.3) is equivalent with the standard structure (Fig. 3.2) with $\alpha' = \frac{\alpha}{m_0}$ and $\beta' = \frac{\beta}{m_0}$.

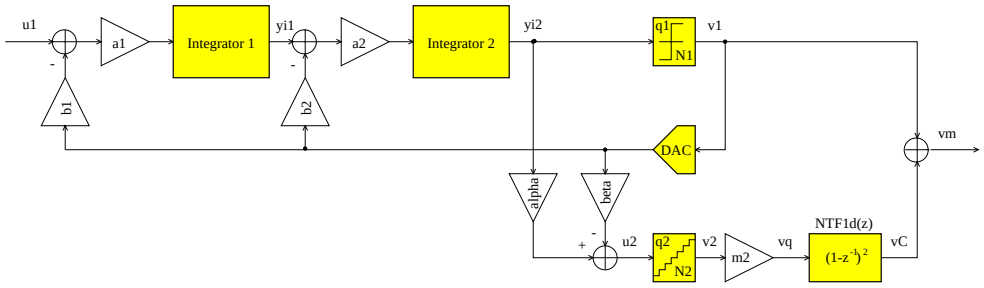

Figure 3.2: Standard structure of the cascaded 2-0 delta-sigma ADC

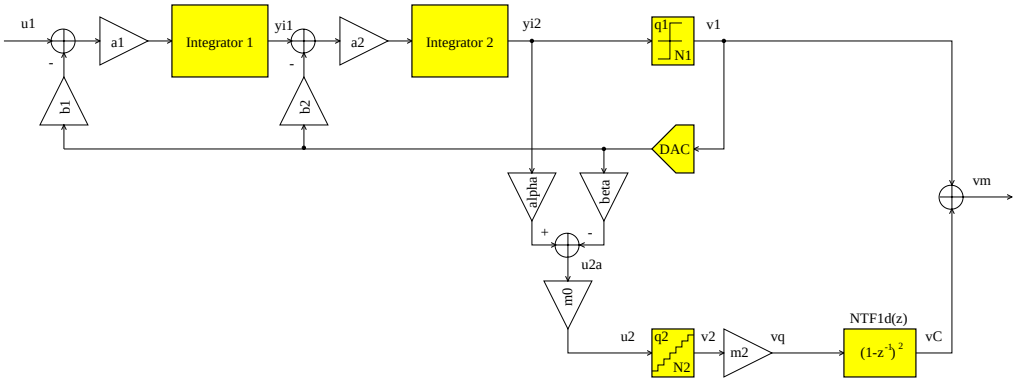

Figure 3.3: Improved standard structure of the cascaded 2-0 $\Delta\Sigma$ ADC

3.1.1 Performance Modeling

In order to present a comparative analysis of these structures, the transfer function of the general architecture (Fig. 3.5) will be derived. The two quantizers were modeled as input signal independent additive white-noise sources (Section 2.1.1) preceded by two gain stages with constant (input signal independent) gain factors $k_1 = \frac{1}{a_1 a_2 b_1}$ ($N_1 = 1$ bit) or $k_1 = 1$ ($N_1 > 1$ bit), and $k_2 = 1$ ($N_2 > 1$ bit). The resulting linearized model is presented in Fig. 3.6. The desired output of the cascaded ADC is given by

$$V_m(z) = z^{-2}\, U_1(z) + m_2\,(1 - z^{-1})^2\, Q_2(z) \neq f(Q_1(z)), \tag{3.7}$$

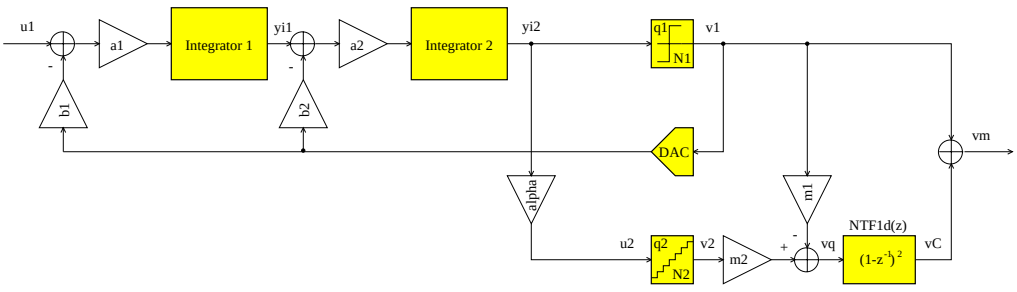

Figure 3.4: Simplified structure of the cascaded 2-0 delta-sigma ADC

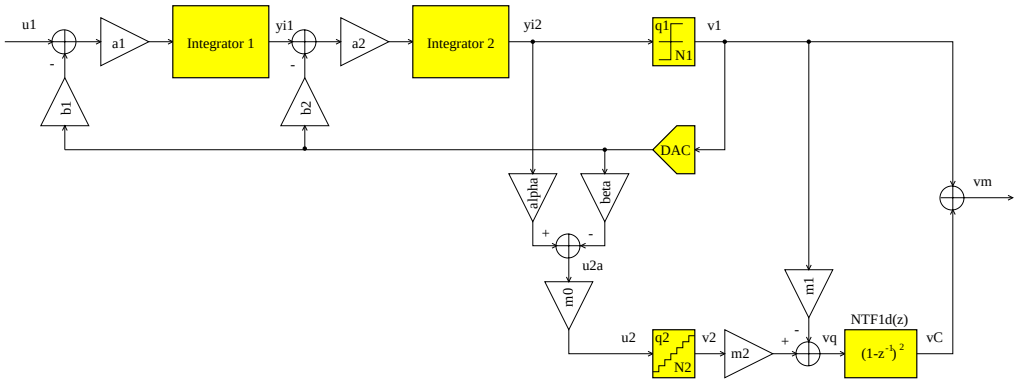

Figure 3.5: General structure of the cascaded 2-0 delta-sigma ADC

which can be obtained from

$$V_m(z) = V_1(z) + V_C(z) \tag{3.8}$$
$$V_1(z) = z^{-2}\,U_1(z) + (1-z^{-1})^2\,Q_1(z) \tag{3.9}$$
$$V_C(z) = -(1-z^{-1})^2\,Q_1(z) + m_2\,(1-z^{-1})^2\,Q_2(z). \tag{3.10}$$

Therefore, the desired residue voltage $V_q(z)$ should be given by

$$V_q(z) = -Q_1(z) + m_2\,Q_2(z), \tag{3.11}$$

but, in general, with $m_2 = \frac{1}{m_0}$ assumed,

$$V_q(z) = (\alpha - k_1\,\beta - k_1\,m_1)\,Y_{i2}(z) - (\beta + m_1)\,Q_1(z) + m_2\,Q_2(z). \tag{3.12}$$

In conclusion, from (3.11) and (3.12) the interstage coefficients should satisfy:

$$\begin{cases} \beta + m_1 = 1 \\ \alpha = k_1\,(\beta + m_1) = k_1 \\ m_2 = \frac{1}{m_0} \end{cases} \tag{3.13}$$

The expected theoretical performance can be calculated by using the linearized model and equation (3.7), so the theoretical signal-to-noise ratio SNR_{th} is given by

$$SNR_{th}(V_m) = 20\,\log_{10}\frac{A_u}{A_{max}} + 6.02\,N_2 + 50\,\log_{10}OSR - 20\,\log_{10}m_2 - 11.14\,[\text{dB}] \tag{3.14}$$

Simulations demonstrated (e.g. Fig. 3.9) that the theoretical $SNR_{th}(V_m)$ and the simulated $SNR(V_m)$ are close until the overloading of the second stage occurs, that is, $|q_2| > \frac{1}{2}\frac{FSR}{2^{N_2}-1}$.

3.1.2 Interstage Coefficients

When $m_1 = 0$, the input to the second stage is simply attenuated by a subunity factor m_0, but this is necessary to keep the second stage from overloading (cf. the

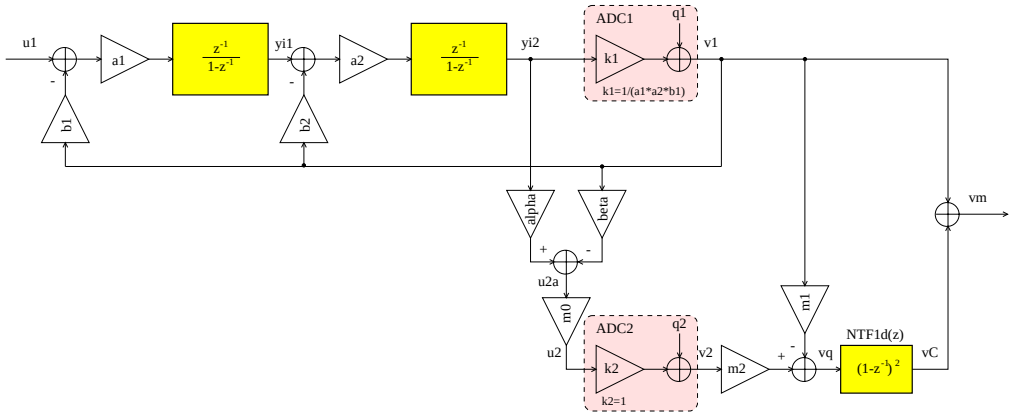

Figure 3.6: Linearized model of the general cascaded 2-0 delta-sigma ADC

improved standard MASH, Fig. 3.2). To compensate for this attenuation, the digital output of the second stage must be scaled by $m_2 = \frac{1}{m_0}$ before being processed by the first-stage quantization error $q_1[n]$ cancellation logic to make this cancellation effective. Note that by doing so the effect of the second-stage quantization error $q_2[n]$ is increased by a factor of m_2. Therefore, the most convenient peak SNR (which can be increased by choosing m_0 large and m_2 small) versus usable input signal range (which can be increased by choosing m_0 small and m_2 large) should be selected by giving different values for m_0.

In addition, the trade-off between small-signal and large-signal performance can be improved by adjusting β and m_1, to achieve a better weighting of the input and the output of the first-stage quantizer in the formation of the second-stage input [38, Section 7.3.1]. When m_1 is nonzero, and hence $\beta \neq 1$, a component of the analog representation of $v_1[n]$ is introduced into the second-stage input, that is, $u_2[n]$ will not be only formed by the first-stage quantization noise $q_1[n]$. This supplementary component of $v_1[n]$ must be digitally subtracted from the output of the second stage before performing the error cancellation. In this way, under the constrains $\beta + m_1 = 1$ and $\alpha = k_1$, the value of β does not affect the final output $v_m[n]$ of the cascaded ADC, given in (3.7). However, the value of β does affect the probability density function (PDF) of the input to the second stage $u_2[n]$, and β may be optimized in order to constrain the signal range at the input to the second stage, and thereby allow the largest possible value for m_0 [38, Section 7.3.1].

It is important to note that a delayed version of the analog input signal $u_1[n]$ is introduced into the second-stage input $u_2[n]$ when the coefficient $\beta \neq 1$. Therefore, the nonlinearities of the second stage may affect the linearity of the overall system. However, the harmonics of $u_1[n]$ introduced by the second-stage ADC are attenuated by $NTF_{1d}(z)$, e.g. by 18 dB for an oversampling ratio of $OSR = 8$. For example, if the second-stage ADC has 10-bit linearity than a 13-bit linearity is still easily achievable for the overall 2-0 MASH ADC which works at an oversampling ratio at least of $OSR = 8$ [34].

Simulation results are presented in Fig. 3.7 illustrating the impact of different values of $m_2 = \frac{1}{m_0}$ on different cascaded 2-0 delta-sigma ADCs. The simplified

structure ($\beta = 1$, $m_1 = 0$, Fig. 3.4 and Fig. 3.7.a) [29], the improved standard structure ($\beta = 0$, $m_1 = 1$, Fig. 3.3 and Fig. 3.7.b), and the general structure (Fig. 3.5) [38, Section 7.3.1] for $\beta = 2$ and $m_1 = -1$ (Fig. 3.7.c) [49] and for $\beta = 4$ and $m_1 = -3$ (Fig. 3.7.d) were investigated. In these simulations $OSR = 16$, $N_1 = 1$ bit, $N_2 = 12$ bits and ideal analog circuits were considered. The $\frac{kT}{C}$-noise was also neglected.

Finally, the probability density function of the second-stage input signal $PDF(u_2)$, correlated with the achieved SNR performance, is presented in Fig. 3.8. The behavior of the general cascaded 2-0 delta-sigma ADC was investigated for different pairs of (β, m_1), where $\beta + m_1 = 1$, and the largest possible m_0 was selected for each pair of (β, m_1) based on similar results with those presented in Fig. 3.7. Note that the tails of $PDF(u_2)$ for $\beta = -1$, $\beta = 0$ and $\beta = 2$ exceeded the available input range ± 1 V to the second stage, and therefore the corresponding SNR performance already had dropped. On the other hand, for $\beta = 4$ the input range u_2 is well bounded even for large input signals.

In conclusion, ($\beta = 2$, $m_1 = -1$, $m_0 = \frac{1}{2}$, $m_2 = 2$) produces the best small-signal performance, but for the best large-signal performance ($\beta = 4$, $m_1 = -3$, $m_0 = \frac{1}{4}$, $m_2 = 4$) should be used. These conclusions are similar to those presented in [38, Section 7.3.1] which were derived for a 2-1 MASH ADC.

3.1.3 Tri-Level Quantizer

From (3.7) and (3.14) it can be observed that if the first-stage quantization noise $Q_1(z)$ gets cancelled due to the equality $NTF_1(z) = NTF_{1d}(z)$, and, in addition, second-order noise shaping is provided by $NTF_1(z) = (1 - z^{-1})^2$, then the first-stage SNR performance does not play any role in the total performance of the cascaded ADC. However, a more careful analysis reveals that m_0 and, therefore m_2, definitely depend on the first stage, because they rely on the scaled probability density function of $u_{2a}[n]$, which is determined by the probability density functions of $y_{i2}[n]$ and $q_1[n]$. Therefore, the usable input signal range $u_1[n]$ can be manipulated from the first stage also, not only be changing the interstage coefficients. In conclusion, using a tri-level quantizer in the first-stage (details in Section 2.5.7), would extend the usable input signal range $u_1[n]$, and, therefore, it would improve the peak $SNR(V_m)$ with about 2-6 dB, depending on the MASH structure.

There are other issues, such as the sensitivity of the cascaded ADC on the test signal injection, but some details will be provided in Sections 4.2.1 and 4.2.2. Finally, the general structure (Fig. 3.5) with $\beta = 2$, $m_1 = -1$, $m_0 = \frac{1}{2}$, $m_2 = 2$ interstage coefficients, and a tri-level quantizer $N_1 = 1.5$ bits in the first stage ($a_1 = \frac{1}{4}$, $a_2 = \frac{1}{2}$, $b_1 = 1$, $b_2 = \frac{1}{2}$ and $k_1 = 8$) was chosen, having the best peak SNR [18]. Simulation results are presented in Fig. 3.9. In these simulations $OSR = 16$, $N_2 = 12$ bits and ideal analog circuits were considered. The $\frac{kT}{C}$-noise was also neglected.

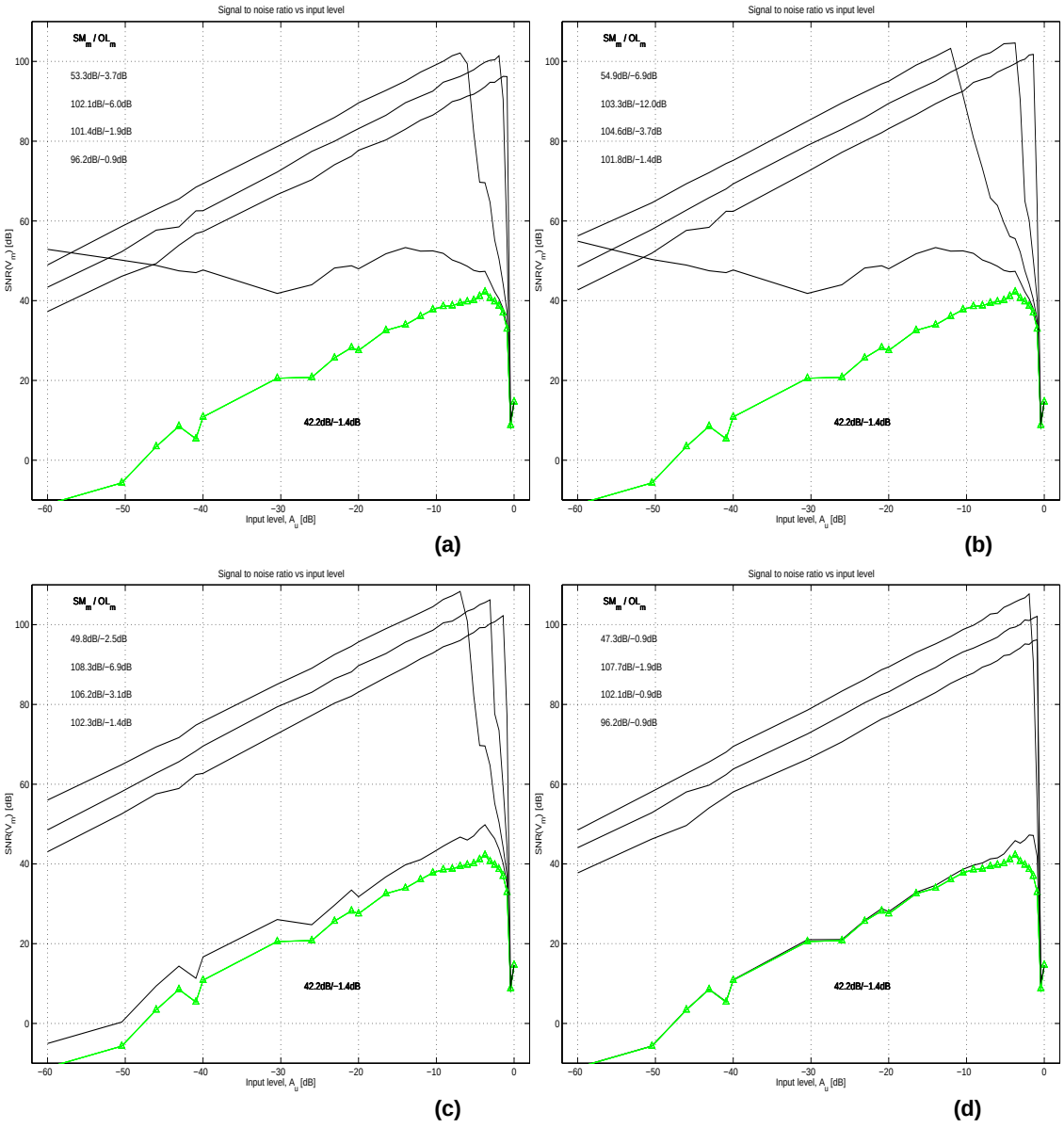

Figure 3.7: Comparative performance analysis between different ideal 2-0 MASH structures for $OSR = 16$, $N_1 = 1$ bit and $N_2 = 12$ bits: (a) simplified structure, $\beta = 1$, $m_1 = 0$, $m_2 = 2, 4, 8, 16$ (top to bottom); (b) improved standard structure, $\beta = 0$, $m_1 = 1$, $m_2 = 1, 2, 4, 8$; (c) general structure, $\beta = 2$, $m_1 = -1$, $m_2 = 1, 2, 4, 8$; (d) general structure, $\beta = 4$, $m_1 = -3$, $m_2 = 2, 4, 8, 16$.

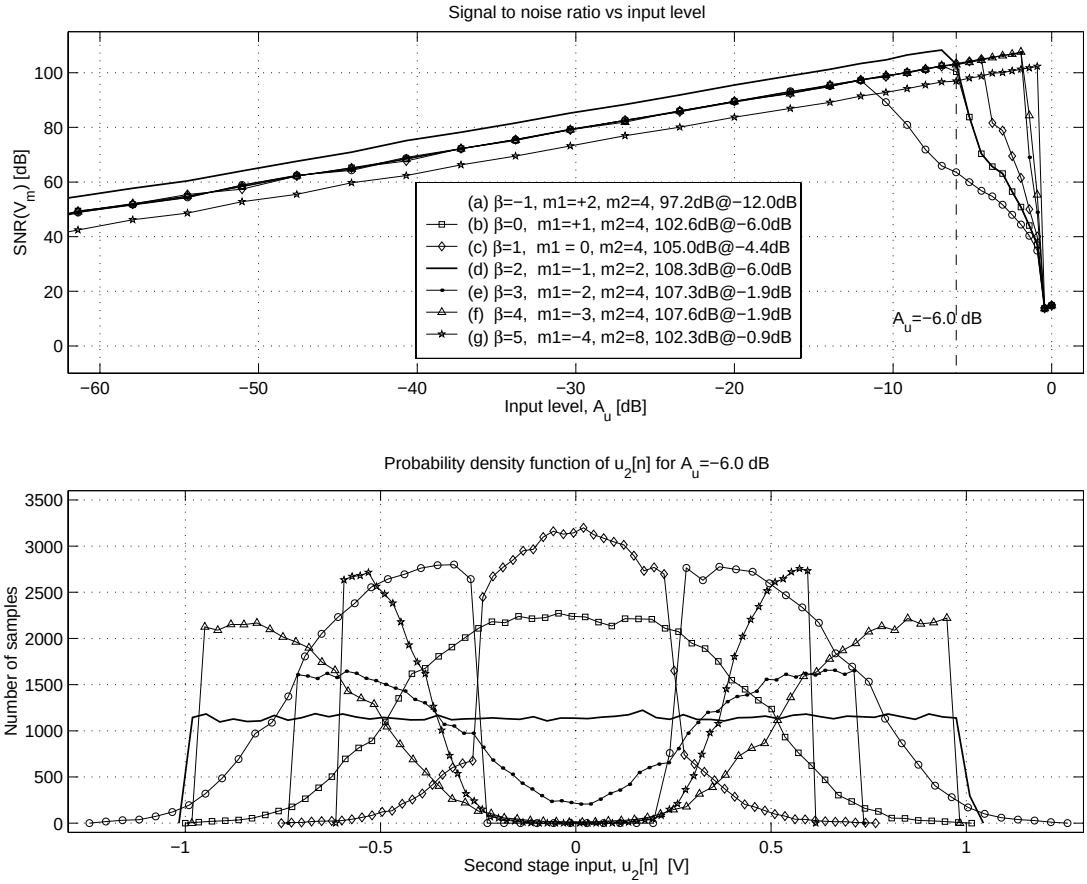

Figure 3.8: SNR performance and $PDF(u_2[n])$ for different β and m_1, assuming ideal MASH, $OSR = 16$, $N_1 = 1$ bit and $N_2 = 12$ bits

3.1.4 Performance Specifications and Limitations

The theoretical, expected performance of an ideal cascaded 2-0 delta-sigma modulator is given by (3.14) which shows the effect of the oversampling ratio OSR [15-dB/octave], of the second-stage resolution N_2 [12-dB/octave], of the inter-stage coefficient m_2 [-6-dB/octave] and the usable input range A_u [6-dB/octave]. In practical design the achievable ideal performance ("ideal": there were no analog circuit imperfections assumed) is limited by the signal bandwidth requirements, hardware complexity and chip area.

In the presented work we are aiming for a large-bandwidth and high-resolution ADC. Therefore, $f_S = 100$ MHz sampling frequency and switched-capacitor implementation were chosen and the modulator will operate at a low oversampling ratio of $OSR = 8$–16. For the second stage a $N_2 = 10$-bit pipelined ADC was chosen, but in the future work this will be hopefully changed with a $N_2 = 12$-bit ADC. The ideal MASH performance is also limited by the thermal noise of the switched capacitors, which is usually called as $\frac{kT}{C}$-noise [39, Section 4.3]. With a fairly large input sampling capacitor of 6 pF this noise floor can be limited to -92 dB (15 bits). Therefore, the achievable performance is presented in Fig. 3.10

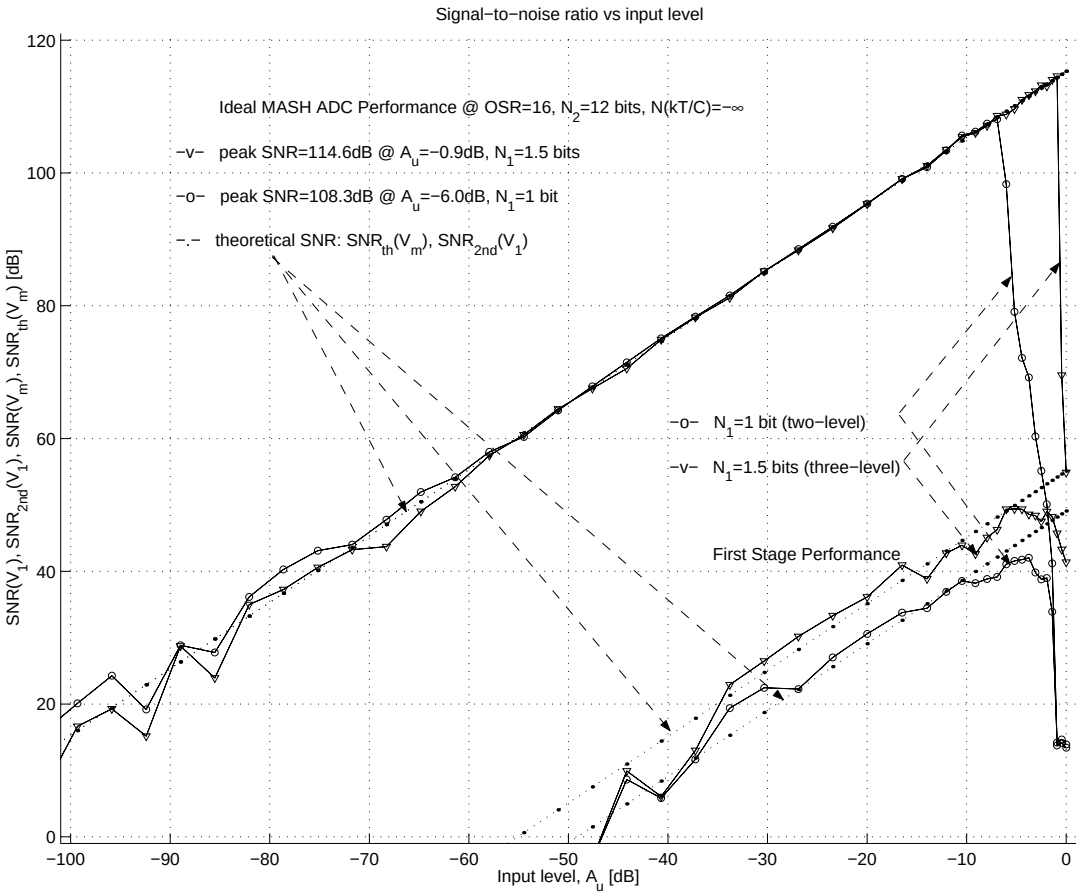

Figure 3.9: Comparative performance of the general MASH ($\beta = 2$, $m_1 = -1$, $m_0 = \frac{1}{2}$, $m_2 = 2$) for bi-level ($N_1 = 1$ bit, $k_1 = 1$) and tri-level ($N_1 = 1.5$ bits, $k_1 = 8$) first stage ($a_1 = \frac{1}{4}$, $a_2 = \frac{1}{2}$, $b_1 = 1$, $b_2 = \frac{1}{2}$)

and a peak SNR of 86 dB was obtained, for the same general 2-0 cascaded delta-sigma ADC architecture which was considered in Fig. 3.9. Unfortunately, due to the analog circuit imperfections this performance drops drastically (details in Section 3.2), but an effective compensation method will be shown, which loses less than 1 bit from the ideal performance (details in Chapter 4). Note that the first stage, that is, a simple second-order delta-sigma ADC, is almost completely insensitive to the analog circuit imperfections and its SNR-curve sneaks between the variations of its ideal counterpart.

In conclusion, we are aiming for a 13-bit converter with 6 MHz of bandwidth.

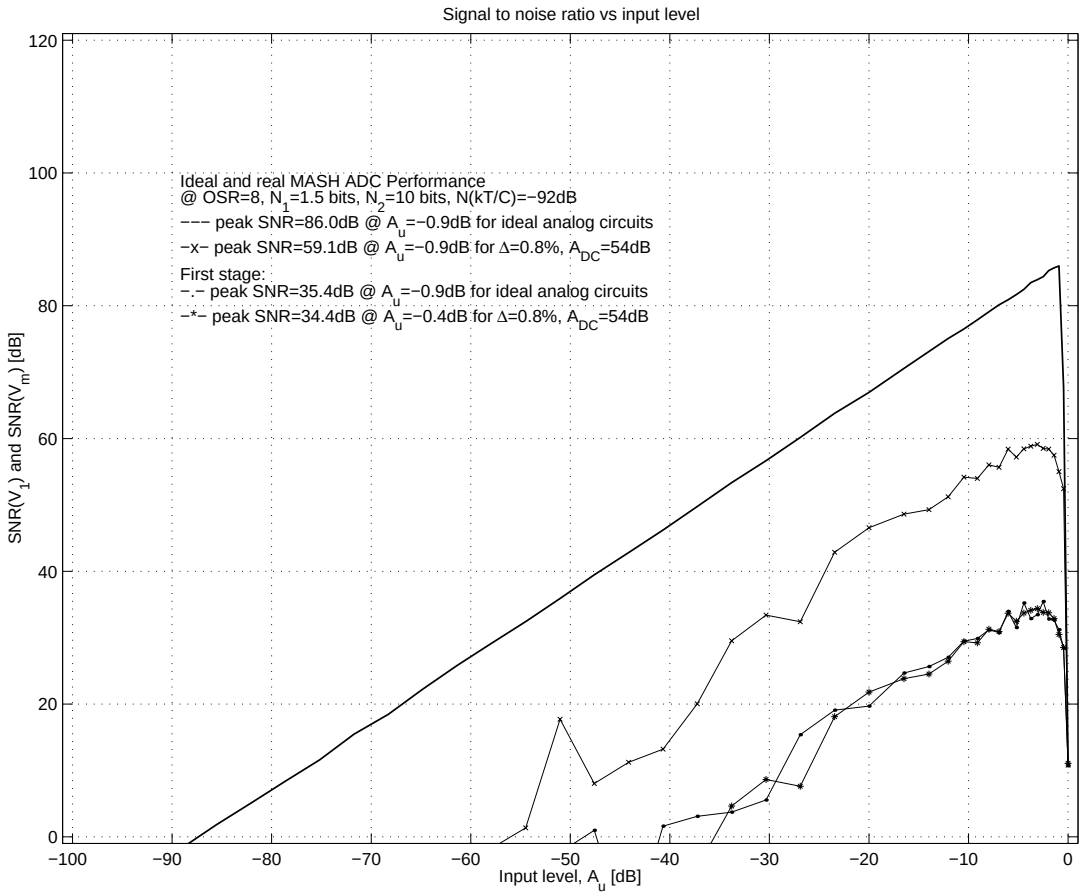

Figure 3.10: Ideal and real cascaded 2-0 delta-sigma ADC SNR performance ($a_1 = \frac{1}{4}$, $a_2 = \frac{1}{2}$, $b_1 = 1$, $b_2 = \frac{1}{2}$, $k_1 = 8$, $\beta = 2$, $m_1 = -1$, $m_0 = \frac{1}{2}$, $m_2 = 2$)

3.2 Analog Circuit Imperfections in Switched-Capacitor Cascaded Delta-Sigma ADCs

The main drawback of cascaded delta-sigma modulators is their significant performance drop due to the analog circuit nonidealities, namely finite DC opamp gain, mismatch between capacitors, nonzero opamp DC offset voltage, and offset and gain errors of the internal ADCs and the feedback DAC [23]. The most serious sources of difficulty are the finite DC opamp gain and the capacitor mismatch. For ideal compensation, the digital compensation filter NTF_{1d} should match perfectly the analog noise transfer function of the first stage NTF_1. In practical implementations, the imperfect matching of the analog transfer function NTF_1 and its digital counterpart NTF_{1d}, leads to noise leakage and significant ($-10 \ldots -30$ dB) performance degradation. The noise leakage can be defined as the residual part of the first quantizer's quantization noise which is not eliminated from the output of the MASH modulator due to the analog circuit imperfections. In other words, due to analog circuit imperfections and, the resulting mismatch between the analog and digital noise transfer functions, the first-stage quantiza-

tion noise will not be perfectly cancelled, but it will appear in the MASH output as quantization noise leakage.

3.2.1 Nonidealities in Switched-Capacitor Integrators

In the switched-capacitor filter implementation of a digital filter, in particular of an integrator, the deviation from the ideal transfer function is mainly determined by the finite opamp gain and the capacitor accuracy [62]. The ideal and the real transfer functions of a switched-capacitor integrator (Fig. 3.11) are given by

$$H_{ideal}(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{-az^{-1}}{1 - pz^{-1}} \tag{3.15}$$

$$H_{real}(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{-a(1 - \delta a)z^{-1}}{1 - p(1 - \delta p)z^{-1}} \tag{3.16}$$

where $p = 1$, $\delta p = \frac{a}{A_{DC}}$ (A_{DC} - DC opamp gain), $a = \frac{C_1}{C_2}$ (capacitor ratio), $\delta a = \Delta_C + \frac{1+a}{A_{DC}}$, $\Delta_C = \frac{\Delta C_2}{C_2} - \frac{\Delta C_1}{C_1}$ (relative capacitor error). Therefore:

$$H_{real}(z) = \frac{-a(1 - \Delta_C - \frac{1+a}{A_{DC}})z^{-1}}{1 - (1 - \frac{a}{A_{DC}})z^{-1}} \tag{3.17}$$

Realistic values for the opamp gain are $A_{DC} = 500 \ldots 10,000$ (54...80 dB) and for the relative capacitor error, for which a uniformly error distribution was assumed, $\frac{\Delta C_x}{C_x} = 0.4\%$, which leads to $\Delta_C = 0.8\%$ [27]. According to simulation results (Fig. 3.10), the zero and pole dislocations of the nonideal transfer function lead to significant performance degradation of the cascaded delta-sigma modulator, about -26 dB for $A_{DC} = 54$ dB and $\Delta_C = 0.8\%$. This was simulated assuming the general cascaded 2-0 delta-sigma ADC (Fig. 3.5).

In addition, it is worth mentioning that a more accurate and complete analysis of the analog circuit imperfections would take into account the errors due to imperfect circuit settling, charge injection and clock feedthrough, and $\frac{1}{f}$ as well as $\frac{kT}{C}$-noise. However, these effects are ignored in the present analysis because its main goal is to study and, later, to compensate the major imperfections [17]. Note that the $\frac{kT}{C}$-noise is ignored in the theoretical analysis, but it is taken into account in the performed simulations.

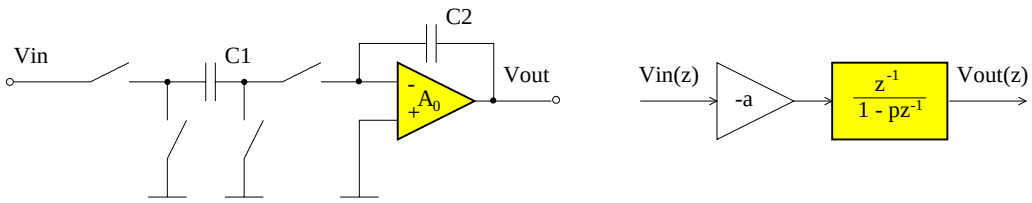

Figure 3.11: Switched-capacitor integrator and its linear model

3.2.2 Noise Leakage in Cascaded Delta-Sigma ADCs

Taking into account the main analog circuit imperfections, which introduce a parasitic leakage path for the first-stage quantization error $q_1[n]$ to the output $v_m[n]$, the ideal and the real output of the cascaded delta-sigma ADC are, respectively:

$$V_{m_{ideal}}(z) = z^{-2}U_1(z) + m_2(1-z^{-1})^2 Q_2(z), \tag{3.18}$$

$$V_{m_{real}}(z) = z^{-2}U_1(z) + m_2(1-z^{-1})^2 Q_2(z) + H_{leakage}(z)Q_1(z) \tag{3.19}$$

Assuming small relative errors due to the finite opamp gain and capacitor mismatch, the noise leakage transfer function can be approximated accurately by a finite Taylor series expansion

$$\begin{aligned} H_{leakage}(z) &= \left.\frac{V_m(z)}{Q_1(z)}\right|_{\substack{U_1(z)=0 \\ Q_2(z)=0}} \qquad (3.20)\\ &= A_0 + A_1\left(1-z^{-1}\right) + A_2\left(1-z^{-1}\right)^2 + \ldots + A_M\left(1-z^{-1}\right)^M \end{aligned}$$

where the coefficients $A_0 \ldots A_M$ are a function of the DC opamp gain A_{DC} and the relative capacitor error Δ_C. The filtering effect of the $(1-z^{-1})^i$ depends on the oversampling ratio OSR. To estimate the order of magnitude of the noise leakage, its first five coefficients $A_0 \ldots A_4$ were calculated for the standard cascaded 2-0 delta-sigma ADC (Fig. 3.2) based on the real integrator model described by (3.17) [29]:

$$A_0 = \delta p_1 \delta p_2 = \frac{a_1 a_2}{A_{DC}^2} \tag{3.21}$$

$$A_1 = -\delta p_1 - \delta p_2 = \frac{a_1 + a_2}{A_{DC}} \tag{3.22}$$

$$\begin{aligned} A_2 &= -\delta a_1 - \delta a_2 - \delta b_1 + 3\delta p_1 + \delta p_2 - \delta\alpha \\ &= 4\Delta_C + \frac{-2a_1 + b_1 + \alpha + 4}{A_{DC}} \end{aligned} \tag{3.23}$$

$$\begin{aligned} A_3 &= 2\delta a_1 + 2\delta b_1 - 2\delta b_2 - 3\delta p_1 + \delta p_2 \\ &= -2\Delta_C + \frac{a_1 - a_2 - 2b_1 + 2b_2 - 2}{A_{DC}} \end{aligned} \tag{3.24}$$

$$\begin{aligned} A_4 &= -\delta a_1 + \delta a_2 - \delta b_1 + 2\delta b_2 + \delta p_1 - \delta p_2 + \delta\alpha - \frac{\beta}{a_1 a_2 \alpha}\delta\beta \\ &= \left(\frac{\beta}{a_1 a_2 \alpha} - 2\right)\Delta_C + \left(b_1 - 2b_2 + \alpha + \frac{\beta(1+\beta)}{a_1 a_2 \alpha} - 2\right)\frac{1}{A_{DC}} \end{aligned} \tag{3.25}$$

Assuming $A_{DC} = 54$ dB and $\Delta_C = 0.8\%$, the order of magnitude of A_0 is 10^{-6} and of $A_1 \ldots A_4$ is $10^{-3} \ldots 10^{-2}$. It can be observed from (3.21)–(3.25) that the first two terms (A_0 and A_1) depend only on the finite opamp gain and, in addition, A_0 seems to be negligibly small.

The noise leakage for the general cascaded 2-0 delta-sigma ADC (Fig. 3.5) could be calculated in the same way, but we did not perform these calculations. A symbolic calculator provided by Mathematica or Maple should be invoked to perform this analysis. In Section 4.1 will be demonstrated that even a very accurate

estimation of $A_0 \ldots A_M$ has low significance because of the random nature of the variables A_{DC} and Δ_C.

However, we did analyze the noise leakage by simulations and some results are presented in Fig. 3.12. The spectrum $Q_1(z)$ of the first-stage quantization error $q_1[n]$ is not a white noise, but it is strongly correlated with the input signal, and it is affected by pattern noise as well, as it was expected for $N_1 = 1.5$ bits. After this quantization error $q_1[n]$ is quantized by the second stage, which randomizes it, $v_q[n]$ looks whiter than $q_1[n]$, but the pattern noise is still present. The second stage is a multibit quantizer with $N_2 = 10$ bits, so the spectrum $Q_2(z)$ of the second-stage quantization error $q_2[n]$ can be considered a nearly white noise, as it was presented in Fig. 2.5 also.

The performance of an ideal switched-capacitor cascaded delta-sigma ADC, for which no analog circuit imperfections were assumed, is only limited by the $\frac{kT}{C}$-noise and the power of the shaped second-stage quantization noise $(1-z^{-1})^2\,Q_2(z)$, if certain OSR was assumed ($V_{m_{ideal}}(z)$ in Fig. 3.12). Unfortunately, this noise curve degrades significantly due to the analog circuit imperfections. This is illus-

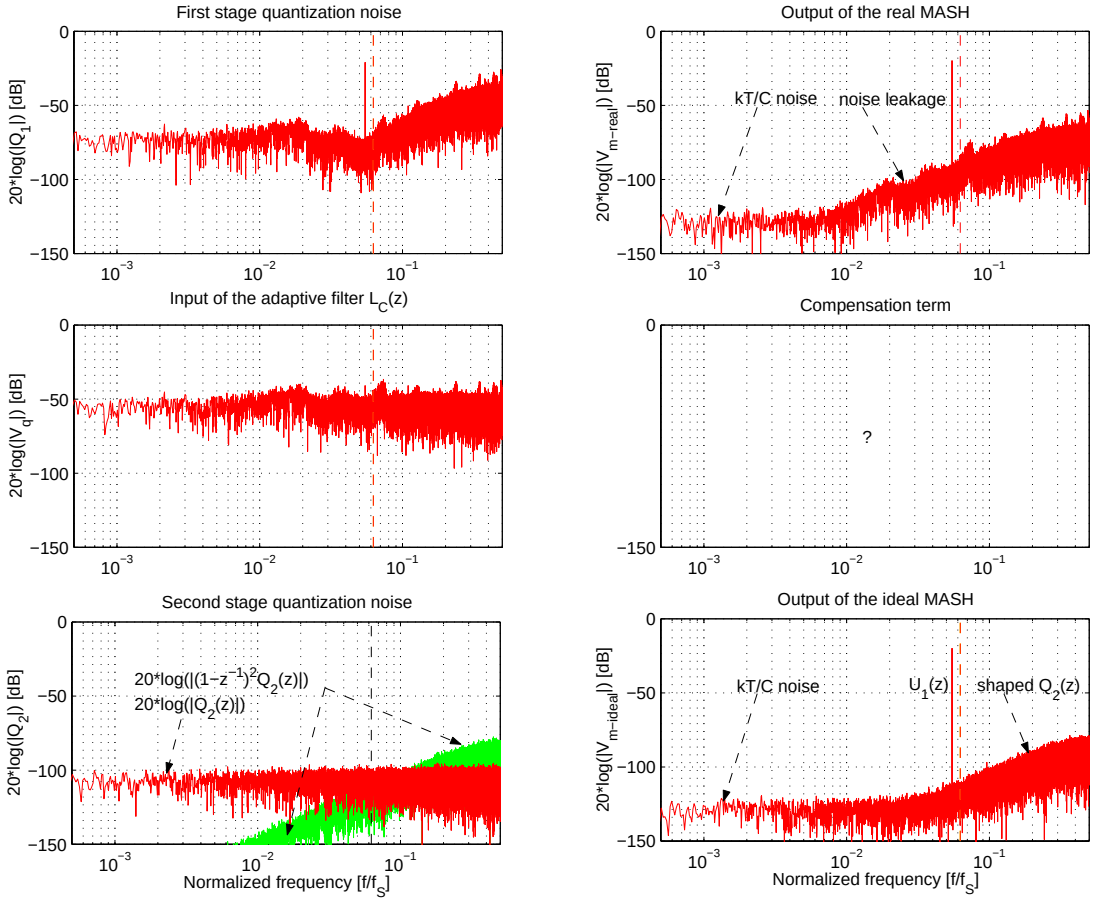

Figure 3.12: Noise leakage in the general cascaded 2-0 delta-sigma ADC ($OSR = 8$, $N_1 = 1.5$ bits, $N_2 = 10$ bits, $A_u = 0.1$ V, $\Delta_C = 0.8\%$, $A_{DC} = 54$ dB and $N\left(\frac{kT}{C}\right) = -92$ dB)

trated by the spectrum $V_{m_{real}}(z)$ of the output $v_m[n]$ of a real MASH. It can be observed that $V_{m_{real}}(z)$ is mainly composed by the noise leakage which has a much bigger power than the shaped second-stage quantization noise $(1-z^{-1})^2\,Q_2(z)$, so the noise leakage limits the performance of the circuit. In addition, $V_{m_{real}}(z)$ looks like a shaped version of $Q_1(z)$, and even the pattern noise is preserved. This demonstrates that the output of the real MASH is highly correlated with the first-stage quantization noise $Q_1(z)$, that is, the origin of the noise leakage is clearly the first-stage quantization noise $Q_1(z)$. In other words, (3.19) is intuitively verified by Fig. 3.12. In addition, one should note that the ideal output $V_{m_{ideal}(z)}$ of the MASH is smooth and free of this pattern noise, which is another great advantage of cascaded delta-sigma modulators.

The only question which remained open: how to change a practical MASH to reach, or at least to get close to, its ideal performance? One possible answer, an effective adaptive digital compensation method, will be presented in the next chapter.

3.3 Conclusions

Cascaded delta-sigma ADCs are suitable for high-resolution and large-bandwidth applications so their analysis presents a high interest in the ADC-design community. Two main issues in dealing with cascaded delta-sigma modulators are to choose an appropriate structure, and to handle the side-effects of the analog circuit imperfections.

First, cascaded delta-sigma ADCs with 1–1.5-bit first stage and 10–12-bit second stage were investigated from structural point of view. The most critical point in this structure is to prevent the second stage from overloading without drastically scaling down its input signal. It was found that by carefully adjusting the interstage coefficients of the MASH, an optimal weighting of the input and the output of the first-stage quantizer in the formation of the second-stage input can be achieved. In addition, using a tri-level quantizer in the first stage extends the dynamic range of the MASH. In conclusion, based on a comparative analysis, it is believed that the cascaded 2-0 delta-sigma structure was optimized for peak-SNR performance, if $N_1 = 1.5$ bits, $a_1 = \frac{1}{4}$, $a_2 = \frac{1}{2}$, $b_1 = 1$, $b_2 = \frac{1}{2}$, $\beta = 2$, $m_1 = -1$, $m_0 = \frac{1}{2}$ and $m_2 = 2$ were used. The ideal peak-SNR performance of the optimized structure [18] (without considering the $\frac{kT}{C}$-noise and, in addition, assuming ideally matched coefficients) showed a 2-bit improvement compared the previous results [17], [31].

It was also shown that the obtained peak SNR of the ideal MASH is too sensitive, and the actual MASH implemented by practical analog circuits, with their natural imperfections, would have a much worse SNR performance. These non-idealities cause quantization noise leakage and performance degradation. Therefore, the nature of the noise leakage was analyzed analytically and by simulations. Based on these results, an effective adaptive noise-leakage digital compensation method was developed, which will be presented in the next chapter.

Chapter 4

Adaptive Digital Compensation for Cascaded 2-0 Delta-Sigma ADCs

The main drawback of cascaded delta-sigma modulators is their high sensitivity to analog circuit imperfections which leads to noise leakage, and significant loss of SNR performance. To reduce the influence of the noise leakage in cascaded delta-sigma modulators, three measures can be applied:

1. **Highly accurate analog circuits** ($NTF_1(z) \longrightarrow NTF_{1d}(z)$)

   - ◇ *method:* to reduce the mismatch between the analog and digital circuits (especially between the analog noise transfer function $NTF_1(z)$ and its digital counterpart $NTF_{1d}(z)$), and, in turn, to reduce the noise leakage by increasing the analog circuit accuracy by using special technology (for example, correlated double sampling and laser trimming);
   - ◇ *limitation:* this is possible only to a limited degree, and, in addition, it increases the production costs.

2. **Multibit quantizer** ($|PSD(Q_1)| \downarrow$)

   - ◇ *method:* to reduce the power of the first-stage quantization noise, and, in turn, to reduce the noise leakage by using multibit quantizer in the first stage;
   - ◇ *limitation:* this is effective only to a limited degree, and, in addition, the linearity of the multibit DAC in the feedback path is critical;
   - ◇ *solution:* either trimming the multibit feedback DAC (high production costs), or using mismatch-shaping DAC (low production costs, but it requires a rather big chip area), or using other analog or digital correction methods for the DAC (still under development).

3. **Digital noise-leakage compensation** ($NTF_1(z)$=$NTF_{1d}(z)$+$L_C(z)$)

- ◇ *method:* to adjust the digital compensation filter $NTF_{1d}(z)$ to match exactly its analog counterpart $NTF_1(z)$, and thus eliminate the noise leakage;
- ◇ *limitation:* the required robustness and hardware complexity of the digital compensation;
- ◇ *solution:* using adaptive noise-leakage cancellation.

In the present work, the last method was chosen and has been explored. The adjustment between the digital and analog filters should happen automatically and preferably on-line, such that variations due to changes in production process parameters as well as effects of drift and aging are eliminated also. In conclusion, adaptive on-line digital compensation was chosen, which offers a potentially powerful solution to reduce the noise-leakage problem. Using this technique, it will be demonstrated in this chapter that a practical MASH can approach the performance of an ideal MASH modulator.

4.1 Adaptive Digital Compensation of the Noise Leakage

In the expression (3.20) for the noise-leakage transfer function $H_{leakage}(z)$, the output errors introduced by the terms $A_i(1-z^{-1})^i$ decrease rapidly with the order i of the term. This shows that the effect of the analog imperfections can be suppressed by incorporating in the structure a simple low-order digital correction path for the quantization error $q_1[n]$ which cancels the quantization-noise leakage signal.

This digital correction can be provided by an adaptive noise-leakage compensation digital FIR filter $L_C(z)$ (Fig. 4.1), which adds a digital correction term $v_L[n]$ to the output $v_C[n]$ of the digital compensation filter $NTF_{1d}(z)$. Therefore, the digital correction term $v_L[n]$, which is the output of the digital FIR filter $L_C(z)$, should be a negative estimate of the noise leakage [29]. Note that we call $NTF_{1d}(z)$ a "digital compensation filter", which cancels the first-stage quantization noise $Q_1(z)$ in the global output $V_m(z)$ of the cascaded delta-sigma ADC if perfect analog circuits are assumed, and we call $L_C(z)$ as "adaptive noise-leakage digital compensation filter" or, shortly, "adaptive (compensation) filter", which is needed to compensate for the noise leakage present in the global output $V_m(z)$ of the MASH due to the analog circuit imperfections.

To understand how this noise-leakage compensation scheme works, first one should analyze the origin of its input signal $V_q(z)$. Based on the linearized model of the cascaded ADC one can recall (3.11) here for convenience:

$$V_q(z) = -Q_1(z) + m_2\, Q_2(z) \cong -Q_1(z), \tag{4.1}$$

that is, $V_q(z)$ is mainly composed by the negative of the first-stage quantization noise $Q_1(z)$, because the power of $Q_2(z)$ is negligibly small compared to the

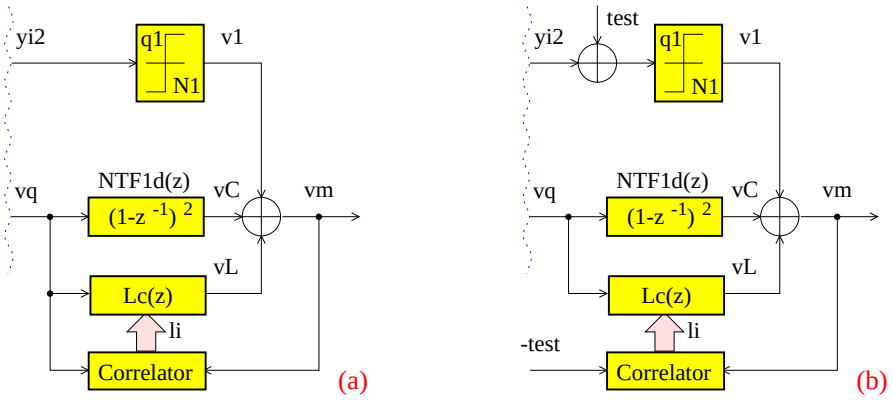

Figure 4.1: Adaptive digital noise-leakage compensation (a) without and (b) with a test signal $test[n]$

power of $Q_1(z)$ in the frequency band of interest. Therefore, for a FIR filter $L_C(z)$ (Fig. 4.1),

$$V_L(z) = V_q(z)\, L_C(z) \cong -Q_1(z)\,(l_0 + l_1 z^{-1} + l_2 z^{-2} + \ldots + l_{M-1} z^{-(M-1)}), \quad (4.2)$$

where the noise-leakage compensation digital FIR filter $L_C(z)$ has M coefficients $\overrightarrow{l} = [l_0, l_1, \ldots l_{M-1}]^T$. The relation (4.2) compared with (3.19) and (3.20) demonstrates that $V_L(z)$ can be a negative estimate of the noise leakage, if the coefficients $\overrightarrow{l}$ of the FIR filter $L_C(z)$ are chosen properly. The coefficients $A_0 \ldots A_M$ of the noise leakage transfer function $H_{leakage}(z)$ can be calculated with good accuracy as functions of A_{DC} and Δ_C, so the coefficients $\overrightarrow{l}$ could in principle be determined also [63], [64]. However, an accurate *a priori* estimation of $A_0 \ldots A_M$ is not possible, because of the random nature of the variables A_{DC} and Δ_C, so the calculated $H_{leakage}(z)$ would be only a coarse estimate of the real one. An accurate evaluation is necessary, because of the high sensitivity of the SNR performance to these values, so a relatively small error in the coefficients $A_0 \ldots A_M$, and in turn of $\overrightarrow{l}$, would cause significant performance degradation. This observation was the main reason why only the nature and the order of magnitude of the noise leakage was derived in Section 3.2.2. In conclusion, a FIR filter, with adaptively tuned coefficients $\overrightarrow{l}$, offers a good solution to cancel the noise leakage.

4.1.1 Adaptive Digital Compensation Algorithms

As mentioned in the previous sections, the coefficients of the noise-leakage compensation digital filter $L_C(z)$ are adjusted through an adaptive algorithm. There are various algorithms available for adaptive FIR digital filtering. One of the well-known adaptive algorithm developed using the stochastic gradient technique, the Widrow-Hoff least-mean-square (LMS) algorithm, is being widely used because of its relatively simple realization [65]. Several block FIR adaptive algorithms have been introduced, including the block-least-mean-square (BLMS) algorithms,

where the system signals are processed in blocks [66]. Various applications of adaptive techniques in data converters can be found in [67], [68], [69], [70]. Active noise control also uses adaptive digital signal processing in order to generate a noise of equal amplitude but opposite phase (also called as "antinoise") to cancel out the unwanted noise [71] — a method somewhat similar to that used in this thesis to reduce the quantization noise leakage.

For random input signals the LMS algorithm minimizes the functional $\mathcal{J}[n] = \mathcal{E}\{e^2[n]\}$, where $e[n]$ is the error signal itself or an appropriate function of the error signal. Minimization of $\mathcal{J}[n]$ is achieved in the LMS algorithm by estimating the gradient of $\mathcal{J}[n]$ and updating the coefficients $\overrightarrow{l}$ of the adaptive filter according to this estimate. In our case, the error is the unwanted presence of the first-stage quantization noise $q_1[n]$ in the output $v_m[n]$ of the cascaded delta-sigma ADC. Therefore, the output $v_m[n]$ is an appropriate function of the effective error signal $q_1[n]$, so it can be considered $e = v_m = f_m\{q_1\}$. Note that $v_m[n]$ contains the input signal $u_1[n]$ as well as the second-stage quantization noise $q_2[n]$, so $v_m = f_m\{u_1, q_1, q_2\}$, but for a functional description of the system, let us first assume $u_1[n] = 0$ and $q_2[n] = 0$. The gradient of $\mathcal{J}[n]$ at the time instance n can be calculated as

$$\nabla\mathcal{J}[n] = \frac{\partial\mathcal{E}\{e^2[n]\}}{\partial\overrightarrow{l}} = \frac{\partial\mathcal{E}\{v_m^2[n]\}}{\partial\overrightarrow{l}} = 2\,\mathcal{E}\{v_m[n]\,\overrightarrow{q_1}[n]\} \tag{4.3}$$

where $\overrightarrow{q_1}[n] = [q_1[n], q_1[n-1], \ldots q_1[n-(M-1)]]^T$. Because it is necessary to calculate actually this estimate of $\nabla\mathcal{J}[n]$, one has to get an estimate of the first-stage quantization noise $q_1[n]$. This is not a difficult task, because from (4.1), $V_q(z) \cong -Q_1(z)$, so in the multiplication from (4.3), $-v_q[n]$ should be used instead of $q_1[n]$ (Fig. 4.1.a). However, we will keep using $q_1[n]$ in the equations in order to illustrate the principle of first-stage quantization noise $q_1[n]$ cancellation. In addition, since we cannot only simply calculate the expectation in (4.3), the LMS algorithm uses an approximation for the gradient of $\mathcal{J}[n]$, the so-called noisy gradient estimate:

$$\nabla\mathcal{J}[n] \approx 2\,v_m[n]\,\overrightarrow{q_1}[n]. \tag{4.4}$$

This estimate leads to the update equation of the LMS algorithm

$$\overrightarrow{l}[n+1] = \overrightarrow{l}[n] + \gamma_{LMS}\,v_m[n]\,\overrightarrow{q_1}[n], \tag{4.5}$$

where $2M$ multiplications and M additions are needed for each update, and the convergence is controlled be the LMS adaptation constant γ_{LMS} [29]. Because the noisy gradient estimate is not an accurate estimate of the real gradient of $\mathcal{J}[n]$, the adaptation coefficient γ_{LMS} has to be very small in order to keep the steady-state error low. Low values for the adaptation coefficient γ_{LMS} require a lengthy adaptation process, and a high resolution for the noise-leakage compensation filter $L_C(z)$ coefficients $\overrightarrow{l}$, resulting in increased hardware complexity. It is advantageous to change the algorithm in order to keep reasonably low resolution for the coefficients $\overrightarrow{l}$.

This can be achieved without significant increase in complexity by using the block-least-mean-square (BLMS) algorithm instead [66]. The BLMS algorithm operates similarly, except that the gradient of $\mathcal{J}[n]$ is estimated by an average over K samples, resulting in a more accurate gradient estimate than the noise gradient, so it allows larger values for γ_{BLMS}. The BLMS gradient estimate for the time instance $n = jK$ is

$$\nabla\mathcal{J}[jK] = \frac{\partial\mathcal{E}\{e^2[jK]\}}{\partial\overrightarrow{l}} \cong \frac{2}{K}\sum_{k=0}^{K-1} v_m[jK-k]\,\overrightarrow{q_1}[jK-k], \tag{4.6}$$

and the update equation of the BLMS algorithm is given by

$$\overrightarrow{l}[(j+1)K] = \overrightarrow{l}[jK] + \gamma_{BLMS}\sum_{k=0}^{K-1} v_m[jK-k]\,\overrightarrow{q_1}[jK-k], \tag{4.7}$$

requiring a convolution over K samples for each filter coefficient update. The complexity seems to be much higher than it was for the LMS algorithm, but as will be shown in Section 4.1.3, it can be drastically reduced.

4.1.2 Test-Signal Approach

As presented in the previous section, the coefficients $\overrightarrow{l}$ of the noise-leakage compensation digital FIR filter $L_C(z)$ should be tuned by the adaptive algorithm in such a way that the first-stage quantization noise $q_1[n]$ gets cancelled in the global output $v_m[n]$ of the MASH. An estimate of the first-stage quantization error $q_1[n]$ is provided by $-v_q[n]$, as shown in (4.1), so the result of the correlation between $v_m[n]$ and $v_q[n]$ could give the required information on how to tune the coefficients $\overrightarrow{l}$ in order to reduce, and finally minimize, the power of $q_1[n]$ in $v_m[n]$ (Fig. 4.1.a). However, in a real cascaded delta-sigma ADC, $v_q[n]$ provides only a coarse estimate of the first-stage quantization noise $q_1[n]$, and due to the analog circuit imperfections, $v_q[n]$ always contains an attenuated component of the input signal $u_1[n]$ in addition to the second-stage quantization noise $q_2[n]$, that is, $v_q = f_q\{q_1, q_2, u_1\}$. As mentioned earlier, the global output of the MASH is also a function of the same variables: $v_m = f_m\{u_1, q_1, q_2\}$. Therefore, the compensation algorithm, which tries to reduce the power of $q_1[n]$ from $v_m[n]$ based on the correlation result between $v_q[n]$ and $v_m[n]$, would reduce not only the quantization noise $q_1[n]$, but also the input signal $u_1[n]$ from $v_m[n]$. This property, the so-called signal-to-noise inversion principle, unfortunately, is a limiting factor for the adaptation algorithm discussed so far, if on-line adaptation is applied.

This problem, however, can be solved if a test signal $test[n]$ is entered into the modulator at its most insensitive node, that is, before the first-stage quantizer (Fig. 4.1.b) [27], [28]. The test signal $test[n]$ chosen is a pseudo-random, uniformly distributed, zero-mean white noise, which is added where the quantization noise is generated, and which behaves similarly to the quantization noise $q_1[n]$ itself. In addition, the test signal is uncorrelated with the input signal $u_1[n]$, or with the quantization noises $q_1[n]$ and $q_2[n]$. Since the test signal $test[n]$ follows

the same parasitic leakage path toward the output $v_m[n]$ as the quantization noise $q_1[n]$, removing the test signal $test[n]$ from the output $v_m[n]$ requires the same operation as removing the remainder of the first quantizer's quantization error $q_1[n]$ from the output $v_m[n]$. In other words, the minimization of the test signal $test[n]$ in the output $v_m[n]$ is equivalent to the minimization of the quantization noise leakage.

Note that a pseudo-noise or a pseudo-random sequence, is a binary sequence with an autocorrelation that resembles, over a period, the autocorrelation of a random binary sequence. It also resembles the autocorrelation of band-limited white noise. Although deterministic, so it can be reproduced, a pseudo-noise sequence has many characteristics that are similar to those of random binary sequences, such as having a nearly equal number of zeros and ones ('0' logic and '1' logic), very low correlation between shifted versions of the sequence, very low cross-correlation between any two sequences, etc. A pseudo-random sequence is usually generated using sequential logic circuits and it is also called maximal-length sequence [72, Section 5.10.1].

When injecting the test signal $test[n]$ into the modulator, based on the linearized model of the general cascaded delta-sigma ADC (Fig. 3.6), (3.19) changes to

$$V_{m_{real}}(z) = z^{-2}U_1(z) + m_2(1-z^{-1})^2Q_2(z) + H_{leakage}(z)(k_1\,Test(z) + Q_1(z)), \tag{4.8}$$

so $v_m = f_m\{u_1, q_1, test, q_2\}$. Even though the test signal $test[n]$ has statistical properties similar to those of band-limited white noise, it is deterministic and fully known. Therefore, it can be detected in the output $v_m[n]$ by using a correlation process between the output $v_m[n]$ and the digital replica of the test signal $test[n]$ (Fig. 4.1.b) which generates an error signal. This error signal is then used to update the coefficient vector $\overrightarrow{l}$ by a gradient method such as the BLMS algorithm. The update equation of the BLMS algorithm (4.7) using the test signal $test[n]$ for adaptation becomes

$$\overrightarrow{l}[(j+1)K] = \overrightarrow{l}[jK] - \gamma_{BLMS}\sum_{k=0}^{K-1} v_m[jK-k]\,\overrightarrow{test}[jK-k], \tag{4.9}$$

where $q_1[n]$ (in fact, $-v_q[n]$!) was replaced by the negated test signal $-test[n]$. The detailed form of the update equation of the BLMS adaptation algorithm (4.9) is given by

$$\begin{aligned}
l_0[(j+1)K] &= l_0[jK] - \gamma_{BLMS}\sum_{k=0}^{K-1} v_m[jK-k]\,test[jK-k] \qquad (4.10)\\
l_1[(j+1)K] &= l_1[jK] - \gamma_{BLMS}\sum_{k=0}^{K-1} v_m[jK-k]\,test[jK-k-1]\\
&\cdots \qquad \cdots\\
l_{M-1}[(j+1)K] &= l_{M-1}[jK] - \gamma_{BLMS}\sum_{k=0}^{K-1} v_m[jK-k]\,test[jK-k-(M-1)]
\end{aligned}$$

The detailed structure of an adaptive digital compensated general cascaded 2-0 delta-sigma ADC is presented in Fig. 4.2. It implements (4.9) and (4.10).

Note that the error correction using the test signal $test[n]$ takes place on-line, in the background during the actual data conversion, so it can follow any drift introduced e.g. by aging or temperature changes. Also, the test signal acts as a dither signal for the first stage of the cascaded delta-sigma modulator, thus improving its performance [38, Chapter 3].

A minor drawback of using test-signal injection is a slight loss in the dynamic range DR due to the earlier overflow of the first-stage quantizer (details in Sections 4.2.0 and 4.2.2). Finally, note that the proposed test-signal approach is a linear correction method, so it can be used for correcting linear errors only, but not any harmonic distortion introduced by the nonlinear implementation of the analog circuitry [21].

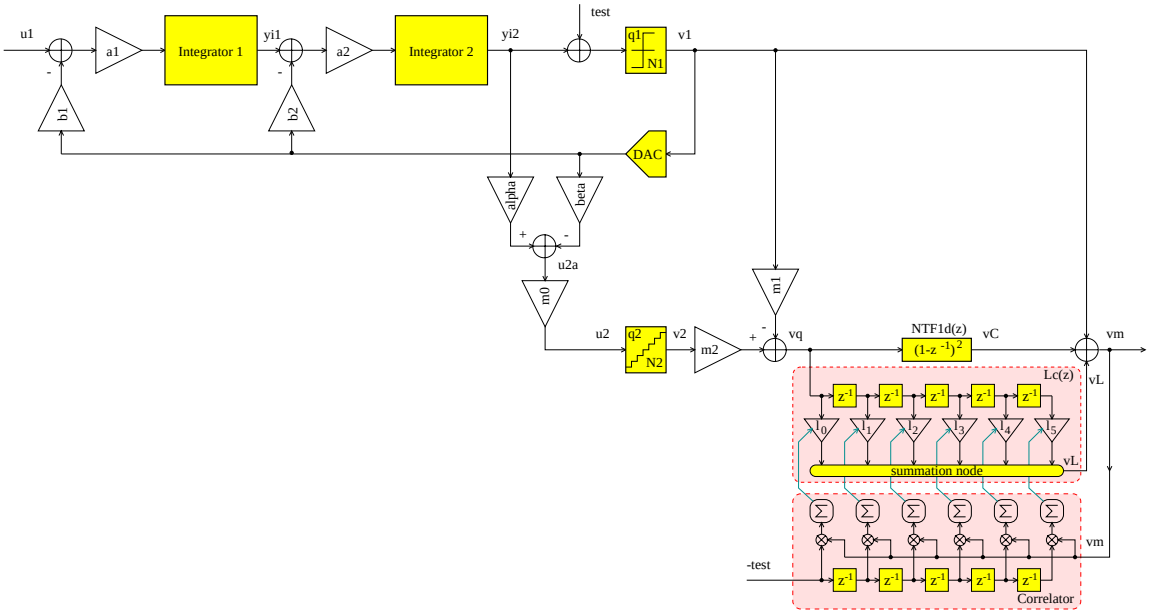

Figure 4.2: Adaptive digital noise-leakage compensation scheme using a test signal $test[n]$ for the general cascaded 2-0 delta-sigma ADC ($M = 6$)

4.1.3 Hardware Implementation of the Adaptive Filter

The adaptive digital compensation method shown so far presents a practical possibility for designing high-performance ADCs only if the adaptive noise-leakage compensation digital filter $L_C(z)$ can be implemented with reasonably simple digital circuitry, which can be integrated in the same chip with the modulator without significantly increasing its complexity. Usually besides large bandwidth and high resolution, low power and small chip area are also desired. In other words, the complexity of the adaptive filter is an important issue, and we are trying to reduce its complexity without significant performance loss.

First of all, one can reduce the complexity of the convolution operations if the test signal is chosen to be a binary sequence [29]. The additional advantage of using a binary test signal is that the analog test signal, which is injected before the quantizer, can be reproduced with a very high accuracy by its digital counterpart, which is used at the input of the correlator (Figs. 4.1.b and 4.2). Hence the convolution operation is reduced to a simple summation of K samples of the output signal, where the sign of the summation is changed according to the sign of the test signal $test[n]$. The resulting sign-block-least-mean-square (SBLMS) algorithm updates the coefficients $\overrightarrow{l}$ according to

$$\overrightarrow{l}[(j+1)K] = \overrightarrow{l}[jK] - \gamma_{SBLMS} \sum_{k=0}^{K-1} v_m[jK-k] \operatorname{sign}\left\{\overrightarrow{test}[jK-k]\right\}. \quad (4.11)$$

The adaptation requires K additions, and M multiplications with the adaptation constant γ_{SBLMS}. The cost of using this simplified algorithm is a much longer convergence time. However, the convergence speed does not matter much in online adaptation if the converged performance is accurate enough.

In order to reduce the hardware complexity further, the coefficient update can be performed as a simple addition with a constant step size γ_{SSBLMS}, which sign is controlled by the sign of the gradient estimate [31]:

$$\overrightarrow{l}[(j+1)K] = \overrightarrow{l}[jK] - \gamma_{SSBLMS} \operatorname{sign}\left\{\sum_{k=0}^{K-1} v_m[jK-k] \operatorname{sign}\left\{\overrightarrow{test}[jK-k]\right\}\right\}, \quad (4.12)$$

so the M multiplications with the adaptation constant γ_{SSBLMS} can be replaced by up-down counting operations instead, which are easy to implement, if γ_{SSBLMS} is chosen to be equal with the step size (1 LSB) of the adaptive filter's coefficients $\overrightarrow{l}$. This algorithm, which update equation was expressed by (4.12), can be called as sign-sign-block-least-mean-square (SSBLMS). In conclusion, every update requires KM additions. Since the update is performed after each K samples, only M additions per sample are required.

The hardware implementation of such an adaptive compensation filter is presented in Fig. 4.3 [17]. The estimated die size of this adaptive digital logic is 0.57 mm^2 in a 0.25 μm standard CMOS process. It allows high-speed operation.

4.2 Adaptive Digital Compensation Process

The functionality of the adaptive general cascaded 2-0 delta-sigma ADC (Fig. 4.2) was verified by extensive simulations. The analog circuit imperfections were modeled by (3.17). The same nonidealities were considered for the analog gain factors α, β and m_0. First, the adaptive noise-leakage compensation digital filter $L_C(z)$ was built from an $M-1 = 5^{th}$ order FIR filter [17]. For adaptively controlling its coefficients $\overrightarrow{l}$, a binary, pseudo-random, uniformly-distributed, zero-mean and white test signal $test[n]$ was used with amplitude $A_t = 0.05$ V. In

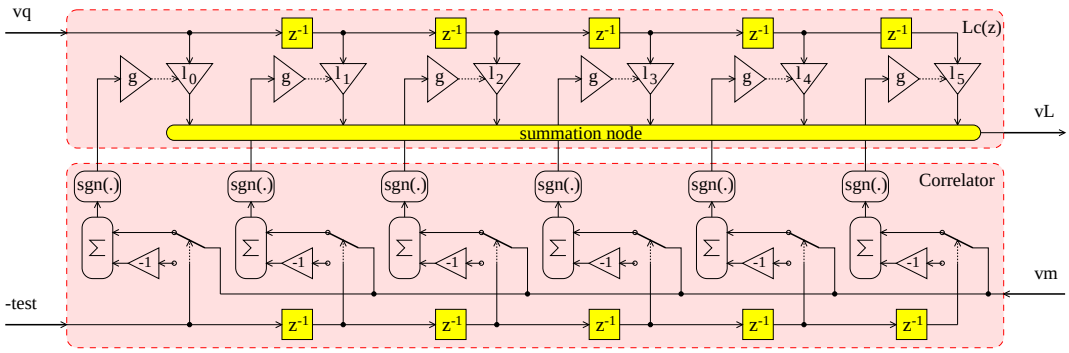

Figure 4.3: Simplified hardware implementation of the correlator using a binary test signal $test[n]$ to update the coefficients l_i of the adaptive noise-leakage compensation digital filter $L_C(z)$ ($g = \gamma_{SSBLMS}$ and $M - 1 = 5$)

addition, the SSBLMS algorithm, (4.12), with a block size of $K = 2^{14}$ and with $\gamma_{SSBLMS} = 4\,10^{-5}$, was used to update the coefficients $\overrightarrow{l}$.

Some simulation results are presented in Fig. 4.4 which demonstrate the adaptive noise-leakage cancellation, because the compensated output has reached the ideal performance at several time instances j, so the noise leakage was effectively suppressed. Due to the fluctuations in the coefficients $\overrightarrow{l}$ (not presented in Fig. 4.4) the compensated performance, that is, the overall MASH performance also fluctuates with a ripple of about 10 dB, which is unacceptably large. In addition, the dynamic range of the compensated output is reduced with about 3 dB in comparison with the dynamic range of the ideal output. To improve the performance presented in Fig. 4.4, the parameters of the adaptive digital filter and of the adaptive noise-leakage cancellation algorithm were carefully studied and optimized. In addition, the properties of the test signal $test[n]$ were studied.

The simulation results presented in Fig. 4.4 can be improved. In on-line adaptation one can tolerate a longer convergence time, but the ripple of the adaptation noise (steady-state error) should definitely be reduced, and the dynamic range should be extended as much as possible. In addition, the hardware complexity of the digital circuitry should be kept reasonable. In conclusion, one can trade lower adaptation speed for higher accuracy, and a very small performance drop for significantly lower digital hardware complexity.

4.2.1 Parameters for the Adaptive Digital Compensation Process

In general, the steady-state error of the adaptation process is directly proportional with the adaptation constant γ_{BLMS}, e.g. γ_{SSBLMS} used in (4.12), so a very low value is desirable for γ_{SSBLMS}. However, the smallest value of the adaptation constant γ_{SSBLMS} is limited by the maximum affordable resolution for the coefficients $\overrightarrow{l}$. A reasonably high resolution of $N_l = 16$ bits was chosen, which leads to $\gamma_{SSBLMS} = 1\ \text{LSB}_{N_l} = \frac{1}{2^{N_l}} \cong 1.5\,10^{-5}$ (for $\overrightarrow{l}$ limited between (-0.5;+0.5)).

Choosing a suitable block size K for the BLMS algorithm, or its SBLMS and

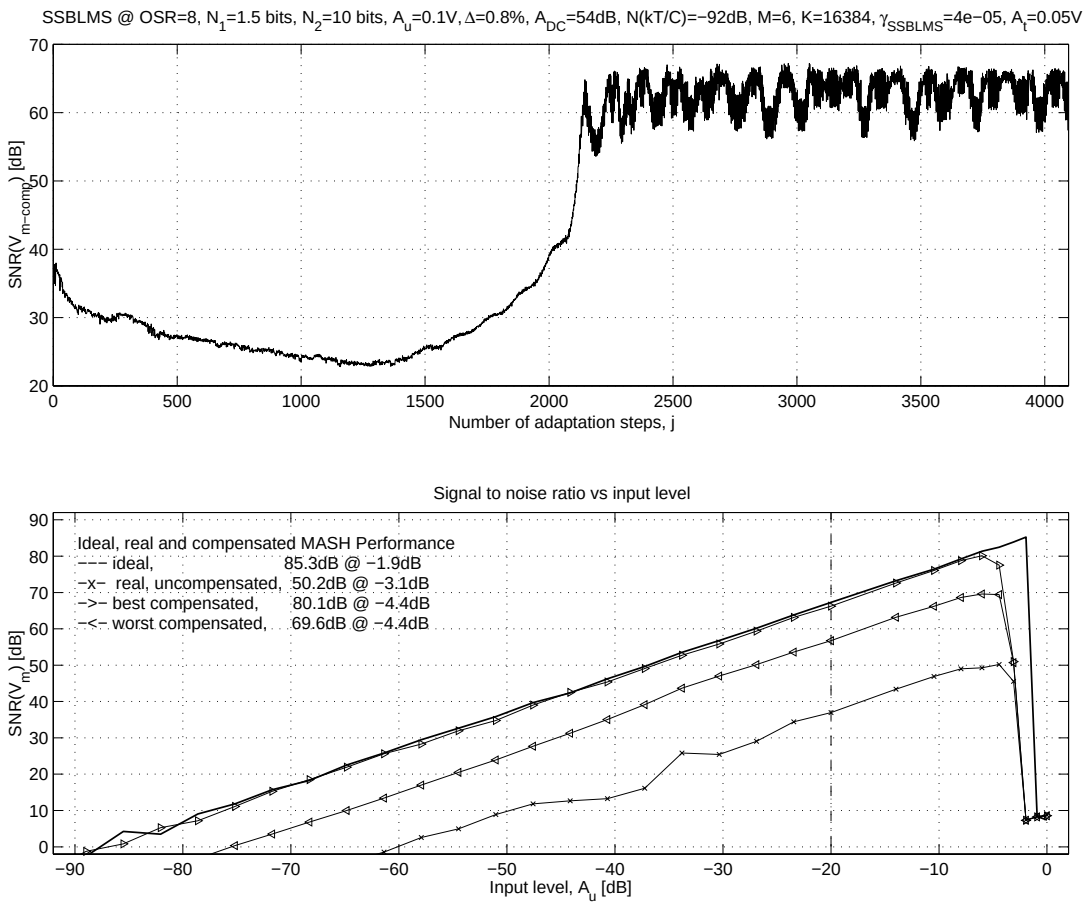

Figure 4.4: Adaptive compensation process and achieved SNR performance

SSBLMS derivatives, needs careful analysis. The gradient of the functional $\mathcal{J}[n]$ is calculated based on the correlation results between the test signal $test[n]$ and the global output $v_m[n]$ of the MASH, which is a function of $v_m = f\{u_1, q_1, test, q_2\}$. Ideally, the signals $u_1[n]$, $q_1[n]$ and $q_2[n]$ are uncorrelated with $test[n]$, and the influence is negligible when one correlates them. However, in BLMS algorithm, the correlation is performed only over a finite number of samples K. Hence, the correlation of $test[n]$ with each of the perturbing signals is not zero, and contributes a noise term to the result of the correlation [29]. These noise terms, should be small enough not to alter the sign of the correlation (in SSBLMS), or at least do it only rarely. The influence of $u_1[n]$, $q_1[n]$ and $q_2[n]$ is determined mainly by the length of the block size K, and it decreases with using a larger block size K. On the other hand, a larger block size K necessitates a larger accumulator (Fig. 4.3) to perform a long-term correlation. Based on simulation results, we have chosen for the block size $K = 2^{16}$, which provides a good estimate of $\nabla\mathcal{J}[n]$ with a good suppression of the unwanted, perturbing correlation terms, and, in addition, it requires only a moderately large accumulator.

In conclusion, with properly chosen adaptation constant $\gamma_{SSBLMS} = 1.5\,10^{-5}$ and block size $K = 2^{16}$, much better SNR performances were obtained than those

presented in Fig. 4.4: the ripple of the adaptation noise was reduced by about 4 dB with the acceptable price of a longer conversion time ($j \approx 6000$ adaptation steps instead of $j \approx 2000$), and a bigger accumulator ($K = 2^{16}$ instead of $K = 2^{14}$). The improved results are presented in Figs. 4.5, 4.6 and 4.7.

The progress of the adaptive compensation process is shown in Fig. 4.5, which demonstrates that the adaptive FIR filter $L_C(z)$ has reached its steady-state after $j \approx 6000$ adaptation steps. However, the coefficients $\overrightarrow{l}$ still fluctuate around their optimal values, which causes the 6-dB ripple of the compensated performance of $V_{m_{real}}(z)$. The adaptation process was performed assuming a single in-band sinewave input with an amplitude of $A_u = 0.1$ V.

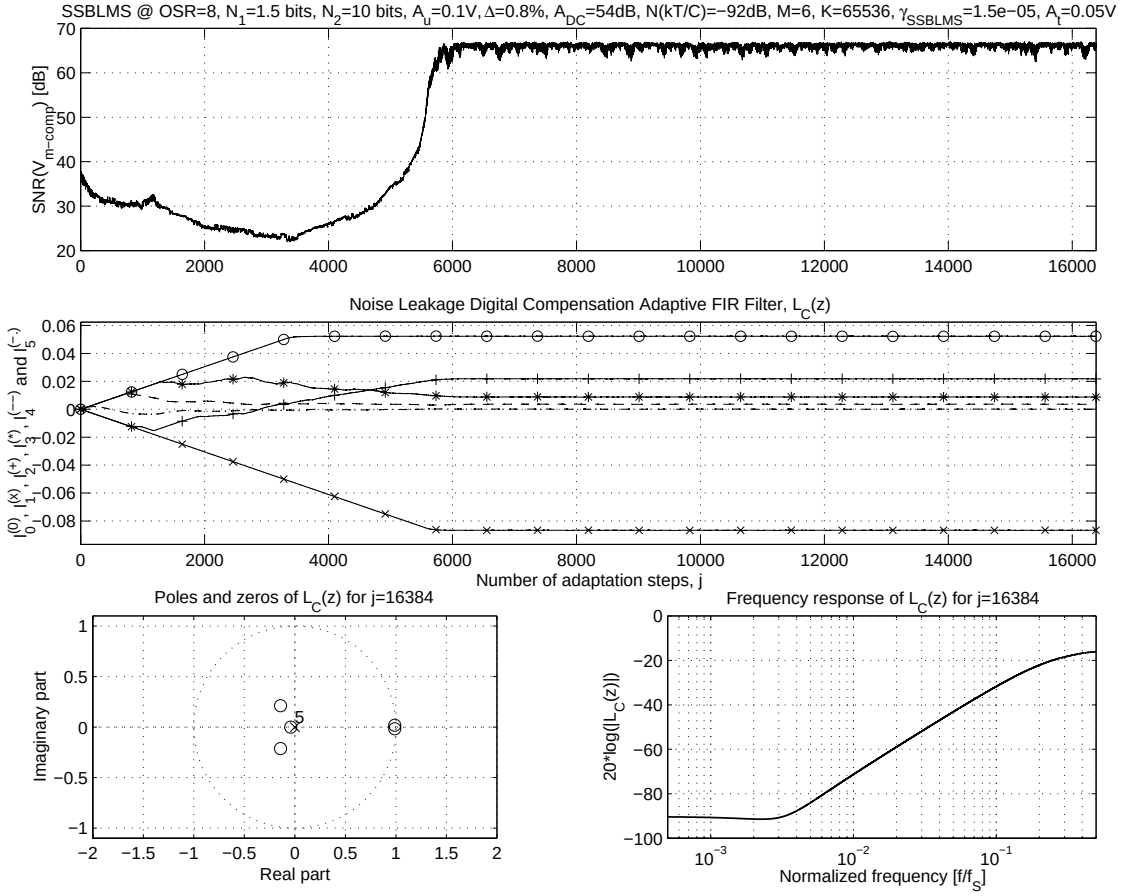

Figure 4.5: Adaptive compensation process ($K = 2^{16}$, $\gamma_{SSBLMS} = 1.5\,10^{-5}$)

Next, the output of the first stage $v_1[n]$ and the global output of the MASH $v_m[n]$ were analyzed in ideal and real, uncompensated and compensated situations (Fig. 4.6). The ideal curves for $SNR(V_1(z))$ and $SNR(V_{m_{ideal}}(z))$ match well those from Fig. 3.10. (Note that in general a resolution of 0.5 dB should be considered in these comparison.) However, the real curves for $SNR(V_{1_{real}}(z))$ and $SNR(V_{m_{real}}(z)) \equiv SNR(V_{m_{uncomp}}(z))$ significantly differ due to the test signal $test[n]$ injection. From (3.19) and (4.8) it follows that the test signal $test[n]$ will be present in the real and uncompensated output $V_{m_{real}}(z)$ due to the noise

leakage, modeled by its transfer function $H_{leakage}(z)$, and therefore it degrades the real and uncompensated SNR performance (Fig. 4.5) compared with the real SNR performance obtained when no test signal was applied (Fig. 3.10). Note that the SNR performance degradation of the real and uncompensated output $V_{m_{real}}(z)$ due to the test-signal injection does not matter at all, because the adaptive algorithm cancels from the output $V_m(z)$ the presence of the first-stage quantization noise $q_1[n]$ as well as the test signal $test[n]$. However, a real undesirable effect of injecting the test signal $test[n]$ is the dynamic range degradation by 2-3 dB, when $A_t = 0.05$ V, because the first and the second stages overload earlier. This degradation can be reduced by decreasing the amplitude of the test signal A_t (Section 4.2.2).

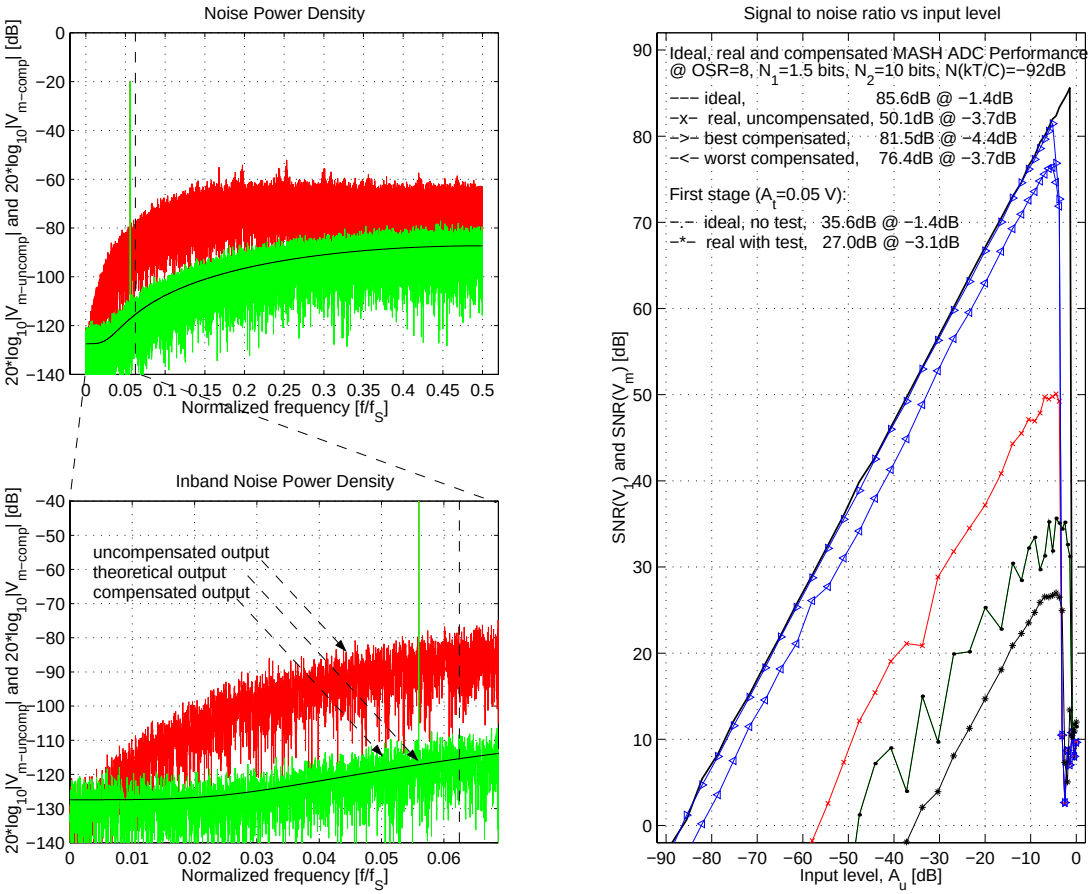

Figure 4.6: Achieved SNR performance ($K = 2^{16}$ and $\gamma_{SSBLMS} = 1.5\,10^{-5}$)

Finally, the results of the adaptation process were presented. In Fig. 4.6 (left) the compensated and uncompensated outputs were compared, and, as it is shown, the spectrum of the compensated output is pressed down near to the theoretical output. The resulting SNR performance is presented in Fig. 4.6 (right). In addition, Fig. 4.7 answers the question raised by Fig. 3.12, namely, what the compensation term looks like. The compensation term $V_L(z)$ is provided by the output of the adaptive noise-leakage compensation filter $L_C(z)$, whose input was $V_q(z)$.

Also, the shape of $V_L(z)$ looks very similar to that of $V_{m_{uncomp}}(z)$, which is mainly composed by the first-stage quantization noise leakage, so it can be concluded that $V_L(z)$ is the negative estimate of the quantization noise leakage indeed. It can be observed that the compensated output $V_{m_{comp}}(z)$ (Fig. 4.7) and the ideal output $V_{m_{ideal}}(z)$ (Fig. 3.12) are almost the same, which demonstrates the effectiveness of the compensation.

In addition, the dithering effect of the test signal $test[n]$ on the first stage quantization noise $q_1[n]$ is shown, i.e. the spectrum $Q_1(z)$ after applying the test signal (Fig. 4.7) is smoother than without it (Fig. 3.12). However, with this small dither signal provided by the $test[n]$, some idle tones and pattern noise are still present in $Q_1(z)$, and in turn in $V_q(z)$ and $V_{m_{uncomp}}(z)$, but these spurious noise components are eliminated by the compensation, and a smooth spectrum results for $V_{m_{comp}}(z)$ (Fig. 4.7).

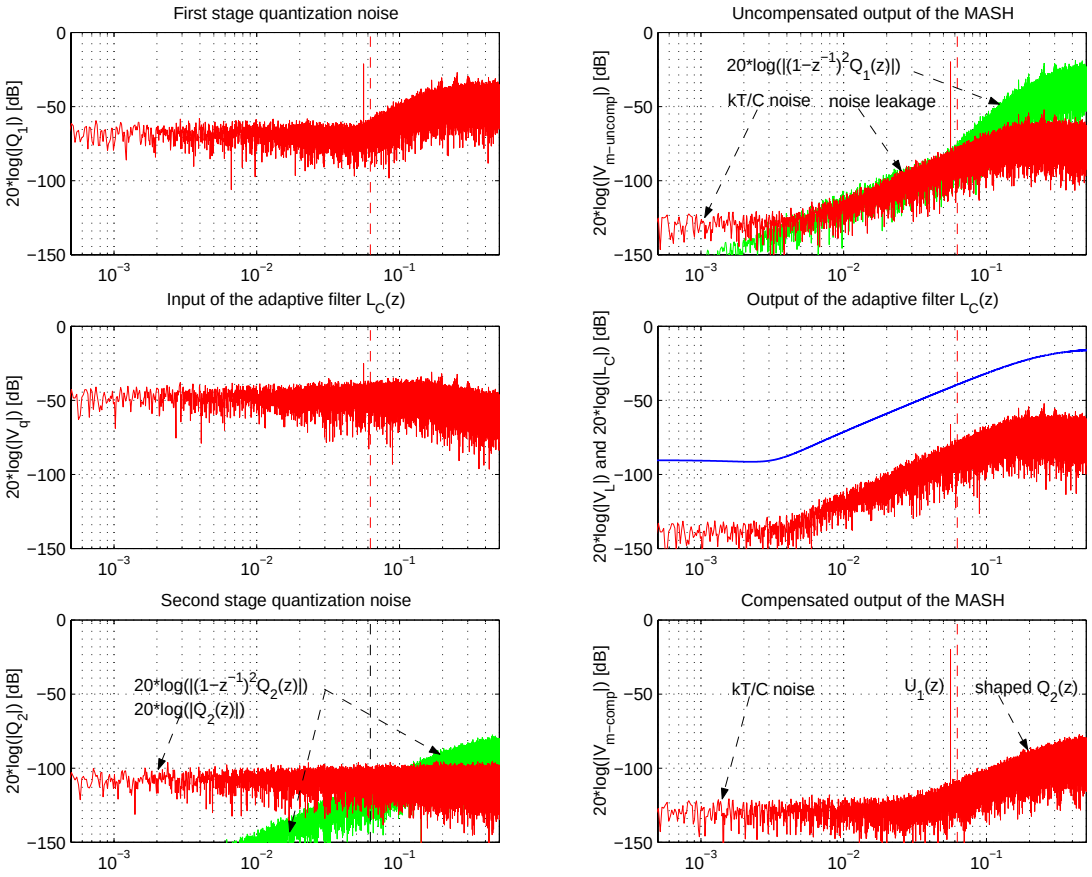

Figure 4.7: Spectral analysis of some internal / external signals of the MASH after a successful adaptive compensation process

4.2.2 Adaptation Process Optimization

An important observation was made in Section 3.2.2, when the order of magnitude of A_0 was claimed to be much smaller than the rest of the noise-leakage

coefficients $A_1 \ldots A_4$. Based on this observation, the input of the adaptive digital filter $L_C(z)$ can be better provided using a $V_q(z)$ prefiltered with a simple digital differentiator (Fig. 4.8)

$$V_{qd}(z) = (1 - z^{-1})\, V_q(z). \tag{4.13}$$

By applying $v_{qd}[n]$, a first-order filtered $v_q[n]$, the effective order of the adaptive noise-leakage digital correction block (with input $v_q[n]$ and output $v_L[n]$) increases with one, and the coefficients $l_0 \ldots l_M$ are shifted up to cancel the higher-order noise-leakage terms $A_1 \ldots A_M$. This very simple operation does not need additional hardware, because $v_{qd}[n]$ can be obtained from the first stage of $NTF_{1d}(z)$ (Fig. 4.8).

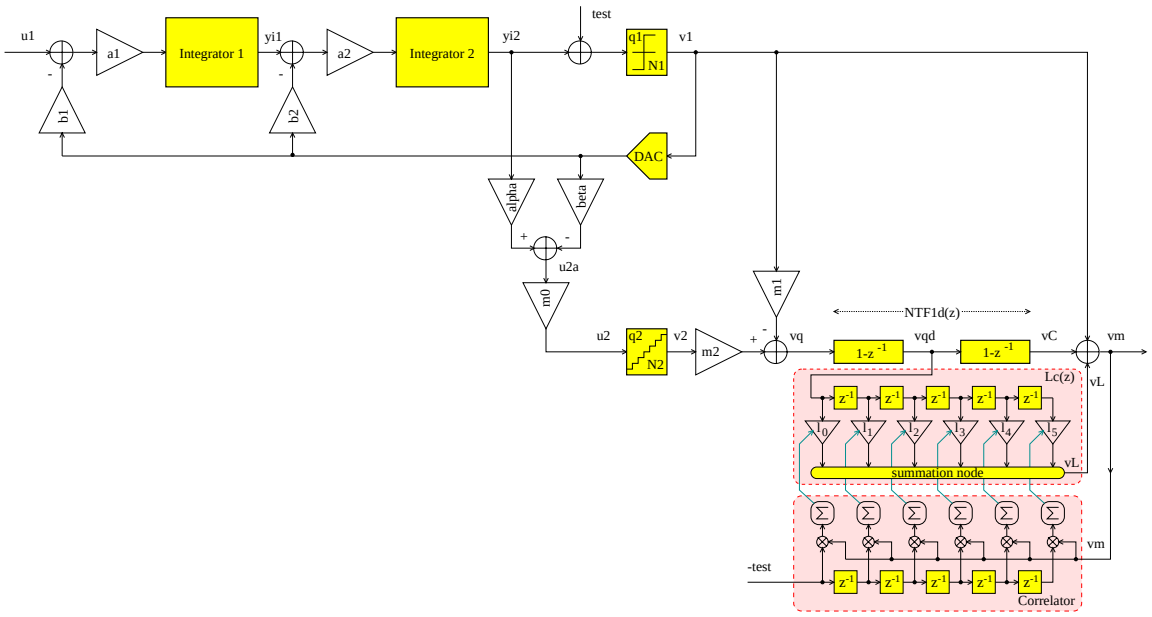

Figure 4.8: Improved adaptive digital noise-leakage compensation scheme using a test signal $test[n]$ for the general cascaded 2-0 delta-sigma ADC

Simulation results for the improved scheme are presented in Fig. 4.9.a, where an $M - 1 = 5^{th}$ order adaptive FIR filter $L_C(z)$ was used to calculate the negative estimate $v_L[n]$ of the noise leakage, having a first-order filtered input $v_{qd}[n]$ (Fig. 4.8). By comparing Figs. 4.9.a and 4.5, it can be observed that the simulation results were improved significantly, and the ripple of the adaptation noise was reduced to the very comfortable value of 1 dB. This performance improvement was achieved due to the use of the extra differentiator at the input of $L_C(z)$ and not due to the increase of the effective order of noise-leakage digital correction block with one order. To support this last statement, an adaptation process was performed with an $M - 1 = 6^{th}$ order adaptive FIR filter $L_C(z)$, but without the differentiator (similar with Fig. 4.2), which results are presented in Fig. 4.9.b. Even if the effective orders of the noise leakage digital correction blocks are the same in Figs. 4.9.a and 4.9.b, adding the differentiator to the front of $L_C(z)$ has

significant performance benefits in addition of simplifying the hardware complexity of $L_C(z)$ with one order. Why is adding a differentiator such a good idea?

The coefficients $\overrightarrow{l}$ of the adaptive FIR filter $L_C(z)$ are estimated and updated on-line by the SSBLMS algorithm (4.12). Due to the finite resolution ($N_l = 16$ bits) of the adaptive FIR filter $L_C(z)$, the estimated coefficients $\overrightarrow{l}$ fluctuate around the optimal solution $\overrightarrow{l_{opt}}$ (global minima of the error surface $\mathcal{J}[n]$) with an error proportional with γ_{SSBLMS} (Section 4.2.1). Fig. 4.9 and Tab. 4.1 show that the effective coefficients $\overrightarrow{l}$ of the adaptive cancellation block, using $L_C(z)$ with and without the differentiator, both converged to the optimal solution $\overrightarrow{l_{opt}}$. However, the fluctuations in the transfer function of $(1 - z^{-1})\, L_C(z)$ ($M = 6$, Fig. 4.9.a) were much smaller than the fluctuations in the transfer function of $L_C(z)$ ($M = 7$, Fig. 4.9.b). (Note that the fluctuations of the equivalent coefficients $\overrightarrow{l}$ are the same in both cases, as is presented in Tab. 4.1.) In the first case, the differentiator performs an explicit and exact first-order shaping of $v_q[n]$, which is necessary in order to estimate the noise leakage $-v_L[n]$. In the second case, this first-order shaping is implicitly realized by $L_C(z)$, but this differentiation is affected by the adaptation noise of the SSBLMS algorithm.

On the other hand, the benefit of the differentiator can be explained by analyzing the spectrum of the noise leakage, which should be compensated. In Fig. 4.7 it is shown that the noise leakage transfer function $H_{leakage}(z)$, (3.20), is only slightly different from a first-order differentiation (compare $V_{m_{uncomp}}$ with $(1 - z^{-1})\, Q_1(z)$). Therefore, the differentiator performs a coarse filtering, letting the adaptive FIR filter $L_C(z)$ to perform a fine correction only, which can be done with more accuracy, that is, smaller ripple. Finally, by using the additional differentiation the ripple of the adaptation noise was reduced by 6 dB [18].

Filter Block	M	l_0	l_1	l_2	l_3	l_4	l_5	l_6
Mean coefficient values, mean$\{\overrightarrow{l}\}$ ($\times 10^{-3}$)								
$(1 - z^{-1})L_C(z)$	6	52.29	−86.65	21.84	8.81	3.60	0.08	0.02
$L_C(z)$	7	52.29	−86.64	21.85	8.81	3.60	0.09	0.00
Fluctuation of coefficients, $\max\{\overrightarrow{l}\} - \min\{\overrightarrow{l}\}$ ($\times 10^{-3}$)								
$(1 - z^{-1})L_C(z)$	6	0.244	0.274	0.305	0.305	0.305	0.274	0.289
$L_C(z)$	7	0.244	0.274	0.289	0.274	0.289	0.274	0.244

Table 4.1: Coefficients of the adaptive digital compensation filter block

The update of the coefficients is based on the result of correlation between the leaked test signal $test[n]$ components present in the output $v_m[n]$, and the digital replica of the originally injected test signal $test[n]$, (4.12). Therefore, to estimate correctly the noise leakage a large test signal is required. On the other hand, a small test signal is preferred to avoid the premature saturation of the first stage and in turn of the whole MASH, due to the test-signal injection. Since the test signal $test[n]$ is uncorrelated with other components of the output signal $v_m[n]$ such as $u_1[n]$, $q_1[n]$ and $q_2[n]$, its power can be measured selectively. Simulations

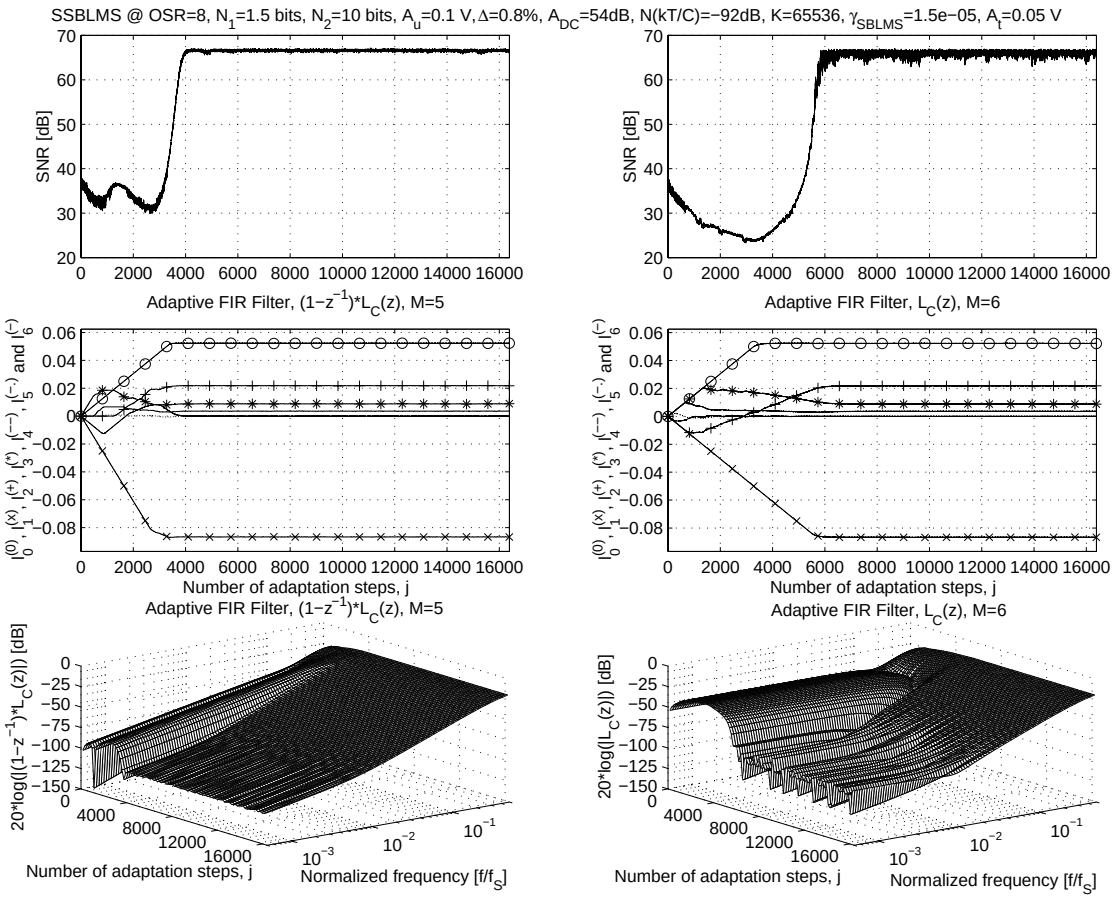

Figure 4.9: (a) Reducing the ripple of the adaptation noise using a differentiator, $M = 6$; (b) adaptation process without differentiator, $M = 7$

show that even if the test-signal power is much lower than the power of other components of the output signal $v_m[n]$ (e.g. the amplitude of the test signal can be as low as $A_t = 0.01$ V), its power can still be determined with high accuracy, and hence the update of the coefficient vector $\overrightarrow{l}$ can be done accurately, and the adaptive compensation process works correctly. In addition, this simulation was performed in fixed-point with 16 bit of accuracy. The concluding results are presented in Figs. 4.10 and 4.11.

After about $j \approx 6000$ adaptation steps (which takes about 3.9 seconds for a sampling frequency of $f_S = 100$ MHz), the adaptive process has converged. After convergence, the coefficient vector $\overrightarrow{l}$ still fluctuates slightly around its steady-state value, due to the inherent error of the SSBLMS update. The ripple of this fluctuation is approximately 0.3×10^{-3} shown for l_0 for $\Delta j = 100$ steps in Fig. 4.10, and numerically for the whole coefficient vector $\overrightarrow{l}$ in Tab. 4.1. This fluctuation in $\overrightarrow{l}$ causes approximately 1-dB adaptation noise in the corrected SNR, shown in detail for $\Delta j = 100$ steps in Fig. 4.10. Finally, Fig. 4.11 shows an SNR performance drop of only 1-2 dB from the ideal SNR curve, and the dynamic range is reduced by only 0.5 dB due to the small test signal. Clearly, the per-

formance of the compensated practical circuit (peak SNR of 84 dB) approaches closely that of the ideal MASH ADC [18], [34]. Note that the performance of SNR=84 dB was obtained by simulations and not by measurements. However, at least a performance of SNR=80 dB should be achievable by the well-designed integrated circuit also (details in Chapter 5). Therefore, 80-dB peak SNR is claimed to be the accuracy of the designed ADC which is used e.g. in Fig. 1.1 and Tab. 1.1.

The last important issue discussed in this section is the order $M-1$ of the adaptive noise-leakage compensation digital FIR filter $L_C(z)$ from adaptation and hardware complexity considerations. So far, we used $M-1=5^{th}$ order adaptive filter with $M=6$ coefficients $l_0 \ldots l_5$. However, it can be observed on Fig. 4.10 that the higher-order coefficients l_4 and l_5 converge to zero, or at least to very small values, so a $M-1=3^{rd}$ order adaptive filter should be enough, which means lower hardware complexity requirements. Simulations confirmed this statement, but we will keep using $M=6$ at least for the first prototype chip, because the noise sources are more complex in a real integrated circuit than our present noise-leakage model, and it is good to keep a small room for the adaptive filter to track the higher-order components of the real noise leakage also. Tab. 4.2 summarizes the final configuration of the adaptive filter $L_C(z)$ for $M=4$, 6 and 10.

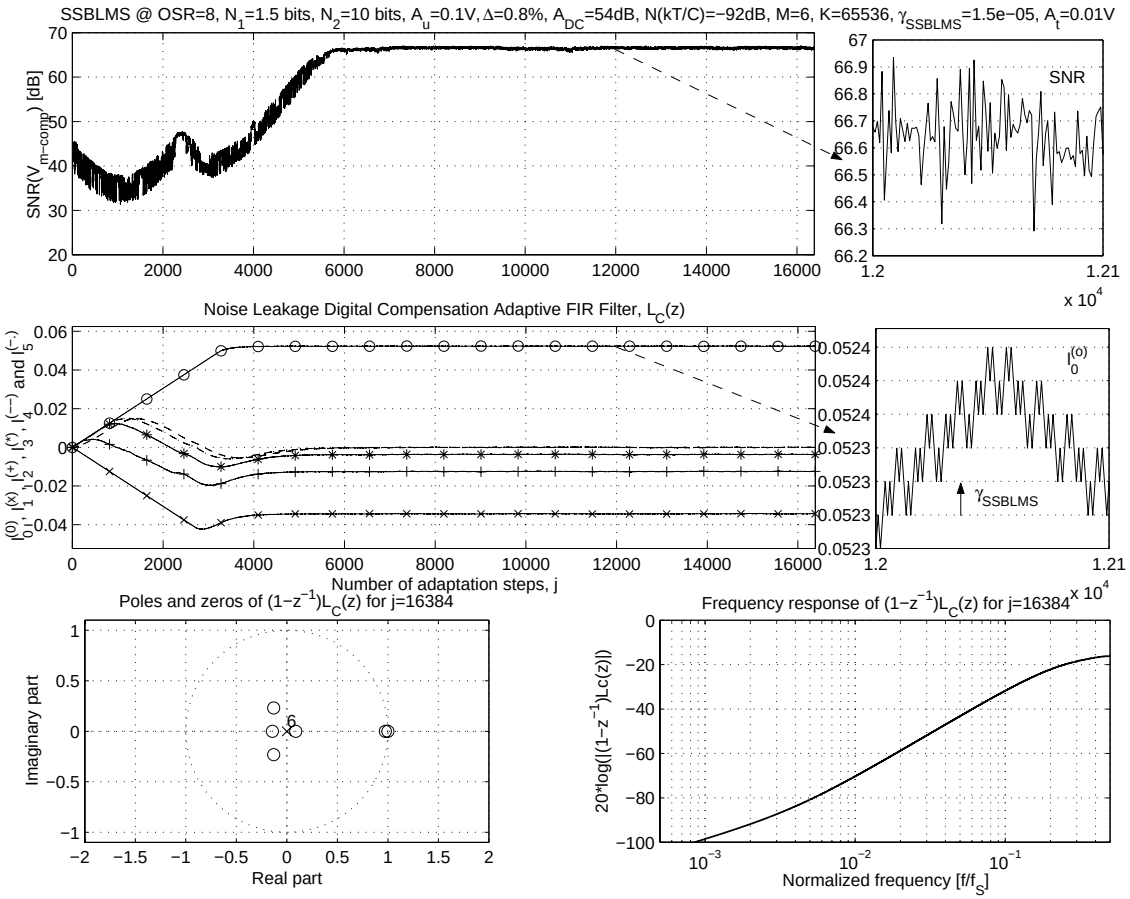

Figure 4.10: Adaptive compensation process (differentiated $v_q[n]$)

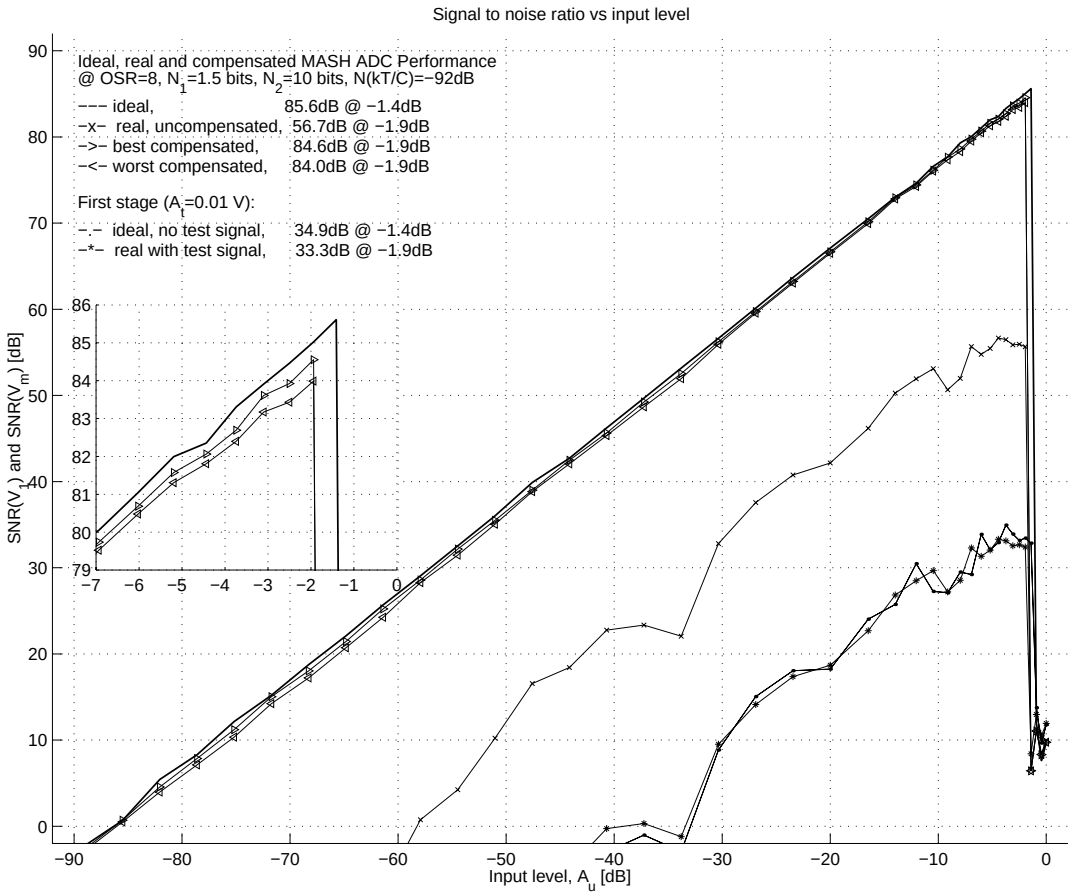

Figure 4.11: Achieved SNR performance (differentiated $v_q[n]$)

In conclusion, by using the optimized adaptive noise-leakage digital compensation, the practical MASH approached closely the ideal MASH performance.

Order of $L_C(z)$	Coefficient values $\overrightarrow{l}$ of $L_C(z)$ $(\times 10^{-3})$					
	l_0	l_1	l_2	l_3	l_4	l_5
$M-1=3$	52.35	-34.37	-12.58	-3.73	—	—
$M-1=5$	52.33	-34.42	-12.60	-3.72	-0.03	$+0.00$
$M-1=9$	52.29	-34.34	-12.52	-3.73	-0.10	-0.01
	—	—	l_6	l_7	l_8	l_9
	—	—	-00.01	-0.01	$+0.04$	$+0.04$

Table 4.2: Coefficients of the adaptive digital compensation filter

4.2.3 Shaped or Unshaped Test Signal

The adaptive filtering method described in the previous sections minimizes the mean-square error of the output $v_m[n]$ using the LMS algorithm, or more pre-

cisely, the SSBLMS algorithm. The algorithm tries to reduce the total power of the test signal present in the output signal $v_m[n]$, and thus also the power of the leaked first quantizer's quantization noise in the same output $v_m[n]$. Hence, it gives uniform weighting of errors over the whole spectrum, that is, it decreases the high-frequency noise leakage as much as the low-frequency noise leakage. The high-frequency noise leakage is eliminated anyway by the following decimation filter, so there is no extra need to reduce the high-frequency components of the noise leakage by adaptation.

In order to eliminate this undesirable effect, one needs to reduce the sensitivity of the adaptation algorithm to out-of-band (high-frequency) noise leakage [29]. This can be achieved by changing the power spectral distribution of the test signal, that is, to produce a frequency-shaped test signal which still has a uniform amplitude distribution, but whose energy is concentrated in-band. The reduction of the out-of-band energy of the test signal is equivalent to assuming that no out-of-band noise leakage is present in the system for the adaptation algorithm, and the adaptation algorithm needs to reduce only the in-band noise leakage. Therefore, one expects that using a low-pass-filtered test signal should lead to a better performance [32].

A shaped, that is, low-pass-filtered test signal can be produced by low-pass filtering a broadband test signal. Using this method would however lead to a multibit test signal, and then unfortunately, the correlator in the adaptation hardware would need multipliers. A simple method of generating a low-pass-filtered test signal, which is still binary, is by upsampling the initial broadband test signal in the time domain [73]. Upsampling is accomplished by inserting $L-1$ replica values between samples, that is, stretching the signal L times in the time domain, which results in a low-pass effect in the frequency domain, or more exactly, in a filtering with the $sinc$ function.

However, the convergence is much noisier for a shaped test signal compared with the convergence with an unshaped, broadband test signal (Fig. 4.12) [33]. Therefore, unfortunately, these results did not validate the shaped test signal method presented above, even if its reasoning seems to be good.

The failure of the shaped test signal method can be explained based on the theory of the so-called spread spectrum modulation techniques used in modern communication systems [72, Section 5.10]. When one performs the on-line correlation over a finite block of samples K between the test signal $test[n]$ and the output of the MASH $v_m = f\{u_1, q_1, test, q_2\}$, the signals $u_1[n]$, $q_1[n]$ and $q_2[n]$ act as perturbations in measuring the power of the test signal $test[n]$ in $v_m[n]$ (Section 4.2.1). Among these perturbations, $u_1[n]$ has the biggest power, so its effect affects most this measurement. In [72, Section 5.10.2] is demonstrated that the perturbation rejection capability is given by the ratio between the bandwidth, in our case, of the test signal $test[n]$ (which is broadband for an unshaped test signal, or narrow-band for a low-pass shaped test signal) and the bandwidth of the "perturbation" $u_1[n]$ (which is obviously narrow-band: $f_B = \frac{f_S}{2\,OSR}$). In conclusion, a broadband or white test signal provides the best performances, because its bandwidth is OSR times larger than that of the low-frequency signal band, and

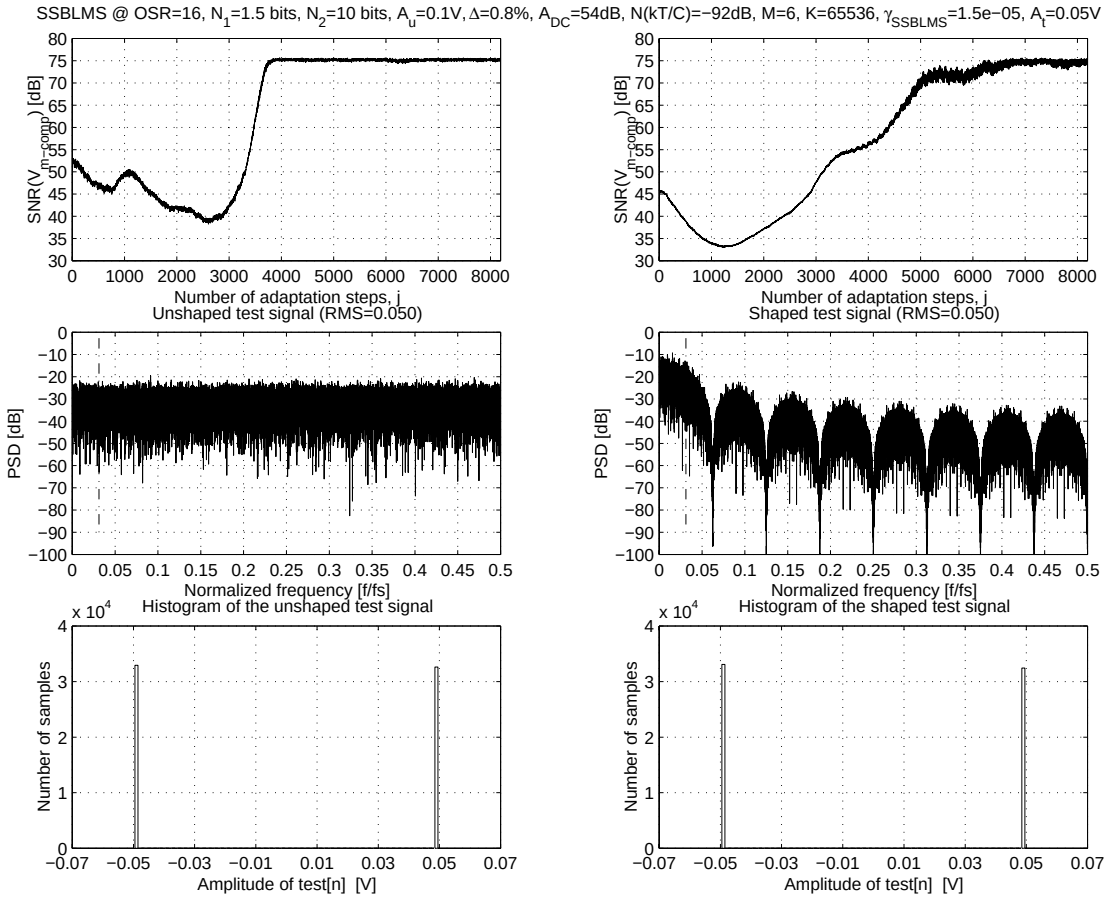

Figure 4.12: Convergence using unshaped or shaped test signal

therefore it has the highest perturbation ($u_1[n]$) rejection capability. Note that the same conclusion was found in [24], that is, larger bandwidth for the calibration signal (which had the same role in [24] as the test signal in the presented approach) led to better performed digital correction.

Extensive simulations showed that using a shaped test signal increased more the unwanted effects of $u_1[n]$ on the correlation result than it would improve the performance based on the reasoning given above (Fig. 4.12). Therefore, we have concluded that a broadband (white) test signal should be used instead [18], [34].

4.3 2-0 MASH ADC with 5-Bit First-Stage Quantization

Finally, to improve further the accuracy of the 2-0 MASH ADC, while preserving its bandwidth, a multibit quantizer can be used in the first-stage delta-sigma ADC [12], [26], [74], [75]. However, the linearity of the multibit DAC in the feedback path is critical, so it needs to be improved by using mismatch shaping or other correction methods (details in Section 2.3.1).

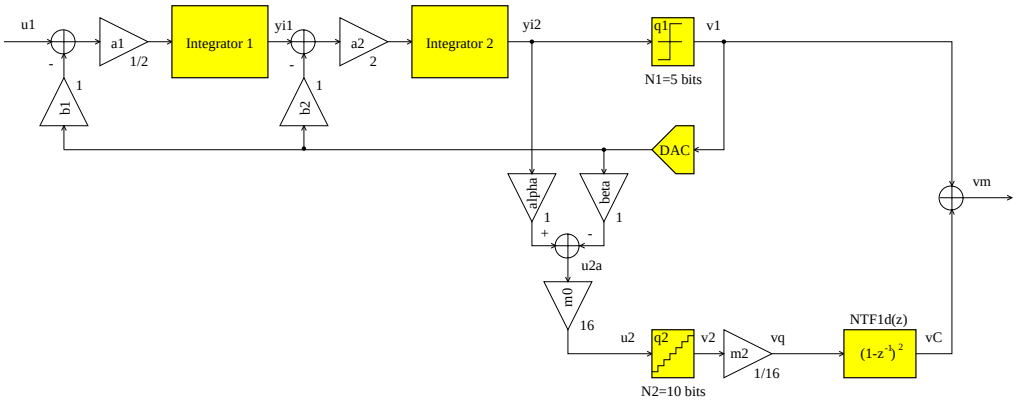

Figure 4.13: High-performance 2-0 MASH ADC

For a multibit first stage, the reduced quantization noise $q_1[n]$ allows the scaling of the input of the second stage $u_2[n]$ by using $m_0 > 1$ and $m_2 = \frac{1}{m_1} < 1$. This will reduce the power of $q_2[n]$, and hence improve the SNR performance of the MASH, as expressed by (3.18). In addition, the multibit first stage leads to decreased sensitivity to analog circuit imperfections [12], because the noise leakage is proportional to the power of $q_1[n]$, as indicated in (3.19). However, the mismatch between $NTF_1(z)$ and $NTF_{1d}(z)$ is still critical, especially when high sampling rates (e.g. $f_S = 100$ MHz) allow only modest DC opamp gains ($A_{DC} = 40$–50 dB). Therefore, our adaptive on-line error correction technique is needed to cancel the negative effect of analog imperfections even for a multibit first stage.

An adaptively corrected 2-0 MASH architecture, similar to the one presented in Fig. 3.3, but with a multibit first stage ($N_1 = 5$ bit) and slightly different coefficients [9], [74] was investigated at behavioral level (Fig. 4.13). Extensive system-level simulation results (with ideal quantizers and ideal DAC) indicated that by using a 5-bit quantizer in the first stage, and a lowered oversampling ratio of $OSR = 4$, it may achieve 16-bit accuracy with a 12-MHz signal bandwidth (Fig. 4.14).

To implement this adaptively-corrected multibit 2-0 cascaded delta-sigma ADC needs further investigations. Especially the feedback DAC needs to meet high (16-bit) linearity requirements at low oversampling ratios ($OSR = 4$). Also, the second-order loop gain at low oversampling ratios provides only a reduced shaping of the nonlinearities of the multibit quantizer (e.g. $|NTF(z)|\Big|_{OSR=4} = -5$ dB), so this issue should be studied as well. Moreover, the $\frac{kT}{C}$-noise floor of the switched capacitors must be set to a lower value than the overall resolution (16-bit), which would require large sampling capacitors due to the targeted high speed of operation ($f_S = 100$ MHz) and low oversampling ratio ($OSR = 4$). The effective implementation of this high-performance converter is beyond the scope of this thesis. However, even this brief analysis shows that the adaptive correction method can significantly improve such a multibit first-stage quantization MASH ADC.

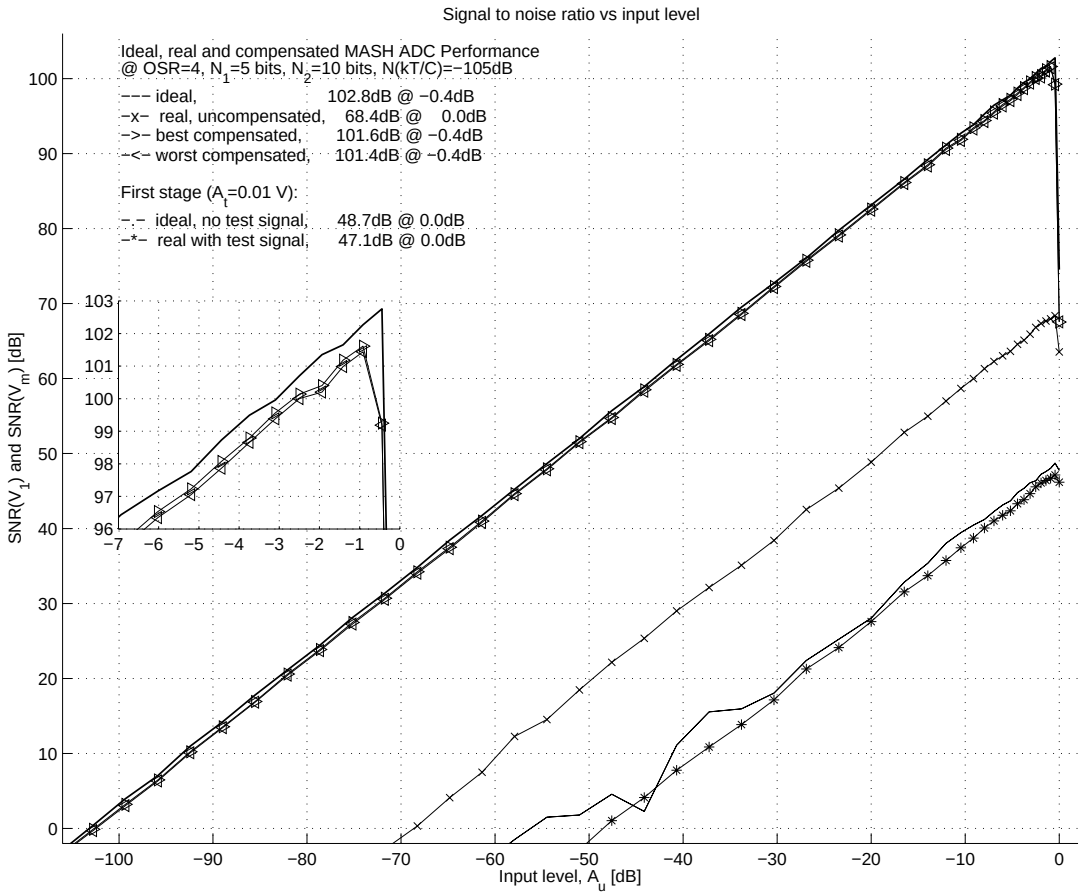

Figure 4.14: Simulated SNR performance of the high-performance 2-0 MASH ADC ($f_S = 100$ MHz, $OSR = 4$, $N_1 = 5$ bit, $N_2 = 10$ bit, $A_{DC} = 54$ dB, and $\Delta_C = 0.4$ %)

4.4 Conclusions

In this chapter, an effective digital error correction method for cascaded delta-sigma converters was presented. Due to the imperfect analog circuits, quantization noise leakage is present in the output, which degrades the performance of the real MASH. This noise leakage can be estimated and cancelled by an adaptive digital FIR filter. In order to perform this estimation on-line, the coefficients of this adaptive filter were updated by the sign-sign-block-least-mean-square algorithm, using a pseudo-random test signal. After a careful design of the adaptive noise-leakage compensation digital FIR filter, it turns out that the required digital hardware for error corrections is quite simple, and also it provides robust operation. Extensive simulations showed an achievable SNR=13-bit @ 6-MHz signal bandwidth analog-to-digital converter, which is a useful performance for a state-of-the-art data converter. The adaptive correction method was extended for 2-0 MASH ADCs with 5-bit first-stage quantization (with ideal quantizers and ideal DAC) in order to gain higher accuracy ($SNR = 16$ bits) and larger bandwidth ($f_B = 12$ MHz). This last circuit needs further investigations before being implemented.

Chapter 5

Prototype Chip Design

This chapter discusses the details of the circuit-level implementation of the adaptive compensated cascaded 2-0 delta-sigma ADC, which was discussed at the behavioral level in the previous chapters. Here, the detailed transistor-level design of the component circuit blocks will be presented. The correct operation is illustrated by selected simulation results. The layout of the prototype chip[1] will be sent out for fabrication soon, so measurement results are not available yet.

The performance specifications for the circuit design were described in Section 3.1.4. The most relevant parameters, from which all the circuit parameters were calculated, are repeated for convenience in Tab. 5.1.

a_1	b_1	a_2	b_2	OSR	$N(\frac{kT}{C})$	α	β	m_0
$\frac{1}{4}$	1	$\frac{1}{2}$	$\frac{1}{2}$	8	-92 dB	8	2	$\frac{1}{2}$

Table 5.1: Parameters for the prototype chip design

5.1 First Stage of the MASH ADC

The first stage of the adaptive digital compensated cascaded 2-0 delta-sigma ADC is a 1.5-bit second-order delta-sigma modulator. Hence, it is composed by 2 integrators, a tri-level quantizer in the feedforward path, and a tri-level digital-to-analog converter in the feedback path (Fig. 2.24).

The circuit-level implementation offers some special challenges due to the targeted speed of operation. In the second-order delta-sigma ADC, all blocks are to be operated with a clock frequency of $f_S = 100$ MHz. The traditional implementations, for example with folded-cascode opamps in a simple integrator structure, are not suitable. The main limitation comes from the gain-bandwidth product of the operational amplifiers, which will be described in more detail in Section 5.1.2.

[1]The prototype chip design, as well this chapter, was contributed by my colleague at Oregon State University, José Silva (`silva@ece.orst.edu`).

5.1.1 Integrators

The integrator structure shown in Fig. 3.11 has been used for low-speed implementations (e.g. f_S = 1 MHz to 10 MHz). However, for operation at the targeted speed of 100 MHz, it is very difficult to design an operational amplifier with sufficiently large gain-bandwidth product. Hence, the traditional implementations, for example with folded-cascode opamps, are not suitable. One was to solve this problem is to use of correlated double-sampling integrators [76], which greatly reduce the gain requirements for the operational amplifiers. Figs. 5.1 and 5.2 show the schematic of the first and second integrators, respectively. They are shown in single-ended version, for simplicity. The actual implementation uses a fully-differential topology.

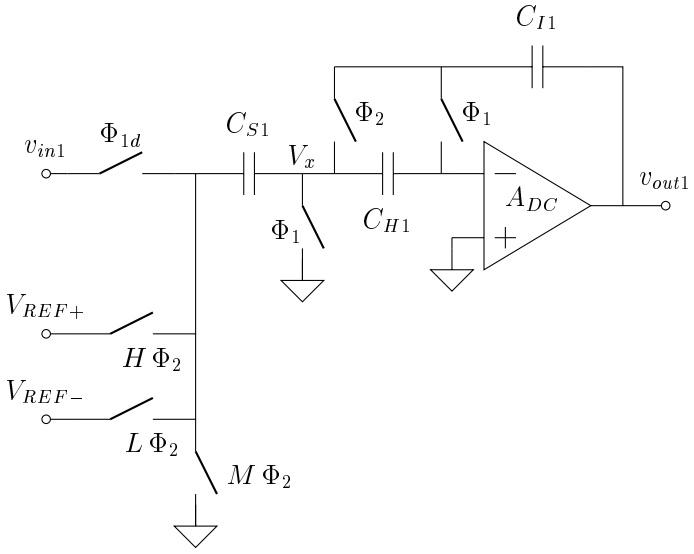

Figure 5.1: First integrator from the first stage of the MASH ADC

The structure is similar to the one shown in Fig. 3.11, except for the addition of the holding capacitor C_H, and a switch connecting the inverting input to the integrating capacitor during phase Φ_1. During this phase, the holding capacitor C_H samples the offset voltage V_{OS} and the gain error voltage $-v_{out}/A_{DC}$ introduced by the operational amplifier. During phase Φ_2, the stored error is used to create an enhanced virtual ground node at V_x. One of the results is that the effective DC gain of the integrator becomes the square of the opamp DC gain. For example, for an opamp with a very small DC gain of, say, 40 dB, the effective gain of the integrator is nearly 80 dB.

Both the first ($i = 1$) and the second ($i = 2$) integrators of the second-order delta-sigma ADC implement the same transfer function:

$$V_{out_i}(z) = (a_i\, V_{in_i}(z) + a_i\, b_i\, V_a(z))\, \frac{z^{-1}}{1 - z^{-1}}, \quad \text{for} \quad i = 1, 2, \qquad (5.1)$$

where $v_a[n]$ is the output voltage of the feedback tri-level digital-to-analog converter, so $v_a[n] \in \{-V_{REF}; 0; +V_{REF}\}$, accordingly to the state of the digital

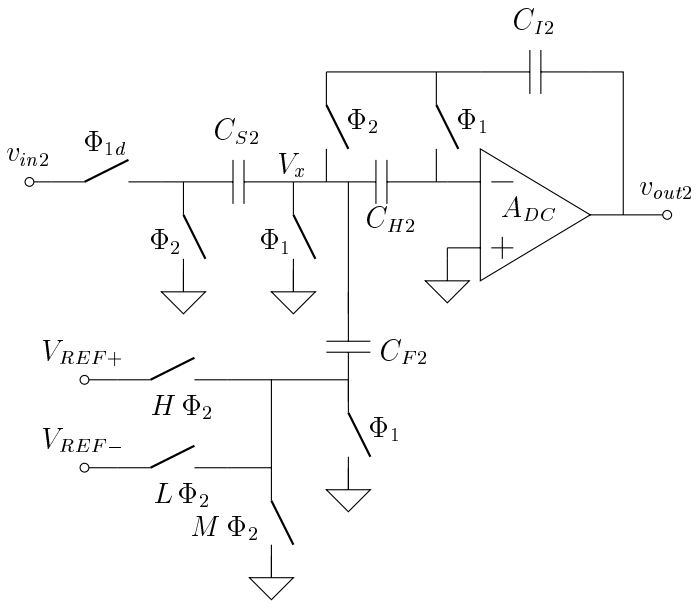

Figure 5.2: Second integrator from the first stage of the MASH ADC

signals H (high), L (low) and M (middle or zero), respectively.

The feedback capacitors C_{Hi}, the integrating capacitors C_{Ii} and the holding capacitors C_{Hi} are all calculated from the sampling capacitors C_{Si}, in order to implement the coefficients of the delta-sigma structure:

$$C_{Fi} = b_i\, C_{Si}, \quad C_{Ii} = \frac{1}{a_1}\, C_{Si}, \quad C_{Hi} = C_{Ii}, \quad \text{for} \quad i = 1, 2. \tag{5.2}$$

The feedback capacitor C_{F1} is not needed in Fig. 5.1. Since $b_1 = 1$, the value of C_{F1} is the same as C_{S1}, so these capacitors were merged, simplifying the circuit and saving chip area. The value of the sampling capacitor C_{Si} is determined by the $\frac{kT}{C}$-noise power level, which imposes a limit on the maximum achievable signal-to-noise ratio SNR for the whole system, given a certain input signal range to the second-order delta-sigma ADC. The performance of the first integrator is the most critical in the modulator (see the discussions in Section 2.5.9), with the minimum size of the sampling capacitor C_{S1} given by

$$C_{S1} = \frac{2\,(1 + b_1)\,k\,T}{\frac{V_{max}^2}{2}\,OSR}\,SNR, \tag{5.3}$$

where V_{max} is the maximum amplitude of $v_{in}[n]$. For $V_{max} = 1$ V and $SNR = 92$ dB, (5.3) sets the minimum capacitor size to 6.7 pF. This value was rounded up to $C_{S1} = 7$ pF. For the second integrator, this requirement is not so important because every error introduced after the first integrator will be reduced by the large low-frequency gain of the first integrator, when it is referred back to the input. Thus, for the second integrator, the noise power is allowed to be twice of the noise power in the first integrator, resulting in $C_{S2} = 2.5$ pF.

In relation to the switches, the following considerations were taken into account. Most nodes have a low potential, and so all switches connected to those nodes are N-type transistors. The exception is the input signal, which needs a CMOS switch. The input switch, controlled by Φ_{1d}, is turned off after the switches controlled by Φ_1. This prevents its signal dependent clock feedthrough and charge injection from affecting the rest of the circuit. The size of the switches was chosen to allow settling for at least $T = 7\,\tau$, where T is half of the clock period ($2\,T = T_S = \frac{1}{f_S} = 10$ ns), and τ is the time constant defined by the switch resistance and the sampling capacitor.

5.1.2 Operational Amplifiers

Before selecting the opamp topology and the corresponding transistor sizes, it is necessary to calculate the specifications that it will have to meet. The most important are the unity-gain frequency f_{ta} and the slew rate SR, but the load capacitance C_L and the power consumption are calculated as well. The required unity-gain frequency f_{ta} is given by

$$f_{ta} = \frac{\ln\, 2^n}{\beta_{fb}\,\pi}\, f_S, \tag{5.4}$$

where $f_S = 100$ MHz is the sampling frequency, β_{fb} is the feedback loop gain, and n is the settling accuracy in bits, which is set to 10 bits, or 0.1% of every voltage step from sample to sample. The feedback loop gain β_{fb} is obtained from return ratio calculations as described in [77]. For the first integrator, the worst case occurs during phase Φ_2, and it is given by

$$\beta_{fb1} = \frac{C_{I1}}{C_{S1} + C_{I1}} = 0.8, \tag{5.5}$$

and for the second integrator the worst case is also during Φ_2, when

$$\beta_{fb2} = \frac{C_{I2}}{C_{S2} + C_{F2} + C_{I2}} = 0.571. \tag{5.6}$$

Substituting these values in (5.4), the unity-gain frequency f_{ta} is calculated to be $f_{ta1} \cong 275.8$ MHz for the first integrator, and $f_{ta2} \cong 386.1$ MHz for the second integrator.

The necessary slew rate SR can be calculated from the maximum voltage step $V_{STEP_{max}}$ at the output of each integrator. For the first integrator, the maximum voltage step $V_{STEP_{max1}}$ is given by

$$V_{STEP_{max1}} = a_1\,(1 + b_1)\,V_{REF}. \tag{5.7}$$

It should be noted that this calculation does not contain any assumptions about the nature of the quantization noise, and therefore it gives a very reliable (in fact, pessimistic) estimate. However, for the second integrator, this parameter is much

more difficult to predict, and so it was obtained from Matlab simulation results. The slew rate SR is then calculated from

$$SR = \frac{V_{STEP_{max}}}{x\, T_S}, \tag{5.8}$$

where $x = 25\%$ is the fraction of the clock phase allowed for slewing. For the first integrator, the slew rate is calculated to be $SR_1 = 400$ V/μs, and for the second integrator, $SR_2 = 320$ V/μs.

The bias current of the differential pair can be calculated from

$$I_{BIAS} = SR \cdot C_L, \tag{5.9}$$

where C_L is the maximum load capacitance seen by each operational amplifier. For the first integrator, during phase Φ_1

$$C_{L_1} \approx C_{S2} + \frac{C_{I1} C_{H1}}{C_{I1} + C_{H1}} = 16.6\,\text{pF}, \tag{5.10}$$

and for the second integrator, during phase Φ_2

$$C_{L_2} \approx C_{I2}\, \frac{C_{I2}\,(C_{S2} + C_{F2} + C_{I2})}{C_{I2} + C_{S2} + C_{F2} + C_{H2}} = 3.38\,\text{pF}. \tag{5.11}$$

Substituting these capacitance values in (5.9), the bias current is determined to be $I_{BIAS_1} = 6.64$ mA for the first integrator, and $I_{BIAS_2} = 1.08$ mA for the second integrator. Finally, the opamp transconductances were calculated from

$$g_m = 2\,\pi\, f_{ta}\, C_L. \tag{5.12}$$

The calculated values are summarized in Tab. 5.2.

In order to achieve the calculated requirements, it is important to use a simple opamp structure. Single-stage opamps have been used frequently in high-frequency SC applications [78], [79], [80]. They give essentially a first-order response, with the non-dominant pole caused by the small parasitic capacitances between the gates and drains of the output transistors. Since this type of amplifier has a very poor DC gain, several techniques have been used to improve this parameter. In [78], the gain is improved by using cascoded transistors, which increases the output impedance by a factor of 100. In [79], the gain is improved by using a dual input telescopic circuit, effectively doubling the input transconductance, and also by cascoding the transistors. In [80], a simple stage with differential regulated cascode transistors is presented.

In this project, we implemented a simple single-stage opamp, with no special features other than cascode transistors, as shown in Fig. 5.3. This structure provides the highest unity-gain bandwidth f_{ta}. Using the opamp in a correlated double sampling integrator further compensates for the effects of the poor DC gain. When comparing the popular folded-cascode implementation with the selected telescopic implementation, one can find that for the same specifications, the

	First Integrator	Second Integrator	Units
Capacitors			
C_S	7.00	2.50	pF
C_F	—	1.25	pF
C_H	28.0	5.00	pF
C_I	28.0	5.00	pF
Opamp parameters			
f_{ta}	275.8	386.1	MHz
SR	400	320	V/μs
C_L	16.8	3.4	pF
I_{BIAS}	6.64	1.08	mA
g_m	28.8	8.2	mA/V
Loop Gain	0.800	0.571	V/V

Table 5.2: Circuit parameters for the first stage of the MASH ADC

former has about twice the power consumption, and a much lower phase margin than the latter.

A common-mode feedback stage is needed to keep the output voltages within the proper region of the operation. The implemented circuit is shown in Fig. 5.4 [81]. The capacitors C_{C+} and C_{C-} generate the average of the output voltages, which is obtained at the node V_x. The capacitors C_{S+} and C_{S-} along with the switches, also implement a low-pass filter and help the common-mode voltage converge to V_{CM}. The differential pair shown in the common-mode feedback

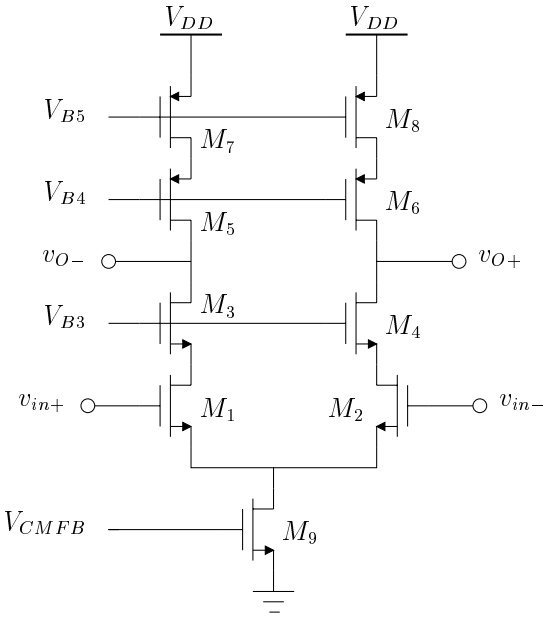

Figure 5.3: Telescopic opamp schematic used in the integrators

circuit, connected in a unity-gain configuration, has a buffering and decoupling function. It reduces the magnitude of glitches, and other non-desirable spurious signals, in the common-mode voltage V_{CMFB}.

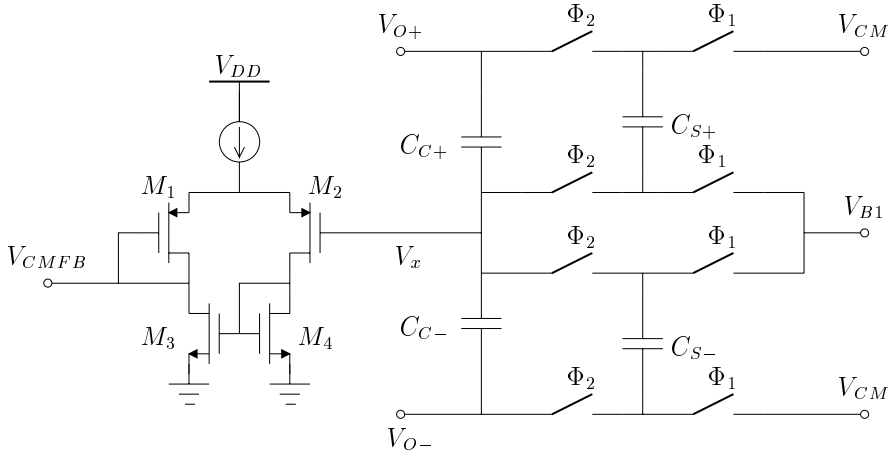

Figure 5.4: Common-mode feedback circuit for the opamps

The bias voltages used in the operational amplifier are generated by the circuit shown in Fig. 5.5. The main part of this circuit is a constant transconductance bias loop [82], which generates V_{B1} and V_{B5}. To a first-order approximation, these voltages are dependent only on the ratio between the sizes of each transistor and M_5. The current through the loop is determined from the off-chip resistor R_{BIAS}. By making $(W/L)_{10} = 4\,(W/L)_5$, the transconductance of M_5 becomes $g_{m5} = 1/R_{BIAS}$. The cascode voltages V_{B3} and V_{B4} are generated by the two wide-swing cascode bias circuit branches. For V_{B4} it is required that

$$(W/L)_{15} = \frac{(W/L)_5}{(n+1)^2} \quad \text{and} \quad (W/L)_6 = \frac{(W/L)_5}{n^2}, \tag{5.13}$$

and, for V_{B3}

$$(W/L)_{21} = \frac{(W/L)_8}{(n+1)^2} \quad \text{and} \quad (W/L)_7 = \frac{(W/L)_8}{n^2}. \tag{5.14}$$

When these conditions are met, each of these branches will set a voltage $n\,V_{eff}$ above saturation.

Finally, the startup circuit makes sure that during power-up, the circuit voltages are not stuck at the ground potential. If this happens, the inverter formed by M_3 and M_4 turns on the transistors M_1 and M_2, which pull the voltages V_{B3} and V_{B2} to the supply rail. Once the currents approach the correct values, V_{B4} will be high enough and the inverter will turn off M_1 and M_2. Note that M_4 operates as an active load, and so it should be long: $(W/L)_4 = 0.5/27.8$.

5.1.3 Tri-Level Quantizer

In order to implement a quantizer with 3 levels, it is necessary to use two comparators and a decoder, as shown in Fig. 5.6. The outputs H, M and L are generated

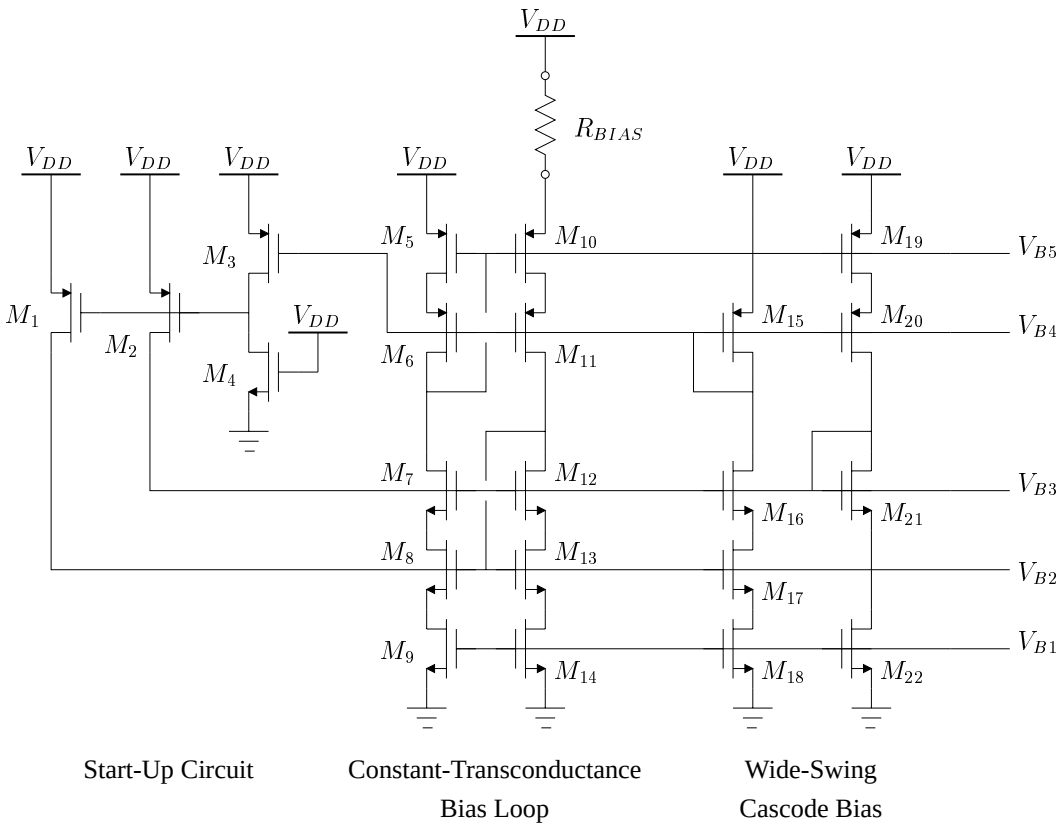

Figure 5.5: Generation of the bias voltages for the opamps

from Q_H and Q_L accordingly to the following logic expressions:

$$H = Q_H\,\overline{Q_L}, \qquad M = \overline{Q_H}\,\overline{Q_L}, \qquad L = \overline{Q_H}\,Q_L. \tag{5.15}$$

The decoder implements these relations with two inverters and three AND or NOR gates.

As all other elements in the modulator, the comparators also have to satisfy stringent speed requirements. However, their accuracy has little influence on the overall performance of the modulator [50]. The literature reports on many different types of comparators, with the fastest ones usually operating in current mode. The typical approach combines the charging of parasitic capacitances with some type of positive feedback.

The implemented comparator, adapted from [83], is shown on Fig. 5.7. It uses simple differential pairs as voltage-to-current converters. The main pair, implemented with M_3 and M_4, is used for the input voltages V_{in+} and V_{in-}. The other two, with lower gains, are used for the threshold voltages V_{TP+} and V_{TP-}, and for the test signals V_{test+} and V_{test-}. The resulting current is used to charge the parasitic capacitances of a simple CMOS inverter. An additional source-follower stage (M_9 and M_{10}), operating in class AB, provides low input impedance and also positive feedback, resulting in a considerable speed improvement.

The comparator uses a flip-flop. Its schematic is presented in Fig. 5.8. This

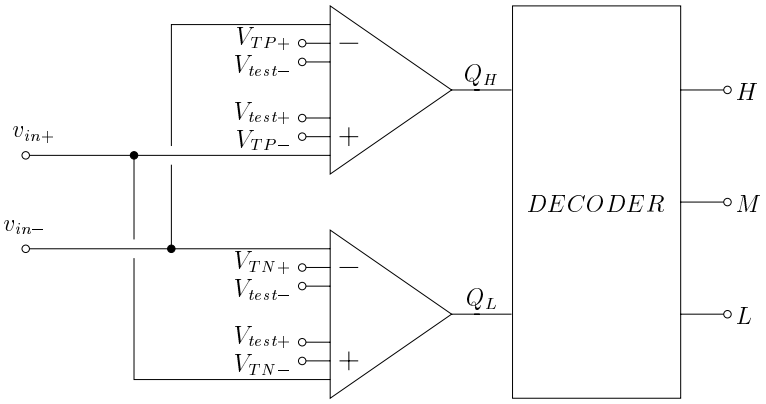

Figure 5.6: Tri-level quantizer for the first stage of the MASH ADC

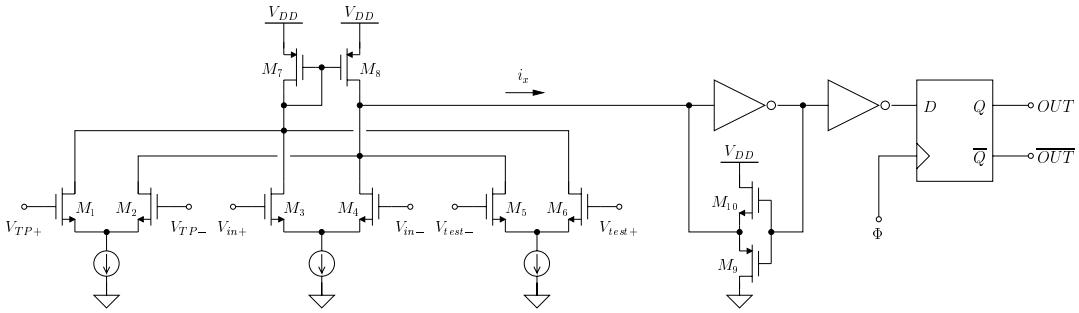

Figure 5.7: Comparator used in the tri-level quantizer

type of configuration, called TSPC (True Single Phase Clock), has been used successfully for various high-speed applications [84]. Although the propagation time is considerably faster than the required for this application, this type of circuit combines both simplicity and low area with very high speed. The circuit uses the internal parasitic capacitances to store the logic state. The input signal D is propagated from the first inverter to the second inverter during the negative edge of the clock signal CK, and from the second inverter to the third inverter during the positive edge of the clock signal CK.

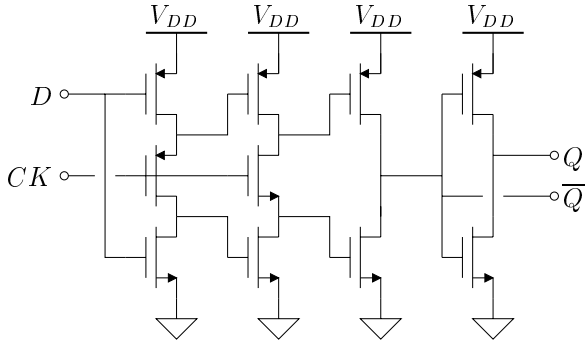

Figure 5.8: TSPC flip-flop used in the comparator

The output of the second integrator is available during Φ_1. During this phase, the comparator decides if the signal level is below or above the threshold. The flip-flop stores this state at the falling edge of Φ_1 right before it is needed, since the integrators only use it during phase Φ_2 of the MASH ADC.

Fig. 5.9 shows a detailed diagram of the first stage. The calculations described above are summarized in Tab. 5.2 on page 86. The total chip capacitance for the first integrator is 76 pF, which for the selected process consumes an area of about 0.125 mm^2. The estimated power consumption for the two integrators is 25 mW.

5.2 Second Stage of the MASH ADC

The second stage of the cascaded 2-0 delta-sigma ADC is a multibit quantizer, which mainly processes the quantization noise of the first-stage quantizer. To provide the weighted difference between the input and the output of the first-stage quantizer, an analog subtraction must be implemented. For the multibit quantizer in this project, a 10-bit pipelined analog-to-digital converter was chosen.

5.2.1 Analog Subtraction

In order to obtain the quantization noise from the first stage, it is necessary to subtract the output of the first stage, $v_1[n]$, from the output of the second integrator, $y_{i2}[n]$. The subtraction is performed by the switched-capacitor circuit shown in Fig. 5.10. The circuit is essentially an amplifier with two inputs. Again, correlated double-sampling techniques are used to improve the performance. Since the $\frac{kT}{C}$-noise is not so important in this stage, the capacitors have a value 16 times smaller than the calculated for the first integrator. The circuit has the transfer function

$$U_2(z) = m_0 \left(\alpha\, Y_{i2}(z) + \beta\, V_{1a}\right) z^{-1}. \tag{5.16}$$

The capacitors implement the coefficients α, β and m_0 as

$$m_0\, \alpha = C_3/C_1, \quad \text{and} \quad m_0\, \beta = C_3/C_2. \tag{5.17}$$

5.2.2 Multibit Quantizer

The second stage is just a multibit quantizer. To implement this multibit analog-to-digital converter, the best option available for this project is a pre-existing 10-bit, 50-MHz pipelined converter, offered by Lucent. However, this poses a problem: how to use a 50 MHz converter in a system which is supposed to run at $f_S = 100$ MHz? There are two possible solutions.

In order to obtain samples at 100 MHz, the system can use two of these pipelined ADCs to form a time-interleaving converter. The circuit diagram is shown in Fig. 5.11. One of the problems with time-interleaving converters is the sensitivity to mismatch, which causes tones at submultiples of the number of

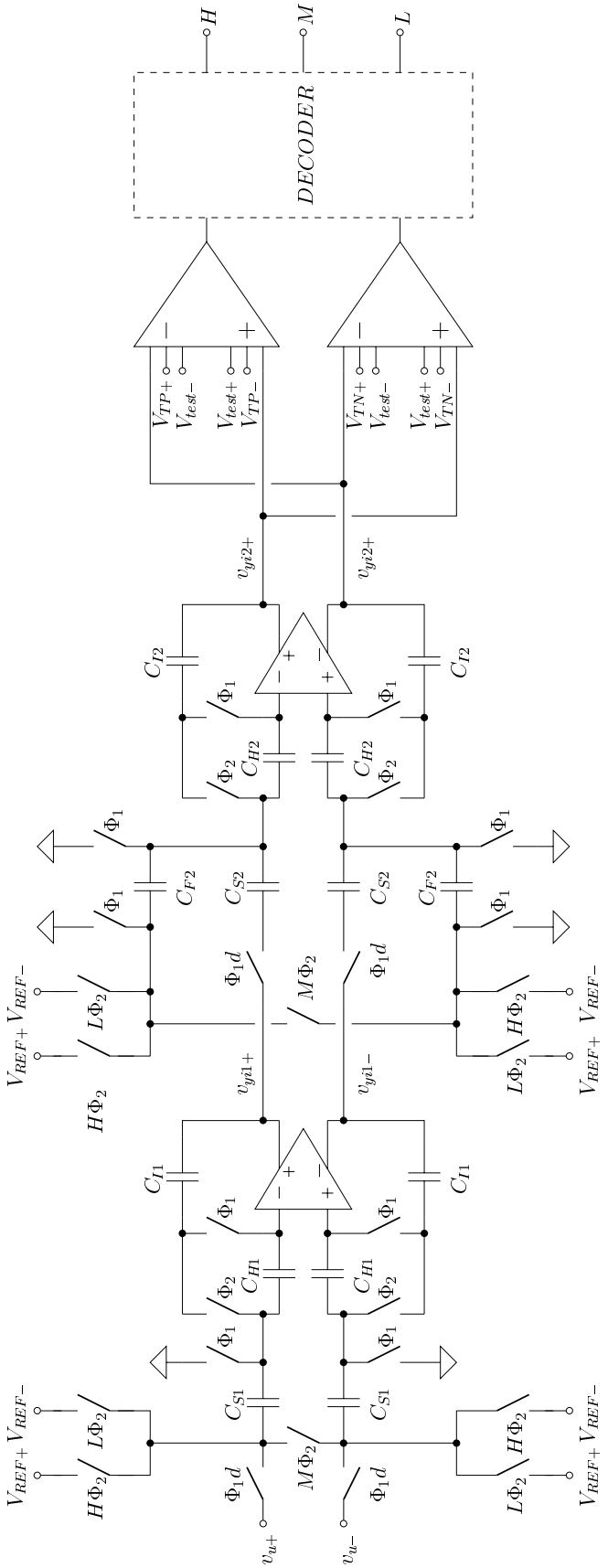

Figure 5.9: Detailed first stage (second-order 1.5-bit delta-sigma ADC) diagram

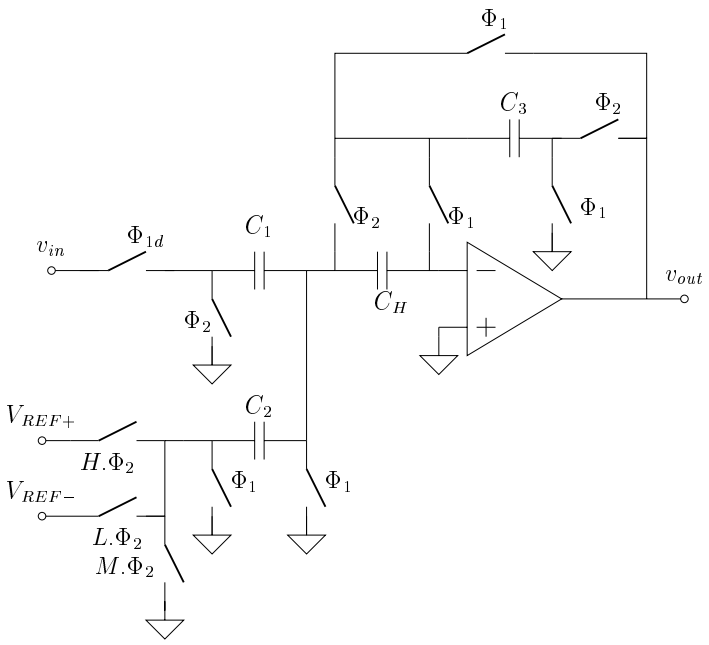

Figure 5.10: Analog subtraction circuit providing the second-stage input u_2

channels [39]. It was observed from simulations that offset errors do not cause any degradation in the SNR, and gain errors cause only negligible effects. This is because the second-stage ADC is followed by a second-order differentiator $NTF_{1d}(z)$ which attenuates the distortions (details in Section 3.1.2).

The second solution, is based on a reduced sample-rate scheme, proposed in [85]. It is more elegant but it needs some structural modifications. The circuit diagram is shown in Fig. 5.12. The principle is based on the interchange of blocks between the modulator structure and the following third-order decimating filter. The transfer function of the decimating filter is given by

$$H(z) = \frac{1}{N^3}\left(\frac{1-z^{-N}}{1-z^{-1}}\right)^3 \tag{5.18}$$

It is possible to cancel part of the denominator of this expression with the FIR filter included after the analog-to-digital converter. Then, the remaining numerator (a

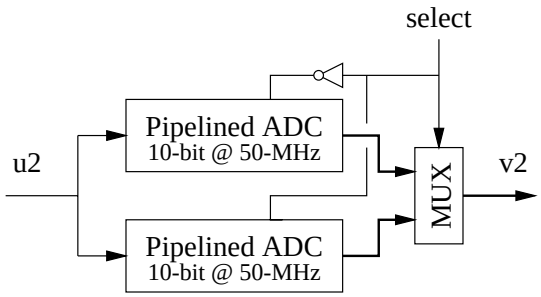

Figure 5.11: Time-interleaved 2 pipelined ADC implementing the second-stage quantizer

differentiator which only needs to perform calculations every N clock cycles) allows a reduction of the clock rate. In particular, if $N = 2$, the ADC can work at 50 MHz. If N is equal to the oversampling ratio OSR, the ADC needs to run only at 12.5 MHz. At this speed, it is easier to get a higher resolution ADC, and therefore a higher SNR for the overall converter. The only drawback of this method is that the quantization noise folds back to the baseband multiplied by a factor of N, which corresponds to a degradation of 3 dB (0.5 bit) for every octave. However, such reduction is acceptable.

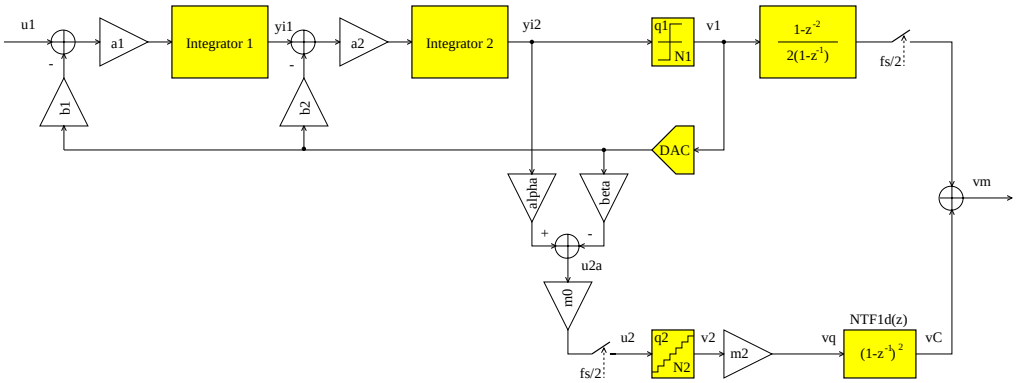

Figure 5.12: MASH structure with reduced sample-rate requirement for the second stage

5.3 Noise Leakage Compensation Logic

In order to reduce, and ideally eliminate, the first-stage quantization noise from the global output $v_m[n]$ of the cascaded 2-0 delta-sigma ADC, one should process digitally the weighted combination $v_q[n]$ of the output of the first stage $v_1[n]$ and the output of the second stage $v_2[n]$ by the first-stage quantization noise cancellation logic. This cancellation logic is basically formed by the digital compensation filter $NTF_{1d}(z)$ and the adaptive noise leakage digital compensation filter $L_C(z)$ (Fig. 4.1).

The simplified hardware implementation of the adaptive compensation filter $L_C(z)$ was already described in Section 4.1.3. Each accumulator of the correlator can be implemented as shown in Fig. 5.13. The multibit output signal $v_m[n]$ of the MASH is converted to its two's-complement representation whenever the $+/-$ line is high. The sign bits $sign_{bit}$ are the output of the accumulators, and are used to update the coefficients $\overrightarrow{l}$ in the adaptive digital FIR filter $L_C(z)$.

5.3.1 Test-Signal Generator

To update the coefficients $\overrightarrow{l}$ of $L_C(z)$ adaptively, a test signal $test[n]$ is injected into the first stage, before the first-stage quantizer (Fig. 4.1.b). The test signal is created by a pseudo-random sequence generator, employing a maximal-length

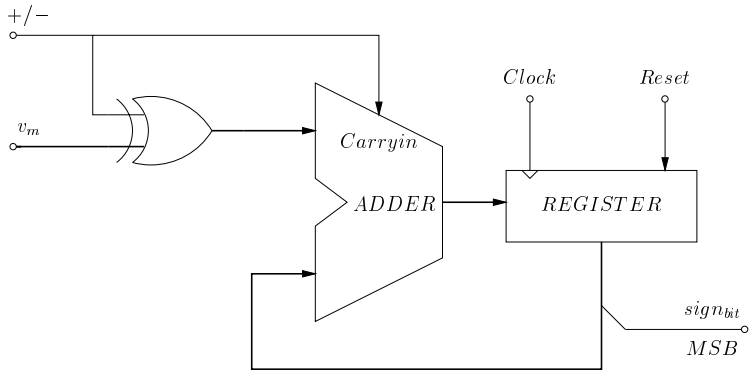

Figure 5.13: Accumulator for the adaptive filter

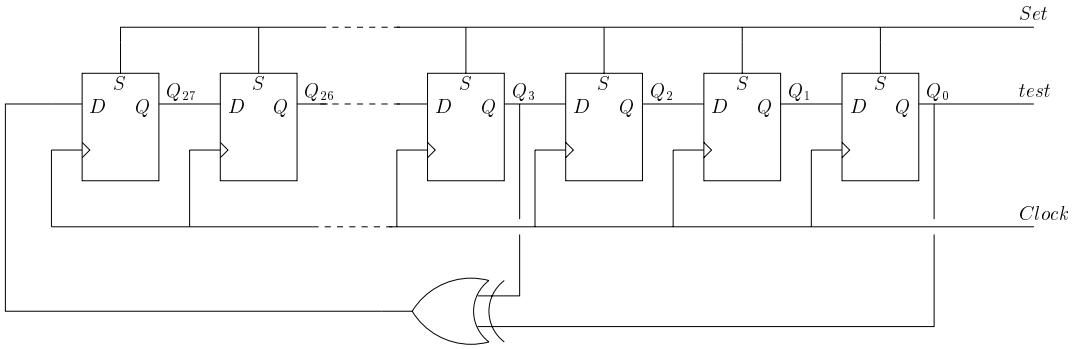

Figure 5.14: 28-bit maximum-length sequence generator

feedback shift register [86]. The circuit is shown on Fig. 5.14. The generated sequence repeats itself with period $T = 2^N/f_S$, where N is the number of flip-flops in the generator. This period should be long enough so that it doesn't affect the main signal. In order to get a period of at least 1 second at a clock rate of $f_S = 100$ MHz, it is necessary to have at least 27 flip-flops. The characteristic equation for a 28-bit sequence generator is simpler than for a 27-bit sequence generator, so a 28-bit sequence generator was chosen, raising the repetition period to 2.7 seconds. Its characteristic equation is implemented by

$$D_i = Q_{i+1}, \qquad D_{27} = Q_0 \oplus Q_3 \tag{5.19}$$

The test signal $test[n]$ is obtained from Q_0. It is applied directly to the correlator, and is used to drive the switches that connect the two analog test signal voltages to the input of quantizer in the first stage.

5.4 Circuit-Level Simulation Results

The circuits are being designed in a 0.25 μm CMOS process provided by Lucent, for a 3.3 V power supply. The capacitors are implemented with a stacked structure, composed of 4 layers of metal and a polysilicon layer. The software package used for the design is Design Framework-II, from Cadence. The circuits are first

described and simulated at schematic level, using Analog Artist and SpectreS. After confirmation of the required performance, the layout for each block is drawn and compared with the schematic for errors. The digital blocks are described only at the schematic level. The operation is verified with a digital simulation tool such as Verilog-XL. The layout for these blocks is then automatically generated by a Place-&-Route tool.

Typical results achieved for the operational amplifiers used in the first stage are summarized in Tab. 5.3. The operational amplifiers were readjusted through simulation to meet the specifications for slow, nominal and fast process parameters. Also, the capacitors used in the design have bottom-plate parasitic values which increase the capacitive loads by about 30%, and which were accounted for in the simulations. It is interesting to note the excellent value obtained for the phase margin. This value can be improved further by reducing the size of the cascode transistors, although this would have the side effect of reducing the available signal swing. The simulated frequency response of the operational amplifier is presented in Fig. 5.15, where most of the information summarized in Tab. 5.3 is illustrated.

Parameter	**First opamp**	**Second opamp**
Gain, A_{DC}	55.3 dB	59.9 dB
Dominant pole	631.1 kHz	467.3 kHz
Unity-gain frequency, f_{ta}	387.1 MHz	462.1 MHz
Non-dominant pole	6.42 GHz	3.94 GHz
Phase margin	95.3^o	96.3^o
Slew-rate, SR	520 V/μs	398 V/μs
Output swing (differential)	1.149 V	1.098 V
Load capacitance, C_L	20 pF	3.6 pF
Power consumption for $V_{DD} = 3.3$ V	26.4 mW	3.3 mW

Table 5.3: Opamp parameters for nominal process case

To simulate the comparator, an input step of 200 mV was applied to its main differential pair, and compared against a zero threshold voltage. The transient simulation, illustrated in Fig. 5.16, shows propagation times of 2.39 ns for the rising edge, and 2.51 ns for the falling edge. These values are at the output of the first stage, before the flip-flop, and they are less than the maximum allowed time of 5 ns. The propagation time of the flip-flop and the decoder logic have effect only during phase Φ_2.

Fig. 5.17 shows a Switcap simulation of the first-stage delta-sigma modulator, as presented in Fig. 5.9. The input signal was a sinewave with $f = 3.125$ MHz and $A_u = 0.4$ V. The netlist included an opamp DC gain of 50 dB. The system was also simulated at the transistor level, but only with a bi-level quantizer, and with an ideal common-mode feedback. In this case, the input-signal frequency was $f = 1$ MHz and its amplitude $A_u = 0.25$ V (-12 dB). The resulting output signal spectrum is shown in Fig. 5.18. The DC component present in the spectrum was

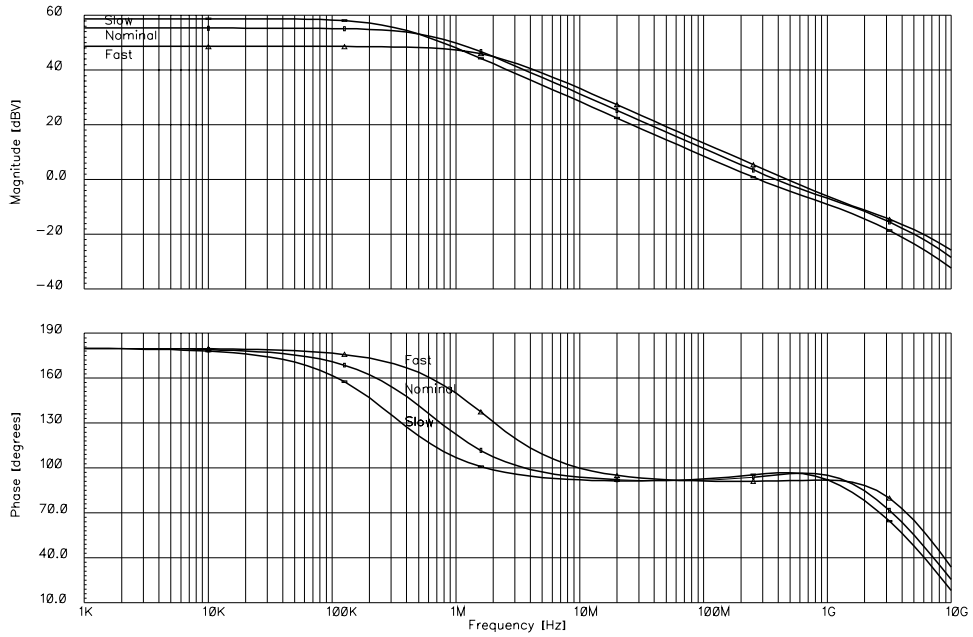

Figure 5.15: Operational amplifier frequency response

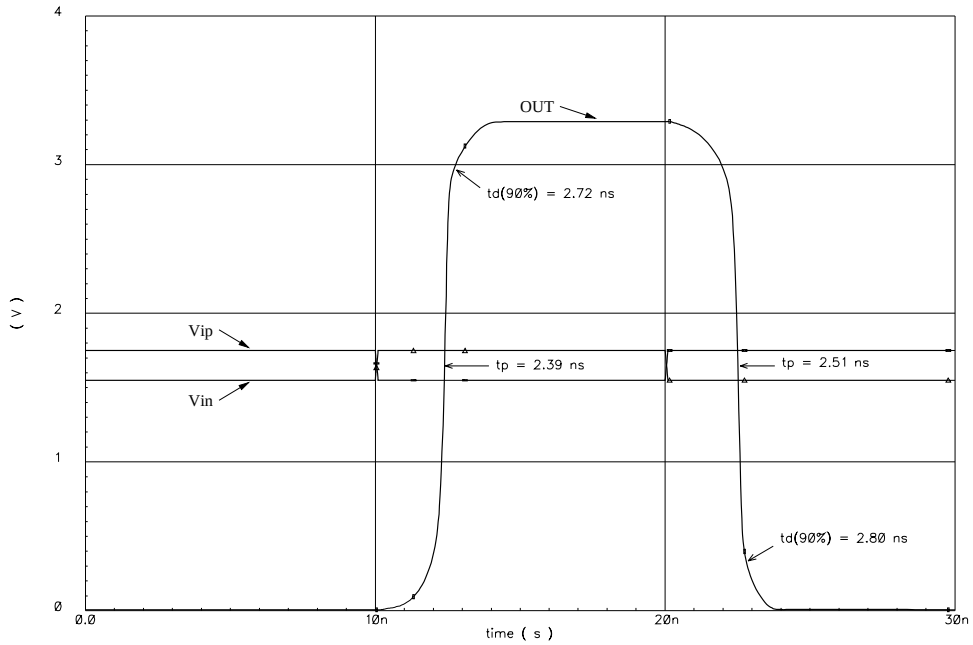

Figure 5.16: Response of the comparator to a step

due to the common-mode output voltage $V_{CM} = 1.65$ V. This last simulation was performed with low accuracy and is intended to illustrate only the functionality of the first stage at the desired frequencies.

5.5 Conclusions

This chapter presented the design of the prototype chip, with an emphasis on the issues raised by the target specifications.

For the first stage, it was seen that, to operate at the desired speed, a combination of correlated double sampling techniques with a simple opamp structure can solve the problems caused by the limited gain-bandwidth product. Also, the speed requirements of the quantizer were met by using a current-based approach, combined with positive feedback, in the comparator.

For the second stage, two techniques were presented to solve the problem of the limited sampling rate provided by the analog-to-digital converter. Also, the implementation of the test signal generator, the correlator, and the FIR filter was discussed near to logic-gate level.

Finally, the functionality of the designed blocks was illustrated with selected simulations.

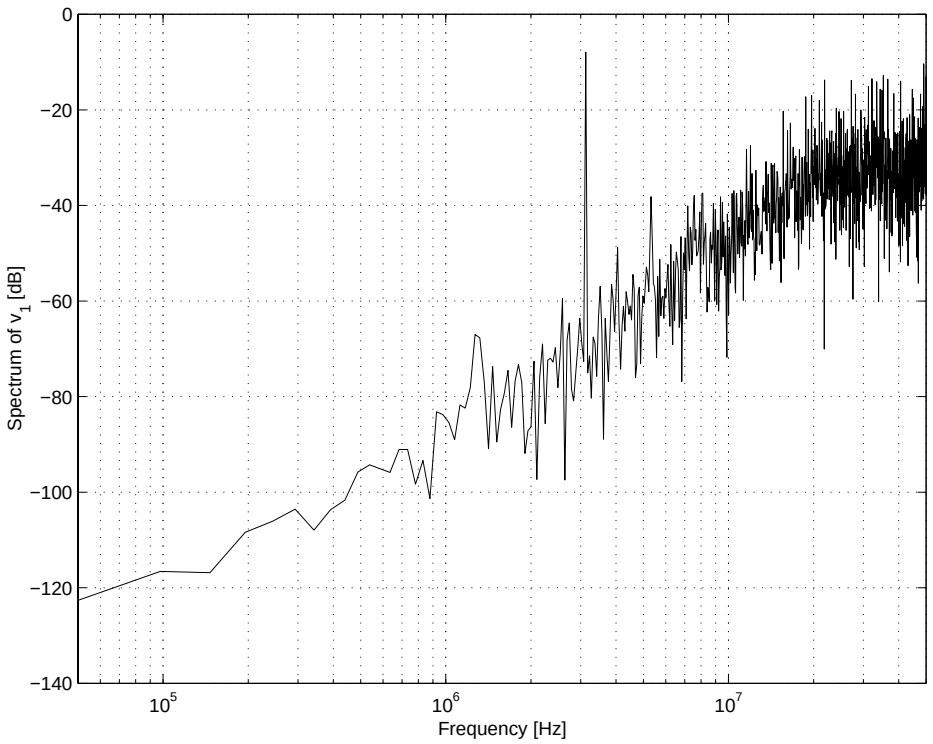

Figure 5.17: Simulation of the first stage in Switcap

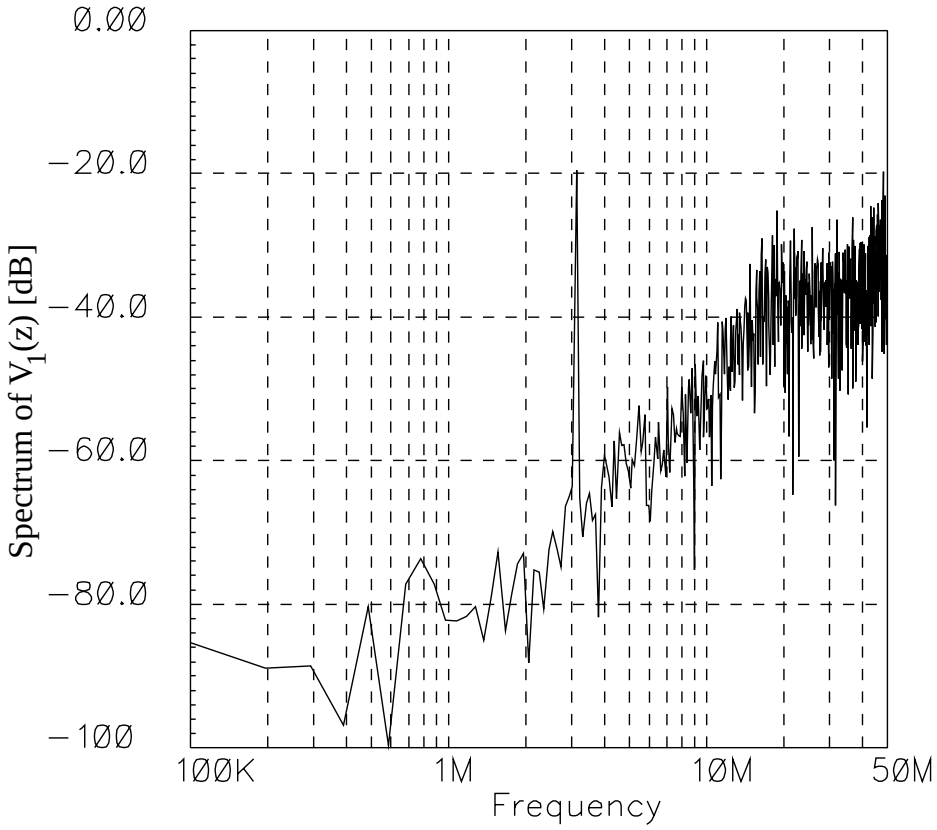

Figure 5.18: Simulation of the first stage at transistor level

Chapter 6

Conclusions and Future Work

Cascaded (MASH) delta-sigma converters offer a good compromise between high accuracy, robust stability and speed. However, they are very sensitive to analog circuit imperfections.

In this thesis, a cascaded 2-0 architecture with 1–1.5-bit first stage and 10–12-bit second stage was investigated. It uses an adaptive digital FIR filter to reduce the noise leakage due to the imperfect error cancellation. For on-line adaptation, a pseudo-random test signal was injected into the first stage and a simplified block-LMS algorithm, the sign-sign-block-least-mean-square algorithm, was used to update the coefficients of the adaptation filter.

In order to achieve the best peak-SNR performance, both the structure and the adaptive error correction of the MASH were investigated.

6.1 Improvements to the Previous Work

The basic theory and some design considerations of the adaptive digital correction method for cascaded delta-sigma analog-to-digital converters presented in this thesis were developed under previous work [27], [28], [29], [30]; also, a working prototype of the integrated ADC was successfully fabricated and tested [17], [31]. However, the reported effective results (signal-to-noise+distortion ratio $SNDR$=75 dB @ f_B=62.5-kHz signal bandwidth) validated only the principle of adaptive noise-leakage compensation, leaving open the question of how to improve this initial performance.

The current thesis deals with the improvements to this technique, and its application in a very fast (sampling frequency f_S=100 MHz, oversampling ratio OSR=8–16, signal bandwidth f_B=3–6 MHz) and high-accuracy (signal-to-noise ratio SNR=13–15-bit) implementation. Such converters have wide applications in high-speed instrumentation, high-definition video, imaging, radar and digital communications.

In order to highlight the improvements made by the author in this thesis [18], [34] to the previous design of Tao Sun [31], [17], a brief comparison is shown in Tab. 6.1.

2-0 MASH ADC structure						
interstage coefficients	α	β	m_0	m_2	m_1	*improvement:*
TS	8	0	$1/8$	8	$+1$	
PK	8	2	$1/2$	2	-1	$+6$ dB in SNR
first-stage resolution	N_1					*improvement:*
TS	1 bit					
PK	1.5 bits					$+6$ dB in SNR
second-stage resolution	N_2					*observation:*
TS	12 bits					clocked at f_S=1 MHz
PK	10 bits					clocked at $\frac{f_S}{2}$=50 MHz
Adaptive correction for the 2-0 MASH ADC						
adaptation parameters	M		B_s		$\overrightarrow{l}$	*improvements:*
TS	5		2^{15}		16 bits	
PK	5		2^{16}		16 bits	2 dB less ripple in SNR
	differentiator to $L_C(z)$					6 dB less ripple in SNR
test-signal amplitude	A_t					*improvement:*
TS	0.5 V					
PK	0.01 V					$+3$ dB in DR
Implementation of the 2-0 MASH ADC						
sampling frequency	f_S					*improvements:*
TS	1 MHz					
PK	100 MHz					challenging circuit design; $100\times$ larger f_B
second stage	*integration*					*improvements in:*
TS	off-chip ADC					
PK	on-chip ADC					noise, area, power
adaptive FIR filter $L_C(z)$	*integration*					*improvement:*
TS	off-chip adaptation					
PK	on-chip adaptive $L_C(z)$					real-time ADC
Overall performance						
accuracy versus speed	SNR		f_B			*observation:*
TS	75 dB		62.5 kHz			measured result
PK	84 dB		6.25 MHz			simulated result

Legend: TS – Tao Sun [17], [31]; PK – Péter Kiss [18], [34]; SNR – signal-to-noise ratio; DR – dynamic range; f_B – signal bandwidth; f_S – sampling frequency;

Table 6.1: Improvements to the previous design

6.2 Original Contributions

This section is intended to summarize the original contributions made by the author in this thesis.

1. **Introduction**

   - ◇ Several high-performance ADCs were analyzed and compared. It turned out that the ADC proposed in this thesis has the highest figure of merit FOM among these state-of-the-art data converters.

2. **Single-Loop Delta-Sigma ADCs**

   - ◇ An overview of the basic concepts and operation of the single-loop delta-sigma ADCs were presented in the first part of this chapter. Detailed calculations and original examples (supported by simulation results) were provided.
   - ◇ Advanced delta-sigma issues were analyzed in detail in the following sections. First, the gain of single-bit and multibit quantizers was analyzed. It was concluded that in the linearized model of a delta-sigma ADC, the gain of a multibit quantizer is defined by the position of its threshold voltages if its output is also a digital sequence of multibit words, and, on the other hand, the gain of a single-bit quantizer is controlled by the feedback loop in such a way that the product of gain factors becomes unity ($a_1 a_2 b_1 k = 1$). Second, it was demonstrated that the DC gain of the signal transfer function $STF(z)$ of a delta-sigma ADC should be chosen to be 1.
   - ◇ A 1.5-bit second-order delta-sigma ADC was designed at system level in order to achieve the most aggressive quantization noise suppression by a noise transfer function of $NTF(z) = (1 - z^{-1})^2$. The designed modulator ($N_1 = 1.5$ bits, $a_1 = \frac{1}{4}$, $a_2 = \frac{1}{2}$, $b_1 = 1$, $b_2 = \frac{1}{2}$, and $k_1 = 8$) provides well-bounded internal voltages which prevent the saturation of the opamps used in the integrators even if a small dither (test) signal is injected before the quantizer. This modulator serves as the first stage in the adaptive 2-0 cascaded delta-sigma ADC.

3. **Cascaded Delta-Sigma ADCs**

   - ◇ The structure of the cascaded delta-sigma modulator was investigated in order to improve its dynamic range DR and peak-SNR performances. The designed interstage coefficients ($\beta = 2$, $m_1 = -1$, $m_0 = \frac{1}{2}$, and $m_2 = 2$) provided 6-dB peak-SNR improvement compared with the previous work. In addition, by using a tri-level quantizer in the first stage, the usable input signal range was extended, which in turn improved the achievable peak SNR by an additional 6 dB. Note that the tri-level quantizer offers a good trade-off between SNR

performance and circuit complexity; as far as the author is aware, tri-level quantizers were not used in other implementations of 2-0 MASH ADCs.

- ◇ It was shown by simulations that the spectrum of the output of a real cascaded delta-sigma ADC is dominated by a shaped version of the first-stage quantization noise (called "quantization noise leakage") due to the imperfect analog circuits used in the implementation of the modulator.

4. **Adaptive Digital Compensation for Cascaded 2-0 $\Delta\Sigma$ ADCs**

   - ◇ Theoretical analysis and extensive simulations both demonstrated that the test signal should be a white and uniformly distributed noise in order to optimize the adaptation process.
   - ◇ The properties of the noise leakage were studied in order to determine the influence of the analog circuit imperfections on the performance of the cascaded ADC, and to build an effective compensator. The presented study indicated that a modification of the previously used adaptive FIR filter can improve the performance. Specifically, a differentiator was added to the compensation structure, which reduced the ripple of the adaptation noise significantly by 6 dB. Also, by carefully choosing the parameters of the adaptation process ($M - 1 = 5$, $K = 2^{16}$, $\gamma_{SSBLMS} = 1.5\,10^{-5}$, and $A_t = 0.01$ V), the ripple of the adaptation noise was further reduced, to the very comfortable value of 1 dB, while the dynamic range dropped only by 0.5 dB from its ideal value due to the small test signal.
   - ◇ It was shown that the minimal order of the adaptive FIR filter is 3. However, a 5^{th} order FIR filter has been implemented to accommodate unforeseen effects.
   - ◇ It was demonstrated that the proposed adaptive compensated 2-0 cascaded delta-sigma ADC provides a hardware-efficient and robust operation.

5. **Prototype Chip Design**

   - ◇ A 1.5-bit second-order switched-capacitor delta-sigma ADC was designed at the transistor level, to be operated at a high speed of $f_S = 100$ MHz. The functionality of the first stage of the adaptive MASH ADC was demonstrated by simulations.
   - ◇ The on-chip implementation of the adaptive noise-leakage compensation digital filter $L_C(z)$ was shown near to logic-gate level.

As outlined above, the optimization of the proposed adaptive compensated cascaded 2-0 delta-sigma architecture at this point is complete.

Based on a comparative analysis, it is believed that the cascaded 2-0 delta-sigma structure was optimized for peak-SNR performance, while maintaining

low-complexity implementation with a tri-level first stage. In addition, the designed adaptive on-line noise-leakage compensation digital FIR filter requires a relatively simple digital hardware, and it provides robust operation. Extensive simulations predicted an achievable SNR=13-bit @ 6-MHz signal bandwidth operation. Such a converter will be faster than any previous high-accuracy delta-sigma ADC, as demonstrated in Fig. 1.1.

6.3 Future Work

As a future work, it would be an interesting project to apply the test-signal based adaptive correction strategy to different cascaded delta-sigma structures. In addition, one could find other applications of the described method in other important areas of mixed-mode circuit applications, where the presented on-line correction technique would be useful. For example, a potential area is the digital correction for DAC nonlinearities, where a digital test signal may be injected, and then the signal itself, or a harmonic of it, adaptively cancelled in the digital domain.

Also, Section 4.3 can be considered as the outline of a new research project to gain higher accuracy (16-bit) and larger bandwidth (12-MHz) than this thesis has shown. Therefore, issues like the analog or digital correction of highly-linear multibit DACs need to be investigated, and such circuits needs to be implemented.

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