POLITEHNICA UNIVERSITY OF BUCHAREST
PhD department of Electrichal Engineering

PHD THESIS SUMMARY

802.11g STANDARD WIRELESS RADIO COMMUNICATIONS FREQUENCY SYNTHESIZER

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KEYWORDS

-Dual loop PLL frequency synthesizer
-Digital-controlled oscillator
-All digital Phase locked loop (ADPLL)
-Fix-N division factor PLL & Adjustable frequency reference
-AlN-CMOS oscillator
- BAW AlN resonator

PHD THESIS CONTENT

Chapter 1: Introduction
Capitolul 2: PLL frequency synthesizer
Capitolul 3: Dual loop WLAN frequency synthesizer having adjustable frequency reference
Capitolul 4: Adjustable frequency reference
Capitolul 5: Conclusions and original contributions

PHD THESIS SUMARRY CONTENT

1. DUAL LOOP WLAN FREQUENCY SYNTHESIZER HAVING ADJUSTABLE FREQUENCY REFERENCE

1.1.CIRCUIT DESCRIPTION

Many high frequency applications as local oscillators for various communication links or network analyzers require the synthesis of a signal having tight error margins for parameters as frequency, settling time and phase noise. A solution to this problem is the phase locked loop (PLL) synthesizer, whose block diagram is given in Fig. 1

The desired signal is provided by the voltage-controlled oscillator (VCO) at its terminal Fout. Usually the frequency reference (FREF) is a quartz oscillator, known for its stability of the oscillation frequency.

The phase and frequency detector (PFD) compares the reference signal REF with the divided oscillator signal available at Fout of the frequency divider (DIV). PFD gives the UP command if Fref > (Fout of DIV) or the DN (down) command if FREF<(Fout of DIV}.

The charge pump (CP) can give at its terminal OUT a positive or a negative current. After being filtered by a low pass filter (LPF), this signal is applied to the VCTRL terminal of the voltage-controlled oscillator (VCO). The positive current increases the oscillation frequency of VCO, while the negative current diminishes its value. PFD has a “dead zone” corresponding to no UP or DOWN output signal (see Fig. 1).

Usually, FREF is an oscillator providing a constant oscillation frequency. In the classical solution the desired VCO frequencies are those imposed for the transmission channels of wireless standard 802.11g, which are obtained with different division ratios of DIV, while the FREF has a constant frequency.

A new approach to a frequency synthesizer is proposed: instead of a fixed frequency reference oscillator and a variable ratio frequency divider we use a variable frequency reference oscillator and a fixed ratio frequency divider.

Moreover, the classical passive quartz resonator is replaced by an active AlN bulk acoustic wave (BAW) resonator which can be built in the same system on a chip (SoC) with the electronic CMOS circuit, due to the high compatibility between these technologies [3].

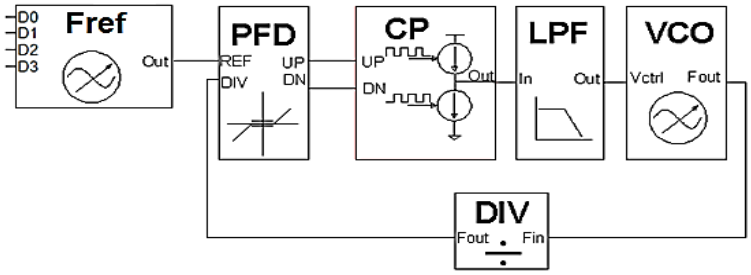

Fig. 1 Block diagram of a PLL synthesizer

In top of that a dual loop architecture is used. This solution has the advantage of a reduced phase noise and settling time with respect to the single loop synthesizer.

The block diagram for this approach is that in Fig. 2. The differences with respect to the classical solution are: the frequency reference gives an output with variable frequency, and the division factor of DIV is constant.

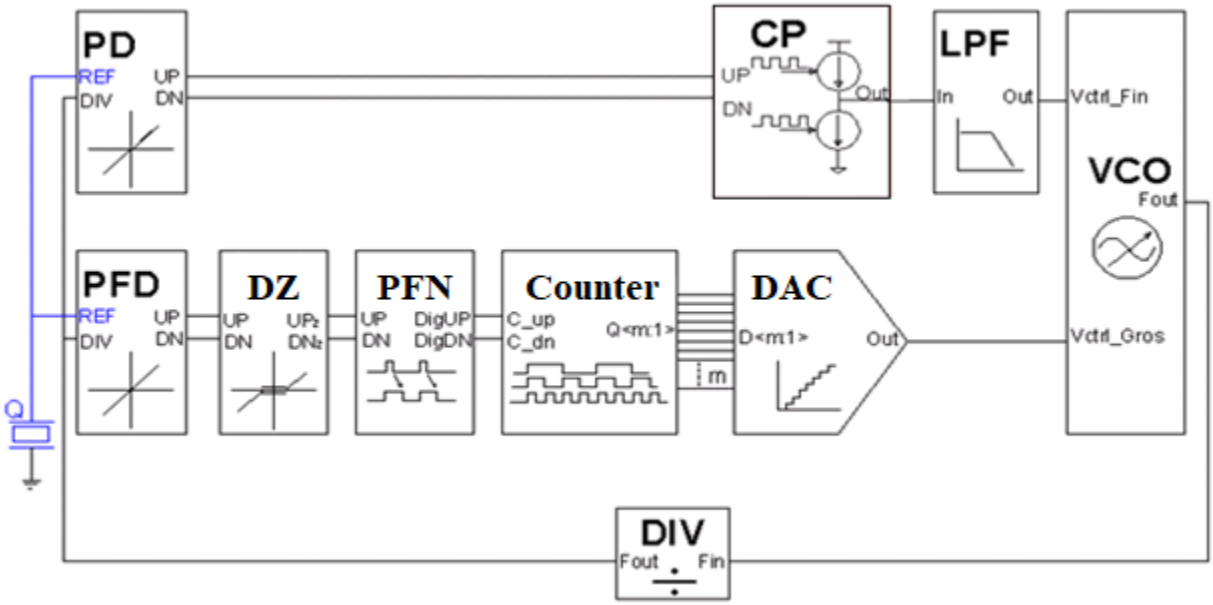

Fig. 2 Dual loop frequency synthesizer

The voltage controlled oscillator has two control inputs, one for a fine frequency adjustment (Vctrl_Fin) and the other for a coarse frequency adjustment (Vctrl_Gros).

The way in which the contributions of the two loops are summed on the oscillator using two different control elements is clearly superior to the way the summation on the filter goes down mainly for two reasons: a) the oscillator would have had a single variable capacitor of very high value involving a high phase noise, at the same time fails to achieve a sufficiently small frequency variation step, b) the low pass filter with high value capacitors, the contribution of the fine-tuning loop does not get to be used at maximum performance.

The first loop presents a predominantly analog topology and controls the low gain input (fine control) of the Vctrl_fin oscillator. The working mode of this loop is on the signal level, so the pulse width from the output of the PD phase detector circuit dictates the size of the frequency jump from the synthesizer output. As we saw in subchapter 2.1, the control on the signal level generates phase noise problems if the gain of the charge pump is high. In our case we minimized the phase noise of the system by achieving a small gain of the charge pump.

1.2.DIGITAL LOOP

The second loop presents a predominantly digital topology and controls the high gain input (coarse control) of the oscillator (Vctrl_Gros). The mode of operation of this loop is on the front of the signal. This way of working has a huge advantage for our application, because we will be able to use it efficiently in the control of the VCO oscillator using extremely narrow pulses from the PFD output. Since we replaced the charge pump we have the advantage that no matter how big

the pulse width from the phase detector output and the PFD frequency, the switching noise will be the same, becuse the synthesizer changes its output frequency with a well determined step with the clock signal transition of the counter (active on the rising front). As we saw in subchapter 2.3, fully digital systems have a limitation of the output frequency range due to the finite states of the counter, this being the main reason why we chose to design a system with two PLL loops.

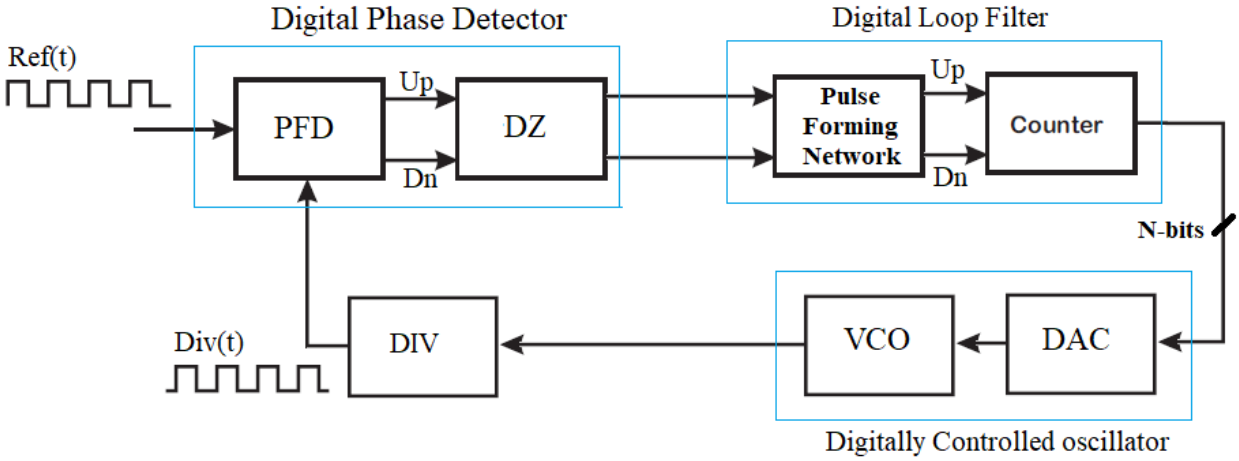

Fig. 3 Digital loop schematic

The digital adjustment loop consists of the following blocks:

-Digital phase and frequency detector (Digital Phase Detector). This block consists of a sequential phase and frequency detector (PFD) to which is added a block that introduces a dead zone in the detection characteristic (DZ). The phase and frequency detector (PFD) provides a digital voltage whose pulse width is proportional to the phase difference of the two input signals. Dead Zone (DZ) circuit that has the role of setting the detection sensitivity of the coarse adjustment loop. In this way, the operation of the digital loop can be limited only in the acquisition mode.

-Digital Loop Filter. It consists of a pulse forming circuit (Pulse Forming Network = PFN) which has the role of controlling the reversible counter on N bits (Counter). The PFN circuit increases the width of the narrow pulses from the DZ output up to 50% of the reference clock period, in order to be able to control the counting direction. The reversible counter (Counter / NR), increments or decrements the output of the digital-to-analog converter DAC depending on the control signal received at the input.

-Digitally controlled oscillator. It consists of an analog-to-digital converter (DAC) and a voltage controlled oscillator of type LC (VCO). Digital to analog converter (DAC) controls the voltage of the VCO oscillator. The variation of the output frequency of the synthesizer is made with the help of the input voltage of the VCO oscillator.

- The frequency from the output of the VCO oscillator is divided by the frequency divider DIV with a fixed division factor N = fixed. The frequency divider is common to the two phase-mounted loops in the frequency synthesizer component.

The phase frequency detector compare the phase of the reference signal Φref(t) with the digital controlled oscillator divided phase Φdiv(t): vd(t)=f(Φdiv(t)– Φi(t)). If Φdiv(t)> Φi(t), on the PFD output, is active UP output, otherwise, will be active DN output. The PFD output signals

(UP1 or DN1) are tiny pulse width. Pulse width modulator (PWM) increase the pulse width of phase frequency detector output signals (UP1 or DN1). The up/down counter, change state in either direction, under the control of an up/down selector input, that cams from the pulse width modulator output. When the selector is in the up state, the counter increments its value. In this case, the digilat controlled oscillator receives at the input commanda to increase the output frequency. When the selector is in the down state, the counter decrements the count. In this case, the digilat controlled oscillator receives at the input commanda to decrease the output frequency. A change in frequency, is proportional with a phase shift. In this way we controll the output frequency to stay fix at the wanted frequency, upon the reference frequency.

1.3.SIMULATION RESULTS OF DUAL LOOP FREQUENCY SYNTHESIZER

The design and transistor-level simulation of each block in the DPLL circuit was done using the SPECTRE simulator in the CADENCE environment, using the 0.18um technological process from TSMC. The frequency synthesizer simulation is partially performed using the models described in the verilog language due to the limited processing resources of the computer used in running the simulations.

The parameters of the frequency synthesizer used in the simulation are presented in the table below:

Table 1 Block parameters used in simulation

Fine-tuning analog loop and coarse-tuning digital loop		
Reference frequency Fref	100MHz	
VCO output frequency	4.8GHz	
Division factor	25*2=50	
CP current	50uA	
Low gain VCO input	10MHz	
Hight gain VCO input	200MHz	
Analog Low pass filter param.	Rz	**62Kohm**
	Cz	**6.33pF**
	Cs	**101pF**

In the following figure we have the test schematic of the dual loop frequency synthesizer.

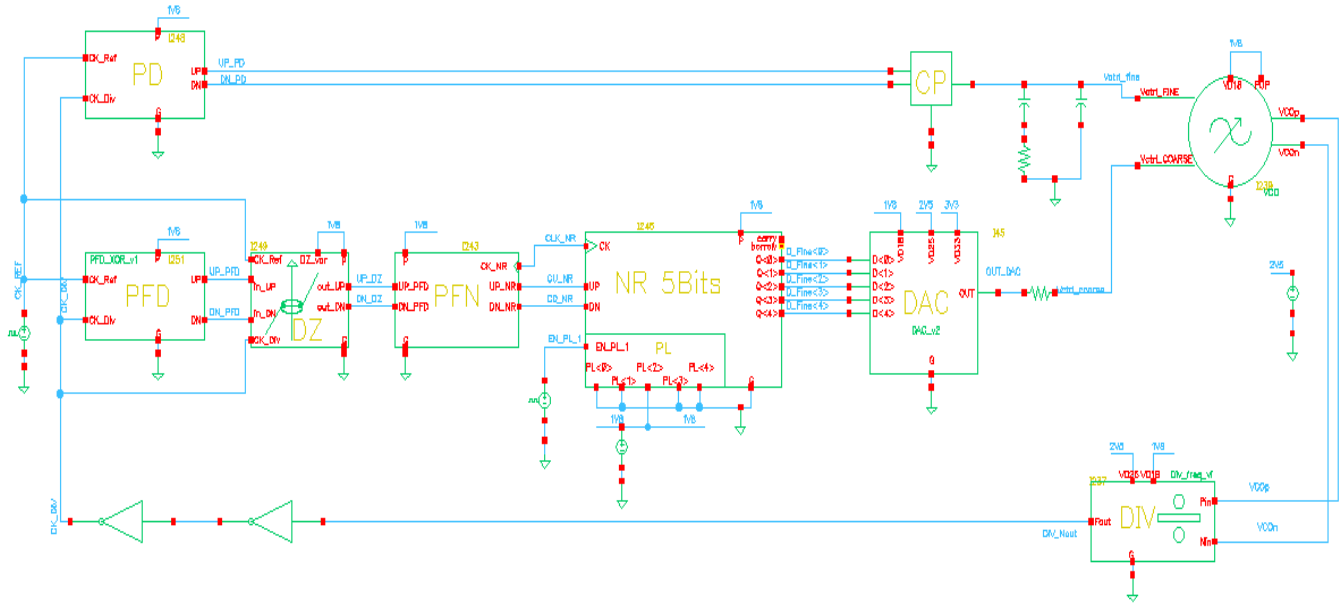

Fig. 4 Test schematic of dual loop frequency synthesizer

The result of the simulation in the transient domain of the two-loop frequency synthesizer are presented below:

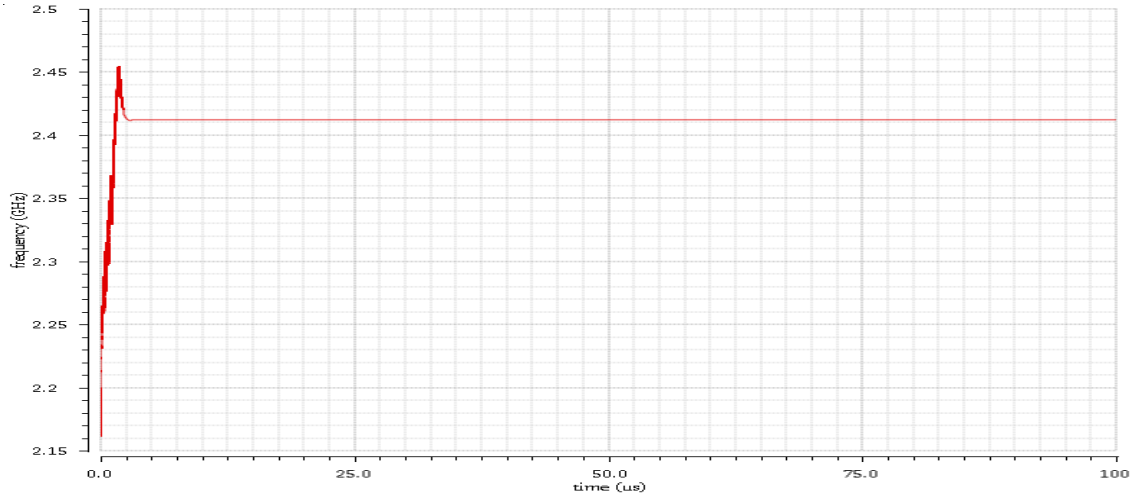

Fig. 5 Start up synthesizer frequency response

The figure above shows the output frequency of the two-loop frequency synthesizer, simulating the most unfavorable case for setting the frequency, namely at startup. It can be seen from the figure that we have a fast setting time, after up to 100us the output frequency of the

synthesizer remains stable.

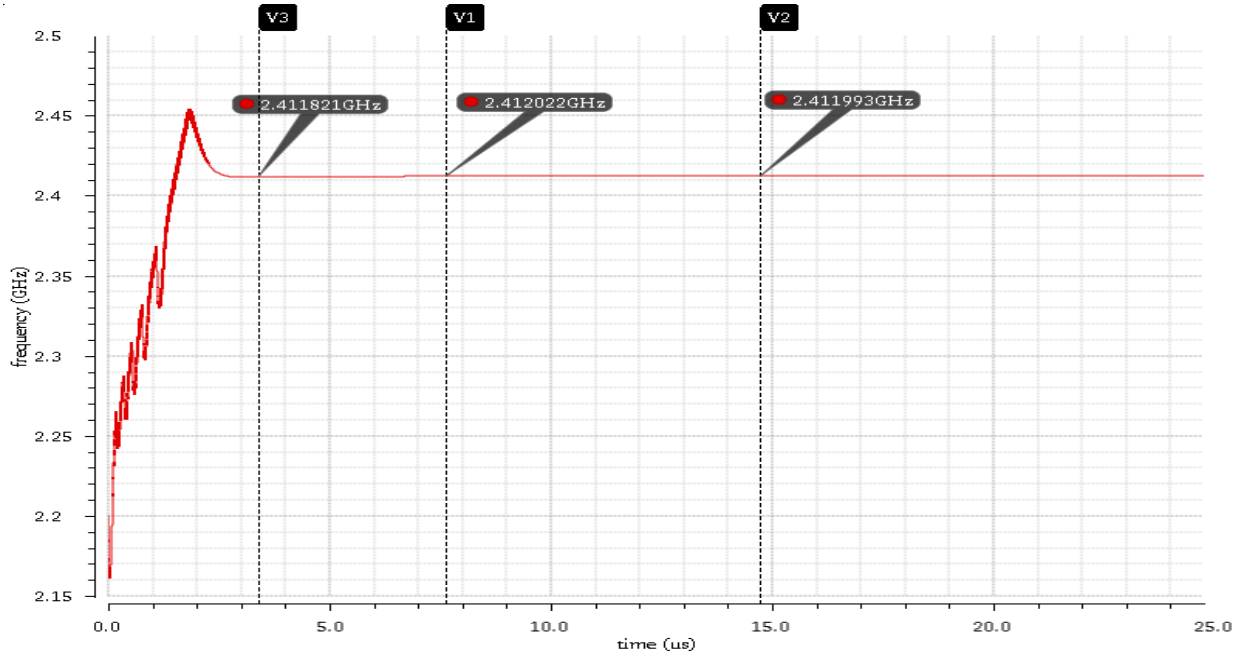

Fig. 6 Zoom of Start up synthesizer frequency response

The figure above shows only the beginning, the first 25us of the simulation to be able to see in detail how the frequency stabilizes. A very fast acquisition regime of up to 3us is observed, following a stabilization of the frequency up to 6.7us near the desired frequency. After 6.7us we can say that the loop has stalled and is working in tracking mode because it reaches the set frequency with a tolerance that falls within the accuracy of ± 25ppm calculated to be 60KHz. It is also observed that the transient regime shows some fluctuations with increases and decreases, behavior that can be caused by the so-called "cycle sleep" phenomenon, the main cause being the phase and frequency comparator that has a detection limitation.

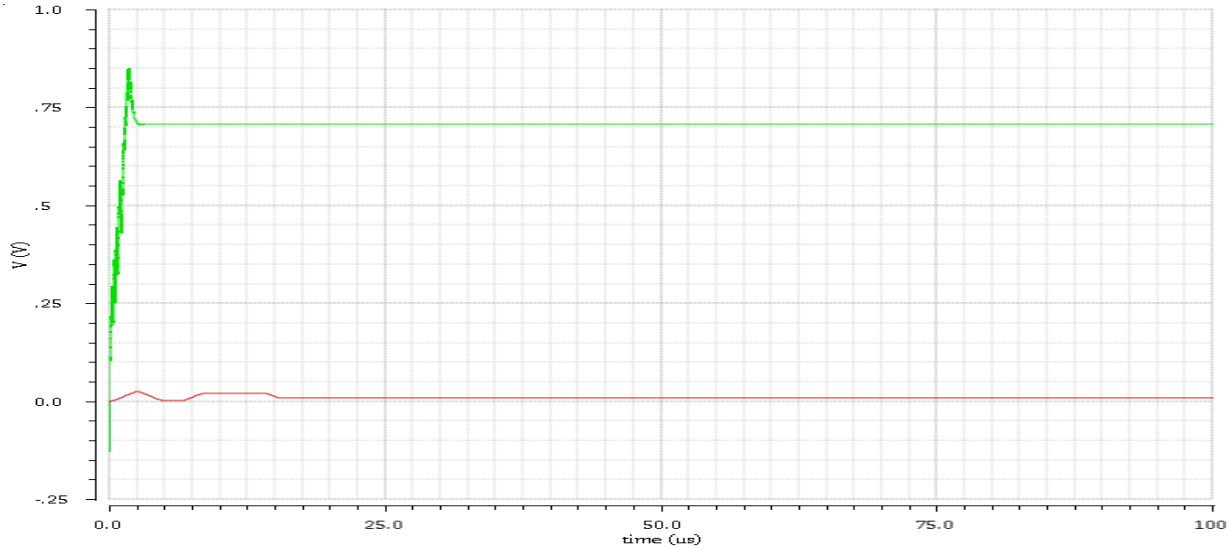

Fig. 7 Voltage control oscillator red=fine tunning and gren= coarse tunning

The figure above shows the oscillator control voltages for the fine reflection (red) and coarse frequency adjustment (green) inputs.

It is observed that the voltage for the coarse control (green) has the same look as the evolution of the output frequency because it is the predominant contributor. It is also observed that we have fast jumps that denote the broadband of the digital filter and the predisposition towards a fast response of the system necessary to obtain a fast frequency time.

It is observed that after 3us a stabilization of the coarse adjustment voltage (green) following that the fine adjustment voltage (red) to determine the final oscillation frequency. We have a slow variation of the control voltage of the fine frequency adjustment (red) which highlights the fact that it filters the high frequency signals to improve the phase noise of the system.

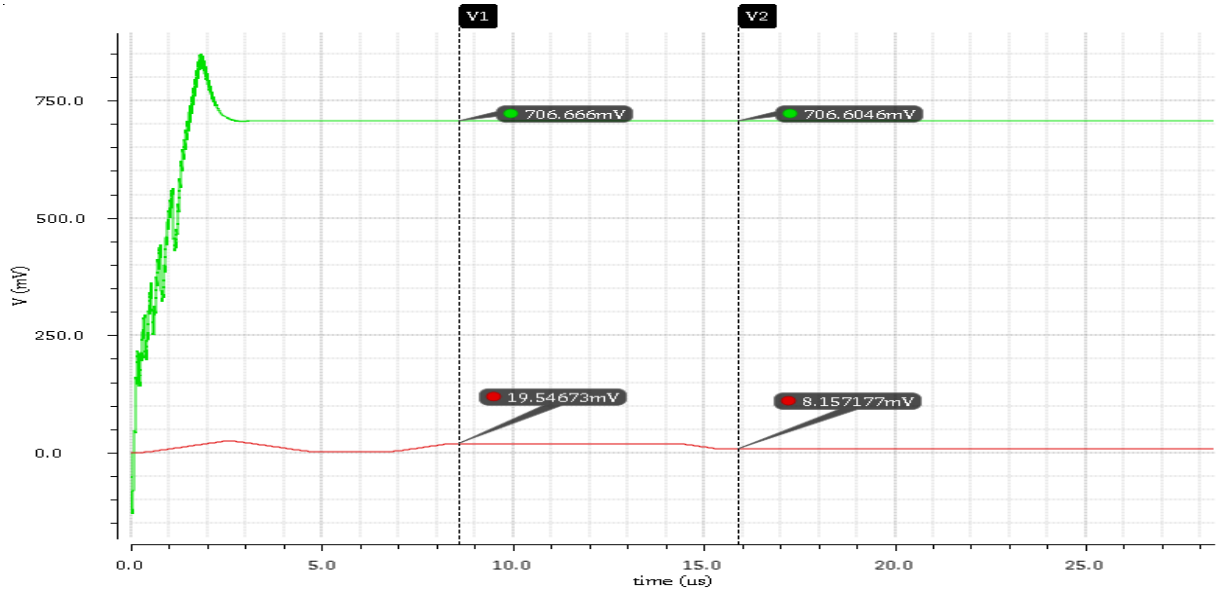

Fig. 8 Voltage control oscillator startup zoom

The figure above is focused on the beginning, the first 25us to observe in detail the voltage variation described above.

The signal from the input of the frequency oscillator faithfully mirrors the variation of the signal from the output of the frequency synthesizer. Thus, based on the control voltage at the input of the oscillator, we can determine the moment when the frequency synthesizer reached the tracking mode where the output frequency of the synthesizer is equal to the input frequency multiplied by the loop splitting factor.

2. FREQUENCY REFERENCE

2.1.CIRCUIT DESCRIPTION

A new approach with respect of the above one is proposed in this paper, namely a PLL frequency synthesizer using a frequency reference, which provides a signal having a set of frequencies, so that the desired set of VCO frequencies can be obtained with a divider whose division ratio remains unchanged.

The frequency reference scheme is presented in the figure below:

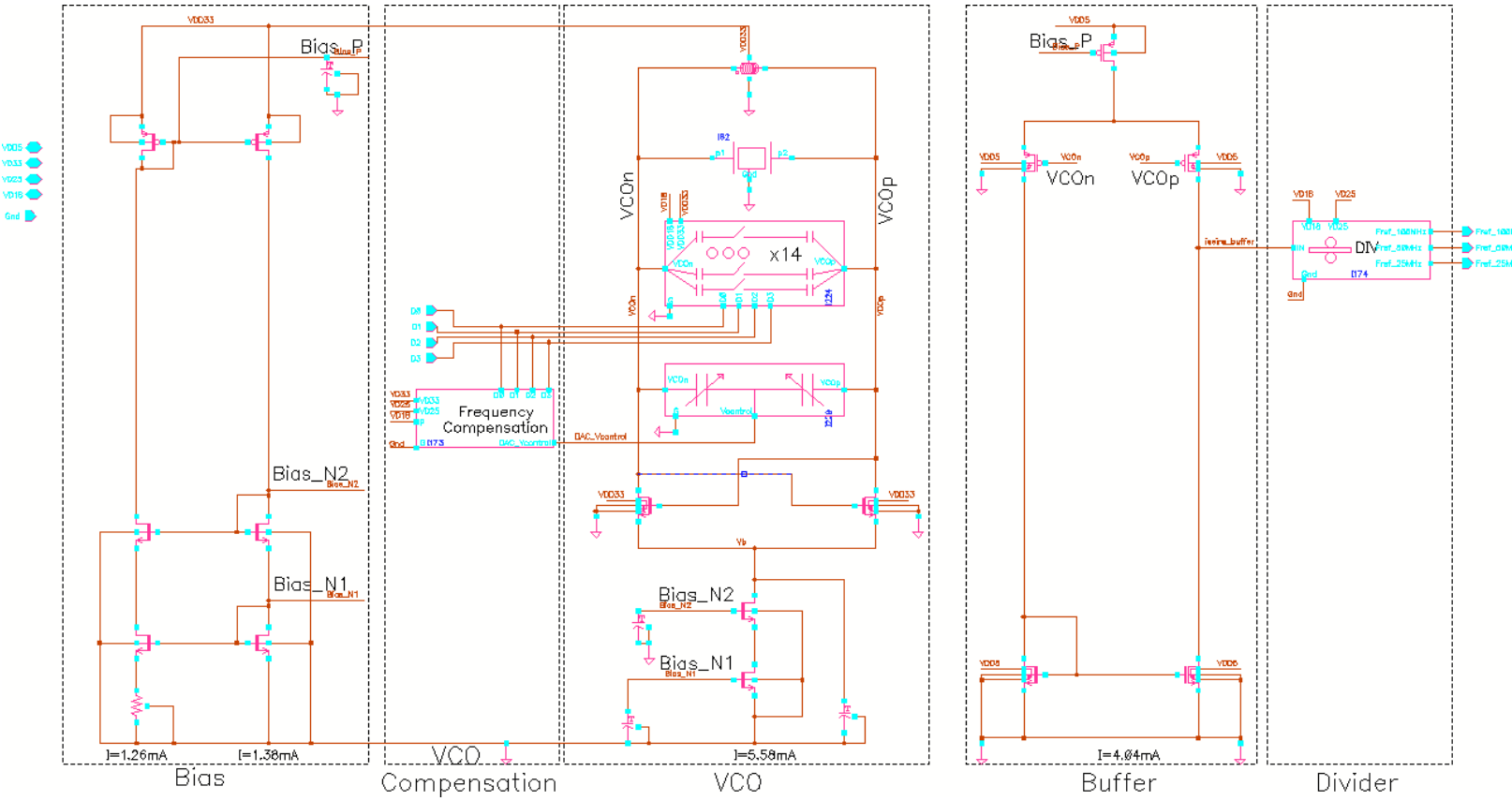

Fig. 9 Variable frequency reference schematic

In above figure, the implementation and characterization of a low phase-noise compensated oscillator (VCO) used as frequency reference for a WLAN wireless transceiver is described.

In this case the frequency reference block Fref contains the blocks in Fig. 2: BIAS (the circuitry for DC supply), VCO (reference oscillator), Compensation (calibration circuit), BUFFER(output buffer), and Divider (frequency divider).

This circuit employs a high Q piezoelectric resonator together with a CMOS cross coupled pair amplifier. A calibration circuit for compensation of frequency errors with respect to process variation is proposed (Compensation).

The DC polarization (BIAS) of the active circuit is made using a Widlar cascoded voltage reference, a 3.3V voltage supply and has a total current consumption of 2.64mA.

The buffer circuit (BUFFER) it is a PMOS differential pair amplifier with a NMOS current mirror active load and a PMOS current source, having a 5V supply voltage and 4.04mA current consumption.

The divider by 10 (DIVIDER) is made with two classical dividers, a divider by 2 followed by a divider by 5.

2.2.CALIBRATION CIRCUIT

The AlN BAW resonance frequencies are influenced by temperature and changes of the technological process. Two types of methods are applied for the frequency drift compensation with temperature of a BAW AlN oscillator working in a certain frequency band. The first one uses a passive compensation, which can lead to a minimum relative error of ±40ppm frequency shift over the entire temperature range [10]. The second one employs an active way of compensation and can lead to a minimum error of ±10ppm over the entire frequency range [11].

The CMOS process changes can lead to variations up to 30% of capacity or resistance values. In the AlN BAW technology, the piezoelectric layer thickness can vary from sample to sample leading to deviations of fs and fp, also.

Some methods based on trimming using passive circuit elements, which compensate OSC frequency errors are described in [12] and [13]. These methods are suitable just for one output frequency; for multiple frequencies their associate testing cost being increased by the trimming process.

Taking into account that a wireless transceiver is placed usually inside a building, this location having no significant temperature variations, a new approach to compensate frequency errors with respect to process variation is proposed. The block schematic of the oscillator calibration circuit is given in Fig. 10.

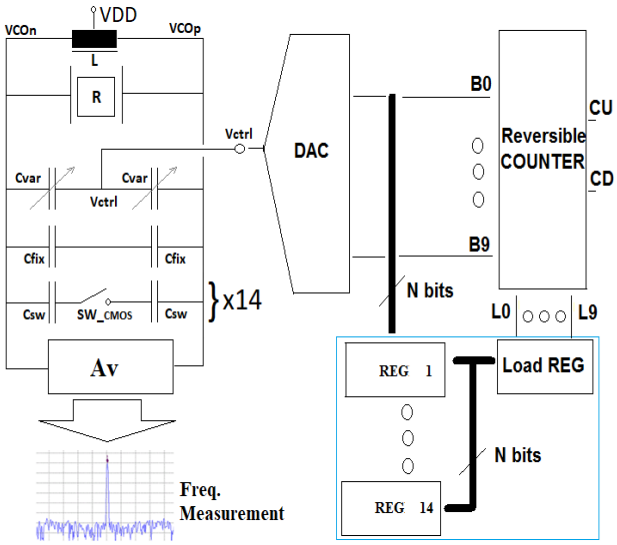

Fig. 10. Block schematic of the calibration circuit

The upper left part of Fig. 10 shows the capacitors in Fig. 6, which are used to obtain the desired oscillation frequencies. The frequency reference calibration is performed for each of the 14 output communication channels when the wireless transceiver is tested. The channel is selected using the appropriate Csw fixed capacitor pair by closing the appropriate set of SW-CMOS switches. At each frequency we drive the Reversible COUNTER to count up (CU) or to count down (CD) in order to sweep the full range of Vctrl values from the output of the digital to analog converter (DAC). The DAC output voltage controls the variable capacitors Cvar till the desired frequency is obtained. When the Spectrum Analyzer measures this value in the reference output, the reversible counter digital output is recorded in the appropriate nonvolatile register (REG1, …, REG14). After the calibration process, the result is a 10 bits digital code for each channel frequency generated by this circuit.

In the normal operation of the frequency reference, when a communication channel is selected with a 4 bits digital word, the same word is used to select its 10 bits code for frequency calibration recorded in the nonvolatile memory. This code is loaded into a 10 bits load register (Load Reg) which controls the reversible counter, in order to command the DAC output voltage to drive variable capacitors Cvar to the values corresponding to the prescribed channel frequency.

2.3. SIMULATION RESULTS OF FREQUENCY REFERENCE

2.3.1.Spectral analysis

Spectral analysis results of the reference frequency circuit for the unbuffered OSC, containing all 14 output frequencies is given in Fig. 11. This picture gives a measure of spectral purity of the unbuffered OSC.

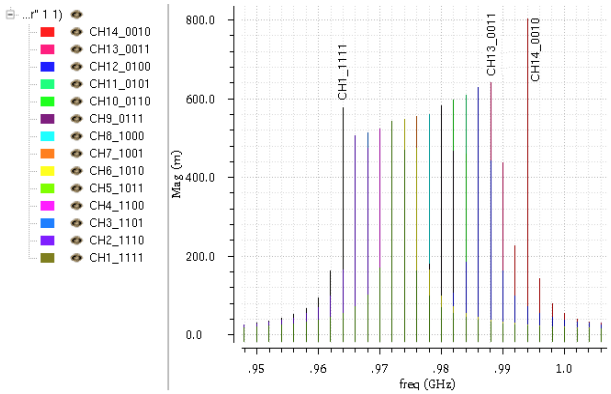

Fig. 11. Spectral analysis of unbuffered OSC

We observe the ascendant trend of the oscillation amplitude for the last 13 frequencies. This effect can be explained by the lowering of the total Q factor determined by adding a new CMOS capacitor in parallel to a BAW resonator, due to the low Q of CMOS capacitors and to the capacitor switch resistance.

As BUF is an amplifier whose output signal is limited by its DC supply, its output signals have the same amplitude for all frequencies.

2.3.2 Phase noise

The 802.11g standard specification regarding the phase noise requirement is described by Interference=+35 dB (measured at 25 MHz offset from the carrier). The phase noise analysis for all 14 channel frequencies, performed at the OSC output (Fig. 2) is presented in Fig. 12. These results are computed with PN analysis of CADENCE. The maximum value of the phase noise is -176.7 dBc/Hz obtained for the channel 5 (Fig. 12). This value complies with the specifications of the 802.11g standard [14].

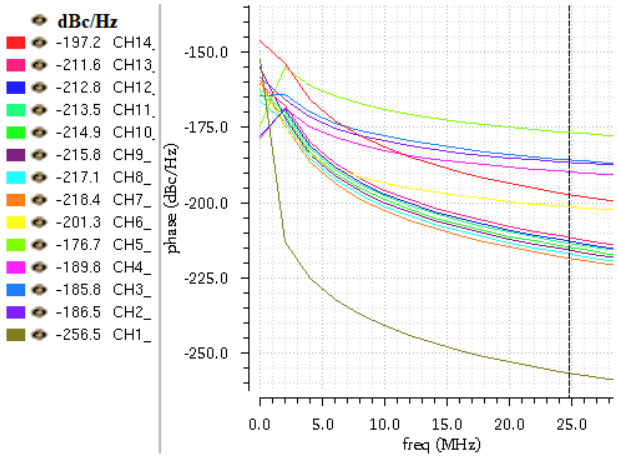

Fig. 12. Unbuffered OSC phase noise analysis

2.3.3 Frequency stability

In order to improve the frequency reference stability, the VCO is designed at high frequency, around 970 MHz. Using the frequency division by 10 the frequency deviation against median value is decreased 10 times. Starting from 802.11g standard specification with ±25 ppm an allowed frequency deviation of ±600 KHz results in the range of 2.4 GHz. At the OSC output, where the simulation result in Fig. 13 is given, this allowed frequency deviation is ±24KHz (between 24.84 KHz for CH1 and 24 KHz for CH14). The simulation results computed with the freq_jitter analysis of CADENCE are given in Fig. 13 and comply with these limits.

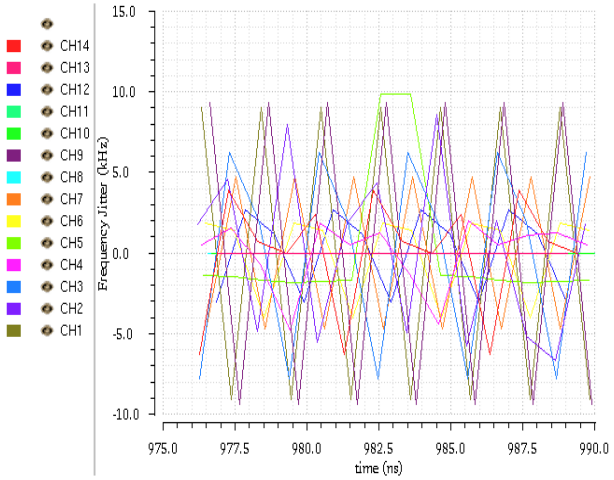

Fig. 13. Unbuffered VCO Jitter analysis

2.3.4 Settling time

The settling time according 802.11g standard specification need to be 224µs for the whole 2.4GHz frequency synthesizer. For the unbuffered frequency reference settling time we impose a limit below 1% (2.24µs) of the total settling time of the wireless transceiver. The maximum settling time is the time to change between communication channel frequencies; The start-up time represents the worst case. Next picture presents the simulation results for the worst case (start-up settling time) for all 14 VCO unbuffered output frequencies.

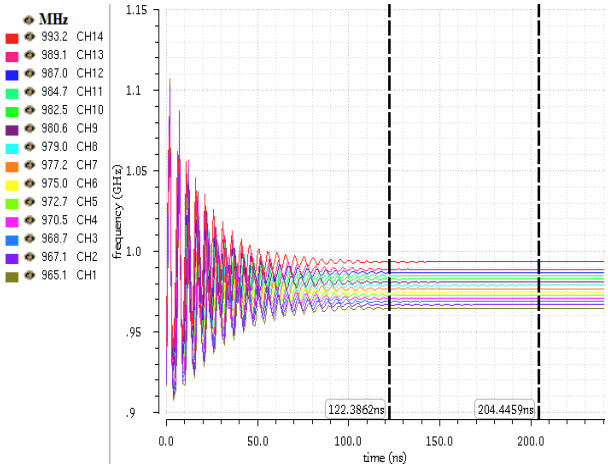

Fig. 14. Unbuffered OSC settling time analysis

We observe that settling time is different across output frequencies. The values are between 122.3ns and 205ns worst case, representing a value smaller than 10-3 from 224µs (the total settling time of a frequency synthesizer given in the 802.11g standard specification) [14].

4. CONCLUSIONS

The approach proposed in this paper has several advantages:

- The possibility to include the MOS circuitry together with the AlN BAW resonator in a system in a package (SiP).
- Using a frequency reference providing a variable frequency signal, the FDIV has a fixed division ratio for all channels of the wireless transceiver. This approach eliminates a main source of noise in the classical solution – the FDIV with variable division factor.
- A compensation circuit for the process variation has been proposed, in order to satisfy the specifications of the wireless standard 802.11g regarding the parameters of the carrier signals for all 14 communication channels.

In order to prove these advantages, some simulations using several CADENCE analyses have been performed, using the design kit of the TSMC 180nm technology.

3.CONCLUSIONS AND ORIGINAL CONTRIBUTIONS

3.1. GENERAL CONCLUSIONS

This doctoral thesis presents two frequency generation solutions within WLAN wireless radio communications systems. The first solution is a variable frequency reference that has fourteen output frequencies for a phase-locked loop. The second solution is a dual-loop frequency synthesizer PLL , which uses the frequency reference block mentioned above. Both circuits are compatible with the 802.11g WLAN communication standard which serves fourteen communication channels in the frequency range 2.412 GHz - 2.484 GHz.

The results of the electrical simulations are obtained using the Specter simulator from the CADENCE design environment. The 0.18um technological process used in the simulations comes from the manufacturer Taiwan Semiconductor Manufacturing Company (TSMC).

In the first chapter is presented the WLAN wireless communication standard as an operating application for the dual loop PLL frequency synthesizer. It begins with a brief introduction to the field of wireless WLAN communication systems, and will address the most important parameters in the design of a frequency synthesizer for the WLAN communication standard 802.11g. There are a number of problems in wireless communication systems due to deviations of the block parameters in the PLL frequency synthesizer.

The second chapter introduces the field of frequency synthesizer circuits. The frequency synthesis methods are presented and we will focus on the principle of indirect frequency synthesis, based on a phase locke loop (PLL). This technique was imposed, both due to the performances related to the broadband of the generated frequencies, the small step of variation and the stability of the output frequency.The main types of PLL are highlighted, and we will focus on two types of phase-locked loops (DPLL and ADPLL).

The frequency synthesizer proposed in this paper is a dual loop architecture, one PLL loop presents the characteristics of digital PLL circuits (DPLL) and the other the characteristics of all digital PLL circuits (ADPLL). For both DPLL and ADPLL, the advantages and disadvantages are presented in order to easily highlight the performance and weaknesses of entire dual-loop frequency synthesizer presented in Chapter 3.

DPLL loop can have several ways of implementation in terms of component blocks used [with or without charge pump, active or passive LPF filter, oscillator type (LC; ring oscillator, etc ...)] . It was considered the presentation of a DPLL that contains the charge pump and LC type oscillator also called CP-PLL because it is the most common topology used in radio communications due his performance. The component blocks, their operation mode and the problems encountered in the CP-PLL are presented.

The ADPLL can also have several ways of implementation in terms of the component blocks used. A review of the component blocks and the implementation modalities is made, following to briefly describe the blocks that are used in the synthesizer proposed in chapter 3.

The circuit proposed in Chapter 3 is designed to meet the design specifications for the WLAN 802.11g communication standard.In the first part of chapter 3 is presented the operation

and design method of the proposed dual loop frequency synthesizer. The simulations performed in the third part ensure that the proposed frequency synthesizer system complies with the requirements imposed by the 802.11g WLAN standard.

In the last part of chapter 3 we have a description of the blocks in the component of the proposed frequency synthesizer and how they work.The current trend is towards the digitization of analog architectures for reasons of area, power, portability of the project to other production technologies. In order to meet the problems of the CP-PLL loop and those of the ADPLL loop reported in Chapter 2, the diagram of a new dual loop frequency synthesizer is presented. At the same time, in order to optimize the compromise achieved in the design of a PLL circuit related to two parameters: noise and frequency settling time, two feedback loops are proposed.The first fine tuning loop of the oscillator is of DPLL type, it has a small gain (gain) on the loop and determines a fine adjustment of the frequency at the system output. Because only the DPLL loop will work in the tracking mode, we will have excellent phase noise performance due to the small gain on the loop that helps us to avoid fast frequency jumps. The filter of this loop is dimensioned with a low cutting frequency to limit the rapid variations of the oscillator control voltage.

The DPLL loop is predominantly analog, consisting of a single digital block: the PD phase detector and the following analog blocks: the CP load pump and the LPF low-pass filter.The second coarse adjustment loop of the oscillator is of ADPLL type, it has a high gain (gain) on the loop and the step of varying the output frequency of the system is approximately equal to the frequency range of the DPLL loop. We say approximately because it is necessary to have a 20% overlap of the DPLL bands between two consecutive steps of the ADPLL frequency. Because in the acquisition (capture) mode, the ADPLL loop will have a majority behavior, it determines a fast settling time with the help of the large gain on the loop. The low pass filter must have a high cutoff frequency to respond quickly to the loop, but at the same time a higher noise component will pass to the oscillator.

The ADPLL loop is mainly made of digital blocks: phase and frequency detector (PFD), Dead_zone circuit (DZ), pulse forming circuit (PFN), reversible counter (Counter) and a single mixed block (digital-to-analog converter).The frequency divider that closes both loops (DPLL and ADPLL) has a fixed division factor, the variation of the output frequency of the synthesizer is made using the frequency reference presented in Chapter 4. Achieving the performance of using a frequency divider very simple a The major advantage of the proposed phase and frequency synthesizer is that it avoids the noise introduced by a high complexity frequency divider such as the whole or fractional type.

Another major advantage of the proposed new dual loop frequency synthesizer is the combination of the phase noise performance of the DPLL loop with the advantages of a fast ride time of the ADPLL loop. Combining the two types of loops, we obtain a system clearly superior to the one with two DPLL loops or two ADPLL loops.

The fourth chapter deals with the design of a variable frequency reference intended to operate together with the frequency synthesizer with fixed division factor proposed in Chapter 3. Thus the frequency at the output of the frequency synthesizer is changed by varying the reference

frequency. You can select fourteen output frequencies that serve the fourteen communication channels within the 802.11g wi-fi standard.

The design and simulation of the electrical circuits of the frequency reference were made in CMOS 0.18um TSMC technology. Not having a BAW resonator design technology produced in AlN technology, an equivalent BDV model with ideal elements was used in the simulations. In order to have an accurate measurement of the resonator model, we used a parameters of BAW resonator produced in AlN technology [107].

Frequency stability and phase noise are the main characteristics of a frequency reference. Each block in the frequency reference component has been designed to minimize noise sources so that the total frequency reference noise is minimal.

This frequency reference is made of a high precision variable oscillator that combines the advantages of achieving a Q quality factor of over 1000 of a resonator produced in AlN technology and the versatility of the circuits produced in CMOS technology.

The oscillator amplifier A consists of a differential pair of NMOS transistors. The resonant circuit is a combination of a BAW piezoelectric resonator and an LC CMOS resonator. MEMS BAW micromechanical resonators have a high Q quality factor and facilitate the trade-off between power consumption and selectivity (Q), having a high potential for versatility with multiple frequency bands [143]. The BAW type piezoelectric resonator made in AlN technology can be easily integrated with the CMOS production process so the variation of the output frequency is made with a series of switched CMOS capacitors.

In order to compensate the variations of the output frequency due to the variation of the technological production process CMOS, the present paper proposes a calibration circuit of the frequency variation with the variation of the technological process. The calibration method involves measuring the fourteen obtainable output frequencies after encapsulation and storing the calibration code for each frequency that compensates for the deviation from the nominal value in a non-volatile memory area (eg fuses or EPROM memory). Thus, in the normal operation of the synthesizer circuit, with the same four bits that select the fourteen output frequencies, the unique calibration code corresponding to the selected frequency will be activated.

3.2 ORIGINAL CONTRIBUTIONS

In this doctoral thesis the following original solutions can be highlighted:

3.2.1 Dual loop and fix division factor frequency synthesizer

Chapter 3 presents original contributions of Dual loop and fix division factor frequency synthesizer:

3.2.1.1 Fix frequency division factor

The whole or fractional frequency divider are noise generating circuits due to the additional logic needed to be able to change the division factor. By changing the output frequency of the

synthesizer using the variable frequency reference [see chapter 4], it gives us the chance to use a divider with a fixed division factor. Thus, the structure and complexity of the frequency divider circuit are substantially simplified, implicitly decreasing the related noise.In the literature we did not find a frequency synthesizer with a phase-locked loop that works at high frequency (2.4GHz, WiFi communications) and has a divider with a fixed division factor.

3.2.1.2 Dual loop frequency synthesizer: DPLL and ADPLL

The literature presents many examples of synthesizer circuits with dual digital phase lock loops (DPLL) or more recently with dual all digital phase locked loops (ADPLL) [see subchapter 2.4]. A novelty in the proposed frequency synthesizer is the fact that the dual loops are different (ADPLL and DPLL), in this way managing to improve the operation of two loops with the help of the particular advantages of each type of loop.

Within the proposed dual-loop synthesizer circuit, we combine the advantage of the low frequency resolution characteristic of DPLL circuits, with the advantage of a fast output frequency setting time offered by an ADPLL loop. Therefore, in comparison with the proposed dual-loop PLL circuit with the DPLL or ADPLL circuit, it has a better phase acquisition speed than DPLL circuit and a better frequency resolution than in the case of the ADPLL circuit [27]

3.2.1.4 Improving the process of aided capture

To reduce the settling time of the PLL circuit, the frequency acquisition is aided by a circuit called in the literature aid circuit. The digital logic used in the aid circuit greatly complicates the electrical schematisc of the PLL loops, but makes the user's work much easier and increases the performance of the final circuit. However, there is the advantage that the aid circuit occurs in the same capsule as the frequency synthesizer [8].

We have a great advantage in the proposed synthesizer, because we use as aid circuit parts already existing in the synthesizer, so there is no additional logic.

In order to reduce the settling time of the proposed frequency synthesizer, the frequency acquisition is aided by two procedures:

-We use two adjustment loops, of which the high gain ADPLL loop ensures a high frequency capture band.

-We start with the control voltage of the oscillator from a value very close to the one at which its output frequency is set

The aid circuit is implemented with the ADPLL loop, which presents the possibility to predefine the oscillation frequency with the help of the parallel charging of the counter. On the parallel charging of the counter, we can put the digital combination that sets the output of the digital analog to DAC converter at the value of control voltage required for the oscillator to oscillate on the desired frequency. In this way we can establish for a certain period a value of the initial oscillation frequency which is very close to the value of the wanted frequency.

3.2.1.2 The design way of ADPLL circuit

The ADPLL loop part of dual loop frequency synthesizer represents an original concept, inspired by the way of performing the direct frequency synthesis. The ADPLL have all the component blocks made digitally and works on the signal front, replacing the working mode on the signal level used in the control of the charge pump block in the DPLL loop.

A unique element is the way in which the ADPLL coarse adjustment loop in the synthesizer circuit is activated automatically depending on the need to use it only for the case of large phase shifts between the input signals. Thus, the ADPLL loop will work at the start of the synthesizer circuit and at the time of high frequency jumps, ensuring a very fast phase acquisition. When the frequency at the output of the oscillator approaches the value of permanent mode, the fully digital loop ADPLL, will cease its activity automatically. Only the analog loop will be used for fine frequency adjustments. This mode of operation has the advantage of obtaining a short frequency settling time as well as a low phase noise.

The ADPLL presented in the chapter is an original concept, which offers a series of advantages due to the replacement of the charge pump with a series of digital blocks that have the possibility to more precisely control the control voltages of the oscillator.

The great advantage of this type of circuit operation is the fact that the system is autonomous, and can decide for itself when to suppress the operation of the ADPLL coarse adjustment loop, by using the dead zone block DZ.

3.2.1.2 Phase noise improvement

The main method of decreasing the phase noise of the synthesizer is achieved by decreasing the gain of the blocks in the analog loop component that is used in the tracking mode. Thus we manage to reduce the implicit load pump currents and the noise determined by them.

Another method of reducing noise is to use two loops. We can transfer most of the gain to the second loop. For a fast settling time of the second loop we need IUP currents, high IDNs at the output of the load pump. A high current in the load pump implies the increase of the dimensions of the CMOS transistors from the component of the current sources and the CMOS switches. A larger transistor has a higher input equivalent capacity. The frequency detector must control a higher output capacity so that the disadvantage of the dead zone from the transfer characteristic that leads implicitly to noise problems appears. By replacing the second loop that has a high gain of the component blocks with a digital loop, all the noise problems mentioned before disappear.

3.2.1.5 Pulse forming network PFN

PFN pulse forming circuit connecting the phase and frequency detector block PFD and the NR counter block is an original concept designed especially for this particular case of digital signal conversion with variable filling factor from the phase and frequency detector, in digital signal with 50% fill factor. We need this block because the control of the counting direction cannot be done with a signal that has a narrow pulse width coming from the output of the phase and frequency detector circuit.

The design of the PFN circuit is not inspired but rather designed specifically for the functionality required for the entire synthesizer system. The basic idea to ensure at the input of the counter a control signal with sufficient pulse width to maintain the counting direction is to make a division by four of the signal from the output of the frequency detector to which is added a simple control logic to have only one active output at a time.

3.2.2 High speed phase frequency detector

The design of the detector proposed in subchapter 3.4.1.2 is better than high-speed PFD presents at point 2.1.1 because of reducing of propagation time throught detector. In the proposed design we manage to eliminate the delay element from the signal path of the high-speed PFD presented at 2.1.1.

The design proposed in 3.4.1.2 is made with digital blocks as opposed to the High speed low power PFD design from point 2.1.1. This gives it the advantage of having better portability when changing the production process.

3.2.3 Frequency reference

In chapter four we have the following original contributions:

3.2.3.1 Fourteen frequencies variable frequency reference

Frequency reference with fourteen switchable values in the range 96.48MHz-99.36 MHz is designed to meet the constraints of the 802.11g wireless communication standard. The frequency reference offers the possibility to select the output frequency of the frequency synthesizer circuit (PLL type) by changing the value of the reference frequency and not the PLL loop division factor as usual. Thus we can facilitate the change of the frequencies related to the fourteen communication channels of the 802.11g wireless communication standard, with the help of the reference frequency.

Achieving a frequency reference with fourteen selectable output frequencies is quite difficult having multiple constraints on the maximum value of the achievable frequency and the quality factor. The frequency reference proposed by us which has the frequency of the undivided internal oscillator approx. 1GHz is better unlike other works where we meet a maximum number of 4 generated frequencies (176MHz, 222MHz, 307MHz and 482MHz) with a maximum frequency of 482MHz [133]. In the case of [133] the frequency variation is made with the help of four BAW resonant circuits unlike in our case where the frequency variation is made with the help of an additional LC CMOS resonator. We get a degradation of the quality factor, but we gain a wide range of values that can be switched.

3.2.3.2 BAW(AlN)-LC(CMOS) resonator design method

The frequency reference circuit design is an iterative process because we have two resonators that are connected in parallel, with different frequency characteristics that must be tuned to operate on the same frequency.The method of designing the selection of the fourteen frequencies is innovative because the LC_CMOS and BAW elements have an interdependence relationship that requires the redesign of one of the resonators when modifying the other.The L_CMOS coil has the role of increasing the fp parallel resonance frequency of the BAW resonator compared to the fs series resonance, in order to offer the possibility for Csw_CMOS switched capacitors to select the fourteen wi-fi communication channels by decreasing the fp frequency to fs. The main idea is to size the ends of the frequency range so that we have an idea of the total capacity needed to sweep this frequency range. By successive simulation iterations, the total capacity is distributed on the fourteen switched capacitors Csw.

3.2.3.3 Frequency compensation method

The method of compensating the variation of the output frequency of the frequency reference block together with the variation of the CMOS / AlN production process is designed in order to minimize the interaction of the human operator in the usual mode of operation of the circuit.In mass production we can find a passive method to compensate the oscillation frequency with the variation of the technological process based on the trimming process [114] [115]. This trimming method is suitable for the case when the oscillator is focused only on a nominal oscillation frequency. In the case of an oscillator with several nominal output frequencies, a new approach is needed. The paper focuses on the realization of a method of frequency compensation with the process, suitable for oscillators with multiple output frequencies. The new compensation method is a dynamic one, offering multiple control ways due to the possibility of software contrhol.The frequency compensation method itself presents a collection of innovative elements that are listed below:

• Dual possibility of storing the fourteen calibration codes using non-volatile solutions: EPROM memories

• How to load the calibration codes and generate the voltage that controls the variable capacitor to compensate the frequency.

3.2.3.4 Single chip integration of reference and synthesizer

The proposed frequency reference uses as main element a BAW type resonator made in AlN technology that has a very good compatibility with the CMOS production process. Due to the very good compatibility between AlN and CMOS technology, it is possible to make an entire 2.4GHz wireless transmitter working in the same capsule that works according to the 802.11g standard.

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