

# PRIMERGY BX920 S3

# System configurator and order-information guide

## June 2014

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# **PRIMERGY Server**

## Instructions

This document contains basic product and configuration information that will enable you to configure your system via System-Architect.

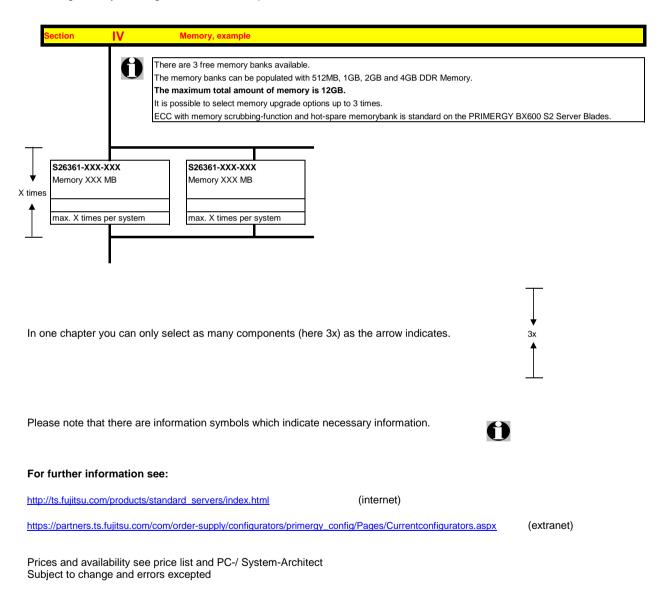
## Only the tool "System-Arcitect" will ensure a fast and proper configuration of your PRIMERGY server or your complete PRIMERGY Rack system.

Please pay attention to the naming conventions:	BX900 S1	System unit 1nd generation
	BX920 S2	Dual Server Blade S2

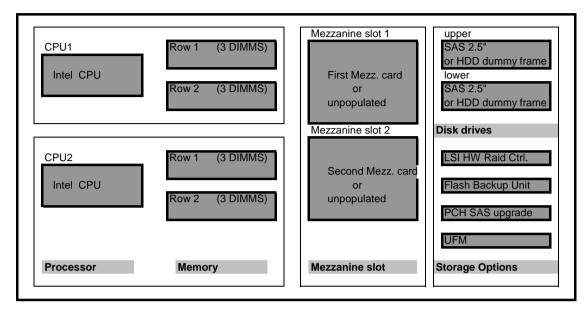
You can configure your individual PRIMERGY server in order to adjust your specific requirements.

The System configurator is divided into several chapters that are identical to the current price list and PC-/ System-Architect.

Please follow the lines. If there is a junction, you can choose which way or component you would like to take. Go through the configurator by following the lines from the top to the bottom.





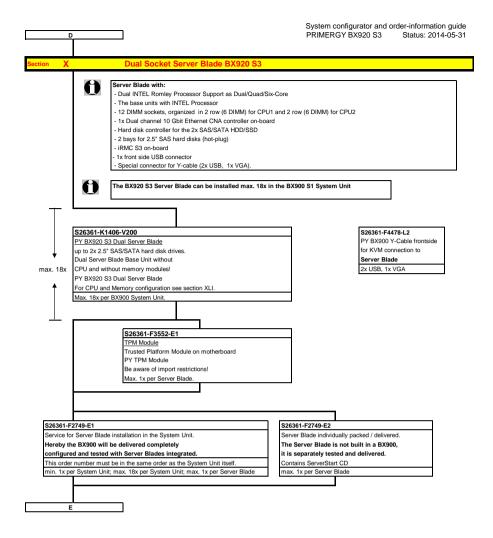


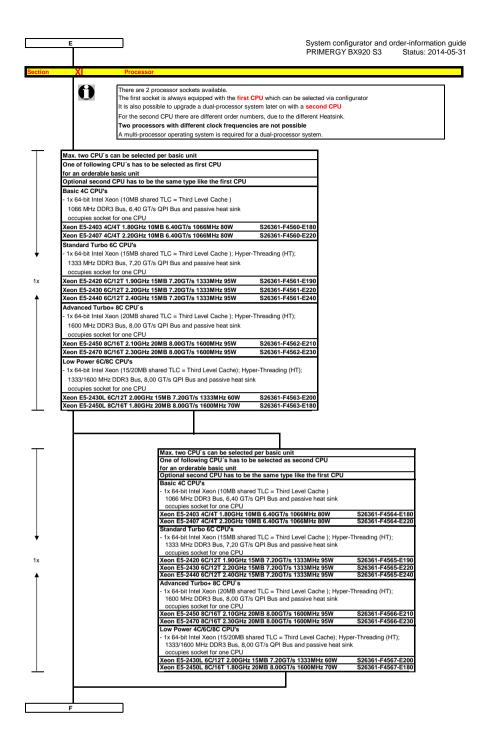
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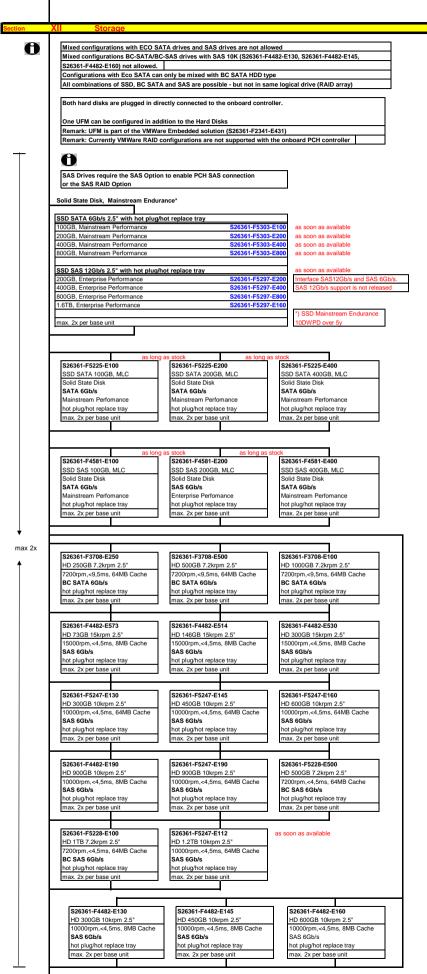
Included in basic unit

Option The population order for the CPU is: CPU1 first, then CPU2

The population order for the DIMMs: for each CPU, the DIMM row 1 (DIMMS 1A 1B 1C) (DIMMS 1D 1E 1F) first, then row 2 (DIMMs 2A, 2B, 2C) (DIMMs 2D, 2E, 2F)

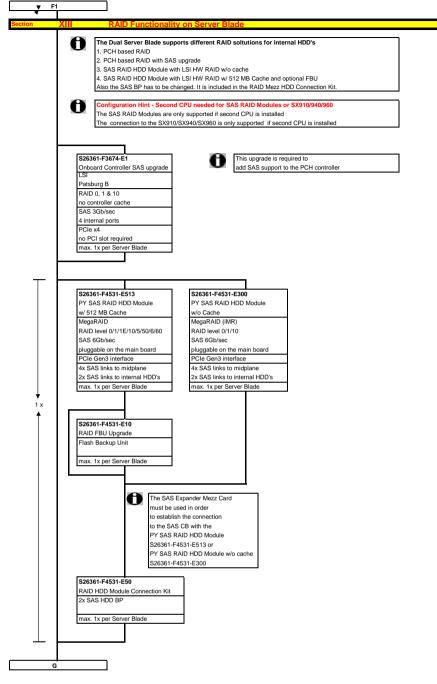


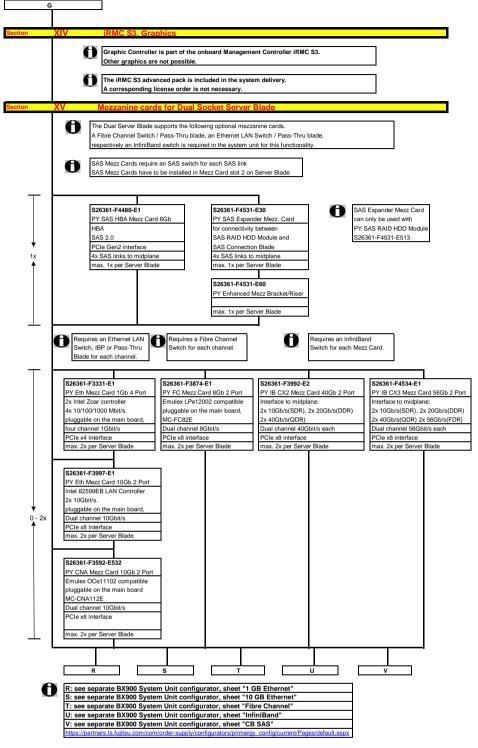


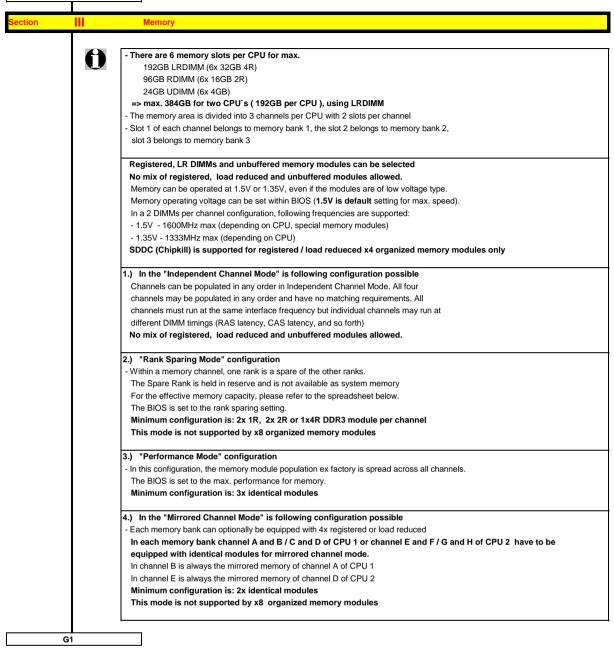


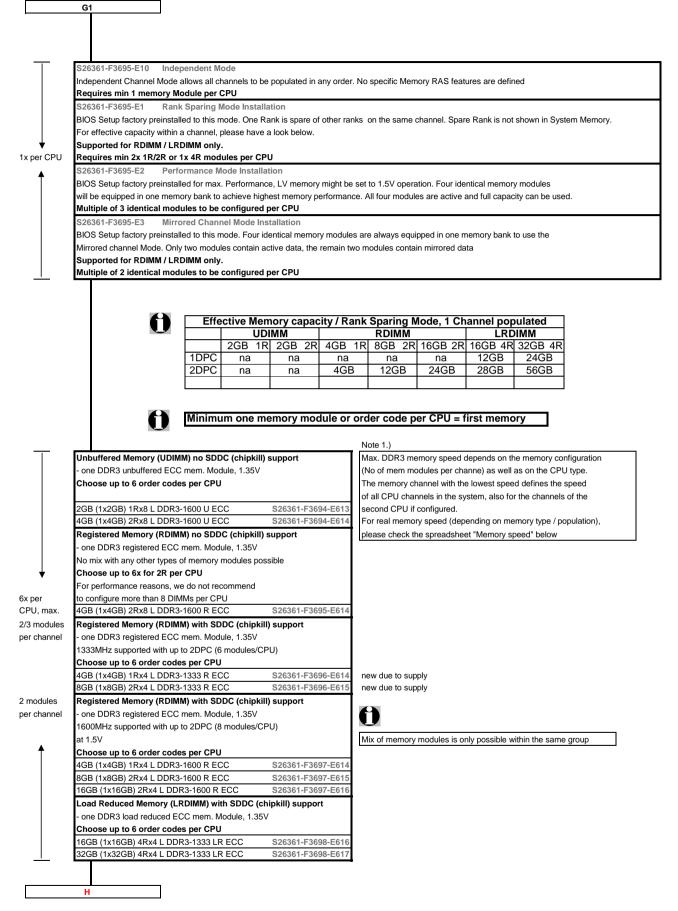
Fujitsu PRIMERGY Server

F1









#### Memory Configuration PRIMERGY BX920 S3

Each CPU offers 6 **Slots** for DDR3 Memory Modules organised in **2 Banks and 3 Channels.** If you need more than 6 Slots you have to configure the 2nd CPU. Depending on the amount of memory configured you can decide between 4 basic modes of operation (see explanation below).

There are 3 different kinds of DDR3 Memory Modules available: UDIMM / RDIMM and LRDIMM UDIMM / RDIMM / LRDIMM offer different functionality. Mix of UDIMM / RDIMM / LRDIMM is not alloved.

If 1.5V and 1.35V DIMMs are mixed, the DIMMs will run at 1.5V

Mode	Configuration UDIMM RDIMM		RDIMM	RDIMM	Application
		ODIMIM	RDIWIW	LRDIMM	
		x8	x8	x4	
SDDC (chipkill) support	any	no	no	yes	detect multi-bit errors
Independant Channel Mode	1, 2 or 3 Modules per Bank	yes	yes	yes	offers max. flexibility, upgradeability, capacity use UDIMM modules for lowest cost
Mirrored Channel Mode *)	2 identical Modules / Bank	no	no	yes	offers maximum security
Performance Mode	3 identical Modules / Bank	yes	yes	yes	offers maximum performance and capacity
Rank Sparing Mode *)	min. 2 Ranks / Channel	no	no	yes	balances security and capacity

\*) For the delivery ex works the system will be prepared with dedicated BIOS setting.

on special release

as soon as available

Capacity	Configuration	UDIMM	RDIMM	LRDIMM	Notes
Min. Memory per CPU	1 Module / CPU	1x2GB	1x4GB	1x 16GB	with one CPU
Max. Memory per CPU	4/6 Modules / CPU	6x4GB	6x16GB	6x 32GB	with one CPU
Max. Memory per System	8/12 Modules / System	48GB	96GB	384GB	if second CPU is configured

#### Memory-Speed:

Max. DDR3 memory speed depends on the memory configuration on one memory channel and the speed of the CPU The memory channel with the lowest speed defines the speed of all CPU channels in the system

Real maximum memory-bus speed depending on CPU type, memory configuration (DPC) and voltage setting (BIOS)																	
UDIMM 1600MHz			RDIMM 1600MHz					LRDIMM 1333MHz									
1.5\	/ [def	ault]	1.35V			1.5V [default]			1.35V			1.5V [default]			1.35V		
1	2	3	1	2	3	1	2	3	1	2	3	1	2	3	1	2	3
DPC	DPC	DPC	DPC	DPC	DPC	DPC	DPC	DPC	DPC	DPC	DPC	DPC	DPC	DPC	DPC	DPC	DPC
1333	1333	-	1066	1066	-	1600	1600	-	1333	1333	-	1333	1333	-	1066	1066	-
1600		-	1333	1000	-	1000	1000	-	1000	1555	-	-	1333	-	1000	1000	-
1333	1333	-	1066	1066	-	1333	1333	-	1333	1333	-	1333	1333	-	1066	1066	-
1066	1066	- 7	1066	1066	-	1066	1066	-	1066	1066	-	1066	1066	-	1066	1066	-
•	1.5 1 DPC 1333 1600 1333	UDI 1.5V [def: 1 2 DPC DPC 1333 1600 1333 1333	UDIMM 1 1.5V [default] 1 2 3 DPC DPC DPC 1333 1333 - 1600 - 1333 1333 -	UDIMM 1600M   1.5V [default] 1   1 2 3 1   DPC DPC DPC DPC   1333 1333 - 1066   16001 - 1333 1333 -	UDIMM 1600MHz   1.5V [default] 1.35\   1 2 3 1 2   DPC DPC DPC DPC DPC   1333 1333 - 1066 1066   1600 - 1333 - 1066 1066   1333 1333 - 1066 1066 1066	UDIMM 1600MHz   1.5V [default] 1.35V   1 2 3 1 2 3   DPC DPC DPC DPC DPC DPC   1333 - 1066 1066 -   1600 - 1333 - 1066 1066   1333 1333 - 1066 1066 -	UDIMM 1600MHz   1.5V [default] 1.35V 1.5V   1 2 3 1 2 3 1   DPC DPC DPC DPC DPC DPC DPC   1333 1333 - 1066 1066 - 1600   1333 1333 - 1066 1066 - 1333	and volt   UDIMM 1600MHz RDI   1.5V [default] 1.35V 1.5V [def   1 2 3 1 2 3 1 2   DPC DPC DPC DPC DPC DPC DPC DPC   1333 1333 - 1066 1066 - 1600 1600   1333 1333 - 1066 1066 - 1333 1333	and voltage s   UDIMM 1600MHz RDIMM 1   1.5V [default] 1.35V 1.5V [default]   1 2 3 1 2 3 1 2 3   DPC DPC DPC DPC DPC DPC DPC DPC DPC   1333 1333 - 1066 1066 - 1600 1600 -   1333 1333 - 1066 1066 - 1333 1333 -	and voltage settin   UDIMM 1600MHz RDIMM 1600M   1.5V [default] 1.35V 1.5V [default]   1 2 3 1 2 3 1   DPC DPC DPC DPC DPC DPC DPC DPC   1333 - 1066 - 1600 1600 - 1333   1600 1333 - 1066 066 - 1333 1333 - 1333	and voltage setting (BI   UDIMM 1600MHz RDIMM 1600MHz   1.5V [default] 1.35V 1.5V [default] 1.35V   1 2 3 1 2 3 1 2 3 1 2 3 1 2 3 1 2 3 1 2 3 1 2 3 1 2 3 1 2 3 1 2 3 1 2 3 1 2 3 1 2 3 1 2 3 1 2 3 1 2 3 1 2 3 1 2 3 1 2 0	and voltage setting (BIOS)   UDIMM 1600MHz RDIMM 1600MHz   1.5V [default] 1.35V 1.5V [default] 1.35V   1 2 3 1 2 3 1 2 3   DPC	and voltage setting (BIOS)   UDIMM 1600MHz RDIMM 1600MHz 1.5V [default] 1.35V 1.5V [default] 1.5V [default] 1.35V 1.5V [default] 1.35V 1.5V [default] 1.33V [default] 1.33V [default] 1.33V [default] 1.33V [default] 1.333 1.333 1.333 1.333 1.333 1.333 1.333	and voltage setting (BIOS)   UDIMM 1600MHz RDIMM 1600MHz LR   1.5V [default] 1.35V 1.5V [default] 1.35V 1.5V [default]   1 2 3 1 2	and voltage setting (BIOS)   UDIMM 1600MHz RDIMM 1600MHz LRDIMM   1.5V [default] 1.35V 1.5V [default] 1.35V 1.5V [default]   1 2 3 1 2 3 1 2 3 1 2 3   DPC <th>and voltage setting (BIOS)   UDIMM 1600MHz RDIMM 1600MHz LRDIMM 133   1.5V [default] 1.35V 1.5V [default] 1.5V [default]</th> <th>and voltage setting (BIOS)   UDIMM 1600MHz RDIMM 1600MHz LRDIMM 1333MHz   1.5V [default] 1.35V 1.5V [default] 1.35V 1.5V [default] 1.35V   1 2 3 <t< th=""></t<></th>	and voltage setting (BIOS)   UDIMM 1600MHz RDIMM 1600MHz LRDIMM 133   1.5V [default] 1.35V 1.5V [default]	and voltage setting (BIOS)   UDIMM 1600MHz RDIMM 1600MHz LRDIMM 1333MHz   1.5V [default] 1.35V 1.5V [default] 1.35V 1.5V [default] 1.35V   1 2 3 <t< th=""></t<>

1R - Single Rank

2R - Dual Rank

4R - Quad Rank

1DPC = 1 DIMM per Channel 2DPC = 2 DIMM per Channel

3DPC = 3 DIMM per Channel

Configuration hints:

- The memory sockets on the systemboard offer a color coding:

Bank I black sockets

Bank II blue sockets

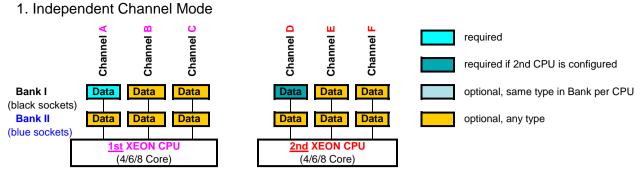
Bank III green sockets

- A so called Bank consits of 1 memory module on every Channel available on one CPU (examples see below) Bank I on CPU 1/2 up to 3 memory modules connected to Channel A - F on the 1st/2nd CPU

Bank II on CPU 1/2 up to 3 memory modules connected to Channel A - F on the 1st/2nd CPU

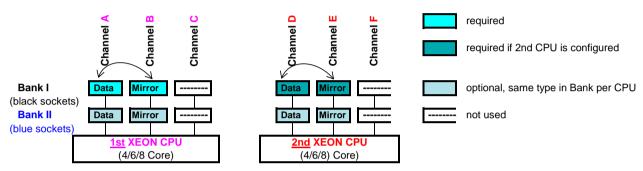
- See below and next page for a detailed descriptions of the memory configuration supported.

System configurator and order-information guide PRIMERGY BX920 S3 Status: 2014-05-31

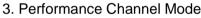


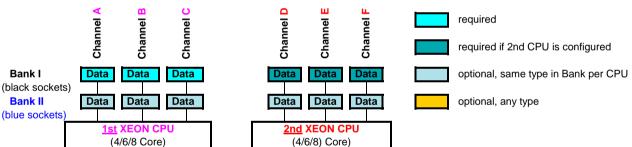
Independent Channel Mode allows all channels to be populated in any order Can run with differently rated DIMMs and use the settings of the slowest DIMM installed in the system

#### 2. Mirrored Channel Mode

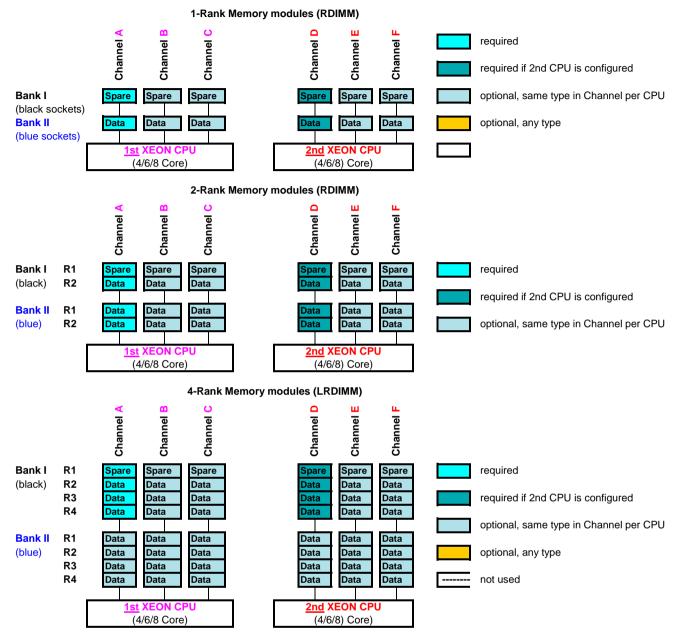


Mirrored Channel Mode requires identical modules on channel A / B (1st CPU) or channel D / E (2nd CPU) 50% of the capacity is used for the mirror => the available memory for applications is only half of the installed memory If this mode is used, a multiple of 2 identical modules has to be ordered.





Performance Channel Mode requires identical modules on all channels of each Bank per CPU. If this mode is used, a multiple of 3 identical modules has to be ordered.



#### 4. Rank Sparing Mode

Rank Sparing Mode requires identical modules (same capacity and technology) within the same channel. The available memory for applications will vary depending on configuration. Please refer to the spreadsheet above "Effective Memory capacity with active Rank Sparing Mode". Population rule for Rank sparing mode is to achieve max. available memory.

## **Change Report**

Date	Order number	Changes
2014-01-31	S26361-F5247-E112	New 1.2TB 2.5" SAS 10K HDD added.
2014-01-31	S26361-F5303-*	New SATA SSDs added.
2014-01-31	S26361-F5297-*	New SAS SSDs added.
2013-10-18	optional USB Comps	no longer available
2013-07-18		Added comment about PCH Vmware limitation
2013-01-15	S26361-F3674-E1	Onboard Controller SAS upgrade - Speed corrected from 6GB/s to 3GB/s
2013-01-08	S26361-F5228-E***	New order number for 2.5" BC SAS 7.2K
2013-01-08	S26361-F5247-E130	New order number for SAS 10K (mix with BC-SATA supported, successor for *F5227*)
2012-10-16	hint	SX910/910/960 only with 2nd CPU modified
2012-10-09	hint	SX910/910/960 only with 2nd CPU
2012-10-02		changed USB info
2012-09-04	S26361-F3592-E532	as soon as available removed
2012-07-23	S26361-F5227-E1*	New order for 2.5" 10K SAS HDD supporting mix with 2.5" BC-SATA HDD
2012-06-28		corrected text for 2 end Y-Cable
2012-06-12	S26361-F5225-E*00	New order for SATA SSD's
2012-05-29		Added 1333 RDIMM
2012-05-01		First Release