

PRIMERGY BX900 Server Blades

System configurator and order-information guide

March 2010

Contents

Instructions
Configuration diagram
Configurator



0 System software

X BX920 S1 Dual Socket

XI Processor

XII Memory

XIII Storage

XIV iRMC S2, Graphics

XV Mezzanine Cards

L Storage Blades

LI SX910 Tape Blade LIV SX940 Storage Blade Disk
LII SX910 SAS Controller LV SX940 SAS Controller
LIII SX910 SAS Tape Drive LVI SX940 Quad Disk Blade

Change report

PRIMERGY Server

Instructions

This document contains basic product and configuration information that will enable you to configure your system via System-Architect.

Only the tool "System-Arcitect" will ensure a fast and proper configuration of your PRIMERGY server or your complete PRIMERGY Rack system.

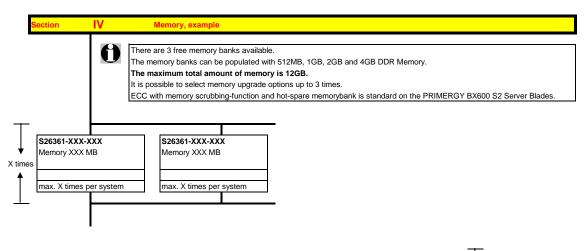
Please pay attention to the naming conventions: BX900 S1 System unit 1nd generation

BX920 S1 Dual Server Blade S1 SX940 S1 Storage Blade Disk SX910 S1 Storage Tape Blade

You can configure your individual PRIMERGY server in order to adjust your specific requirements.

The System configurator is divided into several chapters that are identical to the current price list and PC-/ System-Architect.

Please follow the lines. If there is a junction, you can choose which way or component you would like to take. Go through the configurator by following the lines from the top to the bottom.



In one chapter you can only select as many components (here 3x) as the arrow indicates.





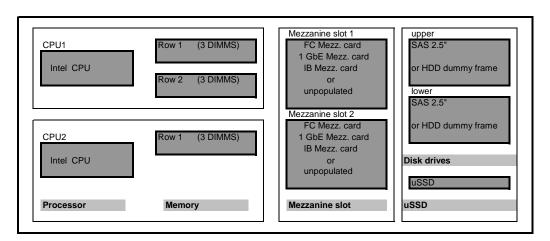
For further information see:

http://ts.fujitsu.com/products/standard_servers/index.html (internet)

https://partners.ts.fujitsu.com/com/order-supply/configurators/primergy_config/current/Pages/default.asp> (extranet)

Prices and availability see price list and PC-/ System-Architect Subject to change and errors excepted

Configuration diagram Dual Server Blade BX920 S1



Key:

Included in basic unit Option

The population order for the CPU is: CPU1 first, then CPU2

The population order for the DIMMs: for each CPU, the DIMM row 1 (DIMMS 1A 1B 1C) (DIMMS 1D 1E 1F) first, then row 2 (DIMMs 2A, 2B, 2C) (DIMMs 2D, 2E, 2F)

Memory Configuration PRIMERGY BX920 S1

The first CPU offers 6 Slots for DDR3 Memory Modules organised in 2 Banks and 3 Channels.

If you need more than 6 Slots you have to configure the 2nd CPU.

The second CPU offers 3 Slots for DDR3 Memory Modules organised in 1 Banks and 3 Channels.

Depending on the amount of memory configured you can decide between 3 basic modes of operation (see explanation below).

There are 2 different kinds of DDR3 Memory Modules available: UDIMM and RDIMM. UDIMM and RDIMM offer different functionality.

Mode	Configuration	UDIMM	RDIMM	Application
chip kill support	any	n.a.	yes	detect multi-bit errors
Independant Channel Mode	1, 2 or 3 Modules per Bank	х	Х	offers max. flexibility, upgradeability, capacity use UDIMM modules for lowest cost
Mirrored Channel Mode	2 identical Modules / Bank	**)	Х	offers maximum security
Performance Mode *)	3 identical Modules / Bank	**)	Х	offers maximum performance and capacity

^{*) =} Performance Mode and Spare mode use different BIOS settings.

Configuration hints:

- The memory sockets on the systemboard offer a color coding:

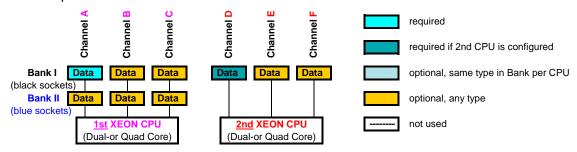
Bank I black sockets
Bank II blue sockets

- A so called Bank consits of 1 memory module on every Channel available on one CPU (examples see below)

Bank I on CPU 1 up to 3 memory modules connected to Channel A, B and C on the first CPU up to 3 memory modules connected to Channel A, B and C on the first CPU Bank I on CPU 2 up to 3 memory modules connected to Channel D, E and F on the second CPU

- See below (next page) for a detailed descriptions of the memory configuration supported.

1. Independent Channel Mode

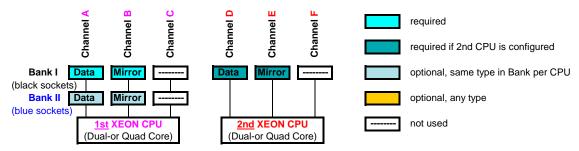


Independent Channel Mode allows all channels to be populated in any order Can run with differently rated DIMMs and use the settings of the slowest DIMM installed in the system Independent Channel Mode is supported using UDIMM or RDIMM memory modules

^{**) =} technically possible but no Order Numbers available, use at your own risk

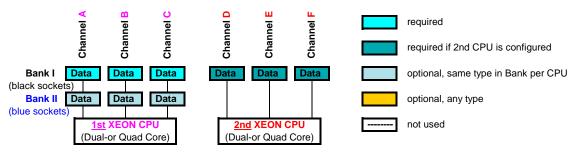
x = order codes available

2. Mirrored Channel Mode

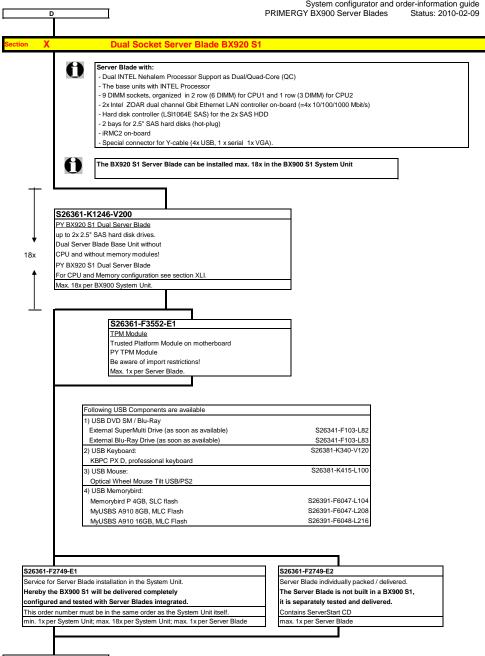


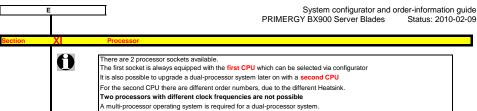
Mirrored Channel Mode requires identical modules on channel A and B (1st CPU) or channel D and E (2nd CPU) 50% of the capacity is used for the mirror => the available memory for applications is only half of the installed memory channel C (1st CPU) or channel F (2nd CPU) are not usable in Mirrored Channel Mode Mirrored Channel Mode is supported using RDIMM memory modules

3. Performance Channel Mode



Performance Channel Mode requires identical modules on all channels of each Bank per CPU Performance Channel Mode is supported using RDIMM memory modules



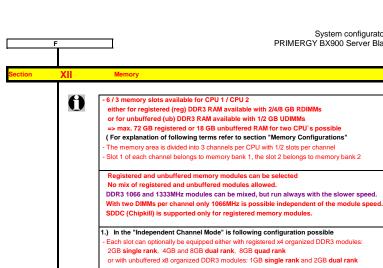


ax. two CPU's can be selected per basic unit One of following CPU's has to be selected as first CPU for an orderable basic unit Optional second CPU has to be the same type like the first CPU Dual-Core CPU with max. DDR3 Bus Speed 800MHz 1x 64-bit Intel Xeon DP (4MB shared TLC = Second Level Cache) and passive heat sink occupies socket for one CPU Con DP E5502 (1,86GHz/4W4,8GT) / 80W Quad-Core CPU's with max. DDR3 Bus Speed 800MHz -1x 64-bit Intel Xeon DP (4MB shared TLC = Second Level Cache) S26361-F3965-E186 and passive heat sink occupies socket for one CPU Xeon DP E5504 (2.00GHz/4M/4,8GT) / 80W S26361-F3966-E200 Xeon DP E5506 (2.13GHz/4M/4,8GT) / 80W Turbo Quad-Core CPU's with max. DDR3 Bus Speed 1066MHz S26361-F3966-E213 1x 64-bit Intel Xeon DP (8MB shared TLC = Second Level Cache) and passive heat sink occupies socket for one CPU Xeon DP E5520 (2.26GHz/8M/5,86GT) / 80W Xeon DP E5530 (2.40GHz/8M/5,86GT) / 80W Xeon DP E5540 (2.53GHz/8M/5,86GT) / 80W S26361-F3967-E226 S26361-F3967-E246 S26361-F3967-E253 Turbo Quad-Core CPU's with max. DDR3 Bus Speed 1333MHz 1x 64-bit Intel Xeon DP (8MB shared TLC = Second Level Cache) and passive heat sink occupies socket for one CPU Xeon DP X5550 (2.66GHz/8M/6,4GT) / 95W S26361-F3968-E266 Xeon DP X5560 (2.80GHz/8M/6,4GT) / 95W Xeon DP X5570 (2.93GHz/8M/6,4CT) / 95W S26361 Low Voltage Quad-Core CPU with max. 800MHz DDR3 speed (4.8GT/s) -1x 64-bit Intel Xeon DP (4MB shared TLC = Second Level Cache) with passive heat sink, occupies socket for one CPU Xeon LV DP L5506 (2,13GHz/4M/4,8GT) / 60W Low Voltage Turbo Quad-Core CPU's with max. DDR3 Bus Speed 1066MHz 1x 64-bit Intel Xeon DP (8MB shared TLC = Second Level Cache) and passive heat sink occupies socket for one CPU Xeon LV DP L5520 (2,26GHz/8M/5,86GT) / 60W Xeon LV DP L5530 (2,4GHz/8M/5,86GT) / 60W S26361-F3969-E22

Note: Max. DDR3 Bus Speed depends on:

- max. DDR3 Bus Speed from the CPU and
- max. DDR3 Memory Speed and
- max. memory modules on one memory channel

Many Arma CRUEs are he releated are haris mit	
Max. two CPU's can be selected per basic unit One of following CPU's can to be selected as second CPU	
for an orderable basic unit	
Optional second CPU has to be the same type like the first CF	011
Dual-Core CPU with max. DDR3 Bus Speed 800MHz	- 0
- 1x 64-bit Intel Xeon DP (4MB shared TLC = Second Level Cache	- 1
and passive heat sink	=)
occupies socket for one CPU	
Xeon DP E5502 (1,86GHz/4M/4,8GT) / 80W	S26361-F3971-E
Quad-Core CPU's with max. DDR3 Bus Speed 800MHz	320301-1 397 1-L
- 1x 64-bit Intel Xeon DP (4MB shared TLC = Second Level Cache	a)
and passive heat sink	- /
occupies socket for one CPU	
Xeon DP E5504 (2.00GHz/4M/4,8GT) / 80W	S26361-F3972-E
Xeon DP E5506 (2.13GHz/4M/4,8GT) / 80W	S26361-F3972-E
Turbo Quad-Core CPU's with max. DDR3 Bus Speed 1066MH	
- 1x 64-bit Intel Xeon DP (8MB shared TLC = Second Level Cache	
and passive heat sink	,
occupies socket for one CPU	
Xeon DP E5520 (2.26GHz/8M/5,86GT) / 80W	S26361-F3973-E
Xeon DP E5530 (2.40GHz/8M/5,86GT) / 80W	S26361-F3973-E
Xeon DP E5540 (2.53GHz/8M/5,86GT) / 80W	S26361-F3973-E
Turbo Quad-Core CPU's with max. DDR3 Bus Speed 1333MF	lz
- 1x 64-bit Intel Xeon DP (8MB shared TLC = Second Level Cache	∍)
and passive heat sink	
occupies socket for one CPU	
Xeon DP X5550 (2.66GHz/8M/6,4GT) / 95W	S26361-F3974-E
Xeon DP X5560 (2.80GHz/8M/6,4GT) / 95W	S26361-F3974-E
Xeon DP X5570 (2.93GHz/8M/6,4GT) / 95W	S26361-F3974-E
Low Voltage Quad-Core CPU with max. 800MHz DDR3 speed	(4.8GT/s)
- 1x 64-bit Intel Xeon DP (4MB shared TLC = Second Level Cache	e)
with passive heat sink, occupies socket for one CPU	
Xeon LV DP L5506 (2,13GHz/4M/4,8GT) / 60W	S26361-F3975-E
Low Voltage Turbo Quad-Core CPU's with max. DDR3 Bus Sp	
- 1x 64-bit Intel Xeon DP (8MB shared TLC = Second Level Cache	∍)
and passive heat sink	
occupies socket for one CPU	
occupies socket for one CPU Xeon LV DP L5520 (2,26GHz/8M/5,86GT) / 60W Xeon LV DP L5530 (2,4GHz/8M/5,86GT) / 60W	S26361-F3975-E2



1.) In the "Independent Channel Mode" is following configuration possible

Each slot can optionally be equipped either with registered x4 organized DDR3 modules: 2GB single rank, 4GB and 8GB dual rank, 8GB quad rank or with unbuffered x8 organized DDR3 modules: 1GB single rank and 2GB dual rank

2.) In the "Mirrored Channel Mode" is following configuration possible

Each memory bank can optionally be equipped with 2x2GB single rank 2x4GB and 2x8GB dual rank DDR3 modules or with 2x8GB guad rank DDR3 modules

In each memory bank channel A and B of CPU 1 or channel D and E of CPU 2 have to be equipped with

identical modules for mirrored channel mode. Channel C of CPU 1 and channel F of CPU 2 is not equipped

In channel B is always the mirrored memory of channel A of CPU 1 In channel E is always the mirrored memory of channel D of CPU 2

No special order codes with UDIMMs are offered for this mode

3.) In the "Performance Channel Mode" is following configuration possible

Each slot of one bank has to be equipped with identical modules for performance channel mode No special order codes with UDIMMs are offered for this mode

- For each CPU minimum 1 memory module has to be configured in independent Channel Mode

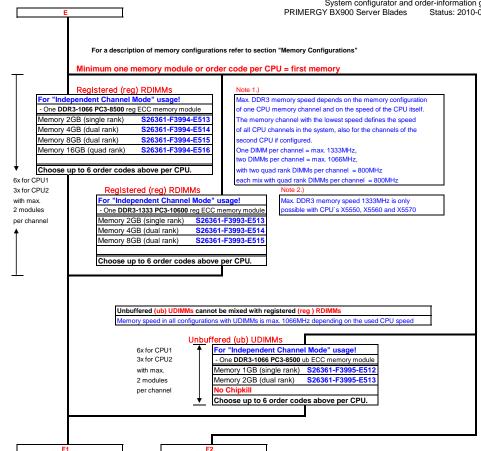
al memory extensions can still be configured up to five times per CPU) or

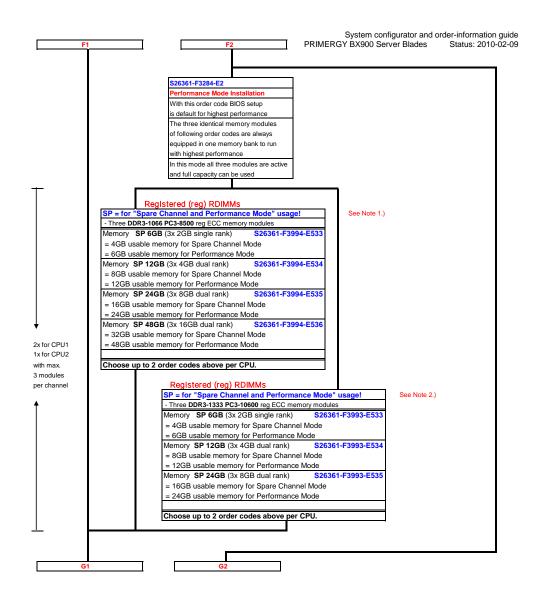
one bank has to be equipped with two modules (channel A+B for CPU 1 or D+E for CPU 2) in Mirrored Channel Mode

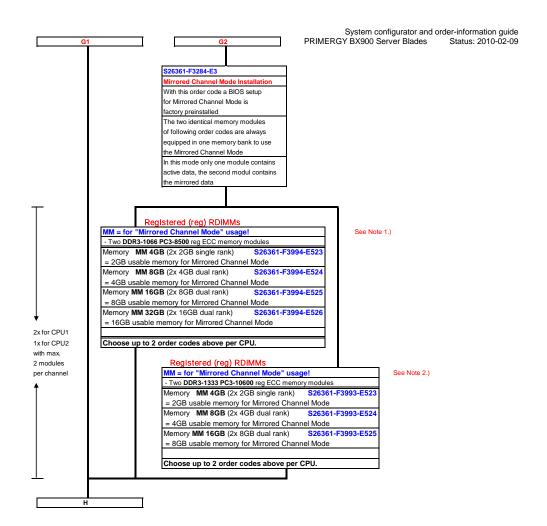
> Additional memory extensions can still be configured up to one time per CPU) or

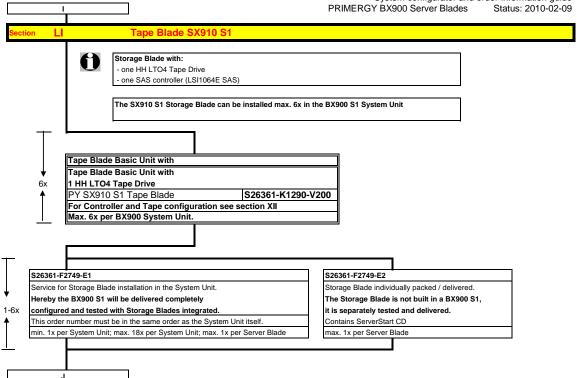
one bank has to be equipped with three modules (channel A+B+C for CPU 1 or D+E+F for CPU 2) In Performance Mode

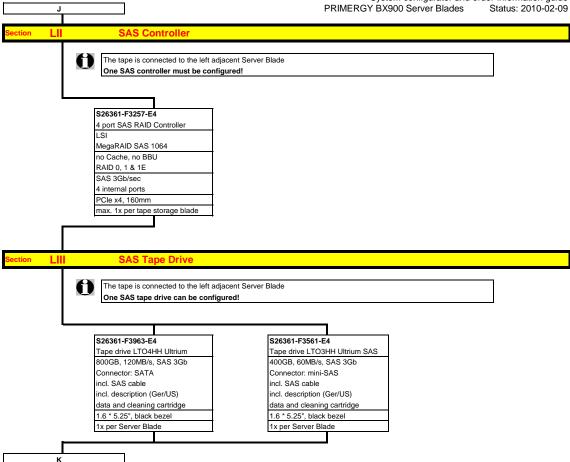
> Additional memory extensions can still be configured up to one time per CPU)

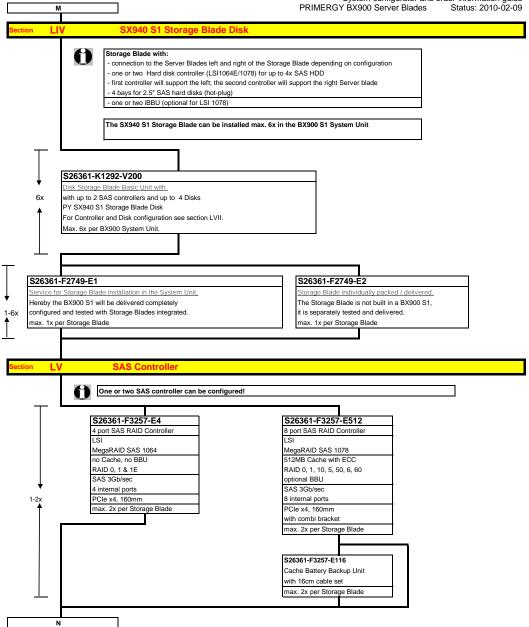


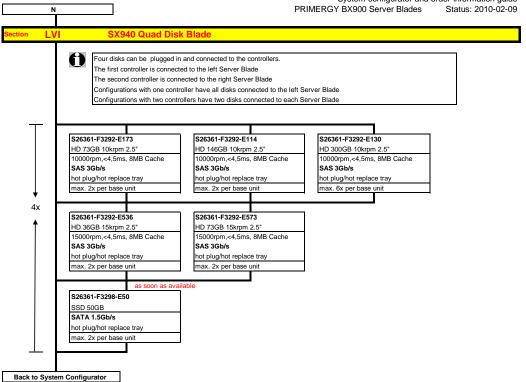












Change Report

Date	Order number	Changes	
2010-02-09	S26391-F264-L226	USB Floppy drive will be phased out by end of February 2010 with no alternative	
2009-08-25	320391-1 204-L220	modified SSD to 32 /64GB Intel types	
2009-08-23	S26361-K1290-V200	SX910 - now available	
2009-07-31	320301-1(1230-7200	USB Device update BX920	
2009-04-22		SSD 50GB comment added "as soon as available"	
2009-03-31		First release	
	J		