Science Arena Publications
Specialty Journal of Electronic and Computer Sciences
Available online at www.sciarena.com
2016, Vol, 2 (1): 47-55

Systematic Design and Simulation of a Delta-Sigma Fractional-N Frequency Synthesizer

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Abstract: *The design principles of a fractional-N delta-sigma frequency synthesizer and the procedure of choosing the proper digital delta-sigma modulator (DDSM) are presented in this paper. Three previously presented spur reduction techniques are addressed and their effect on four types of DDSMs is explored. Furthermore, other factors which are important in choosing a DDSM and their evaluation method are introduced here. Simulation shows that between MASH 1-1-1, single quantizer error feedback modulator (SQ_EFM) and single quantizer multiple feedback modulator (SQ_MFM), the output feedback is the most suitable approach for reducing sputs. And, between these three DDSMs, the one that requires minimum hardware is the best option. If out of band phase noise is critical, single quantizer multiple feedforward modulator (SQ_MFFM) is preferred, although it degrades in-band phase noise.*
Keywords: Digital delta-sigma modulator, PLL, phase noise, spurious tone.

INTRODUCTION

The rapid development of the wireless communication imposes more stringent conditions in designing wireless RF transceivers. Among the others, frequency synthesizers are the most challenging part of a transceiver. Consuming low power, having low phase noise and the absence of spurious tones are the rudimentary targets of the PLL designers. Without any doubt, fractional-N frequency synthesizers are the most important and practical synthesizers. Utilizing delta-sigma modulators, they can reach fine accuracy, even in the order of about 1 Hz [1], with no need to reduce reference frequency. PLL has different blocks and each block can be implemented in various ways. Furthermore, each block needs to be designed by regarding the whole system requirements. So, PLL designing demands a comprehensive systematic view, which this paper aims to cover.

The majority of this paper is assigned to survey DDSMs. Various types of DDSMs are proposed and used in PLLs up to now and different methods for reducing spurs are examined [2-7]. Besides spurs, there are some other issues which a designer needs to consider while choosing a DDSM. Here, some spur reduction techniques and other important measurements are presented.

This paper is organized as follows. Section 2 introduces the systematic analysis of the PLL and the routine of designing a passive loop filter [8]. Analysis and simulation of various topologies of delta-sigma modulators are presented in section 3. Necessary measurements needed to be considered for comparing different DDSMs are also explained in this section. Finally, section 4 represents the simulation of the PLL in MATLAB. Conclusion

2. Systematic Analysis and Loop Filter Design

In the design of a PLL, the first step is a proper systematic analysis. This analysis need to be done in frequency domain. As a result of such analysis, some characteristics of the PLL are determined including BW (Band Width) and phase margin. Besides, required parameters to design different blocks of the PLL like VCO gain, charge pump current and divider modulus are chosen. To perform such analysis, each block is modeled in frequency domain; therefore the whole PLL transfer function can be achieved. As a rule of thumb, the order of the loop filter must be equal or greater than the order of DDSM. Since the 3rd order DDSM is applied here, the 3rd order LPF is chosen. Fig. 1 depicts the PLL block diagram and LPF.

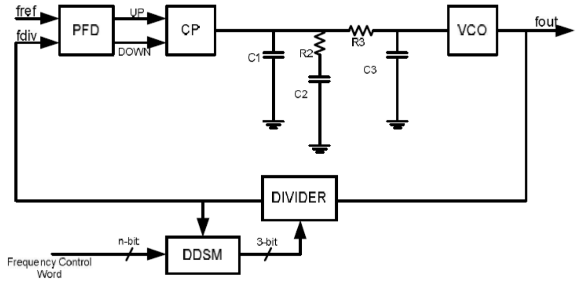

Fig. 1: A figure fitted in a column

Equations (1) and (2) indicate the transfer functions of the LPF and open loop transfer function of the PLL, respectively. Been taken the approach proposed in [8], the zero and poles of the open loop transfer function are attempted to locate in a way that in the required BW the phase margin becomes maximum. To satisfy this condition, first the phase of the open loop transfer function is calculated. It must be equivalent to desired phase noise [??]. Second, phase noise must become maximum in the crossover frequency (the frequency in which the amplitude of the open loop transfer function becomes unity). This means that the deviation of the phase of the PLL open loop transfer function in crossover frequency has to be zero. There is a relationship between crossover frequency (ω_0) and BW of the PLL. By performing extensive simulation, it is found that $\omega_c \approx BW/1.75$. Another parameter is T_{31}, the inverse proportion of the third pole location to first pole, which here is selected ~~to be 0.2. The~~ more this parameter is, the more out of band phase noise is filtered; however, it can not be unity since it will degrade the phase margin. Finally, the two equations obtained from phase transfer function can be solved numerically in MATLAB to determine T_1 and T_2. Other parameters can be achieved through some mathematical relationships. The location of zero and poles and other parameters of the loop are illustrated in TABLE I. Moreover, the Bode diagram of the PLL open loop transfer function is depicted in Fig. 2. As it is obvious, phase margin is maximum in crossover frequency.

$$Z(s) = \frac{1+sT_2}{sA_0(1+sT_1)(1+sT_3)} \tag{1}$$

$$\frac{\theta_O}{\theta_R}(s) = \frac{K_{VCO}K_P}{Ns}\frac{1+sT_2}{sA_0(1+sT_1)(1+sT_3)} \tag{2}$$

TABLE I: Characteristics of PLL and LPF

Parameter	Value	Parameter	Value
$1/T_1$ (Krad/sec)	522.7	N	122
$1/T_2$ Krad/sec	62	R_2 Ω	74
$1/T_3$ Mrad/sec	1.36	R_3 Ω	293
Phase Margin	45°	C_1 nF	17.86
BW KHz	40	C_2 nF	218
K_{VCO} MHz/v	250	C_3 nF	4.16
I_{CP}(mA)	1		

It is not fallacious to say that the most effective parameter on the behavior of the PLL is BW. By increasing BW, lock time decreases and VCO phase noise degrades more. However, the phase noise of other parts of the PLL will worsen the output phase noise. Inversely, by decreasing BW, lock time increases and also, VCO referred phase noise becomes dominant in the output. Also, noise due to the other parts of the PLL will filter

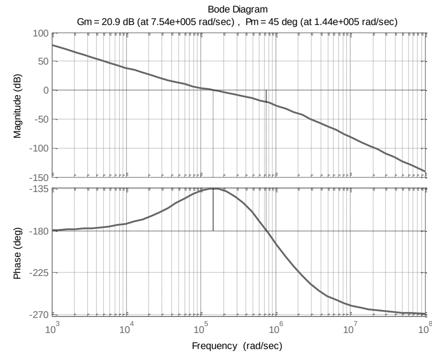

Fig. 2: Bode diagram of the PLL open loop transfer function

more. In delta-sigma PLLs, because of the phase error generated by DDSM in the input of the PFD, BW needs to be lowered to overcome this problem.

3. Digital Delta-Sigma Modulator

DDSMs are divided into two basic categories: single quantizer (single stage) and MASH. Each one has their own advantages and disadvantages. Based on the application, proper one can be chosen. In this section four types of third order DDSM are discussed in detail and necessary measurements for comparing DDSMs are presented.

3.1 Four Types of DDSM

The first and most conventional modulator is MASH 1-1-1. Fig. 3 shows the block diagram and equation (3) shows the output of this modulator. The output of this modulator varies from -3 to 4. The most important advantages of this modulator are its simplicity of implementation and stability. Its binary weighted quantizer does not need any extra circuitry and it is unconditionally stable, i.e. the input can vary from 0 to 1. However it has some disadvantages. The number of its output's levels is rigid and unchangeable. Also, its high frequency quantization noise is not shaped leading to an increase in out of band phase noise.

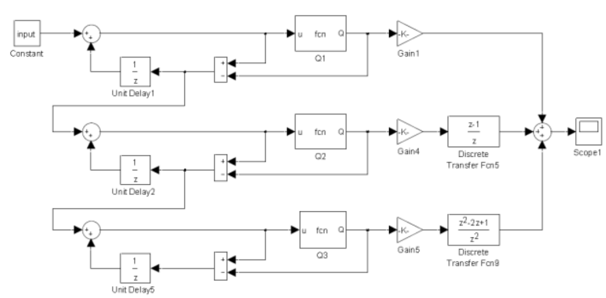

Fig. 3: Block diagram of MASH 1-1-1

$$Y(z) = X(z) + (1 - z^{-1})^3 E(z) \qquad (3)$$

The next two DDSMs are SQ_EFM and SQ_MFM which their block diagrams are shown in Fig. 4 and Fig. 5 respectively. The STF and NTF of them are just like MASH 1-1-1. As a characteristic of SQ modulators, the output can be one bit or multi bit.

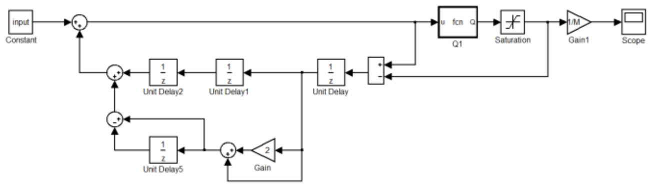

Fig. 4: Block diagram of SQ_EFM

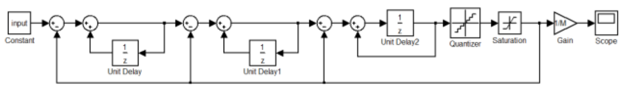

Fig. 5: Block diagram of SQ_MFM

The last modulator is SQ_MFFM [9]. The block diagram of SQ_MFFM is drawn in Fig. 6. Equation (4) indicates NTF of the modulator. It can be seen that the NTF of this modulator is different from three previous modulators since it has two extra poles which filter high frequency quantization noise more effectively.

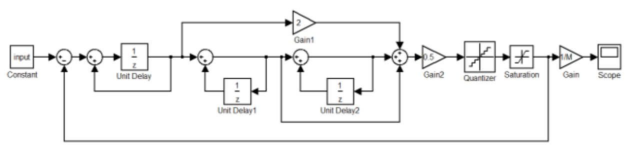

Fig. 6: Block diagram of SQ_MFFM

$$NTF = \frac{(1-z^{-1})^3}{1-z^{-1}+0.5z^{-2}} \qquad (3)$$

3.2 Spur Reduction Techniques

DDSMs are one of the important sources of the spurs in a PLL. A DDSM is a finite state machine and by applying constant input to it, the output will definitely become periodic. Being periodic is the cause of the existence of the spurs, since, the average power of the DDSMs output signal, which is constant if the assumption that the quantization noise is a white noise is true [10], is dissipated over these tones and the number of tones are equal to the period of the modulator. Now if the period is large enough, the power per tone reduces and a smoother spectrum can be achieved. As an example, PSD of MASH 1-1-1 for n=19 and input=$2^n/2$ is depicted in Fig. 7 where n is the number of input bits. In this case the period is 4 and then we can observe 4 spurs in the PSD. In addition to, period depends on the input. To solve this problem, it is always tried to widen the period of the DDSM or more randomize it and also to eliminate the dependency of the period to input amplitude. To aim this goal there are two fundamental approaches [10]: Stochastic and deterministic.

In stochastic approach, dither signal is added to the DDSM's loop (either to input of the loop or before the quantizer). Adding dither fulfills the job of the randomization well but the problem is that it degrades the in-band phase noise. By high pass filtering the dither signal before applying it (shaped dithering), the in-band phase noise improves to some extent.

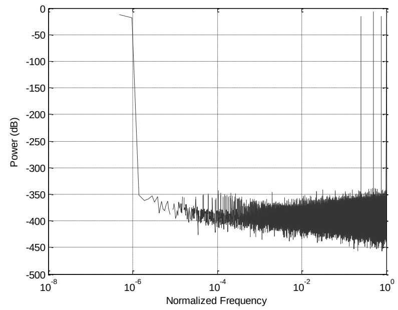

Fig. 7: PSD of MASH 1-1-1 with n=19 and input =$2^n/2$

On the other hand, in the deterministic approach, it is tried to expand the period by changing the structure of the DDSM or set the initial condition for integrators (seeding). This approach does not increase the in-band phase noise. Various types of stochastic and deterministic approaches are proposed so far. Two deterministic approaches including seeding technique [2] and using output feedback [3, 4] and a stochastic approach, first order shaped and non-shaped LSB dithering [6, 7], are selected in this paper to investigate. The output feedback and shaped-dither approaches are examined on MASH 1-1-1, SQ_EFM and SQ_MFM. Based on [6, 7], for third order modulators, the high pass filter order can be just 1. The seeding technique is examined for MASH 1-1-1 and SQ_EFM. For SQ_MFFM, just adding non-shaped dither is examined. In seeding technique, the period of $2^{(n+1)}$ for all inputs is guaranteed for proper initial condition for integrators. By using output feedback, the period of about 2^{3n} for all inputs is guaranteed. As an example, the PSD of SQ_EFM with n=14 and input =$2^{14}/2$ utilizing all three mentioned spur reduction techniques is shown in Fig. 8.

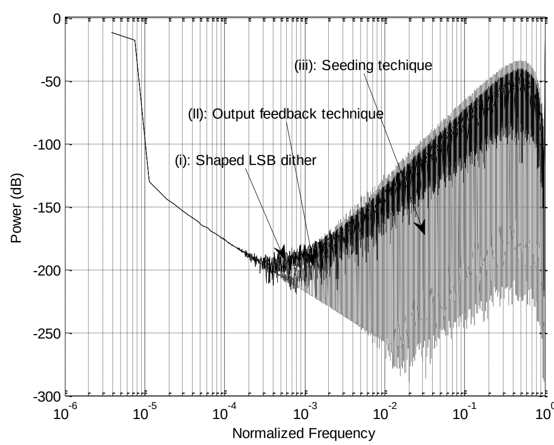

Fig. 8: PSD of a third order SQ_EFM with n=13 and input =$2^n/2$. The FFT length NFFT=2^{18}; (i) Shaped LSB dither, (ii) Output feedback technique and (iii) Seeding technique

Simulations show that in term of randomization, the dithering technique and output feedback technique are almost the same [10] and while implementation, they need almost the same circuitry [3]. But, due to the fact that dithering technique increases the in-band phase noise, it can be said that it's better to use output feedback technique in all cases instead of dithering technique. In cases that coefficient of feedback is unity; definitely, the output feedback technique is the best option, since it does not need any extra circuitry. It is proven mathematically that the performance of the output feedback technique in randomization is far beyond that of seeding technique. In contrast, the seeding technique needs only a few extra hardware to set the first flip-flop of the first accumulator each time the frequency control word changes. To make a conclusion it can be said that from randomization point of view, the output feedback approach is the best alternative technique, particularly in cases that the output feedback coefficient is unity. However, it can be noticed that with large number of input bits, the randomization of seeding technique is acceptably good. Fig. 9 shows the autocorrelation function of quantization error of a SQ_EFM for n=22 and input=$2^{22}/2$. Obviously, there are some peaks in the diagram but they are almost negligible. At the same time, if output feedback technique is utilized, a 22-bit adder will be added. Apparently in cases that hardware is troublesome; one can make a tradeoff between hardware and spurious content and choose seeding technique.

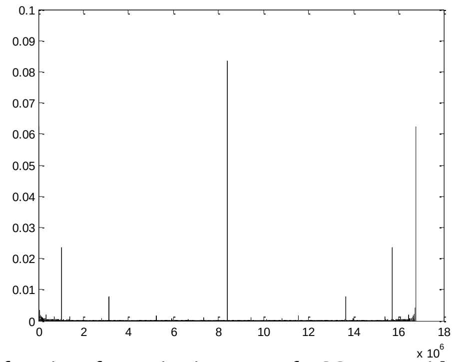

Fig. 9: Autocorrelation function of quantization error of a SQ_EFM with n=19 bit and input=$2^n/2$

3.3 In-band and out of band phase noise

Consider a fractional-N PLL in locked condition; the average of the divider output frequency (f_{div}) is equal to reference frequency (f_{ref}). But, due to the variations in divider modulus, instantaneous f_{div} is a bit different from f_{ref}. This difference is the cause of a phase error at the input of the PFD. The more the range of variation in divider modulus is, the more the phase error happens. Since this variation is produced by DDSM, the less the DDSM's output levels is, the less this phase error becomes. Based on [11], as the high frequency shaped-noise attenuates, the range of variation of DDSM's output reduces. MASH 1-1-1, SQ_EFM and SQ_MFM have the same NTF, which does not attenuate the high frequency shaped noise, while the NTF of the last one has two extra poles that significantly reduce the high frequency shaped noise. The magnitude of NTF of these modulators is drawn in Fig. 10. As offset frequency increases from $0.24f_{ref}$, the quantization noise is more attenuated in SQ_MFFM than the other modulators. So, three mentioned DDSMs modulators cause almost the same phase error but SQ_MFFM produces significantly lower phase error. Fig. 11 shows the phase error histogram of a SQ_EFM with n=19 bit and input =0.49 and Fig. 12 shows the same diagram for a SQ_MFFM with the same conditions. Variance is 0.2 in former and 0.22 in later, which indicates the superiority of SQ_MFFM from other DDSMs in term of phase error.

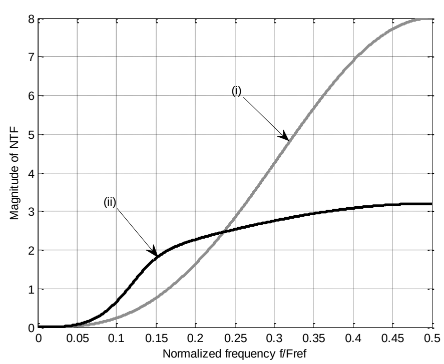

Fig. 10: The magnitude of NTF of (i) MASH 1-1-1, SQ_EFM, SQ_MFM and (ii) SQ_MFFM

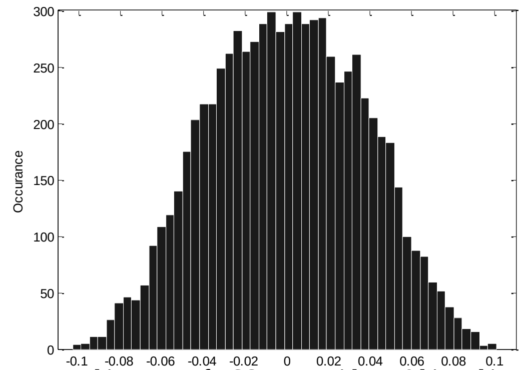

Fig. 11: Phase error histogram of a SQ_EFM with n=19 bit and input =0.49

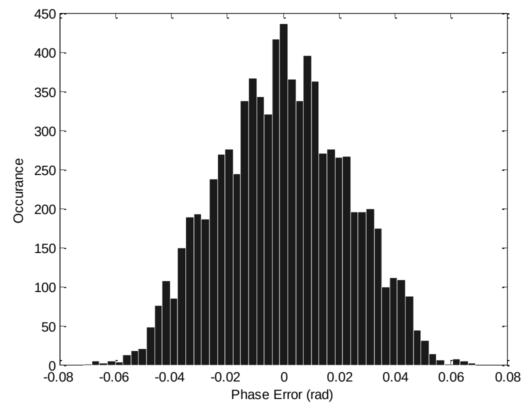

Fig. 12: Phase error histogram of a SQ_MFFM with n=19 bit and input =0.49

Since MASH 1-1-1, SQ_EFM and SQ_MFM have the same NTF; their in-band phase noise is approximately the same. But, as Fig. 10 shows, the low frequency quantization noise in SQ_MFFM is significantly larger than other modulators; consequently, SQ_MFFM has the worst in-band phase noise. This problem is got worse when dither signal is added to more randomize the output since dithering technique degrades the in-band phase noise. Three mentioned spur reduction techniques have no effect on phase error, as simulations confirm it.

Finally, in-band and out of band phase noise put upper limit to the value of BW. This effect is discussed in [11] in more detail.

3.4 Result

To choose a correct DDSM between four types presented here, a trade off needs to be hold. If out of band phase noise is critical, SQ_MFFD or a structure with extra poles on denominator needs to be chosen with LSB dither signal. Not only the in-band phase noise in this modulator is higher but also dithering worsens the issue. Otherwise, one of the other three modulators with a proper dithering technique, stated in detail in section 3.2, can be chosen. These modulators have the same in-band and out of band phase noise characteristic, so required hardware, stable input range (with regarding to quantizer output levels and interval) and implementation complexity are the other parameters to be counted.

4. Simulation Result

A 2.4 GHz fractional-N frequency synthesizer with four different DDSMs is simulated in MATLAB. Output feedback technique is used for MASH 1-1-1, SQ_EFM and SQ_MFM and non-shaped dithering is used for SQ_MFFM. The characteristics of PLL are shown in TABLE I. The lock time, which attributes to frequency step from 2.4 GHz to 2.5 GHz, is

100 us. To reach high frequency resolution and use output feedback technique without increasing in hardware, input bit number is chosen 19; in this way**,** the output feedback coefficient is unity and frequency resolution is 40 Hz. The output PLL spectrums of three first modulators are almost the same and here, for instance, the output spectrum of PLL with MASH 1-1-1 is surveyed. Fig. 10 and Fig. 11 show the measured spectrum of PLL at 2.41 GHz using 3-b third order MASH 1-1-1 and SQ_MFFM. From offset frequency about 300 KHz to about 4 MHz, MASH 1-1-1 has better phase noise than SQ_MFFM. But, from offset frequency 5 MHz, phase noise in SQ_MFFM is lower than MASH 1-1-1 and decreases with more slop than that of MASH 1-1-1.

5. Conclusion

In this paper a systematic design of a fractional-N PLL was presented. Four types of DDSMs were compared and three spur reduction techniques as well. Other essential factors in choosing DDSM were discussed.

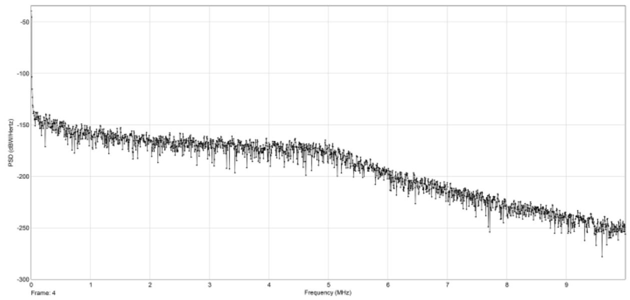

Fig. 13: Output spectrum of PLL with MASH 1-1-1

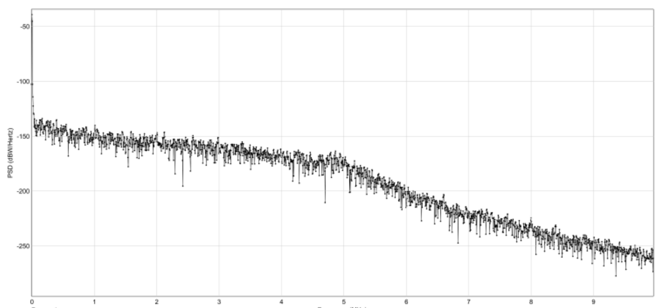

Fig. 14: Output spectrum of PLL with SQ_MFFM

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