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Power Efficient RF/mm-wave Oscillators and Power Amplifiers for Wireless Applications

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Power Efficient RF/mm-wave Oscillators and Power Amplifiers for Wireless Applications

Masoud Babaie

Power Efficient RF/mm-wave Oscillators and Power Amplifiers for Wireless Applications

Proefschrift

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus prof. ir. K.C.A.M. Luyben;
voorzitter van het College voor Promoties,
in het openbaar te verdedigen op

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door

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Printed in the Netherlands.

To my lovely parents, Mahmoud and Shahin
To my lovely brothers, Saeed and Kasra
And last, but not least, to my lovely wife Mina and her respected family

"Insanity is doing the same thing over and over again and expecting different results."

Albert Einstein, 1879-1955

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Chapter

1

Introduction

While mobile phones enjoy the largest production volume ever of any consumer electronics products, the demands they place on RF/mm-wave transceivers are particularly aggressive, especially on integration with digital processors, low area, low power consumption, while being robust against process-voltage-temperature (PVT) variations. Figure 1.1 (a) illustrates the evolution of data rates for wireless LAN, cellular, and wireline short links over time [1]. Interestingly, there is a constant ∼10× increase in bit rate every five years for both wireline and wireless links. Since mobile terminals inherently operate on batteries, their power budget is basically constant. Hence, an ever-decreasing power per bit is required to maintain the system lifetime. As shown in Fig. 1.1 (b), the RF front-end circuitry consumes significant power for typical use cases of mobile terminals such as voice call, web browsing and email [2]. Consequently, power efficiency of RF building blocks has become a major issue, especially when designing system-on-chips (SoC) for wireless communications.

On the other hand, in the upcoming years, the wireless Internet-of-Things (IoT) will enable more objects to be sensed and controlled remotely, realizing more integration between the physical and digital worlds. According to the communications giant Cisco Systems [3], there are currently approximately 15 billion internet-connected objects (things) which is slated to reach 50 billion by 2020, just 2.7 percent of all the things that will be on the planet. However, the system lifetime still tends to be severely limited by its power consumption, available battery technology and efficiency of its energy harvester. Consequently, the key challenge of these wireless sensors is the ability to function at the lowest power possible while being robust to PVT variations. Similarly, the power consumption of RF building blocks should be reduced to satisfy the lifetime demands of IoT systems. Furthermore, RF circuitries such as oscillator and PLL should be able to turn on/off quickly to permit high energy-efficiency during intermittent operation.

It is well known that the power amplifier (PA) is the most power hungry building block of

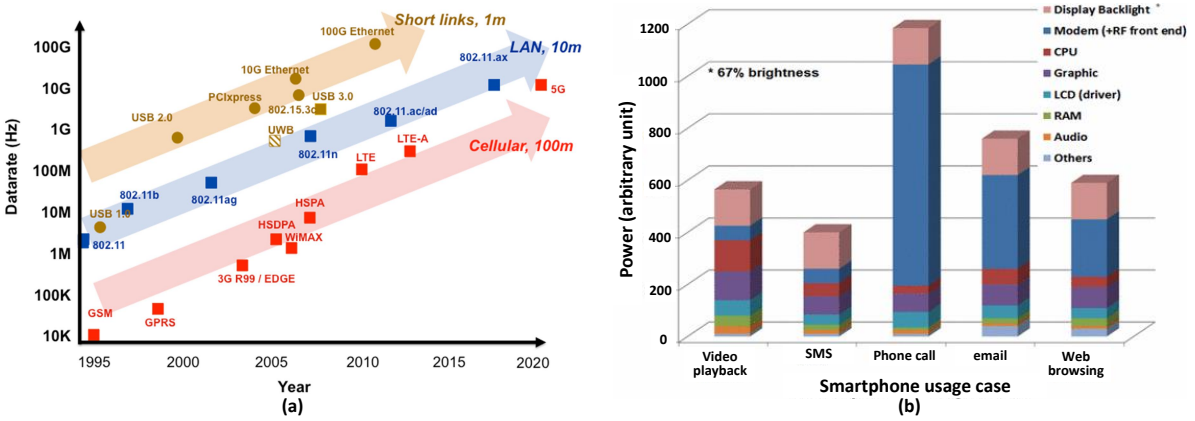


Figure 1.1: (a) evolution of data rates for wireless LAN, cellular, and wireline short links over time [1]; (b) power usage in a smartphone [2].

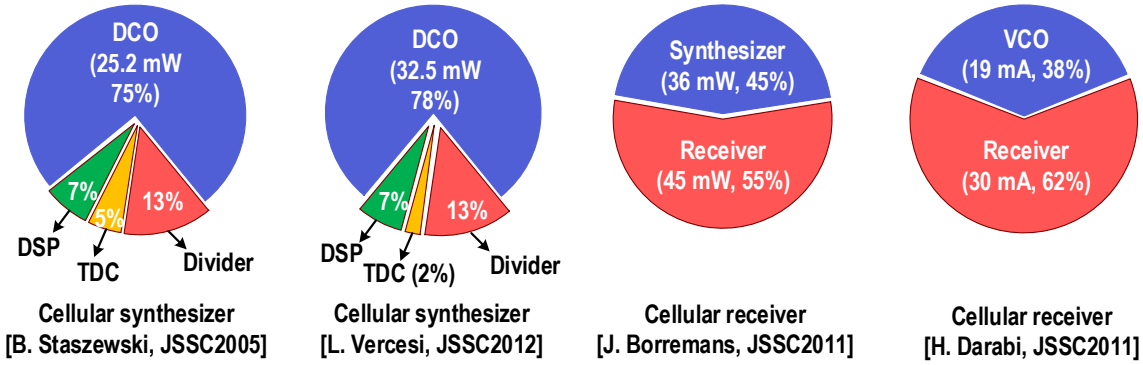


Figure 1.2: Contribution of RF oscillator to the power consumption of cellular frequency synthesizers and receivers.

any wireless radio and consequently any improvement on its power efficiency can significantly extend the battery lifetime of the entire radio. Furthermore, PAs need at least one matching network (including capacitors, inductors and transmission lines) in order to efficiently deliver power to the load. These passives usually occupy large surface on the chip thus making PA as the most area hungry and, consequently, most expensive block in any RF/mm-wave transceiver. This naturally leads to the conclusion that increasing the PA's power efficiency while reducing its size, can significantly improve the performance and cost of the entire wireless system.

The RF oscillator is the second most power hungry block of a wireless radio. As shown in Fig. 1.2, the RF oscillator consumes a disproportionate amounts of the power of a cellular frequency synthesizer [4, 5] and burns more than 30% of the cellular receiver power [6, 7]. Consequently, any power reduction in an RF oscillator will greatly benefit the overall power efficiency of the cellular transceiver. For IoT applications, the commercial perspective is now focusing on Bluetooth Low Energy (BLE). In the state-of-the-art BLE radios [8–10], the PLL power consumption is merely 3-4× lower than that of PA at the maximum BLE output power of 1 mW. However, the frequency synthesizer activity is much longer than that of a PA, making the PLL the most energy-hungry block in a BLE transceiver.

In this dissertation, the main goal is to innovate the RF/mm-wave oscillator and power amplifier structures that demonstrate better performance, lower cost, and higher power efficiency than traditional architectures.

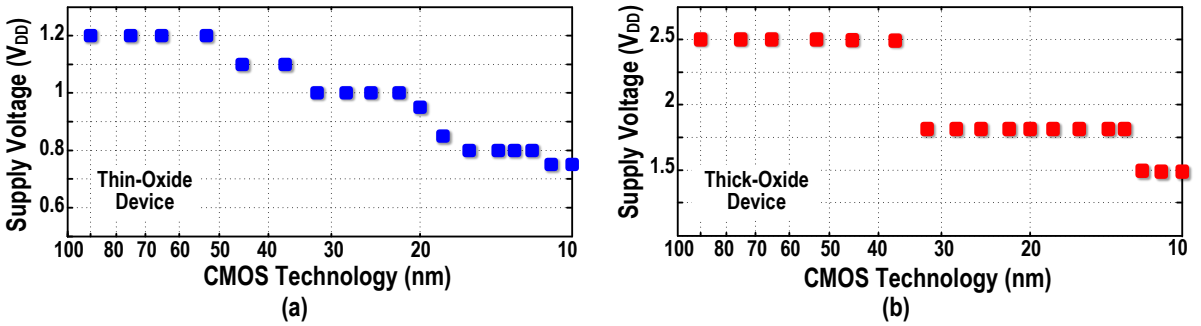


Figure 1.3: Nominal supply voltage versus CMOS technology node for (a) thin-oxide and (b) thick-oxide device.

1.1 Technology Scaling

The size, cost, and power consumption of digital circuits are reduced by technology scaling. However, the design of analog and RF circuits faces many difficulties using more advanced CMOS technologies. Consequently, in the semiconductor industry, there are two divergent trends for choosing a technology node for fabricating analog circuits. One trend is to implement analog circuits in older technology to exploit a higher voltage headroom. This approach is chiefly more in medical, automotive, and high-efficiency lighting applications [11]. Another trend is to implement analog and digital circuits together in the most advanced node such as a 16-nm FinFET. The approach is dictated by the market to achieve highest digital performance with lowest fabrication cost.

The vision for both wireless cellular communication and the Internet of Things keeps moving towards the second strategy [12]. For example, IMEC recently published the first integrated wireless sensor node in 40-nm CMOS including a microcontroller, digital baseband, power management, and BLE transceiver [8]. Furthermore, Intel and DMCE presented a SAW-less HSPA transceiver with on-chip integrated 3G power amplifiers in 65nm at ISSCC 2015 to enable real low-cost monolithic system integration [13]. Consequently, it is instructive to investigate the effects of technology scaling on the performance of an RF/mm-wave oscillator and power amplifiers.

1.1.1 Supply Voltage

To continue implementing increasingly complex functions while reducing the overall solution costs, scaling of CMOS transistors is inevitable. As circuits become denser, all of the physical dimensions of the transistors must be reduced correspondingly. The SiO_2 oxide-layer thickness reduction is accompanied by migrating to smaller supply voltages (see Fig. 1.3). This is to maintain the electric field strength across the oxide in order to prevent the device performance degradation due to the time dependent dielectric breakdown (TDDB) [14]. The supply voltage, V_{DD}, is reduced while RF and analog circuits must maintain their dynamic range, noise performance and output power. For example, the oscillator phase noise performance and power amplifier output power (P_{out}) degrade by 6 dB/octave with the reduction of their supply voltage [15]. To compensate this phase noise penalty, the equivalent input parallel resistance of an LC tank should be proportionally decreased by reducing the tank's inductance. However, the

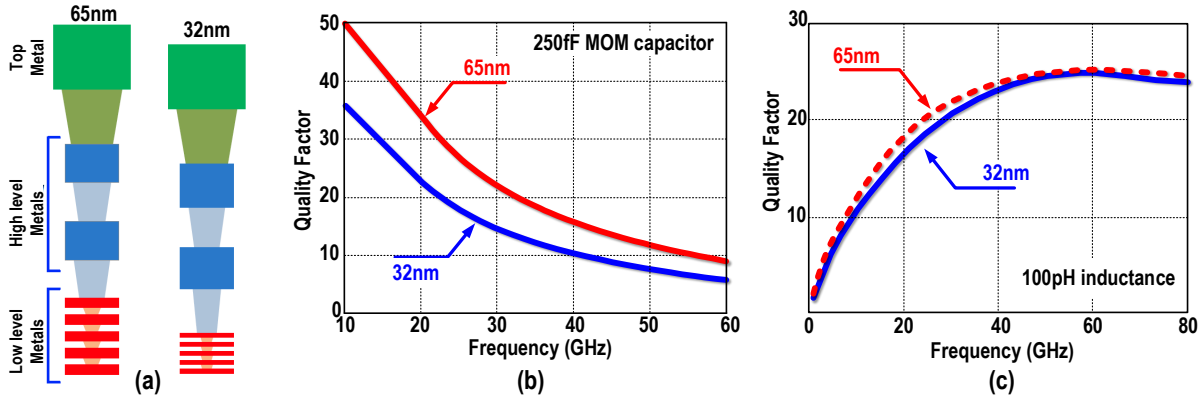


Figure 1.4: (a) Back-end-of-line (BEOL) metallization; quality factor of (b) a 250 fF capacitor, and (c) a 100 pH inductor in 65 nm and 32 nm CMOS technologies [16].

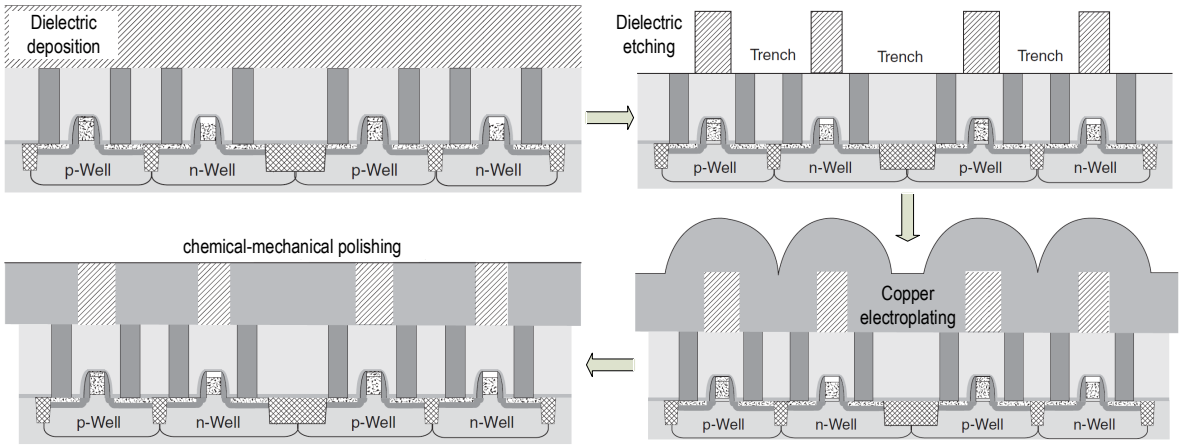


Figure 1.5: Damascene process steps [17].

resistance of the tank's interconnects will start dominating the resonator losses and, consequently, the effective Q-factor and oscillator power efficiency will dramatically drop. To compensate P_{out} penalty in the power amplifier, a smaller load must be seen by PA's transistors. Hence, the PA's matching network must provide a higher impedance transformation ratio. It leads to a larger insertion loss of the matching network and thus a lower efficiency of the PA.

1.1.2 Quality Factor of Passives

Most RF/mm-wave CMOS oscillators and power amplifiers employ passive components such as integrated inductors, transformers, and capacitors to realize on-chip LC tanks and matching/biasing networks. Generally, top thick metal layers are used for the realization of inductive components while thinner lower-level metals are exploited in metal-oxide-metal (MoM) capacitors. Note that the 0.18 μm node was the last generation of 8-inch wafer processes with aluminum metallization as almost all modern processes use copper metallization that improves the resistive loss and current handling capability of passive components. Consequently, the quality factor of passives was improved when RF products migrated from 0.18 μm to 0.13 μm technology.

By migrating to more advanced nano-scale CMOS technologies, however, the thickness of

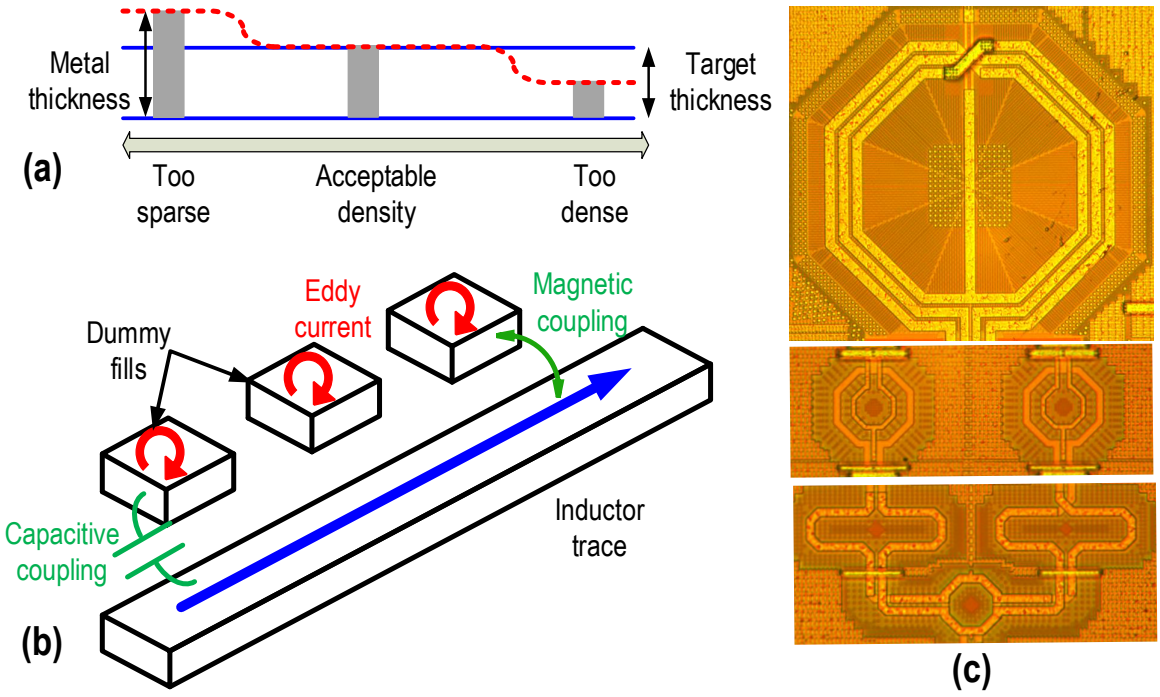


Figure 1.6: (a) Thickness variation by erosion in the CMP stage; (b) electromagnetic coupling between the wire and dummy fills; (c) inductor/transformer with lots of dummy metal fills.

lower level metals and interlayer dielectric layers reduce correspondingly as shown in Fig. 1.4 (a). As a consequence, the physical dimension of a given capacitance becomes smaller but with a worse quality factor (see Fig. 1.4 (b)). Fortunately, the thickness of top thick metal layers almost remains constant with scaling. However, the top-metal is closer to the lossy substrate. Hence, the capacitive parasitic, self-resonant frequency, and quality factor of inductor/transformer slightly degrade with scaling as shown in Fig. 1.4 (c).

As mentioned above, in most advanced CMOS technologies, copper is used for interconnections due to its low sheet resistance, high maximum current density, high thermal conductivity and resilience to electromigration failures. However, it is difficult to pattern copper using conventional etching techniques. Consequently, unlike traditional metallization of aluminum, copper metallization needs an additional damascene process as shown in Fig. 1.5 [17]. The inter-level dielectric is first deposited in the damascene process. Secondly, the dielectric is etched to define trenches where the metal lines will lie. Thirdly, copper is electroplated to fill the patterned oxide trenches. Finally, the surface is planarized and polished to remove surplus copper outside the desired metal lines using chemical-mechanical polishing (CMP). Unfortunately, CMP suffers from dishing and erosion phenomena. Since copper is much softer than the inter-level dielectric, areas with higher metal density are polished much faster than the others. Consequently, the metal thickness of the sparse areas become thicker than that of the dense places as shown in Fig. 1.6 (a) [18]. To resolve this issue, a minimum metal density must be satisfied for the entire chip. For example, the minimum metal density must be at least 25% in any 100 μm$\times$100 μm square in a 28-nm technology. Hence, inductors and transformers must include dummy metal pieces from the lowest to the highest metal layer (see Fig. 1.6 (c)). Metal dummies show negligible effects on the windings self-inductance and the coupling factor. However, as shown in Fig. 1.6 (b), eddy currents in dummy fills increase the loss and thus the inductor's/transformer's Q-factor

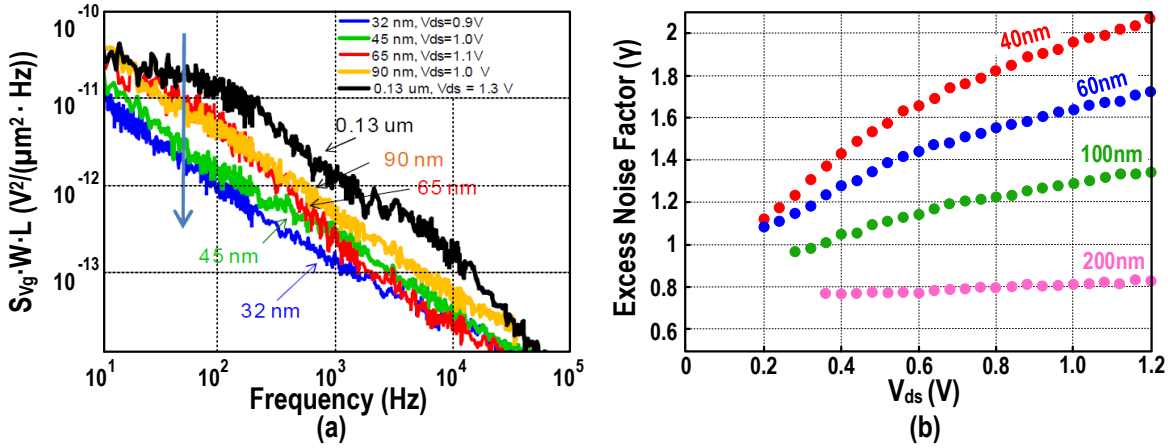


Figure 1.7: (a) Flicker noise scaling trend; (b) measured excess noise (γ) factor versus drain-source voltage at 10 GHz and $V_{gs} = 1.0$ V for different gate lengths of NMOS transistors in 40 nm LP technology [20].

could be degraded by 10% [19].

To conclude this section, the quality factor of passives degrades by migrating to more advanced nano-scale CMOS technologies. It leads to a worse phase noise performance for oscillators and a larger insertion loss for matching networks of power amplifiers.

1.1.3 Noise of Active Devices

Figure 1.7 (a) shows the normalized input referred 1/f noise, S_{vg}, versus frequency for different technology nodes. Due to oxide scaling enabled by high-k/metal gate technologies, the normalized S_{vg} is monotonically reduced with each successive technology node. For the same transistor area, S_{vg} decreases ~10× from the 0.13 μm node to 32 nm node. However, as shown in Fig. 1.7 (b), the excess noise factor of CMOS transistors increases by migrating to finer CMOS technologies. Consequently, oscillator's core transistors inject more thermal noise to the tank, degrading its phase noise performance.

1.2 Thesis Objectives

Based on the aforementioned explanations in Section 1.1, the underlying objective of this dissertation is, therefore, to implement innovative RF/mm-wave oscillator and power amplifier structures to improve the power efficiency of the entire wireless transceiver. The first objective of this thesis is to introduce a new class of operation for RF oscillators to fill the performance/power gap in the ultra-high figure of merit (FoM) and ultra-low phase noise oscillator space currently not satisfied by state-of-the-art structures. The proposed oscillator is also implemented as the heart of an all-digital phase-locked loop to demonstrate its effectiveness on improving the power efficiency of a 4G frequency synthesizer. The second objective is to analyze and understand various design parameters and tradeoffs in the design space of switched-mode power amplifiers. These insights will lead to the design and implementation of two different power amplifiers operating at 2.4 GHz and 60 GHz. The third objective of this thesis is to improve the power

efficiency of a Bluetooth Low Energy transmitter by exploiting a novel digitally controlled oscillator and a class-E/F_2 switched-mode power amplifier.

1.3 Thesis Outline

This thesis is composed of three parts. The main focus of the first part is on the design and implementation of innovative RF oscillators for cellular applications. A comprehensive analysis of switched-mode amplifiers and the design and implementation of a wideband class-E/F_2 mm-wave PA are presented in the second part. Finally, a new transmitter architecture for ultra-low power radios is introduced in the third part of this dissertation.

The first part starts with Chapter 2 by introducing an oscillator topology demonstrating an improved phase noise performance. The proposed oscillator operates in class-F by enforcing a pseudo-square voltage waveform around the LC tank by increasing the third harmonic of the fundamental oscillation voltage through an additional impedance peak. Measurement results of an implemented 65 nm prototype are presented and compared with state-of-the-art oscillators. Furthermore, a comprehensive study of circuit-to-phase-noise conversion mechanisms of different classes of RF oscillator is presented.

In Chapter 3, the proposed class-F oscillator is exploited in a 28 nm all-digital PLL (ADPLL) for 4G mobile phones. Functions of the different building blocks of this PLL are briefly explained. Due to the class-F operation of the digitally controlled oscillator (DCO), the ADPLL demonstrates a 72% power reduction over prior records.

In Chapter 4, a new class of operation for RF oscillators is introduced. The main idea is to enforce a clipped voltage waveform around the LC tank by increasing the second-harmonic of fundamental oscillation voltage through an additional impedance peak, thus giving rise to a class-F_2 operation. This oscillator specifically addresses the ultra-low phase noise design space while maintaining high power efficiency. Extensive experimental results and an insightful reliability analysis are also presented at the end of this chapter.

The second part of this thesis starts with Chapter 5 where a comprehensive analysis of switched-mode amplifiers is presented. Precise analytical voltage-current waveforms, zero-voltage, and zero-slope switching criteria and waveform-dependent parameters of any flavor of a switched-mode PA are quantified. Furthermore, closed-form equations are derived for the optimum size of the switch and different PA's characteristics such as maximum achievable power added efficiency, output power, and maximum operating frequency.

In Chapter 6, a fully integrated 60 GHz power amplifier is presented. The benefits, constraints, and trade-offs of different transmitter structures and extended class-E/F_2 PA are investigated from the mm-wave viewpoint. Implementation details and chip measurement results are also presented. This PA reaches the highest reported product of power-added efficiency and bandwidth. It is achieved through low/moderate coupling-factor transformers in the preliminary stages and a proper second harmonic termination of the output stage, such that it can operate as a class-E/F_2 switched-mode PA at the saturation point.

Chapter 7 is the last part of the dissertation. A novel digitally controlled oscillator with switching current sources is introduced to reduce supply voltage and power without sacrificing its phase noise and startup margins. A fully integrated differential class-E/F_2 switching PA is designed to improve system efficiency at a low output power of 0-3 dBm while fulfilling all

in-band and out of band emission masks. The required matching network is realized by exploiting different behaviors of a 2:1 step-down transformer in differential and common-mode excitations. Based on those innovations, an ultra-low power Bluetooth Low Energy transmitter is proposed that demonstrates the best ever reported system efficiency and phase purity while abiding by the strict 28 nm CMOS technology manufacturing rules.

Finally, Chapter 8 concludes this dissertation and presents suggestions for future developments.

1.4 Original Contributions

The original contributions to the body of knowledge of Solid-State Circuits Society are as follows:

- Introducing a new class of operation of an RF oscillator (Chapter 2, 4);
- Comprehensive analysis of circuit-to-phase-noise conversion mechanisms of different oscillators structures and dispelling common myths (Chapter 2, 4);
- Adapting the proposed class-F oscillator into a 28 nm all-digital phase-locked loop while abiding by strict metal density rules (Chapter 3);
- Applying the general knowledge of CMOS device reliability to high-performance RF oscillators (Chapter 4);
- Comprehensive analysis and systemization of different flavors of class-E/F power amplifiers (Chapter 5);
- Design, implementation, and test of a mm-wave power amplifier with the highest product of power-added efficiency and bandwidth. (Chapter 6);
- Proposing and verifying a switching current source oscillator for ultra-low voltage and power applications (Chapter 7);
- Design and implementation of a fully integrated differential class-E/F_2 switching PA for BLE transmitter (Chapter 7).

Chapter

2

A Class-F CMOS Oscillator

An oscillator topology demonstrating an improved phase noise performance is proposed in this Chapter[1]. It exploits a time-variant phase noise model with insights into the phase noise conversion mechanisms. The proposed oscillator is based on enforcing a pseudo-square voltage waveform around the LC tank by increasing the third-harmonic of the fundamental oscillation voltage through an additional impedance peak. This auxiliary impedance peak is realized by a transformer with moderately coupled resonating windings. As a result, the effective impulse sensitivity function (ISF) decreases thus reducing the oscillator's effective noise factor such that a significant improvement in the oscillator phase noise and power efficiency are achieved. A comprehensive study of circuit-to-phase-noise conversion mechanisms of different oscillators' structures shows the proposed class-F exhibits the lowest phase noise at the same tank's quality factor and supply voltage. The prototype of the class-F oscillator is implemented in TSMC 65-nm standard CMOS. It exhibits average phase noise of -142 dBc/Hz at 3 MHz offset from the carrier over 5.9—7.6 GHz tuning range with figure-of-merit of 192 dBc/Hz. The oscillator occupies 0.12 mm^2 while drawing 12 mA from 1.25 V supply.

2.1 Introduction

Designing voltage-controlled and digitally-controlled oscillators (VCO, DCO) of high spectral purity and low power consumption is quite challenging, especially for GSM transmitter (TX), where the oscillator phase noise must be less than -162 dBc/Hz at 20 MHz offset frequency from 915 MHz carrier [22]. At the same time, the RF oscillator consumes disproportionate amount of power of an RF frequency synthesizer [4], [5] and burns more than 30% of the cellular RX power [7], [23]. Consequently, any power reduction of RF oscillators will greatly benefit

[1]This chapter has been published in the IEEE Journal of Solid-State Circuits [21].

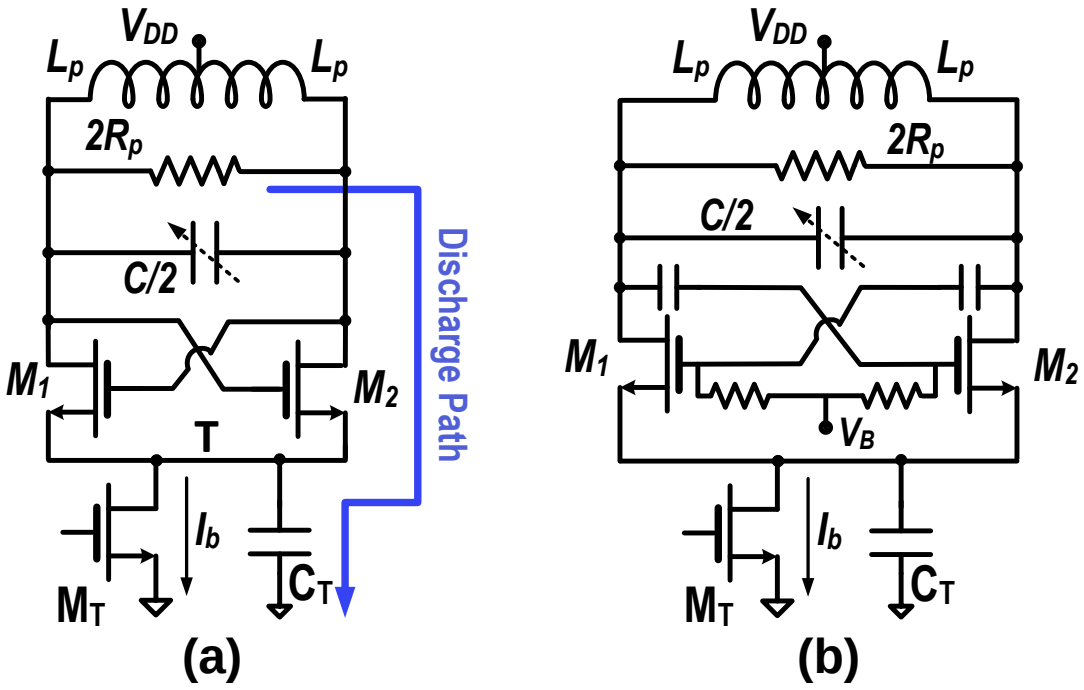


Figure 2.1: Oscillator schematic: (a) traditional class-B; (b) class-C.

the overall transceiver power efficiency and ultimately the battery lifetime. This motivation has encouraged an intensive research to improve the power efficiency of an RF oscillator while satisfying the strict phase noise requirements of the cellular standards.

The traditional class-B oscillator (Fig.2.1(a)) is the most prevalent architecture due its simplicity and robustness. However, its phase noise and power efficiency performance drops dramatically just by replacing the ideal current source with a real one. Indeed, the traditional oscillator reaches its best performance for the oscillation amplitude of near supply voltage V_{DD} [24], [25]. Therefore, the gm-devices $M_{1/2}$ enter deep triode for part of the oscillation period. They exhibit a few tens of ohms of channel resistance. In addition, the tail capacitor C_T should be large enough to filter out thermal noise of M_T around the even harmonics of the fundamental, thus making a low impedance path between node "T" and ground. Consequently, the tank output node finds a discharge path to the ground. It means that the equivalent Q-factor of the tank is degraded dramatically. This event happens alternatively between M_1 and M_2 transistors in each oscillation period. Hence, the phase noise improvement would be negligible by increasing the oscillation voltage swing when the gm-devices enter the triode region and thus, FoM drops dramatically. This degradation seems rather unavoidable in the simple structure of Fig. 2.1(a) since M_T must anyway be very large to reduce the $1/f^3$ phase noise corner of the oscillator and thus its parasitic capacitor alone (i.e., even if C_T is zero) would be large enough to provide discharge path for the tank during the gm-device triode region operation.

The noise filtering technique [26] provides a relatively high impedance between the gm-devices and the current source. Hence, the structure maintains the intrinsic Q-factor of the tank during the entire oscillation period. However, it requires an extra resonator sensitive to parasitic capacitances, increasing the design complexity, area and cost.

Class-C oscillator (Fig.2.1(b)), prevents the gm-devices from entering the triode region [27], [28]. Hence, the tank Q-factor is preserved throughout the oscillation period. The oscillator

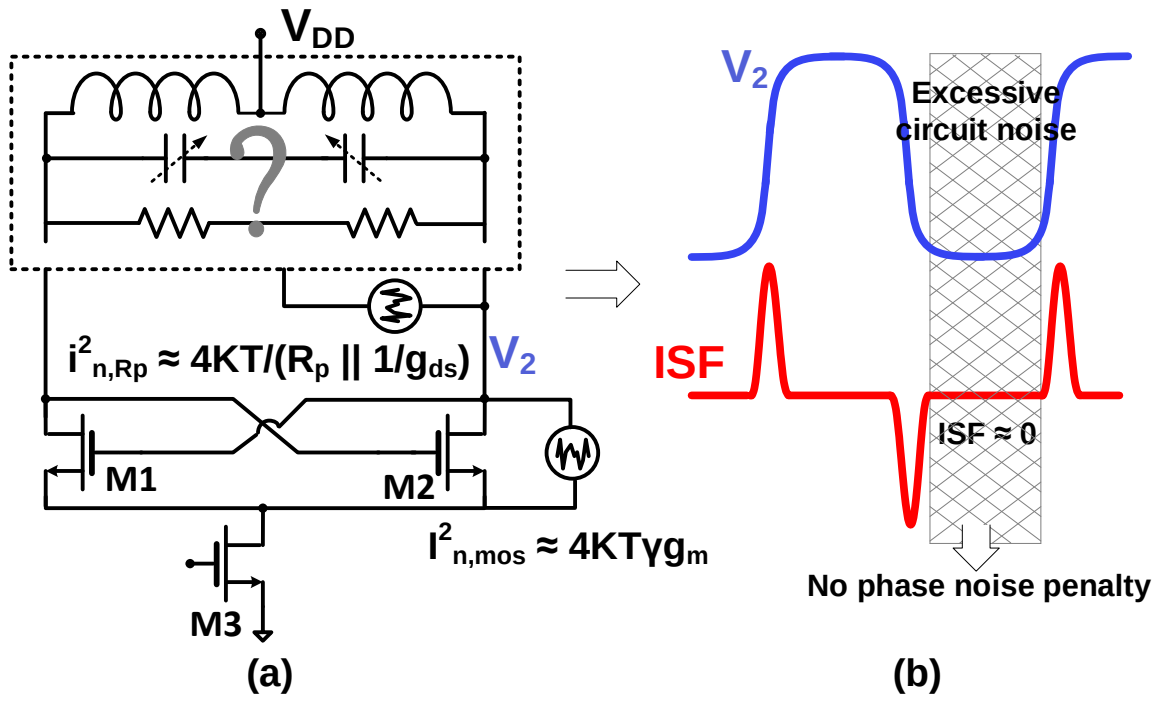


Figure 2.2: Oscillator: (a) noise sources; (b) targeted oscillation voltage (top) and its expected ISF (bottom).

also benefits with 36% power saving from changing the drain current shape from square-wave of the traditional oscillator to the "tall and narrow" form for the class-C operation. However, the constraint of avoiding entering the triode region limits the maximum oscillation amplitude of the class-C oscillator to around $V_{DD}/2$, for the case of bias voltage V_B as low as a threshold voltage of the active devices. It translates to 6 and 3 dB phase noise and FoM penalty, respectively. Consequently, class-C voltage swing constraint limits the lowest achievable phase noise performance.

Harmonic tuning oscillator enforces a pseudo-square voltage waveform around the LC tank through increasing the third-harmonic component of the fundamental oscillation voltage through an additional tank impedance peak at that frequency. Kim *et al.* [29] exploited this technique to improve the phase noise performance of the LC oscillator by increasing the oscillation zero-crossings' slope. However, that structure requires more than two separate LC resonators to make the desired tank input impedance. It increases die area and cost and decreases tuning range due to larger parasitics. Furthermore, the oscillator transconductance loop gain is the same for both resonant frequencies, thus raising the probability of undesired oscillation at the auxiliary tank input impedance. We have resolved the above mentioned concerns and quantified intuitively and theoretically the phase noise and power efficiency improvement of the class-F oscillator compared to other structures [30].

The Chapter is organized as follows: Section 2.2 establishes the environment to introduce the proposed class-F oscillator. The circuit-to-phase-noise conversion mechanisms are studied in Section 2.3. Section 2.4 presents extensive measurement results of the prototype, while Section 2.5 wraps up this Chapter with conclusions.

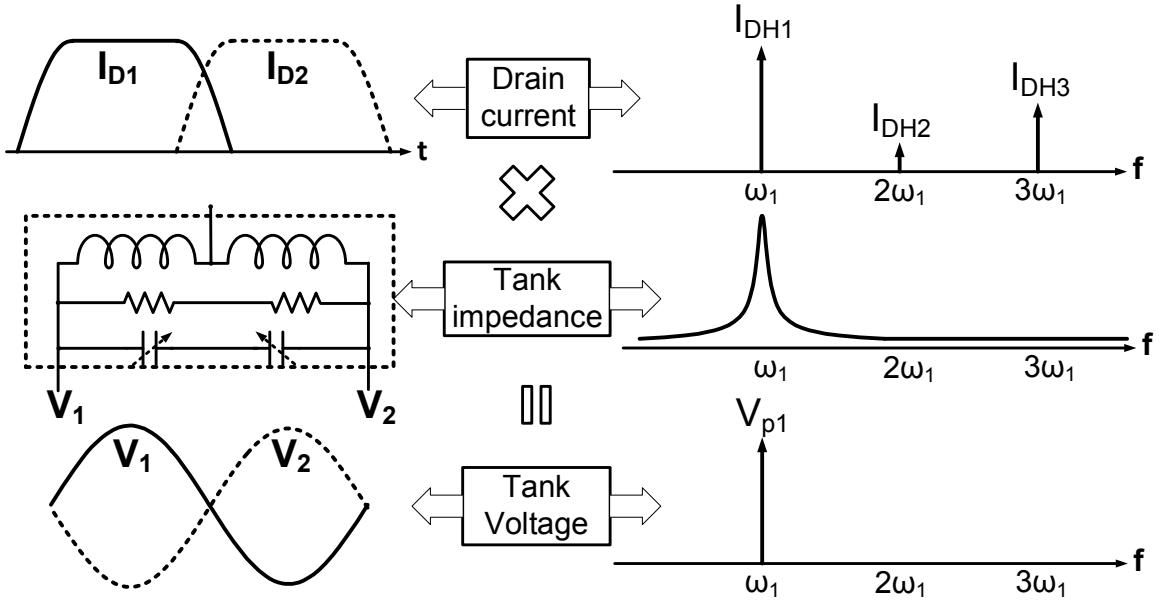


Figure 2.3: Traditional oscillator waveforms in time and frequency domains.

2.2 Evolution Towards Class-F Oscillator

Suppose the oscillation voltage around the tank was a square-wave instead of a sinusoidal. As a consequence, the oscillator would exploit the special ISF [31] properties of the square-wave oscillation voltage to achieve a better phase noise and power efficiency. However, the gm-devices would work in the triode region (shaded area in Fig. 2.2(b)) even longer than in case of the sinusoidal oscillator. Hence, the loaded resonator and gm-device inject more noise to the tank. Nevertheless, ISF value is expected to be negligible in this time span due to the zero derivative of the oscillation voltage [31]. Although the circuit injects huge amount of noise to the tank, the noise cannot change the phase of the oscillation voltage and thus there is no phase noise degradation.

2.2.1 Realizing a Square-Wave across the LC Tank

The above reasoning indicates that the square-wave oscillation voltage has special ISF properties that are beneficial for the oscillator phase noise performance. But how can a square-wave be realized across the tank? Let us take a closer look at the traditional oscillator in the frequency domain. As shown in Fig. 2.3, the drain current of a typical LC-tank oscillator is approximately a square-wave. Hence, it ideally has a fundamental and odd harmonic components. On the other hand, the tank input impedance has a magnitude peak only at the fundamental frequency. Therefore, the tank filters out the harmonic components of the drain current and finally a sinusoidal wave is seen across the tank.

Now, suppose the tank offers another input impedance magnitude peak around the third harmonic of the fundamental frequency (see Fig. 2.4). The tank would be prevented from filtering out the 3rd harmonic component of the drain current. Consequently, the oscillation voltage will contain a significant amount of the 3rd harmonic component in addition to the

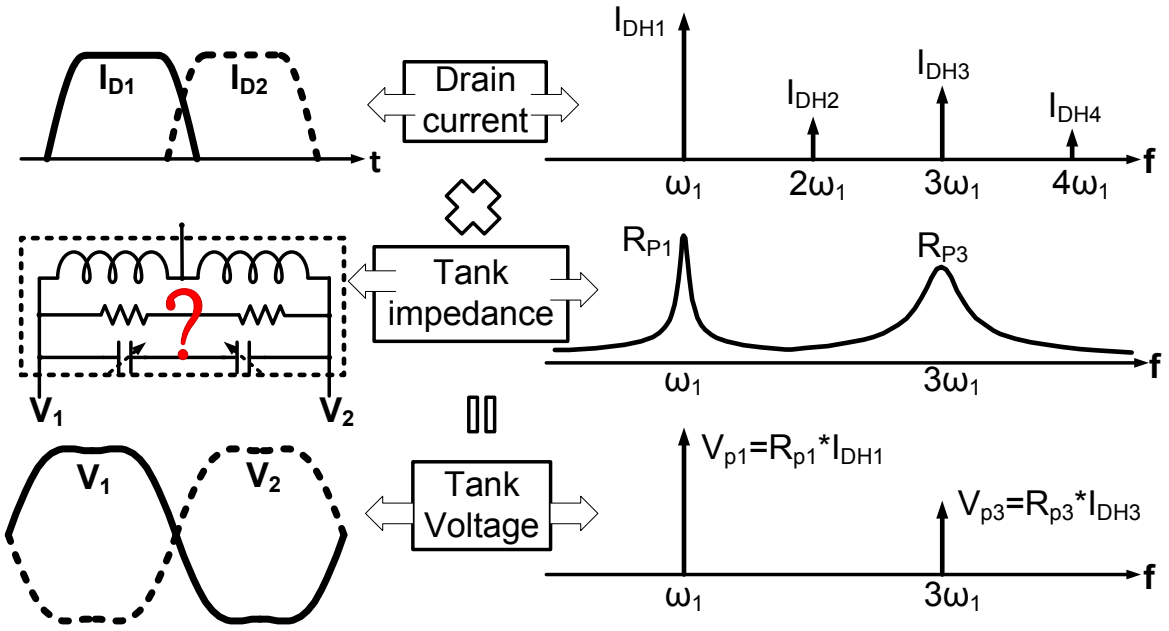


Figure 2.4: Proposed oscillator waveforms in time and frequency domains.

fundamental:

$$V_{in} = V_{p1}\sin(\omega_0 t) + V_{p3}\sin(3\omega_0 t + \Delta\phi) \tag{2.1}$$

ζ is defined as the magnitude ratio of the third-to-first harmonic components of the oscillation voltage.

$$\zeta = \frac{V_{p3}}{V_{p1}} = \left(\frac{R_{p3}}{R_{p1}}\right)\left(\frac{I_{DH3}}{I_{DH1}}\right) \approx 0.33\left(\frac{R_{p3}}{R_{p1}}\right) \tag{2.2}$$

where, R_{p1} and R_{p3} are the tank impedance magnitudes at the main resonant frequency ω_1 and $3\omega_1$, respectively. Figure 2.5 illustrates the oscillation voltage and its related expected ISF function (based on the closed-form equation in [31]) for different ζ values. The ISF rms value of the proposed oscillation waveform can be estimated by the following expression for $-\pi/8 < \Delta\phi < \pi/8$.

$$\Gamma_{rms}^2 = \frac{1}{2}\frac{1+9\zeta^2}{(1+3\zeta)^2} \tag{2.3}$$

The waveform would become a sinusoidal for the extreme case of $\zeta = 0, \infty$ so (2.3) predicts $\Gamma_{rms}^2 = 1/2$, which is well-known for the traditional oscillators. Γ_{rms}^2 reaches its lowest value of $1/4$ for $\zeta = 1/3$, translated to a 3 dB phase noise and FoM improvement compared to the traditional oscillators. Furthermore, ISF of the proposed oscillator is negligible while the circuit injects significant amount of noise to the tank. Consequently, the oscillator FoM improvement could be larger than that predicted by just the ISF rms reduction.

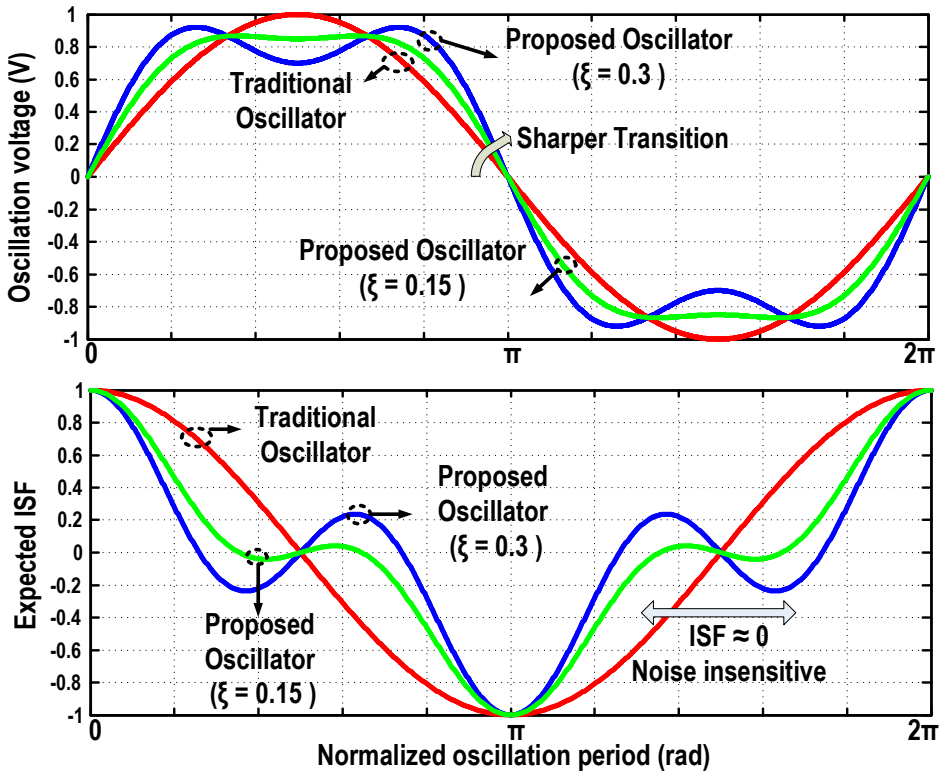


Figure 2.5: The effect of adding 3rd harmonic in the oscillation waveform (top) and its expected ISF (bottom).

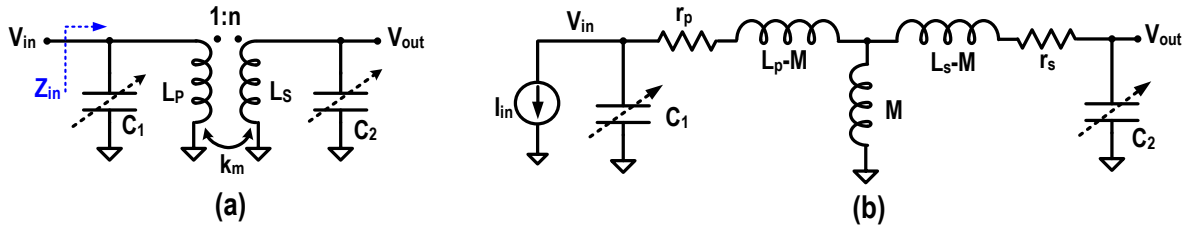


Figure 2.6: Transformer-based resonator (a); and its equivalent circuit (b).

2.2.2 Proposed Tank

The argumentation related to Fig. 2.4 above advocates the use of two resonant frequencies with a ratio of 3. The simplest way of realizing that would be with two separate inductors [29], [32]. However this will be bulky and inefficient. The chosen option in this work is a transformer-based resonator. The preferred resonator consists of a transformer with turns ratio n and tuning capacitors C_1 and C_2 at the transformer's primary and secondary windings, respectively (see Fig. 2.6). Eq. (2.4) expresses the exact mathematical equation of the input impedance of the tank.

$$Z_{in} = \frac{s^3\left(L_pL_sC_2\left(1-k_m^2\right)\right) + s^2\left(C_2\left(L_sr_p + L_pr_s\right)\right) + s\left(L_p + r_sr_pC_2\right)\right) + r_p}{s^4\left(L_pL_sC_1C_2\left(1-k_m^2\right)\right) + s^3\left(C_1C_2\left(L_sr_p + L_pr_s\right)\right) + s^2\left(L_pC_1 + L_sC_2 + r_pr_sC_1C_2\right)\right) + s\left(r_pC_1 + r_sC_2\right) + 1} \tag{2.4}$$

where, k_m is the magnetic coupling factor of the transformer, r_p and r_s model the equivalent series resistance of the primary L_p and secondary L_s inductances [33]. The denominator of

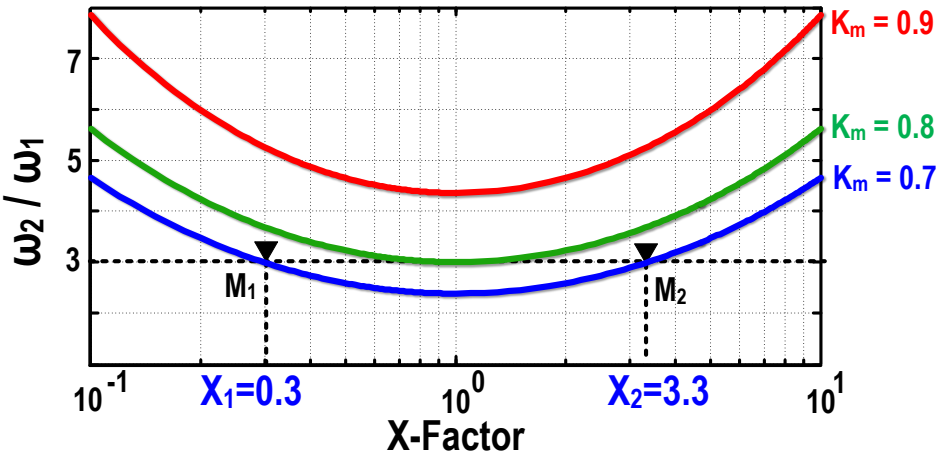


Figure 2.7: Ratio of the tank resonant frequencies versus X-factor for different k_m.

Z_{in} is a fourth-order polynomial for the imperfect coupling factor (i.e., $k_m < 1$). Hence, the tank contains two different conjugate pole pairs, which realize two different resonant frequencies. Consequently, the input impedance has two magnitude peaks at these frequencies. Note that both resonant frequencies can satisfy the Barkhausen criterion with a sufficient loop gain [34]. However, the resulting multi-oscillation behavior is undesired and must be avoided [35]. In our case, it is preferred to see an oscillation at the lower resonant frequency ω_1 and the additional tank impedance at ω_2 is used to make a pseudo-square waveform across the tank. These two possible resonant frequencies can be expressed as

$$\omega_{1,2}^2 = \frac{1 + \left(\frac{L_s C_2}{L_p C_1}\right) \pm \sqrt{1 + \left(\frac{L_s C_2}{L_p C_1}\right)^2 + \left(\frac{L_s C_2}{L_p C_1}\right)(4k_m^2 - 2)}}{2L_s C_2 \left(1 - k_m^2\right)} \tag{2.5}$$

The following expression offers a good estimation of the main resonant frequency of the tank for $0.5 \leq k_m \leq 1$.

$$\omega_1^2 = \frac{1}{(L_p C_1 + L_s C_2)} \tag{2.6}$$

However, we are interested in the ratio of resonant frequencies as given by

$$\frac{\omega_2}{\omega_1} = \sqrt{\frac{1 + X + \sqrt{1 + X^2 + X\left(4k_m^2 - 2\right)}}{1 + X - \sqrt{1 + X^2 + X\left(4k_m^2 - 2\right)}}} \tag{2.7}$$

where, X-factor is defined as

$$X = \left(\frac{L_s}{L_p} \cdot \frac{C_2}{C_1}\right) \tag{2.8}$$

Eq. 2.7 indicates the resonant frequency ratio ω_2/ω_1 is just a function of the transformer inductance ratio L_s/L_p, tuning capacitance ratio C_2/C_1, and transformer magnetic coupling factor k_m. The relative matching of capacitors (and inductors) in today's CMOS technology is expected to be much better than 1%, while the magnetic coupling is controlled through lithography that precisely sets the physical dimensions of the transformer. Consequently, the

relative position of the resonant frequencies is not sensitive to the process variation. The ω_2/ω_1 ratio is illustrated versus X-factor for different k_m in Fig. 2.7. As expected, the ratio moves to higher values for larger k_m and finally the second resonance disappears for the perfect coupling factor. The ratio of ω_2/ω_1 reaches the desired value of 3 at two points for the coupling factor of less than 0.8. Both points put ω_2 at the correct position of $3\omega_1$. However, the desired X-factor should be chosen based on the magnitude ratio $\mathrm{R}_{p2}/\mathrm{R}_{p1}$ of the tank input impedance at resonance. The sum of the even orders of the denominator in (2.4) is zero at resonant frequencies. It can be shown that the first-order terms of the numerator and the denominator are dominant at ω_1. By using (2.6), assuming $Q_p = L_p\omega/r_p$, $Q_s = L_s\omega/r_s$, the tank input impedance at the fundamental frequency is expressed as

$$R_{p1} \approx \frac{L_p}{\omega_1\left(\frac{L_pC_1}{Q_p}+\frac{L_sC_2}{Q_s}\right)} \overset{Q_p=Q_s=Q_0}{\Longrightarrow} R_{p1} \approx L_p\omega_1 Q_0 \tag{2.9}$$

On the other hand, it can be shown that the third-order terms of the numerator and the denominator are dominant in (2.4) at $\omega_2 = 3\omega_1$. It follows that

$$R_{p2} \approx \frac{(1-k_m^2)}{C_1\omega_2\left(\frac{1}{Q_p}+\frac{1}{Q_s}\right)} \overset{Q_p=Q_s=Q_0}{\Longrightarrow} R_{p2} \approx \frac{Q_0\,(1-k_m^2)}{2\;C_1\;\omega_2} \tag{2.10}$$

R_{p2} is a strong function of the coupling factor of the transformer and thus the resulting leakage inductance. Weaker magnetic coupling will result in higher impedance magnitude at ω_2 and, consequently, the second resonance needs a lower transconductance gain to excite. It could even become a dominant pole and the circuit would oscillate at ω_2 instead of ω_1. This phenomenon has been used to extend the oscillator tuning range in [34], [36] and [37]. As explained before, $\mathrm{R}_{p2}/\mathrm{R}_{p1}$ controls the amount of the 3rd harmonic component of the oscillation voltage. The impedance magnitude ratio is equal to

$$\frac{R_{p2}}{R_{p1}} \approx \frac{(1-k_m^2)\,(1+X)}{6} \tag{2.11}$$

Hence, the smaller X-factor results in lower tank equivalent resistance at $\omega_2 = 3\omega_1$. Thus, the tank filters out more of the 3rd harmonic of the drain current and the oscillation voltage becomes more sinusoidal. Figure 2.8(a) illustrates Momentum simulation results of Z_{in} of the transformer-based tank versus frequency for both X-factors that satisfy the resonant frequency ratio of 3. The larger X-factor offers significantly higher tank impedance at ω_2, which is entirely in agreement with the theoretical analysis.

The X-factor is defined as a product of the transformer inductance ratio $\mathrm{L}_s/\mathrm{L}_p$ and tuning capacitance ratio $\mathrm{C}_2/\mathrm{C}_1$. This leads to a question of how best to divide X-factor between the inductance and capacitance ratios. In general, larger $\mathrm{L}_s/\mathrm{L}_p$ results in higher inter-winding voltage gain, which translates to sharper transition at zero-crossings and larger oscillation amplitude at the secondary winding. Both of these effects have a direct consequence on the phase noise improvement. However, the transformer Q-factor drops by increasing the turns ratio. In addition, very large oscillation voltage swing brings up reliability issues due to the gate-oxide breakdown. It turns out that the turns ratio of 2 can satisfy the aforementioned constraints altogether.

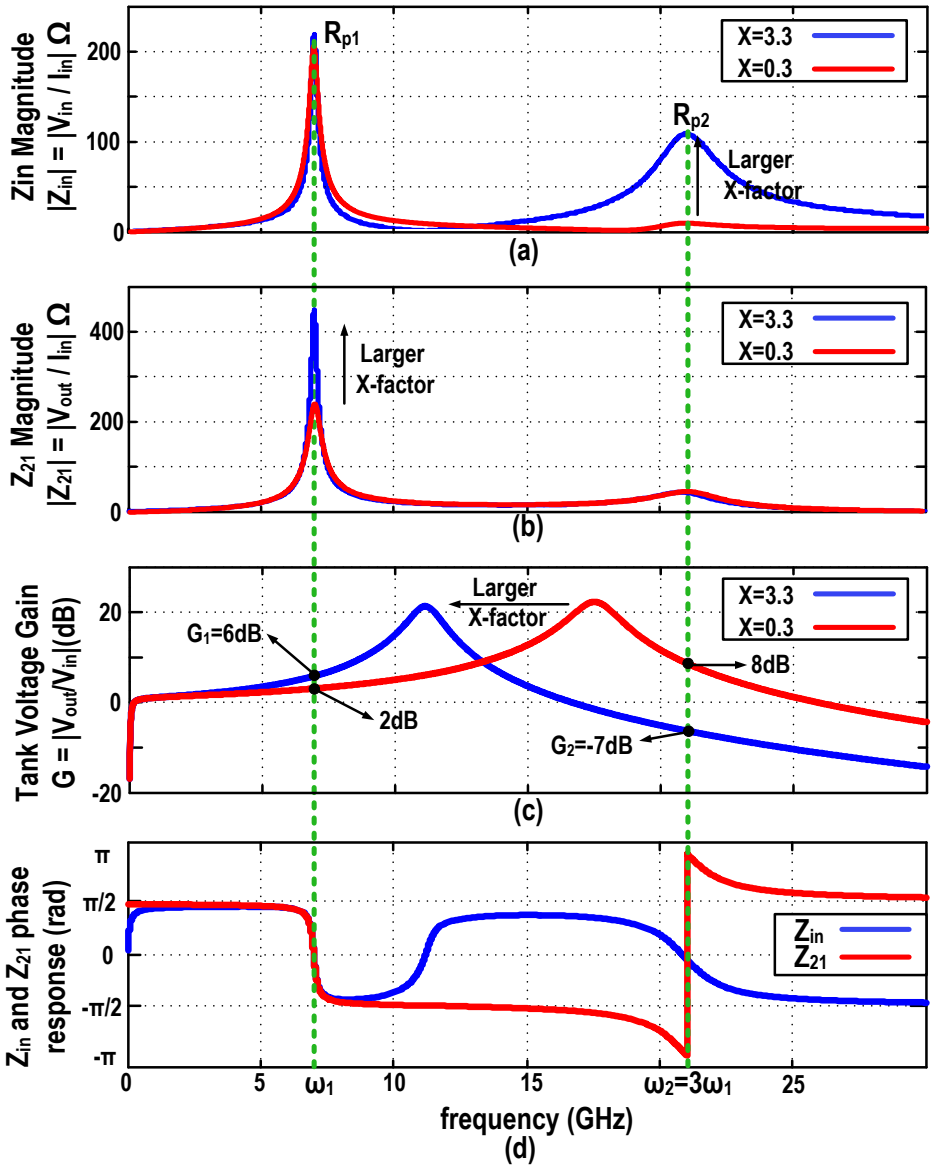


Figure 2.8: The transformer-based tank characteristics: (a) the input impedance, Z_{in} magnitude; (b) the trans-impedance, Z_{21} magnitude; (C) transformer's secondary to primary voltage gain; (d) the phase of Z_{in} and Z_{21} (Momentum simulation).

2.2.3 Voltage Gain of the Tank

The transformer-based resonator, whose schematic was shown in Fig. 2.6, offers a filtering function on the signal path from the primary to the secondary windings. The tank voltage gain is derived as

$$G(s) = \frac{V_{out}}{V_{in}} = \frac{Ms}{s^3\left(L_pL_sC_2\left(1-k_m^2\right)\right) + s^2\left(C_2\left(L_sr_p + L_pr_s\right)\right) + s\left(L_p + r_sr_pC_2\right) + r_p} \tag{2.12}$$

Bode diagram of the tank voltage gain transfer function is shown in Fig. 2.9. The tank exhibits a 20 dB/dec attenuation for frequencies lower than the first pole and offers a constant voltage gain at frequencies between the first pole and the complex conjugate pole pair at ω_p.

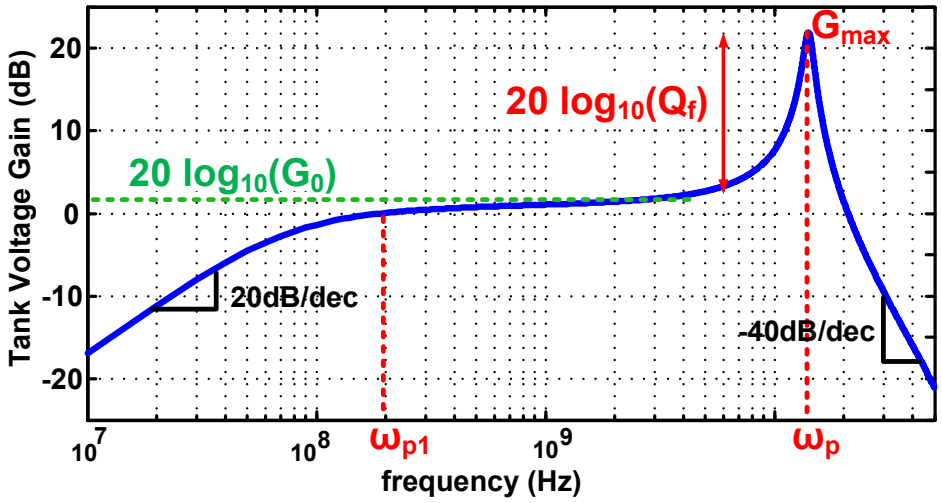


Figure 2.9: Typical secondary-to-primary winding voltage gain of the transformer-based resonator versus frequency.

The gain plot reveals an interesting peak at frequencies around ω_p, beyond which the filter gain drops at the -40 dB/dec slope. The low frequency pole is estimated by

$$\omega_{p1} = \frac{r_p}{L_p} \tag{2.13}$$

By substituting $r_p = L_p\omega/Q_p$, $r_s = L_s\omega/Q_s$ and assuming $Q_p \cdot Q_s \gg 1$, the tank gain transfer function can be simplified to the following equation for the frequencies beyond ω_{p1}.

$$G(s) = \frac{\frac{M}{L_p}}{s^2\left(L_sC_2\left(1-k_m^2\right)\right) + s\left(L_sC_2\omega\left(\frac{1}{Q_p}+\frac{1}{Q_s}\right)\right)+1} \tag{2.14}$$

The main characteristics of the tank voltage gain can be specified by considering it as a biquad filter.

$$G(s) = \frac{G_0}{\left(\frac{s}{\omega_p}\right)^2 + \left(\frac{s}{\omega_p Q_f}\right)+1} \tag{2.15}$$

where,

$$G_0 = k_m n \tag{2.16}$$

The peak frequency is estimated by

$$\omega_p = \sqrt{\frac{1}{L_sC_2\left(1-k_m^2\right)}} \tag{2.17}$$

Q_f represents the amount of gain jump around ω_p and expressed by

$$Q_f = \frac{\left(1-k_m^2\right)}{\frac{1}{Q_p}+\frac{1}{Q_s}} \tag{2.18}$$

Table 2.1: Normalized zero-crossing slope of the proposed oscillator.

	Normalized zero-crossing slope
Traditional LC	1
Proposed tank (primary)	$1+3\zeta = 1+3\cdot1/6 = 1.5$
Proposed tank (secondary)	$G_1\text{-}3G_2\zeta = 2.1 - 3\cdot0.4\cdot1/6 = 1.9$

Hence, the maximum voltage gain is calculated by

$$G_{max} = k_m n \times \frac{(1-k_m^2)}{\frac{1}{Q_p}+\frac{1}{Q_s}} \tag{2.19}$$

Eqs. (2.19) and Fig. 2.9 demonstrate that the transformer-based resonator can offer the voltage gain above $k_m n$ at the frequencies near ω_p for $k_m < 1$ and the peak magnitude is increased by improving Q-factor of the transformer individual inductors. Consequently, ω_1 should be close to ω_p to have higher passive gain at the fundamental frequency and more attenuation at its harmonic components. Eqs. (2.6) and (2.17) indicate that ω_p is always located at frequencies above ω_1 and the frequency gap between them decreases with greater X-factor. Figure 2.8(c) illustrates the voltage gain of the transformer-based tank for two different X-factors that exhibit the same resonant frequencies. The transformer peak gain happens at much higher frequencies for the smaller X-factor and, therefore, the gain is limited to only $k_m n$ (2 dB in this case) at ω_1. However, X-factor is around 3 for the proposed oscillator and, as a consequence, ω_p moves lower and much closer to ω_1. Now, the tank offers higher voltage gain (G_1=6 dB in this case) at the main resonance and more attenuation (G_2=-7 dB) at ω_2. This former translates to larger oscillation voltage swing and thus better phase noise.

As can be seen in Fig. 2.8(d), the input impedance Z_{in} phase is zero at the first and second resonant frequencies. Hence, any injected 3rd harmonic current has a constructive effect resulting in sharper zero-crossings and flat peak for the transformer's primary winding voltage. However, the tank trans-impedance, Z_{21} phase shows a 180 degree phase difference at ω_1 and $\omega_2 = 3\omega_1$. Consequently, the 3rd harmonic current injection at the primary windings leads to a slower zero-crossings slope at the transformer's secondary, which has an adverse outcome on the phase noise performance of the oscillator. Figure 2.8(a-c) illustrates that the proposed transformer-based resonator effectively filters out the 3rd harmonic component of the drain current at the secondary winding in order to minimize these side effects and zero-crossings are sharpened by tank's voltage gain (G_1) at ω_1. Table 2.1 shows that the zero-crossings slope of the proposed oscillator at both transformer's windings are improved compared to the traditional oscillator for the same V_{DD}, which is translated to shorter commutating time and lower active device noise factor.

2.2.4 Proposed Class-F Oscillator

The desired tank impedance, inductance and capacitance ratios were determined above to enforce the pseudo-square-wave oscillation voltage around the tank. Now, two transistors should be customarily added to the transformer-based resonator to sustain the oscillation. There are two options, however, as shown in Fig. 2.10, for connecting the transformer to the active gm-devices. The first option is a transformer-coupled class-F oscillator in which the secondary

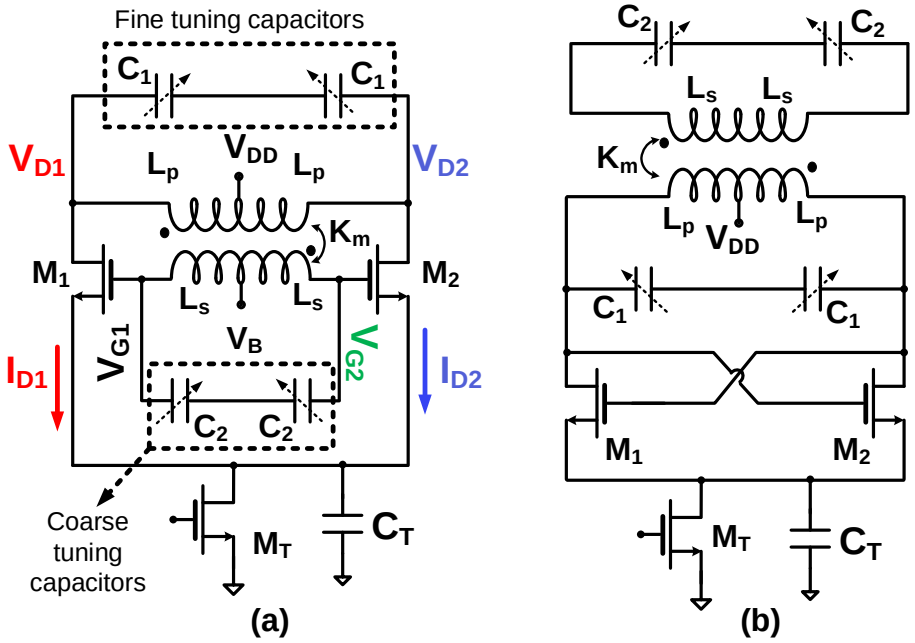


Figure 2.10: Two options of the transformer-based class-F oscillator: (a) transformer-coupled; and (b) cross-coupled. The first option was chosen as more advantageous in this work.

winding is connected to the gate of the gm-devices. The second option is a cross-coupled class-F oscillator with a floating secondary transformer winding, which only physically connects to tuning capacitors C_2. The oscillation voltage swing, the equivalent resonator quality factor and tank input impedance are the same for both options. However, the gm-device sustains larger voltage swing in the first option. Consequently, its commutation time is shorter and the active device noise factor is lower. In addition, the gm-device generates higher amount of the 3rd harmonic, which results in sharper pseudo-square oscillation voltage with lower ISF rms value. The second major difference is about the possibility of oscillation at ω_2 instead of ω_1. The root-locus plot in Fig. 2.11 illustrates the route of pole movements towards zeros for different values of the oscillator loop trans-conductance gain (G_m). As can be seen in Fig. 2.11(b), both resonant frequencies (ω_1, ω_2) can be excited simultaneously with a relatively high value of G_m for the cross-coupled class-F oscillator of Fig. 2.10(b). It can increase the likelihood of the undesired oscillation at ω_2. However, the transformer-coupled circuit of Fig. 2.10(a) demonstrates a different behavior. The lower frequency conjugate pole pair moves into the right-hand plane by increasing the absolute value of G_m, while the higher poles are pushed far away from imaginary axis (see Fig. 2.11(a)). This guarantees the oscillation can only happen at ω_1. Consequently, it becomes clear that the transformer-coupled oscillator is a better option due to its phase noise performance and the guaranty of operation at the right resonant frequency. Nevertheless, the gate parasitic capacitance appears at the drain through a scaling factor of n^2, which reduces its tuning range somewhat as compared to the cross-coupled candidate.

Figure 2.12 (a) illustrates the unconventional oscillation voltage waveforms of the proposed transformer-coupled class-F oscillator. As specified in Section 2.2.3, the 3rd harmonic component of the drain voltage attenuates at the gate and thus a sinusoidal wave is seen there. The gate-drain voltage swing goes as high as $2.7 \cdot V_{DD}$ due to the significant voltage gain of the tank. Hence, using thick oxide gm-devices is a constraint to satisfy the time-dependent dielectric breakdown (TDDB) issue for less than 0.01% failure rate during ten years of the oscillator

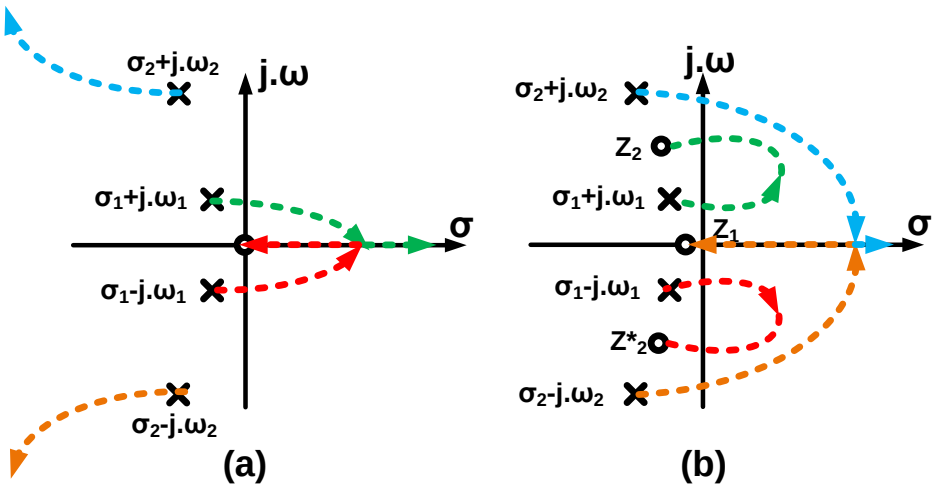


Figure 2.11: Root-locus plot of the transformer-based class-F oscillator: (a) transformer-coupled structure of Fig. 2.10(a); and (b) cross-coupled structure of Fig. 2.10(b).

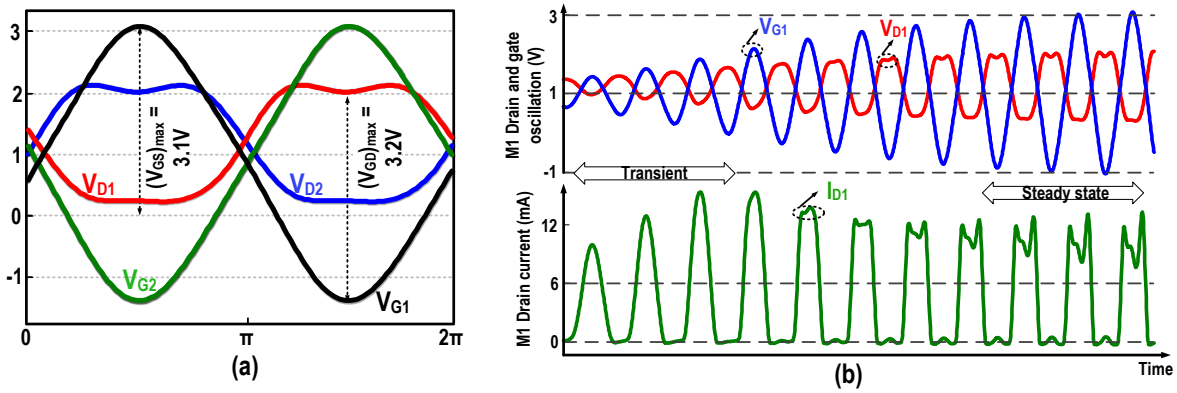


Figure 2.12: (a) Oscillation voltage waveforms and (b) transient response of the class-F oscillator.

operation [38], [39]. The costs are larger parasitics capacitance and slightly lower frequency tuning range.

The frequency tuning requires a bit different consideration in the class-F oscillator. Both C_1 and C_2 must, at a coarse level, be changed simultaneously to maintain L_sC_2/L_pC_1 ratio such that ω_2 aligns with $3\omega_1$.

Figure 2.12 (b) shows the transient response of the class-F oscillator. At power up, the oscillation voltage is very small and the drain current pulses have narrow and tall shape. Even though the tank has an additional impedance at $3\omega_1$, the 3rd harmonic component of the drain current is negligible and, consequently, the drain oscillation resembles a sinusoid. At steady state, gate oscillation voltage swing is large and the gm-device drain current is square-wave. Consequently, the combination of the tank input impedance with significant drain's 3rd harmonic component results in the pseudo-square wave for the drain oscillation voltage. This justifies its "class-F" designation.

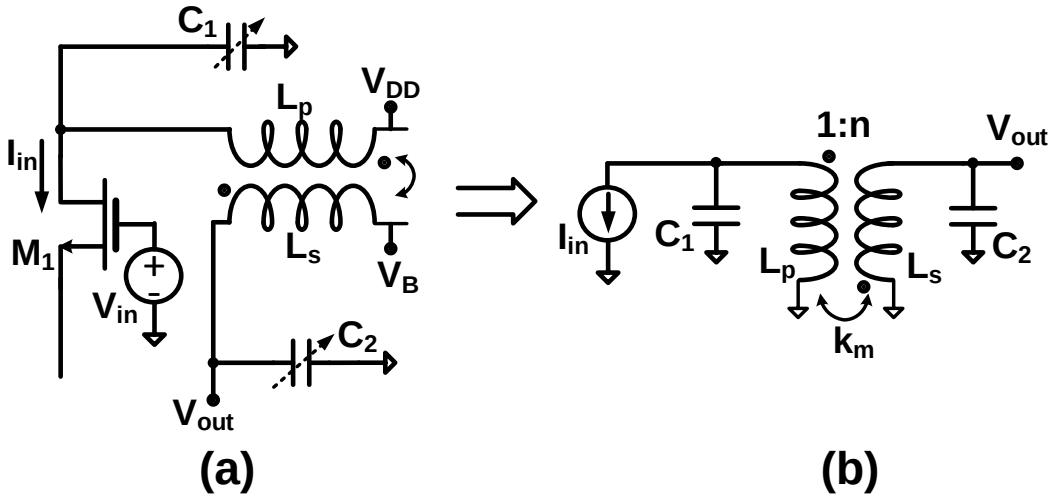


Figure 2.13: Open-loop circuit for unloaded Q-factor calculation (a); its equivalent circuit (b).

2.3 Class-F Phase Noise Performance

2.3.1 Quality Factor of Transformer-based Resonator

The Q-factor of the complex tank, which comprises two coupled resonators, does not appear to be as straightforward in intuitive understanding as the Q-factor of the individual physical inductors. It is, therefore, imperative to understand the relationship between the open-loop Q-factor *of the tank* versus the Q-factor of the inductive and capacitive parts of the resonator.

First, suppose the tuning capacitance losses are negligible. Consequently, the oscillator equivalent Q-factor just includes the tank's inductive part losses. The open-loop Q-factor of the oscillator is defined as $\omega_0/2 \cdot d\phi/d\omega$, where ω_0 is the resonant frequency and $d\phi/d\omega$ denotes the slope of the phase of the oscillator open-loop transfer function [40]. To determine the open-loop Q, we need to break the oscillator loop at the gate of M_1, as shown in Fig. 2.13. The open-loop transfer function is thus given by

$$H(s) = \frac{V_{out}}{I_{in}} = \frac{Ms}{As^4 + Bs^3 + Cs^2 + Ds + 1} \tag{2.20}$$

where, $A = L_pL_sC_1C_2\left(1 - k_m^2\right)$, $B = C_1C_2\left(L_sr_p + L_pr_s\right)$, $C = L_pC_1 + L_sC_2 + r_pr_sC_1C_2$, and, $D = r_pC_1 + r_sC_2$. After carrying out lengthy algebra and considering $(1 - C\omega^2 + A\omega^4 \approx 0)$ at the resonant frequencies,

$$Q_i = -\frac{\omega}{2}\frac{d\phi(\omega)}{d\omega} = \frac{(C\omega - 2A\omega^3)}{(D - B\omega^2)} \tag{2.21}$$

Substituting A, B, C and D into (2.21), then swapping r_p and r_s with $L_p\omega/Q_p$ and $L_s\omega/Q_s$, respectively, and assuming $Q_pQ_s \gg 1$, we obtain

$$Q_i = \frac{(L_pC_1 + L_sC_2) - 2\left(L_pL_sC_1C_2\left(1 - k_m^2\right)\right)\omega^2}{\left(\frac{L_pC_1}{Q_p} + \frac{L_sC_2}{Q_s}\right) - \left(C_1C_2L_sL_p\left(\frac{1}{Q_p} + \frac{1}{Q_s}\right)\right)\omega^2} \tag{2.22}$$

Substituting (2.5) as ω into the above equation and carrying out the mathematics, the tank's

inductive part Q-factor at the main resonance is

$$Q_i = \frac{(1 + X^2 + 2k_m X)}{\left(\frac{1}{Q_p} + \frac{X^2}{Q_s}\right)} \tag{2.23}$$

To help with an intuitive understanding, let us consider a boundary case. Suppose, that C_2 is negligible. Therefore, X-factor is zero and (2.23) predicts that the Q_i equals to Q_p. This is not surprising, because no energy would be stored at the transformer's secondary winding and its Q-factor would not have any contribution to the equivalent Q-factor of the tank. In addition, (2.23) predicts that the equivalent Q-factor of the tank's inductive part can exceed Q-factors of the individual inductors. To the authors' best knowledge, this is the first ever report of quantifying the equivalent Q-factor of the transformer-based resonator at its resonant frequency in a general case that clearly proves Q-factor enhancement over that of the transformer's individual inductors. The maximum tank's inductive part Q-factor is obtained at the following X-factor for a given k_m, Q_p and Q_s.

$$X_{Qmax} = \frac{Q_s}{Q_p} \tag{2.24}$$

For a typical case of $Q_s = Q_p = Q_0$, the maximum Q_i at ω_1 is calculated by

$$X_{Qi,max} = 1 \rightarrow Q_{i,max} = Q_0\,(1 + k_m) \tag{2.25}$$

The above equation indicates that the equivalent Q-factor of the inductive part of the transformer-based resonator can be enhanced by a factor of $1 + k_m$ at the optimum state. However, it does not necessarily mean the Q-factor of the transformer-based tank generally is superior to the simple LC resonator. The reason is that it is not possible to optimize the Q-factor of both windings of a 1:n transformer at a given frequency and one needs to use lower metal layers for the transformer cross connections, which results in more losses and lower Q-factor [41], [42]. For this prototype, the X-factor is around 3 with k_m=0.7 and the simulated Q_p and Q_s are 14 and 20 respectively. Based on (2.23), the equivalent Q-factor of the inductive part of the tank would be about 26, which is higher than that of the transformers' individual inductors. The Q-factor of the switched capacitance largely depends on the tuning range (TR) and operating frequency of the oscillator and is about 42 for the TR of 25% at 7 GHz resulting in an average Q-factor of 16 for the tank in this design.

2.3.2 Phase Noise Mechanism in Class-F Oscillator

According to the linear time-variant model [31], the phase noise of the oscillator at an offset frequency $\Delta\omega$ from its fundamental frequency is expressed as,

$$L(\Delta\omega) = 10\log_{10}\left(\frac{\sum_i N_{L,i}}{2\ q_{max}^2\,(\Delta\omega)^2}\right) \tag{2.26}$$

where, q_{max} is the maximum charge displacement across the tuning capacitor C, and $N_{L,i}$ is the effective noise produced by i^{th} device given by

$$N_{L,i} = \frac{1}{2\pi N^2}\int_0^{2\pi} \Gamma_i^2(t)\ \overline{i_{n,i}^2(t)}dt \tag{2.27}$$

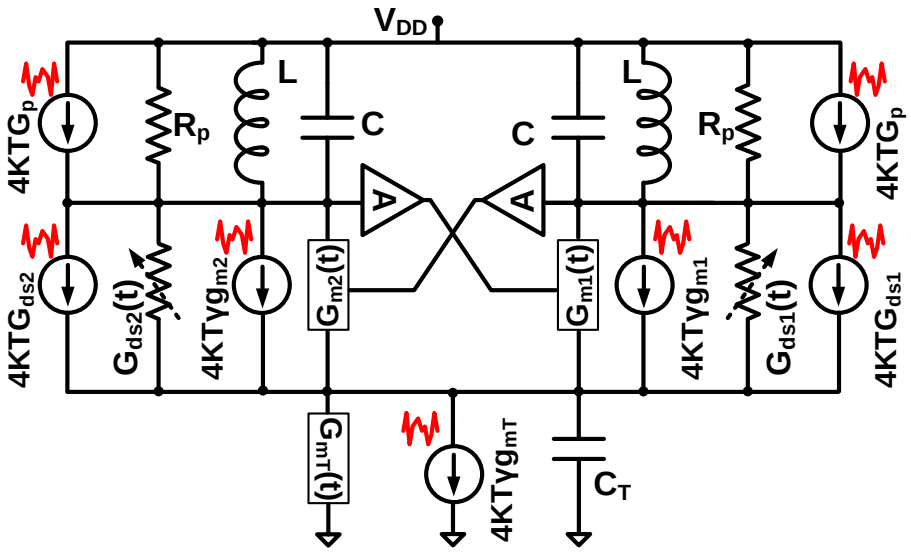


Figure 2.14: RF CMOS oscillator noise sources.

where $\overline{i^2_{n,i}(t)}$ is the white current noise power density of the ith noise source, Γ_i is its relevant ISF function from the corresponding i^{th} device noise, and N is the number of resonators in the oscillator. N is considered one for single-ended and two for differential oscillator topologies with a single LC tank [25].

Figure 2.14 illustrates the major noise sources of CMOS class-B, C and F oscillators. R_p and $G_{ds1,2}(t)$ represent the equivalent tank parallel resistance and channel conductance of the gm transistors, respectively. On the other hand, $G_{m1,2}$ and G_{mT} model the noise due to transconductance gain of active core and current source transistors, respectively. By substituting (2.27) into (2.26) and carrying out algebra, the phase noise equation is simplified to

$$L(\Delta\omega) = 10\log_{10}\left(\frac{K_B\ T\ R_p}{2\ Q_t^2\ V_p^2}\cdot F\cdot\left(\frac{\omega_0}{\Delta\omega}\right)^2\right) \tag{2.28}$$

where Q_t is the tank's equivalent quality factor and V_p is the maximum oscillation voltage amplitude, derived by

$$V_p = \begin{cases} \left(\frac{1}{3}+\zeta\right)\sqrt{(1+\frac{1}{3\zeta})}\cdot\alpha_I\cdot R_p\cdot I_B, & \frac{1}{9}\le\zeta\le 1 \\ (1-\zeta)\cdot\alpha_I\cdot R_p\cdot I_B, & 0\le\zeta\le\frac{1}{9} \end{cases} \tag{2.29}$$

where α_I is the current conversion efficiency of the oscillator, expressed as the ratio of the fundamental component of gm-devices drain current to dc current I_B of the oscillator. F in (2.28) is the effective noise factor of the oscillator, expressed by

$$F = \sum_i \frac{1}{2\pi}\int_0^{2\pi}\Gamma_i^2(t)\ \frac{\overline{i^2_{n,i}(t)}R_p}{4K_BT}dt \tag{2.30}$$

Suppose that C_T is large enough to filter out the thermal noise of the tail transistor. Consequently, F consists of the noise factor of the tank (F_{tank}), transistor channel conductance

(F_{GDS}) and gm of core devices (F_{GM}). The expressions of F_{tank} and F_{GDS} are,

$$F_{Tank} = \frac{1}{\pi}\int_0^{2\pi} \Gamma_{tank}^2(t)dt = 2\Gamma_{rms}^2 \approx \frac{1+9\zeta^2}{(1+3\zeta)^2} \tag{2.31}$$

$$F_{GDS} = \frac{1}{\pi}\int_0^{2\pi} \Gamma_{MOS}^2(t)G_{DS1}(t)R_P dt \approx 2\Gamma_{rms}^2 R_P \cdot G_{DS1EF} \tag{2.32}$$

where G_{DSEF1} is the effective drain-source conductance of one of the gm-devices expressed by

$$G_{DS1EF} = G_{DS1}[0] - G_{DS1}[2] \tag{2.33}$$

where G_{DS1}[k] describes the k_{th} Fourier coefficient of the instantaneous conductance, G_{ds1}(t) [43]. F_{GM} can be calculated by

$$F_{GM} = \frac{1}{\pi}\int_0^{2\pi} \Gamma_{MOS}^2(t)\gamma G_{m1}(t)R_P dt \approx 2\Gamma_{rms}^2 \cdot \gamma \cdot R_P \cdot G_{M1EF} \tag{2.34}$$

Now, the effective negative transconductance of the oscillator needs to overcome the tank and its own channel resistance losses and therefore the noise due to G_M also increases.

$$G_{M1EF} = \frac{1}{A}\left(\frac{1}{R_p} + G_{DS1EF}\right) \tag{2.35}$$

where A is the voltage gain of feedback path between the tank and MOS gate. By substituting (2.35) into (2.34)

$$F_{GM} = 2\ \Gamma_{rms}^2 \cdot \frac{\gamma}{A} \cdot (1 + R_P G_{DS1EF}) \tag{2.36}$$

Consequently, the effective noise factor of the oscillator is given by

$$F = 2\ \Gamma_{rms}^2 \cdot \left(1 + \frac{\gamma}{A}\right) \cdot (1 + R_P G_{DS1EF}) \tag{2.37}$$

This is a general result and applicable to the class-B, C and F. The oscillator FoM normalizes the phase noise performance to the oscillation frequency and power consumption, yielding

$$FoM = -10 \cdot log_{10}\left(\frac{10^3\, K_B\, T}{2\, Q_t^2\, \alpha_I\, \alpha_V} \cdot 2\,\Gamma_{rms}^2 \cdot \left(1 + \frac{\gamma}{A}\right) \cdot (1 + R_P G_{DS1EF})\right) \tag{2.38}$$

where α_V is the voltage efficiency, defined as V_P/V_{DD}. To get a better insight, the circuit-to-phase noise mechanism, relative phase noise and power efficiency of different oscillator classes are also investigated and compared together in this section. Figure 2.15 (a-f) shows the oscillation voltage and drain current for the traditional, class-C and the proposed class-F oscillators for the same V_{DD} (i.e., 1.2 V), tank Q-factor (i.e., 15) and R_P (i.e., 220 Ω).

The α_V must be around 0.8 for the class B and F oscillators due to the voltage drop V_{dsat} across tail transistor needed to keep it in saturation. The combination of the tail capacitance and entering the gm-devices into the linear region reduces α_I of class-B from the theoretical value of $2/\pi$ to around 0.55. Fortunately, α_I is maintained around $2/\pi$ for class-F due to the pseudo-square drain voltage and larger gate amplitude. The class-C oscillator with a dynamic bias of the active transistor offers significant improvements over the traditional class-C, and

Table 2.2: Comparison of different oscillator's classes for the same V_{DD} (1.2 V), tank Q-factor (15), R_P (i.e. 220 Ω), and carrier frequency (7 GHz) at 3 MHz offset frequency.

	Theoretical expression	**Class-B**	**Class-C**	**Class-F**
F_{RP}	$2\Gamma_{rms}^2$	1 (average)	1 (average)	0.7 (best)
F_{GDS}	$2\Gamma_{rms}^2 R_P G_{DSEF1}$	0.56 (worst)	0.07 (best)	0.27 (average)
F_{GM}	$2\Gamma_{rms}^2 \frac{\gamma}{A}(1 + R_P G_{DS1EF})$	1.56γ (worst)	1.07γ (average)	0.7γ (best)
F	$2\,\Gamma_{rms}^2 \left(1 + \frac{\gamma}{A}\right)(1 + R_P G_{DS1EF})$	5.5 dB (worst)	3.9 dB (average)	2.8 dB (best)
α_I	I_{H1}/I_B	0.55 (worst)	0.9 (best)	0.63 (average)
α_V	V_p/V_{DD}	0.8 (best)	0.7 (average)	0.8 (best)
$PN\,(dBc/Hz)$	$10\log_{10}\left(\frac{K_B\,T\,R_p}{2\,Q_0^2\,V_p^2} \cdot F \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2\right)$	-133.5 (worst)	-134 (average)	-136 (best)
$FoM\,(dB)$	$-10log_{10}\left(\frac{1000\,K_B T}{2Q_0^2\alpha_I\alpha_V}F\right)$	191.2 (worst)	194.5 (best)	194.2 (≈ best)

maximizes the oscillation amplitude without compromising the robustness of the oscillator start-up [44]. Nevertheless, its α_V is around 0.7 to avoid gm-devices entering the triode region. Class-C drain current composed of tall and narrow pulses results in α_I equal to 0.9 (ideally 1).

Obtaining the ISF function is the first step in the calculation of the oscillator's effective noise factor. The class-B/C ISF function is a sinusoid in quadrature with the tank voltage [25], [45]. However, finding the exact equation of class-F ISF is not possible, hence, we had to resort to painstakingly long Cadence^{TM} simulations to obtain the ISF curves. Figure 2.15(g) shows the simulated class-F tank equivalent ISF function, which is smaller than the other classes for almost the entire oscillation period.

Figure 2.15(h) demonstrates the tank effective noise factor along the oscillation period for different oscillator classes. The F_{RP} is 32% lower for the proposed class-F due to its special ISF properties. The gm-device M_1 channel conductance across the oscillation period is shown in Fig. 2.15(i). As expected, G_{DS1}(t) of class-F exhibits the largest peak due to high oscillation swing at the gate and, consequently, injects more noise than other structures to the tank. On the other hand, class-C operates only in the saturation region and its effective transistor conductance is negligible. Figure 2.15(j) stronger emphasizes that the gm-device resistive channel noise could even be 7 times higher than the tank noise when the M_1 operates in the linear region. To get a better insight, one need to simultaneously focus on Figs. 2.15(j) and (k). Although the class-F G_{DS1} generates lots of noise in the second half of the period, its relevant ISF value is very small there. Hence, the excessive transistor channel noise cannot convert to the phase noise and as shown in Fig. 2.15(l), the F_{GDS} of class-F is one half of the traditional oscillator. The transconductance loop gain of the different oscillator structures are shown in Fig. 2.15(m). Class-F needs to exhibit the highest effective transconductance loop gain to compensate its larger gm-devices channel resistance losses. However, half of the required loop gain is covered by the transformer-based tank voltage gain. Figure. 2.15(o) demonstrates the active device effective noise factor along the oscillation period. Class-F offers the lowest F_{GM} due to its special ISF

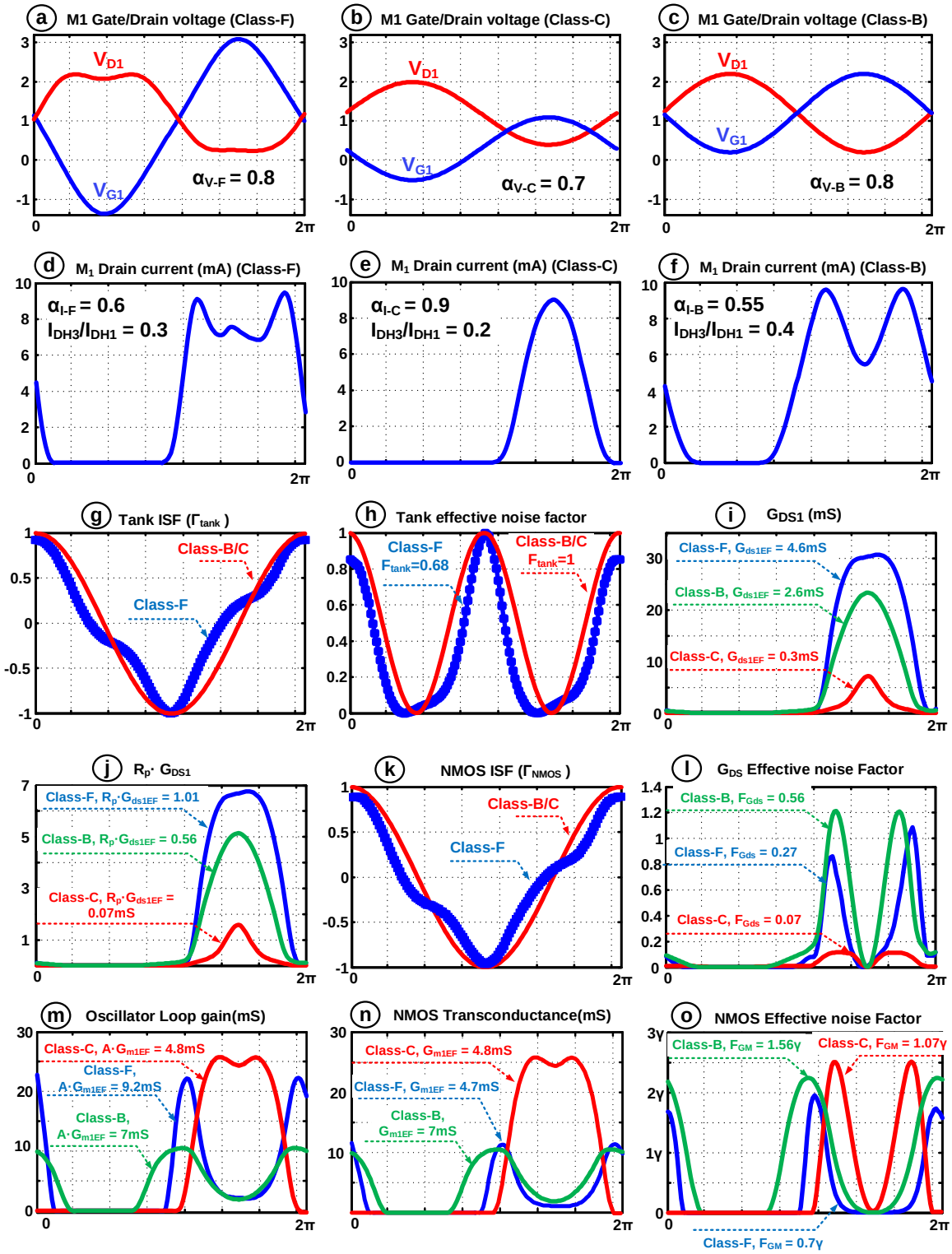


Figure 2.15: Mechanisms of circuit noise to phase noise conversion in different classes of RF CMOS oscillator.

nature and the passive voltage gain between the tank and gate of the gm-transistors.

Table 2.2 summarizes the performance of different oscillator classes of this example. It can be concluded that class-F oscillator achieves the lowest circuit-to-phase noise conversion along the best phase noise performance with almost the same power efficiency as the class-C oscillator.

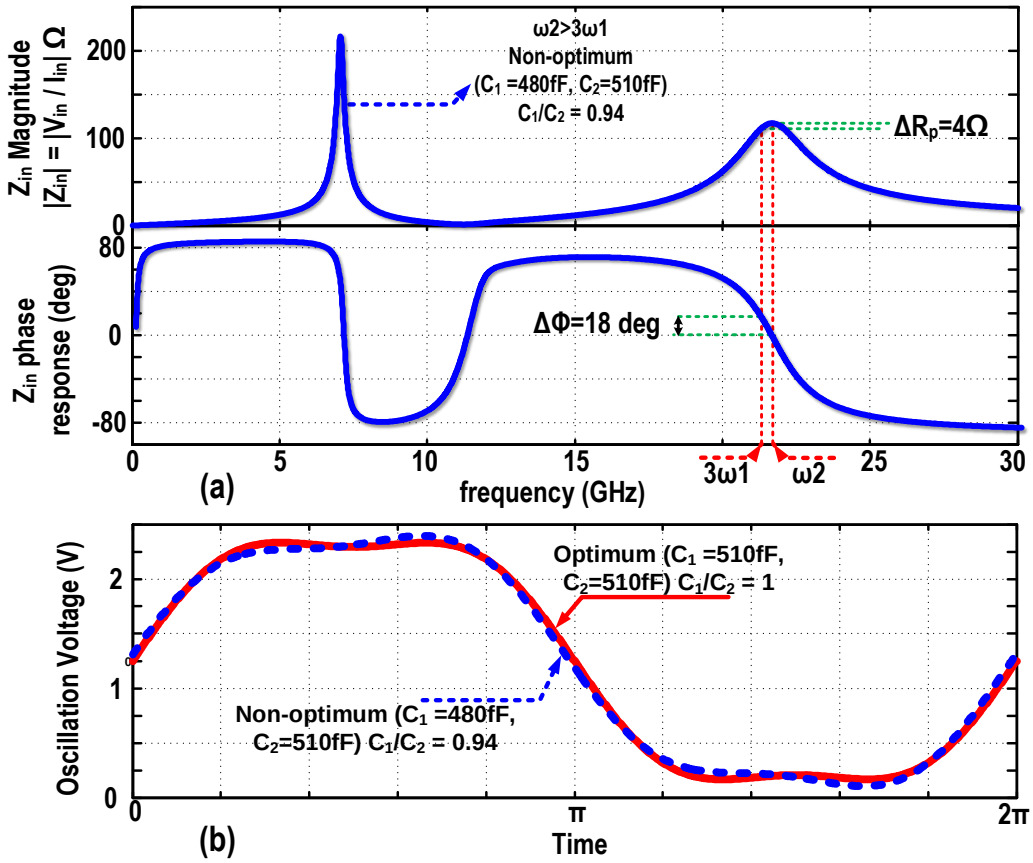


Figure 2.16: Sensitivity of class-F oscillator to the position of the second resonant frequency: tank's input impedance magnitude and phase (top), oscillation waveform (bottom).

The use of transformer in the Class-F configuration offers an additional reduction of the $1/f^3$ phase noise corner. The transformer inherently rejects the common-mode signals. Hence, the 1/f noise of the tail current source can appear at the transformer's primary but it will be effectively filtered out on the path to the secondary winding. Consequently, the AM-to-PM conversion at the C_2 switched capacitors is entirely avoided.

Another 1/f phase noise conversion mechanism is called Groszkowski effect [46]. Groszkowski demonstrated that the presence of harmonic components of the active device current in the tank can cause a frequency drift from the tank resonance [47]. The harmonic components of the drain current mainly take the capacitance path due its lower impedance. As a consequence, the oscillation frequency must shift down to satisfy the resonance condition. Consequently, any variation in harmonic-to-fundamental drain current value due to the 1/f noise of M_T can modulate Groszkowski's frequency shift and show itself as a low frequency noise in the phase noise sidebands [47]. The class-F tank has fortunately two impedance peaks at the fundamental oscillation frequency and its 3rd harmonic. Hence, the 3rd harmonic component (i.e., the strongest among the higher harmonics) of drain current flows to the resistive part of the tank and does not contribute to Groszkowski's frequency shift. It effectively reduces the 1/f noise upconversion to the $1/f^3$ phase noise due to Groszkowski phenomenon.

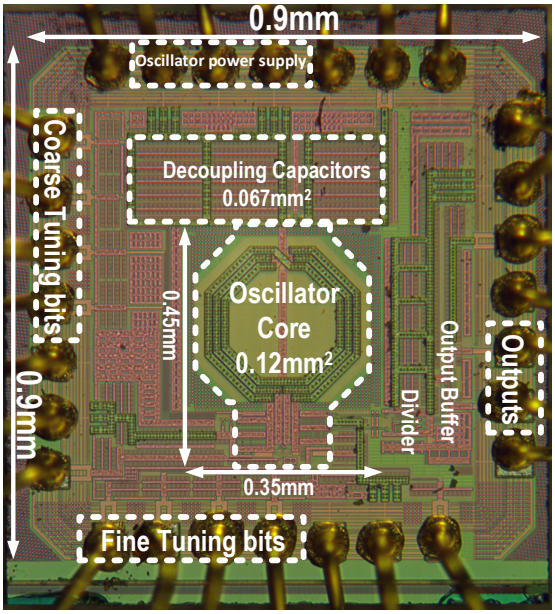


Figure 2.17: Die photograph of class-F oscillator.

2.3.3 Class-F Operation Robustness

Figure 2.16(a) illustrates the tank input impedance magnitude and phase for the imperfect position of the second resonance frequency ω_2. A 6% mismatch is applied to the C_2/C_1 ratio, which shifts ω_2 to frequencies higher than $3\omega_1$. Hence, the 3rd harmonic of the drain current is multiplied by a lower impedance magnitude with a phase shift resulting in a distorted pseudo-square oscillation waveform as shown in Fig. 2.16(b). Intuitively, if the Q-factor at ω_2 was smaller, the tank impedance bandwidth around it would be wider. Therefore, the tank input impedance phase shift and magnitude reduction would be less for a given ω_2 drift from $3\omega_1$. As a consequence, the oscillator would be less sensitive to the position of ω_2 and thus the tuning capacitance ratio. Based on the open-loop Q-factor analysis, substituting $\omega^2 \approx 9/(L_sC_2 + L_pC_1)$ into (2.22), the Q_i is obtained as $0.3Q_0$ at ω_2. Fortunately enough, the proposed tank configuration automatically reduces the equivalent tank Q-factor at ω_2 to 30% of the main resonance Q-factor. This is completely in line with the desire to reduce the sensitivity to the position of ω_2 in class-F. Consequently, a realistic example ± 30 fF variation in C_1 from its optimum point has absolutely no major side effects on the oscillator waveform and thus its phase noise performance, as apparent from Fig. 2.16. It is strongly emphasized that the circuit oscillates based on ω_1 resonance and low Q-factor at ω_2 has no adverse consequence on the oscillator phase noise performance.

2.4 Experimental Results

2.4.1 Implementation Details

The class-F oscillator, whose schematic was shown in Fig. 2.10(a), has been realized in TSMC 1P7M 65-nm CMOS technology with Alucap layer. The differential transistors are thick-oxide devices of 12(4-μm/0.28-μm) dimension to withstand large gate voltage swing. However, the tail

current source M_T is implemented as a thin-oxide 500-μm/0.24-μm device biased in saturation. The large channel length is selected to minimize its 1/f noise. Its large drain-bulk and drain-gate parasitic capacitances combined with C_T = 2 pF MOM capacitor shunt the M_T thermal noise to ground. The step-up 1:2 transformer is realized by stacking the 1.45 μm Alucap layer on top of the 3.4 μm thick top (M7 layer) copper metal. Its primary and secondary differential self-inductances are about 500 pH and 1500 pH, respectively, with the magnetic coupling factor of 0.73. The transformer was designed with a goal of maximizing Q-factor of the secondary winding, Q_s, at the desired operating frequency. Based on (2.23), Q_s is the dominant factor in the tank equivalent Q-factor expression, provided $(L_sC_2)/(L_pC_1)$ is larger than one, which is valid for this oscillator prototype. In addition, the oscillation voltage is sinusoidal across the secondary winding. It means the oscillator phase noise is more sensitive to the circuit noise at the secondary winding compared to the primary side with the pseudo-square waveform. Four switched MOM capacitors $B_{C0} - B_{C3}$ placed across the secondary winding realize coarse tuning bits, while the fine control bits $B_{F0} - B_{F3}$ with LSB size of 20 fF adjust the position of ω_2 near $3\omega_1$. The center tap of the secondary winding is connected to the bias voltage, which is fixed around 1 V to guarantee safe oscillator start-up in all process corners. A resistive shunt buffer interfaces the oscillator output to the dynamic divider [4]. A differential output buffer drives a 50-Ω load. The separation of the oscillator core and divider/output buffer voltage supplies and grounds serves to maximize the isolation between the circuit blocks. The die micrograph is shown in Fig. 2.17. The oscillator core die area is 0.12 mm^2.

2.4.2 Measurement Results

The measured phase noise at 3.7 GHz (after the on-chip ÷2 divider) at 1.25 V and 12 mA current consumption is shown in Fig. 2.18. The phase noise of -142.2 dBc/Hz at 3 MHz offset lies on the 20 dB/dec slope, which extrapolates to -158.7 dBc/Hz at 20 MHz offset (-170.8 dBc/Hz when normalized to 915 MHz) and meets the GSM TX mobile station (MS) specification with a very wide 8 dB margin. The oscillation purity of the class-F oscillator is good enough to compare its performance to cellular basestation (BTS) phase noise requirements. The GSM/DCS "Micro" BTS phase noise requirements are easily met. However, the phase noise would be off by 3 dB for the toughest DCS-1800 "Normal" BTS specification at 800 kHz offset frequency [48]. The 1/f^3 phase noise corner is around 700 kHz at the highest frequency due to the asymmetric layout of the oscillator differential nodes further magnified by the dominance of parasitics in the equivalent tank capacitance. The 1/f^3 phase noise corner moves to around 300 kHz at the middle and low part of the tuning range. The noise floor is -160 dBc/Hz and dominated by thermal noise from the divider and buffers. The oscillator has a 25% tuning range, from 5.9 to 7.6 GHz. Figure 2.19 (a) shows the average phase noise performance of 4 samples at 3 MHz offset frequency across the tuning range (after the divider), together with the corresponding FoM. The average FoM is as high as 192 dBc/Hz and varies about 2 dB across the tuning range. The divided output frequency versus supply is shown in Fig. 2.19 (b) and reveals very low frequency pushing of 50 MHz/V and 18 MHz/V at the highest and lowest frequencies, respectively.

The phase noise of the class-F oscillator was measured at the fixed frequency of 3.5 GHz for two configurations. In the first configuration, the C_2/C_1 ratio was set to one to align the second resonant frequency ω_2 exactly at the 3rd harmonic of the fundamental frequency ω_1. This is the optimum configuration of the class-F oscillator (Fig. 2.20, top). In the second configuration,

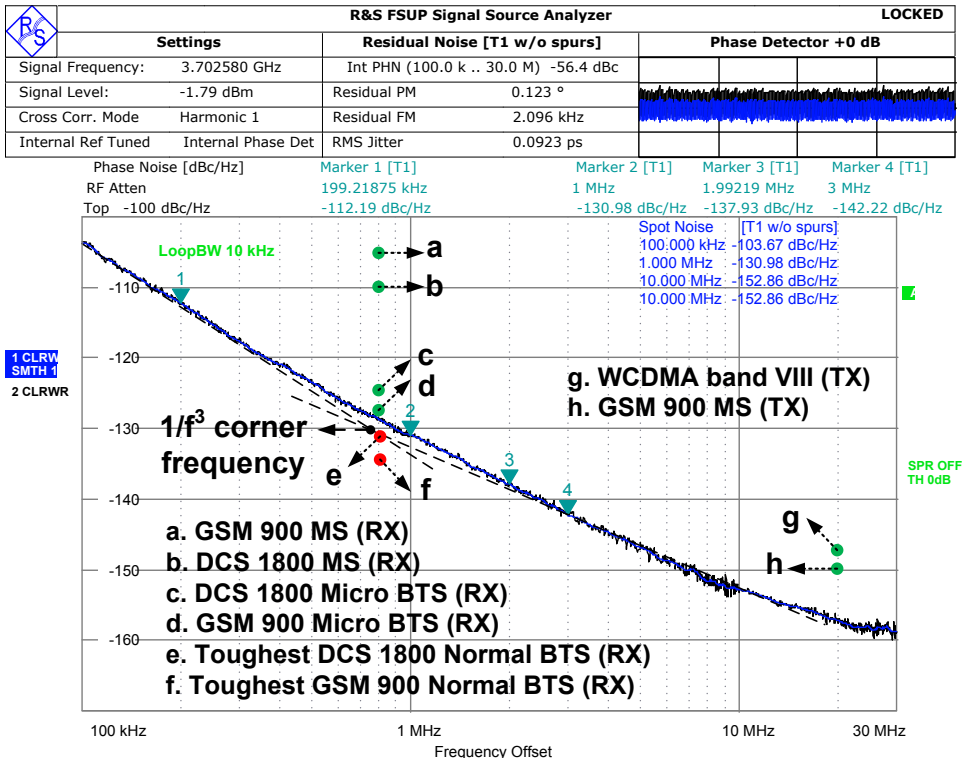


Figure 2.18: Measured phase noise at 3.7 GHz and power dissipation of 15 mW. Specifications (MS: mobile station, BTS: basestation) are normalized to the carrier frequency.

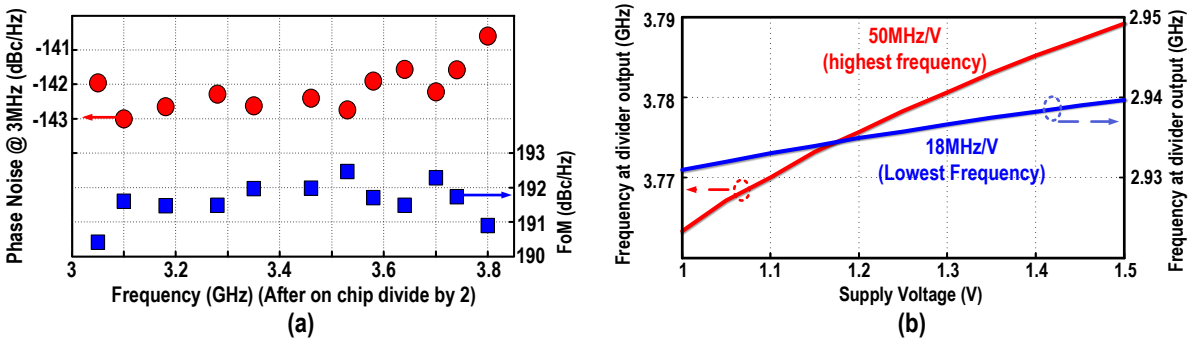


Figure 2.19: (a) Phase noise and figure-of-merit (FoM) at 3 MHz offset versus carrier frequency and (b) frequency pushing due to supply voltage variation.

the oscillation frequency is kept fixed but an unrealistically high 40% mismatch was applied to the C_2/C_1 ratio, which lowers ω_2, in order to see its effects on the phase noise performance (see Fig. 2.20, bottom). As a consequence, the 3rd harmonic component of the drain oscillation voltage is reduced and a phase shift can be seen between voltage waveform components at $3\omega_1$ and ω_1. Therefore, its ISF rms value is worse than optimum, thus causing a 2 dB phase noise degradation in the 20 dB/dec region. In addition, the voltage waveform demonstrates more asymmetry in the rise and fall times, which translates to the non-zero ISF dc value and increases the upconversion factor of the 1/f noise corner of gm-devices. As can be seen in Fig. 2.20, the $1/f^3$ phase noise corner is increased by 25% or 100 kHz in the non-optimum case. It results in a 3 dB phase noise penalty in the flicker noise region.

Table 2.3 summarizes performance of the proposed class-F oscillator and compares it with

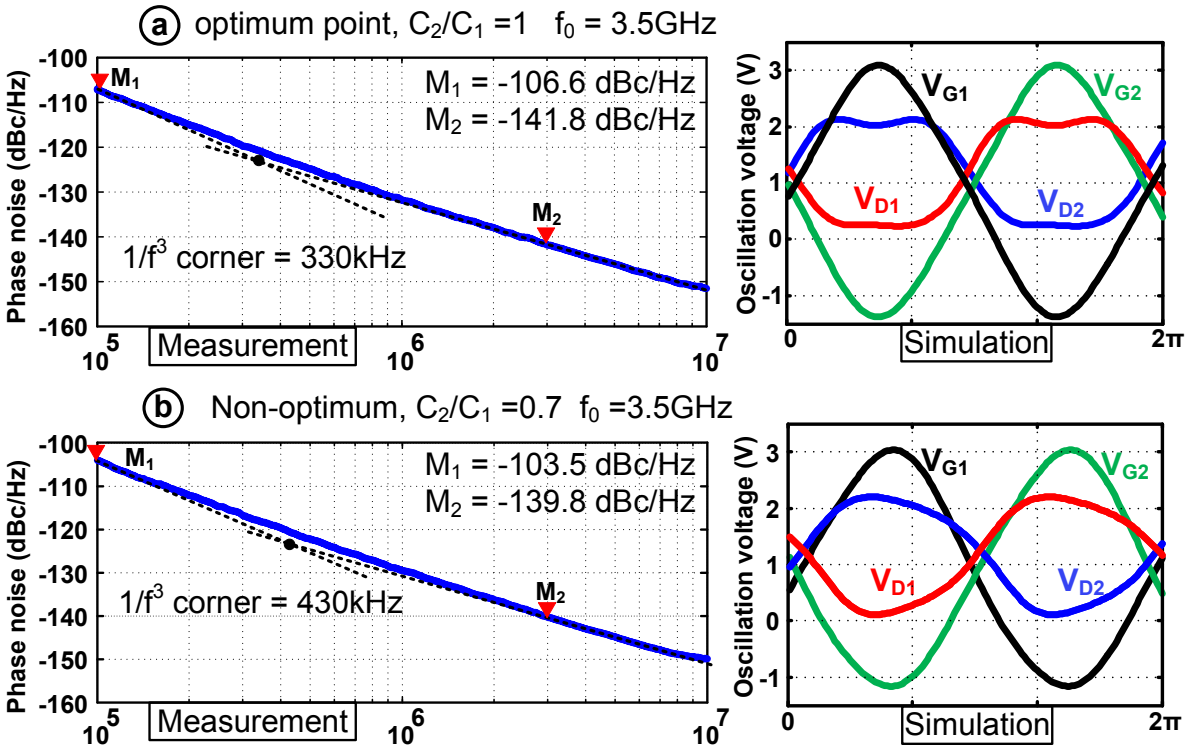


Figure 2.20: Measured phase noise at 3.5 GHz and simulated oscillation waveforms: (a) optimum case; (b) exaggerated non-optimum case.

the relevant state-of-the-art. The class-F demonstrates a 5 dB phase noise and 7 dB FoM improvements over the traditional commercial oscillator [4] with almost the same tuning range. For the same phase noise performance range (-154 to -155 dBc/Hz) at 3 MHz offset for the normalized 915 MHz carrier, the class-F oscillator consumes only 15 mW, which is much lower than with Colpitts [49], class B/C [28], and clip-and-restore [48] topologies. Only the noise-filtering-technique oscillator [26] offers a better power efficiency but at the cost of an extra dedicated inductor and thus larger die. Also, it uses a 2.5V supply thus making it unrealistic in today's scaled CMOS. From the FoM point of view, the class-C oscillator [27] exhibits a better performance than the class-F oscillator. However, the voltage swing constraint in class-C limits its phase noise performance. As can be seen, the class-F demonstrates more than 6 dB better phase noise with almost the same supply voltage. Consequently, the class-F oscillator has reached the best phase noise performance with the highest power efficiency at low voltage supply without the die area penalty of the noise-filtering technique or voltage swing constraint of the class-C VCOs.

2.5 Conclusion

We have proposed a new structure for LC-tank oscillators that introduces an impedance peak around the third harmonic of the oscillating waveform such that the third harmonic of the active device current converts into voltage and, together with the fundamental component, creates a pseudo-square oscillation voltage. The additional peak of the tank impedance is realized with a transformer-based resonator. As a result, the oscillator impulse sensitivity

Table 2.3: Comparison of state-of-the-art oscillators.

	This work	**[27]**	**[26]**	**[48]**	**[28]**	**[49]**	**[4]**	**[37]**
Technology	CMOS 65nm	CMOS 130nm	CMOS 350μm	CMOS 65nm	CMOS 55nm	BiCMOS 0.130μm	CMOS 90nm	CMOS 65nm
Supply voltage (V)	1.25	1	2.5	1.2	1.5	3.3	1.4	0.6
Frequency (GHz)	3.7[1]	5.2	1.2	3.92[1]	3.35[1]	1.56	0.915	3.7
Tuning range (%)	25	14	18	10.2	31.4	9.6	24.3	77
PN at 3 MHz (dBc/Hz)	-142.2	-141.2	-152	-141.7	-142	-150.4	-149	-137.1
Norm. PN[2] (dBc/Hz)	-154.3	-147.5	-154.8	-154.4	-153.3	-155	-149	-149.21
I_{DC} (mA)	12	1.4	3.74	18	12	88	18	17.5
Power consumption (mW)	15	1.4	9.25	25.2	27	290	25.2	10.5
FoM[3] (dB)	192.2	195	195	189.9	189	180	184.6	188.7
FoM$_T$[4] (dB)	200.2	198.4	200.7	190	199	179.7	192.3	206.5
Inductor/transformer No.	1	1	2	2	1	1	1	1
Area (mm^2)	0.14	0.11	N/A	0.19	0.196	N/A	N/A	0.294
Oscillator structure	Class F	Class C	Noise Filtering	Clip-and-Restore	Class B/C	Colpitts	Tradi tional	Dual mode

[1] after on-chip ÷2 divider,
[2] phase noise at 3 MHz offset frequency normalized to 915 MHz carrier,
[3] $FOM = |PN|+20\ log_{10}((f_0/\Delta f))$ - 10 $log_{10}(P_{DC}/1\text{mW})$,
[4] $FOM_T = |PN|+20\ log_{10}((f_0/\Delta f)\ (TR/10))$ - 10 $log_{10}(P_{DC}/1\text{mW})$

function reduces thus lowering the conversion sensitivity of phase noise to various noise sources, whose mechanisms are analyzed in depth. Chief of these mechanisms arises when the active gm-devices periodically enter the triode region during which the LC-tank is heavily loaded while its equivalent quality factor is significantly reduced. The voltage gain, relative pole position, impedance magnitude and equivalent quality factor of the transformer-based resonator are quantified at its two resonant frequencies. The gained insight reveals that the secondary to the primary voltage gain of the transformer can be even larger than its turns ratio. A comprehensive study of circuit-to-phase-noise conversion mechanisms of different oscillators' structures shows the proposed class-F exhibits the lowest phase noise at the same tank's quality factor and supply voltage. Based on this analysis, a class-F oscillator was prototyped in 65-nm CMOS technology. The measurement results prove that the proposed oscillator can achieve a state-of-the-art phase noise performance with the highest power efficiency at low voltage power supply without die area penalty or voltage swing constraint.

2.6 Extension of class-F_3 operation to mm-wave frequency generation

High data-rate wireless communications in the unlicensed 60-GHz band have recently aroused a great interest[1]. Complex modulation and coding schemes employed there require low distortion, leading to strict specifications on a transmit (TX) error vector magnitude (EVM). For example, the IEEE 802.11ad standard requires a TX EVM of -21 dB for a 16QAM modulation [51], which sets stringent phase noise (PN) requirement on the local oscillators (LOs) [52, 53]. Wide tuning range (TR) is also necessary to cover the specified frequency bands (e.g., 57–65 GHz) with

[1] The main contributor of this section is Zhirui Zong from TU Delft. This work has also been published in the IEEE Journal of Solid-State Circuits [50].

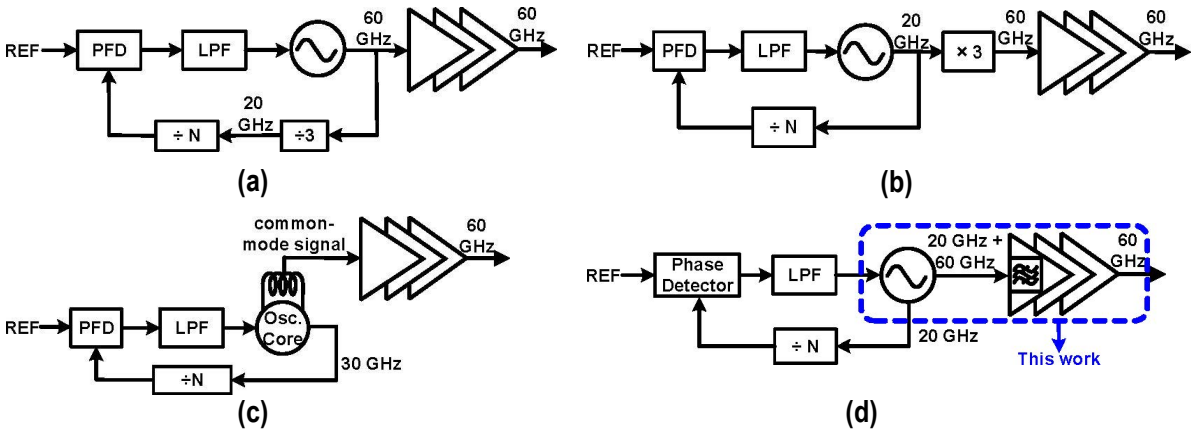


Figure 2.21: Evolution of the mm-wave PLL architecture (a): PLL with fundamental oscillator; (b): PLL with frequency multiplier; (c): PLL with push-push oscillator; (d): proposed PLL with harmonic boosting and extraction.

margin for process and temperature spreads. Meanwhile, long battery lifetime calls for high power-efficiency thus high figure-of-merit (FoM). Unfortunately, 60 GHz frequency generation in CMOS has typically suffered from poor PN, limited TR and high power consumption [54–59].

The traditional PLL architecture employs a 60 GHz oscillator (see Fig. 2.21 (a)), which feeds both a 60 GHz frequency divider back for a phase detection with a frequency reference clock, and a power amplifier to drive an antenna [55]. The difficulties of 60 GHz oscillators are: 1) the parasitic capacitance of active devices takes up a large share of the relatively small tank capacitance, thus limiting the frequency TR; 2) to achieve a TR of $\geq$15%, the poor Q-factor of the tuning capacitance dominates the Q-factor of the 60 GHz resonator, thus limiting the achievable PN. The 60 GHz frequency dividers must achieve large locking range to ensure sufficient overlap with the oscillator TR under PVT variations. However, there is a strong tradeoff between the locking range and the power consumption [60–62].

The aforementioned design challenges in the oscillators and frequency dividers are relieved in PLLs based on frequency multipliers (see Fig. 2.21 (b)) [57, 58, 63]. However, the 60 GHz frequency multipliers in this architecture typically have limited locking range, or consume large power, in order to achieve large locking range [63–66]. In PLLs with N-push oscillators (as shown in Fig. 2.21 (c) for N = 2), the frequency dividers operate at 60/N GHz, and frequency multipliers are avoided. However, this oscillator type suffers from low output power and mismatches among the N oscillators if N $>$ 2 [67–69].

To alleviate the design challenges for mm-wave oscillators and dividers without shifting more stress onto other blocks, a 60 GHz frequency generation technique based on a 20 GHz oscillator and an implicit $\times$3 frequency multiplier is proposed [70]. The basic concept of this work is to simultaneously generate both 20 GHz and a significant level of its third harmonic at 60 GHz inside a 20 GHz oscillator. The generated 60 GHz signal is fed forward to a buffer with natural bandpass filtering, whereas the 20 GHz signal is fed back for phase detection after further frequency division, as shown in Fig. 2.21 (d). Since the oscillator runs at the fundamental frequency of 20 GHz, its resonant tank achieves a better Q-factor than at 60 GHz, which leads to a better PN performance. Moreover, the tank has a larger inductance and capacitance. This increases the variable portion of the total tank capacitance and the frequency TR.

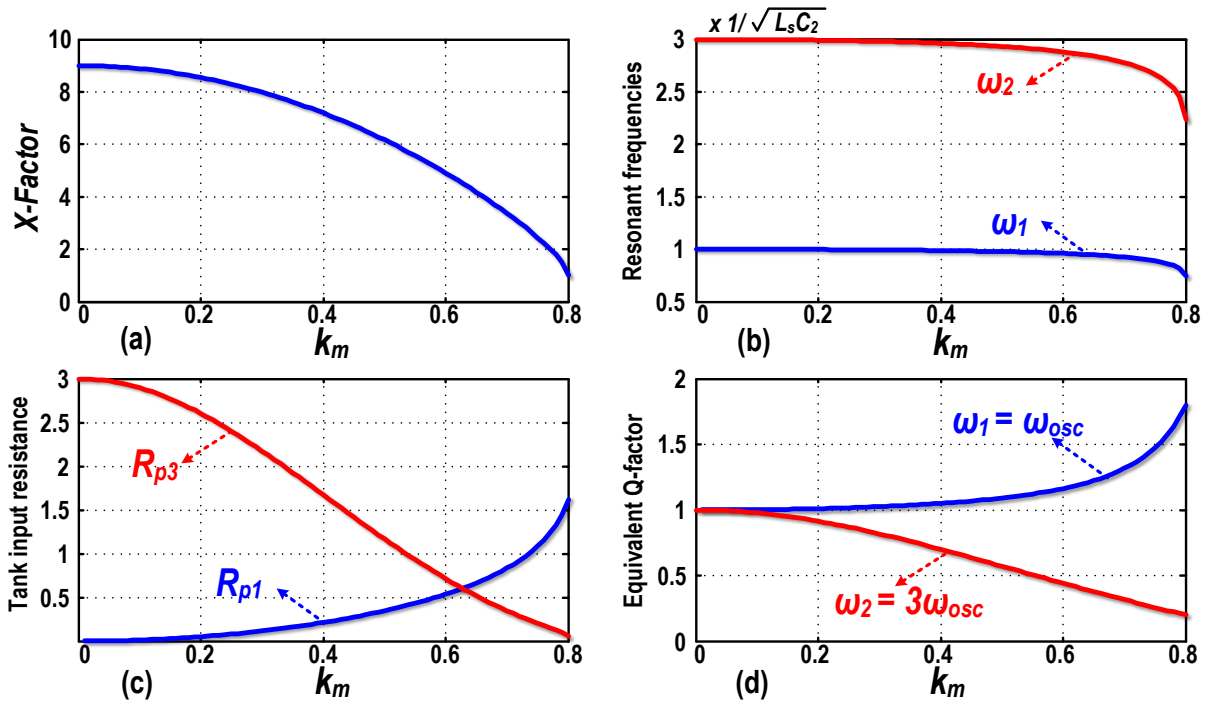


Figure 2.22: Dependency of (a) X-factor; (b) tank's first and second resonant frequencies; (c) R_{p1} and R_{p3}; (d) tank's equivalent Q-factor on k_m (while $\omega_2/\omega_1 = 3$).

As discussed in the previous sections, the third-harmonic injection technique has been exploited in a single-GHz oscillator to shape the oscillation waveforms for a better PN performance. In the original class-F oscillator [21], the magnitude ratio of the third-to-first harmonic components of the drain oscillation voltage was adjusted ~0.15 to achieve the lowest circuit-to-phase noise sensitivity during the triode operation of core transistors. However, instead of acting as an auxiliary therein, the third-harmonic component in this work is the signal of interest; therefore, to make it sufficiently stronger, a larger R_{p3}/R_{p1} is desired. On the other hand, the equivalent Q-factor (Q_{eq}) at the two resonant frequencies affect the oscillator performance dramatically. High Q_{eq} at ω_{osc} promotes low PN, while low Q_{eq} at $3\omega_{osc}$ is appreciated for better tolerance to the possible frequency misalignment between the second resonance and $3\omega_{osc}$. As we can see in Fig. 2.22 (c), R_{p1} decreases with smaller k_m, while R_{p3} behaves opposite. Therefore, smaller k_m is desired for larger R_{p3}/R_{p1}. However, as shown in Fig. 2.22 (d), larger k_m is required for high Q_{eq} at ω_{osc} and low Qeq at $3\omega_{osc}$. By reducing k_m for larger R_{p3}/R_{p1}, both the PN performance and the tolerance to the possible frequency misalignment between the second resonance and $3\omega_{osc}$ will be degraded. As a tradeoff between large third harmonic and optimal oscillator performance, $k_m = 0.61$ is chosen for $R_{p3}/R_{p1} > 1$ with sufficient Q_{eq}. Under this condition, as evident from Fig. 2.22 (a), the ratio of ω_2/ω_1 reaches the desired value of 3 for X-factor of 4.76.

With the above third-harmonic boosting technique, the magnitude ratio of the third-to-first harmonic components of the drain oscillation voltage increases to ~40%. Consequently, the oscillator is able to generate a significant harmonic amplitude at ~60 GHz in addition to the fundamental tone at ~20 GHz. To obtain a clean output spectrum at 60 GHz, the fundamental tone needs to be filtered out. LO buffers, which are commonly found in 60 GHz transceivers, are good bandpass filters by nature and are able to provide such filtering capabilities.

To demonstrate the effectiveness of the proposed mm-wave frequency generation scheme,

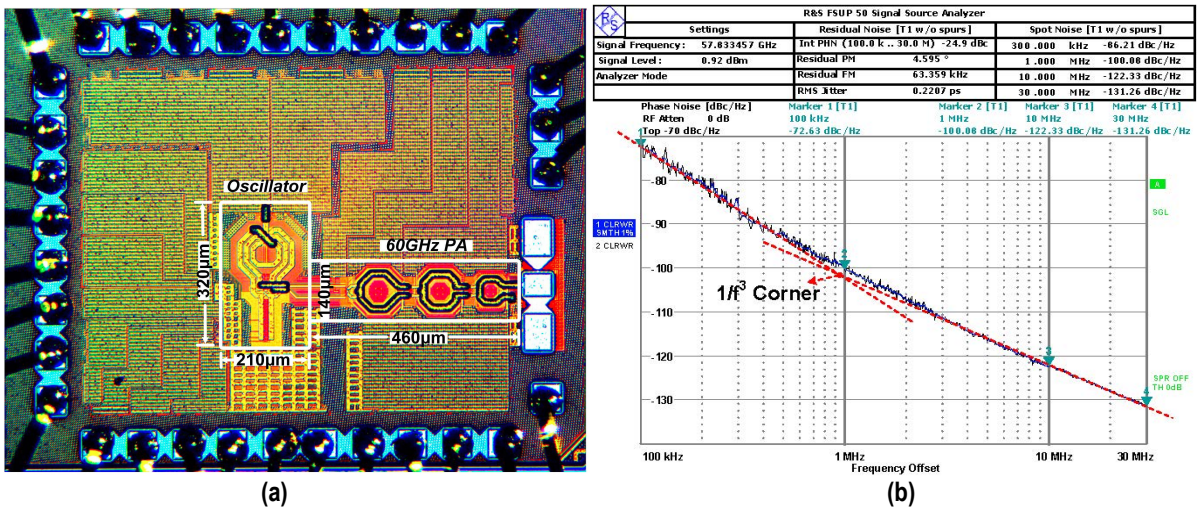


Figure 2.23: (a) Chip micrograph; (b) Measured phase noise at 57.8 GHz.

Table 2.4: Performance Comparison with State-of-the-Art 60 GHz Output Oscillator Systems.

		This work		[71]	[72]	[73]	[74]	[54]	[64]	[75]	[67]
Technology (nm)		40		90	130	90	65	40	65	65	32 SOI
Type		Harmonic extraction		Fundam-ental	Fundam-ental	Fundam-ental	Fundam-ental	Fundam-ental	Freq. tripling	Freq. tripling	CM extraction
P_{DC} (mW)	Osc.	13.5		14	3.9	8.1	8.4-10.8	14	24	10.6	42
	buf.	10.5[1]	22[2]	NA	NA	NA	NA	NA	NA	NA	
	× / ÷ [3]	0		4.8	NA	NA	NA	10	23.3	14	0
V_{DD} (V)		0.7/1	0.7	1.2	1	0.7	1.2	0.9	1.2/1	1.2	1
TR (GHz)		48.4-62.5 (25.4%)		55.8-61.6 (9.8%)	59-65.2 (10%)	53.2-58.4 (9.3%)	57.5-90.1 (41.1%)	53.8-63.3 (16%)	70.5-85.5 (19.2%)	58.3-65.4 (11.5%)	46.4-58.1 (22.4%)
PN (dBc/Hz)	1MHz	-100.1		-94	-95/-91	-91	NA	-91–-94.5	-91.7–-95.8	NA	-89
	10MHz	-122.3		NA	NA	NA	-104.6– -112.2	NA	NA	-115	-118
FoM (dBc/Hz)	1MHz	181.5[1]	179.8[2]	176.8	185/181	177.2	NA	172.7-175.4	176.6	NA	167.7
	10MHz	183.7[1]	182[2]	NA	NA	NA	172-180	NA	NA	176.9	176.7
FoM_T (dBc/Hz)	1MHz	189.6[1]	187.9[2]	176.6	185/181	176.6	NA	176.6-179.5	182.6	NA	174.7
	10MHz	191.8[1]	190.1[2]	NA	NA	NA	184.2-192.2	NA	NA	178.1	183.7

[1] including the power consumption of the *first* buffer/amplifier stage (10.5 mW) at V_{DD}=1.0 V
[2] including the *total* power consumption of the three amplifier stages (22 mW) delivering 0 dBm at V_{DD}=0.7 V
[3] power consumption of the 60 GHz frequency divider or multiplier

the third-harmonic boosting oscillator together with the three-stage 60 GHz output amplifier is prototyped in TSMC 40 nm 1P7M LP CMOS. The chip micrograph is shown in Fig. 2.23 (a). An R&S FSUP50 signal source analyzer is used with an external mixer to measure the oscillator's PN, whose plot is shown in Fig. 2.22 (b) at 57.8 GHz. At 1 MHz offset, the PN is -100.1 dBc/Hz, which is the best ever reported in CMOS. The $1/f^3$ PN corner is 920 kHz. The 60 GHz frequency generator achieves a 25%TR from 48.4 to 62.5 GHz. Table 2.4 summarizes the performance of the proposed 60 GHz frequency generator and compares it with the relevant state-of-the-art.

Chapter

3

An All-Digital PLL Based on Class-F DCO for 4G Phones

In this Chapter, a new architecture of an all-digital PLL (ADPLL) is introduced for advanced cellular radios[1]. It is based on a 1/8-length time-to-digital converter (TDC); and wide tuning range, fine-resolution class-F digitally-controlled oscillator (DCO) with only switchable metal capacitors. The 8 mW DCO emits -157 dBc/Hz at 20 MHz offset at ∼2 GHz, while fully satisfying metal density rules. The 0.4 mW TDC clocked at 40 MHz achieves PVT-stabilized 7 ps resolution for -108 dBc/Hz in-band phase noise. Reference spurs are <-91 dBc, while fractional spurs are <-72 dBc. The ADPLL supports a 2-point modulation and consumes 12 mW while occupying 0.22 mm^2, thus demonstrating both 72% power and 38% area reductions over prior records.

3.1 Introduction

While mobile phones enjoy the largest production volume ever of any consumer electronics product, the demands they place on frequency synthesizers are particularly tough, especially on integration with digital processors, low area, low-power consumption, low phase noise and virtually no spurs, while being robust against PVT variations. In this difficult design environment, the all-digital PLLs (ADPLLs) have shown to outperform analog PLLs in terms of area and power dissipation while having best-in-class RF performance [76] [77]. This is in addition to their expected compatibility with the digital design flow and extensive reconfigurability. These advantages are expected to continue improving with CMOS scaling, although each process node presents a unique set of challenges.

[1]The leader of this project is Feng-Wei Kuo from TSMS RF group. The author directly designed the DCO and divider. He was also involved in the technical discussions of ADPLL design.

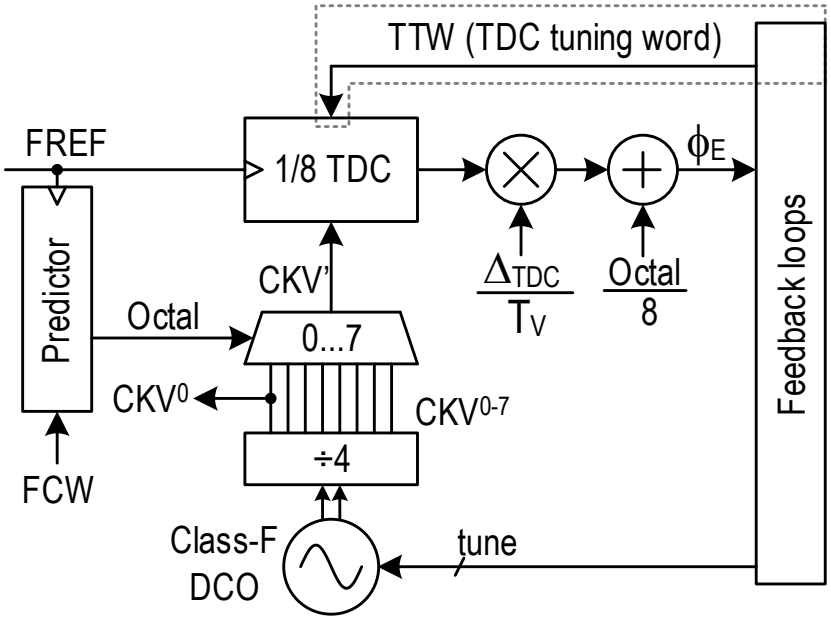


Figure 3.1: TDC within ADPLL and within adaptation loop to make its step size, Δ_{TDC}, PVT-free.

In this Chapter, a new architecture of an ADPLL is introduced for advanced cellular radios. It is optimized to the most advanced production low-leakage CMOS technology (i.e., 28 nm). The DCO addresses the new strict metal density rules and exploits class-F operation to satisfy the strict phase noise requirement of the 4G standard with an excellent power efficiency. The TDC uses phase prediction to reduce the required range and to improve resolution and lower the required linear range, thus saving power [19].

3.2 Time-to-Digital Converter (TDC)

Wireless standards require low integrated phase noise and spurious tones at the same time. It is well known that the TDC quantization of timing estimation between the reference and variable clocks affects the in-band RF output phase noise of the ADPLL. According to [78]:

$$\mathcal{L} = 10\log_{10}\left(\frac{(2\pi)^2}{12}\cdot\left(\frac{\Delta_{TDC}}{T_V}\right)^2\cdot\frac{1}{f_R}\right) \tag{3.1}$$

where, T_V is the variable DCO period, f_R is the reference clock frequency and Δ_{TDC} is the average time resolution of the TDC. Eq (3.1) indicates that ADPLL in-band phase noise can be significantly improved by reducing Δ_{TDC}. The TDC resolution has traditionally been tied to the loaded delay of the basic regenerative circuit, i.e., an inverter. With only ∼10 ps inverter delay now in low-leakage 28 nm CMOS versus ∼30 ps a decade ago, there are over 50 inverters needed to cover the ∼2 GHz (i.e., cellular high-band) variable DCO period. With each inverter introducing a small differential type of non-linearity (DNL), these nonlinearities can quickly accumulate to form a much larger integral type of non-linearity (INL) of the TDC transfer function. The TDC transfer function non-linearity (i.e., INL) can create fractional spurs especially at close to integer-N channels or at wide PLL loop bandwidths [79]. Consequently, a *simultaneous* reduction of the quantization step and TDC dynamic range are required to

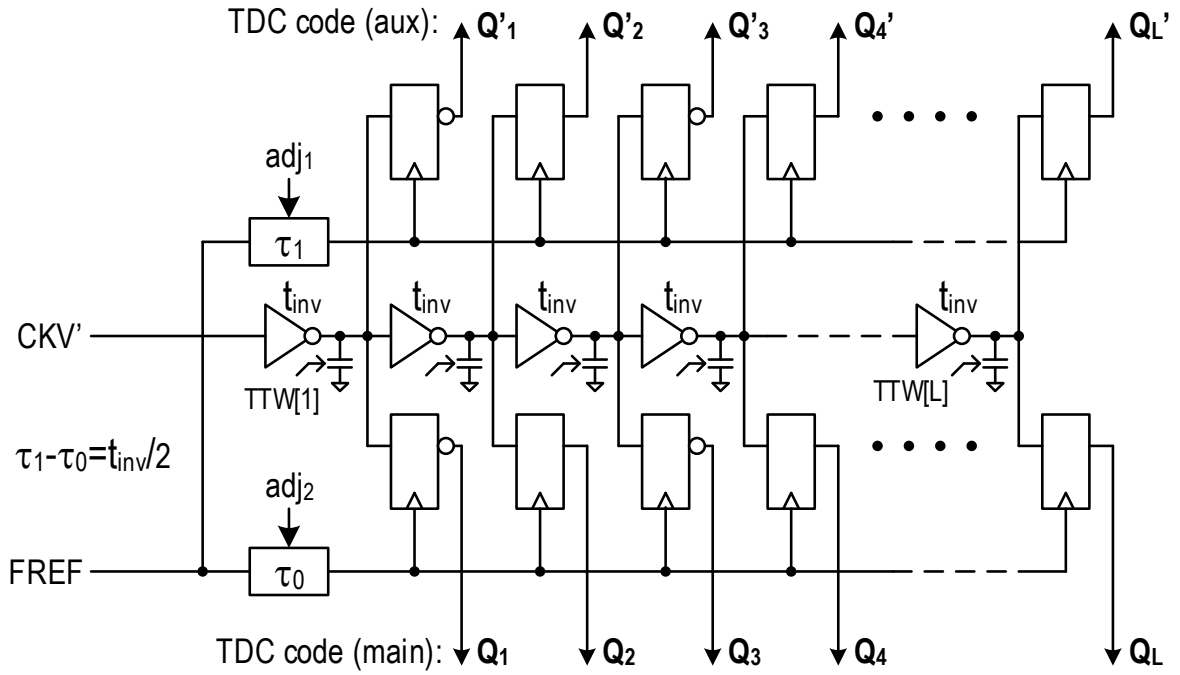


Figure 3.2: Schematic of the parallel TDC with stabilized inverter delay.

respectively achieve a low in-band phase noise and spurious tones. In this work, to keep the fine resolution and linearity, and to reduce the power consumption simultaneously, a 1/8-length TDC with two-staggered-chains topology is proposed.

Traditionally, the TDC has to cover the full range of CKV, as in [76], between the CKV and FREF. TDC range can be reduced by bringing the CKV closer to FREF. This is accomplished by selecting a phase from the multi-phase DCO divider output, CKV^{0-7}, that is closest to FREF, as shown in Fig. 3.1. Consequently, the long string of L (e.g., >50) inverters is shortened by 8x by running the DCO at 4x the carrier frequency and dividing its output by four to create a CKV clock vector, $\text{CKV}^{0\ldots7}$. A phase predictor ensures the TDC input CKV' is $< T_V/8$ by selecting a CKV phase that is closest to FREF. This prediction is based on two MSB bits of a fractional part of reference phase, $R_R[k]$, which is an accumulated frequency command word (FCW). The TDC output, after decoding, is normalized to T_V by the $\Delta t_{TDC}/T_V$ multiplier and the octal estimation, normalized to $T_V/8$, is added to produce the phase error ϕ_E. The DCO tuning word is updated based on ϕ_E.

Fig. 3.2 shows a schematic of the new TDC that exploits a 2-way parallelism to halve its quantization step [80]. The selected DCO variable clock, CKV', goes through a string of L (e.g., ∼15) inverters of $t_{inv} \approx 10\,\text{ps}$ intrinsic delay. The delays are stabilized by an outer feedback loop via "TDC tuning word" (TTW) by digitally turning on/off the NMOS capacitors loading each inverter. This is needed to prevent excessive expansion of inverters at fast process corners and high supply voltages. The inverter output bus is fed to two arrays of flip-flops (FF), which are clocked by FREF delayed by τ_0 and τ_1 for the main and auxiliary FF arrays, respectively. The τ_0 and τ_1 are controlled to maintain their difference of $\tau_0 - \tau_1 = t_{inv}/2$. In this case, the quantization step will be halved to $\Delta_{TDC} = t_{inv}/2 \approx 5\,\text{ps}$ thus doubling the timing resolution. However, the process, voltage and temperature (PVT) stabilizing capacitors increase that delay to 6–7 ps. For non-critical applications, the auxiliary FF array can be shut down by gating off

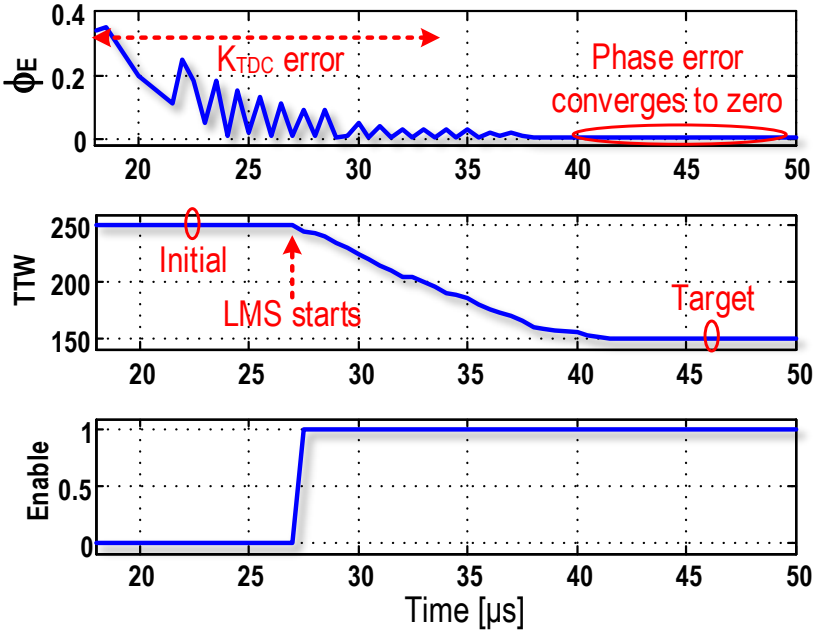


Figure 3.3: Captured real-time internal signals during TDC calibration: phase error (ϕ_E), TDC tuning word (TTW) and TDC calibration enable.

its clock to bring the step size back to $\Delta_{TDC} = t_{inv} \approx 10$–$14$ ps.

Fig. 3.1 also shows a proposed technique to stabilize the TDC step size, Δ_{TDC}. After the ADPLL is locked but before the calibration is enabled, the "ripple" of the phase error ϕ_E is large due to the error between an initial (typically, unknown) value and the desired target of the TDC resolution, Δ_{TDC}. TTW will converge into the target resolution by forcing ϕ_E to zero using a signed-LMS algorithm. This way, independent from PVT, the ADPLL will always settle to the same targeted TDC resolution.

The plots in Fig. 3.3 were captured during lab measurements by dumping the digital signals into on-chip SRAM memory. Until the LMS algorithm starts at time = 27 μs, the phase error exhibits a large ripple, which then keeps on reducing while the TTW settles to the final value corresponding to the targeted Δ_{TDC}. At time ~41 μs, the algorithm has fully settled and the phase error is almost flat at zero.

3.3 ADPLL Architecture

Figure 3.4 shows a block diagram of the proposed multi-rate ADPLL [76]. A class-F DCO is at the heart of the ADPLL, and oscillates from 5.9-to-8.5 GHz. It consists of three different tuning banks with a 120 kHz raw frequency resolution at 8 GHz. A $\Delta\Sigma$ dithering bank operating at CKV/4=~500 MHz improves the frequency resolution to 480 Hz for an 8 GHz carrier. The ~2 GHz ÷4 divider output of 8 phases, CKV^{0-7}, oversamples the external frequency reference (FREF: 10–50MHz) generating CKR^{0-7} vector clock. They sample the variable DCO phase Rv[k] to calculate the phase error, $\phi_E[k]$. To avoid metastability in FREF retiming, FREF is simultaneously oversampled by different phases of CKV and an edge selection signal chooses the path farther away from metastability. The $\phi_E[k]$ is fed to the type-II loop filter (LF) with 4th order IIR. The LF is dynamically switched during frequency acquisition to minimize the settling

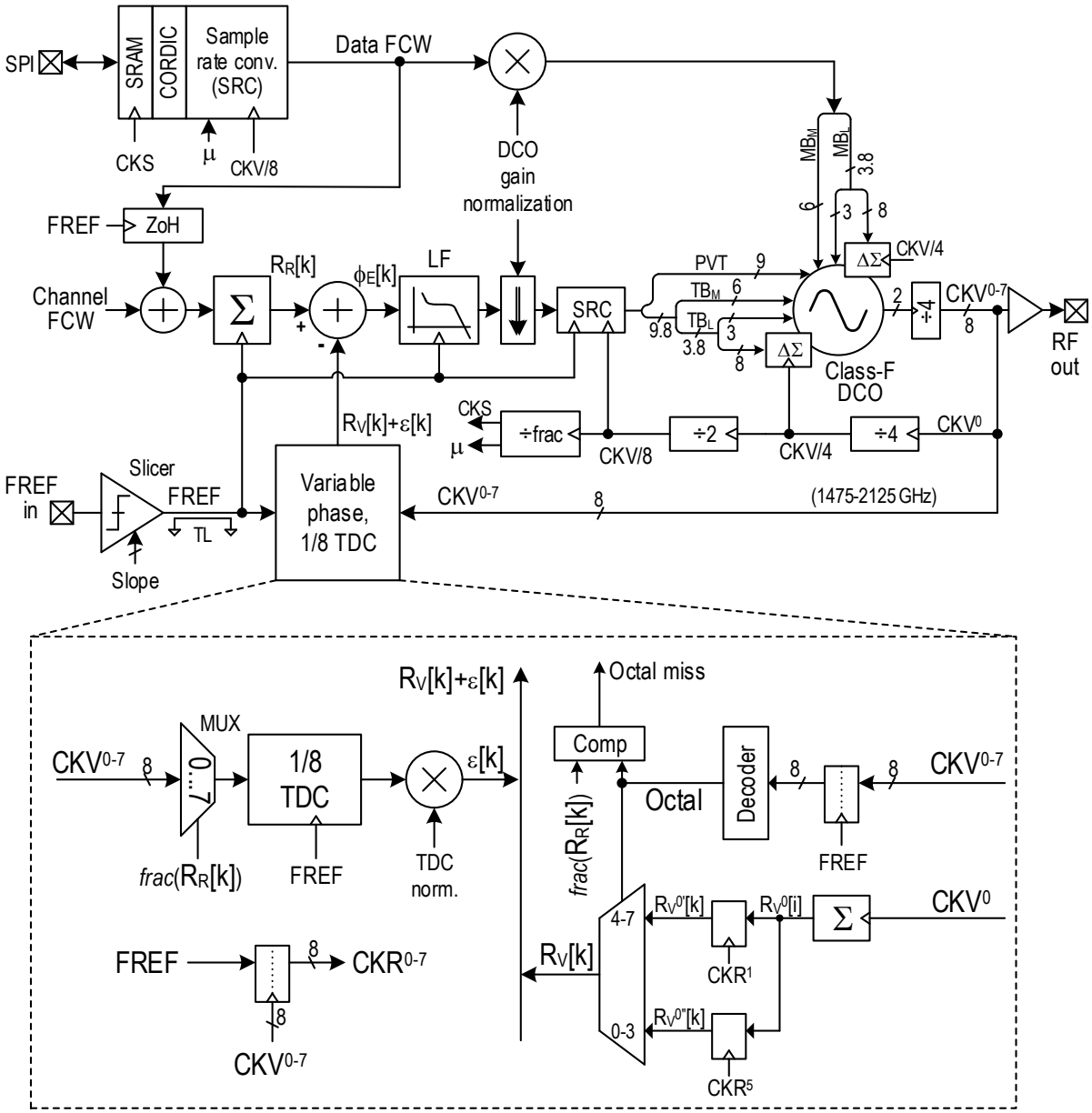


Figure 3.4: Block diagram of the proposed ADPLL with 1/8-length TDC and 2-point frequency modulation (top) and Variable phase calculation circuit (bottom).

time while keeping the phase noise (PN) at optimum. The FREF slicer contains a 3-bit slope control to reduce the FREF spurs at the cost of a slight increase of in-band PN. The built-in DCO gain, K_{DCO}, and TDC gain, K_{TDC}, calibrations are autonomously performed to ensure the wideband FM response [4], [81]. Five wide SRAMs and other digital arithmetic blocks are also integrated on-chip to enable initial system debugging.

The proposed ADPLL also supports frequency modulating (FM) with sample rates much higher than the reference frequency. One data path directly modulates the DCO, while the other data path is compensating and prevents the modulating data from changing the phase error. Consequently, the modulation rate is not limited to the ADPLL close-loop bandwidth. Furthermore, the slow drift of DCO frequency is refined by ADPLL negative feedback. The direct path has high-pass, while the compensating path has low-pass filtering characteristics.

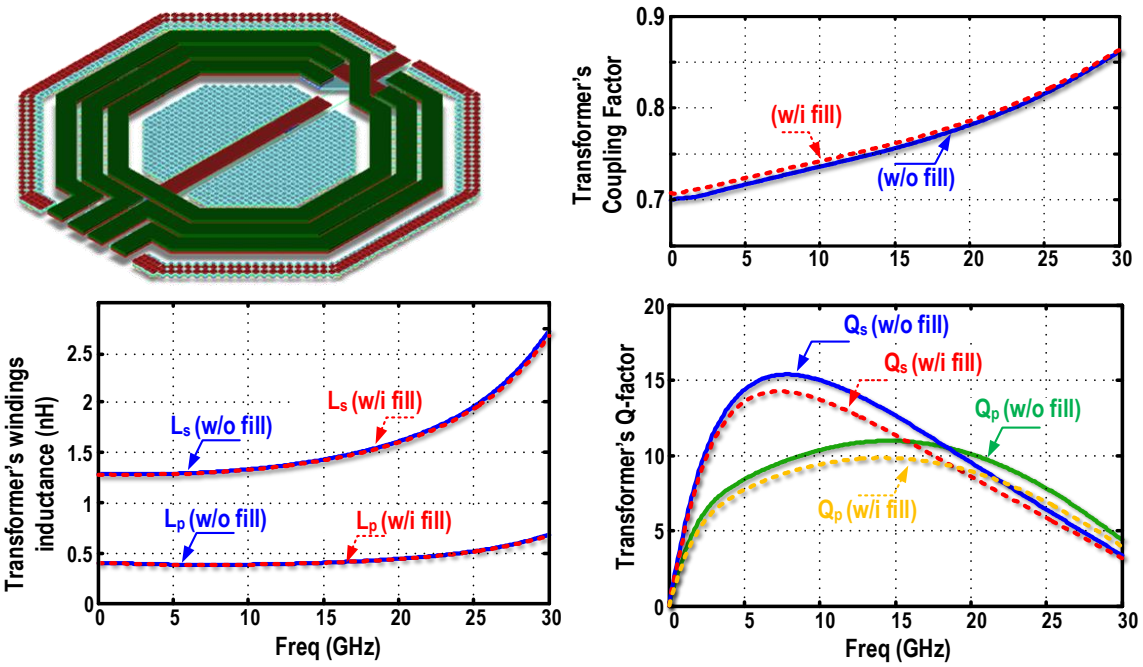


Figure 3.5: Effects of dummy metal fills on the 28 nm CMOS class-F transformer.

An all-pass transfer function for the modulating data can be realized if both paths are combined without any delay difference and DCO gain, K_{DCO}, is accurately estimated. K_{DCO} gain can be automatically estimated via digital averaging techniques as in [4], [81].

The sampling rate of the modulation should be high enough (~250 MHz) to satisfy 4G standard with I/Q 20 MHz channel bandwidth[1]. Consequently, a low integer division of the variable DCO clock (CKV/8) is used as the sampling rate of modulating data. However, the phase error correction of the ADPLL still operates at f_R rate. Hence, the ADPLL has two clock domains (f_R and CKV/8), which interface with each other at the DCO's input. Consequently, as shown in Fig. 3.4, a sampling rate converter (SRC) is required to covert the symbol-related sampling frequency (f_R) into the channel-frequency-dependent rate (CKV/8).

The symbol rate should be preferably implemented in the fixed-frequency clock domain (integer multiple of data rate) for the pulse-shape filtering and the digital baseband. Consequently, a fractional divider is also implemented to produce a stable clock for the baseband signal processing.

3.4 Digitally Controlled Oscillator (DCO)

The 28 nm CMOS technology has strict requirements on design for manufacturing (DFM), especially the 20% minimum metal density rule, which is much stricter than in the previous 40 nm node. Hence, inductors and transformers must include a lot of dummy metal pieces on *all* metal layers. EM simulations of a transformer used in this design are shown in Fig. 3.5. Metal fills show negligible effect on the windings self-inductance and coupling factor k_m. However, Eddy currents in the dummy fills increase the resistive loss and thus transformer's Q-factor is

[1]Note that the Cartesian (I/Q) to the polar (ρ and θ) conversion significantly expands signal's bandwidth.

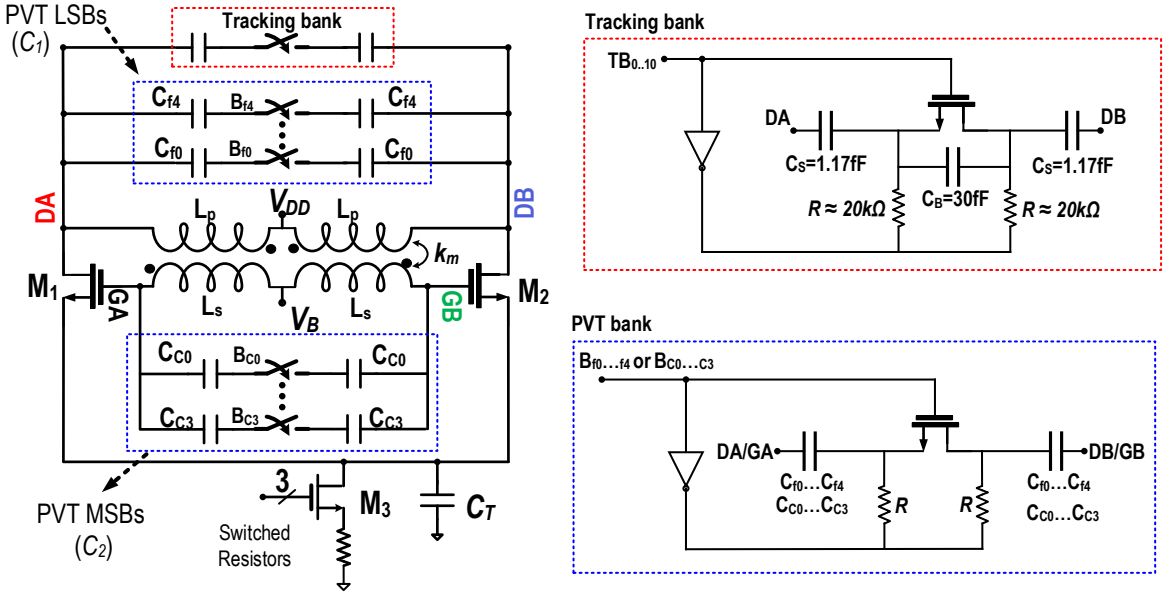


Figure 3.6: Schematic of the class-F DCO.

degraded by 10–20%. Dummy fills also increase the capacitance, thus degrading the self-resonant frequency. Furthermore, the excess noise of transistor, γ, is also increased by migrating to finer CMOS technologies. Consequently, both phenomena hurt the operation of an RF oscillator.

As explained in the previous Chapter, recently introduced class-F oscillator [21], addresses the above issues by: (1) enforcing a pseudo-square voltage across the tank, thus reducing the impulse sensitivity function (ISF), and (2) exploiting the transformer's voltage gain, G_0. The phase noise is less sensitive to the loss of the tank due to its lower ISF, while the effective noise factor of the gm-devices is reduced by G_0. The pseudo-square waveform is realized by increasing the 3rd harmonic of the fundamental oscillation voltage through an additional impedance peak and strong 3rd harmonic of the drain current. The transformer along with tuning switched capacitors realizes a 4th-order tank with two resonant frequencies, in which the first one determines the oscillation frequency, ω_0, and second one should be adjusted around $3\omega_0$ to enforce the pseudo-square voltage waveform. The ratio of resonant frequencies should be 3 with 10% accuracy and controlled by C_2/C_1 for a given transformer with a $k_m \approx 0.7$. As shown in Fig. 3.6, the positive feedback and G_0 are realized by a 1:2 step-up transformer with primary and secondary inductors L_p and L_s, respectively. The aluminum capping layer is strapped to the top copper layer to form the windings and improve the transformer's primary and secondary Q-factors. PVT banks are divided equally between L_p and L_s to guarantee the class-F operation over tuning range, while the tracking bank is located at L_p.

The switched poly resistors, which are digitally friendly and substantially free of 1/f noise, define the tail current. However, a small tail resistor could load the LC tank and lower the effective Q-factor when the oscillation forces M_1 or M_2 into the triode region. Fortunately, tank ISF is negligible during this time span and extensive noise of loaded-Q will not convert to phase noise.

The digitally controlled varactors exploiting C-V characteristics of MOS devices, such as in [76], are entirely avoided here as they are more sensitive to supply pushing and temperature variations. There are 9-bit binary PVT switchable capacitors for coarse tuning, and 63-bit

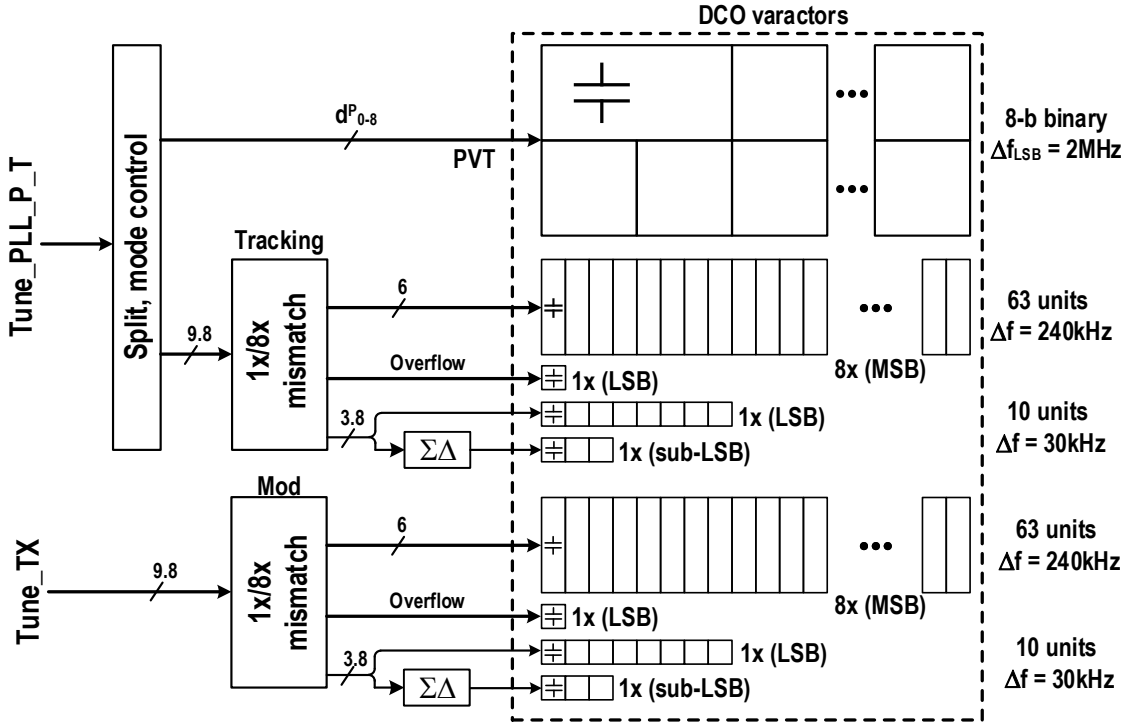


Figure 3.7: The input interface of the proposed DCO.

unary MSB (i.e., 8x) and 10-bit unary LSB (i.e., 1x) switchable capacitors for fine tuning. The segmented unit-weighted fine tuning switch-caps are well matched to provide a linear 9-bit resolution for modulation and drift tracking.

The tracking bank consists of two small capacitors (C_S=1.17 fF) and one big capacitor (C_B=30 fF). The on-state capacitance is determined by two series-connected C_S and the off-state capacitance is determined by two C_S and one C_B connected in series. The difference between the on- and off-states provides a well-defined ultra-small capacitance step size ($\Delta C \approx C_S^2/2C_B \approx$ 20 aF) and thus a fine frequency resolution ($\Delta f = 30$ kHz at $f_0 = 2$ GHz).

The digitally controlled quantized capacitance of the transformer-based tank is split into three major banks as shown in Fig. 3.7. The d^P inputs correspond to the process-voltage-temperature (PVT) and are activated during frequency locking and are frozen afterwards. The PVT bank demonstrates a coarse tuning step of ∼2 MHz at f_0=2 GHz. The DCO features two separate identical tracking (TB) and modulation (MB) banks, which are respectively used for phase-error correction and direct FM modulation. Each bank is segmented with 11 LSB (i.e., 1x ≡ 30 kHz) and 64 MSB (i.e., 8x) unit-weight varactors. Consequently, the tuning range of both banks is 30 kHz×$(11 + 8 \times 64)$ = 15.7 MHz. The LSB part of the tracking bank is further partitioned into 8 integer and 3 fractional varactors, with the latter undergoing high-speed ΔΣ dithering for resolution enhancement. The tracking and modulation tuning words are a fixed-point number with the integer part directly controlling the number of active unit-weighted varactors. The fractional part is fed to the ΔΣ modulator, which produces an integer stream whose average value is equal to that of the fractional input.

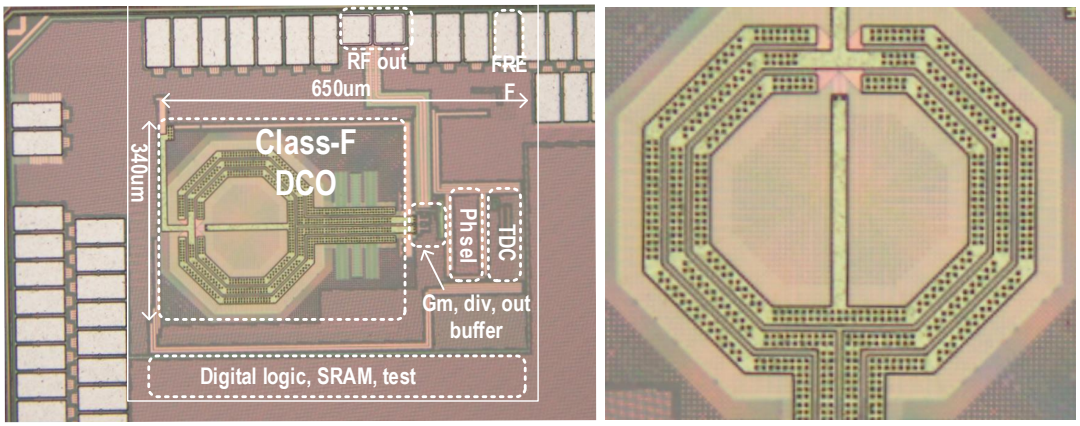


Figure 3.8: Chip micrograph of the ADPLL and the zoomed-in transformer revealing lots of dummy metal fills.

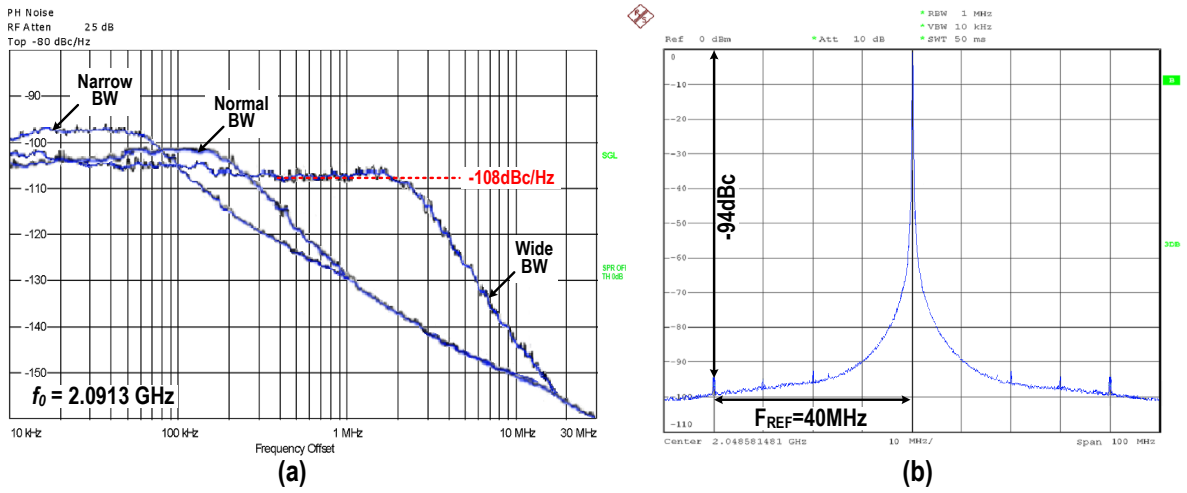


Figure 3.9: Measured ADPLL (a) phase noise and (b) spectrum (a); with 40 MHz FREF. The spectrum, taken with wide loop bandwidth of 1.5 MHz, is virtually spur-free.

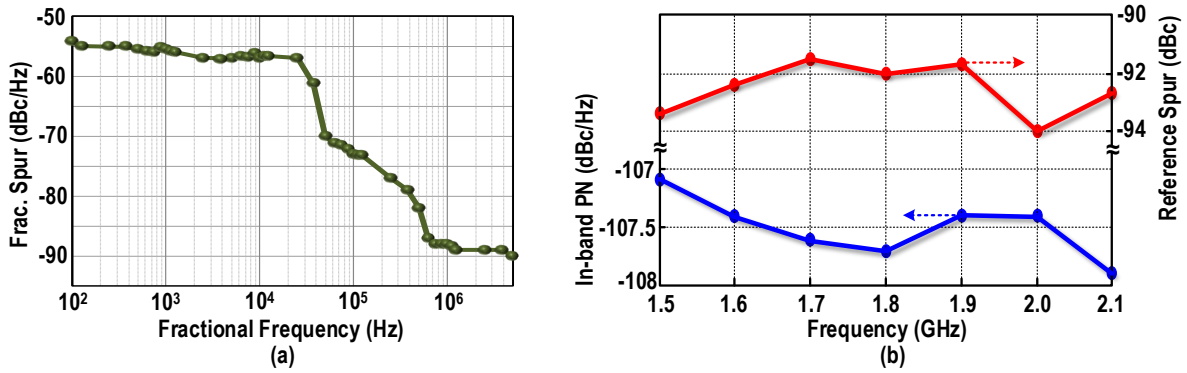


Figure 3.10: (a) Measured largest fractional spurs for fractional frequencies away from 2040 MHz integer-N channel and (b) measured in-band phase noise and reference spurs over 1.5–2.1 GHz in 100 MHz steps.

3.5 Measurement Results

The proposed ADPLL is implemented in 28 nm low-leakage digital CMOS process and meets the tough phase noise and spurious standards of advanced cellular radios. Figure 3.8 shows the

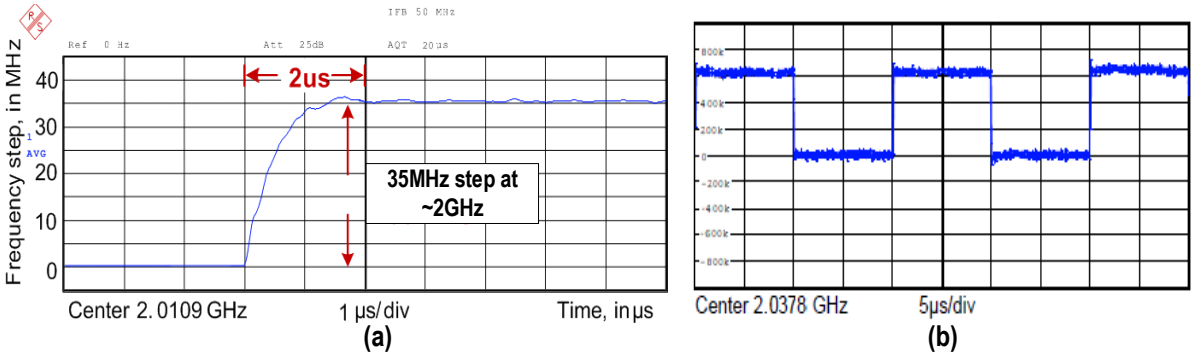


Figure 3.11: (a) Measured demodulated signal during FSK modulation and (b) Measured lock-in time for a frequency step of 35 MHz.

chip micrograph.

Fig. 3.9 shows the measured spectrum and phase noise (PN) at 2.0913 GHz ADPLL output with fractional FCW = 52.2825. An ultra-low level FREF spur of -94 dBc is measured with no other significant spurs observed. PN at 20 MHz offset from the ~2 GHz carrier is -157 dBc/Hz. PN was measured for three different ADPLL loop bandwidths: narrow (~80 kHz), normal (~250 kHz) and wide (~2.5 MHz). The in-band PN of -108 dBc/Hz in wide bandwidth (to filter out the DCO noise) corresponds exactly (according to Eq. (3.1)) to the TDC quantization noise at 7 ps resolution at 40 MHz FREF, while showing no other noise sources. The measured integrated jitter of 253 fs corresponds to the total integrated PN of 0.18°.

The oscillator phase noise is -157 dBc/Hz at 20 MHz offset from 2.09 GHz carrier which extrapolates to -164.2 dBc/Hz when normalized to 915 MHz and meets the GSM TX mobile station specification with 2.2 dB margin. The oscillator consumes ~7.4 mW from 1.05 V supply voltage. As a consequence, the measured FoM of this class-F oscillator is 189 dB. It is among best-in-class despite being 3 dB lower than the original design in 65 nm [21], where it can support larger V_{DD} and does not suffer from the lack of ultra-thick copper metal layer and restrictive metal density rules. It should be noted that a traditional oscillator was also fabricated on the same wafer and shows a 3–4 dB lower FoM.

As shown in Fig. 3.10, the in-band PN varies only 1 dB over the full frequency range, while the reference spur is better than -91 dBc, and the fractional spurs are below -72 dBc. The ultra-low spur levels validate the short TDC approach that limits its INL non-linearity.

To achieve simultaneous fast locking and low integrated phase noise, the loop bandwidth is dynamically controlled via a gearshift technique [82]. During frequency acquisition, the loop operates in type-I, with a wide bandwidth of 2 MHz. It is then switched to type-II, 4th-order IIR filter with the 500 kHz bandwidth when it enters tracking mode. Finally, the loop bandwidth is reduced to 250 kHz to optimize ADPLL integrated phase noise. The measured lock-in time is less than 2 μs for a frequency step of 35 MHz at F_{REF} of 40 MHz as shown in Fig. 3.11 (a).

Figure 3.11 (b) demonstrates the ADPLL two-point frequency modulation (FM) capability when applying FCW samples corresponding to alternating (every 10 μs) sequences of zero and 600 kHz. Both DCO and TDC gains are calibrated automatically via digital averaging techniques as in [4], [81]. The calibrated $\widehat{K_{DCO}}$ is then applied to the gain normalization multiplier in the direct modulation path (see Fig. 3.4). As a consequence, the FM response steps are square thus wideband (i.e., supporting many harmonics).

Table. 3.1 summarizes the ADPLL and compares it against those used in state-of-art advanced

Table 3.1: Performance summary and comparison with published ADPLLs for cellular phones.

	This work	Weltin-Wu JSSC'15	Staszewski JSSC'11	Vercesi JSSC'12	Takinami ISSCC'11	Hsu JSSC'08	Chang ISSCC'08
CMOS node	28nm	65nm	65nm	55nm	65nm	130nm	130nm
Supply (V)	1.05	1.0	1.2	1.2	1.2/1.5	1.5	N/A
Output frequency (GHz)	1.475-2.125	2.8-3.5	1.8-2	1.45-2.025	2.6-4.5	3.2-4.2	3.2-4
Tuning range (%)	36	22.2	22	33	54	27	22.2
Out-of-band PN (dBc/Hz)							
3MHz	-148.2	-149.7	N/A	N/A	N/A	-144.9	-148
20MHz	-164.2	-166	167	165.9	161	-162	-164
DCO power cons. (mW)	7.4	8.3	23	32.5	33	N/A	20[6]
Ultra-thick metal	No	N/A	N/A	N/A	N/A	N/A	N/A
DCO FOM[1] (dB)	188.7	190	186.6	184	179	N/A	<184.2
DCO FOM$_T$[2] (dB)	199.8	197	193.5	194.5	193.7	N/A	<191.1
PN at 400kHz (dBc/Hz)	-121.2	-120.5	N/A	-113.9	-122.8	-120	-129
FREF (MHz)	40	26	38.4	26	78	50	26
PLL bandwidth (kHz)	250	140	N/A	800	1000	500	50
In-of-band PN (dBc/Hz)	-110	-104.6	N/A	-113.9	-122.8	-120	-90.5
Reference spur (dBc)	-94	-81	N/A	N/A	-56	-65	-84
In-band frac. Spur (dBc)	-72	-60	N/A	-50	-40	-42	N/A
Settling time (µsec)	2	N/A	N/A	79	N/A	20	N/A
(AD)PLL power (mW)	11.5	15.6	38.4	41.5	45	39	40[7]
Integrated jitter (fsec)	253	665	N/A	N/A	N/A	200	N/A
PLL FOM[3] (dB)	186.8	187.3	184.4	182.9	177.7	179.3	<181.2
PLL FOM$_T$[4] (dB)	197.9	194.2	191.2	193.3	192.3	188	<191.1
PLL FOM[5] (dB)	241.3	231.6	N/A	N/A	N/A	238	N/A
PLL area (mm^2)	0.22	0.35	0.35	0.7	0.6	0.95	0.86

[1]FoM = |PN|+20 $\log_{10}(f_0/\Delta f)$ - 10 $\log_{10}(P_{DC,osc})$ [2]FoM$_T$ = |PN|+20 $\log_{10}((f_0/\Delta f)$ (TR/10)) - 10 $\log_{10}(P_{DC,osc})$
[3]FoM = |PN|+20 $\log_{10}(f_0/\Delta f)$ - 10 $\log_{10}(P_{DC,PLL})$ [4]FoM$_T$ = |PN|+20 $\log_{10}((f_0/\Delta f)$ (TR/10)) - 10 $\log_{10}(P_{DC,PLL})$
[5]FoM = 10 $\log_{10}(\sigma^2_{t,PLL} \cdot P_{DC,PLL})$, Δf=20 MHz for all FoM calculations,
[6,7] DCO and PLL respectively draw 20 mA and 40 mA from unknown supply voltage in 130 nm CMOS

cellular radios [76, 83–87]. While keeping the best-in-class RF performance, the area and power consumption are significantly better than in the prior ADPLL implementations. The power consumption of the ADPLL is 11.5 mW and represents over 70% reduction versus the prior publications. The FoM that captures the output *spot* phase noise in the upconverted thermal region ($1/f^2$) normalized to the power consumption of DCO and PLL (here they are only within $10\log_{10}(11.5/7.4) = 1.9$ dB to each other) is best-in-class. Further normalizing the FoM to the tuning range of 36% results in FoM$_T$ that is 4.5 dB better than the prior record. The ADPLL loop settles within only 2 μs, made possible by the dynamic hitless gear-shifting of the loop filter coefficients. The ADPLL area is only 0.22 mm^2 and it represents over 35% reduction over the prior record.

3.6 Conclusion

An all-digital PLL was realized in 28-nm CMOS having best-in-class phase noise and spurious emission performance sufficient for LTE cellular phones. The area and power consumption are much better than the prior publications. The new ADPLL architecture predicts the inputs to the time-to-digital converter thus substantially narrowing its range to 1/8 of the 2 GHz output clock period. The TDC resolution is improved by a factor of 2 through parallelism and stabilized to make it largely independent from PVT conditions. The DCO addresses the new strict metal

density rules and exploits class-F operation to satisfy the strict phase noise requirement of 4G standard with a higher power efficiency.

Chapter

4

An Ultra-Low Phase Noise Class-F_2 CMOS Oscillator with 191 dBc/Hz FoM and Long-Term Reliability

In this Chapter, we propose a new class of operation of an RF oscillator that minimizes its phase noise[1]. The main idea is to enforce a clipped voltage waveform around the LC tank by increasing the second-harmonic of fundamental oscillation voltage through an additional impedance peak, thus giving rise to a class-F_2 operation. As a result, the noise contribution of the tail current transistor on the total phase noise can be significantly decreased without sacrificing the oscillator's voltage and current efficiencies. Furthermore, its special impulse sensitivity function (ISF) reduces the phase sensitivity to thermal circuit noise. The prototype of the class-F_2 oscillator is implemented in standard TSMC 65-nm CMOS occupying 0.2 mm^2. It draws 32–38 mA from 1.3 V supply. Its tuning range is 19% covering 7.2–8.8 GHz. It exhibits phase noise of -139 dBc/Hz at 3 MHz offset from 8.7 GHz carrier, translated to an average figure-of-merit of 191 dBc/Hz with less than 2 dB variation across the tuning range. The long term reliability is also investigated with estimated >10-year lifetime.

4.1 Introduction

Spectral purity of RF LC-tank oscillators is typically addressed by improving a quality factor (Q) of its tank, lowering its noise factor (NF), and increasing its power consumption. Even though technology scaling increases the *effective* capacitance ratio, C_{max}/C_{min}, of switchable tuning capacitors and, consequently, the oscillator tuning range, it does not improve the oscillator's spectral purity parameters, such as tank Q-factor and oscillator NF. In fact, the tank Q-factor

[1]This chapter has been published in the IEEE Journal of Solid-State Circuits [88].

is slightly degraded in more advanced technologies mainly due to closer separation between the top-metal and lossy substrate as well as thinner lower-level metals that are used in metal-oxide-metal (MoM) capacitors. On the other hand, transistor excess noise factor, γ, thus oscillator NF, keeps on degrading, thus penalizing the oscillator phase noise (PN). Consequently, the oscillators of excellent spectral purity and power efficiency are becoming more and more challenging as compared to other RF circuitry that is actually gaining from the technology scaling. This has motivated an intensive research leading to recently introduced new oscillator topologies [21]- [89].

In this Chapter, we specifically address the ultra-low phase noise design space while maintaining high power efficiency. We propose a soft-clipping class-F_2 oscillator topology based on enforcing a clipped voltage waveform around the LC tank by increasing the 2nd-harmonic of the fundamental oscillation voltage through an additional impedance peak [89]. This structure shifts the oscillation voltage level so that it provides enough headroom for the tail current without compromising the oscillating amplitude. Consequently, the phase noise contribution of the tail current transistor is effectively reduced while maintaining the oscillator voltage efficiency. Furthermore, the class-F_2 operation clips the oscillation waveform for almost half of the period, thus benefiting from the lower circuit-to-phase noise conversion during this time span.

The Chapter is organized as follows: The trade-offs between the RF oscillator PN and power consumption are investigated in Section 4.2. Section 4.3 establishes the environment to introduce the class-F_2 operation, its benefits and constraints. The circuit-to-PN conversion mechanisms are studied in section 4.4. Section 4.5 presents extensive experimental results. The oscillator long term reliability is studied and quantified in Section 4.6.

4.2 Challenges in Ultra-Low Phase Noise Oscillators

The phase noise (PN) of the traditional oscillator (i.e., class-B) with an ideal current source at an offset frequency $\Delta\omega$ from its fundamental frequency ω_0 could be expressed as,

$$\mathcal{L}(\Delta\omega) = 10\log_{10}\left(\frac{KT}{2\,Q_t^2\,P_{DC}}\frac{1}{\alpha_I\;\alpha_V}\,(1+\gamma)\left(\frac{\omega_0}{\Delta\omega}\right)^2\right) \tag{4.1}$$

where, Q_t is the tank quality factor; α_I is the current efficiency, defined as the ratio of the fundamental current harmonic I_{ω_0} over the oscillator DC current I_{DC}; and α_V is the voltage efficiency, defined as the ratio of the oscillation amplitude V_{osc} (single-ended) over the supply voltage V_{DD}. The oscillator power consumption is

$$P_{DC} = \frac{V_{osc}^2}{\alpha_I \cdot \alpha_V \cdot R_{in}} \tag{4.2}$$

where, R_{in} is an equivalent input parallel resistance of the tank modeling its losses. Eq. (4.1) clearly demonstrates a trade-off between power consumption and PN. To improve the oscillator PN one must increase P_{DC} by scaling down R_{in}. This could be done by lowering the tank inductance while maintaining the optimal Q_t. For example, by keeping on reducing the inductance by half, R_{in} could theoretically decrease by half at the constant Q_t, which would improve phase noise by 3 dB with twice the power consumption at the same FoM[1]. However, at some point, the resistance of the tank's interconnections will start dominating the resonator losses and,

[1]FoM = |PN|+ 20 $\log_{10}(\omega_0/\Delta\omega)$ - 10 $\log_{10}(P_{DC}/1mW)$

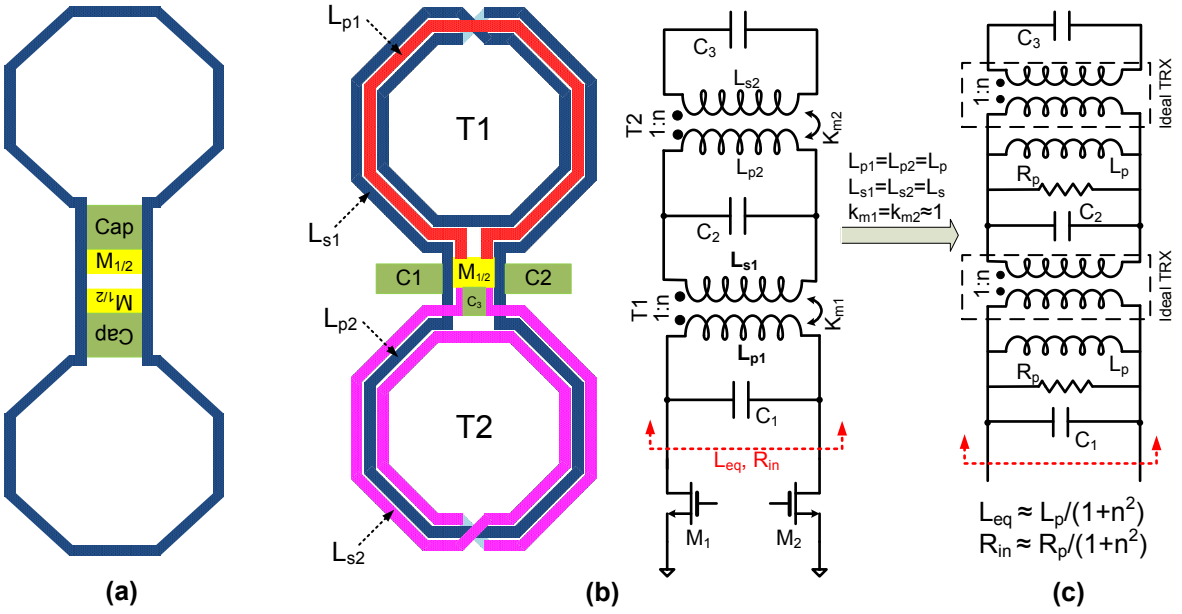


Figure 4.1: Phase noise reduction techniques without sacrificing tank's Q-factor: (a) coupled oscillators, (b) connecting two step-up transformers back-to-back, and (c) its equivalent circuit model.

consequently, the equivalent tank's Q will start decreasing. Hence, the PN-vs.-power trade-off will no longer be beneficial since the FoM will drop dramatically due to the Q-factor degradation.

Coupling N oscillators is an alternative way of trading off the power for PN since it avoids scaling the inductance down to impractically small values. It can theoretically improve PN by a factor of N compared to a single oscillator [90], [91]. Unfortunately, the oscillator size increases linearly, i.e., 4× larger area for just 6 dB of PN improvement.

In this work, we improve the phase noise by utilizing two 1:n transformers that are connected back-to-back [89], as shown in Fig. 4.1(b, c). The equivalent R_{in} and, thus, the oscillator PN are scaled down by a factor of $\sim(1+n^2)$ without sacrificing tank's Q-factor. Hence, PN improvement can potentially be much better than with the coupled oscillators (e.g., Fig. 4.1(a)) at the same die area. In addition, the C_2 and C_3 tuning capacitors, which are not directly connected to the primary of the first transformer, appear at the input of the transformer network via the scaling factor of n^2 and n^4 as can be realized from Fig. 4.1(c). This impedance transformation results in a significant reduction in the required value of all the capacitors (i.e., $\sum_i C_i$), which reduces the routing parasitics (both inductive and capacitive), and improves the tuning range and PN of the oscillator. Even though by increasing the transformer's turns ratio the tank input impedance will be reduced, the transformer Q-factor will not stay at the optimum level and will start dropping at some point [33]. It turns out that the turns ratio of n=2 can satisfy the aforementioned constraints altogether.

To sustain the oscillation of this differential tank, two transistors shall be added. Figure 4.2 illustrates the *preliminary* schematic and waveforms. Unfortunately, as gathered from Fig. 4.3, this structure suffers the same issues as the traditional class-B oscillator when the ideal current source is replaced with a tail bias transistor, M_T. The PN is ideally improved by 20 dB/dec through increasing the oscillation amplitude, provided the gm-devices $M_{1,2}$ operate in saturation

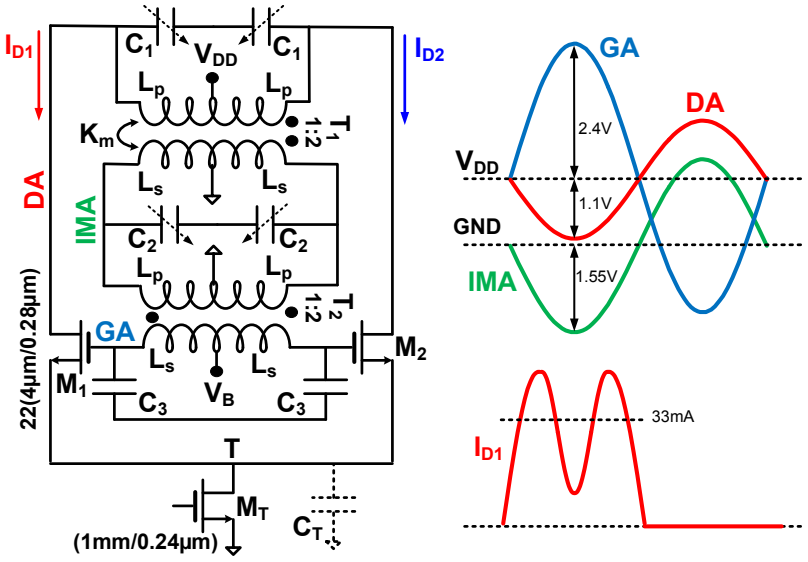


Figure 4.2: Preliminary oscillator schematic and its simulated voltage and estimated current waveforms at f_0=8 GHz, V_{DD}=1.2 V, I_{DC}=33 mA, L_{eq}=80 pH and C_{eq}=4.95 pF.

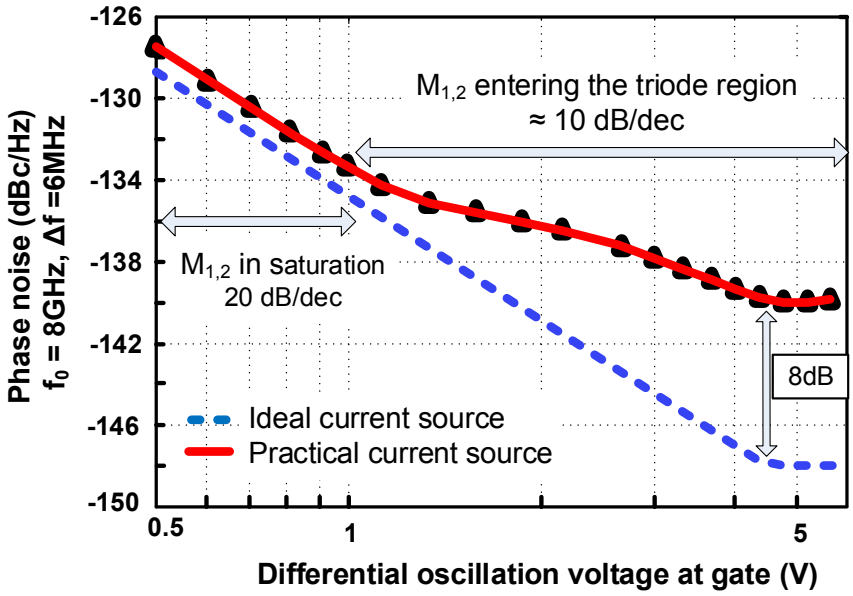


Figure 4.3: Simulated phase noise performance of the preliminary oscillator of Fig. 4.2 versus gate differential oscillation voltage for the ideal and real current sources.

over the entire period. However, the slope of PN improvement deviates from the ideal case when $M_{1,2}$ enter the triode region for a part of the oscillation period [27]. This problem is intensified especially when the oscillator operates at higher frequencies and larger I_{DC} (i.e $\geq$10 mA) is needed to satisfy the stringent spectral purity of the GSM standard [92]. Actually, the combination of the parasitic drain capacitance of the large-size M_T with the entering the triode region by $M_{1,2}$, will cyclically short-circuit the tank, thus degrading its equivalent Q-factor and oscillator PN [26].

Furthermore, the oscillation voltage should provide minimum V_{DSAT} across M_T throughout the entire period to keep it in saturation. Consequently, α_V becomes substantially less than 1, which translates to a significant PN penalty as clearly seen from (4.1). Larger M_T needs

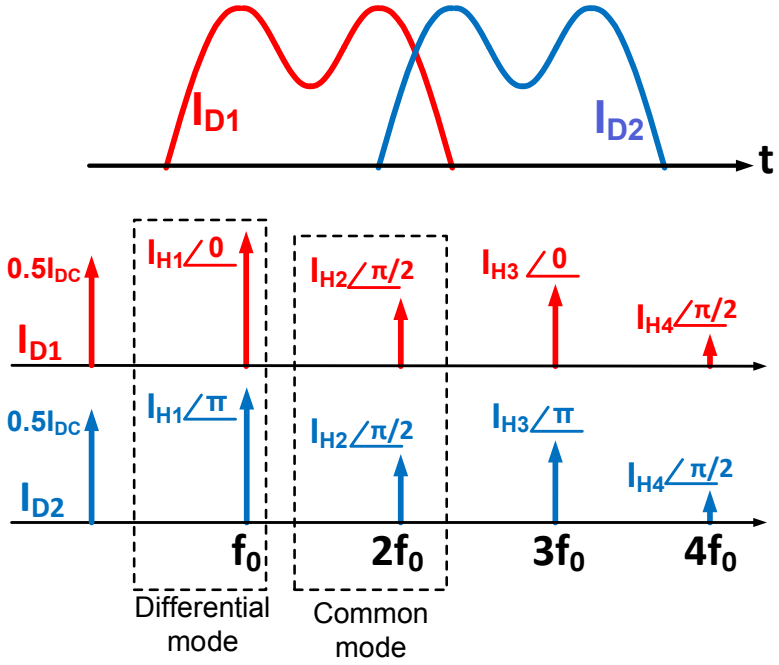


Figure 4.4: Drain current of $M_{1,2}$ devices of Fig. 4.2 in time and frequency domains.

lower V_{DSAT}, which would increase α_V. However, the tail transistor's effective thermal noise will increase significantly for the same I_{DC} [25]. As a consequence, the contribution of M_T to the PN could be larger than that of gm-devices, which translates to a significant increase of the oscillator NF and thus its PN [92]. In addition, the M_T parasitic capacitance, C_T, will also increase with the side effect of a stronger tank loading. On the other hand, the combination of the sinusoidal drain voltage, large C_T and the entering of triode region by $M_{1,2}$, will result in a dimple in the squarish shape of active device drain current (see Fig. 4.2) with a 10–20% reduction in α_I, and thus FoM of the oscillator [21], [92]. All the above reasons contribute to reducing the rate of PN improvement versus V_{osc} to about 10 dB/dec when $M_{1,2}$ enter the triode region for a part of the oscillation period. Hence, a huge 8 dB PN difference in Fig. 4.3 is observed between the ideal and real operation of the oscillator. Consequently, the proposed oscillator must not be sensitive to the excess gm-device noise in the triode intervals. It should also break the trade-off between α_V and NF.

4.3 Evolution Towards Class-F$_2$ Operation

Before introducing our proposed phase noise (PN) reduction technique, let us take a closer look at the harmonic component of the drain current I_D of the M_1 and M_2 gm-devices in Fig. 4.2. Ideally, I_D is a square wave containing fundamental and odd harmonics. The odd harmonics through M_1 and M_2 are 180° mutually out-of-phase and appear as differential-mode (DM) input signals for the tank. The I_D also contains even harmonics due to the large oscillation voltage, non-linearity of $M_{1,2}$ and large parasitic capacitance of M_T. However, the even harmonics through M_1 and M_2 are mutually in-phase with ±90° phase shift to their related odd harmonics, as shown in Fig. 4.4. Consequently, these even harmonics appear as a common-mode (CM) input for the tank. The conventional tank input impedance has only one peak at the fundamental

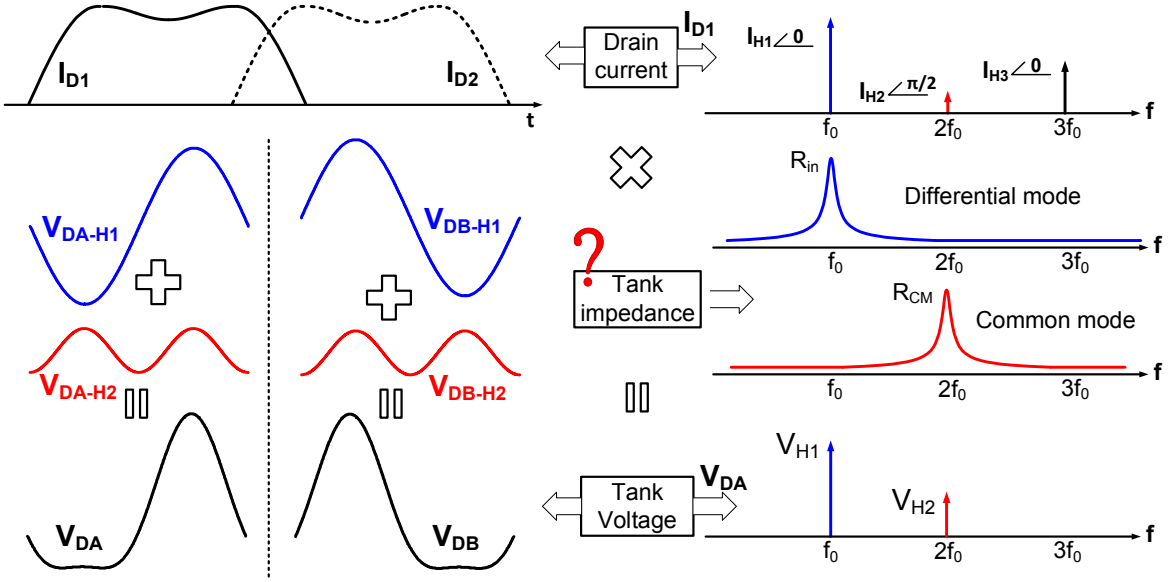


Figure 4.5: Proposed oscillator waveforms in time and frequency domains.

frequency ω_0. Therefore, the tank filters out the drain current harmonics and ultimately a sinusoidal voltage is seen across the tank. Now, suppose the tank offers an additional CM input impedance peak around the second harmonic (see Fig. 4.5). Then, the second harmonic of I_D is multiplied by the tank's CM input impedance to produce a sinusoidal voltage at $2\omega_0$ that is in quadrature to the fundamental oscillation voltage produced by the tank's DM impedance at ω_0. The combination of both waveforms creates the desired oscillation voltage around the tank, as shown in Fig. 4.5, thus justifying the class-F$_2$ designation.

$$V_{DA} = V_{DD} - V_{H1}\sin(\omega_0 t) - V_{H2}\sin\left(2\omega_0 t + \frac{\pi}{2}\right) \tag{4.3}$$

ζ_V is defined as the ratio of the second-to-first harmonic components of the oscillation voltage.

$$\zeta_V = \frac{V_{H2}}{V_{H1}} = \left(\frac{R_{CM}}{R_{in}}\right)\left(\frac{I_{H2}}{I_{H1}}\right) \tag{4.4}$$

where, R_{in} and R_{CM} are, respectively, the tank DM and CM impedance magnitude at ω_0 and $2\omega_0$. Figure 4.6 illustrates the oscillation voltage and its related impulse sensitivity function (ISF) based on Eq. (38) in [31] for different ζ_V values. Clearly, ζ_V should be 0.3 to have the widest flat span in the tank's oscillation voltage. The Γ^2_{rms} is 0.35 for ζ_V=0.3 compared to 0.5 for the traditional oscillator, which leads to a 1.5 dB PN and FoM improvements. Furthermore, ISF is negligible when the gm-devices work in the triode region and inject the most thermal noise into the tank. Consequently, the oscillator FoM improvement should be larger than that predicted by just the ISF_{rms} reduction. More benefits of the class-F$_2$ operation will be revealed in following sections.

The argument related to Fig. 4.5 suggests the creation of an additional CM input impedance peak at the second harmonic of main differential resonance. Incidentally, the proposed step-up 1:2 transformer acts differently to the CM and DM input signals. Fig. 4.7(a) illustrates the induced current at the transformer's secondary when the primary winding is excited by a differential signal. All induced currents circulate in the same direction at the transformer's

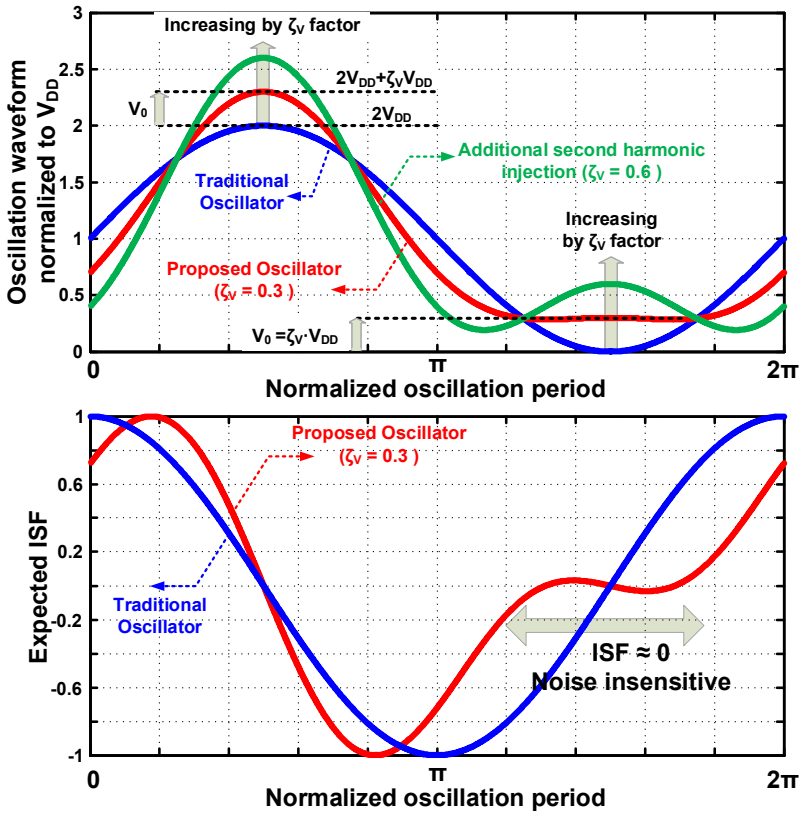


Figure 4.6: Effect of adding 2nd harmonic in the oscillation voltage waveform (top), and its expected ISF based on Eq. (38) in [31] (bottom).

secondary to satisfy Lenz's Law. Consequently, the induced currents add constructively, which leads to a strong inter-winding coupling factor ($k_m \geq 0.7$). However, when the transformer's primary is excited by a CM signal (Fig. 4.7(b)), the induced currents at the right-hand and left-hand halves of the transformer's secondary winding circulate in opposite directions thus largely canceling each other. The residual current results in a very small $k_m \leq 0.2$ for the CM excitation. Consequently, the concept of using two modes of a transformer for waveform shaping (proposed in [93] for a power amplifier) will be adopted here to realize the special tank input impedance of Fig. 4.5. Note that an equivalent lumped-element model in [33], [94] cannot simultaneously cover both CM and DM types of behavior, and would produce wrong results. Hence, we suggest to utilize the transformer's S-parameters and PSS analysis to simulate the proposed class-F$_2$ oscillator.

Figure 4.8 shows the proposed tank of a class-F$_2$ oscillator. The C_{1d} and C_3 are intentionally chosen as fixed capacitors while the DM and CM resonant frequencies are tuned by C_{1c} (fine) and C_2 (coarse). The DM main resonant frequency is

$$f_{1d} = \frac{1}{2\pi\sqrt{L_{eq}C_{eq}}} \approx \frac{1}{2\pi\sqrt{\left(\frac{L_p}{1+n^2}\right)(C_{1c}+C_{1d}+C_2n^2+C_3n^4)}} \tag{4.5}$$

The inductance reduction and capacitance multiplication factors of the dual-transformer tank are directly contained in (4.5). The CM input signal can neither see the second transformer nor C_2 & C_3 due to negligible $k_{m(CM)}$. In addition, differential capacitors also act as open circuit

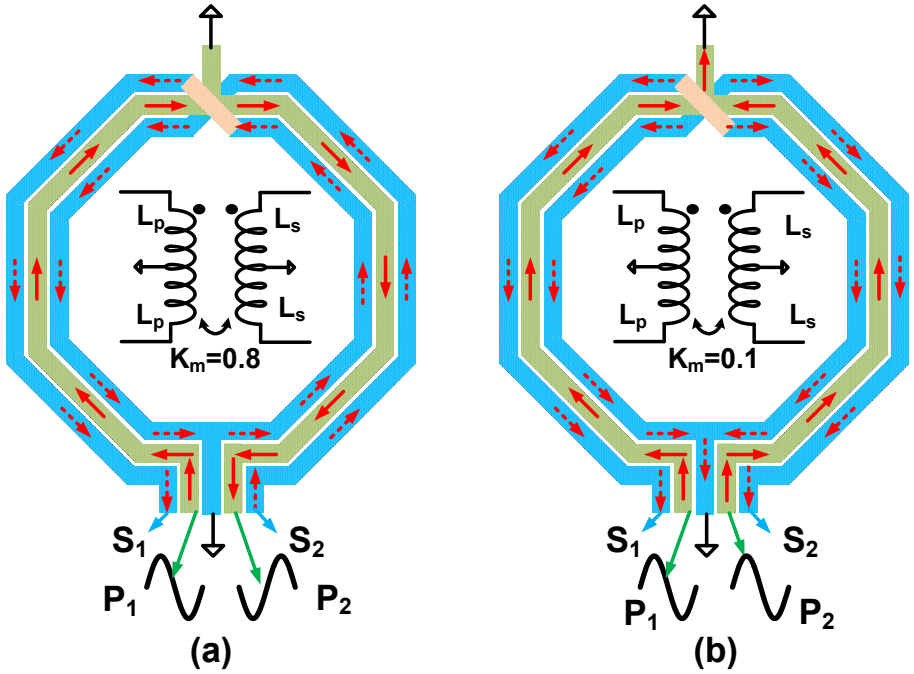


Figure 4.7: Transformer behavior in (a) differential-mode, and (b) common-mode excitations.

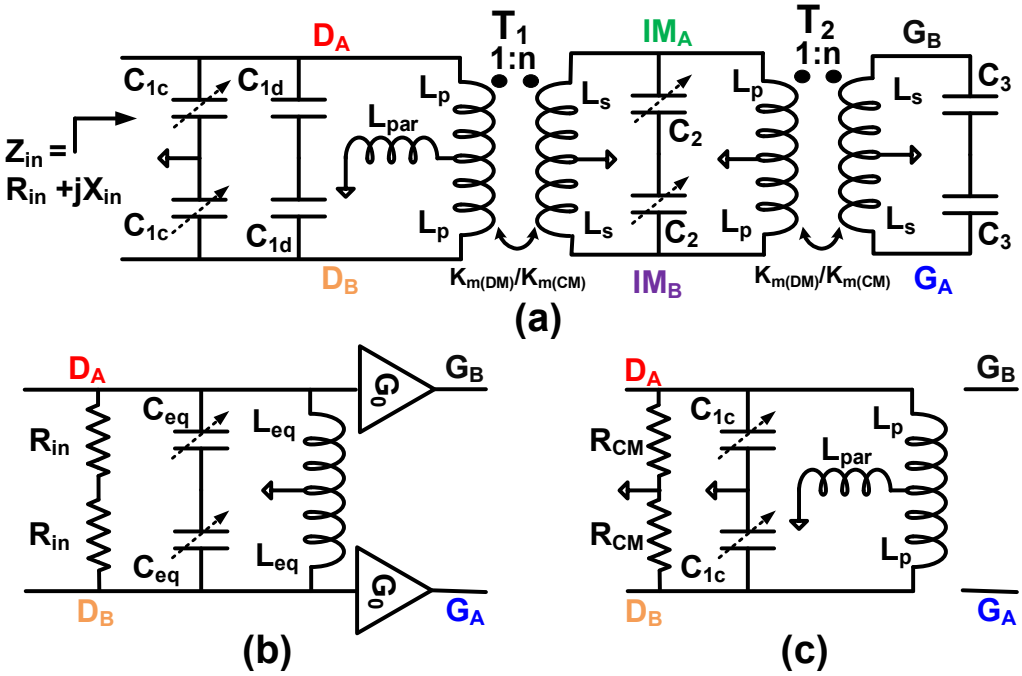


Figure 4.8: Proposed transformer-based resonator: (a) schematic, (b) its simplified equivalent differential-mode circuit ($k_{m(DM)} \approx 1$), (c) simplified tank schematic for common-mode input signals ($k_{m(CM)} \approx 0$).

for the CM signals. Consequently, the tank's CM resonant frequency is

$$f_{1c} = \frac{1}{2\pi\sqrt{L_{cm}C_{1c}}} \approx \frac{1}{2\pi\sqrt{(L_p + 2L_{par})\,C_{1c}}}. \tag{4.6}$$

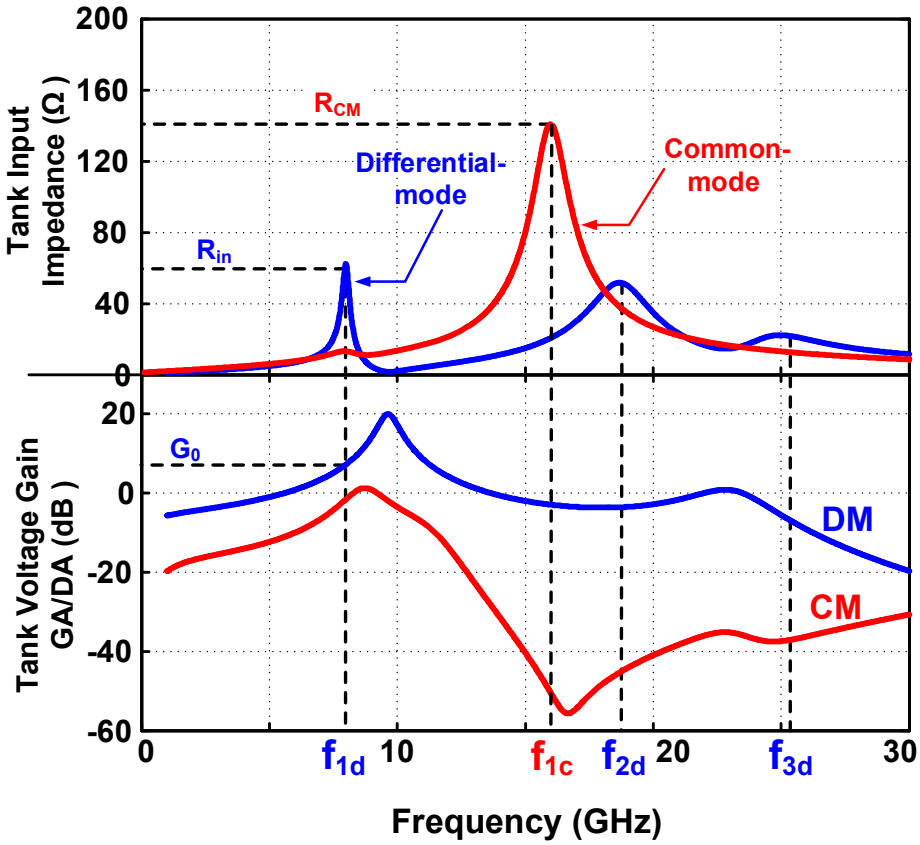


Figure 4.9: Simulated characteristics of the transformer-based tank of Fig. 4.8: (top) magnitude of input impedance Z_{in}; (bottom) tank voltage gain between gate and drain of core devices.

There is no tank impedance scaling for the CM excitation. Hence, the CM input impedance peak should be higher than the DM peak, as clearly seen from Fig. 4.9 (top). To operate properly, CM-to-DM resonance ratio must be adjusted to 2:

$$\zeta_f = \frac{f_{1c}}{f_{1d}} = \sqrt{\frac{L_p}{L_p + 2L_{par}} \cdot \frac{C_{1c} + C_{1d} + C_2 n^2 + C_3 n^4}{C_{1c}\,(1+n^2)}} = 2. \tag{4.7}$$

As a consequence, the frequency tuning requires a bit different consideration than in the class-B oscillators. Both C_{1c} and C_2 must, at least at the coarse level, be changed simultaneously to satisfy (4.7) such that f_{1c} coincides with $2f_{1d}$. This adjustment is entirely a function of the ratio of the tuning capacitors, which is precise thus making ζ_f largely independent from process, voltage and temperature (PVT) variations.

Let us now consider the required accuracy of this ratio ζ_f. The transformer and switching capacitors are designed based on maximum Q-factor at the operating frequency f_{1d}. The tank Q-factor drops at least 3× at $f_{1c} = 2f_{1d}$. Consequently, the tank CM impedance bandwidth is very wide, as seen in Fig. 4.9. Therefore, the oscillator is less sensitive to the position of f_{1c} and thus the tuning capacitance ratio. A realistic 5% error in ζ_f has no significant adverse effects on the oscillator waveform and thus its PN.

The schematic and waveforms of the proposed oscillator are shown in Figs. 4.10 and 4.11. Even though the second harmonic injection reduces the drain oscillation voltage by V_0 during the negative clipping interval, it increases its positive peak by V_0 (see Fig. 4.6(a)). It means the drain oscillation span is shifted from 0-to-2V_{DD} in the traditional oscillator to V_0-to-(2V_{DD}+V_0)

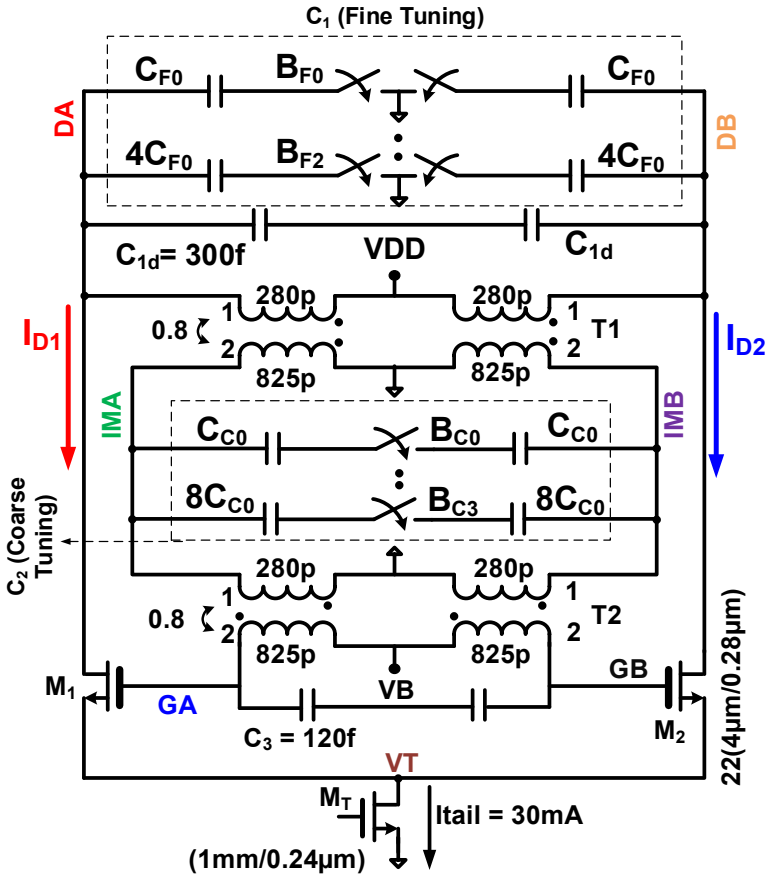


Figure 4.10: Proposed transformer-based class-F$_2$ oscillator schematic.

in the proposed class-F$_2$ operation. Hence, the larger current source voltage headroom and lower noise factor are achieved without compromising the oscillation amplitude. Furthermore, the V_0 headroom also reduces the dimple in the core-device drain current (compare Figs. 4.2 and 4.11), which helps the class-F$_2$ current efficiency to be closer to the ideal value of $2/\pi$.

Figure 4.9 illustrates the tank CM/DM input impedance and passive voltage gain between the gate and drain of $M_{1,2}$ versus frequency. Unfortunately, the tank exhibits two other undesired DM resonant frequencies (f_{2d}, f_{3d}) due to imperfect k_m of the two transformers that create two leakage inductances [33]. Consequently, the circuit loop must guarantee the oscillation only at the desired DM resonance, f_{1d}. Although CM demonstrates much larger input impedance peak, the two transformers effectively reject (attenuate by >40 dB) the CM signals. The root-locus plot in Fig. 4.12 illustrates the DM pole movements toward zeros for different oscillator loop trans-conductance gains G_M. The first and third frequency conjugate pole pairs (ω_{1d} , ω_{3d}) move into the right-hand plane with increasing the absolute value of G_M, while the second conjugate pole ω_{2d} is pushed far away from the imaginary axis. This guarantees that the oscillation will not happen at ω_{2d}. Furthermore, it can be shown that ω_{3d} poles move to much higher frequencies with much lower input impedance peak and tank voltage gain if enough differential capacitance is located at T_1 primary windings. It justifies the existence of the non-switchable differential capacitor C_{1d}. Consequently, the loop gain will not be enough to satisfy the Barkhausen criterion for ω_{3d}.

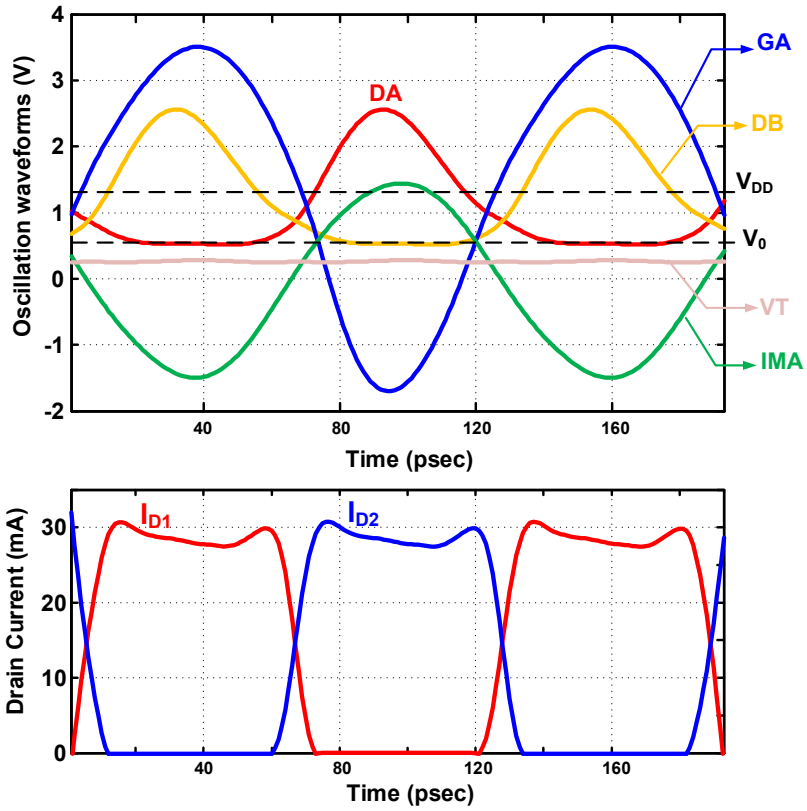


Figure 4.11: Simulated oscillation waveforms of the class-F_2 oscillator at V_{DD}=1.2 V and I_{DC}=29 mA: (top) oscillation voltage of different circuit nodes, (bottom) core transistors drain current.

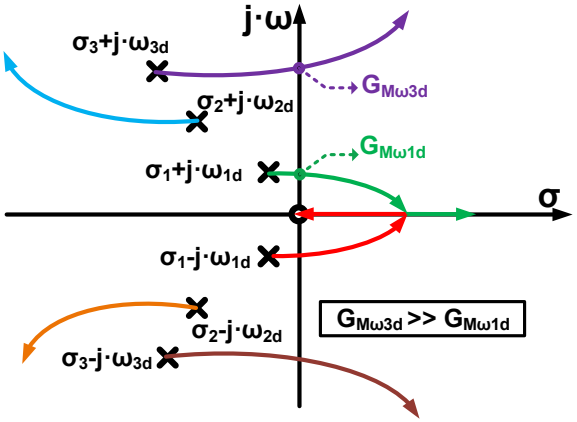


Figure 4.12: Root-locus plot of the class-F_2 oscillator.

4.4 Phase Noise Mechanism in Class-F_2 Oscillator

According to the linear time-variant (LTV) model [31], the phase noise of an oscillator at an offset frequency $\Delta\omega$ from its fundamental frequency ω_0 is expressed as

$$\mathcal{L}(\Delta\omega) = 10\log_{10}\left(\frac{\sum_i N_{L,i}}{2\, q_{max}^2\,(\Delta\omega)^2}\right) \tag{4.8}$$

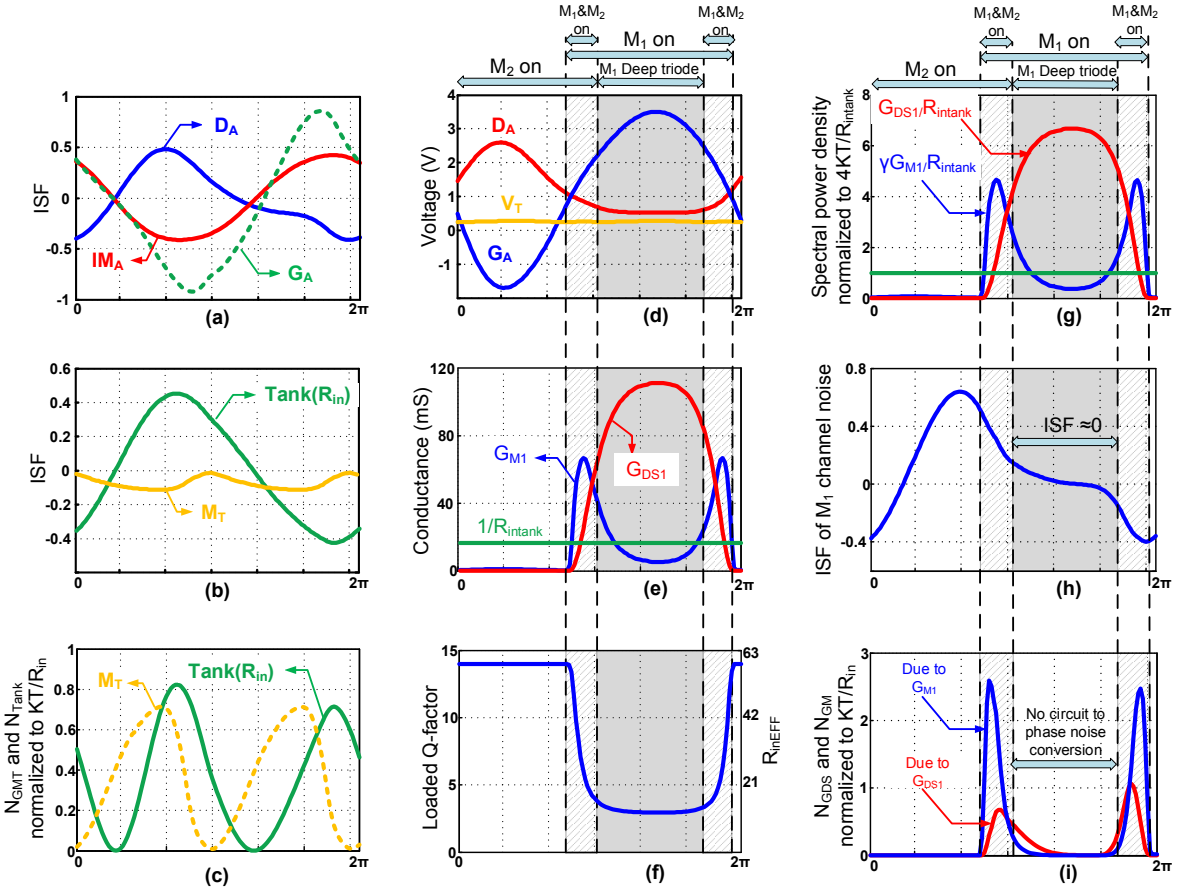


Figure 4.13: Mechanisms of circuit-to-phase noise conversion across the oscillation period in the class-F$_2$ oscillator: (a) simulated ISF of different tank nodes, (b) equivalent ISF in the simplified oscillator schematic of Fig. 4.14, (c) simulated effective power spectral density of the oscillator's noise sources normalized to KT/R$_{in}$, (d) oscillation waveforms and operation region of M$_{1,2}$, (e) transconductance and channel conductance of M$_1$, (f) loaded Q-factor and effective parallel input resistance of the tank, (g) power spectral density of M$_1$ noise sources normalized to 4KT/R$_{in}$, (h) simulated ISF function of M$_1$ channel noise, (i) simulated effective power spectral density of different noise sources of M$_1$ normalized to KT/R$_{in}$.

where, q_{max}=C_{eq}·V_{osc} is the maximum charge displacement across the tuning capacitors and V_{osc}=α_I·R_{in}·I_{DC} is the single-ended oscillation amplitude at the drain of gm-devices. The $N_{L,i}$ in (4.8) is the effective noise power produced by i^{th} device given by

$$N_{L,i} = \frac{1}{2\pi}\int_0^{2\pi} \Gamma_i^2(\omega_0 t)\ \overline{i_{n,i}^2(\omega_0 t)}\, d\,(\omega_0 t) \tag{4.9}$$

where $\overline{i_{n,i}^2}$ is the white noise current density of the ith noise source, Γ_i is its corresponding ISF function. Obtaining the ISF of various oscillator nodes is the first step in calculating the oscillator's PN. The ISF functions are simulated by injecting a 20 femto-coulomb charge (Δq) throughout the oscillation period and measuring the resulting time shifts, Δt_i.

$$\Gamma_i = \omega_0 \cdot \Delta t_i \cdot \frac{q_{max}}{\Delta q} \tag{4.10}$$

Figure. 4.13(a) illustrates the ISF of various tank nodes. The soft clipping reduces by 30%

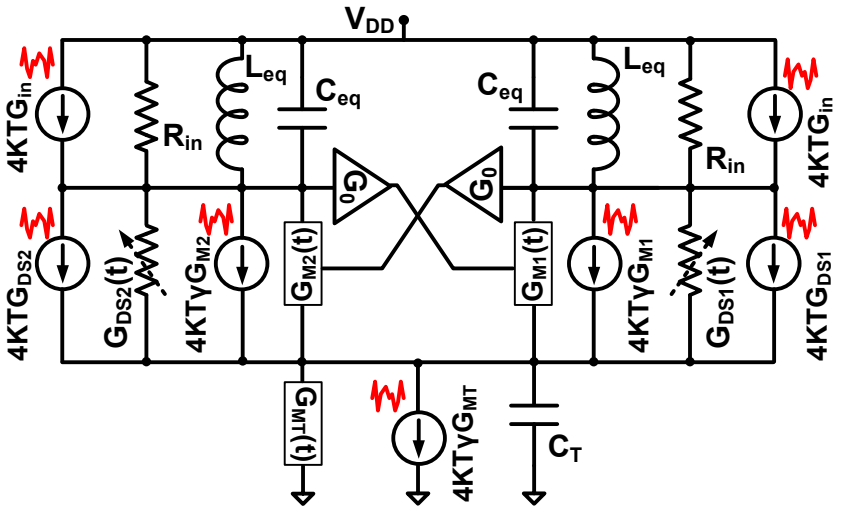


Figure 4.14: Simplified noise source model of the class-F_2 oscillator.

the effect of losses on the oscillator PN due to single-ended switchable C_{1c}[1] and T_1 primary windings. However, ISF functions of the T_1 secondary and T_2 primary/secondary winding noise sources (including C_2 and C_3) are not improved due to the sinusoidal (i.e., conventional) waveforms at $IM_{A,B}$ and $G_{A,B}$ nodes. Figure 4.13(a) indicates that $G_{A,B}$ are the most sensitive nodes. Hence, C_3 is constructed as a fixed MoM capacitor and the transformer was designed with a goal of maximizing Q-factor of the secondary winding.

To calculate a closed-form PN equation, the proposed oscillator model is simplified in Fig. 4.14. The $G_{DS1,2}(t)$ represent the channel conductance of $M_{1,2}$. The $G_{M1,2}(t)$ and $G_{MT}(t)$ model the transconductance gain of $M_{1,2}$ and M_T, respectively. The original tank is pruned to a parallel L_{eq}, C_{eq}, R_{in} with noiseless voltage gain of G_0 (see Fig. 4.8(b)). The simplified tank's equivalent ISF can be roughly estimated by an average of the tank's contributing ISF functions of Fig. 4.13(a) and is shown in Fig. 4.13(b) as green curve. The effective noise power of the tank is illustrated in Fig. 4.13(c) as green curve and its average power is approximated by

$$N_{Tank} = \frac{1}{\pi}\int_0^{2\pi} \frac{4KT}{R_{in}}\Gamma_{tank}^2(\omega_0 t)d(\omega_0 t) \approx 0.8\frac{KT}{R_{in}} \tag{4.11}$$

Consequently, the soft clipping reduces N_{Tank} by 20% compared to the traditional oscillator.

The effects of noise on the oscillator PN due to channel conductance (G_{DS}) and transconductance gain (G_M) of $M_{1,2}$ transistors are separately investigated. Figure 4.13(d) illustrates various operational regions of $M_{1,2}$ across the oscillation period. When $M_{1,2}$ are not turned off, they work mainly in the deep triode region where they exhibit a few ohms of channel resistance, as infdicated in Fig. 4.13(e). Consequently, the combination of the large parasitic capacitance of M_T with low channel resistance of $M_{1,2}$ in this deep triode region makes a low impedance path between the tank and ground. The literature interprets this as the tank loading event and defines implicit parameters such as *effective* tank Q-factor (Q_{eff}) and input parallel resistance (R_{ineff}) to justify the oscillator phase noise degradation due to this phenomenon. As shown in Fig. 4.13(f), the tank Q_{eff} and R_{ineff} drop 4–5× when $M_{1,2}$ operate in the deep triode. These

[1]The single-ended switchable capacitor is used to adjust the CM resonant frequency. However, its Q-factor is almost half that of the differential structure for the same C_{max}/C_{min}. The soft clipping largely compensates the effect of additional losses due to its lower Γ_{rms} value.

"effective" parameters merely indicate that more noise is injected then into the tank. However, they do not ordain how much of that circuit noise converts to phase noise, especially when the drain oscillation wave is not conventionally sinusoidal.

The proper approach should be based on the channel conductance noise power *and* its related ISF. If we had an ideal current source, $M_{1,2}$ noise would be injected to the tank only during the commutating time (hachure areas in Fig. 4.13(e-g)). At the remaining part of oscillation period, one transistor is off and other one is degenerated by the ideal current source and thus noiseless. However, the output impedance of a practical current source is low for such a high I_{DC}=30 mA and f_0=8 GHz. Consequently, $M_{1,2}$ can inject significant amount of noise to the tank when they operate in deep triode region outside the commutating time (i.e., gray area in Fig. 4.13(g)). Note that gm-devices generate ∼7× higher amount of noise compared to the tank loss in the gray area, which can potentially increase the phase noise of the oscillator. However, the ISF of channel noise of $M_{1,2}$ is very small in that time span as shown in Fig. 4.13(h). Hence, the excessive transistor channel noise (or excessive loaded tank noise of the conventional approach) cannot convert to phase noise. Consequently, the effective noise power of the gm-device channel conductance is negligible, as illustrated in Fig. 4.13(i), and its average power is approximated by

$$N_{GDS} = \frac{1}{\pi}\int_0^{2\pi} 4KTG_{DS1}(\omega_0 t)\cdot\Gamma_{M1}^2(\omega_0 t)\cdot d(\omega_0 t) \approx \frac{KT}{R_{in}}\cdot(0.25) \tag{4.12}$$

Note that N_{GDS} is at least 4× larger for the traditional oscillator, especially when a large α_V is needed [43].

Fig. 4.13(e) shows M_1 transconductance gain G_{M1} across the oscillation period. To sustain the oscillation, the combination of the transformers' passive voltage gain (G_0) and effective negative transconductance of the gm-devices needs to overcome the tank and $M_{1,2}$ channel resistance losses. Consequently,

$$G_{M1EF} = \frac{1}{G_0}\cdot\left(\frac{1}{R_{in}} + G_{DS1EF}\right) \tag{4.13}$$

where G_{DS1EF} describes the effective value of the instantaneous conductance $G_{DS1}(t)$ of $M_{1,2}$ [43]. It can be shown that G_{DS1EF} could be as large as $1/R_{in}$ when the oscillator is biased near the voltage limited region [21]. Therefore, the effective noise due to G_M of core transistors can be calculated by

$$\begin{aligned} N_{GM} &= \frac{1}{\pi}\int_0^{2\pi} 4KT\gamma_{M1}G_{M1}(\omega_0 t)\cdot\Gamma_{M1}^2(\omega_0 t)\cdot d(\omega_0 t) \\ &\approx \frac{KT}{R_{in}}\frac{\gamma_{M1}}{G_0}\cdot(1 + R_{in}\cdot G_{DS1EF}) \\ &\approx \frac{KT}{R_{in}}\cdot\left(\frac{2\gamma_{M1}}{G_0}\right) \end{aligned} \tag{4.14}$$

Eq. 4.14 indicates that the second harmonic injection (i.e., class-F_2 operation) demonstrates no benefit for N_{GM} but the transformers' voltage gain still offers significant benefits.

To estimate the PN contribution of M_T, its transconductance should be calculated first.

$$G_{MT} = \frac{2I_{DC}}{V_{gs(M_T)} - V_{th}} \approx \frac{2I_{DC}}{V_T} \tag{4.15}$$

where, V_T is the overdrive voltage of M_T equal to the drain-source voltage. The clipping voltage level is

$$V_0 = V_{DD}\left[1 - \alpha_V\left(1 - \zeta_V\right)\right] \tag{4.16}$$

By dedicating a half of V_0 headroom to M_T,

$$G_{MT} = \frac{4I_{DC}}{V_0} \approx \frac{4I_{DC}}{V_{DD}\left(1 - \alpha_V\left(1 - \zeta_V\right)\right)} \tag{4.17}$$

By substituting I_{DC} with $V_{osc}/(\alpha_I R_{in})$ in (4.17),

$$G_{MT} = \frac{4}{\left(1 - \alpha_V\left(1 - \zeta_V\right)\right) R_{in}\alpha_I}\left(\frac{V_{osc}}{V_{DD}}\right) = \frac{1}{R_{in}}\frac{4\alpha_V}{\left(1 - \alpha_V\left(1 - \zeta_V\right)\right)\alpha_I} \tag{4.18}$$

As discussed earlier, α_I and α_V could be as large as 0.6 and 0.9 in the proposed oscillator and optimum ζ_V is about 0.3. Hence, (4.18) is simplified to $G_{MT} \approx 15/R_{in}$. As revealed by Fig. 4.13(b, orange), $\Gamma_{MT,rms}$ is only 0.08 due to relatively large V_T of the class-F_2 operation. Consequently,

$$N_{MT} = \frac{1}{2\pi}\int_0^{2\pi} 4KT\gamma_{MT}G_{MT}(\omega_0 t)\cdot\Gamma_{MT}^2(\omega_0 t)\cdot d(\omega_0 t) \approx \frac{KT}{R_{in}}\cdot(0.4\gamma_{MT}) \tag{4.19}$$

The contribution of M_T to the PN is less than that of the tank and is about 20% of the total. This share could easily be higher than 50% for the traditional oscillator at the same α_V and I_{DC} as discussed in [92], [26]. Finally, the total oscillator effective noise power (N_T) and noise factor (NF_{Total}) are given by

$$N_T \approx \frac{KT}{R_{in}}\cdot NF_{Total}, \qquad NF_{Total} \approx \left(1.05 + \frac{2\gamma_{M1}}{G_0} + 0.4\gamma_{MT}\right) \tag{4.20}$$

Eq. (4.20) indicates the effective noise factor of the proposed class-F_2 oscillator is very close to the ideal value of $(1+\gamma)$ despite the aforementioned practical issues. The phase noise can easily be calculated by replacing (4.20) in (4.8). The oscillator FoM normalizes the PN performance to ω_0 and P_{DC}, yielding

$$FoM = -10\log_{10}\left(\frac{10^3\cdot KT}{2Q_t^2\alpha_I\alpha_V}\cdot NF_{Total}\right). \tag{4.21}$$

Table 4.1 verifies the solidity of the presented phase noise analysis by comparing the results of SpectreRF^{TM} PSS, Pnoise simulations with the derived theoretical equations. The expressions estimate the oscillator PN and share of different noise sources with an acceptable accuracy.

It is also instructive to compare in Table 4.2 the benefits and drawbacks of the two flavors of class-F operation. Intuitively, the third-harmonic injection in class-F_3 [21] demonstrates a pseudo-square waveform with smaller ISF_{rms} value and shorter commutating time. Consequently, it offers lower NF_{Tank} and NF_{GM}. On the other hand, class-F_2 operation provides larger voltage overhead for the gm-devices and tail current transistor without sacrificing the oscillator α_V. Hence, it exhibits better NF_{MT}, NF_{GDS} and α_V. As expected, the effective noise factor and FoM of both topologies turns out to be identical. However, this implementation of class-F_2 automatically scales down the tank input parallel resistance and thus offers lower PN at price of larger area and slightly lower Q-factor due to the inter-connection of the two transformers.

Table 4.1: Comparison between the results of SpectreRF PSS, Pnoise simulation and theoretical equations at 8 GHz carrier for V_{DD}=1.2 V, R_{in}=60 Ω, L_{eq}=80 pH, γ_{MT}=1.3 and $\gamma_{M1,2}$=1

	Theoretical equations		**SpectreRF simulation**	
	Value	**Share**	**Value**	**Share**
$\mathbf{N_{Tank}}$	$5.50{\cdot}10^{-23}$ V^2/Hz	31%	$4.71{\cdot}10^{-23}$ V^2/Hz	28.4%
$\mathbf{N_{M1,2} = N_{GDS} + N_{GMT}}$	$8.63{\cdot}10^{-23}$ V^2/Hz	48.8%	$8.78{\cdot}10^{-23}$ V^2/Hz	53%
$\mathbf{N_{MT}}$	$3.59{\cdot}10^{-23}$ V^2/Hz	20.2%	$3.08{\cdot}10^{-23}$ V^2/Hz	18.6%
$\mathbf{N_T = N_{Tank} + N_{M1,2} + N_{MT}}$	$17.72{\cdot}10^{-23}$ V^2/Hz	100%	$16.57{\cdot}10^{-23}$ V^2/Hz	100%
$\mathbf{q_{max}}$ **(coulumbs)**	$5.34{\cdot}10^{-12}$		$5.34{\cdot}10^{-12}$	
Phase noise @10MHz	-151dBc/Hz		-151.33dBc/Hz	

Table 4.2: Comparison between two flavors of class-F oscillator for the same carrier frequency=8 GHz, V_{DD}=1.2 V, tank Q-factor=14, Δf=10 MHz and R_P=240 Ω.

	Expression	**Class-F_3** [21]	**Class-F_2**
α_I	I_{ω_0}/I_{DC}	0.6	0.6
α_V	V_{osc}/V_{DD}	0.8	0.9 (✓)
$\mathbf{NF_{Tank}}$	$N_{Tank}/(KT/R_{in})$	0.7 (✓)	0.8
$\mathbf{NF_{GDS}}$	$N_{GDS}/(KT/R_{in})$	0.3	0.25 (✓)
$\mathbf{NF_{GM}}$	$N_{GM}/(KT/R_{in})$	$\approx 0.7\gamma_{M1}$ (✓)	$\approx \gamma_{M1}$
$\mathbf{NF_{GMT}}$	$N_{GMT}/(KT/R_{in})$	$\approx 0.5\gamma_{MT}$	$\approx 0.4\gamma_{MT}$ (✓)
$\mathbf{NF_{Total}}$		3.7dB (✓)	4.1dB
FoM	$\approx -10\log_{10}\left(\frac{KT}{2Q_t^2\ \alpha_I\ \alpha_V}NF\right)$	192.9dB (✓)	192.9dB (✓)
$\mathbf{R_{in}}$		$\approx R_p = 240\Omega$	$\approx R_p/(1+n^2) = 60\Omega$ (✓)
$\mathbf{P_{DC}}$	$\left(\frac{V_{DD}^2}{R_{in}}\frac{\alpha_V}{\alpha_I}\right)$	8mW	36mW
Phase noise	$\approx 10\log_{10}\left(\frac{KT}{2Q_t^2\ P_{DC}}\frac{1}{\alpha_I\ \alpha_V}NF\left(\frac{\omega_0}{\Delta\omega}\right)^2\right)$	-144 dBc/Hz	-150.5 dBc/Hz (✓)

4.5 Experimental Results

This oscillator work targets GSM-900 MHz and DSC-1800 MHz base-station PN requirements. Electromagnetic (EM) simulations reveal that the tank Q-factor would be slightly (i.e., ∼10%) better at 8 GHz as compared to 4 GHz for the same R_{in} and tuning range. However, the 1/f noise up-conversion would be more severe at 8 GHz due to a larger share of the non-linear C_{gs} of gm-devices to the total tank's capacitance. Furthermore, the output impedance of the current source is lower at higher frequencies, which would lead to higher PN penalty due to the tank loading. Consequently, there seems to be altogether no clear performance advantage of the 8 GHz over 4 GHz operation. Considering the fact that the proposed oscillator has two transformers, the 8 GHz center frequency was chosen mainly to save die area.

The proposed class-F_2 oscillator, whose schematic was shown in Fig. 4.10, was realized in TSMC 1P7M 65-nm CMOS process technology. The die photograph is shown in Fig. 4.15. The oscillator core die area is 0.2 mm^2. The differential transistors are thick-oxide devices of 22(4-μm/0.28-μm) dimension. However, the tail current source M_T is implemented as a standard

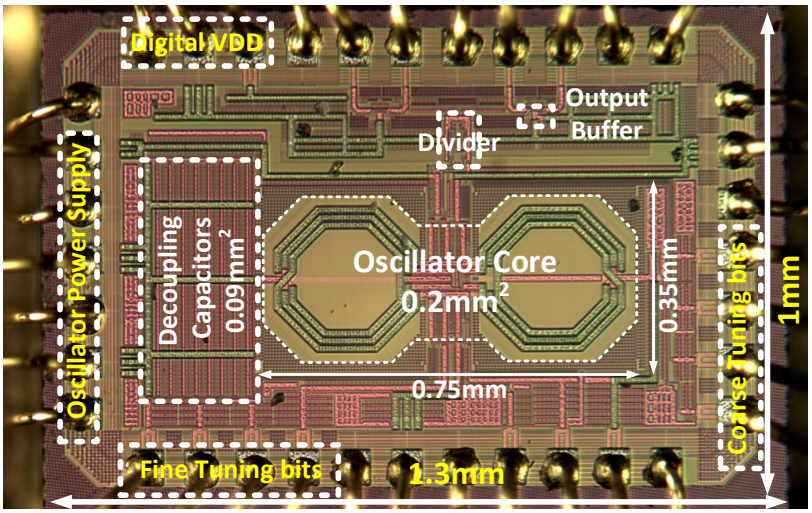


Figure 4.15: Die photograph of the class-F_2 oscillator.

1-mm/0.24-μm thin-oxide (t_{ox}=2.6 nm) device. Note that the thin oxide device produces lower 1/f noise corner than the thick one at the same area [95]. The aluminum capping layer (1.45 μm), which is intended to cover bond-pads, is strapped to the ultra-thick top copper layer (3.4 μm) to form the windings and improve the transformer's primary and secondary Q-factor to 14 and 20, respectively, at 8 GHz. The transformer's primary and secondary differential self-inductance is 560 pH and 1650 pH, respectively, with the DM and CM magnetic coupling factors of 0.8 and 0.15, respectively.

Four differential switched MOM capacitors $B_{C0}-B_{C3}$ with the resolution of 40 fF placed across T_1 secondary realize coarse tuning bits (C_2), while the fine control bits $B_{F0}-B_{F2}$ with LSB of 20 fF adjust ω_c to near $2\omega_{1d}$ to satisfy (4.7) and thus the class-F_2 operation. The effective C_{max}/C_{min} of the switched capacitor structures is determined by the strong tradeoff between the oscillator tuning range (TR) and tank Q-factor degradation due to the switch series resistance. The switched-capacitor's Q-factor is about 45 for 25% TR at 8 GHz. Furthermore, the interconnections of the two transformers also increase the tank losses by 10%, resulting in an average Q-factor of 14 for the entire tank.

The supply voltage connects to the center tap of T_1 primary along with a 100 pF on-chip decoupling capacitor. The center tap of T_2 secondary is connected to the bias voltage V_B, which is fixed at V_{DD} to minimize the number of supply domains and to guarantee safe oscillator start-up. The oscillator is very sensitive to noise at the $M_{1,2}$ gates (see Fig. 4.13(a)). Fortunately, no DC current is drawn from V_B so an RC filter of slow time constant is placed between V_{DD} and V_B to further reduce the bias voltage noise. Both T_1 secondary and T_2 primary windings center taps are connected to ground to avoid any floating nodes and make a return path for the negligible second harmonic current to improve the waveform symmetry.

The measured and simulated PN at 4.35 GHz (after the on-chip ÷2 divider) at 1.3 V and 32 mA current consumption are shown Fig. 4.16. The PN of -145 dBc/Hz at 3 MHz offset lies on the 20 dB/dec region, which extrapolates to -174.7 dBc/Hz at 20 MHz offset (normalized to 915 MHz) and meets the GSM TX mobile station (MS) requirements with a very wide 13 dB margin. The GSM/DCS "micro" base-station (BTS) and DCS "normal" BTS specs are met with a few dB of margin. These PN numbers are the *best ever* published at low V_{DD} (i.e., $\leq$

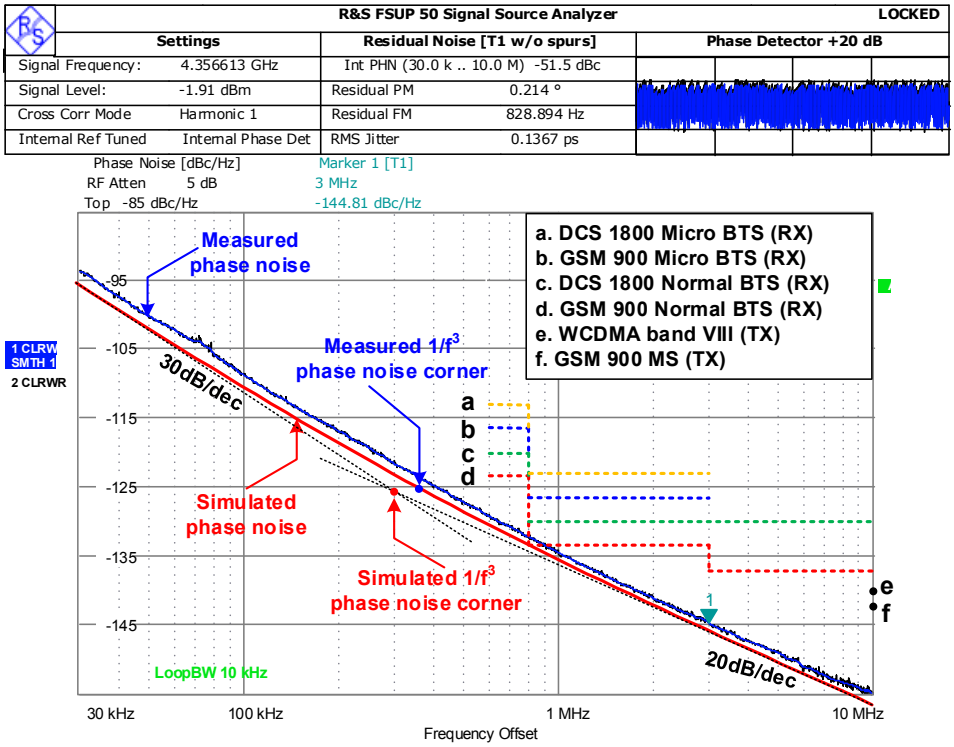


Figure 4.16: Measured (blue) and simulated (red) phase noise plots at 4.35 GHz, V_{DD}=1.3 V and P_{DC}=41 mW. Specifications (MS: mobile station, BTS: basestation) are normalized to the carrier frequency.

1.5 V). However, the toughest GSM base-station "normal" specifications at 800-to-900 kHz offset are within 1 dB of reach. The measured PN is just 1 dB higher than simulation in the 20 dB/dec region due to the power supply noise and additional tank loss caused by the routing of the tuning capacitors and dummy fill metals around the transformer.

The measured $1/f^3$ PN corner shows less than 100 kHz increase over the simulation and is ~350 kHz and ~250 kHz at the highest and lowest side of the tuning range, respectively. This excellent $1/f^3$ performance is achieved thanks to the following reasons: First, the 1/f noise of the tail current source can appear as a CM signal at T_1 primary and modulate the oscillation voltage. However, the T_1 transformer will effectively filter out this CM AM signal, thus preventing any AM-to-PM conversion at the C_2 switched capacitors and nonlinear C_{gs} of gm-devices. Second, the class-F_2 tank has two impedance peaks at the fundamental oscillation frequency and its 2nd harmonic. Hence, the 2nd harmonic of the drain current flows into a resistance of the tank instead of its capacitive part. It effectively reduces the 1/f noise upconversion to the $1/f^3$ phase noise due to Groszkowski phenomenon [24]. Third, the soft clipping effectively reduces the voltage variation of V_T, as shown in Fig. 4.11. Intuitively, it could reduce the DC and even-order coefficients of ISF at this node and thus alleviate the 1/f noise conversion of the tail current transistor.

The PN noise beyond the 10 MHz offset is dominated by thermal noise floor from the divider and buffers set at -162 dBc/Hz. The oscillator has a 19% tuning range from 7.2 to 8.7 GHz. Figure 4.17 shows the phase noise and FoM of the oscillator at 3 MHz offset across the tuning range (after the ÷2 divider). The average FoM is as high as 191 dBc/Hz and varies less than

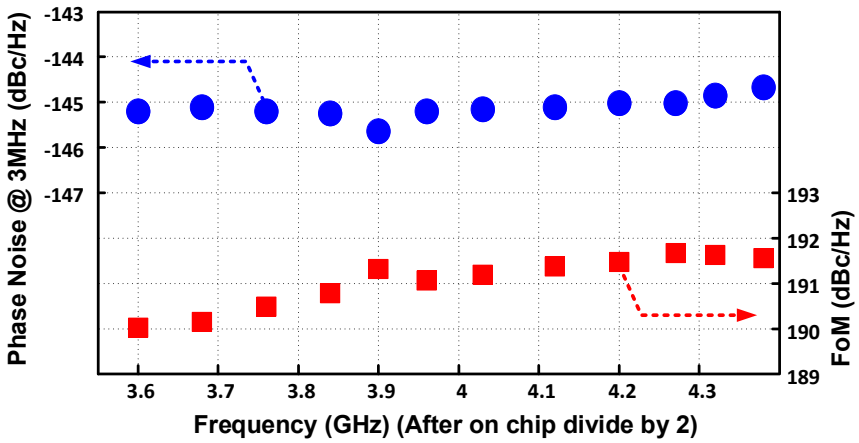


Figure 4.17: Measured phase noise and figure-of-merit (FoM) at 3 MHz offset versus carrier frequency.

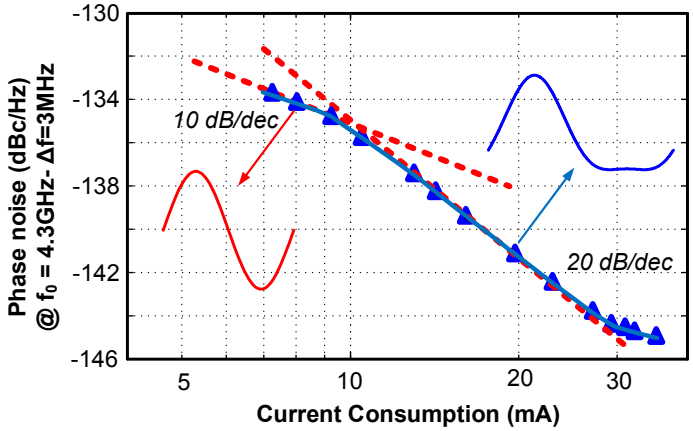


Figure 4.18: Measured phase noise at 3 MHz offset frequency from 4.3 GHz carrier versus the oscillator current consumption.

2 dB. The oscillator also reveals a very low frequency pushing of 42 and 22 MHz/V at the highest and lowest frequencies, respectively.

Figure 4.18 shows the PN performance versus its current consumption. The circuit cannot satisfy Barkhausen oscillation criterion at I_{DC}<7 mA. The oscillator phase noise is improved only by 10 dB/dec between 7 to 12 mA due to the drop in the oscillator current efficiency α_I and loading of the tank's Q-factor by the gm-devices entering the linear region. Note that even though the tank has an additional impedance at $2\omega_0$, the 2nd harmonic of the drain current is negligible and, consequently, the drain oscillation resembles a sinusoid. However, by further increasing the drain current, the soft clipping phenomenon appears where the tank loading and tail transistor noise effects are reduced significantly due to the class-F_2 operation. Consequently, PN improves by almost 20 dB/dec, which demonstrates a few dB of improvement compared to the traditional class-B operation (compare Figs. 4.3 and 4.18). Figure 4.18 also indicates that the circuit can sustain the oscillation even with 4× lower I_{DC} and thus G_{MEF}, which translates into sufficient margin for the oscillator start-up over PVT variations.

Table 4.3 summarizes the performance of the proposed class-F_2 oscillator and compares it with the best spectral purity state-of-the-art oscillators. Note that this oscillator demonstrates

Table 4.3: Comparison of state-of-the-art in ultra-low-phase noise oscillators.

	This Work	[91]	[96]	[21]	[26]	[28]	[49]
Technology	CMOS 65nm	CMOS 65nm	CMOS 65nm	CMOS 65nm	MOS 350μm	CMOS 55nm	BiCMOS 130nm
Supply voltage (V)	1.3	2.15	1.5	1.25	2.5	1.5	3.3
Frequency (GHz)	4.35[1]	4.07	3.92[1]	3.7[1]	1.2	3.35[1]	1.56
Tuning range (%)	19	19	10.2	25	18	31.4	9.6
PN at 3 MHz (dBc/Hz)	-144.8	-146.7	-147.7	-142.2	-152	-142	-150.4
Norm. PN[2] (dBc/Hz)	-158.3	-159.6	-157.2	-154.3	-154.8	-153.3	-155
Power consumption (mW)	41.6	126.8	48	15	9.25	27	290
FoM (dB)	191.8[3]	188.3	190.1	192.2	195	189	180
FoM$_T$[4] (dB)	197.4	193.4	190.3	200.2	200.7	199	179.7
Transformers/inductors count	2	2	2	1	2	1	1
Oscillator structure	Class F_2	Dual core Class-C	Hard clipping	Class F_3	Noise Filtering	Class B/C	Colpitts

[1]after on-chip ÷2 divider. [2]at 3 MHz offset frequency normalized to 915 MHz carrier.
[3] FoM drops to 191.5 dB by considering the divider power consumption of 2.6 mW.
[4]$\text{FOM}_\text{T} = |\text{PN}|+20\ \log_{10}((\text{f}_0/\Delta f)\ (\text{TR}/10))$ - $10\ \log_{10}(\text{P}_\text{DC}/1\text{mW})$

the best PN with the highest power efficiency at relatively low supply voltage while abiding by the process technology reliability rules. Only the dual-core class-C oscillator [91] offers better PN performance but at the price of 1.65× larger V_{DD}, 3× higher power consumption and 3 dB lower FoM or power efficiency.

4.6 Reliability of High-Swing RF Oscillators

RF oscillators are especially vulnerable to device and interconnect failures due to their large voltage and current peaks. The interconnect failure is mainly due to electromigration and can be easily cured by increasing the number of vias and widening high-current metal lines, which fortunately coincide with efforts to optimize the inductor Q-factor. However, the device failure becomes ever more serious and highly circuit dependent in scaled CMOS. Consequently, circuit designers of high-performance (thus, high-swing) RF oscillators must fully comprehended these reliability issues. Time dependent dielectric breakdown (TDDB) and hot carrier injection (HCI) are considered two main failure mechanisms, which limit the max oscillation amplitude [97].

The HCI degradation would occur when the drain current, I_{DS}, and drain-source voltage, V_{DS}, are large at the same time. Thanks to the transformer's voltage gain, the proposed oscillator V_{DD} is low enough such that V_{DS} of its gm-devices can be much less than the standard voltage of thick-oxide transistors (2.5 V) when they operate in on-state (see Fig. 4.11). Consequently, the proposed oscillator is not inherently vulnerable to HCI. However, the large oscillation swing applies a strong electric field across the gate-oxide of gm-devices (V_{DG}, V_{GS}), which can potentially reduce the long term reliability of the proposed oscillator due to TDDB [39].

The oxide breakdown stems from defects, such as electron traps, in the oxide structure. The rate of defect generation is almost proportional to the gate-oxide electric field and its leakage current density. This failure is a time-dependent statistically distributed phenomenon and is

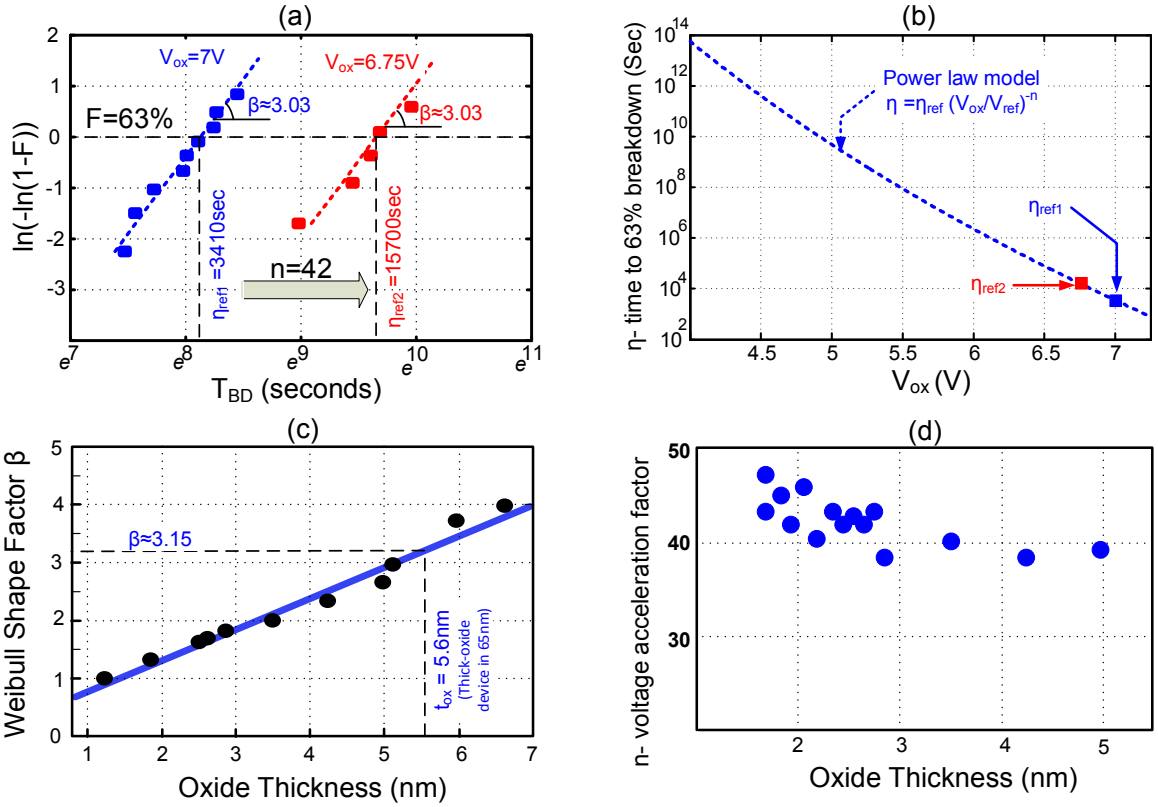


Figure 4.19: (a) Measured cumulative failure rate F versus breakdown time $\mathrm{T_{BD}}$ for 14 samples of a thick-oxide transistor (176μm/0.28μm) at room temperature, (b) the projected η value versus different gate-oxide stress voltage based on the measured η_{ref}, (c) Weibull slope versus gate oxide thickness extracted from measurement results in [14], (d) voltage acceleration versus gate oxide thickness extracted from measurement results in [98].

described by a well-known Weibull distribution:

$$F = 1 - e^{-\left(\frac{T_{BD}}{\eta}\right)^{\beta}} \longrightarrow \eta = T_{BD}\left(-ln\left(1-F\right)\right)^{-1/\beta} \tag{4.22}$$

where F is a cumulative failure probability and $\mathrm{T_{BD}}$ is a random variable for time-to-breakdown [14]. Both β and η are experimental parameters and defined as a Weibull shape slope and characteristic $\mathrm{T_{BD}}$ at $F = 63.2\%$, respectively. η is a strong function of the total gate oxide area ($\mathrm{A_{ox}}$), absolute junction temperature ($\mathrm{T_{ox}}$) and stress voltage across the gate oxide ($\mathrm{V_{ox}}$). The η is usually estimated by means of voltage and temperature acceleration models from results acquired at relatively short measurements to the required product lifetime (e.g., 10 years). It is shown in [14] that η for a given circuit with arbitrary characteristics ($\mathrm{A_{ox}}$, $\mathrm{V_{ox}}$ and $\mathrm{T_{ox}}$) can be extrapolated from the reference data (x_{ref}) by

$$\eta = \eta_{ref}\left(\frac{V_{ox}}{V_{ref}}\right)^{-n} e^{\frac{E_a}{K}\left(\frac{1}{T_{ox}}-\frac{1}{T_{ref}}\right)}\left(\frac{A_{ox}}{A_{ref}}\right)^{-1/\beta} \tag{4.23}$$

where, n and $\mathrm{E_a}$ are, respectively, voltage acceleration and thermal activity energy factors.

The above procedure is now applied to our proposed class-$\mathrm{F_2}$ oscillator to determine its $\mathrm{T_{BD}}$.

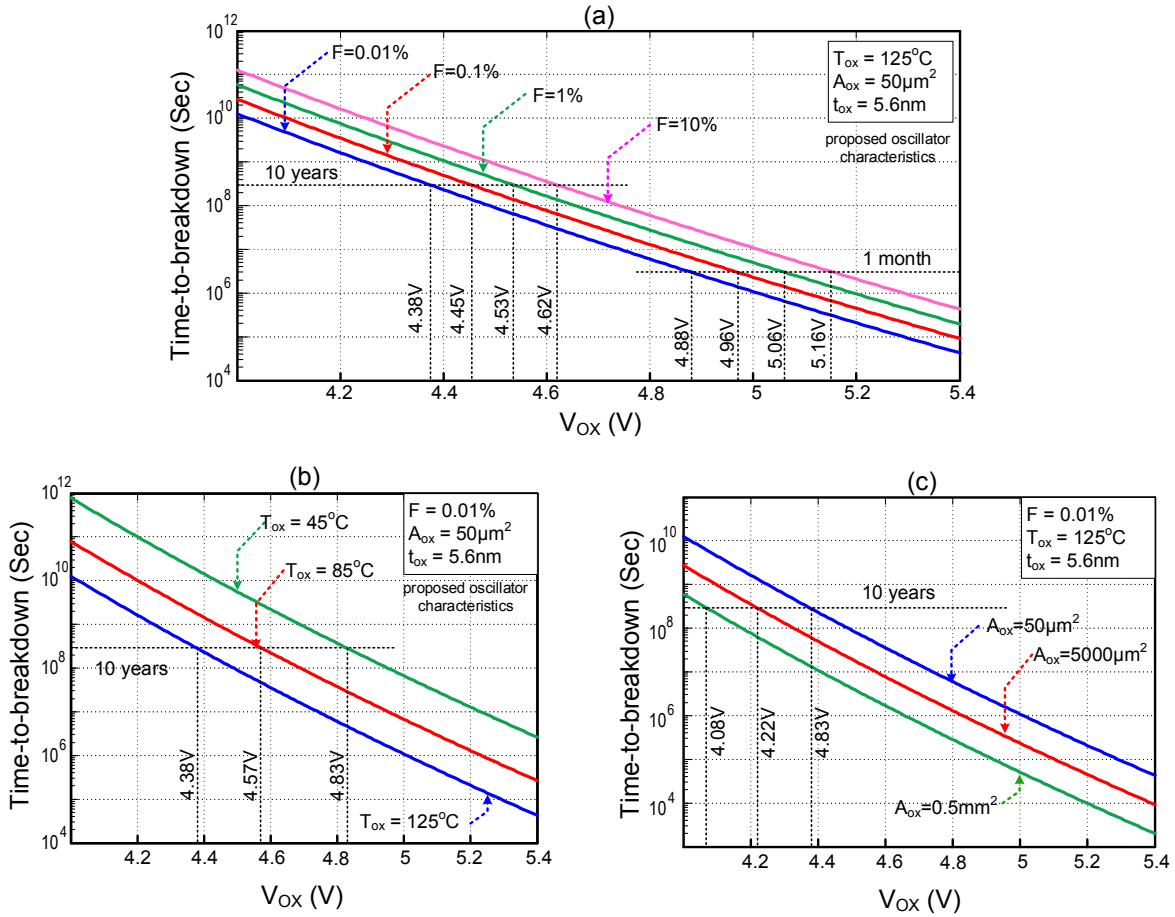


Figure 4.20: Estimated time-to-breakdown (based on the measured parameters of Fig. 4.19(a)) of thick-oxide transistors in 65 nm CMOS versus maximum gate-oxide stress voltage for different (a) cumulative failure rates, (b) temperatures, (c) gate-oxide areas.

Figure 4.19(a) shows the measured F versus T_{BD} for 14 samples of the thick-oxide transistor (176 μm/0.28 μm) at room temperature when a large voltage (6.75 V & 7 V) is applied across the gate. The data points are easily mapped to a Weibull distribution curve as indicated by the dashed line. The cross-over of these curves at F=63.2% specifies the reference η values (η_{ref}). The voltage acceleration ratio n is calculated by applying η_{ref} values and their related V_{ox} in (4.23). Furthermore, the slope of the curves determines β. Consequently, the estimated n and β values are respectively 42 and 3 for the thick-oxide devices (t_{ox}=5.6 nm) in 65nm CMOS, which are close to extracted measured numbers from literature, as shown in Fig. 4.19(c-d) [14], [98]. The E_a is ~0.55 eV and independent from the oxide thickness and temperature [99]. Consequently, the given oscillator η can be estimated by substituting the measured reference and technology parameters and circuit characteristics (A_{ox}, V_{ox}, T_{ox}) in (4.23). Finally, T_{BD} is calculated by substituting the estimated η and the desired F in (4.22).

The lifetime estimation of our circuit as a function of V_{ox} is plotted in Fig. 4.20 for various F, T_{ox} and A_{ox}. The plots indicate that the maximum voltage across the oxide for $M_{1,2}$ transistors should be <4.4 V to ensure <0.01% failure during 10 years at 125°C. The max V_{ox} could be increased if higher failure rate or lower max operating temperature are accepted. The maximum dc voltage is thus established across the gate-oxide. However, the actual nature of stress in

RF oscillators is not dc but an ac voltage $V_{ox}(\omega_0 t)$. Consequently, it is instructive to compare the static max V_{ox} with the actual operation when η changes over the period of the resonant frequency. Hence, the "effective" η is calculated as

$$\frac{1}{\eta_{\text{eff}}} = \frac{1}{2\pi}\int_0^{2\pi} \frac{1}{\eta\left(V_{ox}\left(\omega_0 t\right)\right)}\, d\left(\omega_0 t\right) \tag{4.24}$$

where, $\eta(V_{ox}(\omega_0 t))$ is given by (4.23) and can be expediently simplified to $\eta = B \cdot (V_{ox}(\omega_0 t))^{-n}$.

Starting with the application's desired operating time (i.e., T_{BD}) at a given failure rate (F) in a given technology (i.e., β), the parameter η_{eff} is first established as per (4.22) and is identical for dc and ac operations. For a dc operation, $\eta = B \cdot (V_{dc})^{-n}$ and (4.24) results in

$$V_{dc} = \left(\frac{B}{\eta_{\text{eff}}}\right)^{1/n} \tag{4.25}$$

However, for an ac operation,

$$\frac{1}{\eta_{\text{eff}}} = \frac{1}{2\pi}\int_0^{2\pi} \frac{1}{B\left(0.5V_{ac,max}\left(1+sin\left(\omega_0 t\right)\right)\right)^{-n}}\, d\left(\omega_0 t\right) \tag{4.26}$$

Solving this integral for the voltage acceleration factor n of 42 for the 65-nm CMOS thick-oxide devices,

$$V_{ac,max} = \left(\frac{11.5 \cdot B}{\eta_{\text{eff}}}\right)^{1/n} \tag{4.27}$$

Consequently, the ac to dc maximum tolerable stress voltage ratio ($V_{ac,max}/V_{dc}$) will be $(11.5)^{1/n} \approx 1.06$. We strongly emphasize that there are no significant differences in max V_{ox} at ac-peak and dc conditions due to the sharp slope of T_{BD}-V_{ox} curves in Fig. 4.20. As shown by integrating the voltage-dependent $\eta(V_{ox})$ over the full oscillation cycle, the peak magnitude of the V_{ox} sine wave can be just 6% higher than what is determined for a fixed dc V_{ox}. Consequently, the slightly lower pessimistic value of V_{ox} in the dc condition could be used as an extra margin.

4.7 Conclusion

In this Chapter, we have proposed and analyzed a class-F_2 oscillator where an auxiliary impedance peak is introduced around the second harmonic of the oscillating waveform. The second harmonic of the active device current converts into voltage and, together with the fundamental component, creates a soft clipped oscillation waveform. The class-F_2 operation offers enough headroom for the low noise operation of the tail current transistor without compromising the oscillator current and voltage efficiencies. Furthermore, the special ISF of the soft clipping waveform reduces significantly the circuit-to-phase noise conversion. The additional resonant frequency is realized by exploiting a different transformer behavior in common-mode and differential-mode excitations. In addition, the tank input impedance is also scaled down without sacrificing its Q-factor. Consequently, the proposed structure is able to push the phase noise much lower than practically possible with the traditional LC oscillators while satisfying long-term reliability requirements. The proposed reliability acceleration analysis indicates that the oscillator will function for >10 years with <0.01% failure rate at 125°C.

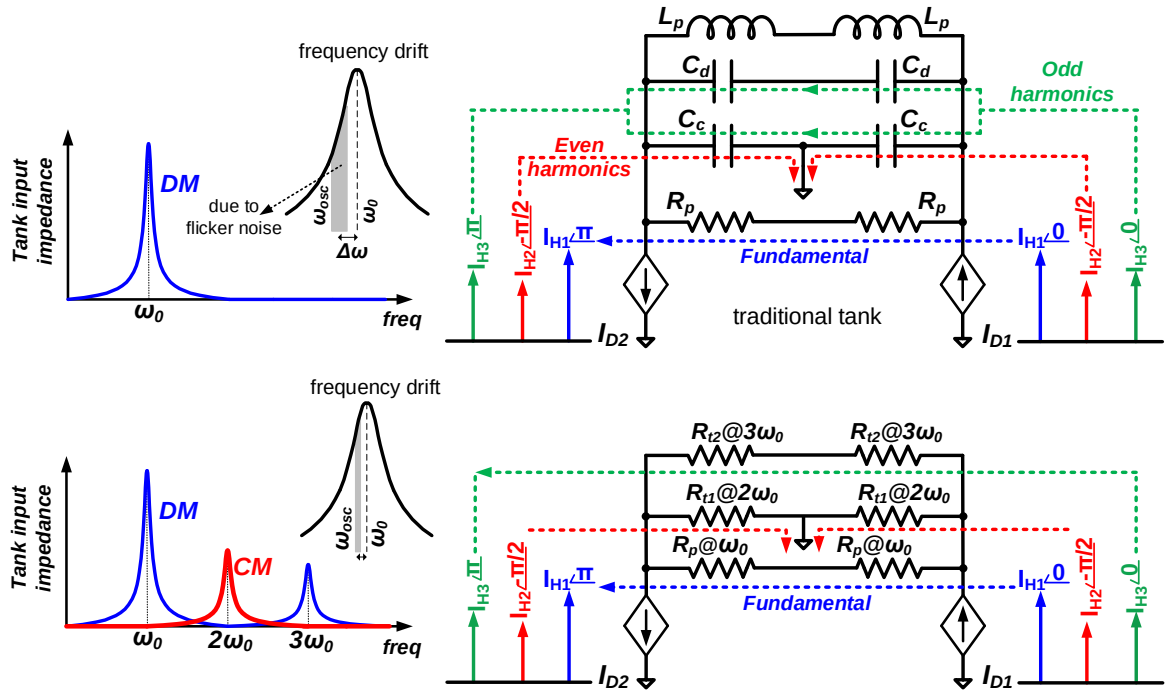


Figure 4.21: Current harmonic paths and frequency drift for a tank without (top) and with (bottom) resistive traps at higher harmonics.

4.8 Extension of class-F$_2$ operation for reducing flicker noise upconversion

The 1/f (flicker) noise upconversion degrades the close-in spectrum of CMOS RF oscillators[1]. The resulting 1/f^3 phase noise (PN) can be an issue in PLLs with a loop bandwidth of <1 MHz, which practically implies all cellular phones. A previously published noise-filtering technique [101] and adding resistors in series with gm-device drains [102] have shown significant reduction of the 1/f^3 oscillator PN corner. However, the former needs an additional tunable inductor and the latter degrades PN in the 20 dB/dec region.

The flicker noise can upconvert via two major phenomena. First, tail current flicker noise can modulate the oscillating waveform amplitude, which can convert to PN through a nonlinear C-V characteristic of varactors and active devices. The second mechanism is the Groszkowski effect [46]: The presence of harmonic components of the active gm device current can cause a frequency drift of the tank resonance (see Fig. 4.21 (top)). The fundamental drain current I_{H1} flows into R_p (equivalent parallel resistance of the tank), while its 2nd- and 3rd-harmonic components, I_{H2} and I_{H3}, mainly take the capacitance path due to its lower impedance. Consequently, the reactive energy stored in the inductance and capacitance is perturbed, shifting the oscillation frequency $\Delta\omega$ lower to satisfy the resonance condition. It can be shown that

$$\Delta\omega = -\frac{\omega_0}{2Q^2}\sum_{k=2}^{\infty} a_k \left(\frac{I_{Hk}}{I_{H1}}\right)^2. \tag{4.28}$$

[1]The main contributor of this section is Mina Shahmohammadi from TU Delft. This work has been published in the ISSCC2016 digest [100].

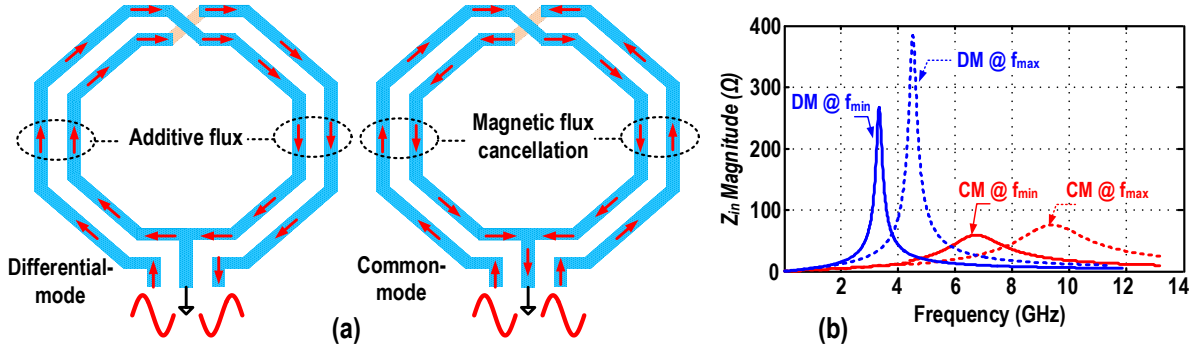


Figure 4.22: Proposed F_2 inductor in DM and CM excitation (top), F_2 tank and its input impedance (bottom).

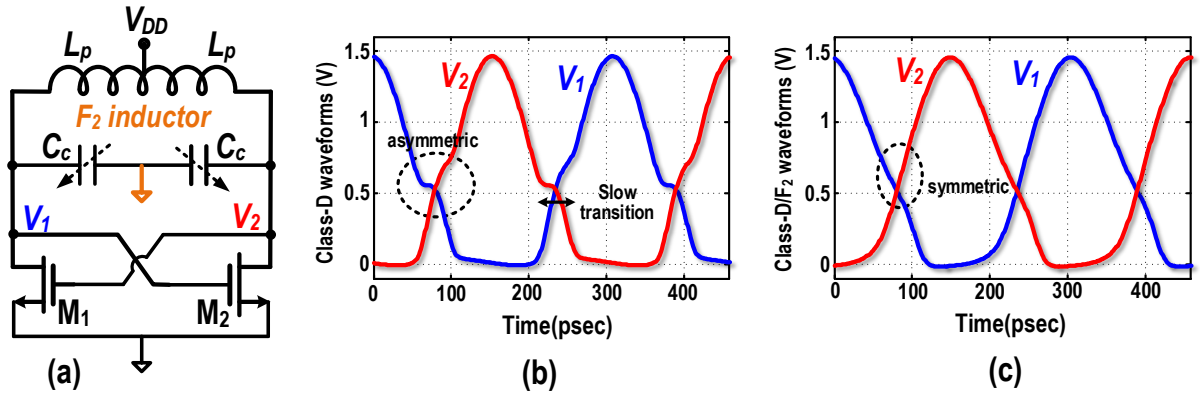


Figure 4.23: (a) Schematic of the proposed class-D/F_2 oscillator; oscillation waveforms of (b) the class-D and (c) class-D/F_2.

This shift is static but any variation in the I_{H2}(or I_{H3})-to-I_{H1} ratio due to the 1/f noise can modulate $\Delta\omega$ and show itself as the $1/f^3$ PN. This phenomenon is clearly visible and now dominant in oscillators with the customary tail current source transistor removed, which is the trend in nanoscale CMOS.

Suppose the tank input impedance Z_{in} demonstrates other peaks at the strong harmonics of the fundamental frequency ω_0. These harmonics would mainly flow into their relative equivalent resistance of Z_{in} instead of its capacitive part as is shown in Fig. 4.21 (bottom). Consequently, Groszkowski's effect on the 1/f noise up-conversion will reduce significantly. Specifically, core transistor flicker noise modulates the 2nd harmonic of the oscillator's virtual ground. This modulation generates 2nd-harmonic current in the parasitic C_{gs} capacitors and gets injected into the tank. Consequently, the I_{H2} component is usually the main contributor to the frequency shift. In this work, we introduce a tank topology that effectively traps I_{H2} in its resistive part without the cost of an extra area. The tank acquires this characteristic from the different behavior of inductors in differential (DM) and common mode (CM) excitations.

Figure 4.22 shows a 2-turn inductor in DM and CM excitations. In DM, the currents in each turn are in the same direction resulting in an additive flux, while in CM, the opposite currents cancel each other's magnetic flux. Due to this cancellation, the effective CM inductance is very low. The "F_2 inductor" is designed with appropriate spacing between the windings and demonstrates a 4× smaller effective inductance for CM inputs than for DM inputs. The CM input signals cannot see the differential capacitances, hence to be able to set a CM resonance,

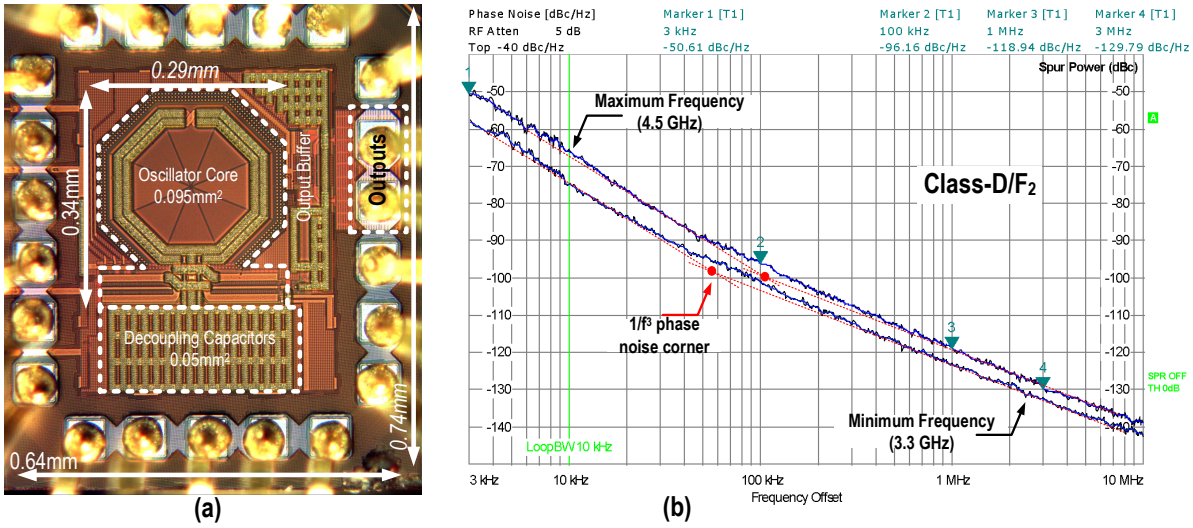


Figure 4.24: (a) Die micrograph of class-D/F$_2$ oscillator; (b) its measured phase noise.

Table 4.4: Performance summary and comparison with relevant state-of-the-art oscillators.

		This work Class-D/F$_2$		Fanori [JSSC'13] Class-D		Fanori [JSSC'13] Noise filtering class-D		Babaie [JSSC'13]	Pepe [JSSC'13]	Murphy [ISSCC'15]	Mostajeran [ISSCC'15]
Technology		40 nm		65 nm		65 nm		65 nm	65 nm	28 nm	130 nm
Thick metal		No		Yes		Yes		Yes	NA	NA	NA
V_{DD} (V)		0.5		0.4		0.4		1.25	1.2	0.9	1.4
Tuning range (%)		31		45		45		25	18	27.2	1.7
Core area (mm²)		0.1		0.12		0.15		0.12	0.08	0.19	0.09
Freq. (GHz)		f_{min}	f_{max}	f_{min}	f_{max}	f_{min}	f_{max}	f_{max}	f_{max}	f_{mid}	f_{mid}
		3.3	4.5	3	4.8	3	4.8	7.4	3.6	3.3	2.4
P_{DC} (mW)		4.1	2.5	6.8	4	6.8	3.6	15	0.72	6.8	4.2
PN (dBc /Hz)	**100kHz**	-101.2	-96.2	-101	-91	-102	-92.5	-98.5	-94.4	-106	88.4
	1MHz	-123.4	-119	-127	-119	-128	-121	-125	-114.4	-130	128.4
	10MHz	-143.4	-139	-149.5	-143.5	-150	-144.5	-147	-134.4	-150	148.4
FoM† (dB)	**100kHz**	185.4	185.3	182.2	178.6	183.2	180.6	184.1	187	188.2	189.8
	1MHz	187.6	188	188.2	186.6	189.2	189.1	190.6	187	192.2	189.8
	10MHz	187.6	188	190.7	191.1	191.2	192.6	192.6	187	192.2	189.8
1/f³ corner (kHz)		60	100	800	2100	650	1500	700	10	200	<10
Freq. pushing (MHz/V)		40 @0.5V	60 @0.5V	140 @0.5V	480 @0.5V	90 @0.5V	390 @0.5V	50 @1.25V	15 @1.2V	NA	NA

†FoM = |PN|+20 $\log_{10}(\omega_0/\Delta\omega)$ - 10 $\log_{10}(P_{DC,osc}/1mW)$

the capacitors across the tank have to be single-ended. The input impedance of the F$_2$ tank, Z_{in}, demonstrates two resonant frequencies, $\omega_{DM} = \omega_0$, and $\omega_{CM} = 2\omega_0$. The precise inductor geometry controlled by lithography maintains $L_{DM}/L_{CM} \approx 4$ and hence $\omega_{CM}/\omega_{DM} \approx 2$ over the full tuning range, TR. The lower and broader CM impedance, compared to that of DM, guarantees the 2nd-harmonic current flowing mainly to the additional resistive part, even if CM resonant frequency is mistuned by 10%.

To demonstrate how this technique can reduce the flicker noise upconversion, we employ the F$_2$-tank to a Class-D oscillator [103]. This class of oscillator is chosen for its strong amount of I_{H2}. The original Class-D oscillator shows promising performance in the 1/f^2 region but it suffers from the strong 1/f noise upconversion and frequency supply pushing. All known mitigation techniques (e.g., [26]) seem either ineffective or unsuitable. As shown in Fig. 4.23 (top) (a), the Class-D/F$_2$ oscillator adopts the F$_2$ tank. The gm-devices M$_1$ and M$_2$ inject a large I_{H2} current into the tank due to the ground-clipping of signals. Figure 4.23 (b) and (c) compare Class-D and

D/F_2 waveforms. Clearly the rise/fall times are more symmetric in the Class-D/F_2 oscillator, which translates to lower DC value of the gm-transistor ISF function and thus lowers the 1/f noise up-conversion. The Class-D oscillator shows 0.8 to 2.5 MHz $1/f^3$ corner frequency. A version of Class-D with a tail-filter technique was also designed in [103]. A resonator at $2\omega_0$ is interposed between the common source of the transistors and ground. This method is only partially effective, lowering the $1/f^3$ PN corner to 0.6 to 1 MHz, since it only linearizes the gm device and partially reduces the I_{H2} amount. Our method traps I_{H2} in the tank and simulations predict the $1/f^3$ PN corner of <50 kHz.

The Class-D/F_2 oscillator was prototyped in a 40 nm 1P8M CMOS process without ultra-thick metal layers. The chip micrograph is shown in Fig. 4.24 (a). The tank employs a 1.5 nH inductor with simulated Q-factor of 12 at 3 GHz. $M_{1,2}$ are (200μm/40nm) low-V_t devices which guarantee start-up and Class-D operation over PVT. Figure 4.24 (b) shows the PN plots at fmax and fmin oscillation frequencies, with V_{DD}=0.5 V. The $1/f^3$ PN corner is ∼100 kHz at f_{max} and reduces to 60 kHz when all switches are on at f_{min}. Table 4.4 summarizes the oscillator performance and compares it with relevant state-of-the-art oscillators.

Chapter

5

Comprehensive Analysis of Switch-mode PAs

Due to the relentless customer demand for high data rate wireless communication, the need for higher frequencies and more efficient power amplifiers has been increasing. The power amplifier is the one of the most power-hungry elements in an RF/mm-wave transceiver, and consequently, any improvement on its power efficiency can extend the battery lifetime of a mobile device. Furthermore, even in the wireless base stations, power-efficient PAs are in demand to reduce the cost of expensive cooling equipment and improve system's long time reliability.

The drain efficiency of the switched-mode power amplifiers is ideally 100% [104, 105], which makes them an attractive candidate for amplifying RF signals. However, they usually demonstrate a significant amplitude-to-amplitude (AM-AM) and amplitude-to-phase (AM-PM) distortions. Fortunately, they are linear in phase and their phase-to-phase (PM-PM) distortion is negligible. Consequently, as a standalone module, switched-mode PA can only support phase modulated signals like FSK. However, by utilizing more advanced digitally-assisted transmitters such as outphasing, envelope elimination & restoration, and direct digital-to-RF conversion architectures, switched-mode PAs can be exploited to support more complex modulation schemes and enhance the system efficiency.

In this chapter, different characteristics of switched-mode PAs are investigated and quantified. It will allow designers to better understand how to choose the best topology among different flavors of switched-mode PAs, suited to meet their various specifications. Different trade-offs between the power gain, output power, drain efficiency, maximum operating frequency, and power added efficiency will be comprehensively studied for various kinds of switched-mode PAs. Thanks to our general approach, the study is even extended to include the non-zero voltage switching (NZVS) operation of power amplifiers. Note that this research picks up where Scott Kee has left the analysis of class-E/F harmonic-tuned switching power amplifier and extend it to more general results [106]. In this work, practical non-idealities are applied to the analysis such that much more accurate equations are obtained for different characteristics of switched-mode

PAs. The new insights provide a better understanding of the tradeoffs in RF/mm-wave PA design.

5.1 Predicting Switching Amplifier Waveforms

Figure 5.1 illustrates a generalized schematic suitable for analyzing most switch-mode power amplifiers [106]. The active device, M_1, is modeled by a perfect switch with its parasitic. $\overline{R_{on}}$ and $\overline{C_{out}}$ respectively model the normalized on-state channel resistance and off-state output capacitance of M_1 transistor. Furthermore, a simple parallel $\overline{R_{in}C_{in}}$ network is added for input power approximation. C_s is the PA desired shunt capacitance to satisfy the zero-voltage and zero-slope switching (ZVS & ZdVS) criteria. The transistor is driven periodically at a fundamental frequency, f_0, with duty cycle D. The matching network contains a bank of bandpass filters, which provide the desired impedance at their tuned frequency and act as an open circuit at other frequencies. Consequently, the current i_x out of the matching network can be calculated as

$$i_x(\theta) = a_0 + \sum_{k=1}^{n} \left(a_k \cdot \cos(k\theta) + b_k \cdot \sin(k\theta)\right) \tag{5.1}$$

where $\theta = \omega_0 t$. a_k and b_k are respectively in-phase and quadrature current component of the matching network at $k \cdot f_0$. At the switch's off-to-on transition instant, the drain voltage is forced from V_0 to zero and thus the C_s charge $Q = C_s \cdot V_0$ is approximately depleted via the switch in the form of Dirac impulse. For the remaining conducting phase, drain voltage almost sticks to 0 and thus i_c reduces to zero [106]. As a result, i_x has to flow to ground through the switch. Hence, the switch current can be calculated by

$$i_s(\theta) = \begin{cases} Q \cdot \delta(\theta) - a_0 - \sum_{k=1}^{n} \left(a_k \cdot \cos(k\theta) + b_k \cdot \sin(k\theta)\right) & 0 < \theta \leq 2\pi D \\ 0 & 2\pi D < \theta \leq 2\pi \end{cases} \tag{5.2}$$

As shown in [106], the above equation can be simplified to

$$i_s(\theta) = -s(\theta) \cdot i_x(\theta) + Q \cdot \sum_{p=-\infty}^{\infty} \delta(\theta - p \cdot 2\pi) \tag{5.3}$$

where $s(\theta)$ is a gate function with a value of one during the conducting phase of the switch and zero otherwise.

$$s(\theta) = \begin{cases} 1 & 0 \leq \theta \leq 2\pi D \\ 0 & 2\pi D \leq \theta \leq 2\pi \end{cases} \xrightarrow{FT} S_k = \begin{cases} D & k = 0 \\ \dfrac{\sin(2\pi D k)}{2\pi k} - j\dfrac{\sin^2(\pi D k)}{\pi k} & k \neq 0 \end{cases} \tag{5.4}$$

The switch is off in the second phase and thus, i_x has to flow to ground through C_s [106]. Consequently, the shunt capacitor current may be estimated by

$$i_c(\theta) = \begin{cases} Q \cdot \delta(\theta) & 0 < \theta \leq 2\pi D \\ -a_0 - \sum_{k=1}^{n} \left(a_k \cdot \cos(k\theta) + b_k \cdot \sin(k\theta)\right) & 2\pi D < \theta \leq 2\pi \end{cases} \tag{5.5}$$

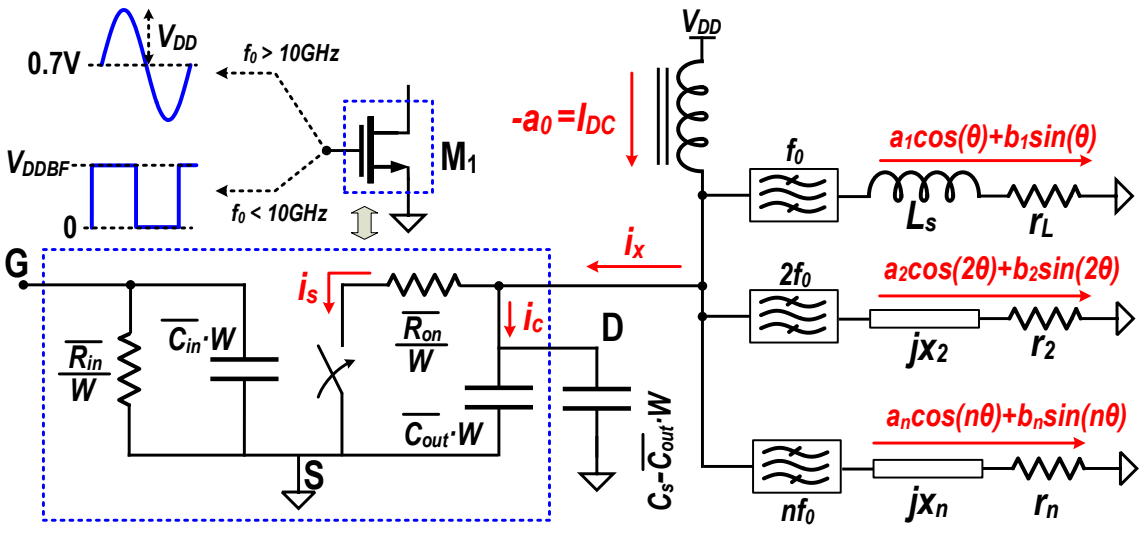


Figure 5.1: Generalized schematic of class-E/F power amplifier including NMOS device circuit model as a switch.

The above equation can be simplified to

$$i_c(\theta) = -\overline{s}\,(\theta) \cdot i_x\,(\theta) - Q \cdot \sum_{p=-\infty}^{\infty} \delta\,(\theta - p \cdot 2\pi) \tag{5.6}$$

and where $\overline{s}\,(\theta)$ is a square-wave with a value of unity when the switch is open and zero otherwise.

$$\overline{s}\,(\theta) = \begin{cases} 0 & 0 \le \theta \le 2\pi D \\ 1 & 2\pi D \le \theta \le 2\pi \end{cases} \xrightarrow{FT} \overline{S_k} = \begin{cases} \overline{D} = 1 - D & k = 0 \\ \dfrac{\sin\left(2\pi \overline{D} k\right)}{2\pi k} + j\dfrac{\sin^2(\pi \overline{D} k)}{\pi k} & k \neq 0 \end{cases} \tag{5.7}$$

By applying Fourier transform to both sides of (5.3) and (5.6), the k_{th} harmonic component of the current of the switch and shunt capacitor can be respectively expressed by the following equations [106].

$$I_s(k) = \frac{Q}{2\pi} - S(k) * I_x\,(k) \tag{5.8}$$

$$I_c(k) = -\frac{Q}{2\pi} - \overline{S}(k) * I_x\,(k) \tag{5.9}$$

The transistor drain voltage can be found by integration of i_c into the shunt capacitance [106].

$$v_d\,(\theta) = \begin{cases} V_{sat} & 0 < \theta \le 2\pi D \\ V_{sat} - \dfrac{1}{C_s \omega_0} \displaystyle\int_{2\pi D}^{\theta} \left(a_0 + \sum_{k=1}^{n} \left(a_k \cdot \cos(k\theta) + b_k \cdot \sin(k\theta)\right)\right) & 2\pi D < \theta \le 2\pi \end{cases} \tag{5.10}$$

where V_{sat} represents the transistor's average V_{DS} in on-state. By applying Fourier transform to both sides of (5.10), the k_{th} harmonic component of the drain voltage can be calculated by

$$V_d(k) = \frac{-j}{kC_s\omega_0} \cdot I_c\,(k) \tag{5.11}$$

Furthermore, the ratio of the k_{th} harmonic component of drain voltage and I_x must be the same as impedance Z_k seen from the input of the matching network at that frequency [106].

$$V_d(k) = Z_k I_x(k) = (r_k + jx_k) I_x(k) \tag{5.12}$$

By equating the equations of (5.11) and (5.12), we have

$$j \cdot k \cdot Z_k \cdot C_s \omega_0 \cdot I_x(k) - I_c(k) = 0 \tag{5.13}$$

By replacing (5.9) in (5.13), a series of equations are obtained for different harmonic components of i_x.

$$j \cdot k \cdot Z_k \cdot C_s \omega_0 \cdot I_x(k) + \overline{S}(k) * I_x(k) + \frac{Q}{2\pi} = 0 \tag{5.14}$$

Eq. (5.14) contains $2n+1$ linear equations (one at DC, two equations at each tuned harmonic) with $2n+2$ unknown variables ($a_0, a_1, ..., a_n, b_1, ..., b_n$, and Q) [106]. For example, suppose that the fundamental and third-harmonic filters are just terminated by certain load impedances. Consequently, there are six unknown variables in the system (a_0, a_1, b_1, a_3, b_3, and Q). However, Eq. (5.14) offers only 5 linear equations (one at DC, two at ω_0 and two at $3\omega_0$). Hence, another equation is needed to help to solve the system. Since the shunt capacitor is directly connected to the supply by a big choke, the capacitor's average voltage must be equal to V_{DD}. This condition provides the last required equation to find the system's unknown variables [106].

$$\begin{aligned} V_{DD} = \frac{1}{2\pi}\int_0^{2\pi} v_d(\theta)d\theta = V_{sat} - \frac{\overline{D^2}\pi a_0}{C_s\omega_0} + \\ \frac{1}{C_s\omega_0}\sum_{k=1}^{n}\left(\frac{\overline{D}}{k}\sin(2\pi kD) + \frac{1-\cos(2\pi kD)}{2\pi k^2}\right)a_k - \left(\frac{\overline{D}}{k}\cos(2\pi kD) + \frac{\sin(2\pi kD)}{2\pi k^2}\right)b_k \end{aligned} \tag{5.15}$$

This expression should be appended to (5.14) to reach a solvable matrix of equations. For example, the matrix of equations would become as follows if the first four harmonics were terminated in the matching network and input duty cycle was 50% [106].

$$\begin{bmatrix} \frac{1}{2} & 0 & \frac{-1}{\pi} & 0 & 0 & 0 & \frac{-1}{3\pi} & 0 & 0 & \frac{1}{2\pi} \\ 0 & \frac{1}{4}-\frac{X_1}{2} & 0.5R_1 & 0 & \frac{-2}{3\pi} & 0 & 0 & 0 & \frac{-4}{15\pi} & \frac{1}{2\pi} \\ \frac{1}{\pi} & 0.5R_1 & \frac{X_1}{2}-\frac{1}{4} & \frac{-1}{3\pi} & 0 & 0 & 0 & \frac{-1}{15\pi} & 0 & 0 \\ 0 & 0 & \frac{1}{3\pi} & \frac{1}{4}-X_2 & R_2 & 0 & \frac{-3}{5\pi} & 0 & 0 & \frac{1}{2\pi} \\ 0 & \frac{2}{3\pi} & 0 & R_2 & X_2-\frac{1}{4} & \frac{-2}{5\pi} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{2}{5\pi} & \frac{1}{4}-\frac{3X_3}{2} & 1.5R_3 & 0 & \frac{-4}{7\pi} & \frac{1}{2\pi} \\ \frac{1}{3\pi} & 0 & 0 & \frac{3}{5\pi} & 0 & 1.5R_3 & \frac{3X_3}{2}-\frac{1}{4} & \frac{-3}{7\pi} & 0 & 0 \\ 0 & 0 & \frac{1}{15\pi} & 0 & 0 & 0 & \frac{3}{7\pi} & \frac{1}{4}-2X_4 & 2R_4 & \frac{1}{2\pi} \\ 0 & \frac{4}{15\pi} & 0 & 0 & 0 & \frac{4}{7\pi} & 0 & 2R_4 & 2X_4-\frac{1}{4} & 0 \\ \frac{-\pi Z_{cs}}{4} & \frac{Z_{cs}}{\pi} & \frac{Z_{cs}}{2} & 0 & \frac{-Z_{cs}}{4} & \frac{Z_{cs}}{9\pi} & \frac{Z_{cs}}{6} & 0 & \frac{-Z_{cs}}{8} & 0 \end{bmatrix} \cdot \begin{bmatrix} a_0 \\ a_1 \\ b_1 \\ a_2 \\ b_2 \\ a_3 \\ b_3 \\ a_4 \\ b_4 \\ Q \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ V_{DD} - V_{sat} \end{bmatrix} \tag{5.16}$$

where R_k and X_k are respectively the real and imaginary parts of tuning impedance Z_k at k_{th}

harmonic, normalized to $Z_{CS} = C_s\omega_0$.

$$R_k = \frac{Re\{Z_k\}}{Z_{cs}} = r_k C_s \omega_0, \qquad X_k = \frac{Im\{Z_k\}}{Z_{cs}} = L_k C_s \omega_0^2 \tag{5.17}$$

For consistency with other papers on this topic [107,108], the design set of K_C, K_X are respectively defined as the normalized tuning resistance and reactance at the fundamental frequency (see Fig. 5.1).

$$K_C = R_1 = r_L C_s \omega_0, \qquad K_X = X_1 = L_s C_s \omega_0^2 \tag{5.18}$$

and the effective quality factor of the fundamental load, K_L, is defined as

$$K_L = \frac{L_s \omega_0}{r_L} = \frac{K_X}{K_C} \tag{5.19}$$

By applying the values of harmonic-tuned loads in the matrix equation (5.16), the system unknown variables ($a_0 ... a_n, b_1 ... b_n$, and Q) and thus the exact voltage/current waveform of all circuit elements are determined.

5.2 Determining ZVS and ZdVS Tuning

Even though the matrix equation of (5.16) enables us to analyze and extract different current and voltage waveforms of any circuit of the type shown in Fig. 5.1, however, the design set has not yet been determined for ZVS and ZdVS criteria. At the switch off-to-on transition, the drain voltage is calculated by

$$V_0 = V_{sat} + \frac{1}{C_s\omega_0}\left(-2\pi\overline{D}a_0 + \sum_{k=1}^{n}\left(\frac{a_k}{k}\sin(2\pi kD) + \frac{b_k}{k}(1-\cos(2\pi kD))\right)\right) \tag{5.20}$$

The ZVS condition requires that V_0 should be about V_{sat}. This condition should be added to (5.14) to generate a set of equations, which satisfy ZVS criterion [106].

$$\begin{bmatrix}
\frac{1}{2} & 0 & \frac{-1}{\pi} & 0 & 0 & 0 & \frac{-1}{3\pi} & 0 & 0 & \frac{1}{2\pi} \\
0 & \frac{1}{4}-\frac{X_1}{2} & 0.5R_1 & 0 & \frac{-2}{3\pi} & 0 & 0 & 0 & \frac{-4}{15\pi} & \frac{1}{2\pi} \\
\frac{1}{\pi} & 0.5R_1 & \frac{X_1}{2}-\frac{1}{4} & \frac{-1}{3\pi} & 0 & 0 & 0 & \frac{-1}{15\pi} & 0 & 0 \\
0 & 0 & \frac{1}{3\pi} & \frac{1}{4}-X_2 & R_2 & 0 & \frac{-3}{5\pi} & 0 & 0 & \frac{1}{2\pi} \\
0 & \frac{2}{3\pi} & 0 & R_2 & X_2-\frac{1}{4} & \frac{-2}{5\pi} & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & \frac{2}{5\pi} & \frac{1}{4}-\frac{3X_3}{2} & 1.5R_3 & 0 & \frac{-4}{7\pi} & \frac{1}{2\pi} \\
\frac{1}{3\pi} & 0 & 0 & \frac{3}{5\pi} & 0 & 1.5R_3 & \frac{3X_3}{2}-\frac{1}{4} & \frac{-3}{7\pi} & 0 & 0 \\
0 & 0 & \frac{1}{15\pi} & 0 & 0 & 0 & \frac{3}{7\pi} & \frac{1}{4}-2X_4 & 2R_4 & \frac{1}{2\pi} \\
0 & \frac{4}{15\pi} & 0 & 0 & 0 & \frac{4}{7\pi} & 0 & 2R_4 & 2X_4-\frac{1}{4} & 0 \\
-\pi & 0 & 2 & 0 & 0 & 0 & \frac{2}{3} & 0 & 0 & 0
\end{bmatrix} \cdot \begin{bmatrix} a_0 \\ a_1 \\ b_1 \\ a_2 \\ b_2 \\ a_3 \\ b_3 \\ a_4 \\ b_4 \\ Q \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ V_0 - V_{sat} \end{bmatrix} \tag{5.21}$$

The above equation indicates that the determinant of the coefficient matrix must be zero to have a set of answers for unknown variables (a_0 to Q) satisfying ZVS criterion. The most common situation is where the impedances are known at the harmonic frequencies and it is desired to

find the load impedance (r_L and L_s) at the fundamental frequency to satisfy ZVS and ZdVS conditions. As explained in [109], resulting equation of (5.21) demonstrates that the normalized fundamental load (K_C and K_X) must lie on a circle, in which the circle center and its radius are a function of the harmonic impedances. On the other hand, the ZdVS condition also demands that the derivative of the drain voltage should be zero at the switch off-to-on transition [106]. Consequently,

$$\frac{dv_d}{d\theta} = Z_{cs}\sum_{k=1}^{n} a_k \longrightarrow \sum_{k=1}^{n} a_k = 0 \tag{5.22}$$

This condition should be added to (5.14) to generate a set of equations for ZdVS satisfaction [106].

$$\begin{bmatrix}
\frac{1}{2} & 0 & \frac{-1}{\pi} & 0 & 0 & 0 & \frac{-1}{3\pi} & 0 & 0 & \frac{1}{2\pi} \\
0 & \frac{1}{4}-\frac{X_1}{2} & 0.5R_1 & 0 & \frac{-2}{3\pi} & 0 & 0 & 0 & \frac{-4}{15\pi} & \frac{1}{2\pi} \\
\frac{1}{\pi} & 0.5R_1 & \frac{X_1}{2}-\frac{1}{4} & \frac{-1}{3\pi} & 0 & 0 & 0 & \frac{-1}{15\pi} & 0 & 0 \\
0 & 0 & \frac{1}{3\pi} & \frac{1}{4}-X_2 & R_2 & 0 & \frac{-3}{5\pi} & 0 & 0 & \frac{1}{2\pi} \\
0 & \frac{2}{3\pi} & 0 & R_2 & X_2-\frac{1}{4} & \frac{-2}{5\pi} & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & \frac{2}{5\pi} & \frac{1}{4}-\frac{3X_3}{2} & 1.5R_3 & 0 & \frac{-4}{7\pi} & \frac{1}{2\pi} \\
\frac{1}{3\pi} & 0 & 0 & \frac{3}{5\pi} & 0 & 1.5R_3 & \frac{3X_3}{2}-\frac{1}{4} & \frac{-3}{7\pi} & 0 & 0 \\
0 & 0 & \frac{1}{15\pi} & 0 & 0 & 0 & \frac{3}{7\pi} & \frac{1}{4}-2X_4 & 2R_4 & \frac{1}{2\pi} \\
0 & \frac{4}{15\pi} & 0 & 0 & 0 & \frac{4}{7\pi} & 0 & 2R_4 & 2X_4-\frac{1}{4} & 0 \\
1 & 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 0
\end{bmatrix} \cdot \begin{bmatrix} a_0 \\ a_1 \\ b_1 \\ a_2 \\ b_2 \\ a_3 \\ b_3 \\ a_4 \\ b_4 \\ Q \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{5.23}$$

This equation indicates that the determinant of the coefficient matrix must be zero to have a set of answers for unknown variables (a_0 to Q) satisfying ZdVS criterion. The resulting equation of (5.23) is another circle for different sets of K_C and K_X, where its center and radius are the functions of the impedances of the tuned harmonics [106]. The intersection point of ZVS and ZdVS circles will satisfy both criteria and shows the optimal set for class-E/F tuning.

5.3 Waveform Figure of Merit

Figure 5.2 illustrates the ZVS and ZdVS circles for different flavors of class-E/F_X PA. The subscript of $_X$ lists the harmonics tuned to class-F^{-1} impedances. Note that the effective load is respectively an open-circuit and short-circuit for even and odd harmonics in a class-F^{-1} PA. However, the optimal fundamental load has a resistive and inductive combination like in a class-E PA. The black points in Fig. 5.2 show the optimal design set (K_C, K_X, K_L) to satisfy both ZVS/ZdVS simultaneously. Now, the value of all circuit elements are obtained and thus, the PA's unknown variables (a_0 to Q) can be calculated via (5.16). As a consequence, PA's waveform and performance figure-of-merits can be also extracted by the equations.

$$F_I = \frac{I_{rms1}}{I_{DC1}}, \quad F_{PI} = \frac{I_{peak1}}{I_{DC1}}, \quad F_V = \frac{V_{pk}-V_{sat}}{V_{DD}-V_{sat}}, \quad F_C = \frac{I_{DC1}}{C_s\omega_0\left(V_{DD}-V_{sat}\right)} \tag{5.24}$$

where, I_{DC1}, I_{rms1} are respectively the root mean square and average values of the switch

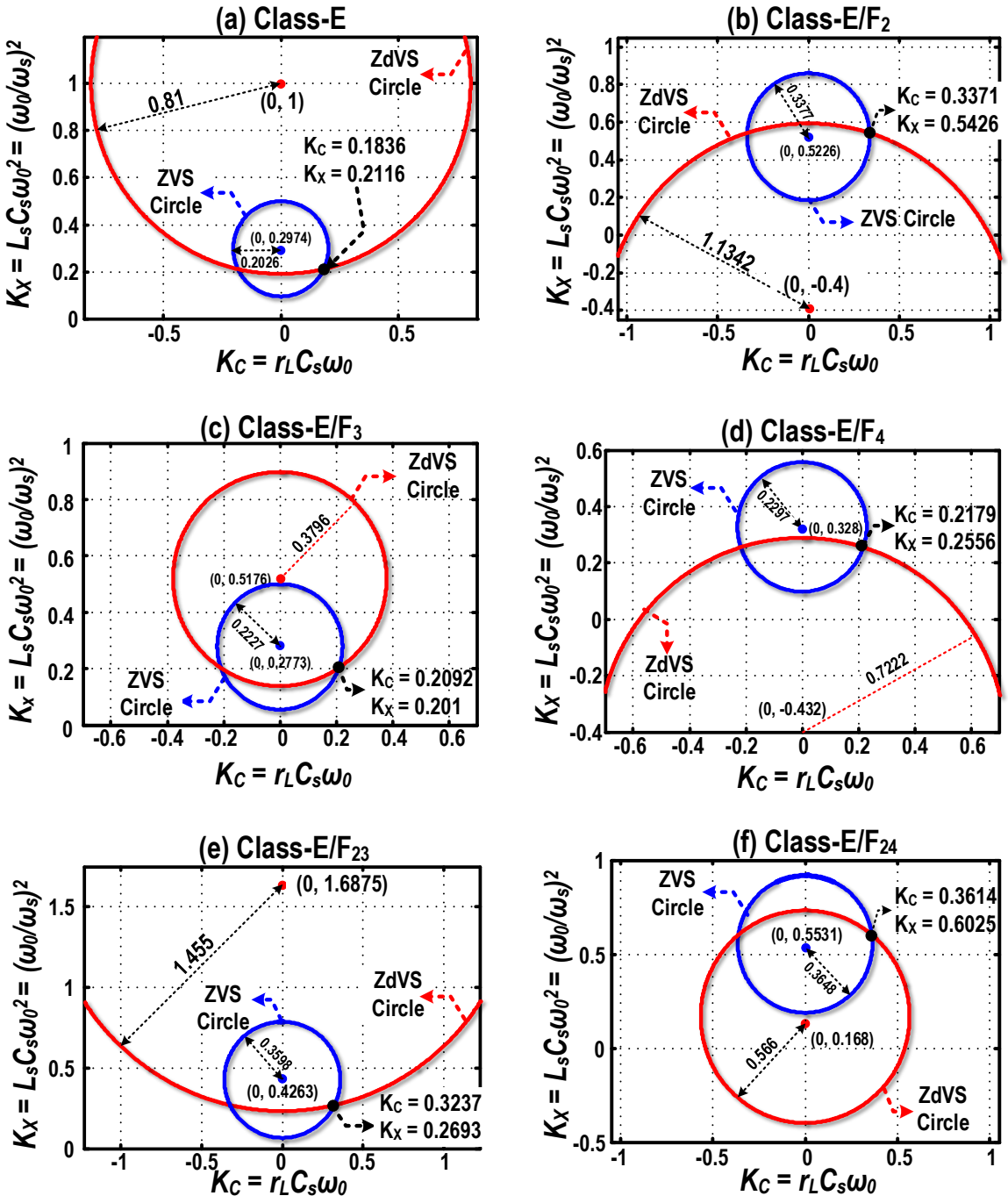


Figure 5.2: ZVS and ZdVS circles for different flavors of class-E/F PA in the normalized impedance plane. The black points show the optimal ZVS/ZdVS tuning.

current waveform. Note that the discharge current of shunt capacitance should not be included in the calculation of I_{rms1} and I_{DC1}. The waveform figure of merits are just a function of matching network strategy and do not change with the operating frequency ω_0=$2\pi f_0$ or CMOS technology. Note that F_C definition is different than in [109]. Since F_C cannot change over frequency, C_s has to reduce with increasing f_0. Hence, C_s limits the transistor's width at mm-wave, which leads to a dramatic increase in R_{on} and thus V_{sat} of the switching device. Consequently, we include

Table 5.1: Waveform FoMs for different flavors of class-E/F PA at ZVS/ZdVS tuning.

Tuning	K_C	K_L	K_X	K_P	F_V	F_I	F_{PI}	F_C
E	0.184	1.152	0.217	0.577	3.56	1.54	2.86	3.14
$\mathbf{E/F}_2$	0.337	1.609	0.543	0.381	3.67	1.48	3.33	1.13
$\mathbf{E/F}_3$	0.209	0.961	0.201	0.657	3.14	1.52	3.06	3.14
$\mathbf{E/F}_{2,3}$	0.323	0.832	0.256	0.747	3.13	1.47	2.67	2.31
$\mathbf{E/F}_4$	0.218	1.173	0.269	0.533	3.34	1.55	3.27	2.45
$\mathbf{E/F}_{2,4}$	0.361	1.667	0.602	0.350	3.43	1.46	3.6	0.97

Table 5.2: Technology dependent parameters for 40 nm CMOS technology.

Parameter	Description	Value
$\overline{R_{on}}$	normalized transistor on-resistance	$850\,\Omega \cdot \mu m$
$\overline{C_{out}}$	normalized transistor off-state output capacitance	$0.65\,fF/\mu m$
$\overline{C_{in}}$	normalized transistor input capacitance	$1\,fF/\mu m$
$\overline{R_{in}}$	normalized transistor input equivalent parallel resistance	$27\,k\Omega \cdot \mu m$
$\overline{I_{out}}$	normalized transistor drain current	$0.6\,mA/\mu m$

the effect of V_{sat} in F_C definition to achieve more practical analytic results than in [109]. Table 5.1 lists the waveform and performance FoMs for different flavors of class-E/F PA at ZVS/ZdVS tuning.

5.4 Technology Dependent Parameters

A simplified model of MOS transistor as a switch is shown in Fig. 5.1. The transistor is modeled by a channel on-resistance ($\overline{R_{on}}/W$), a linear output capacitor ($\overline{C_{out}} \cdot W$) and a parallel ($\overline{R_{in}}/W$)($\overline{C_{out}} \cdot W$) network at the input. It will be shown that the optimum size of the transistor and PA's performance are also strong functions of technology dependent parameters ($\overline{R_{on}}, \overline{C_{out}}, \overline{R_{in}}, \overline{C_{in}}$). Figure 5.3 illustrates the variation of those parameters versus V_{gs} for different V_{ds}. Based on these plots, the effective value of technology dependent parameters is also calculated and shown in Table 5.2 for TSMC 40 nm LP technology.

5.5 Predicting Switching Amplifier Performance

Up to now, we have learned to calculate the waveform FoMs for any given tuning strategy. In the following sections of this chapter, different characteristics of an arbitrary switched-mode PA will be determined versus technology and topology-dependent parameters.

In the non-ZVS condition, the shunt capacitance C_s will be discharged through the switch in the conducting phase. The loss associated with this discharge can be easily calculated by

$$P_{Cs} = 0.5 \cdot C_s \cdot V_0^2 \cdot f_0. \tag{5.25}$$

where, V_0 is the value of drain voltage right before the closing of the switch. By replacing C_s by

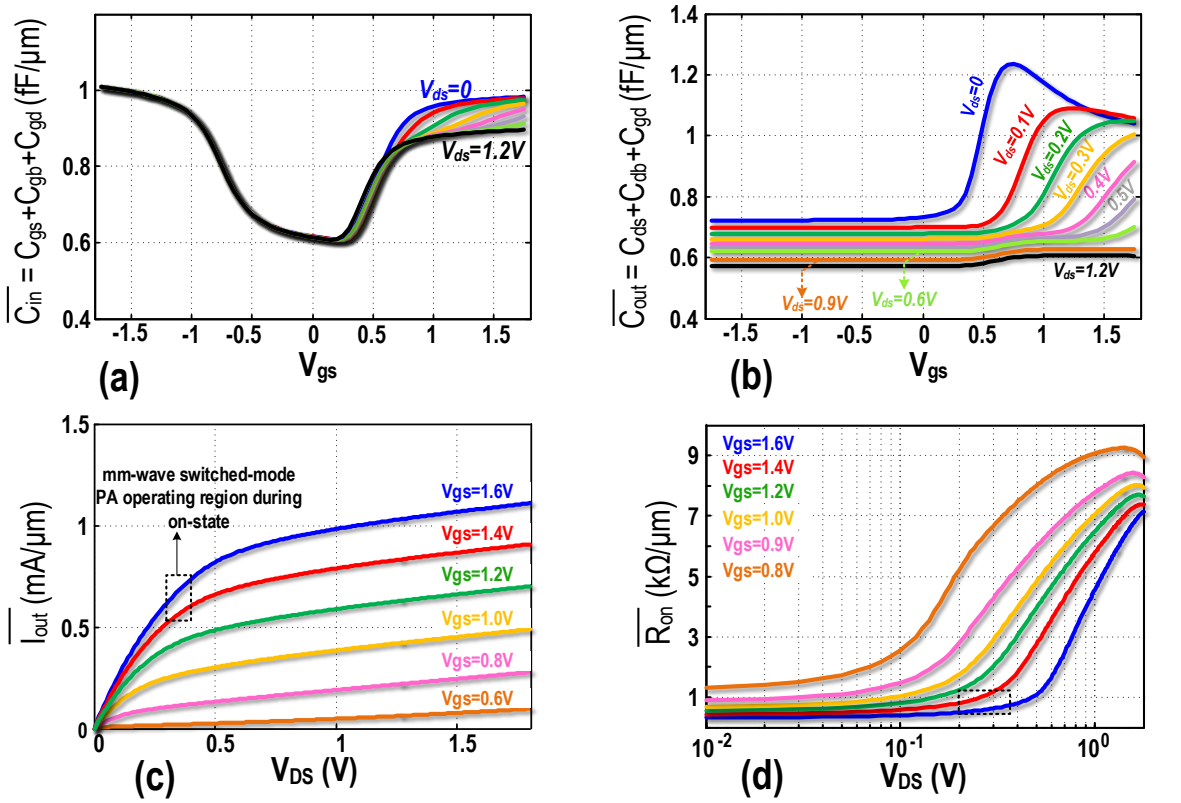


Figure 5.3: Technology dependent parameters in 40 nm CMOS technology, (a) $\overline{C_{in}}$ and (b) $\overline{C_{out}}$ versus V_{gs} for different V_{ds}, (c) $\overline{I_{out}}$ and $\overline{R_{on}}$ versus V_{ds} for different V_{gs}.

$K_C/(r_L \cdot \omega_0)$, P_{Cs} is simplified to

$$P_{Cs} = \frac{K_C}{4\pi} \cdot \frac{V_0^2}{r_L}. \tag{5.26}$$

This capacitive loss results in drawing an additional DC current I_{DC2} from the PA's supply voltage.

$$I_{DC2} = \frac{P_{Cs}}{V_{DD}} \quad \rightarrow \quad I_{DC2} = \frac{K_C \gamma^2}{4\pi} \cdot \frac{V_{DD}}{r_L}. \tag{5.27}$$

where, γ is defined as the ratio of V_0 over V_{DD}. The second part of dissipated power originates from the current flow through the switch on-resistance. The resulting average dissipated power P_{ron} is evaluated by

$$P_{ron} = V_{sat} I_{DC1} = R_{on} I_{rms1}^2. \tag{5.28}$$

where, V_{sat} represents the transistor's average V_{DS} in on-state. By utilizing the last two terms of (5.28), V_{sat} can be estimated by

$$V_{sat} = \frac{R_{on} I_{rms1}^2}{I_{DC1}} \quad \rightarrow \quad V_{sat} = R_{on} I_{DC1} F_I^2. \tag{5.29}$$

By replacing $R_{on} = \overline{R_{on}}/W$ and substituting F_C in (5.29),

$$V_{sat} = V_{DD} \cdot \frac{F_I^2 \overline{R_{on}}}{\left(\frac{W \cdot r_L}{K_C \cdot F_C}\right) + F_I^2 \overline{R_{on}}} \tag{5.30}$$

For the sake of simplicity of the next equations, X and β factors are defined.

$$X = \frac{W \cdot r_L}{K_C \cdot F_C} \qquad \beta = F_I^2 \cdot \overline{R_{on}} \tag{5.31}$$

As a consequence (5.30) is shortened to

$$V_{sat} = V_{DD} \cdot \frac{\beta}{X + \beta} \tag{5.32}$$

The remaining DC current of PA can be estimated by

$$I_{DC1} = F_C \cdot C_s \cdot \omega_0 \cdot (V_{DD} - V_{sat}) \quad \rightarrow \quad I_{DC1} = F_C \cdot K_C \cdot \frac{V_{DD}}{r_L} \cdot \frac{X}{X + \beta} \tag{5.33}$$

Now, the P_{ron} of (5.28) can be rewritten in the form of technology- and topology-dependent parameters.

$$P_{ron} = F_C \cdot K_C \cdot \frac{V_{DD}^2}{r_L} \cdot \frac{\beta X}{(X + \beta)^2} \tag{5.34}$$

The total DC current of PA can be derived by

$$I_{DC} = I_{DC1} + I_{DC2} \quad \rightarrow \quad I_{DC} = F_C \cdot K_C \cdot \frac{V_{DD}}{r_L} \cdot \left(\frac{X}{X + \beta} + \frac{\gamma^2}{4\pi F_C} \right) \tag{5.35}$$

and consequently,

$$P_{DC} = F_C \cdot K_C \cdot \frac{V_{DD}^2}{r_L} \cdot \left(\frac{X}{X + \beta} + \frac{\gamma^2}{4\pi F_C} \right) \tag{5.36}$$

the delivered power to the matching network can be evaluated by

$$P_{out} = P_{DC} - P_{Cs} - P_{ron} \quad \rightarrow \quad P_{out} = F_C \cdot K_C \cdot \frac{V_{DD}^2}{r_L} \cdot \left(\frac{X}{X + \beta} \right)^2 \tag{5.37}$$

The matching network has a vital role of transforming $R_L = 50\,\Omega$ to the desired resistive load (r_L) seen by the transistor. However, the signal power is attenuated by its losses. Hence, a smaller power is delivered to the $50\,\Omega$ load.

$$P_L = \eta_P \cdot P_{out} \quad \rightarrow \quad P_L = \eta_P \cdot F_C \cdot K_C \cdot \frac{V_{DD}^2}{r_L} \cdot \left(\frac{X}{X + \beta} \right)^2 \tag{5.38}$$

where η_p is the matching network efficiency. K_P is a waveform FoM, which determines the capability of a switched-mode PA in delivering power to the load. K_P is described by

$$K_P \equiv \frac{P_{out} \cdot r_L}{(V_{DD} - V_{sat})^2} \tag{5.39}$$

By combining (5.37) and (5.32), K_P can be written as the product of other waveform parameters

$$K_P = K_C \cdot F_C \tag{5.40}$$

It is interesting to see that PA's with higher capacitance tolerance (smaller F_C) can deliver lower power to the load. However, the optimum K_P value depends on the application. In general, the

insertion loss of an on-chip matching network dramatically increases if a very small or very large impedance transformation ratio (ITR) is needed. Hence, it is wise to choose a switched-mode PA that requires ITR of ∼1 to deliver the desired P_{out}. For example, switched-mode PAs with lower K_P are more attractive for ultra-low power applications, like Bluetooth Low Energy. However, a larger K_P is desired for WiFi or GSM standard, when the switches are in low-voltage CMOS technology.

The drain efficiency η_D of Fig. 5.1 PA can be estimated by

$$\eta_D = \frac{P_{out}}{P_{DC}} = \left(\frac{X}{X+\beta}\right) \cdot \left(\frac{4\pi F_C X}{(4\pi F_C + \gamma^2)\, X + \gamma^2 \beta}\right). \tag{5.41}$$

The term β inside the first parentheses shows the effect of the switch on-resistance on the η_D. However, the second term reduces the efficiency due to non-zero voltage switching. Consequently,

$$\eta_r = \frac{X}{X+\beta} \tag{5.42}$$

$$\eta_c = \frac{4\pi F_C X}{(4\pi F_C + \gamma^2)\, X + \gamma^2 \beta} \tag{5.43}$$

Eqs. (5.32) and (5.41) indicate that V_{sat} and η_D improve by using a matching network with lower F_I, K_C, and F_C. Furthermore, migrating to a more advanced technology (lower $\overline{R_{on}}$) is also beneficial to get higher η_D. As expected, increasing the size of the transistor reduces the R_{on} and thus, a better η_D is achievable but at the price of lower gain and increasing the power consumption of driver stage.

The input power P_{in} must also be determined to ensure that the transistor will be properly switched. The driver stage is typically an inverter-based amplifier at $f_0 \leq 10\,\text{GHz}$, which charges and discharges the input capacitance, $\overline{C_{in}} \cdot W$, of the switching transistor. As a consequence,

$$P_{in1} = W \cdot \overline{C_{in}} \cdot V_{DDBF}^2 \cdot f_0 \tag{5.44}$$

where, V_{DDBF} is a supply voltage of the driver stage. The required input power increases linearly with frequency, which limits the power gain of switching transistor at $f_0 \geq 10\,\text{GHz}$. To alleviate that dependency, the driver stage should tune out $\overline{C_{in}} \cdot W$ by utilizing a resonant matching network with a loaded quality factor of Q_{in}. Now, the input signal is sinusoidal and its amplitude should be about V_{DDBF} to force the transistor to operate as a switch. Consequently,

$$\begin{cases} P_{in2} = \dfrac{V_{DDBF}^2}{2 \cdot R_{in}} \\ R_{in} = \dfrac{Q_{in}}{\overline{C_{in}} \cdot W \cdot \omega_0} \end{cases} \rightarrow\ P_{in2} = \frac{\pi}{Q_{in}} \cdot W \cdot \overline{C_{in}} \cdot V_{DDBF}^2 \cdot f_0 \tag{5.45}$$

For consistency throughout the text, we define

$$P_{in} = \epsilon \cdot W \cdot \overline{C_{in}} \cdot V_{DDBF}^2 \cdot f_0, \quad \text{where} \quad \epsilon = \begin{cases} 1 & \text{w/o matching network} \\ \dfrac{\pi}{Q_{in}} & \text{w/i matching network} \end{cases} \tag{5.46}$$

The gain may be found by the ratio of P_L over P_{in}.

$$G_P = \frac{P_L}{P_{in1}} = \eta_p \cdot \frac{X}{(X+\beta)^2} \cdot \frac{1}{\epsilon \overline{C_{in}} f_0} \cdot \left(\frac{V_{DD}}{V_{DDBF}}\right)^2 \tag{5.47}$$

PA's gain can be improved by utilizing a matching network with lower F_I or migrating to more advanced technology (lower $\overline{R_{on}}$). For the simplicity of the next few equations, the following parameters are defined.

$$\alpha_V = \frac{V_{DD}}{V_{DDBF}}, \qquad \zeta = \frac{1}{\epsilon \overline{C_{in}} f_0} \tag{5.48}$$

As a consequence, (5.47) can be simplified to

$$G_P = \eta_P \cdot \zeta \cdot \alpha_V^2 \cdot \frac{X}{(X+\beta)^2} \tag{5.49}$$

The gain efficiency, η_G, of a switched-mode PA can be found by

$$\eta_G = 1 - \frac{1}{G_P} = 1 - \frac{(X+\beta)^2}{\eta_p \cdot \zeta \cdot \alpha_V^2 \cdot X} \tag{5.50}$$

Using this, the power added efficiency (PAE) may be estimated by

$$PAE = \frac{P_L - P_{in}}{P_{DC}} = \eta_p \cdot \frac{P_{out}}{P_{DC}} \cdot \left(1 - \frac{P_{in}}{P_L}\right) = \eta_p \cdot \eta_D \cdot \eta_G \tag{5.51}$$

Consequently,

$$PAE = \eta_p \cdot \left(1 - \frac{(X+\beta)^2}{\eta_p \cdot \zeta \cdot \alpha_V^2 \cdot X}\right) \cdot \left(\frac{X}{X+\beta}\right) \cdot \left(\frac{4\pi F_C X}{(4\pi F_C + \gamma^2)\, X + \gamma^2 \beta}\right) \tag{5.52}$$

As can be gathered from (5.52) and Fig. 5.4, using a larger transistor leads to a lower on-resistance and thus higher drain efficiency. However, that large transistor needs higher input power while generating the same P_{out}. As a result, PA gain and η_G are reduced. Since η_D and η_G exhibit different trends with the increase of transistor size, their product should have a peak at a certain device width. Simulations show that the optimum X-factor changes a bit ($\leq 10\%$) in the non-zero voltage switching condition (compare Fig. 5.4 (a) and (d)). Hence, the optimum X-factor is just calculated at the ZVS condition for the sake of simplicity.

$$\begin{aligned} \frac{d\,(PAE)}{dX} = 0 \quad \rightarrow \quad X_{opt} = \alpha_V \cdot \sqrt{\eta_p \cdot \zeta \cdot \beta} - \beta \quad \rightarrow \\ X_{opt} = F_I \overline{R_{on}} \left(\alpha_V \sqrt{\frac{\eta_p}{\epsilon \overline{R_{on} C_{in}} f_0}} - F_I\right) \end{aligned} \tag{5.53}$$

The above equation and Fig. 5.4 (a)-(c) indicate that both the voltage efficiency and η_p affect the optimum size of the transistor. Furthermore, X_{opt} is only a function of F_I among different waveform FoMs. Class-E/F$_{3,4}$ and F^{-1} or D^{-1} PAs respectively exhibit the highest and lowest value of F_I. Since F_I is almost identical for different flavors of class-E/F amplifier, X_{opt} is not a function of our tuning strategy. Fig. 5.4 also confirms this reasoning.

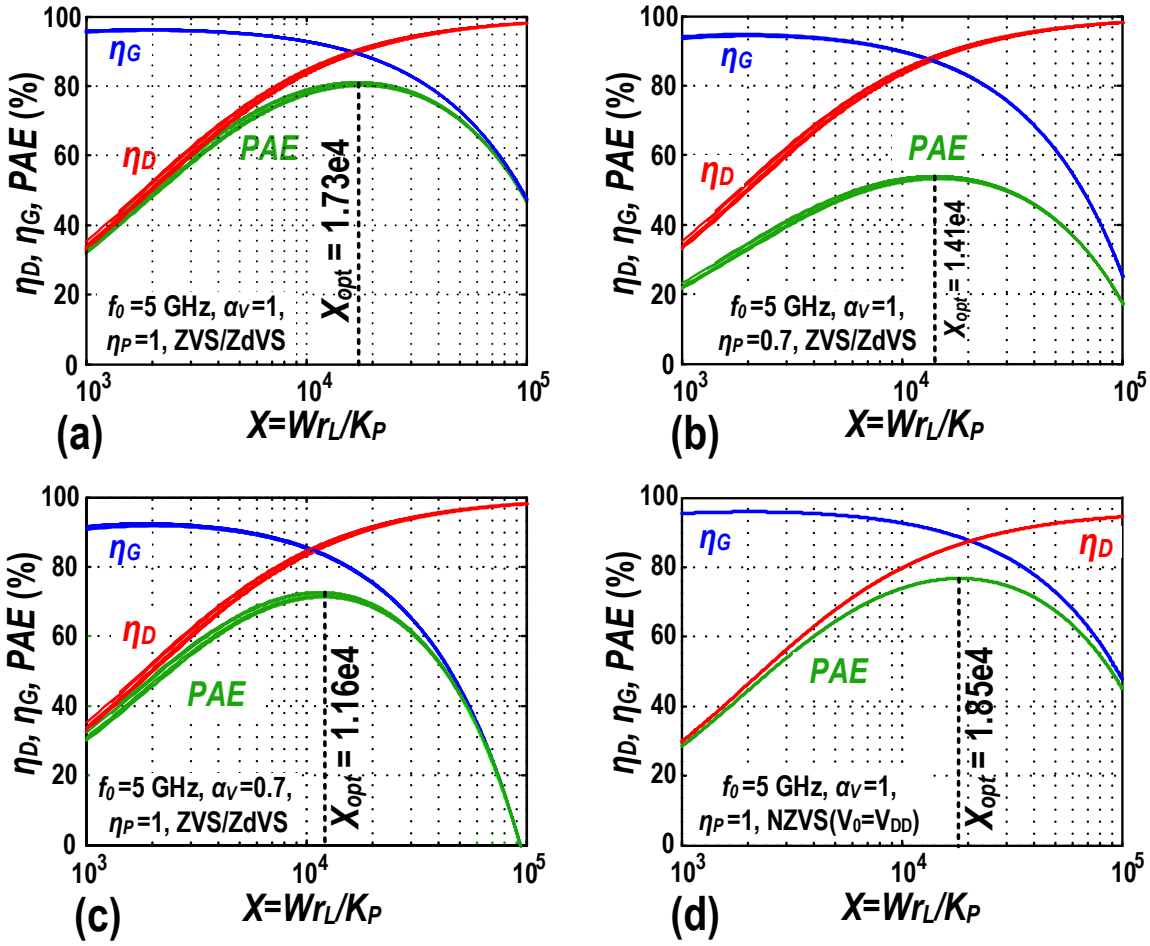


Figure 5.4: Drain, gain and power added effeciency for different flavors of class-E/F PA versus X-factor for technology parameters of $\overline{R_{on}} = 850\,\Omega\mu m$.

The optimum size of the transistor can be estimated by exploiting X-factor definition.

$$W_{opt} = \frac{K_P F_I \overline{R_{on}}}{r_L}\left(\alpha_V \sqrt{\frac{\eta_p}{\epsilon \overline{R_{on}} C_{in} f_0}} - F_I\right) \tag{5.54}$$

The transistor optimum size is a linear function of the PA's output power. Furthermore, W_{opt} reduces at higher frequencies, which makes the PA more sensitive to the transistor's parasitic output capacitance and its channel on-resistance. Beyond W_{opt}, the η_G drop is more severe than η_D improvement. Consequently, it is reasonable to say that the PA operates under a *gain-limited* condition. This optimum point, however, may not be achievable in some cases. It is possible that the current capability of the device $W_{opt}\overline{I_{out}}$ becomes smaller than the required peak current, I_{peak1}, of a switched-mode PA (see Fig. 5.5 (c)) . It means the device is too small to provide the required peak current of switched-mode PA. Consequently, it is reasonable to say the PA is under *current-limited* condition. Under this situation, the optimum device size is W_{min} wherein $I_{peak1} = \overline{I_{out}} \cdot W_{min}$.

$$\overline{I_{out}} \cdot W_{min} = I_{peak1} \quad \rightarrow \quad \overline{I_{out}} \cdot W_{min} = F_{PI} \cdot I_{DC1} \tag{5.55}$$

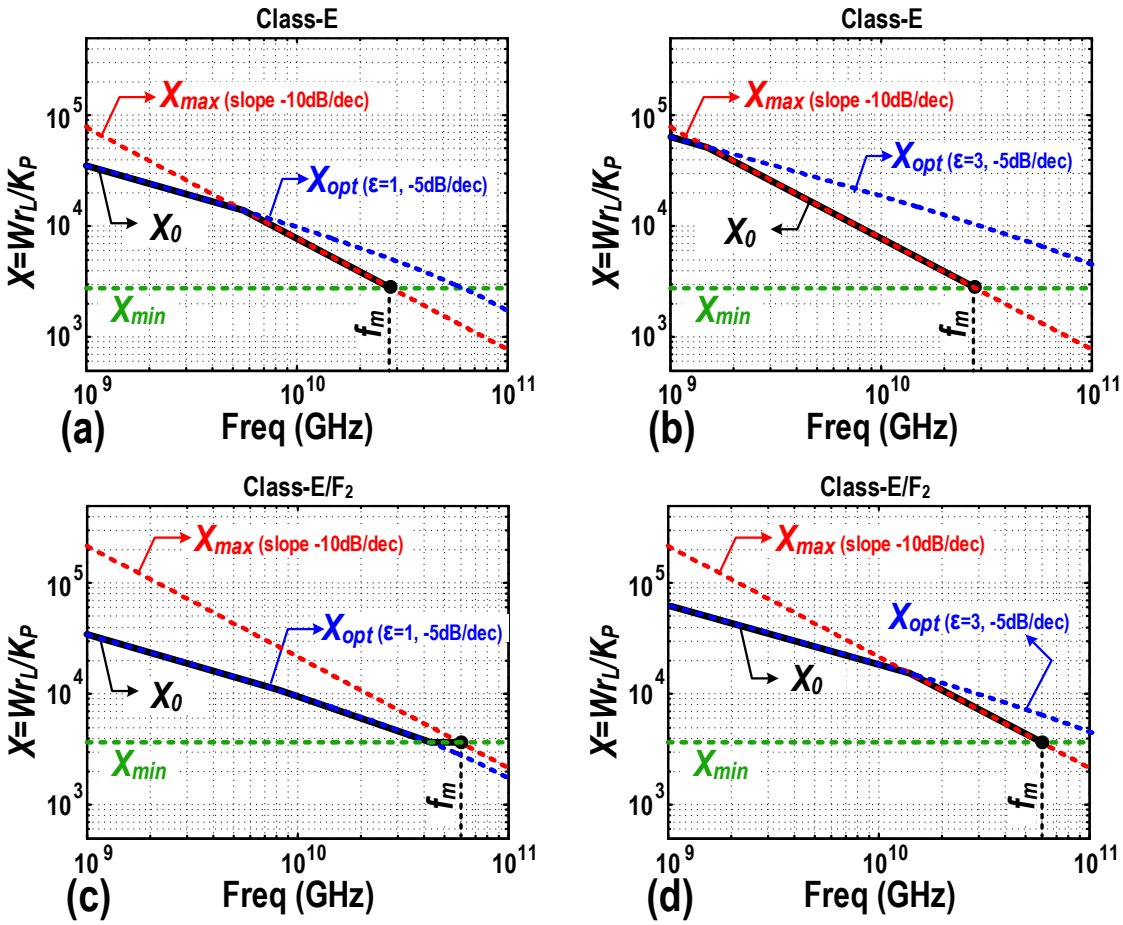


Figure 5.5: X_{opt}, X_{min}, X_{max} and X_0 of class-E and class-E/F$_2$ PA over frequency. ($\overline{R_{on}} = 850\,\Omega\mu m$, $\overline{C_{in}} = 1\,fF/\mu m$, $\overline{C_{out}} = 0.65\,fF/\mu m$, $\overline{I_{out}} = 0.6\,mA/\mu m$)

By using (5.18), (5.33) and carrying out some algebra, we will have

$$W_{min} = \frac{K_P}{r_L \cdot \overline{I_{out}}} \cdot \left(F_{PI} \cdot V_{DD} - F_I^2 \cdot \overline{R_{on}} \cdot \overline{I_{out}} \right) \tag{5.56}$$

and thus,

$$X_{min} = \frac{1}{\overline{I_{out}}} \cdot \left(F_{PI} \cdot V_{DD} - F_I^2 \cdot \overline{R_{on}} \cdot \overline{I_{out}} \right) \tag{5.57}$$

This author has rarely encountered a case which X_{opt} becomes lower than X_{min} for typical values of technology and topology parameters. It is, however, possible that the output parasitic capacitance of the device $W_{opt}\overline{C_{out}}$ becomes larger than the required C_s. It means the device is prohibited from becoming sufficiently large and the PA is under a *capacitance limited* condition. Under this situation, the optimum device size is W_{max}, wherein $C_s = C_{out}$.

$$W_{max} = \frac{C_s}{\overline{C_{out}}} \quad \rightarrow \quad W_{max} = \frac{K_C}{r_L \cdot \overline{C_{out}} \cdot \omega_0} \tag{5.58}$$

As a consequence,

$$X_{max} = \frac{W_{max} \cdot r_L}{K_P} \quad \rightarrow \quad X_{max} = \frac{1}{F_C \cdot \overline{C_{out}} \cdot \omega_0} \tag{5.59}$$

Figure 5.5 illustrates some cases where X_{opt} becomes larger than X_{max}. Consequently, the practical optimum X-factor, X_0, can be found by

$$X_0 = \begin{cases} X_{min} & X_{opt} < X_{min} \\ X_{opt} & X_{min} \leq X_{opt} \leq X_{max} \\ X_{max} & X_{opt} > X_{max} \end{cases} \tag{5.60}$$

Figure 5.6 (a) shows X_0 over frequency for different flavors of switched-mode PA. At low frequencies, X_0 is equal to X_{opt} and thus is almost identical for all flavors of class-E/F PA with the same technology parameters. However, as the frequency increases, X_0 is limited by the switch self-parasitic output capacitance and thus becomes X_{max}. As a result, the PA structures with lower F_C offer larger X_0 and width at their highest PAE. The effect of X_0 on PA's characteristic will be quantified soon.

Figure 5.6 (a) also indicates that the maximum operating frequency is different for each class of switched-mode PAs. Generally, MOS devices must satisfy two conditions for the proper switched-mode PA operation. First, transistor cut-off frequency f_{max} should be at least 3-4× higher than f_0. NMOS f_{max} is about 250 GHz in 40-nm LP CMOS. Hence, the transistors should be fast enough to turn on/off rapidly at $f_0 \leq 60$ GHz. Second, the transistor must be capable of providing the required systematic peak current during switching while its output capacitance C_{out} remains below C_s. Eq. (5.58) indicates that W_{max} reduces linearly with the operating frequency. However, W_{min} is constant over frequency. Consequently, two curves intersect at a frequency of $\omega_m = 2\pi f_m$ as shown in Fig. 5.5. Beyond that frequency, the transistor size becomes impractically small such that the device would not be able to provide the required current. Consequently,

$$X_{max} = X_{min} \quad \rightarrow \quad f_m = \frac{1}{2\pi} \cdot \frac{\overline{I_{out}}}{\overline{C_{out}}} \cdot \frac{1}{F_C \left(F_{PI} V_{DD} - F_I^2 \overline{R_{on} I_{out}} \right)}. \tag{5.61}$$

The f_m increases by migrating to a more advanced technology, which achieves transistors with a higher current capability ($\overline{I_{out}}/\overline{C_{out}}$). Another f_m improvement strategy would be using a PA with lower F_{PI} and F_C. Figure 5.7 predicts f_m for different flavors of class-E/F PA by utilizing (5.61) and waveform and technology parameters of Table. 5.1. Figure 5.7 indicates f_m can be extended to 60 GHz in 40 nm CMOS for the class-E/F_2 operation when the transistor's effective load is realized as an open circuit at the 2nd harmonic, $2\omega_0$. We will see the implementation of that PA in the following chapter.

Eq. (5.61) also indicates that f_m can be improved by reducing V_{DD} and sacrificing P_{out}. However, this conclusion is not ultimately correct, since other parameters are also affected. Indeed, V_{sat} also drops linearly by lowering V_{DD} as can be gathered from (5.30). Since the transistor operates in the triode region, its current capability is a linear function of V_{sat}. Consequently, $\overline{I_{out}}$ reduction will cancel out the improvement of a lower V_{DD} on the f_m. Hence, the maximum operating frequency is more and less constant versus V_{DD} for any switched-mode PA.

The next step is to calculate the PA's different characteristic at the optimum practical transistor size to obtain the highest possible PAE. Under this condition, the drain efficiency due

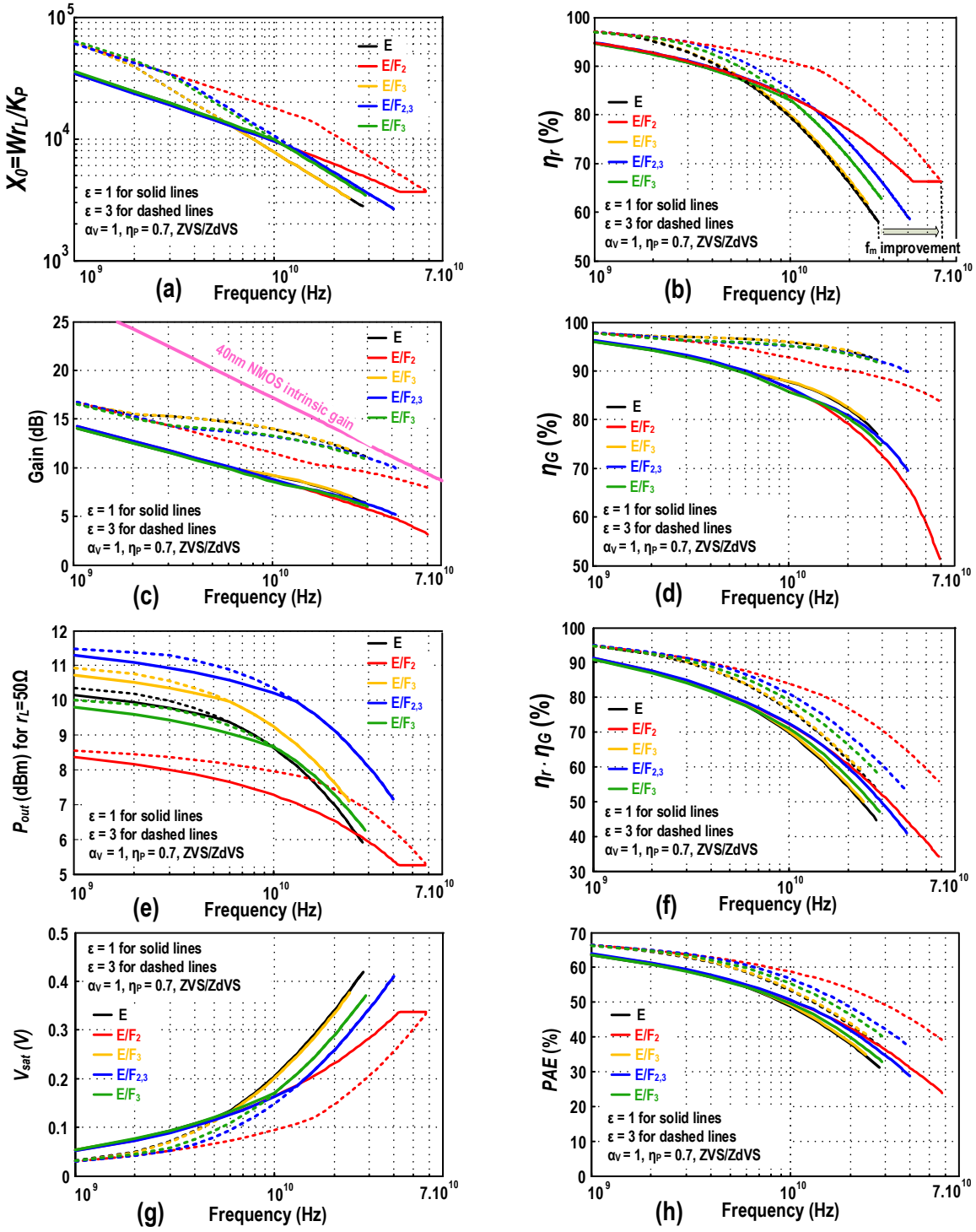


Figure 5.6: Characteristics of different flavors of class-E/F PA versus frequency at the maximum achievable PAE. (40 nm TSMC LP technology: $\overline{R_{on}} = 850\,\Omega\mu m$, $\overline{C_{in}} = 1\,fF/\mu m$, $\overline{C_{out}} = 0.65\,fF/\mu m$, $\overline{I_{out}} = 0.6\,mA/\mu m$)

to the switch on-resistance, η_r, can be estimated by replacing X_0 value of (5.60) in (5.42).

$$\eta_{r(m)} = \begin{cases} 1 - \dfrac{F_I}{\alpha_V} \cdot \sqrt{\dfrac{\epsilon \overline{R_{on}} \cdot \overline{C_{in}} \cdot f_0}{\eta_p}} & X_{opt} \leq X_{max} \\ \dfrac{1}{1 + F_C F_I^2 \overline{R_{on} C_{out}}\, \omega_0} & X_{opt} > X_{max} \end{cases} \tag{5.62}$$

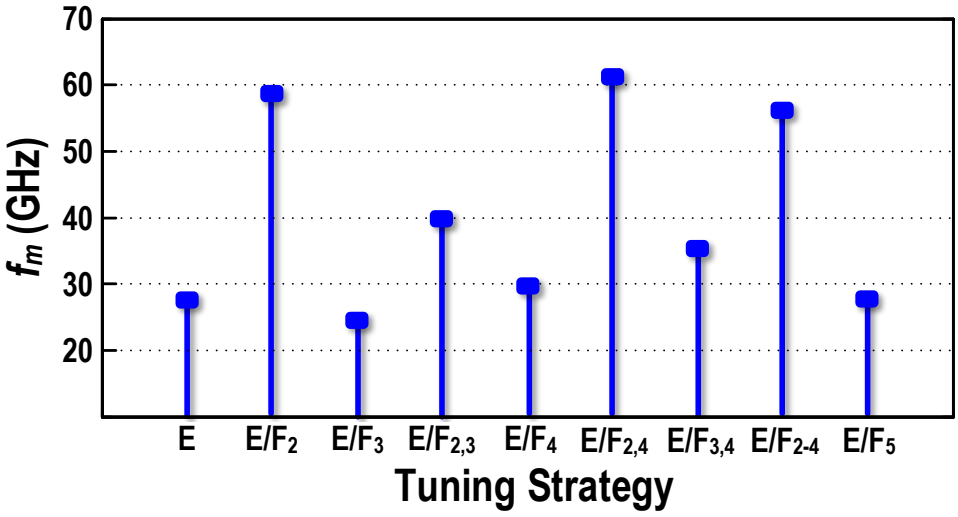


Figure 5.7: Maximum operating frequency of different flavors of class-E/F$_2$ PA. ($\overline{R_{on}} = 850\,\Omega\mu m$, $\overline{C_{in}} = 1\,fF/\mu m$, $\overline{C_{out}} = 0.65\,fF/\mu m$, $\overline{I_{out}} = 0.6\,mA/\mu m$)

Figure 5.6 (b) shows the $\eta_{r(m)}$ versus frequency for different flavors of switched-mode PA. At low frequencies, $X_0 = X_{opt}$ and thus $\eta_{r(m)}$ is almost identical for all flavors of class-E/F PAs with the same technology parameters. However, as the frequency increases, X_0 is limited by the switch self-parasitic output capacitance and thus X_{max}. As a result, PA structures with a lower F_C can tolerate a larger transistor width and demonstrate a higher $\eta_{r(m)}$ at their highest PAE. Figure 5.6 (b) also predicts $\eta_{r(m)}$=65% for 40 nm class-E/F$_2$ PA at 60 GHz. Even though the transistor acts as a switch and provides the PA's required peak current, however, the switch size is relatively small such that its R_{on} degrades $\eta_{r(m)}$ to somewhere between class-A and B.

At the highest PAE, the transistor power gain and its related efficiency $\eta_{G(m)}$ can be respectively found by substituting (5.60) in (5.49) and (5.50).

$$G_{P(m)} = \begin{cases} \dfrac{\alpha_V}{F_I} \cdot \sqrt{\dfrac{\eta_p}{\epsilon \cdot \overline{R_{on}} \cdot \overline{C_{in}} \cdot f_0}} - 1 & X_{opt} \le X_{max} \\ \dfrac{2\pi}{\epsilon} \cdot \dfrac{\overline{C_{out}}}{\overline{C_{in}}} \cdot \dfrac{\alpha_V^2 \eta_p F_C}{\left(1 + F_C F_I^2 \overline{R_{on} C_{out}}\, \omega_0\right)^2} & X_{opt} > X_{max} \end{cases} \tag{5.63}$$

At lower frequencies, the optimum size of the transistor is almost the same for different PA classes and consequently, their $G_{P(m)}$ and $\eta_{G(m)}$ are identical as can be gathered from Fig. 5.6 (c) and (d). However, PA's with a lower F_C demonstrate a lower power gain at the higher frequencies. Furthermore, the output power is also lower for PA's with lower F_C at the same V_{DD} and r_L as shown in Fig. 5.6 (e). It can be concluded that the product of power gain and maximum operating frequency is almost the same for different flavors of switched-mode PA. Consequently, higher f_m and $\eta_{r(m)}$ of class-E/F$_2$ operation is achieved through painful reduction of P_{out} and precious device G_P.

The maximum achievable PAE may be calculated by replacing X_0 value of (5.60) in (5.52).

$$PAE_{max} = \begin{cases} \eta_P \cdot \left(1 - \frac{2F_I}{\alpha_V} \cdot \sqrt{\frac{\epsilon \cdot \overline{R_{on}} \cdot \overline{C_{in}} \cdot f_0}{\eta_p}}\right) & X_{opt} \leq X_{max} \\ \eta_p \cdot \left(\frac{1}{1 + F_C F_I^2 \overline{R_{on} C_{out}} \omega_0}\right) \left(1 - \frac{\epsilon}{2\pi} \cdot \frac{\overline{C_{in}}}{\overline{C_{out}}} \cdot \frac{\left(1 + F_C F_I^2 \overline{R_{on} C_{out}}\, \omega_0\right)^2}{\alpha_V^2 \eta_p F_C}\right) & X_{opt} > X_{max} \end{cases} \tag{5.64}$$

Interestingly, at low frequencies, the highest achievable PAE is almost the same for different flavors of class-E/F PA and it is just a function of V_{DD} and the technology dependent parameters. However, the tuning strategy plays a more important role at the higher frequencies, where the practical optimum size of the transistor is determined by its own parasitic output capacitance. PAs with lower F_C demonstrate a huge PAE advantage over traditional class-E tuning. This superiority is the motivation behind the implementation of a mm-wave class-E/F_2 PA in the next chapter.

5.6 Effects of Oxide Breakdown on PA Performance

Eq (5.64) indicates that PAE_{max} can be improved by utilizing a larger $\alpha_V = V_{DD}/V_{DDBF}$. Unfortunately, V_{DDBF} reduction will increase $\overline{R_{on}}$ with an adverse effect on the PA's efficiency. On the other hand, increasing PA's supply voltage is beneficial for better PAE. It can be understood in the way that the transistor's on-resistance loss P_{ron} results from the switch current, not V_{DD}. One can increase V_{DD} while reducing the device current simultaneously to get the same P_{out} but with a lower P_{ron} and thus higher PAE. Consequently, it is suggested to choose V_{DD} as high as possible. However, this voltage/current trade-off can be applied as long as the peak drain-gate voltage remains below a gate-oxide breakdown voltage V_{BK}. By utilizing the F_V definition and replacing V_{sat} by (5.32), the maximum α_V may be estimated by

$$\alpha_{V-max} = \frac{V_{BK}}{V_{DDBF}} \frac{X + \beta}{F_V \cdot X + \beta} \tag{5.65}$$

By replacing X-factor with the X_{opt} equation, α_{V-max} can be simplified to

$$\alpha_{V-max} = \frac{1}{F_V} \left(\frac{V_{BK}}{V_{DDBF}} + F_I \cdot (F_V - 1) \sqrt{\frac{\epsilon \cdot \overline{R_{on}} \cdot \overline{C_{out}} \cdot f_0}{\eta_P}}\right) \tag{5.66}$$

As expected, PA structures with a lower F_V offer higher α_V and thus better PAE. V_{BK} is a strong function of a transistor technology, temperature and gate oxide area. It is well known that the oxide breakdown can be described by the Weibull distribution [14]:

$$F = 1 - e^{-\left(\frac{T_{BD}}{\eta_B}\right)^{\beta}} \longrightarrow \eta_B = T_{BD} \left(-ln\left(1 - F\right)\right)^{-1/\beta} \tag{5.67}$$

where F is a cumulative failure probability and T_{BD} is a random variable for time-to-breakdown. η_B is a characteristic time-to-breakdown at 63.2% failure probability and β is a Weibull shape slope. The solid circles in Fig. 5.8 (c) are extracted from literature and show the measured η_B for

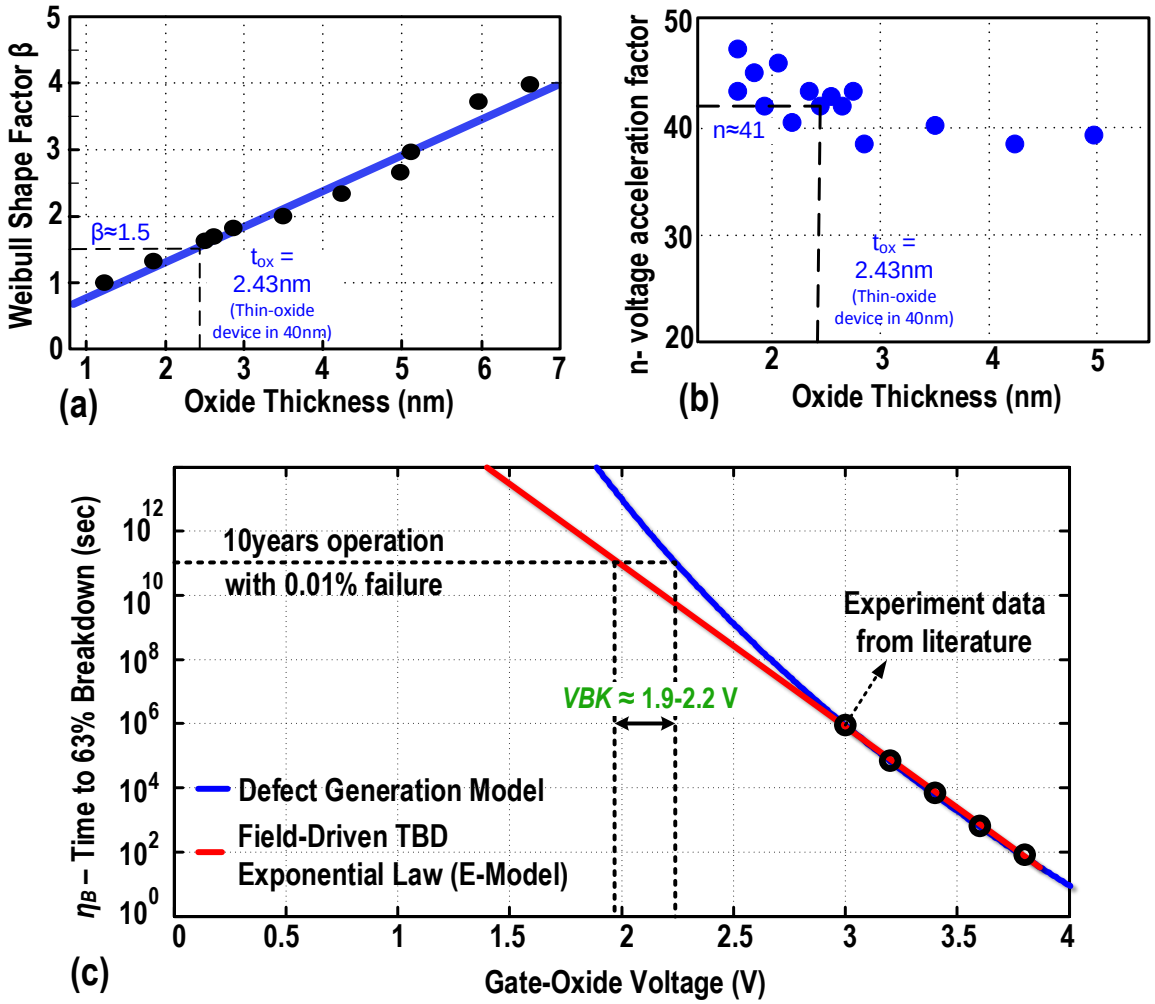


Figure 5.8: (a) Weibull slope versus gate oxide thickness extracted from [14], (b) voltage acceleration versus gate oxide thickness extracted from measurement results in [98], (c) η_B versus gate-oxide voltage. The data points (solid circles) are extracted from literature [110].

a gate-oxide thickness of 2.3 nm, an area of 10^3 μm^2 and a temperature of 140°C [110]. However, the measured η_B are acquired at relatively short measurements to the required product lifetime (e.g., 10 years). Consequently, means of voltage and temperature acceleration models are needed to estimate η_B at lower gate-oxide voltage, V_{ox}.

The field-driven E-model refers to the experimental observation that T_{BD} data can be characterized by $T_0 \cdot e^{(-\gamma_e \cdot E_{ox})}$, where T_0 and γ_e are curve fitting parameters, and E_{ox} is the electric field across the gate-oxide [111]. The η variations based on E-model curve fitting are illustrated by a red line in Fig. 5.8 (c). The model can be safely ruled out for both thin and thick oxide at $E_{ox} \leq 7$ MV/cm. However, this model is not accurate at $V_{ox} \leq 2\,V$. Nevertheless, it is possible to use E-model as a conservative projection [110].

A more realistic projection is the physics-based breakdown model [110] [14], which considers both tunneling current and defect generation phenomena. Based on this model, η_B for a given circuit with arbitrary characteristics (A_{ox}, V_{ox} and T_{ox}) can be extrapolated from the reference

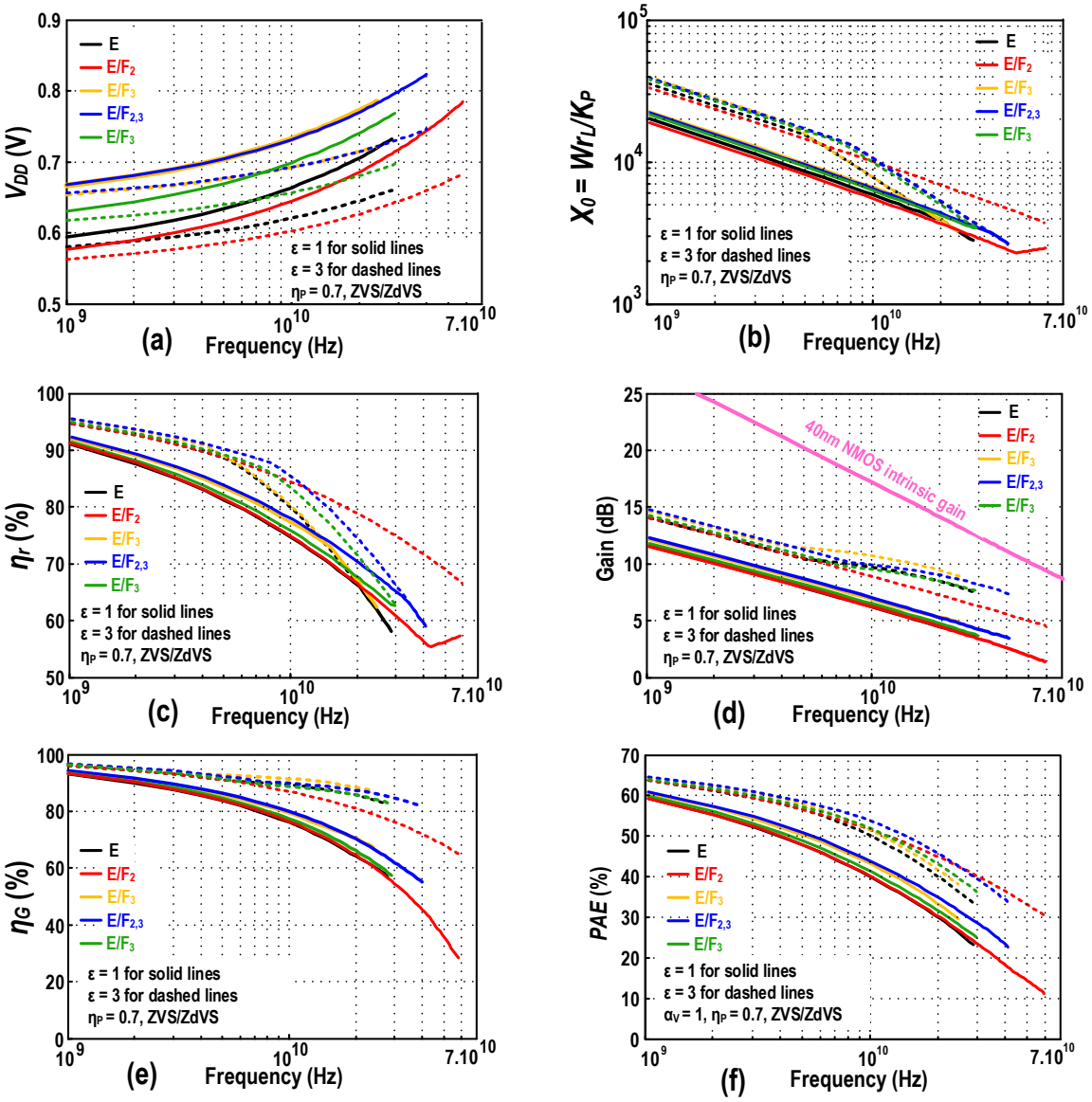


Figure 5.9: Characteristics of different flavors of class-E/F PA versus frequency at the maximum achievable PAE when taken V_{BK} into consideration. ($\overline{R_{on}} = 850\,\Omega\mu m$, $\overline{C_{in}} = 1\,fF/\mu m$, $\overline{C_{out}} = 0.65\,fF/\mu m$, $\overline{I_{out}} = 0.6\,mA/\mu m$, $V_{BK} = 2\,\mathrm{V}$)

data (x_{ref}) by

$$\eta_B = \eta_{ref} \left(\frac{V_{ox}}{V_{ref}}\right)^{-n} e^{\frac{E_a}{K}\left(\frac{1}{T_{ox}} - \frac{1}{T_{ref}}\right)} \left(\frac{A_{ox}}{A_{ref}}\right)^{-1/\beta} \tag{5.68}$$

where, (A_{ox}) is the total gate oxide area , (T_{ox}) absolute junction temperature and (V_{ox}) stress voltage across the gate oxide. Furthermore, n and $\mathrm{E_a}$ are, respectively, voltage acceleration and thermal activity energy factors. The η extrapolation based on "defect-generation" model is also added by a blue line in Fig. 5.8.

The above procedure is now applied to a 40 nm CMOS technology to determine its transistor maximum V_{ox} for less than 0.01% failure rate during 10 years of operating time. Figure 5.8 (a) indicates that Weibull slope is ≈1.5 for 2.43 nm oxide thickness in 40 nm CMOS technology. By exploiting (5.67), the required η_B should be $\sim 1.5 \cdot 10^{11}$. Figure 5.8 (c) shows η_B versus V_{ox}

projection for $A_{ox} = 10^3\,\mu m$ and T_{ox}=140°C. The plot indicates that the maximum voltage across the gate-oxide should be <2 V. Note that the gate area of most PAs is less than $10^3\,\mu m$, which translates to a slightly higher maximum V_{ox} as implied in (5.68).

By considering $V_{BK} = 2\,V$, Fig. 5.9 (a) shows the maximum allowed V_{DD} for a single transistor PA versus frequency. Note that α_{V-max} is only function of F_V and F_I among different waveform FoMs, which are almost identical for all switched-mode PAs as can be gathered from Table 5.1. Consequently, the maximum allowed V_{DD} are similar for different flavors of the class-E/F amplifier.

Figures 5.9 (b)-(d) illustrate different characteristics of switched-mode PA versus frequency when taken V_{BK} into consideration. As a general result, the main specifications of various flavors of class-E/F PAs are very similar at low frequencies (i.e. ≤7-8 GHz). However, as frequency increases, PAs with lower F_C exhibit higher $\eta_{r(m)}$ and PAE_{max} at the price of lower gain and output power.

5.7 Single Device Versus Cascode Structure

The output power of a single-transistor switched-mode PA is limited by the maximum allowed V_{DDmax} due to the time dependent dielectric breakdown (TDDB) phenomenon. It is well-known that the PA's voltage supply can be linearly increased by using cascode devices. In this section, different characteristics of cascode switched-mode PA will be quantified and compared to a single-device scenario. For simplicity, the size of all cascode transistors is assumed to be identical. Note that the effective value of some technology dependent parameters, like $\overline{C_{out}}$, $\overline{C_{in}}$, and $\overline{I_{out}}$, are the same as with a single-device PA. However, the effective $\overline{R_{on}}$ and V_{DDmax} increase linearly by a number of cascode devices, N. Furthermore, waveform FoM parameters are a function of the tuning strategy and do not change with N. Consequently, by utilizing the effective values for technology-dependent parameters, all derived equations of the previous sections are also valid for the cascode structures.

Figure 5.10 compares class-E/F_2 PAs' characteristics for single and cascode structures. The maximum operating frequency, f_m is the first victim of the cascode structure. Except V_{DD} and $\overline{R_{on}}$, other variables of f_m equation (see (5.61)) are identical for both single-device and cascode PAs. However, V_{DD} and $\overline{R_{on}}$ are twice for the cascode structure, resulting in 2× reduction of f_m. However, the output power, gain, $\eta_{G(m)}$ and PAE_{max} of the cascode structure are higher than with the single-device PA at their optimum points for the same load and technology. Consequently, the cascode structure is beneficial for high output power PAs at relatively low frequency (i.e ≤ 10 GHz). Note that the breakdown voltage of drain-bulk junction is about 8-9 V in 40-nm CMOS technology. As a result, V_{DD} of any switched-mode PA should be lower than ≈ $2.5\,V$, which translates to a maximum of 3 or 4 cascode transistors. The bulk of NMOS transistors is isolated in SOI technology. Hence, cascoding a number of transistors is a common solution for improving P_{out} and PAE of a power amplifier but it is limited to only lower operating frequencies.

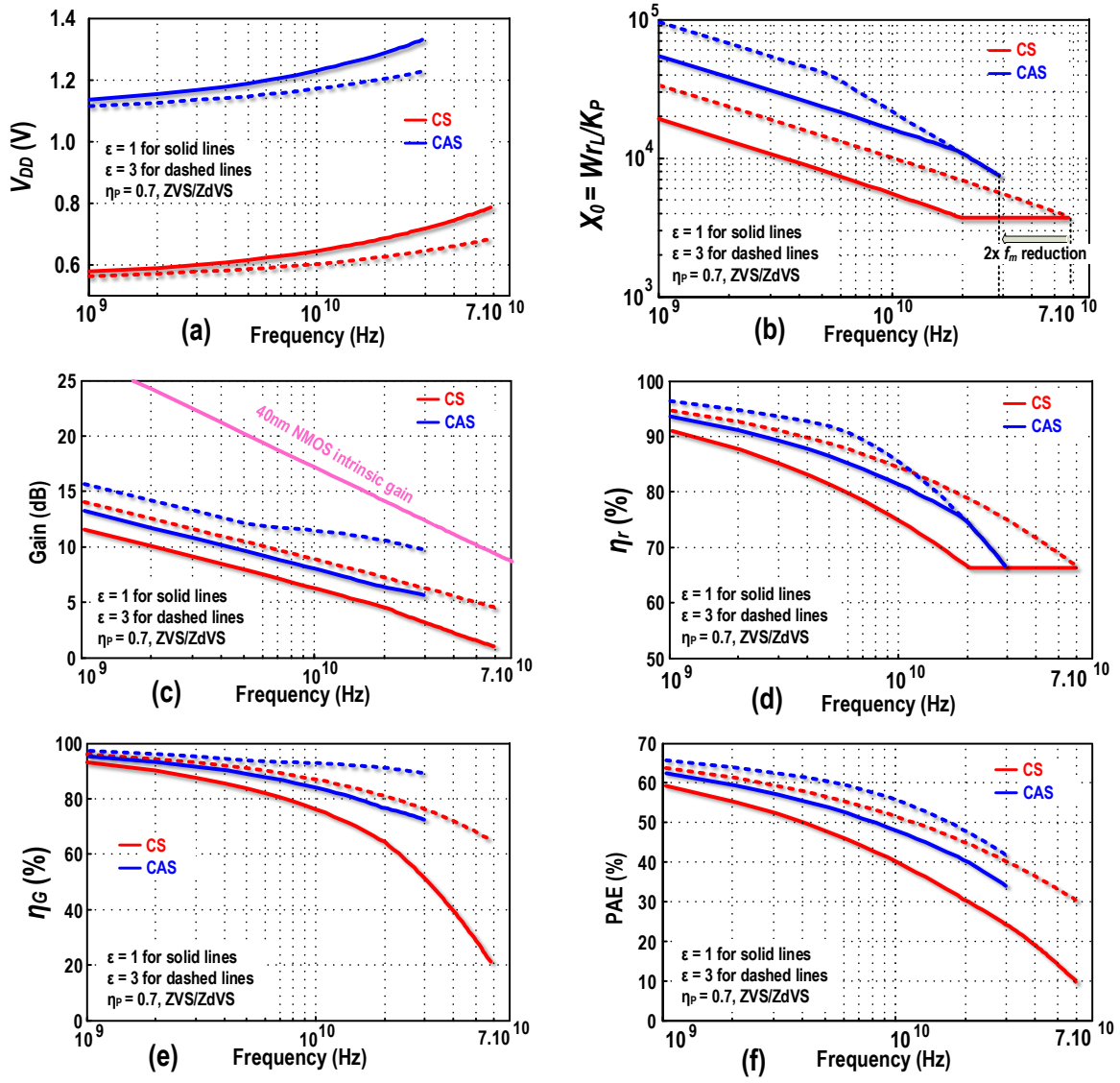


Figure 5.10: Characteristics of single-divice and cascode class-E/F_2 PA versus frequency at the maximum achievable PAE. ($\overline{R_{on}} = 850\,\Omega\mu m$, $\overline{C_{in}} = 1\,fF/\mu m$, $\overline{C_{out}} = 0.65\,fF/\mu m$, $\overline{I_{out}} = 0.6\,mA/\mu m$, $V_{BK} = 2\,\mathrm{V}$)

5.8 Benefits of Non-zero Voltage Switching

It is well-known that the zero voltage switching, ZVS, is a necessary criterion for switched-mode PAs to avoid any overlap between the transistor's voltage-current waveforms and charge loss at the off-to-on transition. Hence, ZVS could guarantee the perfect efficiency of 100% if an ideal switch would be available. However, the channel on-resistance, input, and output parasitic capacitance of the MOS transistor play an important role in adversely affecting the operation of switched-mode PAs. As explained in the previous sections, those imperfections limit significantly the PA's performance even when meeting the ZVS condition.

The above reasoning raises the question of whether introducing some charge loss can help us improve other PA's characteristics, such as on-resistance loss, waveform FoMs, gain, output power and ultimately the system efficiency. From another perspective, zero derivative voltage switching

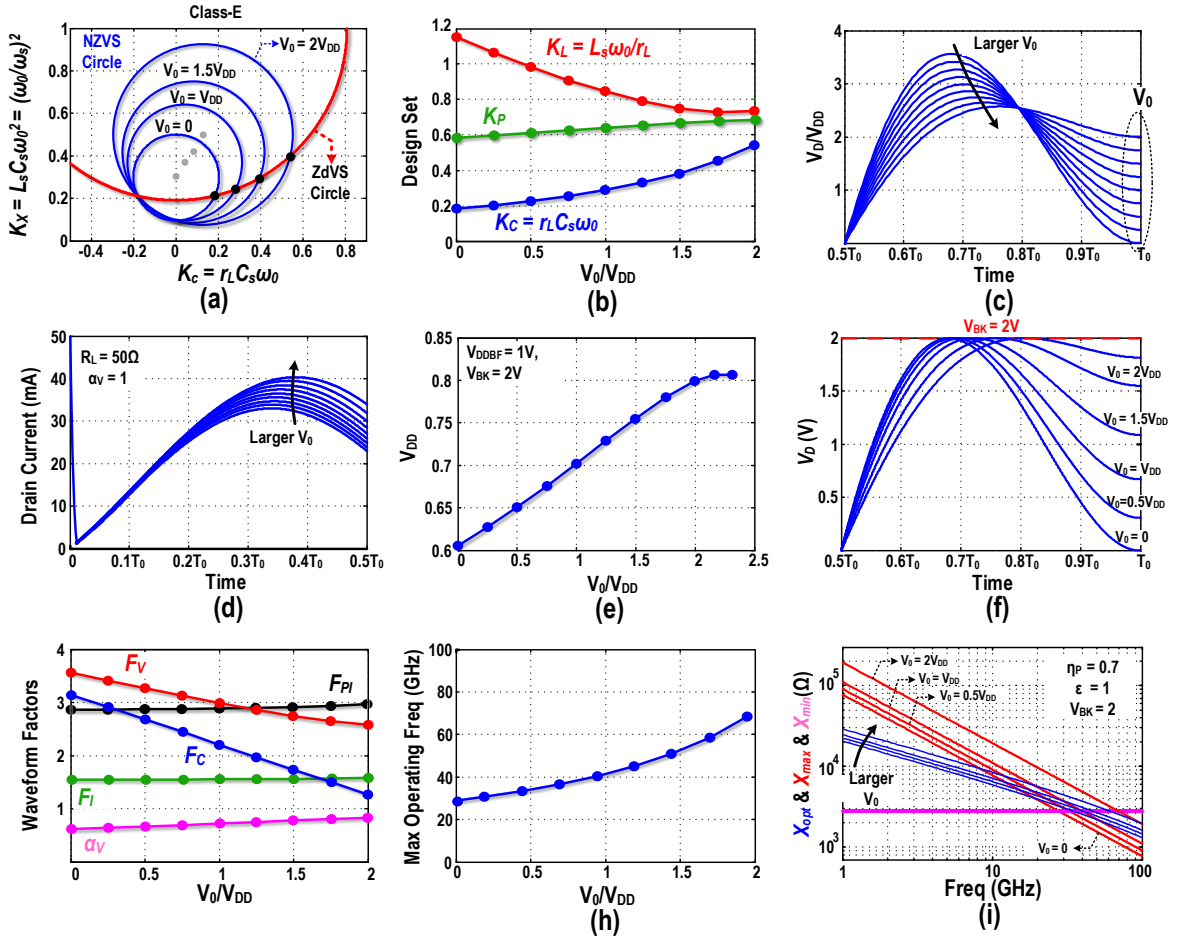


Figure 5.11: The characteristics of non-zero voltage switching PA with class-E type matching netwrok. (a) NZVS and ZdVS circles, (b) PA's design sets versus V_0, (c) Normalized drain volatage and (d) current waveforms, (e) Maximum supply's voltage and (f) shape of drain voltage by considering V_{BK} =2 V, (g) Waveform FoM parameters, (h) Maximum operating frequency and (i) X_{min}, X_{max} and X_{opt} versus V_0. ($\overline{R_{on}} = 850\,\Omega\mu m$, $\overline{C_{in}} = 1\,fF/\mu m$, $\overline{C_{out}} = 0.65\,fF/\mu m$, $\overline{I_{out}} = 0.6\,mA/\mu m$, $V_{BK} = 2$ V)

(ZdVS) alleviates the sensitivity of PA's performance to the passive component variations. Hence, it is desired to satisfy the ZdVS criterion even if PA works at the non-zero voltage switching (NZVS) condition. In this section, the benefits and constraints of NZVS/ZdVS switched-mode PAs are investigated and quantified.

At the first step, the optimal design set (K_C, K_L, K_X) of class-E/F$_X$ PA should be found through the intercept point of NZVS and ZdVS circles obtained by the matrix equations of (5.21) and (5.23). Figure 5.11 (a) illustrates those circles for the class-E tuning strategy at different off-to-on switching voltage levels, V_0. The center of NZVS circles move to right and top in the $K_X - K_C$ plane and their radius becomes larger as V_0 increases. As a result, the optimal K_C and thus shunt capacitance, C_s are larger by increasing V_0 as shown in Fig. 5.11 (b). It means the transistor is allowed to potentially have more parasitic output capacitance and become wider with less channel on-resistance. This trend shows a clear trade-off between charge and on-resistance losses in a NZVS switched-mode PA.

The required series inductance of the PA, L_s, is typically realized by a multi-turn inductor

or the leakage inductance of a transformer. As can be gathered from Fig. 5.11 (a) and (b), K_L and thus L_s, reduce with an increased V_0. Hence, the size and number of turns of the inductive part of the matching network are shrunk thanks to the NZVS operation. This leads to an improvement in the effective quality factor and insertion loss of the matching network. Consequently, there is a trade-off between the charge loss and matching network efficiency in a NZVS PA.

By replacing thus obtained matching network design sets in the matrix equation of (5.16), the voltage and current waveforms are derived and shown in Fig. 5.11 (c) and (d). Since the drain is connected to the supply via a big choke, its average voltage should be equal to V_{DD}. The peak of the drain voltage waveform and thus F_V reduce significantly at a higher V_0. This directly translates to a higher tolerated α_V and V_{DD} for NZVS PAs, as shown in Fig. 5.11 (e). Note that the transistor's on-resistance loss P_{ron} originates from the device current. NZVS PAs increase V_{DD} while reducing the device current simultaneously to get the same P_{out} but with a lower P_{ron}. This reasoning points to the second trade-off between the charge and on-resistance losses in NZVS PAs.

As the switch closes, the shunt capacitance, C_s is discharged through the transistor in a form of impulse current with a time constant τ_{cs}. Beyond the discharge span, however, the shape of the drain current is very similar to that for ZVS PA at the same tuning conditions. Hence, F_I and F_{PI} are almost identical over V_0 as shown in Fig. 5.11 (g). However, the fundamental component of the drain current, and the thus PA's power capability coefficient K_P, slightly increases with a larger V_0, as shown in Fig. 5.11 (b). Consequently, Except for F_I and F_{PI}, other waveform FoM parameters improve significantly with the NZVS operation as summarized in Fig. 5.11 (g) for a NZVS PA with a class-E type of matching network.

The maximum operating frequency, f_m, and X_{max} of the switched-mode PA are a strong function of F_C and thus they linearly improve with a larger V_0, as can be gathered from Fig. 5.11 (h) and (i), respectively. This demonstrates an explicit trade-off between the charge loss and maximum operation frequency of a NZVS PA.

Figure 5.12 compares various efficiencies and power breakdown of a class-E type of matching network switched-mode PA at the ZVS and NZVS criteria. Note that the PAs' supply voltage is assumed to be fixed for left-side figures (a, c, and e). However, V_{DDPA} is adjusted such that the peak drain voltage of the PA remains constant at $V_{BK} = 2\,V$ for the right-side figures (b, d, and f). The trend of η_G and η_D versus X-factor are shown in Fig. 5.12 (a) and (b). Since the output power is ideally not a function of the switch size, the power gain and η_G should be higher at small X-factors. However, the device channel resistance and thus η_D improve as X-factor grows. Consequently, the optimum PAE happens somewhere between those regions. Since K_P is larger for the NZVS operation, the switch can generate higher P_{out} at the same transistor width and input power. As a result, the device power gain and thus η_G is slightly higher for the NZVS operation at the same X-factor. However, the η_D is less for the NZVS switched-mode PA due to its additional charge loss. Consequently, the highest achievable PAE occurs at the larger X-factor, and thus the device width, for NZVS operation. Furthermore, the $\text{PAE}_{\max}$ is just $\leq 10\%$ lower for the extreme case of $V_0/V_{DD} = 1.5$.

Figures 5.12 (c) and (d) show the breakdown of PA's DC versus the transition voltage level, V_0, at $\text{PAE}_{\max}$. All power levels are normalized to P_{DC} of a traditional ZVS class-E PA. For $V_0/V_{DD} \leq 0.5$, the charge loss, P_{Cs}, is negligible compared to the wasted power due to device

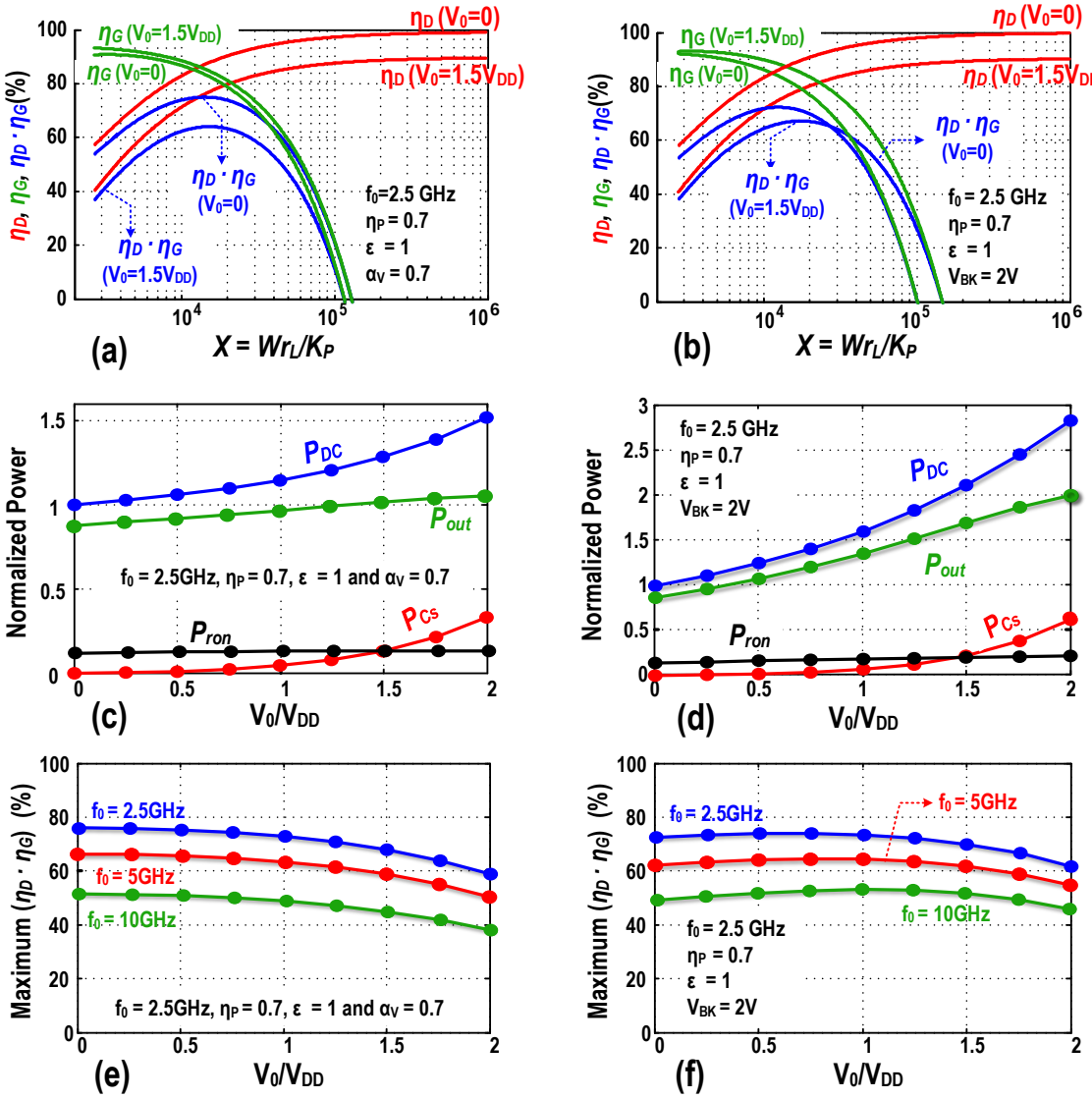


Figure 5.12: Different characteristics of non-zero voltage switching PA with class-E type matching netwrok. (a), (b) The drain and gain efficiencies versus X-factor, (c), (d) the normalized power breakdown of PA versus V_0, (e) and (f) maximum achievable product of drain and gain efficiencies versus V_0. Note that the V_{DD} is constant over V_0 in the left-side figures. However, the maximum drain voltage is kept fixed at V_{BK} for the right-side figures.

channel resistance, P_{ron}. However, P_{Cs} grows quadratically with V_0 in NZVS operation and finally becomes the dominant loss mechanism for $V_0 \geq 1.5V_{DD}$. As aforementioned, the optimum device width becomes larger as V_0 grows, reducing the device channel resistance. However, the switch current slightly increases with a larger V_0, as can be gathered from Fig. 5.11 (d). Consequently, those effects almost cancel out their influence on P_{ron}, making it insensitive to the V_0 variations. The output power, P_{out} also increases in the NZVS operation due to two phenomena. First, the fundamental component of the drain voltage-current waveforms and thus K_P increase by a larger V_0. Second, the PA's supply voltage can be raised to higher values due to the F_V reduction as suggested in Fig. 5.11 (e). The P_{DC} should also increase to cover the additional output power and P_{Cs} loss.

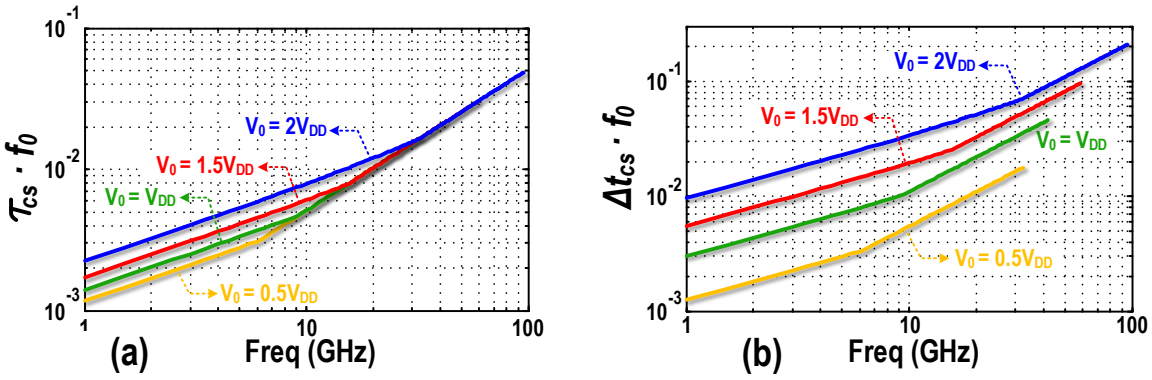


Figure 5.13: (a) The shunt capacitance discharge time constant τ_{cs} and (b) its discharge time Δt versus frequency for different V_0.

In NZVS operation, the improvement of PA's vital parameters, such as F_V, F_C, K_C and K_P can easily compensate the side effect of additional charge loss on the maximum achievable PAE. As shown in Fig. 5.12 (e), even at the constant V_{DD}, the PAE_{max} remains at the same level for $V_0 \leq 0.75V_{DD}$. More interestingly, as evident from Fig. 5.12 (f), the PAE reaches its maximum at $V_0 \approx 0.75V_{DD}$ while V_{DDPA} is adjusted such that the peak drain voltage of PA remains constant at $V_{BK} = 2\,V$.

Note that the insertion loss of the matching network has been considered and stays the same for different V_0 in this analysis. However, as mentioned before, K_L and thus the inductive part of the matching network is shrunk as V_0 grows. It leads to a higher quality factor for the matching network, and, consequently the superiority of NZVS operation is extended from the system efficiency standpoint.

For the sake of simplicity of the above analysis, it was assumed that the shunt capacitance discharge is completed within a small fraction of the device turn-on time. The validity of that assumption is investigated in this section. The time constant of the discharge current is derived by

$$\tau_{cs} = \frac{\overline{R_{on}} \cdot C_s}{W}. \tag{5.69}$$

Using the definitions of K_C and X-factor, τ_{cs} can be written as

$$\tau_{cs} = \frac{\overline{R_{on}}}{X \cdot F_C \cdot \omega_0} \longrightarrow \frac{\tau_{cs}}{T_0} = \frac{\overline{R_{on}}}{2\pi \cdot F_C \cdot X} \quad . \tag{5.70}$$

Figure 5.13 (a) illustrates the period-normalized discharge time constant versus frequency at the PAE_{max} for a class-E type matching network in 40 nm CMOS technology. Since F_C reduces in the NZVS operation, τ_{cs} increases with a larger V_0. As can be gathered from Fig. 5.13 (a), τ_{cs} only occupies a small fraction of the switch on-state time. Consequently, it is possible and convenient to model the discharge event by an impulse current flowing to ground through the transistor. Note that X-factor can be as large as X_{max} at the extreme condition. It sets a minimum limit for τ_{cs}, which can be estimated by

$$\left(\frac{\tau_{cs}}{T_0}\right)_{min} = \overline{R_{on}} \cdot \overline{C_{out}} \cdot f_0 \quad . \tag{5.71}$$

As expected, the minimum achievable τ_{cs} is just a function of the technology-dependent parameters and gets improved with the technology. Unfortunately, the limited current sinking capability of practical MOS transistors changes the shape of the discharge current waveform from an impulse to a pulse with the amplitude of $\overline{I_{out} \cdot W}$ and duration of Δt_{ch}. The discharge time may be estimated by

$$\Delta t_{ch} = \frac{C_s \cdot V_0}{\overline{I_{out}} \cdot W} \quad . \tag{5.72}$$

Replacing C_s and W with $K_C/r_L\omega_0$ and $K_P X/r_L$, respectively, Δt_{ch} is calculated by

$$\Delta t_{ch} = \frac{V_0}{\overline{I_{out}} \cdot X \cdot F_C \cdot \omega_0} \longrightarrow \frac{\Delta t_{ch}}{T_0} = \frac{V_0}{2\pi \cdot F_C \cdot X \cdot \overline{I_{out}}} \quad . \tag{5.73}$$

Figure 5.13 (b) illustrates the normalized discharge time versus frequency at the PAE_{max} for a class-E type matching network in 40 nm CMOS technology. The Δt_{ch} may occupy more than 20% of the switch on-state time at the mm-wave frequencies. Nevertheless, it is possible to safely model the discharge event by a short pulse current flowing to ground through the transistor. The minimum Δt_{ch} is achieved at $X = X_{max}$, where

$$\Delta t_{ch} = \frac{\overline{C_{out}}}{\overline{I_{out}}} \cdot V_0 \cdot f_0 \tag{5.74}$$

The minimum achievable Δt_{ch} is a function of V_0 and technology-dependent parameters and gets improved over the technology.

5.9 Conclusion

The precise analytical voltage-current waveforms, zero-voltage and zero-slope switching criteria and waveform dependent parameters of any flavor of a switched-mode PA have been quantified in this chapter. Closed-form equations are derived for the optimum size of the switch and different PA's characteristics, such as maximum achievable power added efficiency, PAE_{max}, output power, and maximum operating frequency. In the current CMOS technologies, the PAE_{max} is almost identical at the relatively low operating frequency of $f_0 \leq 10\,GHz$ for all flavors of class-E/F power amplifiers. However, as frequency increases, the optimum size of the switch is dictated by the transistor parasitic capacitance and, consequently, PAs with lower F_C demonstrate a higher PAE_{max}. It was also concluded that the output power and even PAE_{max} of a switched-mode PA improve in the cascode structure but at the price of $2\times$ lower maximum operating frequency. It was also shown that almost all vital parameters of the switched mode PA like F_C, F_V, K_C and K_L improve by NZVS operation such that they can easily compensate the side effect of additional charge loss on the maximum achievable PAE. Interestingly, PAE_{max} is even higher at $V_0 \approx 0.75 V_{DD}$ for a class-E type switched-mode PA while the drain voltage is kept below the gate-oxide breakdown threshold.

Chapter

6

A Wideband 60 GHz Class-E/F_2 Power Amplifier in 40 nm CMOS

A key challenge of 60 GHz CMOS radios is the poor efficiency of their power amplifier (PA). Employing nonlinear switched-mode PAs within digitally intensive transmitter architectures such as outphasing and direct digital-to-RF conversion can improve the total system efficiency. However, switching at mm-wave is not a trivial matter due to the substantial output capacitance and low current driving capability of CMOS transistors.

This chapter presents a fully integrated 60 GHz power amplifier in 40 nm CMOS that reaches the highest reported product of power-added efficiency and bandwidth. It is achieved through low/moderate coupling-factor transformers in preliminary stages and a proper second-harmonic termination of the output stage to enable it to operate as a class-E/F_2 switched-mode PA at the saturation point. The three-stage PA delivers 17.9 dBm saturated output power with a 20% peak PAE. It demonstrates a bandwidth of 9.7 GHz with a peak gain of 21.6 dB.

6.1 Transmitter Architectures from mm-wave Viewpoint

The wireless standard dubbed WiGig (802.11ad WiFi) enables devices to support applications that require extremely rapid communication such as uncompressed video transmission, wireless display, rapid upload/download, and wireless docking. This technology uses the 60 GHz frequency band to achieve the required multi-giga bit data rate of the aforementioned applications. Figure 6.1 illustrates the channel plan and frequency allocations of the 60 GHz band in different regions. The band comprises four channels, each 2.16 GHz wide [112]. Consequently, a transmitter must have ∼9 GHz bandwidth to support the WiGig worldwide standard.

To support the high data rate in a spectrally efficient manner, WiGig employs complex

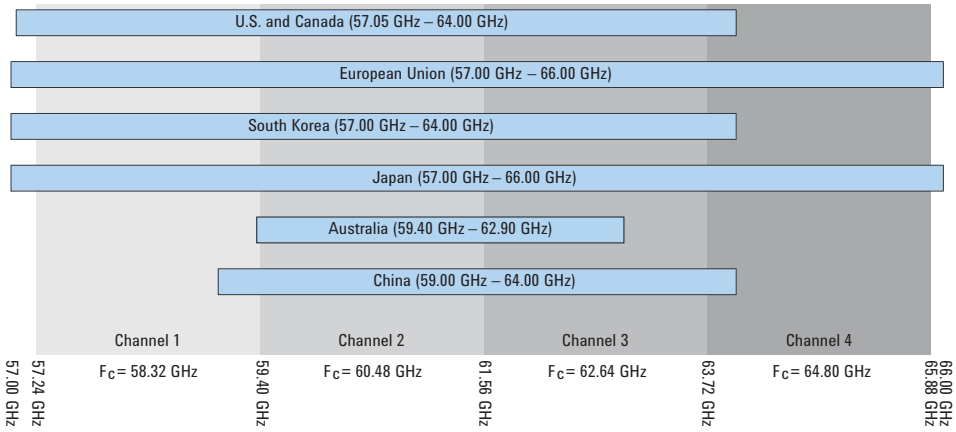


Figure 6.1: 60 GHz band channel plan and frequency allocations by region [112].

Table 6.1: WiGig data rates and modulation schemes for single-carrier and OFDM configurations.

Modulation type	Coding rate					Raw Rate (Mbit/s)					Sensitivity (dBm)					EVM (dB)				
Single Carrier																				
π/2 BPSK	1/4	1/2	5/8	3/4	13/16	385	770	962	1155	1251	-68	-66	-65	-64	-62	-6	-7	-9	-10	-12
π/2 QPSK	1/2		5/8		3/4	13/16	1540		1925		2310	2502	-63	-62	-61	-59	-11	-12	-13	-15
π/2 16QAM	1/2			5/8		3/4	3080			3850		4620	-55	-54		-53	-19		-20	-21
OFDM																				
SQPSK	1/2				5/8		693				866		-66			-64	-7			-9
QPSK	1/2		5/8			3/4	1386			1732		2079	-63	-62		-60	-10	-11		-13
16-QAM	1/2	5/8		3/4		13/16	2772		3465		4158	4504	-58	-56	-54	-53	-15	-17	-19	-20
64-QAM	5/8		3/4			13/16	5197			6237		6756	-51	-49		-47	-22	-24		-26

modulation schemes (quadrature amplitude modulation, QAM) as shown in Table 6.1. It also exploits an orthogonal frequency-division multiplexing (OFDM) scheme to mitigate multi-path effect. The use of the QAM modulation and multiple subcarriers increases the peak-to-average power ratio (PAPR) of the signal, imposing stringent linearity requirements on the transmitter. Consequently, a linear power amplifier must be used in the conventional I/Q transmitter architecture as shown in Fig. 6.2 (a) [113]. However, the efficiency of a linear class-A PA diminishes quickly by P_{out} with backing off from PA's peak power leading to a poor system efficiency (i.e., <10%) for mm-wave traditional I/Q transmitters [52, 114, 115].

To improve the system efficiency, envelope tracking architecture dynamically adjusts the PA supply voltage according to the signal envelope (see Fig. 6.2 (b)). However, the PA's input signal has a non-constant envelope and thus a linear PA is still required. In this structure, the supply voltage adaptively scales with the signal amplitude while its DC current remains constant. Consequently, the system efficiency decreases by $\sim \sqrt{P_{out}}$ with reducing its output power.

Since the realization of a simultaneous linearity and efficiency is extremely challenging, intensive research has been conducted for transmitter structures that can exploit nonlinear switched-mode PAs and yet transmit amplitude information [116]. The benefits and constraints of those structures are investigated from the mm-wave perspective.

Polar transmitter structures [117] with origins in the envelope elimination and restoration techniques (EER) [118] can further enhance the system efficiency by exploiting switched-mode PAs. In this architecture, the baseband I/Q signal is first converted to amplitude (AM) and (PM) signals. Since the PA amplifies the constant envelope PM signal, it can be non-linear

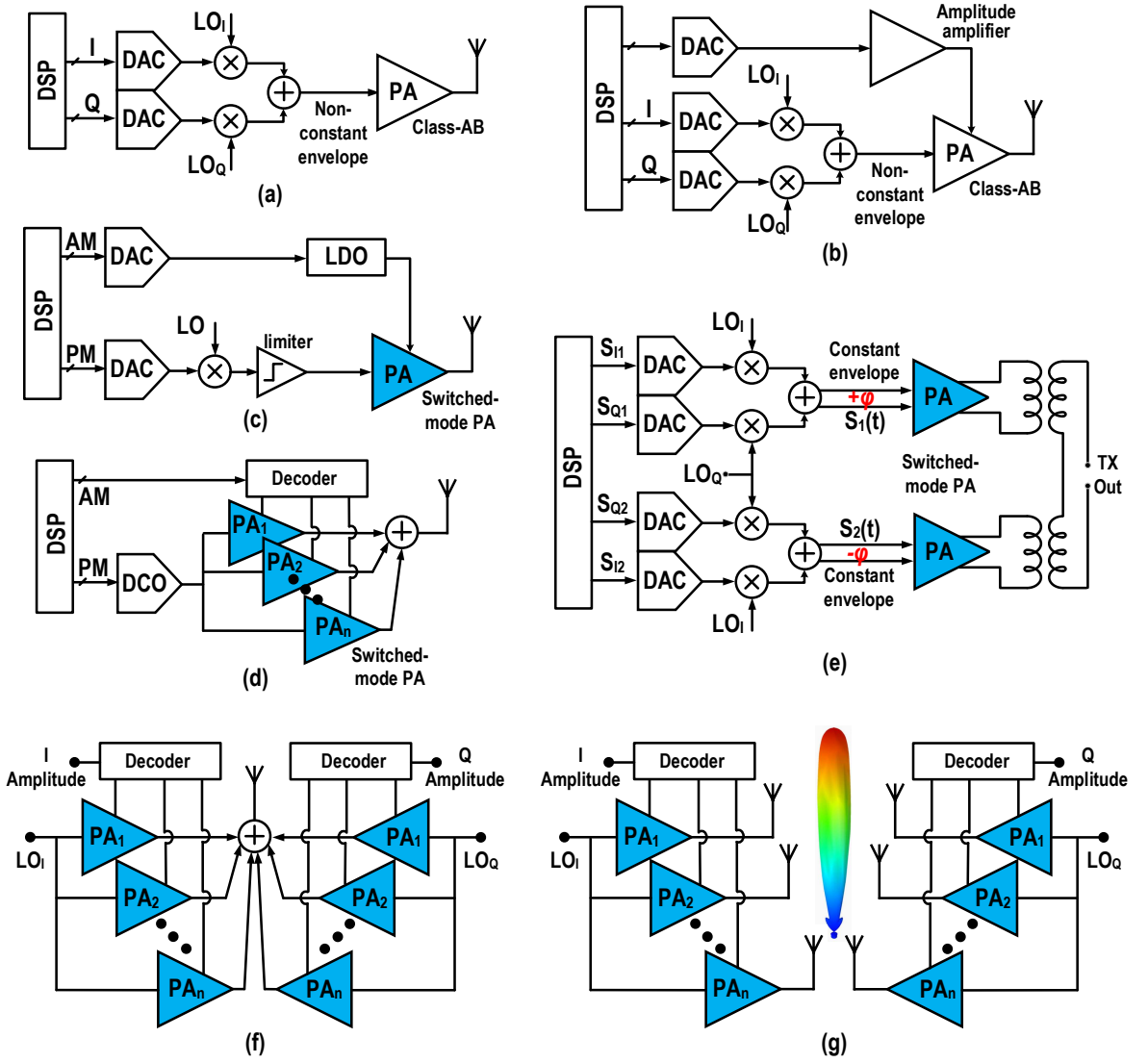


Figure 6.2: Different transmitter architectures: (a) traditional analog-intensive I/Q; (b) Envelope tracking; (c) analog-intensive polar; (d) digitally-intensive polar; (e) outphasing; (f) digitally intensive I/Q structure with on-chip and (g) spatial combining.

and thus efficient. In the analog-intensive approach, the amplitude data is also restored by modulating the PA's supply voltage as demonstrated in Fig. 6.2 (c) [119, 120]. As a consequence, PA drain efficiency remains almost constant at back-off. In the digitally-intensive approach, however, the power amplifier acts as an RF digital-to-analog converter (RFDAC) [4]. The amplitude information is restored by modulating the effective width of the PA's transistor. The PA works as a switched-mode amplifier at the maximum power. However, as P_{out} reduces, the transistor becomes smaller and thus works as a current source rather than a switch. The PA almost operates as a linear amplifier at back-off where its DC current adaptively scales by the signal amplitude while V_{DD} remains constant. Consequently, in a digitally-intensive polar structure, PA's efficiency drops by $\sqrt{P_{out}}$, and resembles the class-B behavior.

Due to a bandwidth expansion of I/Q to polar conversion, both AM and PM paths should support signals with at least 10 GHz bandwidth even for a relatively relaxed adjacent channel

leakage ratio (ACLR) of -30 dBc in the WiGig standard. However, realizing such a large BW is extremely challenging for both the phase and supply modulators. Furthermore, matching the delay between the envelope and phase paths could be very difficult [121]. Consequently, the polar architecture can hardly satisfy the data rate requirement of mm-wave transmitters.

In an outphasing architecture, the linear amplification is achieved by vector summation of two constant-envelope signals as shown in Fig. 6.2 (e) [122, 123]. Since each PA only deals with a constant envelope signal, non-linear switched-mode amplifiers can be used to maximize the peak efficiency. Since two signal paths are identical, delay mismatch is lower and easier to compensate compared with the polar architecture. Furthermore, as explained in [124], for an outphasing TX, the bandwidth of baseband circuitry (i.e., DAC) should be only 2× higher compared with the I/Q structure to reach the same error vector magnitude (EVM). The back-off characteristic of this topology is a strong function of its combining matching network. The transmitter demonstrates a class-A type behavior at back-off if an isolating combiner, such as the Wilkinson combiner, is used. The back-off efficiency of the outphasing structure improves if non-isolating combiners are used. However, the interaction between PAs results in spectral regrowth, and thus a complicated two-dimensional pre-distortion scheme is required to alleviate this phenomenon. Recently, mm-wave outphasing transmitters have been demonstrated with both transformer combining [124] and spatial combining [125]. However, both designs utilize a saturated linear PA, and their back-off curves are close to class-A behavior.

The digitally intensive I/Q modulators are a strong candidate for realization of high data rate mm-wave transmitters [93]. They do not suffer from bandwidth expansion of polar and outphasing structures due to linear summation of I and Q signals as exhibited in Fig. 6.2 (g) and (h) [126]. The structure consists of separate arrays of sub-PAs for I and Q paths. The I/Q amplitude information is realized by digitally switching on a certain number of sub PAs [127, 128]. Consequently, each sub-PA deals with a constant envelope signal and thus non-linear switched-mode amplifiers can be employed to improve the system efficiency. Furthermore, PA's DC current dynamically scales with the signal amplitude by switching off unnecessary sub-PAs. Consequently, PA's efficiency decreases by $\sqrt{P_{out}}$ at back-off output power similar to that of a class-B amplifier.

In spite of the aforementioned benefits, an implementation of the I/Q combiner is the most difficult challenge of this approach. Transformer-based combiners exhibit very small insertion loss, however, they suffer from mutual interactions between I/Q paths due to a lack of isolation [128]. Consequently, a complex two dimensional pre-distortion scheme is required for the transmitter linearization. This issue is alleviated by employing 25% duty-cycle non-overlap clocks for I and Q paths [127]. However, realizing such a clock scheme is not yet possible at mm-wave frequencies. The I/Q interaction would be completely prevented by employing non-isolating combiners such as Wilkinson. However, such combiners demonstrate higher insertion loss and thus reduce the total system efficiency. In a quadrature spatial combing TX [93], I and Q signals are summed in the far field. Consequently, the combiner insertion loss will be negligible, and the isolation between I and Q paths can easily exceed 20 dB by separating I/Q antenna greater than half wavelength. Unfortunately, I/Q summation is ideally realized only at one

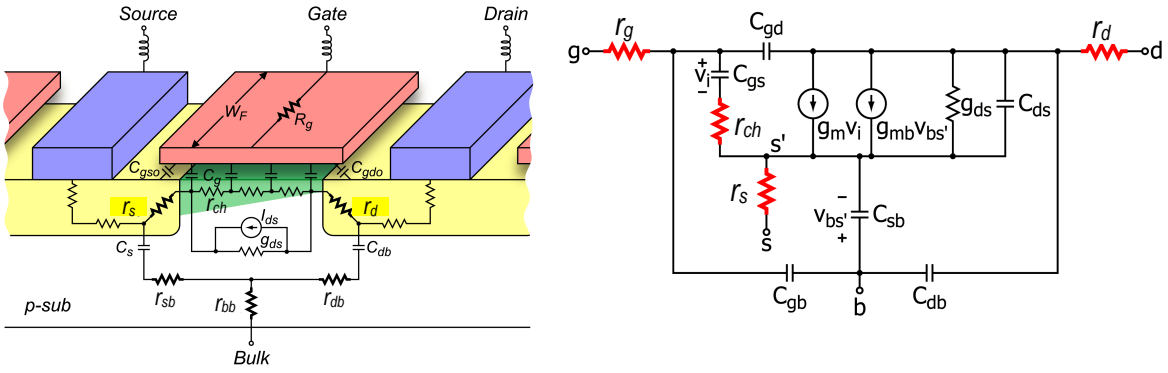


Figure 6.3: Structure and circuit model of a MOSFET with its parasitic elements [129].

particular spatial angle. Hence, transmitter EVM gradually degrades when the receiver is moved away from that angle. This issue can potentially limit the application of this structure to cellular backhauls where the receiver is spatially fixed and highly directional antennas are used.

To conclude this section, a key challenge of 60 GHz CMOS radios is the poor efficiency of their power amplifier. Employing nonlinear switched-mode PAs within digitally intensive transmitter architectures such as outphasing and direct digital-to-RF conversion can improve the total system efficiency. However, switching PAs are rarely seen at mm-wave due to the large output capacitance and low current capability of CMOS transistors. The only such report, Chen et al. [93], exploits a special two-turn inductor to realize a switch-mode PA at 60 GHz. However, that inductor must be large enough to simultaneously satisfy the required reactance for both fundamental and second harmonic. Consequently, its relatively large inductance limits the output transistor size so the PA output power is ≤ 10 dBm.

In this chapter, we propose a new architecture of a fully integrated *switched-mode* wideband 60 GHz PA in standard digital 40 nm CMOS. With a proper second-harmonic termination of its output matching network, the required systematic peak current of the final stage is reduced such that it can act as a class-E/F_2 *switched-mode* PA at saturation. Transformers of low/moderate coupling are also utilized in the preliminary stages to improve the overall bandwidth. We also propose a technique to stabilize transformer-based mm-wave amplifiers against various modes of undesired oscillations.

6.2 Optimizing Active Devices at mm-wave Frequencies

The output power, gain, and efficiency of an mm-wave power amplifier can be significantly improved by optimizing the maximum frequency of current gain (f_t) and power gain (f_{max}) of the NMOS transistor. Both cut-off frequencies are strong functions of device and interconnect parasitics and may be estimated by the following equations [129].

$$f_t = \frac{1}{2\pi} \cdot \frac{g_m}{C_{gs} + C_{gd} + C_{gb}} \tag{6.1}$$

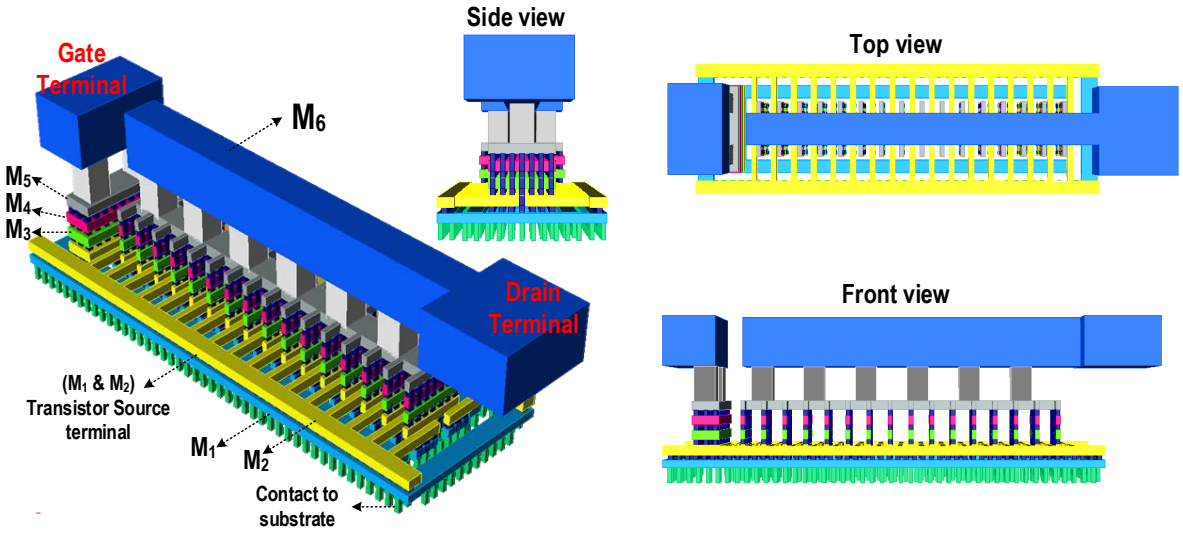


Figure 6.4: Optimal layout of 32·1μm/40nm transistor.

$$f_{max} = \frac{g_m}{2\sqrt{r_g\left(g_m\frac{C_{gd}}{C_{gg}}\right) + (r_g + r_{ch} + r_s)g_{ds}}} \tag{6.2}$$

where, g_m is the transistor's transconductance gain, C_{gg} is its total gate capacitance, g_{ds} is the device's output conductance, and r_g, r_{ch} and r_s are, respectively, the gate, channel, and source resistances as shown in Fig. 6.3. The f_{max} can be improved by increasing a device g_m (thus its power consumption) and minimizing the gate-drain (C_{gd}) along the gate resistance (r_g). The gate is made of the salicide polysilicon and its resistances is given by [130, 131]

$$r_g = \kappa \cdot \frac{1}{3} \cdot \frac{W_F}{N_F L_F} \cdot R_{g,sh} \tag{6.3}$$

where, $R_{g,sh}$ is the sheet resistance of the polysilicon gate, W_F and L_F are the finger width and channel length, respectively, and N_F is the number of transistor's finger. The factor 1/3 accounts for the distributed nature of the RC line across the channel. The κ factor is equal to unity for a gate contacted on one side and to 1/4 when the gate is connected by metal lines on both the source and drain sides.

As can be ascertained from (6.2) and (6.3), at the constant transistor width, W, r_g, and thus f_{max} can be improved by increasing N_F (lowering W_F). However, at some point, this approach stops increasing f_{max} because the device layout becomes larger and longer routes are required to connect the transistor's different terminals from its multiple fingers, leading to a larger parasitic capacitance (i.e., C_{gd}). It also introduces additional resistive losses as well as reduction in the device power gain due to resistive/inductive source degeneration. Considering both scenarios, finger widths of 0.8-1.5 μm and N_F of ~100 are an optimal set for maximizing f_{max} and maximum stable gain (MSG) of MOS transistor at 60 GHz in 40 nm CMOS technology.

Figure 6.4 shows the layout of unit transistor cell which is designed to optimize the transistor interconnect parasitic and power gain[1]. It includes 32 fingers with a finger width of 1 μm (i.e., 32×1μm/40 nm), occupying an area of 6.7×3.2 μm^2. As suggested in (6.3), the gate poly fingers

[1]This structure is first proposed in [132] and adopted here by some modifications.

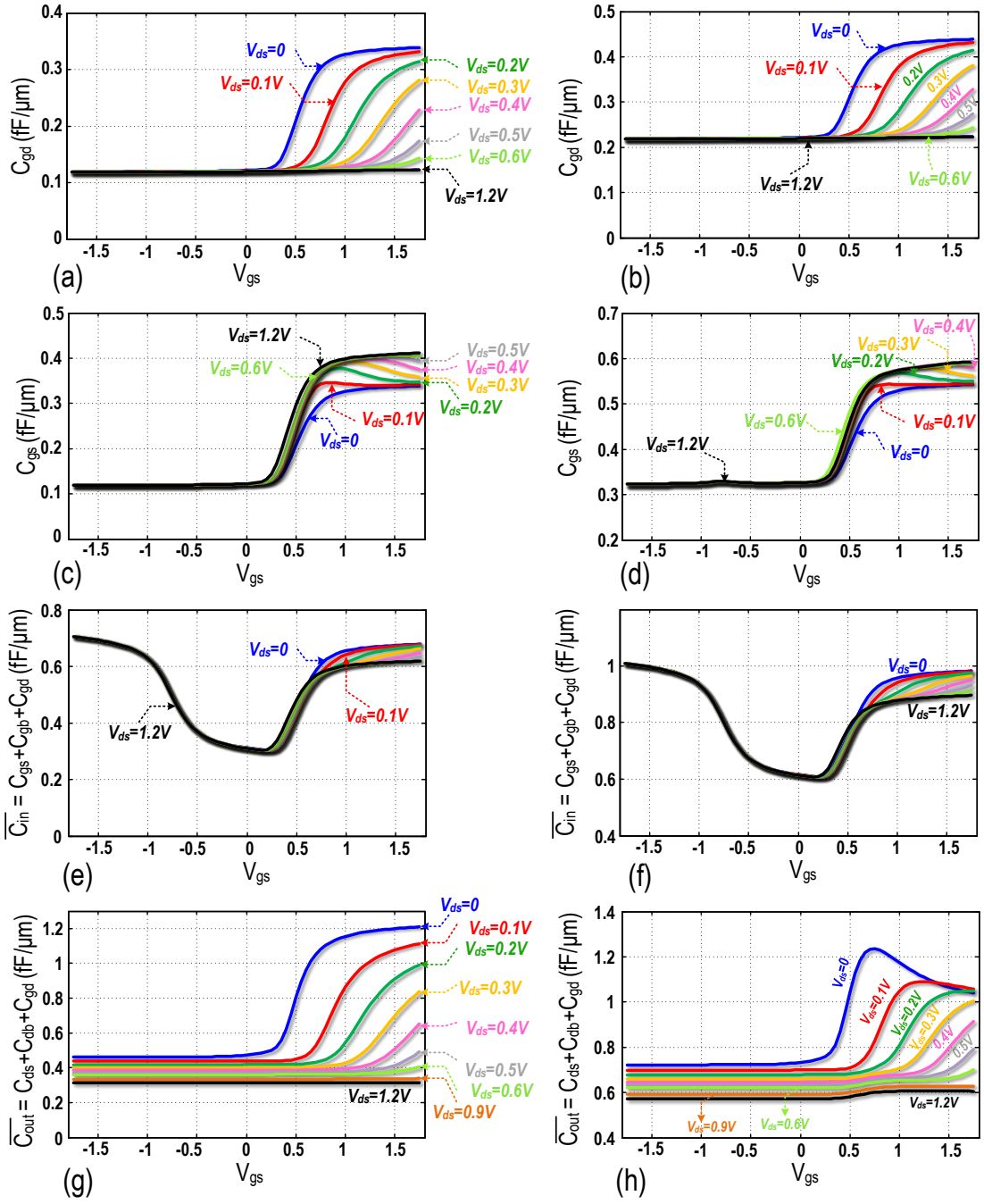


Figure 6.5: Normalized parasitic capacitances of an NMOS transistor excluding (left) and including (right) extrinsic interconnect parasitics.

are brought out from both transistor sides. Double contacts connect the gate poly fingers to metal-1. Two metal-1 line with width of 0.25 μm connect all gate fingers of each side and travel the entire distance to one end of the layout. Finally, vias_{1-6} connect the gate terminal to metal-6 for further top-level routings.

Each of the source fingers are first connected to metal-2 by 6 parallel via_{1-2}. The source nodes are then brought out from both transistor sides on metal-2 and connected to the bulk ring at a 0.5μm distance to the device. Source lines on metal-2 perpendicularly cross the gate lines on metal-1, increasing device C_{gs}. Note that C_{gs} demonstrates much less effect on the

device stability, f_{max} and power gain rather than C_{gd}. Hence, minimizing interconnect parasitic capacitance of C_{gd} should be the first priority of layout optimization. To prevent the resistive and inductive degeneration, the source lines are then distributed on both metal-1 and metal-2 with width of 1.5 μm.

Each of the drain fingers are first connected to metal-5 by 7 parallel via$_{1-5}$. The drain line runs on top of the transistors on both metal-5 and metal-6 at a width of 0.5 μm to keep the current density well below the maximum rate allowed by the manufacturer. Finally, the drain node is brought out from the opposite side of gate terminal, minimizing the overlap between the gate and drain and thus the extrinsic C_{gd}.

Figure 6.5 illustrates normalized parasitic capacitances of an NMOS transistor in different regions of operation with and without the extrinsic interconnect parasitics. For the intrinsic device, C_{gd}/W=C_{gs}/W=C_{ov} $\approx$ 0.1 fF/μm while the transistor is off. The C_{gd}/W remains constant to C_{ov} in the saturation region. However, the nonuniform vertical electrical field of the gate oxide along the channel increases C_{gs}/W to $\approx C_{ov} + 0.66LC_{ox} \approx 0.4$ fF/μm [133]. If the device operates in the deep triode, the source and drain will almost have identical voltages. Hence, the gate channel capacitance, $WL \cdot (C_{ox} \approx 14\,\text{mF}/\mu\text{m}^2)$, must be equally divided between gate-source and gate-drain terminals. Therefore, C_{gd}/W=$C_{gs}/W \approx C_{ov}+0.5LC_{ox} \approx 0.33$ fF/μm. As can be gathered from 6.5 (a-d), the interconnections increase the C_{gd}/W and C_{gs}/W of the intrinsic transistors by 0.1 fF/μm and 0.2 fF/μm, respectively. Consequently, the normalized equivalent input and output capacitance ($\overline{C_{in}}$&$\overline{C_{out}}$) may be respectively estimated by $\sim$1 fF/μm and $\sim$0.65 fF/μm.

To deliver even higher power to the load, more unit transistors can be placed next to each other and connected in parallel to realize a larger device [134]. Figure 6.6 illustrates the schematic and layout of a pseudo differential amplifier with naturalization capacitors. Each device consists of 4 unit transistors which are located on both sides. The gate and drain terminals of unit transistors are directly connected by thick metal layers to minimize the length and resistance of interconnections. The source of transistors are connected to the ground plane which is realized by stacking the first two lower metal layers. The neutralization capacitors are made by metal-oxide-metal capacitors and placed in the middle of the layout.

A key advantage of this structure is that the normalized input and output capacitance of the transistors, and thus the maximum operating frequency of the switched-mode PA, almost remains fairly constant with increasing the device width. However, the source current of the last unit experiences a longer path to reach the common ground node of the pseudo differential amplifier, introducing a distributed impedance, Z_u, in the source network. It can be shown that the overall transconductance of the large transistor can by calculated by [135]

$$g_{m,T} = \frac{N \cdot g_{m,u}}{1 + N \cdot g_{m,u} \cdot \left(\frac{N \cdot Z_u}{3}\right)} \tag{6.4}$$

where, $g_{m,u}$ is the transconductance gain of the unit transistors. Eq. 6.4 indicates that, as the number of units N increases, $g_{m,T}$ rises and finally reaches a maximum. It also suggests the number of units should be well below the saturation point to avoid a waste of current. By considering $g_{m,u}$ of $\sim$25mA/V for a 32μm/40nm device at V_{gs}=0.7 V and $Z_u = 0.25 + j\omega_0 3pH$, the overall transconductance increases almost linearly for $N \leq$4. Consequently, the devices used in the different stages of the proposed PA include 2-to-4 unit transistors simultaneously

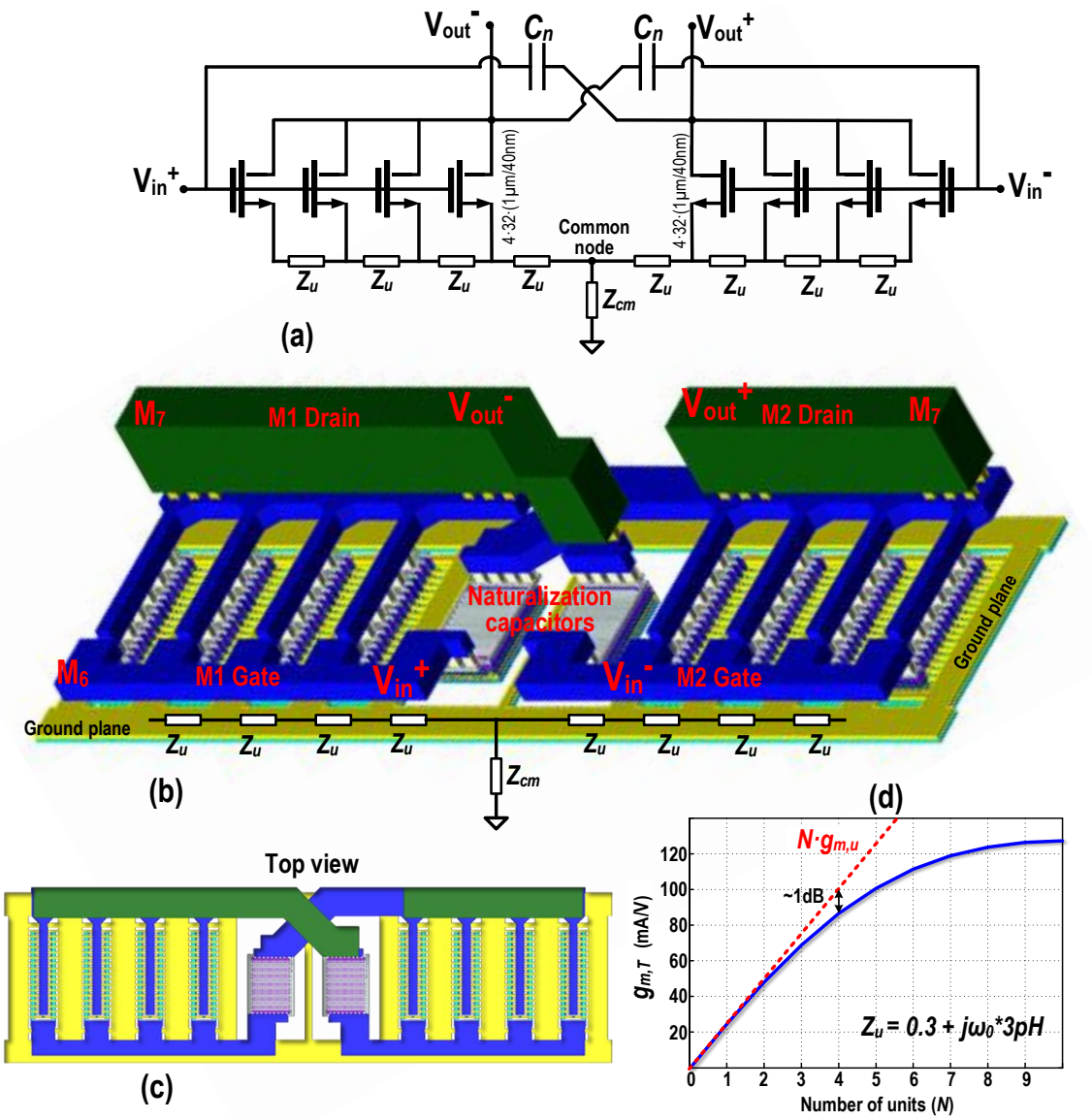


Figure 6.6: (a) Schematic and (b, c) layout of the neutralized differential amplifier; (d) the overall transconductance of the large device versus the number of unit transistors.

optimizing the amplifier output power, gain, and efficiency.

Figure 6.7 shows the simulated f_t and f_{max} of a 3·32·1μm/40nm transistor with extrinsic interconnect parasitics versus V_{ds} for different V_{gs}. It respectively achieves a peak of 220 GHz and 260 GHz for f_t and f_{max}.

6.3 Power Amplifier Design

The optimum layout, characteristics, and different parasitic components of an NMOS transistor have thus far been quantified. In this section, the primary goal is to provide design criteria for an mm-wave PA such that its final stage acts as a switched-mode amplifier at saturation, improving the system efficiency. However, realizing a switched-mode PA at mm-wave is not trivial due to the large output capacitance and low current driving capability of

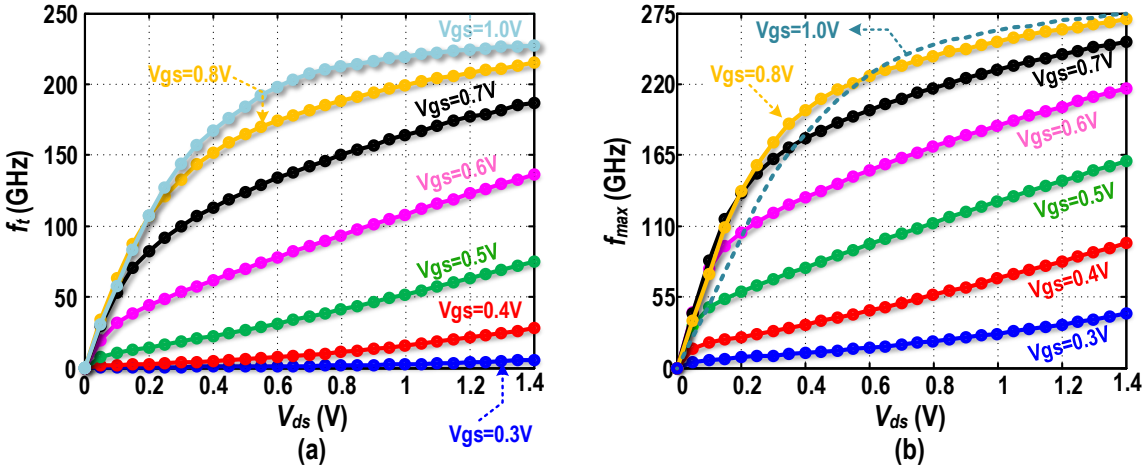


Figure 6.7: Simulated (a) f_t and (b) f_{max} of a 96·1μm/40nm with extrinsic interconnect parasitics versus V_{ds} for different V_{gs}.

CMOS transistors. As discussed in the previous chapter, the MOS transistor must be capable of providing the required systematic peak current of a switched-mode PA while its output capacitance, C_{out}, remains smaller than the PA desired shunt capacitance, C_s. Unfortunately, the MOS transistor's current capability ($\overline{I_{out}}/\overline{C_{out}}$) is relatively inadequate and places a limit on the maximum operating frequency of switched-mode PA, f_m.

As quantified in the previous chapter, f_m increases by migrating to a more advanced technology to obtain transistors with a higher current capability ($\overline{I_{out}}/\overline{C_{out}}$). Another f_m improvement strategy would be using a PA with lower waveform FoM of F_C. It has been shown that F_C reduces ~3× just by realizing an open circuit as the transistor's effective load at the 2nd harmonic ($2\omega_0$). Consequently, f_m can be extended to 60 GHz in 40nm CMOS technology for a class-E/F$_2$ operation. However, smaller F_C also reduces the PA's power gain (G_p), DC current, and output power (P_{out}). Consequently, higher f_m of class-E/F$_2$ operation is achieved through painful reduction of P_{out} and precious device G_p, which can potentially reduce the total PAE.

Figure 6.8 depicts the schematic of the proposed PA [136]. A 3-stage common-source pseudo-differential pair is selected to compensate for the gain penalty of the class-E/F$_2$ operation in the last stage. A transformer-based power splitter converts the singled-ended S$_{\text{in}}$ input to two differential signals feeding pre-drivers. Another set of splitters is added before the four parallel units of the output stage. A combination of series-parallel combining is used in the output matching network to sum up the output power from four pseudo-differential pairs [137]. The detailed design procedure of each stage is investigated in the following subsections.

6.3.1 Amplifier Configuration

Common-source (CS), common-gate (CG), cascode, and neutralized common-source pseudo differential pair (N-CS) can be generally used for implementing an amplifier stage at mm-wave frequencies. Figure 6.9 (a) compares the simulated maximum available gain (MAG) for abovementioned structures. All transistors are biased near peak f_{max} ($V_{gs} = 0.7$ V and $V_{DS} = 1$V). The CG topology is not an appropriate candidate for a 60 GHz amplifier due to its lowest power

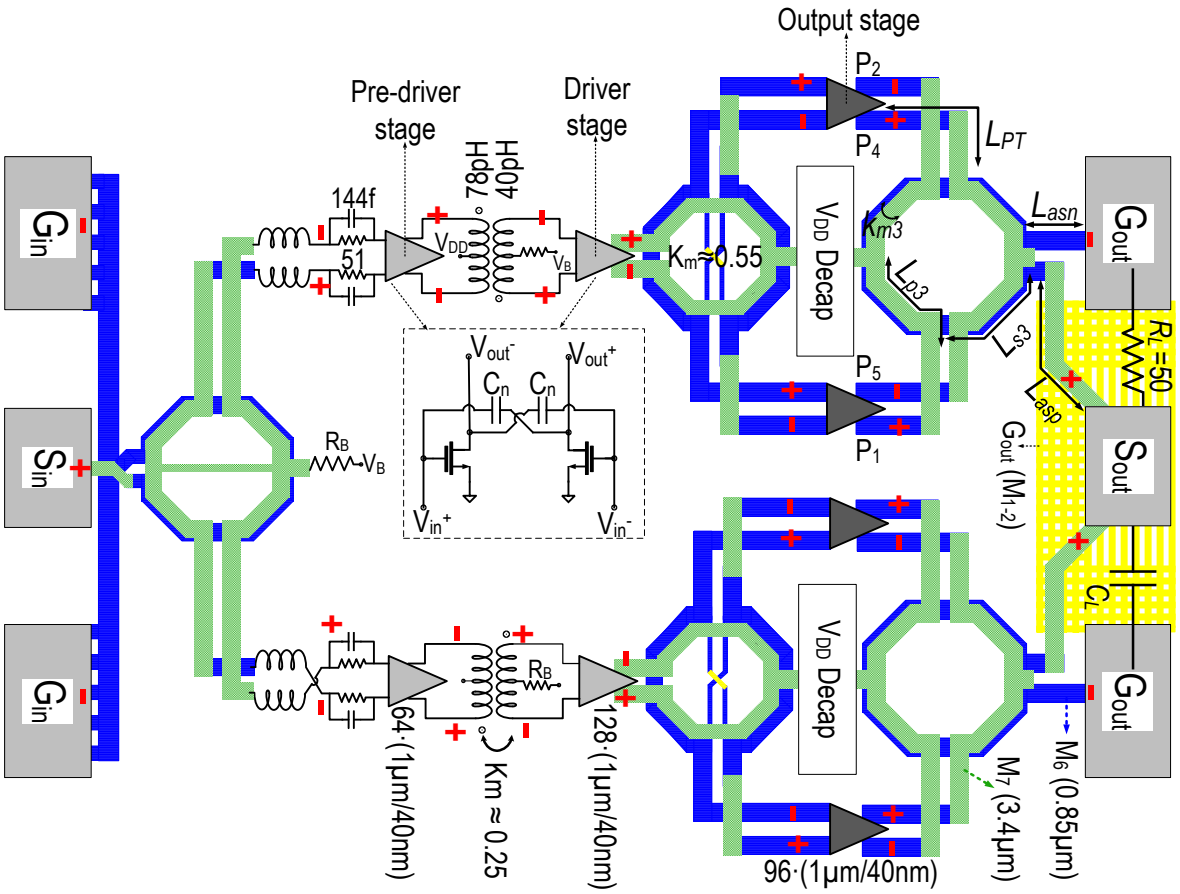


Figure 6.8: Schematic and layout of the proposed 60 GHz PA.

gain. It can merely compensate the insertion loss of its own input and output matching networks at mm-wave frequencies. However, it can be used at the input to simplify the matching to 50 Ω [132].

By utilizing the cascode structure, the supply voltage can be increased to twice the nominal value and thus the output power can also increase. The cascode amplifier exhibits a power gain, G_p, of ∼14 dB at 60 GHz, which is ∼4 dB larger than that for the CS stage. However, cascode topology is potentially more sensitive to parasitics and undesired oscillations. At mm-wave frequencies, the cascode device is degenerated at the source by a parasitic capacitance to ground. It can be shown that this capacitance reduces G_p and realizes a negative resistance seen from the gate of the cascode device. Furthermore, due to the reduced pitch in the 40-nm technology, the drain-source capacitance, C_{ds}, of the cascode transistor is so substantial such that it degrades the reverse isolation of the structure at mm-wave frequencies and thus can potentially create stability issues. Finally, as explained in the previous chapter, the maximum operating frequency of any switched-mode PA reduces to half by replacing the CS with the cascode structure.

The C_{gd} parasitic creates a negative feedback path between the transistor's drain (output) and gate (input) which limits the device power gain and reverse isolation and potentially causes instability. Providing a compensating current to cancel this unwanted feedback is referred to as neutralization [138]. This technique can be easily implemented by cross-connecting two metal-oxide-metal (MOM) capacitors, C_n, between the drains and gates of a pseudo differential pair as shown in Fig. 6.9 (b). The optimum value of C_n should be chosen $\sim C_{gd}$ to maximize the

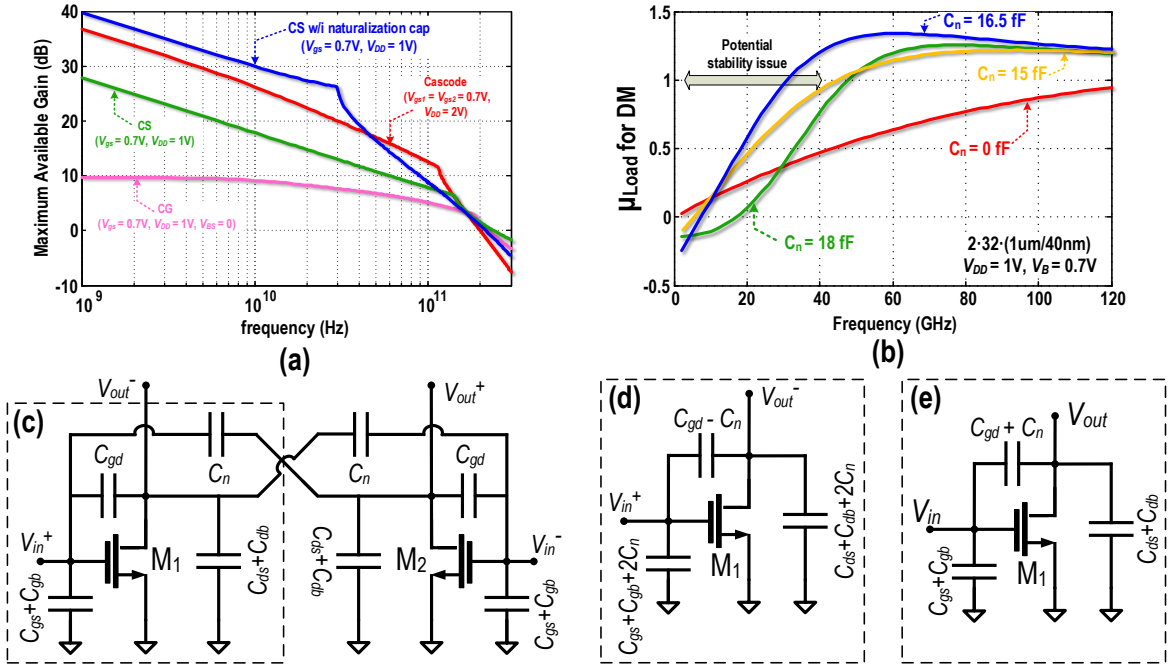


Figure 6.9: (a) Simulated maximum available gain for different amplifier structures; (b) Edwards-Sinsky stability factor for differential amplifier with various C_n; (c) neutralized differential amplifier with its parasitic capacitances; Equivalent model for parasitic capacitances of a neutralized transistor in (d) DM and (e) CM excitation.

Edwards-Sinsky stability factor, μ (see Fig. 6.9 (c)) [132]. As can be determined from Fig. 6.9, the neutralized amplifier offers a 3 dB higher gain along greater stability at 60 GHz. Hence, this technique is exploited for the first two stages of the proposed amplifier.

Figures 6.9 (d) and (e) respectively show the equivalent model for parasitic capacitances of a neutralized transistor for DM and CM input signals. Due to the loading effect of the neutralized capacitors, the effective input and output capacitance of the device increase by C_n in the differential mode. It leads to a significant reduction of $\overline{I_{out}}/\overline{C_{out}}$, degrading the maximum operating frequency of any switched mode PA (see (5.61)). Furthermore, the neutralization capacitors degrade the common-mode stability by increasing the feedback capacitance of each device from C_{gd} to $C_{gd} + C_n$. It will also be shown that the output stage is more sensitive to CM instability rather than a differential one. Consequently, the neutralization technique is not employed for the output stage of the proposed amplifier.

6.3.2 Output Matching Network

Transformers are widely used in the output matching network of mm-wave PAs due to their low insertion loss, compactness, and providing the optimum load impedance for the output transistors. Figure 6.10 illustrates a general schematic of a transformer-based matching network which simultaneously performs m-series (i.e., voltage) and p-parallel (i.e., current) combining. It can be shown that the equivalent load resistance, r_L, seen by each PA's transistor, may be estimated by

$$r_L = \frac{p}{m} \cdot (\frac{k_m}{n})^2 \cdot R_L \tag{6.5}$$

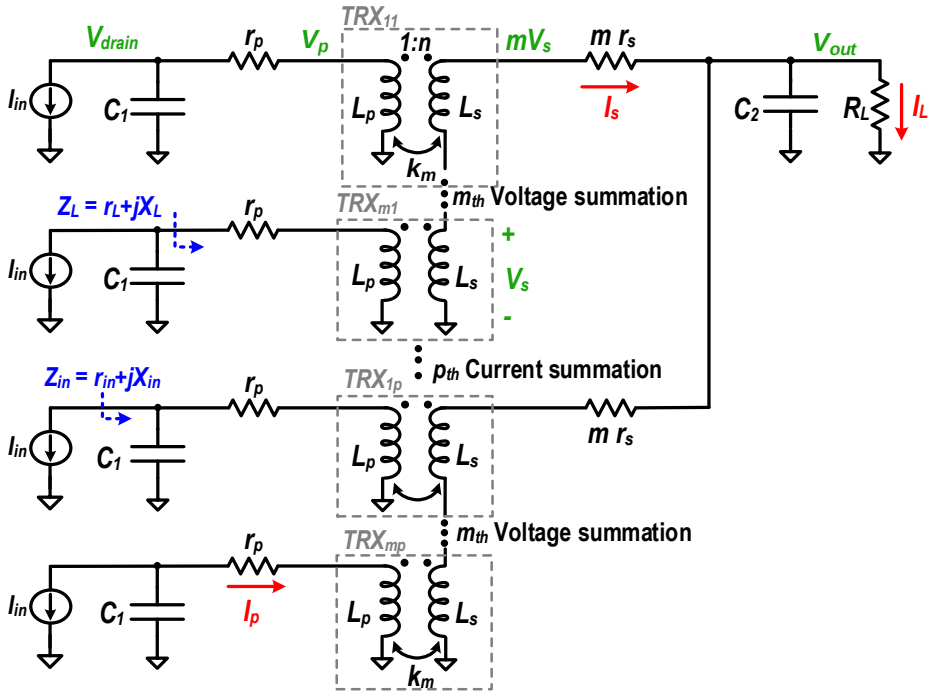


Figure 6.10: Transformer-based matching network with m-way voltage and p-way current summation.

while the insertion loss of the matching network is optimized. As a consequence, the output power of the PA is calculated by

$$P_{out} = m \cdot p \cdot K_P \cdot \frac{V_{DD}^2}{r_L} \rightarrow P_{out} = \left(\frac{m \cdot n}{k_m}\right)^2 \cdot K_P \cdot \frac{V_{DD}^2}{R_L}. \tag{6.6}$$

Given the V_{DD} constraints, in order to deliver greater power to the load, it is desirable to reduce r_L by employing larger m and transformer's turns ratio, n. The insertion loss of the transformer-based matching network is, in theory, independent of n. At mm-wave frequencies, however, the transformer's coupling factor, k_m, and its windings Q-factors significantly reduce when n >1. Since the efficiency of a transformer is a strong function of its k_m and Q-factors, its insertion loss increases dramatically as n increases. Consequently, substantially increasing n is not a wise choise to raise P_{out}. On the other hand, as m grows, each transistor experiences smaller r_L and thus can theoretically deliver m times larger power. The output power of m transistors are combined by the matching network, and consequently, P_{out} can increase by a factor of m^2. However, this approach cannot be easily adapted for mm-wave PAs. For example, r_L theoretically reduces to 6.25 Ω for a four-way ($m = 4$) distributed active transformer (DAT) combiner [139] with $n = 1$ and $k_m = 0.7$. Load-pull simulations indicate that such a low r_L is a suitable load for a 200μm/40nm transistor. It means that six unit-transistors of 32μm/40nm should be connected in parallel to realize such a large device, thus introducing a significant penalty on the transistor's G_p, f_{max} and P_{sat}, as can also be determined from Fig 6.6 (d). By adding a two-way current (p=2) combiner to that four-way ($m = 4$) DAT structure, r_L enhances to 12.5 Ω which is now the suitable load for a 100μm/40nm transistor. In this approach, the output devices can be smaller for the same P_{out} which effectively improves the transistors' internal loss and f_{max}. Hence, they can generate a stronger 2nd harmonic current that is also

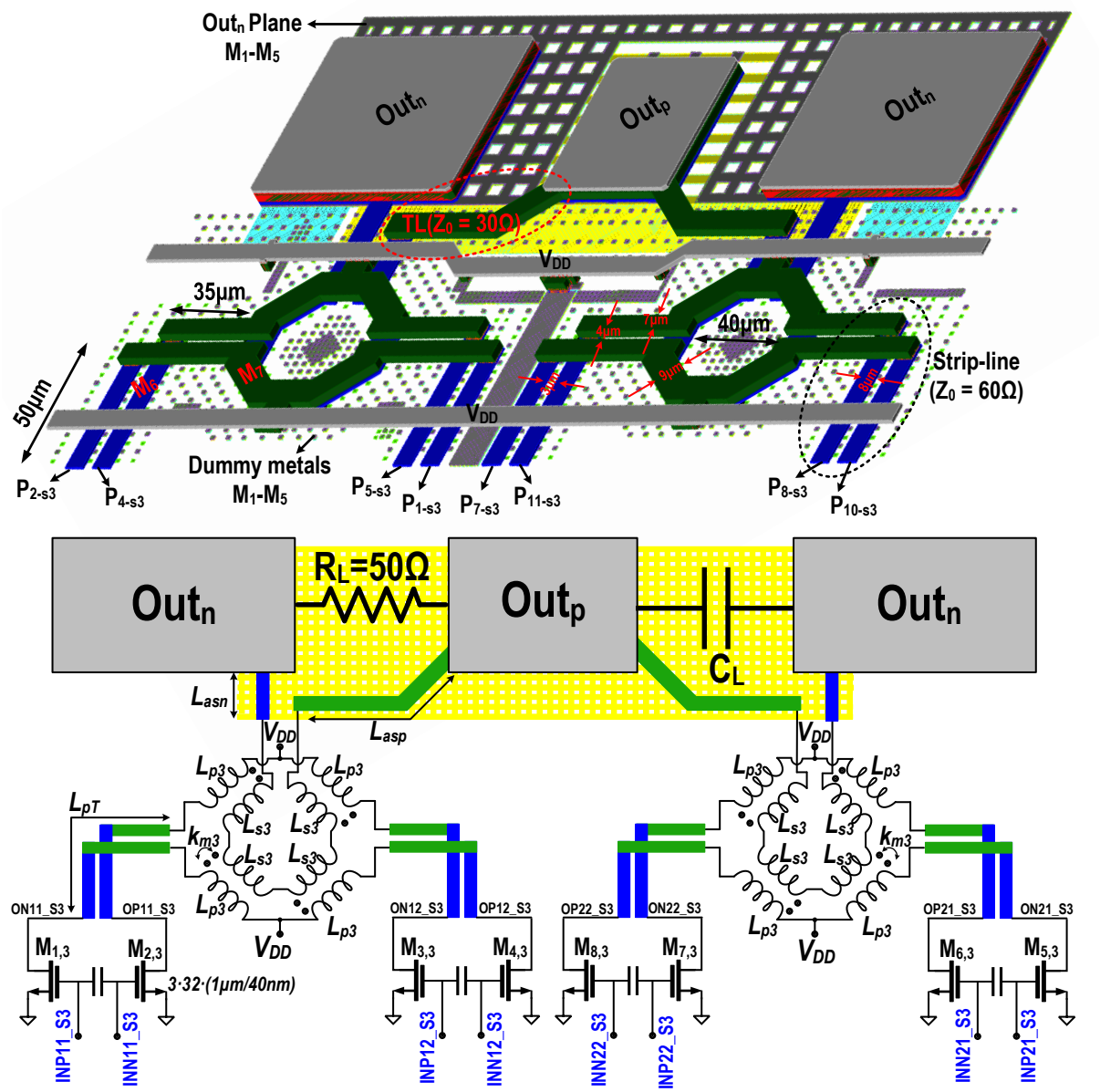


Figure 6.11: Schematic and layout of the last stage of PA.

beneficial for the intended class-E/F$_2$ operation.

Figure 6.11 shows the schematic and layout of the output stage of the proposed amplifier. It consists of two 2-way differential series (m=4) and one 2-way parallel (p=2) combiners to sum up the output power from four pseudo-differential pairs. The voltage and current summations are respectively performed by two transformers and the output RF ground-signal-ground (GSG) pads. The ground pads are connected to each other with a stack of metal-1 to metal-5 lines. However, they are isolated from the chip ground to improve the balance of the impedance seen at different input ports of the matching network. Unfortunately, the inductance of the transformer's primary winding is not large enough to provide the required imaginary impedance of the output transistors. To satisfy that, two pairs of differential strip lines are inserted between the transformer and the output differential pairs.

A self-shielding transformer structure is employed as the power combiner. In general, the winding with a lower voltage swing should be selected as a shield to the other winding. However,

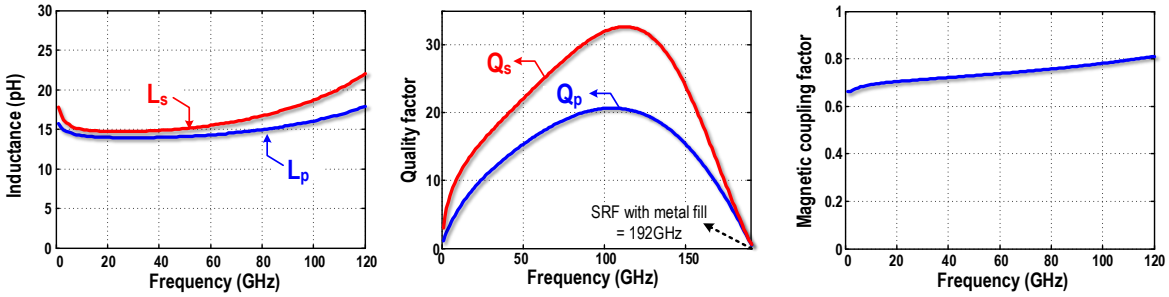


Figure 6.12: Different characteristics of the transformer used in the output matching network.

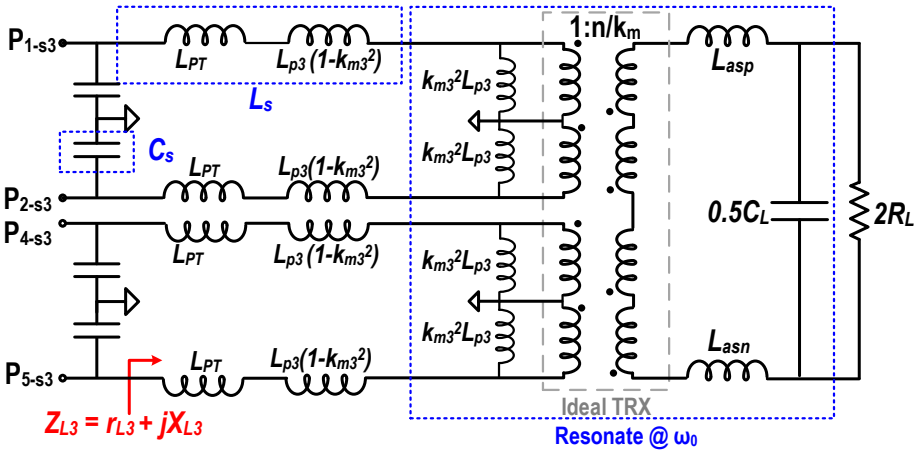


Figure 6.13: Equivalent half-circuit model of output matching network for differential excitation.

the parasitic capacitance from the transformer's primary winding to the substrate increases the total shunt capacitance experienced by the PA's transistors and can potentially limit the maximum operating frequency and proper operation of class-E/F_2 PA. Hence, the primary winding is implemented in the top metal. Employing the broadside-coupled transformer also improves the transformer's coupling factor to ∼0.75 but at the expense of increased inter-winding capacitance which subsequently reduces the self-resonance frequency of the transformer to ∼190 GHz for the differential-mode excitation. As shown in Fig. 6.12, the simulated self-inductance of the primary and secondary windings are, respectively, 14 pH and 16 pH with a Q-factor of 16 and 22 at 60 GHz. The center taps of the transformer's primary winding are virtual grounds that are used for the DC feed lines. The maximum allowed DC current due to electro-migration is ∼8 mA/μm for thick metal layer (metal-6) in 40-nm technology used in this work. By considering a ∼25 mA DC current for each transistor, supply lines should be wider than 8 μm to abide by the manufacturability rules.

6.3.3 Output Matching Network Behavior to DM and CM Input Signals

Figure 6.13 shows the half-circuit model of the output matching network for the differential-mode (DM) input signals. It can be demonstrated that the total effective inductance at the output of the matching network $(4L_{s3}+L_{asn}+L_{asp})/2$ must approximately resonate with the parasitic capacitance of the pad, C_L, at the operating frequency, ω_0, to optimize its insertion

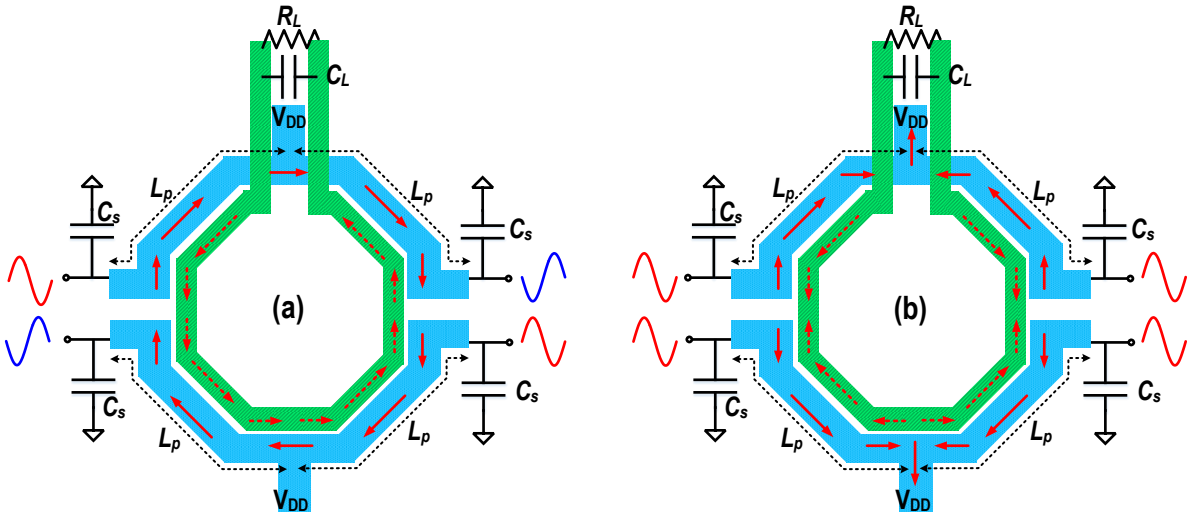


Figure 6.14: Transformer behavior in differential-mode (a) and common-mode (b) excitations.

loss.

$$\omega_0 = \frac{1}{\sqrt{0.5(4L_{s3} + L_{asn} + L_{asp})C_L}} \tag{6.7}$$

The combination of the transformer leakage inductance $L_{p3}(1\text{-}k_{m3}^2)$ and the effective inductance of differential strip-lines, L_{PT}, along eith output parasitic capacitance of the transistor, $(\overline{C_{out}} \cdot W)$ respectively realize the required series inductance, L_{ser}, and shunt capacitance, C_s, of a switched-mode PA. Consequently,

$$L_{ser} = L_{PT} + L_{p3}(1 - k_{m3}^2) \qquad C_s = \overline{C_{out}} \cdot W \tag{6.8}$$

Furthermore, L_{ser} and C_s must also satisfy the zero voltage and zero-slope operation of class-E/F$_2$ PA by

$$L_{ser} = \frac{K_L \cdot r_L}{\omega_0} \qquad and \qquad C_s = \frac{K_C}{r_L \cdot \omega_0}. \tag{6.9}$$

As explained in the previous chapter, K_L and K_C are the design sets obtained from the intersection point of ZVS and ZdVS circles. The design sets will be quantified for the proposed mm-wave PA in the next subsection.

Class-E/F$_2$ PA requires the creation of an additional CM resonance at $2\omega_0$. Fortunately, the output matching network behavior is quite different for the DM and CM input signals. As shown in Fig. 6.14 (a), for the DM input signals, all induced currents circulate in the same direction at the transformer's secondary to satisfy Lenz's Law. Consequently, the induced currents add up constructively which leads to a strong inter-winding coupling factor ($k_m \geq 0.7$). However, when the transformer's primary is excited by a CM signal (Fig. 6.14 (b)), the induced currents at the right-up/left-down and right-down/left-up quarters of the transformer's secondary winding circulate in opposite directions thus largely canceling each other. The residual current results in a very small $k_m \leq 0.2$ for the CM excitation. Hence, the circuit elements at the transformer's secondary side such as R_L, C_L, L_{s3} and even inter-winding capacitance cannot be seen by the even harmonics. Consequently, the transmission line and the transformer primary inductance, which is seen by the CM signals, has to resonate with C_s at $2\omega_0$ to satisfy the

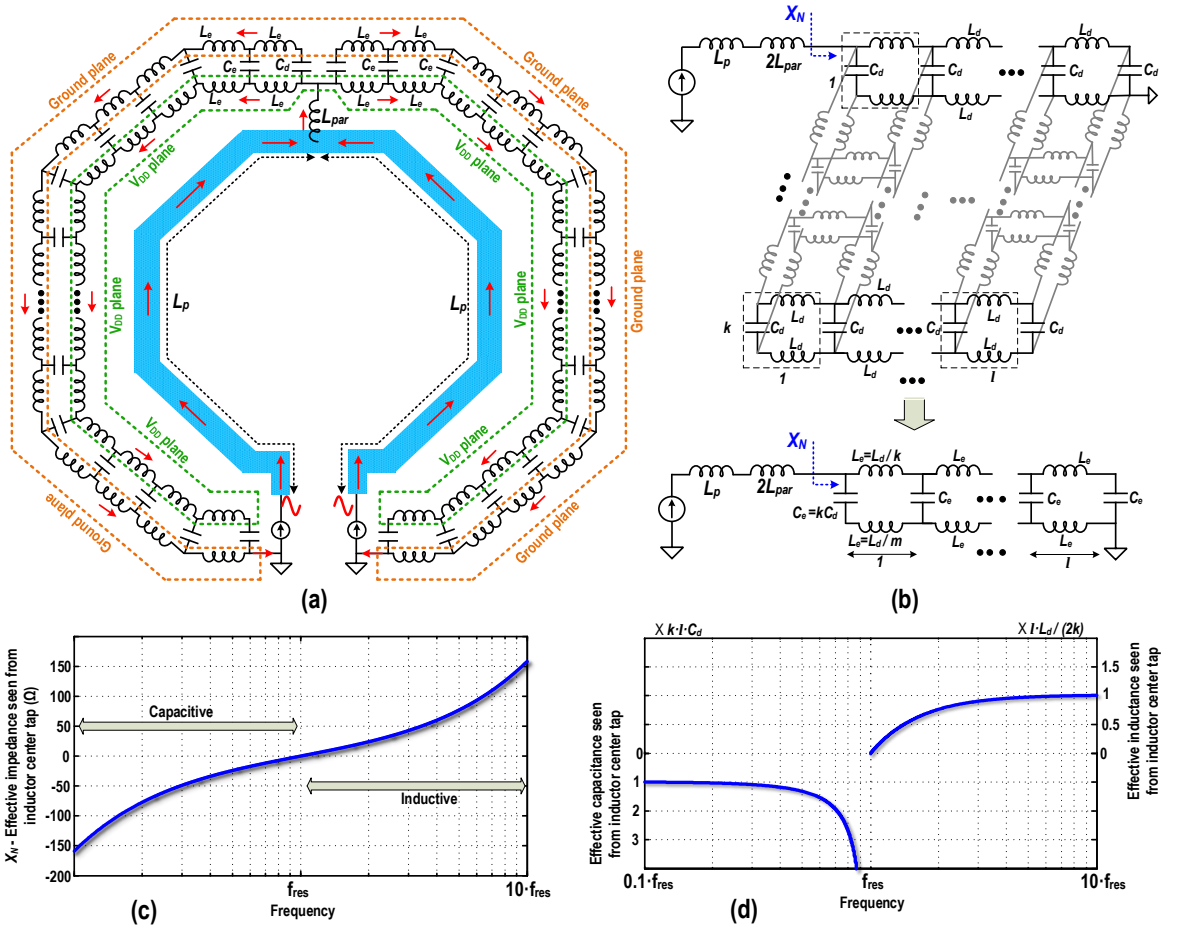


Figure 6.15: (a) Simplified layout and (b) equivalent circuit model of the effective CM inductance seen by PA transistors; (c, d) effective impedance of the bypass network.

class-E/F_2 operation. Note that the meaningful inductance must be defined for a closed loop. The statement "the inductance of the transmission line and transformer's primary" is rather meaningless as this is only a partial inductance. The complete inductance must also include the route from the transformer's center tap to the transistors' source.

For the sake of simplicity, the layout and equivalent circuit model of the effective CM inductance seen by the PA's transistors is shown in Fig. 6.15 (a) and (b) for a single turn differential inductor. The combination of bypass capacitors with the supply and ground inductance realizes a distributed LC line between the inductor's center tap and transistor's source. This structure exhibits a resonant frequency at

$$f_{res} = \frac{1}{2\pi \cdot l \cdot \sqrt{(L_d/\sqrt{(2)}) \cdot C_d}} \tag{6.10}$$

where, l is the total length between the inductor's center tap and transistor's source. The L_d and C_d respectively represent the density of ground/supply inductance and bypass capacitance per area. As can be ascertained from Fig. 6.15 (c) and (d), the effective impedance of the bypass structure reaches zero at f_{res} and respectively becomes capacitive and inductive at frequencies below and beyond f_{res}. To achieve simultaneous efficient bypassing and reducing the CM inductance seen by the PA's transistors, f_{res} should be adjusted to $\sim 2\omega_0$. Since both L_d and

l are respectively fixed by metal thickness (technology) and the transformer's dimension, C_d is the only 'knob' to tune f_{res}. For example, by considering $L_d = 1\text{pH}/\mu\text{m}^2$ and $l = 50\,\mu$m, the density of the bypass capacitors should be $\sim 1\,\text{fF}/\mu\text{m}^2$ to adjust f_{res} at 120 GHz. Under this condition, the CM inductance seen by PA's transistors is given by

$$L_{cm} = L_{PT} + L_{p3} \approx L_{ser}. \tag{6.11}$$

Consequently, the inductance experienced by the PA's transistors is almost identical at fundamental and second harmonic frequencies. It means that if ω_{cm} is adjusted to $2\omega_0$, conjugate matching is also achieved at $2\omega_0$ which can potentially degrade the transistor's gain and output power. It raises the question: what is the optimum ω_{cm} to simultaneously achieve high power gain, large P_{out}, and switched-mode operation for a mm-wave PA?

6.3.4 Extended Class-E/F$_2$ PA

Class-E/F$_2$ operation relies on realizing an open circuit as the transistor effective load at $2\omega_0$. However, it turns out that ZVS and ZdVS compliant waveform can be also achieved even if the common-mode resonant frequency, ω_{cm}, is adjusted at an arbitrary frequency. It means the second harmonic impedance seen by the switch devices can be any arbitrary point on the entire perimeter of the Smith Chart [140]. The extended Class-E/F$_2$ tuning can potentially offer more flexibility for making mutual tradeoffs between waveform FoMs and PA's maximum operating frequency (f_m), gain, P_{out} and PAE.

Figure 6.16 (a) illustrates the ZVS and ZdVS circles of an extended class-E/F$_2$ PA for different ξ=ω_{cm}/ω_0. The optimal design sets (K_C, K_L, K_X) are obtained through the intercept point of ZVS and ZdVS circles and shown in Fig. 6.16 (b). By reducing ξ, all design sets become smaller and finally reach the same values as in the traditional class-E PA. As can be concluded from (6.9), L_{ser} is proportional to K_L thus the inductive part of the matching network is diminished by a smaller ξ. This leads to an improvement in the effective quality factor and insertion loss of the matching network. However, the optimal K_C, and thus C_s, reduce by a smaller ξ. It means the switching transistor can potentially have less parasitic output capacitance and becomes smaller with higher on-resistance thereby lowering the drain efficiency. This trend shows a clear tradeoff between the insertion loss of the matching network and the transistor's on-resistance loss in the extended class-E/F$_2$ operation.

By replacing the obtained design sets in the matrix equation of (5.16), the drain voltage and current waveforms are derived and depicted in Fig. 6.16 (c) and (d). The voltage waveforms are almost identical for different ξ. However, as ξ increases, stronger second harmonic content is present in the current waveforms such that the direction of the switch current is reversed for $\xi > 2.25$. The fundamental component of the drain current, and thus the PA's power capability, reduces with a larger ξ as shown in Fig. 6.16 (e).

Based on V-I waveforms, the four waveform FoMs of F_V, F_I, F_C, and F_{PI} are calculated and shown in Fig. 6.16 (f). Neither F_V and F_I change significantly with ξ. However, F_C reduces with a larger ξ, resulting in more tolerance to the transistor's output capacitance. The behavior of F_{PI} is not monotonic. It initially reduces slightly and reaches its minimum at ξ=1.5 and then begins increasing.

Based on the variation of topology-dependent parameters, the performance of the extended

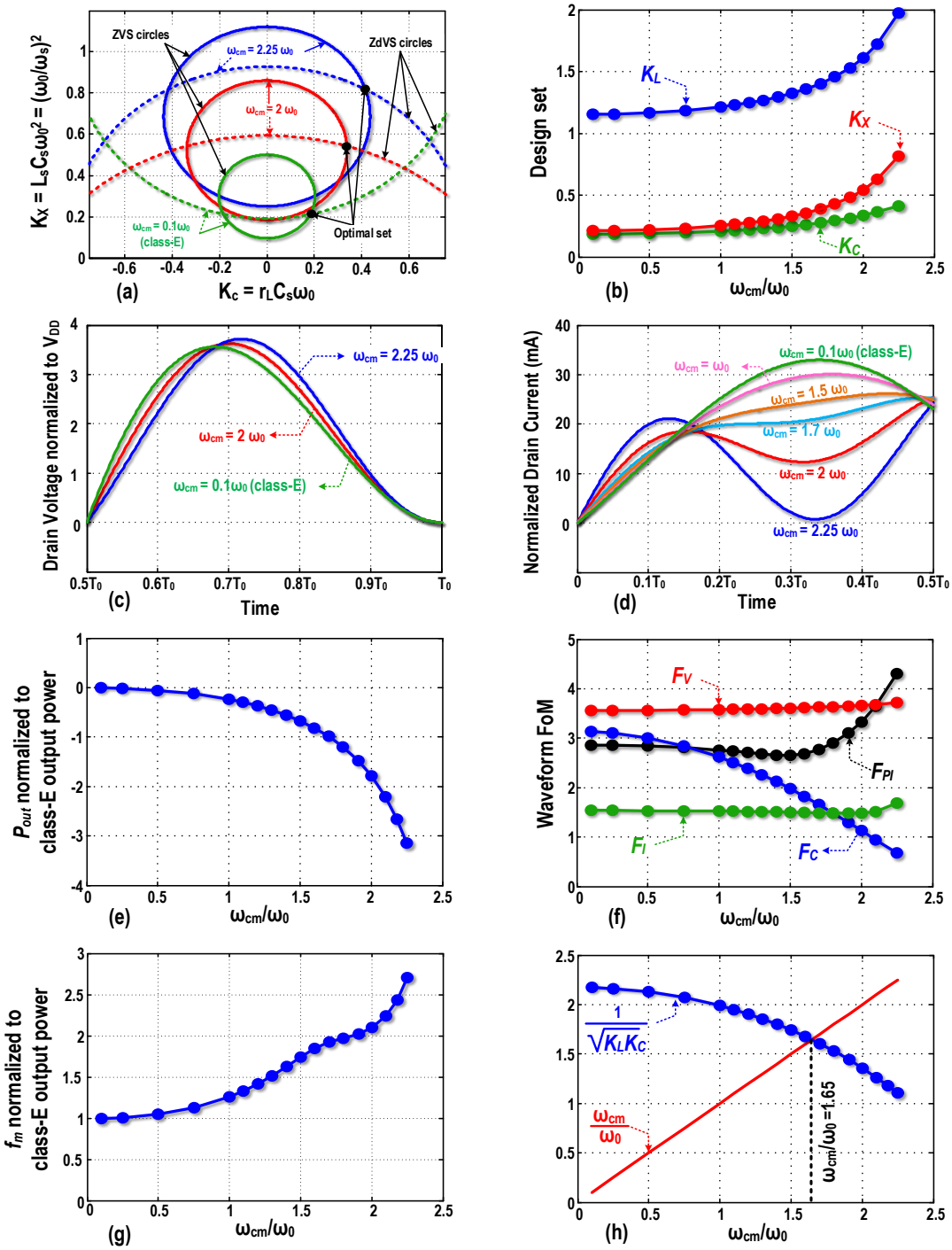


Figure 6.16: Different characteristics of extended class-E/F$_2$ PA versus ω_{cm}.

class-E/F$_2$ PA is almost identical for $1.6<\xi<2.1$. As an example, f_m of the extended class-E/F$_2$ PA is shown in Fig. 6.16 (g). Due to the lower product of F_C and F_{PI} (see (5.61)), f_m increases monotonically with ξ. However, the slope of f_m improvement becomes smaller for $\xi>1.5$ due to F_{PI} increase. Consequently, f_m is almost constant for $1.6<\xi<2.1$.

As explained in the previous subsection, for the proposed matching network, the inductance seen by PA's transistors is almost identical at fundamental and 2nd harmonic frequencies.

Consequently,

$$\omega_{cm} = \frac{1}{\sqrt{L_{cm} \cdot C_s}} \rightarrow \omega_{cm} = \frac{1}{\sqrt{L_{ser} \cdot C_s}} \tag{6.12}$$

By exploiting the K_L and K_C definitions, we have

$$\omega_{cm} = \frac{1}{\sqrt{L_{cm} \cdot C_s}} \xrightarrow{L_{ser}=\frac{K_L r_L}{\omega_0}, \quad C_s=\frac{K_C}{r_L \omega_0}} \frac{\omega_{cm}}{\omega_0} = \frac{1}{\sqrt{K_L K_C}}. \tag{6.13}$$

It places another constraint on the position of ω_{cm} for the extended class-E/F$_2$ operation. As illustrated in Fig. 6.16 (g), the above equation is merely satisfied at ω_{cm}=1.7ω_0. The effects of this tuning strategy on G_p and P_{out} of output transistors will be investigated in the next subsection.

6.3.5 Effects of CM Resistive Loss on PA's Performance

The drain current of any switched-mode PA contains significant higher-order harmonic components such that any resistive termination at such harmonics would lead to an additional power loss. Consequently, the input impedance of the matching network with these harmonics must be either purely reactive, open-circuit, or short-circuit to avoid wasting power at the harmonics. However, the quality factor of on-chip passive components are quite inadequate, resulting in the resistive termination at the harmonics and thus degrading the PA's efficiency. In this subsection, the side effects of the poor Q-factor of the common-mode resonance, Q_{cm} on the performance of an extended class-E/F$_2$ PA are investigated.

Figure 6.17 (a) shows the ZVS and ZdVS circles of the extended class-E/F$_2$ PA for different Q_{cm}. The optimal design sets (K_C, K_L, K_X) are obtained through the intercept point of ZVS and ZdVS circles and shown in Fig. 6.17 (b). The design sets do not change significantly when Q_{cm}>10. However, as Q_{cm} diminishes, K_C becomes smaller, leading to a smaller output transistor with a higher channel on-resistance and thus lower drain efficiency.

By replacing the obtained design sets in the matrix equation of (5.16), the drain voltage and current waveforms are derived and shown in Fig. 6.17 (c) and (d). The voltage waveforms are almost identical for different Q_{cm}. However, as Q_{cm} reduces, weaker second harmonic content is present in the current waveform such that both F_I and F_{PI} degrade as shown in Fig. 6.17 (e).

Figure 6.17 (f) illustrates the drain efficiency of the extended class-E/F$_2$ PA versus Q_{cm} for different ω_{cm}. It was assumed that both switch and matching network at ω_0 are ideal (insertion loss and channel on-resistance are zero). Therefore, the resistive loss at $2\omega_0$ is the only source of the drain efficiency degradation. As expected, this penalty increases with lower Q_{cm}. However, the degradation is almost tolerable for Q_{cm}>15. This plot also indicates that the efficiency penalty is more significant while ω_{cm} is adjusted closer to $2\omega_0$. However, as ω_{cm} moves farther away from $2\omega_0$, the benefits of class-E/F$_2$ operation, like its higher maximum operating frequency, begin disappearing. By considering both scenarios, it is again desired to select $\omega_{cm} \approx 1.7\omega_0$.

6.3.6 Optimum Output Matching Network and Device Size

The matching network geometry is initiated by choosing the switch transistor dimension such that its output capacitor absorbs the entire C_s. However, C_s also depends on series inductance, L_{ser}, and the load resistance presented by the matching network. Hence, several iterations

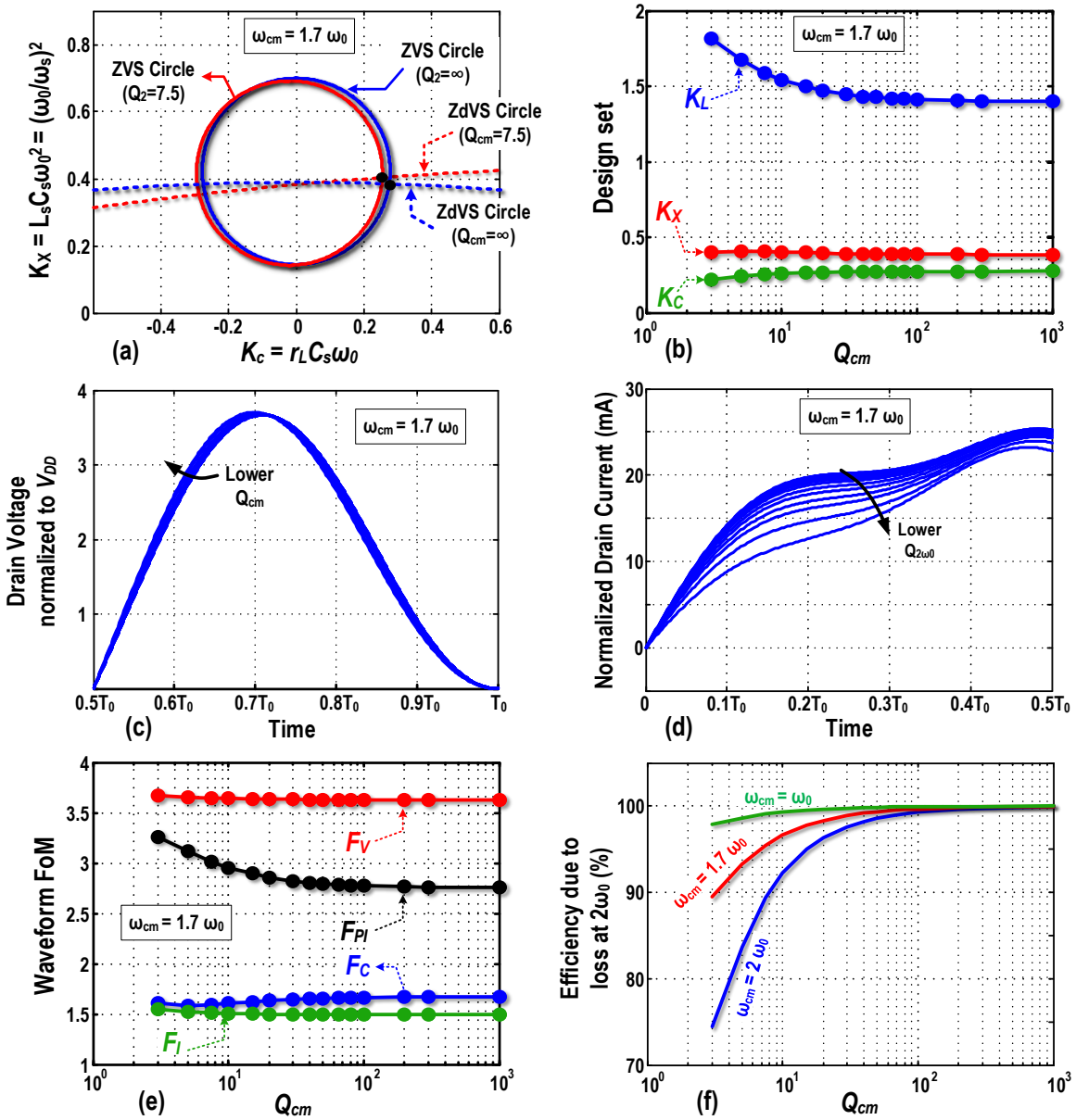


Figure 6.17: Different characteristics of class-E/F$_2$ PA versus the quality factor of common-mode resonant frequency.

are needed to find the optimal size combination of the transistor, transformer, and matching network. This procedure results in an optimal unit power transistor size of 3·32·(1μm/40nm).

For the next step, the optimum load impedance of the output transistor must be selected by giving simultaneous considerations to the PA's output power, gain, and efficiency while ensuring stability over all frequencies. At the optimum load, the output transistors must be capable of delivering the required output power with the highest possible efficiency and power gain. Figure 6.18 illustrates the load stability circle, constant power gain (G_p) contours, constant P_{sat}, and PAE circles on the Smith charts for output transistors with an ideal series-parallel combiner. The main goal is to find a load impedance that offers simultaneous high P_{sat}, G_p and PAE, however, as far as possible from the load stability circle. Furthermore, as explained in the previous subsections, the inductive part of that optimum load and transistor's output capacitor must create a CM resonance at $\sim$1.7ω_0 to satisfy the extended class-E/F$_2$ operation.

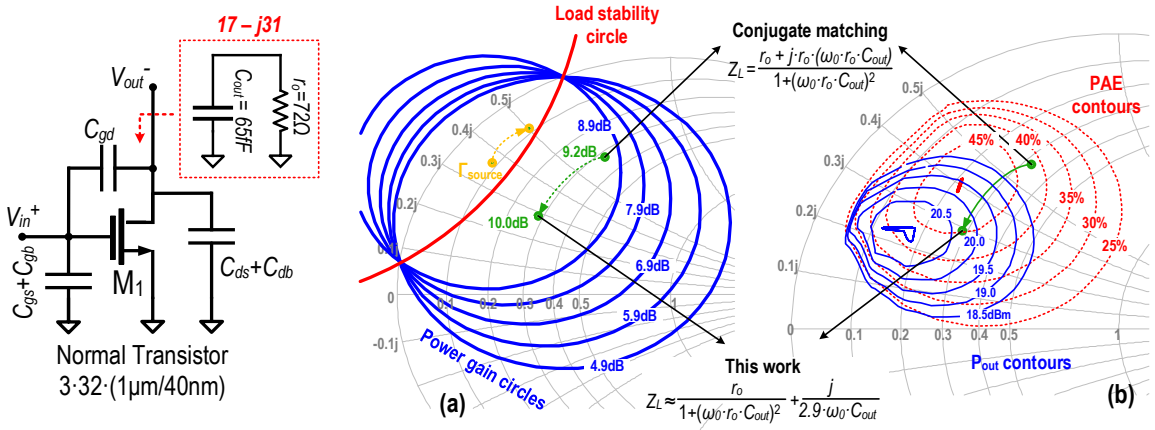


Figure 6.18: (a) Load stability circle and constant power gain circles for 3·32·(1μm/40nm) transistor; (b) constant PAE and P_{sat} circles for the last stage with an ideal series-parallel combiner.

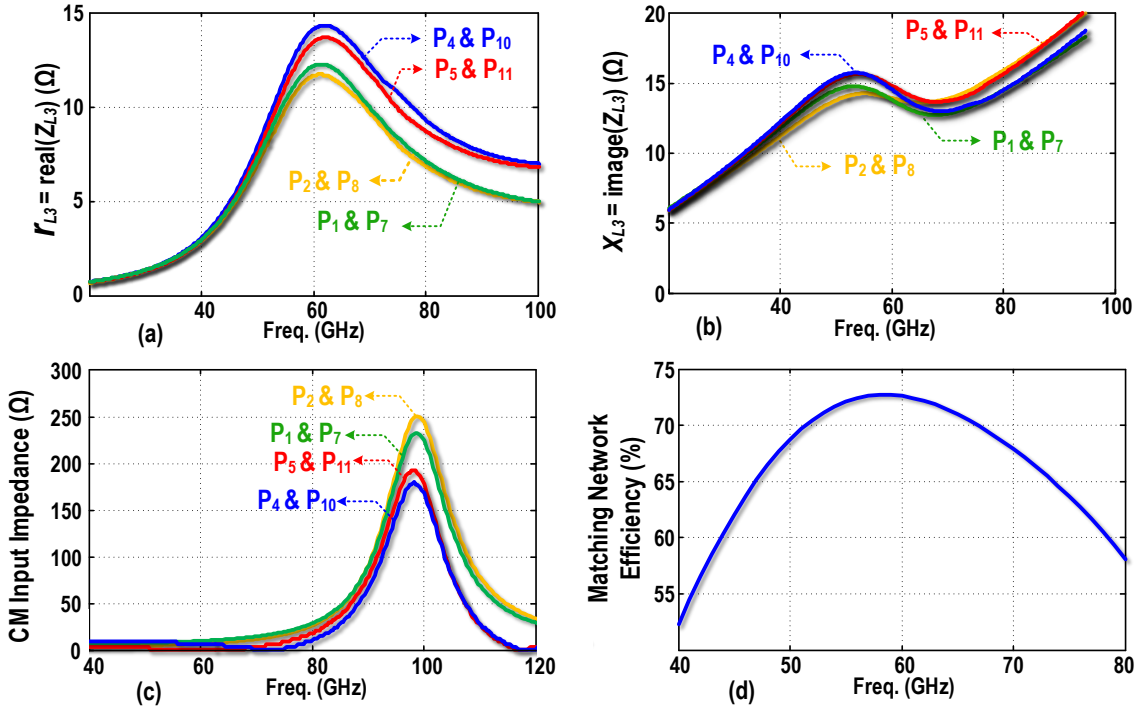


Figure 6.19: (a) Real and (b) imaginary parts of the impedance seen at the different input ports of the output matching network; (c) CM input impedance; (d) passive efficiency of the output matching network.

Consequently, the optimum load impedance ($Z_{opt} = r_{opt} + j \cdot X_{opt}$) may be estimated by

$$r_{opt} \approx real\{r_o \| \frac{1}{C_{out} \cdot \omega_0}\} \rightarrow r_o \approx \frac{1}{1 + (r_o \cdot C_{out} \cdot \omega_0)^2}, \tag{6.14}$$

$$X_{opt} \approx \frac{1}{C_{out} \cdot \omega_0 \cdot \left(\frac{\omega_{cm}}{\omega_0}\right)^2} \rightarrow L_{opt} \approx \frac{1}{C_{out} \cdot \omega_0^2}. \tag{6.15}$$

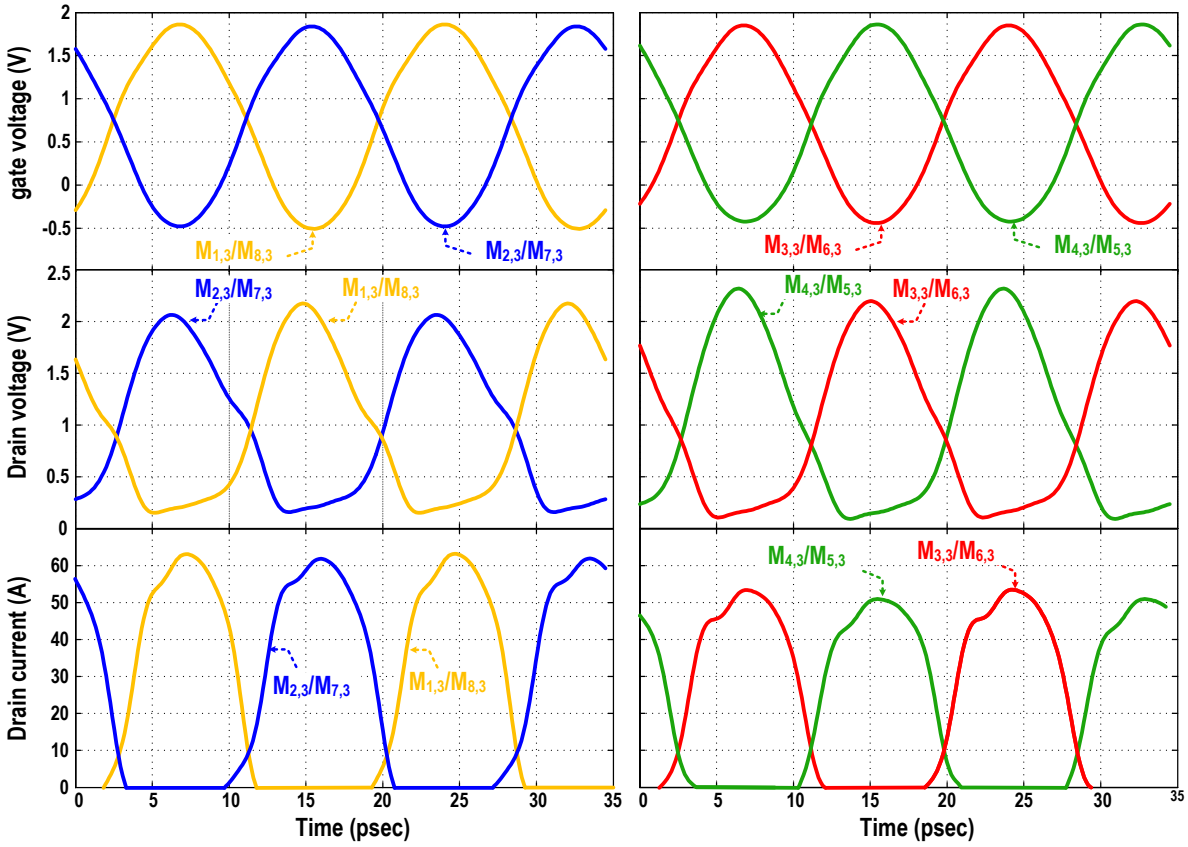


Figure 6.20: Different waveforms of output transistors at 58 GHz.

where r_o and C_{out} are respectively output resistance and capacitance of the output transistors. As shown in Fig. 6.18, the optimal normalized impedance is approximately 0.26+0.22j, giving an output power of 20 dBm with 40% PAE for eight output transistors with an ideal series-parallel combiner. Load-pull and small-signal simulation also indicate that Z_{opt} is almost identical for $0.6\,\text{V}<V_{gs}<0.9\,\text{V}$ and $0.9\,\text{V}<V_{DD}<1.1\,\text{V}$ which helps to fairly compare the performance of the proposed PA under different bias conditions.

For the next step, the geometry of the output matching network of Fig. 6.11 should be optimized to efficiently transform the load impedance (50 Ω load plus pad parasitic capacitance, C_L) to the chosen value of Z_{opt} for each output transistors.

Figures 6.19 (a) and (b) illustrate the real (r_{L3}) and imaginary (X_{L3}) parts of the impedance seen in Fig. 6.11 at the different input ports of the output matching network. As explained in subsection 6.3.2, r_{L3} is mainly determined by the voltage (m) and current (p) summation factors of the output matching network as well as the transformer's turns ratio (n) and coupling factor (k_m). However, the interwinding capacitance between the transformer's primary and secondary windings (C_{ov}) creates an imbalance in the impedance transformation ratio of different input ports of the matching network. The ports (P_{4-s3} and P_{5-s3}) that are farther from the virtual ground of secondary winding see a larger output voltage swing. Consequently, they see a higher load resistance as shown in Fig. 6.19 (a). However, since most of the required series inductance is provided by the strip lines, C_{ov} has fewer side effects on X_{L3}, and consequently, a smaller imbalance is seen in Fig. 6.19 (b).

The CM resonant frequency of the output matching network is simulated by adding a 65 fF

capacitor (as C_s) in parallel with each input port and exciting the structure with in-phase current sources. The transmission line and transformer primary inductance, which are seen by CM signals, resonate with C_s at ∼100 GHz to satisfy the extended class-E/F$_2$ operation (see Fig. 6.19 (c)). Note that, since the secondary winding acts as a floating metal for CM input signals, C_{ov} connects in series with the parasitic capacitance between the secondary coil and substrate. It effectively reduces the transformer's undesired parasitic capacitance and thus the self-resonance frequency of the transformer improves in the CM excitation.

The passive power transfer efficiency (η_p) of the matching network is simulated by exciting the input ports of the structure with differential-mode signals and calculating the ratio of P_{out} (power delivered to the 50 Ω load) to the total input power. Note that η_p cannot be directly calculated from the simulated maximum available gain (MAG) of the structure. MAG is calculated by the assumption of load conjugate matching. However, the load impedance is fixed by the 50 Ω load here. The complete output matching network (including the output RF ground-signal-ground (GSG) pads) demonstrates a simulated η_p exceeding 70% from 52-to-66 GHz, as shown in Fig. 6.19 (d).

The voltage and current waveforms of output transistors are exhibited in Fig. 6.20. Clearly, the waveforms are almost identical to the ideal waveforms of extended class-E/F$_2$ PA with $\omega_{cm}/\omega_0 \approx 1.7$. Furthermore, the overlap between large voltage and current has been significantly reduced. However, the mismatch between the effective loads seen from different input ports of the output matching network creates a minor imbalance between V-I waveforms of the output transistors.

6.3.7 Low/Moderate Coupling-Factor Transformer for Wideband PAs

The effective Q-factor of the PA input/output matching network is degraded by the 50 Ω load and RF pad parasitic capacitance, $C_L \leq 50$ fF, to approximately 1–2 at 60 GHz, thus making these networks wideband. However, the input impedance of the output MOS transistors is considered as load to the inter-stage matching network where $Q_{eff} = \overline{R_{in} C_{in}} \omega_0 \approx 10$ at 60 GHz. Hence, the impedance seen at the input of the transformer network ($r_{in} + jX_{in}$ in Fig. 6.21 (a)) changes significantly over frequency and thus limits the PA bandwidth. One could employ a low Q-factor inter-stage matching network to enhance the amplifier bandwidth. However, this approach dramatically degrades insertion loss of the matching network and efficiency of the PA. As an alternative, this work employs low/moderate magnetic coupling factor transformers for matching the successive PA stages.

Figure 6.21 (a) shows a simplified schematic of a transformer-based matching network where R_L and C_L respectively represent the equivalent input parallel resistance and capacitance of the subsequent stage. The input impedance of this network can be calculated by

$$Z_{in} = \frac{s \cdot \left(\left(L_p L_s R_L C_L \left(1 - k_m^2\right) \right) s^2 + \left(L_p L_s \left(1 - k_m^2\right) \right) s + L_P R_L \right)}{L_s C_L R_L s^2 + L_s s + R_L} \tag{6.16}$$

As a result, the imaginary part of Z_{in} may be estimated by

$$X_{in} = L_p \omega \cdot \frac{1 - L_s C_L \left(1 - k_m^2\right) \omega^2}{1 - L_s C_L \omega^2} \tag{6.17}$$

Consequently, the transfer function of the imaginary part of the impedance seen by the

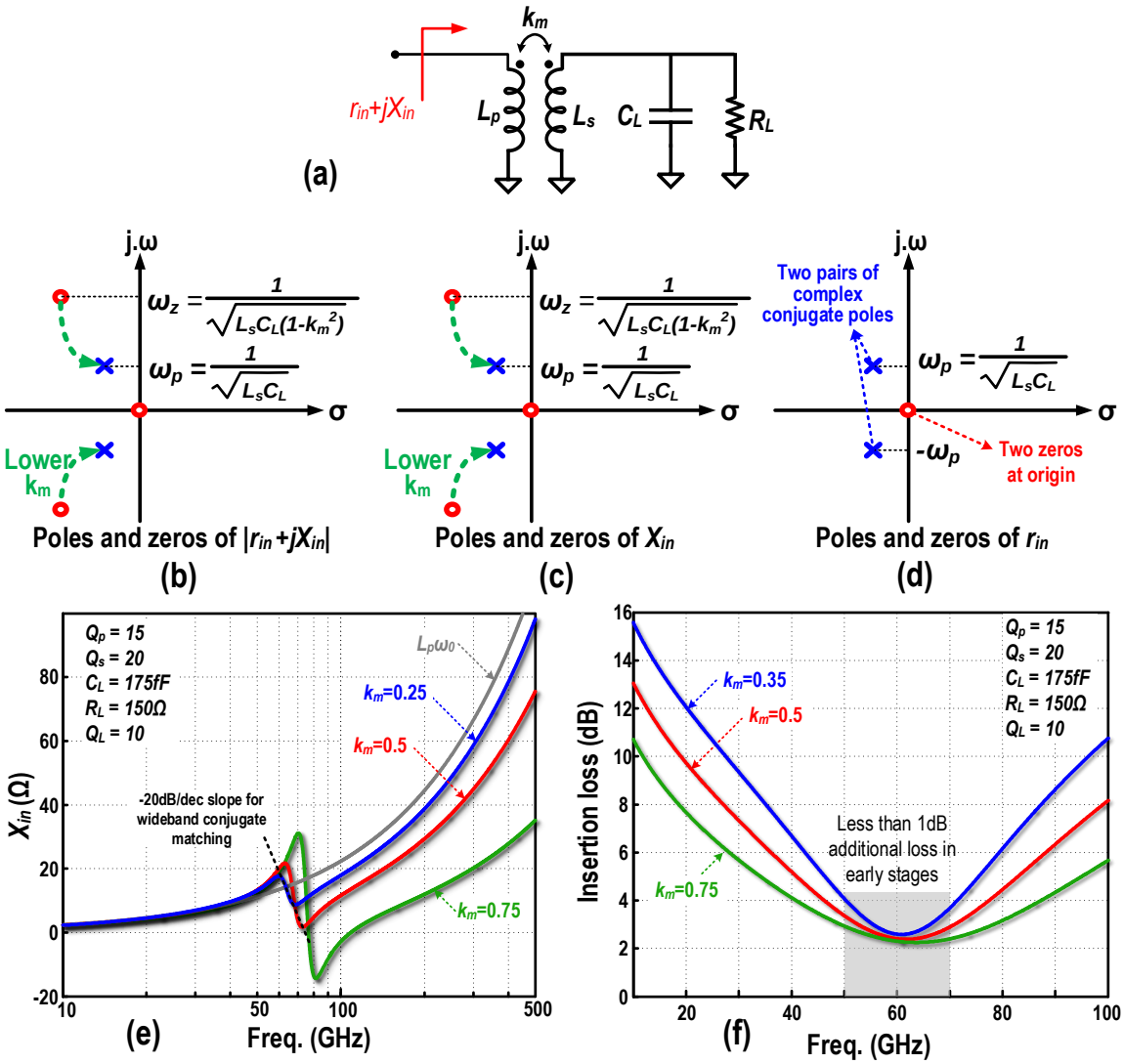


Figure 6.21: (a) Transformer for inter-stage matching; poles and zeros of (b) $|Z_{in}|$, (c) X_{in} and (d) r_{in}; (e) X_{in} and (f) transformer power transfer efficiency versus frequency for different k_m.

successive stage has two conjugate poles at $\omega_p = \pm 1/\sqrt{L_s C_L}$ and two conjugate zeros at $\omega_z = \pm 1/\sqrt{L_s C_L (1-k_m^2)}$ (see Fig. 6.21 (c)). Under a high k_m case ($\geq$0.7), the conjugate zeros pair occurs at a much higher frequency than the poles of the system. Hence, a significant variation is seen in X_{in} (see Fig. 6.21 (e)). However, the zero/pole pairs come closer together with lower k_m, and a flatter region is observed in the X_{in} plot. Hence, the transistor sees its desired reactance over a wider frequency range. However, as k_m reduces, the transformer's efficiency drops. EM simulations show that the additional insertion loss penalty is only $\leq$1.0 dB over the BW by using a k_m=0.35 transformer (see Fig. 6.21 (f)). That penalty occurs at the primary stages where it has negligible effect on the total PAE [141].

It can also be shown that the transfer function of the real part of the impedance seen by the successive stage has two zeros at origin and two pairs of conjugate poles at $\omega_p = \pm 1/\sqrt{L_s C_L}$ (see Fig. 6.21 (d)). Consequently, reducing k_m does not help the transistor of the successive stage to see its desired resistance for a wider bandwidth. However, since the device gain is more sensitive to the reactive part of its load impedance, PA's bandwidth increases anyway with a

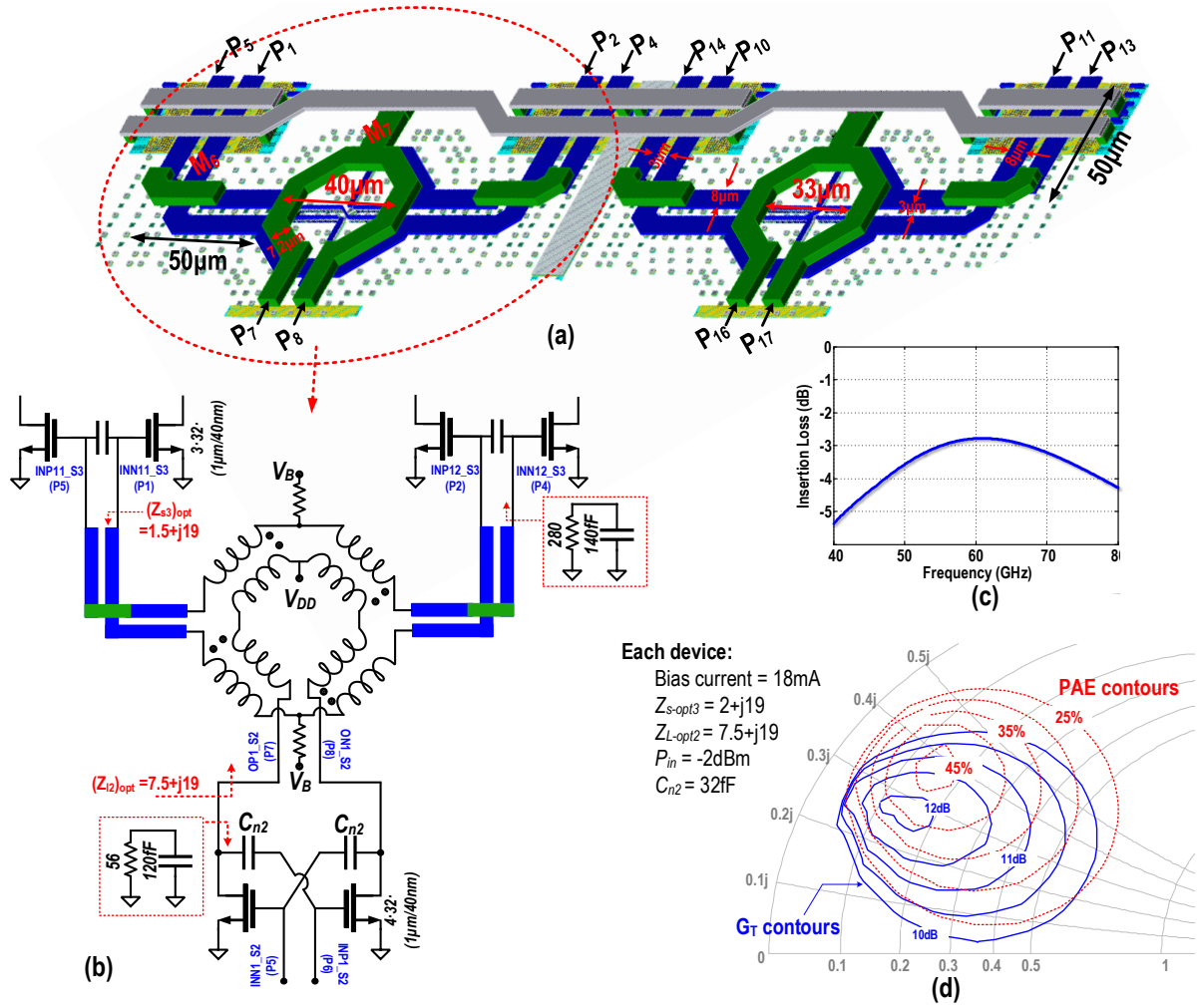


Figure 6.22: (a) Layout of the driver matching network; (b) simplified schematic of the driver amplifier; (c) constant G_p and PAE contours for 4·32·(1μm/40nm) device; (d) insertion loss of the driver matching network.

lower k_m. Hence, low and moderate k_m transformers are respectively used for matching input and driver stages.

6.3.8 Driver Stage

The input power of each transistor of the output stage should be ~3 dBm in order to reach its compression point. By considering ~3 dB insertion loss for the inter-stage matching network, the driver stage must be capable of delivering ~6 dBm. Furthermore, special attention should be paid to avoid compressing the driver stage when the output stage begins saturating. In other words, the linearity of the PA should not be degraded by the driver stages. To consider both scenarios, the total width of the driver devices are just scaled down by a factor of 1.5 compared to that of the output transistors. Note that the preceding stages are progressively sized down by 2× in most of the state-of-the-art mm-wave PAs [132, 134, 137, 139, 141, 142]. Consequently, in this work, the power consumption of the driver stage are traded for higher linearity and P_{1dB} of the entire PA.

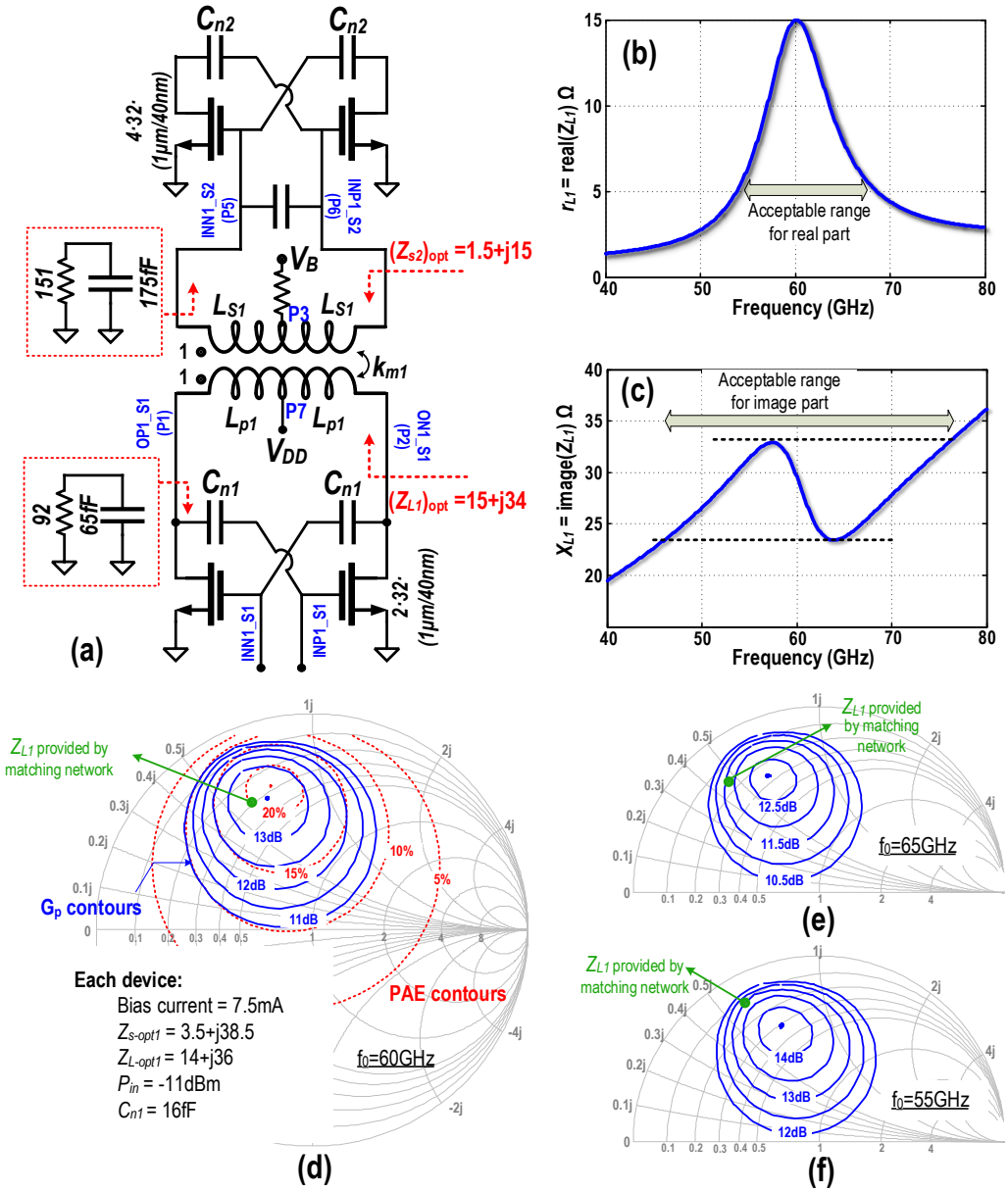


Figure 6.23: (a) simplified schematic of the driver amplifier; (b) real and (c) imaginary parts of the impedance seen at the input ports of the pre-driver matching network; constant G_p contours for 2·32·(1μm/40nm) device at (d) 60 GHz, (e) 55 GHz and (f) 65 GHz.

The driver stage is shown in Fig. 6.22 (b) and realized by the neutralized pseudo-differential amplifier with the transistor dimension of 4·32·(1μm/40nm) which is biased in the class-A regime with a current density of 0.14 mA/μm. The neutralization capacitor, C_{n2}, is 32 fF, making the amplifier unconditionally stable in the differential-mode. Figure 6.22 (d) illustrates the constant power gain (G_p) and PAE contours of the driver transistor for P_{in}=-2 dBm. The optimal normalized impedance is approximately 0.15+0.3j, giving a G_p of 12 dB with 40% PAE.

The inter-stage matching network is illustrated in Fig. 6.22 (a) and realized by the transformer-based splitter along with the differential transmission lines. It transforms the input impedance of the output stage (Z_{s3}=1.5-j19 Ω) to the desired load impedance of the driver stage (Z_{opt2}=7.5+j15 Ω). The complete driver matching network demonstrates a simulated insertion loss of ∼3 dB as shown in Fig. 6.22 (c).

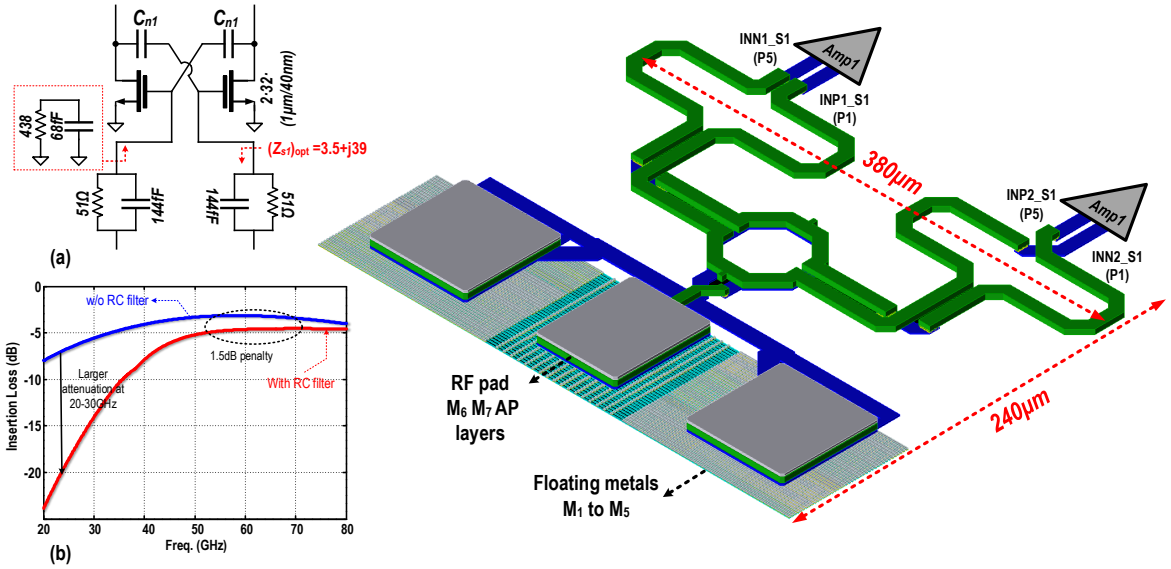


Figure 6.24: (a) Schematic and (b) insertion loss of the input matching network.

6.3.9 First Stage

A similar procedure can be adopted for the design of the pre-driver and its matching network. The key difference is that the required output power level of the pre-driver is much lower and more attention should be paid to power gain. The required input power of each transistor of the driver stage should be ∼-6 dBm to push output devices to their compression point. By considering the ∼3 dB insertion loss for the inter-stage matching network, the pre-driver transistor must be capable of solely generating ∼-3 dBm. Hence, the width of pre-driver devices are scaled down by 2× compared to that of the driver transistors.

The pre-driver stage is shown in Fig. 6.23 (a) and realized by a low k_m transformer and the neutralized pseudo-differential amplifier with the transistor dimension of 2·32·(1μm/40nm). Figure 6.23 (d) illustrates the constant power gain (G_p) and PAE contours of the pre-driver transistor for P_{in}=-11 dBm. The optimal normalized impedance is approximately 0.15+0.7j, giving a G_p of 13 dB with 20% PAE. Figure 6.23 (b) illustrates the real (r_{L1}) and imaginary (X_{L1}) parts of the impedance seen at the input ports of the pre-driver matching network. As can be ascertained from Fig. 6.23 (d), (e) and (f), due to the loosely coupled transformer, the driver transistors see their desired impedance for a very wide frequency range (55-to-65 GHz).

Figure 6.24 shows the input matching network of the proposed PA. A transformer-based power splitter converts the input signal to two differential transmission lines feeding pre-drivers. Since input capacitance of the pre-driver transistors is relatively small, a large inductance is needed to resonate with it at 60 GHz. Hence, two series differential inductors are also added to the input matching network. As can be concluded from Fig 6.9 (b), even with the neutralization capacitors, the pseudo differential pair is not unconditionally stable for frequencies below 35 GHz. To ensure the pre-driver stability, a parallel RC network is added to its input to introduce >10 dB resistive loss at f_0<35 GHz. At the desired frequency band, the impedance of the 144 fF capacitor is lower than 51 Ω resistance, allowing input signal to reach the input of the pre-driver. However, the Q-factor of 144 fF MOM capacitor is inadequate poor at 60 GHz, increasing the insertion loss of the input matching network by 1.5 dB as shown in Fig. 6.24 (b).

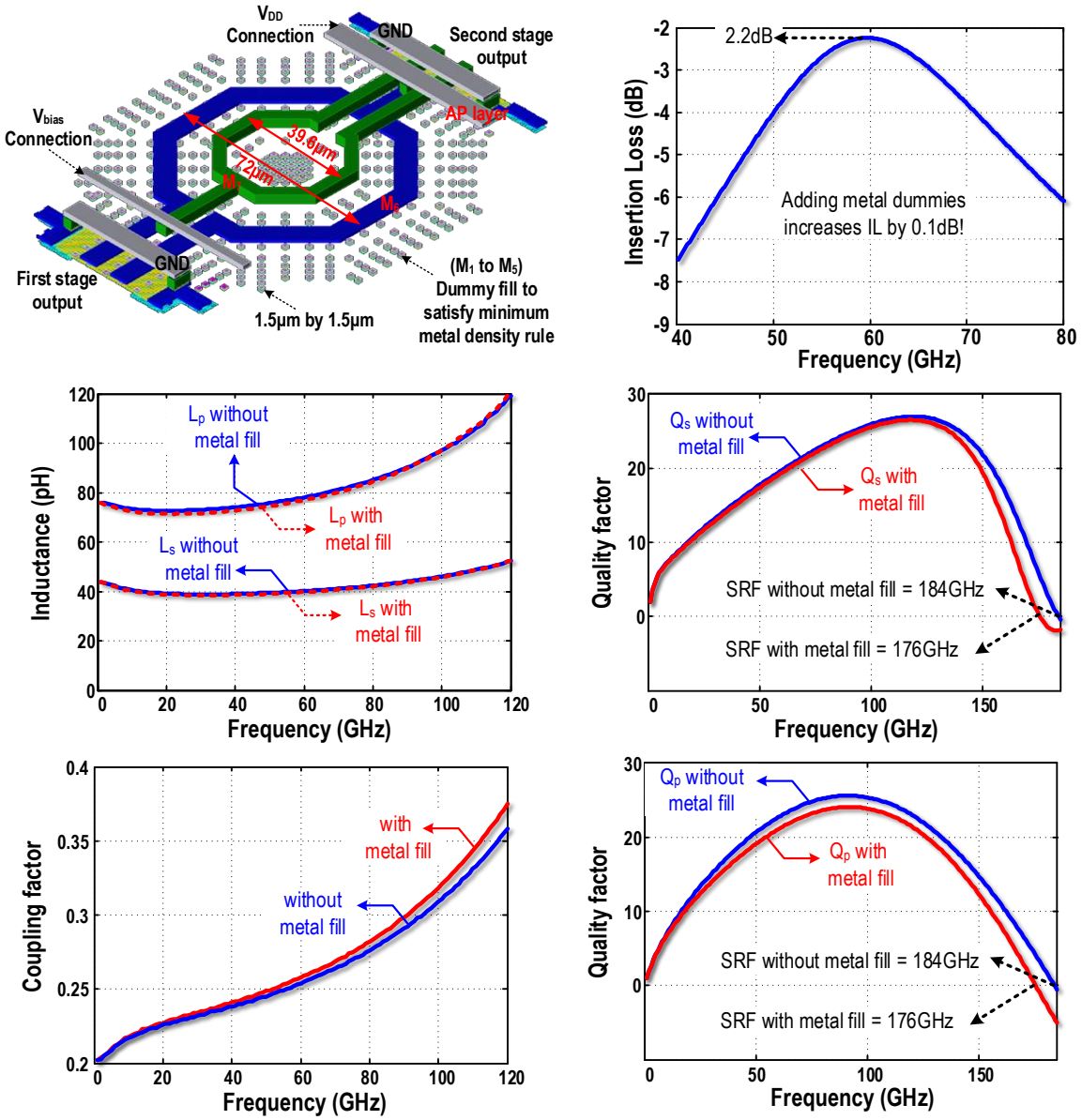


Figure 6.25: Different characteristics of the pre-driver matching network with and without dummy metals.

6.3.10 Effects of Dummy Metals on Transformer's Performance

To comply with the strict metal density rules, all transformers are completely filled with dummy metal strips. The amount of the metal fills directly below the transformer windings is kept at a minimum to reduce the extra parasitic capacitance and eddy current losses. However, EM simulations also reveal an additional loss of 0.1–0.4 dB for each matching network. Figure 6.25 shows different characteristics of the pre-driver matching network with and without dummy metals. Metal fills show negligible effect on the windings self-inductance and coupling factor k_m. However, eddy currents in the dummy fills increase the resistive loss and thus the transformer's Q-factor is degraded by ∼10%. Dummy fills also increase the capacitance, thus degrading the self-resonant frequency.

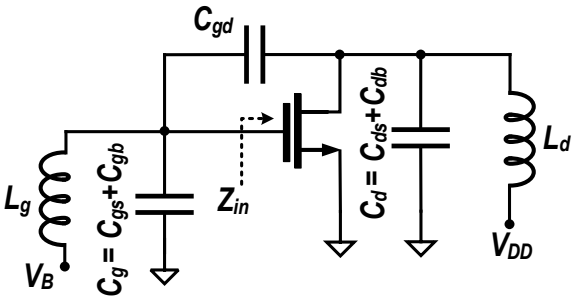


Figure 6.26: Common-source amplifier with its parasitic capacitances and matching networks.

6.3.11 Power Amplifier Stability

Stability is one of the major concerns in PA design. Since undesired oscillation can occur at any frequency, the load/source impedance of PA's transistors should be far away from the load/source stability circles over all frequencies. These conditions can be tested by employing Edwards and Sinsky Factors (μ_{source} and μ_{load}) [143]. It can be shown that either μ_{source} >1 or μ_{load} >1 is necessary and sufficient for the unconditional stability of a two-port network. Furthermore, a larger μ_{source} (μ_{load}) means that the amplifier's load (source) impedance is farther away from the load (source) instability circle and thus is more stable. Note that the Edwards and Sinsky stability condition should be separately satisfied for both differential-mode (DM) and common-mode (CM) excitations to ensure the PA's stability.

Any common-source amplifier along with its parasitic capacitance C_{gd} and matching networks (see Fig. 6.26) can potentially act as a dual circuit to a Pierce oscillator. The input admittance of the amplifier can be calculated by

$$Y_{in} = \frac{L_d L_g \left(C_g C_{gd} + C_g C_d + C_{gd} C d\right) s^4 + g_m L_d L_g C_{gd} s^3 + \left(L_d \left(C_{gd} + C_d\right) + L_g \left(C_g + C_{gd}\right)\right) s^2 + 1}{L_g s + L_g L_d \left(C_{gd} + C_d\right) s^3}. \tag{6.18}$$

As a consequence, the resonant frequency of this circuit may be estimated by

$$\omega_{osc}^2 = \frac{1}{\left(L_d + L_g\right) \cdot \left(C_{gd} + \frac{C_g C_d}{C_g + C_d}\right)}. \tag{6.19}$$

Since both gate and drain inductors are selected to respectively resonate with the transistor's input and output capacitances, ω_{osc} is always smaller but very close to the operating frequency band (≈0.7–0.8ω_0) where the transistor gain is higher but the insertion loss of the wideband transformers does not significantly increase. It increases the possibility of both CM and DM instabilities. The input conductance of the amplifier can be approximated by

$$G_{in} = -\frac{g_m L_d C_{gd} \omega_{osc}^2}{1 - L_d \left(C_{gd} + C_d\right) \omega_{osc}^2}. \tag{6.20}$$

Note that $L_d(C_{gd} + C_d) \cdot \omega_{osc}^2$ is always smaller than 1. Consequently, G_{in} is negative, indicating that the circuit can potentially oscillate. Note that the effective Q-factor of the PA input/output matching network is degraded by the 50 Ω load to about 1–2 at 60 GHz and even lower at ω_{osc}. Consequently, G_{in} cannot compensate the effective parallel resistance of

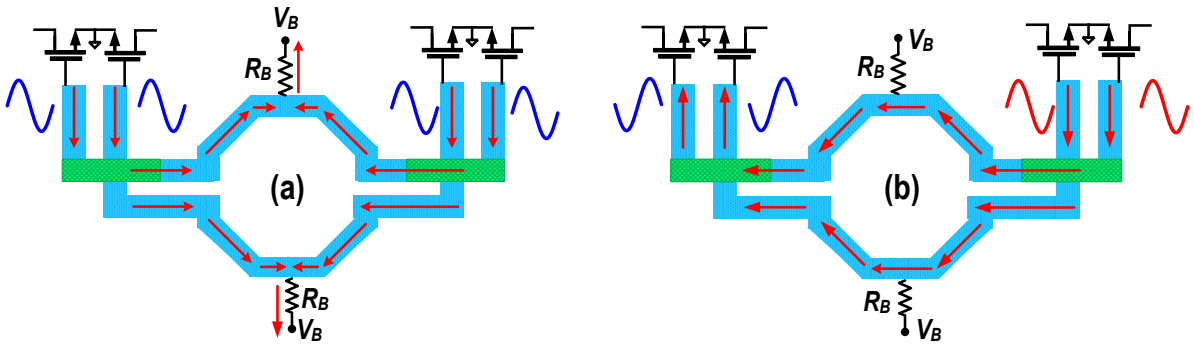


Figure 6.27: (a) Damping the undesired CM oscillation; (b) a combination of CM and DM oscillation.

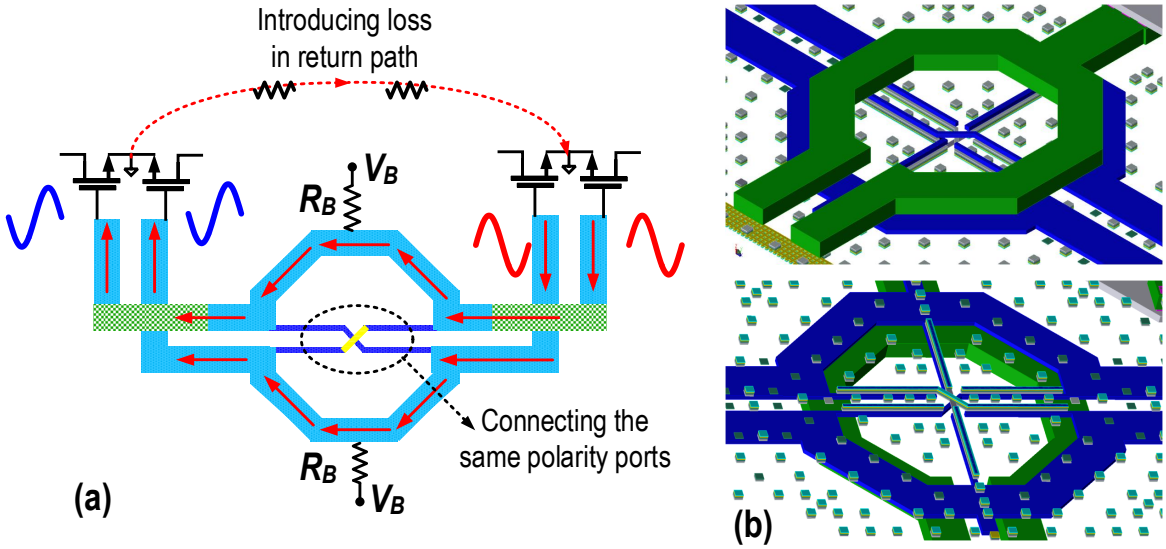


Figure 6.28: (a) Damping the undesired combination of CM and DM oscillation; (b) layout of the proposed transformer-based splitter.

those networks, and any DM oscillation is dampened. On the other hand, by employing the neutralization technique in the driver stages, the effective gate-drain capacitance, and thus $|G_{in}|$ significantly reduce, making that amplifier unconditionally stable in the differential mode.

The situation is entirely different for the CM stability. As explained in Section 6.3.3, the CM signals cannot see the 50 Ω input/output loads. Hence, the effective Q-factor of the input/output matching network is relatively large such that G_{in} can easily compensate the effective parallel resistance of those networks. Furthermore, the effective gate-drain capacitance is $C_{gd} + C_n$ as shown in Fig. 6.9 (e). Hence, the neutralization technique degrades the CM stability. Since ω_{osc} is very close to ω_0, neither adding an RC stabilization network at the MOS gate nor matching network loss can dampen the oscillation without affecting the precious power gain at the operating frequency. Fortunately, using relatively large resistors (R_B ~3 kΩ) between the center tap of the secondary windings of the input and inter-stage transformers and gate bias voltage can cancel out the CM currents at the transformer secondary winding as depicted in Fig. 6.27 (a). Hence, any CM oscillation will be dampened.

Interestingly, a combination of CM and DM oscillation can potentially happen in the transformer splitter. As shown in Fig. 6.27 (b), each differential pair could oscillate in CM but

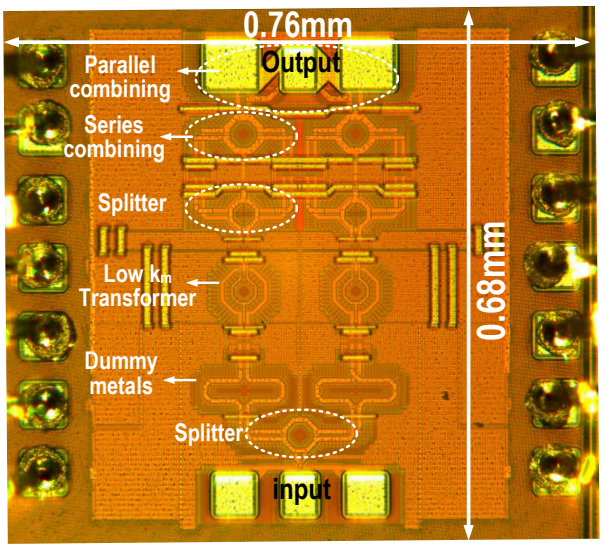


Figure 6.29: Chip micrograph.

with a 180° phase shift to each other. Hence, neither neutralization capacitors nor R_B will dampen this oscillation. We propose adding a weak cross connection between the splitter's in-phase ports to reduce the loop gain in this oscillation mode without affecting the splitter's primary function (see Fig. 6.28). Another solution would be to add a lossy path between the ground connections of two pseudo-differential pairs across the splitter.

6.4 Measurement Results

The proposed mm-wave PA is fabricated in TSMC 40 nm 1.1 V 1P7M LP CMOS technology. The chip micrograph is shown in Fig. 6.29 and is completely filled with dummy metal strips to comply with the strict metal density rules. Due to the use of transformer-based splitters and combiners, PA only occupies 0.26 mm^2 including the input and output pads. The PA is immune to the stray magnetic field since it is almost symmetrical across the axis of the input and output RF pads. The DC pads are wire bonded to a printed circuit board (PCB) while input and output RF pads are accessed by infinity I67 GSG probes.

Small-signal measurements are performed by the Agilent E8361 vector network analyzer, and the results are calibrated employing a Cascade Microtech (short-open-thru-load) calibration kit with the substrate specifications of Material: Alumina, Thickness: 635μm, Dielectric constant: 9.9. The measured and simulated small signal gain (S_{21}) of the PA is exhibited in Fig. 6.30. Note that the losses of the input and output GSG pads have not been de-embedded from simulations or measurements. With 1 V supply, the PA achieves a peak power gain of 21.6 dB at 58 GHz with BW_{-3dB} of 9.7 GHz (51.5 to 61.2 GHz). Compared to the simulation, the measured S_{21} is ~2.5 dB is lower and PA bandwidth is shifted ~2.5 GHz towards lower frequencies. The difference between the simulated and measured data is likely due to misalignment of the center frequencies of the bandpass response of PA's stages. It appears that the parasitic capacitances of the transistors are slightly larger than the values predicted in the model. The lower gain is probably due to resistive/inductive degeneration of common-source amplifiers.

Figure 6.30 (b) and (c) show the measured and simulated S_{11} and S_{22} from 35-to-67 GHz

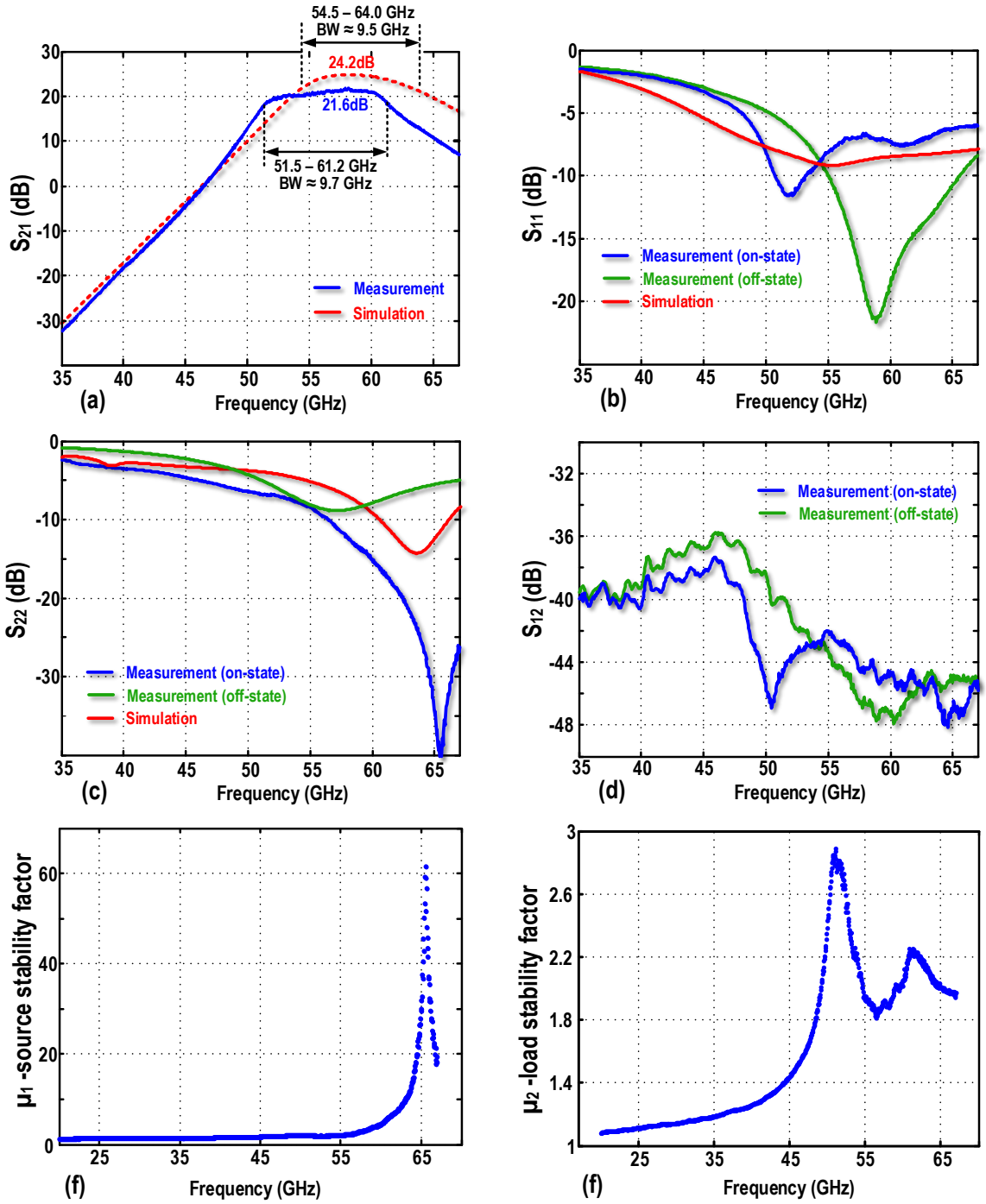
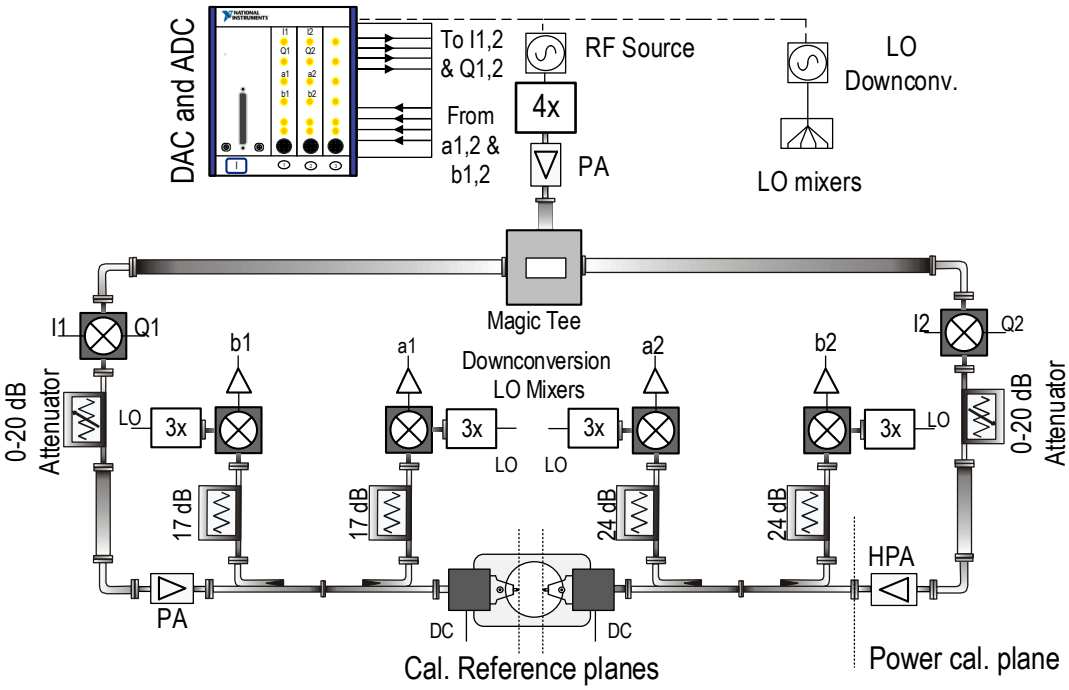


Figure 6.30: (a-d) S-parameter measurement results; measured (e) μ_{source} and μ_{load} stability factors.

with the 1 V supply. Both return losses conform to the trend predicted by simulations. The S_{11}, S_{22} are respectively better than -6 dB and -7 dB within 50–67 GHz. The reverse isolation (S_{12}) is better than -35 dB across the measured band. The S_{12} is almost identical when PA is on or off, showing the substrate leakage limits the PA's reverse isolation. The measured μ_{source} and μ_{load} stability factors are respectively shown in Fig. 6.30 (e) and (f), indicating the PA is unconditionally stable over the measured frequency band.

The large-signal measurements are performed by a mixed-signal active load-pull setup [144],



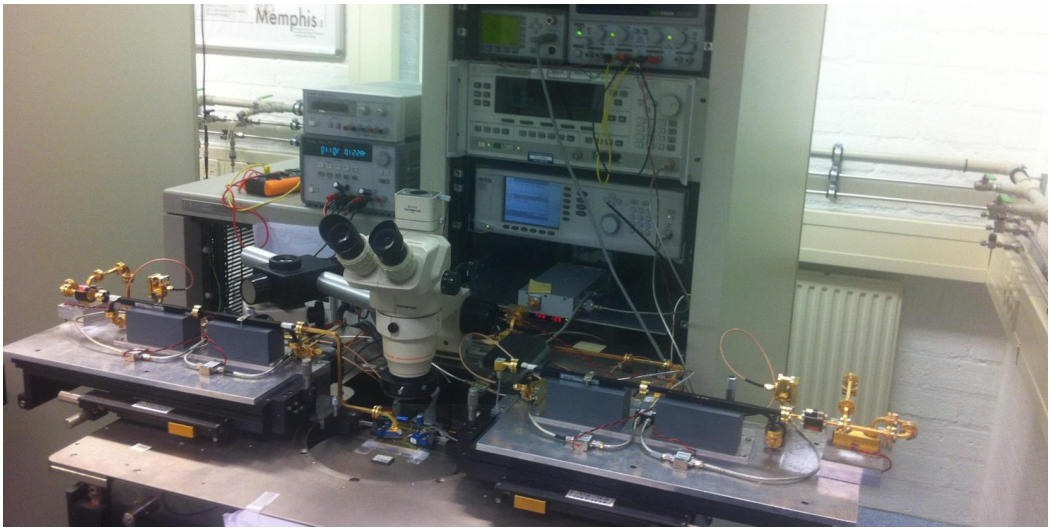


Figure 6.31: Mixed-signal active load-pull setup for large-signal measurements [144].

which is shown in Fig. 6.31[1]. A quick overview of the system is offered below, and the interested reader is directed to [144] for more details. The mm-wave input signal is generated by a ∼15 GHz signal generator followed by a 4× multiplier. The RF signal is then split using a waveguide Magic Tee. Note that the open-loop active load-pull systems realize the desired reflection coefficients by directly injecting a signal with a proper amplitude and phase into the device under test (DUT). Consequently, an in-phase/quadrature (IQ) mixer is placed in both input and output branches to control the amplitude and phase of RF signals. An attenuator is then employed to improve the dynamic range of the generated signal by maximizing the voltage swing at the IF ports of the mixer for a given mm-wave power level. A power amplifier is also exploited in both input and output sections to guarantee sufficient driving power for DUT. Two bi-directional waveguide reflectometers are finally added for the real-time measurement of the incident and

[1]The mixed-signal active load-pull measurement was implemented by Luca Galatro from TU Delft.

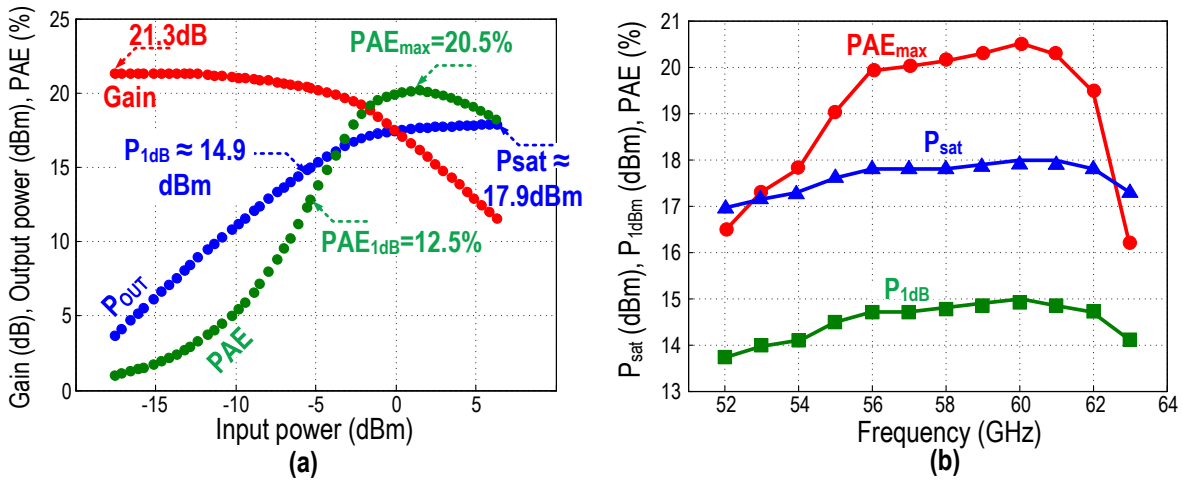


Figure 6.32: (a) Measured gain, output power and power added efficiency versus input power; (b) Measured P_{sat}, P_{1dB} and PAE across frequency.

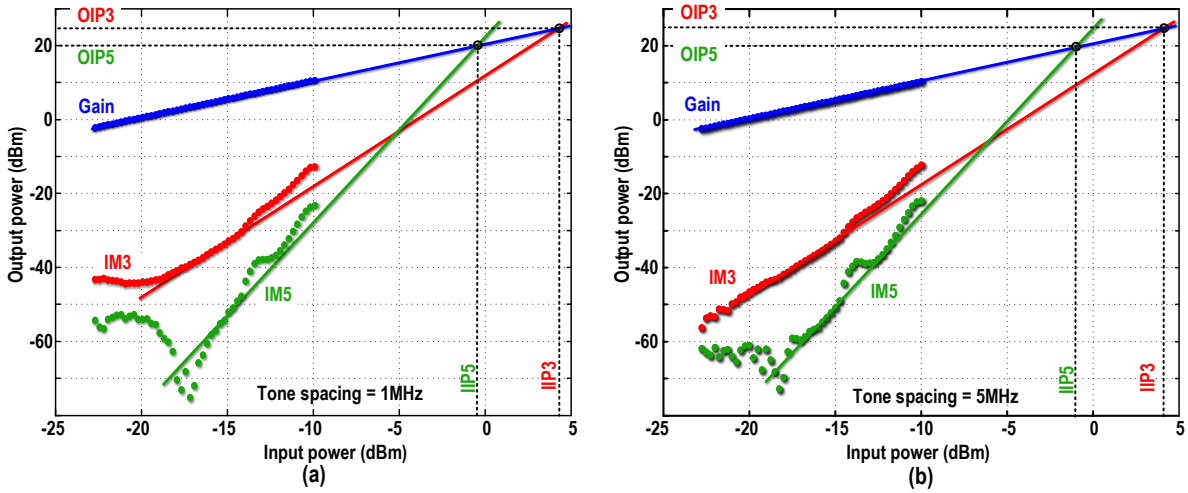


Figure 6.33: Measured two-tone intermodulation for the PA with tone frequency spacing of (a) 1 MHz and (b) 5 MHz.

reflected waves. The coupled waves are then down-converted by fundamental mixers and the resulting IF signals are acquired with 14-bits 40 MHz ADC converters.

Figure 6.32 (a) illustrates the measured output power, gain, and PAE versus input power at 58 GHz for a 1 V supply. The monotonic behavior between the input/output power also indicates PA's stability. The measured P_{1dB} and P_{sat} are respectively 14.9 dBm and 17.9 dBm. Consuming ~0.28 A from a 1 V supply, the peak-PAE is 20.5% for 1.5 dBm input power. However, the simulated P_{sat} and PAE are respectively 18.6 dBm and 25%. The difference between the simulated and measured data is likely due to the greater imbalance in the CM resonance and impedance transformation ratio of different input ports of the output matching. Figure 6.32 (b) shows the measured P_{sat}, P_{1dB} and PAE over the bandwidth of the PA. The PA maintains over 16.9 dBm P_{sat}, 13.8 dBm P_{1dB} and 16% PAE from 52 GHz to 63 GHz.

A two-tone intermodulation measurement is performed on the PA to assess its linearity. Figure 6.33 shows the third-order and fifth-order intermodulation distortion (IMD_3 and IMD_5) as a function of input power for different frequency spacing between the two tones. It can

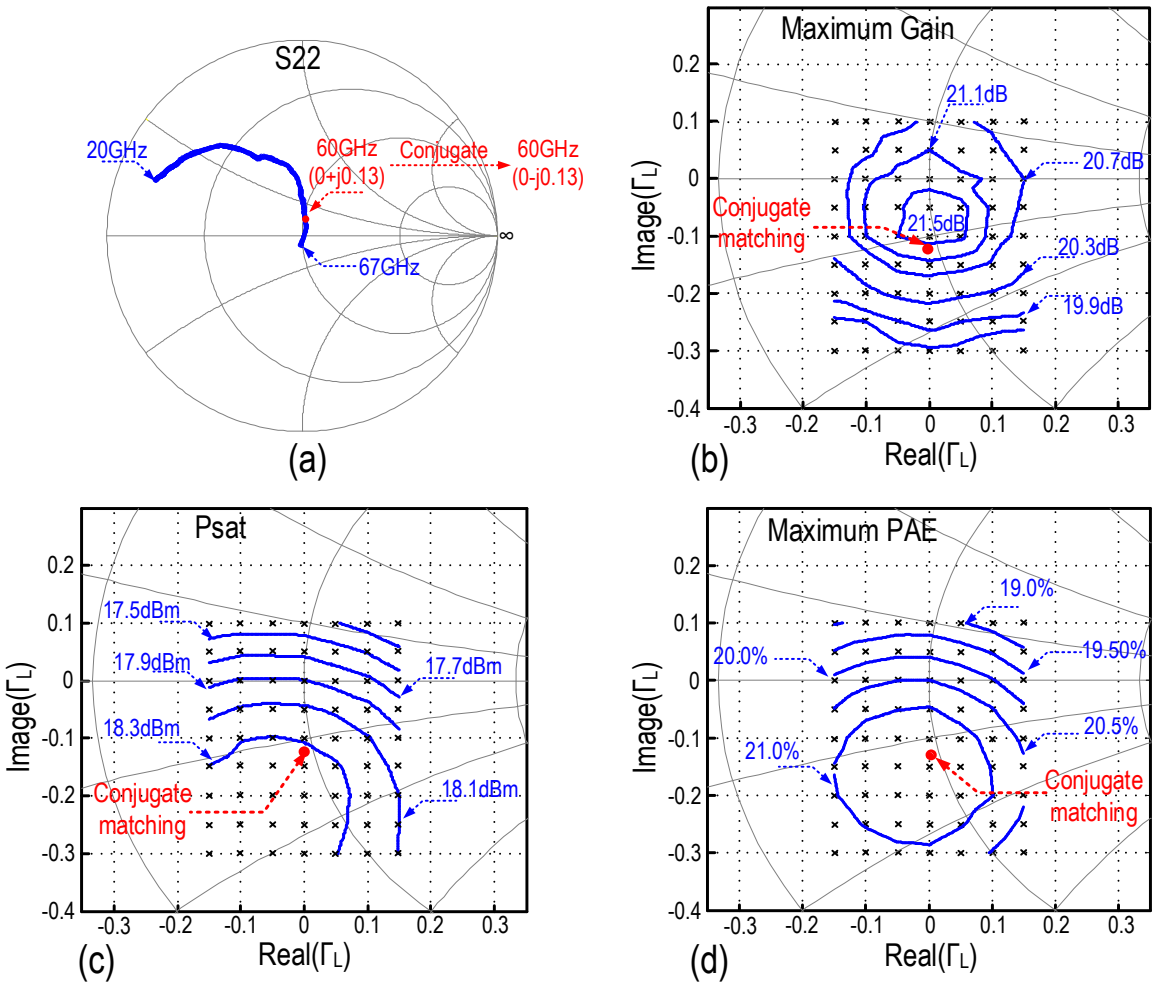


Figure 6.34: Measured (a) S_{22}, (b) constant gain, (c) constant P_{sat}, and (d) constant PAE contours at 60 GHz.

be seen that the IMD_3 and IMD_5 point respectively demonstrate a slope of 30 dB/dec and 50 dB/dec, as would be expected in a linear amplifier. The measured IIP_3 and OIP_3 are 4 dBm and 24 dBm, respectively. On the other hand, the measured IIP_5 and OIP_5 are -0.5 dBm and 20 dBm, respectively.

The mixed-signal open-loop active load-pull setup also allows generating any desired reflection coefficient at both input and output ports of the DUT by controlling the amplitude and phase of injected signals. Consequently, the large signal performance of the proposed PA is evaluated for -0.15+j0.3$\leq \Gamma_L \leq$0.15+j0.15 (40$\leq R_L \leq$60, and -18$\leq X_L \leq$6) at 60 GHz. Figure 6.34 illustrates PA's constant gain, P_{sat}, and PAE contours and also verifies the PA stability over load variation.

Table 6.2 shows a comparison of state-of-the-art 60 GHz CMOS PAs. Our PA achieves comparable BW_{-3dB} as in a 28 nm PA [141] (which uses higher f_{max} devices) but with a much higher PAE. For $P_{sat}\approx$18 dBm, only class-AB PA in [124] demonstrates a better PAE but at a lower gain and BW. Furthermore, the product of PAE and BW reaches the best reported.

Table 6.2: Comparison table of 60 GHz CMOS power amplifiers.

	This Work	Zhao JSSC2013	Chen ISSCC2013	Chen ISSCC2011	Thyagarajan TCAS2014	Law ISSCC2010
CMOS Technology	40nm	40nm	65nm	65nm	28nm	90nm
Supply Voltage (V)	1	1	1	1	2.1	1.2
Frequency (GHz)	60	60	60	60	60	60
Max Gain (dB)	21.5	21.2	N/A	20.3	24.4	20.6
3dB BW (GHz)	9.7	5.5	7	9	11	8
BW/f_c (%)	16	10	11.5	15	18.4	13.4
P_{-1dB} (dBm)	14.9	14	N/A	15	11.7	18.2
P_{-1dB} variation over BW	1.2dB	3 dB	N/A	1.2 dB	3.7 dB	N/A
P_{sat} (dBm)	17.9	17.4	9.6	18.6	16.5	19.9
P_{sat} variation over BW	1dB	0.8 dB	2 dB	0.6dB	2.5 dB	N/A
PAE_{max} %	20.5	28.5	28.5	15.1	12.6	14.2
Active area (mm^2)	0.25	0.115†	0.11†	0.175†	0.22†	1.75†
FoM‡	88.1	88.7	N/A	86.5	87.5	87.6
PAE·BW/fc	3.32%	2.78%	3.32%	2.27%	2.31%	2.31%
Topology	3 stage CS Parallel/series E/F_2	1st-stage CG 2nd, 3rd stage CS Series Comb.	Cartesian Digital-to-RF E/F_2	3 stage CS Series Comb.	1st-stage CS 2nd, 3rd stage CA Parallel Comb.	2 stage CS Wilkinson

CS: common source, CG: common gate, CA: cascode
†: Graphically estimated (including RF pads)
‡: FoM = P_{sat}[dBm] + $Gain$[dB] + 20log(f_c[GHz]) + 10log(PAE_{max}[%])

6.5 Conclusion

The benefits, constraints, and trade-offs of different transmitter structures and extended class-E/F_2 PA have been investigated from the mm-wave perspective. Several design techniques are employed in this design to achieve the best product of PAE and bandwidth. First, this PA utilizes a proper second-harmonic termination in the last stage so that it can operate as a class-E/F_2 switched-mode PA at the saturation point. Second, the additional resonance is realized without degrading the insertion loss of the output matching network and by exploiting a different transformer behavior in common-mode and differential-mode excitations. Third, a current-voltage combiner is proposed to simultaneously optimize f_{max} of the output transistors, PA's output power, and the insertion loss of the output matching network. Forth, low/moderate coupling-factor transformers are used in the preliminary stages to provide the transistors optimum load for a larger bandwidth. Fifth, the PA is stabilized against the combination of DM and CM oscillation mode. The resulting new proposed architecture of a fully integrated 60 GHz power amplifier was realized in 40-nm bulk CMOS. The PA prototype produces a saturated power of 17.9 dBm with 20.5% PAE at 60 GHz from a 1 V supply. The PA maximum gain is 21.5 dB, and its -3 dB bandwidth exceeds 9 GHz. The PA is stability was also verified over load variation with a mixed-signal active load-pull measurement setup.

Chapter

7

Bluetooth-Low Energy Transmitter

We propose a new transmitter (TX) architecture for ultra-low power radios[1]. An all-digital PLL employs a digitally controlled oscillator with switching current sources to reduce supply voltage and power without sacrificing its phase noise and startup margins. It also reduces 1/f noise allowing the ADPLL, after settling, to reduce its sampling rate or shut it off entirely during direct DCO data modulation. The switching power amplifier integrates its matching network while operating in class-E/F_2 to maximally enhance its efficiency. The transmitter is realized in 28nm CMOS and satisfies all metal density and other manufacturing rules. It consumes 3.6 mW/5.5 mW while delivering 0 dBm/3 dBm RF power in Bluetooth Low-Energy.

7.1 Introduction

Ultra-low-power (ULP) radios underpin short-range communications for wireless internet-of-things (IoT). Since RF transmitters (TX) have consumed a significant portion, if not the majority, of the radio's power, the IoT system lifetime tends to be severely limited by the TX power consumption and available battery technology.

Figure 7.1 shows the system lifetime for various battery choices as a function of current consumption. State-of-the-art Bluetooth Low Energy (BLE) radios [8, 10] consume ~7 mW and thus can *continuously* operate no more than 40 hours on an SR44 battery, which has a comparable dimension to the radio module. This directly causes inconvenient battery replacements at least every few months, which limits their attractiveness from the market perspective. The lifetime can be easily increased by employing larger batteries but that comes at a price of increased weight and dimensions and it is clearly against the miniaturization vision of IoT. This has motivated an

[1]This chapter is based on the paper published in the IEEE Journal of Solid-State Circuits [145].

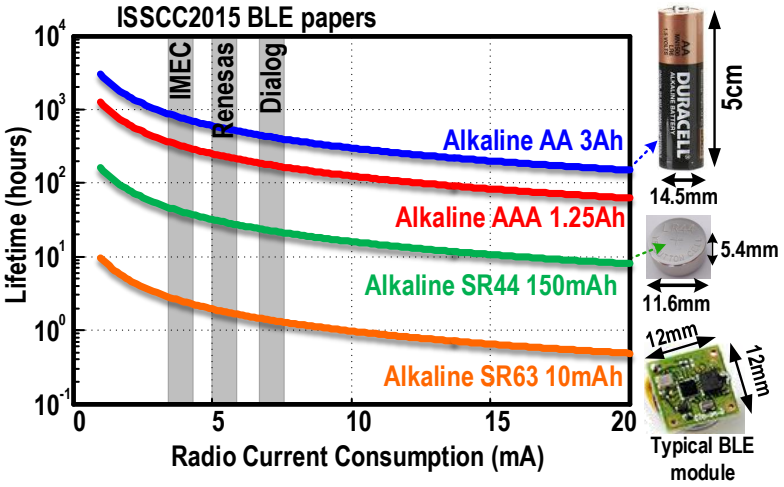


Figure 7.1: BLE system lifetime versus radio current consumption for various battery types.

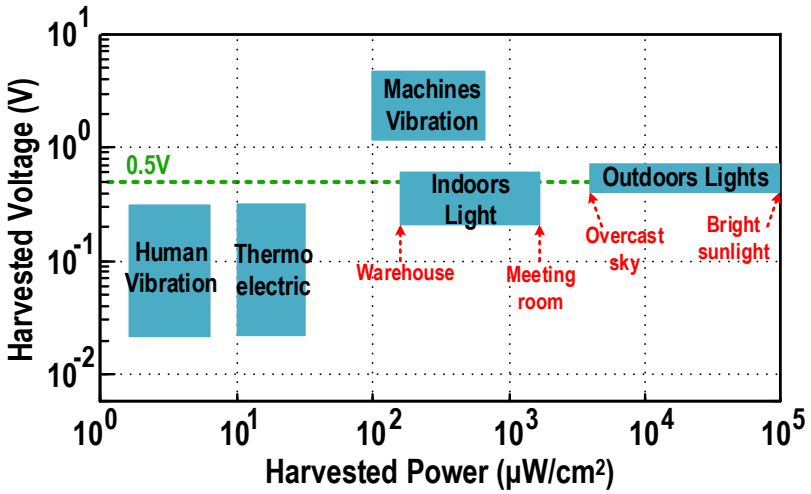


Figure 7.2: Delivered voltage and power density for various harvester types.

intensive research leading to miniaturized transceivers with a high power efficiency [8–10,146–154].

Energy harvesting from a surrounding environment can enable and further spur the IoT applications by significantly extending their lifetime. The delivered voltage versus power density of different harvesting methodologies is depicted in Fig. 7.2 [152] [155]. Solar cells offer the highest harvested power per area in both indoor and outdoor conditions. However, they provide lower voltages (0.25–0.75 V) than the expected deep-nanoscale CMOS supply of ∼1 V. Hence, boost converters are typically used to bring the supply level up to the required ∼1 V. As can be gathered from Table 7.1, the relatively poor efficiency (≤80%) of state-of-the-art boost converters wastes the harvested energy, thus worsening the system-level efficiency, in addition to increasing the hardware complexity coupled with issues of switching ripples. Consequently, it would be highly desirable for the ULP transceivers to operate directly from the harvested voltage.

In this paper, several new system and circuit techniques are exploited to enhance the ULP transmitter efficiency: First, the most energy-hungry circuitry, such as a digitally controlled oscillator (DCO) and an output stage of a power amplifier (PA), can operate directly at the

Table 7.1: Performance summary of state-of-the-art boost converters.

	[156] ISSCC'12	[157] ISSCC'14	[158] ISSCC'15
Technology	N/A	65nm CMOS	0.18μm CMOS
Input voltage range	0.1–2.9 V	0.15–0.5 V	0.45–3 V
Output voltage range	3 V	0.5–0.6 V	3.3 V
Efficiency @V_{in}=0.5V	$\leq$ 80%	$\leq$ 72.5%	$\leq$ 78.5%

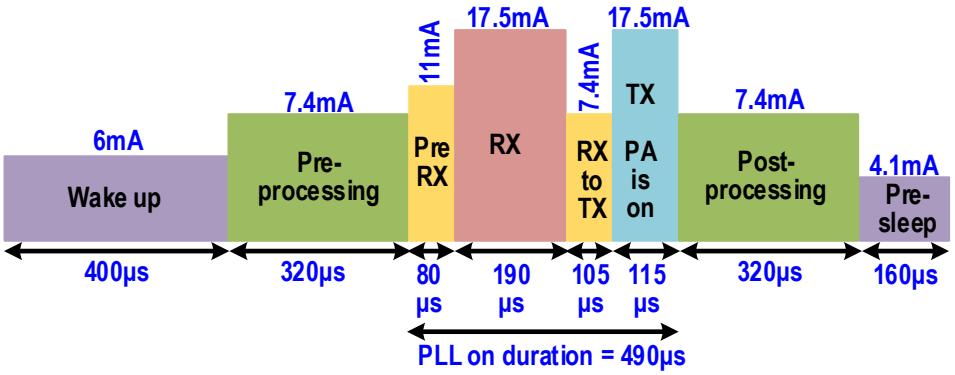


Figure 7.3: Power consumption breakdown of a Texas Instruments CC2541 BLE device during a single connection event.

low voltage of harvesters. Second, a new switching current-source oscillator optimized for 28 nm CMOS reduces power and supply voltage without compromising the robustness of the oscillator start-up or loading its tank quality factor. Third, thanks to the low wander (i.e, low flicker noise) of the DCO, digital power consumption of the rest of all-digital PLL (ADPLL) is saved by scaling the rate of a sampling clock to the point of complete stillness. Last, a fully integrated differential class-E/F_2 switching PA is utilized to optimize high power added efficiency (PAE) at low output power of 0–3 dBm.

The paper is organized as follows: Section 7.2 introduces a new RF oscillator topology that is suitable for ultra-low voltage/power applications. The tradeoffs between the output power, matching network insertion loss, drain and power added efficiency (PAE) of the class-E/F_2 PA are investigated in Section 7.3. The all-digital PLL (ADPLL) and the TX architecture are discussed in Section 7.4. Section 7.5 presents extensive experimental results.

7.2 Switching Current-Source DCO

Designers shall be able to better optimize the power budget of various IoT radio blocks by understanding the characteristics of BLE power profile. Figure 7.3 illustrates an example power transient breakdown of a commercial BLE device, CC2541, from Texas Instruments during a single connection event [159]. Detailed characteristics of the BLE power profile will, of course, depend on a specific application and the BLE device itself. However, the durations of data reception and transmission will typically remain stable for a specific event. Consequently, representative activity times of various BLE RF blocks can be discerned from Fig. 7.3. Henceforth, the frequency synthesizer activity is at least 3 times longer than that for a PA. Furthermore,

the literature survey indicates that the power consumption of a PLL is merely 3–4 times lower than that of the PA at the maximum BLE output power of 1 mW. This ratio gets even more dramatic as the transmitter output power goes down. By considering both scenarios, the energy consumption of the frequency synthesizer could be as large as the PA. Consequently, RF oscillators, as one of the BLE transceiver's most power hungry circuitry, must be very power efficient and preferably operate directly at the energy harvester output. In this section, a new RF oscillator topology is proposed to address the aforementioned constraints without sacrificing manufacturability and phase purity [160].

7.2.1 Oscillator Power Consumption Tradeoffs

The oscillator phase noise (PN) requirements can be calculated by considering the toughest BLE blocking profile:

$$\mathcal{L}(\Delta\omega) = P_{signal} - P_{blocker} - SNR_{min} - 10log_{10}(BW). \tag{7.1}$$

The received packet error rate (PER) must be better than 30.8% while the wanted signal is just 3 dB above the reference sensitivity level of -70 dBm and in face of an in-band blocker of -40 dBm located at 3 MHz offset from the desired channel. Furthermore, the required signal-to-noise ratio (SNR) should be better than 15 dB to support such PER for a GFSK signal with a modulation index $m = 0.5$ [161]. By replacing the aforementioned values in (7.1), PN shall be better than -105 dBc/Hz at $\Delta\omega = 2\pi \cdot 3\,\text{MHz}$. Hence, the PN requirements are quite trivial for IoT applications and can be easily met by LC oscillators as long as Barkhausen start-up criterion is satisfied over process, voltage and temperature (PVT) variations[1]. Consequently, reducing oscillator power consumption, P_{DC}, is the ultimate goal in IoT applications.

The PN of any class of an RF oscillator (i.e., class-B) at an offset frequency $\Delta\omega$ from its resonating frequency ω_0 can be expressed as

$$\mathcal{L}(\Delta\omega) = 10\log_{10}\left(\frac{KT}{2\,Q_t^2\,\alpha_I\,\alpha_V\,P_{DC}} \cdot F \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2\right) \tag{7.2}$$

where, K is the Boltzmann's constant, T is the absolute temperature, Q_t is the LC-tank quality factor; α_I is the current efficiency, defined as ratio of the fundamental current harmonic I_{ω_0} over the oscillator DC current I_{DC}; and α_V is the voltage efficiency, defined as a ratio of the single-ended oscillation amplitude, $V_{osc}/2$, over the supply voltage V_{DD} [88] [163]. Furthermore, F is the effective noise factor of the oscillator.

Eq. 7.2 clearly demonstrates a trade-off between the oscillator's P_{DC} and PN. Furthermore, the oscillator's figure-of-merit (FoM) normalizes the PN performance to the oscillation frequency and power consumption, yielding

$$FoM = 10\log_{10}\left(\frac{10^3 KT}{2\,Q_t^2\,\alpha_I\,\alpha_V} \cdot F\right) \tag{7.3}$$

[1]Ring oscillators can also satisfy such a relaxed phase noise requirement. However, they consume much higher power than LC oscillators at $f_0 \geq 1\,\text{GHz}$ [162].

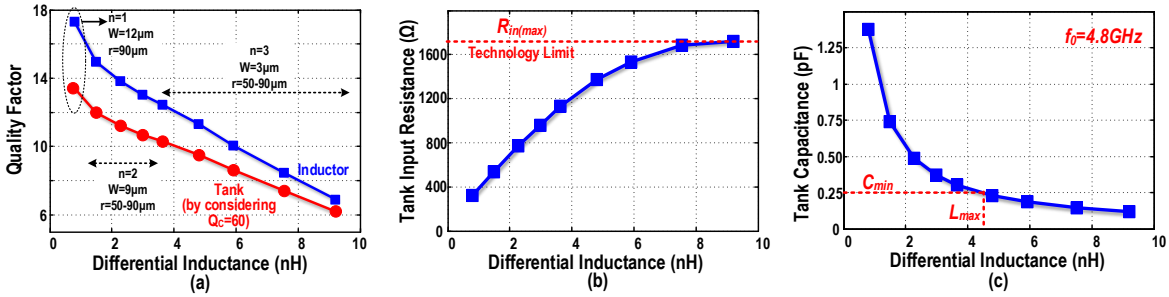


Figure 7.4: Dependency of various inductor parameters in 28 nm LP CMOS across inductance value: (a) inductor and tank Q-factor; (b) equivalent differential input resistance of the tank; and (c) required tank capacitance at 4.8 GHz resonance. Note that at this point the inductors are without dummy metal fills.

The effective noise factor F is expressed by [27] [21]

$$F = \frac{R_{in}}{2KT} \cdot \sum_i \frac{1}{2\pi} \int_0^{2\pi} \overline{i_{n,i}^2(\phi)} \cdot \Gamma_i^2(\phi)\, d\phi \tag{7.4}$$

where, $\phi = \omega_0 t$, $\overline{i_{n,i}^2(\phi)}$ is the white current noise power density of the ith noise source, Γ_i is its relevant ISF function from the corresponding i^{th} device noise [31]. Finally, R_{in} is an equivalent differential input parallel resistance of the tank's losses. The oscillator I_{DC} may be estimated by one of the following equations:

$$I_{DC} = \frac{I_{\omega_0}}{\alpha_I} \xrightarrow{I_{\omega_0}=\frac{V_{osc}}{R_{in}}} I_{DC} = \frac{V_{osc}}{R_{in}} \cdot \frac{1}{\alpha_I} \xrightarrow{V_{osc}=2\alpha_V V_{DD}} I_{DC} = \frac{2V_{DD}}{R_{in}} \cdot \frac{\alpha_V}{\alpha_I}. \tag{7.5}$$

As a result, the RF oscillator's P_{DC} is derived by

$$P_{DC} = \frac{V_{DD}^2}{R_{in}} \cdot \frac{\alpha_V}{\alpha_I}. \tag{7.6}$$

Eq. 7.6 indicates that the minimum achievable P_{DC} can be expressed in terms of a set of *optimization* parameters, such as R_{in}, and a set of *topology*-dependent parameters, such as minimum supply voltage ($V_{DD,min}$), current and voltage efficiencies.

Lower P_{DC} is typically achieved by scaling up R_{in}=$L_p\omega_0 Q_t$ simply via a large multi-turn inductor, as in [164]. For example, while maintaining a constant Q_t, doubling L_P would theoretically double R_{in}, which would reduce P_{DC} by half but at a cost of a 3 dB PN degradation. However, at some point, that tradeoff stops due to a dramatic drop in the inductor's self-resonant frequency and Q-factor. Figure 7.4 (a) shows the simulated Q-factor of several multi-turn inductors in 28 nm CMOS versus their inductance values. As the inductor enlarges, the magnetic and capacitive coupling to the low-resistivity substrate increases, such that the tank Q-factor drops almost linearly with L_P. As can be gathered from Fig. 7.4 (b), this constraint sets an upper limit on maximum R_{in}=$L_p\omega_0 Q_t$, which is chiefly a function of the technology node. Note that the inductor's value is largely dependent on its physical dimensions, rather than on the technology. However, the tank Q-factor is a bit degraded in the most recent process nodes (i.e., 28 nm) mainly due to more stringent minimum metal density rules, closer separation between the top-metal and substrate as well as thinner lower-level metals that are used in metal-oxide-metal

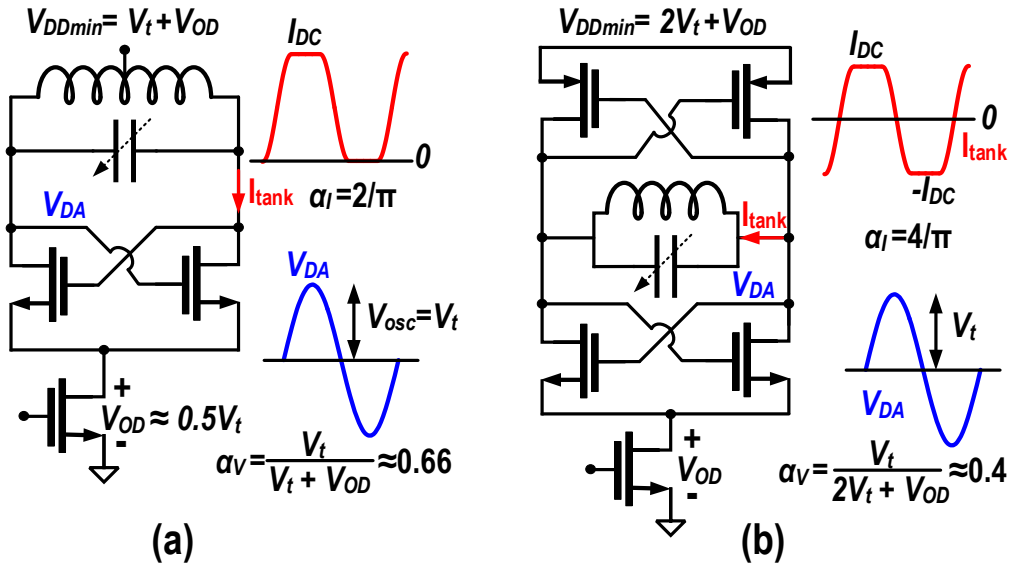


Figure 7.5: $V_{DD,min}$, α_I and α_V parameters for: (a) cross-coupled NMOS; and (b) complementary push-pull oscillators.

Table 7.2: Minimum P_{DC} for different RF oscillator topologies.

Topology	$V_{DD,min}$ †	α_V ‡	α_I *	P_{DCmin}	$\alpha_V.\alpha_I$
OSC_N	$V_t + V_{OD} \approx 1.5V_t$	0.66	$2/\pi$	$4.66\,V_t^2/R_{in}$	0.42
OSC_{NP}	$2V_t + V_{OD} \approx 2.5V_t$	0.4	$4/\pi$	$3.92\,V_t^2/R_{in}$	0.51
OSC_{NP} with tail filter	$2V_t + V_{OD} \approx 2.5V_t$	0.63	$4/\pi$	$6.2\,V_t^2/R_{in}$	0.8
Class-C_{NP}	$2V_t + V_{OD} \approx 2.5V_t$	0.25	2	$0.15\text{mW} + 1.56\,V_t^2/R_{in}$	0.5
Class-D	$\approx V_t$	1.635	0.5	$6.54\,V_t^2/R_{in}$	0.82
Class-F_3	$V_t + V_{OD} \approx 1.5V_t$	0.66	$2/\pi$	$4.66\,V_t^2/R_{in}$	0.42
This work	$V_t + V_{OD} \approx 1.5V_t$	0.33	$4/\pi$	$1.2\,V_t^2/R_{in}$	0.42

† by considering V_{OD}=0.5V_t for the current source, ‡ at the minimum V_{DD}, * ideal value

(MoM) capacitors. As a consequence, it is expected that $R_{in(max)}$ slightly reduces by migrating to finer CMOS technologies.

Parasitic capacitance of inductor windings, gm-devices, switchable capacitors and oscillator routings determines a minimum floor of the tank's capacitance, which appears to be ∼250 fF at $f_0 = 4.8$ GHz. It puts another restriction on L_p and $R_{in(max)}$ to ∼4.5 nH and ∼1.3 $k\Omega$ and sets an lower limit on P_{DC} of each oscillator structure. Under this condition, the tank's Q-factor drops to ≤9. This explains the poor FoM of RF oscillators in modern BLE transceivers.

The topology-dependent parameters also play an important role in trying to reduce P_{DC}. Eq. (7.6) favors structures that offer higher α_I or can sustain oscillation with smaller V_{DD} and α_V. On the other hand, $\alpha_V \cdot \alpha_I$ should be maximized to avoid any penalty on FoM [163] [165], as evident from (7.2). Consequently, to efficiently reduce P_{DC} without disproportionately worsening the FoM, it is desired to employ structures with a higher α_I and a lower minimum V_{DD}. To get a better insight, Fig. 7.5 shows such effects for the traditional cross-coupled NMOS-only

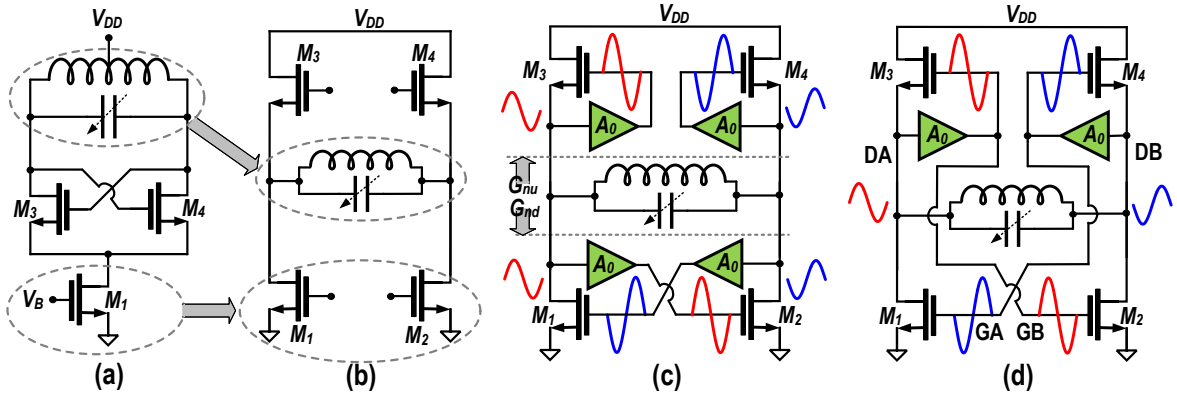


Figure 7.6: Evolution towards the switching current-source oscillator.

(OSC_N) and complementary push-pull (OSC_NP) structures [25] [45]. Due to the less stacking of transistors, the $V_{DD,min}$ of OSC_N can go 40% lower than in OSC_NP. However, α_I of OSC_NP is doubled due to the switching of tank current direction every half period. Its oscillation swing, and thus α_V, is also 50% smaller. Hence, OSC_NP offers $\sim$3$\times$ lower α_V/α_I. However, both structures demonstrate similar $\alpha_V \cdot \alpha_I$ product [166]. Consequently, each of them has its own set of advantages and drawbacks such that the minimum achievable P_{DC} and FoM is almost identical, as shown in Table 7.2. Note that applying a tail filtering technique to a class-B oscillator increases its α_V [163] [167], which is in line of the FoM optimization but against the P_{DC} reduction, as evident from (7.2) and (7.6). Furthermore, while maintaining the same R_{in}, a class-F_3 operation does not reduce P_{DC} of traditional oscillators, since its minimum V_{DD}, α_V and α_I are identical to OSC_N [21].

A push-pull class-C oscillator appears as an excellent choice for ULP applications due to its largest α_I and smallest α_V [168], as per Table 7.2. However, it needs an additional complex biasing circuitry (e.g., an opamp) to guarantee the proper oscillator start-up and to keep the transistors in saturation during the on-state. There are also strong mutual tradeoffs between the biasing circuit's P_{DC}, oscillator's amplitude stability and PN, much intensified in ULP applications where the tank capacitance tends to be smaller [169]. As a consequence, the biasing circuitry can end up consuming comparable power as the ULP oscillator itself. On the other hand, V_{DD} of class-D oscillators can go below a threshold voltage, V_t. However, due to hard switching of core transistors, its α_V and α_I are respectively higher and lower than other structures [103], as shown in Table 7.2. According to (7.6), this trend is against the P_{DC} reduction. Consequently, the current oscillator structures have issues with reaching simultaneous ultra-low power *and* voltage operation.

In this work, we propose to convert the fixed current source of the traditional NMOS topology into a structure with alternating current sources such that the tank current direction can change every half-period. Consequently, the benefits of low supply of the OSC_N topology and higher α_I of OSC_NP structure are combined to reduce power consumption further than practically possible in the traditional oscillators.

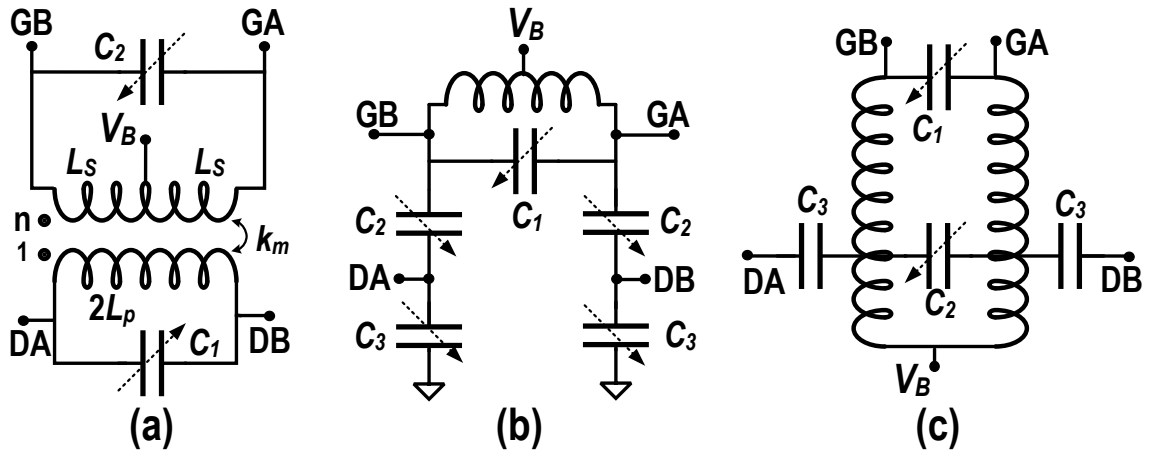


Figure 7.7: Various options of a tank providing voltage gain.

7.2.2 Switching Current Source Oscillator

Figure 7.6 shows an evolution towards the switching current-source oscillator. The $\mathrm{OSC_N}$ topology is chosen as a starting point due to its low V_{DD} capability. To reduce P_{DC} further, it is desired to switch the direction of the LC-tank current in each half period, which will double α_I. Consequently, we propose to split the fixed current source $\mathrm{M_1}$ in Fig. 7.6 (a) into two switchable current sources, $\mathrm{M_1}$ and $\mathrm{M_2}$, as suggested in Fig. 7.6 (b). This allows for the tank to be disconnected from the V_{DD} feed and be moved in-between the upper and lower NMOS transistor pairs to give rise to an H-bridge configuration. In the next step, the passive voltage gain blocks, A_0, are added to the NMOS gates, as shown in Fig. 7.6 (c). Both upper and lower NMOS pairs should each independently demonstrate *synchronized* positive feedback to realize the switching of the tank current direction. The "master" positive feedback enforces the differential-mode operation and is realized by the lower-pair transistors configured in a conventional cross-coupled manner. Its negative conductance seen by the tank may be estimated by

$$G_{down} = \frac{-A_0}{4} \cdot \left(g_{m1}(\phi) + g_{m2}(\phi)\right). \tag{7.7}$$

On the other upper side, the differential-mode oscillation of the tank is reinforced by the $\mathrm{M_{3,4}}$ devices which realize the second positive feedback. [1] The negative conductance seen by the tank into the upper pair can be calculated by

$$G_{up} = G_{down} = \frac{-\left(A_0 - 1\right)}{4} \cdot \left(g_{m3}(\phi) + g_{m4}(\phi)\right). \tag{7.8}$$

Eq. (7.8) clearly indicates that the voltage gain block is necessary and A_0 must be safely larger than 1 to be able to present a negative conductance to the tank, thus enabling the H-bridge switching. By merging the redundant voltage gain blocks, the proposed switching current-source oscillator is shown in Fig. 7.6 (d). Note that the tank with an implicit voltage gain can be realized by using a capacitive divider, autotransformer or step-up transformer, as illustrated in Fig. 7.7. The transformer-based tank is chosen in this work due to its simplicity.

[1] It should be noted that the "master/slave" view is mainly valid from a small-signal standpoint. Both are equally important when considering the large-signal switching operation.

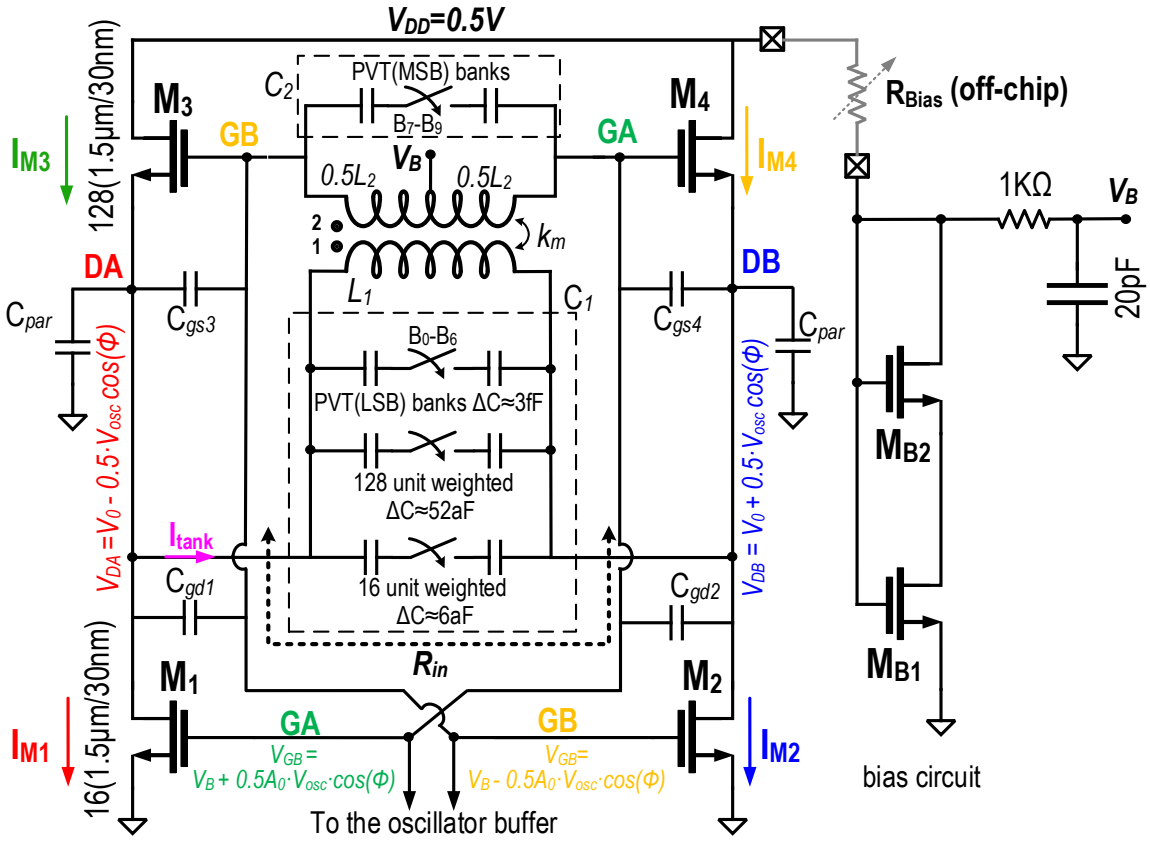


Figure 7.8: Schematic of the proposed switching current-source oscillator.

Figures 7.8–7.9 illustrate the proposed oscillator schematic as well as waveforms and various operational regions of M_{1-4} transistors across the oscillation period. The two-port resonator consists of a step-up 1:2 transformer and tuning capacitors, C_1, C_2, at its primary and secondary windings. The transistors $M_{1,2}$ set the oscillator's DC current, while the $M_{3,4}$ pair acts as a switching current source. Both $M_{1,2}$ and M_{3-4} pairs play an equally vital role of switching the tank current direction. As can be gathered from Fig. 7.9, G_B oscillation voltage is high within the first half-period. Hence, only M_2 and M_3 transistors are on and the current flows from left to right side of the tank. However, M_1 and M_4 are turned on for the second half-period and the tank's current direction is reversed. Consequently, just like in the push-pull structure, the tank current flow is reversed every half-period, thus doubling the oscillator's α_I to $4/\pi$.

The V_{DD} of the proposed oscillator can be as low as $V_{OD1}+V_{OD3}\approx V_t$, which is extremely small for an oscillator with a capability of switching the tank current direction. This makes it suitable for a direct connection to solar cells. Note that the oscillation swing cannot go further than $V_{OD1,2}$ at DA/DB nodes, which is chosen ~150 mV to satisfy the system's phase noise requirement by a few dB margin. However, the maximum required voltage of the circuit is determined by the bias voltage V_B.

$$V_B \approx V_{OD1} + V_{gs3}. \tag{7.9}$$

Eq. (7.9) implies that $M_{3,4}$ should work in weak-inversion keeping $V_{gs3}<V_t$ to achieve lower $V_{DD,min}$. However, the transistor's cut-off frequency f_{max} drops dramatically in the subthreshold

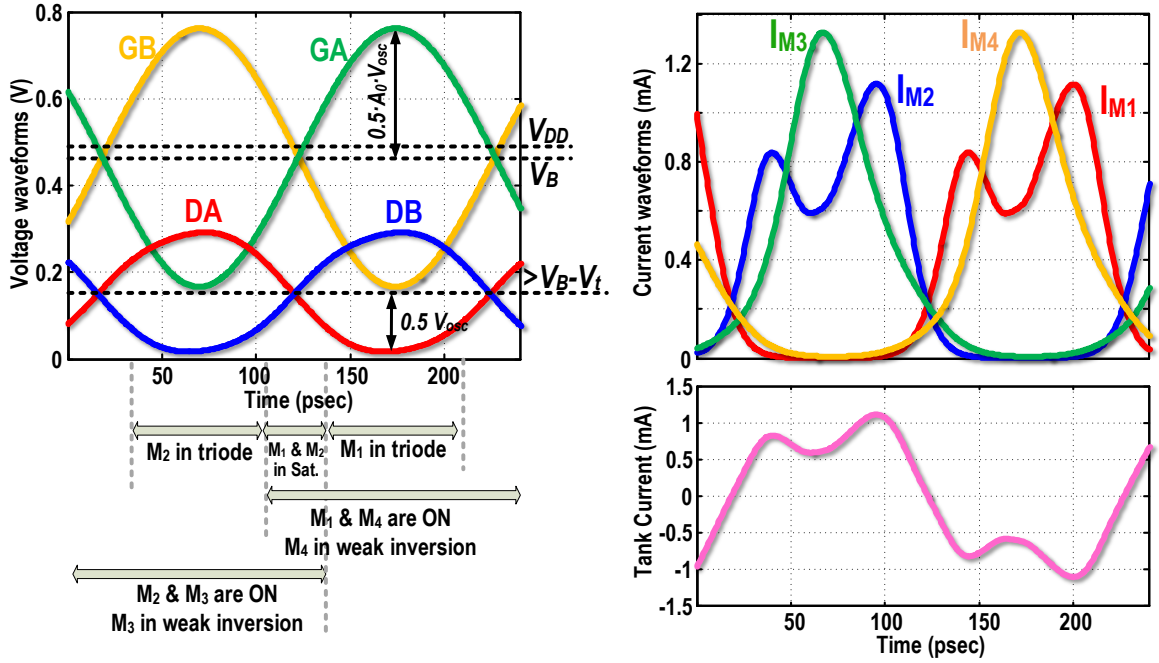


Figure 7.9: Waveforms and various operational regions of M_{1-4} transistors across the oscillation period.

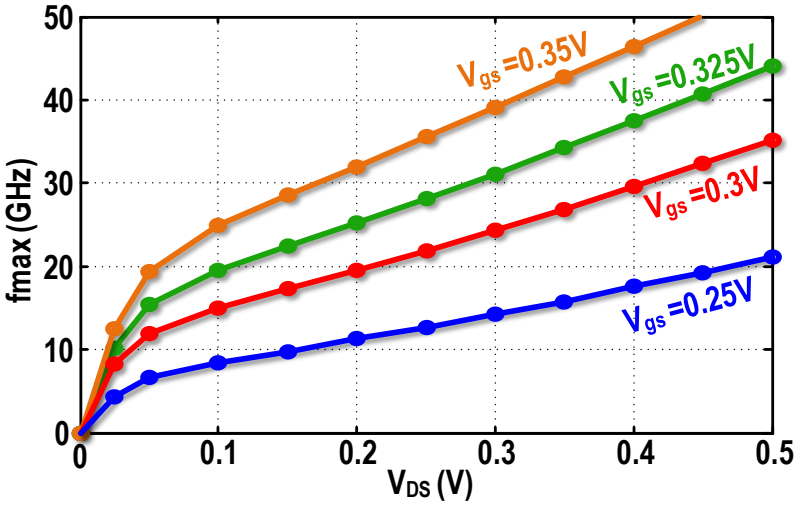


Figure 7.10: f_{max} of low-V_t 28 nm transistor versus V_{DS} for different V_{GS}.

operation. Note that f_{max} should be at least 4× higher than the operating frequency $f_0 = 4.8$ GHz to guarantee the oscillator start-up over PVT variations. This constraint limits $V_{gs3} \approx 0.32$ V for $V_{OD3} \approx 150$ mV, as can be gathered from Fig. 7.10. Consequently, even by considering only the tougher V_B requirement, the proposed structure can operate at V_{DD} as low as 0.5 V, on par with OSC_N.

Such a low V_{DD} and oscillation swing can easily lead to start-up problems in the traditional structures. It will certainly increase power consumption, P_{buf}, of the following buffer, which would require more gain in order to provide a rail-to-rail swing at its output that is interpreted as a local oscillator (LO) clock. Fortunately, the transformer gain enhances the oscillation swing at $M_{1,2}$ gates to even beyond V_{DD}, guaranteeing the oscillator start-up and reduction of P_{buf}. Consequently, the oscillator buffer is connected to the secondary winding of the transformer in

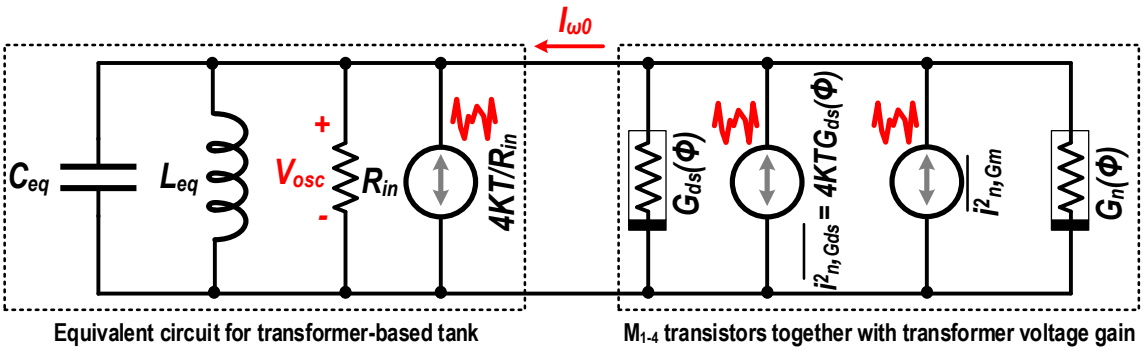


Figure 7.11: Generic noise circuit model of the proposed oscillator.

this design.

As can be gathered from Fig. 7.9, the $M_{3,4}$ switching current source transistors operate in a class-C manner as in a Colpitts oscillator, meaning that they deliver more or less narrow-and-tall current pulses. However, their non-zero conduction angle is quite wide, $\sim\pi$, due to the low overdrive voltage in the subthreshold operation. On the other hand, $M_{1,2}$ operate in a class-B manner like cross-coupled oscillators, meaning that they deliver square-shape current pulses. Hence, the shapes of drain currents are quite different for the lower and upper pairs. However, their fundamental components demonstrate the same amplitude ($\alpha_I \approx 2/\pi$) and phase to realize the constructive oscillation voltage across the tank. The higher drain harmonics obviously show different characteristics. However, they are filtered out by the tank's selectivity characteristic. Note that the current through a transistor of the upper pair will have two paths to ground: through the corresponding transistor of the lower pair and through the single-ended capacitors. Consequently, the single-ended capacitors sink the higher current harmonics of $M_{3,4}$ transistors.

7.2.3 Thermal Noise Upconversion in The Proposed Oscillator

To calculate a closed-form PN equation, the proposed oscillator model is simplified in Fig.7.11. At the resonant frequency, the transformer-based tank can be modeled by an equivalent LC-tank of elements L_{eq}, C_{eq} and R_{in}[1]. On the other hand, M_{1-4} transistors together with the passive voltage gain of the transformer are decomposed into two nonlinear time-variant conductances. The first one is always negative to compensate for the circuit losses[2]: $G_n(\phi) = G_{nd}(\phi) + G_{nu}(\phi) = \frac{-1}{4}\left[A_0\left(g_{m1}(\phi) + g_{m2}(\phi)\right) + (A_0 - 1)\cdot\left(g_{m3}(\phi) + g_{m4}(\phi)\right)\right]$. The second one is always positive, $G_{ds}(\phi) = \frac{1}{4}\sum g_{ds,1:4}(\phi)$, modeling the equivalent channel conductance of M_{1-4} devices. The noise sources of M_{1-4} are uncorrelated and always find a path through the tank and via C_{par} to ground. To get a better insight, the equivalent noise due to channel conductance, $\overline{i^2_{n,Gds}(\phi)} = 4KTG_{ds}(\phi)$, and due to transconductance gain, $\overline{i^2_{n,Gm}(\phi)} = KT(\gamma_1\left(g_{m1}(\phi) + g_{m2}(\phi)\right) + \gamma_4\left(g_{m3}(\phi) + g_{m4}(\phi)\right))$, of M_{1-4} are modeled separately here.

It is well known that the relevant impulse sensitivity function of noise sources associated with a sinusoidal waveform oscillator, $V_{osc}\cdot\cos\phi$, may be estimated by $\Gamma = \sin(\phi)$ [31] [25]. By

[1]The interested reader is directed to [170] for accurate closed-form equations of L_{eq}, C_{eq} and R_{in}.
[2]Calculated following the method in [43].

exploiting (7.4), the effective noise factor due to resistive losses of the oscillator becomes

$$F_{loss} = \frac{R_{in}}{2KT} \cdot \frac{1}{2\pi} \int_0^{2\pi} 4KT \left(\frac{1}{R_{in}} + G_{ds}(\phi) \right) \cdot \sin^2(\phi) \cdot d\phi = \\ \frac{1}{2\pi} \int_0^{2\pi} 2\sin^2(\phi) d\phi + R_{in} \left(\frac{1}{2\pi} \int_0^{2\pi} G_{ds}(\phi) \cdot d\phi - \frac{1}{2\pi} \int_0^{2\pi} G_{ds}(\phi) \cdot \cos(2\phi) \cdot d\phi \right) \rightarrow \\ F_{loss} = 1 + R_{in} \left(G_{DS}[0] - G_{DS}[2] \right) = 1 + R_{in} G_{DSEF} = 1 + \frac{R_{in}}{2} \left(G_{DS1EF} + G_{DS4EF} \right). \tag{7.10}$$

where, $G_{DS}[k]$ describes the k_{th} Fourier coefficient of the instantaneous $G_{ds}(\phi)$. To get better insight, different components of above equation are graphically illustrated in Fig. 7.12 (a)-(c). The literature interprets $R_{in}G_{DSEF}$ term in (7.10) as the tank loading effect[1]. In our design, M_1 and M_2 alternatively enter the triode region for part of the oscillation period and exhibit a large channel conductance. As shown in Fig. 7.12 (a), simulated $0.5R_{in}G_{DS1EF}$ can be as large as 0.6 for the lower pair transistors. However, $M_{3,4}$ work only in saturation and demonstrate small channel conductance for their entire on-state operation, as evident from Fig. 7.12 (a). Hence, the simulated value of $0.5R_{in}G_{DS4EF}$ is as low as 0.15 for upper pair transistors. Note that both NMOS and PMOS pairs of the OSC_{NP} structure simultaneously enter the triode region for part of the oscillation period and load the tank from both sides. In the proposed structure, however, only one side of the tank is connected to the AC ground when either M_1/M_2 is in triode while the other side sees high impedance. Hence, this structure at least preserves the charge of differential capacitors over the entire oscillation period. Consequently, compared to the traditional oscillators, the tank loading effect is somewhat reduced here.

To sustain the oscillation, the average power dissipated in the oscillator's resistive loss, $R_{in} + 1/G_{ds}(\phi)$, must equal the average power delivered by the negative resistance, $G_n(\phi)$, of the active devices. As proved in [43], this energy conservation requirement results in

$$G_{NEF} = G_{NDEF} + G_{NUEF} = -\left(\frac{1}{R_{in}} + G_{DSEF} \right) \rightarrow \\ \frac{A_0}{4} \left(G_{M1EF} + G_{M2EF} \right) + \frac{(A_0 - 1)}{4} \cdot \left(G_{M3EF} + G_{M4EF} \right) = \frac{1 + R_{in}G_{DSEF}}{R_{in}}. \tag{7.11}$$

As with OSC_{NP} [45] [43], both upper and lower feedback mechanisms should exhibit almost identical, i.e., ∼50%, contribution to the compensation of oscillator losses. Consequently,

$$G_{M1EF} + G_{M2EF} = \frac{2}{A_0} \cdot \frac{1 + R_{in}G_{DSEF}}{R_{in}}, \quad and, \quad G_{M3EF} + G_{M4EF} = \frac{2}{A_0 - 1} \cdot \frac{1 + R_{in}G_{DSEF}}{R_{in}} \tag{7.12}$$

By exploiting (7.4), the effective noise factor due to transconductance gain is calculated as

$$F_{active} = \frac{1}{2\pi} \int_0^{2\pi} \overline{i_{Gm}^2(\phi)} \cdot \sin^2(\phi) \cdot \frac{R_{in}}{2KT} \cdot d\phi = \\ R_{in} \left(\frac{1}{2\pi} \int_0^{2\pi} \frac{1}{4} \sum_{i=1}^{4} \gamma_i g_{m,i}(\phi) d\phi - \frac{1}{2\pi} \int_0^{2\pi} \frac{1}{4} \sum_{i=1}^{4} \gamma_i g_{m,i}(\phi) \cdot \cos(2\phi) d\phi \right) \rightarrow \\ F_{active} = \frac{R_{in}}{4} \left[\gamma_1 \left(G_{M1EF} + G_{M2EF} \right) + \gamma_4 \left(G_{M3EF} + G_{M4EF} \right) \right] \tag{7.13}$$

[1]The interested reader is directed to Appendix A for accurate closed-form equations of G_{DS1EF} and G_{DS4EF}.

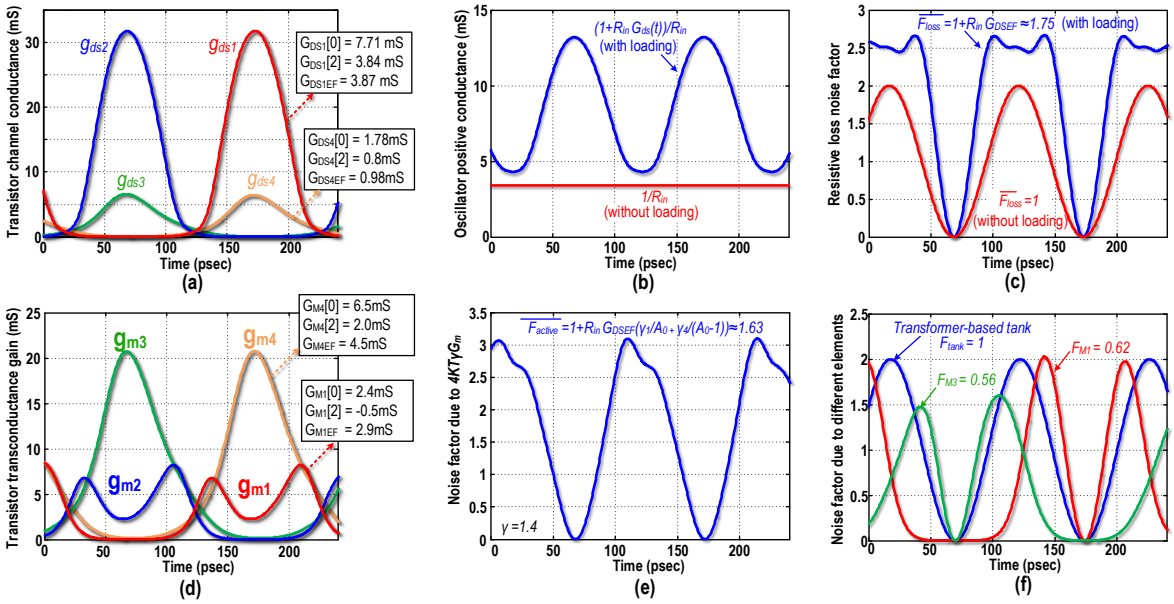


Figure 7.12: Circuit-to-phase noise conversion across the oscillation period in the switching current-source oscillator. Simulated (a) Channel conductance of M_{1-4}; (b) Conductance due to resistive losses; (c) Noise factor due to losses; (d) Transconductance of M_{1-4}; (e) Effective noise factor due to transconductance gain; (f) Effective noise factors due to different oscillator's components.

To get better insight, different components of above equation are graphically illustrated in Fig. 7.12 (d)–(e). By merging (7.12) into (7.13), we have

$$F_{active} = (1 + R_{in}G_{DSEF}) \cdot \left(\frac{\gamma_1}{2A_0} + \frac{\gamma_4}{2(A_0 - 1)}\right) \tag{7.14}$$

As discussed in conjunction with Fig. 7.6 (c), the transformer's passive voltage gain, A_0, covers a significant part of the required loop gain of the lower positive feedback. Hence, the lower-pair transistors have to compensate only $1/(2A_0)$ of the circuit losses. For the upper positive feedback however, A_0 covers a smaller part of the required loop gain. Consequently, the upper transistors should work harder and compensate $1/(2(A_0 - 1))$ of the oscillator loss. Consequently, as (7.14) indicates, the G_M noise contribution by the lower pair is smaller. However, its effect on F_{loss} is larger such that both pairs demonstrate more or less the same contribution to the oscillator PN (see Fig. 7.12 (f)). Finally, the total oscillator effective noise factor is given by

$$F = F_{loss} + F_{active} = (1 + R_{in}G_{DSEF}) \cdot \left(1 + \frac{\gamma_1}{2A_0} + \frac{\gamma_4}{2(A_0 - 1)}\right) \tag{7.15}$$

By considering $\gamma_1 = \gamma_4$ =1.4 and A_0=2.15, the noise factor of the proposed oscillator is ∼5.3 dB, which is just 1.5 dB higher than the ideal value of (1+γ) despite the aforementioned practical issues of designing ulta-low voltage and power oscillators. The phase noise and FoM of the proposed oscillator can be calculated by replacing (7.15) in (7.2).

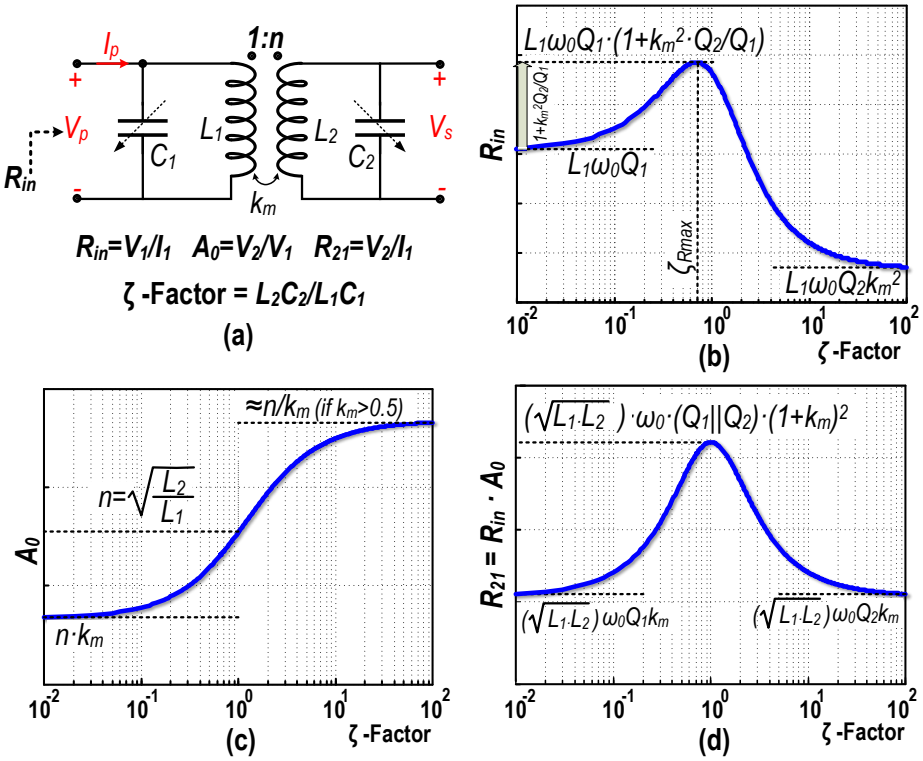


Figure 7.13: Transformer-based tank: (a) schematic; (b) input parallel resistance; (c) voltage gain; and (d) R_{21} versus ζ-factor.

7.2.4 1/f Noise Upconversion in The Proposed Oscillator

Several techniques have been exploited to improve the oscillator's 1/f noise upconversion. First, dynamically switching the bias-setting devices $M_{1,2}$ will reduce their flicker noise, as also demonstrated in [171]. It also lowers a DC component of their effective impulse sensitivity function. Second, as discussed in [100], a second-order harmonic of the gm-devices' drain current flows into the capacitive part of the tank due to its lower impedance and creates asymmetric rise and fall times for the oscillation waveform. It directly increases a DC value of the oscillator ISF and thus its $1/f^3$ PN corner. As suggested in [100] and [172], this phenomenon can be alleviated by realizing an auxiliary resonance at $2\omega_0$ such that the second harmonic current flows into equivalent resistance of the tank in order to avoid disturbing the rise and fall time symmetry of the oscillation voltage. Since common-mode signals, such as a second harmonic of the drain current, cannot see the tuning capacitance at the transformer secondary winding [88], the auxiliary $2\omega_0$ can be realized without die area penalty and by adjusting the single-ended capacitance at the transformer primary winding [100].

The last source of the 1/f noise is M_{B1} in the biasing circuitry. By exploiting long channel device for biasing, its power consumption becomes negligible compared to the oscillator core while $M_{B1/B2}$ occupy larger area and thus generate lower 1/f noise. Consequently, based on aforementioned techniques, a lower $1/f^3$ PN corner is expected than in the traditional oscillators.

7.2.5 Optimizing Transformer-based Tank

The transformer-based tank's input equivalent resistance, R_{in}, and voltage gain, A_0, should be maximized for the best system efficiency. Both optimization parameters are a strong function

of ζ=L_2C_2/L_1C_1 [170], as shown in Fig. 7.13. R_{in} may be estimated by

$$R_{in} = L_1\omega_0 Q_1 \cdot \frac{(1-(\frac{\omega_0}{\omega_s})^2(1-k_m^2))\zeta}{-(\frac{\omega_0}{\omega_s})^4(1+\frac{Q_1}{Q_2})+(\frac{\omega_0}{\omega_s})^2(1+\frac{Q_1}{Q_2}\zeta)} \tag{7.16}$$

where, $\omega_s^2 = 1/L_2C_2$, and Q_1 and Q_2 are respectively the Q-factors of the transformer's primary and secondary windings. It can be shown that R_{in} reaches its maximum when

$$\zeta_{Rmax} = \frac{Q_2}{Q_1} \cdot \left(\frac{Q_2}{Q_1+Q_2} \cdot k_m^2 + \frac{Q_1}{Q_1+Q_2}\right). \tag{7.17}$$

Note that the tank Q-factor is maximized at different $\zeta = Q_2/Q_1$ [21]. The maximum R_{in} is obtained by inserting (7.17) into (7.16)

$$R_{inmax} = L_1\omega_0 Q_1 \cdot \left(1 + k_m^2 \cdot \frac{Q_2}{Q_1}\right). \tag{7.18}$$

Consequently, the transformer's coupling factor k_m enhances R_{in} by a factor of $\sim(1+k_m^2)$ at ζ_{Rmax}. For this reason, the switched-capacitor banks are distributed between the transformer's primary and secondary to roughly satisfy (7.17). For $k_m \geq 0.5$, the voltage gain of the transformer-based tank may be estimated by

$$A_0 = \frac{2k_m n}{1-\zeta+\sqrt{1+\zeta^2+\zeta(4k_m^2-2)}}. \tag{7.19}$$

As shown in Fig. 7.13 (c), A_0 increases with larger ζ. Note that larger R_{in} and A_0 are desired to reduce P_{DC} and P_{buf}, respectively. To consider both scenarios, trans-impedance R_{21}=$R_{in}\cdot A_0$ term is defined and depicted in Fig. 7.13 (d). R_{21} reaches its maximum at ζ=1 for $Q_1 \approx Q_2$, which is reasonable for monolithic transformers. We also define the maximum of R_{21} as the transformer FoM = $(Q_1 \| Q_2)\cdot(1+k_m)^2\cdot\sqrt{L_1L_2}\cdot\omega_0$. Consequently, the transformer dimensions and winding spacing are chosen to maximize this term.

7.3 Class-E/F$_2$ Switched-mode Power Amplifier

The second most energy-hungry block in a BLE transceiver is the PA[1]. Designing a fully integrated PA optimized for low output power ($P_{out} < 3$ dBm) with high power-added efficiency (PAE > 40%) is very challenging, especially when the level of all harmonics must be suppressed to below -41 dBm to fulfill the FCC 15.247 regulation. To deliver such a low P_{out} with the highest PAE to the $R_L = 50\,\Omega$ load, the equivalent resistance r_L seen by PA switching transistors must be *scaled up* by the PA's output matching network.

A single-ended class-D PA generates the lowest P_{out} among various flavors of switched-mode PAs when compared at the same supply voltage V_{DDPA} and r_L. Hence, the impedance transformation ratio, ITR=r_L/R_L, and therefore insertion loss of its matching network, can be theoretically the lowest, making the class-D PA an attractive choice for efficient and fully integrated BLE transmitters, as can be also gathered from literature [8]– [10]. However, the

[1]PA is the most power-hungry block in a BLE radio, but it is the second in energy consumption due to its shorter operational cycles – see Fig. 7.3.

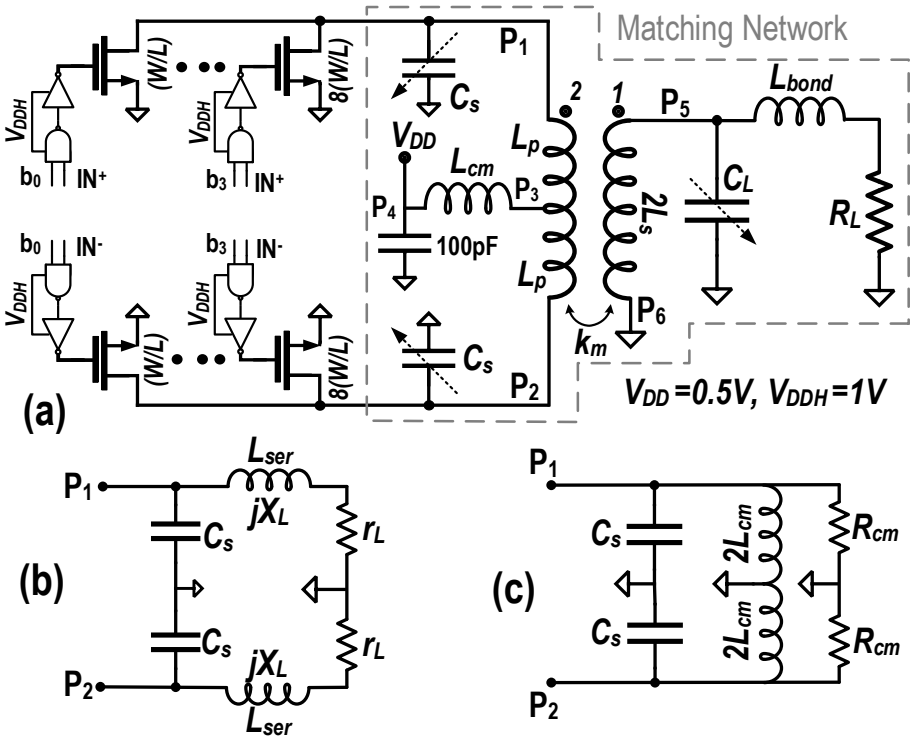


Figure 7.14: (a) Schematic of the proposed class-E/F_2 PA. Equivalent circuit PA's matching network for (b) differential, and (c) common-mode excitations.

second-harmonic emission of single-ended class-D PAs is quite poor and thus an additional feedback structure is needed to adjust the PA's conduction angle to $\sim\pi$ in order to suppress all even-order harmonics [8]– [10]. However, that circuitry worsens the system power consumption, die area and complexity. Furthermore, a loaded Q-factor of a class-D series LC matching network $Q_L = L_s\omega_0/R_L$ is quite low ($\sim$1 for L_s as large as 3.5 nH). Hence, its filtering function would not be even close enough to suppress the 3rd harmonic to $\leq$ -41 dBm. As a consequence, an additional on-chip [9], [10] or off-chip [8] low-pass filter is required. This approach dramatically increases the matching network insertion loss and area such that the original benefits of single-ended class-D PAs are lost and the BLE system efficiency is limited to $\leq 20\%$ in the state-of-the-art publications [8]– [10]. It is also well-known that a discharge of parasitic capacitance of the class-D output switches further increases the PA losses. Furthermore, Q-factor of a single-ended inductor used in a class-D PA is lower than that of a differential one [173], which makes its matching network's insertion loss even worse. Finally, the last stage of class-D PA cannot operate directly at the low solar cell voltage due to stacking of NMOS and PMOS transistors.

In this work, a fully integrated differential class-E/F_2 PA (Fig. 7.14 (a)) is exploited to address the aforementioned issues. The unique characteristics of the proposed PA and its matching network will be optimized in the following subsections.

7.3.1 Efficiency and Selectivity Tradeoff in Transformer-based Matching Network

Figure 7.15 illustrates a general schematic of a transformer-based matching network of a switched-mode PA, which performs simultaneously m-series (i.e., voltage) and p-parallel (i.e., current) combining [174] [175]. As proven in Appendix B, the matching network efficiency η_p

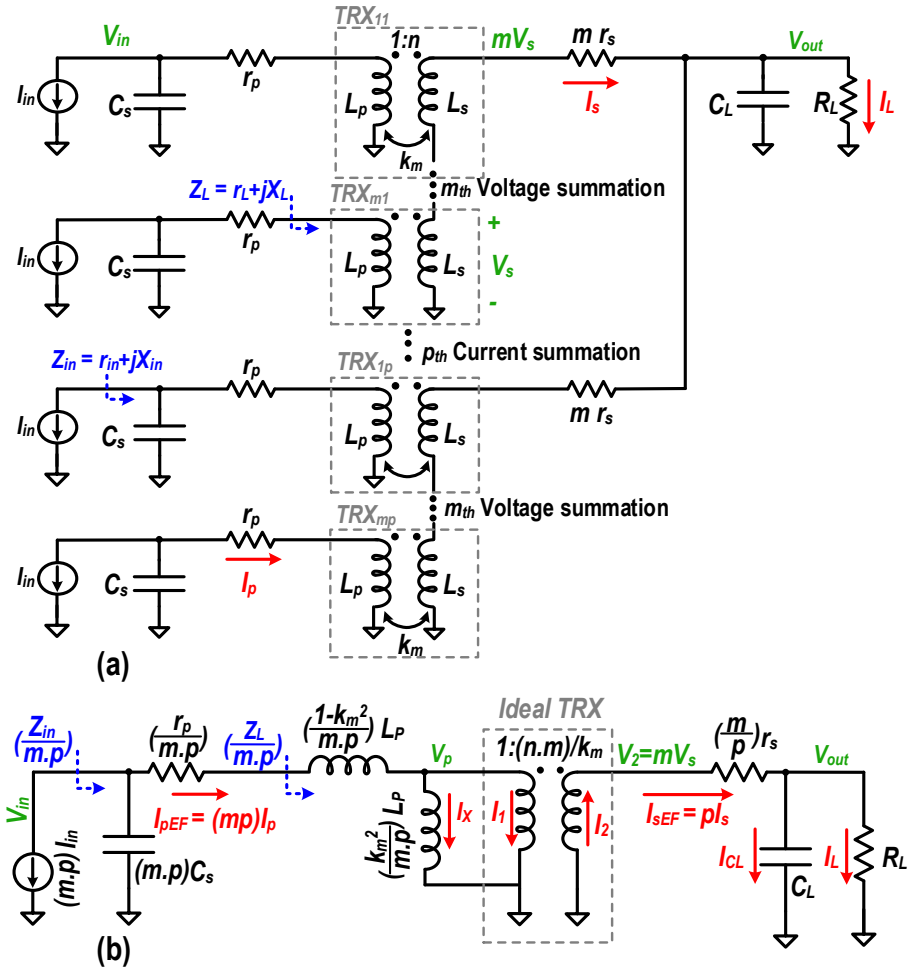


Figure 7.15: (a) Transformer-based matching network with m-way voltage and p-way current summation; and (b) its equivalent circuit model.

can be calculated as

$$\eta_p = \frac{R_L}{R_L + \frac{m}{p}\frac{L_s\omega_0}{Q_s} \mid 1 + jR_LC_L\omega_0 \mid^2 + \frac{m}{p}\frac{L_s\omega_0}{k_m^2 Q_p} \mid \frac{1}{Q_s} + \frac{pR_L}{mL_s\omega_0} - R_LC_L\omega_0 + j(1 + \frac{R_LC_L\omega_0}{Q_s}) \mid^2}. \tag{7.20}$$

η_p is a strong function of the effective inductance seen by the load, mL_s/p, and C_L. Hence, for the sake of simplicity, ξ is defined as $p/(mL_sC_L\omega_0^2)$. We also define $Q_L = R_LC_L\omega_0$ as the loaded Q-factor of the secondary side of the matching network. The η_p reaches its local maximum when

$$\frac{\partial \eta_p}{\partial C_L} = 0 \rightarrow \xi_{opt} = \frac{p}{mL_{s(opt)}C_L\omega_0^2} = 1 + \frac{1}{Q_s^2} + k_m^2\left(\frac{Q_p}{Q_s}\right) \tag{7.21}$$

By exploiting the Q_L definition above and replacing $L_{s(opt)}$ from (7.21) into L_s in (7.20), and carrying out lengthy algebra, the local maximum of η_p may be estimated by

$$\eta_{p(opt)} = \frac{1}{1 + \frac{1+Q_L^2}{\xi_{opt}Q_sQ_L} + \frac{1}{\xi_{opt}k_m^2Q_pQ_L} \cdot \left(\left(\frac{1}{Q_s} + Q_L\left(\xi_{opt} - 1\right)\right)^2 + \left(1 + \frac{Q_L}{Q_s}\right)^2\right)}. \tag{7.22}$$

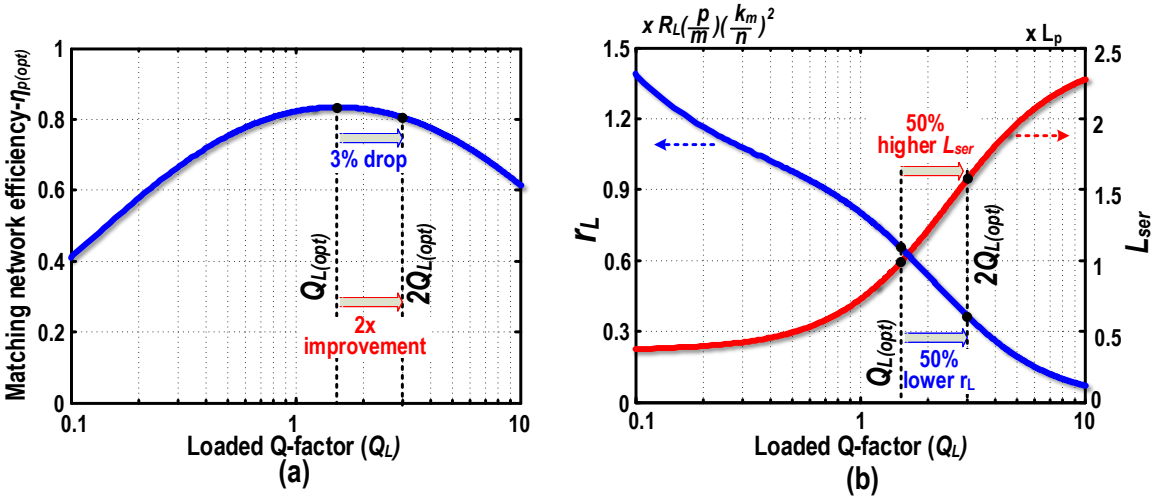


Figure 7.16: (a) Maximum possible efficiency, $\eta_{p,(opt)}$, and estimated effective Q-factor, Q_{MN}; and (b) real and imaginary parts of the equivalent impedance, Z_L, seen at the transformer's primary winding versus C_L. Conditions: Q_p=11, Q_s=17, k_m=0.8, n=0.5 and f_0=2.45 GHz.

Figure 7.16 (a) shows the maximum possible passive efficiency $\eta_{p(opt)}$ versus Q_L. As can be seen, there exists a global optimum Q_L that maximizes the transformer-based matching network efficiency at a given frequency. The η_p reaches its global maximum when

$$\frac{\partial \eta_{p(opt)}}{\partial Q_L} = 0 \rightarrow Q_{L(opt)} = \sqrt{\frac{Q_s^2}{1 + k_m^2 Q_p Q_s}} \xrightarrow{k_m^2 Q_p Q_s \gg 1} Q_{L(opt)} \approx \frac{1}{k_m}\sqrt{\frac{Q_s}{Q_p}}. \tag{7.23}$$

As a result, the global optimum load capacitance, $C_{L(opt)}$, may be estimated by $\frac{1}{k_m R_L \omega_0}\sqrt{\frac{Q_s}{Q_p}}$. Note that both (7.21) and (7.23) are more general and accurate than in [174]. Using the optimum ξ and Q_L, the maximum η_p will be given by

$$\eta_{p(max)} = \frac{1}{1 + \frac{2}{k_m^2 Q_p Q_s}\left(1 + \sqrt{1 + k_m^2 Q_p Q_s}\right)}, \tag{7.24}$$

which is the same result as in [174]. As can be realized form Fig. 7.16 (a), there is a strong tradeoff between the frequency selectivity and efficiency of the transformer-based matching network for $Q_L \geq Q_{L(opt)}$. Fortunately, the $\partial\eta_p/\partial Q_L$ slope is small around $Q_L = Q_{L(opt)}$. Combined with the fact that the effective Q-factor of the matching network improves almost linearly with Q_L, it is therefore desired to use $Q_L = 2Q_{L(opt)}$ ($C_L = 2C_{L(opt)}$) to double the frequency selectivity of the matching network for the price of a negligible, i.e., $\leq 5\%$, efficiency drop.

7.3.2 Impedance Transformation

The matching network should also realize the required load resistance, r_L, and series inductance, L_{ser} for proper zero-voltage and zero-slope switching (ZVS and ZdVS) operation of the class-E/F PA. As shown in Appendix B, r_L may be estimated by

$$r_L \approx R_L \cdot \frac{p}{m}\left(\frac{k_m}{n}\right)^2 \cdot \frac{Q_s + Q_L/\xi}{2\xi Q_L + Q_s + Q_L^2 Q_s(\xi - 1)^2} \tag{7.25}$$

To deliver a relatively low output power $P_{out} \leq 3\,\text{dBm}$ to the antenna, realizing a larger r_L is desired. Unfortunately, as can be gathered from (7.25), the voltage summation and imperfect magnetic coupling factor k_m of the matching network's transformer exhibit reverse effect of reducing r_L. The p-way current combining enhances r_L but at the price of $(p-1)$ extra transformers and thus a dramatic increase in the PA die area [175] [136]. Hence, the parallel combining is not considered in this work. Eq. (7.25) further indicates that a step-down transformer (n:1) with a large turns ratio ($n > 1$) could be used to enhance r_L. However, Q-factor of transformer windings, and thus its efficiency, drops dramatically as n grows. Consequently, the turns ratio of 2 was chosen in consideration of both the r_L enhancement and η_p optimization scenarios. P_{out} is further reduced by using V_{DD}=0.5 V (i.e., half the regular supply level) for the drains of switching transistors with the side effect of ∼6 dB lower power gain for PA's transistors. However, the power gain of 28 nm NMOS devices is high enough at a relatively low frequency of 2.4 GHz such that the 6 dB power gain penalty has a negligible effect on the total system efficiency. Furthermore, the drain voltage peak of the switching transistors is now ≤1.5 V, thus alleviating reliability issues due to a gate-oxide breakdown [88] [39].

As shown in Appendix B, the equivalent series inductance, L_{ser}, seen from the transformer's primary is

$$L_{ser} = L_p \left[(1 - k_m^2) + k_m^2 \cdot \frac{2\xi Q_L + Q_L^2 Q_s \xi(\xi - 1)}{2\xi Q_L + Q_s + Q_L^2 Q_s (\xi - 1)^2} \right]. \tag{7.26}$$

Note that switched-mode PAs typically need a large L_{ser} to satisfy the ZVS/ZdVS criteria, which leads to a big inductor with a reduced Q-factor. As can be gathered from (7.26) and Fig. 7.16 (b), L_{ser} increases with a larger C_L and thus Q_L for $\xi \geq 1$, which coincides with efforts to optimize η_p (see (7.21)). More interestingly, L_{ser} can even be larger than the transformer's primary inductance, L_p, for $C_L \geq C_{L(opt)}$, which helps to reduce both matching network dimensions and insertion loss. Unfortunately, r_L reduces with C_L and thus the highest PA efficiency occurs at higher output power levels. Consequently, it is again desired to choose $C_L \approx 2C_{L(opt)}$ by considering the tradeoff between r_L and L_{ser} enhancement factors.

7.3.3 Class-E/F$_2$ Operation

Figure 7.14 (b) illustrates an equivalent circuit of the PA matching network in the differential mode at the fundamental frequency ω_0. At all higher odd harmonics, L_{ser} presents high impedance and thus the only load seen by the switch is its parallel capacitance, C_s. Hence, for odd harmonics the load impedance behaves similarly as in the traditional class-E PA.

As illustrated in Fig. 7.17, the step-down 2:1 transformer acts differently to the common-mode (CM) and differential-mode (DM) input signals. When the transformer's primary is excited by a CM signal [Fig. 7.17(b)], the magnetic flux excited within two turns of the primary winding cancels itself out [93]. Consequently, the transformer's primary inductance is negligible and no current is induced at the transformer's secondary ($k_{m-CM} \approx 0$). Hence, R_L, L_s and C_L cannot be seen by even harmonics of drain current.

Furthermore, the CM inductance, $2L_{cm}$, seen by the switching transistors is mainly determined by the dimension of the trace between the transformer's center-tap and decoupling capacitors at the V_{DD} node. Together with C_s, $2L_{cm}$ realizes a CM resonance, ω_{cm}. Note that P_{out} of the class-E PA can be reduced by ∼2 dB at the same r_L and V_{DD} by means of an addi-

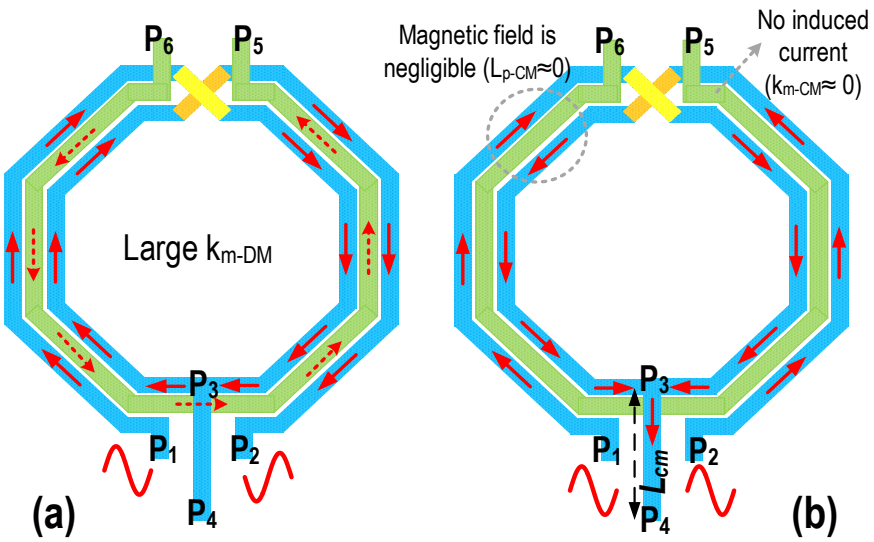


Figure 7.17: Behavior of a 2:1 step-down transformer in: (a) differential-mode, and (b) common-mode excitations.

Table 7.3: Design sets for different flavors of class-E/F PA.

Tuning	K_C	K_L	K_P
E	0.184	1.152	0.577
E/F$_2$	0.337	1.609	0.381
E/F$_3$	0.209	0.961	0.657
E/F$_{2,3}$	0.323	0.832	0.747
E/F$_4$	0.218	1.173	0.533
E/F$_{2,4}$	0.361	1.667	0.350

tional open circuit acting as the switches' effective load at $\sim 2\omega_0$ (i.e., class-E/F$_2$ operation [109]), as can be gathered from the power factor, K_p, column in Table 7.3. Consequently, this PA needs smaller impedance transformation ratio for P_{out} <3dBm, which results in a lower insertion loss for its matching network and thus higher system efficiency. However, in practice, limited value of an equivalent parallel resistance of the CM resonance, R_{cm}, leads to a power loss at the second harmonic and thus a penalty on the PA's efficiency if ω_{cm} is set at precisely $2\omega_0$. Consequently, in this design, we adjust the CM resonance slightly lower (i.e., at $\sim 1.8\omega_0$) to benefit form the lower power factor of semi class-E/F$_2$ operation while avoiding the additional power loss at even harmonics.

Table 7.3 summarizes the design sets of class-E/F$_X$ PAs for satisfying the ZVS/ZdVS criteria. The design procedure starts by calculating r_L for a given V_{DD} and P_{out} by

$$r_L = m \cdot p \cdot K_P \cdot \frac{(V_{DD} - V_{Dsat})^2}{P_{out}} \cdot \eta_p. \tag{7.27}$$

where, V_{Dsat} represents the transistor's average V_{DS} in the on-state. As explained in [136], V_{Dsat} is a strong function of the switch size, technology and topology-dependent parameters, and it is set to ~ 0.12 V to maximize the PAE of the proposed PA. The shunt capacitance, C_s, and series

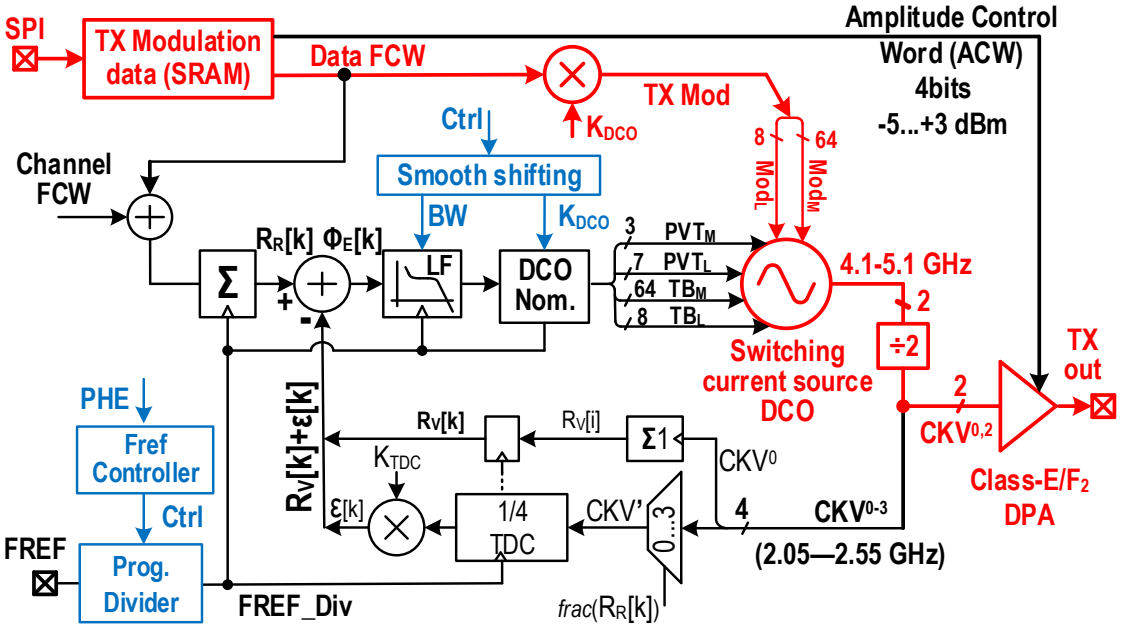


Figure 7.18: Block diagram of the 2.4 GHz ULP Bluetooth Low-Energy transmitter.

inductance, L_{ser}, may be estimated by exploiting K_c and K_L definitions:

$$C_s = \frac{K_C}{r_L \cdot \omega_0} \quad and \quad L_{ser} = \frac{K_L \cdot r_L}{\omega_0}. \tag{7.28}$$

Now, the transformer geometry should be designed to realize the required r_L and L_{ser} by (7.25)–(7.26) while optimizing the matching network efficiency via (7.21)–(7.24). In this work, the circuit variables are as follows: $r_L \approx 30\,\Omega, C_s \approx 750\,fF, L_s \approx 440\,pH, C_L \approx 3.5\,pF$.

7.4 All-Digital Phase-Locked Loop and Transmitter Architecture

Fig. 7.18 shows a block diagram of the proposed ultra-low power (ULP) all-digital PLL (ADPLL), whose architecture is adapted from a high-performance cellular 4G ADPLL disclosed in [19]. Due to the relaxed PN requirements of BLE, the DCO ΣΔ dithering [82] was removed thanks to the fine switchable capacitance of the tracking bank varactors producing a fine step size of 4 kHz. The DCO features two separate tracking banks (TB): 1) phase-error correction, and 2) direct FM modulation. Each bank is segmented with LSB (i.e., 1x ≡ 4 kHz) and MSB (i.e., 8x) unit-weights. The each TB range is $4\,\text{kHz}\times(8+8\times 64) = 2.08\,\text{MHz}$.

The DCO clock is divided by two to generate four phases of a variable carrier clock, CKV^{0-3}, in the Bluetooth frequency range of f_V = 2402–2478 MHz. Two of its phases, $\text{CKV}^{0,2}$, are fed as differential clock signals to the digital PA (DPA) in Fig. 7.14 (a). The four CKV^{0-3} phases are routed to the phase detection circuitry, which selects the phase whose rising clock edge is *expected* to be the closest to the rising clock edge of a frequency reference (FREF) clock. This prediction is based on two MSB bits of a fractional part of reference phase, $R_R[k]$, which is an accumulated frequency command word (FCW). By means of this prediction, the selected TDC

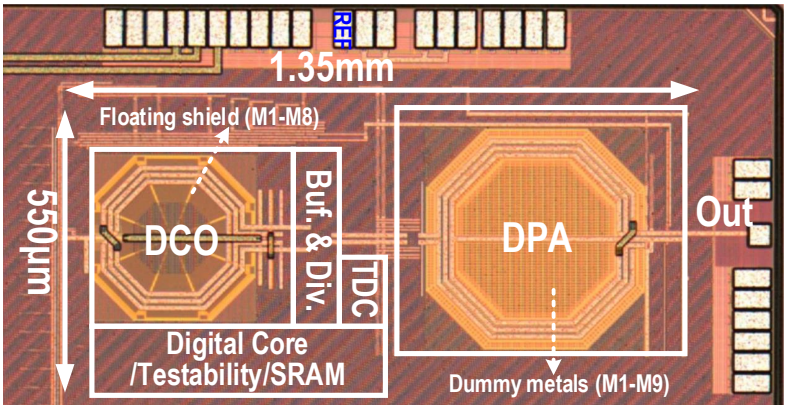


Figure 7.19: Die micrograph of the proposed ULP transmitter.

input clock CKV' spans a quarter of the original required TDC range, i.e., $T_V/4$, where T_V is the CKV clock period. This way, the long string of 417 ps/12 ps >35 TDC inverters is shortened by 4x, improving linearity and power consumption by the same amount.

The TDC output, after decoding, is normalized to T_V by the Δ_{TDC}/T_V multiplier and the quadrant estimation, normalized to $T_V/4$, is added to produce the phase error ϕ_E. The DCO tuning word is updated based on ϕ_E. The $\phi_E[k]$ is fed to the type-II loop filter (LF) with 4th-order IIR. The LF is dynamically switched during frequency acquisition to minimize the settling time while keeping the phase noise (PN) at optimum. The built-in DCO gain, K_{DCO}, and TDC gain, K_{TDC}, calibrations are autonomously performed to ensure the wideband FM response.

The following architectural innovations allow the ADPLL to support ULP operation (highlighted in blue): The effective sampling rate of the phase detector and its related DCO update is dynamically controlled by scaling-down the FREF clock and simultaneously adjusting the LF coefficients in order to keep the same bandwidth and LF transfer-function characteristics. During the ADPLL settling, the full FREF rate is used, but afterwards its rate could get substantially reduced (e.g., 8x), or completely shut down, thus saving power consumption of the digital circuitry. The resulting in-band PN degradation is tolerable due to low PN of the DCO. In fact, freezing FREF would incur sufficiently low frequency drift during the BLE 376μs packets, while keeping in operation the bare minimum of circuitry highlighted in red.

7.5 Experimental Results

Figure 7.19 shows the die photo of the 0.75 mm^2 ULP TX in TSMC 1P9M 28 nm CMOS. Both DCO and PA transformers' windings are realized with top ultra-thick metal[1]. However, they include a lot of dummy metal pieces on *all* metal layers (M1–M9) to satisfy very strict minimum metal density manufacturing rule of advanced ($\leq$28 nm) technology nodes. Note that the dummy metals must be significantly thinner than the skin depth at the given frequency to avoid any attenuation of the magnetic field. The skin depth of copper is ~0.9 μm at 4.8 GHz, which is much larger than the thickness of lower level metals (M1–M7). Hence, adding small

[1]Implementation of this transmitter has been a joint project with the RF group of TSMC. All measurements have been done by TSMC.

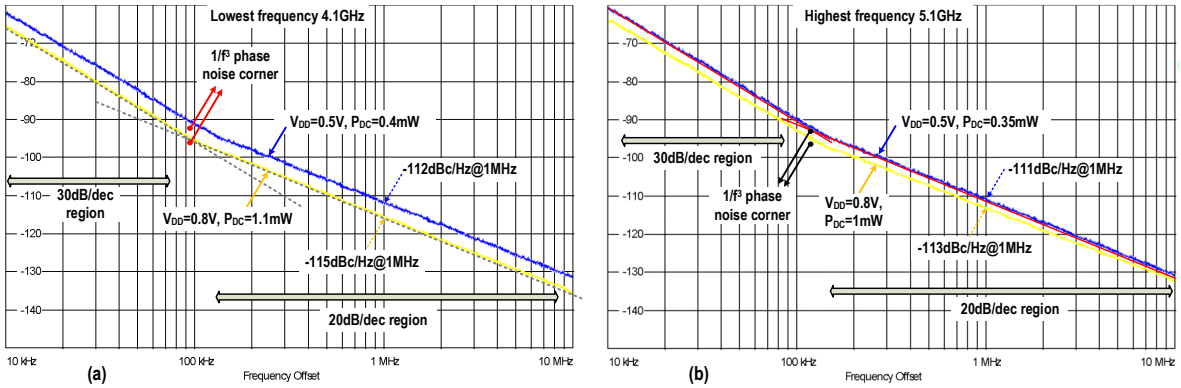


Figure 7.20: Measured phase noise of the proposed oscillator at (a) lowest and (b) highest frequency.

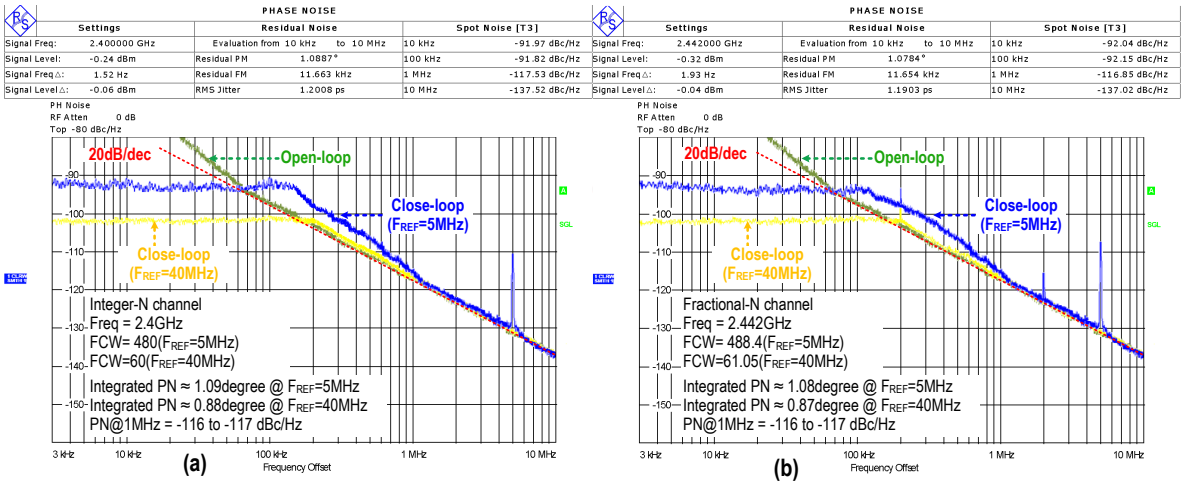


Figure 7.21: Measured transmitter phase noise in open-loop and different close-loop configurations for (a) integer-N and (b) fractional-N channels.

metal pieces (i.e, $3\,\mu$m $\times$ $3\,\mu$m) on these layers should not cause any major issues on the performance of inductive elements. However, the thickness of top metal layers (M8 & M9) is comparable with the copper skin depth at $f_0 \geq 1$ GHz. Hence, adding M8 and M9 dummy metals reduces the transformers' magnetic field and thus their Q-factor by ~10%. This leads to a negligible reduction of PA's matching network efficiency (i.e, $\leq$ 3%), 10% increase in the DCO's power consumption and ~1 dB degradation of its FoM.

Figure 7.20 displays the phase noise of the proposed oscillator at the lowest and highest tuning frequencies for V_{DD} = 0.5 V and 0.8 V, while $R_{in} \approx 310\,\Omega$. The measured PN is -111 dBc/Hz at 1 MHz offset from 5.1 GHz carrier while consuming ~0.35 mW at 0.5 V. As justified in Section 7.2.4, the 1/f^3 PN corner of the oscillator is extremely low (i.e., $\leq$100 kHz) across the tuning range (TR) of 22% (i.e., from 4.1 to 5.1 GHz). Its average FoM is 189 dBc and varies $\pm$1 dB across the TR. For the supply frequency pushing measurements, the oscillator's V_{DD} supply is swept within 0.4–0.6 V while the off-chip bias resistor R_{Bias} (see Fig. 7.8) is removed and V_B is directly connected to an external reference voltage[1]. Contrary to the OSC$_{\text{NP}}$

[1]Since V_B biasing does not consume any DC current, the current consumption of its internal biasing circuit is extremely low (<20μA); therefore, realizing an on-chip V_B voltage reference with a good PSRR would be quite straightforward.

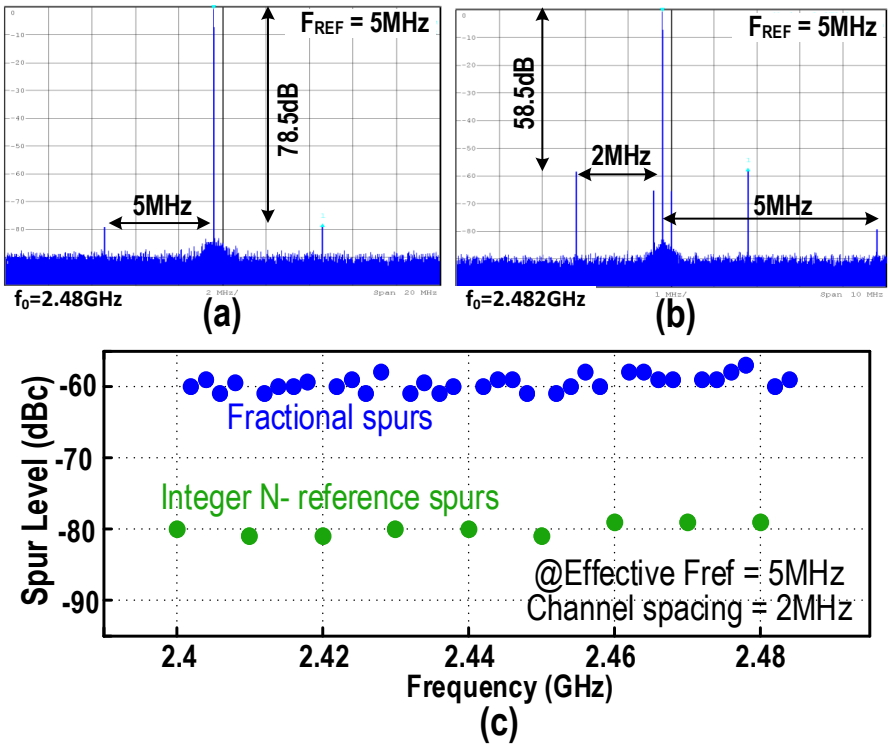


Figure 7.22: Measured ADPLL spectrum for (a) integer-N and (b) fractional-N channels; (c) ADPLL fractional, reference and open-loop spurs versus BLE channels.

structure, V_{DD} perturbations here cannot directly modulate V_{gs} and thus the oscillator's DC current and nonlinear C_{gs} of M_{1-4} devices. Consequently, the worst-case supply frequency pushing is very low, 10–12 MHz/V across TR, thus making the oscillator suitable for direct connection to solar cells and integration with a PA.

Figure 7.21 shows the phase noise plot of the proposed transmitter at different configurations for both integer-N and fractional-N BLE channels. When used as LO at *undivided* 40 MHz FREF, the ADPLL consumes 1.4 mW with integrated PN of 0.87° (yellow line in Fig. 7.21). It exhibits in-band PN of -101 dBc/Hz, which corresponds to an average time resolution of ∼12 ps for TDC. Thanks to the low wander of the DCO, digital power consumption of the rest of ADPLL can be saved by scaling the rate of sampling clock to 5 MHz. However, the in-band PN increases by $10\log_{10}(40/5) = 9$ dB to -92 dBc/Hz with integrated PN of ∼1.08° (blue line in Fig. 7.21).

Figure 7.22 shows a representative spectrum of the ADPLL at integer-N and fractional-N channels and summarizes the worst case spur for each BLE channel. The reference spur is ∼-80 dBc and the worst-case fractional spur is ∼-60 dBc. The open-loop spurs are lower than -90dBc and well below the noise floor of our measurement equipment.

Figure 7.23 shows the spectrum of the transmitter for 1Mb/s GFSK modulation at different modulation indexes and its burst modulation quality. The transmitter fulfills all spectrum mask requirements, while its FSK error is 2.6%.

To achieve simultaneous fast locking and power savings, the loop bandwidth is dynamically controlled via a gearshift technique [82]. During frequency acquisition, the loop operates in

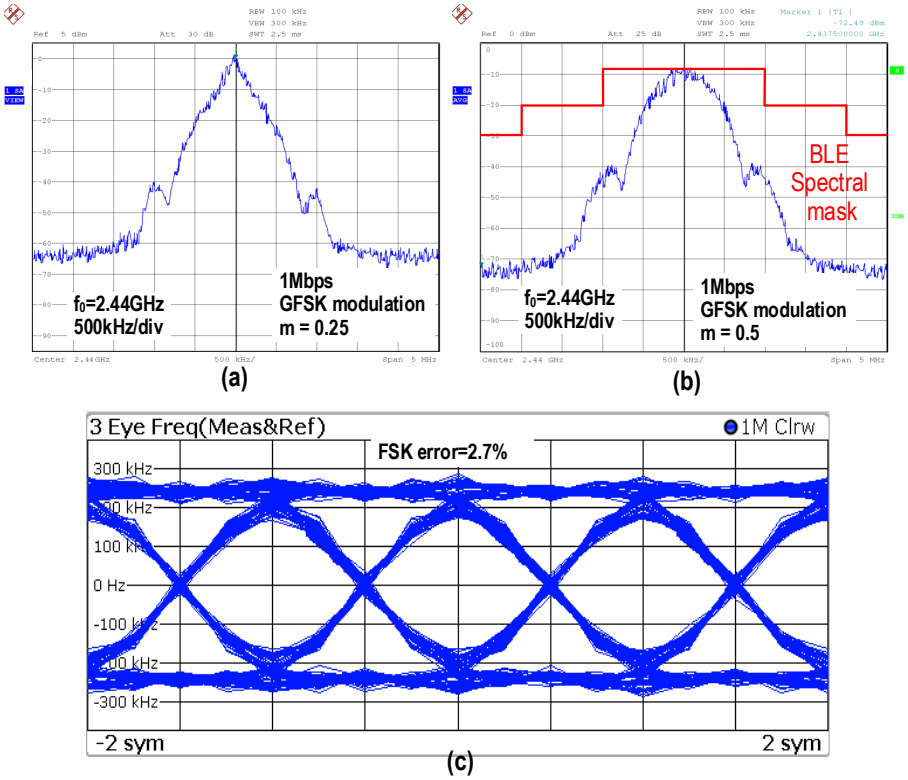


Figure 7.23: Bluetooth GFSK modulation spectrum for modulation index of (a) m=0.25, (b) m=0.5, and (c) burst-mode modulation accuracy.

type-I, with a wide bandwidth of 2 MHz. It is then switched to type-II, 4th-order IIR filter with the 500 kHz bandwidth when it enters tracking mode. Finally, the loop bandwidth is reduced to 200 kHz to optimize ADPLL integrated jitter. The measured lock-in time is less than 15 μs for F_{REF} of 40 MHz as shown in Fig. 7.24 (a). Thanks to the low flicker noise, frequency pushing and pulling of the DCO, its frequency drift is extremely small, as demonstrated Fig. 7.24 (b). Consequently, the rest of ADPLL can be shut-down during the modulation to improve the power efficiency of the BLE transmitter. The maximum difference between 0/1 frequency at the start of a BLE packet and 0/1 frequencies within the packet payload should be less than ±50 kHz. This specification is properly satisfied with over an order-of-magnitude margin even while in the open loop operation, as shown in Fig. 7.24 (b) and (c).

The PA output level is adjustable between -5 to +3 dBm and reaches peak PAE of 41%, which includes the power consumption of two stages of PA drivers (see Fig. 7.25 (a)). The measured TX harmonic emissions are shown in Fig. 7.25 (b). Due to the differential operation, proper second-harmonic termination and trading negligible efficiency loss for higher loaded Q-factor of PA's matching network, second and third harmonics remain well below the -41 dBm regulatory limit. The proposed TX consumes 3.6/5.5 mW during the open-loop 1 Mb/s GFSK BLE modulation at 0/3 dBm output, resulting in η_{TX}=28/36% total TX efficiency. The power consumption would increase by 0.8 mW with TDC, variable counter and digital circuitry turned on when the ADPLL is clocked at 40 MHz FREF. Thus, even in the closed loop, with η_{TX}=23/32% at 0/3 dBm, it is still 1.5x more power efficient than the prior record. The TX power breakdown is also illustrated in Fig. 7.25 (c).

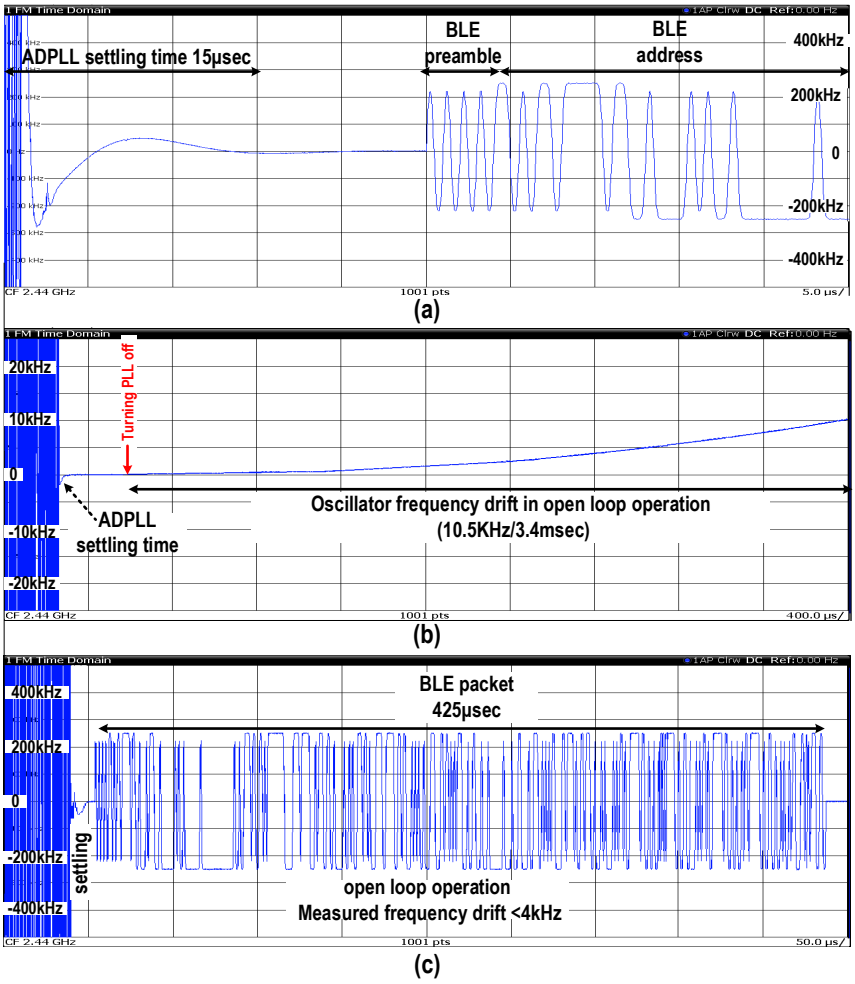


Figure 7.24: (a) ADPLL settling; (b) oscillator frequency drift and (c) demodulated TX frequency for 425 μsec BLE packet in the open-loop operation.

Table 7.4 summarizes the performance and compares it with leading ULP transmitters [8–10, 146–149]. The proposed ULP TX achieves the lowest power consumption and phase noise.

7.6 Conclusion

We have proposed an ultra-low power (ULP) Bluetooth Low Energy (BLE) transmitter that demonstrates the best ever reported system efficiency and phase purity, while abiding by the strict 28 nm CMOS technology manufacturing rules. A new switching current source oscillator combines advantages of low supply voltage of the conventional NMOS cross-coupled oscillator with high current efficiency of the complementary push-pull oscillator to reduce the oscillator supply voltage and dissipated power further than practically possible in the traditional oscillators. Due to the low wander of DCO, digital power consumption of ADPLL can be significantly saved by scaling down the rate of sampling clock after settling or even shutting it off entirely during direct DCO data modulation. A fully integrated differential class-E/F_2 switching PA is utilized to improve system efficiency at low output power of 0–3 dBm while fulfilling all in-band and out of band emission masks. Its required matching network was realized by exploiting different behaviors of a 2:1 step-down transformer in differential and common-mode excitations.

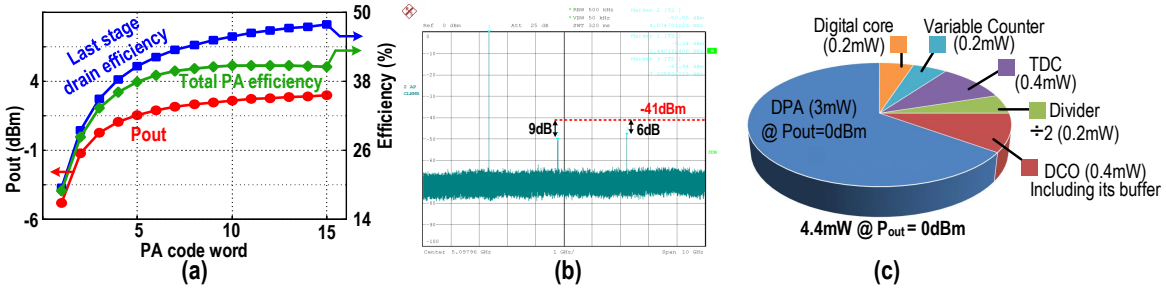


Figure 7.25: (a) PA characteristics; (b) TX harmonic emissions; and (c) TX power breakdown at P_{out}=0 dBm.

Table 7.4: Performance summary and comparison with state-of-the-art.

	This work			ISSCC'15 IMEC	JSSC'15 Dialog	ISSCC'15 Renesas	ISSCC'12 Toumaz	ESSCIRC'14 Frontier	TMTT2013 J. Masuch	CC2640 TI	
CMOS technology	28nm			40nm	55nm	40nm	130nm	65nm	130nm	N/A	
OSC PN @1MHz (dBc/Hz)	-116 to -117			-110	-111.5	N/A	-107	-108.2	-110	-109	
OSC FoM (dB)	188-189			183	179	N/A	N/A	N/A	185	N/A	
OSC tuning range	2.05-2.55GHz (22%)			25%	20%	N/A	N/A	N/A	N/A	N/A	
PLL in-band PN (dBc/Hz)	-92 @ FREF=5MHz -101@ FREF=40MHz			-90	N/A	N/A	-87	-87.5	-100	N/A	
Integrated PN (degree)	1.08 @ FREF=5MHz 0.87 @ FREF=40MHz			1.5	N/A	N/A	N/A	N/A	N/A	N/A	
PLL FoM* (dB)	-238.65			-236	N/A	N/A	N/A	N/A	N/A	N/A	
PLL settling time(µs)	15			15	15	N/A	N/A	N/A	N/A	N/A	
Reference/Fractional spurs (dBc)	-80 / -60			-70 / -38	N/A	N/A	N/A	N/A	-75/-37	N/A	
TX Modulation error	2.70%			5%	N/A	N/A	7.30%	7%	N/A	N/A	
Output power (dBm)	-5 to +3			-2/1	-20 to 0	0	-30 to +5	-10 to -3	1.6	-21 to +5	
Total PA efficiency	41%			25%	30%	<30%	N/A	<25%	26.80%	N/A	
On-chip matching network	Yes			No	Yes	Yes	No	No	Yes	No	
Strongest harmonic emission	HD3/-47dBc			HD2/-49dBc	HD2/-50dBc	HD3/-48dBc	N/A	N/A	HD3/-34dBc	-46dBc	
Supply voltage (V)	0.5 / 1			1	0.9-3.3	1.1	1	1.1	1	1.8-3.8	
TX power consumption (mW)	@P_{OUT}	0dBm	3dBm	-2dBm	0dBm	0dBm	0dBm	-3dBm	1.6dBm	0dBm	5dBm
	open-loop	3.6	5.5	4.2	10.1†	7.7†	8.9†	5.1†	5.9	18.3	27.3
	close-loop	4.4	6.3								
TX efficiency (P_{OUT}/P_{DC})	open-loop	28%	36%	15%	10%	13%	12%	10%	25%	5.5%	11.5%
	close-loop	23%	32%								
TX active area (mm²)	0.65			0.6†	0.6‡	0.6‡	1‡	0.6‡	0.6‡	N/A	

* FoM=$10\log_{10}[\sigma^2_{jitter}\cdot(P_{DC,PLL}/1mW)]$ †including DC-DC converters, ‡graphically estimated

Furthermore, for both proposed oscillator and power amplifier, accurate key analytical equations are derived to provide useful design insights.

7.7 Appendix A

Consider the switching current-source oscillator of Fig. 7.8. Since M_{3-4} transistors work only in weak inversion and saturation during their on-state, short-channel modulation effects should be considered in the G_{DS4EF} calculation in (7.10). It is well known that $g_{ds4}(\phi) = \lambda \cdot I_{M4}(\phi)$, where, I_{M4} and λ are, respectively, the drain current and channel-length modulation coefficient of M_4. As a result, G_{DS4EF} is estimated as

$$G_{DS4EF} = G_{DS4}[0] - G_{DS4}[2] = \frac{1}{2\pi}\int_0^{2\pi} g_{ds4}(\phi)\cdot(1-\cos 2\phi)\,d\phi = \frac{\lambda\cdot I_{DC}}{2}\cdot\left(1-\frac{I_{M4,H2}}{I_{DC}}\right) \tag{7.29}$$

where, $I_{M4,H2}$ is the 2nd harmonic of I_{M4}. By considering $\lambda = 4.8\,\mathrm{V}^{-1}$, $I_{M4,H2}/I_{DC}$=0.33, and, $I_{DC} = 750\,\mu$A, the calculated G_{DS4EF} becomes 1.2 mS, which agrees fairly well with the simulation results in Fig. 7.12 (a).

On the other hand, since M_1 works in saturation only for a short part of the oscillation cycle and its channel conductance, g_{ds1}, is much larger in the triode region, a square-law behavior in the G_{DS1EF} calculation in (7.10) seems a good assumption. As a result, g_{ds1} may be estimated by

$$g_{ds1}(\phi) = \begin{cases} K_1\left[(V_B - V_t - V_0) + 0.5V_{osc}\left(1 + A_0\right)\cos\phi\right] & -\theta_0 \le \phi \le \theta_0 \\ 0 & -\pi \le \phi \le -\theta_0,\ and,\ \theta_0 \le \phi \le \pi \end{cases} \tag{7.30}$$

where, $K_1 = \mu_n C_{ox} W_1/L_1$, and, V_0 is the DC voltage at DA and DB. θ_0 is the triode angle calculated as

$$\theta_0 = \cos^{-1}\left(\frac{V_0 + V_t - V_B}{0.5V_{osc}\left(1 + A_0\right)}\right) \tag{7.31}$$

By exploiting the G_{DS1EF} definition and carrying out a lengthy algebra, we obtain

$$G_{DS1EF} = \frac{K_1}{2\pi}\left[2\left(V_B - V_0 - V_t\right)\cdot\left(\theta_0 - \sin(\theta_0)\cos(\theta_0)\right) + \frac{2}{3}V_{osc}\left(1 + A_0\right)\sin^3(\theta_0)\right] \tag{7.32}$$

By replacing the oscillator's circuit parameters ($V_B = 0.45\,V, V_t = 0.485\,V, V_0 = 0.15\,V, V_{osc} = 0.3\,V, A_0 = 2.15$, and, $K_1 = 0.125\,A/V$) in (7.31) and (7.32), the calculated G_{DS1EF} is equal to 3.81 mS, which is in good agreement with the simulations (see Fig. 7.12 (a)).

7.8 Appendix B

Consider the transformer-based matching network shown in Fig. 7.15 (b). The current through the secondary and primary windings of the ideal transformer can be respectively calculated by

$$I_{sEF} = pI_s = I_L\left(1 + jR_LC_L\omega_0\right), \qquad \text{and} \qquad I_1 = \frac{mn}{k_m}I_{sEF} = I_L\frac{mn}{k_m}\left(1 + jR_LC_L\omega_0\right). \tag{7.33}$$

Furthermore, the voltage across the magnetizing inductance, $L_pk_m^2/(mp)$, is given by

$$\begin{gathered} V_p = I_L\frac{k_m}{mn}\left(R_L + \frac{mr_s}{p}(1 + jR_LC_L\omega_0)\right) \xrightarrow{r_s = L_s\omega_0/Q_s} \\ V_p = I_L\frac{k_mL_s\omega_0}{np}\left(\frac{pR_L}{mL_s\omega_0} + \frac{1}{Q_s} + j\frac{R_LC_L\omega_0}{Q_s}\right). \end{gathered} \tag{7.34}$$

Consequently, the current through the leakage inductance, $L_p(1 - k_m^2)/(mp)$, is calculated by

$$I_{pEF} = I_1 + \frac{mpV_p}{jk_m^2L_p\omega_0} = I_L\frac{mn}{jk_m}\left(\left(\frac{pR_L}{mL_s\omega_0} + \frac{1}{Q_s} - R_LC_L\omega_0\right) + j\left(1 + \frac{R_LC_L\omega_0}{Q_s}\right)\right). \tag{7.35}$$

As a result, the total power dissipated in the transformers' secondary and primary is respectively estimated:

$$P_{rs} = \frac{mr_s}{p}\left|I_{sEF}\right|^2 \xrightarrow{r_s = L_s\omega_0/Q_s\ and\ (7.33)} P_{rs} = I_L^2\frac{m}{p}\frac{L_s\omega_0}{Q_s}\left|1 + jR_LC_L\omega_0\right|^2, \tag{7.36}$$

and,

$$P_{rp} = \frac{r_p}{mp}\left|I_{pEF}\right|^2 \xrightarrow{r_p=L_p\omega_0/Q_p \text{ and } (7.35)}$$
$$P_{rp} = I_L^2 \frac{m}{p}\frac{L_s\omega_0}{k_m^2 Q_p}\left|\left(\frac{1}{Q_s}+\frac{pR_L}{mL_s\omega_0}-R_L C_L\omega_0\right)+j(1+\frac{R_L C_L\omega_0}{Q_s})\right|^2. \tag{7.37}$$

The matching network efficiency, η_p, is the ratio of power delivered to the load, P_L, over total power: $\eta_p = P_L/(P_L + P_{rp} + P_{rs})$. By exploiting (7.36) and (7.37), (7.20) is obtained.

On the other hand, the load Z_L seen from the input ports of the matching network (see Fig. 7.15) can be calculated by

$$Z_L = j(1-k_m^2)L_p\omega_0 + \frac{mpV_p}{I_{pEF}} \rightarrow Z_L = jL_p\omega_0\left[(1-k_m^2)+k_m^2\frac{(1+\xi Q_L Q_s)+jQ_L}{(1+Q_L Q_s(\xi-1))+j(Q_L+Q_s)}\right]. \tag{7.38}$$

As a result, the equivalent series inductance and load resistance seen from the transformer's primary can be respectively estimated by

$$L_{ser} = \frac{Im\{Z_L\}}{\omega_0} = L_p\left[(1-k_m^2)+k_m^2\frac{1+2\xi Q_L Q_s+Q_L^2+Q_L^2Q_s^2\xi(\xi-1)}{1+2\xi Q_L Q_s+Q_L^2+Q_s^2+Q_L^2Q_s^2(\xi-1)^2}\right], \tag{7.39}$$

and,

$$r_L = Re\{Z_L\} = k_m^2 L_p\omega_0 Q_L \cdot \frac{\frac{Q_s}{Q_L}(1+Q_L^2+\xi Q_L Q_s)}{1+2\xi Q_L Q_s+Q_L^2+Q_s^2+Q_L^2Q_s^2(\xi-1)^2}. \tag{7.40}$$

By exploiting Q_L and ξ definitions, we have

$$r_L = R_L \cdot \frac{p}{m}(\frac{k_m}{n})^2 \cdot \frac{\frac{Q_s}{\xi Q_L}(1+Q_L^2+\xi Q_L Q_s)}{1+2\xi Q_L Q_s+Q_L^2+Q_s^2+Q_L^2Q_s^2(\xi-1)^2}. \tag{7.41}$$

By considering $Q_s \gg 1$ and $Q_s^2 \gg Q_L^2$, (7.41) and (7.39) are immediately simplified to (7.25) and (7.26).

Chapter

8

Conclusion

This dissertation focuses on the analysis, design, and implementation of RF/mm-wave oscillators and power amplifiers as the most power-hungry blocks of any wireless transceiver. Furthermore, a 4G all-digital phase locked loop and a Bluetooth Low Energy transmitter are also implemented by exploiting the proposed oscillators and power amplifiers topologies. As a result, both systems demonstrate higher power efficiency over prior records. In this aspect, the final chapter of this work is presented. Section 8.1 summarizes the thesis, and it also repeats the accomplishments achieved throughout this thesis. Finally, Section 8.2 provides some suggestions and recommendations for future improvements of this research work.

8.1 The Thesis Outcome

While wireless industry enjoys the largest production volume ever of any consumer electronics product, the demands they place on RF/mm-wave transceivers are particularly tough, especially on integration with digital processors, low area, and low power consumption while being robust against process-voltage-temperature variations. Since wireless terminals usually operate on batteries, RF/mm-wave oscillators and power amplifiers as the most power hungry blocks of any transceiver should be very power efficient. On the other hand, the vision for wireless communication systems keeps moving towards more mature integration strategy. This trend dictates RF and digital circuits implemented together in the advanced technology nodes. However, as described in Chapter 2, the performance of RF/mm-wave oscillators and power amplifiers slightly degrades with scaling. This has motivated an intensive research leading to introduced new oscillator and power amplifier topologies.

In Chapter 2, a new structure for LC-tank oscillators is presented. It introduces an impedance peak around the third harmonic of the oscillating waveform such that the third harmonic of

the active device current converts into voltage and, together with the fundamental component, creates a pseudo-square oscillation voltage. As a result, the oscillator circuit-to-phase noise conversion is reduced. The major mechanisms arise when the active gm-devices periodically enter the triode region during which the LC-tank is heavily loaded while its equivalent quality factor is significantly reduced. A class-F oscillator was prototyped in 65-nm CMOS technology. The measurement results prove that the proposed oscillator can achieve a state-of-the-art phase noise performance with the highest power efficiency at low voltage power supply without die area penalty or voltage swing constraint. In Chapter 3, the proposed class-F oscillator is exploited in a 28nm all-digital PLL for 4G mobile phones. Thanks to the power efficiency of the digitally controlled oscillator, ADPLL demonstrates a 72% power reduction over prior records.

In Chapter 4, another flavor of a class-F oscillator is introduced. The main idea is to enforce a clipped voltage waveform around the LC tank by increasing the second-harmonic of fundamental oscillation voltage through an additional impedance peak thus giving rise to a class-F_2 operation. It also offers enough headroom for the low noise operation of the tail current transistor without compromising the oscillator current and voltage efficiencies. Furthermore, the special ISF of the soft clipping waveform significantly reduces the circuit-to-phase noise conversion. Consequently, the proposed structure is able to push the phase noise much lower than practically possible with the traditional LC oscillators while satisfying long-term reliability requirements.

The precise analytical voltage-current waveforms, zero-voltage, and zero-slope switching criteria and waveform dependent parameters of any flavor of a switched-mode PA are quantified in Chapter 5. Furthermore, closed-form equations are derived for the optimum size of the switch and different PA's characteristics such as maximum achievable power added efficiency, output power and maximum operating frequency. Based on this analysis, a 40 nm 60 GHz Class-E/F_2 power amplifier is implemented in Chapter 6. This PA utilizes a proper second-harmonic termination in the last stage and low/moderate magnetic coupling factor transformers in the intermediate stages to reach the best product of power added efficiency and bandwidth. The PA is also stabilized against the combination of differential and common oscillation modes.

Finally, an ultra-low power Bluetooth Low Energy (BLE) transmitter is introduced in Chapter 7. An all-digital PLL employs a digitally controlled oscillator with switching current sources to reduce supply voltage and power without sacrificing its phase noise and startup margins. It also reduces 1/f noise allowing the ADPLL, after settling, to reduce its sampling rate or shut it off entirely during direct DCO data modulation. The switching power amplifier integrates its matching network while operating in class-E/F_2 to maximally enhance its efficiency. The transmitter is realized in 28-nm CMOS and satisfies all metal density and other manufacturing rules. It consumes 3.6 mW/5.5 mW while delivering 0 dBm/3 dBm RF power in Bluetooth Low Energy.

8.2 Some Suggestions for Future Developments

The presented research introduced different oscillator and power amplifier topologies showing high power efficiency and also verified their effectiveness in real systems within commercial settings. The results open new opportunities for further research and developments.

- To improve the phase noise and FoM of a class-F_3 oscillator, the magnitude ratio of the third-to-first harmonic components of the drain oscillation voltage should be close to

1/3. It can be done by reducing coupling factor of the transformer to 0.6 and adjusting L_sC_2/L_pC_1 of 5 (please, refer to Chapter 2.).

- The flicker noise upconversion of RF oscillators significantly reduces by adding an auxiliary resonance at the second harmonic of the fundamental frequency (class-F_2 operation). This phenomenon can lead us to achieve yet more insights into flicker noise upconversion mechanisms and to find new methods to further improve $1/f^3$ phase noise corner of RF oscillators.

- The derivation in Section 2.3 offers a good insight but still more works to be done to reach a complete portrait of circuit-to-phase noise conversion of the transformer-based oscillators.

- The required passive voltage gain of all proposed oscillators is realized with step-up transformers. However, the quality factor of transformer's windings degrades dramatically with increasing its turns ratio and thus its voltage gain. It leads to a significant penalty on the oscillator phase noise and power efficiency. A higher passive voltage gain and tank's quality factor may be achieved by employing either capacitive voltage dividers or autotransformers. (please, refer to Chapter 7.)

- As explained in Chapter 5, vital parameters of a switched-mode PA, such as F_C, F_V, K_C, and K_L improve by operating in the domain of non-zero voltage, but zero derivative voltage, switching. These improvements easily compensate the side effect of additional charge loss on the maximum achievable power added efficiency (PAE) of the switched-mode amplifier. Consequently, non-zero voltage switching power amplifiers offer better linearity, higher maximum operating frequency, and output power at the same level of PAE as with the zero-voltage switching amplifiers. More work should be done to further investigate and implement it.

- The antenna must be shared between the transmitter and the receiver in a Bluetooth Low Energy system. Hence, PA and LNA matching networks have to be revised to alleviate harmful interactions. I recommend using PA's matching network to improve the receiver's blocker resilience and employing LNA's matching network to reduce harmonic emissions of the PA in the TX mode.

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Summary

[1] In the next few years, Fifth Generation (5G) cellular systems and the wireless Internet-of-Things (IoT) are expected to see significant deployment to realize more integration between the physical and digital worlds, promising high data rate communications and enabling more objects to be remotely sensed and controlled. Since mobile terminals inherently operate on batteries, an ever-decreasing power per bit is required to improve the system battery lifetime. Similarly, the power consumption of RF/mm-wave building blocks should be reduced to satisfy the lifetime demands of cellular and IoT systems.

On the other hand, in a system-on-chip (SoC), the choice of technology node is often driven by the performance and cost of digital circuits, which occupy most of the area. An RF/analog designer may play a small role in driving this decision. Therefore, it is not rare to find the worst lineup of process options available to an RF/analog designer. The size, cost, and power consumption of digital circuits are reduced by technology scaling. However, the design of analog/RF circuits faces many difficulties using more advanced CMOS technologies. For example, the supply voltage is reduced while RF and analog circuits must maintain their dynamic range, noise performance, and output power. Consequently, new analog/RF techniques are required to achieve a fully integrated power/area efficient transceivers in low-voltage deep nanoscale CMOS technology.

RF/mm-wave oscillators and power amplifiers are recognized as the most power-hungry blocks of any wireless transceiver. Consequently, any power reduction in them will greatly benefit the overall power efficiency of the radio. Furthermore, they have not significantly benefited from technology scaling. Hence, the main focus of this dissertation is to innovate the RF/mm-wave oscillator and power amplifier structures that demonstrate better performance, lower cost, and higher power efficiency than traditional architectures.

This thesis is composed of three parts. The main focus of the first part (Chapter 2–4) is on the design and implementation of innovative RF/mm-wave oscillators for wireless applications.

[1] Mr. Malotaux has translated the summary as well as proposition of this dissertation into Dutch. Then, Prof. de Vreede has revised the summary.

A new class of operation for RF oscillators is introduced to fill the performance/power gap in the ultra-high figure of merit and ultra-low phase noise oscillator space currently not satisfied by state-of-the-art structures. The main idea is to enforce a clipped voltage waveform around the LC tank by increasing the harmonic components of the oscillation voltage through additional impedance peaks, thus giving rise to a class-F operation. As a result, the circuit-to-phase noise conversion decreases in class-F oscillators such that a significant improvement in the oscillator's phase noise and power efficiency are achieved. The auxiliary impedance peaks are realized by exploiting the different behavior of a step-up transformer in common-mode and differential-mode excitations or employing a transformer's leakage inductance. The proposed oscillator is also implemented as the heart of an all-digital phase-locked loop to demonstrate its effectiveness on improving the power efficiency of a Fourth Generation (4G) frequency synthesizer.

The objective of the second part of this dissertation (Chapter 5–6) is about analysis and design of RF/mm-wave switched-mode power amplifiers. Different characteristics of switched-mode PAs are investigated and quantified in Chapter 5. This allows designers to better understand how to choose the best topology among different flavors of switched-mode PAs suited to meet their various specifications. Different trade-offs between the power gain, output power, drain efficiency, maximum operating frequency, and power added efficiency are comprehensively studied for various kinds of switched-mode PAs. These insights lead to the design and implementation of a fully integrated 60 GHz power amplifier in Chapter 6. This PA reaches the highest reported product of power-added efficiency and bandwidth. It is achieved through low/moderate coupling-factor transformers in preliminary stages and a proper second-harmonic termination of the output stage such that it can operate as a class-E/F_2 switched-mode PA at the saturation point.

Finally, a new transmitter architecture for ultra-low power radios is introduced in the third part of this dissertation (Chapter 7). A novel digitally controlled oscillator with switching current sources is introduced to reduce supply voltage and power without sacrificing its phase noise and startup margins. Due to the low wander of DCO, digital power consumption of ADPLL can be significantly saved by scaling down the rate of sampling clock after settling or even shutting it off entirely during direct DCO data modulation. A fully integrated differential class-E/F_2 switching PA is designed to improve system efficiency at low output power of 0–3 dBm while fulfilling all in-band and out-of-band emission masks. Based on those innovations, an ultra-low power Bluetooth Low Energy transmitter is proposed that demonstrates the best ever reported system efficiency and phase purity. Furthermore, for both proposed oscillator and power amplifier, accurate key analytical equations are derived to provide useful design insights.

Samenvatting

[1] Het is de verwachting dat in de komende paar jaar, Vijfde Generatie (5G) mobiele netwerken en het internet-der-dingen (IoT) op grote schaal worden toegepast om verregaande integratie tussen de fysische en digitale wereld te realiseren, dit met de belofte van snellere datacommunicatie en ondersteuning van meer objecten die op afstand kunnen worden uitgelezen en gecontroleerd. Omdat mobiele apparaten afhankelijk zijn van batterijen is een steeds verdere afname van de energie-per-bit noodzakelijk om de batterijlevensduur te verlengen. Evenzo is het dus wenselijk om het vermogensverbruik van de RF/mm-golf schakelingen in mobiele en IoT systemen te reduceren om aan de batterijlevensduureisen van deze systemen te voldoen.

In een "systeem-op-chip" (SoC) wordt de keuze van de technologiegeneratie vaak bepaald door de prestatie en kostprijs van de digitale schakelingen die vaak het grootste deel van het IC oppervlakte innemen. De analoge/RF ontwerper heeft bij deze technologiekeuze maar een beperkte rol. Het is daarom ook niet ongewoon dat de gekozen technologie verre van ideaal is voor het ontwerp van hoogfrequente- en analoge schakelingen. De benodigde oppervlakte, kosten en energieverbruik van digitale schakelingen worden sterk verminderd door technologische schaling. Deze schaling brengt echter voor het ontwerp van de analoge- en hoogfrequente schakelingen veel complicaties met zich mee. Zo wordt de voedingsspanning verminderd, terwijl het dynamisch bereik, ruisprestaties en uitgangsvermogen van deze RF- en analoge schakelingen moeten worden behouden. Hierdoor is er behoefte aan nieuwe analoge/RF ontwerptechnieken die volledig geïntegreerde en energie/oppervlak efficiënte zend-ontvangst schakelingen mogelijk maken en goed functioneren bij de lagere voedingsspanningen van geavanceerde CMOS technologieën.

RF/mm-wave oscillatoren en eindversterkers worden in het algemeen gezien als de meest energieverslindende functies in elke zend-ontvangstschakeling. Vandaar dat een efficiëntieverbetering in een van deze bouwblokken sterk bijdraagt in het energieverbruik van de gehele radio. Bovendien ondervinden deze schakelingen nauwelijks enig voordeel van technologische schaling. Deze scriptie stelt zich dan ook als doel om innovaties in de oscillator en vermogensversterker te

[1] Mijn hartelijke dank gaat uit naar de heer Satoshi Malotaux van de Technische Universiteit Delft. De heer Malotaux heeft zowel de samenvatting als het stellingen van dit proefschrift vertaald in het Nederlands. Prof. de Vreede heeft de Nederlandse versie van de samenvatting bijgewerkt.

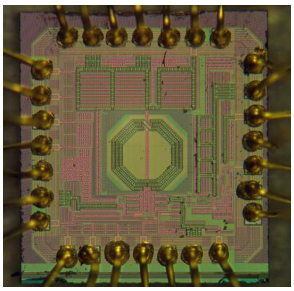
bewerkstelligen die leiden tot betere prestaties, lagere kosten en een hogere efficiëntie dan die van traditionele radioarchitecturen.

Dit proefschrift bestaat uit drie delen. Het eerste deel (hoofdstuk 2–4) richt zich op het ontwerpen en implementeren van innovatieve RF/mm-wave oscillatoren voor draadloze toepassingen. Een nieuwe werkconditie voor RF oscillatoren wordt geïntroduceerd om de tekortkomingen van de huidige "state-of-the-art" ultra-lage faseruis oscillatoren, in termen van hun prestatie parameters, te overwinnen. Het belangrijkste idee hierbij is om een afgetopte spanningsgolfvorm over de LC tank af te dwingen door het verhogen van de harmonische componenten, m.b.v. extra hoge impedanties voor deze frequenties wat leidt tot "klasse-F" operatie. Dit leidt tot een lagere circuit-faseruis omzetting waardoor deze "klasse-F" oscillatoren een significante verbetering in hun faseruis gedrag en efficiëntie laten zien. De extra impedantie pieken worden gerealiseerd door het optimaal benutten van de verschillen in het common-mode en differentiaal-mode gedrag van een spanning-verhogende transformator of door slim gebruik te maken van de "lek-inductantie". De geïntroduceerde oscillator is ook geïmplementeerd als het hart van een volledig gedigitaliseerde fase-gesynchroniseerde frequentiegenerator (phase-locked loop) om de efficiencyverbetering bij 4G applicaties aan te tonen.

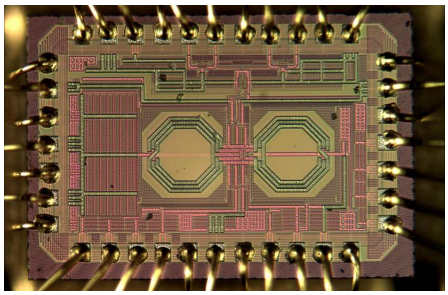
Het tweede deel van dit proefschrift (hoofdstuk 5–6) gaat over de analyse en het ontwerp van RF/mm-golf geschakelde vermogensversterkers. In hoofdstuk 5 worden de verschillende eigenschappen van deze architecturen onderzocht en gekwantificeerd. Dit geeft een ontwerper het benodigde inzicht om, vanuit de verschillende geschakelde vermogensversterkers configuraties, de juiste topologie keuze te maken voor het behalen van de gewenste specificaties. Verschillende ontwerpafwegingen tussen vermogensversterking, zendvermogen, maximaal haalbare werkfrequentie, drain- en toegevoegd-vermogen efficiency zijn grondig bestudeerd voor een aantal type geschakelde vermogensversterkers. Deze inzichten hebben geleid tot het ontwerp en de implementatie van de, in hoofdstuk 6 beschreven, volledige geïntegreerde 60 GHz vermogensversterker. Deze versterker behaalde het tot nu toe hoogst gerapporteerde product tussen toegevoegd-vermogen, efficiency en bandbreedte. Dit wordt bereikt door gebruik te maken van lage/matige-koppeling transformatoren in de aanstuurtrappen en een goede tweede harmonische afsluiting van de versterker eindtrap, zodanig dat deze opereert als een klasse-E/F_2 geschakelde vermogens versterker in het verzadigingspunt.

zonder in te boeten aan faseruis en opstartmarge. Door de lage drift van de DCO kan het stroomverbruik van ADPLL aanzienlijk worden gereduceerd d.m.v. het verlagen van de bemonsteringklok, of deze zelfs geheel te stoppen gedurende directe DCO datamodulatie. Een volledig geïntegreerde differentieel klasse-E/F_2 geschakelde PA is ontworpen om de systeemefficiëntie te verbeteren bij lage uitgangsvermogens van 0–3 dBm, terwijl aan alle in-band en out-of-band emissiemaskers wordt voldaan. Op basis van deze innovaties is een ultra-low-power Bluetooth Low Energy-zender gepresenteerd die het beste ooit vermelde systeemrendement en fasezuiverheid behaald. Verder zijn voor zowel de geïntroduceerde oscillator als eindversterker, nauwkeurige analytische vergelijkingen gegeven om nuttige ontwerpinzichten te verschaffen

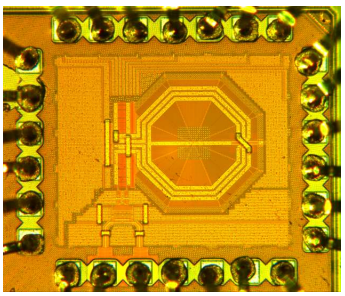
Chip Micrograph Gallery



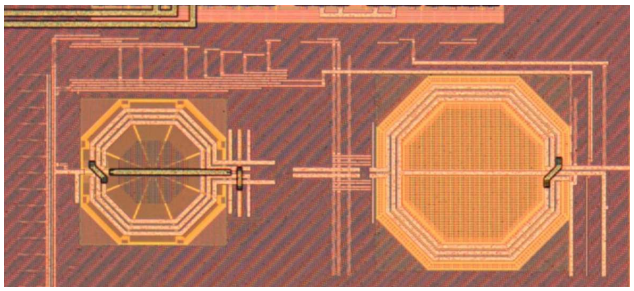
A Class-F CMOS Oscillator in 65nm [ISSCC2013, JSSC2013]



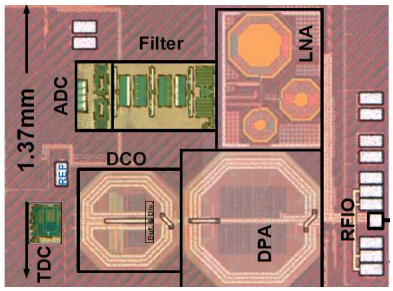
An ultra-low phase noise class-F_2 oscillator in 65nm [RFIC2013, JSSC2015]



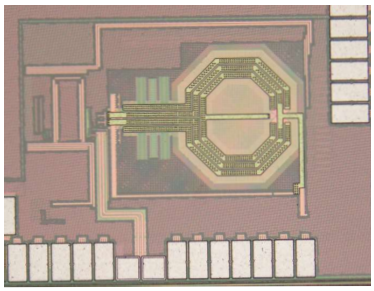
A 0.5mW Switching Current Source Oscillator in 40nm [RFIC2015]



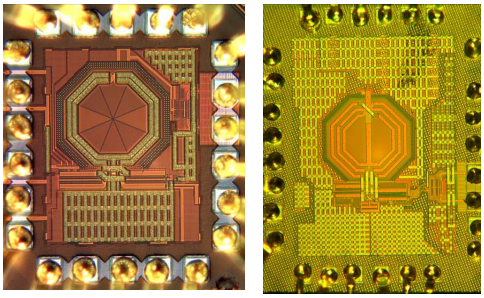
A Bluetooth Low-Energy Transmitter with 36% System Efficiency in 28nm [ESSCIRC2015, JSSC2016] (with TSMC RF group)



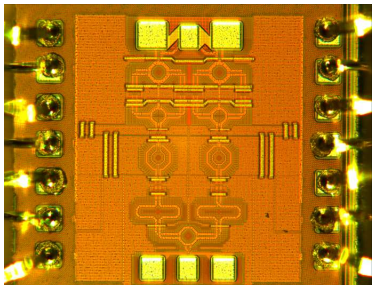
A Bluetooth Low-Energy Transceiver in 28nm [VLSI2016] (with S. Binsfeld and TSMC RF group)



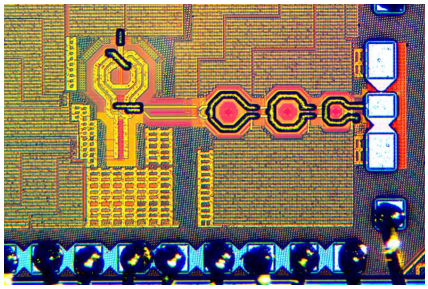
An All-Digital PLL for 4G Phones in 28nm [VLSI2014] (with TSMC RF group)



A 1/f Noise Upconversion Reduction Technique for RF Oscillators in 40nm [ISSCC2015] (with M. Shahmohammadi)



A wideband 60GHz class-E/F_2 PA in 40nm [RFIC2015]



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