

Supply Regulation Techniques for Phase-Locked Loops

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Abstract— Phase-locked loops (PLLs) which employ voltage regulators for low supply-noise sensitivity often rely upon significant decoupling capacitance to suppress negative (Gnd) supply noise and maintain low jitter. This paper compares various supply regulation techniques on the basis of their ability to reject noise from both positive and negative supplies. A novel replica-based dual-supply regulation technique is proposed which allows for significant reduction in decoupling capacitance for a given supply noise rejection. Comparison simulations in a 90nm CMOS technology show the replica-based dual-supply regulation technique achieving a worst case noise sensitivity of 1.6 rad/V, an improvement of 7.5 rad/V (15.1dB) relative to a single-supply replica-based regulator topology. At 4.7GHz, the replica-based dual-supply regulated PLL consumes 11mW from a 1.2V supply.

I. INTRODUCTION

Increased integration in system-on-a-chip (SOC) architectures requires analog circuit blocks to maintain high performance in environments with large amounts of digital switching noise. While PLLs which employ voltage-controlled oscillators (VCOs) with full-swing CMOS delay elements are attractive due to their fast switching, design simplicity, and portability, these architectures are sensitive to supply-noise which induces jitter on the PLL output clocks. Employing a voltage regulator to generate the VCO control voltage, as shown in Fig. 1, reduces this supply-noise induced jitter by attenuating noise originating from the positive (Vdd) supply; while an often large amount of decoupling capacitance suppresses high-frequency noise from the negative (Gnd) supply. Simple regulator structures require high power consumption to maintain power supply rejection out to high noise frequencies; motivating recent research into replica-based regulator topologies [1-3] for improved energy efficiency.

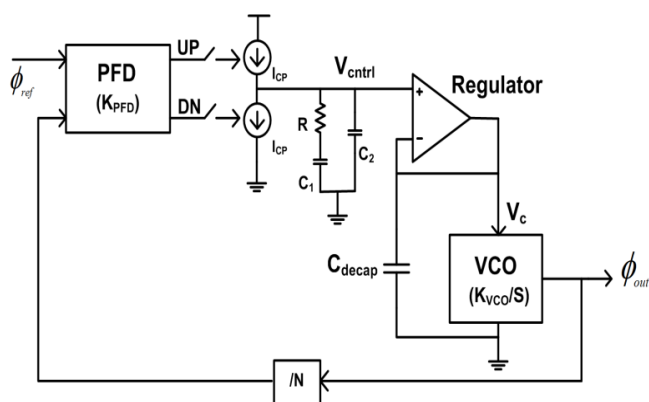


Fig. 1. PLL Block Diagram

While the VCO typically displays the highest sensitivity to supply-noise, the other PLL blocks also contribute to the total output jitter, with their noise transfer functions shaped by the closed-loop system. The PLL closed loop transfer function from the input phase to the output phase is a low pass filter which rejects input noise with frequencies higher than the PLL bandwidth. A bandpass response with center frequency at the PLL bandwidth is observed from the VCO control input to the PLL output. These PLL transfer functions reveal that the regulators should have good supply noise rejection at least up to the PLL bandwidth, while achieving higher regulator bandwidth provides additional high frequency jitter suppression.

A number of supply regulation techniques for PLLs have been reported recently. [1] discusses the concept of replica based regulation for stability, improvement in DC gain, and increase in power supply rejection bandwidth. [2] and [3] use the replica concept without feedback from the main arm to further increase the regulator power supply rejection bandwidth. While these techniques are effective in supply-noise induced jitter suppression, they all rely upon significant decoupling capacitance to suppress negative-supply noise, which can be significant in SOCs with multiple supply domains sharing a common ground rail. This paper compares various supply regulation techniques on the basis of their ability to reject noise originating from both positive and negative supplies. In addition, a novel replica-based dual-supply regulation technique is proposed which allows for significant reduction in decoupling capacitance for a given supply noise rejection.

II. SINGLE SUPPLY REGULATION

As the VCO is often the most supply-noise sensitive block in a PLL, using a low-dropout regulator to provide the positive supply of a supply-tuned VCO is a common technique for reducing jitter. However, considering that the VCO frequency is set by the difference between the regulated control voltage, V_c , and the negative supply, the amount of decoupling capacitance employed can have a large impact on this overall differential VCO control voltage noise in the presence of significant negative-supply noise. A simplified regulator small-signal model for the positive VCO supply is shown in Fig. 2. With finite impedance on both supply rails, switching current will induce independent supply noise modeled as $V_{n\text{vdd}}$ and $V_{n\text{gnd}}$.

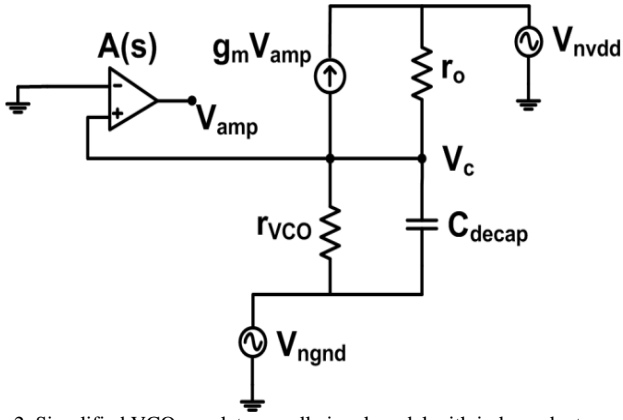


Fig. 2. Simplified VCO-regulator small-signal model with independent supply noise sources

The effect of V_{nvdd} on the regulated control voltage V_c , (using the principle of superposition and hence, shorting V_{ngnd}) can be derived as

$$V_c = \frac{V_{nvdd}}{r_o} \left[\frac{1}{Z_{VCO}} + A(s)g_m + \frac{1}{r_o} \right]^{-1} \quad \text{--- (1a)}$$

with,

$$Z_{VCO} = r_{VCO} \parallel \frac{1}{sC_{decap}}. \quad \text{--- (1b)}$$

From eqn (1a) it can be concluded that with a high gain-bandwidth regulator (high $A(s)g_m$) the variations in the positive supply are suppressed on the differential VCO control voltage.

Similarly, deriving the effect from V_{ngnd} results in

$$V_c - V_{ngnd} = V_{ngnd} \left[\frac{1}{Z_{VCO}} \left(\frac{1}{Z_{VCO}} + A(s)g_m + \frac{1}{r_o} \right)^{-1} - 1 \right]. \quad \text{--- (2)}$$

Here the VCO conductance, $1/Z_{VCO}$, has a strong impact, with a large amount of decoupling capacitance resulting in V_c and V_{ngnd} undergoing similar variations, and hence high differential VCO control voltage noise suppression. However, if the decoupling capacitance is insufficient to yield a high VCO conductance, a significant amount of V_{ngnd} can appear on the differential VCO control voltage.

As earlier alluded to, regulator bandwidth plays an important role, with the amplifier pole location relative to the regulator output pole determining the power supply rejection (PSR) characteristics. If the amplifier pole is dominant, which is the case in conventional simple regulators (a single stage op-amp with a large PMOS current source) due to the output current source size, the supply-noise transfer function displays a peak after the amplifier pole (Fig. 3). While making the regulator output pole dominant reduces peaking, this can be difficult to implement due to the feedback loop gain reducing the regulator output impedance; necessitating both significant current to reduce the amplifier output impedance and a large regulator output capacitance for adequate pole separation.

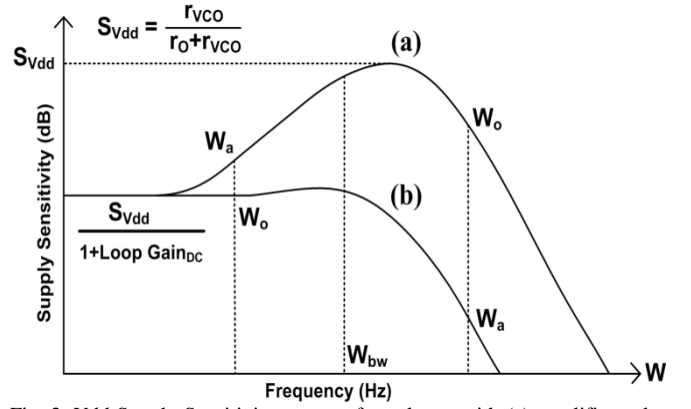


Fig. 3. Vdd Supply Sensitivity curves of regulators with (a) amplifier pole as dominant pole (b) output pole as dominant pole

One solution to make the regulator output pole dominant with reasonable power and area consumption is the replica based regulator introduced in [1] and extended in [2], [3]. The regulation loop consists of the superposition of the replica and the load arms weighed appropriately. This gives good power supply rejection over a wide range of frequencies while maintaining regulator loop stability with a lesser value of decoupling capacitance. A simplified block diagram of a replica based regulator system is shown in Fig. 4.

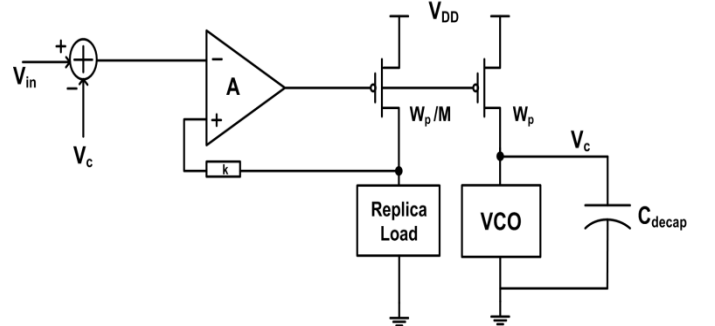


Fig. 4. Replica based regulator

The regulation loop consists of both the replica and load voltages weighed appropriately by a factor 'k'. This gives better control over the loop dynamics and allows us to use a reasonable size of decoupling capacitor to make the output pole dominant and increase the PSR bandwidth.

III. DUAL SUPPLY REGULATION

Analysis in the previous section revealed that single supply regulation is not sufficient to suppress noise from the negative supply without significant decoupling capacitance. An alternative is to use regulation for the negative supply as well. Fig. 5 shows a simplified model of dual regulation applied to a VCO where V_{cp} & V_{cn} are the regulated supply voltages to the VCO. V_{cp} and V_{cn} can either be generated from a differential loop filter [4] or V_{cn} can be a fixed voltage derived from a low drop out regulator with V_{cp} being generated from the loop filter.

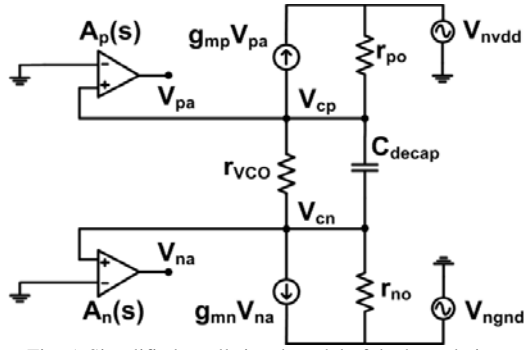


Fig. 5. Simplified small signal model of dual regulation

In order to derive the effect of Vdd and Gnd noise on V_{cp} - V_{cn} respectively, by superposition

$$V_{cp} - V_{cn} = \frac{V_{nvdd}}{r_{po}} \left[\frac{2}{Z_{VCO}} + A_p(s)g_{mp} + \frac{1}{r_{po}} \right]^{-1} \quad \text{--- (3a)}$$

$$V_{cp} - V_{cn} = \frac{V_{nvngnd}}{r_{no}} \left[\frac{2}{Z_{VCO}} + A_n(s)g_{mn} + \frac{1}{r_{no}} \right]^{-1} \quad \text{--- (3b)}$$

The above equations have been derived with a simplifying assumption that the loop gains of the Vdd and Gnd regulation loops are equal. Ideally, the variations on the two supply rails are eliminated totally if $A(s)g_m$ is high and the decoupling capacitance can be reduced drastically. However, the supply noise suppression is still limited by the simple regulator's bandwidth constraints. Thus, in order to suppress the supply noise with a further reduction in decoupling capacitance, the replica-based dual-supply regulation architecture shown in Fig. 6 is proposed.

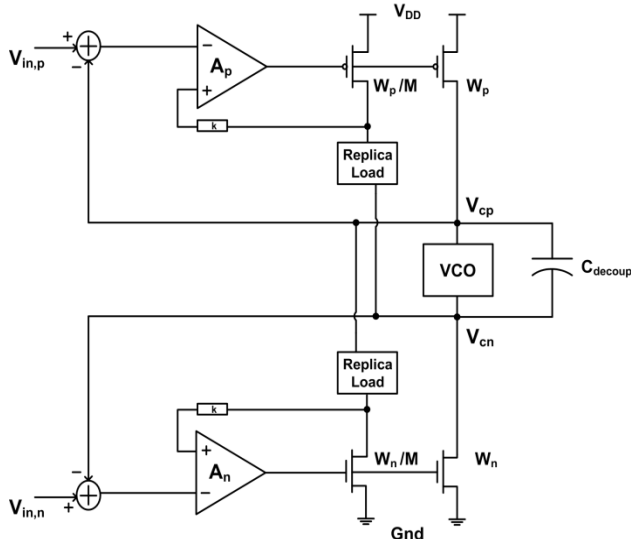


Fig. 6. Replica-based dual supply regulation

In this proposed architecture both the regulators are coupled through the VCO and replica loads, with the negative-supply regulator replica load terminated to the positive-supply regulator output, and vice-versa. This allows the replica load impedance to track the VCO impedance, minimizing the

regulators' voltage offset and maintaining optimal supply rejection.

Fig. 7 shows the simulated power supply rejection at the VCO control nodes ($V_{cp} - V_{cn}$) as a function of the decoupling capacitor for different regulation schemes with noise injected on both supply rails. For the proposed replica-based dual-supply regulated architecture, both the bandwidth extension offered by replica-load topology and the increased coupling of the VCO differential supplies with the replica loads terminated at opposite regulator outputs allow for an improvement of over 20dB in power supply rejection for a given decoupling capacitance. The PSRR starts increasing beyond 100pF, where the RC filter formed by the output impedance of the load current source, VCO impedance and the decoupling capacitance, has its cutoff and starts attenuating the applied noise of 20MHz. For higher capacitances, the PSRR increases steeply for all the regulators because of the output RC filter. It should also be noted that using a triple well process where the bulks of the NMOS transistors can be connected to their sources, gives an improvement of about 2dB in the PSRR.

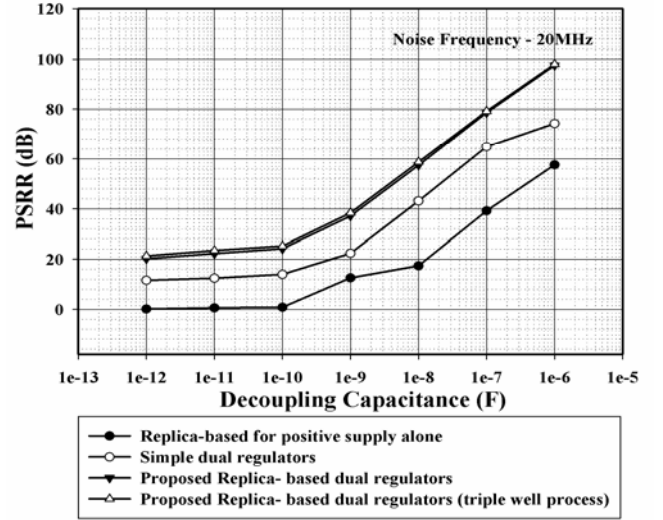


Fig. 7. Simulated PSRR @ V_c as a function of decoupling capacitance

IV. DUAL SUPPLY REGULATED PLL

While the VCO is the most supply noise sensitive block in a PLL, it is not the only one that contributes to output jitter. The other blocks in a PLL such as the Phase/Frequency detector, Charge Pump and Divider are also susceptible to supply noise and contribute to output jitter. Thus, the proposed dual-supply regulation technique is extended to the other loop blocks, with the complete PLL block diagram shown in Fig. 8.

The proposed regulator architecture was designed in tandem with the PLL loop characteristics to reduce the jitter caused by supply noise while keeping the decoupling capacitance as minimum as possible. In order to ensure that the positive & negative supplies track each other, both the regulators are made dependent on each other. The replica load in the positive supply regulator is terminated to the regulated output of the negative supply regulator and vice versa. This allows the regulators to track the variations in either of them and a

reasonable size of decoupling capacitor can be used to keep the differential supply voltage clean.

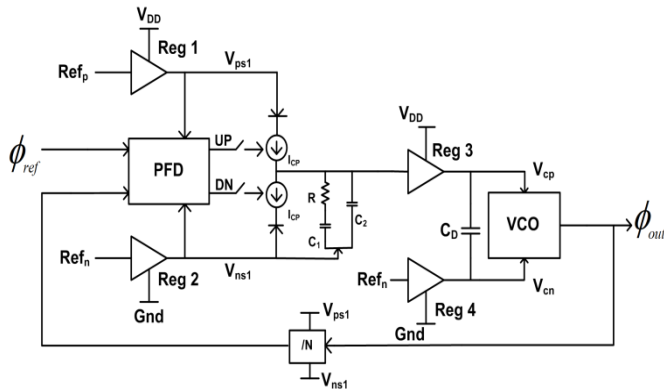


Fig. 8. PLL with dual supply regulation

The power supply for the VCO is handled by a separate regulator pair in order to ensure that any supply variations that might be introduced by the divider, which is a digital block does not get coupled to the VCO. The prototype schematics were designed in a standard (non-triple well) 90nm CMOS process operating on a 1.2V supply voltage. The reference voltages Ref_p & Ref_n are 1V and 0.2V, respectively and are assumed to be clean. It is also assumed that the bandgap reference voltages used for the regulators are clean. They can also be derived from the VCO control voltage which serves as the reference to the regulator in the VCO control path [5].

In order to measure the supply noise sensitivity, tones of amplitude 50m Vpk-pk with different phase content were injected into both the supply rails and the jitter performance was measured. A comparison of supply noise sensitivities of the different regulation schemes in terms of rad/V for a decoupling capacitance of 130pF is shown in Fig. 9. While the single supply replica-based regulator has poor supply sensitivity, the use of dual simple regulators improves the supply sensitivity at low frequencies. However, the simple regulators utilize more than ten times the current used in the replica based regulators to achieve stability for the same output capacitance leading to a total power consumption of 20mW in the PLL. The proposed replica-based dual supply regulation technique achieves a worst case supply sensitivity of 1.6 rad/V, compared to the 9.1 rad/V achieved in the single supply regulator case for the same decoupling capacitance. It is important to note that the replica load of the positive supply regulator must be terminated to the regulated output of the negative supply regulator and vice versa. Failing to do so would degrade the performance as shown in the last curve of Fig. 9. The total power consumption of the proposed replica based dual supply regulated PLL is 11mW with the VCO consuming 5mW of power. The use of this replica-based dual regulation scheme would allow us to reduce the decoupling capacitance by more than twice than in a single supply regulation scheme as seen by the curve with 65pF decoupling capacitance for the proposed technique.

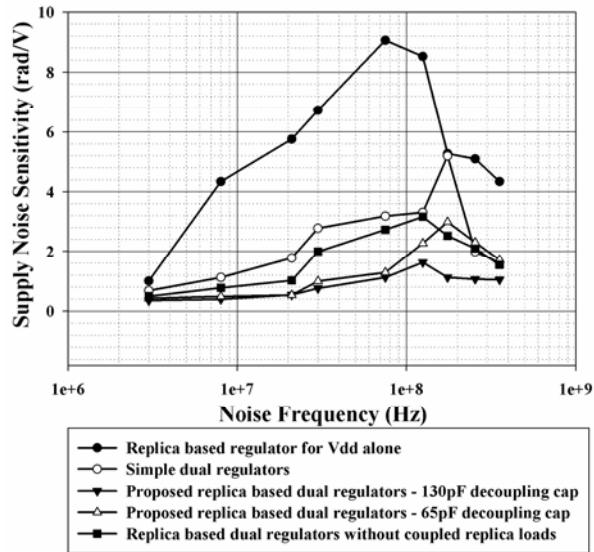


Fig. 9. Simulated Supply noise sensitivity of different regulation schemes

V. CONCLUSION

This paper compares supply regulation techniques for phase locked loops. Analysis and simulation results show that single-supply regulator architectures rely upon replica-based regulators and significant decoupling capacitance to achieve adequate supply sensitivity and jitter performance. The proposed dual-supply regulation architecture actively attenuates negative-supply noise and allows for a dramatic reduction in decoupling capacitance. However, this architecture is still susceptible to bandwidth limitations of simple regulator topologies. Employing replica-based regulators in this improved architecture allows for further performance gains, with reduced supply noise sensitivity, power, and the potential to employ less than half the decoupling capacitance relative to simple regulator topologies.

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