ADVANCE PROGRAMME

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DATE 19

Design, Automation and Test in Europe

25–29 MARCH 2019, FLORENCE, ITALY

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AutoCAD & Inventor Magazin covers more than just IT subjects - we report on all aspects of professional life that are important for constructing engineers and planners. We focus especially on innovations in drive technology, automation technology, connectivity, construction components, fluid technology, electrical engineering and materials.

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Chip Design covers all of the technical challenges and implementation options engineers face in the development and manufacture of today's complex integrated circuits. Chip Design is the only media network dedicated to the advanced IC Design market. Visit www.chipdesignmag.com to stay informed about the latest developments in chip modeling, architecture, design, test and manufacture, from EDA tools to digital and analog hardware issues. The System Level Design and Low Power Engineering Portals offer focused editorial content you won't want to miss. And, be sure to visit www.eecatalog.com for valuable information about all of Extension Media's outstanding technology resources.

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www.eandtmagazine.com

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www.elinor.se

Sensors

Sensors (ISSN 1424-8220; CODEN: SENSC9) is an open access journal published monthly online by MDPI. Sensors devotes to fast publication of the latest achievements of technological developments and scientific research in the huge area of physical, chemical and biochemical sensors, including remote sensing and sensor networks. Both experimental and theoretical papers are published, including all aspects of sensor design, technology, proof of concept and application. Sensors organizes special issues devoted to specific sensing areas and application each year.

www.mdpi.com/journal/sensors

WELCOME TO DATE 2019

Dear Colleague,

We proudly present the Advance Programme of DATE 2019. DATE combines the world's favourite electronic systems design and test conference with an international exhibition for electronic design, automation and test, from system-level hardware and software implementation right down to integrated circuit design.

Out of a total of 834 paper submissions received, a large share (38%) is coming from authors in Europe, 28% of submissions are from the Americas, 33% from Asia, and 1% from the rest of the world. This distribution demonstrates DATE's international character, global reach and impact.

For the 22nd successive year, DATE has prepared an exciting technical programme. With the help of 326 members of the Technical Programme Committee who carried out 3276 reviews (mostly four reviews per submission), finally, 202 papers (24%) were selected for regular presentation and 91 additional ones (cumulatively 35%, including all papers) for interactive presentation.

The DATE conference will take place from 25 to 29 March 2019 at the Firenze Fiera in Florence, Italy.

On the first day of the DATE week, five in-depth technical tutorials on the main topics of DATE as well as two hands-on industry tutorials will be given by leading experts in their respective fields. The topics cover Machine Learning for Manufacturing and Test, OpenCL Design Flows for FPGAs, Approximate Computing, Hardware-based Security, and Safety and Security in Automotive, while the hands-on tutorials are on Quantum Computing with IBM Q and Python Productivity for Xilinx Zynq.

During the Opening Ceremony on Tuesday, plenary keynote lectures will be given by Astrid Elbe, Managing Director of Intel Labs Europe, and Jürgen Bortolazzi, Director Driver Assistance Systems and Highly Automated Driving at Porsche. On the same day, the Executive Track offers a series of business panels with executive speakers from companies leading the design and automation industry, discussing hot topics. Furthermore, a talk by Claudio Giorgione, Curator of the Leonardo Department at the National Museum of Science and Technology Milano, will give insight into life and work of Leonardo da Vinci in line with the 500th anniversary of his death, which is celebrated in Florence in 2019.

The main conference programme from Tuesday to Thursday includes 58 technical sessions organized in parallel tracks from the four areas

D – Design Methods & Tools
A – Application Design
T – Test and Dependability
E – Embedded and Cyber-physical Systems

and from several special sessions on Hot Topics, such as Emerging Design Technologies, Design and Test of Secure Systems, IoT Security, Embedded Systems for Deep Learning, Augmented Living and Personalized Healthcare, Robotics and Industry 4.0, as well as results and lessons learned from European projects. Additionally, there are numerous Interactive Presentations which are organized into five IP sessions.

Two Special Days in the programme will focus on areas bringing new challenges to the system design community: Embedded Meets Hyperscale and HPC and Model-Based Design of Intelligent Systems. Each of the Special Days will have a full programme of panels, tutorials and technical presentations and a lunchtime keynote.

Heterogeneous computing with multiple, specialised processors and application-specific accelerators is vital for embedded systems to

Jürgen Teich

Franco Fummi

meet performance, latency, and efficiency targets. The same goals of fast, efficient, and cost-effective processing are also gating factors for the evolution of hyperscale data centre (DC) and high-performance computing (HPC) and Moore's law no longer provides the necessary efficiency gains. The theme of the special day Embedded Meets Hyperscale and HPC is to showcase this confluence of methods and technologies to better understand, how heterogeneous computing is shaping the future of hyperscale DCs and HPC.

The special day on Model-Based Design of Intelligent Systems will explore all that is needed to lift model-based design into the era of intelligent systems. Topics addressed are, among others, model-based design frameworks for IoT systems, model-based machine learning, and application of model-based design in safety-critical and autonomous systems. The special day will also emphasise the upcoming challenges in this domain and invite the DATE community to help overcome them.

To inform attendees on commercial and design-related topics, there will be a full programme in the Exhibition Theatre, which will combine presentations by exhibiting companies, best-practice reports by industry leaders on their latest design projects and selected conference special sessions. Two of the highlights will be a newly created Publisher's Session and a career session called Inspiring Futures, giving companies the opportunity to introduce their work and job portfolios.

The conference is complemented by an exhibition, running for three days (Tuesday – Thursday), including exhibition booths from companies, and collaborative research initiatives including EU project presentations. The exhibition provides a unique networking opportunity and is the perfect venue for industries to meet university professors to foster university programme and especially for PhD students to meet future employers.

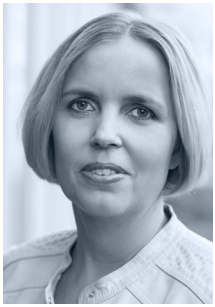
On Friday, ten full-day workshops cover several hot topics from areas like (a) Open Source and Machine Learning in EDA, (b) Emerging Techniques for Memories, Interconnections, and Quantum Computing, (c) Hardware Design, Synthesis, and Approximate Computing, as well as EDA in application domains such as (d) Autonomous Systems and IoT. Furthermore, an International F1/10 Autonomous Racing Demo will take place, supported by IEEE CEDA.

We wish you an exciting and memorable DATE 2019, a successful exhibition visit and an entertaining DATE Party on Wednesday evening.

DATE 2019 General Chair
Jürgen Teich
Friedrich-Alexander-Universität Erlangen-Nürnberg, DE

DATE 2019 Programme Chair
Franco Fummi
Università di Verona, IT

TUESDAY OPENING SESSION



Astrid Elbe

26 March 2019, 0915 – 0950, Auditorium

1.1.1

Working with Safe, Deterministic and Secure Intelligence from Cloud to Edge

Astrid Elbe, Intel Labs Europe, DE

The Internet of Things (IoT) will be the largest revolution in the data economy. At Intel, we understand the exponential power of data, and we're making it practical and economical to put it to work from the edge to the cloud. Intel® technologies purpose-built for IoT deliver optimized performance at every point, practical ways to use artificial intelligence, broad connectivity support, and a built-in foundation of functional safety, time determinism and security to help protect and make dependable your data and systems. Proven solutions from our partner ecosystem can reduce the time, cost, and risk of IoT deployments. By harnessing the massive flood of data generated by connected things—and using it to gain actionable insights—we'll accelerate business transformation to a degree never seen before.

Managing services and infrastructure at the edge is a complex balancing act that has to meet much more demanding timing and dependability constraints and requires vastly more speed and precision than in a conventional cloud data center. Satisfying the competing objectives of stringent Quality of Service (QoS) and workload consolidation in this complex IoT environment requires new approaches and advancements. Virtualization alone does not deliver the full potential for this IoT transformation. E.g. for challenging industrial workloads an automatic and self-managing approach will be needed.

Jürgen Bortolazzi

26 March 2019, 0955 – 1030, Auditorium

1.1.2 Assisted and Automated Driving

Jürgen Bortolazzi, Porsche, DE

Since the introduction of Park Distance Control and Adaptive Cruise Control in the Mid 2000s, PORSCHE follows a systematic strategy to adapt driver assistance and automated driving to their product lines. There is no contradiction to the philosophy of a sports car: customers that enjoy driving on their own in case of appropriate traffic conditions expect significant ease of driving in stressful, time-consuming situations like traffic jams, or heavily occupied parking spaces. Furthermore, new functionalities like the predictive Innodrive system enabling efficient cruise control based on sophisticated planning algorithms provides a perfect contribution to the PORSCHE Intelligent Performance strategy.

Although the common discussion focuses on the higher levels of automation from SAE Level 3 to Level 4, at least for the next decade Level 1 and 2 systems will play a significant role being the technological state-of-the-art for a majority of cars. Therefore, PORSCHE focuses on increasing the performance and functionality of Level1/2 driver assistance system in parallel to participating in development programs to enable Level3/4 automated driving. This offers the opportunity to systematically build the necessary competency both in the technological fields of sensing, sensor fusion, planning and control as well as the necessary processes, methods and tools that are mandatory to develop, approve and release higher level automated systems. Systems Engineering has to be combined with approaches to process very large amounts of data whereas traditional random road based testing has to be replaced by a combination of virtual and systematic real world testing. Last but not least, a new end-to-end EE architecture is necessary to provide the seamless integration of the vehicle into an IT based service infrastructure.

TUESDAY LUNCHTIME KEYNOTE

Claudio Giorgione

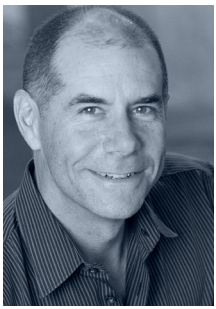
26 March 2019, 1350 – 1420, Room 1

3.0

Leonardo da Vinci, Humanism and Engineering between Florence and Milan

Claudio Giorgione, Curator, Museo Nazionale della Scienza e della Tecnologia Leonardo da Vinci, Milano, IT

The machines and mechanical elements drawn by Leonardo through the course of his itinerary as engineer and technologist belong to the most disparate fields, highlighting his curiosity about the technological culture of his times. Just as for the other sectors of his activity, the first machines depicted by Leonardo follow in the tradition of the Renaissance Florentine workshop and are characterized by a practical, empirical approach aimed at resolution of problems progressively as they arose. During his first Milanese period (1482-1499), Leonardo was experimenting with, and refining ever more effective graphical systems of representation, which he would proceed in applying also to other sectors, like anatomy, architecture, and military engineering. Sections, prospect views, and transparent views were used to decompose machines into their constituent elements, finding solutions for automating and rendering more efficient the existing traditional mechanisms, or for conceiving completely new mechanisms. Leonardo moved, particularly in the 1490s, from documentation of practical problems to a more theoretical analysis of the principles regulating the functioning of machines, from the study of mechanical elements to their inter-relation. The studies on friction and on motion in general are to be inserted into this perspective, which led him to the idea of compiling a treatise on mechanics, based on the analysis of mechanisms and gears, the so-called “elementi macchinali”.



David Pellerin

27 March 2019, 1345 – 1420, Room 1

7.0

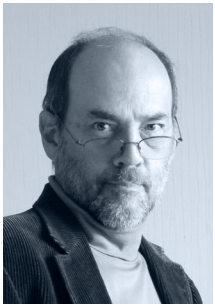
Heterogeneous, High Scale Computing in the Era of Intelligent, Cloud-Connected Devices

David Pellerin, Amazon, US

Rapid advances in connected devices, coupled with machine learning and "data lake" methods of advanced analytics, have led to an explosion in demand for non-traditional, highly scalable computing and storage platforms. This increasing demand is being seen in the public cloud as well as in cloud-connected IoT edge devices. AI/ML is at the heart of many the newest, most advanced analytics and IoT applications, ranging from robotics and autonomous vehicles, to cloud-connected products such as Alexa, to smart factories and consumer-facing services in the financial and healthcare sectors. In support of these important workloads, alternative methods of computing are being deployed in the cloud and at the edge. These alternative, heterogeneous computing methods include CPUs, GPUs, FPGAs, and other emerging acceleration technologies. This talk presents examples of such use-cases within Amazon, as well examples of how Amazon customers increasingly rely on AI/ML, accelerated using alternative computing methods and coupled with smart, cloud-connected devices to create next-generation intelligent products. The talk will conclude with examples of how cloud-based semiconductor design is being enhanced using these same methods.

Supported by IEEE CEDA

THURSDAY LUNCHTIME KEYNOTE



Edward A. Lee

28 March 2019, 1320 – 1350, Room 1

11.0

A Fundamental Look at Models and Intelligence

Edward A. Lee, University of California, Berkeley, US

Models are central to building confidence in complex software systems. Type systems, interface theories, formal semantics, concurrent models of computation, component models, and ontologies all augment classical software engineering techniques such as object-oriented design to catch errors and to make software more modular and composable. Every model lives within a modeling framework, ideally giving semantics to the model, and many modeling frameworks have been developed that enable rigorous analysis and proof of properties. But every such modeling framework is an imperfect mirror of reality. A computer system operating in the physical world may or may not accurately reflect behaviors predicted by a model, and the model may not reflect behaviors that are critical to correct operation of the software. Software in a cyber-physical system, for example, has timing properties that are rarely represented in formal models. As artificial intelligence gets more widely used, the problem gets worse, with predictability and explainability seemingly evaporating. In this talk, I will examine the limitations in the use of models. I will show that two very different classes of models are used in practice, classes that I call "scientific models" and "engineering models." These two classes have complementary properties, and many misuses of models stem from confusion about which class is being used. Scientific models of intelligent systems are very different from engineering models.

This printed programme is intended to provide delegates with an easy reference document during their attendance at DATE 2019. Full conference information including all technical programme details, information on awards, conference registration costs, information about accommodation, travel offers and social events is available on the conference website **www.date-conference.com**

Dates and Venue

The conference will take place from 25 to 29 March 2019, at the Firenze Fiera, Florence, IT.

Firenze Fiera
www.firenzefiera.it

Fortezza da Basso
Padiglione Spadolini, lower floor
(Main conference venue
Monday – Friday)
Viale Filippo Strozzi no. 1.
50123 Florence, IT

Palazzo dei Congressi
Auditorium
(Opening Session
Tuesday morning)
Piazza Adua 1
50123 Florence, IT

The accompanying exhibition is scheduled from 26 to 28 March 2019, and will take place in the Exhibition Area of the conference venue, which also hosts the coffee breaks.

Online Programme

The full technical conference programme is also available on the website **www.date-conference.com** where you will be able to view the entire details of the programme and plan your attendance in advance.

Internet Access

Free wireless internet access is available on-site throughout the whole congress center during the entire DATE week. The WLAN login code will be provided at the registration desk upon arrival.

Proceedings

The conference proceedings are available for download on-site through the DATE-WLAN for every fully registered conference delegate at the following link: www.date-conference.com/proceedings.

WHOVA Conference App

The Whova app can be downloaded via the following link or in the Apple/Google stores for free: https://whova.com/download Please install the app and search for the conference **“DATE 2019”**
→ Password: “DATE”

GENERAL INFORMATION

A browser version can be accessed at
https://whova.com/webapp/e/date_201903/

Online Conference Evaluation via the WHOVA App ("survey" button): Every fully registered delegate, who completes the online conference evaluation via the app, will receive one of the exclusive DATE collector mugs at the registration desk (when showing the confirmation page).

Coffee Break in the Exhibition Area

On all conference days (Tuesday to Thursday), coffee and tea will be served during the coffee breaks at the below-mentioned times in the Exhibition Area in the Padiglione Spadolini of Fortezza da Basso.

Lunch Break (Lunch Area)

On all conference days (Tuesday to Thursday), a seated lunch (lunch buffet) will be offered in the Lunch Area to fully registered conference delegates only. There will be a lunch voucher control at the entrance to the lunch break area.

Tuesday, 26 March 2019

Coffee Break	1030 – 1130
Lunch Break	1300 – 1430
Keynote Lecture in "Room 1"	1350 – 1420
Coffee Break	1600 – 1700

Wednesday, 27 March 2019

Coffee Break	1000 – 1100
Lunch Break	1230 – 1430
Keynote Lecture in "Room 1"	1345 – 1420
Coffee Break	1600 – 1700

Thursday, 28 March 2019

Coffee Break	1000 – 1100
Lunch Break	1230 – 1400
Keynote Lecture in "Room 1"	1320 – 1350
Coffee Break	1530 – 1600

Welcome Reception & PhD Forum Monday, 25 March 2019

hosted by EDAA, ACM SIGDA, and IEEE CEDA

All registered conference delegates and exhibition visitors are kindly invited to join the DATE 2019 Welcome Reception & subsequent PhD Forum, which will take place on Monday, 25 March 2019, from 1800 – 2100 in the Lunch Area of the conference venue.

The PhD Forum of the DATE Conference is a poster session and a buffet style dinner hosted by the European Design Automation Association (EDAA), the ACM Special Interest Group on Design Automation (SIGDA), and the IEEE Council on Electronic Design Automation (CEDA). The purpose of the PhD Forum is to offer a forum for PhD students to discuss their thesis and research work with people of the design automation and system design community. It represents a good opportunity for students to get exposure on the job market and to receive valuable feedback on their work.

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Exhibition Reception

Tuesday, 26 March 2019

supported by Destination Florence Convention and Visitors Bureau

The Exhibition Reception will take place on Tuesday, 26 March 2019, from 1830 to 1930 in the Exhibition Area of the conference venue, where free drinks for all conference delegates and exhibition visitors will be offered.

DATE Party | Networking Event

Wednesday, 27 March 2019

The DATE Party traditionally states one of the highlights of the DATE week. As one of the main networking opportunities during the DATE week, it is a perfect occasion to meet friends and colleagues in a relaxed atmosphere while enjoying local amenities. It is scheduled on 27 March 2019, from 1930 to 2300.

As in 2018, the DATE Party will again feature the awards presentation of the Best Paper Awards and Best IP Award.

This year, it will take place at Palazzo Borghese, which is located in the heart of Firenze and is a beautiful example of neoclassic architecture. It belonged to Prince Camillo Borghese, who took temporary residence here after his marriage to Pauline Bonaparte (sister of Napoleon). The rich Prince renovated the building on the occasion of the wedding between Grand Duke Ferdinand III and Princess Maria Ferdinanda of Saxony in May 1821, commending the work to the young architect Gaetano Baccani. The inauguration party was on the 31 January 1822, and the Florentine nobles were really surprised at such magnificent work: marbles, paintings, and antique furniture gave notoriety to Baccani and the people's affection to the Prince because, with his request, he had given jobs to many different artisans.
Nowadays Palazzo Borghese, still maintaining the ancient splendor and pomp, is located close to the city center and will offer a special setting for the DATE Party 2019.

Please kindly note that it is not a seated dinner.

All delegates, exhibitors and their guests are invited to attend the networking event. Please note that entrance is only possible with a valid party ticket. Each full conference registration includes a ticket for the DATE Party (which needs to be booked during the online registration process though). Additional tickets can be purchased on-site at

the registration desk (subject to availability of tickets). Price for extra ticket: 70 € per person.

Route description

→ https://www.palazzoborghese.it/en/contacts/

The Palazzo Borghese is located within the restricted traffic area (Zona a traffico limitato – ZTL) of Florence, which has been created to protect the historic city centre from excessive traffic. Hence, the best way to get to the Palazzo is by walking through the historic centre.

Walking distance:
25 minutes / ~2 km from Fortezza da Basso

Interactive Presentations
(sponsored by the Cadence Academic Network)

Interactive presentations allow presenters to interactively discuss novel ideas and work in progress, which may require additional research work and discussion, with other researchers working in the same area. Interested attendees can walk around freely and talk to any author they want in a vivid face-to-face format. IP presentations will also be accompanied by a poster. Each IP will additionally be introduced in a relevant regular session prior to the IP Session in a one-minute presentation.
To give an overview, there will be one central projection displaying a list of all the presentations going on at the same time in the IP area. Interactive Presentation (IP) Sessions will be held in the Poster Area in 30-minute time slots on the following days:

Tuesday, 26 March 2019

IP Session 1	Poster Area	1600 – 1630

Wednesday, 27 March 2019

IP Session 2	Poster Area	1000 – 1030
IP Session 3	Poster Area	1600 – 1630
Presentation of the Best IP Award	during the DATE Party (Palazzo Borghese)	approx. 2100

Thursday, 28 March 2019

IP Session 4	Poster Area	1000 – 1030
IP Session 5	Poster Area	1530 – 1600

cadence®
ACADEMIC NETWORK

Co-Chairs:
Giovanni De Micheli, EPF Lausanne, CH
Marco Casale-Rossi, Synopsys, IT

DATE 2019 will again feature an Executive Track of presentations by leading industry and academia representatives. This one-day program will be held on Tuesday, 26 March, the first day of the DATE conference immediately after the Opening Session and will run in parallel to the technical conference tracks. It will be comprised of two panels, a lunch keynote and a hot topic session.

2019 marks the 500th anniversary of Leonardo da Vinci's death and the lunch keynote by Dr. Claudio Giorgione, Curator of the Leonardo Department of the National Museum of Science and Technology, Milan, Italy, will provide an overview of Leonardo's many contributions to engineering between Florence and Milan.

The panels gather a unique group of experts from all over the world to discuss the next wave of innovations that will fuel applications such as 5G, AI, ADAS, HPC, and IoT. The hot topic session will offer new perspectives about the future of test, with a special focus on emerging technologies and applications.

This year's Executive Track should offer prospective attendees valuable information about the vision and roadmaps of leading companies and research institutions from a business and technology point-of-view.

2.1 Executive Panel: Life After CMOS

Chair: G. Dan Hutcheson, VLSI Research, US

→ See Page 41

3.0 LUNCHTIME KEYNOTE: Leonardo da Vinci, Humanism and Engineering between Florence and Milan

Claudio Giorgione, Curator, Museo Nazionale della Scienza e della Tecnologia Leonardo da Vinci, Milano, IT

→ See Page 8

3.1 Executive Panel: Semiconductor IP, Surfing the Next Big Wave

Chair: Raul Camposano, Sage Design Automation, US

→ See Page 47

4.1 Executive Session: The Future of Test

Chair: Subhasish Mitra, Stanford University, US

→ See Page 55

Embedded meets Hyperscale and HPC

Co-Chairs:
Christoph Hagleitner, IBM Research Zurich, CH
Christian Plessl, Paderborn University, DE

Heterogeneous computing with multiple, specialized processors and application-specific accelerators is vital for embedded systems to meet performance, latency, and efficiency targets. The same goals of fast, efficient, and cost-effective processing are also gating factors for the evolution of hyperscale data center (DC) and high-performance computing (HPC) and Moore's law no longer provides the necessary efficiency gains. Hence, we can witness a spread of technologies pioneered in embedded systems to hyperscale DCs and HPC systems, e.g., the use of specialized computing resources, massive parallelism, model-driven and domain-specific programming, task models, co-scheduling, and others. The theme of this special day is to highlight this confluence of methods and technologies to better understand, how heterogeneous computing is shaping the future of hyperscale DCs and HPC.

5.1 Special Day Session: Heterogeneous Computing in the Datacenter and in HPC

→ See Page 60

6.1 Special Day Session: Near-memory computing

→ See Page 67

7.0 LUNCHTIME KEYNOTE: Heterogeneous, High Scale Computing in the Era of Intelligent, Cloud-Connected Devices

→ See Page 9

7.1 Special Day Session: Tools and Runtime Systems

→ See Page 73

8.1 Special Day Panel: What can HPC and hyperscale learn from embedded computing

→ See Page 80

Model-Based Design of Intelligent Systems

Co-Chairs:
Marc Geilen, Eindhoven University of Technology, NL
Sander Stuijk, Eindhoven University of Technology, NL
Patricia Derler, National Instruments, US

The complexity of today's cyber-physical systems is already enormous, but the rise of intelligent systems will further accelerate the design complexity. Good models and associated design processes are needed to keep the development under control and deliver high quality systems in increasingly shorter time frames. Model-based design places models at the centre of the development cycle. This methodology has been successfully employed to develop embedded systems, starting from well-defined, analyzable models, from which software and hardware realizations can be generated automatically. This special day will explore all that is needed to lift model-based design into the era of intelligent systems. Topics addressed are, among other things, model-based design frameworks for IoT systems, model-based machine learning, and application of model-based design in safety-critical and autonomous systems. The special day will also highlight the upcoming challenges in this domain and invite the DATE community to help overcome them.

9.1 **Special Day Session: Experiences from the trenches, model-based design at work**

→ See Page 86

10.1 **Special Day Session: Hot topic: Model-Based Machine Learning**

→ See Page 93

11.0 **LUNCHTIME KEYNOTE: A Fundamental Look at Models and Intelligence**

→ See Page 10

11.1 **Special Day Session: MBD of Cyber-Physical Systems**

→ See Page 98

12.1 **Special Day Session: MBD of Safe and Secure Systems**

→ See Page 104

SPECIAL & EU SESSIONS

Special Session Chairs:
Andreas Herkersdorf, Technische Universität München, DE
Tulika Mitra, National University of Singapore, SG

DATE 2019 offers a collection of excellent special sessions organized by leading experts on topics that are of general interest and are complementary to the regular paper session. The range of topics include superconductive electronics, flexible electronics, quantum computers, 3D sensors, heterogeneous processors, open-source hardware, safety-critical applications, system-on-chip verification, graph analytics, and rebooting computing models.

European Projects Chair:
Martin Schoeberl, Technical University of Denmark, DK

2.3 Special Session: Circuit design and design automation for flexible electronics

Chair: Jamil Kawa, Synopsys, US

→ See Page 42

3.2 Special Session: Smart Resource Management and Design Space Exploration for Heterogenous Processors

Chair: Petru Eles, Linköping University, SE
Co-Chair: Sudeep Pasricha, Colorado State University, US

→ See Page 48

4.8 Embedded Tutorial: Paving the Way for Very Large Scale Integration of Superconductive Electronics

Chair: Jamil Kawa, Synopsys, US

→ See Page 59

5.3 EU Projects

Chair: Martin Schoeberl, Technical University of Denmark, DK

→ See Page 61

5.8 Special Session: The ARAMiS II Project – Efficient Use of Multicore for safety-critical Applications

Chair: Timo Sandmann, Karlsruhe Institute of Technology, DE

→ See Page 64

6.2 Special Session: 3D Sensor – Hardware to Application

Chair: Fabien Clermidy, CEA-Leti, FR
Co-Chair: Pascal Vivet, CEA-Leti, FR

→ See Page 67

8.2 Special Session: Innovative methods for verifying Systems-on-Chip: digital, mixed-signal, security and software

Chair: Ulf Schlichtmann, TUM, DE
Co-Chair: Giovanni De Micheli, EPFL, CH

→ See Page 81

9.3 Special Session: RISC-V or RISK-V? Towards Secure Open Hardware

Chair: Georg Sigl, TUM, DE

→ See Page 87

9.8 Special Session: IBM's Qiskit Tool Chain: Developing for and Working with Real Quantum Computers

Chair: Robert Wille, Johannes Kepler University Linz, AT

→ See Page 90

10.2 Special Session: Enabling Graph Analytics at Extreme Scales: Design Challenges, Advances, and Opportunities

Chair: Partha Pande, Washington State University, US

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11.3 Special Session: Rebooting our Computing Models

Chair: Pierre-Emmanuel Gaillardon, University of Utah, US
Co-Chair: Ian O'Connor, Ecole Centrale of Lyon, FR

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EVENT OVERVIEW

MON

- Monday Tutorials
- Welcome Reception & PhD Forum, hosted by EDAA, ACM SIGDA, and IEEE CEDA

TUE

- Opening Session: Plenary, Awards Ceremony & Keynote Addresses
- Executive Sessions and Keynote
- Technical Conference
- Interactive Presentation IP1
- Vendor Exhibition & Exhibition Theatre
- University Booth
- Fringe Meetings & Co-Located Workshops
- Exhibition Reception
  supported by Destination Florence Convention and Visitors Bureau

WED

- Special Day on "Embedded Meets Hyperscale and HPC" and Keynote
- Interactive Presentations IP2 and IP3
- Technical Conference
- Vendor Exhibition & Exhibition Theatre
- University Booth
- Fringe Meetings & Co-Located Workshops
- DATE Party | Networking Event

THU

- Special Day on "Model-Based Design of Intelligent Systems" and Keynote
- Technical Conference
- Interactive Presentations IP4 and IP5
- Vendor Exhibition & Exhibition Theatre
- University Booth
- Fringe Meetings & Co-Located Workshops

FRI

- Special Interest Workshops
- International F1/10 Autonomous Racing Demo supported by IEEE CEDA

CONTACTS

DATE 2019 Conference Organization
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1300	Tutorial and Conference Registration			
1530–1600	Tutorial Coffee Break			
	Registered participants can attend any tutorial and may move between tutorials during the session.			
	Room 4	Room 9	Room 5	Room 6
1400–1800	M01 Applications of Machine Learning in Semiconductor Manufacturing and Test	M02 OpenCL design flows for Intel and Xilinx FPGAs – common optimization strategies, design patterns and vendor-specific differences	M03 A Comprehensive Analysis of Approximate Computing Techniques: From Component- to Application-Level	M04 Hardware-based Security Solutions for the Internet of Things
	Room 8	Room 7		
1400–1800	M05 Safety and Security in Automotive 2.0 Era	M07 Quantum Computing, intro to IBM Q and Qiskit		
1800–2100	Welcome Reception & PhD Forum hosted by EDAA, ACM SIGDA, and IEEE CEDA, incl. Awards Presentation, Lunch Area			

MONDAY EVENTS

25 March 2019, 1800 – 2100, Lunch Area

FM01

Welcome Reception & PhD Forum, hosted by EDAA, ACM SIGDA, and IEEE CEDA

Organiser: Robert Wille, Johannes Kepler University Linz, AT

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TUESDAY, 26 MARCH 2019

0730	Registration | Speaker's Breakfast, Lunch Area			
0830 – 1030	1.1 Opening Session: Plenary, Awards Ceremony & Keynote Addresses, Auditorium			
1030 – 1130	Exhibition and Coffee Break			
	Track 1	Track 2	Track 3	Track 4
	Room 1	Room 2	Room 3	Room 4
1130 – 1300	2.1 Executive Panel: Life After CMOS	2.2 Physical Attacks	2.3 Special Session: Circuit design and design automation for flexible electronics	2.4 Temperature and Variability Driven Modeling and Runtime Management
1300 – 1430	Exhibition and Lunch Break, Lunch Area 1350 – 1420 3.0 LUNCHTIME KEYNOTE SESSION Room 1			
	Room 1	Room 2	Room 3	Room 4
1430 – 1600	3.1 Executive Panel: Semiconductor IP, Surfing the Next Big Wave	3.2 Special Session: Smart Resource Management and Design Space Exploration for Heterogenous Processors	3.3 Methods and Characterisation techniques for Reliability	3.4 Physical Design, Extraction and Timing Analysis
1600 – 1700	Exhibition and Coffee Break 1600 – 1630 IP1 Interactive Presentations, Poster Area 1615 – 1645 3ps.8 How to Publish Your Research Work, Exhibition Theatre			
	Room 1	Room 2	Room 3	Room 4
1700 – 1830	4.1 Executive Session: The Future of Test	4.2 Reconfigurable Architecture and Tools	4.3 Improving test generation and coverage	4.4 Digital processing with emerging memory technologies
1830 – 1930	EXHIBITION RECEPTION in the Exhibition Area			

TUE Keynote
Opening Session
Executive Session
Special & EU Session
IP Session
Exhibition Theatre

Registration | Speaker's Breakfast, Lunch Area				0730
1.1 Opening Session: Plenary, Awards Ceremony & Keynote Addresses, Auditorium				0830 – 1030
Exhibition and Coffee Break				1030 – 1130
Track 5	Track 6	Track 7	Track 8	
Room 5	Room 6	Room 7	Exhibition Theatre	
2.5 Solutions for reliability and security of mixed-signal circuits	2.6 Computational and resource-efficiency in quantum and approximate computing	2.7 Analysis and optimization techniques for neural networks	2.8 How Electronic Systems can benefit from Machine Learning and from ESD Alliance	1130 – 1300
Exhibition and Lunch Break, Lunch Area 1350 – 1420 3.0 LUNCHTIME KEYNOTE SESSION Room 1				1300 – 1430
Room 5	Room 6	Room 7	Exhibition Theatre	
3.5 Hardware authentication and attack prevention	3.6 Software Solutions for Reliable Memories	3.7 Design Automation of Cyber-Physical Systems	3.8 DFG Collaborative Funding Instruments	1430 – 1600
Exhibition and Coffee Break 1600 – 1630 IP1 Interactive Presentations, Poster Area 1615 – 1645 3ps.8 How to Publish Your Research Work, Exhibition Theatre				1600 – 1700
Room 5	Room 6	Room 7	Exhibition Theatre	
4.5 Hardware Trojans and Split Manufacturing	4.6 Smart Communication Solutions for Automotive Systems	4.7 Energy and power efficiency in GPU-based systems	4.8 Embedded Tutorial: Paving the Way for Very Large Scale Integration of Superconductive Electronics	1700 – 1830
EXHIBITION RECEPTION in the Exhibition Area				1830 – 1930

D-Track A-Track T-Track E-Track

WEDNESDAY, 27 MARCH 2019

0730	Registration | Speaker's Breakfast, Lunch Area			
	Track 1	Track 2	Track 3	Track 4
	Room 1	Room 2	Room 3	Room 4
0830–1000	5.1 Special Day on "Embedded Meets Hyper-scale and HPC" Session: Heterogeneous Computing in the Datacenter and in HPC	5.2 Improving Formal Verification and Applications to GPUs and High-Level Synthesis	5.3 EU Projects	5.4 Emerging technologies for better NoCs
1000 – 1100	Exhibition and Coffee Break 1000 – 1030 IP2 Interactive Presentations Poster Area			
	Room 1	Room 2	Room 3	Room 4
1100 – 1230	6.1 Special Day on "Embedded Meets Hyper-scale and HPC" Session: Near-memory computing	6.2 Special Session: 3D Sensor – Hardware to Application	6.3 When Approximation Meets Dependability	6.4 Hardware support for microarchitecture performance
1230 – 1430	Exhibition and Lunch Break, Lunch Area 1345 – 1420 7.0 LUNCHTIME KEYNOTE SESSION Room 1			
	Room 1	Room 2	Room 3	Room 4
1430 – 1600	7.1 Special Day on "Embedded Meets Hyper-scale and HPC" Session: Tools and Runtime Systems	7.2 Accelerators using novel memory technologies	7.3 CPU and GPU microarchitecture dependability	7.4 Low Power Design: From Highly-Optimized Power Delivery Networks to CNN Accelerators
1600 – 1700	Exhibition and Coffee Break 1600–1630 IP3 Interactive Presentations Poster Area			
	Room 1	Room 2	Room 3	Room 4
1700 – 1830	8.1 Special Day on "Embedded Meets Hyper-scale and HPC" Panel: What can HPC and hyperscale learn from embedded computing	8.2 Special Session: Innovative methods for verifying Systems-on-Chip: digital, mixed-signal, security and software	8.3 Test Preparation and Generation	8.4 Applications of Reconfigurable Computing
1930 – 2300	DATE Party | Networking Event		Palazzo Borghese (incl. Best Paper Awards & Best IP Award)	

WED Keynote

Special Day Session | Special & EU Session | IP Session | Exhibition Theatre

Registration | Speaker's Breakfast, Lunch Area				0730
Track 5	Track 6	Track 7	Track 8	
Room 5	Room 6	Room 7	Exhibition Theatre	
5.5 Hardware Obfuscation	5.6 Energy efficiency in IoT – Edge to Cloud	5.7 Data-driven Acceleration	5.8 Special Session: The ARAMiS II Project – Efficient Use of Multicore for safety-critical Applications	0830–1000
Exhibition and Coffee Break 1000 – 1030 IP2 Interactive Presentations Poster Area				1000 – 1100
Room 5	Room 6	Room 7	Exhibition Theatre	
6.5 System Level Security	6.6 Intelligent Wearable and Implantable Sensors for Augmented Living	6.7 How Secure and Verified is your Cyber-Physical System?	6.8 TETRAMAX: Smart funding for digitalization of Europe's Industry	1100 – 1230
Exhibition and Lunch Break, Lunch Area 1345 – 1420 7.0 LUNCHTIME KEYNOTE SESSION Room 1				1230 – 1430
Room 5	Room 6	Room 7	Exhibition Theatre	
7.5 Reliable and Persistent: From Cache to File system	7.6 Optimization of Smart Energy Systems	7.7 Toward Correct and Secure Embedded Systems	7.8 Inspiring futures! Careers Session @ DATE (part 1)	1430 – 1600
Exhibition and Coffee Break 1600–1630 IP3 Interactive Presentations Poster Area				1600 – 1700
Room 5	Room 6	Room 7	Exhibition Theatre	
8.5 Don't Forget the Memory	8.6 Robotics and Industry 4.0	8.7 Embedded hardware architectures for deep neural networks	8.8 Inspiring futures! Careers Session @ DATE (part 2)	1700 – 1830
DATE Party | Networking Event		Palazzo Borghese (incl. Best Paper Awards & Best IP Award)		1930 – 2300

D-Track A-Track T-Track E-Track

THURSDAY, 28 MARCH 2019

0730	Registration | Speaker's Breakfast, Lunch Area			
	Track 1	Track 2	Track 3	Track 4
	Room 1	Room 2	Room 3	Room 4
0830–1000	9.1 Special Day on "Model-Based Design of Intelligent Systems" Session: Experiences from the trenches, model-based design at work	9.2 High-Level Synthesis	9.3 Special Session: RISC-V or RISK-V? Towards Secure Open Hardware	9.4 Where do NoC and Machine Learning meet?
1000 – 1100	Exhibition and Coffee Break 1000 – 1030 IP4 Interactive Presentations Poster Area			
	Room 1	Room 2	Room 3	Room 4
1100 – 1230	10.1 Special Day on "Model-Based Design of Intelligent Systems" Session: Hot topic: Model-Based Machine Learning	10.2 Special Session: Enabling Graph Analytics at Extreme Scales: Design Challenges, Advances, and Opportunities	10.3 System-level Dependability for Multicore and Real-time Systems	10.4 Disruptive Technologies Ain't Fake News!
1230 – 1400	Exhibition and Lunch Break, Lunch Area 1320 – 1350 11.0 LUNCHTIME KEYNOTE SESSION Room 1			
	Room 1	Room 2	Room 3	Room 4
1400 – 1530	11.1 Special Day on "Model-Based Design of Intelligent Systems" Session: MBD of Cyber-Physical Systems	11.2 Novel techniques in optimization and high-level modeling of mixed-signal circuits	11.3 Special Session: Rebooting our Computing Models	11.4 Learning Gets Smarter
1530 – 1600	Exhibition and Coffee Break 1530–1600 IP5 Interactive Presentations Poster Area			
	Room 1	Room 2	Room 3	Room 4
1600 – 1730	12.1 Special Day on "Model-Based Design of Intelligent Systems" Session: MBD of Safe and Secure Systems	12.2 The Art of Synthesizing Logic	12.3 Aging, calibration circuits and yield	12.4 Design and Optimization for Low-Power Applications

THU Keynote
Special Day Session | Special & EU Session | IP Session | Exhibition Theatre

Registration | Speaker's Breakfast, Lunch Area				0730
Track 5	Track 6	Track 7	Track 8	
Room 5	Room 6	Room 7	Exhibition Theatre	
9.5 Attacking Memory and I/O Bottlenecks	9.6 Reliability of highly-parallel architectures: an industrial perspective	9.7 Runtime Predictability	9.8 Special Session: IBM's Qiskit Tool Chain: Developing for and Working with Real Quantum Computers	0830–1000
Exhibition and Coffee Break 1000 – 1030 IP4 Interactive Presentations Poster Area				1000 – 1100
Room 5	Room 6	Room 7	Exhibition Theatre	
10.5 SSD and data placement	10.6 Self-adaptive resource management	10.7 Architectures for emerging machine learning techniques	10.8 Europe digitization: Smart Anything Everywhere Initiative & FED4SAE, open calls and success stories	1100 – 1230
Exhibition and Lunch Break, Lunch Area 1320 – 1350 11.0 LUNCHTIME KEYNOTE SESSION Room 1				1230 – 1400
Room 5	Room 6	Room 7	Exhibition Theatre	
11.5 Vitello e Mozzarella alla Fiorentina: Virtualization, Multicore, and Fault-Tolerance	11.6 Design Automation Solutions for Microfluidic Platforms and Tasks	11.7 Extending Scheduling Schemes	11.8 An Industry Approach to FPGA/ ARM System Development and Verification (part 1)	1400 – 1530
Exhibition and Coffee Break 1530–1600 IP5 Interactive Presentations Poster Area				1530 – 1600
Room 5	Room 6	Room 7	Exhibition Theatre	
12.5 System Modelling for Analysis and Simulation	12.6 Trojans and public key implementation challenges	12.7 Emerging Strategies for Deep Neural Network Hardware	12.8 An Industry Approach to FPGA/ARM System Development and Verification (part 2)	1600 – 1730

D-Track A-Track T-Track E-Track

FRIDAY, 29 MARCH 2019

0730 – 0830	Workshop Registration and Welcome Refreshments
1000 – 1030	Coffee Break
1200 – 1300	Lunch Break
1430 – 1500	Coffee Break

0830 – 1730 Room 3	0830 – 1730 Room 2	0830 – 1730 Room 1	0830 – 1730 Room 9	0830 – 1700 Room 5
W01 The 5th International Workshop on Optical/Photonic Interconnects for Computing Systems (OPTICS)	W02 Recent Trends in Memristor Science & Technology	W03 DATE Workshop on Autonomous Systems Design (ASD2019)	W04 6th Workshop on Design Automation for Understanding Hardware Designs (DUHDE6)	W05 AxC: 4th Workshop on Approximate Computing
0845 – 1615 Room 6	0830 – 1730 Room 7	0830 – 1730 Room 10	0830 – 1730 Room 8	0845 – 1730 Room 4
W06 2nd International Workshop on Embedded Software for the Industrial IoT (ESIIT 2019)	W07 Workshop on Machine Learning for CAD	W08 Grand Challenges and Research Tools for Quantum Computing	W09 Quo vadis, Logic Synthesis?	W10 Workshop on Open-Source Design Automation for FPGAs – OSDA

FRIDAY EVENTS

29 March 2019, 1000 – 1500, between Rooms 1 and 4

FM03

International F1/10 Autonomous Racing Demo supported by IEEE CEDA

Organisers:
Paolo Burgio, University of Modena and Reggio Emilia, IT
Marko Bertogna, Modena and Reggio Emilia, IT

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Monday Tutorials Chair:
Marco Platzner, Paderborn University, DE

1300 **Tutorial and Conference Registration**

1400-1530 **Tutorials**

1530-1600 **Coffee Break**

1600-1800 **Tutorials**

1800–2100 **Welcome Reception & PhD Forum**
hosted by EDAA, ACM SIGDA, and IEEE CEDA

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M01 **Applications of Machine Learning in Semiconductor Manufacturing and Test**
Room 4 1400 – 1800

M02 **OpenCL design flows for Intel and Xilinx FPGAs – common optimization strategies, design patterns and vendor-specific differences**
Room 9 1400 – 1800

M03 **A Comprehensive Analysis of Approximate Computing Techniques: From Component- to Application-Level**
Room 5 1400 – 1800

M04 **Hardware-based Security Solutions for the Internet of Things**
Room 6 1400 – 1800

M05 **Safety and Security in Automotive 2.0 Era**
Room 8 1400 – 1800

M07 **Quantum Computing, intro to IBM Q and Qiskit**
Room 7 1400 – 1800

MONDAY, 25 MARCH 2019

M01 Applications of Machine Learning in Semiconductor Manufacturing and Test

Room 4 1400 – 1800

Organisers:
Haralampos-G. Stratigopoulos, Sorbonne Université, CNRS, LIP6, FR
Yiorgos Makris, The University of Texas at Dallas, US

Throughout the lifetime of an integrated circuit, a wealth of data is collected for ensuring its robust and reliable operation. Ranging from design-time simulations to process characterization monitors, and from high-volume specification tests to diagnostic measurements on customer returns, the information inherent in this data is invaluable. Mining this information using machine learning methods has seen intense interest and numerous breakthroughs in recent years. This tutorial seeks to elucidate the utility of machine learning in semiconductor manufacturing and test. Relevant concepts from machine learning will be introduced, agglomerated with current practice, and showcased using industrial data. Recommendations for practitioners will also be given.

1400 – 1420 Introduction and Motivation

Speakers:
Haralampos-G. Stratigopoulos, Sorbonne Université, CNRS, LIP6, FR
Yiorgos Makris, The University of Texas at Dallas, US

Part I will motivate the need, the challenges, and the benefits of using machine learning and will discuss its utility on actual test- and yield-related industrial problems. We will give an abstract representation of problems that can be tackled using machine learning. We will also illustrate the link between machine learning and semiconductor manufacturing and test.

1420 – 1530 Overview of Machine Learning Applications in Semiconductor Manufacturing and Test

Speaker:
Yiorgos Makris, The University of Texas at Dallas, US

Part II will provide a concise and comprehensive overview of applications of machine learning in semiconductor manufacturing and test. For each application, we will define the problem, we will explain how machine learning can come to the rescue, and we will show a case study on industrial datasets. Applications include: alternate test for analog/mixed-signal/RF ICs, test compaction, fault diagnosis, yield learning, post-manufacturing tuning, outlier detection, adaptive test, wafer-level spatial & lot-level spatiotemporal correlation modeling, analog test metrics estimation, neuromorphic on-chip testers, hotspot detection, board-level fault diagnosis, trimming, die inking, pre-silicon verification and post-silicon validation, yield estimation in fab-to-fab migration, yield estimation when transitioning from one design generation to the next.

1530 – 1600 Coffee Break for Tutorials

1600 – 1645 Recommendations for Practitioners

Speaker:
Haralampos-G. Stratigopoulos, Sorbonne Université, CNRS, LIP6, FR

Part III will illustrate the main practical issues when applying machine learning techniques. It will provide several recommendations based on the presenters' own experience in developing several applications in the past. Practical issues that will be discussed include: types of learning machines, feature extraction, feature selection, training and validation processes, dataset preparation, limited and unbalanced datasets, non-stationary datasets, metrics for generalization error, mitigating the generalization error, explainable artificial intelligence.

1645 – 1745 **Selected Applications in Depth**

Speakers:
Haralampos-G. Stratigopoulos, Sorbonne Université, CNRS, LIP6, FR
Yiorgos Makris, The University of Texas at Dallas, US

Part IV will describe in more detail selected applications of machine learning in semiconductor manufacturing and test. We will delve into the following four mainstream applications: alternate test for analog/mixed-signal/RF ICs, adaptive test, yield learning, and hotspot detection. For each application we will discuss the collection of training data, the choice of learning models, the training procedures, etc., and we will provide several cases studies on actual industrial data.

1745 – 1800 **Emerging Applications**

Speaker:
Haralampos-G. Stratigopoulos, Sorbonne Université, CNRS, LIP6, FR

Part V will discuss emerging applications. In particular, we will discuss whether deep learning methods open new opportunities for solving efficiently test and semiconductor manufacturing problems. We will also discuss the "inverse" problem of testing machine learning hardware. In particular, we will discuss to what extent testing machine learning hardware is any different from testing any regular integrated circuit. We will also discuss fault tolerance methods that gain interest thanks to the integration of machine learning hardware in autonomous vehicles and systems.

1800 – 2100 Welcome Reception & PhD Forum

hosted by EDAA, ACM SIGDA, and IEEE CEDA

M02 OpenCL design flows for Intel and Xilinx FPGAs – common optimization strategies, design patterns and vendor-specific differences

Room 9 1400 – 1800

Organiser: Tobias Kenter, Paderborn University, DE

An increasing fraction of new results in the reconfigurable computing domain are obtained with the help of high level synthesis tools. Among the more popular tools are the OpenCL based Xilinx SDAccel and Intel FPGA SDK for OpenCL. Since they are building upon the same programming model and source language, one would hope for portability between different OpenCL based FPGA designs. However, the vast majority of published research is only optimized for one vendor tool and FPGA family. In their dissemination and training activities, both vendors focus on promoting effective design patterns with their respective tools and for their respective hardware.

In this tutorial, we want to broaden that scope and provide training for both tool chains. During two years of PostDoc research, the workshop organizer has gained extensive experience and insights into these tools. This tutorial will contain step by step optimization examples with performance models based on analysis of generated reports and complemented with measurements and profiling data. We will present design patterns that work well for both tools and thus can promote portability of OpenCL based FPGA designs, but also shed light on differences. Based on examples, we will illustrate the central difference in pipelining of nested loops, which has implications on local memory ports, replication and predictability of design space exploration.

1400 – 1440 **OpenCL and FPGA design: common constructs and patterns**
Speaker: Tobias Kenter, Paderborn Center for Parallel Computing, DE

1440 – 1530 **Key differences between Intel FPGA and Xilinx tools: outer loop pipelining, local memory ports and replication**
Speaker: Tobias Kenter, Paderborn Center for Parallel Computing, DE

1530 – 1600 Coffee Break for Tutorials

1600 – 1710 **Simple, yet efficient matrix multiplication designs with OpenCL**
Chair: Tobias Kenter, Paderborn Center for Parallel Computing, DE

- Design example with Xilinx SDAccel
- Design example with Intel FPGA SDK for OpenCL
- Discussion of the used abstraction levels: what do we want the compile to infer, what do we want to express explicitly?

1710 – 1800 **OpenCL FPGA success stories, complex design examples, libraries**
Speaker: Tobias Kenter, Paderborn Center for Parallel Computing, DE

1800 – 2100 Welcome Reception & PhD Forum
hosted by EDAA, ACM SIGDA, and IEEE CEDA

M03 A Comprehensive Analysis of Approximate Computing Techniques: From Component- to Application-Level

Room 5 1400 – 1800

Organisers:
Daniel Menard, INSA Rennes / IETR, FR
Alberto Bosio, INL, FR
Olivier Sentieys, INRIA, FR

A new design paradigm, Approximate Computing (AxC), has been established to investigate how computing systems can be more energy efficient, faster, and less complex. Intuitively, instead of performing exact computation and, consequently, requiring a high amount of resources, AxC aims to selectively relax the specifications, trading accuracy off for efficiency. It has been demonstrated in the literature the effectiveness of imprecise computation for both software and hardware components implementing inexact algorithms, showing an inherent resiliency to errors.

This tutorial introduces basic and advanced topics on AxC. We intend to follow a bottom-up approach: from component, up to application-level. More in detail, we will first present existing approximate computing techniques according to three levels: hardware, data and computation. At hardware level, functional approximation through inexact operators and voltage over-scaling will be detailed. At data level, approximation can be carried-out by using efficient arithmetic, precision scaling, less data or less-up-to-date data. We will present some compile-time results in terms of energy-efficiency, area, performance versus accuracy of computations when using customized arithmetic (fixed-point, floating-point) and also, we will try to derive some conclusions by comparing the different paradigms. At computation level, algorithmic transformations are used to reduce complexity by skipping or approximating parts of the processing. The concepts of loop perforation, early termination, memoïzation, and computation approximation will be detailed.

The second part of the tutorial is dedicated to methods and tools to exploit efficiently approximate computing. First of all, the different approaches to analyze approximation effects on application quality will be described. Then the complex problem of word-length optimization for fixed-point and floating-point is considered. Finally, the different frameworks for design space exploration will be detailed.

The last part of the tutorial is devoted to present how AxC paradigm can be exploited in the context of safety-critical applications. More in particular, the tutorial will show how design efficient and low-cost fault tolerance mechanisms.

THE OUTLINE OF THE PRESENTATION IS AS FOLLOWS

- General introduction Motivations
- Techniques for approximate computing
  - Data level approximation
  - Hardware level approximation
  - Computation level approximation
- Methods and tools for approximate computing
  - Analysis of approximation effect on application quality
  - Word-length optimization for fixed-point and floating-point
  - Design space explorationGeneral introduction Motivations
- Approximate Computing for Safety-Critical Applications
  - Approximate Computing VS Reliability
  - Implement low cost fault tolerant techniques exploiting AxC
  - Results

1800 – 2100 Welcome Reception & PhD Forum
hosted by EDAA, ACM SIGDA, and IEEE CEDA

MONDAY, 25 MARCH 2019

M04 Hardware-based Security Solutions for the Internet of Things

Room 6 1400 – 1800

Organiser and Chair: Basel Halak, University of Southampton, GB
Co-Chair: Maire O'Neill, Queen's University Belfast, GB

The security of the internet of things is one of the major challenges facing both engineers and researcher alike. This technology has led to billions of low power devices to become entrenched in our lives. Reports state that currently 15 billion IoT devices are currently deployed, and deployment is expected to reach 50 billion by the year 2020. This massive deployment of devices has led to significant security concerns. Various attacks have shown weaknesses in IoT infrastructure, with a swarm of light bulbs potentially leaving a city in darkness, rogue devices attacking infrastructure to attacks in critical infrastructure.

This tutorial, a combined effort of four leading international universities in the field of hardware-based IoT security, aims to disseminate the latest research results and state-of-the-art techniques in this field DATE community.

The tutorial will be highly beneficial for both experienced researchers and students considering delving into this topic.

THE TUTORIAL HAS THE FOLLOWING OBJECTIVES:

- To describe the security challenges of internet of things devices
- To explain the basics of attestation techniques for IoT devices
- To explain the principles of lightweight authentications techniques
- To explain the design principles of Physically Unclonable Functions
- To Describe open research problems in the area of designing hardware-security schemes for IoT applications.

1400 – 1405 **Chair Introduction**
Chair: Basel Halak, University of Southampton, GB

1405 – 1445 **Hardware based Lightweight Authentication for IoT Application**
Speaker: Gang Qu, University of Maryland, College Park, US

In many embedded systems and the Internet of Things (IoT) applications, resources like CPU, memory, and battery power are limited that they cannot afford the classic cryptographic security solutions. Meanwhile, the security requirement on these systems/devices is not as high as the traditional secure systems. In this talk, we use authentication as an example to demonstrate how hardware and physical characteristics can help to build lightweight security primitives such as authentication protocols. More specifically, we will report our recent work that utilizes the traditional CMOS, the emerging RRAM technologies, and voltage over scaling (VoS) technique for user and device authentication as well as GPS spoofing detection. These practical approaches are promising alternatives for the classical crypto-based authentication protocols for the embedded and IoT devices in the smart world.

1445 – 1530 **Device Attestation for IoT and Resources-Constrained Systems**
Speaker: Yier Jin, The University of Central Florida, US

In recent years we have seen a rise in popularity of networked devices. As a consequence, a need to ensure secure and reliable operation of these devices has also risen.

Device attestation is a promising solution to the operational demands of embedded devices, especially those widely used in Internet of Things (IoT) and Cyber-Physical System (CPS).

In this tutorial, we summarize the basics of device attestation. We then present a summary of attestation approaches by classifying them based on their functionality and reliability guarantees they provide to networked devices. Lastly, we discuss the limitations and potential issues current mechanisms exhibit and propose new research directions.

1530 – 1600 Coffee Break for Tutorials

1600 – 1645 **Securing IoT Devices using Physically Unclonable Functions**
Speaker: Basel Halak, University of Southampton, GB

Physically Unclonable Functions (PUFs) exploit the intrinsic manufacturing process variations to generate a unique signature for each silicon chip; this technology allows building lightweight cryptographic primitive suitable for resource-constrained IoT devices. The first part of this tutorial provides a comprehensive overview on the design principles of physically unclonable functions and their main evaluation metrics. The second part explains why we need the PUF technology and how to use it to build robust defense mechanisms against emerging security threats facing IoT technologies, in this context, we give specific examples that includes; secure cryptographic keys generation/storage, authentication protocols, and low cost secure sensors. The final part of this tutorial outlines the outstanding security challenges facing PUF technology and their potential countermeasures, including mathematical modelling attacks using machine-learning algorithms, side channel attacks and physical cloning attacks. The tutorial concludes with a summary of learned lessons and directions for the future.

1645 – 1730 **Practical Design Guidelines PUF using FPGA**
Speaker: Maire O'Neill, Queen's University Belfast, GB

A Physical unclonable function (PUF) is a security primitive which enables the extraction of a digital identifier from electronic devices, based on the inherent silicon variation between devices which occurs during the manufacturing process. Many PUF implementations for ASICs and FPGAs have been proposed to date. However, on FPGA they often offer insufficient uniqueness and reliability, and consume excessive FPGA resources. This talk will focus on how to design efficient, lightweight and scalable PUF identification (ID) generator circuits specifically for FPGAs that offer compact designs, high uniqueness and good reliability. It will also discuss the challenges in designing challenge-response PUF circuits on FPGAs, including their vulnerability to machine-learning attacks. This talk will focus on how to design efficient, lightweight and scalable PUF identification (ID) generator circuits specifically for FPGAs that offer compact designs, high uniqueness and good reliability. It will also discuss the challenges in designing challenge-response PUF circuits on FPGAs, including their vulnerability to machine-learning attacks.

1800 – 2100 Welcome Reception & PhD Forum
hosted by EDAA, ACM SIGDA, and IEEE CEDA

MONDAY, 25 MARCH 2019

M05 Safety and Security in Automotive 2.0 Era

Room 8 1400 – 1800

Organiser: Srivaths Ravi, Texas Instruments, IN

Speakers:
Prasanth Viswanathan Pillai, Texas Instruments, IN
Srivaths Ravi, Texas Instruments, IN

The increasing semiconductor consumption has been spurred by a revolution witnessed in the automotive industry. The integration of electronics and networking into conventional automobile driven by infotainment and ADAS a few years back is accelerated by megatrends of EV/HEV, autonomous driving and shared mobility. These trends, termed sometimes as "Automotive 2.0", drive various requirements into the semiconductors being sourced. Of these, safety and security requirements are becoming paramount due to their impact and liability. This tutorial leverages the authors' experiences in driving safety and security as a part of semiconductor development cycles. By breaking down complex system requirements into foundational ones at semiconductor level, the tutorial is intended to provide an accessible treatment of the subject for any semiconductor developer.

1400 – 1420 **Introduction**

PART A: Introduction starts with a brief overview of the top level trends in automotive and semiconductor industries that are driving various design requirements, including the emerging concerns of safety and security.

1420 – 1530 **Automotive Functional Safety I**

PART B: Automotive Functional Safety I is the first of a two part module on automotive functional safety for a semiconductor developer. Using the presenters' experience in leading functional safety compliant chip development and certification, the module examines various aspects of the automotive functional safety standard ISO 26262 and its parent industrial safety standard IEC61508. We start with the foundations of functional safety including key terminology and metrics, safety compliant development process for HW/SW, component and system level safety mechanisms, and qualitative safety analysis.

1530 – 1600 Coffee Break for Tutorials

1600 – 1650 **Automotive Functional Safety II**

PART C: Automotive Functional Safety II is the second of a two part module on automotive functional safety for a semiconductor developer. This module first covers the various techniques that are used in the quantitative safety analysis phase that follows qualitative safety analysis. We then survey the readiness of safety EDA ecosystem today from the eyes of a semiconductor developer. We conclude with emerging functional safety topics of interest and review the key changes in the 2nd edition of ISO26262.

1650 – 1800 **Automotive Security: Moving from Ad-hoc to Standards**

PART D: Automotive Security: Moving from Ad-hoc to Standards is a module crafted to share the latest knowhow from a rapidly evolving domain – automotive security. The module starts with a detailed look at attack surface of an automobile and the various threat "opportunities". Then, we survey the foundational HW/SW mechanisms necessary to secure automotive electronics and also review emerging standards for secure automotive semiconductor development. Finally, we examine the curious relationship of security and safety that designers need to grapple with.

1800 – 2100 Welcome Reception & PhD Forum
hosted by EDAA, ACM SIGDA, and IEEE CEDA

M07 Quantum Computing, intro to IBM Q and Qiskit

Room 7 1400 – 1800

Organiser: Leon Stok, IBM, US

Speakers:
Leon Stok, IBM, US
SheshaShayee Raghunathan, IBM, IN
Robert Perricone, IBM, US

Though early in its development, quantum computing is now available on real hardware via the cloud through IBM Q. This radically new kind of computing holds open the possibility of solving some problems that are now and perhaps always will be intractable for "classical" computers.

In this talk we'll discuss the motivation for quantum computing and the types of problems to which it might be applied. We'll describe the basics of the technology and show where we are in the timeline toward reaching quantum advantage: the point where quantum computing shows demonstrable and significant advantage over classical computers and algorithms.

We'll continue by describing the no-charge IBM Q Experience where more than 90,000 people have used IBM's offerings to learn and experiment with quantum computing.

We will give an hands-on introduction to Qiskit and show how to run several quantum programs on IBM Q and simulator systems.

Feel free to look at: https://qiskit.org for more information.

1800 – 2100 Welcome Reception & PhD Forum
hosted by EDAA, ACM SIGDA, and IEEE CEDA

MAIN CONFERENCE

26 — 28 MARCH 2019

TECHNICAL PROGRAMME

1.1 Opening Session: Plenary, Awards Ceremony & Keynote Addresses

Auditorium 0830 – 1030

Chair: Jürgen Teich, Friedrich-Alexander-Universität Erlangen-Nürnberg, DE
Co-Chair: Franco Fummi, Università di Verona, IT

0830 **Welcome Addresses**

Jürgen Teich
DATE 2019 General Chair

Franco Fummi
DATE 2019 Programme Chair

0845 **Presentation of awards**

2019 EDAA Achievement Award
(Jacob Abraham, University of Texas at Austin, US)

EDAA Outstanding Dissertations Award 2018

DATE Fellow Award
(Jan Madsen, Technical University of Denmark, DK
Jano Gebelein, Goethe-University Frankfurt, DE)

IEEE Fellow Award
(Antun Domic, Synopsys, US
Luca Fanucci, University of Pisa, IT)

IEEE CEDA Service Award
(Jan Madsen, Technical University of Denmark, DK)

IEEE CS TTTC Outstanding Contribution Award
(Jürgen Teich, Friedrich-Alexander-Universität Erlangen-Nürnberg, DE)

0915 **Keynote Addresses**

Working with Safe, Deterministic and Secure Intelligence from Cloud to Edge
Astrid Elbe, Intel Labs Europe, DE

→ See Page 6

Assisted and Automated Driving
Jürgen Bortolazzi, Porsche, DE

→ See Page 7

1030 **Coffee Break** in the Exhibition Area
at Fortezza da Basso, Padiglione Spadolini, lower floor

2.1 Executive Panel: Life After CMOS

Room 1 1130 – 1300

Organisers:
Marco Casale-Rossi, Synopsys, IT
Jamil Kawa, Synopsys, US

Chair: G. Dan Hutcheson, VLSI Research, US

Sixty years ago, Robert Noyce filed U.S. Patent 2,981,877, which marked the birth of the monolithic integrated circuit. Roughly thirty years later, the IC broke the 1-micron barrier — a 100X improvement over Noyce's IC. Today, 7-nanometer is in early manufacturing, and 5-nanometer is under development, marking another 100X improvement. This cannot continue forever: the silicon atom diameter is 2.92 Ångstroms, approximately 0.3 nanometers. Even if we envision the use of atomic layer epitaxy — where we take the cross section of a FET to be that of a single silicon atom source/drain separated by a channel of a single silicon atom vacancy resulting in a handful total available carriers — will it be possible to design and manufacture an IC made of trillions of those transistors in volume? And even if the progress in Moore's law continues relentlessly by going vertical — we have already infringed the second clause of Moore's law: "at the same cost." Yet, the computing and memory requirements of artificial intelligence (AI), biochemistry, medicine, pharmacology, and physics applications greatly exceed the capabilities of current electronics and are unlikely to be met by evolutionary improvements in devices, channel and interconnect materials, or integrated circuit architectures alone. Meeting them means thinking outside the CMOS box. Many are already doing so with circuits based on super-conducting electronics (SCE) and architectures based on quantum computing (QC), where researchers have made significant advances in recent years. In the short term, Josephson junction-based SCE promise to reinvigorate HPC by delivering at least an order of magnitude more performance while using 100-1,000X less power. In the long term, today's foundations for new classes of computers based on the laws of quantum physics — or quantum computers (QC) — may dramatically change the landscape of HPC. They already bring the promise of solving today's intractable problems. This panel, moderated by Dan Hutcheson, brings together some of the industry's greatest thinkers to explore these questions, to color an image of our industry's future, and to go beyond the CMOS box.

Panelists:
Alessandro Curioni, IBM, CH
Antun Domic, Synopsys, US
Mark Heiligman, IARPA, US
Buvna Ayyagari-Sangamalli, AMAT, US

1300 **Lunch Break** in Lunch Area

2.2 Physical Attacks

Room 2 1130 – 1300

Chair: Lejla Batina, Radboud University, NL
Co-Chair: Elif Kavun, University of Sheffield, GB

This session covers state of the art fault analysis techniques such as persistent fault analysis, electromagnetic fault injection, and glitching. In addition, a practical attack is described on a very popular platform together with its corresponding countermeasure. Other topics in this session include the reconfigurability of FPGAs to defend against side-channel attacks and spying on IoT devices' temperature via DRAM.

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1130 **One Fault is All it Needs: Breaking Higher-Order Masking with Persistent Fault Analysis**
Speaker: Shivam Bhasin, Nanyang Technological University, SG
Authors: Jingyu Pan[1], Shivam Bhasin[2], Fan Zhang[3] and Kui Ren[3]
[1]Nanyang Technological University, Zhejiang University, CN; [2]Temasek Laboratories, Nanyang Technological University, SG; [3]Zhejiang University, CN

1200 **Multi-Tenant FPGA-based Reconfigurable Systems: Attacks and Defenses**
Speaker: Krishnendu Chakrabarty, Duke University, US
Authors: Rana Elnaggar[1], Ramesh Karri[2] and Krishnendu Chakrabarty[1]
[1]Duke University, US; [2]NYU, US

1230 **Spying on Temperature using DRAM**
Speaker: Nikolaos Athanasios Anagnostopoulos, TU Darmstadt, DE
Authors: Wenjie Xiong[1], Nikolaos Athanasios Anagnostopoulos[2], André Schaller[2], Stefan Katzenbeisser[2] and Jakub Szefer[1]
[1]Yale University, US; [2]Technische Universität Darmstadt, DE

1245 **Mitigating Power Supply Glitch based Fault Attacks with Fast All-Digital Clock Modulation Circuit**
Speaker: Nikhil Chawla, Georgia Institute of Technology, US
Authors: Arvind Singh[1], Monodeep Kar[2], Nikhil Chawla[1] and Saibal Mukhopadhyay[1]
[1]Georgia Institute of Technology, US; [2]Intel Corporation, US

IPs **IP1-1, IP1-2, IP1-3, IP1-4**

1300 **Lunch Break** in Lunch Area

2.3 Special Session: Circuit design and design automation for flexible electronics

Room 3 1130 – 1300

Organisers:
Jim Huang, Hewlett Packard Labs, US
Mehdi Tahoori, Karlsruhe Institute of Technology (KIT), DE

Chair: Jamil Kawa, Synopsys, US

Flexible electronics is an emerging and fast growing field which can be used in many demanding and emerging application domains such as wearables, smart sensors, and Internet of Things (IoT). There are several technologies, processes and paradigms which can be used to design and fabricate flexible circuits. Unlike traditional computing and electronics domain which is mostly driven by performance characteristics, flexible electronics are mainly associated with low fabrication costs (as they are used even in consumer market) and low energy consumption (as they could be used in energy-harvested systems). While the main advances in this field is mainly focused on fabrication and process aspects, the design and in particular design automation flow, had limited exposure. The purpose of this special session is to bring to the attention of design automation community on some of the key advances in the field of flexible electronics as well as some of the design (automation) aspects, which can hopefully inspire some further attention by design automation community to this fast-growing field.

1130 **Dual-gate self-aligned a-InGaZnO transistor model for flexible circuit applications**
Speaker: Kris Myny, imec, BE
Authors: Florian De Roose, Hikmet Çeliker, Jan Genoe, Wim Dehaene and Kris Myny, imec, BE

1152 **Predictive Modeling and Design Automation of Inorganic Printed Electronics**
Speaker: Jasmin Aghassi-Hagmann, Offenburg University of Applied Sciences / Institute of Nanotechnology at Karlsruhe Institute of Technology, DE
Authors: Farhan Rasheed[1], Michael Hefenbrock[1], Rajendra Bishnoi[1], Michael Beigl[1], Jasmin Aghassi-Hagmann[2] and Mehdi B. Tahoori[1]
[1]Karlsruhe Institute of Technology (KIT), DE; [2]Offenburg University of Applied Sciences / Institute of Nanotechnology at Karlsruhe Institute of Technology), DE

1214 **Process Design Kit and Design Automation for Flexible Hybrid Electronics**
Speaker: Tsung-Ching Jim Huang, Hewlett-Packard Labs, US
Authors: Tsung-Ching Jim Huang[1], Ting Lei[2], Leilai Shao[3], Sridhar Sivapurapu[4], Madhavan Swaminathan[4], Sicheng Li[1], Zhenan Bao[2], Kwang-Ting Cheng[3] and Raymond Beausoleil[1]
[1]Hewlett-Packard Labs, US; [2]Department of Chemical Engineering, Stanford University, US; [3]Department of Electrical and Computer Engineering, University of California, US; [4]School of Electrical and Computer Engineering, Georgia Institute of Technology, US;

1236 **Circuit Design and Design Automation for Printed Electronics**
Speaker: Eugenio Cantatore, Eindhoven University of Technology, NL
Authors: M. Fattori[1], J.A. Fijn[1], L. Hu[1], Eugenio Cantatore[1], Fabrizion Torricelli[2] and Micael Charbonneau[3]
[1]Eindhoven University of Technology, NL; [2]University of Brescia, IT; [3]CEA-LITEN, FR

1300 **Lunch Break** in Lunch Area

2.4 Temperature and Variability Driven Modeling and Runtime Management

Room 4 1130 – 1300

Chair: Marco Domenico Santambrogio, Polytechnic University of Milan, IT
Co-Chair: Ronald Dreslinski Jr, University of Michigan, US

Thermal modelling, hot spot prediction and optimization, and managing temperature variability during run-time are key questions to be answered during system design. This session consists of four regular papers and two IP papers that address these challenges using novel techniques ranging from manufacturing and hardware, all the way up to computational models. Considerations such as lithographic variations, cooling system design, run-time adaptivity are discussed in these papers.

1130 **Hot Spot Identification and System Parameterized Thermal Modeling for Multi-Core Processors Through Infrared Thermal Imaging**
Speaker: Sheldon Tan, University of California, Riverside, US
Authors: Sheriff Sadiqbatcha[1], Hengyang Zhao[1], Hussam Amrouch[2], Joerg Henkel[2] and Sheldon Tan[1]
[1]University of California, Riverside, US; [2]Karlsruhe Institute of Technology, DE

1200 **Litho-GPA: Gaussian Process Assurance for Lithography Hotspot Detection**
Speaker: David Z. Pan, University of Texas, Austin, US
Authors: Wei Ye, Mohamed Baker Alawieh, Meng Li, Yibo Lin and David Z. Pan, University of Texas, Austin, US

1230 **PinT: Polynomial in Temperature Decode Weights in a Neuromorphic Architecture**
Speaker: Scott Reid, Stanford University, US
Authors: Scott Reid, Antonio Montoya and Kwabena Boahen, Stanford University, US

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1245 **Enhancing Two-Phase Cooling Efficiency through Thermal-Aware Workload Mapping for Power-Hungry Servers**
Speaker: Arman Iranfar, EPFL, CH
Authors: Arman Iranfar, Ali Pahlevan, Marina Zapater and David Atienza, EPFL, CH

IPs **IP1-5, IP1-6**

1300 **Lunch Break** in Lunch Area

2.5 Solutions for reliability and security of mixed-signal circuits

Room 5 1130 – 1300

Chair: Georges Gielen, KU Leuven, BE
Co-Chair: Manuel Barragan, TIMA, FR

The session presents techniques to analyse and optimize analog/mixed-signal circuits towards high reliability and security, addressing IR-aware routing, lifetime-aware optimization as well as securing mixed-signal circuits via logic locking.

1130 **IR-aware Power Net Routing for Multi-Voltage Mixed-Signal Design**
Speaker: Mark Po-Hung Lin, National Chung Cheng University, TG
Authors: Shuo-Hui Wang, Yen-Yu Su, Guan-Hong Liou and Mark Po-Hung Lin, National Chung Cheng University, TW

1200 **Generation of Lifetime-Aware Pareto-Optimal Fronts Using a Stochastic Reliability Simulator**
Authors: Antonio Toro-Frias[1], Pablo Saraza-Canflanca[1], Fabio Passos[1], Pablo Martin-Lloret[1], Rafael Castro-Lopez[1], Elisenda Roca[1], Javier Martin-Martinez[2], Rosana Rodriguez[2], Montserrat Nafria[2] and Francisco Vidal Fernandez[1]
[1]Instituto de Microelectrónica de Sevilla, ES; [2]Universitat Autonoma de Barcelona, ES

1230 **MixLock: Securing Mixed-Signal Circuits via Logic Locking**
Speaker: Julian Leonhard, Sorbonne Université, CNRS, LIP6, FR
Authors: Julian Leonhard[1], Muhammad Yasin[2], Shadi Turk[3], Mohammed Thari Nabeel[4], Marie-Minerve Louërat[1], Roselyne Chotin-Avot[1], Hassan Aboushady[1], Ozgur Sinanoglu[4] and Haralampos-G. Stratigopoulos[1]
[1]Sorbonne Université, CNRS, LIP6, FR; [2]New York University, US; [3]Seamless Waves, FR; [4]New York University Abu Dhabi, AE

IPs **IP1-7**

1300 **Lunch Break** in Lunch Area

2.6 Computational and resource-efficiency in quantum and approximate computing

Room 6 1130 – 1300

Chair: Martin Trefzer, University of York, GB
Co-Chair: Lukas Sekanina, Brno University of Technology, CZ

Achieving computational and resource-efficiency is often promised by emerging technologies. This session addresses various aspects of efficiency in the context of quantum and approximate computing. Simulation of quantum computations is very computationally expensive. The first paper shows how a smart utilization of decision diagrams can significantly accelerate this process. Approximate computing is often advocated as an approach enabling to build more resource-efficient computing systems. The second paper of this session deals with an automated circuit approximation method capable of exploiting data distributions observable in the target application. The third paper presents a new application for approximate circuits in the area of wireless sensor networks. Finally, an efficient approximate random dropout technique for training acceleration of neural networks running on GPU is proposed in the fourth paper.

1130 **Matrix-Vector vs. Matrix-Matrix Multiplication: Potential in DD-based Simulation of Quantum Computations**
Speaker: Alwin Zulehner, Johannes Kepler University Linz, AT
Authors: Alwin Zulehner and Robert Wille, Johannes Kepler University Linz, AT

1200 **Automated Circuit Approximation Method Driven by Data Distribution**
Speaker: Lukas Sekanina, Brno University of Technology, CZ
Authors: Zdenek Vasicek, Vojtech Mrazek and Lukas Sekanina, Brno University of Technology, CZ

1230 **Trading Digital Accuracy for Power in an RSSI Computation of a Sensor Network Transceiver**
Speaker: Paul Detterer, Eindhoven University of Technology, NL
Authors: Paul Detterer, Cumhur Erdin, Majid Nabi, Jose Pineda de Gyvez, Twan Basten and Hailong Jiao, Eindhoven University of Technology, NL

1245 **Approximate Random Dropout for DNN training acceleration in GPGPU**
Speaker: Li Jiang, Shanghai Jiao Tong University, CN
Authors: Zhuoran Song, Ru Wang, Dongyu Ru, Zhenghao Peng, Hongru Huang, Hai Zhao, Xiaoyao Liang and Li Jiang, Shanghai Jiao Tong University, CN

IPs **IP1-8, IP1-9, IP1-10**

1300 **Lunch Break** in Lunch Area

2.7 Analysis and optimization techniques for neural networks

Room 7 1130 – 1300

Chair: Sai Pudukot, Georg Mason University, US
Co-Chair: Mohamed Sabry, NTU, SG

This session presents three papers with new approaches to characterize the neural network behavior on edge devices in order to optimize their performance and energy consumption according to the target application.

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1130 **Low-Complexity Dynamic Channel Scaling of Noise-Resilient CNN for Intelligent Edge Devices**
Speaker: Younghoon Byun, Pohang University of Science and Technology (POSTECH), KR
Authors: Younghoon Byun, Minho Ha, Jeonghun Kim, Sunggu Lee and Youngjoo Lee, Pohang University of Science and Technology (POSTECH), KR

1200 **Data Locality Optimization of Depthwise Separable Convolutions for CNN Inference Accelerators**
Speaker: Hao-Ning Wu, National Tsing Hua University, TW
Authors: Hao-Ning Wu and Chih-Tsun Huang, National Tsing Hua University, TW

1230 **A Binary Learning Framework for Hyperdimensional Computing**
Speaker: Mohsen Imani, University of California, San Diego, US
Authors: Mohsen Imani[1], John Messerly[1], Fan Wu[2], Wang Pi[3] and Tajana Rosing[1]
[1]University of California San Diego, US; [2]University of California Riverside, US; [3]Peking University, CN

IPs **IP1-11, IP1-12, IP1-13**

1300 **Lunch Break** in Lunch Area

2.8 How Electronic Systems can benefit from Machine Learning and from ESD Alliance

Exhibition Theatre 1130 – 1300

Organiser: Jürgen Haase, edacentrum, DE

In this session the Electronic System Design Alliance will present their newest initiatives and results. Mentor, a Siemens Business will discuss approaches for application of Machine Learning for designing and producing microelectronics products. IngeniArs will analyze scenarios for realizing smart edge devices by using accelerators for executing Machine Learning and Deep Learning algorithms.

1130 **Machine Learning is Changing the Game for Variability and Characterization and will soon help Analog and Digital Verification**
Speaker: Amit Gupta, Mentor, a Siemens Business, US

1200 **Machine Learning at the Edge for embedded and low power platforms: exploiting the Intel Movidius Neural Computing Stick**
Speaker: Gionata Benelli, IngeniArs, IT

1230 **The ESD Alliance - At the Center of the Semiconductor Universe**
Speaker: Paul Cohen, ESDA, US

1300 **Lunch Break** in Lunch Area

3.0 LUNCHTIME KEYNOTE SESSION

Room 1 1350 – 1420

Chair: Marco Casale-Rossi, Synopsys, IT
Co-Chair: Giovanni De Micheli, EPFL, CH

1350 **Leonardo da Vinci, Humanism and Engineering between Florence and Milan**
Speaker: Claudio Giorgione, Museo Nazionale della Scienza e della Tecnologia Leonardo da Vinci, IT

→ See Page 8

3.1 Executive Panel: Semiconductor IP, Surfing the Next Big Wave

Room 1 1430 – 1600

Organisers:
Giovanni De Micheli, EPFL, CH
Jamil Kawa, Synopsys, US

Chair: Raul Camposano, Sage Design Automation, US

Semiconductor IP has made a great deal of progress since ARM was incorporated in 1990, almost thirty years ago, while the IC was breaking the 1-micron barrier, and power was becoming designers' biggest concern. Back then, semiconductor IP was "hard", physical-IP, which required complex porting to each and every different process technology. Over the last thirty years, and thanks to the transition from "hard" to "soft", synthesizable-IP, it has dramatically expanded, and now spans processors, interconnect, interface, FPGA, and complete sub-systems, and has become a critical enabler of modern systems-on-a-chip. Our industry is now moving to the 7/5 nanometer nodes: power remains a concern, but it is the lagging processors frequency, the latency across the processors, memory, and storage stacks, as well as the signal losses in electrical transmission lines that prevents breakthrough improvements. After decades of dominance by general purpose CPU and GPU, innovation is disrupting computing architectures: massively parallel Tensor Processing Units (TPU) are emerging that have demonstrated unprecedented performance; new memories are emerging that may complement 3D DRAM and NAND; new technologies are emerging such as super-conducting electronics and silicon photonics, which require an unprecedented level of collaboration to rapidly achieve the maturity levels required for the design and manufacturing of VLSI systems. This panel, moderated by EDA industry veteran Raul Camposano, will explore the challenges and the opportunities of semiconductor IP for the next decade.

Panelists:

Alessandro Cremonesi, STMicroelectronics, IT
K. Charles Janac, Arteris, US
Joachim Kunkel, Synopsys, US
Andrei Vladimirescu, Berkeley, US
Greg Yeric, ARM, US

1600 **Coffee Break** in Exhibition Area

3.2 Special Session: Smart Resource Management and Design Space Exploration for Heterogenous Processors

Room 2 1430 – 1600

Organisers:
Partha Pande, Washington State University, US
Jörg Henkel, Karlsruhe Institute of Technology, DE

Chair: Petru Eles, Linköping University, SE
Co-Chair: Sudeep Pasricha, Colorado State University, US

We experience a phenomenal growth in exciting, yet demanding, application areas such as deep learning, graph analytics, and scientific computing. These application areas have driven a demand for new devices that package high-performance computing into smaller form-factors that operate in heavily constrained application scenarios (e.g., deep learning inference in embedded systems). Naturally, this presents new design challenges to meet ever increasing performance, cost, and energy efficiency requirements. This special session will consider a holistic approach to the broad topic of heterogeneous architectures. Towards this end, it consists of three forward-looking talks addressing the fundamental challenges, existing proposals, and new approaches for designing and exploring heterogeneous systems. The first talk will focus on utilizing various learning techniques to achieve thermal efficiency in a heterogeneous system. The second talk will shift the discussion toward the problems of designing these heterogeneous systems to accelerate applications. We will present innovative machine learning techniques that can be used to make efficient application-specific hardware design as easy and inexpensive as developing the corresponding application software. Finally, achieving stringent performance requirements under tight thermal constraints require a systematic stability analysis due to the positive feedback between leakage power and temperature. The third talk will present a power-temperature stability and safety analysis technique that reveals the sufficient conditions under which the power-temperature trajectory converges to a stable fixed point. The following paragraphs briefly outline each topic that will be covered in this special session.

1430 **Smart Thermal Management for Heterogeneous Multicores**
Speaker: Joerg Henkel, Chair for Embedded Systems (CES), Karlsruhe Institute of Technology (KIT), DE
Authors: Joerg Henkel, Heba Khdr and Martin Rapp, Karlsruhe Institute of Technology, DE

1500 **Design and Optimization of Heterogeneous Manycore Systems enabled by Emerging Interconnect Technologies: Promises and Challenges**
Speaker: Partha Pande, Washington State University, US
Authors: Biresh Kumar Joardar[1], Ryan Kim[2], Janardhan Rao Doppa[1] and Partha Pratim Pande[1]
[1]Washington State University, US; [2]Colorado State University, US

1530 **Power and Thermal Analysis of Commercial Mobile Platforms: Experiments and Case Studies**
Speaker: Umit Ogras, Arizona State University, US
Authors: Ganapati Bhat[1], Suat Gumussoy[2] and Umit Ogras[1]
[1]Arizona State University, US; [2]Mathworks, US

1600 **Coffee Break** in Exhibition Area

3.3 Methods and Characterisation techniques for Reliability

Room 3 1430 – 1600

Chair: Said Hamdioui, TU Delft, NL
Co-Chair: Arnaud Virazel, LIRMM, FR

This sections discusses the characterisation of BIT and ESD as well as a methodology to analyse the aging of SRAMs

1430 **New method for the automated massive characterization of Bias Temperature Instability in CMOS transistors**
Speaker: Pablo Sarazá Canflanca, Universidad de Sevilla, ES
Authors: Pablo Saraza-Canflanca[1], Javier Diaz-Fortuny[2], Rafael Castro-Lopez[1], Elisenda Roca[1], Javier Martin-Martinez[2], Rosana Rodriguez[2], Montserrat Nafria[2] and Francisco Vidal Fernandez[1]
[1]Instituto de Microelectrónica de Sevilla, ES; [2]Universitat Autonoma de Barcelona UAB, ES

1500 **Guilty As Charged: Computational Reliability Threats Posed By Electrostatic Discharge-induced Soft Errors**
Speaker: Keven Feng, University of Illinois at Urbana Champaign, US
Authors: Keven Feng, Sandeep Vora, Rui Jiang, Elyse Rosenbaum and Shobha Vasudevan, ECE at University of Illinois at Urbana-Champaign, US

1530 **Methodology for Application-Dependent Degradation Analysis of Memory Timing**
Speaker: Daniel Kraak, Delft University of Technology, NL
Authors: Daniel Kraak[1], Innocent Agbo[1], Mottaqiallah Taouil[1], Said Hamdioui[1], Pieter Weckx[2], Stefan Cosemans[2] and Francky Catthoor[2]
[1]Delft University of Technology, NL; [2]imec vzw., BE

IPs **IP1-14, IP1-15, IP1-16, IP1-17, IP1-18**

1600 **Coffee Break** in Exhibition Area

3.4 Physical Design, Extraction and Timing Analysis

Room 4 1430 – 1600

Chair: Patrick Groeneveld, Cadence Design Systems, US
Co-Chair: Po-Hung Lin Mark, National Chung Cheng University, TW

The first paper uses multivariate linear regression to increase the efficiency of corner based timing analysis. The second paper proposes an approach for zero skew clock tree construction yielding superior wire-length performance. The following two papers present macro placement algorithms: one adopting a dataflow driven approach, the other using a routability driven convolutional neural network predictor. The last paper addresses issues on reusability and reproducibility in parallelized random walk based capacitance extraction.

1430 **"Unobserved Corner" Prediction: Reducing Timing Analysis Effort for Faster Design Convergence in Advanced-Node Design**
Speaker: Uday Mallappa, University of California San Diego, US
Authors: Andrew Kahng, Uday Mallappa, Lawrence Saul and Shangyuan Tong, University of California San Diego, US

1500 **Dim Sum: Light Clock Tree by Small Diameter Sum**
Speaker: Gengjie Chen, The Chinese University of Hong Kong, HK
Authors: Gengjie Chen and Evangeline Young, The Chinese University of Hong Kong, HK

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1515 **Routability-Driven Macro Placement with Embedded CNN-Based Prediction Model**
Speaker: Yu-Hung Huang, National Taiwan University of Science and Technology, TW
Authors: Yu-Hung Huang[1], Zhiyao Xie[2], Guan-Qi Fang[1], Tao-Chun Yu[1], Haoxing Ren[3], Shao-Yun Fang[1], Yiran Chen[2] and Jiang Hu[4]
[1]National Taiwan University of Science and Technology, TW; [2]Duke University, US; [3]NVIDIA Corporation, US; [4]Texas A&M University, US

1530 **RTL-Aware Dataflow-Driven Macro Placement**
Speaker: Alexandre Vidal Obiols, Polytechnic University of Catalonia, ES
Authors: Alexandre Vidal Obiols[1], Jordi Cortadella[1], Jordi Petit[1], Marc Galceran-Oms[2] and Ferran Martorell[2]
[1]UPC, ES; [2]eSilicon EMEA, Barcelona, ES

1545 **Realizing Reproducible and Reusable Parallel Floating Random Walk Solvers for Practical Usage**
Speaker: Mingye Song, Tsinghua University, CN
Authors: Mingye Song[1], Zhezhao Xu[1], Wenjian Yu[1] and Lei Yin[2]
[1]Tsinghua University, CN; [2]ANSYS Inc., US

IPs **IP1-19, IP1-20**

1600 **Coffee Break** in Exhibition Area

3.5 Hardware authentication and attack prevention

Room 5 1430 – 1600

Chair: Johanna Sepulveda, TUM, DE
Co-Chair: Ilia Polian, University of Stuttgart, DE

Electronics industry involves considerable investment, which turns the protection of their Intellectual Property a main concern. The development of new technologies will depend on it. In this session, solutions based on obfuscated microfluidic biochips and PUF-like Quantum Dots (QD) devices are shown. Moreover, and attack that challenges PUF-based identifier techniques using machine learning is presented.

1430 **Optically Interrogated Unique Object with Simulation Attack Prevention**
Speaker: Povilas Marcinkevicius, Lancaster University, GB
Authors: Povilas Marcinkevicius, Ibrahim Ethem Bagci, Nema M. Abdelazim, Christopher S. Woodhead, Robert J. Young and Utz Roedig, Lancaster University, GB

1500 **PUFs Deep Attacks: Enhanced modeling attacks using deep learning techniques to break the security of double arbiter PUFs**
Speaker: Mahmoud Khalafalla, University Of Waterloo, CA
Authors: Mahmoud Khalafalla and Catherine Gebotys, University of Waterloo, CA

1530 **Desieve the Attacker: Thwarting IP Theft in Sieve-Valve-based Biochips**
Speaker: Shayan Mohammed, New York University, US
Authors: Mohammed Shayan[1], Sukanta Bhattacharjee[2], Yong Rafael Song[2], Krishnendu Chakrabarty[3] and Ramesh Karri[4]
[1]New York University, US; [2]New York University Abu Dhabi, AE; [3]Duke University, US; [4]NYU, US

1600 **Coffee Break** in Exhibition Area

3.6 Software Solutions for Reliable Memories

Room 6 1430 – 1600

Chair: Valentin Gherman, CEA-Leti, FR
Co-Chair: Borzoo Bonakdarpour, Iowa State University, US

This session explores solutions for reliable memories at different levels. The first paper introduces a process-variation-resilient space allocation scheme for open-channel SSD with 3D charge-trap flash memory. The second paper presents an architecture-independent framework to mitigate read disturbance errors in STT-RAM. Finally, the third paper proposes a wear leveling aware memory allocator for PCM memories. The IP presentation deals with memory dependency speculation and how to take advantage of it during the Dynamic Binary Translation process by using VLIW cores.

1430 **PATCH: Process-Variation-Resilient Space Allocation for Open-Channel SSD with 3D Flash**
Speaker: Yi Wang, Shenzhen University, CN
Authors: Jing Chen[1], Yi Wang[1], Amelie Chi Zhou[1], Rui Mao[1] and Tao Li[2]
[1]Shenzhen University, CN; [2]University of Florida, US

1500 **Compiler-Directed and Architecture-Independent Mitigation of Read Disturbance Errors in STT-RAM**
Speaker: Chengmo Yang, University of Delaware, US
Authors: Fateme Sadat Hosseini and Chengmo Yang, University of Delaware, US

1530 **A Wear Leveling Aware Memory Allocator for Both Stack and Heap Management in PCM-based Main Memory Systems**
Speaker: Qingan Li, Wuhan University, CN
Authors: Wei Li[1], Ziqi Shuai[1], Chun Xue[2], Mengting Yuan[1] and Qingan Li[1]
[1]Wuhan University, CN; [2]City University of Hong Kong, HK

IPs **IP1-21**

1600 **Coffee Break** in Exhibition Area

3.7 Design Automation of Cyber-Physical Systems

Room 7 1430 – 1600

Chair: Lei Bu, Nanjing University, CN
Co-Chair: Stefano Centomo, University of Verona, IT

The session addresses design techniques for modern cyber-physical systems, e.g., design of the computation/communication platform according to system dynamics, design of variable-delay controllers and, last but not least, assume-guarantee contract optimization.

1430 **Exploiting System Dynamics for Resource-Efficient Automotive CPS Design**
Speaker: Wanli Chang, University of York, GB
Authors: Leslie Maldonado[1], Wanli Chang[2], Debayan Roy[3], Anuradha Annaswamy[1], Dip Goswami[4] and Samarjit Chakraborty[3]
[1]MIT, US; [2]University of York, GB; [3]TUM, DE; [4]Eindhoven University of Technology, NL

1500 **Implementation-aware design of image-based control with on-line measurable variable-delay**
Speaker: Robinson Medina, Eindhoven University of Technology & TNO Powertrains, NL
Authors: Róbinson Alberto Medina Sánchez, Sander Stuijk, Dip Goswami and Twan Basten, Eindhoven University of Technology, NL

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1530 **Optimizing Assume-Guarantee Contracts for the Design of Cyber-Physical Systems**
Speaker: Chanwook Oh, University of Southern California, US
Authors: Chanwook Oh[1], Eunsuk Kang[2], Shinichi Shiraishi[2] and Pierluigi Nuzzo[1]
[1]University of Southern California, US; [2]Toyota InfoTechnology Center, US

1600 **Coffee Break** in Exhibition Area

3.8 DFG Collaborative Funding Instruments

Exhibition Theatre 1430 – 1600

Organiser: Jürgen Teich, Friedrich-Alexander-Universität Erlangen-Nürnberg, DE
Moderator: Andreas Raabe, DFG, DE

Collaborative interdisciplinary research is considered of paramount importance today for the achievement of breakthroughs and jumps in technical innovation. In this session, program director Dr. Andreas Raabe introduces which types of collaborative funding instruments are offered by the Deutsche Forschungsgemeinschaft (DFG) in Germany, but also funding opportunities for international cooperations. After an introduction into different funding instruments for short, medium and long term collaborative research, concrete example initiatives in the scope of topics of DATE will be shortly introduced and summarized by representatives with a majority of these initiatives also exhibiting during the conference week.

1430 **DFG Collaborative Funding Instruments - An Overview**
Speaker: Andreas Raabe, DFG, DE

1445 **Priority Program: SPP1648 Software for Exascale Computing**
Speaker: Hans-Joachim Bungartz, TUM, DE

1452 **Priority Program: SPP2037 Scalable Data Management for Future Hardware**
Speaker: Kai-Uwe Sattler, TU Ilmenau, DE

1500 **Research Unit: FOR1800 Controlling Concurrent Change - towards self-aware automotive and space vehicles**
Speaker: Rolf Ernst, TU Braunschweig, IDA, DE

1507 **Collaborative Research Centre: SFB 901 On-the-fly Computing**
Speaker: Marco Platzner, Paderborn University, DE

1515 **Collaborative Research Centre: SFB 876 Providing Information by Resource-Constrained Data Analysis**
Speaker: Jian-Jia Chen, TU Dortmund, DE

1522 **Transregional Research Centre: TR89 Invasive Computing**
Speaker: Jürgen Teich, Friedrich-Alexander-Universität Erlangen-Nürnberg, DE

1530 **Collaborative Research Centre: SFB 912 Highly Adaptive Energy Efficient Computing**
Speaker: Gerhard Fettweis, Technische Universität Dresden, DE

1537 **Bi-National Research Project: Conquering MPSoC Complexity with Principles of a Self-Aware Information**
Speaker: Andreas Herkersdorf, TUM, DE
Author: Rolf Ernst, TU Braunschweig, IDA, DE

1600 **Coffee Break** in Exhibition Area

3ps.8 Publisher's Session: How to Publish Your Research Work

Exhibition Theatre 1615 – 1645

1615 **Speaker: Charles Glaser,** Springer, US

This publisher's session invites all attendees to discuss how and why to publish their research work with Springer Nature. Charles Glaser, Editorial Director for Springer, will present his advice for collaboration in research dissemination. He will be available in this session, as well as the entire exhibition, to discuss the publication of your next book.

IP1 Interactive Presentations

Poster Area 1600 – 1630
supported by Cadence Academic Network

Interactive Presentations run simultaneously during a 30-minute slot. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session.

IP1-1 **Fault Injection on Hidden Registers in a RISC-V Rocket processor and Software Countermeasures**
Speaker: Johan Laurent, Univ. Grenoble Alpes, Grenoble INP, LCIS, FR
Authors: Johan Laurent[1], Vincent Beroulle[1], Christophe Deleuze[1] and Florian Pebay-Peyroula[2]
[1]LCIS - Grenoble Institute of Technology - Univ. Grenoble Alpes, FR; [2]CEA-Leti, FR

IP1-2 **Methodology for EM Fault Injection: Charge-based Fault Model**
Speaker: Haohao Liao, University of Waterloo, CA
Authors: Haohao Liao and Catherine Gebotys, University of Waterloo, CA

IP1-3 **Securing Cryptographic Circuits by Exploiting Implementation Diversity and Partial Reconfiguration on FPGAs**
Speaker: Benjamin Hettwer, Robert Bosch GmbH, DE
Authors: Benjamin Hettwer[1], Johannes Petersen[2], Stefan Gehrer[1], Heike Neumann[2] and Tim Güneysu[3]
[1]Robert Bosch GmbH, Corporate Sector Research, DE; [2]Hamburg University of Applied Sciences, DE; [3]Horst Görtz Institute for IT Security, Ruhr-University Bochum, DE

IP1-4 **STT-ANGIE: Asynchronous True Random Number Generator Using STT-MTJ**
Speaker: Ben Perach, Faculty of Electrical Engineering,Technion - Israel Institute of Technology, IL
Authors: Ben Perach and Shahar Kvatinsky, Technion, IL

IP1-5 **Adaptive Transient Leakage-Aware Linearised Model for Thermal Analysis of 3-D ICs**
Speaker: Milan Mihajlovic, University of Manchester, GB
Authors: Chao Zhang, Milan Mihajlovic and Vasilis Pavlidis, The University of Manchester, GB

IP1-6 **FastCool: Leakage Aware Dynamic Thermal Management of 3D Memories**
Speaker: Lokesh Siddhu, IIT Delhi, IN
Authors: Lokesh Siddhu and Preeti Ranjan Panda, Indian Institute of Technology, Delhi, IN

IP1-7 **On the use of causal feature selection in the context of machine-learning indirect test**
Speaker: Manuel Barragán, TIMA laboraory, FR
Authors: Manuel Barragán[1], Gildas Leger[2], Florent Cilici[1], Estelle Lauga-Larroze[3], Sylvain Bourdel[3] and Salvador Mir[1]
[1]TIMA Laboratory, FR; [2]Instituto de Microelectronica de Sevilla, IMSE-CNM, (CSIC – Universidad de Sevilla), ES; [3]RFICLab, FR

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IP1-8 **Accuracy and Compactness in Decision Diagrams for Quantum Computation**
Speaker: Alwin Zulehner, Johannes Kepler University Linz, AT
Authors: Alwin Zulehner[1], Philipp Niemann[2], Rolf Drechsler[3] and Robert Wille[1]
[1]Johannes Kepler University Linz, AT; [2]Cyber-Physical Systems, DFKI GmbH, DE; [3]University of Bremen, DE

IP1-9 **One Method - All Error-Metrics: A Three-Stage Approach for Error-Metric Evaluation in Approximate**
Speaker: Saman Fröhlich, University of Bremen/DFKI GmbH, DE
Authors: Saman Fröhlich[1], Daniel Grosse[2] and Rolf Drechsler[2]
[1]University of Bremen/DFKI GmbH, DE; [2]University of Bremen, DE

IP1-10 **Reversible Pebbling Game for Quantum Memory Management**
Speaker: Giulia Meuli, EPFL, CH
Authors: Giulia Meuli[1], Mathias Soeken[1], Martin Roetteler[2], Nikolaj Bjorner[2] and Giovanni De Micheli[1]
[1]EPFL, CH; [2]Microsoft, US

IP1-11 **TypeCNN: CNN Development Framework With Flexible Data Types**
Speaker: Lukas Sekanina, Brno University of Technology, CZ
Authors: Petr Rek and Lukas Sekanina, Brno University of Technology, CZ

IP1-12 **Guaranteed Compression Rate for Activations in CNNs using a Frequency Pruning Approach**
Speaker: Sebatian Vogel, Robert Bosch GmbH, DE
Authors: Sebastian Vogel[1], Christoph Schorn[1], Andre Guntoro[1] and Gerd Ascheid[2]
[1]Robert Bosch GmbH, DE; [2]RWTH Aachen University, DE

IP1-13 **Runtime Monitoring Neuron Activation Patterns**
Speaker: Chih-Hong Cheng, fortiss, DE
Authors: Chih-Hong Cheng[1], Georg Nührenberg[1] and Hirotoshi Yasuoka[2]
[1]fortiss - Landesforschungsinstitut des Freistaats Bayern, DE; [2]DENSO Corporation, JP

IP1-14 **Chip Health Tracking Using Dynamic In-Situ Delay Monitoring**
Speaker: Hadi Ahmadi Balef, Eindhoven University of Technology, NL
Authors: Hadi Ahmadi Balef, Kees Goossens and José Pineda de Gyvez, Eindhoven University of Technology, NL

IP1-15 **PCFI: Program Counter Guided Fault Injection for Accelerating GPU Reliability Assessment**
Speaker: Fritz Previlon, Northeastern University, US
Authors: Fritz Previlon, Charu Kalra, Devesh Tiwari and David Kaeli, Northeastern University, US

IP1-16 **Characterizing the Reliability and Threshold Voltage Shifting of 3D Charge Trap NAND Flash**
Speaker: Weihua Liu, Huazhong University of Science and Technology, CN
Authors: Weihua Liu[1], Fei Wu[1], Meng Zhang[1], Yifei Wang[1], Zhonghai Lu[2], Xiangfeng Lu[3] and Changsheng Xie[1]
[1]Huazhong University of Science and Technology, CN; [2]KTH Royal Institute of Technology, SE; [3]Beijing Memblaze Technology Co., Ltd., CN

IP1-17 **Hidden Delay Fault Sensor for Test, Reliability and Security**
Speaker: Giorgio Di Natale, CNRS - TIMA, FR
Authors: Giorgio Di Natale[1], Elena Ioana Vatajelu[2], Kalpana Senthamarai Kannan[2] and Lorena Anghel[3]
[1]LIRMM, FR; [2]TIMA, FR; [3]Grenoble-Alpes University, FR

IP1-18 **Effect of Device Variation on mapping Binary Neural Network to Memristor Crossbar Array**
Speaker: Wooseok Yi, POSTECH, KR
Authors: Wooseok Yi, Yulhwa Kim and Jae-Joon Kim, Pohang University of Science and Technology, KR

IP1-19 **Accurate Wirelength Prediction for Placement-Aware Synthesis through Machine Learning**
Speaker: Daijoon Hyun, KAIST, KR
Authors: Daijoon Hyun, Yuepeng Fan and Youngsoo Shin, KAIST, KR

IP1-20 **A Mixed-Height Standard Cell Placement Flow for Digital Circuit Blocks**
Speaker: Yi-Cheng Zhao, National Tsing Hua University, TW
Authors: Yi-Cheng Zhao[1], Yu-Chieh Lin[1], Ting-Chi Wang[1], Ting-Hsiung Wang[2], Yun-Ru Wu[2], Hsin-Chang Lin[2] and Shu-Yi Kao[2]
[1]National Tsing Hua University, TW; [2]Realtek Semiconductor Corp., TW

IP1-21 **Aggressive Memory Speculation in HW/SW Co-Designed Machines**
Speaker: Simon Rokicki, INRIA, FR
Authors: Simon Rokicki, Erven Rohou and Steven Derrien, IRISA, Rennes, FR

4.1 Executive Session: The Future of Test

Room 1 1700 – 1830

Chair: Subhasish Mitra, Stanford University, US

This session titled "The Future of Test" explores various aspects of test: from traditional manufacturing test, to its role in addressing yield and reliability at advanced technology nodes, all the way to the design and test of quantum computers. The role of testing beyond manufacturing (e.g., in system validation and security) will also be explored.

1700 **Yield and Reliability Challenges and Solutions at 7nm and Below**
Speaker and Author: Andrzej Strojwas, Carnegie Mellon University and PDF Solutions, US

1730 **Three possible alternate realities for the future of test**
Speaker and Author: Jeff Rearick, AMD, US

1800 **What about the Design and Test of Quantum Computers?**
Speaker and Author: Leon Stok, IBM, US

1830 **Exhibition Reception** in Exhibition Area
supported by Destination Florence Convention and Visitors Bureau

4.2 Reconfigurable Architecture and Tools

Room 2 1700 – 1830

Chair: Smail Niar, Université Polytechnique Hauts-de-France, FR
Co-Chair: Lars Bauer, Karlsruhe Institute of Technology, DE

This session presents three papers that improved application mapping onto coarse-grained reconfigurable arrays, thermal aware application mapping for FPGAs, and hardware security coprocessor for reconfigurable CPUs, along with two interactive presentations that introduce novel hardware accelerator interfaces to multi-core CPUs and approximate arithmetic components.

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1700 **Context-memory Aware Mapping for Energy Efficient Acceleration with CGRAs**
Speaker: Satyajit Das, Univ. Bretagne-Sud, CNRS UMR 6285, Lab-STICC, FR
Authors: Satyajit Das, Kevin Martin and Philippe Coussy, Université de Bretagne-Sud, FR

1730 **Thermal-Aware Design and Flow for FPGA Performance Improvement**
Speaker: Tajana Rosing, University of California, San Diego, US
Authors: Behnam Khaleghi and Tajana Rosing, University of California, San Diego, US

1800 **FIXER: Flow Integrity Extensions for Embedded RISC-V**
Speaker: Swaroop Ghosh, The Pennsylvania State University, US
Authors: Asmit De, Aditya Basu, Swaroop Ghosh and Trent Jaeger, Pennsylvania State University, US

IPs **IP2-1, IP2-2**

1830 **Exhibition Reception** in Exhibition Area
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4.3 Improving test generation and coverage

Room 3 1700 – 1830

Chair: Jaan Raik, Tallinn University of Technology, EE
Co-Chair: Sara Vinco, Polytechnic of Turin, IT

This session targets improving coverage from different perspectives, to activate multiple targets with concolic testing, to improve functional coverage metrics for instruction set simulators, and to achieve path coverage in SystemC-AMS. Three IPs complete the session covering optimizations for system verification and design.

1700 **Automated Activation of Multiple Targets in RTL Models using Concolic Testing**
Speaker: Prabhat Mishra, University of Florida, US
Authors: Yangdi Lyu, Alif Ahmed and Prabhat Mishra, University of Florida, US

1730 **Verifying Instruction Set Simulators using Coverage-guided Fuzzing**
Speaker: Vladimir Herdt, University of Bremen, DE
Authors: Vladimir Herdt, Daniel Grosse, Hoang M. Le and Rolf Drechsler, University of Bremen, DE

1800 **Data Flow Testing for SystemC-AMS Timed Data Flow Models**
Speaker: Muhammad Hassan, DFKI GmbH, DE
Authors: Muhammad Hassan, Daniel Grosse, Hoang M. Le and Rolf Drechsler, University of Bremen, DE

IPs **IP2-3, IP2-4, IP2-5**

1830 **Exhibition Reception** in Exhibition Area
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4.4 Digital processing with emerging memory technologies

Room 4 1700 – 1830

Chair: Shahar Kvatinsky, Technion, IL
Co-Chair: Elena-Ioana Vataleju, TIMA, FR

This session looks at how emerging memory technologies improve the processing in digital systems for applications like processing-in-memory, graph processing, Binary Neural Networks and nonvolatile processors.

1700 **SAID: A Supergate-Aided Logic Synthesis Flow for Memristive Crossbars**
Speaker: Roberto Giorgio Rizzo, Politecnico di Torino, IT
Authors: Valerio Tenace[1], Roberto Giorgio Rizzo[1], Debjyoti Bhattacharjee[2], Anupam Chattopadhyay[2] and Andrea Calimera[1]
[1]Politecnico di Torino, IT; [2]Nanyang Technological University, SG

1730 **GraphS: A Graph Processing Accelerator Leveraging SOT-MRAM**
Speaker: Deliang Fan, University of Central Florida, US
Authors: Shaahin Angizi, Jiao Sun, Wei Zhang and Deliang Fan, University of Central Florida, US

1800 **CORN: In-Buffer Computing for Binary Neural Network**
Speaker: Liang Chang, Beihang University, CN
Authors: Liang Chang[1], Xin Ma[2], Zhaohao Wang[1], Youguang Zhang[1], Weisheng Zhao[1] and Yuan Xie[2]
[1]Beihang University, CN; [2]University of California, Santa Barbara, US

1815 **An Energy Efficient Non-Volatile Flip-Flop based on CoMET Technology**
Speaker: Robert Perricone, University of Notre Dame, US
Authors: Robert Perricone[1], Zhaoxin Liang[2], Meghna Mankalale[2], Michael Niemier[1], Sachin S. Sapatnekar[2], Jian-Ping Wang[2] and X, Sharon Hu[1]
[1]University of Notre Dame, US; [2]University of Minnesota, US

1830 **Exhibition Reception** in Exhibition Area
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4.5 Hardware Trojans and Split Manufacturing

Room 5 1700 – 1830

Chair: Nele Mentens, KU Leuven, BE
Co-Chair: Giorgio Di Natale, TIMA, FR

This session elaborates on Hardware Trojans, which are an emerging threat to the security of hardware-software systems. Furthermore, it discusses split manufacturing as a technique to strengthen the security of semiconductor supply chains.

1700 **Hardware Trojan in Emerging Non-Volatile Memories**
Speaker: Swaroop Ghosh, The Pennsylvania State University, US
Authors: Mohammad Nasim Imtiaz Khan, Karthikeyan Nagarajan and Swaroop Ghosh, Pennsylvania State University, US

1730 **Evaluating Assertion Set Completeness to Expose Hardware Trojans and Verification Blindspots**
Speaker: Nicole Fern, University of California Santa Barbara, US
Authors: Nicole Fern[1] and Tim Cheng[2]
[1]University of California Santa Barbara, US; [2]HKUST, HK

1800 **Efficient Test Generation for Trojan Detection using Side Channel Analysis**
Speaker: Prabhat Mishra, University of Florida, US
Authors: Yangdi Lyu and Prabhat Mishra, University of Florida, US

1815 **A New Paradigm in Split Manufacturing: Lock the FEOL, Unlock at the BEOL**
Speaker: Abhrajit Sengupta, New York University, US
Authors: Abhrajit Sengupta[1], Mohammed Nabeel[2], Johann Knetchel[3] and Ozgur Sinanoglu[4]
[1]New York University, US; [2]New York University Abu Dhabi, IN; [3]New York University Abu Dhabi, DE; [4]New York University Abu Dhabi, AE

IPs **IP2-6**

1830 **Exhibition Reception** in Exhibition Area
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4.6 Smart Communication Solutions for Automotive Systems

Room 6 1700 – 1830

Chair: Dirk Ziegenbein, Robert Bosch GmbH, DE
Co-Chair: Selma Saidi, Hamburg University of Technology, DE

In this session, three approaches to smart communication in automotive systems design are presented. The first paper optimizes end-to-end latencies for time-sensitive networks with frame preemption. The second paper introduces a consensus scheme for vehicle platoon maneuvers. The third paper presents a decentralized approach to non-neighbor charge balancing in battery packs.

1700 **Design Optimization of Frame Preemption in Real-Time Switched Ethernet**
Speaker: Taeju Park, University of Michigan, US
Authors: Taeju Park[1], Soheil Samii[2] and Kang Shin[1]
[1]University of Michigan, US; [2]General Motors Research & Development, US

1730 **CUBA: Chained Unanimous Byzantine Agreement for Decentralized Platoon Management**
Speaker: Emanuel Regnath, TUM, DE
Authors: Emanuel Regnath and Sebastian Steinhorst, TUM, DE

1800 **Decentralized Non-Neighbor Active Charge Balancing in Large Battery Packs**
Speaker: Alexander Lamprecht, TUM CREATE, SG
Authors: Alexander Lamprecht[1], Martin Baumann[2], Tobias Massier[1] and Sebastian Steinhorst[2]
[1]TUM CREATE, SG; [2]TUM, DE

IPs **IP2-7, IP2-8**

1830 **Exhibition Reception** in Exhibition Area
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4.7 Energy and power efficiency in GPU-based systems

Room 7 1700 – 1830

Chair: Muhammad Shafique, TU Wien, AT
Co-Chair: William Fornaciari, Politecnico di Milano, IT

This session presents three papers, two on energy efficiency for GPU-based systems and one about exploring performance and accuracy tradeoffs when using GPUs for SNN modeling. The first paper presents an online thermal and energy management mechanism for CPU-GPU system enabled by efficient thread partitioning, mapping, and respective models. The second paper identifies choke points in GPUs and boost the choke point induced critical warps for achieving high energy efficiency. The third paper presents a GPU-accelerated SNN simulator that introduces stochasticity in STDP and capability of performing low-precision simulation.

1700 **TEEM: Online Thermal- and Energy-Efficiency Management on CPU-GPU MPSoCs**
Speaker: Amit Kumar Singh, University of Essex, GB
Authors: Samuel Isuwa, Somdip Dey, Amit Kumar Singh and Klaus McDonald-Maier, University of Essex, GB

1730 **Predicting Critical Warps in Near-Threshold GPGPU Applications using a Dynamic Choke Point Analysis**
Speaker: Sourav Sanyal, Utah State University, US
Authors: Sourav Sanyal, Prabal Basu, Aatreyi Bal, Sanghamitra Roy and Koushik Chakraborty, Utah State University, US

1800 **Fast and Low-Precision Learning in GPU-Accelerated Spiking Neural Network**
Speaker: Xueyuan She, Georgia Institute of Technology, US
Authors: Xueyuan She, Yun Long and Saibal Mukhopadhyay, Georgia Institute of Technology, US

1830 **Exhibition Reception** in Exhibition Area
supported by Destination Florence Convention and Visitors Bureau

4.8 Embedded Tutorial: Paving the Way for Very Large Scale Integration of Superconductive Electronics

Exhibition Theatre 1700 – 1830

Organisers:
Jamil Kawa, Synopsys, US
Massoud Pedram, USC, US

Chair: Jamil Kawa, Synopsys, US

Superconductive electronics (SCE) based on single flux quantum (SFQ) family of logic cells has appeared as a potent and within-reach "beyond-CMOS" technology. With proven switching speeds in 100's of GHz and energy dissipation approaching 10^(-19) Joules per transition (and lower for the adiabatic family), it is one of the most promising post-CMOS technologies that can break the current performance limit of 4 or so GHz CMOS processors, delivering a 30GHz single-threaded performance for a SCE processor. The state-of-the-art in terms of libraries, simulation and analysis, compact modeling, synthesis, physical design of SFQ-based logic is far behind that of CMOS, with semi-manual design of 16-bit SFQ adders, simple filters and ADCs, and bit-serial processors defining the state-of-the-art. To fulfill the potential of SCE logic families, it is essential that design methodologies and tools are developed to enable fully automated design of SCE VLSI circuits and processors on chip. The ac- and dc-biased SFQ logic families (such as RSFQ, ERSFQ, and AQFP) are, however, fundamentally different from CMOS logic families, for example, in terms of their reliance on two-terminal Josephson junctions with complex voltage-current (current-phase) behavior, cryogenic operation, pulse-based signaling, prevalence of inductors as key passive element, clocked nature of most logic cells and need for path balancing, limited fanout count of typically 2 or 3, use of biasing currents as the power source, etc. This tutorial aims at introducing the SCE SFQ technology starting from JJ device modeling and simulation to compact modeling of logic cells and superconductive transmission lines, to specialized logic synthesis, clock tree synthesis, bias distribution, and place&route engines.

1700 **Physics-based modeling and device simulation of Josephson Junctions**
Author: Pooya Jannaty, Synopsys, US

1730 **Architectures, synthesis flow, and place & route engine for DC-biased SFQ logic circuits**
Author: Massoud Pedram, USC, US

1800 **Library design and design tools for adiabatic quantum-flux-parametron logic circuits (AC-biased SFQ logic)**
Author: Nobuyuki Yoshikawa, Yokohama National University, JP

1830 **Exhibition Reception** in Exhibition Area
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WEDNESDAY, 27 MARCH 2019

5.1 Special Day on "Embedded Meets Hyperscale and HPC" Session: Heterogeneous Computing in the Datacenter and in HPC

Room 1 0830 – 1000

Chair: Christian Plessl, Paderborn University, DE
Co-Chair: Christoph Hagleitner, IBM Research, CH

Heterogeneous computing systems with accelerators are claiming the top ranks in the TOP500 list of the largest HPC computing systems and find increasing adoption in hyperscale cloud datacenters. Accelerators offer performance and efficiency gains despite the diminishing returns from traditional technology scaling. The talks in this session will set the stage for this special day and analyze the value proposition of accelerators for traditional and emerging workloads. An overview of this vibrant environment will be followed by more detailed presentations on systems using GPUs and FPGAs

0830 **Silicon Heterogeneity in the Cloud**
Speaker and Author: Babak Falsafi, EPFL, CH

0830 **GPU accelerated computing in HPC and in the data center**
Speaker and Author: Peter Messmer, NVidia, US

0900 **Heterogeneous Compute Architectures for Deep Learning in the Cloud**
Speaker and Author: Ken O'Brien, Xilinx Research, IE

1000 **Coffee Break** in Exhibition Area

5.2 Improving Formal Verification and Applications to GPUs and High-Level Synthesis

Room 2 0830 – 1000

Chair: Alessandro Cimatti, Fondazione Bruno Kessler, IT
Co-Chair: Gianpiero Cabodi, Politecnico di Torino, IT

The session includes three technical and three application papers. The technical papers aim at improving and evaluating advanced model checking engines, and combining algebraic reasoning and SAT. The application papers show how formal verification is used for the correctness of GPU assembly programs, equivalence checking for high-level synthesis, and assessing failure rates of CMOS.

0830 **fbPDR: In-depth combination of forward and backward analysis in Property Directed Reachability**
Speaker: Tobias Seufert, University of Freiburg, DE
Authors: Tobias Seufert and Christoph Scholl, University Freiburg, DE

0900 **High Coverage Concolic Equivalence Checking**
Speaker: Sagar Chaki, Mentor, US
Authors: Pritam Roy, Sagar Chaki and Pankaj Chauhan, Mentor, US

0930 **Bosphorus: Bridging ANF and CNF Solvers**
Speaker: Mate Soos, National University of Singapore, SG
Authors: Davin Choo[1], Mate Soos[2], Kian Ming A. Chai[1] and Kuldeep S Meel[2]
[1]DSO National Laboratories, SG; [2]National University of Singapore, SG

0945 **CUDA au Coq: A Framework for Machine-validating GPU Assembly Programs**
Speaker: Benjamin Ferrell, University Texas at Dallas, US
Authors: Benjamin Ferrell, Jun Duan and Kevin Hamlen, University of Texas at Dallas, US

IPs **IP2-9, IP2-10**

1000 **Coffee Break** in Exhibition Area

5.3 EU Projects

Room 3 0830 – 1000

Chair: Martin Schoeberl, Technical University of Denmark, DK

0830 **AXIOM: A Scalable, Efficient and Reconfigurable Embedded Platform**
Speaker: Roberto Giorgi, University of Siena, IT
Authors: Roberto Giorgi, Marco Procaccini and Farnam Khalili, University of Siena, IT

0900 **Applications of Computation-In-Memory Architectures based on Memristive Devices**
Speaker: Said Hamdioui, Delft University of Technology, NL
Authors: Said Hamdioui[1], Abu Sebastian[2], Shidhartha Das[3], Geethan Karunaratne[4], Hoang Anh Du Nguyen[1], Manuel Le Gallo[2], Siebren Schaafsma[5], Abbas Rahimi[4], Mottaqiallah Taouil[1], Francky Catthoor[6], Luca Benini[4], Sandeep Pande[5] and Fernando G. Redondo[3]
[1]Delft University of Technology, NL; [2]IBM, CH; [3]ARM Ltd., GB; [4]ETHZ, CH; [5]IMEC, NL; [6]IMEC, BE

0915 **Chip-to-Cloud: an Autonomous and Energy Efficient Platform for Smart Vision Applications**
Speaker: Simone Ciccia, Istituto Superiore Mario Boella (ISMB), IT
Authors: Alberto Scionti, Simone Ciccia, Olivier Terzo and Giorgio Giordanengo, Istituto Superiore Mario Boella, IT

0930 **On the Use of Hackathons to Enhance Collaboration in Large Collaborative Projects -A Preliminary Case Study of the MegaM@Rt2 EU Project -**
Speaker: Gunnar Widforss, Mälardalen University, SE
Authors: Andrey Sadovykh[1], Dragos Truscan[2], Pierluigi Pierini[3], Gunnar Widforss[4], Adnan Ashraf[2], Hugo Bruneliere[5], Pavel Smrz[6], Alessandra Bagnato[7], Wasif Afzal[4] and Alexandra Espinosa Hortelano[4]
[1]SOFTEAM; Innopolis University, FR; [2]Abo Akademi, FI; [3]Intecs S.p.A., IT; [4]Maelardalens Hoegskola, SE; [5]Association pour la Recherche et le Développement des Méthodes et Processus Industriels, FR; [6]Brno University of Technology, CZ; [7]SOFTEAM, FR

0945 **Realization of Four-Terminal Switching Lattices: Technology Development and Circuit Modeling**
Speaker: Mustafa Altun, Istanbul Technical University, TR
Authors: Serzat Safaltin[1], Oguz Gencer[1], M. Ceylan Morgul[1], Levent Aksoy[1], Sebahattin Gurmen[1], Csaba Andras Moritz[2] and Mustafa Altun[1]
[1]Istanbul Technical University, TR; [2]University of Massachusetts, Amherst, US

IPs **IP2-11, IP2-12**

1000 **Coffee Break** in Exhibition Area

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5.4 Emerging technologies for better NoCs

Room 4 0830 – 1000

Chair: Davide Bertozzi, Università di Ferrara, IT
Co-Chair: Gilles Sassatelli, LIRMM CNRS / University of Montpellier, FR

This section discusses emerging technologies such as Photonics and ReRam applied to NoCs to enhance functional and non-functional systems parameters. The first paper presents a flexible communication fabric for chiplets ensuring near-100% chip assembly yield. The second paper addresses the energy minimization problem in photonic NoCs by adaptively switching on and off the lasers still accounting for the thermal sensitivity of optical devices. The third paper proposes a NoC-based architecture for training CNNs using ReRAMs for in-memory computing to maximize energy efficiency.

0830 **SiPterposer: A Fault-Tolerant Substrate for Flexible System-in-Package Design**
Speaker: Pete Ehrett, University of Michigan, US
Authors: Pete Ehrett, Todd Austin and Valeria Bertacco, University of Michigan, US

0900 **WAVES: Wavelength Selection for Power-Efficient 2.5D-Integrated Photonic NoCs**
Speaker: Aditya Narayan, Boston University, US
Authors: Aditya Narayan[1], Yvain Thonnart[2], Pascal Vivet[2], César Fuguet Tortolero[2] and Ayse Kivilcim Coskun[1]
[1]Boston University, US; [2]Univ. Grenoble Alpes, CEA-LETI, FR

0930 **REGENT: A Heterogeneous ReRAM/GPU-based Architecture Enabled by NoC for Training CNNs**
Speaker: Biresh Joardar, Washington State University, US
Authors: Biresh Joardar[1], Bing Li[2], Jana Doppa[1], Hai (Helen) Li[2], Partha Pratim Pande[1] and Krishnendu Chakrabarty[2]
[1]Washington State University, US; [2]Duke University, US

IPs **IP2-13, IP2-14**

1000 **Coffee Break** in Exhibition Area

5.5 Hardware Obfuscation

Room 5 0830 – 1000

Chair: Francesco Regazzoni, ALARI-USI, CH
Co-Chair: Daniel Grosse, University of Bremen, DE

Obfuscation is becoming a popular technique to protect IPs and designs. This session reports the last advances in protection based on obfuscation and on methodology for attacking them.

0830 **Design Obfuscation through Selective Post-Fabrication Transistor-Level Programming**
Speaker: Yiorgos Makris, The University of Texas at Dallas, US
Authors: Mustafa Shihab, Jingxiang Tian, Gaurav Rajavendra Reddy, Bo Hu, William Swartz Jr., Benjamin Carrion Schaefer, Carl Sechen and Yiorgos Makris, The University of Texas at Dallas, US

0900 **KC2: Key-Condition Crunching for Fast Sequential Circuit Deobfuscation**
Speaker: Yier Jin, University of Florida, US
Authors: Kaveh Shamsi[1], Meng Li[2], David Z. Pan[2] and Yier Jin[1]
[1]University of Florida, US; [2]University of Texas, Austin, US

0930 **Piercing Logic Locking Keys through Redundancy Identification**
Speaker: Alex Orailoglu, University of California, San Diego, US
Authors: Leon Li and Alex Orailoglu, UC San Diego, US

IPs **IP2-15, IP2-16**

1000 **Coffee Break** in Exhibition Area

5.6 Energy efficiency in IoT – Edge to Cloud

Room 6 0830 – 1000

Chair: Semeen Rehman, TU Wien, AT
Co-Chair: Baris Aksanli, San Diego State University, US

This session includes three papers discussing energy efficiency in the IoT device hierarchy. The first paper shows an energy-aware checkpointing mechanism for devices capable of energy harvesting. The second paper builds an energy-efficient, hardware-supported synchronization mechanism for ultra-low-power devices. The third paper implements energy-efficient video transcoding for cloud servers. The session also features an IP paper, that proposes a software/hardware co-design of a digital baseband processor for the IoT applications.

0830 **FlexiCheck: An Adaptive Checkpointing Architecture for Energy Harvesting Devices**
Speaker: Priyanka Singla, IIT Delhi, IN
Authors: Priyanka Singla, Shubhankar Suman Singh and Smruti R. Sarangi, IIT Delhi, IN

0900 **Hardware-Accelerated Energy-Efficient Synchronization and Communication for Ultra-Low-Power Tightly Coupled Clusters**
Speaker: Florian Glaser, ETH Zurich, CH
Authors: Florian Glaser[1], Germain Haugou[1], Davide Rossi[2], Qiuting Huang[1] and Luca Benini[1]
[1]ETH Zürich, CH; [2]Università di Bologna, IT

0930 **MAMUT: Multi-Agent Reinforcement Learning for Efficient Real-Time Multi-User Video Transcoding**
Speaker: Luis Costero, Universidad Complutense de Madrid, ES
Authors: Luis Costero[1], Arman Iranfar[2], Marina Zapater[2], Francisco D. Igual[1], Katzalin Olcoz[1] and David Atienza[2]
[1]Dpto. de Arquitectura de computadores y Automática. Universidad Complutense de Madrid, ES; [2]Embedded Systems Laboratory (ESL), Swiss Federal Institute of Technology Lausanne (EPFL), CH

IPs **IP2-17**

1000 **Coffee Break** in Exhibition Area

5.7 Data-driven Acceleration

Room 7 0830 – 1000

Chair: Anca Molnos, CEA-Leti, FR
Co-Chair: Borzoo Bonakdarpour, Iowa State University, US

This session presents accelerated computing paradigms guided by application-data criticality. The first paper presents a compiler for processing-in-memory (PIM) architectures. The second paper proposes a novel kernel tilling approach to reduce access to L2 cache. The third paper introduces data subsetting to reduce memory traffic for approximate computing platforms. The IPs deal with the RISC5 extensions for low-precision floating-point operations and GPU-based predictable execution.

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0830 **A compiler for Automatic Selection of Suitable Processing-in-Memory Instructions**
Speaker: Luigi Carro, UFRGS - Federal University of Rio Grande do Sul, BR
Authors: Hameeza Ahmed[1], Paulo Cesar Santos[2], Joao Paulo Lima[2], Rafael F. de Moura[2], Marco Antonio Zanata Alves[2], Antonio Carlos Schneider Beck[2] and Luigi Carro[2]
[1]NED University of Engineering and Technology, PK; [2]UFRGS – Universidade Federal do Rio Grande do Sul, BR

0900 **Cache-Aware Kernel Tiling: An Approach for System-Level Performance Optimization of GPU-Based Applications**
Speaker: Arian Maghazeh, Linköping University, SE
Authors: Arian Maghazeh[1], Sudipta Chattopadhyay[2], Petru Eles[1] and Zebo Peng[1]
[1]Linköping University, SE; [2]Singapore University of Technology and Design (SUTD), SG

0930 **Data Subsetting: A Data-Centric Approach to Approximate Computing**
Speaker: Younghoon Kim, Purdue University, KR
Authors: Younghoon Kim[1], Swagath Venkataramani[2], Nitin Chandrachoodan[3] and Anand Raghunathan[1]
[1]Purdue University, US; [2]IBM T. J. Watson Research Center, US; [3]Indian Institute of Technology Madras, IN

IPs **IP2-18, IP2-19, IP2-20**

1000 **Coffee Break** in Exhibition Area

5.8 Special Session: The ARAMiS II Project - Efficient Use of Multicore for safety-critical Applications

Exhibition Theatre 0830 – 1000

Organisers:
Timo Sandmann, Karlsruhe Institute of Technology, DE
Jürgen Becker, Karlsruhe Institute of Technology, DE

Chair: Timo Sandmann, Karlsruhe Institute of Technology, DE

Safety-critical applications in the domains automotive and avionics as well as the future topic Industry 4.0 show a clear and still increasing demand for digital processing power. This demand for processing power is needed, e.g. for highly automated driving and connected machines with realtime requirements. Furthermore, this demand is substantiated by an increasing interaction and integration with other systems and services. This justifies the usage of multicore technology in embedded systems in the near future, which is already successfully applied in other application domains like PCs, tablets and smartphones. However, safety-critical applications in the above-mentioned domains show many additional complex requirements, which at present can, if at all, only be fulfilled partly with an unjustified high development effort. The proposed special session shall present a summary of the most important achieved results and research topics regarding an efficient use of multicore systems in safetycritical applications.

0830 **ARAMiS II project overview**
Author: Rolf Ernst, TU Braunschweig, DE

0852 **ARAMiS II development process for model-based multicore software development**
Author: Kuntz Stefan, Continental AG, US

0914 **Methods and tools supporting multicore development**
Author: Bernhard Bauer, University of Augsburg, DE

0936 **Automotive powertrain demonstrator**
Author: Sebastian Kehr, Denso Automotive Deutschland GmbH, DE

1000 **Coffee Break** in Exhibition Area

IP2 Interactive Presentations

Poster Area 1000 – 1030
supported by Cadence Academic Network

Interactive Presentations run simultaneously during a 30-minute slot. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session.

IP2-1 TransRec: Improving Adaptability in Single-ISA Heterogeneous Systems with Transparent and Reconfigurable Acceleration

Speaker: Marcelo Brandalero, Universidade Federal do Rio Grande do Sul (UFRGS), BR
Authors: Marcelo Brandalero[1], Muhammad Shafique[2], Luigi Carro[1] and Antonio Carlos Schneider Beck[1]
[1]UFRGS - Universidade Federal do Rio Grande do Sul, BR; [2]Vienna University of Technology (TU Wien), AT

IP2-2 CADE: Configurable Approximate Divider for Energy Efficiency

Speaker: Mohsen Imani, University of California, San Diego, US
Authors: Mohsen Imani, Ricardo Garcia, Andrew Huang and Tajana Rosing, University of California San Diego, US

IP2-3 HCFTL: A Locality-Aware Page-Level Flash Translation Layer

Speaker: Hao Chen, University of Science and Technology of China, CN
Authors: Hao Chen[1], Cheng Li[1], Yubiao Pan[2], Min Lyu[1], Yongkun Li[1] and Yinlong Xu[1]
[1]University of Science and Technology of China, CN; [2]Huaqiao University, CN

IP2-4 Model Checking is Possible to Verify Large-scale Vehicle Distributed Application Systems

Speaker: Haitao Zhang, School of Information Science and Engineering, Lanzhou University, CN
Authors: Haitao Zhang[1], Ayang Tuo[1] and Guoqiang Li[2]
[1]Lanzhou University, CN; [2]Shanghai Jiao Tong University, CN

IP2-5 Automatic Assertion Generation from Natural Language Specifications Using Subtree Analysis

Speaker: Ian Harris, University of California, Irvine, US
Authors: Junchen Zhao and Ian Harris, University of California Irvine, US

IP2-6 Detection of Hardware Trojans in SystemC HLS Designs via Coverage-guided Fuzzing

Speaker: Niklas Bruns, Cyber-Physical Systems, DFKI GmbH, DE
Authors: Hoang M. Le, Daniel Grosse, Niklas Bruns and Rolf Drechsler, University of Bremen, DE

IP2-7 Design Optimization for Hardware-Based Message Filters in Broadcast Buses

Speaker: Lea Schönberger, TU Dortmund University, DE
Authors: Lea Schönberger, Georg von der Brüggen, Horst Schirmeier and Jian-Jia Chen, Technical University of Dortmund, DE

IP2-8 Vehicle Sequence Reordering with Cooperative Adaptive Cruise Control

Speaker: Yun-Yun Tsai, National Tsing Hua University, TW
Authors: Ta-Wei Huang[1], Yun-Yun Tsai[1], Chung-Wei Lin[2] and Tsung-Yi Ho[1]
[1]National Tsing Hua University, TW; [2]National Taiwan University, TW

IP2-9 Using Statistical Model Checking to Assess Reliability for Bathtub-Shaped Failure Rates

Speaker and Author: Josef Strnadel, Brno University of Technology, CZ

IP2-10 Empirical Evaluation of IC3-based Model Checking Techniques on Verilog RTL Designs

Speaker: Aman Goel, University of Michigan, US
Authors: Aman Goel and Karem Sakallah, University of Michigan, US

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IP2-11 **Co-design Implications of On-Demand-Acceleration for Cloud Healthcare Analytics: The AEGLE approach**
Speaker: Konstantina Koliogeorgi, National Technical University of Athens, GR
Authors: Dimosthenis Masouros[1], Konstantina Koliogeorgi[1], Georgios Zervakis[1], Alexandra Kosvyra[2], Achilleas Chytas[2], Sotirios Xydis[1], Ioanna Chouvarda[2] and Dimitrios Soudris[3]
[1]National Technical University of Athens, GR; [2]Aristotle University of Thessaloniki, GR; [3]Democritus University of Thrace, GR

IP2-12 **Modular FPGA Acceleration of Data Analytics in Heterogenous Computing**
Speaker: Christoforos Kachris, ICCS-NTUA, GR
Authors: Christoforos Kachris, Dimitrios Soudris and Elias Koromilas, Democritus University of Thrace, GR

IP2-13 **ACDC: An Accuracy- and Congestion-aware Dynamic Traffic Control Method for Networks-on-Chip**
Speaker: Siyuan Xiao, South China University of Technology, CN
Authors: Siyuan Xiao[1], Xiaohang Wang[1], Maurizio Palesi[2], Amit Kumar Singh[3] and Terrence Mak[4]
[1]South China University of Technology, CN; [2]University of Catania, IT; [3]University of Essex, GB; [4]University of Southampton, GB

IP2-14 **Power and Performance Optimal NoC Design for CPU-GPU Architecture Using Formal Models**
Speaker: Nader Bagherzadeh, University of California Irvine, US
Authors: Lulwah Alhubail and Nader Bagherzadeh, University of California - Irvine, US

IP2-15 **Deep Learning-Based Circuit Recognition Using Sparse Mapping and Level-Dependent Decaying Sum Circuit Representation**
Speaker: Massoud Pedram, University of Southern California, US
Authors: Arash Fayyazi, Soheil Shababi, Pierluigi Nuzzo, Shahin Nazarian and Massoud Pedram, University of Southern California, US

IP2-16 **Partial Encryption of Behavioral IPs to Selectively Control the Design Space in High-Level Synthesis**
Speaker: Zi Wang, The University of Texas at Dallas, US
Authors: Zi Wang and Benjamin Carrion Schaefer, The University of Texas at Dallas, US

IP2-17 **Software-Hardware Co-Design of Multi-Standard Digital Baseband Processor for IoT**
Speaker: Carolynn Bernier, CEA-Leti, FR
Authors: Hela Belhadj Amor and Carolynn Bernier, CEA, LETI, FR

IP2-18 **Taming Data Caches for Predictable Execution on GPU-based SoCs**
Speaker: Björn Forsberg, ETH Zürich, CH
Authors: Björn Forsberg[1], Luca Benini[2] and Andrea Marongiu[2]
[1]ETH Zürich, CH; [2]Università di Bologna, IT

IP2-19 **Design and Evaluation of SmallFloat SIMD extensions to the RISC-V ISA**
Speaker: Giuseppe Tagliavini, Università di Bologna, IT
Authors: Giuseppe Tagliavini[1], Stefan Mach[2], Davide Rossi[1], Andrea Marongiu[1] and Luca Benini[1]
[1]Università di Bologna, IT; [2]ETH Zurich, CH

IP2-20 **vDARM: Dynamic Adaptive Resource Management for Virtualized Multiprocessor Systems**
Speaker: Jianmin Qian, Shanghai Jiao Tong University, CN
Authors: Jianmin Qian, Jian Li, Ruhui Ma and Haibing Guan, Shanghai Jiao Tong University, CN

6.1 Special Day on "Embedded Meets Hyperscale and HPC" Session: Near-memory computing

Room 1 1100 – 1230

Chair: Christoph Hagleitner, IBM Research, CH
Co-Chair: Christian Plessl, Paderborn University, DE

While it used to be easy to increase the peak computational capabilities of processors by exploiting the growth in available transistors delivered by Moore's law, the latency and bandwidth of the memory system did not improve at the same pace. Today's microprocessors hide this fact behind a complex memory hierarchy, but often fail to optimally utilize the available memory bandwidth across a broad range of applications. Near-memory computing takes a fresh look at the memory system and proposes innovations ranging from micro-architecture to the runtime system to address these bottlenecks and build more balanced computing systems.

1100 **NTX: An energy-efficient streaming accelerator for floating-point generalized reduction workloads in 22nm FD-SOI**
Speaker: Luca Benini, IIS, ETH Zürich, CH
Authors: Fabian Schuiki, Michael Schaffner and Luca Benini, IIS, ETH Zürich, CH

1130 **Near-Memory Processing: It's the Hardware AND Software, Silly!**
Speaker and Author: Boris Grot, University of Edinburgh, GB

1200 **Coherently Attached Programmable Near-Memory Acceleration Platform and its application to Stencil Processing**
Speaker: Jan van Lunteren, IBM Research Zurich, CH
Authors: Jan van Lunteren, Ronald Luijten, Dionysios Diamantopoulos, Florian Auernhammer, Christoph Hagleitner, Lorenzo Chelini, Stefano Corda and Gagandeep Singh, IBM Research Zurich, CH

1230 **Lunch Break** in Lunch Area

6.2 Special Session: 3D Sensor - Hardware to Application

Room 2 1100 – 1230

Organisers:
Pascal Vivet, CEA-Leti, FR
Saibal Mukhopadhyay, Georgia Institute of Technology, US

Chair: Fabien Clermidy, CEA-Leti, FR
Co-Chair: Pascal Vivet, CEA-Leti, FR

The 3D integration has emerged as a key enabler to continue performance growth of Moore's law. An application where 3D has already shown potential for tremendous benefit is the design of high-throughput and/or energy-efficient sensors. The ability to stack heterogeneous components in a small volume coupled with potential for highly parallel access between sensing and processing has fueled new generation of senor platforms. Moreover, close proximity of processing and sensing has also lead to innovations in designing smart systems with in-built intelligence. This session will present four talks illustrating how 3D integration creates a platform for designing innovative sensors for applications ranging from high-performance imaging to ultra-low-power IoT platforms to bio-sensing. The first two talks will focus on application of 3D integration to high-performance and smart imaging. The first will present a detailed overview of recent advancements in 3D image sensor design, while the second talk will discuss the feasibility of embedding machine learning based feedback control within a 3D image sensor to create highly intelligent cameras. The third talk will present the concept of mm-scale sensors through 3D die stacking for ultra-low-power applications. Finally, the fourth talk will discuss design of innovative biosensors using fine-grain 3D integration.

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1100 **Advanced 3D Technologies and Architectures for 3D Smart Image Sensors**
Speaker: Pascal Vivet, CEA-Leti, FR
Authors: Pascal Vivet[1], Gilles Sicard[1], Laurent Millet[1], Stephane Chevobbe[2], Karim Ben Chehida[2], Luis Angel Cubero MonteAlegre[1], Maxence Bouvier[1], Alexandre Valentian[1], Maria Lepecq[2], Thomas Dombek[2], Olivier Bichler[2], Sebastien Thuriès[1], Didier Lattard[1], Cheramy Séverine[1], Perrine Batude[1] and Fabien Clermidy[1]
[1]CEA-Leti, FR; [2]CEA-LIST, FR

1122 **A Camera with Brain - Embedding Machine Learning in 3D**
Speaker: Saibal Mukhopadhyay, Georgia Institute of Technology, US
Authors: Burhan Ahmad Mudassar, Priyabrata Saha, Yun Long, Muhammad Faisal Amir, Evan Gebhardt, Taesik Na, Jong Hwan Ko, Marilyn Wolf and Saibal Mukhopadhyay, Georgia Institute of Technology, US

1144 **IoT2 - the Internet of Tiny Things: Realizing mm-scale sensors through 3D die stacking**
Speaker: David Blaauw, University of Michigan, US
Authors: Sechang Oh, Minchang Cho, Xiao Wu, Yejoong Kim, Li-Xuan Chuo, Wootaek Lim, Pat Pannuto, Suyoung Bang, Kaiyuan Yang, Hun-Seok Kim, Dennis Sylvester and David Blaauw, University of Michigan, US

1206 **3D Interconnects and Integration technologies for Biosensor Systems**
Speaker and Author: Muhannad Bakir, Georgia Institute of Technology, US

1230 **Lunch Break** in Lunch Area

6.3 When Approximation Meets Dependability

Room 3 1100 – 1230

Chair: George Constantinides, Imperial College London, GB
Co-Chair: Rishad Shafik, Newcastle University, GB

Approximation and dependability are conflicting design requirements. To meet performance, dependability and/or power trade-offs require approaches with insightful analysis and design methodologies. This session presents approximation driven paradigms in designing arithmetic units and developing fault detection schemes using machine learning.

1100 **Sensor-Based Approximate Adder Design for Accelerating Error-Tolerant and Deep-Learning Applications**
Speaker: Ning-Chi Huang, National Chiao Tung University, TW
Authors: Ning-Chi Huang, Szu-Ying Chen and Kai-Chiang Wu, Department of Computer Science, National Chiao Tung University, TW

1130 **Low-Power Variation-Aware Cores based on Dynamic Data-Dependent Bitwidth Truncation**
Speaker: Ioannis Tsiokanos, Queen's University Belfast, GB
Authors: Ioannis Tsiokanos, Lev Mukhanov and Georgios Karakonstantis, Queen's University Belfast, GB

1200 **A Smart Fault Detection Scheme for Reliable Image Processing Applications**
Speaker: Luca Cassano, Politecnico di Milano, IT
Authors: Matteo Biasielli, Cristiana Bolchini, Luca Cassano and Antonio Miele, Politecnico di Milano, IT

IPs **IP3-1**

1230 **Lunch Break** in Lunch Area

6.4 Hardware support for microarchitecture performance

Room 4 1100 – 1230

Chair: Cristina Silvano, Politecnico di Milano, IT
Co-Chair: Sylvain Collange, INRIA/IRISA, FR

This session deals with hardware mechanisms for high-performance or embedded real-time processors to improve their efficiency or their performance beyond what is possible to achieve by software. The first paper proposes low-overhead hardware support to enhance system interrupts checking multicore contentions. The second paper reduces the costly instruction scheduling operations in aggressive OoO processors. The third paper is about dynamic analysis of instruction flow and generating vectorized code at runtime.

1100 **Maximum-Contention Control Unit (MCCU): Resource Access Count and Contention Time Enforcement**
Speaker: Jordi Cardona, Univ. Politècnica de Barcelona and Barcelona Supercomputing Center, ES
Authors: Jordi Cardona[1], Carles Hernandez[2], Jaume Abella[2] and Francisco Cazorla[2]
[1]Barcelona Supercomputing Center and Universitat Politecnica de Catalunya, ES; [2]Barcelona Supercomputing Center, ES

1130 **FIFOrder MicroArchitecture: Ready-Aware Instruction Scheduling for OoO Processors**
Speaker: Mehdi Alipour, Uppsala University, SE
Authors: Mehdi Alipour[1], Rakesh Kumar[2], Stefanos Kaxiras[1] and David Black-Schaffer[1]
[1]Uppsala University, SE; [2]Norwegian University of Science and Technology, NO

1200 **Boosting SIMD Benefits through a Run-time and Energy Efficient DLP Detection**
Speaker: Mateus Rutzig, UFSM, BR
Authors: Michael Jordan, Tiago Knorst, Julio Vicenzi and Mateus Beck Rutzig, UFSM, BR

IPs **IP3-2, IP3-3, IP3-4**

1230 **Lunch Break** in Lunch Area

6.5 System Level Security

Room 5 1100 – 1230

Chair: Lionel Torres, University of Montpellier, FR
Co-Chair: Pascal Benoit, University of Montpellier, FR

This session includes four papers on hardware based techniques to support security: to detect malware, to provide secure intermittent computation, to protect the kernel and to self-attest.

1100 **2SMaRT: A Two-Stage Machine Learning-Based Approach for Run-Time Specialized Hardware-Assisted Malware Detection**
Speaker: Houman Homayoun, George Mason University, US
Authors: Hossein Sayadi[1], Hosein Mohammadi Makrani[1], Sai Manoj Pudukotai Dinakarrao[1], Tinoosh Mohsenin[2], Avesta Sasan[1], Setareh Rafatirad[1] and Houman Homayoun[1]
[1]George Mason University, US; [2]University of Maryland Baltimore County, US

1130 **Secure Intermittent Computing Protocol: Protecting State Across Power Loss**
Speaker: Archanaa S. Krishnan, Virginia Tech, US
Authors: Archanaa S. Krishnan, Charles Suslowicz, Daniel Dinu and Patrick Schaumont, Virginia Tech, US

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1200 **RiskiM: Toward Complete Kernel Protection with Hardware Support**
Speaker: Dongil Hwang, Seoul National University, KR
Authors: Dongil Hwang, Myonghoon Yang, Seongil Jeon, Younghan Lee, Donghyun Kwon and Yunheung Paek, Dept. of Electrical and Computer Engineering and Inter-University Semiconductor Research Center (ISRC), Seoul National University, KR

1215 **SACHa: Self-Attestation of Configurable Hardware**
Speaker: Jo Vliegen, imec-COSIC/ESAT, KU Leuven, BE
Authors: Jo Vliegen[1], Md Masoom Rabbani[2], Mauro Conti[2] and Nele Mentens[1]
[1]KU Leuven, BE; [2]University of Padua, IT

IPs **IP3-5, IP3-6**

1230 **Lunch Break** in Lunch Area

6.6 Intelligent Wearable and Implantable Sensors for Augmented Living

Room 6 1100 – 1230

Chair: Daniela De Venuto, Politecnico di Bari, IT
Co-Chair: Theocharis Theocharides, University of Cyprus, CY

This session brings together a set of novel technologies that exploit artificial intelligence and data analytics on low-power wearable and implantable sensors, for real-time augmented living and assistive healthcare.

1100 **Laelaps: An Energy-Efficient Seizure Detection Algorithm from Long-term Human iEEG Recordings without False Alarms**
Speaker: Alessio Burrello, Department of Information Technology and Electrical Engineering, ETH Zurich, CH
Authors: Alessio Burrello[1], Lukas Cavigelli[1], Kaspar Schindler[2], Luca Benini[1] and Abbas Rahimi[1]
[1]Department of Information Technology and Electrical Engineering, ETH Zurich, CH; [2]Sleep-Wake-Epilepsy-Center, Department of Neurology, Inselspital, Bern University Hospital, University Bern., CH

1130 **Automatic Time-Frequency Analysis of MRPs for Mind-controlled Mechatronic Devices**
Speaker: Giovanni Mezzina, Politecnico di Bari, IT
Authors: Daniela De Venuto and Giovanni Mezzina, Politecnico di Bari, IT

1200 **A Self-Learning Methodology for Epileptic Seizure Detection with Minimally-Supervised Edge Labeling**
Speaker: Damián Pascual, EPFL, CH
Authors: Damián Pascual[1], Amir Aminifar[2] and David Atienza[1]
[1]EPFL, CH; [2]Swiss Federal Institute of Technology Lausanne (EPFL), CH

IPs **IP3-7, IP3-8, IP3-9, IP3-10**

1230 **Lunch Break** in Lunch Area

6.7 How Secure and Verified is your Cyber-Physical System?

Room 7 1100 – 1230

Chair: Wanli Chang, University of York, GB
Co-Chair: Mingsong Chen, East China Normal University, CN

The session addresses security and verification aspects for the design of modern cyber-physical systems. Conditional Generative Adversarial Networks are used to increase security. Lightweight machine learning is used to detect malware at network node level. Stochastic model predictive control is used to limit malware diffusion in the network. Bounded model checking with linear programming is used for on-line verification of the cyber-physical system.

1100 **GAN-Sec: Generative Adversarial Network Modeling for the Security Analysis of Cyber-Physical Production Systems**
Speaker: Mohammad Al Faruque, University of California, Irvine, US
Authors: Sujit Rokka Chhetri, Anthony Bahadir Lopez, Jiang Wan and Mohammad Al Faruque, University of California, Irvine, US

1130 **Lightweight Node-level Malware Detection and Network-level Malware Confinement in IoT Networks**
Speaker: Sai Manoj Pudukotai Dinakarrao, George Mason University, US
Authors: Sai Manoj Pudukotai Dinakarrao, Hossein Sayadi, Hosein Mohammadi Makrani, Cameron Nowzari, Setareh Rafatirad and Houman Homayoun, George Mason University, US

1200 **Incremental Online Verification of Dynamic Cyber-Physical Systems**
Speaker: Lei Bu, Nanjing University, CN
Authors: Lei Bu[1], Shaopeng Xing[1], Xinyue Ren[1], Yang Yang[1], Qixin Wang[2] and Xuandong Li[1]
[1]Nanjing University, CN; [2]Dept. of Computing, The Hong Kong Polytechnic Univ., HK

1215 **Self-Secured Control with Anomaly Detection and Recovery in Automotive Cyber-Physical Systems**
Speaker: Korosh Vatanparvar, University of California, Irvine, US
Authors: Korosh Vatanparvar and Mohammad Al Faruque, University of California, Irvine, US

1230 **Lunch Break** in Lunch Area

6.8 TETRAMAX: Smart funding for digitalization of Europe's Industry

Exhibition Theatre 1100 – 1230

Organisers:
Luca Fanucci, University of Pisa, IT
Bernd Janson, ZENIT GmbH, DE

Moderator: Luca Fanucci, University of Pisa, IT

One of the most demanding challenge for Europe's Industry is to implement information technologies. Besides technical problems during the installation and replacement of analogue processes, digitalization touches the whole process of interaction and exchange in and outside companies. Threats like hacks with misuse of personal data, system blackouts or lack of qualified IT experts are heavily discussed and prevent many players, especially smaller SMEs, from fostering digitalization so far. But even if all those problems will be solved the question about the contribution of digitalization to CO2 reduction and lower energy consumption is still remaining. New promising innovations like blockchain technologies seem to completely fail at least from the energy saving point of view. To receive solutions for all aspects of digitalization with focus on Cyber Physical Systems (CPS) and via the instrument of Digital Innovation Hubs (DIH) the European Commission started its Smart Anything Everywhere (SAE) Initiative to foster transfer from research to business. The Horizon 2020 Innovation Action TETRAMAX is one of them offering smart and individual funding schemes for European university-industry cooperation. The technology transfer concept focuses on direct cooperation - Technology Transfer Experiments (TTX) - between universities and SMEs supported by open innovation networks and other stakeholders like investors. The session speakers will demonstrate in a pragmatic way and by use of concrete examples how technology transfer can be initiated and implemented in practice and to overcome the associated pitfalls and use the innovation opportunities. Amongst others, the goal is to motivate more stakeholders to engage in international technology transfer and become part of TETRAMAX.

During the session, TETRAMAX representatives will share their experiences and insights as researcher, founder, entrepreneur, investor or consultant.

1100 **Presentation of TETRAMAX**
Speaker: Rainer Leupers, RWTH Aachen, DE

1115 **EVERMORE**
Speaker: Davide Rossi, Università di Bologna, IT

1130 **Carrots**
Speaker: Antonio Solinas, Lifely, IT

1145 **TETRaWIN**
Speaker: Neven Rusković, Spica Sustativi d.o.o., HR

1200 **EuroLab4HPC - Joining forces towards European leadership in Exascale computing systems**
Speaker: Per Stenström, Chalmers University of Technology, SE

1215 **Open innovation business based on efficient networking**
Speaker: Bernd Janson, ZENIT GmbH, DE

1230 **Lunch Break** in Lunch Area

7.0 LUNCHTIME KEYNOTE SESSION

Room 1 1345 – 1420
supported by IEEE CEDA

Chair: Christoph Hagleitner, IBM Research, CH
Co-Chair: Christian Plessl, Paderborn University, DE

1345 **IEEE CEDA Luncheon Announcement**
Speaker: David Atienza, EPFL, CH

1350 **Heterogeneous, High Scale Computing in the Era of Intelligent, Cloud-Connected Devices**
Speaker: David Pellerin, Amazon, US

→ See Page 9

7.1 Special Day on "Embedded Meets Hyperscale and HPC" Session: Tools and Runtime Systems

Room 1 1430 – 1600

Chair: Christian Plessl, Paderborn University, DE
Co-Chair: Christoph Hagleitner, IBM Research, CH

Programming and operating heterogeneous computing systems that use multiple computing resources poses additional challenges to the programmer, e.g. handling different programming and execution models, partitioning application to exploit the strength of each resource type, or modeling and optimizing the overall and efficiency. In this session, we will discuss tools and runtime systems that support the developer with these tasks by raising the level of abstraction for application specification

1430 **Extreme Heterogeneity in High Performance Computing**
Speaker and Author: Jeffrey S Vetter, Oak Ridge National Laboratory, US

1500 **Homogenizing Heterogeneity: the OmpSs approach**
Speaker and Author: Jesus Labarta, Barcelona Supercomputing Center, ES

1530 **Automatic code restructuring for FPGAs: current status, trends and open issues**
Speaker and Author: João M. P. Cardoso, University of Porto/FEUP, PT

1600 **Coffee Break** in Exhibition Area

7.2 Accelerators using novel memory technologies

Room 2 1430 – 1600

Chair: Mladen Berekovic, TU Braunschweig, DE
Co-Chair: Andrea Marongiu, Università di Bologna, IT

The session focuses on accelerating three complex applications. They all use novel combination of memory and computing elements to achieve this goal. The first paper focuses on pattern matching and proposes to use resistive-RAM (RRAM) to accelerate an Automata Processor (AP). The second one focuses on Homomorphic Encryption (HE) and improves the performance and energy consumption using near-data processing on a 3D-stacked memory (Hybrid Memory Cube). The third paper focuses on Inference (DCNN) proposes a 3D-stacked neuromorphic architecture consisting of Processing Elements and multiple DRAM layers.

1430 **Time-division Multiplexing Automata Processor**
Speaker: Jintao Yu, Delft University of Technology, NL
Authors: Jintao Yu, Hoang Anh Du Nguyen, Muath Abu Lebdeh, Mottaqiallah Taouil and Said Hamdioui, Delft University of Technology, NL

1500 **Near-Data Acceleration of Privacy-Preserving Biomarker Search with 3D-Stacked Memory**
Speaker: Alvin Oliver Glova, University of California, Santa Barbara, US
Authors: Alvin Oliver Glova, Itir Akgun, Shuangchen Li, Xing Hu and Yuan Xie, University of California, Santa Barbara, US

1530 **Towards Cross-Platform Inference on Edge Devices with Emerging Neuromorphic Architecture**
Speaker: Yi Wang, Shenzhen University, CN
Authors: Shangyu Wu[1], Yi Wang[1], Amelie Chi Zhou[1], Rui Mao[1], Zili Shao[2] and Tao Li[3]
[1]Shenzhen University, CN; [2]The Chinese University of Hong Kong, HK; [3]University of Florida, US

IPs **IP3-11, IP3-12, IP3-13**

1600 **Coffee Break** in Exhibition Area

7.3 CPU and GPU microarchitecture dependability

Room 3 1430 – 1600

Chair: Michail Maniatakos, NYU Abu Dhabi, UA
Co-Chair: Nikolaos Foutris, University of Manchester, GB

This session first focuses on the dependability of out-of-order processors and specifically in the register renaming sub-system and the L1 cache. Then, it analyzes the main requirements to enable ISO26262 ASIL-D compliance for Commercial Off-The-Shelf (COTS) GPUs.

1430 **Error-Shielded Register Renaming Subsystem for a Dynamically Scheduled Out-of-Order Core**
Authors: Ron Gabor[1], Yiannakis Sazeides[2], Arkady Bramnik[1], Alexandros Andreou[2], Chrysostomos Nicopoulos[2], Karyofyllis Patsidis[3], Dimitris Konstantinou[3] and Giorgos Dimitrakopoulos[3]
[1]Intel, IL; [2]University of Cyprus, CY; [3]Democritus University of Thrace, GR

1500 **LAEC: Look-Ahead Error Correction Codes in Embedded Processors L1 Data Cache**
Authors: Pedro Benedicte[1], Carles Hernandez[2], Jaume Abella[2] and Francisco Cazorla[2]
[1]Barcelona Supercomputing Center and Universitat Politècnica de Catalunya, ES; [2]Barcelona Supercomputing Center, ES

1530 **High-Integrity GPU Designs for Critical Real-Time Automotive Systems**
Speaker: Sergi Alcaide Portet, Universitat Politècnica de Catalunya - Barcelona Supercomputing Center, ES
Authors: Sergi Alcaide[1], Leonidas Kosmidis[2], Carles Hernandez[2] and Jaume Abella[2]
[1]Universitat Politècnica de Catalunya - Barcelona Supercomputing Center (BSC), ES; [2]Barcelona Supercomputing Center, ES

IPs **IP3-14, IP3-15**

1600 **Coffee Break** in Exhibition Area

7.4 Low Power Design: From Highly-Optimized Power Delivery Networks to CNN Accelerators

Room 4 1430 – 1600

Chair: Pascal Vivet, CEA-Leti, FR
Co-Chair: Andrea Bartolini, Università di Bologna, IT
The session presents four papers covering power optimization through the whole design stack. The first paper presents an innovative power mesh IR optimization in an advanced technology node. The second paper presents a new formulation and optimization strategy to get the best efficiency from on-chip switch cap converters for heterogeneous many cores. While the third paper presents an optimized power delivery network for 3D integrated systems. Finally, the fourth paper presents a power efficient accelerator based on associative CAMs for CNN inference.

1430 **Detailed Placement for IR Drop Mitigation by Power Staple Insertion in Sub-10nm VLSI**
Speaker: Minsoo Kim, UC San Diego, US
Authors: Sun ik Heo[1], Andrew Kahng[2], Minsoo Kim[3], Lutong Wang[3] and Chutong Yang[3]
[1]Samsung Electronics Co., Ltd., KR; [2]University of California San Diego, US; [3]UC San Diego, US

1500 **Optimizing the Energy Efficiency of Power Supply in Heterogeneous Multicore Chips with Integrated Switched-Capacitor Converters**
Speaker: Lu Wang, ShanghaiTech University, CN
Authors: Lu Wang[1], Leilei Wang[1], Dejia Shang[1], Cheng Zhuo[2] and Pingqiang Zhou[1]
[1]ShanghaiTech University, CN; [2]Zhejiang University, CN

1530 **Power Delivery Pathfinding for Emerging Die-to-Wafer Integration Technology**
Speaker: Seungwon Kim, Ulsan National Institute of Science and Technology, KR
Authors: Andrew B. Kahng[1], Seokhyeong Kang[2], Seungwon Kim[3], Kambiz Samadi[4] and Bangqi Xu[1]
[1]UC San Diego, US; [2]Pohang University of Science and Technology, KR; [3]Ulsan National Institute of Science and Technology (UNIST), KR; [4]Qualcomm Technologies, Inc., US

1545 **Energy-Efficient Convolutional Neural Networks via Recurrent Data Reuse**
Speaker: Luca Mocerino, Politecnico di Torino, IT
Authors: Luca Mocerino, Valerio Tenace and Andrea Calimera, Politecnico di Torino, IT

IPs **IP3-16**

1600 **Coffee Break** in Exhibition Area

7.5 Reliable and Persistent: From Cache to File system

Room 5 1430 – 1600

Chair: Chengmo Yang, University of Delaware, US
Co-Chair: Alexandre Levisse, EPFL - ESL, CH

This session integrates both hardware and software optimizations aiming at enhancing reliability and performance of non-volatile caches and main memory. The first paper proposes a novel cache design to completely eliminate the accumulation of read disturbances in STT-MRAM without compromising cache performance. The second paper makes adaptive page migration decisions between DRAM and NVRAM as workload changes and hot/cold pattern varies. The third paper aims to reduce write amplification caused by frequently-updated inodes in journaling file systems, while maintaining crash consistency using persistent memory.

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1430 **Enhancing Reliability of STT-MRAM Caches by Eliminating Read Disturbance Accumulation**
Speaker: Hossein Asadi, Sharif University of Technology, IR
Authors: Elham Cheshmikhani[1], Hamed Farbeh[2] and Hossein Asadi[1]
[1]Sharif University of Technology, IR; [2]Amirkabir University of Technology, IR

1500 **UIMigrate: Adaptive Data Migration for Hybrid Non-Volatile Memory Systems**
Speaker: Duo Liu, College of Computer Science, Chongqing University, CN
Authors: Yujuan Tan[1], Baiping Wang[1], Zhichao Yan[2], Qiuwei Deng[1], Xianzhang Chen[1] and Duo Liu[1]
[1]Chongqing University, CN; [2]University of Texas Arlington, CN

1530 **Reducing Write Amplification for Inodes of Journaling File Systems using Persistent Memory**
Speaker: Xianzhang Chen, Chongqing University, CN
Authors: Chaoshu Yang, Duo Liu, Xianzhang Chen, Runyu Zhang, Wenbin Wang, Moming Duan and Yujuan Tan, Chongqing University, CN

1600 **Coffee Break** in Exhibition Area

7.6 Optimization of Smart Energy Systems

Room 6 1430 – 1600

Chair: Davide Quaglia, University of Verona, IT
Co-Chair: Massimo Poncino, Politecnico di Torino, IT

In this session, three approaches to optimizing smart grid and photovoltaic systems are presented, targeting cost, efficiency, and privacy.

1430 **Cost/Privacy Co-optimization in Smart Energy Grids**
Speaker: Alma Proebstl, TUM, DE
Authors: Alma Proebstl, Sangyoung Park, Sebastian Steinhorst and Samarjit Chakraborty, TUM, DE

1500 **A Low-Complexity Framework for Distributed Energy Market Targeting Smart-Grid**
Speaker: Kostas Siozios, Dept. of Physics, Aristotle University of Thessaloniki, GR
Authors: Kostas Siozios and Stylianos Siskos, Department of Physics, Aristotle University of Thessaloniki, GR

1530 **Irradiance-Driven Partial Reconfiguration of PV Panels**
Speaker: Enrico Macii, Politecnico di Torino, IT
Authors: Daniele Jahier Pagliari, Sara Vinco, Enrico Macii and Massimo Poncino, Politecnico di Torino, IT

IPs **IP3-17**

1600 **Coffee Break** in Exhibition Area

7.7 Toward Correct and Secure Embedded Systems

Room 7 1430 – 1600

Chair: Todd Austin, University of Michigan, US
Co-Chair: Ylies Falcone, University Grenoble Alpes, FR

This session will explore novel techniques for developing embedded systems with strong assurances of correctness and security. The correctness topics explored include verification of execution deadlines and correctness enforcement in the field. The security topics to be explored include efficient behavioral analysis of malware, improved protection of machine learning algorithms from adversarial attacks, and zero-footprint hardware Trojan attacks.

1430 **Better Late Than Never Verification of Embedded Systems After Deployment**
Authors: Martin Ring[1], Fritjof Bornebusch[1], Christoph Lüth[1], Robert Wille[2] and Rolf Drechsler[1]
[1]University of Bremen, DE; [2]Johannes Kepler University Linz, AT

1500 **Efficient Computation of Deadline-Miss Probability and Potential Pitfalls**
Speaker: Kuan-Hsun Chen, TU Dortmund, DE
Authors: Kuan-Hsun Chen, Niklas Ueter, Georg von der Brüggen and Jian-Jia Chen, Technical University of Dortmund, DE

1515 **FAdeML: Understanding the Impact of Pre-Processing Noise Filtering on Adversarial Machine Learning**
Speaker: Faiq Khalid, Department of computer engineering, TU Wien, AT
Authors: Faiq Khalid[1], Muhammad Abdullah Hanif[1], Semeen Rehman[1], Junaid Qadir[2] and Muhammad Shafique[1]
[1]Vienna University of Technology (TU Wien), AT; [2]Information Technology University, Lahore, PK

1530 **Real-Time Anomalous Branch Behavior Inference with a GPU-inspired Engine for Machine Learning Models**
Speaker: Hyunyoung Oh, Seoul National University, KR
Authors: Hyunyoung Oh[1], Hayoon Yi[1], Hyeokjun Choe[1], Yeongpil Cho[2], Sungroh Yoon[1] and Yunheung Paek[1]
[1]Seoul National University, KR; [2]Soongsil University, KR

1545 **TrojanZero: Switching Activity-Aware Design of Undetectable Hardware Trojans with Zero Power and Area Footprint**
Speaker: Imran Abbasi, NUST, PK
Authors: Imran Abbasi[1], Faiq Khalid[2], Semeen Rehman[2], Awais Kamboh[1], Axel Jantsch[2], Siddharth Garg[3] and Muhammad Shafique[2]
[1]NUST, PK; [2]Vienna University of Technology (TU Wien), AT; [3]University of Waterloo, CA

IPs **IP3-18**

1600 **Coffee Break** in Exhibition Area

7.8 Inspiring futures! Careers Session @ DATE (part 1)

Exhibition Theatre 1430 – 1600

Organisers:
Luca Fanucci, University of Pisa, IT
Rossano Massai, University of Pisa, IT
Xavier Salazar, Barcelona Supercomputing Center, ES

Moderator: Luca Fanucci, University of Pisa, IT

This session aims to bring together recruiters – mostly companies large and small, as well as universities and research centres – with potential jobseekers in the technology areas covered by DATE and HiPEAC.

The progamme will be tailored to the needs of the students and researchers. It will include:

- career insights and mentoring by the HiPEAC officer for recruitment activities and a careers advisor from a local university
- company pitches
- time for informal networking

1430 **Academia or Industry? - or everything! Career and internship opportunities powered by HiPEAC**
Speaker: Xavier Salazar, Barcelona Supercomputing Center, ES

1445 **How to kick start your career in an ever-changing world**
Speaker: Antonella Magliocchi, University of Pisa, IT

1515 **Inspiring Futures @ Infineon Technologies**
Speaker: Simone Fontanesi, Infineon Technologies, AT

1530 **Inspiring Futures @ Cadence**
Speaker: Anton Klotz, Cadence Design Systems, DE

1545 **Inspiring Futures @ eSilicon**
Speaker: Fernando De Bernardinis, eSilicon, IT

1600 **Coffee Break** in Exhibition Area

IP3 Interactive Presentations

Poster Area 1600 – 1630
supported by Cadence Academic Network

Interactive Presentations run simultaneously during a 30-minute slot. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session.

IP3-1 **Non-Intrusive Self-Test Library for Automotive Critical Applications: Constraints and Solutions**
Speaker: Ernesto Sanchez, Politecnico di Torino, IT
Authors: Paolo Bernardi[1], Riccardo Cantoro[1], Andrea Floridia[1], Davide Piumatti[1], Cozmin Pogonea[1], Annachiara Ruospo[1], Ernesto Sanchez[1], Sergio De Luca[2] and Alessandro Sansonetti[2]
[1]Politecnico di Torino, IT; [2]STMicroelectronics, IT

IP3-2 **Dependency-Resolving Intra-Unit Pipeline Architecture for High-Throughput Multipliers**
Speaker: Dae Hyun Kim, Washington State University, US
Authors: Jihee Seo and Dae Hyun Kim, Washington State University, US

IP3-3 **A Hardware-Efficient Logarithmic Multiplier with Improved Accuracy**
Authors: Mohammad Saeed Ansari, Bruce Cockburn and Jie Han, University of Alberta, CA

IP3-4 **Lightweight hardware support for selective coherence in heterogeneous manycore accelerators**
Speaker: Alessandro Cilardo, CeRICT, IT
Authors: Alessandro Cilardo, Mirko Gagliardi and Vincenzo Scotti, University of Naples Federico II, IT

IP3-5 **Functional Analysis Attacks on Logic Locking**
Speaker: Pramod Subramanyan, Indian Institute of Technology Kanpur, IN
Authors: Deepak Sirone and Pramod Subramanyan, Indian Institute of Technology Kanpur, IN

IP3-6 **SigAttack: New High-level SAT-based Attack on Logic Encryptions**
Speaker: Hai Zhou, Northwestern University, US
Authors: Yuanqi Shen[1], You Li[1], Shuyu Kong[2], Amin Rezaei[1] and Hai Zhou[1]
[1]Northwestern University, US; [2]northwestern university, CN

IP3-7 **ZeroPowerTouch: Zero-Power Smart Receiver for Touch Communication and Sensing for Internet of Thing and Wearable Applications**
Speaker: Michele Magno, ETH Zurich, CH
Authors: Philipp Mayer, Raphael Strebel and Michele Magno, ETH Zurich, CH

IP3-8 **Tailoring SVM Inference for Resource-Efficient ECG-Based Epilepsy Monitors**
Speaker: Lorenzo Ferretti, Università della Svizzera italiana, CH
Authors: Lorenzo Ferretti[1], Giovanni Ansaloni[1], Laura Pozzi[1], Amir Aminifar[2], David Atienza[2], Leila Cammoun[3] and Philippe Ryvlin[3]
[1]USI Lugano, CH; [2]EPFL, CH; [3]Centre Hospitalier Universitaire Vaudois, CH

IP3-9 **An indoor localization system to detect areas causing the freezing of gait in Parkinsonians**
Speaker: Graziano Pravadelli, Dept. of Computer Science, Univ. of Verona, IT
Authors: Florenc Demrozi[1], Vladislav Bragoi[1], Federico Tramarin[2] and Graziano Pravadelli[1]
[1]Department of Computer Science, University of Verona, IT; [2]Department of Information Engineering, University of Padua, IT

IP3-10 **Assembly-Related Chip/Package Co-Design of Heterogeneous Systems Manufactured by Micro-Transfer Printing**
Speaker: Tilman Horst, Technische Universität Dresden, DE
Authors: Robert Fischbach, Tilman Horst and Jens Lienig, Technische Universität Dresden, DE

IP3-11 **Visual Inertial Odometry At the Edge - A Hardware-Software Co-design Approach for Ultra-low Latency and Power**
Speaker: Dipan Kumar Mandal, Intel Corporation, IN
Authors: Dipan Kumar Mandal[1], Srivatsava Jandhyala[1], Om J Omer[1], Gurpreet S Kalsi[1], Biji George[1], Gopi Neela[1], Santhosh Kumar Rethinagiri[1], Sreenivas Subramoney[1], Hong Wong[2], Lance Hacking[2] and Belliappa Kuttanna[2]
[1]Intel Corporation, IN; [2]Intel Corporation, US

IP3-12 **CapsAcc: An Efficient Hardware Accelerator for CapsuleNets with Data Reuse**
Speaker: Alberto Marchisio, Vienna University of Technology (TU Wien), AT
Authors: Alberto Marchisio, Muhammad Abdullah Hanif and Muhammad Shafique, Vienna University of Technology (TU Wien), AT

IP3-13 **SDCNN: An efficient sparse deconvolutional neural network accelerator on FPGA**
Speaker: Suk-Ju Kang, Sogang University, KR
Authors: Jung-Woo Chang, Keon-Woo Kang and Suk-Ju Kang, Sogang University, KR

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IP3-14 **A Fine-Grained Soft Error Resilient Architecture under Power Considerations**
Speaker: Sajjad Hussain, Chair for Embedded Systems, KIT, Karlsruhe, DE
Authors: Sajjad Hussain[1], Muhammad Shafique[2] and Joerg Henkel[1]
[1]Karlsruhe Institute of Technology, DE; [2]Vienna University of Technology (TU Wien), AT

IP3-15 **Fine-Grained Hardware Mitigation for Multiple Long-Duration Transients on VLIW Function Units**
Speaker: Angeliki Kritikakou, University of Rennes 1 - IRISA/INRIA, FR
Authors: Rafail Psiakis[1], Angeliki Kritikakou[1] and Olivier Sentieys[2]
[1]Univ Rennes/IRISA/INRIA, FR; [2]INRIA, FR

IP3-16 **Adaptive Word Reordering for Low-Power Inter-Chip Communication**
Speaker: Eleni Maragkoudaki, University of Manchester, GB
Authors: Eleni Maragkoudaki[1], Przemyslaw Mroszczyk[2] and Vasilis Pavlidis[3]
[1]University of Manchester, GB; [2]Qualcomm, IE; [3]The University of Manchester, GB

IP3-17 **Machine-Learning-Driven Matrix Ordering for Power Grid Analysis**
Speaker: Wenjian Yu, Tsinghua University, CN
Authors: Ganqu Cui[1], Wenjian Yu[1], Xin Li[2], Zhiyu Zeng[3] and Ben Gu[3]
[1]Tsinghua University, CN; [2]Duke University, US; [3]Cadence Design Systems, Inc., US

IP3-18 **Assertion-Based Verification through Binary Instrumentation**
Speaker: Laurence Pierre, Univ. Grenoble Alpes, FR
Authors: Enzo Brignon and Laurence Pierre, TIMA Lab (Univ. Grenoble Alpes, CNRS, Grenoble INP), FR

8.1 Special Day on "Embedded Meets Hyperscale and HPC" Panel: What can HPC and hyperscale learn from embedded computing

Room 1 1700 – 1830

Co-Chairs:
Christoph Hagleitner, IBM Research Zurich, CH
Christian Plessl, Paderborn University, DE

Despite their very different origins, HPC/datacenter technologies and applications face similar challenges than embedded computing. For example, embedded systems have used heterogeneous architectures with specialized co-processors for a very long time due to strict realtime or efficiency constraints. Hence, the EDA community has extensively studied models, algorithms and tools for application analysis, optimization and operation. In contrast, HPC and datacenters applications are designed to harvest the performance of networked, massively parallel but homogeneous computing resources. In this panel, our experts will debate with the audience, what the datacenter and embedded communities can learn from each other.

Panelists:
Peter Messmer, NVidia, US
Luca Benini, Università di Bologna, IT
Boris Grot, University of Edinburgh, GB
Jan van Lunteren, IBM Research Zurich, CH
Jeffrey S Vetter, Oak Ridge National Laboratory, US
Jesus Labarta, Barcelona Supercomputing Center, ES
João M. P. Cardoso, University of Porto/FEUP, PT
Babak Falsafi, EPFL, CH

8.2 Special Session: Innovative methods for verifying Systems-on-Chip: digital, mixed-signal, security and software

Room 2 1700 – 1830

Organisers:
Subhasish Mitra, Stanford University, US
Georges Gielen, KU Leuven, BE

Chair: Ulf Schlichtmann, TUM, DE
Co-Chair: Giovanni De Micheli, EPFL, CH

Modern-day integrated circuits can contain several billions of transistors, multiple cores and memories, several analog and mixed-signal blocks, etc. While designing such chips is a huge effort, their verification is a true nightmare. Traditional techniques require extremely long computation times and may fail to capture all bugs in the system. These problems are exacerbated by even more difficult challenges: hardware security (e.g. the recent Spectre/Meltdown attacks stemming from hardware designs), system safety (e.g. for automotive applications), and software complexity (firmware and software form a significant component of complex Systems-on-Chip). This special session focuses on novel approaches from industry and academia to overcome these seemingly insurmountable outstanding challenges. Most importantly, this session will discuss not only design bugs but also the new challenges (stated above) that design verification must address – major directions for the DATE research community.

1700 **Hardware and firmware verification and validation: an algorithm-to-firmware development methodology**
Speaker: Henry Cox, MediaTek, US
Authors: Henry Cox and Harry Chen, MediaTek, US

1730 **Processor Hardware Security Vulnerabilities and their Detection by Unique Program Execution Checking**
Speaker: Wolfgang Kunz, University of Kaiserslautern, DE
Authors: Mohammad Rahmani Fadiheh[1], Dominik Stoffel[1], Clark Barrett[2], Subhasish Mitra[2] and Wolfgang Kunz[1]
[1]University of Kaiserslautern, DE; [2]Stanford University, US

1800 **Symbolic QED Pre-silicon Verification for Automotive Microcontroller Cores: Industrial Case Study**
Speaker: Subhasish Mitra, Stanford University, US
Authors: Eshan Singh[1], Keerthikumara Devarajegowda[2], Sebastian Simon[3], Ralf Schnieder[3], Karthik Ganesan[1], Mohammad Fadiheh[4], Dominik Stoffel[4], Wolfgang Kunz[4], Clark Barrett[1], Wolfgang Ecker[5] and Subhasish Mitra[1]
[1]Stanford University, US; [2]Infineon Technologies AG/Technische Universität Kaiserslautern, DE; [3]Infineon Technologies, DE; [4]Technische Universität Kaiserslautern, DE; [5]Infineon Technologies AG/Technische Universität München, DE

1815 **Review of Methodologies for Pre- and Post-Silicon Analog Verification in Mixed-Signal SOCs**
Speaker: Georges Gielen, KU Leuven, BE
Authors: Georges Gielen[1], Nektar Xama[1], Karthik Ganesan[2] and Subhasish Mitra[2]
[1]KU Leuven, BE; [2]Stanford University, US

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8.3 Test Preparation and Generation

Room 3 1700 – 1830

Chair: Matteo Sonza Reorda, Politecnico di Torino, IT
Co-Chair: Grzegorz Mrugalski, Mentor, A Siemens Business, PL

Deep Neural Networks and Approximate Circuits are of increasing importance in many applications. They pose completely new challenges with respect to test generation. Promising approaches to face these challenges are presented by papers 1 and 4. Reconfigurable Scan Networks allow flexible access to embedded instruments for post-silicon test, validation and debug or diagnosis. On the other hand this creates security issues that have to be taken into account. Paper 2 provides an approach to guarantee secure data flow. Resynthesis for improving testability is the topic of paper 3.

1700 **On Functional Test Generation for Deep Neural Network IPs**
Speaker: Bo Luo, The Chinese University of Hong Kong, HK
Authors: Bo Luo, Yu Li, Lingxiao Wei and Qiang Xu, The Chinese University of Hong Kong, HK

1730 **On Secure Data Flow in Reconfigurable Scan Networks**
Speaker: Pascal Raiola, University of Freiburg, DE
Authors: Pascal Raiola[1], Benjamin Thiemann[1], Jan Burchard[2], Ahmed Atteya[3], Natalia Lylina[3], Hans-Joachim Wunderlich[3], Bernd Becker[1] and Matthias Sauer[1]
[1]University of Freiburg, DE; [2]Mentor, a Siemens Business, DE; [3]University of Stuttgart, DE

1800 **Resynthesis for Avoiding Undetectable Faults Based on Design-for-Manufacturability Guidelines**
Speaker: Naixing Wang, Purdue University, US
Authors: Naixing Wang[1], Irith Pomeranz[1], Sudhakar Reddy[2], Arani Sinha[3] and Srikanth Venkataraman[3]
[1]Purdue University, US; [2]University of Iowa, US; [3]Intel, US

1815 **Test Pattern Generation for Approximate Circuits Based on Boolean Satisfiability**
Speaker: Anteneh Gebregiorgis, Karlsruhe Institute of Technology, DE
Authors: Anteneh Gebregiorgis and Mehdi B. Tahoori, Karlsruhe Institute of Technology, DE

8.4 Applications of Reconfigurable Computing

Room 4 1700 – 1830

Chair: Suhaib Fahmy, University of Warwick, GB
Co-Chair: Marco Platzner, Paderborn University, DE

This session presents three papers that advance the state of the art in FPGA-based applications for autonomous driving, circuit analysis, and time-series data processing, and one interactive presentation on mapping deep neural networks to multi-FPGA platforms.

1700 **Adaptive Vehicle Detection for Real-time Autonomous Driving System**
Speaker: Maryam Hemmati, The University of Auckland, NZ
Authors: Maryam Hemmati[1], Morteza Biglari-Abhari[1] and Smail Niar[2]
[1]University of Auckland, NZ; [2]University of Valenciennes and Hainaut-Cambresis, FR

1730 **An Efficient FPGA-based Floating Random Walk Solver for Capacitance Extraction using SDAccel**
Speaker: Xin Wei, Fudan University, CN
Authors: Xin Wei[1], Changhao Yan[1], Hai Zhou[2], Dian Zhou[1] and Xuan Zeng[1]
[1]Fudan University, CN; [2]Northwestern University, US

1800 **Accelerating Itemset sampling using satisfiability constraints on FPGA**
Speaker: Mael Gueguen, Univ Rennes, Inria, CNRS, IRISA, FR
Authors: Mael Gueguen[1], Olivier Sentieys[2] and Alexandre Termier[1]
[1]Univ Rennes, CNRS, IRISA, FR; [2]INRIA, FR

IPs **IP4-1**

8.5 Don't Forget the Memory

Room 5 1700 – 1830

Chair: Christian Pilato, Politecnico di Milano, IT
Co-Chair: Olivier Sentieys, INRIA, FR

Multi-core systems demand new solutions to overcome the increasing memory gap and emerging memory technologies still need to find a suitable place in the traditional memory system. This session showcases different proposals covering memory, storage, and OS. The first presentation improves the parallelism of the Open-Channel SSD Linux implementation. The second presentation proposes a method to orchestrate multicore memory requests to maintain the main memory locality. The third presentation proposes a new method to improve directory entry lookup in deep directory structures. An interactive presentation completes the session with a new cache replacement algorithm for NVM disk read caches.

1700 **DS-Cache: A Refined Directory Entry Lookup Cache with Prefix-Awareness for Mobile Devices**
Speaker: Zhaoyan Shen, Shandong University, CN
Authors: Lei Han[1], Bin Xiao[1], Xuwei Dong[2], Zhaoyan Shen[3] and Zili Shao[4]
[1]The Hong Kong Polytechnic University, HK; [2]Northwestern Polytechnical University, CN; [3]Shandong University, CN; [4]The Chinese University of Hong Kong, HK

1730 **Improving the DRAM Access Efficiency for Matrix Multiplication on Multicore Accelerators**
Speaker: Sheng Ma, National University of Defense Technology, CN
Authors: Sheng Ma, Yang Guo, Shenggang Chen, Libo Huang and Zhiying Wang, National University of Defense Technology, CN

1800 **QBLK: Towards Fully Exploiting the Parallelism of Open-Channel SSDs**
Speaker: Hongwei Qin, Wuhan National Laboratory for Optoelectronics, Key Laboratory of Information Storage System, Engineering Research Center of data storage systems and Technology, Ministry of Education of China, School of Computer Science and Technology, Huazhong University, CN
Authors: Hongwei Qin, Dan Feng, Wei Tong, Jingning Liu and Yutong Zhao, Wuhan National Lab for Optoelectronics, CN

IPs **IP4-2, IP4-3**

8.6 Robotics and Industry 4.0

Room 6 1700 – 1830

Chair: Federica Ferraguti, University of Modena-Reggio, IT
Co-Chair: Armin Schoenlieb, Infineon Technologies, AT

This session presents new results in the field of robotics and cyberphysical systems applied to Industry 4.0. The session includes theoretical results as well as evaluation of relevant use-cases.

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1700 **A methodology for comparative analysis of collaborative robots for Industry 4.0**
Speaker: Marcello Bonfè, University of Ferrara, IT
Authors: Federica Ferraguti[1], Andrea Pertosa[1], Cristian Secchi[1], Cesare Fantuzzi[1] and Marcello Bonfè[2]
[1]University of Modena and Reggio Emilia, IT; [2]University of Ferrara, IT

1730 **Hybrid Sensing Approach For Coded Modulation Time-of-Flight Cameras**
Speaker: Armin Schoenlieb, Infineon Technologies, AT
Authors: Armin Schoenlieb[1], Hannes Plank[1], Christian Steger[2], Gerald Holweg[1] and Norbert Druml[1]
[1]Infineon Technologies, AT; [2]Graz University of Technology, AT

1800 **Communication-Computation co-Design of Decentralized Task Chain in CPS Applications**
Speaker: Eli Bozorgzadeh, University of California, Irvine, US
Authors: Seyyed Ahmad Razavi, Eli Bozorgzadeh and Solmaz Kia, University of California, Irvine, US

1815 **Resource Manager for Scalable Performance in ROS Distributed Environments**
Speaker: Daisuke Fukutomi, Ritsumeikan University, JP
Authors: Daisuke Fukutomi[1], Takuya Azumi[2], Shinpei Kato[3] and Nobuhiko Nishio[1]
[1]Ritsumeikan University, JP; [2]Saitama University, JP; [3]The University of Tokyo, JP

IPs **IP4-4, IP4-5, IP4-6**

8.7 Embedded hardware architectures for deep neural networks

Room 7 1700 – 1830

Chair: Sandeep Pande, IMEC-NL, NL
Co-Chair: Kyuho Lee, Ulsan National Institute of Science and Technology (UNIST), KR

This session presents papers that address various research challenges including optimization of deep neural networks for edge devices, multiplierless neural network acceleration, design space exploration of CNNs on FPGAs and accelerating local binary pattern networks on FPGAs.

1700 **Self-Supervised Quantization of Pre-Trained Neural Networks for Multiplierless Acceleration**
Speaker: Sebastian Vogel, Robert Bosch GmbH, DE
Authors: Sebastian Vogel[1], Jannik Springer[1], Andre Guntoro[1] and Gerd Ascheid[2]
[1]Robert Bosch GmbH, DE; [2]RWTH Aachen University, DE

1730 **Multi-objective Precision Optimization of Deep Neural Networks for Edge Devices**
Speaker: Nhut-Minh Ho, National University of Singapore, SG
Authors: Nhut-Minh Ho, Ramesh Vaddi and Weng-Fai Wong, National University of Singapore, SG

1800 **Towards Design Space Exploration and Optimization of Fast Algorithms for Convolutional Neural Networks (CNNs) on FPGAs**
Speaker: Muhammad Adeel Pasha, LUMS, PK
Authors: Afzal Ahmad and Muhammad Adeel Pasha, Department of Electrical Engineering, SBASSE, LUMS, PK

1815 **Accelerating Local Binary Pattern Networks with Software Programmable FPGAs**
Speaker: Jeng-Hau Lin, UC San Diego, US
Authors: Jeng-Hau Lin, Atieh Lotfi, Vahideh Akhlaghi, Zhuowen Tu and Rajesh Gupta, UC San Diego, US

IPs **IP4-7, IP4-8, IP4-9**

8.8 Inspiring futures! Careers Session @ DATE (part 2)

Exhibition Theatre 1700 – 1830

Organisers:
Luca Fanucci, University of Pisa, IT
Rossano Massai, University of Pisa, IT
Xavier Salazar, Barcelona Supercomputing Center, ES

Moderator: Luca Fanucci, University of Pisa, IT

This session aims to bring together recruiters – mostly companies large and small, as well as universities and research centres – with potential jobseekers in the technology areas covered by DATE and HiPEAC.

The progamme will be tailored to the needs of the students and researchers. It will include:

- career insights and mentoring by the HiPEAC officer for recruitment activities and a careers advisor from a local university
- company pitches
- time for informal networking

1700 **Inspiring Futures @ Microtest**
Speaker: Eluisa Ghilardi, Microtest, IT

1715 **Inspiring Futures @ Cobham Gaisler**
Speaker: Jan Andersson, Cobham Gaisler, SE

1730 **Inspiring Futures @ IngeniArs**
Speaker: Camila Giunti, IngeniArs, IT

1745 **Inspiring Futures @ Intel**
Speaker: Neslihan Kose Cihangir, Intel, DE

Party DATE Party | Networking Event

1930 – 2300

→ See Page 13

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9.1 Special Day on "Model-Based Design of Intelligent Systems" Session: Experiences from the trenches, model-based design at work

Room 1 0830 – 1000

Chair: Ingo Sander, KTH, SE
Co-Chair: Sander Stuijk, Eindhoven University of Technology, NL

0830 **Model Based Design at THALES: The current status and new challenges**
Speaker and Author: Laurent Rioux, Thales, FR

0900 **Model-Based Design for Controls, AI, and Communications in Intelligent Systems**
Speaker and Author: Pieter Mosterman, Mathworks, US

0930 **Model Driven Development of TWINSCAN software, but not from scratch**
Speaker and Author: Ramon Schiffelers, ASML, NL

1000 **Coffee Break** in Exhibition Area

9.2 High-Level Synthesis

Room 2 0830 – 1000

Chair: Yuko Hara-Azumi, Tokyo Institute of Technology, JP
Co-Chair: Jordi Cortadella, UPC, ES

In this session, we show how high-level synthesis (HLS) can be used to protected IPs and to exploit high-level information to predict the outcome of the physical design. First, the protection of a high-level IP model in a cloud-based synthesis context is discussed by using functional locking. The second talk investigates how the concepts of hardware Trojans can be used during HLS to add watermarks to IPs. A novel approach is then proposed to estimate the routing congestion at physical level during HLS. The interactive presentation discusses how to estimate the hardware cost and the software performance for the hardware/software interface.

0830 **Transient Key-based Obfuscation for HLS in an Untrusted Cloud Environment**
Speaker: Hannah Badier, ENSTA Bretagne, Lab-STICC, Brest, FR
Authors: Hannah Badier[1], Jean-Christophe Le Lann[1], Philippe Coussy[2] and Guy Gogniat[3]
[1]ENSTA Bretagne, FR; [2]Universite de Bretagne-Sud / Lab-STICC, FR; [3]Université Bretagne Sud, FR

0900 **High-Level Synthesis of Benevolent Trojans**
Speaker: Christian Pilato, Politecnico di Milano, IT
Authors: Christian Pilato[1], Kanad Basu[2], Mohammed Shayan[2], Francesco Regazzoni[3] and Ramesh Karri[2]
[1]Politecnico di Milano, IT; [2]NYU, US; [3]ALaRI, CH

0930 **Machine Learning Based Routing Congestion Prediction in FPGA High-Level Synthesis**
Speaker: Jieru Zhao, HKUST, CN
Authors: Jieru Zhao[1], Tingyuan Liang[2], Sharad Sinha[3] and Wei Zhang[1]
[1]Hong Kong University of Science and Technology, HK; [2]HKUST, CN; [3]Indian Institute of Technology Goa, IN

IPs **IP4-10, IP4-11, IP4-12, IP4-13**

1000 **Coffee Break** in Exhibition Area

9.3 Special Session: RISC-V or RISK-V? Towards Secure Open Hardware

Room 3 0830 – 1000

Chair: Georg Sigl, TUM, DE

The end of Moore's law is pushing the renewed interest on entirely new computing and System-on-Chip (SoC) design approaches to meet the requirements of largely diverse applications. Cloud computing, Internet-of-Things and artificial intelligence are pushing the development of a wide variety of complex SoCs that integrate heterogeneous IP hardware components from different providers. Especially when it comes to building complex, highly customized SoCs, it will be desirable that SoC designers could select verified, open source hardware blocks in the same manner that software developers are doing today. Open source hardware opens a path towards an ultra-fast design cycle for complex and highly customized SOCs. RISC-V is a free and open instruction set architecture (ISA), which enables a new era of processor innovation. RISC-V has captured attention of research and industrial communities; however security is still a main concern in this architecture. RISC-V allows the development of open source hardware with hardware security extensions and secure coprocessors able to be checked by many users at the source level. This could be a further driver to create open source secure RISC-V implementations. Such implementations must resist microarchitectural attacks such as Meltdown or Spectre. Currently researchers often try to fix the michroarchitecture security problems in closed source hardware with software, while their origin is in hardware. Open source hardware allows the development of countermeasures open to a wide research community in both hardware and software together, yielding to much more secure and performant solutions. On the other hand unsecure RISC-V implementations pose a major threat on our systems. In order to avoid that RISC-V becomes a security RISK-V, more research and development in both architectural and microarchitectural security solutions is required. This special session focuses on chances and risks offered by open source hardware based on RISC-V. A trend in modern SoCs is the integration of a dedicated security module with its own CPU which is hardened against attacks. RISC-V processors hardened against hardware attacks could be an ideal open source secure element, which can be easily integrated into SOCs, offering a transparent open source trust anchor for SOCs. The first talk will give an example how to secure RISC-V processors against hardware attacks. RISC-V currently lacks security features provided in standard processors such as trusted execution environments or enclaves. While all the known approaches in this area have known weaknesses the open source hardware project offers new chances to improve enclave's security by new concepts. This area will be covered by the second presentation. Security modules usually need accelerators for standardized cryptographic operations. How to integrate security coprocessors in a RISC-V system will be covered by the third talk. The last presentation will give an application example where RISC-V based processors are integrated in a SOC for both, the data processing as a multicore system and one additional as a hardware security module. The session consists of four presentations ranging from isolated on- or off-chip secure elements based on RISC-V, open-source projects for building trusted execution environments (TEE) with secure hardware enclaves based on the RISC-V, design of side-channel and fault attack resistant of crypto accelerators based on RISC-V and an application example using a RISC-V based SOC.

0830 **Protecting RISC-V Processors against Physical Side Channel Attacks**
Speaker: Stefan Mangard, Graz University of Technology, AT
Authors: Thomas Unterluggauer, Robert Schilling, Mario Werner and Stefan Mangard, Graz University of Technology, AT

0900 **Sanctorum: A lightweight security monitor for secure enclaves**
Speaker: Ilia Lebedev, MIT, US
Authors: Ilia Lebedev[1], Kyle Hogan[1], Jules Drean[1], David Kohlbrenner[2], Dayeol Lee[2], Krste Asanović[2], Dawn Song[2] and Srinivas Devadas[1]
[1]MIT, US; [2]UC Berkeley, US

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0930 **Towards Reliable and Secure Post-Quantum Co-Processor based on RISC-V**
Speaker: Johanna Sepulveda, TUM, DE
Authors: Tim Fritzmann[1], Uzair Sharif[1], Daniel Mueller-Gritschneder[1], Cezar Rodolfo Wedig Reinbrecht[2], Ulf Schlichtmann[1] and Johanna Sepulveda[1]
[1]TUM, DE; [2]UFRGS, BR

0945 **A Security Architecture for RISC-V based IoT Devices**
Speaker: Matthias Hiller, Fraunhofer AISEC, DE
Authors: Lukas Auer[1], Christian Skubich[2] and Matthias Hiller[1]
[1]Fraunhofer AISEC, DE; [2]Fraunhofer IIS / EAS, DE

1000 **Coffee Break** in Exhibition Area

9.4 Where do NoC and Machine Learning meet?

Room 4 0830 – 1000

Chair: Masoud Daneshtalab, Mälardalen University, SE
Co-Chair: Sébastien Le Beux, Lyon Institute of Nanotechnology, FR

The NoC design is being enhanced using machine intelligence technologies to drive system more efficiently. Denial-of-Service is one attack, caused by a malicious intellectual property core flooding the network, that can affect a NoC. In this session a lightweight and real-time DoS attack detection mechanism will be presented with timely attack detection and minor area and power overhead. Find a trade-offs among error rate, packet retransmission, performance, and energy is a very challenging topic. In this session a proactive fault-tolerant mechanism to optimize energy efficiency and performance with reinforcement learning (RL) will be proposed. Method to exploit the elasticity and noise-tolerance features of deep learning algorithms to circumvent the bottleneck of on-chip inter-core data moving and accelerate their execution will be discussed in this session. This method shows a better interconnects energy efficiency. Taking into account the fact that we can predict the destination of some packets ahead at the network interface we can establishes a highway from the source to the destination built up by reserving virtual channel. This mechanism can reduce the target packets' transfer latency and will be presented in this session.

0830 **Real-time Detection and Localization of DoS Attacks in NoC based SoCs**
Speaker: Subodha Charles, University of Florida, US
Authors: Subodha Charles, Yangdi Lyu and Prabhat Mishra, University of Florida, US

0900 **High-performance, Energy-efficient, Fault-tolerant Network-on-Chip Design Using Reinforcement Learning**
Speaker: Ke Wang, George Washington University, US
Authors: Ke Wang[1], Ahmed Louri[1], Avinash Karanth[2] and Razvan Bunescu[2]
[1]George Washington University, US; [2]Ohio University, US

0930 **Learn-to-Scale: Parallelizing Deep Learning Inference on Chip Multiprocessor Architecture**
Speaker: Kaiwei Zou, Institute of Computing Technology, Chinese Academy of Sciences, CN
Authors: Kaiwei Zou, Ying Wang, Huawei Li and Xiaowei Li, Institute of Computing Technology, Chinese Academy of Sciences, CN

0945 **Advance Virtual Channel Reservation**
Speaker: Boqian Wang, KTH Royal Institute of Technology, SE
Authors: Boqian Wang[1] and Zhonghai Lu[2]
[1]KTH Royal Institute of Technology, National University of Defense Technology, CN; [2]KTH Royal Institute of Technology, CN

1000 **Coffee Break** in Exhibition Area

9.5 Attacking Memory and I/O Bottlenecks

Room 5 0830 – 1000

Chair: Leonidas Kosmidis, Barcelona Supercomputing Center, ES
Co-Chair: Cristina Silvano, Politecnico di Milano, IT

Focusing on the memory hierarchy and memory and I/O bottlenecks, this session presents new techniques to better exploit the GPU cache memory by using new adaptive compression techniques, by enhancing the GPU cache utilization by exploiting non-frequently accessed blocks, and by proposing a new smart SSD-based I/O caching system. The papers in this section showcase new opportunities for alternative cache solutions.

0830 **SLC: Memory Access Granularity Aware Selective Lossy Compression for GPUs**
Speaker: Sohan Lal, Technical University of Berlin, DE
Authors: Sohan Lal, Jan Lucas and Ben Juurlink, Technical University of Berlin, DE

0900 **LoSCache: Leveraging Locality Similarity to Build Energy-Efficient GPU L2 Cache**
Speaker: Jingweijia Tan, Jilin University, CN
Authors: Jingweijia Tan[1], Kaige Yan[2], Shuaiwen Leon Song[3] and Xin Fu[4]
[1]Jilin University, CN; [2]College of Communication Engineering, Jilin University, CN; [3]Pacific Northwest National Laboratory, US; [4]University of Houston, US

0930 **LBICA: A Load Balancer for I/O Cache Architectures**
Speaker: Saba Ahmadian, Sharif University of Technology, IR
Authors: Saba Ahmadian, Reza Salkhordeh and Hossein Asadi, Sharif University of Technology, IR

IPs **IP4-14, IP4-15**

1000 **Coffee Break** in Exhibition Area

9.6 Reliability of highly-parallel architectures: an industrial perspective

Room 6 0830 – 1000

Chair: Doris Keitel-Schulz, Infineon Technologies, DE
Co-Chair: Fabien Clermidy, CEA, FR

This session addresses the issues of proving, verifying and enhancing highly-parallel designs on four different application domains ranging from Solid-State-Drive to 5G

0830 **AURIX TC277 Multicore Contention Model Integration for Automotive Applications**
Speaker: Jaume Abella, Barcelona Supercomputing Center (BSC), ES
Authors: Enrico Mezzetti[1], Luca Barbina[2], Jaume Abella[1], Stefania Botta[2] and Francisco Cazorla[1]
[1]Barcelona Supercomputing Center, ES; [2]Magneti Marelli S.p.A., IT

0900 **Seamless SoC Verification Using Virtual Platforms: An Industrial Case Study**
Speaker: Kyungsu Kang, Samsung Electronics, KR
Authors: Kyungsu Kang, Sangho Park, Byeongwook Bae, Jungyun Choi, SungGil Lee, Byunghoon Lee and Jong-Bae Lee, Samsung, KR

0930 **Multicore Early Design Stage Guaranteed Performance Estimates for the Space Domain**
Speaker: Mikel Fernandez, Barcelona Supercomputing Center, ES
Authors: Mikel Fernandez, Gabriel Fernandez, Jaume Abella and Francisco Cazorla, Barcelona Supercomputing Center, ES

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0945 **Polar Code Decoder Framework**
Speaker: Timo Lehnigk-Emden, Creonic GmbH, DE
Authors: Timo Lehnigk-Emden[1], Matthias Alles[1], Claus Kestel[2] and Norbert Wehn[2]
[1]Creonic GmbH, DE; [2]University of Kaiserslautern, DE

1000 **Coffee Break** in Exhibition Area

9.7 Runtime Predictability

Room 7 0830 – 1000

Chair: Rolf Ernst, TU Braunschweig, DE
Co-Chair: Gerhard Fohler, University of Kaiserslautern, DE

This session includes papers that address the runtime predictability at level of HW and SW. Potential applications are in the area of autonomous systems.

0830 **Increasing Accuracy of Timing Models: From CPA to CPA+**
Speaker: Leonie Köhler, TU Braunschweig, DE
Authors: Leonie Köhler[1], Borislav Nikolic[1], Marc Boyer[2] and Rolf Ernst[1]
[1]Technische Universität Braunschweig, DE; [2]ONERA, FR

0900 **Scratchpad Memories with Ownership**
Speaker: Martin Schoeberl, Technical Uniersity of Denmark, DK
Authors: Martin Schoeberl, Tórur Biskopstø Strøm, Oktay Baris and Jens Sparsø, Technical University of Denmark, DK

0930 **A Container-based DoS Attack-Resilient Control Framework for Real-Time UAV Systems**
Speaker: Jiyang Chen, University of Illinois at Urbana Champaign, US
Authors: Jiyang Chen[1], Zhiwei Feng[2], Jen-Yang Wen[1], Bo Liu[3] and Lui Sha[1]
[1]University of Illinois at Urbana-Champaign, US; [2]Northeastern University, CN; [3]NVIDIA, US

0945 **An Exact Schedulability Test for Non-Preemptive Self-Suspending Real-Time Tasks**
Speaker: Mitra Nasri, Delft University of Technology, NL
Authors: Beyazit Yalcinkaya[1], Mitra Nasri[1] and Björn Brandenburg[2]
[1]Max Planck Institute for Software Systems, DE; [2]MPI-SWS, DE

1000 **Coffee Break** in Exhibition Area

9.8 Special Session: IBM's Qiskit Tool Chain: Developing for and Working with Real Quantum Computers

Exhibition Theatre 0830 – 1000

Organiser: Robert Wille, Johannes Kepler University Linz, AT
Chair: Robert Wille, Johannes Kepler University Linz, AT

Quantum computers promise substantial speedups over conventional computers for many practical relevant applications such as quantum chemistry, optimization, machine learning, cryptography, quantum simulation, systems of linear equations, and many more. While considered "dreams of the future" for a long time, recent years have shown impressive accomplishments - leading to the first real quantum computers which can be utilized by everyone. A leading force within this development is IBM Research which launched the IBM Q Experience - the first industrial initiative to build universal quantum computers and make them accessible to a broad audience through a cloud access. In the meantime, a worldwide network of Fortune 500 companies, academic institutions, and startups work within this initiative and collaborate to advance quantum computing. This special session aims to foster this potential by introducing Qiskit to the EDA community as well as showcasing suc-

cess stories on how to develop new methods for as well as how to work with the tool - eventually allowing for efficiently and robustly executing algorithms on a real quantum computer. To this end, the special session covers all sides: IBM's own perspective on Qiskit and the IBM Q Experience, the developer view on how to develop new methods for Qiskit (sometimes outperforming IBM's own solutions using EDA expertise), as well as the user-view on how Qiskit and its extensions can be utilized to actually work with quantum computers.

0830 **Qiskit: An Overview of the Open-Source Framework for Quantum Computing**
Author: Yehuda Naveh, IBM Research, US

0900 **Developing for Qiskit: Introducing EDA Methods into the Toolkit**
Author: Robert Wille, Johannes Kepler University Linz, AT

0930 **Using Qiskit: NISQ-era Compilation for Qiskit**
Author: Rod Van Meter, Keio University, JP

1000 **Coffee Break** in Exhibition Area

IP4 Interactive Presentations

Poster Area 1000 – 1030
supported by Cadence Academic Network

Interactive Presentations run simultaneously during a 30-minute slot. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session.

IP4-1 **An Efficient Mapping Approach to Large-Scale DNNs on Multi-FPGA Architectures**
Speaker: Jiaxi Zhang, Peking University, CN
Authors: Wentai Zhang[1], Jiaxi Zhang[1], Minghua Shen[2], Guojie Luo[1] and Nong Xiao[3]
[1]Peking University, CN; [2]Sun Yat-sen University, CN; [3]Sun Yat-Sen University, CN

IP4-2 **A Write-Efficient Cache Algorithm based on Macroscopic Trend for NVM-based Read Cache**
Speaker: Ning Bao, Renmin University of China, CN
Authors: Ning Bao[1], Yunpeng Chai[1] and Xiao Qin[2]
[1]Renmin University of China, CN; [2]Auburn University, US

IP4-3 **SRAM Design Exploration with Integrated Application-Aware Aging Analysis**
Speaker: Alexandra Listl, TUM, DE
Authors: Alexandra Listl[1], Daniel Mueller-Gritschneder[2], Sani Nassif[3] and Ulf Schlichtmann[2]
[1]Chair of Electronic Design Automation, DE; [2]TUM, DE; [3]Radyalis, US

IP4-4 **From Multi-Level to Abstract-based Simulation of a Production Line**
Speaker: Stefano Centomo, University of Verona, IT
Authors: Stefano Centomo, Enrico Fraccaroli and Marco Panato, University of Verona, IT

IP4-5 **Accurate Dynamic Modelling of Hydraulic Servomechanisms**
Speaker: Manuel Pencelli, Yanmar R&D Europe S.r.l., IT
Authors: Manuel Pencelli[1], Renzo Villa[2], Alfredo Argiolas[1], Gianni Ferretti[2], Marta Niccolini[1], Matteo Ragaglia[1], Paolo Rocco[2] and Andrea Maria Zanchettin[2]
[1]YANMAR R&D EUROPE S.R.L, IT; [2]Politecnico di Milano, IT

IP4-6 **Planning with Real-Time Collision Avoidance for Cooperating Agents under Rigid Body Constraint**
Speaker: Federico Vesentini, University of Verona, IT

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Authors: Nicola Piccinelli, Federico Vesentini and Riccardo Muradore, University of Verona, IT

IP4-7 **The Case for Exploiting Underutilized Resources in Heterogeneous Mobile Architectures**
Speaker: Nikil Dutt, University of California, Irvine, US
Authors: Chenying Hsieh, Nikil Dutt and Ardalan Amiri Sani, UC Irvine, US

IP4-8 **Online Rare Category Detection for Edge Computing**
Speaker: Yufei Cui, City University of Hong Kong, HK
Authors: Yufei Cui[1], Qiao Li[1], Sarana Nutanong[2] and Chun Jason Xue[1]
[1]City University of Hong Kong, HK; [2]Vidyasirimedhi Institute of Science and Technology, TH

IP4-9 **RAGra: Leveraging Monolithic 3D ReRAM for Massively-Parallel Graph Processing**
Speaker: Yu Huang, Huazhong University of Science and Technology, CN
Authors: Yu Huang, Long Zheng, Xiaofei Liao, Hai Jin, Pengcheng Yao and Chuangyi Gui, Huazhong University of Science and Technology, CN

IP4-10 **Accurate Cost Estimation of Memory Systems Inspired by Machine Learning for Computer Vision**
Speaker: Lorenzo Servadei, Infineon Technologies, DE
Authors: Lorenzo Servadei[1], Elena Zennaro[1], Keerthikumara Devarajegowda[1], Martin Manzinger[1], Wolfgang Ecker[1] and Robert Wille[2]
[1]Infineon AG, DE; [2]Johannes Kepler University Linz, AT

IP4-11 **Practical Causality Handling for Synchronous Languages**
Speaker: Steven Smyth, Kiel University, DE
Authors: Steven Smyth, Alexander Schulz-Rosengarten and Reinhard von Hanxleden, Dept. of Computer Science, Kiel University, DE

IP4-12 **Application Performance Prediction and Optimization Under Cache Allocation Technology**
Speaker: Yeseong Kim, UCSD, US
Authors: Yeseong Kim[1], Ankit More[2], Emily Shriver[2] and Tajana Rosing[1]
[1]University of California San Diego, US; [2]Intel, US

IP4-13 **Generalized Matrix Factorization Techniques for Approximate Logic Synthesis**
Speaker: Sherief Reda, Brown University, US
Authors: Soheil Hashemi and Sherief Reda, Brown University, US

IP4-14 **CARS: A Multi-layer Conflict-Aware Request Scheduler for NVMe SSDs**
Speaker: Tianming Yang, Huanghuai University, CN
Authors: Tianming Yang[1], Ping Huang[2], Weiying Zhang[3], Haitao Wu[1] and Longxin Lin[4]
[1]Huanghuai University, CN; [2]Temple University, US; [3]Northeastern University, CN; [4]Jinan University, CN

IP4-15 **Queue Based Memory Management Unit for Heterogeneous MPSoCs**
Speaker: Robert Wittig, Technische Universität Dresden, DE
Authors: Robert Wittig, Mattis Hasler, Emil Matus and Gerhard Fettweis, Technische Universität Dresden, DE

10.1 Special Day on "Model-Based Design of Intelligent Systems" Session: Hot topic: Model-Based Machine Learning

Room 1 1100 – 1230

Chair: Andreas Gerstlauer, University of Texas, Austin, US
Co-Chair: Patricia Derler, National Instruments, US

1100 **Embedded Systems' Automation following OMG's Model Driven Architecture Vision**
Speaker: Wolfgang Ecker, Infineon Technologies, DE
Authors: Wolfgang Ecker[1], Keerthikumara Devarajegowda[2], Michael Werner[1], Zhao Han[1] and Lorenzo Servadei[3]
[1]Infineon Technologies AG / TU Munich, DE; [2]Infineon Technologies AG/TU Kaiserslautern, DE; [3]Infineon Technologies AG/Johannes Kepler University Linz, DE

1130 **Formal computation models in neuromorphic computing: challenges and opportunities**
Speaker and Author: Orlando Moreira, GrAI Matter Labs, NL

1200 **Automated Signal Processing Design through Bayesian Model-based Machine Learning**
Speaker and Author: Bert de Vries, GN ReSound, NL

1230 **Lunch Break** in Lunch Area

10.2 Special Session: Enabling Graph Analytics at Extreme Scales: Design Challenges, Advances, and Opportunities

Room 2 1100 – 1230

Organiser: Ananth Kalyanaraman, Washington State University, US
Chair: Partha Pande, Washington State University, US

A hot topic special session on enabling extreme scale graph analytics using innovations in algorithms and architectures is proposed. The special session will host three talks by speakers who work at the intersection of graph analytics and high performance computing. Through these talks, the session will cover the spectrum of unique challenges, latest advances, and exciting opportunities for research and development that exist in this emerging research area. The special session will serve as an avenue for discussion of recent advances that have started to show that graph analytics and computer architecture are capable of benefiting from one another and spawning new research directions. The goal is to build a new vibrant community at the intersection of graph analytics and HPC architecture, by fostering an environment conducive to active engagement and exchange of ideas between the two groups.

1100 **A Brief Survey of Algorithms, Architectures, and Challenges toward Extreme-scale Graph Analytics**
Speaker: Ananth Kalyanaraman, Washington State University, US
Authors: Ananth Kalyanaraman and Partha Pratim Pande, Washington State University, US

1130 **An Enhanced Parallel Graph Platform for Real-world Data Analytic Workflows**
Speaker: John Feo, Pacific Northwest National Laboratory, US
Authors: Vito Giovanni Castellana, Maurizio Drocco, John Feo, Andrew Lumsdaine, Joseph Manzano, Andres Marquez, Marco Minutoli, Joshua Suetterlein, Antonino Tumeo and Marcin Zalewski, Pacific Northwest National Laboratory, US

1200 **Scaling up Network Centrality Computations**
Speaker: Henning Meyerhenke, Humboldt-University Berlin, DE
Authors: Henning Meyerhenke and Alexander van der Grinten, Humboldt-University Berlin, DE

1230 **Lunch Break** in Lunch Area

10.3 System-level Dependability for Multicore and Real-time Systems

Room 3 1100 – 1230

Chair: Stefano Di Carlo, Politecnico di Torino, IT
Co-Chair: Luca Cassano, Politecnico di Milano, IT

This session covers topics ranging from reliability assessments in heterogeneous systems, optimization of the availability in real-time systems under permanent and transient faults, as well as fault tolerant techniques in many core systems.

1100 **Identifying the Most Reliable Collaborative Workload Distribution in Heterogeneous Devices**
Speaker: Paolo Rech, UFRGS, BR
Authors: Gabriel Piscoya Dávila, Daniel Oliveira, Philippe Navaux and Paolo Rech, UFRGS, BR

1130 **CE-Based Optimization for Real-time System Availability under Learned Soft Error Rate**
Speaker: Liying Li, East China Normal University, CN
Authors: Liying Li[1], Tongquan Wei[1], Junlong Zhou[2], Mingsong Chen[1] and X, Sharon Hu[3]
[1]East China Normal University, CN; [2]Nanjing University of Science and Technology, CN; [3]University of Notre Dame, US

1200 **A Deterministic-Path Routing Algorithm for Tolerating Many Faults on Wafer-Level NoC**
Speaker: Ying Zhang, Tongji University, CN
Authors: Zhongsheng Chen[1], Ying Zhang[1], Zebo Peng[2] and Jianhui Jiang[1]
[1]Tongji University, CN; [2]Linköping University, SE

IPs **IP5-1, IP5-2, IP5-3**

1230 **Lunch Break** in Lunch Area

10.4 Disruptive Technologies Ain't Fake News!

Room 4 1100 – 1230

Chair: Elena Gnani, Università di Bologna, IT
Co-Chair: Aida Todri-Sanial, CNRS-LIRMM, FR

Wanna see something real? This is the right session that covers a wide variety of disruptive technologies: from wireless 3D integration to photonics and thin film electronics, all the way to quantum computing.

1100 **CoDAPT: A Concurrent Data And Power Transceiver for Fully Wireless 3D-ICs**
Speaker: Benjamin Fletcher, University of Southampton, GB
Authors: Benjamin Fletcher[1], Shidhartha Das[2] and Terrence Mak[1]
[1]University of Southampton, GB; [2]ARM Ltd., GB

1130 **Compiling permutations for superconducting QPUs**
Speaker: Mathias Soeken, EPFL, CH
Authors: Mathias Soeken, Fereshte Mozafari, Bruno Schmitt and Giovanni De Micheli, EPFL, CH

1200 **Stochastic Computing with Integrated Optics**
Speaker: Sébastien Le Beux, École Centrale de Lyon, FR
Authors: Hassnaa El-Derhalli[1], Sébastien Le Beux[2] and Sofiene Tahar[1]
[1]Concordia University, CA; [2]Lyon Institute of Nanotechnology, FR

1215 **Inkjet-Printed True Random Number Generator based on Additive Resistor Tuning**
Speaker: Ahmet Turan Erozan, Karlsruhe Institute of Technology, DE
Authors: Ahmet Turan Erozan[1], Rajendra Bishnoi[1], Jasmin Aghassi-Hagmann[2] and Mehdi Tahoori[1]
[1]Karlsruhe Institute of Technology, DE; [2]Karlsruhe Institute of Technology, Offenburg University of Applied Science, DE

IPs **IP5-4**

1230 **Lunch Break** in Lunch Area

10.5 SSD and data placement

Room 5 1100 – 1230

Chair: Olivier Sentieys, INRIA, FR
Co-Chair: Hamid Tabani, Barcelona Supercomputing Center, BSC, ES

This session deals with some solutions to improve memory and storage throughput and latency. The first two papers propose solutions for SSD-based storage while the latter covers data placement and management in CPU-FPGA multicore systems.

1100 **HotR: Alleviating Read/Write Interference with Hot Read Data Replication for Flash Storage**
Speaker: Hong Jiang, The University of Texas at Arlington, US
Authors: Suzhen Wu[1], Weiwei Zhang[1], Bo Mao[1] and Hong Jiang[2]
[1]Xiamen University, CN; [2]The University of Texas at Arlington, US

1130 **RAFS: A RAID-Aware File System to Reduce the Parity Update Overhead for SSD RAID**
Speaker: Chenlei Tang, Huazhong University of Science and Technology, CN
Authors: Chenlei Tang[1], Jiguang Wan[1], Yifeng Zhu[2], Zhiyuan Liu[1], Peng Xu[1], Fei Wu[1] and Changsheng Xie[1]
[1]Huazhong University of Science and Technology, CN; [2]University of Maine, US

1200 **Automatic data placement for CPU-FPGA heterogeneous multiprocessor system-on-chips**
Speaker: Shiqing Li, Shandong University, CN
Authors: Shiqing Li, Yixun Wei and Lei Ju, Shandong University, CN

IPs **IP5-5**

1230 **Lunch Break** in Lunch Area

10.6 Self-adaptive resource management

Room 6 1100 – 1230

Chair: Geoff Merret, University of Southampton, GB
Co-Chair: Andy Pimantel, University of Amsterdam, NL

This session covers run-time resource management techniques for multicores, edge computing devices and storage systems. Proposed techniques are based on either machine learning or heuristics.

1100 **A Runtime Resource Management Policy for OpenCL Workloads on Heterogeneous Multicores**
Speaker: Antonio Miele, Politecnico di Milano, IT
Authors: Daniele Angioletti, Francesco Bertani, Cristiana Bolchini, Francesco Cerizzi and Antonio Miele, Politecnico di Milano, IT

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1130 **DMRM: Distributed Market-Based Resource Management of Edge Computing Systems**
Speaker: Dimosthenis Masouros, National Technical University of Athens, GR
Authors: Manolis Katsaragakis[1], Dimosthenis Masouros[1], Vasileios Tsoutsouras[1], Farzad Samie[2], Lars Bauer[2], Joerg Henkel[2] and Dimitrios Soudris[3]
[1]National Technical University of Athens, GR; [2]Karlsruhe Institute of Technology, DE; [3]Democritus University of Thrace, GR

1200 **Goal-Driven Autonomy for Efficient On-chip Resource Management: Translating Objectives to Goals**
Speaker: Anil Kanduri, University of Turku, FI
Authors: Elham Shamsa[1], Anil Kanduri[1], Amir M. Rahmani[2], Pasi Liljeberg[1], Axel Jantsch[3] and Nikil Dutt[4]
[1]University of Turku, FI; [2]University of California Irvine & TU Wien, US; [3]Vienna University of Technology (TU Wien), AT; [4]UC Irvine, US

1215 **Scrub Unleveling: Achieving High Data Reliability at Low Scrubbing Cost**
Speaker: Tianming Jiang, Huazhong University of Science and Technology, CN
Authors: Tianming Jiang[1], Ping Huang[2] and Ke Zhou[1]
[1]Huazhong University of Science and Technology, CN; [2]Temple University, US

IPs **IP5-6, IP5-7**

1230 **Lunch Break** in Lunch Area

10.7 Architectures for emerging machine learning techniques

Room 7 1100 – 1230

Chair: Sander Stuijk, Eindhoven University of Technology, NL
Co-Chair: Marina Zapater, EPFL, CH

The first paper presents a reinforcement learning approach to optimize the accelerator parameters. The second paper showcases how a memory Trojan can be used to attack, and lower the accuracy of a neural network. The last two papers introduce hardware accelerators to improve the energy consumption of the network.

1100 **Learning to infer: RL-based search for DNN primitive selection on Heterogeneous Embedded Systems**
Speaker: Miguel de Prado, HES-SO/ETHZ, CH
Authors: Miguel de Prado[1], Nuria Pazos[2] and Luca Benini[1]
[1]Integrated Systems Laboratory, ETH Zurich & Haute Ecole Arc Ingénierie, HES-SO, CH; [2]Haute Ecole Arc Ingénierie, HES-SO, CH

1130 **Memory Trojan Attack on Neural Network Accelerators**
Speaker: Xing Hu, University of California, Santa Barbara, CN
Authors: Yang Zhao[1], Xing Hu[1], Shuangchen Li[1], Jing Ye[2], Lei Deng[1], Yu Ji[3], Jianyu Xu[4], Dong Wu[3] and Yuan Xie[1]
[1]University of California, Santa Barbara, US; [2]State Key Laboratory of Computer Architecture, Institute of Computing Technology, Chinese Academy of Sciences, CN; [3]Tsinghua University, University of California, Santa Barbara, CN; [4]Tsinghua University, CN

1200 **Deep Positron: A Deep Neural Network Using the Posit Number System**
Speaker: Zachariah Carmichael, Rochester Institute of Technology, US
Authors: Zachariah Carmichael[1], Hamed F. Langroudi[1], Char Khazanov[1], Jeffrey Lillie[1], John L. Gustafson[2] and Dhireesha Kudithipudi[1]
[1]Rochester Institute of Technology, US; [2]National University of Singapore, SG

1215 **Learning to Skip Ineffectual Recurrent Computations in LSTMs**
Speaker: Zhengyun Ji, McGill University, CA
Authors: Arash Ardakani, Zhengyun Ji and Warren Gross, McGill University, CA

IPs **IP5-8, IP5-9, IP5-10**

1230 **Lunch Break** in Lunch Area

10.8 Europe digitization: Smart Anything Everywhere Initiative & FED4SAE, open calls and success stories

Exhibition Theatre 1100 – 1230

Organiser: Isabelle Dor, Commissariat à l'énergie atomique et aux énergies alternatives, FR
Chair: Marcello Coppola, STMicroelectronics, FR

The goal of Smart Anything Everywhere (SAE) initiative is to support SMEs, start-ups and mid-caps to enhance their products and services through the inclusion of innovative digital technologies. SAE H2020 projects provide one stop-shops to help companies to become more competitive through the adoption of the latest digital technologies. A SME tailored service is now available to provide access to R&D and digital competences, training to develop technical skills, business management support and networking opportunities. Cascade funding is available through SAE open calls, but also I4MS focusing on manufacturing.

FED4SAE project aims at bringing innovative Cyber-Physical System technologies to businesses from any sectors and any companies. The presentation of awarded projects illustrate FED4SAE one-stop-shop to accelerate CPS developments combining i) Access to leading-edge CPS platforms, Advanced Technologies, and Testbeds from Industrials and R&D centers, ii) Technical coaching from domain experts, iii) Innovation Management support, iv) Up to €60k in financial support to innovative companies plus access to further VC funding, v) and Access to potential users and suppliers across value chains throughout Europe. This session will confront the view point of large industrial, RTOs and SMEs and their targeted objectives and impact.

1100 **SAE, an example of EC initiative to support Europe digitization**
Speaker: Isabelle Dor, Commissariat à l'énergie atomique et aux énergies alternatives, FR

1115 **SME, RTO, industrial: how SAE support the collaboration**
Marcello Coppola, STMicroelectronics, FR
Michael Setton, Digital Catapult, GB
Rosanna Zaza, Alitec Srl, IT
Giovanni Gherardi, Energica Motor Company, IT

1230 **Lunch Break** in Lunch Area

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11.0 LUNCHTIME KEYNOTE SESSION

Room 1 1320 – 1350

Chair: Marc Geilen, Eindhoven University of Technology, NL
Co-Chair: Sander Stuijk, Eindhoven University of Technology, NL

1320 **A Fundamental Look at Models and Intelligence**
Speaker: Edward Lee, UC Berkeley, US

→ See Page 10

11.1 Special Day on "Model-Based Design of Intelligent Systems" Session: MBD of Cyber-Physical Systems

Room 1 1400 – 1530

Chair: Eugenio Villar, Universidad de Cantabria, ES
Co-Chair: Marc Geilen, Eindhoven University of Technology, NL

1400 **Specifying and Evaluating Quality Metrics for Vision-based Perception Systems**
Speaker: Jyotirmoy Deshmukh, Arizona State University, US
Authors: Adel Dokhanchi, Aniruddh Puranic, Xin Qin, Anand Balakrishnan, Heni Ben Amor, Georgios Fainekos and Jyotirmoy V. Deshmukh, Univ. of Southern California, US

1430 **Modeling Cross-Layer Interactions for Designing Certifiable Cyber-Physical Systems**
Speaker: Samarjit Chakraborty, TUM, DE
Authors: Samarjit Chakraborty, James H. Anderson, Martin Becker, Helmut Graeb, Samiran Halder, Ravindra Metta, Lothar Thiele, Stavros Tripakis and Anand Yeolekar, TUM, DE

1500 **Steps toward verified programming of embedded computing devices**
Speaker: Jean-Pierre Talpin, INRIA, FR
Authors: Jean-Pierre Talpin[1], Jean-Joseph Marty[1], Shravan Narayan[2], Deian Stefan[2] and Rajesh Gupta[2]
[1]INRIA, FR; [2]University of California at San Diego, US

1530 **Coffee Break** in Exhibition Area

11.2 Novel techniques in optimization and high-level modeling of mixed-signal circuits

Room 2 1400 – 1530

Chair: Francisco V. Fernandez, IMSE, ES
Co-Chair: Mark Po-Hung Lin, National Chung Cheng University, TW

New techniques are presented for the automated behavioral model generation and efficient numerical-symbolic simulation of analog/mixed-signal circuits. Also a Bayesian optimization approach for efficient analog circuit synthesis is presented.

1400 **Behavioral Modeling of Transistor-Level Circuits using Automatic Abstraction to Hybrid Automata**
Speaker: Ahmad Tarraf, Goethe University Frankfurt, DE
Authors: Ahmad Tarraf and Lars Hedrich, Goethe University Frankfurt, DE

1430 **Nubolic Simulation of AMS Systems with Data Flow and Discrete Event Models**
Speaker: Carna Zivkovic, University of Kaiserslautern, DE
Authors: Carna Zivkovic and Christoph Grimm, University of Kaiserslautern, DE

1500 **Bayesian Optimization Approach for Analog Circuit Synthesis Using Neural Network**
Speaker: Shuhan Zhang, Fudan University, CN
Authors: Shuhan Zhang, Wenlong Lv, Fan Yang, Changhao Yan, Dian Zhou and Xuan Zeng, Fudan University, CN

IPs **IP5-11**

1530 **Coffee Break** in Exhibition Area

11.3 Special Session: Rebooting our Computing Models

Room 3 1400 – 1530

Organiser: Pierre-Emmanuel Gaillardon, University of Utah, US
Chair: Pierre-Emmanuel Gaillardon, University of Utah, US
Co-Chair: Ian O'Connor, Ecole Centrale of Lyon, FR

With the current slowing down of Moore's Law, standard Von Neumann computing architectures are struggling more than ever to sustain the increase of computing needs. While alternative design approaches, such as the use of optimized accelerators or advanced power management techniques are successfully employed in contemporary designs, the trend keeps worsening due to the ever-increasing gap between on-chip and off-chip memory data rates. This trend, known as Von Neumann bottleneck, not only limits the system performance, but also acts nowadays as a limiter of the energy scaling. The quest towards more energy-efficiency requires solutions that disrupt the Von Neumann paradigm. In this hot topic session, we intend to elaborate on disruptive computing models far beyond our current Von Neumann computing model. Three talks will be provided: The first talk, from researchers from TU Delft, will cover quantum computing from the most basic physics to the practicalities of making a useful computer, including micro architecture and programming language). The second talk, from researchers from the University of Notre Dame, Georgia Tech and Penn State, will present new ways of computing using intrinsic oscillators. The third talk, from researchers from The University of California San Diego, will focus on memcomputing where self-organizing logic gates can be employed to solve complex computing problems very efficiently. In addition to provide a clear perspective to the DATE community beyond the currently hot novel architectures, such as neuromorphic or in-memory computing, this proposal also serve the purpose of tightening the link between DATE and the EDA community at large with the mission and roles of the IEEE Rebooting Computing Initiative - https://rebootingcomputing.ieee.org - that endorses it. We believe it will stimulate the EDA researchers to look into new grounds to develop their activities.

1400 **From Qubit to Computer**
Authors: Koen Bertels and Carmen G. Almudever, TU Delft, NL

1430 **Intrinsic Computing using weakly coupled oscillators**
Author: Nagadastagiri Reddy, Penn State, US

1500 **The Memcomputing Paradigm**
Author: Massimiliano Di Ventra, UCSD, US

1530 **Coffee Break** in Exhibition Area

11.4 Learning Gets Smarter

Room 4 1400 – 1530

Chair: Yuanqing Cheng, Beihang University, CN
Co-Chair: Mariagrazia Graziano, Politecnico di Torino, IT

Come and learn how emerging technologies enable deep learning and beyond for a wide range of applications: from industry speech recognition in industrial cloud computing to drones at the edge.

1400 **NeuADC: Neural Network-Inspired RRAM-Based Synthesizable Analog-to-Digital Conversion with Reconfigurable Quantization Support**
Speaker: Xuan Zhang, Washington University St. Louis, US
Authors: Weidong Cao, Xin He, Ayan Chakrabarti and Xuan Zhang, Washington University, US

1430 **Holylight: A Nanophotonic Accelerator for Deep Learning in Data Centers**
Speaker: Weichen Liu, School of Computer Science and Engineering, Nanyang Technological University, Singapore, CN
Authors: Weichen Liu[1], Wenyang Liu[2], Yichen Ye[3], Qian Lou[4], Yiyuan Xie[3] and Lei Jiang[5]
[1]Nanyang Technological University, SG; [2]College of Computer Science, Chongqing University, CN; [3]College of Electronics and Information Engineering, Southwest University, CN; [4]Department of Intelligent Systems Engineering, Indiana University, US; [5]Indiana University Bloomington, US

1500 **Transfer and Online Reinforcement Learning in STT-MRAM Based Embedded Systems for Autonomous Drones**
Speaker: Insik Yoon, Georgia Institute of Technology, US
Authors: Insik Yoon[1], Aqeel Anwar[1], Titash Rakshit[2] and Arijit Raychowdhury[1]
[1]Georgia Institute of Technology, US; [2]Samsung, US

1515 **AIX: A high performance and energy efficient inference accelerator on FPGA for a DNN-based commercial speech recognition**
Speaker: Minwook Ahn, SK Telecom, KR
Authors: Minwook Ahn, Seok Joong Hwang, Wonsub Kim, Seungrok Jung, Yeonbok Lee, Mookyoung Chung, Woohyung Lim and Youngjoon Kim, SK Telecom, KR

1530 **Coffee Break** in Exhibition Area

11.5 Vitello e Mozzarella alla Fiorentina: Virtualization, Multicore, and Fault-Tolerance

Room 5 1400 – 1530

Chair: Philippe Coussy, Universite de Bretagne-Sud / Lab-STICC, FR
Co-Chair: Michael Glass, Ulm University, DE

This session showcases innovation solutions for optimizing the performance of multiprocessors and virtual machines, as well as fault-tolerant deep neural networks (DNNs). The first paper presents an approach to improve virtual-machine (VM) performance in scenarios where multiple VMs share a single physical storage device. The second paper applies formal (ILP-based) and heuristic techniques to the problem of scheduling approximate computing tasks in asymmetric multiprocessors containing cores with different performance/power trade-offs. The third paper introduces techniques to improve the robustness of DNNs to bit-flip errors, such as those due to single-event-upsets in space and military applications. Two interactive presentations round out the session, with the first being on task and data migration in virtualized multiprocessors, and the second on how to optimize the performance of machine learning tasks in compute clusters.

1400 **VM-aware Flush Mechanism for Mitigating Inter-VM I/O Interference**
Speaker: Taehyung Lee, Sungkyunkwan University, KR
Authors: Taehyung Lee, Minho Lee and Young Ik Eom, Sungkyunkwan University, KR

1430 **An Efficient Bit-Flip Resilience Optimization Method for Deep Neural Networks**
Speaker: Christoph Schorn, Robert Bosch GmbH, DE
Authors: Christoph Schorn[1], Andre Guntoro[1] and Gerd Ascheid[2]
[1]Robert Bosch GmbH, DE; [2]RWTH Aachen University, DE

1500 **Approximation-aware Task Deployment on Asymmetric Multicore Processors**
Speaker: Lei Mo, INRIA, FR
Authors: Lei Mo[1], Angeliki Kritikakou[2] and Olivier Sentieys[1]
[1]INRIA, FR; [2]IRISA/INRIA, Univ. Rennes, FR

IPs **IP5-12, IP5-13**

1530 **Coffee Break** in Exhibition Area

11.6 Design Automation Solutions for Microfluidic Platforms and Tasks

Room 6 1400 – 1530

Chair: Robert Wille, Johannes Kepler University Linz, AT
Co-Chair: Andy Tyrrell, University of York, GB

The session provides talks on design automation for microfluidic devices which covers both, a wide range of different platforms and tasks. More precisely, the presentations are covering platforms such as biochips based on micro-electrode-dot arrays (MEDA biochips), flow-based biochips, and Programmable Microfluidic Devices (PMDs). The covered tasks include parameter space exploration, physical synthesis, and washing. This variety makes this session ideal for both, experts already working in the area and interest in the latest results but also researchers who are curios about this domain and want to get a closer insight.

1400 **BioScan: Parameter-Space Exploration of Synthetic Biocircuits Using MEDA Biochips**
Speaker: Mohamed Ibrahim, Intel Corporation, US
Authors: Mohamed Ibrahim[1], Bhargab Bhattacharya[2] and Krishnendu Chakrabarty[1]
[1]Duke University, US; [2]Indian Statistical Institute, Kolkata, IN

1430 **Physical Synthesis of Flow-Based Microfluidic Biochips Considering Distributed Channel Storage**
Speaker: Xing Huang, National Tsing Hua University, TW
Authors: Zhisheng Chen[1], Xing Huang[2], Wenzhong Guo[1], Bing Li[3], Tsung-Yi Ho[2] and Ulf Schlichtmann[3]
[1]Fuzhou University, CN; [2]National Tsing Hua University, TW; [3]TUM, DE

1500 **Block-Flushing: A Block-based Washing Algorithm for Programmable Microfluidic Devices**
Speaker: Bing Li, TUM, DE
Authors: Yu-Huei Lin[1], Tsung-Yi Ho[1], Bing Li[2] and Ulf Schlichtmann[2]
[1]National Tsing Hua University, TW; [2]TUM, DE

IPs **IP5-14, IP5-15, IP5-16**

1530 **Coffee Break** in Exhibition Area

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11.7 Extending Scheduling Schemes

Room 7 1400 – 1530

Chair: Marco Di Natale, Scuola Superiore Sant'Anna of Pisa, IT
Co-Chair: Mitra Nasri, TU Delft, NL

This session presents papers with generalization of fixed-priority, global EDF, and applications to synchronous data flows.

1400 **Analyzing GEDF Scheduling for Parallel Real-Time Tasks with Arbitrary Deadlines**
Speaker: Xu Jiang, The Hong Kong Polytechnic University, HK
Authors: Xu Jiang[1], Nan Guan[1], Di Liu[2] and Weichen Liu[3]
[1]The Hong Kong Polytechnic University, HK; [2]Yunnan University, CN; [3]Nanyang Technological University, SG

1430 **Simple and General Methods for Fixed-Priority Schedulability in Optimization Problems**
Speaker: Paolo Pazzaglia, Scuola Superiore Sant Anna, Pisa, IT
Authors: Paolo Pazzaglia, Alessandro Biondi and Marco Di Natale, Scuola Superiore Sant'Anna, IT

1500 **Hard Real-Time Scheduling of Streaming Applications Modeled as Cyclic CSDF Graphs**
Speaker: Sobhan Niknam, Leiden University, NL
Authors: Sobhan Niknam, Peng Wang and Todor Stefanov, Leiden University, NL

1530 **Coffee Break** in Exhibition Area

11.8 An Industry Approach to FPGA/ARM System Development and Verification (part 1)

Exhibition Theatre 1400 – 1530

Organiser and Speaker: John Zhao, MathWorks, US

MATLAB and Simulink provide a rich environment for embedded-system development, with libraries of proven, specialized algorithms ready to use for specific applications. The environment enables a model-based design workflow for fast prototyping and implementation of the algorithms on heterogeneous embedded targets, such as MPSoC. A system-level design approach enables architectural exploration and partitioning, as well as coordination between SW and HW development workflows. Functional verification throughout the design process improves coverage and test-case generation while reducing the time and resources required.

In this set of tutorial sessions, you will learn

- How to evaluate hardware and software system architectures using latest feature in Simulink
- How to implement an application that leverages the FPGA and ARM core of a Zynq SOC
- The flexibility and diversity of the approach through examples that include prototyping a motor control algorithm and a video-processing algorithm.
- A HW/SW co-design workflow that combines system level design and simulation with automatic code generation

1530 **Coffee Break** in Exhibition Area

IP5 Interactive Presentations

Poster Area 1530 – 1600
supported by Cadence Academic Network

Interactive Presentations run simultaneously during a 30-minute slot. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session.

IP5-1 Thermal-Awareness in a Soft Error Tolerant Architecture

Speaker: Sajjad Hussain, Chair for Embedded Systems, KIT, DE
Authors: Sajjad Hussain[1], Muhammad Shafique[2] and Joerg Henkel[1]
[1]Karlsruhe Institute of Technology, DE; [2]Vienna University of Technology (TU Wien), AT

IP5-2 A software-level Redundant MultiThreading for Soft/Hard Error Detection and Recovery

Speaker: Hwisoo So, Yonsei University, KR
Authors: Moslem Didehban[1], HwiSoo So[2], Aviral Shrivastava[1] and Kyoungwoo Lee[2]
[1]Arizona State University, US; [2]Yonsei University, KR

IP5-3 Common-Mode Failure Mitigation: Increasing Diversity through High-Level Synthesis

Speaker: Farah Naz Taher, University of Texas at Dallas, US
Authors: Farah Naz Taher[1], Matthew Joslin[1], Anjana Balachandran[2], Zhiqi Zhu[1] and Benjamin Carrion Schaefer[1]
[1]The University of Texas at Dallas, US; [2]The Hong Kong Polytechnic University, HK

IP5-4 Exploiting Wavelength Division Multiplexing for Optical Logic Synthesis

Speaker: David Z. Pan, University of Texas, Austin, US
Authors: Zheng Zhao[1], Derong Liu[2], Zhoufeng Ying[1], Biying Xu[1], Chenghao Feng[1], Ray T. Chen[1] and David Z. Pan[1]
[1]University of Texas, Austin, US; [2]Cadence Design Systems, US

IP5-5 IgnoreTM: Opportunistically Ignoring Timing Violations for Energy Savings using HTM

Speaker: Dimitra Papagiannopoulou, University of Massachusetts Lowell, US
Authors: Dimitra Papagiannopoulou[1], Sungseob Whang[2], Tali Moreshet[3] and Iris Bahar[4]
[1]University of Massachusetts Lowell, US; [2]CloudHealth Technologies, US; [3]Boston University, US; [4]Brown University, US

IP5-6 Using Machine Learning for Quality Configurable Approximate Computing

Speaker: Mahmoud Masadeh, Concordia University, CA
Authors: Mahmoud Masadeh, Osman Hasan and Sofiene Tahar, Department of Electrical and Computer Engineering, Concordia University, Montreal, Quebec, CA

IP5-7 Prediction-Based Task Migration on S-NUCA Many-Cores

Speaker: Martin Rapp, Karlsruhe Institute of Technology, DE
Authors: Martin Rapp[1], Anuj Pathania[1], Tulika Mitra[2] and Joerg Henkel[1]
[1]Karlsruhe Institute of Technology, DE; [2]National University of Singapore, SG

IP5-8 Design of Hardware-Friendly Memory Enhanced Neural Networks

Speaker: Ann Franchesca Laguna, University of Notre Dame, US
Authors: Ann Franchesca Laguna, Michael Niemier and X, Sharon Hu, University of Notre Dame, US

IP5-9 Energy-Efficient Inference Accelerator for Memory-Augmented Neural Networks on an FPGA

Speaker: Seongsik Park, Seoul National University, KR
Authors: Seongsik Park, Jaehee Jang, Seijoon Kim and Sungroh Yoon, Seoul National University, KR

IP5-10 **HDCluster: An Accurate Clustering Using Brain-Inspired High-Dimensional Computing**
Speaker: Mohsen Imani, University of California, San Diego, US
Authors: Mohsen Imani, Yeseong Kim, Thomas Worley, Saransh Gupta and Tajana Rosing, University of California San Diego, US

IP5-11 **Finding All DC Operating Points Using Interval-Arithmetic Based Verification Algorithms**
Speaker: Itrat A. Akhter, University of British Columbia, CA
Authors: Itrat Akhter, Justin Reiher and Mark Greenstreet, University of British Columbia, CA

IP5-12 **GENIE: QoS-guided Dynamic Scheduling for CNN-based Tasks on SME Clusters**
Speaker: Zhaoyun Chen, National University of Defense Technology, CN
Authors: Zhaoyun Chen, Lei Luo, Haoduo Yang, Jie Yu, Mei Wen and Chunyuan Zhang, National University of Defense Technology, CN

IP5-13 **Adiabatic Implementation of Manchester Encoding for Passive NFC System**
Speaker: Sachin Maheshwari, University of Westminster, GB
Authors: Sachin Maheshwari[1] and Izzet Kale[2]
[1]university of Westminster, GB; [2]University of Westminster, GB

IP5-14 **A Pulse Width Modulation based Power-elastic and Robust Mixed-signal Perceptron Design**
Speaker: Sergey Mileiko, MR, GB
Authors: Sergey Mileiko[1], Rishad Shafik[1], Alex Yakovlev[1] and Jonathan Edwards[2]
[1]Newcastle University, GB; [2]Temporal Computing, GB

IP5-15 **Fault Localization in Programmable Microfluidic Devices**
Speaker: Ulf Schlichtmann, TUM, DE
Authors: Alessandro Bernardini, Chunfeng Liu, Bing Li and Ulf Schlichtmann, TUM, DE

IP5-16 **Thermal Sensing Using Micro-ring Resonators in Optical Network-on-Chip**
Speaker: Mengquan Li, Chongqing University, CN
Authors: Weichen Liu[1], Mengquan Li[2], Wanli Chang[3], Chunhua Xiao[2], Yiyuan Xie[4], Nan Guan[5] and Lei Jiang[6]
[1]Nanyang Technological University, SG; [2]Chongqing University, CN; [3]University of York, GB; [4]Southwest University, CN; [5]Hong Kong Polytechnic University, HK; [6]Indiana University Bloomington, US

12.1 Special Day on "Model-Based Design of Intelligent Systems" Session: MBD of Safe and Secure Systems

Room 1 1600 – 1730

Chair: Frédéric Mallet, Université Nice Sophia Antipolis, FR
Co-Chair: Marc Geilen, Eindhoven University of Technology, NL

1600 **Semantic Integration Platform for Cyber-Physical System Design**
Speaker: Qishen Zhang, Institute for Software Integrated Systems Vanderbilt University, US
Authors: Qishen Zhang, Ted Bapty, Tamas Kecskes and Janos Sztipanovits, Vanderbilt University, US

1630 **Worst-Case Cause-Effect Reaction Latency in Systems with Non-Blocking Communication**
Speaker: Yi Wang, Uppsala University, SE
Authors: Jakaria Abdullah, Gaoyang Dai and Yi Wang, Uppsala University, SE

1700 **Harmonizing Safety, Security and Performance Requirements in Embedded Systems**
Speaker: Ludovic Apvrille, LTCI, Télécom ParisTech, Université Paris-Saclay, FR
Authors: Ludovic Apvrille and Letitia Li, Télécom ParisTech, FR

12.2 The Art of Synthesizing Logic

Room 2 1600 – 1730

Chair: Cortadella Jordi, UPC, ES
Co-Chair: Tiziano Villa, University of Verona, IT

The recent progress in logic synthesis is presented in this session. The research targets new emerging applications of synthesis and extends the current computing limits of logic synthesis. The first paper introduces an approximate synthesis algorithm for realizing a logic function on a lattice using Boolean satisfiability. The second paper presents a scalable Boolean optimization flow including enhancements to difference-based resubstitution, AIG optimization and kerneling. The third paper improves exact logic synthesis techniques and integrates them into a scalable generic logic rewriting algorithm. The fourth paper proposes a polynomial-time algorithm for computing the closest symmetric approximation for a Boolean function.

1600 **A Satisfiability-Based Approximate Algorithm for Logic Synthesis Using Switching Lattices**
Speaker: Levent Aksoy, Istabul Technical University, TR
Authors: Levent Aksoy and Mustafa Altun, Istanbul Technical University, TR

1630 **Scalable Boolean Methods in a Modern Synthesis Flow**
Speaker: Eleonora Testa, EPFL, CH
Authors: Eleonora Testa[1], Luca Amaru[2], Mathias Soeken[1], Alan Mishchenko[3], Patrick Vuillod[2], Jiong Luo[2], Christopher Casares[2], Pierre-Emmanuel Gaillardon[4] and Giovanni De Micheli[1]
[1]EPFL, CH; [2]Synopsys Inc., US; [3]UC Berkeley, US; [4]University of Utah, US

1700 **On-the-fly and DAG-aware: Rewriting Boolean Networks with Exact Synthesis**
Speaker: Heinz Riener, EPFL, CH
Authors: Heinz Riener[1], Winston Haaswijk[1], Alan Mishchenko[2], Giovanni De Micheli[1] and Mathias Soeken[1]
[1]EPFL, CH; [2]UC Berkeley, US

1715 **Approximate Logic Synthesis by Symmetrization**
Speaker: Anna Bernasconi, Universita, IT
Authors: Anna Bernasconi[1], Valentina Ciriani[2] and Tiziano Villa[3]
[1]Università di Pisa, IT; [2]Università degli Studi di Milano, IT; [3]Dipartimento d'Informatica, Università di Verona, IT

12.3 Aging, calibration circuits and yield

Room 3 1600 – 1730

Chair: Hank Walker, TAMU, US
Co-Chair: Naghmeh Karimi, University of Maryland Baltimore county, US

This session discusses methods to mitigate defects, faults, variability and reliability.

1600 **Package and Chip Accelerated Aging Tests for Power MOSFET Reliability Evaluation**
Speaker: Tingyou Lin, Department of LAD Technology, Vanguard International Semiconductor, TW
Authors: Tingyou Lin[1], Chauchin Su[1], Chung-Chih Hung[1], Karuna Nidhi[2], Chily Tu[2] and Shao-Chang Huang[2]
[1]National Chiao Tung University, TW; [2]Vanguard International Semiconductor Corporation, TW

1630 **Bayesian Optimized Importance Sampling for High Sigma Failure Rate Estimation**
Speaker: Dennis Weller, Karlsruhe Institute of Technology, DE
Authors: Dennis Weller, Michael Hefenbrock, Mohammad Saber Golanbari, Michael Beigl and Mehdi Tahoori, Karlsruhe Institute of Technology, DE

1700 **Wafer-Level Adaptive Vmin Calibration Seed Forecasting**
Speaker: Yiorgos Makris, The University of Texas at Dallas, US
Authors: Constantinos Xanthopoulos[1], Deepika Neethirajan[1], Sirish Boddikurapati[2], Amit Nahar[2] and Yiorgos Makris[1]
[1]The University of Texas at Dallas, US; [2]Texas Instruments Inc., US

1715 **Single-event double-upset self-recoverable and single-event transient pulse filterable latch design for low power applications**
Speaker: Aibin Yan, Anhui University, CN
Authors: Aibin Yan[1], Yuanjie Hu[1], Jie Song[1] and Xiaoqing Wen[2]
[1]Anhui University, CN; [2]Kyushu Institute of Technology, JP

12.4 Design and Optimization for Low-Power Applications

Room 4 1600 – 1730

Chair: Giuseppe Tagliavini, Università di Bologna, IT
Co-Chair: Jan Madsen, Technical University of Denmark, DK

This session explores low-power design from different point of views, from neural network based scheduling of multicores and image processing, to ultra low-power for near-threshold computing and continuous monitoring IoT sensors.

1600 **Dynamic Scheduling on Heterogeneous Multicores**
Speaker: Ann Gordon-Ross, University of Florida, US
Authors: Ayobami Edun, Ruben Vazquez, Ann Gordon-Ross and Greg Stitt, University of Florida, US

1630 **Selecting the Optimal Energy Point in Near-Threshold Computing**
Speaker: Sami Salamin, Karlsruhe Institute of Technology (KIT), DE
Authors: Sami Salamin, Hussam Amrouch and Joerg Henkel, Karlsruhe Institute of Technology, DE

1700 **Exploration and Design of Low-Energy Logic Cells for 1 kHz Always-on Systems**
Speaker: Maxime Feyerick, ESAT-MICAS, KU Leuven, BE
Authors: Maxime Feyerick, Jaro De Roose and Marian Verhelst, KU Leuven, BE

1715 **Enabling Energy-Efficient Unsupervised Monocular Depth Estimation on ARMv7-Based Platforms**
Speaker: Antonio Cipolletta, Politecnico di Torino, IT
Authors: Valentino Peluso[1], Antonio Cipolletta[1], Andrea Calimera[1], Matteo Poggi[2], Fabio Tosi[2] and Stefano Mattoccia[2]
[1]Politecnico di Torino, IT; [2]Università di Bologna, IT

12.5 System Modelling for Analysis and Simulation

Room 5 1600 – 1730

Chair: Ingo Sander, KTH Royal Institute of Technology, SE
Co-Chair: Gianluca Palermo, Politecnico di Milano, IT

The session highlights the importance of system modelling for design, performance analysis and optimisation. The first paper proposes a novel dataflow model of computation supporting reconfigurability for dynamic systems. The second paper combines the synchronous dataflow model of computation with a probabilistic method for real-time analysis. Finally, the last paper addresses the simulation of SystemC-based virtual prototypes using speculative temporal decoupling.

1600 **RDF: Reconfigurable Dataflow**
Speaker: Xavier Nicollin, Univ. Grenoble Alpes, FR
Authors: Pascal Fradet[1], Alain Girault[1], Ruby Krishnaswamy[2], Xavier Nicollin[3] and Arash Shafiei[2]
[1]INRIA, FR; [2]Orange, FR; [3]G-INP, FR

1630 **Probabilistic State-Based RT-Analysis of SDFGs on MPSoCs with Shared Memory Communication**
Speaker: Ralf Stemmer, Carl von Ossietzky Universität Oldenburg, DE
Authors: Ralf Stemmer[1], Henning Schlender[1], Maher Fakih[2], Kim Grüttner[2] and Wolfgang Nebel[1]
[1]University of Oldenburg, DE; [2]OFFIS e.V., DE

1700 **Speculative Temporal Decoupling Using fork()**
Speaker: Matthias Jung, Fraunhofer IESE, DE
Authors: Matthias Jung[1], Frank Schnicke[1], Markus Damm[1], Thomas Kuhn[1] and Norbert Wehn[2]
[1]Fraunhofer IESE, DE; [2]University of Kaiserslautern, DE

12.6 Trojans and public key implementation challenges

Room 6 1600 – 1730

Chair: Patrick Schaumont, Virginia Tech, US
Co-Chair: Nele Mentens, KU Leuven, BE

This session contains 2 pagers on Trojans, of which one is on formal methods to design and detect, and the other of practical attacks in the context of multi-tenant FPGAs. The other two papers discuss implementation challenges of public key in ASIC and FPGA.

1600 **When Capacitors Attack: Formal Method Driven Design and Detection of Charge-Domain Trojans**
Speaker: Yier Jin, University of Florida, US
Authors: Xiaolong Guo[1], Huifeng Zhu[2], Yier Jin[1] and Xuan Zhang[2]
[1]University of Florida, US; [2]Washington University in St. Louis, US

1630 **FourQ on ASIC: Breaking Speed Records for Elliptic Curve Scalar Multiplication**
Speaker: Hiromitsu Awano, The University of Tokyo, JP
Authors: Hiromitsu Awano and Makoto Ikeda, The University of Tokyo, JP

1700 **DArL: Dynamic Parameter Adjustment for LWE-based Secure Inference**
Speaker: Song Bian, Kyoto University, JP
Authors: Song Bian, Masayuki Hiromoto and Takashi Sato, Kyoto University, JP

1715 **Timing Violation Induced Faults in Multi-Tenant FPGAs**

Speaker: Mirjana Stojilovic, EPFL, CH
Authors: Dina Mahmoud and Mirjana Stojilovic, EPFL, CH

12.7 Emerging Strategies for Deep Neural Network Hardware

Room 7 1600 – 1730

Chair: Jim Harkin, University of Ulster, GB
Co-Chair: Li Jiang, Institute: Shanghai Jiao Tong University, CN

This session presents new approaches to the acceleration of deep neural networks focused on ReRAM-based architectures with papers focusing on the key challenges of reliable operation with unreliable devices and strategies for counter-aging effects. In addition, 3D ReRAM are proposed in the acceleration of general graphics processing. In the evolution of stochastic computing, emerging work on low-cost and energy efficient convolutional neural networks is also explored with deterministic bit-stream processing.

1600 **Aging-aware Lifetime Enhancement for Memristor-based Neuromorphic Computing**
Speaker: Shuhang Zhang, TUM, DE
Authors: Shuhang Zhang[1], Grace Li Zhang[1], Bing Li[1], Hai (Helen) Li[2] and Ulf Schlichtmann[1]
[1]TUM, DE; [2]Duke University, US

1630 **Energy-Efficient Convolutional Neural Networks with Deterministic Bit-Stream Processing**
Speaker: M. Hassan Najafi, University of Louisiana at Lafayette, US
Authors: Sayed Abdolrasoul Faraji[1], M. Hassan Najafi[2], Bingzhe Li[1], Kia Bazargan[3] and David Lilja[1]
[1]University of Minnesota, Twin Cities, US; [2]University of Louisiana at Lafayette, US; [3]University of Minnesota, US

1700 **RED: A ReRAM-based Deconvolution Accelerator**
Speaker: Hai (Helen) Li, Duke University, US
Authors: Zichen Fan[1], Ziru Li[1], Bing Li[2], Yiran Chen[2] and Hai (Helen) Li[2]
[1]Tsinghua University, CN; [2]Duke University, US

1715 **Design of Reliable DNN Accelerator with Un-reliable ReRAM**
Speaker: Saibal Mukhopadhyay, GEORGIA TECH, US
Authors: Yun Long and Saibal Mukhopadhyay, Georgia Institute of Technology, US

12.8 An Industry Approach to FPGA/ARM System Development and Verification (part 2)

Exhibition Theatre 1600 – 1730

Organiser and Speaker: John Zhao, MathWorks, US

Part 2 of tutorial (see Session 11.8 for description).

Friday Workshops Co-Chairs:
Francisco Cazorla, Barcelona Supercomputing Center and IIIA-CSIC, ES
Michael Glaß, Ulm University, DE

0730 **Workshop Registration**

0830–1000 **Workshops**

1000–1030 **Coffee Break**
International F1/10 Autonomous Racing Demo
supported by IEEE CEDA – Session 1

1030–1200 **Workshops**

1200–1300 **Lunch Break**
International F1/10 Autonomous Racing Demo
supported by IEEE CEDA – Session 2

1300–1430 **Workshops**

1430–1500 **Coffee Break**
International F1/10 Autonomous Racing Demo
supported by IEEE CEDA – Session 3

1500–1730 **Workshops**

W01 The 5th International Workshop on Optical / Photonic Interconnects for Computing Systems (OPTICS)
Room 3 0830 – 1730

W02 Recent Trends in Memristor Science & Technology: the journey from single memristor device towards 100 trillion synapses of brain
Room 2 0830 – 1730

W03 DATE Workshop on Autonomous Systems Design (ASD2019)
Room 1 0830 – 1730

W04 6th Workshop on Design Automation for Understanding Hardware Designs (DUHDE6)
Room 9 0830 – 1730

W05 AxC: 4th Workshop on Approximate Computing
Room 5 0830 – 1700

W06 2nd International Workshop on Embedded Software for the Industrial IoT (ESIIT 2019)
Room 6 0845 – 1615

W07 Workshop on Machine Learning for CAD
Room 7 0830 – 1730

W08 Grand Challenges and Research Tools for Quantum Computing
Room 10 0830 – 1730

W09 Quo vadis, Logic Synthesis?
Room 8 0830 – 1730

W10 Workshop on Open-Source Design Automation for FPGAs – OSDA
Room 4 0845 – 1730

W01 The 5th International Workshop on Optical / Photonic Interconnects for Computing Systems (OPTICS)

Room 3 0830 – 1730

General Co-Chairs:
Jiang Xu, Hong Kong University of Science and Technology, HK
Mahdi Nikdast, Colorado State University, US
Gabriela Nicolescu, Ecole Polytechnique de Montréal, CA

Programme Committee Chair:
Sébastien Le Beux, Lyon Institute of Nanotechnology FR

Programme Committee Members:
Alan Mickelson, University of Colorado Boulder, US
Ayse Coskun, Boston University, US
José L. Abellán, Universidad Católica de Murcia, SP
Nikos Hardavellas, Northwestern University, US
Olivier Sentieys, INRIA, FR
Tohru Ishihara, Kyoto University, JP
Yaoyao Ye, Shanghai Jiao Tong University, CN
Yoan Léger, CNRS – FOTON, FR

WORKSHOP FOCUS:

As Moore's Law is slowing down, an exploration of alternative technologies are developed to replace traditional CMOS-based architectures at the heart of data processing. Moreover, stringent application constraints on massive data transfers in data centers, artificial intelligence systems, and embedded high-performance computing (eHPC), requires new communication-centric systems with novel interconnect technologies. Silicon photonics is a prime candidate to achieve this thanks to its compatibility with CMOS fabrication process, scalability, and growing maturity. OPTICS aims at discussing the most recent advances in silicon photonics for computing systems, covering topics from the device fabrication all the way up to the system-level design through circuit optimization with Electronic-Photonic Design Automation (EPDA). The workshop is of interest to researchers working on silicon photonics, high-performance computing systems and EDA/EPDA. It is comprised of invited talks of the highest caliber from industry and academia addressing most recent outcomes. Ideas and new opportunities are discussed during a panel and a refereed poster presentations session highlights works-in progress.

TOPICS TO BE DISCUSSED INCLUDE BUT ARE NOT LIMITED TO:

- EPDA (Electronic-Photonic Design Automation): non-uniformity/thermal aware design, floor-planning, crosstalk-aware interconnects modeling and simulation, etc.
- Inter/Intra-chip Interconnects: hybrid optical-electronic interconnects, passive/active-based optical switched networks, communication protocols, I/O design etc.
- Applications: embedded high-performance computing, data center, reservoir computing, all-optical logic gates, etc.
- Silicon Photonics Devices and Circuits: circuit demonstrator, on-chip lasers, photodetectors, electro-optic modulators, optical switches, athermal devices, etc.

0830 – 0840 Introduction to OPTICS

0840 – 1000 From system level simulations to silicon photonic circuit fabrication

0840 – 0940 Keynote: EPDA for EPSoC design: From co-simulation to photonic circuit generators
Vladimir Stojanovic, UC Berkeley, US

0940 – 1000 MPW services for Photonics & ICs prototyping
Invited Speaker: Jean Christophe Crebier, CMP, FR

1000 – 1030 Coffee Break

1030 – 1150 Silicon Photonics for on-chip interconnects, IO and computing

1030 – 1050 3 µm and 12 µm SOI platforms for optical interconnects and I/O coupling
Invited Speaker: Timo Aalto, VTT, FI

1050 – 1110 Electronics-photonics integration in advanced CMOS platforms using a photonics module: a transceiver application in 65 nm bulk CMOS
Invited Speaker: Fabio Pavanello, IMEC, BE

1110 – 1130 Advancing silicon photonics for traditional and novel computing paradigms
Invited Speaker: Bert Offrein, IBM Zurich, CH

1130 – 1150 Integrated Optical Neural Networks Exploiting Light Speed Approximate Parallel Multipliers
Invited Speaker: Jun Shiomi, Kyoto University, JP

1150 – 1200 Poster Presentation (session 1)

Design Automation for Wavelength-Routed Optical NoCs
Tsun-Ming Tseng, Ulf Schlichtmann, TUM, DE

High-Radix Nonblocking Integrated Optical Switching Fabric for Data Center
Zhifei Wang, Jiang Xu, Peng Yang, et al., HKUST, CN

Integrated spiking nanolaser
Maxime Delmulle, Sylvain Combrié, Fabrice Raineri and Alfredo De Rossi, Thales and Research Technology, FR, and C2N, FR

RSON: an Inter/Intra-Chip Silicon Photonic Network for Rack-Scale Computing Systems
Peng Yang, Zhifei Wang, Zhehui Wang and Jiang Xu, HKUST, CN

Hardware Emulation Platform of Optical Network-on-Chip
Lucien Del Bosque, Ian O'ConnoR and Sébastien Le Beux, ECL, FR

BOSIM: Holistic Optical Switch Models for Silicon Photonic Networks
Xuanqi Chen, Zhifei Wang and Yi-Shing Chang, et al., HKUST, CN and Intel, US

Stochastic Computing with Integrated Optics
Hassnaa El-Derhalli, Sébastien Le Beux and Sofiene Tahar, Concordia University, CA

1200 – 1300 Lunch Break

FRIDAY, 29 MARCH 2019

1300 – 1420 New Devices for New Architectures

1300 – 1320 Recent advances in silicon photonics
Invited Speaker: Laurent Vivien, C2N, FR

1320 – 1340 Mode division multiplexing for optical networks on chip – potential and limitations
Invited Speaker: Christophe Peucheret, Foton, FR

1340 – 1400 III-V semiconductor on silicon nanodevices for high performance computing
Invited Speaker: Fabrice Raineri, Paris-Sud University, FR

1400 – 1420 Hardware-software Co-design of Optical Neural Networks
Invited Speaker: Zheng Zhao, Zhoufeng Ying, Ray T. Chen and **David Z. Pan,** The University of Texas at Austin, US

1420 – 1430 Poster presentation (session 2)

FODON: Ultra-High-Radix Low-Loss Optical Switching Fabric
Zhifei Wang, Zhehui Wang and Jiang Xu, et al., HKUST, CN

All-optical sampling with hybrid III-V on Silicon nano-resonators for photonic computing
Léa Constans, Sylvain Combrié, Fabrice Raineri and Alfredo De Rossi, Thales and Research Technology, FR and C2N, FR

MOCA: an Inter/Intra-Chip Optical Network for Memory
Zhehui Wang, Jiang Xu and Zhifei Wang, et al., HKUST, CN

Enabling System-Level Design with Optical Networks On-Chip Through Architecture Integration and Topology Synthesis
Mahdi Tala, Maddalena Nonato and Oliver Schrape, et al., University of Ferrara, IT and IHP Microelectronics, DE

Quantitative Analysis of Optical/Electrical Interconnects and Optical-Electrical Interfaces
Zhehui Wang, Jiang Xu and Zhifei Wang, et al., HKUST, CN

Light Up your Many Core
Clément Zrounba, Sébastien Le Beux and Ian O'Connor, ECL, FR

Crosstalk Noise Reduction through Adaptive Power Control in Inter/Intra-Chip Optical Networks
Luan Huu Kinh Duong, Peng Yang and Zhifei Wang, et al., HKUST, CN

1430 – 1500 Coffee Break

1500–1620 **Toward large scale on-chip optical interconnects**

1500–1520 Designing large-scale photonic integrated circuits
Invited Speaker: Umar Khan, IMEC, BE

1520–1540 EDA for WRONoCs: From Topology to Physical Design, and Breaking Down Barriers
Invited Speaker: Ulf Schlichtmann, TUM, DE

1540–1600 A System-Level Perspective on Silicon Photonic Network-on-Chips
Invited Speaker: Aditya Narayan, Boston University, US

1600–1620 ONoCs: from offline optimization to run time adaptability
Invited Speaker: Cédric Killian, IRISA/INRIA, FR

1620–1720 **Panel: Bringing on-chip optical interconnects into the real world**

Chair: Davide Bertozzi, University of Ferrara, IT

Panelists:
Ian O'Connor, ECL, FR
Yvain Thonnart, CEA-Leti, FR
Laurent Vivien, C2N, FR
Vladimir Stojanovic, UC Berkeley, US

1720–1730 Concluding Remarks and Closing Session

W02

Recent Trends in Memristor Science & Technology: the journey from single memristor device towards 100 trillion synapses of brain

Room 2 0830 – 1730

Organisers:
Kyeong-Sik Min, Kookmin University, KR
Ronald Tetzlaff, Technische Universität Dresden, DE
Fernando Corinto, Politecnico di Torino, IT

AIM AND FOCUS

This workshop focuses on Recent Trends in Memristor Science & Technology: the journey from single memristor device towards 100 trillion synapses of brain. Memristors were predicted theoretically in 1971 and demonstrated experimentally in 2008. Since then, a lot of researches have been done to develop memristor technology for possible uses of non-volatile memories, analog circuits, computing logics, neuromorphic systems, etc. In this special workshop of memristor science and technology, we have some invited talks about the recent state-of-the-art techniques of memristor circuits & systems, integration, fabrication, etc. We also discuss how memristor-based neuromorphic systems can mimic human brain's neuronal architecture with ~1011 neurons and ~1014 synapses for realizing future neuromorphic systems. We hope that this workshop can be a premier forum, where we review the recent challenges of memristor technology and discuss future possibility of artificial-intelligence hardware which can be based on memristor science and technology.

KEYNOTE AND INVITED SPEAKERS

Leon O. Chua, Berkeley, USA. He is widely known for his invention of the memristor and the Chua's Circuit. His research has been recognized internationally through numerous major awards, including 16 honorary doctorates from major universities in Europe and Japan, and 7 U.S. patents. He was elected as a foreign member of the European Academy of Sciences (Academia Europea) in 1997, a foreign member of the Hungarian Academy of Sciences in 2007, and an honorary fellow of the Institute of Advanced Study at the Technical University of Munich, Germany, in 2012. He was honored with many major prizes, including the Frederick Emmons Award in 1974, the IEEE Neural Networks Pioneer Award in 2000, the first IEEE Gustav Kirchhoff Award in 2005, the Guggenheim Fellow award in 2010, Leverhulme Professor Award (United Kingdom) during 2010 – 2011, and the EU Marie Curie Fellow award, 2013. Prof. Chua is a Recipient of the top 15 most cited authors Award in 2002 from all fields of engineering published during the 10-year period 1991 to 2001, from the Current Contents (ISI) database.

Daniele Ielmini, Politecnico Milano, Italy. He received the Laurea (cum laude) and Ph.D. in Nuclear Engineering from Politecnico di Milano in 1995 e 2000, respectively. He is a Full Professor at the Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, after appointments as Assistant Professor in 2002 and Associate Professor in 2010. He held visiting positions at Intel Corporation (2006), Stanford University (2006) and the University of Illinois at Urbana-Champaign (2010). His research interests include the modeling and characterization of non-volatile memories, such as nanocrystal memory, charge trap memory, phase change memory (PCM), resistive switching memory (RRAM), and spin-transfer torque magnetic memory (STT-MRAM). In 2016, he coedited the book 'Resistive switching - from fundamental redox-processes to device applications' for Wiley-VCH. He authored/coauthored 8 book chapters, more than 250 papers published in international journals and presented at international conferences, and 6 patents. His works received more than 5300 citations, with an H-index of 41 (Scopus, October 2016). He has served in several Technical Subcommittees of international conferences, such as IEEE-IEDM (2008 – 2009), IEEE-IRPS (2006 – 2008), IEEE-SISC (2008 – 2010), INFOS (2011 – 2017), ISCAS (2016 – 2017) and DATE (2017). He is a Senior Member of the IEEE. He was recognized a Highly Cited Researcher by Thomson Reuters in 2015. He received the Intel Outstanding Researcher Award in 2013, the ERC Consolidator Grant in 2014, and the IEEE-EDS Paul Rappaport Award in 2015.

Hyunsang Hwang received his Ph.D. in Materials Science from the University of Texas at Austin, USA in 1992. After five years at LG Semicon as a senior researcher, he became a Professor of Materials Science and Engineering at Gwangju Institute of Science and Technology (GIST), South Korea in 1997. Since 2012, he has been a Professor at Pohang University of Science and Technology (POSTECH), South Korea. He has published more than 360 journal papers and 32 IEDM/VLSI technology papers. His current research interests include neuromorphic device, ReRAM and selector devices.

Wei Lu, University of Michigan. His research interest includes high-density memory based on two-terminal resistive devices (RRAM), memristors and memristive systems, neuromorphic circuits, aggressively scaled nanowire transistors, and other emerging electrical devices. He received his B.S. (1996) and Ph.D (2003) in physics from Tsinghua University, Beijing, China, and Rice University, Houston, TX respectively. From 2003 to 2005, he was a postdoctoral research fellow at Harvard University, Cambridge, MA. He joined the faculty of the University of Michigan in 2005 and is currently a Professor and Director of the Lurie Nanofabrication Facility. He is an IEEE Fellow, Associate Editor for Nanoscale, a recipient of the NSF CAREER Award in 2009, EECS Outstanding Achievement Award in 2012, 2014-15 Rexford E. Hall Innovation Excellence Award, and the 2016 – 2017 David E. Liddle Research Excellent Award. To date he has published over 100 journal papers that have received over 20,000 citations with an h-factor of 61 (Google Scholar). Prof. Lu is currently advising 11 Ph.D. students and 3 Postdocs. He is also co-founder and Chief Scientist of Crossbar Inc, a Silicon Valley semiconductor company with over $100M VC funding to date to develop next generation non-volatile memories.

Said Hamdioui, TU Delft, Netherlands. He received the MSEE and PhD degrees (both with honors) from the Delft University of Technology, Delft, The Netherlands. He is currently with the Delft University of Technology. He has more than eight years of experience in industry and academia as a consultant and/or as researcher and developer on test issues in general and memory testing in particular. He spent a couple of years with Intel Corporation in Santa Clara and Folsom, California, where he was responsible for developing new low-cost and efficient test solutions for advanced Intel single-port and multiport embedded cache designs in the new generations of microprocessors. In addition, he spent more than one and half years with Philips Semiconductors in France and The Netherlands, where he was responsible for driving advanced product debug and yield ramp activities and for developing systematic ways of reducing the time in yield improvement for advanced semiconductor memories. Dr. Hamdioui is the author of a book and about 40 conference and journal papers in the area of testing; many of them are the result of cooperation with industrial partners (e.g., Intel, ST, Infineon, etc). His research interests include VLSI test and reliability, deep-submicron CMOS IC design and test, systematic fault modeling, test generation and optimization for semiconductor memories, design for testability, BIST, yield enhancement, product engineering, etc. He was the recipient of the European Design Automation Association (EDAA) Award for 2001. He is a member of the IEEE.

Abu Sebastian, IBM Zurich. He is a Principal Research Staff Member and Master Inventor at IBM Research - Zurich. He received a B. E. (Hons.) degree in Electrical and Electronics Engineering from BITS Pilani, India, in 1998 and M.S. and Ph.D. degrees in Electrical Engineering (minor in Mathematics) from Iowa State University in 1999 and 2004, respectively. He was a contributor to several key projects in the space of storage and memory technologies and currently leads the research effort on in-memory computing at IBM Zurich. Dr. Sebastian is a co-recipient of the 2009 IEEE Control Systems Technology Award and the 2009 IEEE Transactions on Control Systems Technology Outstanding Paper Award. In 2013 he received the IFAC Mechatronic Systems Young Researcher Award for his contributions to the field of mico-/nanoscale mechatronic systems. In 2015 he was awarded the European Research Council (ERC) consolidator grant. Dr. Sebastian served on the editorial board of the journal, Mechatronics from 2008 till 2015 and served on the memory technologies committee of the IEDM from 2015 – 2016.

Mirko Prezioso, Mentium Technologies Inc., Santa Barbara, USA. He received the M.S. degree in theoretical condensed matter physics and the Ph.D. degree in advanced materials science and technology from the University of Parma, Parma, Italy, in 2004 and 2008, respectively. Since 2013, he has been a Research Assistant Professor with the University of California at Santa Barbara, Santa Barbara, CA, USA, where he has been working on memristors and neuromorphic hardware.

Qiangfei Xia, University of Massachusetts, Amherst, USA. Dr. Qiangfei Xia is a professor of Electrical & Computer Engineering at UMass Amherst and head of the Nanodevices and Integrated Systems Lab . He received his Ph.D. in Electrical Engineering in 2007 from Princeton University, where he was a recipient of the Guggenheim Fellowship in Engineering (a graduate fellowship from Princeton). He then spent three years as a research associate in the Hewlett Packard Laboratories in Palo Alto, California. In October 2010, he joined the faculty of UMass Amherst as an assistant professor (tenure clock started in January 2011). He was promoted to an associate professor with tenure in January 2016 and then a full professor in September 2018. Dr. Xia's research interests include beyond-CMOS devices, integrated systems and enabling technologies, with applications in machine intelligence, reconfigurable RF systems and hardware security. He has received a DARPA Young Faculty Award (YFA), an NSF CAREER Award, and the Barbara H. and Joseph I. Goldstein Outstanding Junior Faculty Award. Dr. Xia teaches freshman to graduate level courses, including Introduction to Electrical and Computer Engineering (ENGIN 112), Semiconductor Devices (ECE 344), Microelectronic Fabrication (ECE571) and Nanostructure Engineering (ECE 597/697NS). He was nominated for the Distinguished Teaching Award (DTA), a campus-wide highest honor to recognize exemplary teaching at UMass. Dr. Xia serves as a technical committee member for the International Conference on Electron, Ion, and Photon Beam Technology and Nanofabrication (EIPBN) conference, and the IEEE International Symposium on Circuits and Systems (ISCAS), to name a few. He was the co-program chair for the 14th International Conference on Nanoimprint & Nanoprint Technology (NNT). He is also an active panelist for U.S. and international funding agencies, and a peer reviewer for tens of international archival journals and conferences. Within UMass, his most notable service is the building of a brand new clean room facility in the Marcus Hall. He is a senior member of IEEE and SPIE.

Kyeong-Sik Min, Kookmin University, Seoul, Korea. He received the B.S. degree in electronics and computer engineering from Korea University, Seoul, South Korea, in 1991, and the M.S.E.E. and Ph. D. degrees in electrical engineering from Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 1993 and 1997, respectively. In 1997, he joined Hynix Semiconductor, Inc., where he was engaged in the development of low-power and high-speed DRAM circuits. From 2001 to 2002, he was a Research Associate with the University of Tokyo, Tokyo, Japan, where he designed low-leakage memories and low-leakage logic circuits. In September 2002, he joined the Faculty of Kookmin University, Seoul, South Korea, where he is currently a Professor in the School of Electrical Engineering. He was a Visiting Professor with the University of California, Merced, Merced, CA, USA, from August 2008 to July 2009. His research interests include low-power VLSI, memory design, and power IC design. He is a member of the Institute of Electronics Engineers of Korea, and the Institute of Electronics, Information, and Communication Engineers in Japan. He was on various technical program committees, such as Asian Solid-State Circuits Conference, International SoC Design Conference, and Korean Conference on Semiconductors. He and his students were the recipient of the IDEC CAD & Design Methodology Award (2011), IDEC Chip Design Contest Award (2011), and IDEC Chip Design Contest Award (2012).

Fernando Corinto, Politecnico di Torino, Italy. He received the Laurea degree in electronics and the Ph.D. degree in electronics and communications engineering in 2001 and 2005, respectively, and the European Doctorate in 2005, all from the Politecnico di Torino, Torino, Italy. In 2004, he won a Marie Curie Fellowship (within the 'Marie Curie Actions' under the Sixth Framework Programme). He is currently an Assistant Professor of Circuit Theory with the Dipartimento di Elettronica, Politecnico di Torino. His research activities are mainly in the areas of nonlinear dynamical circuits and systems and locally coupled nonlinear/nanoscale networks. He is coauthor of more than 90 international journal and conference papers. He has been reviewer of several papers for international journals and

conferences and chair of sessions in international conferences. He is the principal investigator of several research projects. Since 2010, he is Senior Member of the IEEE, Member of the IEEE CAS Technical Committees on Cellular Nanoscale Networks and Array Computing and Nonlinear Circuit and Systems. He is also Visiting Professor at PPCU of Budapest, since 2007. Dr. Corinto was the Technical Program Chair for the 13th Workshop on Cellular Nanoscale Networks and their Applications and 3rd Symposium on Memristor.

Ronald Tetzlaff, TU Dresden, Germany. He is a Full Professor of Fundamentals of Electrical Engineering at Technische Universität Dresden, Germany. His scientific interests lie in the theory of signals and systems, system modelling and identification, Volterra systems, cellular nonlinear networks, and memristors. From 1999 to 2003 he was Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART I: REGULAR PAPERS. Prof. Tetzlaff was "Distinguished Lecturer" of the IEEE CAS Society (2001 – 2002). He is a member of the ITG, of the German Society of Electrical Engineers, and of the German URSI Committee.

Alon Ascoli received a Ph.D. Degree in Electronic Engineering from University College Dublin in 2006. From 2006 to 2009 he worked as RFIC analog engineer at CSR Sweden AB. From 2009 to 2012 he was Research Assistant in the Department of Electronics and Telecommunications at Politecnico di Torino. Since 2018 he is Scientific Collaborator with the Department of Microelectronics, Brno University of Technology, Brno, Czech Republic. Since 2012 he is Scientific Collaborator in the Faculty of Electrical and Computer Engineering, Technische Universität Dresden, where he is currently pursuing a Habilitation in Fundamentals of Electrical Engineering. His research interests lie in the area of nonlinear circuits and systems, networks of oscillators, Cellular Nonlinear Networks and memristors. Dr. Ascoli was honored with the International Journal of Circuit Theory and its Applications (IJCTA) 2007 Best Paper Award. He acts as Secretary for the Cellular Nanoscale Networks and Array Computing Technical Committee (CNNAC) since May 2017. In April 2017 he was conferred the habilitation title as Associate Professor in Electrical Circuit Theory from the Italian Ministry of Education. In November 2017 he was conferred a Performance Bonus Award from Technische Universität Dresden. Since 2014 he is Management Committee Substitute for Germany in the COST Action IC1401 MemoCIS "Memristors - Devices, Models, Circuits, Systems, and Applications". He has been Program Chair and Special Session Chair for the 15th International Workshop on Cellular Nanoscale Networks and their Applications (CNNA) in 2016. He is the Technical Program Chair for the International Conference on Memristive Materials, Devices, and Systems (MEMRISYS) 2019.

FRIDAY, 29 MARCH 2019

0830 – 0845 Opening session

0845 – 1000 Keynote: No Backtracking Rules the foundation of all non-volatile memristors
Leon O. Chua, UC Berkeley, US

1000 – 1030 Coffee Break

1030 – 1100 Emerging devices and circuits for analogue in-memory computing
Invited Speaker: Daniele Ielmini, Politecnico Milano, IT

1100 – 1130 Resistive switching based Synapse and Threshold switching based Neuron Devices for neuromorphic system
Invited Speaker: Hyunsang Hwang, POSTECH, KR

1130 – 1200 RRAM foundations for neuromorphic and in-memory computing systems
Invited Speaker: Wei Lu, University of Michigan, US

1200 – 1300 Lunch Break

1300 – 1330 Computation-in-Memory Based on Memristive Devices: What is all about and what is still missing?
Invited Speaker: Said Hamdioui, TU Delft, NL

1330 – 1400 Memristive circuits for neurocomputing and beyond: a progress update
Invited Speaker: Mirko Prezioso, Mentium Technologies Inc., US

1400 – 1430 Computing using imprecise computational memory
Invited Speaker: Abu Sebastian, IBM Zurich, CH

1430 – 1500 Coffee Break

1500 – 1530 Memristive Crossbar Arrays for Brain-Inspired Computing
Invited Speaker: Qiangfei Xia, University of Massachusetts, Amherst, US

1530 – 1555 Memristor-crossbar-based neural networks: from ideal to reality
Invited Speaker: Kyeong-Sik Min, Kookmin University, KR

1555 – 1620 Computing with Memristor Oscillatory Networks
Invited Speaker: Fernando Corinto, Politecnico di Torino, IT

1620 – 1645 Memristor Cellular Neural Network-inspired Paradigms for Signal Processing
Invited Speaker: Ronald Tetzlaff, TU Dresden, DE

1645 – 1710 Store / Retrieve Gene Design and Analysis for Bistable-like Memristor CNN
Invited Speaker: Alon Ascoli, TU Dresden, DE

W03 DATE Workshop on Autonomous Systems Design (ASD2019)

Room 1 0830 – 1730

Organisers:
Rolf Ernst, TU Braunschweig, DE
Selma Saidi, Hamburg University of Technology, DE
Dirk Ziegenbein, Robert Bosch GmbH, DE

ASD is the 1st international workshop on Autonomous Systems Design. The goal of ASD is to explore recent industrial and academic methods and methodologies in autonomous systems design. This includes several areas:

- Embedded and cyber-physical systems platforms that implement and execute the autonomous system functions including their architectures, hardware, software and communication.
- The design for autonomous systems including processes, modelling, optimization, verification, validation, and test.
- All aspects of dependable systems design for autonomous systems including, but not limited to, functional safety concepts, fail-operational systems design, functional safety for applications with machine learning, safe and secure changes and updates, autonomous systems security.

HIGHLIGHTS

The workshop consists of regular sessions with papers selected from an open call for papers, complemented by invited talks, and an exhibition with posters and live demos. In addition, the workshop will feature the two following distinguished keynotes:

0830 – 0950 Keynotes Session

Keynote 1
Challenges of Automated and Connected Driving

Thomas Form, Head of Electronics and Vehicle Research, Volkswagen AG, DE

In recent years, various publications and presentations from a lot of companies have shown the improvements in the sector of automated driving. The vehicle- and mobility-concept SEDRIC is a current example from the Volkswagen AG. However, for a release of these technologies there are several unresolved issues regarding sensor technologies, redundancies as well as verification and validation questions. Regarding sensors, the main objectives are miniaturization and reduction of system costs. Advantages and disadvantages of existing solutions have to be evaluated. In addition to economic aspects, ensuring the redundancy of the system is absolute necessary. Is, for example, Artificial Intelligence able to provide an independent second or third function path? Regarding verification and validation concepts, current discussions are focused on which scenarios have to be tested and how, in order to enable regulatory authorities to approve the release of automated driving functions? It is conceivable, that this is an automotive industry wide task that can only be solved in cooperation with all stakeholders

Born in 1959, Thomas Form studied Electrical Engineering at the University of Braunschweig, Germany, joined the Institute for Communication Engineering as research fellow in 1987 and received his Ph.D. in 1992. Up to 2002 he worked as a senior engineer in the Centre for Electromagnetic Compatibility of Volkswagen AG. In 2002 Dr. Form was appointed as the head of Telephone-/Telematics and Antenna systems development. He became a professor for "Electronic Vehicle Systems" in the Institute of Control Engineering at the Technical University Braunschweig in 2005 and participated with the CAROLO-Team in the finals of the DARPA URBAN Challenge 2007. From 2007 to 2009 he was responsible for concept development, module- and project management in the VW Electric/Electronic development. In 2009 he was appointed as head of the "Elec-

tronics and Vehicle Research" within Volkswagen Group research. Major achievements were the presentation of AUDI "Jack" vehicle driving in L3 automatic mode with Journalists from San Francisco to CES 2015 in Las Vegas and the presentation of the autonomous driving pod "SEDRIC" in 2017. Since 2016 he is the coordinator of the German national funded project PEGASUS which wants to answer the question "L3 Highway Chauffeur – how safe is safe enough and how to prove it". He got the Uni-DAS e.V. ADAS Award for significant influence on the development and introduction of driver assistance systems in 2017.

Keynote 2:
AUTOSAR Adaptive – Challenging the Impossible

Masaki Gondo, Software CTO at eSOL Co., Ltd., JP

The vast researches related to autonomous driving seem steadily progressing - it no longer makes news to just have some research vehicle drive autonomously. However, bringing this technology to the market, with all the associated legal, societal, and ethical responsibilities, with justifiable cost efficiency, is hard at its best, and impossible at its worst. Furthermore, the automotive industry is facing drastic challenges in electric vehicles, connected services, which also heavily impact the whole vehicle architecture.AUTOSAR (AUTomotive Open System ARchitecture) is a worldwide development partnership of automotive interested parties. One of its latest challenges is to develop the software platform specification for the highly automated and autonomous driving, named AUTOSAR Adaptive Platform. This talk gives an overview of the challenges of such a platform, followed by the solution approach of AUTOSAR reflecting the industrial needs, and the overall architecture of AUTOSAR Adaptive. It also introduces a new multi-kernel OS technology the author develops, describing why such OS architecture is essential for coping with the challenge in the long run.

Masaki is CTO at eSOL, the company that provides POSIX/AUTOSAR/TRON RTOS, various software development tools, and various engineering services. Graduated from the State University of New York, Masaki has more than 20 years of experience in the field of OS architecture and related technologies for use in wide range of embedded system applications including automotive, industrial, and electronic appliances. He has authored/co-authored multiple popular Japanese books/international articles on OS and embedded systems, and given technical talks in conferences worldwide. While serving as a CTO directing the technology strategy and architecture at eSOL, he acts as one of the architects in Task Force Architecture of Adaptive Platform. His interest in recent years spans from next-generation OS/platform architectures, parallel processing, adaptive systems including machine learning, as well as scrum/kanban based development.

0950–1000 **Interactive Presentations**

IP1: A Dependable Detection Mechanism for Intersection Management of Connected Autonomous Vehicles
Rachel Dedinsky, Mohammad Khayatian, Mohammadreza Mehrabian and Aviral Shrivastava
Arizona State University, USA

IP2: A LIDAR Only Perception System for Autonomous Vehicle
Mohamed Yazid Lachachi, Abdelmalik Taleb-Ahmed, Smail Niar and Mohamed Ouslim
Université Polytechnique Hauts-de-France, FR

IP3: Generation of a Reconfigurable Probabilistic Decision Making Engine based on Decision Networks: UAV Case Study
Sara Zermani and Catherine Dezan
Lab-STICC, FR

1000–1030 Coffee Break

1030–1200 **Development Approaches for Autonomous Systems**

1030 Bringing the Next Generation Robot Operating System on Deeply Embedded Autonomous Platforms
Ralph Lange, Robert Bosch GmbH, DE

1100 IDF-Autoware: Integrated Development Framework for ROS-based Self-driving Systems Using MATLAB/Simulink
Shota Tokunaga[1], Yuki Horita[2], Yasuhiro Oda[2] and Takuya Azumi[3]
[1]Graduate School of Engineering Science, Osaka University
[2]Hitachi Automotive Systems, Ltd
[3]Graduate School of Science and Engineering, Saitama University, JP

1120 Feasibility Study and Benchmarking of Embedded MPC for Vehicle Platoons
Inaki Martin Soroa[1], Amr Ibrahim[1], Dip Goswami[1] and Hong Li[2]
[1]Eindhoven University of Technology
[2]NXP Semiconductor, NL

1140 A Multiview Approach Toward Updatable Vehicle Automation Systems
Marcus Nolte, Mischa Möstl, Johannes Schlatow and Rolf ErnstTechnical University of Braunschweig, DE

1200–1300 Lunch Break

1300–1430 **Dependable Autonomous Systems**

1300 Autonomous Data Center – Feedback Control for Predictable Cloud Computing
Martina Maggio, University of Lund, SE

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1330 **Fault-Tolerance by Graceful Degradation for Car Platoons**
Mohammed Baha E. Zarrouki[1], Verena Klös[1], Markus Grabowski[2] and Sabine Glesner[1]
[1]Technische Universität Berlin, DE, [2]Assystem Germany GmbH

1350 **Safety and Security Analysis of AEB for L4 Autonomous Vehicle using STPA**
Shefali Sharma[1], Adan Flores[1], Chris Hobbs[2], Jeff Stafford[3] and Sebastian Fischmeister[1]
[1]University of Waterloo, CA
[2]QNX Software Systems Limited,CA
[3]Renesas Electronics America Inc.

1410 **Towards a Formal Model of Recursive Self-Reflection**
Axel Jantsch, TU Wien, AT

1430 – 1500 Coffee Break

1500 – 1630 Research Clusters on Autonomous Systems

1500 **An approach to automotive service-oriented software architectures in a multi-partner research project**
Stefan Kowalewski, RWTH Aachen, DE

1530 **Controlling Concurrent Change- Design Automation for Critical Systems Integration**
Rolf Ernst, TU Braunschweig, DE

1600 **Panel Discussion**

1630 – 1730 Closing & Exhibition

W04 6th Workshop on Design Automation for Understanding Hardware Designs (DUHDE6)

Room 9 0830 – 1730

Organisers and Moderators:
Christian Krieg, Vienna University of Technology, AT
Oliver Keszöcze, Friedrich-Alexander-Universität Erlangen-Nürnberg, DE

Programme Committee Members:
Maciej Ciesielski, University of Massachusetts, US
Azadeh Davoodi, University of Wisconsin-Madison, US
Görschwin Fey, Technische Universität Hamburg, DE
Tara Ghasempouri, Tallinn University of Technology, EE
Ian Harris, University of Californa Irvine, US
Jan Malburg, German Aerospace Center, DE
Heinz Riener, EPFL, CH
Jannis Germany Stoppe, DFKI GmbH, DE
Pramod Subramanyan, Indian Institute of Technology Kanpur, IN
Georg Weissenbacher, Vienna University of Technology, AT
Clifford Wolf, Symbiotic EDA, AT
Cunxi Yu, EPFL, CH

Understanding a hardware design can be a tough process. When entering a large team as a new member, when extending a legacy design, or when documenting a new design, a lack in understanding the details of a design is a major obstacle for productivity. In software engineering, topics like software maintenance, software understanding or reverse engineering are well established in the research community and partially tackled by tools. In the hardware area, the re-use of IP-blocks, the growing size of designs and design teams leads to similar problems. Understanding of hardware requires deep insight into concurrently operating units, optimizations to reduce the required area, and specially tailored functional units for a particular use. In hardware security, it is vital to verify properties for security-critical paths of a design, which includes to fully understand a design pre- and post-synthesis.

TOPICS

The workshop focus includes but is not limited to the following topics in design understanding:

- Design descriptions from the formal specification level (FSL) to electronic system level(ESL) down to register transfer level (RTL)
- Extraction of high-level properties
- Knowledge extraction from design structures at any level of abstraction
- Feature localization: Localization of code implementing specialized functionality
- Data/Control path extraction
- Reverse engineering
- Innovative GUIs for design and verification
- Analysis of interaction between hardware and software
- Metrics for (open-source) intellectual property (IP) cores
- Formal methods for design understanding
- Machine learning for design understanding
- Future applications of design understanding

0830 – 0845 Workshop opening

Moderators: Christian Krieg, TU Wien, AT
Oliver Keszöcze, Friedrich-Alexander-Universität Erlangen-Nürnberg, DE

FRIDAY, 29 MARCH 2019

0845 – 0930 **Invited talk: Addressing Integrated Circuit Integrity Using Statistical Analysis and Machine Learning Techniques**
Speaker: Burcin Cakir, Princeton University, US

Burcin Cakir received her B.S. degree from Electrical Engineering Department of Bilkent University, and her Ph.D. degree from Princeton University. Her research motivation is formulating models that can represent real systems accurately and express mathematical bases/frameworks for further analysis. She had experience in developing algorithms and analyses to help design secure hardware systems. She is a recipient of Francis Robbins Upton Fellowship award from Princeton University. Her work on Hardware Trojan detection received Best Paper Award at DATE Conference (2015). She also has served as a referee on various journals and conferences and gave workshop and seminar talks. Besides her work at Princeton, she also had experience in industry research with two internships at Microsoft Research (MSR) in Redmond and Cambridge Labs.

0930 – 1000 **Paper presentation block 1**

0930 Towards Gate-Level Design of QCA Circuits

1000 – 1030 Coffee Break

1030 – 1200 **Paper presentation block 2**

1030 Deductive Binary Code Verification Based on Source-Code-Level ACSL Specifications

1100 Extracting Assertions for Conflicts in HDL Descriptions

1130 Complete Specification Mining

1200 – 1300 Lunch Break

1300 – 1400 **Invited talk: Reverse Engineering for Security: Views From the Top and the Bottom.**
Speaker: Pramod Subramanyan, Indian Institute of Technology Kaipur, IN

Recent years have seen much hand-wringing about security concerns posed by malicious hardware designs. Seemingly at the other end of the spectrum are inadvertent hardware design flaws that lead to security breaches. The former concern has led to development of algorithmic reverse engineering techniques, Hardware Trojan detection algorithms and side-channel analysis algorithms – all of which aim to algorithmically discover malicious behavior from the bottom up. The latter concern has led to the progress in top-down security verification techniques based on model checking and syntax-guided synthesis. In this talk, I will try to review some recent progress in both top-down and bottom-up analysis. I will argue that both top-down and bottom-up techniques can synergistically benefit each other.

Pramod Subramanyan is an Assistant Professor in the Department of Computer Science and Engineering at the Indian Institute of Technology, Kanpur. He obtained his Ph.D. from Princeton University and subsequent to his Ph.D., he was a postdoctoral scholar at the University of California, Berkeley. His research interests lie at the intersection of systems security and formal methods. His current research is focused on system-building techniques that can provide verifiable guarantees of security. Pramod's research has won several awards including the Best Paper Award at the ACM Computer and Communication Security conference, the ACM SIGDA Outstanding Ph.D. Dissertation in Electronic Design Automation Award, the Best Student Paper Award at IEEE Symposium on Hardware-Oriented Security and Trust.

1400–1430 Paper presentation block 3

1400 Generating a UML Sequence Diagram from a Natural Language Scenario Description

1430–1500 Coffee Break

1500–1600 Invited talk: Project Trellis: open bitstream documentation for the Lattice ECP5 FPGAs

Speaker: David Shah, Symbiotic EDA, GB

The Lattice ECP5 is a family of mid-range (up to 85k logic cells) FPGAs. Project Trellis has created open source bitstream, architecture and timing documentation for them; in order to open up a better understanding of their internals. This has led to the development of an end-to-end open source Verilog to bitstream flow for these parts using Yosys for synthesis and nextpnr for place-and-route, and opens the door to low-level experimentation not possible within the constraints of the vendor FPGA tools. Open source compilers such as GCC and LLVM are now widely used and accepted in the software development community; and developing open bitstream documentation is a first step to bringing the FPGA ecosystem to parity with this.

This talk will describe the processes used to build this open documentation, detail some of the interesting lessons learnt along the way, and describe some of the possibilities that bitstream documentation bring for development and verification - with almost everything discussed equally applicable to FPGAs from other vendors.

David Shah is a engineer at Symbiotic EDA and a Electronic and Information Engineering student at Imperial College London. He entered the world of open source FPGAs by extending Project Icestorm, the iCE40 bitstream documentation project, to include the newer iCE40 UltraPlus FPGAs. As well developing Project Trellis, he has been involved in the development of a new open source FPGA place-and-route tool, nextpnr.

1600–1730 Paper presentation block 4

1600 Engineering of an Effective Automatic Assertion-based Verification Platform

1630 Design Mapper: Dataflow Analysis for Better Floorplans

1700 Using AI for the Performance Verification of High-End Processors

1715 The Verification Cockpit - Harnessing Data Analytics for the HW Verification Process

FRIDAY, 29 MARCH 2019

W05 AxC: 4th Workshop on Approximate Computing

Room 5 0830 – 1700

Programme Chair: Alberto Bosio, INL, FR

General Co-Chairs:
Mario Barbareschi, University of Naples Federico II, IT
Claus Braun, University of Stuttgart, DE

AIM OF THE WORKSHOP:

The investigation of connections between AxC paradigm and the verification, the test and the reliability of digital circuits from two points of view:

- how the approximate computing paradigm impacts the design and manufacturing flow of integrated circuits;
- how the verification, testing and reliability disciplines can be exploited in the approximate computing paradigms.

KEYNOTES:

- Prof. Kaushik Roy, title: Re-Engineering Computing with Neuro-Inspired Learning: Devices, Circuits, Systems. and Approximations
- Dr. Cristiano Malossi, title: Transprecision Computing for Energy-Efficiency

0830 – 0900 Opening Session

0900 – 1000 Keynote 1: Re-Engineering Computing with Neuro-Inspired Learning: Devices, Circuits, Systems. and Approximations
Kaushik Roy, School of Electrical and Computer Engineering of Purdue University, US

1000 – 1030 Coffee Break

1030 – 1200 Technical Session 1

Resilience-based Mapping of Deep Neural Network Operations to Approximate Computing Units
Christoph Schorn[1], Matthias Roth [2], Andre Guntoro[1] and Gerd Ascheid[3]
[1]Robert Bosch GmbH, DE, [2] Esslingen University of Applied Sciences, DE, [3]RWTH Aachen University, DE

Noise Budgeting in Multiple-Kernel Word-Length Optimization
Van-Phu Ha, Tomofumi Yuki and Olivier Sentieys, University of Rennes 1, FR

Reliability Evaluation of Mixed-Precision Architectures
Paolo Rech, Fernando Fernandes dos Santos and Daniel Oliveira, UFRGS, BR

Approximate Computing of Transcendental Functions Applied to Artificial Neural Networks
Xin Fan, Arthur Ruder, Cecilia Höffler and Tobias Gemmeke, IDS, RWTH Aachen Univ, DE

1200–1300 Lunch Break

1300–1330 **Invited Talk: Approximate Computing in HPC: building from ground up**
Alessandro Cilardo, Università degli Studi di Napoli Federico II, IT

1330–1430 **Keynote 2: Transprecision Computing for Energy-Efficiency**
Cristiano Malossi, IBM Research of Zurich, CH

1430–1500 Coffee Break

1500–1700 **Technical Session 2**

Targeting Approximation through Data Lifetime: A Quest for Optimization Metrics
Alessandro Savino[1], Michele Portolan[2], Stefano Di Carlo[1] and Regis Leveugle[2]
[1]Politecnico di Torino, IT, [2]University Grenoble Alpes, TIMA, FR

Jump Search: A Fast Technique for the Synthesis of Approximate Circuits
Linus Witschen, Hassan Ghasemzadeh Mohammadi, Matthias Artmann and Marco Platzner, Paderborn University, DE

An Approximate Communication Technique for Energy Efficient Networks on Chip
Giuseppe Ascia[1], Vincenzo Catania[1], John Jose[2], Salvatore Monteleone[1], Maurizio Palesi[1] and Davide Patti[1]
[1]University of Catania, IT, [2] Indian Institute of Technology Guwahati, IN

Adjustable Precision Computing Using Redundant Arithmetic
Ali Skaf, Mona Ezzadeen, Mounir Benabdenbi and Laurent Fesquet, TIMA, FR

Towards One Million Component Library of Approximate Circuits
Lukas Sekanina, Zdenek Vasicek and Vojtech Mrazek, Brno University of Technology, CZ

Exploiting Approximate Computing to Increase System Lifetime
E. Sanchez[1], P. Bernardi[1] and W. J. Perez-Holguin[2]
[1]Politecnico di Torino, IT, [2]Universidad Pedagógica y Tecnológica de Colombia, CO

Approximate Computing for Sizing Hidden Layer in CNN
Stefano Marrone and Carlo Sansone, University of Naples Federico II, IT

W06 2nd International Workshop on Embedded Software for the Industrial IoT (ESIIT 2019)

Room 6 0845 – 1615

Organisers:
Oliver Bringmann, University of Tuebingen / FZI, DE
Wolfgang Ecker, Infineon Technologies, DE
Wolfgang Müller, Paderborn University, DE
Daniel Müller-Gritschneder, Technische Universität München, DE

MOTIVATION AND OBJECTIVES

The Internet-of-things (IoT) is emerging as the backbone for industrial automation. The tremendous impact of IoT to industrial applications is a key reason for IoT research and developments to grow dramatically in importance and economic impact for the next decade. At the edge of the IoT, ultra-thin devices with extremely small software memory footprints need to be cheap and capable to run with extremely small amounts of energy support over a very long lifetime. At the same time, IoT software must provide smart functions including real-time computing capabilities, connectivity, security, safety, and remote update mechanisms. These constraints put a high pressure on IoT software development based on the specific properties of IoT devices.

The ESIIT 2019 joint academic/industry workshop will focus on software development and maintenance of IoT devices addressing the very limited resources and power dissipation of IoT edge nodes in the context of a very long life cycle in an operational IoT network. This covers issues like software synthesis, configurability, safety, security, upgrades, fault recovery, maintenance as well as constraints and opportunities from newly emerging IoT hardware platforms. The workshop intends to provide an open platform for exchange and communication on new directions and requirements to academia and industry. We plan to especially give industrial speakers and leading research experts a platform to present the requirements and most recent results in today's and future industrial IoT-constrained software development and maintenance. The main objectives are:

- to invite industrial experts to present current and future needs and requirements
- to present and discuss novel technologies and ideas from different research areas and domains
- to explore and align trends and future needs for IoT platform development and maintenance from the perspective of academia and industry.

HIGHLIGHTS

ESIIT 2019 will feature a range academic talks with poster presentation as well as three invited industrial presentations.

- Invited talk from Michael Velten (Infineon Technologies AG)
  Title: Proposals for IP-XACT Extensions from Embedded Controller Use Cases
- Invited talk from Aljoscha Kirchner (Robert Bosch GmbH)
  Title: Automation of Embedded Software Development for Smart Sensor ASICs
- Invited talk from Thomas Kuhn (Fraunhofer IESE
  Title: BaSys 4.0: An Open Source Middle for the Industrial Internet of Things

0845 – 0900 Opening

0900 – 1000 Session I: Invited Industrial Session

0900 Proposals for IP-XACT Extensions from Embedded Controller Use Cases
Michael Velten and Wolfgang Ecker, Infineon Technologies, DE

0930 Automation of Embedded Software Development for Smart Sensor ASICs
Aljoscha Kirchner[1], Jan-Hendrik Oetjens[1] and Oliver Bringmann[2]
[1]Robert Bosch GmbH, DE; [2]Universität Tübingen, DE

1000 – 1030 Coffee Break & Poster Discussions

1030 – 1130 Session II: Applications for the IOT

1030 An Experimental Platform for Cooperative Work with Context-Oriented Programming and Hardware Reconfiguration for Industry IoT
Harumi Watanabe[1], Mikiko Sato[1], Ikuta Tanigawa[2], Mariya Kawamura[1], Nobuhiko Ogura[3] and Takeshi Ohkawa[4]
[1]Tokai University, JP; [2]Kyushu University, JP; [3]Tokyo City University, JP; [4]Utsunomiya University, JP

1045 Inertial Sensor Based Robot Gesture Detection for Safe Human-Robot Interaction
Johann-Peter Wolff[1], Christian Haubelt[1], Rolf Schmedes[2] and Kim Grüttner[2]
[1]University of Rostock, DE; [2]OFFIS - Institut für Informatik, DE

1100 An Open-Source, IoT-Tailored Face Detection Software
Panagiotis Kalodimas[1], Antonis Nikitakis[1] and Ioannis Papaefstathiou[2]
[1]Technical University of Crete, GR; [2]Aristotle University of Thessaloniki, GR

1115 Component-based FPGA Development of Intelligent Image Processing for Industrial IoT Devices
Kenta Arai, Takeshi Ohkawa, Kanemitsu Ootsu and Takashi Yokota, Utsunomiya University, JP

1130 – 1200 Session III: Invited Industrial Presentations

1130 BaSys 4.0: An Open-Source Middleware for the Industrial Internet of Things
Frank Schnicke, Markus Damm and Thomas Kuhn, Fraunhofer IESE, DE

1200 – 1300 Lunch Break & Poster Discussions

1300 – 1430 Session IV: Safety, Security, Performance and Power Optimizations & Analysis for the IoT

1300 Firmware-Driven Optimization of the Hardware/Software Interface for IoT Nodes
Rafael Stahl, Daniel Müller-Gritschneder and Ulf Schlichtmann, TUM, DE

1315 A Heuristic for Multi Objective Software Application Mappings on Heterogeneous MPSoCs
Gereon Führ[1], Ahmed Hallawa[1], Rainer Leupers[1], Gerd Ascheid[1] and Awaid-Ud-Din Shaheen[2]
[1]RWTH Aachen, DE; [2]Silexica GmbH, DE

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1330 **Source-level Power Simulation of IoT Firmware for Energy Evaluation**
Michael Kuhn and Oliver Bringmann, Universität Tübingen, DE

1345 **Towards Distributed Runtime Monitoring with C++ Contracts**
Rolf Schmedes and Philipp Ittershagen, OFFIS - Institut für Informatik, DE

1400 **Security Chain Tool for IoT Secure Applications**
Christoph Schmittner and Abdelkader Magdy Shaaban, Austrian Institute of Technology, AT

1415 **QEMU for Dynamic Memory Analysis of Security Sensitive Software**
Peer Adelt[1], Bastian Koppelmann[1], Wolfgang Müller[1], Christoph Scheytt[1] and Benedikt Driessen[2]
[1]Heinz Nixdorf Institute, DE; [2]Kasper & Oswald GmbH, DE

1430 – 1500 Coffee Break & Poster Discussions

1500 – 1600 Session V: Model Based Frameworks for IoT Software Development

1500 **A Syntax Oriented Code Generation Approach for SoC Design Automation**
Michael Werner, Andreas Neumeier and Wolfgang Ecker, Infineon Technologies, DE

1515 **Ecosystem for Agile Design of Future-Proof RISC-V Based IoT-Devices**
Leon Hielscher[1], Frederik Haxel[1], Arthur Kühlwein[1], Sebastian Reiter[1], Alexander Viehl[1], Oliver Bringmann[1] and Wolfgang Rosenstiel[2]
[1]FZI Forschungszentrum Informatik, DE; [2]University of Tübingen, DE

1530 **Towards Stateflow Model-Aware Debugging Using Model-to-Source Tags with LLDB**
Bewoayia Kebianyor, Philipp Ittershagen and Kim Grüttner, OFFIS - Institut für Informatik, DE

1545 **Tackling the Challenges of Internet-of-Things-Development Using Models**
Rupert Schlick and Willibald Krenn, Austrian Institute of Technology, AT

1600 – 1615 Plenary Discussions & Closing

W07 Workshop on Machine Learning for CAD

Room 7 0830–1730

Organisers:
Hussam Amrouch, Karlsruhe Institute of Technology (KIT), DE
Jörg Henkel, Karlsruher Institut für Technologie (KIT), DE
Marilyn Wolf, Georgia Tech, US

This workshop focuses on machine learning methods for all aspects of CAD and electronic system design. Advances in machine learning (ML) over the past half-dozen years have revolutionized the effectiveness of ML for a variety of applications. However, design processes present challenges that require parallel advances in ML and CAD as compared to traditional ML applications such as image classification. As such, the purpose of the workshop is to discuss, define and provide a roadmap for the special needs for ML for CAD where CAD is broadly defined as design time techniques as well as run-time techniques. The results of the workshop will be published in a special issue at ACM Transactions on Design Automation of Electronic Systems (TODAES).

Invited Speakers and Panelists:

Krishnendu Chakrabarty, Duke University,US
Rolf Drechsler, University of Bremen, DE
Paul Franzon, North Carolina State University, US
Siddharth Garg, New York University, US
Georges Gielen, KU Leuven, BE
Rajesh Gupta, UC San Diego, US
Ulf Schlichtmann, TU Munich, DE
Dimitrios Soudris, University of Athens, GR
Norbert Wehn, TU Kaiserslautern, DE
Kai-Chiang Wu, National Chiao Tung University, TW
Lilia Zaourar, CEA-LIST, FR

0830 **Design Space Exploration using Machine Learningo**

0830–0900 Machine Learning Approaches for Efficient Design Space Exploration of Application-specific NoCs
Ulf Schlichtmann, TU Munich, DE

0900–0930 Machine Learning for Design Space Exploration of CPS
Lilia Zaourar, CEA-LIST, FR

0930–1000 Machine Learning Techniques for VLSI CAD
Rajesh Gupta, UC San Diego, US

1000 Coffee Break

1030 Design for Reliability using Machine Learning

1030–1100 Resilience Evaluation for Approximating SystemC Designs Using Machine Learning Techniques
Rolf Drechsler, University of Bremen, DE

1100–1130 ML4TPU: Machine Learning for Energy Efficient and Reliable ML Hardware
Siddharth Garg, New York University, US

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1130 – 1200 Learning-based methodologies for assessing chip health in terms of aging and reliability
Kai-Chiang, National Chiao Tung University, TW

1200 Lunch Break

1300 Design-Time and Run-Time Machine Learning Techniques for SoCs

1300 – 1330 Designing Your Circuits with Robots
Paul Franzon, North Carolina State University, US

1330 – 1400 Predictive Analytics for Run-Time Anomaly Detection and Failure Prediction in Complex Core Routers
Krishnendu Chakrabarty, Duke University, US

1400 – 1430 A Methodology for Application Implementation onto 3-D FPGAs
Dimitrios Soudris, University of Athens, GR

1430 Coffee Break

1500 Machine Learning for Circuit Modeling

1500 – 1530 AI learning techniques in design and test of analog integrated circuits
Georges Gielen, KU Leuven, BE

1530 – 1600 Modeling of DRAM Behavior with Recurrent Neural Networks
Norbert Wehn, TU Kaiserslautern, DE

1600 – 1615 Poster: Machine Learning in Logic Synthesis
Lukas Sekanina, Brno Institute of Technology, CZ

1615 – 1630 Poster: Fast FPGA Routing Algorithm using Graph Neural Network
Huiyuan Song, PKU Advanced Institute of Information Technology, CN

1630 Panel: Where Do We Go From Here?

Panelists:
Paul Franzon, North Carolina State University, US
Rajesh Gupta, UC San Diego, US
Lilia Zaourar, CEA-LIST, FR
Norbert Wehn, TU Kaiserslautern, DE

Moderator: Marilyn Wolf, Georgia Tech, US

1730 Workshop Wrap-up
Joint dinner with discussion of future plans (buy-your-own-meal)
Location: Ristorante Buca Mario

W08 Grand Challenges and Research Tools for Quantum Computing

Room 10 0830–1730

Organiser: Ali Javadi, IBM, US

WORKSHOP DETAILS:

Quantum computing is at an inflection point, where 72-qubit (quantum bit) machines have been built, 100-qubit machines are just around the corner, and even 1000-qubit machines are perhaps only a few years away. These machines have the potential to fundamentally change our concept of what is computable and demonstrate practical applications in areas such as quantum chemistry, optimization, and quantum simulation.

Yet a significant resource gap remains between practical quantum algorithms and near-term machines. Software and architectures are what are needed to increase the efficiency of algorithms and machines and close this gap. There is a urgent shortage of the necessary computer scientists to work on closing this gap (there are over 60 public and private companies trying to hire in this area).

This workshop will outline the grand research challenges in closing this gap, including programming language design, software and hardware verification, defining and perforating abstraction boundaries, cross-layer optimization, managing parallelism and communication, mapping and scheduling computations, reducing control complexity, machine-specific optimizations, and many more. Some of these challenges can be approached with minimal quantum computing background and some will require greater depth.

We will introduce the basic concepts and resources to enable researchers to begin to delve into these challenges. We will also introduce quantum algorithms of near-term significance.

Finally, we will provide an overview and hands-on experience with an end-to-end set of software tools from a high-level programming language to running experiments on cloud-access IBM quantum machines. These tools will be a combination of the Scaffold Quantum Programming Language/Compiler and the IBM Qiskit tools and interfaces.

This workshop will be highly interactive. Participants will install our tools and work with code examples running on real quantum hardware at IBM, all organized within Jupyter notebooks, throughout the afternoon.

ORGANISERS

Fred Chong (UChicago) – co-author of the Scaffold compiler and simulation tools for quantum computing and a synthesis lecture on quantum computing for computer architects.

Ken Brown (Duke) – Leading researcher in the control of quantum systems for both understanding the natural world and developing new technologies. His current research areas are the development of robust quantum computers and the study of molecular properties at cold and ultracold temperatures.

Andrew Cross (IBM Research) – Researcher in quantum computing theory, author of the Quantum Assembly (QASM) language and the Qiskit compiler for cloud-access to IBM quantum machines, and expert in quantum error correction.

Diana Franklin (UChicago) – Education lead of EPiQC. Co-author of the Scaffold compiler and simulation tools for quantum computing.

Ali Javadi-Abhari (IBM Research) – co-author of the Scaffold compiler and simulation tools for quantum computing and researcher for IBM's Qiskit quantum computing tools and cloud access to IBM's prototype machines.

TEACHING ASSISTANTS

Pranav Gokhale (UChicago) – second year PhD student in quantum computer architecture

Xin-Chuan (Ryan) Wu (UChicago) – third year PhD student in quantum computer architecture

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0830	Intro to Grand Challenges in Quantum Computing Fred Chong (UChicago)
1000	Coffee Break
1030	Basics of Quantum Computing Diana Franklin (UChicago)
1200	Lunch Break
1300	Basic Algorithms, Tools for Compilation (Hands-on Demo) Ali Javadi-Abhari (IBM)
1430	Coffee Break
1500	Algorithms for Quantum Chemistry Ken Brown (Duke)
1730	Workshop Wrap-up

W09 Quo vadis, Logic Synthesis?

Room 8 0830 – 1730

Organisers:
Tiziano Villa, Dipartimento d'Informatica, Università di Verona, IT
Luca Carloni, Columbia University, US

Speakers:
Luca Amaru, Synopsys, US
Anna Bernasconi, Università di Pisa, IT
Valentina Ciriani, Università degli Studi di Milano, IT
Jordi Cortadella, Universitat Politecnica de Catalunya, ES
Masahiro Fujita, University of Tokyo, JP
Jie-Hong Jiang, National Taiwan University, TW
Weikang Qian, Shanghai Jiao Tong University, CN
Sherief Reda, Brown University, US
Marc Riedel, University of Minnesota, US
Tsutomu Sasao, Meiji University, JP
Mathias Soeken, Integrated System Laboratory – EPFL, CH
Andres Takach, Calypto Design Systems, US
Gabriella Trucco, Università degli Studi di Milano, IT
Luca Carloni, Columbia University, US
Tiziano Villa, Dipartimento d'Informatica, Università di Verona, IT

In 1984, the book on Espresso by R. Brayton, G. Hachtel, C. McMullen and A. Sangiovanni-Vincentelli provided the first layer of the foundations of modern logic synthesis. The work done around that time by leading academic and industrial research laboratories triggered the first wave of modern logic design tools like Espresso, MIS, SIS and VIS, which then became the backbone of the industrial design chains offered by the newborn Electronic Design Automation Industry. After many research breakthroughs and industrial successes, it is time for an assessment of the perspectives of logic synthesis, both as a core technology in digital system design and an enabling technology in other domains (biological synthesis, machine learning for data analysis, etc.). To achieve this goal, this workshop brings together an inclusive list of speakers from both academia and industry, to report on the state-of-art and strategic directions of the field.

0830 – 0840 **Introduction**
Luca Carloni, Columbia University, US and
Tiziano Villa, Dipartimento d'Informatica, Università di Verona, IT

0840 – 0900 **Thirty-five years after the Espresso book: a retrospective on logic synthesis**
Tiziano Villa, Dipartimento d'Informatica, Università di Verona, IT

0900 – 1000 **Algorithmic foundations of logic synthesis - Part 1**

Extracting functions from Boolean relations
Jordi Cortadella, Universitat Politecnica de Catalunya, ES

Expressing flexibility in logic synthesis by Boolean relations
Anna Bernasconi, Università di Pisa, IT

1000 – 1015 Coffee Break

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1015 – 1115 Algorithmic foundations of logic synthesis – Part 2

Craig interpolation in logic synthesis applications
Jie-Hong Jiang, National Taiwan University, TW

SAT in logic synthesis
Mathias Soeken, Integrated System Laboratory – EPFL, CH

1115 – 1215 Synthesis for emerging technologies

XOR gates in emerging technologies
Valentina Ciriani, Università degli Studi di Milano, IT

Majority Logic Synthesis
Luca Amaru, Synopsys, US

1215 – 1315 Lunch Break

1315 – 1415 Approximate synthesis

Approximate logic synthesis for area and delay optimization
Weikang Qian, Shanghai Jiao Tong University, CN

Systematic approaches to approximate logic synthesis
Sherief Reda, Brown University, US

1415 – 1515 High-level synthesis

High-level synthesis: status and future trends
Andres Takach, Calypto Design Systems, US

How high-level synthesis enables design for reusability of hardware accelerators
Luca Carloni, Columbia University, US

1515 – 1530 Coffee Break

1530 – 1630 Logic synthesis and machine learning

Automated synthesis of distributed/parallel computing through templates and inductive reasoning
Masahiro Fujita, University of Tokyo, JP

On the minimization of variables to represent sparse multi-valued input decision diagrams
Tsutomu Sasao, Meiji University, JP

1630 – 1730 Logic synthesis and biological models

Synthetic biology: application of logic synthesis to biological models
Gabriella Trucco, Università degli Studi di Milano, IT

Stochastic logic applied to DNA computing
Marc Riedel, University of Minnesota, US

W10 Workshop on Open-Source Design Automation for FPGAs - OSDA

Room 4 0845 – 1730

Organisers:
Eddie Hung, University of British Columbia, CA
Christian Krieg, Vienna University of Technology, AT
Clifford Wolf, Symbiotic EDA, AT

Programme Committee Members:
Andrea Borga, oliscience, NL
Xin Fang, Northeastern University, US
Shane Fleming, Imperial College London, GB
Hipolito Guzman-Miranda, University of Sevilla, ES
Steve Hoover, Redwood EDA, US
Dirk Koch, University of Manchester, GB
Mieszko Lis, University of British Columbia, CA
Brent Nelson, Brigham Young University, US
Steffen Reith, RheinMain University of Applied Sciences, DE
Davide Rossi, University of Bologna, IT

website: osda.gitlab.io

FPGAs are increasingly finding themselves in huge data-centers as well as in the hands of hobbyists. However the wide availability of these high and low cost devices contrasts with the narrow ways in which one can access them – through proprietary closed-source tools and IP – which can hamper the realisation and deployment of novel FPGA-based applications and EDA innovations. Open-source is a proven and prevalent success when it comes to CPU and GPU silicon, and there are already efforts to drive reconfigurable silicon towards the same trend.

This one-day workshop aims to bring together industrial, academic, and hobbyist actors to explore, disseminate, and network over ongoing efforts for open design automation, with a view to enabling unfettered research and development, improving EDA quality, and lowering the barriers and risks to entry for industry. These aims are particularly poignant due to the recent efforts across the European Union (and beyond) that mandate "open access" for publicly funded research to both published manuscripts as well as any code necessary for reproducing its conclusions.

TOPICS OF INTEREST AT OSDA INCLUDE, BUT ARE NOT LIMITED TO:

- Open-source FPGA tools – the latest developments, breakthroughs, challenges and surveys on the toolflows required to target real silicon parts: synthesis, simulation, place and route, etc.
- Open-source IP for FPGAs – contributions that enrich the IP ecosystem and reduce the need to "re-invent the wheel", e.g. PCIe and DDR controllers, debug infrastructure, etc.
- Design methodologies provided as open-source – such as alternative hardware description languages (e.g. derived from Python, Scala), domain specific languages (DSL), high level synthesis (HLS), asynchronous methods, and others.
- Directions on where the open-source FPGA movement should go, current weaknesses in the toolchain, and/or perspectives from industry on how open-source can affect aspects of safety, security, verification, IP protection, time-to-market, datacenter/cloud infrastructure, etc.
- Discussions and case studies on how to license, acquire funding, and commercialise technologies surrounding open-source hardware, which may be different to open software.

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0845 – 0900 **Welcome**

0900 – 1000 **Keynote: PULP – An Open-Source RISC-V Based Multi-Core Platform for In-Sensor Analytics**
Davide Rossi, Università di Bologna, IT

The "internet of everything" envisions trillions of connected objects loaded with high- bandwidth sensors requiring massive amounts of local signal processing, fusion, pattern extraction and classification. While silicon access cost is naturally decreasing due to the twilight of the Moore's law, the access to hardware IPs still represents a huge barrier for innovative start-ups and companies approaching the market of IoT. In this context, the recent growth of high-quality open source hardware IPs represents a promising way to surpass this barrier, paving the way for a number of exciting applications of open-source electronics. In this talk, I will describe the evolution of the open-source Parallel-Ultra-Low-Power (PULP) platform as well as opportunities and challenges for next generation open source computing systems.

Speaker biography: Davide Rossi, received the PhD from the University of Bologna, Italy, in 2012. He has been a post doc researcher in the Department of Electrical, Electronic and Information Engineering "Guglielmo Marconi" at the University of Bologna since 2015, where he currently holds an assistant professor position. His research interests focus on energy efficient digital architectures in the domain of heterogeneous and reconfigurable multi and many-core systems on a chip. This includes architectures, design implementation strategies, and runtime support to address performance, energy efficiency, and reliability issues of both high end embedded platforms and ultra-low-power computing platforms targeting the IoT domain. In these fields, he has published more than 80 paper in international peer- reviewed conferences and journals.

1000 – 1030 Coffee Break & Demos

nextpnr – a portable FPGA place and route tool
David Shah and Eddie Hung, SymbioticEDA, AT

OpenFPGA: a Complete Open Source Framework for FPGA Prototyping
Baudouin Chauviere, Aurélien Alacchi, Edouard Giacomin, Xifan Tang and Pierre-Emmanuel Gaillardon, University of Utah, US

1030 – 1130 **Session 1: Full Papers**

LiteX: an open-source SoC builder and library based on Migen Python DSL
Florent Kermarrec, Sébastien Bourdeauducq, Jean-Christophe Le Lann and Hannah Badier, Enjoy-Digital, FR

On Hardware Verification In An Open Source Context
Ben Marshall, University of Bristol, UK

PyGears: A Functional Approach to Hardware Design
Bogdan Vukobratović, Andrea Erdeljan and Damjan Rakanović, University of Novi Sad, RS

1130 – 1200 **LegUp High-Level Synthesis and its Commercialization**
Jason Anderson, University of Toronto, CA

High-level synthesis (HLS) is the automated synthesis of a hardware cir-

cuit from a software program first proposed in the 1980s, and spending decades on the sidelines of mainstream RTL digital design, there has been tremendous buzz around HLS technology in recent years. HLS is on the upswing as a design methodology for field-programmable gate arrays (FPGAs) to improve designer productivity and ultimately, to make FPGA technology accessible to software engineers having limited hardware expertise. The hope is that down the road, software developers can use HLS to realize FPGA-based accelerators customized to applications that work in tandem with standard processors to raise computational throughput and energy efficiency. In this talk, I will overview the trends behind the recent drive towards FPGA HLS and why the need for, and use of, HLS will only become more pronounced in the coming years. The talk will highlight current HLS research directions and expose some of the challenges for HLS that may hinder its update in the digital design community. I will describe work underway in the LegUp HLS project at the University of Toronto -- a publicly available HLS research tool that has been downloaded by over 5000 groups from around the world. LegUp HLS technology is being commercialized in a start-up company, LegUp Computing Inc. (https://www.legupcomputing.com/), which was founded in 2015 and received seed funding from Intel Capital in 2018. A key value proposition of LegUp HLS is FPGA-vendor agnosticism – synthesized circuits can be targeted to any FPGA.

Speaker Biography: Jason Anderson (http://janders.eecg.toronto.edu/) is Professor and Associate Chair, Research, with the Dept. of Electrical and Computer Engineering, University of Toronto, and holds the Jeffrey Skoll Endowed Chair. He joined the FPGA Implementation Tools Group, Xilinx, Inc., San Jose, CA, USA, in 1997, where he was involved in placement, routing, and synthesis. He became a Principal Engineer at Xilinx in 2007 and joined the university in 2008. His research interests are all aspects of tools, architectures, and circuits for FPGAs. He has co-authored over 90 peer-reviewed research publications, 4 book chapters, holds 29 U.S. patents, and was Program Co-Chair for FPL 2016, Program Chair for ACM FPGA 2017, and is General Chair for ACM FPGA 2018. He is Co-Founder and Chief Scientific Advisor of LegUp Computing Inc.

1200 – 1245 Lunch Break

1245 – 1330 Panel discussion: How does one commercialise/ undertake research on open-source EDA/IP?

The Panelists will be discussing whether it is possible to build a (stable!) business or research group around open-source – when the things that you are building is ostensibly given away for free. Topics explored will be panelist's experiences with doing this, their opinions on the various open-source licenses (copyleft versus permissive) in the context of hardware, their views on whether open and closed-source can co-exist, and the momentum within the EU to mandate "open access" research.

Panelists:

Andrea Borga, oliscience, NL
Ulrich Drepper, Red Hat, DE
Hipolito Guzman, University of Sevilla, ES
Clifford Wolf, Symbiotic EDA, AT

1330 – 1400 VHDL Reuse: from Vendor Independence to Open Source

Daniel van der Schuur, ASTRON, NL

ASTRONs mission is to make discoveries in radio astronomy happen. The high performance streaming data systems we build to do that naturally have FPGAs at their hearts. To balance project requirements, cost and availability of FPGA devices, ASTRON uses an approach that is both vendor and application independent. With generic, universal FPGA platforms (UniBoard, UniBoard2, Perentie), new science applications can take advantage of already available hardware. By also having a vendor independent VHDL library and tool flow, new FPGA hardware can also

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be adopted/developed with minimal firmware rework needed. This talk is about the advantages of vendor independence and how we chose to implement this, covering VHDL source code, vendor IP, library structures and simulation and synthesis tools. Another important aspect is the automated regression testing of the firmware library as it is updated on a daily basis. All this is made possible and structured by ASTRONs scripted tool flow, which is to be released as open source on OpenCores.org. Finally, this talk will cover how and why ASTRON is going to release its firmware library on OpenCores, and the technical challanges in doing so.

Speaker biography: Daniel van der Schuur is a digital designer at the Netherlands Institute for Radio Astronomy (ASTRON). As ASTRON designs, builds and operates complex high performance hybrid (FPGA, GPU, CPU, fiber networks) systems to make new discoveries, Daniel is passionate about reducing the time to science - from streaming system design to VHDL implementation.

1400 – 1430 **Session 2 – Lightning Talks**

Enabling FPGA Domain-specific Compilers Through Open Source
Alireza Kaviani and Chris Lavin, Xilinx Research Labs, US

Minitracer: A minimalist requirements tracer for HDL designs
Carlos López-Melendo and Hipólito Guzmán-Miranda, University of Seville, ES

OpenFPGA: a Complete Open Source Framework for FPGA Prototyping
Baudouin Chauviere, Aurélien Alacchi and Edouard Giacomin, Xifan Tang and Pierre-Emmanuel Gaillardon, University of Utah, US

Draft of CERN OHL (Open Hardware Licence) v2: We need your feedback
Tristan Gingold, CERN, CH

GHDL: Present and Future
Tristan Gingold, CERN, CH

1430 – 1500 Coffee Break & Posters

1500 – 1545 **UVVM – The fastest growing FPGA verification methodology world-wide!**
Espen Tallaksen, Bitvis, NO

On average half the development time for an FPGA is spent on verification. It is possible to significantly reduce this time, and major reductions can be accomplished with only minor adjustments and no extra cost. For an FPGA design we all know that the architecture – all the way from the top to the micro architecture – is critical for both the FPGA quality and the development time. It should really be obvious that this also applies to the testbench. UVVM (the open source Universal VHDL Verification Methodology) was developed to solve this and will reduce the verification time significantly while at the same time improving the product quality. UVVM provides a very simple and powerful architecture that allow designers to build their own test harness much faster than ever before - using a mix of their own and open source verification components. UVVM also provides an architecture, methodology and library to allow VHDL verification components to be made extremely efficiently. And maybe the most important feature – UVVM allows the best possible testbench and test case overview using high level commands for both DUT interface control and synchronization. The great overview, maintainability, extensibility, modifiability and reuse has resulted in an extraordinary fast spread of this methodology – and according to the

2018 Wilson Research report UVVM was the by far fastest growing FPGA verification methodology over the last two years. UVVM is the new standardised VHDL testbench architecture, recommended by Doulos and backed by ESA (the European Space Agency) through a contract for further extension of the UVVM functionality. This presentation will show you how simple this is to understand, build and control. It will also show the latest features from the ESA project and further planned extensions.

Speaker Biography: Espen Tallaksen is the managing director and founder of Bitvis, an independent design centre for embedded software and FPGA. He graduated from the University of Glasgow (Scotland) in 1987 and has 30 years' experience with FPGA and ASIC development from Philips Semiconductors in Switzerland and various companies in Norway, including his earlier founded company Digitas. During twenty years Espen has had a special interest for methodology cultivation and pragmatic efficiency and quality improvement. One result of this interest is the UVVM verification platform that is currently being used by a huge number of companies world-wide. He has given many presentations and keynotes on various technical aspects of FPGA development.

1545 – 1645 **Session 3 – Full papers**

PRGA: An Open-source Framework for Building and Using Custom FPGAs
Ang Li and David Wentzlaff, Princeton University, US

An Open-source Framework for Xilinx FPGA Reliability Evaluation
Aitzan Sari, Vasileios Vlagkoulis and Mihalis Psarakis, University of Piraes, GR

Python Wraps Yosys for Rapid Open-Source EDA Application Development
Benedikt Tutzer, Christian Krieg, Clifford Wolf and Axel Jantsch, TU Wien, AT

1645 – 1715 **FuseSoC – Cores never been so much fun**
Olof Kindgren, Qamcom Research & Technology, SE

In many ways, HDL developers have been many years behind their counterparts in the software world. One such area is core management. Where the software developers simply specify which libraries they depend on, HDL developers rely on copying around source code. Where software developers can select their build tool with a flick of a switch, HDL developers use tool-specific project files powered by custom makefiles. FuseSoC rectifies this by bringing a modern package manager and a uniform build system to HDL developers, making it easy to reuse existing code, change tools and move projects between FPGAs from different vendors. Having been around for seven years there are now hundreds of FuseSoC-compatible cores and 14 different simulation, synthesis and lint tools supported. This presentation will give an overview of where FuseSoC can help spending less time on the cores, and more time on the core business

Speaker biography: Olof Kindgren is a senior digital design engineer working for Qamcom Research & Technology. He became actively involved with free and open source silicon through the OpenRISC project in 2011 and has since then worked on many FOSSi projects with a special interest in tools and collaborations. Notable work include the FuseSoc IP core package manager; SERV, the award-winning RISC-V CPU and ipyxact, the IP-XACT Python library. In 2015, he also co-founded FOSSi Foundation, a vendor-independent organization with the mission to promote and assist Open Source Silicon in academia, the industry and for hobbyists alike.

1715 – 1730 Closing remarks

EXHIBITION THEATRE SESSIONS

Exhibition Theatre Chair: Jürgen Haase, edacentrum GmbH, DE

In addition to the conference programme, there will be nine Exhibition Workshops as part of the exhibition. These workshops will feature technical presentations on the state-of-the-art in our industry, tutorials, information on funding opportunities for research and as a special highlight career sessions for students. The theatre is located in the centre of the exhibition hall, close to the booths and the rooms of the technical conference.

The Exhibition Theatre sessions are open to conference delegates as well as to exhibition visitors.

2.8 How Electronic Systems can benefit from Machine Learning and from ESD Alliance

Tuesday 1130 – 1300 → See Page 46

In this session the Electronic System Design Alliance will present their newest initatives and results. Mentor, a Siemens Business will discuss approaches for application of Machine Learning for designing and producing microelectronics products. IngeniArs will analyze scenarios for realizing smart edge devices by using accelerators for executing Machine Learning and Deep Learning algorithms.

3.8 DFG Collaborative Funding Instruments

Tuesday 1430 – 1600 → See Page 52

Collaborative interdisciplinary research is considered of paramount importance today for the achievement of breakthroughs and jumps in technical innovation. In this session, program director Dr. Andreas Raabe introduces which types of collaborative funding instruments are offered by the Deutsche Forschungsgemeinschaft (DFG) in Germany, but also funding opportunities for international cooperations. After an introduction into different funding instruments for short, medium and long term collaborative research, concrete example initiatives in the scope of topics of DATE will be shortly introduced and summarized by representatives with a majority of these initiatives also exhibiting during the conference week.

3ps.8 Publisher's Session: How to Publish Your Research Work

Tuesday 1615 – 1645 → See Page 53

This publisher's session invites all attendees to discuss how and why to publish their research work with Springer Nature. Charles Glaser, Editorial Director for Springer, will present his advice for collaboration in research dissemination. He will be available in this session, as well as the entire exhibition, to discuss the publication of your next book.

4.8 Embedded Tutorial: Paving the Way for Very Large Scale Integration of Superconductive Electronics

Tuesday 1700 – 1830 → See Page 59

5.8

Special Session: The ARAMiS II Project - Efficient Use of Multicore for safety-critical Applications

Wednesday 0830 – 1000 → See Page 64

6.8

TETRAMAX: Smart funding for digitalization of Europe's Industry

Wednesday 1100 – 1230 → See Page 72

One of the most demanding challenge for Europe's Industry is to implement information technologies and to transfer knowledge from research to business. The session speakers will demonstrate in a pragmatic way and by use of concrete examples how technology transfer can be initiated and implemented in practice and to overcome the associated pitfalls and use the innovation opportunities.

Inspiring futures! Careers Session @ DATE

7.8

Part 1

Wednesday 1430 – 1600 → See Page 78

8.8

Part 2

Wednesday 1700 – 1830 → See Page 85

This session aims to bring together recruiters – mostly companies large and small, as well as universities and research centres – with potential jobseekers in the technology areas covered by DATE and HiPEAC. The programme will be tailored to the needs of the students and researchers.

9.8

Special Session: IBM's Qiskit Tool Chain: Developing for and Working with Real Quantum Computers

Thursday 0830 – 1000 → See Page 90

10.8

Europe digitization: Smart Anything Everywhere Initiative & FED4SAE, open calls and success stories

Thursday 1100 – 1230 → See Page 97

FED4SAE project aims at bringing innovative Cyber-Physical System technologies to businesses from any sectors and any companies. The presentation of awarded projects illustrate FED4SAE one-stop-shop to accelerate CPS developments combining i) Access to leading-edge CPS platforms, Advanced Technologies, and Testbeds from Industrials and R&D centers, ii) Technical coaching from domain experts, iii) Innovation Management support, iv) Up to €60k in financial support to innovative companies plus access to further VC funding, v) and Access to potential users and suppliers across value chains throughout Europe. This session will confront the view point of large industrial, RTOs and SMEs and their targeted objectives and impact.

EXHIBITION THEATRE SESSIONS

An Industry Approach to FPGA/ARM System Development and Verification

11.8 Part 1

Thursday 1400 – 1530 → See Page 102

12.8 Part 2

Thursday 1600 – 1730 → See Page 108

MATLAB and Simulink provide a rich environment for embedded-system development, with libraries of proven, specialized algorithms ready to use for specific applications. The environment enables a model-based design workflow for fast prototyping and implementation of the algorithms on heterogeneous embedded targets, such as MPSoC. A system-level design approach enables architectural exploration and partitioning, as well as coordination between SW and HW development workflows. Functional verification throughout the design process improves coverage and test-case generation while reducing the time and resources required.

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University Booth at DATE 2019

The University Booth is organised during DATE and will be located in the exhibition area. All demonstrations will take place from Tuesday, 26 March, to Thursday, 28 March 2019, during DATE. Universities and public research institutes have been invited to submit hardware or software demonstrators.

The University Booth programme is composed of 32 demonstrations from ten different countries, presenting software and hardware solutions. The programme is organised in nine sessions of 2 or 2.5 h duration and will cover the topics:

- Electronic Design Automation Prototypes
- Hardware Design and Test Prototypes
- Heterogeneous Computing: Embedded meets Hyperscale and HPC
- Model-Based Design of Intelligent Systems

The University Booth at DATE 2019 invites you to find out more about the latest trends in software and hardware from the international research community.

Most demonstrators will be shown more than once, giving visitors more flexibility to come to the booth and find out about the latest innovations.

We are sure that the demonstrators will give an attractive supplement to the DATE conference program and exhibition. We would like to thank all contributors to this programme.

More information is available online at https://www.date-conference.com/exhibition/u-booth. The University Booth programme is included in the conference booklet and available online at https://www.date-conference.com/exhibition/ub-programme. The following demonstrators will be presented at the University Booth.

A FAST PROTOTYPING FRAMEWORK FOR SERVICE-ORIENTED AUTOMOTIVE APPLICATIONS

Authors: Matthias Becker, Zhonghai Lu and De-Jiu Chen, KTH Royal Institute of Technology, SE

Timeslots:

UB02.3	Tuesday, 26 March 2019	1230 – 1500
UB03.3	Tuesday, 26 March 2019	1500 – 1730
UB07.3	Wednesday, 27 March 2019	1400 – 1600

Service-Oriented Architectures (SOA) provide a flexible platform for advanced automotive software applications. We present a research platform for fast prototyping of platform software and applications. The hardware is built around a RC car. Several sensors and actuators are connected over microcontrollers that can be accessed from higher-level ECUs over bus connections. User applications are executed on 4 Linux-based ECUs which communicate over a multi-hop Ethernet network. All communication of applications is realized over SOME-IP, an automotive middleware layer that is based on the SOA principle. The development framework generates code skeletons for user tasks, and all required management and configuration code of the underlying SOA framework, based on a user specified application model. It is then automatically transferred and compiled on the respective ECUs. We show the usability of the platform by a remote-operation scenario.

A MODULAR RECONFIGURABLE DIGITAL MICROFLUIDICS PLATFORM

Authors: Georgi Tanev[1], Winnie Svendsen[2] and Jan Madsen[3]
[1]Technical University of Denmark, DK; [2]DTU Bioengineering, DK
[3]DTU Compute, DK

Timeslots:

UB02.10	Tuesday, 26 March 2019	1230 – 1500
UB08.8	Wednesday, 27 March 2019	1600 – 1800
UB10.4	Thursday, 28 March 2019	1200 – 1430

Digital microfluidics is a lab-on-a-chip (LOC) technology that allows for manipulation of a small amount of liquids on a chip-scaled device patterned with individually addressable electrodes. Microliter sized droplets can be programmatically dispensed, moved, mixed, react, split and stored thus implementing sample preparation protocols. Combining digital microfluidics with miniaturized analytical methods allows biomedical lab assays to be implemented on a LOC device that provides full sample-to-answer functionality. The growing complexity and integration of the LOC devices impose the need of software tools and hardware instruments to design, simulate, program and operate the broad range of LOC instrumentation needs. To address this matter, we present a modular reconfigurable microfluidics instrumentation platform (shown in Figure 1) capable of evolving to match the instrumentation needs of a specific LOC. The prototype shown in Figure 2 serves the purpose to demonstrate the platform.

A RISC-V BASED VIRTUAL PROTOTYPE WITH AN INTEGRATED HARDWARE-IN-THE-LOOP RADAR

Authors: Peer Adelt, Denis Zeinel, Bastian Koppelmann, Wolfgang Mueller and Christoph Scheytt, Paderborn University, DE

Timeslot:

UB06.6	Wednesday, 27 March 2019	1200 – 1400

Our demonstration shows a small radar sensor in interactive communication with a RISC-V processor board and a RISC-V Virtual Prototype (VP) where the VP and the processor concurrently execute exactly the same target compiled software without a visible difference in reaction time. This demonstrates that widely available open source based virtual prototyping environments provide an adequate, stable, and efficient framework for the analysis of such embedded applications. The demonstration integrates our in-house developed 120GHz radar sensor via CAN bus with the SiFive RISC-V HiFive1 development board and our QEMU based VP. For the HiFive1 integration, we developed an Ardunio compliant board with an SPI-CAN adapter and a display. For the VP integration, we implemented the same components as QEMU QOM hardware models. Though the VP is executed in a linux based VirtualBox virtual machine on top of an additional host operating system, the impact of both is not visible in this setup.

UNIVERSITY BOOTH

ACSIM: A NOVEL, SIMULATOR FOR HETEROGENEOUS PARALLEL AND DISTRIBUTED SYSTEMS THAT IN-CORPORATE CUSTOM HARDWARE ACCELERATORS

Authors: Nikolaos Tampouratzis[1] and Ioannis Papaefstathiou[2]
[1]Technical University of Crete, GR; [2]Synelixis Solutions LTD, GR

Timeslots:

UB01.5	Tuesday, 26 March 2019	1030 – 1230
UB02.5	Tuesday, 26 March 2019	1230 – 1500

The growing use of hardware accelerators in both embedded (e.g. automotive) and high-end systems (e.g. Clouds) triggers an urgent demand for simulation frameworks that can simulate in an integrated manner all the components (i.e. CPUs, Memories, Networks, Hardware Accelerators) of a system-under-design (SuD). By utilizing such a simulator, software design can proceed in parallel with hardware development which results in the reduction of the so important time-to-market. The main problem, however, is that currently there is a shortage of such simulation frameworks; most simulators used for modelling the user applications (i.e. full-system CPU/Mem/Peripherals) lack any type of support for tailor-made hardware accelerators. ACSIM framework is the first known open-source, high-performance simulator that can handle holistically system-of-systems including processors, peripherals, accelerators and networks. The complete ACSIM framework together with its sophisticated GUI will be presented.

ADDRESSING MAN-IN-THE-MIDDLE THREAT IN EXTENSIVELY CONNECTED CARS AND NEXT-GENERATION AUTOMOTIVE NETWORKS

Authors: Luca Crocetti, Luca Baldanzi and Luca Fanucci, University of Pisa, IT

Timeslots:

UB03.10	Tuesday, 26 March 2019	1500 – 1730
UB07.6	Wednesday, 27 March 2019	1400 – 1600
UB08.6	Wednesday, 27 March 2019	1600 – 1800

Today's trend in the automotive industry is to integrate more and more interconnected electronics systems in order to offer functionalities and services orientated to the autonomous driving, also by adoption of wireless communication links such as Wi-Fi 802.11p. Thus a connected car results to act as a node of many and heterogeneous networks and thus being exposed to the typical threats of the IT field. The proposed demo aims to investigate the security vulnerabilities of a hypothetical real application scenario exploiting the wireless links and to target the related cybersecurity mechanisms required to counteract possible attacks. The demo consists of two FPGA boards that act as nodes of a 802.11p based network, one as the car and one as an infrastructure unit, and a laptop that acts as malicious entity and performs a Man-In-The-Middle attack. The emulated malicious node alters the communication between the two FPGA nodes and expose the car-like FPGA node to threats as car stealing.

APODOSIS: ADVANCED ORCHESTRATOR FOR SMART-BUILDINGS

Authors: Kostas Siozios[1] and Stylianos Siskos[2]
[1]Aristotle University of Thessaloniki, GR
[2]Department of Physics, Aristotle University of Thessaloniki, GR

Timeslots:

UB02.9	Tuesday, 26 March 2019	1230 – 1500
UB10.5	Thursday, 28 March 2019	1200 – 1430

This work presents a distributed system for supporting advanced orchestrator of a smart grid environment. By efficiently control energy production from renewable sources and the energy loads, it is feasible to minimize the energy cost. In contrast to similar approaches, the proposed decision-making is performed in a distributed manner, while it also exhibits limited computational complexity.

ASAM: AUTOMATIC SYNTHESIS OF ALGORITHMS ON MULTI CHIP/FPGA WITH COMMUNICATION CONSTRAINTS

Authors: Amir Masoud Gharehbaghi, Tomohiro Maruoka, Yukio Miyasaka, Akihiro Goda, Amir Masoud Gharehbaghi and Masahiro Fujita, The University of Tokyo, JP

Timeslots:

UB03.4	Tuesday, 26 March 2019	1500 – 1730
UB07.7	Wednesday, 27 March 2019	1400 – 1600
UB09.3	Thursday, 28 March 2019	1000 – 1200

Mapping of large systems/computations on multiple chips/multiple cores needs sophisticated compilation methods. In this demonstration, we present our compiler tools for multi-chip and multi-core systems that considers communication architecture and the related constraints for optimal mapping. Specifically, we demonstrate compilation methods for multi-chip connected with ring topology, and multi-core connected with mesh topology, assuming fine-grained reconfigurable cores, as well as generalization techniques for large problems size as convolutional neural networks. We will demonstrate our mappings methods starting from data-flow graphs (DFGs) and equations, specifically with applications to convolutional neural networks (CNNs) for convolution layers as well as fully connected layers.

UNIVERSITY BOOTH

CS: CRAZYSQUARE

Authors: Federica Caruso[1], Federica Caruso[1], Tania Di Mascio[1], Alessandro D'Errico[1], Marco Pennese[2], Luigi Pomante1, Claudia Rinaldi[1] and Marco Santic[1]
[1]University of L'Aquila, IT; [2]Ministry of Education, IT

Timeslots:

UB05.5	Wednesday, 27 March 2019	1000 – 1200
UB09.5	Thursday, 28 March 2019	1000 – 1200

CrazySquare (CS) is an adaptive learning system, developed as a serious game for music education, specifically indicated for young teenager approaching music for the first time. CS is based on recent educative directions which consist of using a more direct approach to sound instead of the musical notation alone. It has been inspired by a paper-based procedure that is currently used in an Italian middle school. CS represents a support for such teachers who prefer involving their students in a playful dimension of learning rhythmic notation and pitch, and, at the same time, teaching playing a musical instrument. To reach such goals in a cost-effective way, CS fully exploits all the recent advances in the EDA domain. In fact, it is based on a framework composed of mobile applications that will be integrated with augmented reality HW/SW tools to provide virtual/augmented musical instruments. The proposed demo will show the main features of the current CS framework implementation.

DESIGN SPACE EXPLORATION FRAMEWORKS FOR APPROXIMATE COMPUTING

Authors: Alberto Bosio[1], Olivier Sentieys[2] and Daniel Ménard[3]
[1]University of Lyon, FR; [2]University of Rennes, INRIA/IRISA, FR
[3]INSA Rennes - IETR, FR

Timeslots:

UB01.7	Tuesday, 26 March 2019	1030 – 1230
UB06.9	Wednesday, 27 March 2019	1200 – 1400
UB09.10	Thursday, 28 March 2019	1000 – 1200

Approximate Computing (AxC) investigates how to design energy efficient, faster, and less complex computing systems. Instead of performing exact computation and, consequently, requiring a high amount of resources, AxC aims to selectively relax the specifications, trading accuracy off for efficiency. The goal of this demonstrator, is to present a Design Space Exploration framework able to automatically explore the impact of different approximate operators on a given application accordingly to the required level of accuracy and the available HW architecture. The first demonstration relates to the word-length optimization of variables in a software or hardware system to explore cost (e.g., energy) and quality trade-off solution. The tool is scalable and targets both customized fixed-point and floating-point arithmetic. The second demonstration is about the use of other approximate techniques. The proposed demonstrator is linked with the DATE19 Monday Tutorial M03.

EDP PLAYER: A DESIGN ASSISTANT FOR PROCEDURAL DESIGN AUTOMATION OF ANALOG INTEGRATED CIRCUITS

Authors: Matthias Schweikardt[1], Husni Habal[2] and Jürgen Scheible[1]
[1]Hochschule Reutlingen, DE; [2]Infineon Technologies, DE

Timeslots:

UB06.2	Wednesday, 27 March 2019	1200 – 1400
UB07.2	Wednesday, 27 March 2019	1400 – 1600

In this demonstration, we address procedural circuit design automation of analog integrated circuits. Procedural automation means, that the knowledge-based strategy of human experts is captured in an executable script, which makes it reusable. We call this principle EDP (Expert Design Plan). An EDP can cover different performance parameters, technologies and topologies. We present the EDP Player, which enables the creation and execution of plain EDPs. The tool provides a preliminary version of an instruction set tailored to the typical manual analog circuit design flow, called EDPL (EDP-Language). The tool is fully integrated within Cadence Virtuoso based on Cadence SKILL. The tool has been utilized for three different examples: the automated design of a miller operational amplifier, a bandgap, and the automated creation of variants of a smart power IC. The usage of EDPs leads to a strong reduction of design time without loss of both design quality and reliability.

EQ-PYD-NET: ENERGY-EFFICIENT MONOCULAR DEPTH ESTIMATION ON ARM-BASED EMBEDDED PLATFORMS

Authors: Andrea Calimera[1], Valentino Peluso[1], Antonio Cipolletta[1], Matteo Poggi[2], Fabio Tosi[2] and Stefano Mattoccia[2]
[1]Politecnico di Torino, IT; [2]Università di Bologna, IT

Timeslots:

UB02.4	Tuesday, 26 March 2019	1230 – 1500
UB07.4	Wednesday, 27 March 2019	1400 – 1600
UB08.4	Wednesday, 27 March 2019	1600 – 1800

The demonstration intends to show the implementation of energy-efficient monocular depth estimation using a low-cost CPU for low-power embedded systems. Through the demo we're going to present the PyD-Net depth estimation network, which consists of a lightweight CNN designed for CPUs and able to approach state-of-the-art accuracy. Then we introduce an accuracy-driven complexity reduction strategy based on a hardware-friendly fixed-point quantization. The objective is (i) to demonstrate the portability of the Quantized PyD-Net model into a general-purpose RISC architecture of the ARM Cortex family, (ii) quantify the accuracy-energy tradeoff of unsupervised monocular estimation to establish its use in the embedded domain. During the live demonstration the QPyD-Net will be made running on a Raspberry PI board powered by a Broadcom BCM2837 chip-set.

HEPSYCODE-MC: ELECTRONIC SYSTEM-LEVEL METHODOLOGY FOR HW/SW CO-DESIGN OF MIXED-CRITICALITY EMBEDDED SYSTEMS

Authors: Luigi Pomante[1], Vittoriano Muttillo[1], Marco Santic[1] and Emilio Incerto[2]
[1]Università degli Studi dell'Aquila - DEWS, IT; [2]IMT Lucca, IT

Timeslots:

UB05.4	Wednesday, 27 March 2019	1000 – 1200
UB09.4	Thursday, 28 March 2019	1000 – 1200

Heterogeneous parallel architectures have been recently exploited for a wide range of embedded application domains. Embedded systems based on such kind of architectures can include different processor cores, memories, dedicated ICs and a set of connections among them. Moreover, especially in automotive and aerospace application domains, they are even more subjected to mixed-criticality constraints. So, this demo addresses the problem of the ESL HW/SW co-design of mixed-criticality embedded systems that exploit hypervisor (HPV) technologies. In particular, it shows an enhanced CSP/SystemC-based design space exploration step, in the context of an existing HW/SW co-design flow that, given the system specification is able to (semi)automatically propose to the designer: - a custom heterogeneous parallel HPV-based architecture; - an HW/SW partitioning of the application; - a mapping of the partitioned entities onto the proposed architecture.

HIPACC: SYNTHESIZING HIGH-PERFORMANCE IMAGE PROCESSING APPLICATIONS WITH HIPACC

Authors: M. Akif Oezkan[1],Oliver Reiche[1], Bo Qiao[1], Richard Membarth[2], Jürgen Teich[1] and Frank Hannig[1]
[1]Friedrich-Alexander-Universität Erlangen–Nürnberg (FAU), DE
[2]German Research Center for Artificial Intelligence (DFKI), DE

Timeslot:

UB01.4	Tuesday, 26 March 2019	1030 – 1230

Programming heterogeneous platforms to achieve high performance is laborious since writing efficient code requires tuning at a low level with architecture-specific optimizations and is based on drastically differing programming models. Performance portability across different platforms can be achieved by decoupling the algorithm description from the target implementation. We present Hipacc (http://hipacc-lang.org), a framework consisting of an open-source image processing DSL and a compiler to target CPUs, GPUs, and FPGAs from the same program. We demonstrate Hipacc's productivity by considering real-world computer vision applications, e.g. optical flow, and generating target code (C++, OpenCL, C-based HLS) for three platforms (CPU and GPU in a laptop and an FPGA board). Finally, we showcase real-time processing of images acquired by a USB camera on these platforms.

LABSMILING: A SAAS FRAMEWORK, COMPOSED OF A NUMBER OF REMOTELY ACCESSIBLE TESTBEDS AND RELATED SW TOOLS, FOR ANALYSIS, DESIGN AND MANAGEMENT OF LOW DATA-RATE WIRELESS PERSONAL AREA NETWORKS BASED ON IEEE 802.15.4

Authors: Carlo Centofanti, Luigi Pomante, Marco Santic and Walter Tiberti, University of L'Aquila, IT

Timeslots:

UB05.8	Wednesday, 27 March 2019	1000 – 1200
UB07.9	Wednesday, 27 March 2019	1400 – 1600
UB09.6	Thursday, 28 March 2019	1000 – 1200

Low data-rate wireless personal area networks (LR-WPANs) are constantly increasing their presence in the fields of IoT, wearable, home automation, health monitoring. The development, deployment and testing of SW based on IEEE 802.15.4 standard (and derivations, e.g. 15.4e), require the exploitation of a testbed as the network grows in complexity and heterogeneity. This demo shows LabSmiling: a SaaS framework which connects testbeds deployed in a real-world-environment and the related SW tools that make available a meaningful (but still scalable) number of physical devices (sensor nodes) to developers. It provides a comfortable out-of-the-box service designed to fulfill developer needs giving them full control on single motes (program, reset, physical power on/off, up/down links, commands/messages/packets in/from the network). Advanced services are: full-customizable testing scenario, validation/testing protocol compliances/extensions, run low level packet sniffers with QoS metrics.

LOGIC MINIMIZER: LOGIC MINIMIZERS FOR PARTIALLY DEFINED FUNCTIONS

Authors: Tsutomu Sasao, Kyu Matsuura, Kazuyuki Kai and Yukihiro Iguchi, Meiji University, JP

Timeslots:

UB05.2	Wednesday, 27 March 2019	1000 – 1200
UB08.2	Wednesday, 27 March 2019	1600 – 1800

This demonstration shows a minimization system for partially defined functions. The minimizer reduces the number of the input variables to represent the function using linear transformations. Applications include implementations of random functions; code converter; IP address table; English word list; and URL list. Outline of Demonstration In the demonstration, a PC and a poster are used to show:

- Introduction of partially defined functions.
- A method to reduce variables by linear decompositions.
- Implementation of code converters.
- Implementation of IP address tables.
- Implementation of English dictionaries.
- Implementation of random functions.
- Implementation of URL lists.

UNIVERSITY BOOTH

MASCARA: A MACHINE LEARNING AUTOMATIC SPEECH RECOGNITION PLATFORM FOR USERS WITH DYSARTHRIA

Authors: Davide Mulfari, Gabriele Meoni, Marco Marini and Luca Fanucci, University of Pisa, IT

Timeslots:

UB02.6	Tuesday, 26 March 2019	1230 – 1500
UB03.6	Tuesday, 26 March 2019	1500 – 1730
UB06.8	Wednesday, 27 March 2019	1200 – 1400

We exploit machine learning technology to build Automatic Speech Recognition (ASR) solutions for people with dysarthria, a speech disorder characterized by low intelligibility of users' speaking and related to many motor disabilities. Within the field of ASR, nowadays popular voice assistant solutions (e.g.,Apple Siri) perform poorly on dysarthric speech processing, so users with disabilities cannot benefit from such technologies in many scenarios, like smart home. To address these issues, a custom ASR has been prototyped using a speaker dependent approach: it recognizes predefined keywords from disabled Italian persons who have already shared their voices. The demo shows our edge computing platform for speech recognition and its usage within the field of human computer interaction. We also present a mobile app allowing users to record and to share voice while they say selected keywords. With these data, we enrich our speech model in order to serve many application scenarios.

MDC: MULTI-DATAFLOW COMPOSER TOOL: DATAFLOW TO HARDWARE COMPOSITION AND OPTIMIZATION OF RECONFIGURABLE ACCELERATORS

Authors: Francesca Palumbo[1], Carlo Sau[2], Tiziana Fanni[2], Claudio Rubattu[1] and Luigi Raffo[2]
[1]University of Sassari, IT; [2]University of Cagliari, IT

Timeslots:

UB01.6	Tuesday, 26 March 2019	1030 – 1230
UB05.6	Wednesday, 27 March 2019	1000 – 1200

UNICA-Eolab and UNISS-IDEA booth is demonstrating the capabilities of the Multi-Dataflow Component (MDC) tool: a model-based toolset for design and development of virtual coarse-grain reconfigurable (CGR) circuits. MDC provides multi-function substrate composition, optimization and integration in real environments.

1 Baseline Core: automatic composition of CGR substrates. Inputs kernels are provided as dataflow networks, and target agnostic RTL description is derived. [FPGA(1)/ASIC(2)]

2 Profiler: automated design space exploration to determine the optimal multi-functional CGR substrate given a set of constraints. [2]

3 Power Manager: power consumption minimization. Model level identification of the logic regions to determine optimal power/clock domains and apply saving strategies. [1/2]

4 Prototyper: automatic generation of Xilinx-compliant IPs and APIs. [1] MDC is part of the H2020 CERBERO toolchain. Material: http://sites.unica.it/rpct/ and IDEA Lab Channel www.goo.gl/7fXme3.

MECO: AN AUTONOMIC MANAGER FOR EDGE-COMPUTING PLATFORMS

Authors: Gabriella D'Andrea, Tania Di Mascio, Luigi Pomante and Giacomo Valente, University of L'Aquila, IT

Timeslots:

UB05.9	Wednesday, 27 March 2019	1000 – 1200
UB07.8	Wednesday, 27 March 2019	1400 – 1600
UB09.9	Thursday, 28 March 2019	1000 – 1200

In the Cyber-Physical-Systems word, the need for hardware platforms able to satisfy increasing requirements in computing performance, while keeping the adaptability imposed by the interactions with the physical world is leading on the use FPGAs, due to their inherent run-time reconfigurability. So, this demo presents an implementation of a self-adaptive loop for edge- computing devices targeting FPGAs. An adaptive run-time manager, together with a smart monitoring system, evaluates the quality of service and determines whether is convenient to perform a dynamic partial reconfiguration. The whole development flow, that exploits a library of elements to compose the monitoring system and then selects the appropriate manager, will be shown by means of a reference use case implemented on a Zynq Ultrascale+ SoC. Finally, a comparison among different functionalities will be illustrated as well.

MICROPLAN: MICRO-SYSTEM DESIGN AND PRODUCTION PLANNING TOOL

Authors: Horst Tilman, Robert Fischbach and Jens Lienig, Technische Universität Dresden, DE

Timeslots:

UB01.3	Tuesday, 26 March 2019	1030 – 1230
UB03.1	Tuesday, 26 March 2019	1500 – 1730
UB06.3	Wednesday, 27 March 2019	1200 – 1400
UB10.3	Thursday, 28 March 2019	1200 – 1430

We present a tool that enables to layout and plan the production of heterogeneous micro-systems. The tool consists of a simple layout editor, a visualization of the wafer utilization and eventually a calculation of the production cost for a given order quantity. Being superior with regard to performance, heterogeneous systems are often rendered unviable due to high production costs. However, using our tool allows users to design heterogeneous systems with an emphasis on low production costs. The tool is developed within the MICROPRINCE project and in close cooperation with X-Fab. The tool doesn't require installation and can be used by any visitor on their smartphone or computer.

UNIVERSITY BOOTH

MROS AND ZYTLEBOT: DESIGN PLATFORMS FOR EMBEDDED ROBOT SYSTEMS

Authors: Hideki Takase[1], Yasuhiro Nitta[1] and So Tamura[2]
[1]Kyoto University, JP; [2]Kyoto Universiy, JP

Timeslots:

UB06.4	Wednesday, 27 March 2019	1200 – 1400
UB08.9	Wednesday, 27 March 2019	1600 – 1800

We are researching design platforms for robot systems based on ROS (Robot Operating System). In the booth, we will present the current status of two research activities. The first project is mROS, a lightweight runtime environment of ROS nodes. mROS offers a ROS-compatible communication library to be operated on the embedded mid-range processor which cannot be operated with Linux. mROS contributes to utilizing low power embedded devices into the ROS system. We will show the case study of mROS on the distributed camera system. The second is ZytleBot, an autonomous driving robot as an FPGA integrated platform utilizing the Xilinx programmable SoC. In ZytleBot, the FPGA performs preprocessing of the road surface image acquired from the camera and calculation of HOG feature calculation for signal detection. We achieved about 5 times faster performance by utilizing the FPGA. We will demonstrate the real-time signal detection task on the ZytleBot that won FPT'18 FPGA design competition.

POETS: PARTIALLY ORDERED EVENT DRIVEN SYSTEMS

Authors: Jonathan Beaumont[1], Ghaith Tarawneh[2], Shane Fleming[1], Matthew Naylor[3], Andrew Brown[4], Andrey Mokhov[2], Simon Moore[3] and David Thomas[1]
[1]Imperial College London, GB; [2]Newcastle University, GB
[3]University of Cambridge, GB; [4]University of Southampton, GB

Timeslot:

UB08.10	Wednesday, 27 March 2019	1600 – 1800

POETS technology is based on the idea of an extremely large number of small cores embedded in a fast, hardware, parallel communications infrastructure. The application network communication is effected by small, fixed size hardware data packets (a few bytes). This project is a collaborative effort between four UK universities, researching and developing a software methodology and the hardware to realise the potential of this architecture. A POETS booth will consist of live demonstrations of applications benefiting from this architecture, such as Graph Traversal algorithms, Heat Dissipation Equations and Dissipative Particle Dynamics. Applications run on hardware based in Cambridge, and laptops display visualisations of these applications, produced from data output received via wi-fi, allowing visitors to view these applications in real-time. Some of the demonstrations are interactive; a visitor can affect the application and see how this changes the outcome in real-time.

PREESM: GENERATING ENERGY-OPTIMIZED ADAPTIVE SOFTWARE ON A HETEROGENEOUS PLATFORM WITH PREESM

Authors: Maxime Pelcat[1], Karol Desnos[1], Daniel Menard[1], Florian Arrestier[1], Alexandre Honorat[1], Claudio Rubattu[2], Antoine Morvan[1], Julien Heulot[1] and Jean-François Nezan[1]
[1]INSA Rennes/IETR, FR; [2]UNISS, INSA Rennes/IETR, FR

Timeslots:

UB03.5	Tuesday, 26 March 2019	1500 – 1730
UB06.5	Wednesday, 27 March 2019	1200 – 1400
UB08.5	Wednesday, 27 March 2019	1600 – 1800

This Booth demonstrates how PREESM and SPIDER tools generate energy-optimized sensor-based adaptive software on a heterogeneous platform. PREESM is a rapid system prototyping tool provided with a runtime manager named SPIDER. PREESM simulates stream processing applications and generates code for multi/many-cores. Processing can either be statically mapped or adaptively managed by SPIDER. Steps when using PREESM are: 1- Model your Application: PREESM provides you with a dataflow language, designed to express parallelism. 2- Model your Architecture: PREESM simulates and generates code for a wide range of systems (e.g., ARM, DSP, FPGA). 3- Prototype and Run your Design: PREESM takes mapping decisions and provides early design space information such as scheduling, memory use, and core loads. PREESM and SPIDER are available on GitHub, and supported by tutorials and a reactive community. PREESM and SPIDER are part of the H2020 CERBERO toolchain. http://preesm.org

REQV: A TOOL FOR REQUIREMENTS FORMAL CONSISTENCY CHECKING

Authors: Luca Pulina[1], Massimo Narizzano[2], Armando Tacchella[2] and Simone Vuotto[1]
[1]University of Sassari, IT; [2]University of Genoa, IT

Timeslots:

UB03.8	Tuesday, 26 March 2019	1500 – 1730
UB07.10	Wednesday, 27 March 2019	1400 – 1600
UB09.8	Thursday, 28 March 2019	1000 – 1200
UB10.8	Thursday, 28 March 2019	1200 – 1430

In the demo we will present ReqV, a tool for requirements formal consistency checking developed in the context of the H2020 EU project CERBERO (http://www.cerbero-h2020.eu/tools-and-tutorials/). ReqV takes as input a set of requirements expressed in natural language, so it does not require any background knowledge of formal methods and logical languages. A video tutorial is currently available at http://www.cluster-prossimo.it/docs/ReqV_video.mp4. The basic technologies used in ReqV are an extension of Property Specification Patterns to constrained numerical signals – which enables to write useful requirements specifications in the context of Cyber-Physical Systems – and Linear Temporal Logic satisfiability solvers for the formal consistency checking part. In the case of inconsistency of the set of input requirements, ReqV can also extract the minimal set of conflicting requirements, in order to help the designer to correct a wrong specification.

RESCUE: EDA TOOLSET FOR INTERDEPENDENT ASPECTS OF RELIABILITY, SECURITY AND QUALITY IN NANOELECTRONIC SYSTEMS DESIGN

Authors: Cemil Cem Gürsoy[1], Guilherme Cardoso Medeiros[2], Junchao Chen[3], Nevin George[4], Josie Esteban Rodriguez Condia[5], Thomas Lange[6], Aleksa Damljanovic[5], Raphael Segabinazzi Ferreira[4], Aneesh Balakrishnan[6], Xinhui Anna Lai[1], Shayesteh Masoumian[7], Dmytro Petryk[3], Troya Cagil Koylu[2], Felipe Augusto da Silva[8], Ahmet Cagri Bagbaba[8] and Maksim Jenihhin[1]
[1]Tallinn University of Technology, EE; [2]Delft University of Technology, NL; [3]IHP, DE; [4]BTU Cottbus-Senftenberg, DE; [5]Politecnico di Torino, IT; [6]IROC Technologies, FR; [7]Intrinsic ID B.V., NL
[8]Cadence Design Systems GmbH, DE

Timeslots:

UB01.8	Tuesday, 26 March 2019	1030 – 1230
UB02.8	Tuesday, 26 March 2019	1230 – 1500
UB07.1	Wednesday, 27 March 2019	1400 – 1600
UB08.1	Wednesday, 27 March 2019	1600 – 1800
UB09.2	Thursday, 28 March 2019	1000 – 1200
UB10.2	Thursday, 28 March 2019	1200 – 1430

The demonstrator will introduce an EDA toolset developed by a team of PhD students in the H2020-MSCA-ITN RESCUE project. The recent trends for the computing systems include machine intelligence in the era of IoT, complex safety-critical applications, extreme miniaturization of technologies and intensive interaction with the physical world. These trends set tough requirements on mutually dependent extra-functional design aspects. RESCUE is focused on the key challenges for reliability (functional safety, ageing, soft errors), security (tamper-resistance, PUF technology, intelligent security) and quality (novel fault models, functional test, FMEA/FMECA, verification/debug) and related EDA methodologies. The objective of the interdisciplinary cross-sectoral team from Tallinn UT, TU Delft, BTU Cottbus, POLITO, IHP, IROC, Intrinsic-ID, Cadence and Bosch is to develop in collaboration a holistic EDA toolset for modelling, assessment and enhancement of these extra-functional design aspects.

RISC-V VP: RISC-V BASED VIRTUAL PROTOTYPE: AN OPEN SOURCE PLATFORM FOR MODELING AND VERIFICATION

Authors: Vladimir Herdt[1], Daniel Große[2], Hoang M. Le1 and Rolf Drechsler[2]
[1]University of Bremen, DE; [2]University of Bremen, DFKI GmbH, DE

Timeslots:

UB01.9	Tuesday, 26 March 2019	1030 – 1230
UB05.10	Wednesday, 27 March 2019	1000 – 1200

RISC-V, being an open and free Instruction Set Architecture (ISA), is gaining huge popularity as processor ISA in Internet-of-Things (IoT) devices. We propose an open source RISC-V based Virtual Prototype (VP) demonstrator (available at http://www.systemc-verification.org/riscv-vp). Our VP is implemented in standard compliant SystemC using a generic bus system with TLM 2.0 communication. At the heart of our VP is a 32 bit RISC-V (RV32IMAC) Instruction Set Simulator (ISS) with support for compressed instructions. This enables our VP to emulate IoT devices that work with a small amount of memory and limited resources. Our VP can be used as platform for early SW development and verification, as well as other system-level use cases. We support the GCC toolchain, provide SW debug, coverage measurement capabilities and support FreeRTOS. Our VP is designed as configurable and extensible platform. For example we provide the configuration for the RISC-V HiFive1 board from SiFive.

SCCHARTS: THE KIELER SCCHARTS EDITOR - A MODULAR OPEN-SOURCE MODELING SUITE WITH AUTOMATIC DIAGRAM SYNTHESIS

Authors: Steven Smyth[1], Alexander Schulz-Rosengarten[1], Christian Motika[2] and Reinhard von Hanxleden[1]
[1]Kiel University, DE; [2]Lufthansa Technik, DE

Timeslots:

UB02.7	Tuesday, 26 March 2019	1230 – 1500
UB03.7	Tuesday, 26 March 2019	1500 – 1730
UB05.7	Wednesday, 27 March 2019	1000 – 1200
UB06.7	Wednesday, 27 March 2019	1200 – 1400

When using high-level DSLs, the model-based approach promises a more transparent and efficient development process, for example in the hardware domain. By leveraging the compilation workflow to a meta level, the tool developer and the modeler can benefit from an interactive development process. Combined with modern transient view technologies, working with model transformation systems becomes transparent and less time consuming. Modeling tools should guide the modeler to potential issues and provide means to understand details about the transformations. The KIELER SCCharts Editor is a modular, open-source modeling suite, using the synchronous language SCCharts as main demonstrator. The editor supports compilation, automatic syntheses of intermediate results, and deployment to different platforms, both software and hardware. The modular concept of the compiler framework allows for rapid application and prototype development. The concepts can be applied to other languages or domains.

SETA-RAY: A NEW IDE TOOL FOR PREDICTING, ANALYZING AND MITIGATING RADIATION-INDUCED SOFT ERRORS ON FPGAS

Authors: Luca Sterpone, Boyang Du and Sarah Azimi, Politecnico di Torino, IT

Timeslots:

UB01.10	Tuesday, 26 March 2019	1030 – 1230
UB03.9	Tuesday, 26 March 2019	1500 – 1730
UB08.7	Wednesday, 27 March 2019	1600 – 1800
UB09.7	Thursday, 28 March 2019	1000 – 1200

One of the main concern for FPGA adopted in mission critical application such as space and avionic fields is radiation-induced soft errors. Therefore, we propose an IDE including two software tools compatible with commercial EDA tools. RAD-RAY as the first and only developed tool capable to predict the source of the SET phenomena by taking in to account the features of the radiation environment such as the type, LET and interaction angle of the particles, the material and physical layout of the device exposed to the radiation. The predicted source SET pulse in provided to the SETA tool as the second developed tool integrated with the commercial FPGA design tool for evaluating the sensitivity of the industrial circuit implemented on Flash-based FPGA and mitigate the original netlist based on the performed analysis. This IDE is supported by ESA and Thales Alenia Space. It has been applied to the EUCLID space mission project that will be launched in 2021.

UNIVERSITY BOOTH

SWARM: SELF-ORGANIZED WIRING AND ARRANGEMENT OF RESPONSIVE MODULES

Authors: Daniel Marolt and Jürgen Scheible, Hochschule Reutlingen, DE

Timeslots:

UB05.3	Wednesday, 27 March 2019	1000 – 1200
UB08.3	Wednesday, 27 March 2019	1600 – 1800

This demonstration exemplifies a new automation methodology for layout design of analog integrated circuits: Self-organized Wiring and Arrangement of Responsive Modules (SWARM). Based on the idea of decentralization, it addresses the task with an innovative multi-agent system. Its basic principle, similar to the roundup of a sheep herd, is to let responsive layout modules (implemented as procedural generators) interact with each other in a user-defined layout zone. Each module is allowed to autonomously move, rotate and deform itself, while a supervising control organ successively tightens the layout zone to steer the interaction towards increasingly compact layout arrangements. Considering various principles of self-organization, SWARM is able to evoke the phenomenon of emergence: although each module only has a limited viewpoint and selfishly pursues its personal objectives, remarkable overall solutions can emerge on the global scale.

T-CREST: THE TIME-PREDICTABLE MULTICORE PROCESSOR T-CREST

Authors: Martin Schöberl, Luca Pezzarossa and Jens Sparso, Technical University of Denmark, DK

Timeslots:

UB03.2	Tuesday, 26 March 2019	1500 – 1730
UB07.5	Wednesday, 27 March 2019	1400 – 1600

Future real-time systems, such as advanced control systems or real-time image recognition, need more powerful processors, but still a system where the worst-case execution time (WCET) can be statically predicted. Multicore processors are one answer to the need for more processing power. However, it is still an open research question how to best organize and implement time-predictable communication between processing cores. T-CREST is an open-source multicore processor for research on time-predictable computer architecture. In consists of several Patmos processors connected by various time-predictable communication structures: access to shared off-chip, access to shared on-chip memory, and the Argo network-on-chip for fast inter-processor communication. T-CREST is supported by open-source development tools, such as compilation and WCET analysis. To best of our knowledge, T-CREST is the only fully open-source architecture for research on future real-time multicore architectures.

TIMING & POWER CHARACTERIZATION FRAMEWORK FOR EMBEDDED PROCESSORS

Authors: Mark Kettner and Frank Oppenheimer, OFFIS - Institute for Information Technology, DE

Timeslots:

UB01.1	Tuesday, 26 March 2019	1030 – 1230
UB02.1	Tuesday, 26 March 2019	1230 – 1500
UB05.1	Wednesday, 27 March 2019	1000 – 1200
UB06.1	Wednesday, 27 March 2019	1200 – 1400

We present a framework that significantly reduces the effort for creating accurate energy/timing models for embedded processors covering different conditions (e.g. varying temperature and clock frequency). It supports the systematic collection of large amount of timing and power data needed to cover the complete microprocessors' ISA in different working conditions. Since manual measurements are tedious and error-prone we present an automated approach. The physical setup consists of a processor board, a power measurement device, a heating element and a logic analyser observing the processor's GPIOs. The software consists of a code-generator for characterization binaries, a control program which orchestrates the physical setup and the evaluation software which generates the desired timing and power data. We will demonstrate this framework for an ARM Cortex-M microcontroller and present interesting and even undocumented behaviour while using certain CPU and FPU features.

TINYWIDS: A INTRUSION DETECTION SYSTEM FOR WIRELESS SENSOR NETWORKS

Authors: Walter Tiberti[1] and Luigi Pomante[2]
[1]University of L'Aquila, IT; [2]DEWS, IT

Timeslots:

UB09.1	Thursday, 28 March 2019	1000 – 1200
UB10.1	Thursday, 28 March 2019	1200 – 1430

In the domain of Wireless Sensor Networks (WSN), providing an effective security solution to protect the motes and their communications is challenging. Due to the hard constraints on performance, storage and energy consumption, normal network-security related techniques cannot be applied. Focusing on the "Intrusion Detection" problem, we propose a real-world application of our WSN Intrusion Detection System (WIDS). WIDS exploits the Weak Process Models to classify potential security issues in the WSN and to notify the operators when an attack tentative is detected. In this demonstration, we show how our IDS works, how it detects some basic attacks and how the IDS can evolve to fullfil the needs of secure WSN deployments.

WTG: WAVEFORM TRANSITION GRAPHS: A DESIGNER-FRIENDLY FORMALISM FOR ASYNCHRONOUS CIRCUITS

Authors: Danil Sokolov, Newcastle University, GB

Timeslots:

UB01.2	Tuesday, 26 March 2019	1030 – 1230
UB02.2	Tuesday, 26 March 2019	1230 – 1500

Asynchronous circuits are a promising class of digital circuits that has numerous advantages over their synchronous counterparts, especially in the domain of "little digital" speed-independent (SI) controllers. Nonetheless, their adoption has not been widespread, which in part is attributed to the difficulty of entry into complex models employed for specification of SI circuits, like Signal Transition Graphs (STGs), by electronic designers. We propose a new model called Waveform Transition Graphs (WTGs) which resembles the timing diagrams, that are very familiar to circuit designers, and defines its formal behaviour semantics. This formalization enables translation of the WTGs into equivalent STGs in order to reuse the existing body of research and tools for verification and logic synthesis of speed-independent circuits. The development of WTGs has been automated in the Workcraft toolkit (https://workcraft.org), allowing their conversion into STGs, verification and synthesis.

SEE YOU AT THE UNIVERSITY BOOTH!

University Booth Co-Chairs
Elena Ioana Vatajelu, TIMA, FR
Andreas Vörg, edacentrum, DE

university-booth@date-conference.com

FRINGE MEETINGS & CO-LOCATED WORKSHOPS

A number of specialist interest groups will be holding their meetings at DATE 2019. The following meetings are scheduled at the moment. A complete list of fringe meetings can also be found on the DATE homepage **www.date-conference.com**

Date & Time	Title	Room
MON 1800 – 2100	**Welcome Reception & PhD Forum, hosted by EDAA, ACM SIGDA, and IEEE CEDA**	Lunch Area
TUE 1300 – 1430	**ETTTC Meeting**	Room 10
TUE 1600 – 1800	**EDAA General Assembly**	Room 10
WED 0830 – 1130	**Exceeding Reliably the Energy Scaling Limits in Commodity Servers for Edge/Cloud Deployments**	Room 9
WED 1230 – 1430	**Meeting of the IFIP Working Group 10.5**	Room 10
THU 0830 – 1230	**AMASS Open Industrial Workshop**	Room 10
THU 0900 – 1500	**Accelerate real-time high definition video processing designs with Digilent Zybo Z7, a Zynq-7000 AP SoC Platform and Xilinx Vivado HLS**	Room 9
THU 1230 – 1330	**DATE Sister Events Meeting**	Lunch Area
FRI 1000 – 1500	**International F1/10 Autonomous Racing Demo supported by IEEE CEDA**	between rooms 1 and 4

MON

Welcome Reception & PhD Forum, hosted by EDAA, ACM SIGDA, and IEEE CEDA

Lunch Area 1800 - 2100

PhD Forum Chair: Robert Wille, Johannes Kepler University Linz, AT

All registered conference delegates and exhibition visitors are kindly invited to join the DATE 2019 Welcome Reception and subsequent PhD Forum, which will take place on Monday, 25 March 2019, from 1800 - 2100 at the DATE venue in the Lunch Area.

The PhD Forum of the DATE Conference is a poster session and a buffet style dinner hosted by the European Design Automation Association (EDAA), the ACM Special Interest Group on Design Automation (SIGDA), and the IEEE Council on Electronic Design Automation (CEDA). The purpose of the PhD Forum is to offer a forum for PhD students to discuss their thesis and research work with people of the design automation and system design community. It represents a good opportunity for students to get exposure on the job market and to receive valuable feedback on their work.

FM01-1 **Adaptive Runtime Resource Management for Mobile CMPs through Self-awareness**
Author: Bryan Donyanavard, University of California, Irvine, US

FM01-3 **Optimization of Trustworthy Biomolecular Quantitative Analysis Using Cyber-Physical Microfluidic Platforms**
Mohamed Ibrahim, Duke University, US

FM01-5 **Analysis and Optimization of Reliability Issues of VLSI Power Grid Networks**
Author: Sukanta Dey, Indian Institute of Technology Guwahati, IN

FM01-6 **Computer-Aided Design for Quantum Computing**
Author: Alwin Zulehner, Johannes Kepler University Linz, AT

FM01-7 **New Views for Stochastic Computing: From Time-Encoding to Deterministic Processing**
Author: M. Hassan Najafi, University of Louisiana at Lafayette, US

FM01-9 **System-level Mapping and Synthesis of Data Flow-Oriented Applications on MPSoCs**
Authors: Tobias Schwarzer and Jürgen Teich, Friedrich-Alexander-Universität Erlangen-Nürnberg, DE

FM01-14 **Compositional Circuit Design with Asynchronous Concepts**
Author: Jonathan Beaumont, Imperial College London, GB

FM01-15 **Automatic Methods for the Design of Droplet Microfluidics**
Author: Andreas Grimmer, Johannes Kepler University Linz, AT

FM01-16 **Worst-Case Execution Time Guarantees for Runtime-Reconfigurable Architectures**
Authors: Marvin Damschen, Lars Bauer and Joerg Henkel, Karlsruhe Institute of Technology, DE

FM01-17 **Architecture and Programming Model Support For Reconfigurable Accelerators in Multi-Core Embedded Systems**
Author: Satyajit Das, Université de Bretagne-Sud, FR

FM01-18 **Supervised Testing of Embedded Concurrent Software**
Author: Jasmin Jahic, Fraunhofer IESE, DE

FM01-19 **Advanced 3D-Integrated Memory Subsystems for Embedded and High Performance Computing Systems**
Author: Deepak Mathew, University of Kaiserslautern, DE

FM01-20 **Controlling Writes for Energy Efficient Non-Volatile Cache Management in Chip Multiprocessors**
Author: Sukarn Agarwal, Indian Institute of Technology Guwahati, IN

FM01-21 **Design Techniques for Energy-Quality Scalable Digital Systems**
Author: Daniele Jahier Pagliari, Politecnico di Torino, IT

FM01-23 **MuTARe: A Multi-Target Adaptive Reconfigurable Architecture**
Author: Marcelo Brandalero, Universidade Federal do Rio Grande do Sul, BR

FM01-25 **Bitstream-level Proof-Carrying Hardware**
Author: Tobias Wiersema, Paderborn University, DE

FM01-26 **Efficient Virtual Prototype Verification Techniques: Theory, Implementation and Application**
Author: Vladimir Herdt, University of Bremen, DE

FM01-27 **Hybrid-DBT: Hardware-Accelerated Dynamic Binary Translation targeting VLIW processors**
Author: Simon Rokicki, Irisa, FR

FRINGE MEETINGS & CO-LOCATED WORKSHOPS

FM01-28 **Low-power Architectures for Automatic Speech Recognition**
Author: Hamid Tabani, Barcelona Supercomputing Center, ES

FM01-30 **Low Overhead & Energy Efficient Storage Path for Next Generation Computer Systems**
Author: Athanasios Stratikopoulos, The University of Manchester, GB

FM01-31 **A Model driven Framework with Assertion Based Verification Support for Embedded Systems Design Automation**
Author: Muhammad Waseem Anwar, National University of Sciences & Technology (NUST), PK

FM01-32 **Optimization and Analysis for Dependable Software on Unreliable Hardware Platforms**
Author: Kuan-Hsun Chen, Technical University of Dortmund, DE

FM01-33 **Multiple NoC based Custom Implementation and Traffic Distribution to attain Energy Efficient CMPs**
Authors: Sonal Yadav, Vijay Laxmi and Manoj Singh Gaur, MNIT Jaipur, IN

FM01-37 **True Random Number Generators for FPGAs**
Author: Bohan Yang, ESAT/COSIC and iMinds, KU Leuven, BE

FM01-38 **HW/SW Co-Design Methodology for Mixed-Criticality and Real-Time Embedded Systems**
Author: Vittoriano Muttillo, University of L'Aquila, IT

FM01-41 **Improving Bundled-Data Handshake Circuits**
Author: Norman Kluge, Hasso-Plattner-Institut, University of Potsdam, DE

FM01-43 **IC Design of an Inductorless DC/DC Converter with Wide Input Voltage Range in Low-Cost CMOS**
Author: Gabriele Ciarpi, University of Pisa, IT

FM01-44 **Monolithic-3D Integration based Memory Design techniques towards Robust and in-memory computing**
Authors: Srivatsa Rangachar Srinivasa[1], John (Jack) Sampson[1], Meng-Fan (Marvin) Chang[2] and Vijaykrishnan Narayanan[1]
[1]Penn State University US; [2]National Tsing Hua University, TW

FM01-47 **Cross-Layer Synthesis and Integration Methodology of Wavelength-Routed Optical Networks-on-Chip for 3D-Stacked Parallel Computing Systems**
Author: Mahdi Tala, University of Ferrara, IT

FM01-48 **Adaptive Knobs for Resource Efficient Computing**
Author: Anil Kanduri, University of Turku, FI

FM01-52 **Device-Circuit Co-design Employing Phase Transitioning Materials for Low Power Digital Applications**
Author: Ahmedullah Aziz, Purdue University, US

FM01-53 **Advanced CAD Frameworks for Design IP Protection**
Author: Satwik Patnaik, New York University, US

FM01-54 **Emerging Computing: Acceleration of Big Data Applications**
Author: Mohsen Imani, University of California San Diego, US

TUE

ETTTC Meeting

Room 10 1300 - 1430

Organiser: Alberto Bosio, INL, FR

The European Test Technology Technical Council (ETTTC) is the European section of the TTTC. ETTTC is a volunteer professional organization sponsored by the IEEE Computer Society. TTTC's goals are to contribute to our members' professional development and advancement, to help them solve engineering problems in electronic test, and to help advance the state-of-the art. This meeting provides all actors involved in test technology to share information on upcoming events and projects.

TUE

EDAA General Assembly

Room 10 1600 - 1800

Organiser: Norbert Wehn, University of Kaiserslautern, DE

General assembly meeting for the members of EDAA, open to everyone interested in Electronic Design Automation.

WED

Exceeding Reliably the Energy Scaling Limits in Commodity Servers for Edge/Cloud Deployments

Room 9 0830 - 1130

Organiser: Georgios Karakonstantis, Queen's University Belfast, GB

Conservative design margins in modern processor/memory chips may guarantee correct execution of the software layers of computing systems under various operating conditions, accounting for the inherent variability among different cores/cells of the same chip, among different manufactured chips and among different workloads; however such margins limit significantly the energy efficiency.
In this workshop, we will present recent methods and studies on design-time voltage/refresh-rate margins characterization and identification in modern multicore CPUs and DRAMs within commodity servers. In addition, we will discuss how such methods can guide informed decisions at the software layers for exceeding the conservative energy scaling limits, while presenting mechanisms at the virtualization (Hypervisor) and resource management (Openstack) layers for ensuring reliable system operation in Edge and Cloud deployments.
The workshop will include talks by IBM Research, ARM, WorldSensing, Queen's University and Universities of Athens, Cyprus and Thessaly revealing challenges and latest results from academia and industry.
The research presented in this workshop is supported by the Horizon 2020 UniServer project (http://www.uniserver2020.eu/).

WED

Meeting of the IFIP Working Group 10.5

Room 10 1230 - 1430

Organiser: Masahiro Fujita, University of Tokyo, JP

International Federation for Information Processing (IFIP) is the leading multinational, non-political organization in Information & Communications Technologies and Sciences and is recognized by United Nations and other world bodies. It has over 100 Working Groups and 13 Technical Committees. This is a meeting organized by WG10.5 (VLSI related technologies).

THU

AMASS Open Industrial Workshop

Room 10 0830 - 1230

Organiser: Jose Luis de la Vara, Universidad Carlos III de Mardrid, ES

AMASS (https://www.amass-ecsel.eu/) is a H2020-ECSEL R&D project between industry and research organisations that has created and consolidated the de-facto European-wide open tool platform, ecosystem, and self-sustainable community for assurance and certification of safety-critical systems (https://www.polarsys.org/opencert/). The ultimate goal of AMASS is to lower certification costs in face of rapidly changing features and market needs. This has been achieved by establishing a novel holistic and reuse-oriented approach for architecture-driven assurance (fully compatible with standards such as SysML), for multi-concern assurance (for co-analysis and co-assurance of e.g. security and safety aspects), and for seamless interoperability between assurance and engineering activities along with third-party activities (e.g. external assessments and supplier assurance).The workshop is targeted at both practitioners and researchers aiming to gain awareness of the latest advances on cost-effective assurance and certification of safety-critical systems, and of how the corresponding solutions work. We will present practical aspects and concrete application examples of the main AMASS results in two main sessions: Introduction to the AMASS concepts and methodology and Application of the AMASS approach.

THU

Accelerate real-time high definition video processing designs with Digilent Zybo Z7, a Zynq-7000 AP SoC Platform and Xilinx Vivado HLS

Room 9 0900 - 1500

Organiser: Cristina Dabacan, Digilent, RO
Speaker: Elod Gyorgy, FPGA Team leader at Digilent, RO

The workshop aligns with Digilent's mission of providing a hands-on, project-based, open-ended approach to education. Attendees will use Digilent Zybo Z7 (a Xilinx Zynq SoC FPGA platform), PCAM (5MP camera sensor) and Xilinx Vivado HLx to implement a real-time high definition video processing application.

Examples in the workshop materials are based on both high-level programming language (C++) and hardware description language (VHDL). Trainers will demonstrate HLS design flow, IP core usage, simulation and hardware debugging. Participants will leave the workshop with instructional materials and PCAM, 5MP camera sensor so that they can easily adopt this innovative technique in their own courses and projects.

Topics covered:
- Explain parallelism and program execution
- Introduce Xilinx FPGA Architecture and Vivado HLS
- Introduce Digilent Zybo Z7 and PCAM
- Accelerate video processing algorithm on Xilinx Vivado
- Implement video processing design on Digilent Zybo Z7 and PCAM

THU

DATE Sister Events Meeting

Lunch Area 1230 - 1330

Organiser: Norbert Wehn, University of Kaiserslautern, DE

Meeting of the represenatives from ASP-DAC, ICCAD, DAC and DATE

FRI

International F1/10 Autonomous Racing Demo supported by IEEE CEDA

between rooms 1 and 4 1000 - 1500

Organisers:
Paolo Burgio, University of Modena and Reggio Emilia, IT
Marko Bertogna, Modena and Reggio Emilia, IT

The F1/10 is an open-source, affordable, and high-performance 1/10 scale autonomous vehicle testbed. The F1/10 carries a full suite of sensors, perception, planning, control, and networking software stacks that are similar to full scale solutions. The F1/10 testbed enables research and education in autonomous and cooperative systems, making autonomy more accessible.

Indeed, a F1/10 vehicle featuring most advanced sensors can be set-up in one week with few thousands euros following our tutorials, and is currently used by universities around the world to do research in the field of computer vision, machine learning, real-time systems, autonomous systems, vehicle dynamics control, highly-cooperative fleets of vehicles and drones.

During the event, the High-Performance Real-Time Lab (HiPeRT - https://hipert.unimore.it/) from University of Modena and Reggio Emilia will bring its fully autonomous F1/10 prototypes, and perform demo sessions of:

- Single-lap time trials, where the goal of vehicles is to complete a single lap alone, in the shortest time possible
- Long-stint sessions, where the goal of the vehicle is to complete as many laps as possible in three minutes, i.e., where the crashes hazard must me minimal, and driver reliability is the key
- Head-to-head race sessions, where two or more vehicle exercise their algorithms for object tracking and collision avoidance in a complex and challenging scenario

These vehicles will participate in the 4th F1/10 International Autonomous Racing Competition (http://f1tenth.org/), which gathers researchers and makers from all around the world in two days of challenges and networking, fostering the exchange of ideas and cooperations in the community.

The competition is held twice per year between Europe and North America, and now is at its fourth edition. Last event was in Turin, and the next one will take place in Montreal, Canada in April 2019.

Join the community!

The demo sessions will take place during the break times of the Friday Workshops.

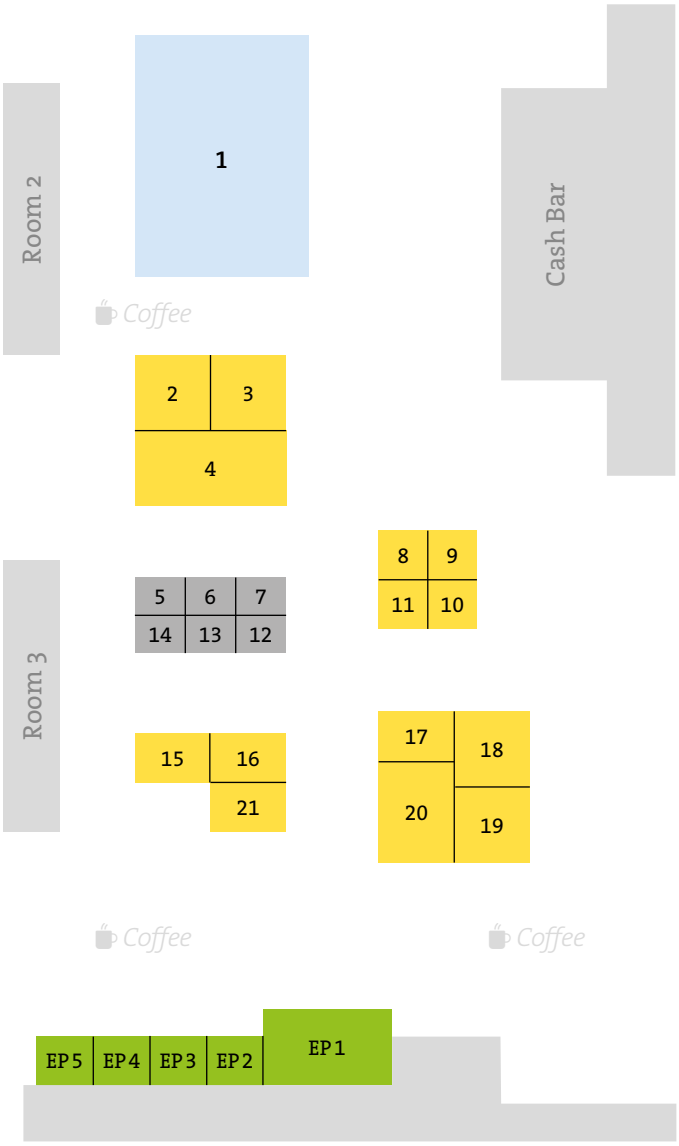
All participants, who are registered for one of the Friday Workshops, are cordially invited to join the presentation area in front of Room 1.

EXHIBITION GUIDE

On behalf of the whole Organising Committee, we thank you very much for visiting DATE 2019 and are happy to welcoming you in the beautiful city of Florence, Italy!

All corporate sponsors and participating exhibitors are listed with contact details and information about their products and services being presented at the conference. The company profiles will assist you in finding the right solution and/or person to contact.

EXHIBITION FLOOR PLAN



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COMPANY PROFILES

BOOTH 21

Advantest Europe GmbH

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A world-class technology company, Advantest is a leading producer of automatic test equipment for the semiconductor industry and a premier manufacturer of measuring instruments used in the design and production of electronic instruments and systems. Our exhibit, Cloud Testing Service, offers an alternative to standard test hardware. CTS addresses the challenges facing major chipmakers, R&D engineers, design labs, universities and research institutes to get access to large ATE testers to debug and test their devices. It is specially set up with a flexibly, pay per use model, ideal for R&D.

The main features of CTS include:

- Small and portable personal tester with all signals, features and performance
- Multiple IPs to customize testing needs and simple EDA data migration
- Easy testing through GUI interfaces
- No capital investment in tester hardware

www.cts-advantest.com/en

ASIC and SOC Design:
Physical Analysis (Timing, Themal, Signal) • Verification

Test:
Design for Test • Logic Analysis • Test Automation (ATPG, BIST) • Silicon Validation

SPONSOR

Cadence Academic Network

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Cadence Academic Network was launched by Cadence in 2007. The aim was to promote the proliferation of leading-edge technologies and methodologies at universities renowned for their engineering and design excellence. A knowledge network among selected universities, research institutes, industry advisors and Cadence was established to facilitate the sharing of technology expertise in the areas of verification, design and implementation of microelectronic systems.

Cadence Academic Network is sponsoring the DATE Interactive Presentations (IPs) again.

EP 4

CAEN

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CAEN is one of the most important spin-offs of the Italian Nuclear Physics Research Institute and it was founded in Viareggio in 1979. CAEN designs and manufactures sophisticated electronic equipment for nuclear physics research and is today among the world's leading companies in the field: there are hundreds of thousand CAEN Low/High Voltage and data acquisition channels now working in all most important Nuclear Physics Laboratories.

Over the years, CAEN has diversified its offer, extending its market, taking part into national and international programs and becoming a real "Innovation Company". In this way CAEN added to its core business new experiences such as UHF RFID, microelectronics, aerospace, biomed, and homeland security.

CAEN is known today as the only company in the world able to offer, besides a complete range of power supply and data acquisition systems, a large choice of Front-End modules implemented using ASICs internally developed, totaling more than 250 catalogue products. However, this number is not exhaustive: part of CAEN production is custom designed for Big Science. One of the main users is CERN, which hosts the LHC and where ATLAS and CMS experiments have recently demonstrated the existence of the particle known as the "Higgs boson". This demonstration culminated with the awarding of the Nobel Prize for Physics 2013 to Francois Englert and Peter W. Higgs.

CAEN counts on more than 30 electronic engineers and physics PhDs are taking to the next level the technological content and pushing forward innovation, proudly delivering "Tools for discovery".

BOOTH 2

Circuits Multi-Projects (CMP)

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Circuits Multi-Projects (CMP) is a manufacturing broker for ICs and MEMS, for prototyping and low volume production. Since 1981, more than 600 Institutions from 70 countries have been served, more than 8100 projects have been prototyped through 1100 manufacturing runs, and 74 different technologies have been interfaced. Integrated Circuits are available on CMOS, SiGe BiCMOS, HV-CMOS, CMOS-Opto from STMicroelectronics and ams down to 28 nm FDSOI. Design kits for most IC CAD tools and Engineering kits for MEMS are available. Assembling is provided in a wide range of plastic and ceramic packages.

ASIC and SOC Design:
MEMS Design

Services:
Prototyping • Foundry & Manufacturing

EP 2

CLASS. Edge and Cloud Computation: A Highly Distributed Software for Big Data Analytics

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CLASS aims to develop a novel software architecture framework to help big data developers to efficiently distributing data analytics workloads along the compute continuum (from edge to cloud) in a complete and transparent way, while providing sound real-time guarantees. This ability opens the door to the use of big data into critical real-time systems, providing to them superior data analytics capabilities to implement more intelligent and autonomous control applications.

The capabilities of the CLASS framework will be demonstrated on a real smart-city use case in the City of Modena (Italy), featuring a heavy sensor infrastructure to collect real-time data across a wide urban area, and three connected vehicles equipped with heterogeneous sensors/actuators and V2X connectivity to enhance the driving experience.

The CLASS project has received funding from the European Union's Horizon 2020 research and innovation programme under the grant agreement No 780622

BOOTH 6

Cobham Gaisler AB

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Cobham Gaisler AB is a provider of system-on-chip (SoC) solutions for advanced applications in the commercial and space flight domain. Cobham Gaisler's products consist of user-customizable 32-bit SPARC V8 processor cores, peripheral IP cores and associated software and development tools. Our solutions help companies and research institutes develop highly competitive application-specific SoC designs, as well as providing radiation- hardened components for the space market.

The key product is the LEON synthesizable processor model together with a full development environment and a library of well over one hundred IP cores (GRLIB). The LEON processor and the library of IP cores are highly configurable, and are suitable for SoC designs. The processor combines high performance and an advanced architecture with low gate count and low power consumption. Implementing the SPARC V8 architecture (IEEE-1754), the LEON processor offers a truly open and well supported instruction set. Besides offering flexible stand-alone IP cores for integration in existing designs, the GRLIB design environment provides EDA tool and target technology integration for many existing FPGA and ASIC technologies, making system implementation quick and straightforward.

One outstanding feature of the IP-core library is that it also has always been distributed as free open-source, available from http://gaisler.com/index.php/products/ipcores/soclibrary. The open-source version of GRLIB is complete and perfectly suitable for complex SoC design in research and other less constrained environments.

The IP core offering is complemented by a software infrastructure consisting of instruction set simulators, debug tools, compilers and operating systems, both commercial and free open-source.

Test:
System Test

Services:
Design Consultancy

Embedded Software Development:
Compilers • Real Time Operating Systems • Software/Modelling

Hardware:
FPGA & Reconfigurable Platforms • Development Boards

Semiconductor IP:
CPUs & Controllers • Encryption IP • Memory IP • On-Chip Bus Interconnect • On-Chip Debug • Processor Platforms • Synthesizable Libraries • Test IP

Application-Specific IP:
Data Communication • Networking • Security • Telecommunication

BOOTH 17

Collaborative Research Center SFB 876 – Providing Information by Resource-Constrained Data Analysis

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The collaborative research center CRC 876 (SFB 876) brings together the research areas of data analysis (data mining, machine learning, statistics) and embedded systems (cyber-physical systems,embedded systems) and expands them such that information from distributed, dynamic data masses becomes available for decision processes in real-time, on site. The acquisition and storage of high-throughput experiments in biomedicine, astrophysical telescopes or particle-physical experiments exceeds the capacity of today's computers, so that the analysis must be pushed to the edge, i.e., to the sensor. Also, the analysis of production processes that leads to direct interventions or the prediction of traffic for a better mobility management would benefit from at least a partial analysis directly at the data sources. The analysis of distributed, streaming data requires novel algorithms and models, that take into account the resource restrictions. Already at the start of our CRC 876, we pointed out that data analysis should inspect more closely its execution on diverse platforms. We defined resource constraints as the relation between the demands of analysing big data and the technical capabilities of a platform or device.

Since 2011, the DFG has been funding the major research project. In 2019 the CRC 876 funding has been guaranteed for a further four years. Involved are five faculties of the TU Dortmund: Computer Science, Statistics, Electrical Engineering and Information Technology, Mechanical engineering and Physics. The TU Dortmund is working together with the University of Duisburg-Essen, the University Hospital Essen, as well as with the Leibniz- Institute for Analytical Sciences -ISAS e.V.

ASIC and SOC Design:
Power & Optimisation

System-Level Design:
Acceleration & Emulation • Hardware/Software Co-Design

Services:
Prototyping • Data Management and Collaboration • Training

Embedded Software Development:
Compilers • Real Time Operating Systems • Debuggers • Software/Modelling

BOOTH 18

Collaborative Research Centre 901 – On-The-Fly Computing

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The objective of CRC 901 – On-The-Fly Computing (OTF Computing) – is to develop techniques and processes for automatic on-the-fly configuration and provision of individual IT services out of base services that are available on world-wide markets.In addition to the configuration by special OTF service providers and the provision by so-called OTF Compute Centers, this involves developing methods for quality assurance and the protection of participating clients and providers, methods for the target-oriented further development of markets, and methods to support the interaction of the participants in dynamically changing markets.

CRC 901 is divided into four project areas. Project area A is concerned with the algorithmic and economic basics for organizing large dynamic markets. This involves, on the one hand, algorithmic processes for organizing large networks in general and the interaction in networks in particular and, on the other hand, economic concepts for incentive systems in order to direct the participants in the markets. Project area B investigates processes of the modeling, composition and quality analysis of services and service configurations aiming at on-the-fly development of high-quality IT services. Project area C develops reliable execution environments for on-the-fly computing and is concerned with questions of the stability and security of markets, the organization of highly heterogeneous OTF Compute Centers and the provision of configured services by those centers.

ASIC and SOC Design:
Verification

System-Level Design:
Hardware/Software Co-Design

Hardware:
FPGA & Reconfigurable Platforms

COMPANY PROFILES

SPONSOR

Destination Florence Convention and Visitors Bureau

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Operating since 1995, Destination Florence Convention and Visitors Bureau is the official destination promoter, with the mission to increase quality and importance of events, destination weddings and luxury market in Florence. Our company is proud to have nearly 300 members, representing the top-quality offer of the destination and this, together with the official partnership with the Florence Municipality, allowed us to open the doors of the city for our clients.

The activity of promotion of Destination Florence CVB is heading for M.I.C.E., destination weddings and leisure markets.

The aim of the M.I.C.E. division, called Firenze Convention Bureau, is to increase quantity, quality and importance of events, conferences to be held in the city, finding and suggesting the best services and rates thanks to the support of our partners. FCB offers expert services for corporate, associations and independent meeting planners in order to support them on the venue selection process as well as in planning and producing successful meetings, incentives, conventions, exhibitions and events. FCB can provide a wide range of information about the city, including: accommodation and transportation facilities, lists of local suppliers such as Professional Congress Organizers (PCO), Destination Management Companies (DMC), hotels and party service suppliers such as AV, interpretation services, sightseeing companies, unique venues and tourist resources, stand contractors.

BOOTH 8

DFG SPP 2037 – Scalable Data Management for Future Hardware

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The priority programme 2037 „Scalable Data Management for Future Hardware" is funded by the german research funding organization DFG and comprises 10 projects from german universities. The programme is based on the observation that the currently used database concepts and systems are not well prepared to support emerging application domains such as eSciences, Industry 4.0, Internet of Things or Digital Humanities: From a user's perspective flexible domain-specific access interfaces are requires; novel data models for these application domains have to be integrated; consistency guarantees which reduce flexibility and performance should be adaptable according to the requirements; and the volume and velocity of data caused by ubiquitous sensors have to be mastered by massive scalability and online processing. At the same time current and future hardware trends such as many-core CPUs, co-processors like GPU and FPGA, novel storage technologies like NVRAM and SSD as well as high-speed networks provide new opportunities.

In order to open up the exemplarily mentioned application domains together with exploiting the potential of future hardware generations it becomes necessary now, to fundamentally rethink current database architectures. Thus, the objective of the priority programme is to answer the scientific questions related to these issues. As a result, we expect the development and evaluation of architectures and abstractions for flexible and scalable data management techniques which provide extensibility regarding new data models including processing and access mechanisms for emerging applications, and exploit the features of modern and heterogeneous hardware as well as system-level services.

EP 2

ELASTIC. A Software Architecture for Extreme-Scale Big-Data Analytics in Fog Computing Ecosystems

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W www.elastic-project.eu

ELASTIC will produce a novel software architecture to distribute resources from edge to cloud. The software includes the development of a new concept of elasticity, ensuring smooth performance across the compute continuum in an innovative fog-computing environment. The project aims to significantly increase the data analytics capabilities of extreme-scale big-data workloads, while fulfilling multiple non-functional requirements, including real time, energy efficiency, security and unstable communications.

ELASTIC includes a smart-mobility use case, deploying a sensor network to collect the data from the tram network of Florence (Italy). The trams will feature advanced embedded architectures, V21 connectivity, heterogeneous sensors and access to cloud resources, improving public/private transport interaction and allowing the creation of advanced driving assistance applications.

The ELASTIC project has received funding from the European Union's Horizon 2020 research and innovation programme under the grant agreement No 825473

BOOTH 20

Embedded Systems Initiative (ESI)

Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU) /
Interdisziplinäres Zentrum für Eingebettete Systeme (ESI)
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The Interdisciplinary Centre for Embedded Systems (ESI) combines the expertise in all aspects related to embedded systems design of currently 15 departments of the Friedrich-Alexander-Universität Erlangen-Nürnberg. ESI functions as a central point of contact for cooperation between companies and research institutes of the FAU Erlangen-Nürnberg, allowing to offer diverse and special expertise in cooperation with companies of various sectors. ESI functions as a central point of contact for cooperation between companies and research institutes of the FAU Erlangen-Nürnberg in the Emdedded Systems Domain.

Along with basic research, practical user knowledge is essential to successfully developed embedded systems. The Fraunhofer Institute for Integrated Circuits (IIS) is well-known for its knowledge in applied research. The ESI Application Centre builds a bridge between basic research of the FAU and applied research knowledge of the Fraunhofer IIS to master the complexity of future research and innovations. Our research topics are bundled in the ESI Application Centre in three Labs:

- Automation@ESI (Industrial Automation, Industry 4.0)
- Automotive@ESI (Sensors and driver assistence systems)
- Fitness@ESI (wireless sensors and training assistence)

The ESI Application Centre offers:

- Interdisciplinary solutions focused on your needs
- Independent development, evaluation and implementation of Embedded Systems according to your specifications
- Many years of research experience and successfully concluded research projects as well as effective cooperations
- Scientific know-how especially in the following areas:
  - Multicore Systems
  - Design Methods, especially Hardware-Software-Co-Design
  - Wireless Communication and Localisation
  - Integrated Sensors
  - Machine Learning, Pattern Analysis and Image and Data Processing

Services:
Design Consultancy • Prototyping

COMPANY PROFILES

EP 1

Eurolab4HPC

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Eurolab4HPC is a 2-year Horizon 2020 funded project committed to make Europe excel in academic research and innovation in HPC technology. To reach this goal it has defined 4 actions:

1. To structure the HPC community by adding members to develop a community of excellence that engages in focused high-quality cross-stack activity.
2. To promote entrepreneurship by building an innovation pipeline from general purpose entrepreneurial training, business prototyping, business plan development and helping with funding. Take a look at our events calendar.
3. To stimulate technology transfer by connecting with other technology transfer activities and providing competitive seed funding for HPC technology transfer. New open calls in 2019!
4. To disseminate community news by investing substantial resources in dissemination activities, creating a stronger Eurolab4HPC brand.

For further information visit: eurolab4hpc.eu and don't forget to visit our stand here at DATE 2019!

BOOTH 3

EUROPRACTICE

EUROPRACTICE IC office & IC Manufacturing Center
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EUROPRACTICE was launched by the European Commission in 1989 to help companies improve their competitive position in world markets by adopting ASIC, Multi-Chip Module or Microsystems solutions in their products. The program helps to reduce the perceived risks and costs associated with these technologies by offering potential users a range of services, including initial advice and ongoing support, reduced entry costs and a clear route to chip manufacture and product supply.

Since its creation, EUROPRACTICE has bridged the gap between academia and industry in the high-tech world by offering more than 600 European universities and research institutes affordable access to the latest IC (Integrated Circuits) design tools and technologies. This is reflected in the training provided by universities from which the best IC design engineers emerge, essential for the SMEs innovation in new IC products.

The ultimate goal of EUROPRACTICE is to enhance European industrial competitiveness in the global marketplace. The EUROPRACTICE services are open to industrial companies (especially SMEs), research institutes and academic users.

SERVICES OFFERED TO EUROPEAN SMEs AND ACADEMIC INSTITUTIONS:

The mission statement of EUROPRACTICE is to provide the European industry and academia with a platform to develop smart integrated systems, from advanced prototype design to volume production. The latter is achieved by providing affordable and easier access to a wide range of state-of-the-art industry-grade fabrication technologies and design

tools complemented with training and support to the customer in all critical steps which are needed.

- Affordable access to industry-standard and state-of-the-art design (CAD) tools
- Distribution and full support of high-quality cell libraries and design kits for the most popular CAD tools
- Low-cost prototyping in various technologies (both ASIC and More than Moore) via MPW runs
- Access to advanced packaging and smart system integration
- Training courses in advanced design flows and on various technologiesIC

SERVICES OFFERED TO THE GLOBAL INDUSTRY:

EUROPRACTICE also offers industry worldwide access to microelectronic and microsystem design services, MPW prototyping, small volume production, packaging and test operations. Note, this does not include access to design tools.

Industry from all over the world have rapidly discovered the benefits of using the EUROPRACTICE IC service to help bring new product designs to market quickly and cost-effectively. The EUROPRACTICE ASIC route supports especially those companies who do not always need the full range of services or high production volumes. Those companies will gain from the flexible access to silicon prototype and production capacity at leading foundries, design services, high quality support and manufacturing expertise. This you can get all from EUROPRACTICE IC service, a service that is already established for 20 years in the market.

THE EUROPRACTICE SERVICES ARE OFFERED BY THE FOLLOWING CENTERS:

- imec (Belgium)
- Fraunhofer-Institut für Integrierte Schaltungen (Fraunhofer IIS) (Germany)
- STFC Rutherford Appleton Laboratory (United Kingdom)
- CMP (France)
- Tyndall National Institute (Ireland)

EP 3

FED4SAE

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Through the Smart Anything Everywhere initiative, the European Commission is helping digitize European industry. FED4SAE is part of this strategy, targeting a large network of 'small' companies (startups, small/ medium enterprises and midcaps), including both technology specialists and low-tech companies. These companies can request solutions for specific use cases, which FED4SAE's industrial and advanced platforms will provide. This will include solutions comprising one of several components, such as sensors, data fusion/processing technology and actuators. These components make up cyber-physical systems, which link the physical and digital worlds.

FED4SAE also helps participants with innovation management, providing coaching and opportunities for networking to identify the best stakeholders – private investors, national/regional initiatives, business angels, potential customers, and so on.

In summary, FED4SAE offers companies:

- technical expertise via advanced platforms, that are either innovative technical solutions or testbeds which add value to the product
- product support via industrial platforms, being existing products provided by market leaders in the domain of cyber-physical and embedded systems, which can bring the innovation to a state of maturity
- innovation management, focusing on business, to help your innovation get to the market via the FED4SAE consortium and the Smart Anything Everywhere ecosystem
- up to €60,000 in funding, representing 70% of the declared budget of the work done

The kind of experiments which will be funded will address any smart application domain (mobility, city, health & well-being, industry, sensor, etc.), involving both advanced and industrial platforms supported by FED4SAE. The experiments shall be pan-European, allowing the awarded company to collaborate with cross-border advanced platforms and industrial partners.

You just need to provide the idea and we will help you get it to market – don't miss this opportunity!

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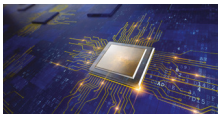

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- Thursday is Training Day *Sponsored by:* ARM

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DAC PAVILLION

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- Teardowns

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10:00am - 6:00pm

Tuesday, June 4
10:00am - 6:00pm

Wednesday, June 5
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Daily Networking Receptions

- Monday
- Tuesday
- Wednesday

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#56DAC

COMPANY PROFILES

BOOTH 12

Floadia Corporation

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W www.floadia.com

Floadia, Japanese company, provides Low power, cost Effective and Easily embedded Flash IPs. We are world-class experts in Non-Volatile Memory technology, design, test QA and production. Enjoy our cost effective and high quality eNVM solutions for your IoT, AI, and Automotive applications.

Semiconductor IP:
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Application-Specific IP:
Analogue & Mixed Signal IP

EP 1

HiPEAC - European Network on High Performance and Embedded Architecture and Compilation

HiPEAC
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Since 2004, the HiPEAC (High Performance and Embedded Architecture and Compilation) project has provided a hub for European researchers in computing systems; today, its network, the biggest of its kind in the world, numbers around 2000 specialists. HiPEAC members include both top-class researchers and industry representatives who want to shape the development of computing systems. Members benefit from a series of advantages, including industry insight, training, recruitment and peer-to-peer interaction.

HiPEAC organizes four networking events per year: the HiPEAC conference, two Computing Systems Weeks and a summer school. As part of the HiPEAC community, you can also contribute to the biennial HiPEAC Vision, an influential roadmap which informs European technology research policy areas. In addition, the project offers training, mobility support, help in finding excellent computing candidates and dissemination support.

The latest incarnation of the project, HiPEAC 5, began on 1 December 2017 and is delivered by 13 partners, led by Ghent University. It is funded by the European Union's Horizon 2020 research and innovation programme under grant agreement no. 779656.

To join for free email membership@hipeac.net.

For further information visit https://www.hipeac.net/network/#/industry/ and don't forget to visit our stand here at DATE 2019!

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IEEE Council on Electronic Design Automation (IEEE CEDA)

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The Council on Electronic Design Automation (CEDA) was established to foster design automation of electronic circuits and systems at all levels. The Council's field of interest spans the theory, implementation, and use of EDA/CAD tools to design integrated electronic circuits and systems. This includes tools that automate all levels of the design, analysis, and verification of hardware and embedded software up to and including complete working systems. CEDA enables the exchange of technical information by sponsoring publications, conferences and workshops and through local chapters for volunteers activities.

If you are interested please contact admin@ieee-ceda.com or check our website for more information about our activities and how to become a member for free.

BOOTH 14

Infineon Technologies Austria AG

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Infineon Technologies Austria AG is a group subsidiary of Infineon Technologies AG, a worldleading provider of semiconductor solutions that make life easier, safer and greener. Microelectronics from Infineon reduce the energy consumption of consumer electronics, domestic appliances and industrial facilities. They make a major contribution to the convenience, security and sustainability of vehicles, and enable secure transactions in the Internet of Things.

Besides Germany, Infineon Austria is the only subsidiary within the group that pools competencies for research and development, production as well as global business responsibility. The head office is in Villach, with further branches in Graz, Klagenfurt, Linz and Vienna. With 4,201 employees from around 60 countries (including 1,813 in research and development), in the financial year 2018 (ending in September) the company achieved a turnover of € 2.9 billion. An R&D expense rate of €498 million makes Infineon Austria one of the strongest industrial research companys' in Austria.

Further information at www.infineon.com/austria

ASIC and SOC Design:
Physical Analysis (Timing, Themal, Signal) • Verification • Analogue and Mixed-Signal Design • MEMS Design • RF Design

System-Level Design:
Physical Analysis • Hardware/Software Co-Design

Test:
Design for Test • Test Automation (ATPG, BIST) • Mixed-Signal Test

Embedded Software Development:
Software/Modelling

Semiconductor IP:
Analogue & Mixed Signal IP • CPUs & Controllers • Embedded Software IP • Test IP • Verification IO

Application-Specific IP:
Analogue & Mixed Signal IP • Digital Signal Processing • Security • Telecommunication • Wireless Communication

BOOTH 13

IngeniArs S.r.l.

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Innovative Italian start-up IngeniArs was born in 2014 out of its joint founders' extensive experience in the areas of electronics and advanced computer science engineering research. The company responds to the ever-increasing demand for innovation in the strategic aerospace, healthcare and automotive fields, offering highly advanced hardware/software products and managing the full lifecycle of electronics, microelectronics and embedded systems. IngeniArs already has several major achievements, such as obtaining prime contracts with the ESA and winning the EU Horizon 2020 SME Instrument Phase 1 and 2 projects.

ASIC and SOC Design:
Design Entry • Behavioural Modelling & Simulation • Synthesis • Power & Optimisation • Physical Analysis (Timing, Themal, Signal) • Verification

System-Level Design:
Behavioural Modelling & Analysis • Acceleration & Emulation • Hardware/Software Co-Design

Test:
Design for Test • System Test

Services:
Design Consultancy • Prototyping

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FPGA & Reconfigurable Platforms

Semiconductor IP:
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Application-Specific IP:
Data Communication • Digital Signal Processing • Networking • Security • Telecommunication

BOOTH 11

Intel

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Intel (NASDAQ: INTC), a leader in the semiconductor industry, is shaping the data-centric future with computing and communications technology that is the foundation of the world's innovations. The company's engineering expertise is helping address the world's greatest challenges as well as helping secure, power and connect billions of devices and the infrastructure of the smart, connected world – from the cloud to the network to the edge and everything in between. Find more information about Intel at newsroom.intel.com and intel.com.

BOOTH 20

Invasive Computing - CRC/Transregio 89

Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU)
SFB/Transregio 89: Invasives Rechnen (InvasIC)
Lehrstuhl für Informatik
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In the Transregional Collaborative Research Centre "Invasive Computing" (abbr. "InvasIC") scientific researchers from the Friedrich-Alexander-Universität Erlangen-Nürnberg, the Technische Universität München as well as the Karlsruhe Institute of Technology investigate together a novel paradigm for the design and programming of future parallel computing systems.

Its unique characteristic is to give a programmer explicit handles to specify and argue about resource requirements desired, or required in different phases of execution: Using an invade command, an application may instruct the operating system to claim a set of processors, memory and communication resources for being allocated for a, by default, subsequent exclusive use. In an infect phase, the application workload is then spread and executed on the obtained claim of resources. A retreat command finally frees a claim again, and the application may resume sequential execution. To support this idea of self-adaptive and resource-aware programming, not only novel programming concepts, languages, compilers, and operating system concepts had to be developed from scratch, but also revolutionary architectural changes in the design of MPSoCs (multiprocessor system-on-a-chip) including mechanisms to allocate and isolate resources on demand.

Find out more about the CRC/Transregio 89 on www.invasic.de.

ASIC and SOC Design:
Behavioural Modelling & Simulation • Power & Optimisation • Verification

System-Level Design:
Behavioural Modelling & Analysis • Acceleration & Emulation • Hardware/Software Co-Design

Test:
System Test

Embedded Software Development:
Compilers • Software/Modelling

Hardware:
FPGA & Reconfigurable Platforms

Semiconductor IP:
CPUs & Controllers • On-Chip Bus Interconnect • Processor Platforms

BOOTH 5

MathWorks

3 Apple Hill Drive Natick, MA
United States

W www.mathworks.com

MathWorks is the leading developer of mathematical computing software. Engineers and scientists worldwide rely on its products to accelerate the pace of discovery, innovation, and development.

MATLAB®, the language of technical computing, is a programming environment for algorithm development, data analysis, visualization, and numeric computation. Simulink® is a graphical environment for simulation and Model-Based Design of multidomain dynamic and embedded systems. The company produces nearly 100 additional products for specialized tasks such as deep learning, computer vision, robotics, and C and HDL code generation.

MATLAB and Simulink are used throughout the automotive, aerospace, communications, electronics, and industrial automation industries as fundamental tools for research and development. They are also used for modeling and simulation in increasingly technical fields, such as financial services and computational biology. MATLAB and Simulink enable the design and development of a wide range of advanced products, including automotive systems, aerospace flight control and avionics, telecommunications and other electronics equipment, industrial machinery, and medical devices. More than 5000 colleges and universities around the world use MATLAB and Simulink for teaching and research in a broad range of technical disciplines.

ASIC and SOC Design:
Behavioural Modelling & Simulation • Verification • Analogue and Mixed-Signal Design • RF Design

System-Level Design:
Behavioural Modelling & Analysis • Hardware/Software Co-Design

Test:
System Test

Services:
Design Consultancy • Training

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Design Entry • Verification • Analogue and Mixed-Signal Design

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Design for Test

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BOOTH 16

Microtest

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System-Level Design:
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Application-Specific IP:
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BOOTH EP5

MNEMOSENE

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MNEMOSENE is an ambitious Research and Innovation Action addressing the theme "Development of new approaches to scale functional performance of information processing and storage substantially beyond the state-of-the-art technologies with a focus on ultra-low power and high performance" of the European Union's Horizon 2020 ICT research and innovation programme.

MNEMOSENE will focus on the development, design and demonstration of a Computation-In-Memory (CIM) architecture based on extending arrays of non-volatile resistive switching devices (memristors) with logic functionality inside or around the cell array. CIM architectures allow integration of information processing and storage at the same physical location, having the potential to (a) eliminate the communication and memory bottleneck, (b) support massive parallelism to increase the overall performance, (c) drastically enhance energy efficiency, and (d) be cheaper to manufacture. Development of such a radically innovative computing architecture will be a real breakthrough, enabling the solution of many computational problems in minutes rather than days at affordable energy and cost, resulting in orders of magnitude increase in performance.

Coordinated by Delft Technical University (NL), the project consortium includes eight other partners from six different countries: Eindhoven University of Technology and IMEC (NL), ETH Zurich and IBM Research – Zurich (CH), Arm (UK), RWTH Aachen University (DE), INRIA (FR) and Intelligentsia Consultants (LU).

The MNEMOSENE Project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement number 780215.

ASIC and SOC Design:
Behavioural Modelling & Simulation

System-Level Design:
Behavioural Modelling & Analysis • Acceleration & Emulation

Embedded Software Development:
Compilers

Semiconductor IP:
Memory IP • On-Chip Bus Interconnect

BOOTH 9

Research Unit: FOR1800 Controlling Concurrent Change – Towards Self-Aware Automotive And Space Vehicles

Institute of Computer and Network Engineering
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Embedded systems for safety critical and high availability applications have moved from isolated components to highly integrated mixed criticality networked systems with numerous shared resources. The resulting function interference challenges the design process, in particular in autonomous systems which shall independently manage software updates and hardware reconfigurations. With support from the German DFG, a group of 8 PIs has investigated automated integration of critical applications using self-adaptation with self-protection based on contracting and self-awareness. Applications are vehicle automation and autonomous platforms for space robotics. The DATE special session 3.8 will include a talk summarizing the Research Unit activities.

During the DATE Conference 2019, posters will highlight the architectures, methods and main achievements. Various demonstrators will illustrate the research approach and results. The demonstrators include an autonomous road vehicle controlled by self-managed software with contract-based integration and monitoring of critical functions, a collaborating mobile robot pair with dynamic hardware self-reconfiguration for operation under varying radiation stress, and a simulated group of vehicles co-operating under limited trust. The robot pair will also give a life demonstration as part of the Friday DATE Workshop on Autonomous Systems Design.

ASIC and SOC Design:
Verification

System-Level Design:
Hardware/Software Co-Design

Test:
Design for Test • System Test

Embedded Software Development:
Real Time Operating Systems • Software/Modelling

Semiconductor IP:
Embedded FPGA • Embedded Software IP

Hardware:
FPGA & Reconfigurable Platforms

Application-Specific IP:
Digital Signal Processing • Security

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BOOTH 7

SEMI

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BOOTH 10

SPP1648 Software for Exascale Computing (SPPEXA)

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The Priority Programme "Software for Exascale Computing" (SPPEXA) of the German Research Foundation (DFG) addresses fundamental research on the various aspects of HPC software, which is particularly urgent against the background that we have entered the era of ubiquitous massive parallelism. SPPEXA started in 2013 and is implemented in two three-year funding phases, with 17 project consortia and more than 40 institutions involved.

Thus,SPPEXA has joined the other national initiatives to pave the road towards exascale computing.

ASIC and SOC Design:
Power & Optimisation • Verification

System-Level Design:
Hardware/Software Co-Design

Test:
System Test

Services:
Training

Embedded Software Development:
Compilers • Software/Modelling

Hardware:
FPGA & Reconfigurable Platforms

Application-Specific IP:
Data Communication • Networking

BOOTH 4

Springer Nature

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BOOTH 15

Symbiotic EDA

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Symbiotic EDA provides training, software and support services for improving digital design productivity and functional safety. Their formal verification tools reduces the effort necessary to find and fix hard to find bugs within VHDL, Verilog, or SystemVerilog designs.

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EP 1

TETRAMAX

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The mission of the EU-funded TETRAMAX innovation action is to build on three activity lines in the domain of Customized Low-Energy Computing (CLEC) for Cyber-Physical Systems and the Internet of Things: (1) stimulating, co-funding, and evaluating different cross-border Technology Transfer Experiments (TTX) via innovative CLEC technologies to first-time users and broad markets in European ICT industries, (2) building and leveraging a new European CLEC competence center network, offering technology brokerage, one-stop shop assistance and CLEC training to SMEs and mid-caps, with a clear path towards new regional Digital Innovation Hubs (DIH), and (3) paving the way towards self-sustainability.

Within the framework of a variety of open calls for application of TTX, the immediate ambition of TETRAMAX is to support 50+ industry clients all over Europe with innovative technologies, leading to an estimated revenue increase of €25m based on 50+ new or improved CLEC-based products, 10+ entirely new businesses/SMEs initiated, as well as 30+ new permanent jobs and significant cost savings in product manufacturing. Being the leading European DIH for CLEC, TETRAMAX will accelerate digitalization within European industries. In the long term, TETRAMAX will be the trailblazer towards a reinforced and sustainable ecosystem infrastructure, providing CLEC competence, services and a continuous innovation stream at European scale, yet with strong regional presence as preferred by SMEs.

The TETRAMAX project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement number 761349.

ASIC and SOC Design:
Power & Optimisation

System-Level Design:
Hardware/Software Co-Design

Services:
Design Consultancy • Prototyping • Training

BOOTH 1

University Booth

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The University Booth fosters the transfer of academic work to industry. The University Booth is part of the DATE 2019 exhibition and is free of

charge for presenters and their visitors. The University Booth is sponsored by the DATE Sponsor's Committee. The University Booth will be organized for EDA software and hardware demonstrations. Universities and public research institutes are invited to present innovative hardware and software demonstrations. All demonstrations will be hosted in the DATE exhibition area, within a dedicated time slot.

Research institutes and universities interested in demonstrating their mature prototypes and pre-commercial results can find submission details at https://www.date-conference.com/exhibition/u-booth.

The final programme of the University Booth is available online at https://www.date-conference.com/exhibition/ub-programme.

The University Booth is organized by the University Booth Co-Chairs
Elena Ioana Vatajelu, TIMA, FR
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Design Entry • Behavioural Modelling & Simulation • Synthesis • Power & Optimisation • Physical Analysis (Timing, Themal, Signal) • Verification • Analogue and Mixed-Signal Design • MEMS Design • RF Design

System-Level Design:
Behavioural Modelling & Analysis • Physical Analysis • Acceleration & Emulation • Hardware/Software Co-Design • Package Design • PCB & MCM Design

Test:
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Application-Specific IP:
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D12 Logical and Physical Analysis and Design
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Co-Chair: Elena Dubrova, Royal Institute of Technology - KTH, SE

D13 Emerging Design Technologies for Future Computing
Chair: Aida Todri-Sanial, CNRS-LIRMM/University of Montpellier, FR
Co-Chair: Subhasish Mitra, Stanford University, US

D14 Emerging Design Technologies for Future Memories
Chair: Jean-Michel Portal, Aix-Marseille University, FR
Co-Chair: Pierre-Emmanuel Gaillardon, University of Utah, US

A1 Power-efficient and Sustainable Computing
Chair: Muhammad Shafique, Vienna University of Technology (TU Wien), AT
Co-Chair: Baris Aksanli, San Diego State University, US

A2 Robotics and Industry 4.0
Chair: Paolo Fiorini, University of Verona, IT
Co-Chair: Torsten Kroeger, Karlsruhe Institute of Technology, DE

A3 Automotive Systems and Smart Energy Systems
Chair: Davide Brunelli, University of Trento, IT
Co-Chair: Sebastian Steinhorst, TUM, DE

TECHNICAL PROGRAMME TOPIC CHAIRS

A4
Augmented Living and Personalized Healthcare
Chair: Theocharis Theocharides, University of Cyprus, CY
Co-Chair: Elisabetta Farella, Fondazione Bruno Kessler (FBK), IT

A5
Secure Systems, Circuits and Architectures
Chair: Ingrid Verbauwhede, KU Leuven - COSIC, BE
Co-Chair: Lionel Torres, University of Montpellier, FR

A6
Self-adaptive and Learning Systems
Chair: Antonio Miele, Politecnico di Milano, IT
Co-Chair: Gilles Sassatelli, LIRMM CNRS / University of Montpellier 2, FR

A7
Applications of Emerging Technologies
Chair: Andy Tyrrell, University of York, GB
Co-Chair: Yu Wang, Nanjing University of Posts and Telecommunications, CN

A8
Industrial Experiences Brief Papers
Chair: Fabien Clermidy, CEA-Leti, FR
Co-Chair: Norbert Wehn, University of Kaiserslautern, DE

T1
Modeling and Mitigation of Defects, Faults, Variability, and Reliability
Chair: Said Hamdioui, Delft University of Technology, NL
Co-Chair: Jose Pineda, NXP Semiconductors, NL

T2
Test Generation, Test Architectures, Design for Test and Diagnosis
Chair: Patrick Girard, LIRMM, FR
Co-Chair: Bernd Becker, University of Freiburg, DE

T3
Microarchitecture-Level Dependability
Chair: Jaume Abella, Barcelona Supercomputing Center (BSC-CNS), ES
Co-Chair: Ramon Canal, UPC, ES

T4
System-Level Dependability
Chair: Maria K. Michael, Electrical and Computer Engineering & KIOS Center of Excellence, University of Cyprus, CY
Co-Chair: Georgios Karakonstantis, Queen's University Belfast, GB

DT5
Design and Test for Analog and Mixed-Signal Circuits and Systems and MEMS
Chair: Georges Gielen, KU Leuven, BE
Co-Chair: Francisco V. Fernandez, IMSE-CNM, CSIC and Univ. Sevilla, ES

DT6
Design and Test of Secure Systems
Chair: Ilia Polian, University of Stuttgart, DE
Co-Chair: Lejla Batina, Radboud University Nijmegen, NL

E1
Real-time and Dependable Systems
Chair: Kai Lampka, Electrobit Automotive GmbH, DE
Co-Chair: Dionisio de Niz, Carnegie Mellon University, US

E2
Embedded Systems for Deep Learning
Chair: Akash Kumar, Technische Universität Dresden, DE
Co-Chair: Sander Stuijk, Eindhoven University of Technology, NL

E3
Model-Based Design, Verification and Security for Embedded Systems
Chair: Ylies Falcone, University of Grenoble Alpes, Inria, FR
Co-Chair: Todd Austin, University of Michigan, US

E4
Embedded Software Architecture, Compilers and Tool Chains
Chair: Borzoo Bonakdarpour, Iowa State University, US
Co-Chair: Eli Bozorgzadeh, University of California, Irvine, US

E5
Cyber-Physical Systems Design
Chair: Shiyan Hu, Michigan Technological University, US
Co-Chair: Davide Quaglia, University of Verona, IT

DETAILED INDEX

Scope of the Event

The 23rd DATE conference and exhibition is the main European event bringing together designers and design automation users, researchers, and vendors, as well as specialists in hardware and software design, test, and manufacturing of electronic circuits and systems. DATE puts strong emphasis on both technology and systems, covering ICs/SoCs, emerging technologies, embedded systems, and embedded software.

Structure of the Event

The five-day event consists of a conference with plenary invited papers, regular papers, panels, hot-topic sessions, tutorials, workshops, special focus days, and a track for executives. The scientific conference is complemented by a commercial exhibition showing the state-of-the-art in design and test tools, methodologies, IP and design services, reconfigurable and other hardware platforms, embedded software, and (industrial) design experiences from different application domains, such as automotive, wireless, telecom and multimedia applications. The organization of user group meetings, fringe meetings, a university booth, a PhD forum, vendor presentations and social events offers a wide variety of extra opportunities to meet and exchange information on relevant issues for the design automation, design, and test communities. Special space will also be allocated for EU-funded projects to show their results.
More details are given on the DATE website: www.date-conference.com.

CONFERENCE & EXHIBITION
09—13 March 2020
Alpexpo, Grenoble, France

Areas of Interest

Within the scope of the conference, the main areas of interest are: embedded systems, design methodologies, EDA algorithms and tools, testing of electronic circuits and systems, embedded software, application design, and industrial design experiences. Topics of interest include, but are not restricted to:

- System Specification and Modeling
- System Design, Synthesis, and Optimization
- Simulation and Validation
- Design of Low Power Systems
- Power Estimation and Optimization
- Green Computing Systems and Applications
- Temperature-Aware Design
- Temperature Modeling and Management
- Emerging Technologies for Computing Systems
- Emerging Memory Technologies and Applications
- Formal Methods and Verification
- Network-on-Chip
- Architectural and Microarchitectural Design
- Reconfigurable Computing
- Physical Design and Verification
- Analog and Mixed-Signal Circuits and Systems
- Interconnect and Packaging Modeling
- Communication, Consumer, and Multimedia Systems
- Transportation Systems
- Medical, Healthcare, and Assistive Technology Systems
- Energy Generation, Recovery, and Management Systems
- Secure Systems
- Reliable and Dependable Systems
- Test for Defects, Variability, and Reliability
- Test Generation, Simulation, and Diagnosis
- Test for Mixed-Signal, Analog, RF, MEMS
- Test Access, Design-for-Test, Test Compression, System Test
- On-Line Testing and Fault Tolerance
- Real-time and Networked Systems
- Compilers and Code Generation for Embedded Systems
- Model-based Design and Verification for Embedded Systems
- Embedded Software Architectures and Principles
- Software and Optimization for MPSoCs, Many-core, GPU-based, or Heterogeneous Systems

Submission of Papers

All papers have to be submitted electronically by Sunday, 8 September 2019, via: www.date-conference.com

Papers can be submitted either for standard oral presentation or for interactive presentation. The Program Committee also encourages proposals for Special Sessions, Tutorials, Friday Workshops, University Booth, PhD Forum and Exhibition Theatre.

Chairs

General Chair: Giorgio Di Natale, CNRS/TIMA, FR
giorgio.di-natale@univ-grenoble-alpes.fr

Programme Chair: Cristiana Bolchini, Politecnico di Milano, IT
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Conference Organization

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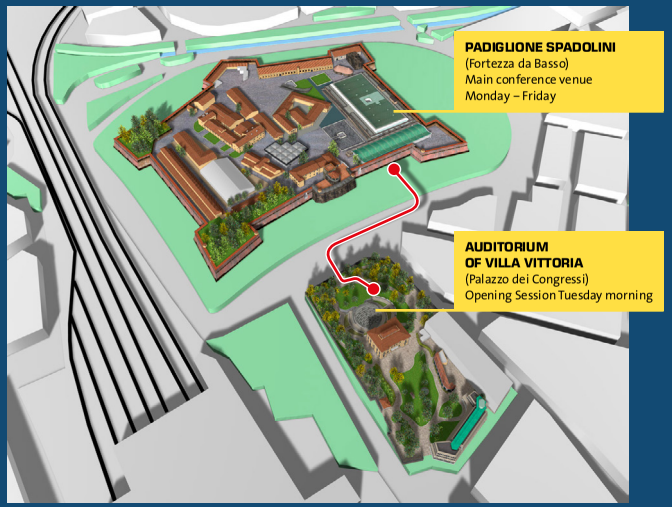
VENUE PLAN

Overview of Firenze Fiera



Walk between Auditorium and main conference venue

Padiglione Spadolini, Lower Floor