STDN RANGING EQUIPMENT

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FINAL REPORT

Prepared for

GODDARD SPACE FLIGHT CENTER

Greenbelt, Maryland 20771

1. Report No.	2. Government Accession No.	3. Recipient's Catalog No
4. Title and Subtitle STDN RANGING EQUIPMENT Final Report		5. Report Date December 1975 6. Performing Organization Code
7. Author(s) C. E. Jones, et al.		8. Performing Organization Report No. R-75-074
9. Performing Organization Name and Address General Dynamics Electronics Division P.O. Box 81127 San Diego, California 92138		10. Work Unit No 11. Contract or Grant No 13. Type of Report and Period Covered Final Report
12. Sponsoring Agency Name and Address Goddard Space Flight Center Greenbelt, Maryland 20771 F. W. Herold, Code 813.3		14. Sponsoring Agency Code

15. Supplementary Notes

16. Abstract

The final results of the STDN Ranging Equipment program are summarized. Basic design concepts and final design approaches are described. Theoretical analyses which define requirements and support the design approaches are presented. Design verification criteria are delineated and verification test results are specified.

17. Key Words	18. Distribution Statement		
Doppler Range and Range Rate CW Tracking			
19. Security Classif. (of this report) Unclassified	20. Security Classif. (of this page) Unclassified	21. No of Pages	22. Price

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1. INTRODUCTION

The STDN Ranging Equipment operates in conjunction with other ground station equipment to provide precision range and doppler measurements for a wide variety of spaceborne vehicles. Operating with vehicles carrying an S-band phase-locked transponder, the Ranging Equipment provides unambiguous range data at distances greater than 500,000 kilometers, and nondestructive doppler data for carrier doppler frequencies up to 230 kHz. The system is designed for vehicle dynamics of over 15,000 meters/sec and 150 meters/sec/sec. The ranging system employes sinusoidal modulation and extremely narrowband processing techniques to provide high accuracy range data with low received signal strength.

2. DESIGN SUMMARY

2.1 SYSTEM OBJECTIVES

The Ranging Equipment (RE) described provides the NASA Spaceflight Tracking and Data Network (STDN) with precision ranging and carrier doppler measurement capability for spacecraft. This equipment provides ranging determination for spacecraft up to greater than 500,000 kilometers and data for range rate determination for S-band carrier doppler shifts up to ±230 kHz corresponding to range rates up to 15,300 meters/sec.

The equipment:

- Provides range data to an accuracy of 1.0 meter rms with a resolution of 0.15 meter
- Provides nondestructive carrier doppler data to an incremental accuracy of 0.01 cycles rms with a resolution of 0.001 cycles
- Provides rapid automatic acquisition
- Provides display of range and doppler data
- Provides self-test features for calibration and maintenance
- Is fully compatible with existing and planned spaceborne and ground-based equipment

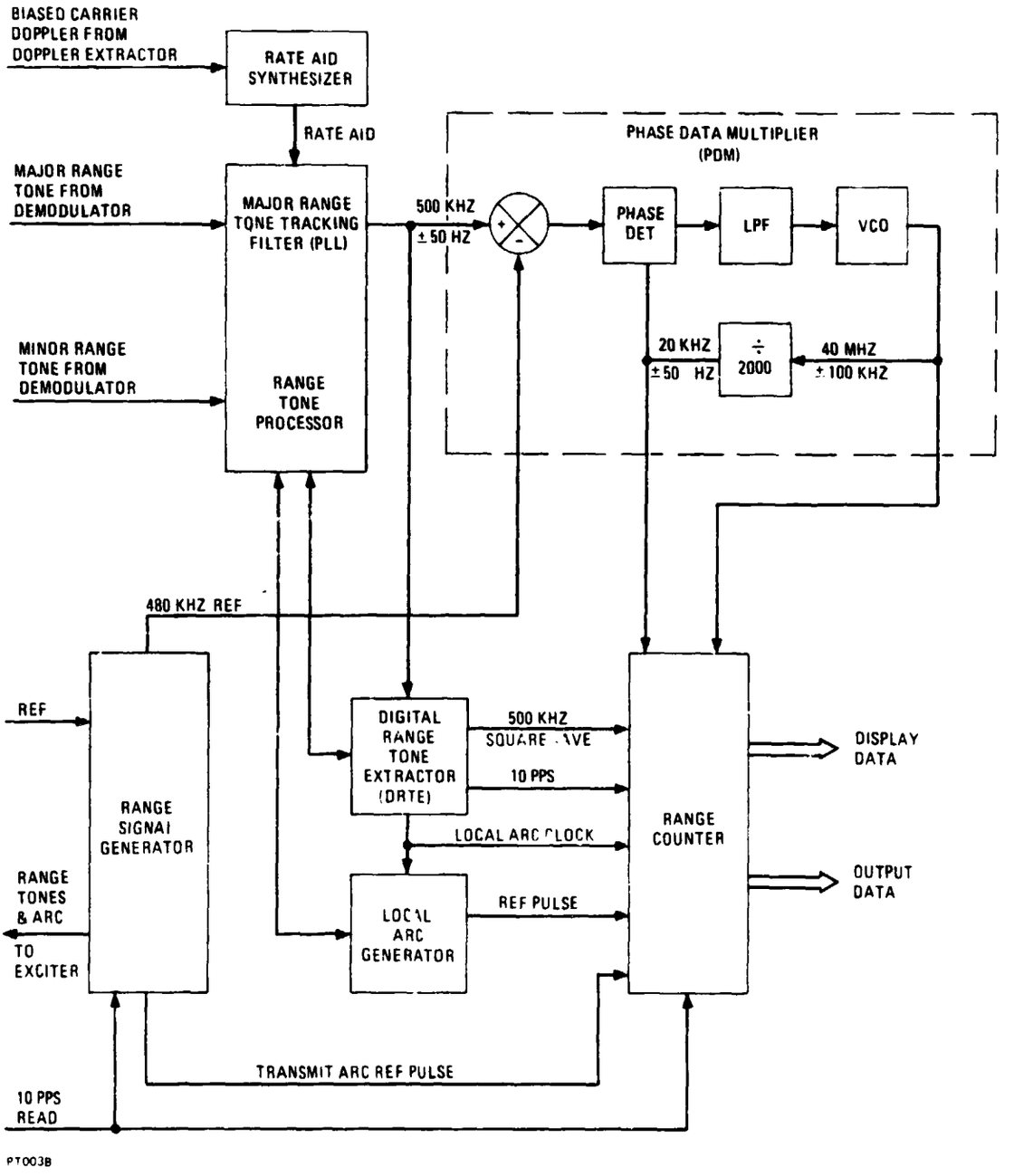

Figure 2.2.1-1. Ranging Equipment, Range Measurement Concept.

2.2 MEASUREMENT CONCEPTS

2.2.1 RANGE

The ranging system (Figure 2.2.1-1) employs a harmonic tone waveform, combined with an ARC (Ambiguity Resolving Code), and uses phase delay measurement techniques for range determination. Each output range value is independent of previous values and is an unambiguous measure of total phase delay in units nominally equal to 0.15 meter. Each output range value corresponds to the instantaneous phase delay of the major range tone at the time specified by the output data time tag within ±25 nanoseconds. (Major range tone signal flow is further illustrated in Figure 4.7.2-1.*)

Rate aid signals, derived from the carrier doppler, are used by the major range tone tracking circuits to:

- Minimize initial phase lock acquisition time
- Minimize loop phase lag errors due to signal dynamics
- Allow use of very narrow bandwidths to reduce receiver noise errors.

Minor range tones and digital phase matching techniques are employed for resolving cyclic ambiguities of the major range tone. A pseudo-random ARC is employed for resolving ambiguities of the lowest frequency (10 Hz) minor range tone. The minor range tones or the ARC subcarrier are used to modulate the carrier during the range ambiguity resolving process, but all baseband power is concentrated in the major range tone during the period of accurate ranging after ambiguities are resolved.

A third-order PLL (phase lock loop) is used as a tracking filter for the major range tone. A rate aid signal is supplied to the PLL to permit the use of a very narrow loop bandwidth without causing excessive lag error due to signal dynamics.

The rate aid signal is generated by a rate aid synthesizer using a biased carrier doppler signal and system reference signals. The input/output doppler ratio of the rate aid synthesizer is selectable to provide sufficiently accurate rate aid over the assigned range of carrier frequencies.

The phase difference between the transmitted range tone and the filtered output of the PLL at 500 kHz is translated to 20 kHz for fine phase measurement using a PDM (Phase Data Multiplier).

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*For convenience bound in Appendix A.

The instantaneous phase difference between the 20 kHz reference and data signals is contained in the +2000 scaler in the PDM at the time of axis crossing of the 20 kHz reference signal. For actual data output, however, this instantaneous phase data is obtained through a separate +2000 counter which is synchronized to the 20 kHz PDM input signal.

The scaler count is read out to a buffer to be formatted for display and for external use. Phase delay is obtained as the ratio of the incremental count m, divided by the counts per cycle M, and is directly convertible to time delay as:

$$t_v = T\ (m/M)$$

Where:

t_v = Vernier time delay value

$T = 2 \times 10^{-6}$ sec, the period of the 500 kHz range tone

m = Count value

M = 2000, the counter scaling ratio

The range increment size is given by T/M and is 1 nanosecond (nominally 0.15 meter).

A count of integer cycles of phase delay of the 500 kHz range tone is obtained by readout, at 10 pps, of the contents of a +50,000 counter which operates on the 500 kHz square wave used in the Digital Range Tone Extractor (DRTE) and which resets at a 10 pps rate in synchronism with the DRTE.

The ambiguity interval of the delay data is extended beyond 0.1 second (correspond to the 10 Hz range tone) by readout of the difference in phasing of the transmitted and local Ambiguity Resolving Codes.

The combination of whole cycle count and incremental cycle count is provided in one output data word which gives a round-trip range tone delay value with a resolution (increment size) of 1 nanosecond and which is unambigiou to 6.3 seconds (approximately 959,000 km).

Each output is "on time" and independent of all other sampled range values.

2.2.2 DOPPLER

The doppler data system counts incremental cycles of carrier doppler (in 0.001 cycle increments) and provides a non-destructive on-time readout of the

instantaneous accumulated count. This provides non-destructive doppler data with a uniform 0.1 second sampling interval. Doppler counts can be continuously accumulated for 156 minutes at the maximum doppler.

The doppler data system (Figure 2.2.2-1) accepts an arbitrarily biased doppler signal from the MFR (together with reference signals from the exciter and MFR synthesizer and from the system frequency standard) and provides an output doppler signal with a 70 MHz bias. This output-bias-plus-doppler signal is translated to a 1.0 MHz bias frequency and then tracked by a phase lock loop which acts as phase data multiplier. The resultant bias-plus-multiplied-doppler signal, which is available at the input of the ÷250 counter in the PDM feedback circuit, is then translated to a new bias frequency at two phases separated 90°. The two phases of the 60 MHz ±57.5 MHz data signal are then employed in a high-speed counter for readout and display. The two different phases allow digitizing in 1/4-cycle increments. This 1/4-cycle incrementing coupled with the prior multiplication by 250 provides an overall resolution (increment size) of 0.001 cycle of the input data. (Total overall system frequency coherence and signal flow is further illustrated in Figure 4.1-1.)

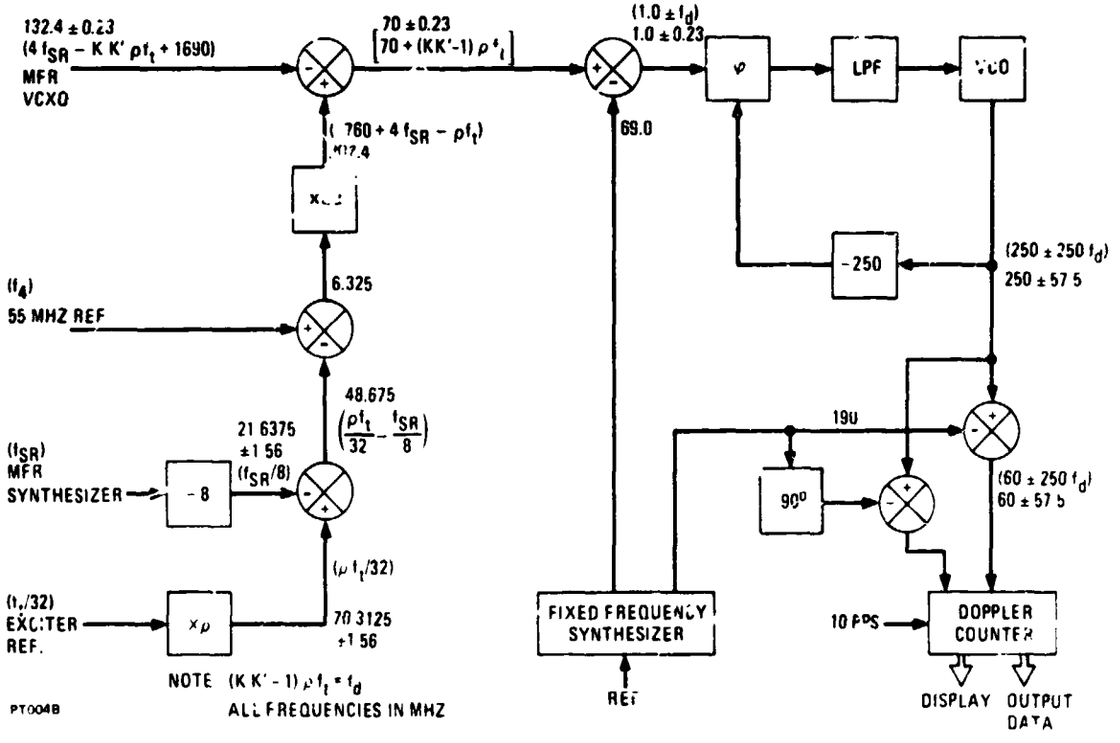

Figure 2.2.2-1. Doppler Measurement Concept

2.3 SIMPLIFIED FUNCTIONAL DESCRIPTION

Utilizing the measurement principles described previously, the STDN Ranging Equipment has been configured into a system as shown in Figure 2.3-1.* This system is basically comprised of the following functions:

- Fixed Frequency Synthesizer
- Range Measurement
- Doppler Measurement
- Test Simulator
  - Range Simulator
  - Doppler Simulator
- Interface/Control

These functions are described below; a detailed description of the implementation of these functions is given in Paragraph 3.2.

2.3.1 FIXED FREQUENCY SYNTHESIZER

The 5.0 MHz station frequency standard in the Station Timing System is used to derive all the reference signals required within the Ranging Equipment. The 40 MHz output from the Fixed Frequency Synthesizer is used to generate the range tones and also a 400 KHz reference signal from the Modulation Combiner. The reference signals generated within the Fixed Frequency Synthesizer are used to derive both range and doppler data and also to provide the synthetic signals for simulation of the equipment. Using 5 MHz station frequency standard to derive both the reference frequencies and range tones provides frequency coherence with the Station Equipment.

2.3.2 RANGE MEASUREMENT

The range measurement equipment which is essentially the equipment on the left-hand side of the block diagram (Figure 2.3-1), performs two basic functions:

- Range Signal Generation
- Range Determination

The 10 pps timing pulse from the Station Timing System is used to synchronize these functions.

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*For convenience bound in Appendix A.

2.3.2.1 RANGE SIGNAL GENERATION — The range signal generation equipment, comprised of the Range Tone Generator, Transmit Ambiguity Resolving Code (ARC) Generator and Modulation Combiner, produces the signals and the modulation waveform to the Station Exciter necessary for the unambiguous measurement of range.

From the 40 MHz reference signal the Range Tone Generator derives the major range tones at 500 kHz, 100 kHz, and 20 kHz; the minor range tones at 4 kHz, 800 Hz, 160 Hz, 40 Hz, and 10 Hz; and generates a separate 500 kHz and 100 kHz signal used in the Modulation Combiner to provide a 400 kHz reference signal. The 10 pps signal from the Station Timing System is used to synchronize a data read-out control within the Range Tone Generator and distributed to the Transmit ARC Generator, the Range Counter and Doppler Counter.

The ARC Generator provides 1023 bit pseudo-random code sequence at 160 bits per second. It provides an output pulse at the start of each transmitted ARC cycle for synchronization of the Range Counter and provides a 10 pps signal to the Local ARC Generator for its synchronization.

The Modulation Combiner performs the functions of:

1. Complementing all minor tones below 4 kHz onto the 4 kHz
2. Modulation of the 4 kHz tone, when required, with the pseudo-random ARC
3. Combining selected range tones and/or the subcarrier for use by the exciter to modulate the transmitted carrier
4. Generation of a 160 Hz ARC clock signal
5. Generation of a 400 kHz reference signal.

2.3.2.2 RANGE DETERMINATION — From modulation present on the Multi-Function Receiver (MFR) 110 MHz intermediate frequency signal, target range is determined, displayed on the Ranging equipment console, and transmitted in a 32 bit format to the Station Tracking Data Formatter. The Range Demodulator, Rate Aid Synthesizer, Range Tone Processor, Phase Data Multiplier, Digital Range Tone Extractor (DRTE), Local ARC Generator, and Range Counter make this determination.

The Range Demodulator is used to demodulate and level control the major tones, minor tones, complemented minor tones and ARC modulated 4 kHz subcarrier as received from the IF signal of the MFR. Level control is accomplished using a coherent AGC technique (based on the major range tone power derived in the Range Tone Processor) with gain adjustment performed prior to demodulation.

The function of the Rate Aid Synthesizer is to develop signals which consist of a bias frequency plus approximate major range tone doppler for the Range Tone Processor. These signals are developed by dividing the extracted carrier doppler (from Doppler Extractor) by a number approximately equal to the frequency ratio of the received carrier to the range tone frequency. This is used to cancel the frequency dynamics on the received major tones, thereby allowing the use of very narrowband tone tracking filters with small lag errors due to doppler dynamics. This unit also provides a 500 kHz rate aided signal for range simulation purposes.

The Range Tone Processor (RTP) performs all analog operations associated with acquisition and tracking of the ranging signals. The RTP receives the combined ranging signals from the Range Demodulator and controls the acquisition and tracking of these signals using signals generated in the DRTE and the Local ARC Generator. The RTP employs a rate-aided PLL in tracking the received major range tone and produces a 500 kHz output signal for use by the Phase Data Multiplier, the DRTE, and the Range Counter.

The DRTE uses the input 500 kHz tone in the synthesis of the lower frequency range tones and the 160 pps as a clock for the Local ARC Generator. Phasing of the synthesized signals is controlled by the DRTE to obtain a phase match between the synthesized and received signals. The DRTE produces a 10 pps signal which is synchronous with the simultaneous axis crossings of the synthesized range tones. A reset signal is produced and is used to synchronize the reset of both the Local and Transmit ARC Generators.

The Local ARC Generator uses the 160 pps clock from the DRTE in producing a replica of the transmitted ARC. The timing of the synthesized ARC is controlled by a signal from the Transmit ARC. An output reference pulse to the Range Counter is produced at the start of each local ARC cycle.

The Phase Data Multiplier translates the phase difference between the data and reference 500 kHz range tones to a set of data and reference 20 kHz signals and multiplies the resultant data signal phase and frequency by 2000. The resultant 40 MHz signal is used in the Range Counter to obtain a 500 kHz range tone phase delay resolution of 1/2000 of a cycle.

The Range Counter generates output range values using clock and reference pulses supplied by the PDM and DRTE and by the Transmit and Local ARC Generators. The data output to the Tracking Data Formatter is a 32-bit binary word, while the output to the operation control panel display is an 10-character BCD word. A 10 pps signal is also sent to the Tracking Data Formatter to indicate the period of valid data taking.

2.3.3 DOPPLER MEASUREMENT

The doppler measurement is performed by the Doppler Extractor, Doppler Multiplier, and Doppler Counter. Doppler data is derived from the selected "best" VCXO signal from the Multi-Function Receiver. This data is transmitted as 42 bit binary information to the Tracking Data Formatter and is also displayed on the operating console of the Ranging Equipment.

The Doppler Extractor and VCO Select are shown separately on the Functional Block Diagram (Figure 2.3-1) for clarity in explaining their functions. The VCO Select logic compares the AGC from both channels of the MFR and selects the strongest VCO signal. The MFR lock signal is used as an inhibit signal in the VCO select logic in the event that the MFR-VCO signal selected is not in a lock mode. The Doppler Extractor utilizes the selected VCO signal, the synthesizer signal (160.6-185.6 MHz) from the MFR and a multiple of the Exciter transmitted frequency ($F_T/32$ = 63.3-66.2 MHz) to produce a "bias-plus-doppler" signal at 70 ± 0.23 MHz. This "bias-plus-doppler" signal is used by the Rate Aid Synthesizer as described in the previous section.

The Doppler Multiplier takes the 70 MHz signal, and using 190 MHz and 69 MHz reference signals produces a new "bias-plus-multiplied-doppler" at 60 MHz ± 57.5 MHz. The signal is sent to the Doppler Counter in two phases separated 90°. This phasing of the signal permits the Dopper Counter to provide an increment size of 1/4-cycle of multiplied doppler.

The Doppler Counter continuously accumulates a count of axis crossings of the bias-plus-multiplied-doppler signal and provides a 10 per second readout of the instantaneous cumulative count, including the residual 1/4-cycle increments. This provides a combined increment size of 0.001 cycle of the input doppler. The data output for external use by the Tracking Data Formatter is a 42-bit binary word. A separate output data word is provided for decimal display of the count accumulated in a 0.1 second interval. The display is updated once every 0.4 seconds.

2.3.4 TEST SIMULATOR

The simulator, containing a doppler simulator and a Range Simulator, provides test signals for exercising the Ranging Equipment to verify proper operation. The Ranging Equipment can be configured, in conjunction with the Test Simulator, to check operation of all components of the Doppler Data Extractor and the Range Extractor. Table 2.3.4-1 lists the operating and test modes with mode identification numbers.

The Doppler Simulator generates a set of signals for use in the Doppler Extractor. Appropriate combinations of these signals and signals from the RE interface are

Table 2.3.4-1. Ranging Equipment Test and Operate Modes

MODE NUMBER	MODE FUNCTION
1	NORMAL OPERATE
2	BYPASS SIMULATE
a.	Doppler and Dynamic Range Test
b.	Doppler or Static Range Test
3	NORMAL SIMULATE
a.	Doppler and Dynamic Range Test
b.	Doppler or Static Range Test

selected for use in the Doppler Extractor for each mode listed in Table 2.3.4-1. Signal connections within the Doppler Simulator and Doppler Extractor are changed as required to obtain the several test modes.

The Range Simulator, comprised of the Simulation Range Signal Generator and Test Modulator, generates a set of ranging signals (range tones and ARC) identical to those produced by Range Signal generation (Paragraph 2.3.2), but with selectable static or dynamic delay. Its output signal is equivalent to the output 110 MHz carrier of the Multi-Function Receiver.

The Rate Aid Synthesizer provides an auxiliary output which provides a source of properly scaled dynamics for the ranging signals.

2.3.5 INTERFACE/CONTROL

The Interface/Control logic circuitry is used to transfer commands from the Station Computer to the Ranging Equipment and to command verification and status monitoring from the Ranging Equipment to the computer. The Interface/Control logic also provides Ranging Equipment status to the Tracking Data Formatter. Table 2.3.5-1 defines the command and control signals from the computer in addition to the other station equipment signals used by the Ranging Equipment. Table 2.3.5-2 defines the signals from the ranging equipment to the station equipment.

Table 2.3.5-1. Station Equipment Signals to Ranging Equipment

SIGNAL	FROM	TO	CHARACTERISTICS	REMARKS
Reference	Timing System	Rate Aid Synthesizer, Doppler Multiplier, Fixed Frequency Synthesizer	5 MHz. 0.7 Vrms into 50 ohm load. Stability ~ 1 in 10^9	Basic Timing Signal for Ranging Equipment
Reference	Timing System	Range Tone Generator	10 PPS "1" = 0 ± 0.5V 80 msec "0" = -6 ± 0.5V 20 msec Risetime ~ 10 nanosec Stable within 5 nanosec "On-Time" ~ positive going edge of pulse	Timing Signal for sampling range and doppler data
Exciter Ready	Exciter	Control Logic	Standard Logic Level	Used to inhibit modulation signal to Exciter
Transmit Frequency Reference	Exciter	Doppler Extractor	Ft/32 = 63.28 ± 66.25 MHz Level: 0 dBm ± 2 dB into 50 ohms	
Reference	MFR	Doppler Extractor	55 MHz Level: -12 dB into 50 ohms	Not used - Signal generated within Fixed Frequency Synthesizer
IF	MFR	Range Demodulator	110 MHz Level: -83 dBm ± 2 dB into 50 ohms	Carrier for range tones
AGC - 1	MFR	Doppler Extractor	Level: 0 to ±8Vdc into 1000 ohms 0V = strong signal condition	Used for selection of VCXO
AGC - 2	MFR	Doppler Extractor	See above	See above
VCXO-1	MFR	Doppler Extractor	Freq: 132.4 MHz (nom) Level: +4 dBm ± 2 dB into 50 ohms	Used for S-band doppler extraction
VCXO-2	MFR	Doppler Extractor	See above	See above
Synthesizer Output	MFR	Doppler Extractor	Freq. Range: 160.6 to 185.6 MHz. in 2.5 kHz steps Level: +4 dBm ± 2 dB into 50 ohms	Represents 400-500 MHz if tuning range of receiver in 10 kHz steps
Lock - 1	MFR	Doppler Extractor	Standard Logic Level	Indicates lock status of receiver secondary phase lock loops
Lock -2	MFR	Doppler Extractor	Standard Logic Level	See above
Resolution Tone Select	Computer	Control Logic	Standard Logic Level	Selects major tone
Start/Reset	Computer	Control Logic	Standard Logic Level	To enable ranging acquisition
Modulation ON/OFF	Computer	Control Logic	Standard Logic Level	Used in series with "Exciter Ready" to inhibit output to Exciter
One-Way/Two-Way Doppler	Computer	Control Logic	Standard Logic Level	Indication only

Table 2.3.5-2. Ranging Equipment Signals to Station Equipment

SIGNAL	FROM	TO	CHARACTERISTICS	REMARKS
Tone Modulation	Modulation Combiner	Exciter	Level 0 to 4V p to p cont. adjustable, into 50 ohms	4 volts corresponds to 3 radians phase deviation of Exciter
Resolution Tone Selected	Modulation Combiner	Computer	Dry, 1/2 amp closure	Status indication regardless of LOCAL or COMPUTER Control
Start Initiated	Control Logic	Computer	Dry, 1/2 amp closure	Status indication regardless of LOCAL or COMPUTER Control
Modulation ON/OFF	Control Logic	Computer	Dry, 1/2 amp closure	
ARC Use/Bypass	Control Logic	Computer	Dry, 1/2 amp closure	
ONE Way/Two Way Doppler Selected	Control Logic	Computer	Dry, 1/2 amp closure	
Local/Computer Selected	Data Processor Control Panel	Computer	Dry, 1/2 amp closur	
Range Acquired	Range Counter	Computer	Dry, 1/2 amp closure	
RF Ready	Control Logic	Computer	Dry, 1/2 amp closure	Status indication regardless of LOCAL or COMPUTER Control
Range Data	Range Counter	Tracking Data Formatter	32 bits Standard Logic Level	
Range Granularity (500/100/20 kHz)	Control Logic	Tracking Data Formatter	2 bits Standard Logic Level	Shows position of Resolution Tone Selector Switch
Range Acquired	Control Logic	Tracking Data Formatter	1 bit Standard Logic Level	Bit is set when all tones have been acquired and first range word is ready for outputting; also required by Computer
Modulation ON/OFF	Control Logic	Tracking Data Formatter	1 bit Standard Logic Level	Information also required by Computer
Doppler Data	Doppler Counter	Tracking Data Formatter	42 bits Standard Logic Level	
Doppler Good/Bad	Control Logic	Tracking Data Formatter	1 bit Standard Logic Level	Bit is set when MFR Lock -1, -2 signal received and Counter is ready to output. Bit shall appear on 6 separate pins
One Way/Two Way Doppler Selected	Control Logic	Tracking Data Formatter	1 bit Standard Logic Level	Set by position of One-Way/Two-Way Selector Switch
VCO Change/Doppler Bad	Doppler Extractor	Tracking Data Formatter	1 bit Standard Logic Level	Must be displayed for 100 milliseconds from time of fault. Bits shall appear on 6 separate pins
Bias plus Doppler	Doppler Multiplier	Tracking Data Formatter	1.0 ± 0.23 MHz	Temporary usage to satisfy interim station configuration
Data Available	Range Counter	Tracking Data Formatter	10 pps	Indicates period of valid data

2.4 SYSTEM OPERATION

2.4.1 OPERATIONAL CHARACTERISTICS

2.4.1.1 RANGE MEASUREMENT — Range measurement is performed using a hybrid ranging technique that employs side-tones and a pseudo-random binary-encoded ambiguity resolving code. The available ranging tones are: 500 kHz, 100 kHz, 20 kHz, 4 kHz, 800 Hz, 160 Hz, 40 Hz, and 10 Hz.

Any one of the three highest available tones may be selected as the major tone used to obtain range data resolution. During ranging operations, the selected major tone is transmitted continuously and the lower tones are sequentially applied to resolve range ambiguities. For transmission, the 800 Hz tone is complemented on the high side of the 4 kHz and thus becomes 4.8 kHz. The three lowest tones are transmitted double sideband-suppressed carrier using the 4 kHz tone as a subcarrier. This eliminates modulation components close to the carrier which could degrade carrier acquisition and tracking. The lowest sidetone (10 Hz) gives an ambiguity interval of 0.1 sec, approximately 15,000 kilometers.

An ambiguity resolving code (ARC) having a length of 1023 bits is bi-phase modulated on the 4 kHz tone. The code bit rate of 160/sec gives a code period of 6.39375 seconds, corresponding to an unambiguous range of approximately 958,000 kilometers. However, the range word readout size of 32 bits limits the maximum range readout to 644,000 km.

Ranging signal delay is measured with a time increment size of 1 nanosecond corresponding to an approximate range increment size of 0.15 meter.

2.4.1.2 DOPPLER MEASUREMENT — Doppler measurement consists of a periodic readout (10/sec) of a continuously accumulated count of cycle increments of a doppler-plus-bias signal. Frequency translation and multiplication, provide a resolution of 1000 increments per cycle of extracted-carrier doppler.

2.4.1.3 RATE AIDED TRACKING — Rate-aided tracking is used to permit the using of a narrow bandwidth range tone tracking PLL with severe signal dynamics. A rate-aid signal is synthesized from the extracted doppler-plus-bias signal with a fractional error of 1 part in 17,600, or less. As a result, the PLL bandwidth can be very narrow to minimize noise error in the output range data without incurring excessive lag error for range acceleration magnitudes of 150 meter/sec^2 or less.

2.4.1.4 ACQUISITION PROCESS CONTROL — The acquisition process requires phase lock and amplitude lock to the major range tone, the successive application of minor range tones and the ARC to modulate the up-link carrier, and matching the locally generated counterpart signals to the returned modulation signal.

The process is initiated after receipt of exciter ready status from the Exciter and a phase lock status from the MFR.

The operator can select options for controlling the sequence of steps and the integration time for each correlation of local and returned signals. The selectable options are: 1) automatic, operator, or computer control of the sequence of application of tones and ARC; and 2) automatic or operator control of integration time (and the resultant adjustment) for each correlation.

2.4.1.5 SIMULATION — The Test Simulator provides the means for exercising the doppler and range data extraction functions of the Ranging Equipment. A static value of range can be inserted at the control panel for a check of range output data for normal signal routing or with the transmitter/transponder/receiver path by-passed.

In addition, a doppler value can be inserted at the control panel for a check of doppler output data. The resultant extracted doppler signal can be used in the Range Simulator to obtain coherently related doppler data and change of the range data. In this mode, a dynamic range is simulated. This can also be accomplished either in conjunction with the MFR and Exciter or with them bypassed.

2.4.2 OPERATIONAL SEQUENCE

The basic Ranging Equipment operational sequence for a tracking operation comprises a preparation sequence and an acquisition sequence.

2.4.2.1 PREPARATION SEQUENCE — During the preparation sequence the major tone is selected; if necessary the alignment of minor range tones, and the setting of the Range Calibration Adjust (zero-set) are checked and adjusted. After completion of alignment and zero-set operations, the equipment controls are set for initiation of ranging operations upon receipt of exciter ready and receiver lock status bits.

2.4.2.2. ACQUISITION — The acquisition operations are sequentially performed either automatically or step-by-step manually, in accordance with the setting of the Manual/Automatic switch. The acquisition process is initiated with the application of the selected major range tone to the modulation input of the exciter. The major range tone modulates the carrier continuously during tracking operations.

As soon as phase lock by the PLL of the Range Tone Processor is achieved, the first minor range tone is applied, as modulation, and phase correlation between the received minor tone and the equivalent synthesized tone from the DRTE is measured. If the correlation value is insufficient, pulses are deleted in the DRTE scaler for that tone causing the tone to lag, and the correlation is measured again. The process is repeated until in-phase indications have been obtained. As soon as the in-phase

condition for one tone is verified, that tone is removed from the exciter modulation input and the next lower tone is applied. The phase adjustment process is performed, in sequence, for each successively lower frequency minor tone until all of the minor tones of the DRTE have been matched to their respective received tones.

After acquisition of range tones through 10 Hz has been completed, the Ambiguity Resolving Code is applied on its sub-carrier to modulate the transmitted carrier. Correlation between the local ARC and the received ARC is measured. If correlation is not obtained, the local ARC is delayed 16 bit positions and the correlation is again measured. The process is repeated until full correlation of local and received codes is obtained and verified. Once correlation is achieved, then the ARC modulated subcarrier is removed from the exciter modulation input and tracking continues with major range tone as the sole modulator of the up-link carrier. The use of the ARC may be bypassed if desired.

2.4.3 CALIBRATION AND CHECKOUT

Calibration of the Ranging Equipment is performed in conjunction with the Station Equipment. The Station Equipment is locked onto the transponder on the Station Collimation Tower. The surveyed distance between the station and the tower should then be displayed on the Range Display on the Ranging Equipment. If there is a discrepancy between the Range Display and the surveyed range, the Range Calibration Adjust thumbwheels are then set so that the Range Display and surveyed range are in accord. This places a fixed bias into the Range Counter to compensate for total equipment delays and provide a true range display. In general, the thumbwheel settings will be dependent upon the major range tone selected. Thus the calibration procedure must be performed using the major range tone which will be used for the actual mission.

Since the doppler measurement channel is frequency coherent (See Paragraphs 2.2.2 and 4.1) with the Station Timing System, doppler measurements need not be calibrated. As may be seen in the System Error Analysis (Section 4.), the ranging portion of the system has been designed to minimize errors such as those caused by environmental factors. However, it is recommended that the range calibration process be performed at least once every 8 hours or immediately before each mission to provide confidence in the range measurement.

It is also recommended to exercise and align the system using the Test Simulator before a tracking mission. The Ranging Equipment should be exercised in the BY-PASS SIMULATE mode first. In this mode both doppler and range measurement channels may be checked by by-passing the Station MFR and Exciter. In the NORMAL SIMULATE mode the ranging equipment is exercised using the MFR and Exciter.

3. SYSTEM DESCRIPTION

3.1 PHYSICAL

3.1.1 CABINET DESCRIPTION

The steel cabinet is nominally 87 inches high including the pontoon base, 24 inches wide, and 30 inches deep. See Figure 3.1.1-1. Side panels and a full length rear door will be provided; all are removable.

Under floor cooling and cabling are utilized. Intersystem cabling enters an interconnection panel in the rear while cool air openings are at the forward bottom portion of the cabinet. The air is forced up through the equipment by an exhaust fan at the top of the cabinet. Environmental and cooling conditions are given in Specifications S-571-P-37A and S-571-P-6A. Those conditions most pertinent for design considerations are:

- Ambient Air Temperature 50° to 100°F
- Forced Air (from floor pressure)
  - Intake Temperature 53° to 63°F
  - Exhaust Temperature (above intake) 10° to 40°F

The heat dissipation within the cabinet is conservatively estimated at 1000 watts, half occurring within the power supply drawers. With a 40°F rise relative to the maximum inlet temperature of 63°, and allowing 775 watts of external heat absorbed from the worse case environmental temperature due to radiation and convection, the required air flow rate can be determined by:

$$\text{Flow rate} = K\left(\frac{Q}{\Delta t}\right)$$

where

Q = Heat dissipation rate
Δt = Temperature gradient
$K = 1/c_p\rho$
c_p = Specific heat
ρ = Density

For air, $c_p = 0.2402$ BTU/lb/°F, $\rho = 0.075$ lb/ft^3, and

$$K = 55.5 \text{ ft}^3 \cdot \text{°F/BTU} = 3.18 \text{ (°F/watt)(ft}^3\text{/min)}$$

Thus far Q = 1775 watts and $\Delta t = 40°$ F

$$\text{Flow rate} = 3.18 \times 1775/40 = 141 \text{ ft}^3/\text{min}$$

The fan used produces 150 CFM of air through the cabinet.

It is estimated that the cabinet internal temperature will vary less than 24°F. with an air flow of 150 cubic feet per minute, an intake air temperature variation of 10° F, and an ambient room temperature variation of 50° F. This variation has been used in

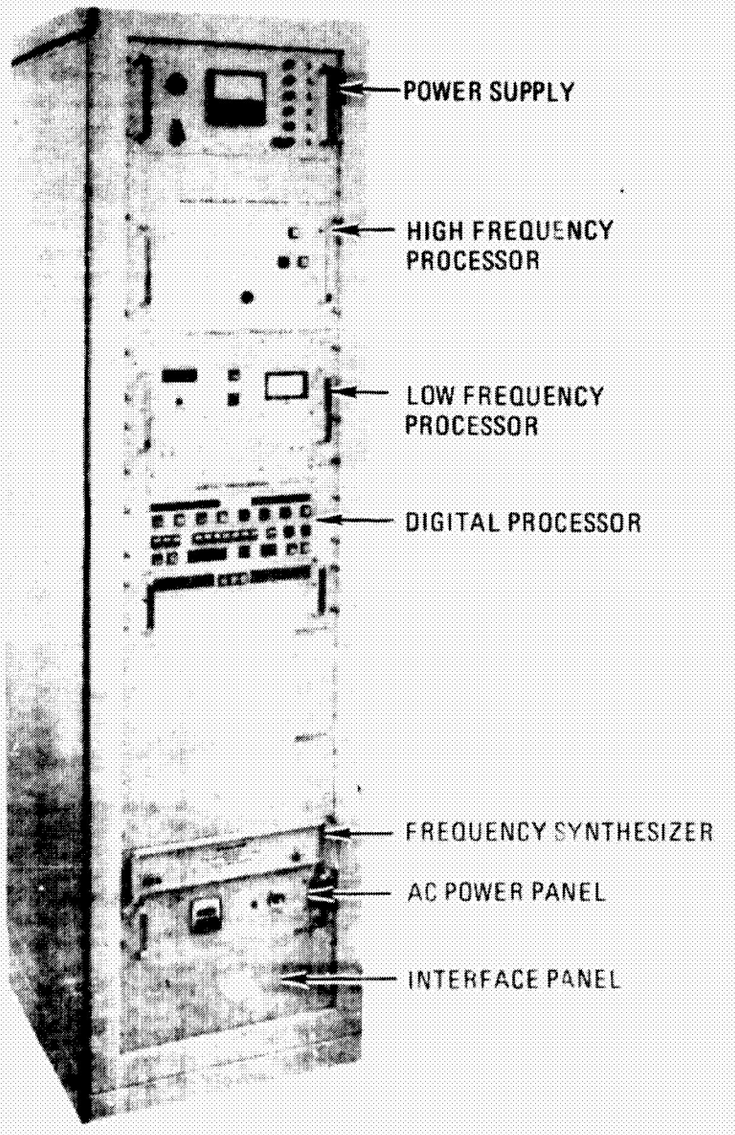


Figure 3.1.1-1. STDN Ranging Equipment, Panel Arrangement

all circuit designs and analysis to determine stability over the required operating environment.

Because the power supply is the worst heat producing unit and contains the least temperature sensitive components, it is located as close to the air exhaust as possible — at the top of the cabinet. See Figure 3.1.1-1. This allows cool inlet air to scrub the electronic chassis before it is heated by the power supply.

Small, quiet blowers are used in all chassis to eliminate hot spots. These small air circulators also allow safe temporary drawer operation outside of the cooled cabinet environment — troubleshooting on the bench, for example.

AC power is distributed to the various chassis by a plugmold. A co bus, electrically connected to all chassis as well as to the cabinet frame, is use return path for dc voltages.

Cabinet-to-drawer interfacing cables are supported by cable retractors, with easily disconnectable connectors used at the drawer interface.

3.1.2 CHASSIS DESCRIPTION

All drawers are mounted with quick disconnect slides. The levels of eye sight, overhead reach, and wrist height are those tabulated by MIL-STD-1472, "Human Engineering Design Criteria for Military Systems, Equipment and Facilities."

3.1.2.1 POWER SUPPLY — This unit is basically a collection of off-the-shelf standard power supply modules. The supporting chassis contains cooling fans for convection cooling.

3.1.2.2 HIGH FREQUENCY PROCESSOR — This chassis consists mostly of printed wiring boards shielded by metallic cans. The wiring (lower portion) of the unit is solidly covered. The upper portion is enclosed by a perforated metal cover to obtain shielding with minimum cooling air obstruction.

3.1.2.3 LOW FREQUENCY PROCESSOR -- This unit is identical in design and construction to the High Frequency Processor, except that the printed wiring boards are not shielded.

3.1.2.4 DIGITAL PROCESSOR — This is a completely covered drawer utilizing integrated circuits mounted on several packaging panels. These packaging panels contain rows of sockets which accept dual-in-line ICs. The front panel is large enough to contain the necessary switches and indicators to control and monitor the system.

3.1.2.5 FREQUENCY SYNTHESIZER – This unit is a rack-mounted version of Rockland Systems Corporation, Model 5100 Frequency Synthesizer.

3.1.3 INDICATORS AND CONTROLS

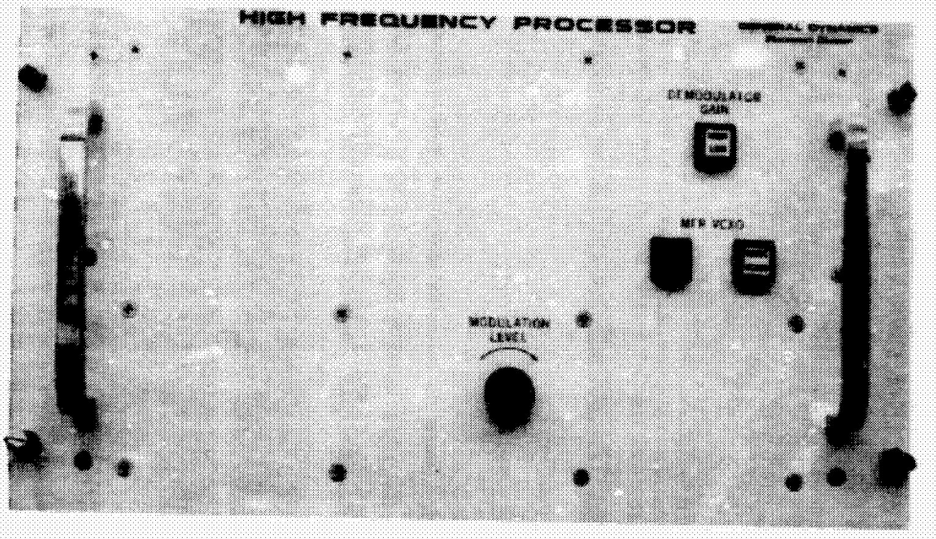
Front panel indicators and controls, which are available on the three major drawers, are illustrated in Figure 3.1.3-1 and described in Table 3.1.3-1.

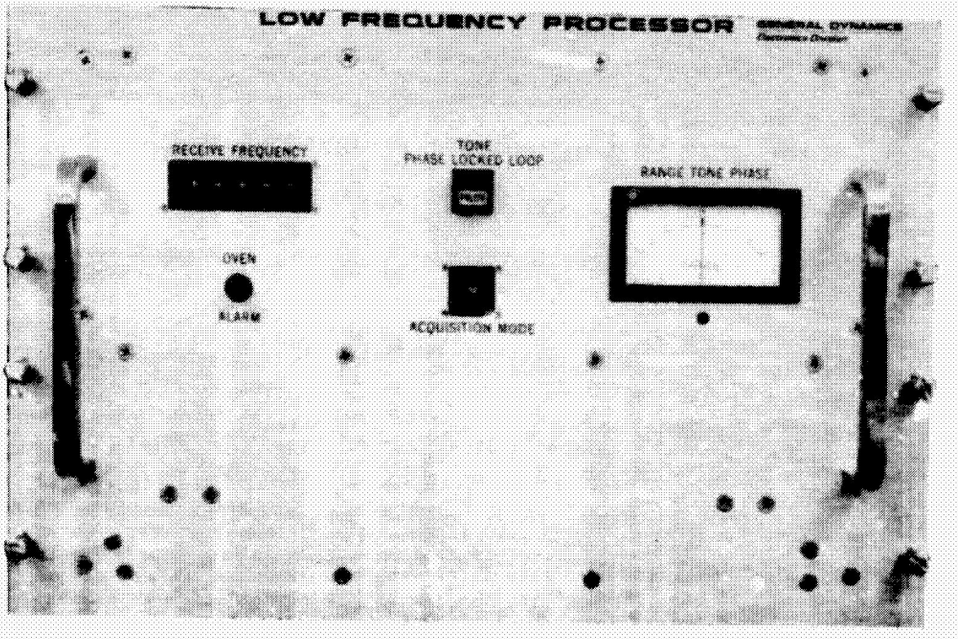
TABLE 3.1.3-1 Controls and Indicators

NAME AND/OR POSITION	TYPE OF CONTROL/INDICATOR	FUNCTION
Received Frequency	5-Section Thumbwheel Switch	Sets nominal received frequency for use by Rate Aid Synthesizer
Tone PLL Status	2-Section Indicator	Indicates: a) Loop is locked to actual major range tone b) Loop is locked to pilot tone c) Loop is not locked
Acquisition Mode - PLL	5-Position Thumbwheel Switch	Used to select acquisition mode of phased lock loop in Range Tone Processor
Phase Meter	Meter	Used in manual mode to observe phase comparison
Modulation - ON/OFF	Pushbutton Switch/Indicator	Controls application of modulation to the Exciter
Modulation Level Adjust	Potentiometer	Sets amplitude of modulation to the Exciter
MFR VCXO Select	Pushbutton Switch/Indicator	Allows and indicates manual or automatic VCO selection
VCXO-1/VCXO-2	Pushbutton Switch/Indication	Selects and/or indicates VCXO being used
Range Display	10 Characters	Indicates current range measurement in nanoseconds
Doppler Display	9 Characters, including sign	Indicates current doppler measurement in HZ
Normal/Simulate	Pushbutton Switch/Indicator	Selects and indicates input signals to ranging equipment from simulator or station equipment
Local/Computer	Pushbutton Switch/Indicator	Selects and indicates control of ranging equipment
RF Ready	Pilot Light	Indicates exciter ready and receiver lock status is received
Sync Loss	Pilot Light	Indicates loss of reference pulse synch
Doppler Reset	Momentary Pushbutton/Indicator	Initiates automatic VCO select process and resets Doppler Counter

TABLE 3.1.3-1 Controls and Indicators (Continued)

NAME AND/OR POSITION	TYPE OF CONTROL/INDICATOR	FUNCTION
One Way/Two Way	Pushbutton Switch/Indicator	a) Indicates mode of doppler operation b) Provides status signal to Computer and Tracking Data Formatter
Range Start/Reset	Pushbutton Switch/Indicator	a) Enables ranging acquisition during manual or automatic operation b) Enables and indicates reset and restart of ranging operation
Major Range Tone Select	Pushbutton Switch/Indicator (for each major range tone)	a) Selects major range tone b) Indicates lock for tone selected
Minor Range Tone Select	Pushbutton Switch/Indicator (for each range tone)	a) Select and indication of range tone (manual) b) Indicates acquisition or lock of range tone (automatic) c) Indication of range tone (automatic)
ARC On/Lock	Pushbutton Switch/Indicator	Manual selection of ARC and correlation indication
Range Complete	Pilot Light	Indicates all range tones acquired
Automatic/Manual	Pushbutton Switch/Indicator	Selects and indicates mode of ranging acquisition
Manual Shift	Pushbutton Switch/Indicator	Used in manual mode to achieve phase match of minor tones and ARC
Range Calibration	5-Section Thumbwheel Switch	Sets range calibration numbers for removal from range readout (Zeroset)
Integration Time Select	1-Section Thumbwheel Switch (6 positions, 1 Auto plus 5 selections)	Provides manual selection of integration time or selection of automatic mode
ARC Preset	2-Section Thumbwheel Switch	Presets ambiguity number in ARC generator
ARC Use/Bypass	Pushbutton Switch/Indicator	Allows bypassing use of ARC in ranging
ARC Alarm Reset	Pushbutton Switch/Indicator	Indicates error in ambiguity number and allows manual ARC reset
Check Ambiguity	Pushbutton Switch/Indicator	a) Indicates loss of lock by MRT PLL after ranging complete b) Can be reset manually
Static Range Select	10-Section Thumbwheel Switch	Used to select range for use in static range simulation
Insert Data	Momentary Pushbutton	Inserts selected static range value
Static/Dynamic	Pushbutton Switch/Indicator	Used to select static or dynamic range simulation when in simulation mode
Normal/Bypass	Pushbutton Switch/Indicator	Selects and indicates mode of simulator operation
Doppler Select	10-Section Thumbwheel Switch	Used to select doppler for use in simulation





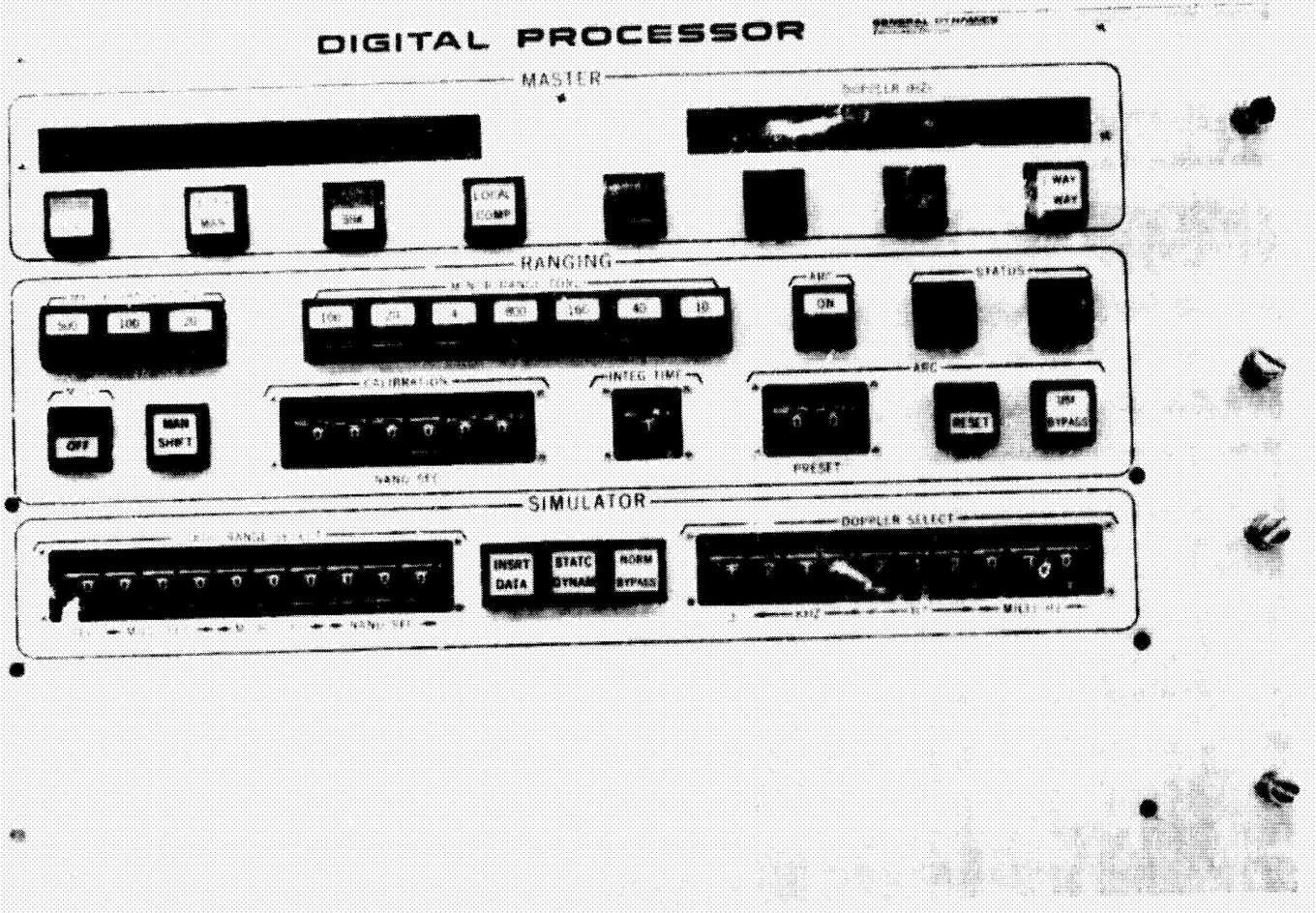


Figure 3.1.3-1. STDN Ranging Equipment, Front Panel Controls and Indicators

3.2 FUNCTIONAL

3.2.1 RANGE TONE GENERATOR (RTG)

The Range Tone Generator (Figure 3.2.1-1)* produces the following phase coherent output signals: 500 kHz, 100 kHz, 20 kHz, 4 kHz, 800 Hz, 160 Hz, 40 Hz, and 10 Hz. All of the outputs are digitally synthesized from an input 40 MHz reference signal and are synchronized to within 25 nanoseconds of an input 10 pps reference pulse train. In particular, the 10 pps output is synchronized to the positive going edge of the 10 pps input.

The RTG operates from a 40 MHz reference coherently produced from the 5 MHz system reference input. The 40 MHz is used (instead of operating directly from 5 MHz or 1 MHz) to provide the required 25 nanosecond settability without the need for an analog phase shifter. The 40 MHz reference signal is divided down to a 1 MHz pulse train using divide-by-five and divide-by-eight synchronous counters as shown in Figure 3.2.1-2. The 1 MHz is power driven for subsequent use as the clock signal for the remainder of the countdown chain. This insures that the countdown chain output skew is dependent only on the differential delays of the gates and the output divide-by-two flip-flops. Typically, the differential delays are less than 5 nanoseconds and stable within 1 nanosecond. Since the divide-by-five and divide-by-eight counters are capable of reset by the same sync circuit, the 1 MHz output (and thus all lower frequency outputs) can be positioned in time in 25 nanosecond increments.

*For convenience, bound in Appendix A.

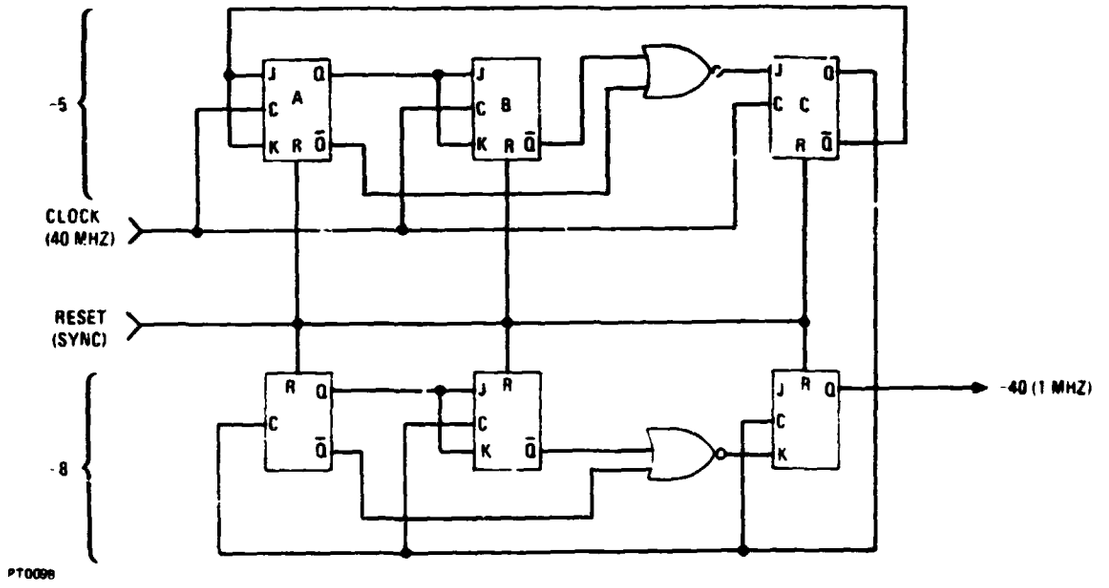


Figure 3.2.1-2. Divide-by-Forty Circuit

The Range Tone Generator outputs are the source of the transmitted range tones as well as other system reference frequencies. The output AND-OR gates select outputs either from the RTG frequency divider chain in the NORMAL mode or from the simulator RTG frequency divider chain when in the SIMULATE mode. For all minor range tones, outputs are produced in two phases: 0° and 72° for 4 kHz, 800 Hz, and 160 Hz; and 0° and 90° for 40 Hz and 10 Hz. The two different phases are used in the Modulation Combiner tc provide the phase shift capability necessary for equalizing system delays during alignment. (A typical divide-by-five circuit which produces the two required phases is illustrated in Figure 3.2.1-3.)

In addition to supplying the range tones themselves, the RTG also supplies 400 kHz and 100 kHz signals to the Modulation Combiner to produce 400 kHz and the 10 pps sampling pulse for use in the Transmit ARC Generator and in the Range and Doppler Counters.

Synchronization of the range tones with the 10 pps input sync signal is achieved by detecting leading edge coincidence of 10 pps sync signal and the synthesized 10 Hz signal. If they are not coincident within 25 nsec, a reset pulse is provided to the countdown chain setting it to the all-zeros state which presets the countdown chain by 1 count (25 nsec) such that the next comparison between the 10 pps sync signal and the synthesized 10 Hz signal ideally would result in the 10 Hz synthesized signal arriving 25 nsec early at the next comparison. However, the uncertainty in the next transition of the divider chain 40 mHz clock will result in the 10 Hz synthesized signal arriving t nsec

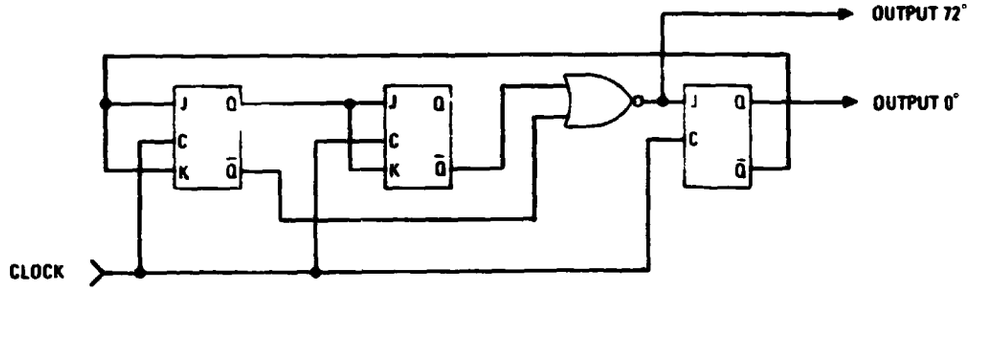


Figure 3.2.1-3. Typical Divide-by-Five Circuit.

late, where $0 \leq t \leq 25$ nsec. Thus, the next comparison will result in a skew S equal to

$$S = (25 - t) \text{ nsec}$$

where

$$0 \leq t \leq 25 \text{ nsec}$$

This skew is biased at +12.5 nsec. The bias is removed by delaying the release of the divider chain reset signal with respect to the 10 Hz sync by 12.5 nsec. The skew is now

$$S = (25 - 12.5 - t) \text{ nsec}$$

where

$$0 \leq t \leq 25 \text{ nsec}$$

Thus, the maximum deviation of the skew is ±12.5 nsec. The 12.5 nsec delay in the release of the reset is implemented by a one-shot circuit.

Figure 3.2.1-4 shows the synchronization circuit. The leading edge of the sync signal and the 10 pps from the countdown chain create 25 nsec pulses by driving one-shot circuits as shown. If the two one-shot pulses do not overlap, counter AB advances to the two state enabling the next zero state of the sync signal to reset the countdown chain. The reset is released at the positive transition of the sync signal delayed 12.5 nsec by the one-shot. When the 2 one-shot pulses overlap (a synchronized condition) a pulse is set to the synchronizing counter AB resetting it to the initial state. Because of the asymmetry of the sync signal, gate D is provided to allow synchronization of the two signals independent of the out-of synchronization phase relationship. A red light is driven from the sync circuit to display an out-of sync condition.

The Range Tone Generator circuitry is physically located in the Digital Processor drawer.

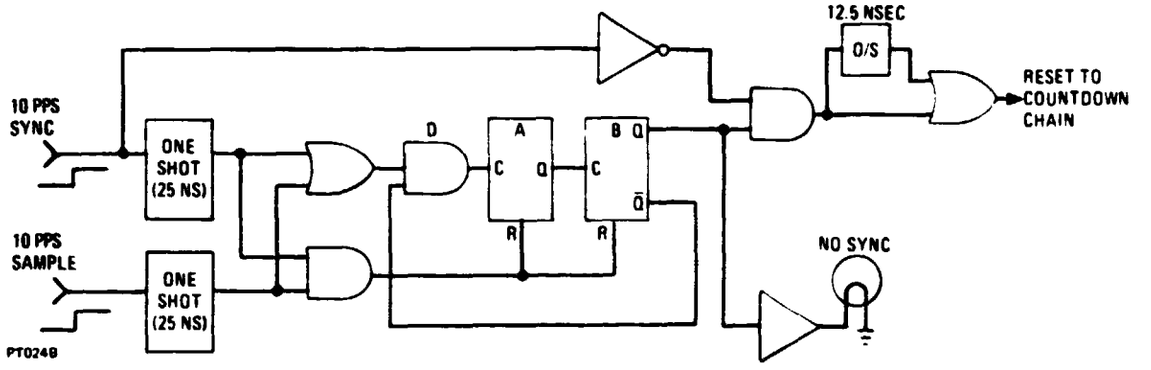


Figure 3.2.1-4. Synchronization Circuit.

3.2.2 TRANSMIT ARC GENERATOR

For resolving ambiguities in the 10 Hz range tone, the Transmit ARC Generator (Figure 3.2.2-1) produces a pseudo-random ambiguity resolving code (ARC) using a 10-bit shift register as a sequence generator.

The ARC reset signal from the Digital Range Tone Extractor (DRTE) initializes the code generator to the all 1's state. The next leading edge of the 10 Hz square wave from the Range Tone Generator enables the 160 Hz shift register clock (from the Modulation Combiner) and sets the Local ARC start signal. The Q7 and Q10 outputs of the shift register are exclusively OR'd to produce a 1023-bit pseudo-random code for feedback to the shift register serial input and for input to the Modulation Combiner where it is used to bi-phase modulate a 4 kHz subcarrier.

The generator is supplied with an all 1's detector circuit which provides an output pulse each time the sequence goes through this reference condition. The time between this output and a similar output from the Local ARC Generator represents the coarse range data.

Since the code length is 1023 bits, and the code is clocked at a rate of 160 bits per second, the code length is 6.39375 seconds. This provides an ambiguity resolving capability of approximately 958,000 kilometers.

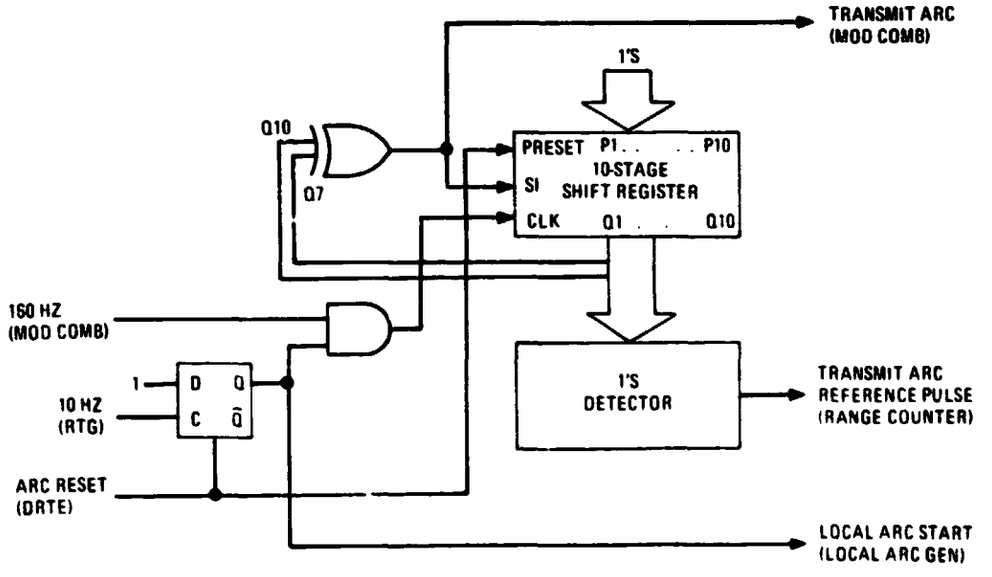


Figure 3.2.2-1. Transmit ARC Generator, Block Diagram

The Transmit ARC Generator circuitry is located in the Digital Processor drawer.

3.2.3 MODULATION COMBINER

The Modulation Combiner (Figure 3.2.3-1) combines the 8 range tones and ARC for modulation of the up-link carrier via the Exciter. In general, this is accomplished by:

1. High-side complementing the 800 Hz tone onto the 4kHz tone
2. Bi-phase modulation of a 4 kHz sub-carrier with the 160 Hz, 40 Hz or 10 Hz tone or with the ARC
3. Linear combining the major range tone (500 kHz, 100 kHz, or 20 kHz) with a minor range tone or the ARC modulated sub-carrier
4. Providing level adjustment to control modulation index of various tones, and phase shifters for some minor tones for initial ambiguity alignment
5. In addition, this unit generates a 400 KHz reference signal for use by the fixed frequency synthesizer

All the range tones are provided to the Modulation Combiner by the Range Tone Generator in squarewave form. For all range tones below 20 kHz, two phases are supplied which allow for continuous phase shifting of the minor range tones over a range of at least 72° or 90° as appropriate. This capability provides the required tolerance for initial system alignment. Because the phase shifter will produce harmonic energy and amplitude change over the control range, it is followed by a filter and limiter. No phase shifters are included for the 500 KHz, 100 KHz or 20 KHz tone in order to minimize phase drifts due to temperature and level variations. This is important since phase variations of a major range tone contributes directly to range measurement error. Phase shifters for 100 kHz and 20 kHz phase alignment are provided in the Range Tone Processor. However, those phase shifters are not in the signal path when the tone is selected as the major range tone.

The 500 kHz through 4 kHz tones are transmitted as sinusoids with harmonics down at least 40 dB. The 800 Hz tone is transmitted as the upper sideband of 4 kHz at 4.8 kHz. Harmonics of the 4.8 kHz are down 40 dB and the lower sideband of 4 kHz (at 3.2 kHz) is down 20 dB. The minor range tones below 800 Hz are complemented onto the 4 kHz range tone in the form of double sidebands of a 4 kHz supressed carrier. (The 4 kHz subcarrier is bi-phase modulated with the minor range tone.) For these tones the complementing balanced modulator is followed by a bandpass filter passing frequencies from 3.2 kHz to 4.8 kHz. This filter insures that the lowest frequency modulation energy of significant power is at least 3.2 kHz removed from the carrier, thus avoiding carrier tracking interference.

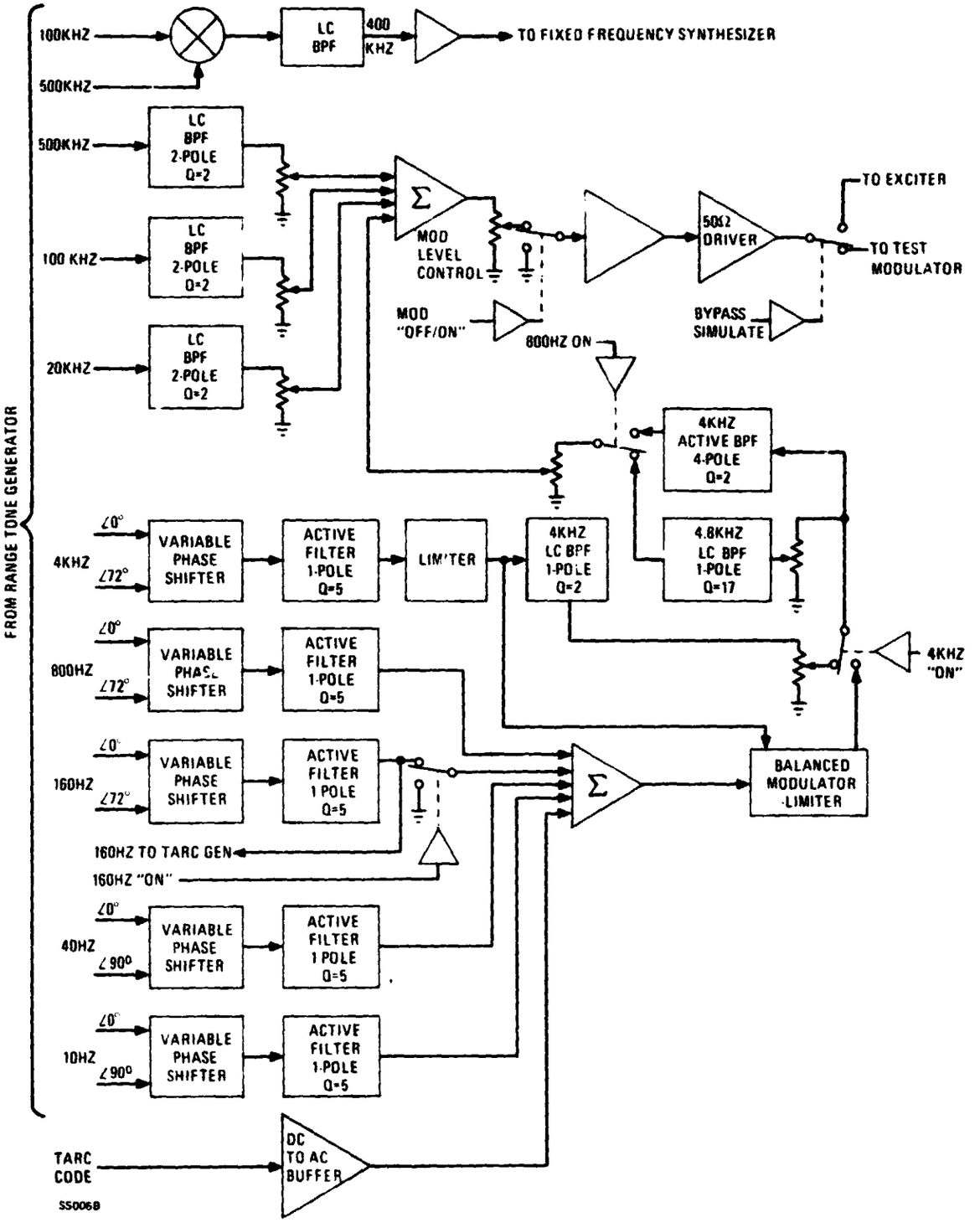


Figure 3.2.3-1. Modulation Combiner, Block Diagram.

The ARC is applied to the complementing balanced modulator in the same manner as the tones are applied. This results in a bi-phase modulated 4 kHz signal.

The minor tones and ARC signals are linearly combined with the selected major tone in a summing amplifier where each major range tone signal level is individually adjustable. This combined output is passed through a variable gain amplifier and provided to the Exciter. This final gain control is located on the high frequency processor front panel and adjusts the output to the Exciter from 0 to 4 V peak-to-peak.

The Modulation Combiner also produces a 400 kHz reference signal for use in the Fixed Frequency Synthesizer. This reference is generated by mixing 100 kHz and 500 kHz square waves from the Range Tone Generator.

The circuits necessary to implement these functions are located in the High Frequency Processor drawer.

3.2.4 RANGE DEMODULATOR

The Range Demodulator is part of the range signal generator subsystem and is physically located in high frequency processor (Figure 3.2.4-1). The function of range demodulator A2A5 is to demodulate and level control the major tones, minor tones, complemented minor tones, and ARC modulated 4 kHz subcarrier. Level control is

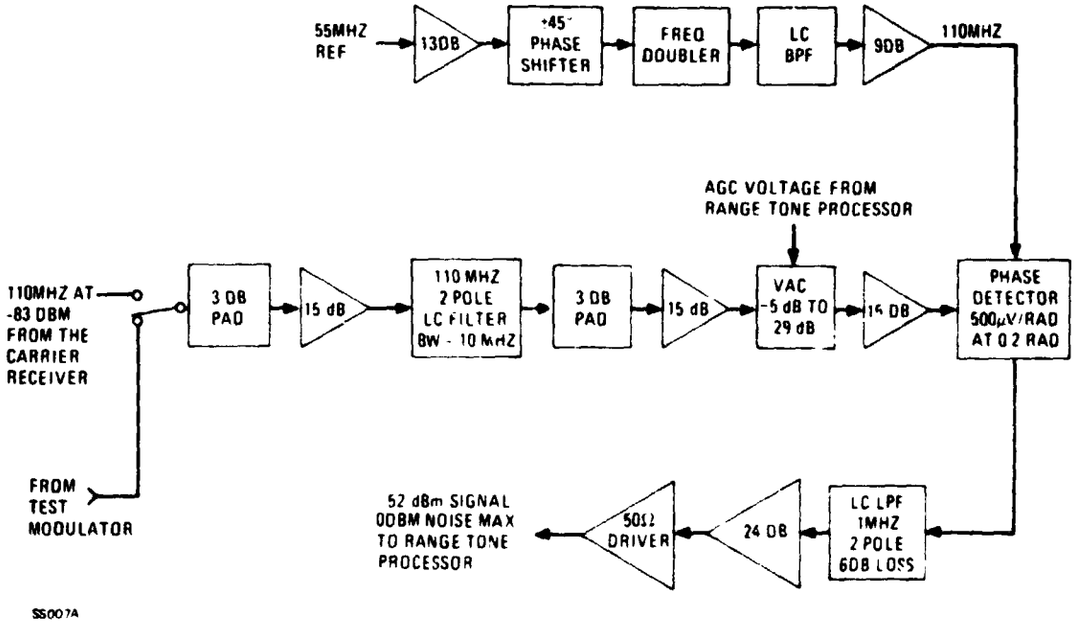


Figure 3.2.4-1. Range Demodulator, Block Diagram.

accomplished using a coherent agc technique based on the major range tone power, with gain adjustment performed prior to demodulation. This technique provides less range tone phase delay variation and eliminates signal suppression and the resultant s/n ratio deterioration.

The receiver if signal is passed through a 3-dB pad to maintain a good 50-ohm impedance level and is then filtered by a 2-pole 10-MHz bandwidth filter to reduce noise energy. The signal then flows through a voltage controlled, solid-state attenuator. The attenuator uses pin diodes to minimize group delay over its control range. The control voltage comes from the range tone P11 and changes the attenuation over a minimum 21-dB range.

Sensitivity of the range tone detector is changed such that the demodulated range tone amplitude remains constant for modulation indices from 0.2 radian to 1.5 radians. A high-level, double-balanced mixer is used as a phase detector. The input level is made as high as possible, but not high enough to cause gain compression, thus eliminating possible group delay variations under a high noise environment.

The reference signal to the detector is capable of being phase shifted to ensure maximum sensitivity from the detector. The detector output is filtered in a 1-MHz low-pass filter to further reduce noise energy and is amplified to an output level of -52 dBm for the signal, and 0.6 volt peak for the noise in the noisiest environment. This output goes to the range tone processor.

3.2.5 RATE AID SYNTHESIZER

The Rate Aid Synthesizer develops signals which consist of a bias frequency plus an approximation of the major range tone doppler. See Figure 3.2.5-1. The signals are developed by dividing the extracted carrier doppler by a number approximately equal to the ratio of the received carrier frequency to the major range tone frequency. This operation is performed to partially cancel the frequency dynamics of the received major tones, thereby allowing the use of narrow band tone tracking filters with small lag errors due to doppler dynamics. The division is performed in a pair of digital frequency dividers programmable from front panel thumbwheel switches. The Rate Aid Synthesizer also provides a 500 kHz rate-aided signal for range simulation purposes and a fixed $1.\overline{6}$ MHz pilot tone to the Range Tone Processor.

Two separate paths are used to develop the bias-plus-doppler for the range tone tracking loops. The two separate paths (one for bias only, and one for bias-plus-doppler) are necessary because of the variable division factor. In this design the initial bias is cancelled at Mixer M2 and the new bias frequency is injected at Mixer M1. The new bias frequency is independent of the original bias frequency and can be chosen arbitrarily. A spurious analysis lead to the selection of $2.1\overline{6}$ MHz (2 1/6 MHz) as the bias frequency for the 500 kHz range tone doppler rate aid. This selection results in excellent spurious performance in the processor. Bias frequencies for the two lower major range tone frequencies are $1.7\overline{6}$ MHz and $1.68\overline{6}$ MHz which also result in excellent spurious performance for the 100 kHz and 20 kHz range tones.

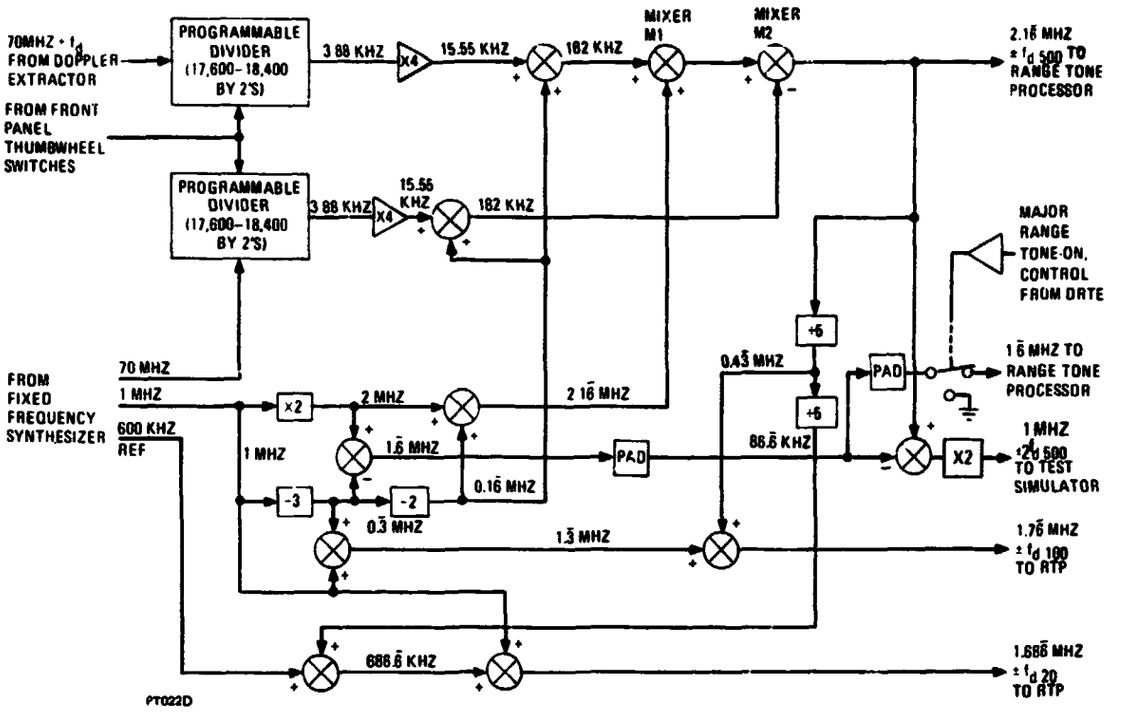


Figure 3.2.5-1. Rate Aid Synthesizer, Block Diagram.

The programmable dividers in conjunction with the ×4 multipliers following them allow setting of the doppler division ratio from 4400 to 4600 in steps of 1/2. This provides 400 selectable ratios corresponding to the 100 MHz received carrier tuning range. Thus, the ratio can be selected to correspond to the closest 250 kHz carrier frequency and the maximum error will correspond to 125 kHz. The rate-aid signal will then reduce to range tone doppler in the Range Tone Processor to a maximum of 0.003 Hz.

The Rate Aid Synthesizer includes circuitry associated with the Test Simulator. In particular, the unit produces an output which is twice the synthesized 500 kHz range tone doppler with a bias frequency of 500 kHz. This output thus simulates the phase and frequency characteristics of the received 500 kHz range tone with doppler. This signal is used by the Test Simulator for dynamic range simulation.

The Rate Aid Synthesizer circuitry is contained in the Low Frequency Processor drawer.

3.2.6 RANGE TONE PROCESSOR

The Range Tone Processor (Figure 3.2.6-1) performs signal processing of the received range modulation signal. This includes narrowband filtering of the major

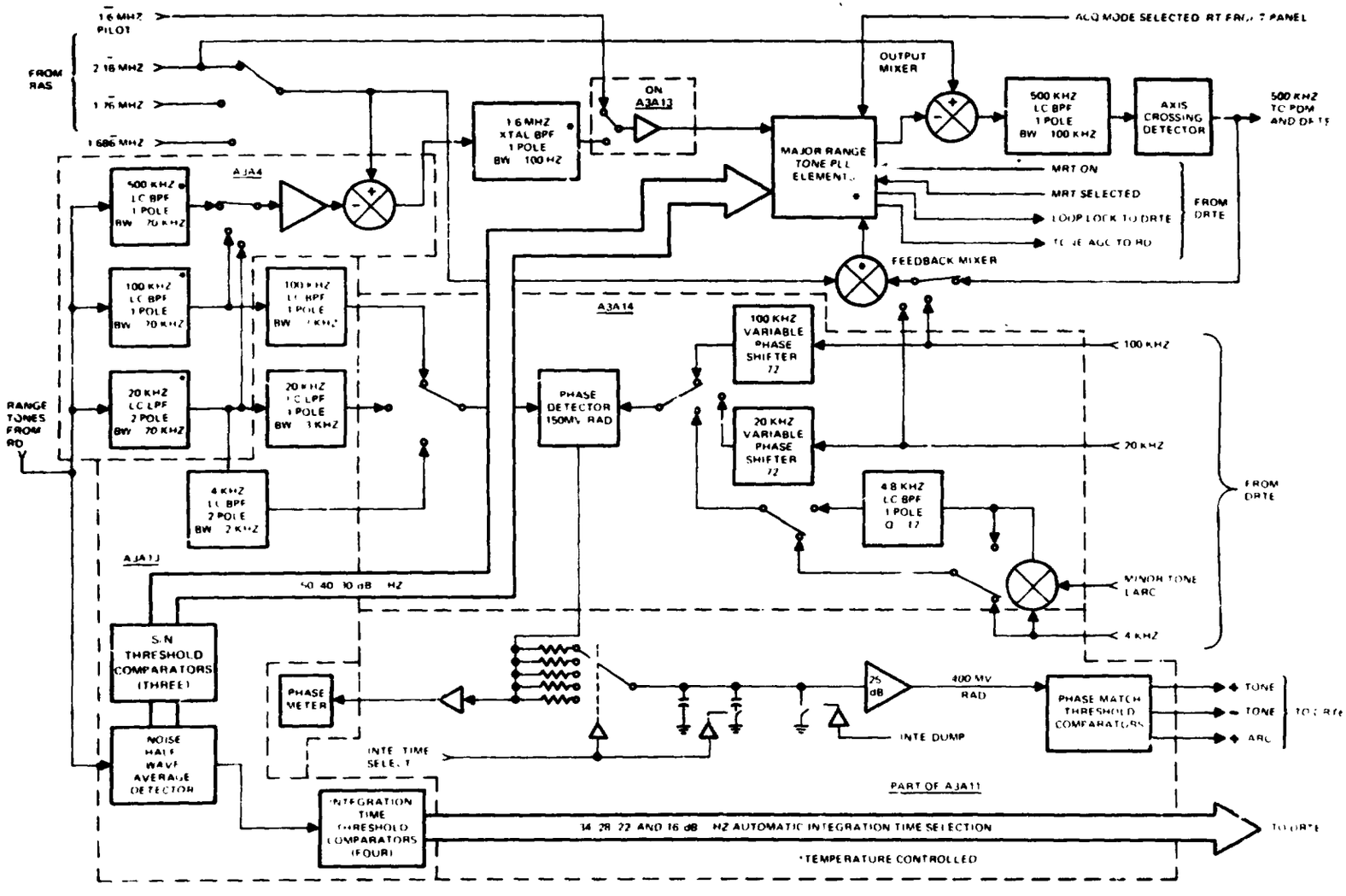


Figure 3.2.6-1. Range Tone Processor, Block Diagram.

range tone and coherent phase detection of the minor range tones and ARC. Additionally, this unit provides an AGC voltage to keep the demodulated major range tone level constant and changes the minor range tone integration time automatically, depending on the range tone signal-to-noise ratio.

Narrowband filtering of the major range tone is achieved using a phase-locked loop (PLL) with rate-aid. The input rate-aid mixer decreases the doppler on the major range tone before the PLL, thus allowing the PLL to have a very narrow bandwidth without excessive lag. A third-order loop is used during tracking to minimize lag errors to meet the required range accuracy under full doppler dynamics. The rate-aid mixer following the PLL restores true doppler information to the major tone. (Supporting analysis for the major range tone processing is presented in Paragraph 4.3).

The frequencies used for rate-aid injection have been selected to eliminate potential mixer products which could introduce phase error on the tracked tone. After the input mixer, the rate-aided tone is filtered by a crystal filter with approximately a 160 Hz noise bandwidth. This maintains the signal-to-noise ratio at the Phase Detector above -15 dB and thus insures good noise offset performance. Note that after input rate-aid mixing, the major tone utilizes the same circuit elements, whether it is 500, 100, or 20 kHz. This is a result of changing the rate-aid signal to produce a constant bias frequency ($1.\overline{6}$ MHz) input signal to the PLL. Several components are maintained within a controlled temperature range to reduce phase drifts. For tracking the major tones, the phase detector reference signal is of a double-sideband suppressed carrier nature The effect of using this signal as a reference is a reduction in the phase detector sensitivity. This is a minor effect and is compensated for by added gain in the compensation function of the major range tone PLL. The 500 kHz output from the output rate-aid mixer drives the phase data multiplier, which decreases the increment size of the digital range data, and the DRTE which synthesizes the lower frequency range tones. Note that the 500 kHz output filter and axis crossing detector are in the feedforward path and thus do not contribute to phase drift errors.

The phase of the 100 kHz and 20 kHz tones (when used as minor tones), and the phase of the complemented tones that are only minor tones (4 kHz, 800 Hz, 160 Hz, 40 Hz, 10 Hz) are detected in a high-noise (-32 dB S/N) performance detector. Comparing the phases of the complemented tones yields the same information as comparing the phases of the tones themselves. The reference complemented tone is changed by mixing a 4 kHz reference with the minor tone. The minor tone phase is changed during the digital phase-matching process which changes the phase of the reference complemented minor tone. The ARC is handled in the same manner as a minor tone. Phase shifters at 100 kHz and 20 kHz are provided for initial ambiguity alignment.

The minor tone phase detector outputs are routed to a front panel meter for manual phase matching and to an integrate-and-compare circuit for automatic phase matching. The integrator time constant can be changed automatically, depending on the range

tone S/N, or manually with a front panel thumbwheel switch. Automatic integration time selection is accomplished by detecting the amplitude of the noise and signal at the input to this unit and comparing that amplitude to reference voltages in comparators. The output of the integrator is compared to two reference voltages (V_A and V_B) to control digital phase shifting. The DRTE shifts the synthesized tone in 72° increments for all but 40 Hz and 10 Hz, which are shifted in 90° increments. Note that phase matching is complete when a peak output from the comparison phase detector is reached.

The integrate and compare for the ARC yields a correlation or noncorrelation signal utilizing one comparison voltage V_C.

The Major Range Tone PLL elements are shown in Figure 3.2.6-2. Except for the phase detectors, VCXO, and AGC circuits, this function is implemented digitally because of its inherent flexibility which eases the acquisition problem, particularly at a S/ϕ of +30 dB-Hz. A pilot tone (1.$\bar{6}$ MHz) is used to keep the VCXO on frequency to minimize acquisition time. When the PLL is switched from the pilot to the data 1.$\bar{6}$ MHz, the VCO offset "remembers" the control voltage at which VCXO will remain at 1.$\bar{6}$ MHz and uses it as a bias thereafter.

Slew control is necessary to minimize acquisition time and is accomplished by: 1) digitally phase shifting the feedback signal when the phase error is large; and 2) directional analog slew voltage to drive the VCXO toward minimum phase error when the

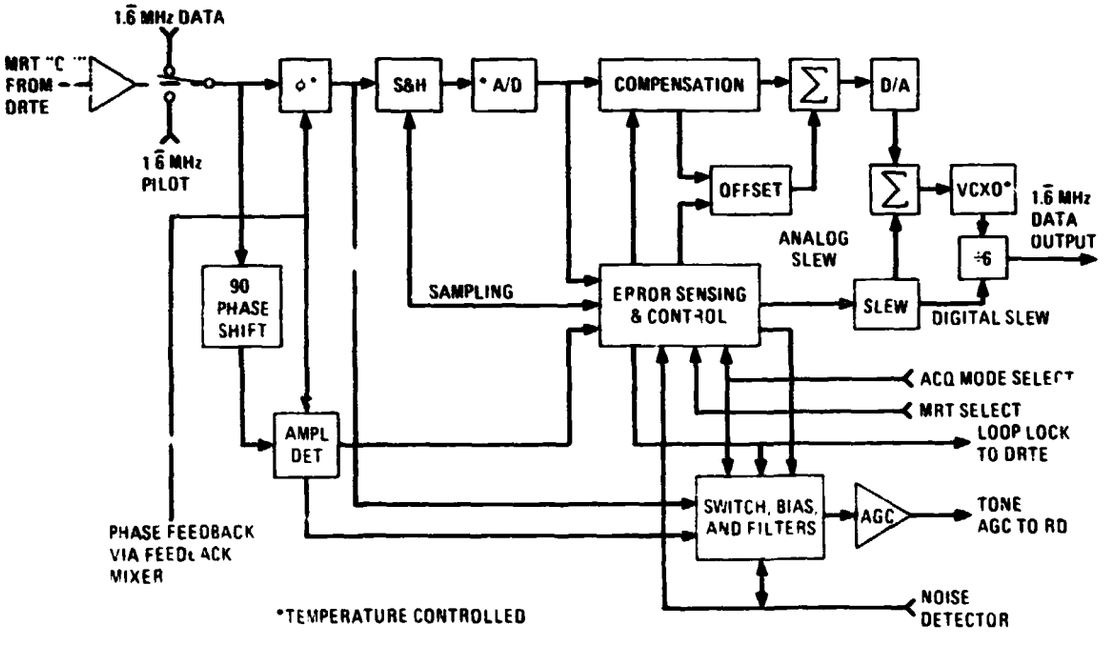


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Figure 3.2.6-2. Major Range Tone PLL Elements.

error is small. Logic to perform this function receives input information from the loop phase detector and amplitude detector.

Figure 3.2.6-3 shows basic information flow in the PLL compensation circuitry. Digital techniques are employed to obtain 2nd and 3rd order loop operation with near perfect integrators. The PLL compensation transfer functions for the two modes of operation are:

2nd Order PLL

$$\frac{e_{out}}{e_{in}}(S) = \frac{G\,N}{K_{\varphi}K_{vco}}(1+\omega_a/S)$$

$$= \frac{G\,N}{K_{\varphi}K_{vco}}\;\frac{S+\omega_a}{S}$$

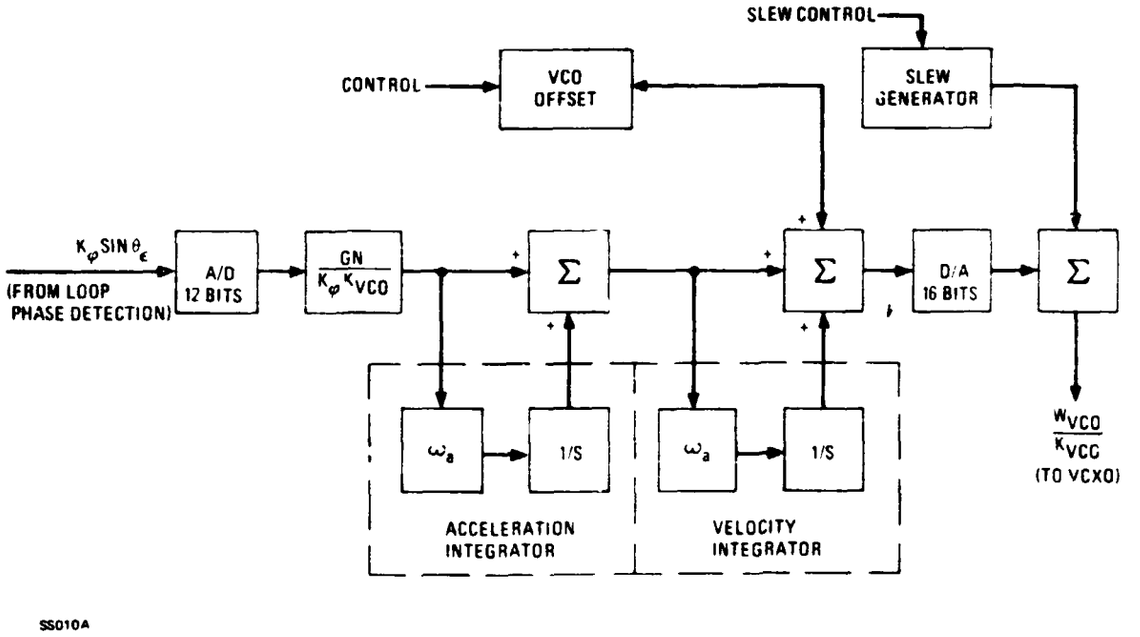

Figure 3.2.6-3. Major Range Tone PLL Compensation for 3rd Order Mode of Operation.

3rd Order PLL

$$\frac{e_{out}}{e_{in}}(S) = \frac{G\,N}{K_{\varphi} K_{vco}}(1+\omega_a/S)(1+\omega_a/S)$$

$$= \frac{G\,N}{K_{\varphi} K_{vco}} \frac{(S+\omega_a)^2}{S^2}$$

The resultant open loop functions are:

2nd Order PLL

$$\frac{\theta_o}{\theta_\epsilon}(S) = \frac{G(S+\omega_a)}{S^2}$$

3rd Order PLL

$$\frac{\theta_o}{\theta_\epsilon}(S) = \frac{G(S+\omega_a)^2}{S^3}$$

The loop constants were chosen to obtain a nominal 20% overshoot for a small step error of phase, corresponding to a damping factor of $\zeta = 0.707$ for the 2nd order configuration.

The values of G and ω_a are set in accordance with desired PLL one-sided noise bandwidth, BN_1 (HZ), as follows:

2nd Order PLL

$$G = 2.66\ BN_1$$

$$\omega_a = 1.33\ BN_1$$

3rd Order PLL

$$G = 3.03\ BN_1$$

$$\omega_a = 0.449\ BN_1$$

The range tone processor also contains the modulation index automatic gain control detector, feedback circuit, and comparator. Together with the range demodulator automatic gain control attenuator, the input voltage to the loop phase detector is held constant to within 0.6 dB for received major range tone indices from 0.2 radians to 1.5 radians. The transfer function takes the general form of G(S) = 1/(ST + K). The design is based on having a good S/N ratio ($\geq$ + 12 dB) in the automatic gain control loop bandwidth when operating with an index of β = 0.2 randian and at a major range tone S/ϕ of +10 dB - Hz. The automatic gain control noise bandwidth rapidly increases as the index increases since the pin diode attenuator is a logarithmic device and therefore increases the loop gain accordingly. At an index of 0.2 radian the time constant (τ) is approximately 40 seconds and the loop gain (K) is approximately 20 resulting in a noise bandwidth (bn) of approximately 0.25 Hz. Because of this small bandwidth required to handle noisy low-index signals, the fastest acquisition mode (4 seconds) cannot be used with an index below 0.5 radians.

3.2.7 PHASE DATA MULTIPLIER (PDM)

The function of this unit (Figure 3.2.7-1) is to multiply the major range tone phase information to allow digitizing the phase in 2000 increments corresponding to approximately 0.15 meter.

The 500 kHz from major range tone PLL of the Range Tone Processor is mixed with a stable reference 480 kHz to produce a 20 kHz ±50 Hz signal which contains the range tone phase information. A ×2000 frequency multiplication is then performed using a second-order tracking loop with a bandwidth of 2 kHz. This bandwidth is made wide to allow reduction of self-generated VCO noise via feedback and to insure that the PLL will lock-up in 2 seconds, should it become unlocked. Voltage limiting in the loop filter ensures that the VCO will remain on frequency in the absence of an input signal. The Q of the LC tank circuit in the VCO is made high to produce a stable carrier. The VCO output frequency contains the major range tone phase information, but multiplied 2000 times.

To close the loop, a divider circuit divides the VCO frequency by 2000 where it is used as the phase detector reference, and as the range counter reset.

The circuits to implement this function are located in the Low Frequency Processor drawer.

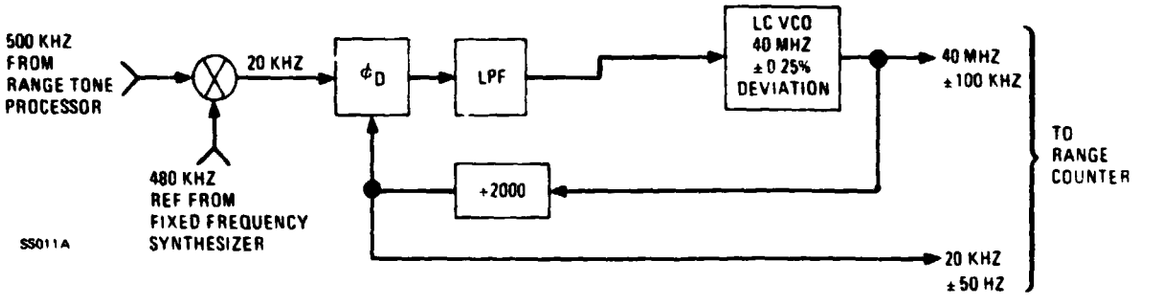

Figure 3.2.7-1. Phase Data Multiplier, Block Diagram.

3.2.8 DIGITAL RANGE TONE EXTRACTOR (DRTE)

The DRTE (Figure 3.2.8-1) consists of a frequency-divider chain for synthesizing local range tones, a manual and automatic circuit for digitally phase-matching the synthesized tones to the received range tones, tone selection and sequencing logic for manually and automatically selecting and sequencing the tones for phase-matching, selection gates for implementing the control function and, integrator and dump control logic for manual and automatic selection of integrating (correlating) and dump control.

The frequency divider chain (see Figure 3.2.8-2) is implemented similar to the Range Tone Generator divider chain. A 500 kHz square wave is digitally multiplied by 2 to produce a 1 Mpps waveform. The 1 Mpps is repeatedly divided by five to produce 200 kpps, 40 kpps, 8 kpps, 1.6 kpps and 320 pps. The 320 pps is divided by four twice to produce 80 pps and 20 pps. Each pulse train from 1 Mpps to the 20 pps is synchronously divided by two using the 1 Mpps as a clock to produce the following coherent output square waves: 500 kHz, 100 kHz, 20 kHz, 4 kHz, 800 Hz, 160 Hz, 40 Hz, and 10 Hz. These local range tones are phase compared to the received range tones in the RTP and the error signal then used to control the digital phase matching process. All frequencies are capable of being phase shifted with respect to the 500 kHz square wave in multiples of 72° except for the 40 Hz and 10 Hz which are in multiples of 90°. Utilizing the two groups of signals prefix by "D" and "C" (delete and count) in the block diagram, the phase shifting process is achieved by counting the "C" pps signal at 10 times the frequency to be phase shifted (8 times the frequency for 40 and 10 Hz) and deleting pairs of pulses (by utilizing the corresponding "D" pps lines) for each 72° phase shift (for 40 Hz and 10 Hz a 90° phase shift is achieved by deleting two pulses at 8 times the frequency to be phase shifted).

The phase error signal in the Range Tone Processor is integrated and applied to a comparator to produce logic levels "A" and "B", for automatic phase matching of tones, and to logic level "C: for ARC correlation (see description under RTP). The logic levels are received by the digital phase matching circuit for completing the phase matching process in a minimum number of steps; the logic used is given in Table 3.2.8-1. Phase match is always accomplished in, at most, three steps using this logic. In the block diagram the pulse delete logic performs the implementation of the logic table. The inputs HT signifies matching of 160 Hz to 100 kHz range tones and LT for the 10 Hz and 40 Hz tone. For the high tones phase shifts of 72°, 144° or 216° can be implemented in a single comparison by deleting 1, 2 or 3 pair of pulses at 10 times the frequency being matched. For the low tones (40 Hz and 10 Hz) phase shifts of 90° or 180° can be implemented by deleting 1 or 2 pairs of pulses at 8 times the frequency being matched. The pulse delete counter receives the phase shift commands and the count frequency input from the Pulse Delete Synchronizer and outputs a pulse blanking signal synchronized to the pps count frequency. This blanking pulse is steered via the selection gates to the proper blanking input of the Frequency

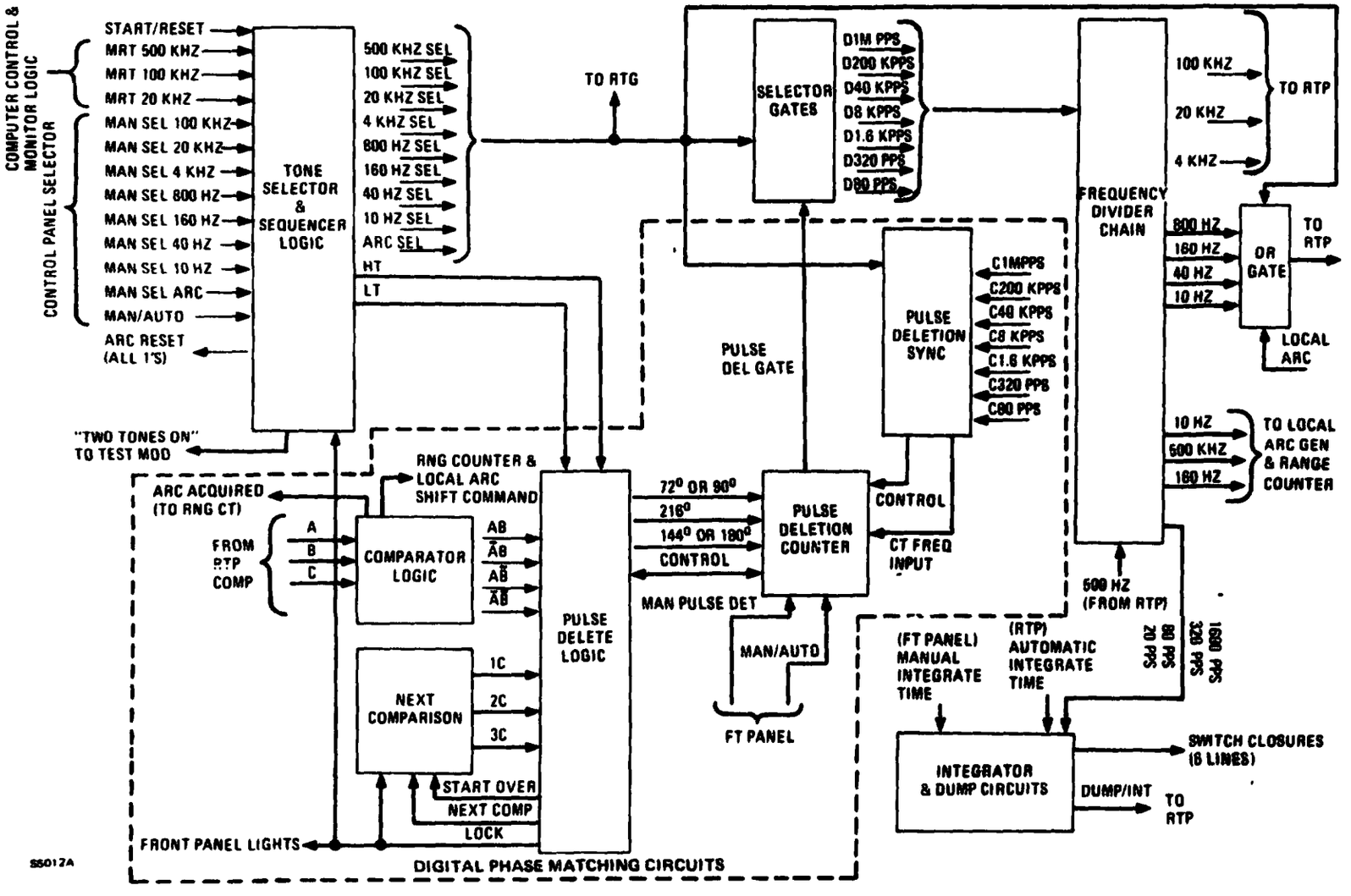

Figure 3.2.8-1. Digital Range Tone Extractor, Block Diagram.

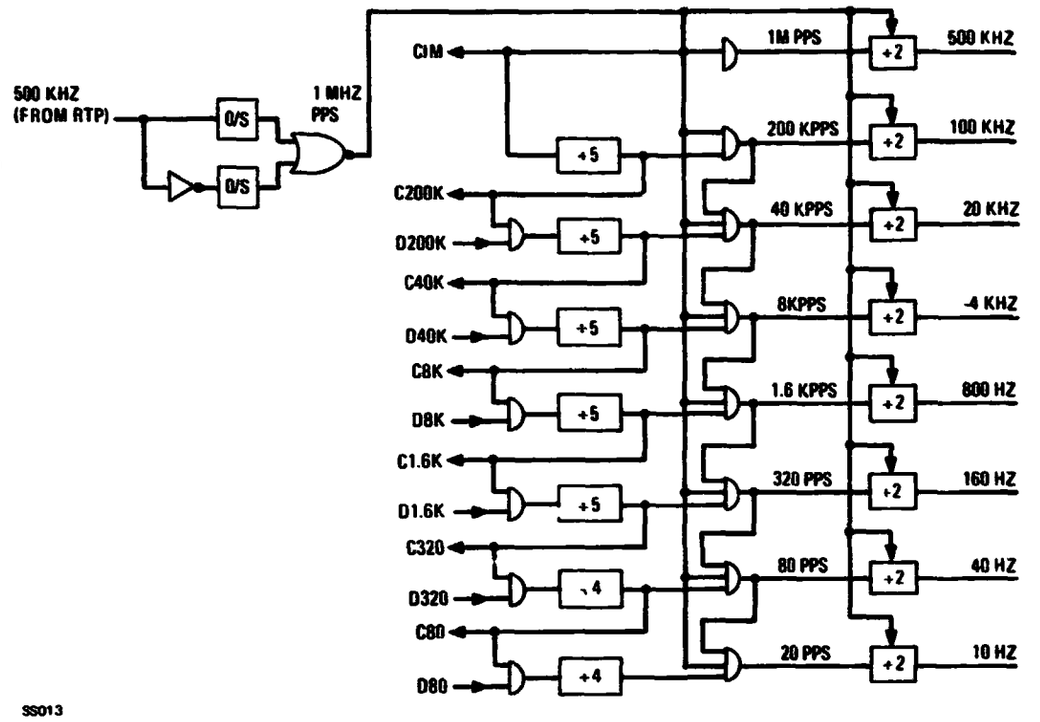

Figure 3.2.8-2. Frequency Divider Chain, Block Diagram

Divider Chain. The pulse deletion technique for phase shifting delays the next transition of the waveform being phase shifted as shown in Figure 3.2.8-3.

The tone selection and sequencer logic receives inputs from the Control Panel, for manual selection of the minor tones and the ARC. Signals are also received from the Interface/Control Logic, for selection of the major range tones, and from the pulse delete logic for sequencing the tone for phase matching in the automatic mode.

The integrate and dump control provides the RTP with integrate and dump timing gates together with switch closure logic to implement the automatic integrator and dump function in the RTP. Time optimization is achieved by utilizing signals from the frequency-divider chain.

3.2.9 LOCAL ARC GENERATOR

The pseudo-random code produced by the Local ARC Generator is the same code produced by the Transmit ARC Generator.

Table 3.2.8-1. Digital Range Tone Extractor Pulse Delete Logic

FIRST COMPARISON RESULT*		ACTION REQUIRED	SECOND COMPARISON RESULT*		ACTION REQUIRED	THIRD COMPARISON RESULT*		ACTION REQUIRED
A	B		A	B		A	B	
1	1	None (wait for next comparison)	1	1	Give in-lock indication			
			Any other		Start over			
0	1	Delete 1 pair of pulses (72°)	1	1	None (wait for next comparison)	1	1	Give in-lock indication
						Any other		Give alarm & start over
			0	0	Delete 3 pairs of pulses (216°)	1	1	Give in-lock indication
			Any other		Start over	Any other		Give alarm & start over
0	0	Delete 2 pairs of pulses (144°)	1	1	Give in-lock indication			
			0	1	Delete 1 pair of pulses (72°)	1	1	Give in-lock indication
						Any other		Give alarm & start over
			Any other		Start over			
1	0	Give alarm & start over						

*Logical states of analog comparator outputs

A. Logic for 160 Hz to 100 kHz Range Tones

FIRST COMPARISON RESULT		ACTION REQUIRED	SECOND COMPARISON RESULT		ACTION REQUIRED	THIRD COMPARISON RESULT		ACTION REQUIRED
A	B		A	B		A	B	
1	1	None (wait for next comparison)	1	1	Give in-lock indication			
			Any other		Start over			
0	1	Delete 1 pulse (90°)	1	1	None (wait for next comparison)	1	1	Give in-lock indication
						Any other		Give alarm & start over
			0	0	Delete 2 pulses (180°)	1	1	Give in-lock indication
			Any other		Start over	Any other		Give alarm & start over
0	0	Delete 2 pulses (180°)	1	1	Give in-lock indication			
			Any other		Start over			
1	0	Give alarm & start over						

B. Logic for 40 Hz and 10 Hz Range Tones

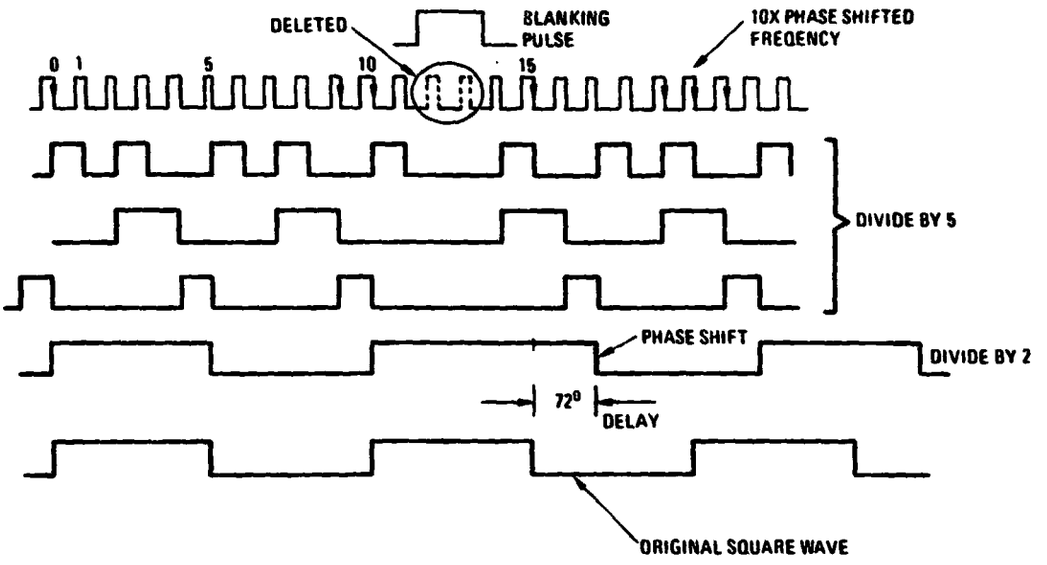

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Figure 3.2.8-3. Pulse Deletion Technique Waveforms

As shown in Figure 3.2.9-1 an ARC reset signal from the DRTE sets the generator to the all 1's state. If the local ARC start signal from the Transmit ARC Generator has been set, the next leading edge of the 10 Hz square wave from the DRTE enables the 160 Hz clock (also from the DRTE) to the 10-stage shift-register generator. The Q7 and Q10 outputs of the shift register are exclusively ORed to produce a 1023-bit pseudo-random code for feedback to the shift register serial input and for input to the Range Tone Processor (via the DRTE tone control) where it is compared for correlation with the received code. If correlation between the received code and the Local ARC Generator code is not detected, it is desired to retard the local ARC by 16 bits or 1/10 second in range and test again for correlation. A shift command (which can be produced manually or automatically from the DRTE with proper sequencing) advances the pseudo-random code 1007 bits which is equivalent to retarding the generator 16 bits. The shift clock is 500 kHz (from the DRTE) and does not disturb the basic synchronization between the received code and the Local ARC Generator. Using this technique, the shift can be accomplished much more rapidly, thus reducing acquisition time.

The all 1's detector circuit provides an output pulse to the Range Counter each time the code cycles through this reference condition.

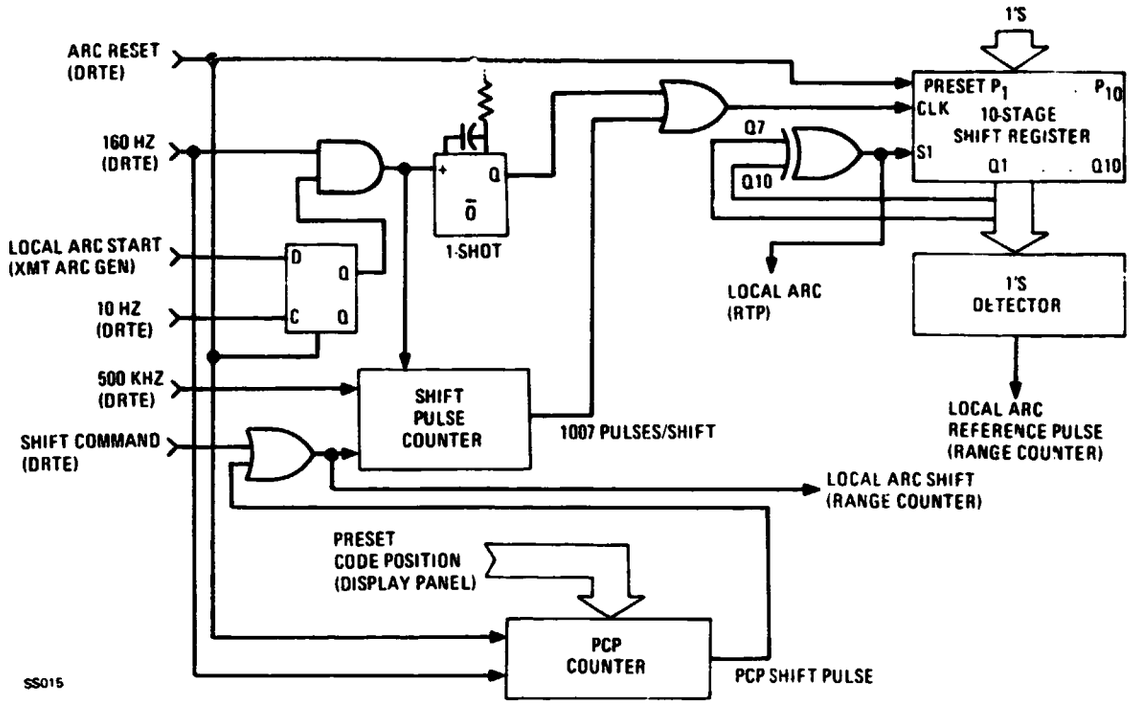

Figure 3.2.9-1. Local ARC Generator, Block Diagram

As indicated in Figure 3.2.9-1, the local code position may be preset using front panel thumbwheel switches.

The Local ARC Generator circuitry is located in the Digital Processor drawer.

3.2.10 RANGE COUNTER

The Range Counter (Figure 3.2.10-1) uses signals from the Phase Data Multiplier (fine data), from the Digital Range Tone Extractor (intermediate data), and from the Transmit and Local ARC Generators (coarse data). The fine, intermediate, and coarse range data are combined to provide a single binary number representing unambiguous range. The number is in units of nanoseconds corresponding to an increment size of approximately 0.15 meter. It has a maximum value of about 4.29 seconds (limited by 32 bit word) corresponding to an unambiguous range of approximately 644,000 kilometers. This binary number is provided as the range data output to the Tracking Data Formatter and is also converted for display.

Fine range is obtained by counting the 40 MHz signal from the Phase Data Multiplier (PDM). The fine data counter (Figure 3.2.10-2) is reset at 20 kHz (also from the PDM).

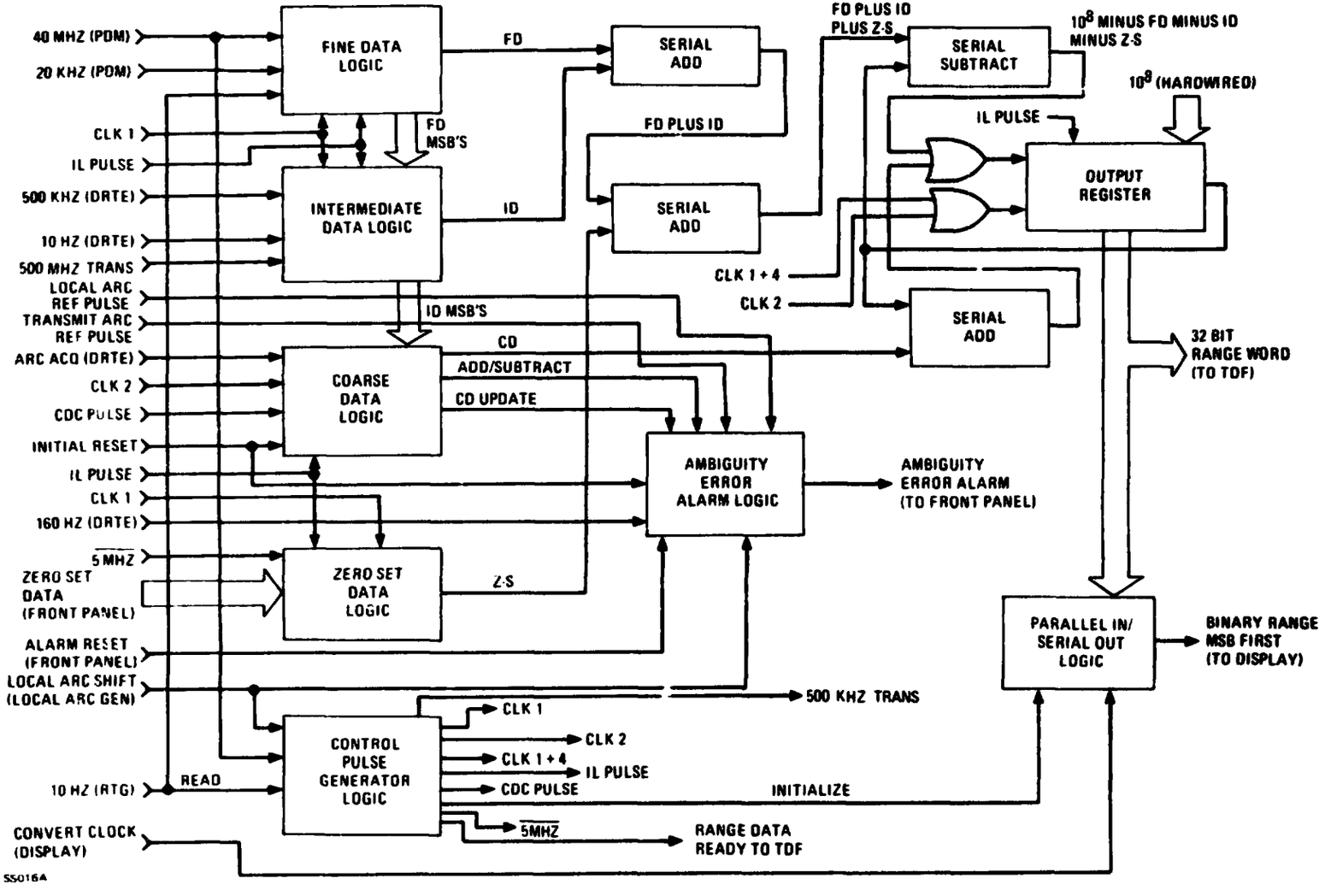

Figure 3.2.10-1. Range Counter, Block Diagram

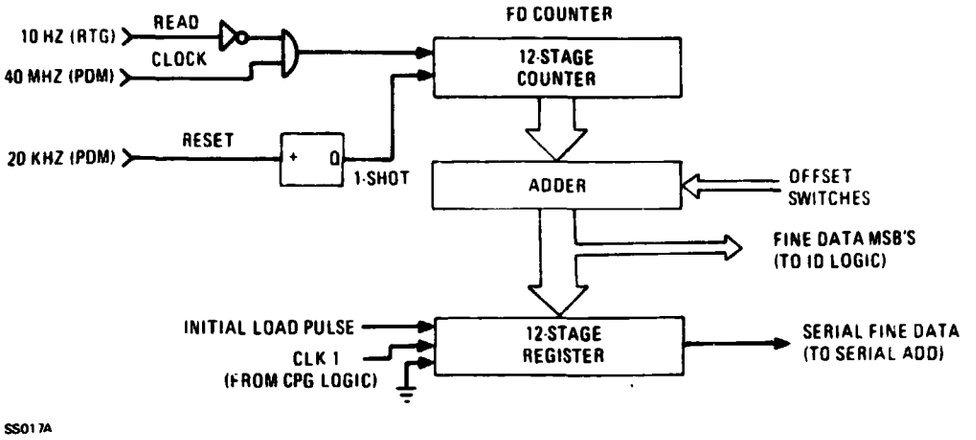

Figure 3.2.10-2. Fine Data Logic, Block Diagram

The counter 40 MHz clock is inhibited on the leading edge of the 10 Hz read signal from the Range Tone Generator (RTG). The 10 Hz read signal also starts the control pulse generator (Figure 3.2.10-1) sequence which begins with the initial load pulse. The output of the fine data counter is transferred to the fine data register by the initial load pulse and then combined with the coarse, intermediate, and zero-set numbers. The fine data counter has a range of 0-1999 with a resolution of 1 nsec. The number represents phase between the transmitted and received major range tone and is ambiguous in 2000 nsec increments. Since the 500 kHz RTP signal and the 20 kHz PDM signal are not guaranteed to have leading edge synchronism, data must be added to the FD counter causing a "spillout" on a 500 kHz transistion.

Intermediate range is obtained by counting the 500 kHz from the DRTE with the value of each count being 2000 nsec. This is accomplished by adding a value of 2000 into an accumulator (Figure 3.2.10-3) for each 500 kHz leading edge. The accumulator is reset by the 10 Hz leading edge from the DRTE. The output of the accumulator is transferred to the intermediate data register by the initial load pulse. To prevent this transfer from occurring while the accumulator is being updated, the initial load pulse is inhibited 200 nsec around the leading edge of the 500 kHz from the DRTE. This condition is indicated by the 500 kHz transition indicator. In the case where the 10 Hz read signal (from the RTG) occurs within 200 nsec before the leading edge of the 500 kHz the initial load pulse will occur after the leading edge of the 500 kHz, therefore causing a range error of +2000 nsec. The ID correction logic detects this case and automatically subtracts 2000 from the intermediate data as it is combined with the coarse, fine and zero-set numbers.

The intermediate range value varies from zero to 99,998,000 nsec with a resolution of 2000 nsec and an ambiguity interval of 0.1 second. Therefore, the combined fine and intermediate numbers can range from zero to 99,999,999 nsec. Since both the fine and intermediate counts are reset (or started) by signals synchronized with the received major range tone and are read by a signal (10 Hz read) synchronized with the transmitted major range tone their combined value must be subtracted from 0.1 second to obtain the delay (ambiguous in 0.1 second increments) in the received 10 Hz minor range tone.

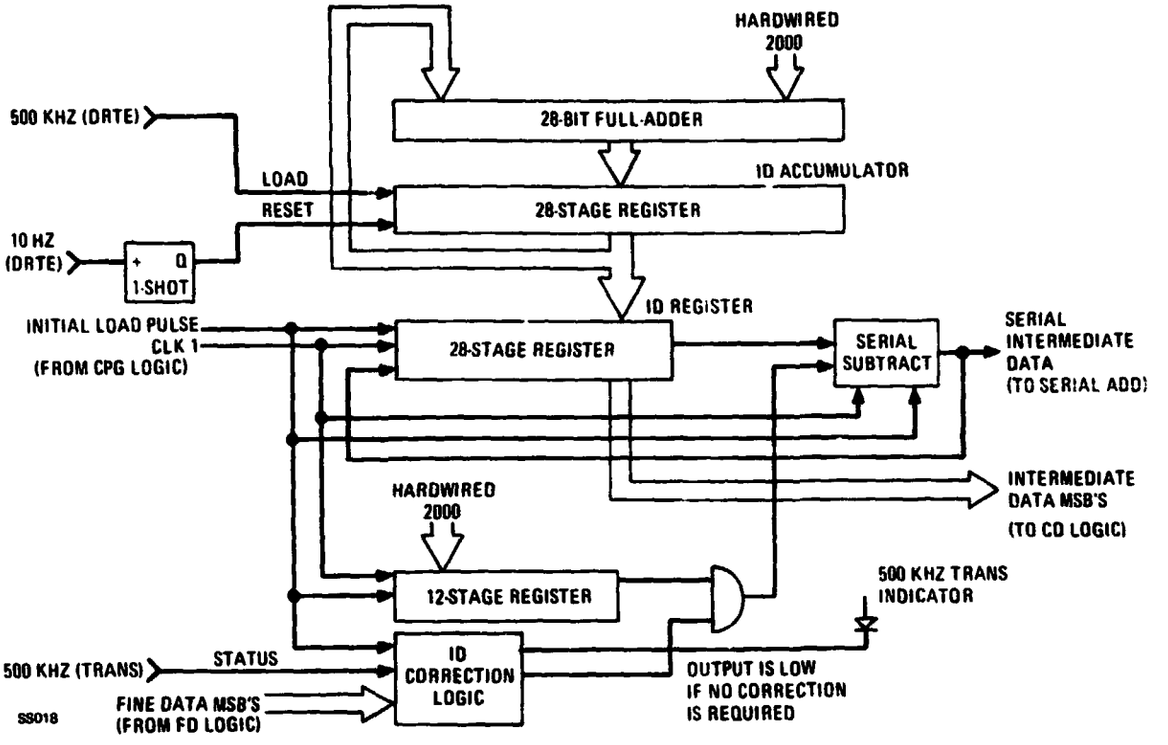

Figure 3.2.10-3. Intermediate Data Logic, Block Diagram

The range zero-set number is transferred from front panel thumbwheel switches into the zero-set data register (Figure 3.2.10-4). It is then combined with the dynamic range data so that the output data is properly calibrated. The zero-set value can range from zero to 999,999 nsec in 1 nsec increments.

Coarse range is obtained initially by counting the shifts required to match the Local ARC Generator output with the received ARC signal during acquisition. The value of each count is 10^8 nsec; see Figure 3.2.10-5. After ambiguities have been resolved during ARC acquisition, the coarse range is updated as a function of the intermediate range value. After the intermediate data is corrected (if necessary) following the read signal, the two most significant bits (MSB's) of the intermediate range number are compared with the MSB's from the previous sample and the coarse range accumulator is updated according to the following logic:

MSB's @ t-1	MSB's @ t	Update
11	00	Subtract 10^8
00	11	Add 10^8
ANY OTHER COMBINATION		No change

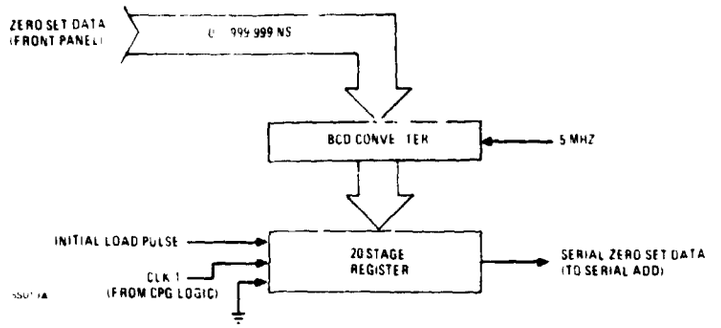

Figure 3.2.10-4. Zero-Set Data Logic, Block Diagram

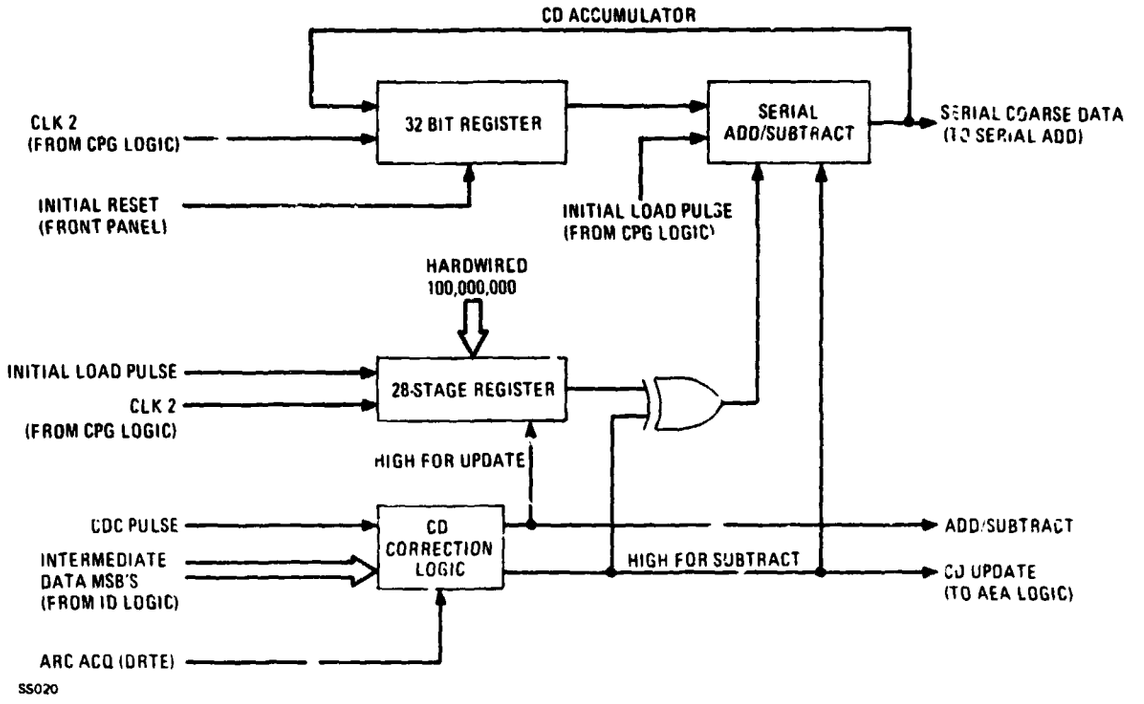

Figure 3.2.10-5. Coarse Data Logic, Block Diagram

The updated coarse range data is then combined with the fine, intermediate and zero-set combination and stored in the output register. The updated coarse range is also loaded into the coarse data accumulator. The output register holds the 32-bit binary range word which can range from zero to 4,294,967,295 nsec (roughly 4.29 sec).

The coarse range is also computed in the Ambiguity Error Alarm logic (Figure 3.2.10-6). The 8-stage UP/DN counter is incremented and updated in the same

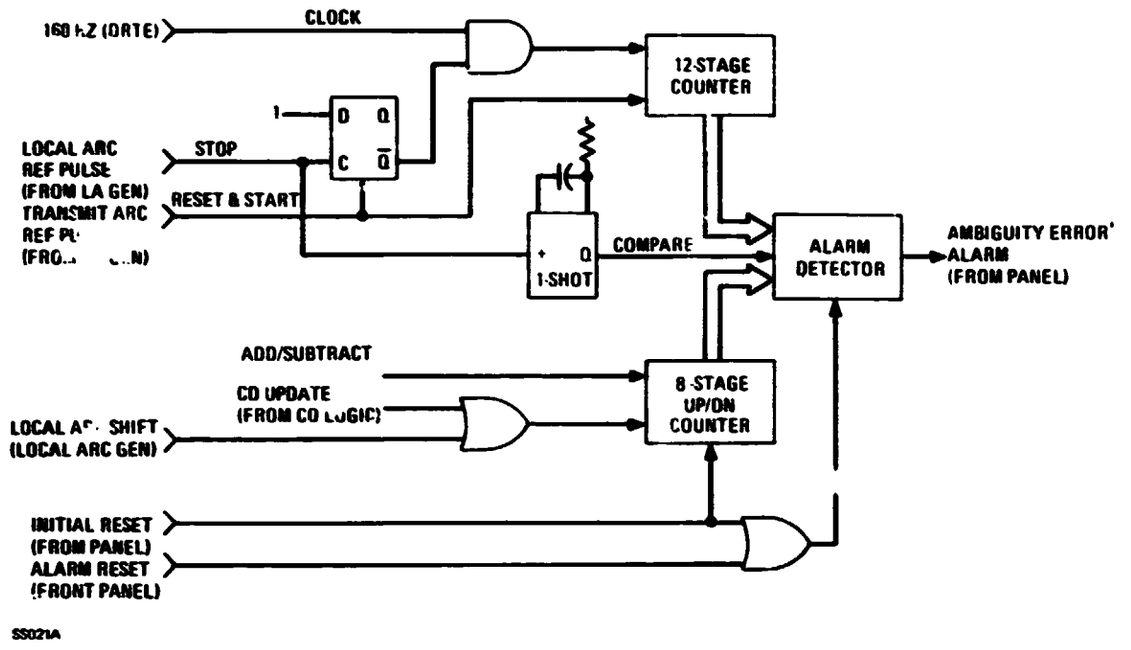

Figure 3.2.10-6. Ambiguity Error Alarm Logic Diagram

manner as the coarse data accumulator. Its resolution, however, is 0.1 second. The 12-stage counter counts at 160 Hz (from the DRTE) starting at zero on the Transmit ARC reference pulse and stopping on the Local ARC reference pulse. When the 2 counter outputs are compared for error, only the 8 most significant bits from the 160 Hz counter are compared thus dividing the count by 16 and giving it a resolution of 0.1 second to compare with the 8-stage UP/ON counter resolution. If an error is detected an ambiguity error alarm signal is sent to the front panel. The outputs are compared for error after every local ARC reference pulse.

The display of range is in units of nanoseconds. The binary number in the output register is transferred to the Parallel In/Serial Out Logic (see Figure 3.2.10-7) where it is stored until the convert clock (from the display) transfers it out, MSB first, to the display where it is converted to BCD for display. The display is updated once every 0.4 seconds.

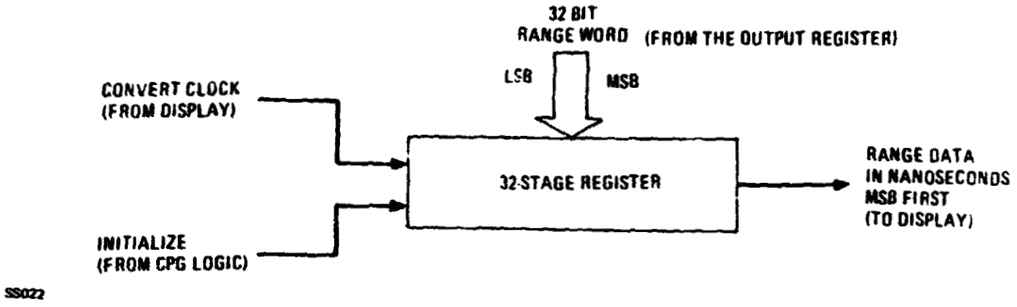

Figure 3.2.10-7. Parallel In/Serial Out Logic

3.2.11 SIMULATION RANGE SIGNAL GENERATOR (RSG)

The Simulation Range Signal Generator provides a capability for static or dynamic range simulation. For static range simulation, the transmitted ranging signal (modulation) is delayed by any preselected value over the entire unambiguous range capability of the system. The selectable delay increment size is 1 nanosecond, or nominally 0.15 meter of one-way range. Thus, any range may be simulated to a resolution equal to the range measurement system resolution. For dynamic range simulation, the transmitted ranging signal contains a simulated doppler component which is in exact proportion to simulated carrier doppler. Thus, the output range data is dynamic and "tracks" with the carrier doppler data.

The Simulation Range Signal Generator and its relation to the normal Range Signal Generator is illustrated in Figure 3.2.11-1. The Simulation RSG contains a range tone generator and transmit ARC generator which are very similar to those used in the normal mode of operation. In addition, it contains preset counters, synchronous dividers, a mixer, and a filter to implement the selectable delay.

3.2.11.1 STATIC RANGE SIMULATION — For static range simulation, the output tones and ARC are time delayed relative to the normal tones and ARC in accordance with the programmable counter selections. The programmed delay is maintained relative to the normal modulation by synchronizing to the 10 pps "on-time" pulse train from the normal RTG.

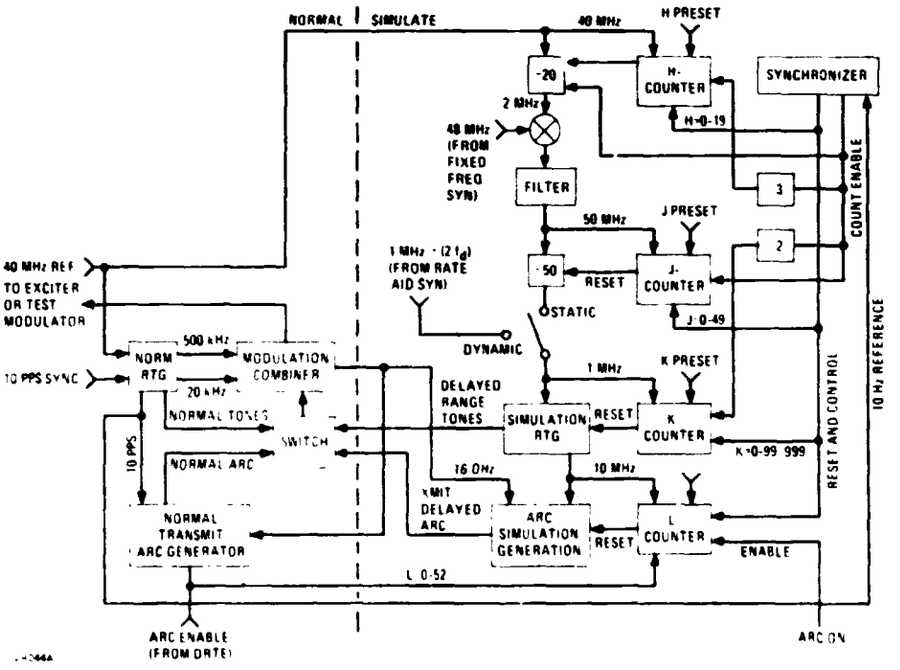

Figure 3.2.11-1. Relationship of Simulation and Normal Range Signal Generators, Block Diagram

The H-counter is programmable from 0 to 19, and delays the range modulation output from 0 to 19 nanoseconds in one nanosecond increments. The 1 nanosecond resolution is achieved by the offset-mixer which scales the delay increment from 25 to 1 nanoseconds. Thus, the H-counter can delay the phase of the 500 kHz in 19 increments of 1 nanosecond each.

The J-counter is programmable from 0 to 49 and delays the range modulation output in 20 nanosecond intervals from 0 to 980 nanoseconds. Thus, the H and J counters combined delay the modulation output in 1 nanosecond increments from 0 to 999 nanoseconds.

The K-counter is programmable from 0 to 99,999 and delays the range modulation output in 1 μsec intervals. The H, J, and K counters combined delay the modulation output in 1 nanosecond increments from 0 to 0.099,999,999 seconds. The L-counter is programmable from 0 to 62 and delays the ARC output from 0 to 6.2 seconds in 0.1 second increments. The delay is relative to the normal Transmit ARC Generator code output and is synchronized by a reset signal from the normal ARC generator.

The total combined delay from the H, J, K, and L counters delay the modulation output in 1 nanosecond increments from 0 to 6.299,999,999 seconds. Encoding of the preset counters is achieved by manually inserting the desired delay into 10 thumbwheel switches located on the front panel.

The synchronizer circuit for the Range Simulator receives the 10 Hz reference from the normal RTG and the preset insert pulse, activated manually from the front panel. The synchronizer outputs a preset load pulse and a count enable signal synchronized to preload and which then start the counters coherent with the 10 Hz reference. At the first 10 Hz, the divide-by-20 that produces the 2 MHz is enabled to ensure a stable 50 MHz on the second 10 Hz received. At this time 20 nanosecond delays are produced by deleting 50 MHz pulses from the J preset input. The K and L counters delete pulses sequentially after the completion of the 50 MHz deletions. Since the 50-MHz is phase shifted by the 40-MHz in 1 nanosecond increments (after the third 10-Hz) deleting the 50-MHz first ensures that synchronizing the 50-MHz with respect to the 10-Hz does not produce a variable delay in the range of ± 10 nanoseconds.

The Simulation Range Tone Generator (Figure 3.2.11-2) uses the same divider chain employed in the normal RTG. Phase coherency is produced at the preset count in the combined H, J, and K counters after the 10 Hz reference.

For producing ambiguities in the 10 Hz range tone, the Simulation ARC Generator produces a pseudo-random code the same as the Transmit ARC and the Local ARC. The 160 Hz clock is obtained from the Simulation RTG. As shown in Figure 3.2.11-3,

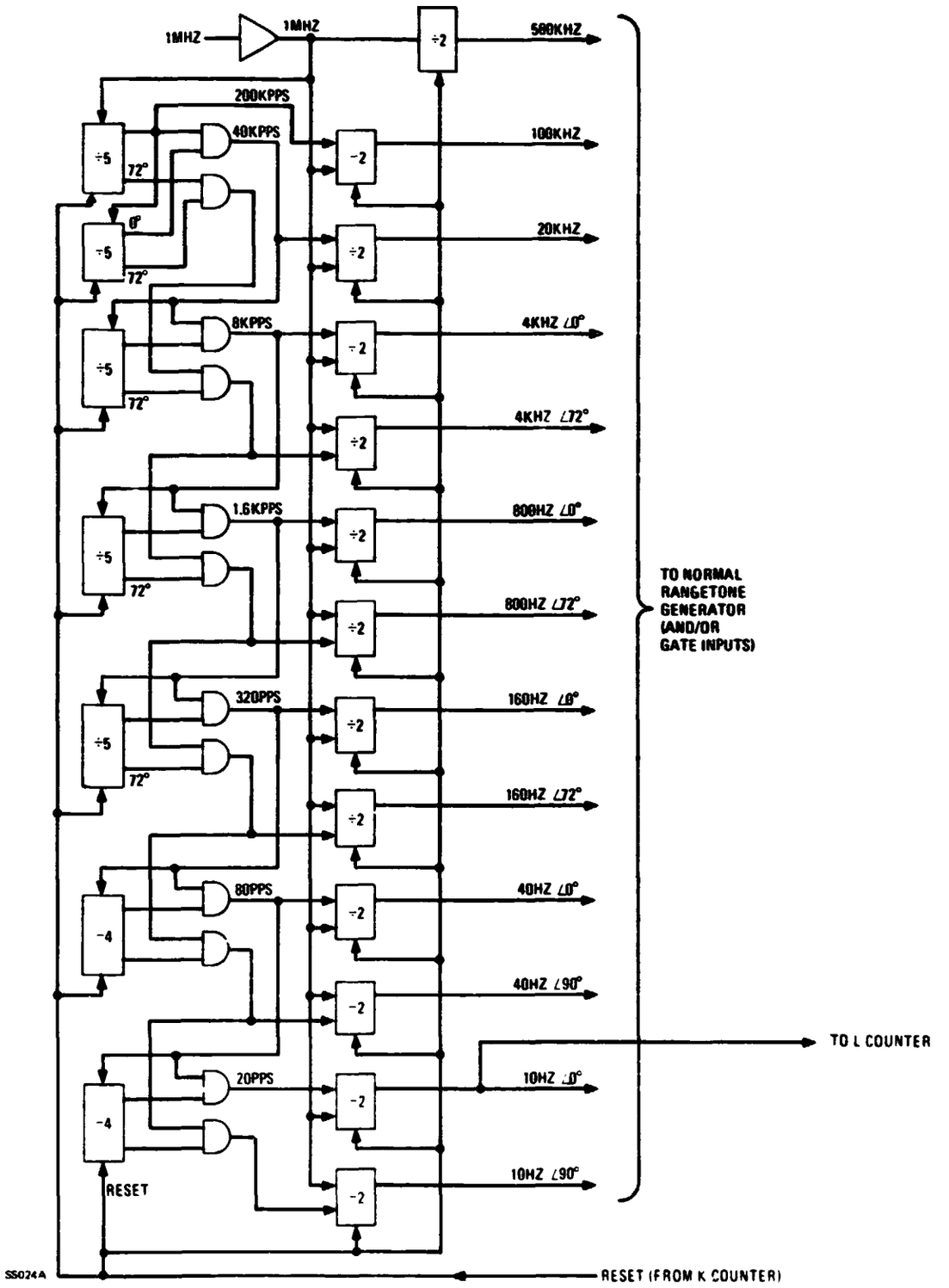

Figure 3.2.11-2. Simulation Range Tone Generator, Block Diagram

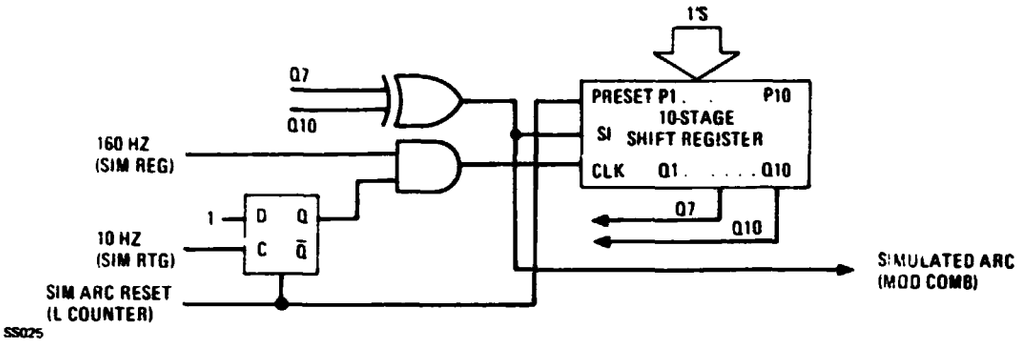

Figure 3.2.11-3. Simulation ARC Generator, Block Diagram

an all 1's detector isn't used here since the Simulation ARC Generator is only used to produce a delayed ARC bit stream which is switched to the Modulation Combiner in place of the Transmit ARC output during simulation.

The 10-stage shift register is preset by the Simulation ARC Reset signal (from the L Counter) which is delayed by a multiple of 1/10 second from the normal ARC Reset. The next leading edge of the 10 Hz square wave from the Simulation RTG enables the 160 Hz shift register clock.

The LC bandpass filter at 50 MHz reduces the major undesired signal, the lower sideband at 46 MHz, to 15 dB below the 50 MHz signal by virtue of being a 2-pole design with a Q of 16. The expected phase drift with temperature variation is reduced by the following ÷100 circuit so that at 500 kHz, the phase drift is very small.

3.2.11.2 DYNAMIC RANGE SIMULATION – For dynamic range simulation, the modulation signal from the Simulation RSG is provided with a doppler component which is in the exact proportion to simulated carrier doppler. The doppler is introduced by driving the Simulation RTG with a 1 MHz + 2 x 500 kHz doppler signal specially derived in the Rate Aid Synthesizer (see 3.2.5). In the case of dynamic range simulation, the H and J counters have no effect on the output since they affect only the 1 MHz static signal which is not used. However, the K and L counters do operate and set the initial phase of the 100 kHz and lower frequency ranging signals.

3.2.12 TEST MODULATOR

This unit provides the proper ranging spectrum for testing the Ranging Equipment. The phase modulation is performed at 22 MHz, derived from a phase shiftable 11 MHz source. See Figure 3.2.12-1. The phase shifter is necessary because the 110 MHz

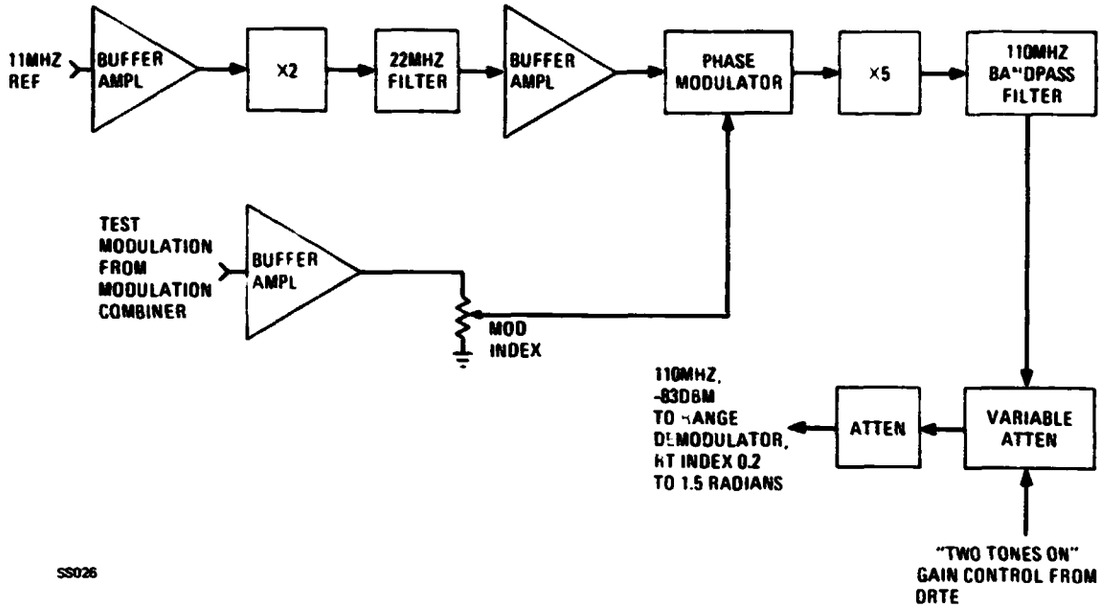

Figure 3.2.12-1. Test Modulator, Block Diagram

output must be at the same phase as the received 1[illegible] MHz signal to achieve the same output level from the Range Demodulator phase detector. The output of the modulator is multiplied by 5 to develop the 110 MHz output. This multiplication allows a lower index at the modulator and thus good linearity. The output level is increased via a variable gain amplifier to keep the major range tone at a constant level, (i.e., what the MFR does by means of AGC) with or without a minor tone applied.

3.2.13 DOPPLER EXTRACTOR

The Doppler Extractor combines signals from the MFR, the Exciter, and the Fixed Frequency Synthesizer to produce an output consisting of a 70 MHz fixed bias frequency plus the two-way carrier doppler frequency, as shown in Figure 3.2.13-1. The doppler data is contained in the MFR VCXO and Frequency Synthesizer frequencies while the actual operating frequency is contained in the Exciter Reference frequency.

The most critical filtering is within the ρ multiplier circuitry. As in the case of the 55 MHz reference from the Fixed Frequency Synthesizer, all spurious which would fall within the 60 kHz tracking bandwidth of the doppler multiplier must be suppressed

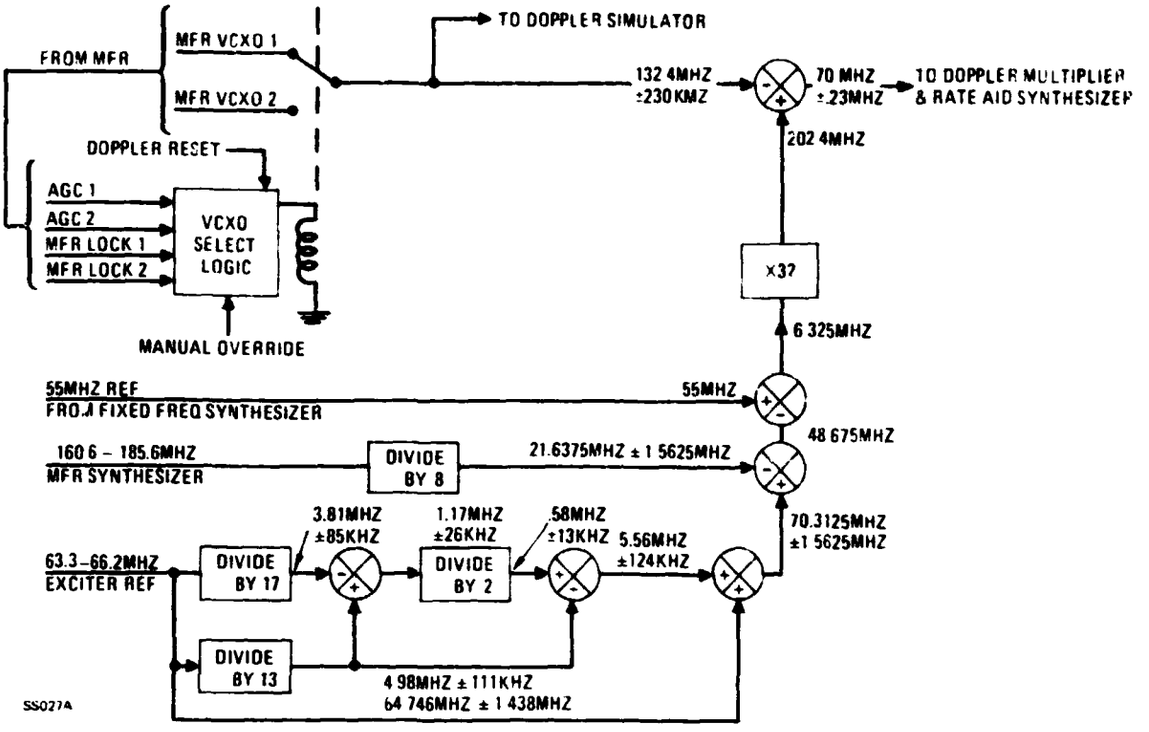

Figure 3.2.13-1. Doppler Extractor, Block Diagram

by greater than 65 dB at the input of the ×32 multiplier. An analysis shows, that the worst-case filtering is required following the mixing of 0.58 MHz ±13 kHz (F_O) with 4.98 MHz ± 111 kHz (F_X) to obtain 5.56 MHz ± 124 kHz. To suppress F_X to the required level two cascaded 3-pole filters are required following the mixer. All other filtering is accomplished by lower order filters.

The frequency division required for the signals from the MFR Synthesizer and the exciter reference is accomplished through the use of ECL high-speed digital logic. This logic series has an additional advantage of being able to directly drive low impedance loads and transmission lines.

The ×32 multiplier is configured utilizing conventional multiplying techniques. The first two stages consist of active double balanced modulators with their inputs capacitively coupled. When wired in this manner the output is the second harmonic of the input. A hot carrier diode quadrupler followed by a hot carrier diode doubler completes the multiplication chain.

The VCXO select logic is designed to switch to the MFR VCXO with the highest AGC level provided that the corresponding VCXO is locked. Selection evaluation occurs only upon a change in MFR lock status. A manual override feature is also incorporated.

The circuitry of the Doppler Extractor is located in the High Frequency Processor Drawer.

3.2.14 DOPPLER MULTIPLIER

The function of this unit is to multiply the carrier doppler information by 250 to contribute to data digitizing in increments of 1/1000 cycle, as shown in Figure 3.2.14-1.

The bias (70 MHz) plus doppler is mixed with a stable reference signal at 69 MHz to lower the bias frequency to 1.0 MHz. Frequency multiplication by a factor of 250 is then performed using a phase-locked loop (PLL). The PLL low-pass filter is designed to yield a second-order tracking loop with a tracking bandwidth of approximately 60 kHz. This bandwidth is made wide to reduce self-generated VCO noise via feedback and to insure good acquisition and Doppler rate tracking performance. In the absence of an input signal the VCO offset voltage is small enough to ensure the VCO frequency will be within the lock-up range of the loop.

The VCO is an octave range, VHF transistor, varicap tuned oscillator. Because of the octave range tuning of the oscillator, the phase noise is contained in a relatively wide bandwidth; but with the wide tracking loop bandwidth (60 kHz), the VCO noise is greatly reduced so that the loop output signal is sufficiently stable. Due to the nonlinear nature of this VCO, the bandwidth varies over the operating range from approximately 110 kHz to 35 kHz. It also puts out approximately 4 dB more power at the high frequency end and results in causing resetting at the high end whenever the loop becomes unlocked. This action necessitates a RESET whenever a new input frequency is likely to be acquired. This RESET makes a one-time sweep through the VCO control range.

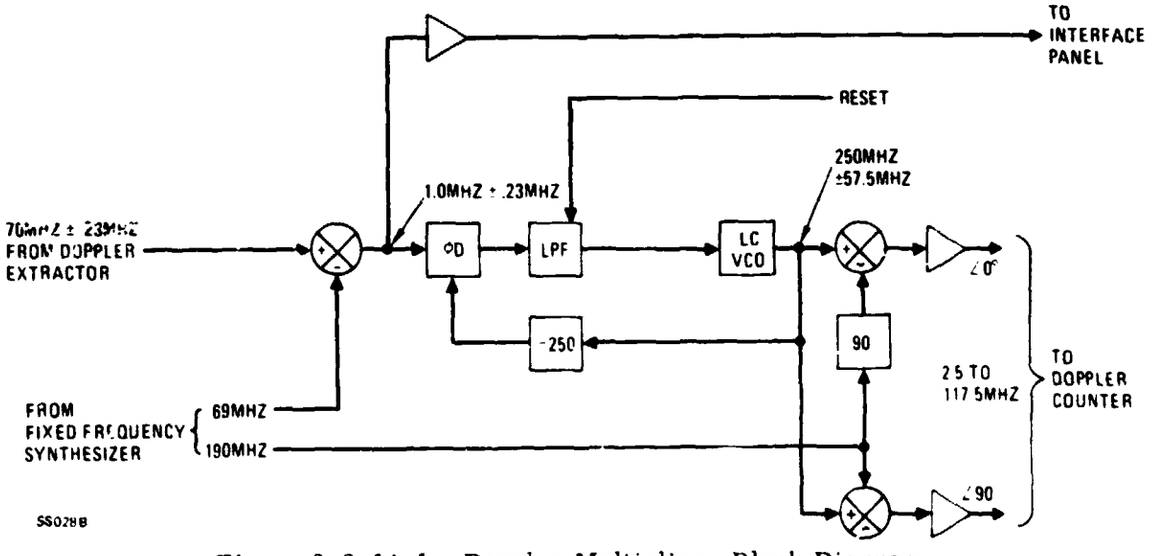

Figure 3.2.14-1. Doppler Multiplier, Block Diagram

To close the loop, a divider circuit divides the VCO frequency by 250: the output is then used as the reference for the phase detector. The first two stages of the divider utilize ECL UHF flip-flops.

The VCO output is then mixed with a 190 MHz reference signal to reduce th bias frequency to 60 MHz where it can be more readily counted. Two outputs are furnished to the doppler counter 90° apart to facilitate digital multiplication of ×4 thus accomplishing data incrementation in 1/1000 of a cycle. As in the Doppler Extractor all fixed-tuned filtering is made relatively broadband to minimize phase shifts due to frequency change. This is essential to reduce error in the output doppler count.

The circuits to implement the Doppler Multiplier are located in the High Frequency Processor drawer.

3.2.15 DOPPLER COUNTER

The Doppler Counter (Figure 3.2.15-1) accepts the output of the Doppler Multiplier which varies from 2.5 MHz to 117.5 MHz as a function of carrier doppler varying from -230 kHz to +230 kHz. There are two outputs. First is a 42 bit binary output that is provided to the Tracking Data Formatter (TDF) at a 10 per second rate: this binary number is an accumulation of the bias-plus-doppler count since an initial start time and, at maximum doppler, overflows in about 156 minutes. The second output is to a decimal display and is an accumulation of the doppler count for a 0.1 second sampling interval.

To achieve a resolution of 10^{-3} cycles with a straightforward counting technique would require counting at a frequency in excess of 460 MHz, (for maximum positive doppler) and either reading the counter "on the fly" or switching counters. To avoid this state-of-the-art risk a lower frequency f_{in} (117.5 MHz max) is input in quadrature with phases designated as f_{in_0} and $f_{in_{90}}$. The phase f_{in_0} is counted directly and provides the coarse resolution (4 parts in 10^{-3} cycles). Both phases f_{in_0} and $f_{in_{90}}$ are compared at the time of the 10 pps read pulse to yield the required 1 part in 10^{-3} cycles resolution.

The frequency f_{in_0} is given by

$$f_{in_0} = 250\ (240\ \text{kHz} + f_d) = \frac{10^3}{4}\ (240\ \text{kHz} + f_d)$$

where

240 kHz = bias frequency

f_d = Doppler frequency $\left[-230\ \text{kHz} \leq f_d \leq +230\ \text{kHz}\right]$

The maximum counting frequency f_{in_0} is 117.5 MHz corresponding to a doppler frequency of +230 kHz. The LSB of the counter has a binary weight of 2^2 and effectively

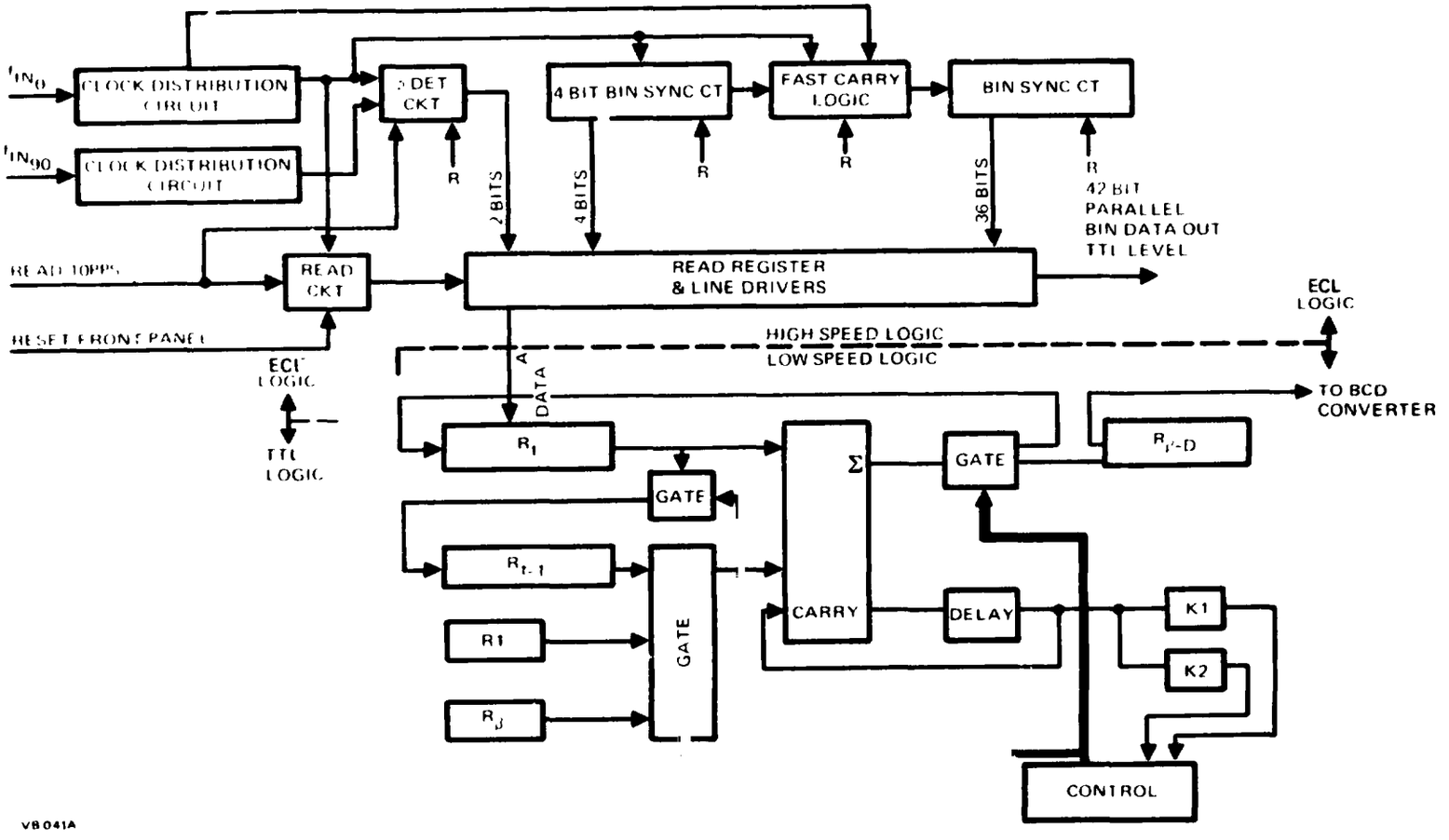

Figure 3.2.15-1. Doppler Counter, Block Diagram

multiplies f_{in0} by 4. Binary weights of 2^0 and 2^1 are determined from the phase comparison circuit at read time and added to the value in the counter. The addition does not create a carry and is achieved by tagging the 2 bits of the phase comparison as the LSB's of the overall count and transferring these two bits and the count in the counter to a holding register at the time of the read pulse. Each sample period increases the value of the holding resistor by 10^3 (240 kHz + f_d). The resolution is 1 part in 10^{-3}.

Referring to the block diagram, the control logic circuit in the low speed logic section operates to transfer the doppler count of the previous read pulse to register (t-1) and the doppler count of the present read pulse to register (t). The input to register (t) is also transferred in parallel to the Tracking Data Formatter transfer logic for input to the TDF. This data is the sum of all previous counts since the initial start time. The new cumulative count is available at the formatter no later than 2 microseconds after occurrence of the 10 pps on-time sample pulse.

Although this slight delay exists in getting the data to the TDF and ready for readout, it is emphasized that the data was "dumped" (sampled) precisely (within 25 nanoseconds) on time and thus corresponds to the true doppler count (within a fraction of a count) at the precise time of the 10 pps sample pulse.

For display purposes only, the display and difference logic takes the difference of the accumulated reading (t) - (t-1) and subtracts the bias frequency (240 kHz x 10^3) from this difference. Thus, if the input is 117.5 MHz for 1/10 second corresponding to a doppler of 230 MHz, the count in the counter is 4 x 11.75 x 10^6 = 47,000,000: subtract 0.1 x 240 x 10^6 = 230,000.00. If the input corresponds to minimum doppler of -230 kHz the count is 4 x 0.25 x 10^6 = 1,000,000; subtract 0.1 x 240 x 10^6 = -230,000.00. At this point, the number is still in binary form. The control logic provides shift pulses to transfer the data to the serial-binary to parallel-BCD converter for decimal display. The BCD converter control logic accepts new data and updates the display only once per second.

At a maximum input frequency of doppler-plus-bias of 117.5 MHz (a period of 8.51 nsec) device delay times of a few nanoseconds become significant. The critical design problem is to construct the counter such that at read time the count can be extracted without stopping the counter and without upsetting the accumulating count. In short, the count difference t - (t-1) between any two read pulses must be accurate to ±1 count.

The counting unit (Figure 3.2.15-2*) is divided into four parts:

1. A four-stage high-speed synchronous counter generating intermediate resolution

*For convenience bound as Appendix A.

2. A 36 binary bit synchronous counter accumulating carrier (coarse data) from the high speed counter
3. A phase comparison circuit generating fine count data
4. A read pulse synchronizing circuit to transfer the count at read time to the holding register after the counter outputs have settled

The four-bit synchronous counter utilizes MECL 10231 "D" flip-flops and 10105 gates having propagation delays of 3.3 nsec. Thus, the maximum counting speed is about $10^9/6.6 = 150$ MHz. This is sufficiently above the required 117.5 MHz to guarantee reliable operation. The carry generation is started at counter state 1110 (see waveform diagram Figure 3.2.15-3). The carry gate is enabled 3.3 nsec after counter state 1111 and is ANDed with state 1111 clock (negative logic). The positive-going edge of the carry gate clocks the coarse counter stages advancing the count 1 bit (weight of 2^6). A carry is generated every 136.16 nsec. Set-up time for the MECL 10231 flip-flop is 1 nsec and is below the maximum counter set-up time of 1.91 nsec. The coarse counter consists of 9 stages of a MECL 10136 synchronous hexadecimal counter. The carry out of one stage is input to the succeeding stage and overrides the common clock (carry output of the four-bit counter) thus allowing devices to be cascaded to provide a fully synchronous counter. Propagation delay from clock input to data out is 5 nsec, worst case, and from clock input to carry out is 11.5 nsec worst case, thus for 9 stages a worst-case propagation delay of 103.5 nsec

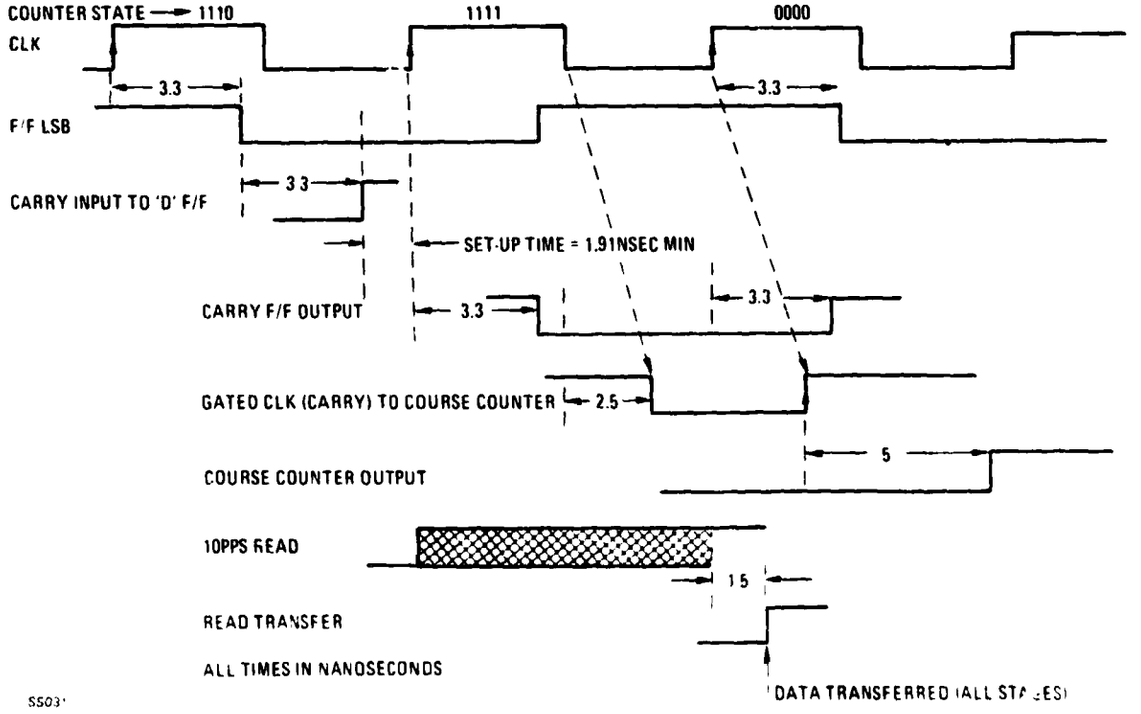

Figure 3.2.15-3. High Speed Counter Waveforms

exists from the clock until the last carry out has settled. The carry clock input has a repetition period of over 136 nsec which is well in excess of the propagation delay.

The phase comparison circuit consists of two MECL 10231 "D" flip-flops commonly clocked by the positive-going edge of the read pulse. Each flip-flop has one phase of the clock as the D inputs as shown in Figure 3.2.15-2. When the flip-flops are clocked by the read pulse the clock phases are transferrred to the output and held until the transfer pulse transfers the data to the holding register. Each positive going edge of CLK_0 advances the four stage counter 1 bit (weight of 2^2). Referring to Figure 3.2.15-4, the quadrature relationship has four states: 0, 1, 2, and 3 (overall count weights of 2^0 and 2^1). The state at read time is 'latched', decoded and appears at the input to the transfer register in binary for subsequent addition to the overall count.

The read pulse synchronizer circuit implements transferring the counter count to the holding register on the next positive read edge. This insures transferring data while it is stable and not going through a transition. To satisfy the above condition, the read pulse synchronizer must clock the holding register within 3.3 nsec (worse case) of the positive going edge of CLK_0 (see Figure 3.2.15-3). Thus, the propagation delay of the device must be less than 3.3 nsec. The flip-flop used in this application is a MECL III MC1690 having a propagation delay of 1.5 nsec. The cross-coupled gate serves to release the counter reset at the first read pulse after an initial reset has been activated from the front panel.

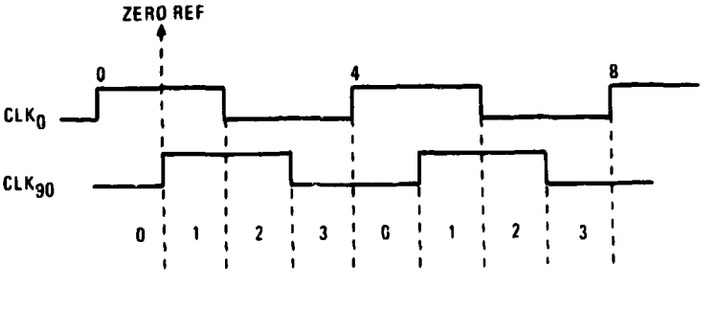

Figure 3.2.15-4. Phase Comparator Waveforms

3.2.16 DOPPLER SIMULATOR

The Doppler Simulator (Figure 3.2.16-1) provides test signals to exercise the Doppler Data Extractor over simulated doppler excursions of -230 kHz to +230kHz in increments of 0.001 Hz.

The simulator operates in either the normal mode or one of two simulation modes: Bypass Simulate and Normal Simulate. The doppler simulation capability is exactly the same for both simulation modes.

In the normal mode, the MFR VCXO, the MFR Synthesizer and the Exciter reference ($F_t/32$) are provided to the Doppler Extractor from the Doppler Simulator while a 55 MHz reference is also provided from the Fixed Frequency Synthesizer.

For the bypass simulation mode, the Doppler Simulator provides substitute signals generated within the Fixed Frequency Synthesizer for the MFR VCO, the MFR Synthesizer, and the Exciter reference signal ($f_t/32$). These signals provide the capability of exercising the entire Doppler Data Extractor. The substitute MFR VCO is provided by a variable frequency synthesizer which provides a ±0.230 MHz frequency variation in 0.001 Hz steps to simulate the maximum doppler.

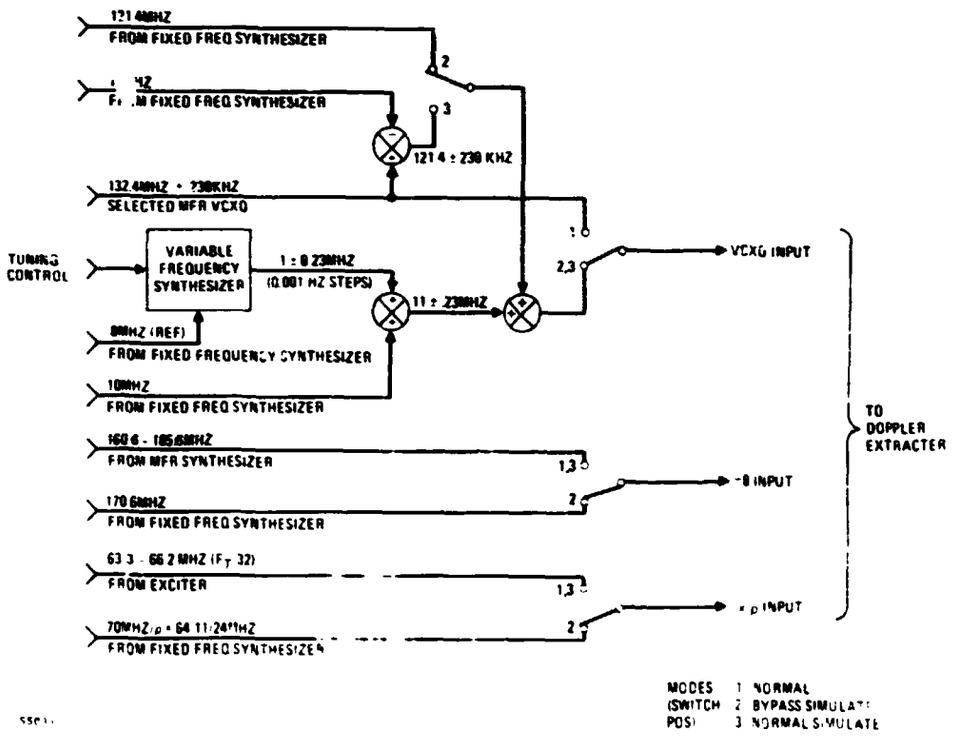

Figure 3.2.16-1. Doppler Synthesizer, Block Diagram

The synthesizer is a Rockland Model 5100 modified by removing all controls and monitors from the front panel with the exception of the POWER ON/OFF switch and a 1 volt P/P signal monitor jack. As can be verified by the signal coherence diagram Figure 3.2.16-2A, this test mode maintains full system coherence and thereby provides completely controlled doppler simulation with a predictable doppler data output.

In the normal simulate mode, the Doppler Data Extractor is exercised while connected to and using the input signals from the MFR and the Exciter. This is accomplished by using the MFR synthesizer and Exciter reference signals as in the normal mode while modifying the MFR VCO signal by adding simulated doppler. As in the other mode this simulation mode also exercises the Doppler Data Extractor over a range of 0 to ±230 kHz in 0.001 Hz steps while maintaining system coherence. Signal flow and coherence in this mode is shown in the signal coherence diagram Figure 3.2.16-2B.

The implementation of the Doppler Simulator is shown in Figure 3.2.16-1. Inputs are from the MFR, Exciter, Fixed Frequency Synthesizer and the Doppler frequency Synthesizer. All remaining signals are generated using conventional mixing and filtering techniques. In generating the transmit reference simulation signal (64-11/24 MHz), sidebands at 40 kHz, where encountered, result in a 70 MHz doppler signal into the doppler multiplier with the 40 kHz sideband down ≈35 dB. This results in a doppler count jitter of ≈8 counts rms.

The circuitry comprising the Doppler Simulator is housed in the High Frequency Processor Drawer. The Doppler Synthesizer is a separate self-contained chassis.

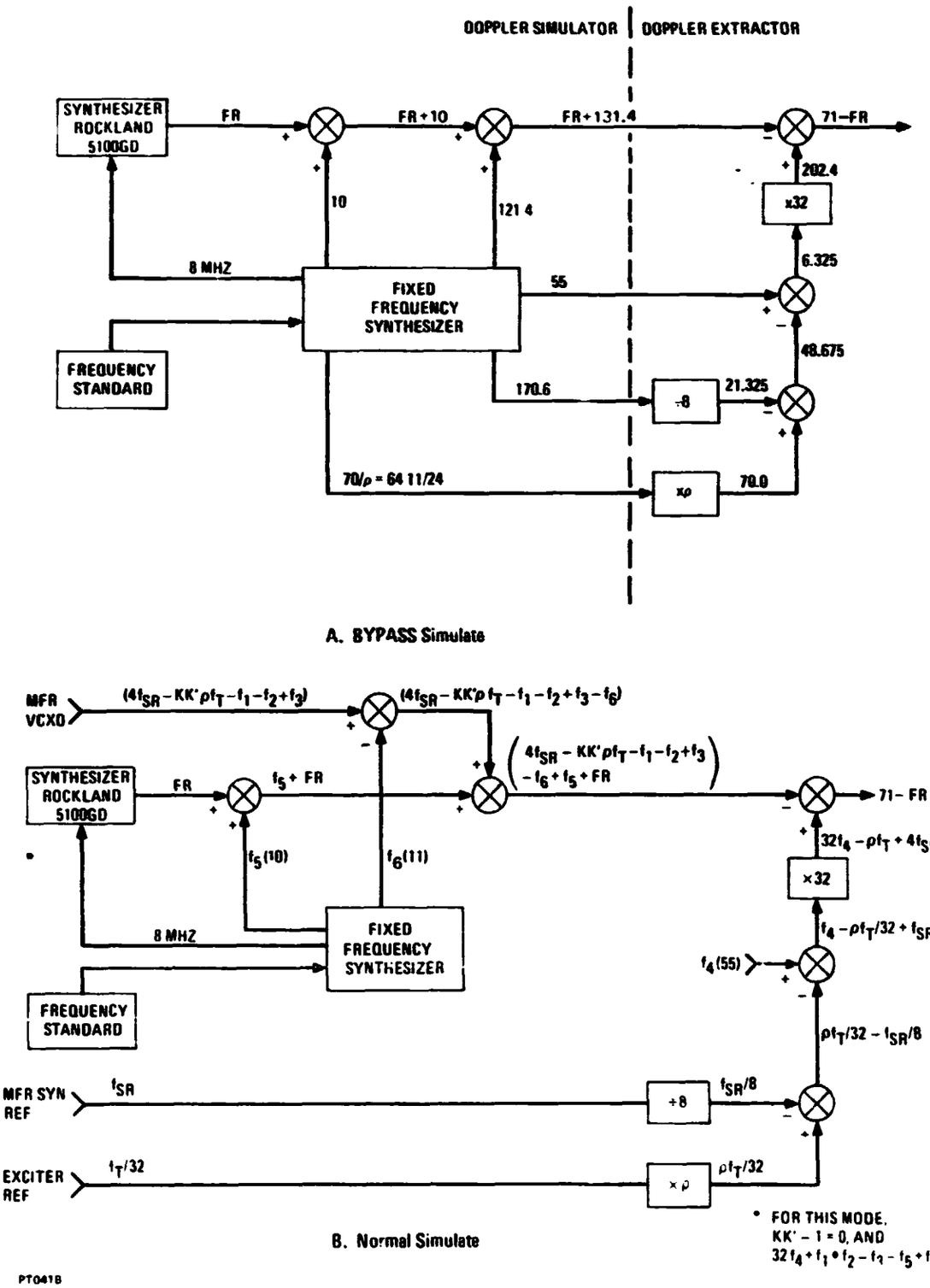

Figure 3.2.16-2. Doppler Simulator, Coherence Diagrams

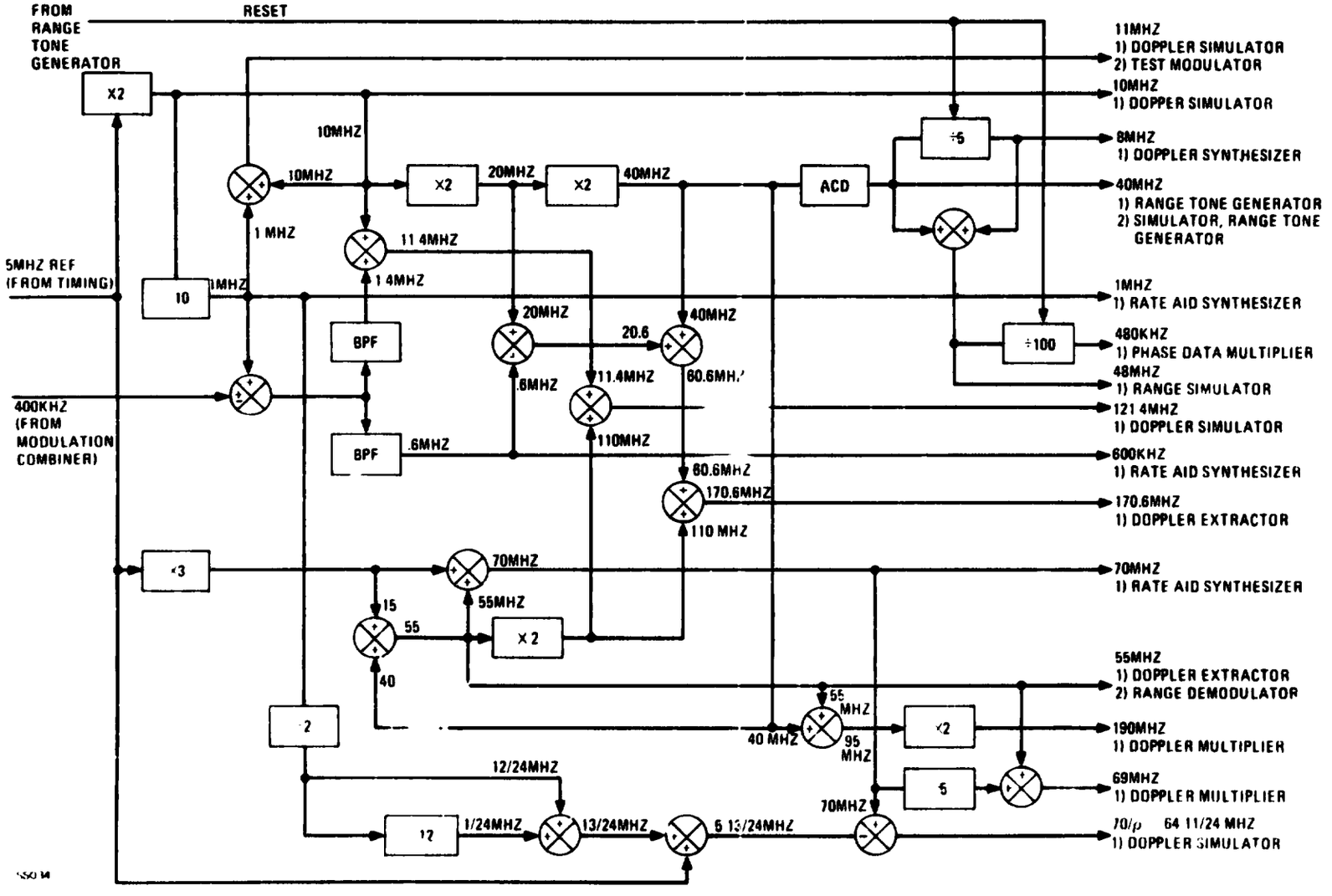

Figure 3.2.17-1. Fixed Frequency Synthesizer, Block Diagram

3.2.17 FIXED FREQUENCY SYNTHESIZER

Fixed frequency reference signals for use throughout the Ranging Equipment are generated in the Fixed Frequency Synthesizer. All the fixed frequencies are generated from two references: a 5 MHz reference from the frequency standard in the Station Timing System, and a 400 kHz reference from the Modulation Combiner. As shown in Figure 3.2.17-1, the frequencies are synthesized using conventional mixing, multiplication, division, and filtering techniques; for clarity the amplification and filtering stages have not been shown.

An analysis of the phase noise requirements in the Doppler Multiplier phase locked loop indicates that all reference frequencies generated for use in the Doppler Extractor with the exception of the 170.6 MHz reference must have a minimum of 65 dB suppression of the spurious signals which fall within the 60 kHz tracking bandwidth. This somewhat stringent requirement is due to the > 32 (+30 dB) multiplication of the fixed reference frequencies within the Doppler Extractor. Since the 170.6 MHz reference is divided by eight prior to its multiplication, an improvement of approximately 20 dB in its phase noise will be obtained. The spurious suppression requirement for this reference is therefore 45 dB. All other fixed frequencies generated within the Fixed Frequency Synthesizer are required to have all spurious signals suppressed by greater than 35 dB.

3.2.18 INTERFACE/CONTROL LOGIC

The Interface/Control Logic (Figure 3.2.18-1) interfaces the Ranging Equipment with a computer and a Tracking Data Formatter. The computer can monitor the RE by examining the contact closures applied to the computer. When the local/computer control (from the front panel) is in the computer position the computer can directly control the RE with TTL compatible logic levels applied to the computer control inputs. Range and doppler data with RE status lines are supplied to the TDF as TTL logic levels; see Figure 3.2.18-2. Where multiple parallel data lines are used, a common ground connection will be used.

3.2.19 AC/DC POWER

A single breaker mounted on the AC POWER panel controls application of the 60 Hz, single-phase 115 Vac power to the Ranging Equipment. Whenever power is applied, a green incandescent ON indicator is illuminated and an elapsed time meter energized.

The elapsed time meter provides a total registration of 9999.9 hours. Two ac line filters are mounted at the rear of the chassis to reduce radio frequency emanations from the Ranging Equipment.

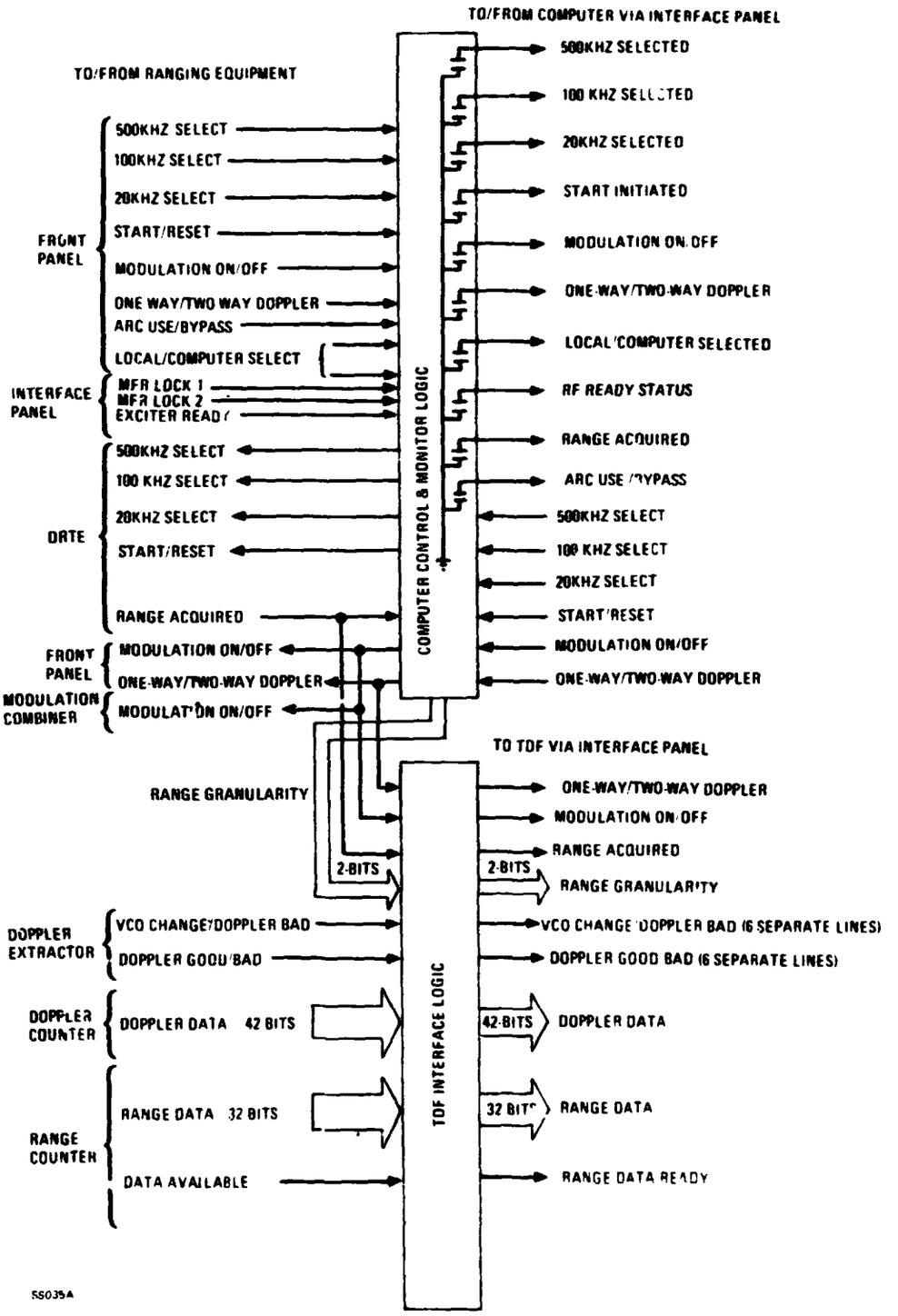

Figure 3.2.18-1. Interface/Control Logic, Block Diagram

The dc power supplies are all mounted within two power supply drawers mounted in the ranging equipment cabinet. A selector switch is provided on the front panel with a meter so that the voltage from each supply can be individually monitored. Adjustment of each voltage is provided by a screwdriver potentiometer accessible on each supply module inside the drawer.

The following supply voltages are provided:

VOLTAGE (volt)	USE
+15.0	Analog circuitry
-15.0	Analog circuitry
-5.2	ECL Digital Logic
+5.0	TTL Digital Logic
+24.0	Analog circuitry
+24.0	Lamp and relay supply

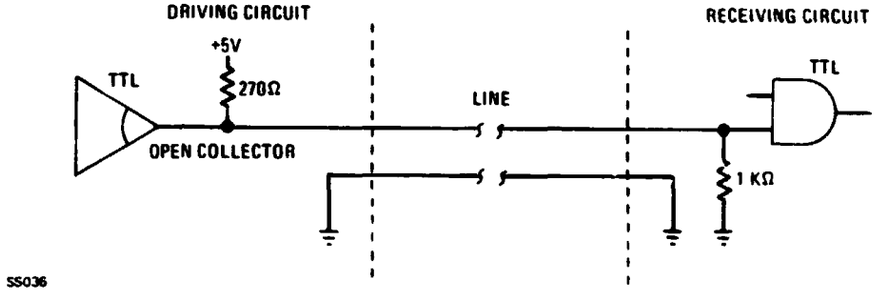

Figure 3.2.18-2. Basic Interface Logic

All of the dc supplies are current limited, short circuit proof and have regulation better than 0.1% from no-load to full-load with a constant ac line voltage. The dc power supply system has been designed to operate so that less than 80% of the rated current of each supply is required under normal operating conditions.

4. SUPPORTING ANALYSES

4.1 DOPPLER SYSTEM FREQUENCY COHERENCE

Figure 4.1-1* is a flow diagram showing the frequency relationships of the doppler system through the output of the Doppler Extractor. (Coherence within the Ranging Equipment was shown in Paragraph 2.2.2.)

The transmitted frequency f_T is shifted to Kf_T on the uplink, multiplied by "ρ" in the transponder to $K\rho f_T$ and retransmitted to the receiver. The downlink signal is shifted to $KK'\rho f_T$ at the receiver. The signal frequency processing within the system is defined by equations at various points in the system.

The output signal of the extractor is a bias-plus-doppler signal represented by:

$$(KK'-1)\,\rho f_T + 70 = f_b + f_d$$

Where:

f_b = 70 MHz, bias frequency

f_d = $(KK'-1)\,\rho f_T$, doppler on returned carrier

ρ = 240/221, transponder turn-around frequency ratio

f_T = Ground transmitter carrier frequency (MHz)

4.2 MAJOR RANGE TONE PROCESSING COHERENCE

The Range Tone Processor uses a "rate-aid" signal to track the received major range tone with a narrowband phase lock loop.

The coherence relationships, for the Rate Aid Synthesizer, between the doppler input signal and the synthesized output signals are shown in Figure 4.2-1. (A 70 MHz system reference signal and a signal used to obtain a dynamic range simulation are also shown.)

The coherence relationships for tracking of the 500 kHz, 100 kHz or 20 kHz tones as the major range tone are shown in Figures 4.2-2 through 4.2-4.

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*For convenience bound in Appendix A.

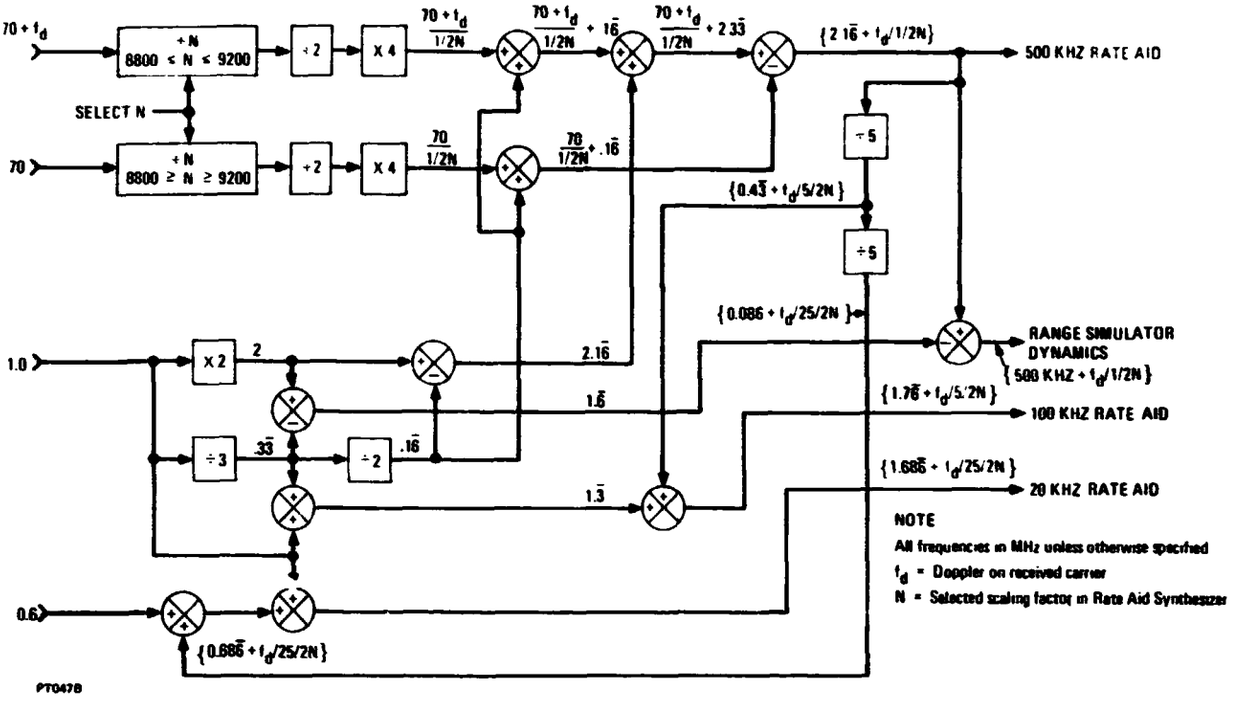


Figure 4.2-1. Rate Aid Synthesizer Coherence

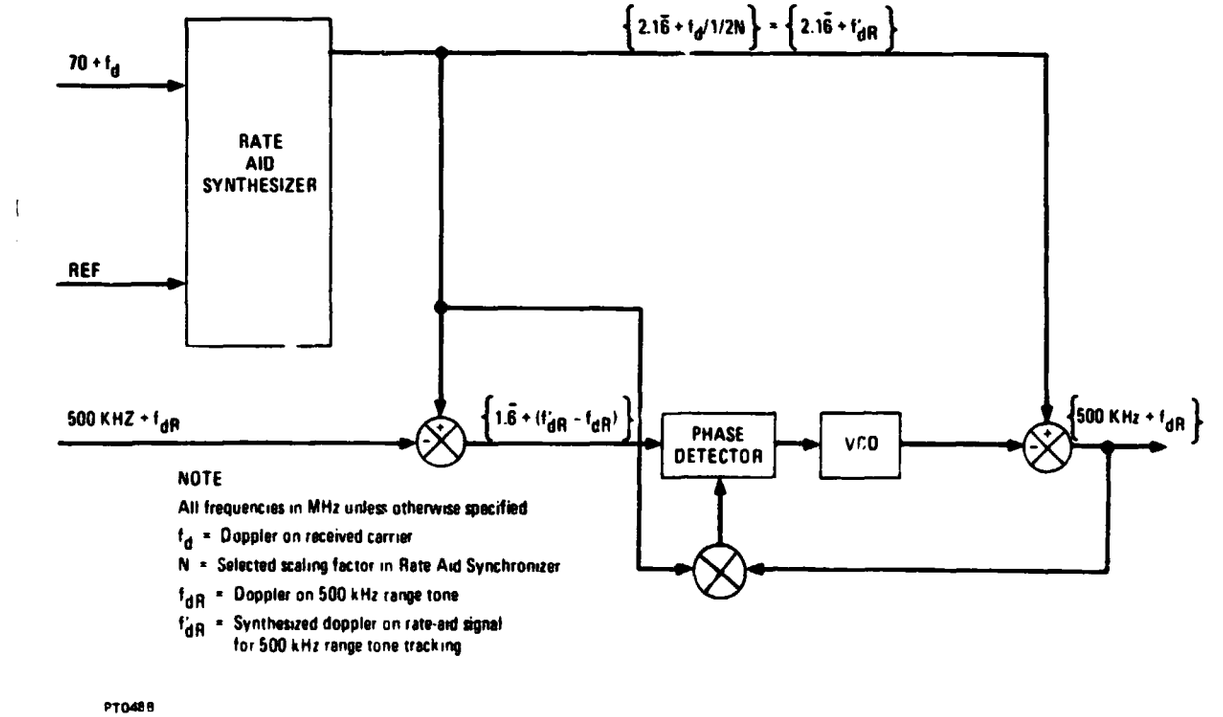


Figure 4.2-2. 500 kHz Range Tone Processing Coherence

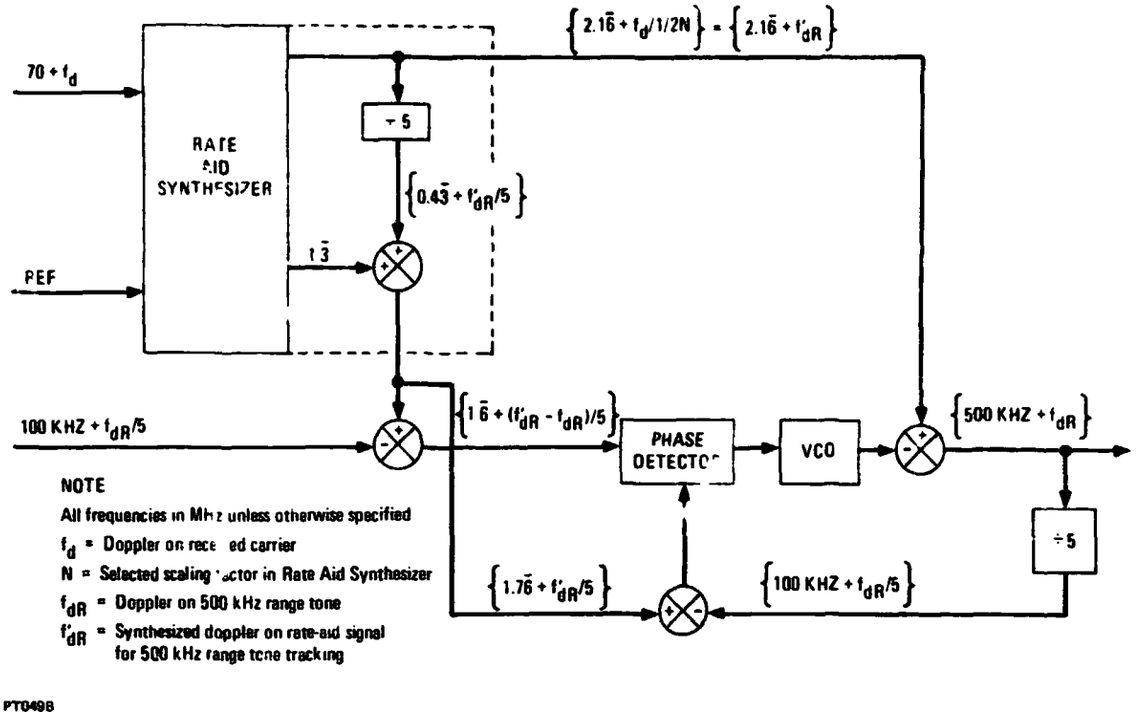


Figure 4.2-3. 100 kHz Major Tone Processing Coherence

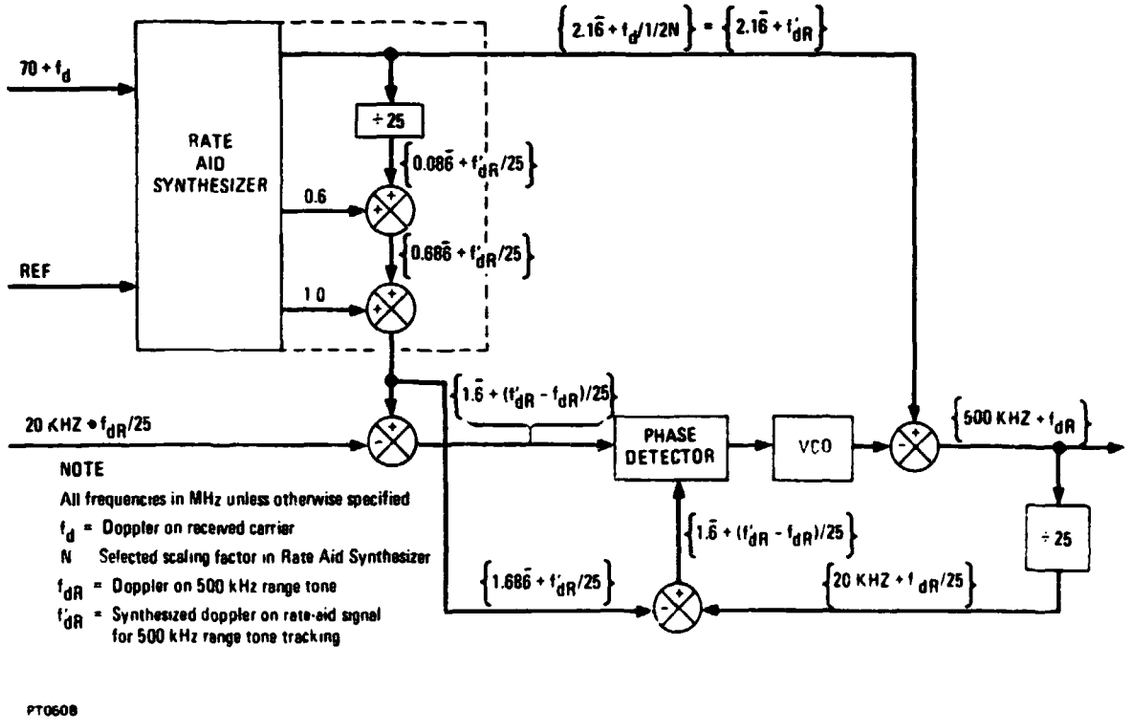


Figure 4.2-4. 20 kHz Major Range Tone Processing Coherence

4.3 MAJOR RANGE TONE PLL

4.3.1 REQUIREMENTS

System performance requirements which dictate design parameters of the major range tone PLL are imposed by signal dynamics, random noise error allocation, and time allowed for track acquisition and settling of acquisition transients to within error budget values.

4.3.1.1 SIGNAL DYNAMICS — Signal dynamics, specified in terms of carrier doppler and doppler rate, correspond to the following range dynamics:

$$\dot{R} \leq 15{,}000 \text{ meters/sec}$$

$$\ddot{R} \leq 150 \text{ meters/sec}^2$$

Range data errors are to be within budget for these steady-state dynamics. In addition, tracking is to be maintained with degraded accuracy for

$$\ddot{R} \leq 352 \text{ meters/sec}^2$$

To minimize lag and transient errors and acquisition times with the required narrow PLL bandwidths, a carrier rate aid signal is employed to cancel range dynamics to within one part in 17600 (57 ppm). The resultant worst-case residual signal dynamics, for the range tone PLL, correspond to:

$$(1.5 \times 10^4 \text{ m/sec}) / 17600 = 0.852 \text{ meter/sec}$$

$$(150 \text{ m/sec}^2) / 17600 = 8.52 \times 10^{-3} \text{ meter/sec}^2$$

$$(352 \text{ m/sec}^2) / 17600 = 2 \times 10^{-2} \text{ meter/sec}^2$$

The resultant maximum residual doppler and doppler rate within the major range tone PLL for the several tones are listed in Table 4.3.1.1-1.

4.3.1.2 RANDOM NOISE ERROR — The random noise error requirement is established by Figure 1 of Specification S-813-P-19 (revised) which is reproduced in Figure 4.3.1.2-1. An analysis of that figure indicates that at low values of S/ϕ, where input additive noise is dominant, the tone loop one-sided noise bandwidth (BN_1) must

Table 4.3.1.1-1. Maximum PLL Doppler and Doppler Rate

RANGE TONE (kHz)	SPECIFIED TRACK VALUE		MAXIMUM VALUE
	DOPPLER (DEG/SEC)	RATE (DEG/SEC^2)	RATE (DEG/SEC^2)
20	4.09×10^{-2}	4.09×10^{-4}	9.60×10^{-4}
100	.205	2.05×10^{-3}	4.80×10^{-3}
500	1.023	1.023×10^{-2}	2.40×10^{-2}

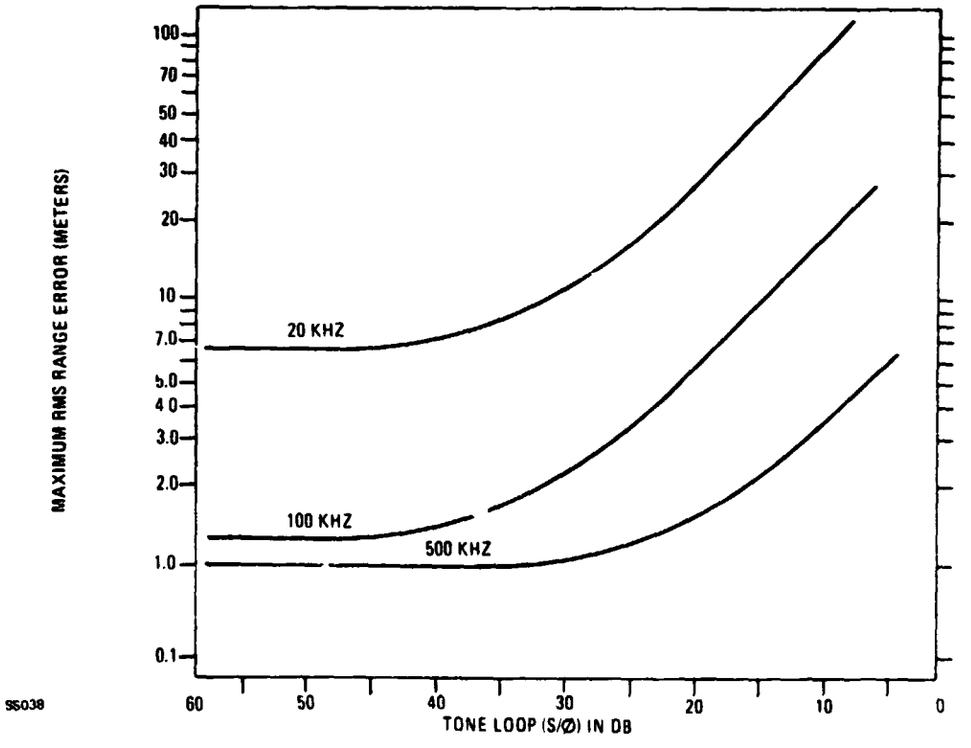


Figure 4.3.1.2-1. Range Accuracy Requirement

be 0.05 Hz or less for either of the three major range tones (MRT). Allowable maximum bandwidths at other points of interest are:

S/ϕ = 30 dB - Hz

BN_1 = 0.2 Hz for 500 kHz MRT

BN_1 = 0.05 Hz for 100 kHz and 20 kHz MRT

S/ϕ = 50 dB - Hz

BN_1 = 6 Hz for 500 kHz

BN_1 = 1 Hz for 100 kHz and 20 kHz MRT

4.3.1.3 ACQUISITION TIME — The major range tone PLL is required to acquire track and operate within its error budget within the following time spans:

1. Near Earth - ($S/\phi \geq$ 50 dB - Hz)

$$t_{acq} \leq 4 \text{ sec}$$

2. Lunar Range - (S/ϕ = 30 dB - Hz)

$$t_{acq} \leq 22 \text{ sec}$$

For the near-earth case, the full specified signal dynamics given in Paragraph 4.3.1.1 may be present during acquisition. For the lunar-range case, maximum dynamics present during acquisition are one-fifth (20%) of the full specified dynamics.

4.3.2 PHASE ACQUISITION PERFORMANCE

4.3.2.1 PROCEDURE — The acquisition of accurate tracking of the major range tone is accomplished in three basic steps:

1. Step and/or slew PLL output signal to near null error condition (open loop)
2. Close loop and operate as a 2nd-order PLL with relatively wide noise bandwidth until phase and velocity transients have settled
3. Reduce loop bandwidth to final value in 3rd-order configuration

Acquisition is completed when transient errors have decayed to within the budgeted values. Note, however, that after step 1 only, phase control has been sufficiently achieved to begin the ambiguity resolution process (minor tone acquisition).

The total time required to complete the acquisition process increases as the major range tone S/ϕ and the acquisition and tracking bandwidths decrease.

4.3.2.2 SLEW PERFORMANCE — The initial step in acquisition of range tone phase lock is an open-loop slew toward the stable null. This slew toward null is accomplished in two steps:

1. Shift phase digitally 180° using VCXO divide by 6.

2a. For 500 kHz + 100 kHz MRT, slew toward null at fixed rate using VCXO frequency offset until measured phase error is zero (actual error may not be zero due to lag and presence of noise).

2b. For 20 kHz, digitally slew using VCXO divide by 6 until measured phase error is zero.

The time required to accomplish each step is constrained by the detector filter noise bandwidth required by the range tone S/ϕ and the resultant filter lag and slew rate limitation.

The phase error input to the PLL, when first [illegible]-order configuration, is determined by the error of stopping slew caused by null r[illegible]nd random noise (and by signal dynamics).

A single-pole, low-pass filter is used to improve null detection S/N for slew control for low range tone S/ϕ values. The detector output is a sinusoidal function of frequency $\dot{\theta}$ slew/360 Hz. The filter causes a lag of the error signal of:

$$\theta_{Lag} = \arctan\left(\dot{\theta}\ \text{slew}/180\ \Delta f_{3dB}\right)$$

where,

$\dot{\theta}$ Slew = PLL slew rate (deg/sec)

Δf_{3db} = Half-power frequency of low-pass filter

The null detector phase lag for various slew rates and detection bandwidths will be

Slew Rate (°/sec)	Detection Bandwidth (Hz)	Lag Error (Degrees)
200	3.50	9°
120	3.50	5.4°
200	1.25	25°
120	1.25	15°

No filter phase lag occurs when maximum noise bandwidth (160 Hz two-sided) is used, since this bandwidth is determined by a bandpass filter ahead of the PLL phase detector. The equivalent phase error due to random noise at the input of the slew control logic circuit (slew detection filter output) is:

$$\sigma_\theta = \arctan \sqrt{N/2S}$$

$$= \arctan \sqrt{BN_1/(S/\varphi)}$$

where,

BN_1 = One-sided noise bandwidth of filter $\simeq 1.6\, f_{3dB}$

σ_θ = RMS error of apparent phase

S/φ = Range tone S/N power density ratio

f_{3dB} = Half-power bandwidth of filter (low-pass)

The random noise error contribution to phase error at end of slew is listed in Table 4.3.2.2-1 for appropriate combinations of S/φ and f_{3dB}.

Table 4.3.2.2-1. Random Noise Error Contribution to Phase Error

f_{3dB} (Hz)	S/φ (dB-Hz)	σ_θ (Deg)	BN_1
50*	50	1.62	80
5	30	5.11	8
1	30	2.29	1.6
1	12	20	0.16

*Obtained from 100 Hz BPF ahead of PLL phase detector

4.3.2.3 TRANSIENT RESPONSE — Figures 4.3.2.3-1 through 4.3.2.3-6 are generalized cases and show normalized PLL transient responses to small, step inputs of position, velocity, or acceleration (step is small when d (sin θ_ϵ) / d $\theta_\epsilon \simeq 1$).

Figures 4.3.2.3-1 through 4.3.2.3-3 apply to a 2nd-order loop with a nominally perfect velocity integrator and a damping factor $\zeta = 0.707$. The open loop transfer function for such a loop is:

$$G(S) = \frac{2\zeta\omega_0 (S + \omega_0 / 2\zeta)}{S^2}$$

$$= \frac{\sqrt{2}\,\omega_0 (S + \omega_0 / \sqrt{2})}{S^2}$$

$$= \frac{2.663\ BN_1 (S + 1.331\ BN_1)}{S^2}$$

where,

BN_1 = One-sided noise bandwidth of loop

ω_0 = BN_1 / 0.531 for $\zeta = 0.707$ and 20% position step error overshoot

Figures 4.3.2.3-4 through 4.3.2.3-6 apply to a 3rd-order loop with nominally perfect integrators and an open-loop transfer function of:

$$G(S) = \frac{9\omega_0}{4} \frac{\left(S + \omega_0/3\right)^2}{S^3}$$

$$= \frac{3.0283\ BN_1 \left(S + 0.4486\ BN_1\right)^2}{S^3}$$

where,

ω_0 = BN_1 / 0.743 for 20% position step error overshoot

The scales of all figures are as follows:

1. Time is presented as the product BN_1 x Time, thus actual time is t = (scale time)/BN_1.

2. Error is presented as the ratio of [Error/(Input Step)] / $(BN_1)^i$,

   where,

   i = 0 for position step

   i = 1 for velocity step

   i = 2 for acceleration step

The predicted closed-loop transient response of the MRT PLL for a number of conditions is illustrated in Figures 4.3.2.3-7 through 4 3.2.3-15. These responses were obtained through computer simulation of the PLL with input conditions corresponding to nominal worst case situations. Descriptive data pertinent to the various figures is summarized in Table 4.3.2.3-1. In all cases:

1. The response starts at the time the PLL is initially closed in a 2nd-order configuration. This is after any required slewing is completed.

2. The initial phase error simulated at the time of loop closure is greater than or equal to the one sigma uncertainty in phase due to noise present in the observation bandwidth used during slew.

3. The loop is allowed to settle in the second-order configuration for approximately 5 time constants (BN_1 t = 5).

4. After settling in the initial 2nd-order configuration, the loop bandwidth is reduced and the configuration changed to 3rd-order.

5. The assumed phase error at the time of bandwidth reduction and configuration change is the rms error due to noise in the initial bandwidth. (This is the reason for the apparent step error in the figures).

6. The signal frequency dynamics present during the acquisition process correspond to the full specified dynamics for the strong signal cases (S/o = 50 dB-Hz) and one-fifth of that for the medium (S/o = 30 dB-Hz) and weak (S/o = 12 db-Hz) signal cases.

7. For the cases where signal dynamics have a significant effect, the phase error due to noise at the time of bandwidth switching is introduced in both polarities.

Figure 4.3.1.2-1 establishes the range accuracy requirements for the system. From this figure, the total allowable rms phase error under various conditions can be

determined. The total allowable values are listed in Table 4.3.2.3-2. A portion of this total allowable error can then be allocated to transient lock-up error to account for the residual phase error due to transients at the time acquisition is considered completed. Figures 4.3.2.3-7 through 4.3.2.3-15 can then be used to determine the time (after initially closing the loop) required to get the residual transient phase error within the allocated amount. The allocated transient phase errors and the required times are also given in Table 4.3.2.3-2. In some cases, the allocated transient error is approximately two-thirds of the total allowable phase error. Although this may seem large, it should be noted that the responses represented by Figures 4.3.2.3-7 through 4.3.2.3-15 are for severe cases (maximum required dynamics, minimum S/ø within range, and maximum rate-aid error) and in general, the errors will be considerably less. Furthermore, the error can be in either direction and statistically should combine with other errors in a root-sum-square manner.

Table 4.3.2.3-1. Transient Response Descriptive Data

	Figure 4.3.2.3-								
	-7	-8	-9	-10	-11	-12	-13	-14	-15
MRT Frequency (kHz)	500	100	20	500	100	20	500	100	20
S/ϕ (dB-Hz)	50	50	50	30	30	30	12	12	12
$\dot{\theta}$ (deg/sec)	1.0	0.20	0.04	0.2	0.04	0.008	0.2	0.04	0.008
$\ddot{\theta}$ (deg/sec^2)	0.01	0.002	0.0004	0.002	0.0004	0.00008	0.002	0.0004	0.00008
Initial phase error (deg)	4	4	4	4	4	4	25	25	25
Second-order bandwidth (Hz) (one-sided)	4.8	4.8	4.8	0.6	0.6	0.6	0.15	0.15	0.15
Second-order S/N (dB)	40	40	40	29	29	29	17	17	17
Second-order rms phase error due to noise (deg)	0.4	0.4	0.4	1.4	1.4	1.4	5.6	5.6	5.6
Third-order bandwidth (Hz) (one sided)	0.6	0.6	0.6	0.0375	0.0375	0.0375	0.0375	0.0375	0.0375
Third-order S/N (dB)	49	49	49	41	41	41	23	23	23
Third-order rms phase error due to noise (deg)	0.14	0.14	0.14	0.35	0.35	0.35	2.8	2.8	2.8

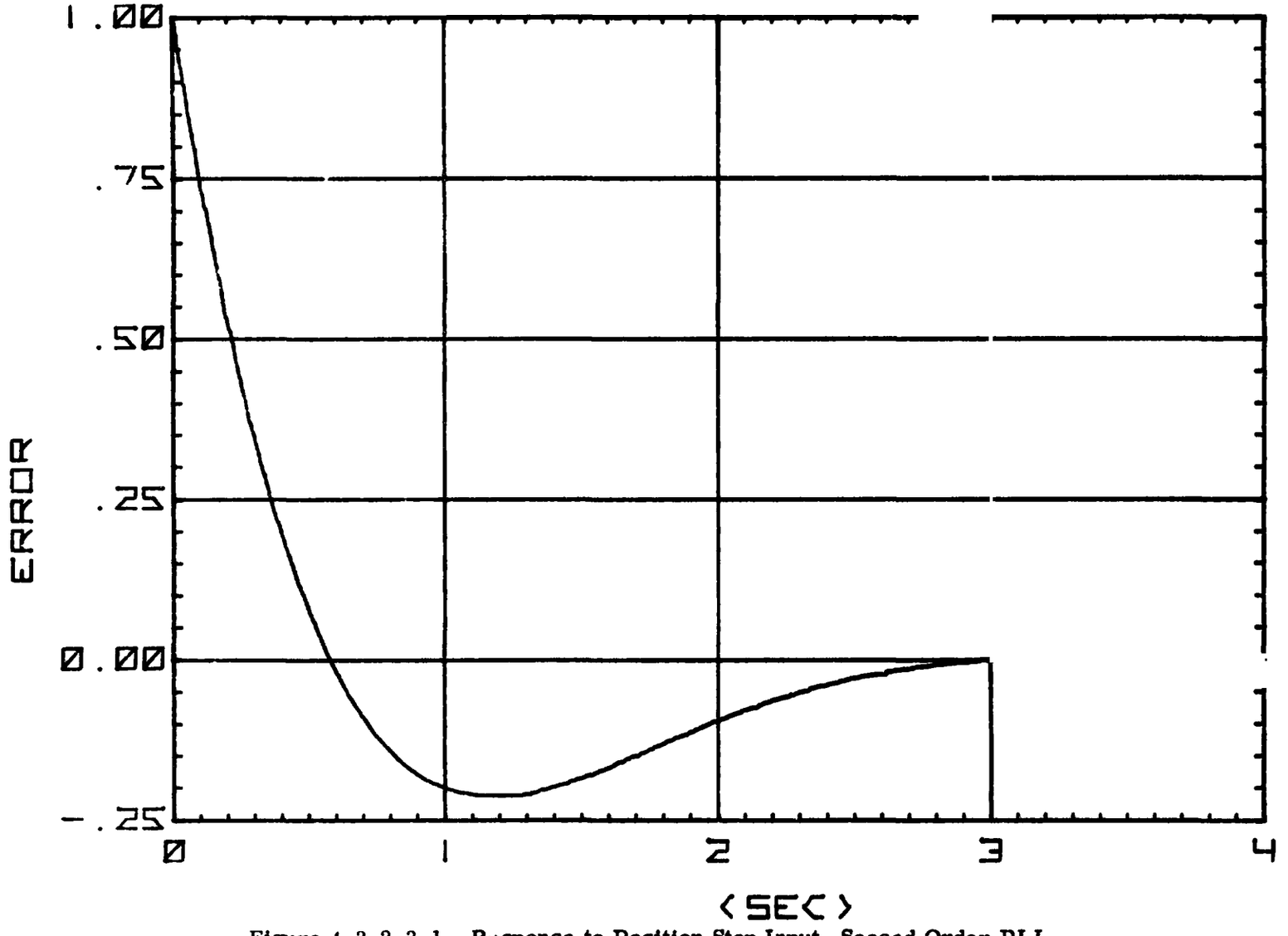


Figure 4.3.2.3-1. Response to Position Step Input, Second Order PLL

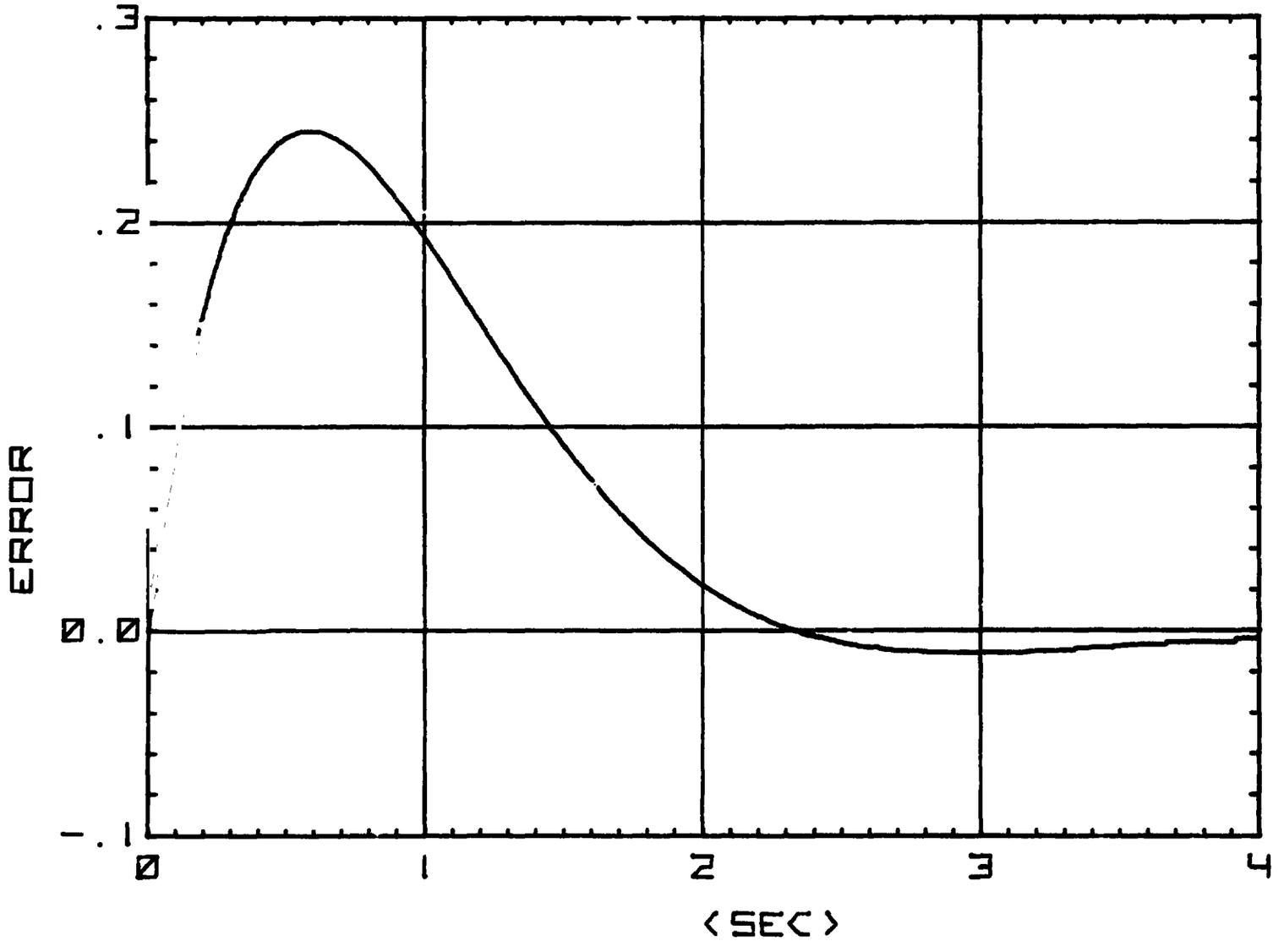


Figure 4.3.2.3-2. Response to Velocity Step Input, Second Order PLL

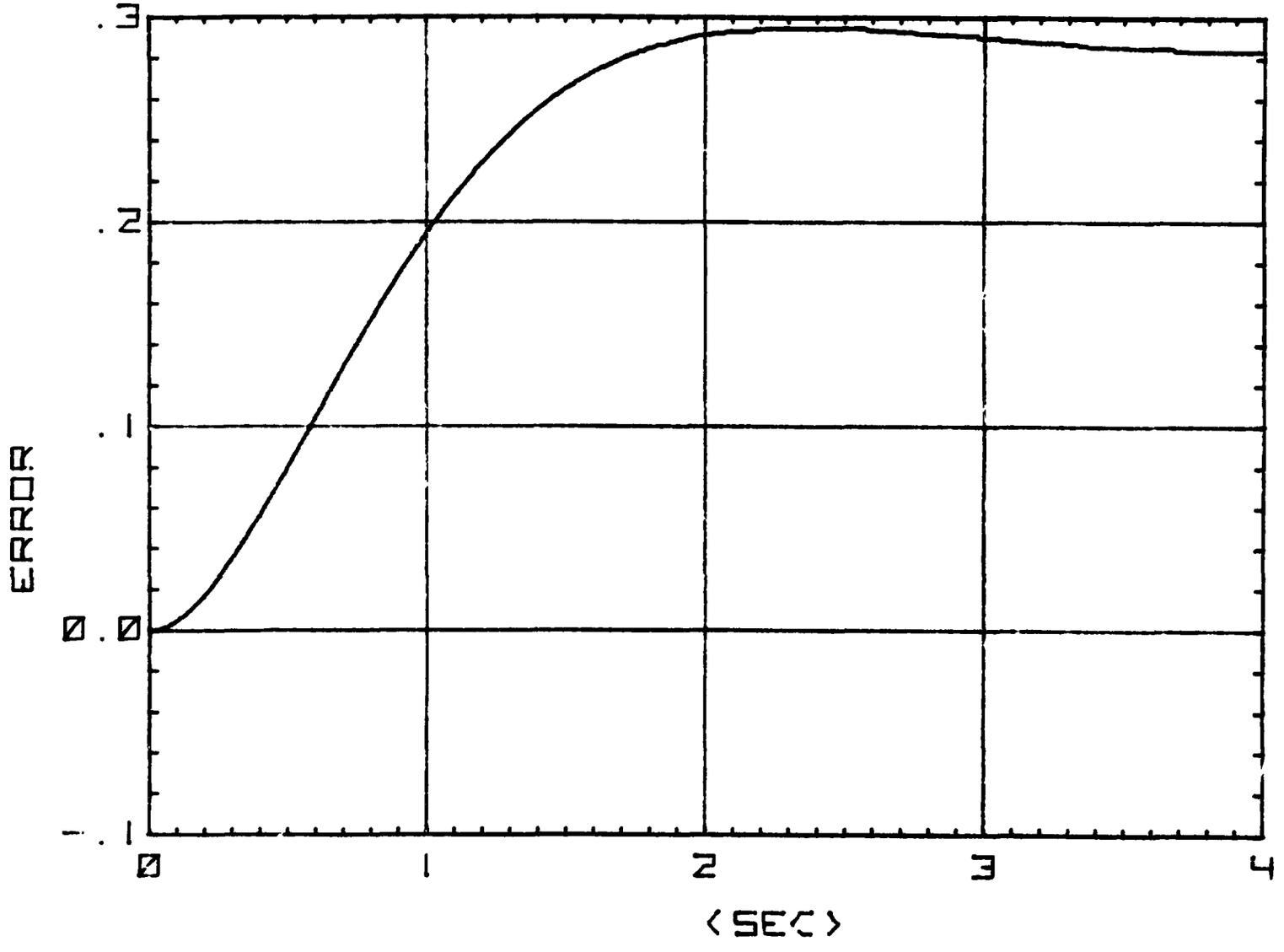


Figure 4.3.2.3-3. Response to Acceleration Step Input, Second Order PLL

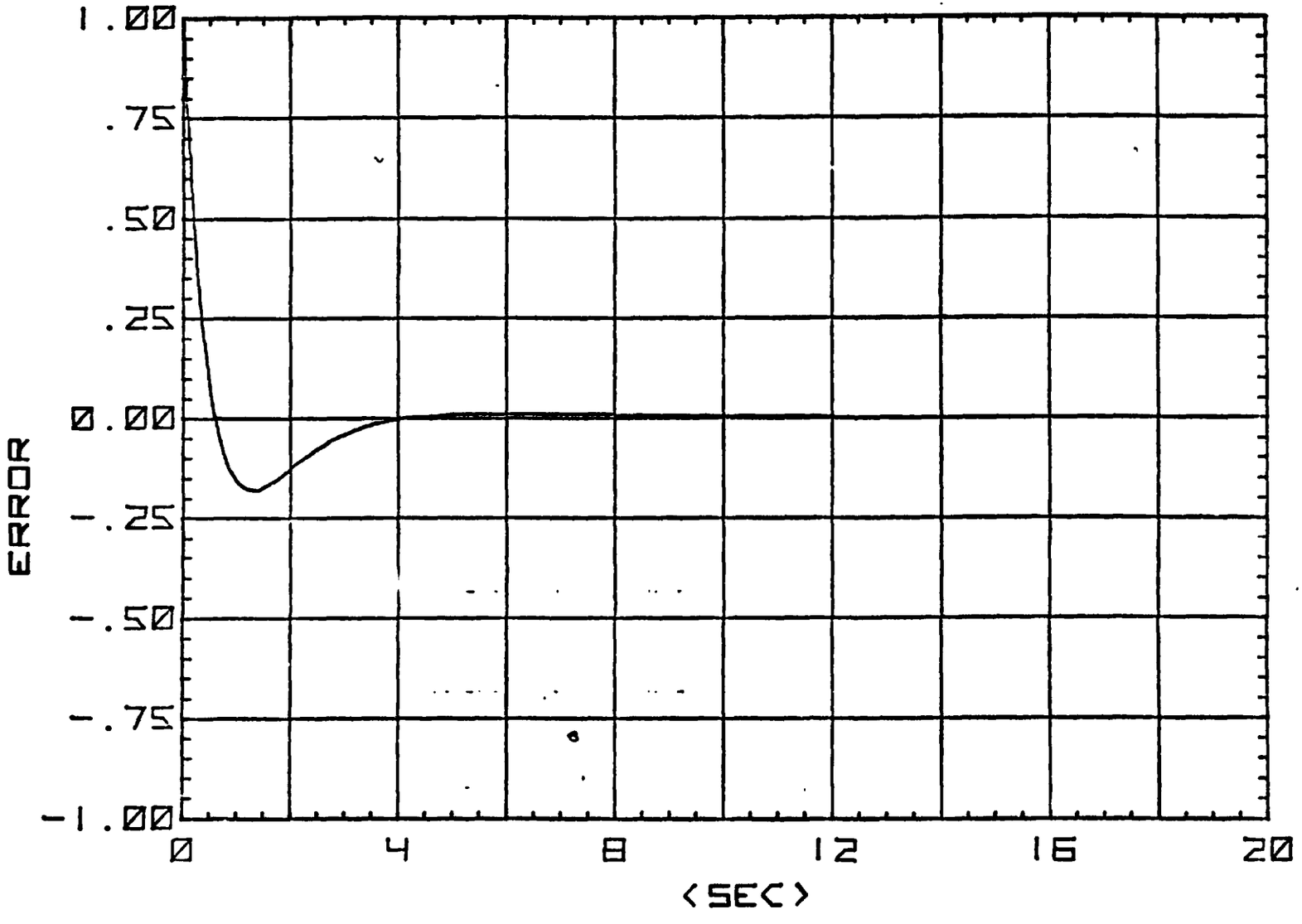


Figure 4.3.2.3-4. Response to Position Step Input, Third Order PLL

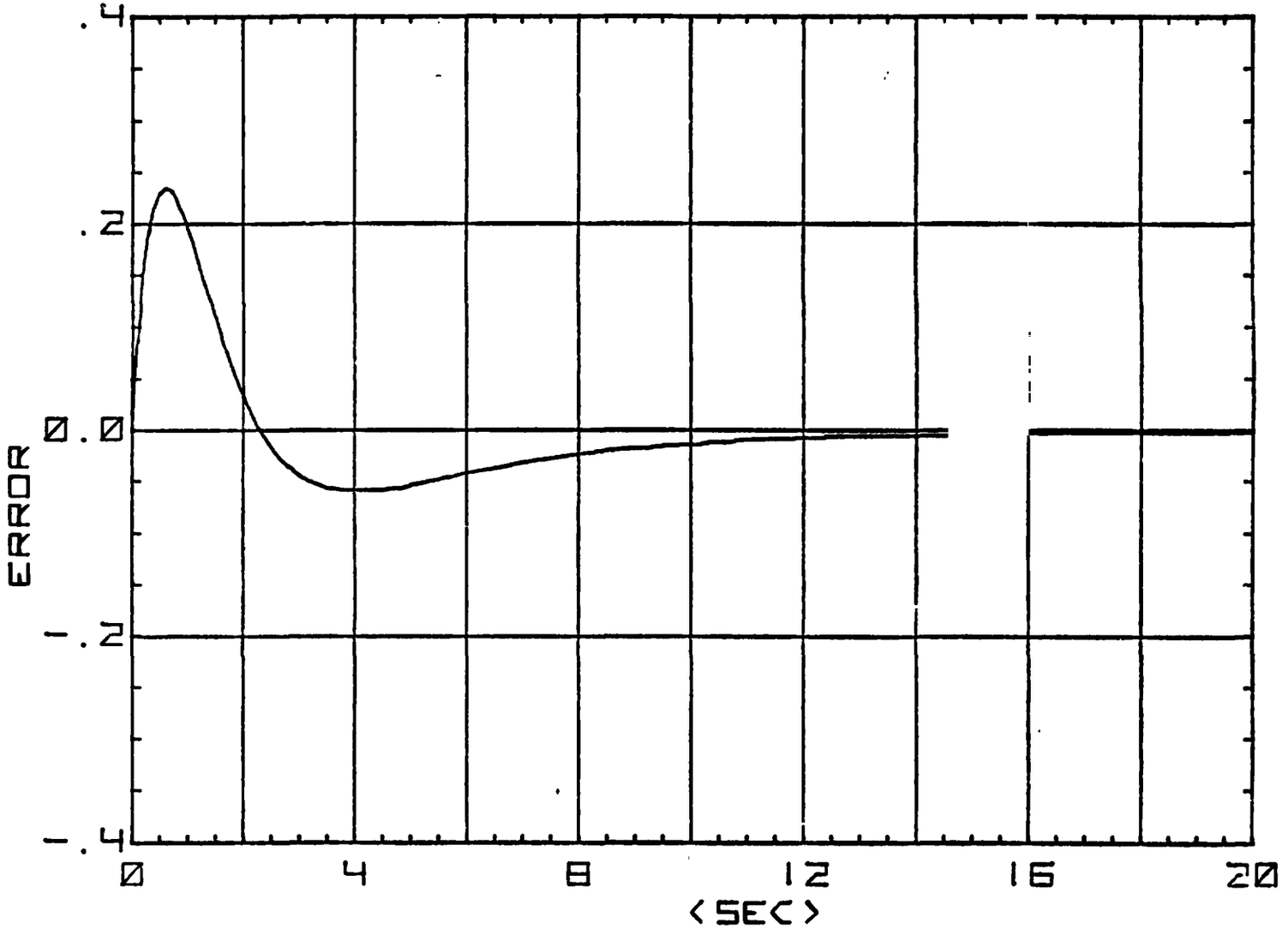


Figure 4.3.2.3-5. Response to Velocity Step Input, Third Order PLL

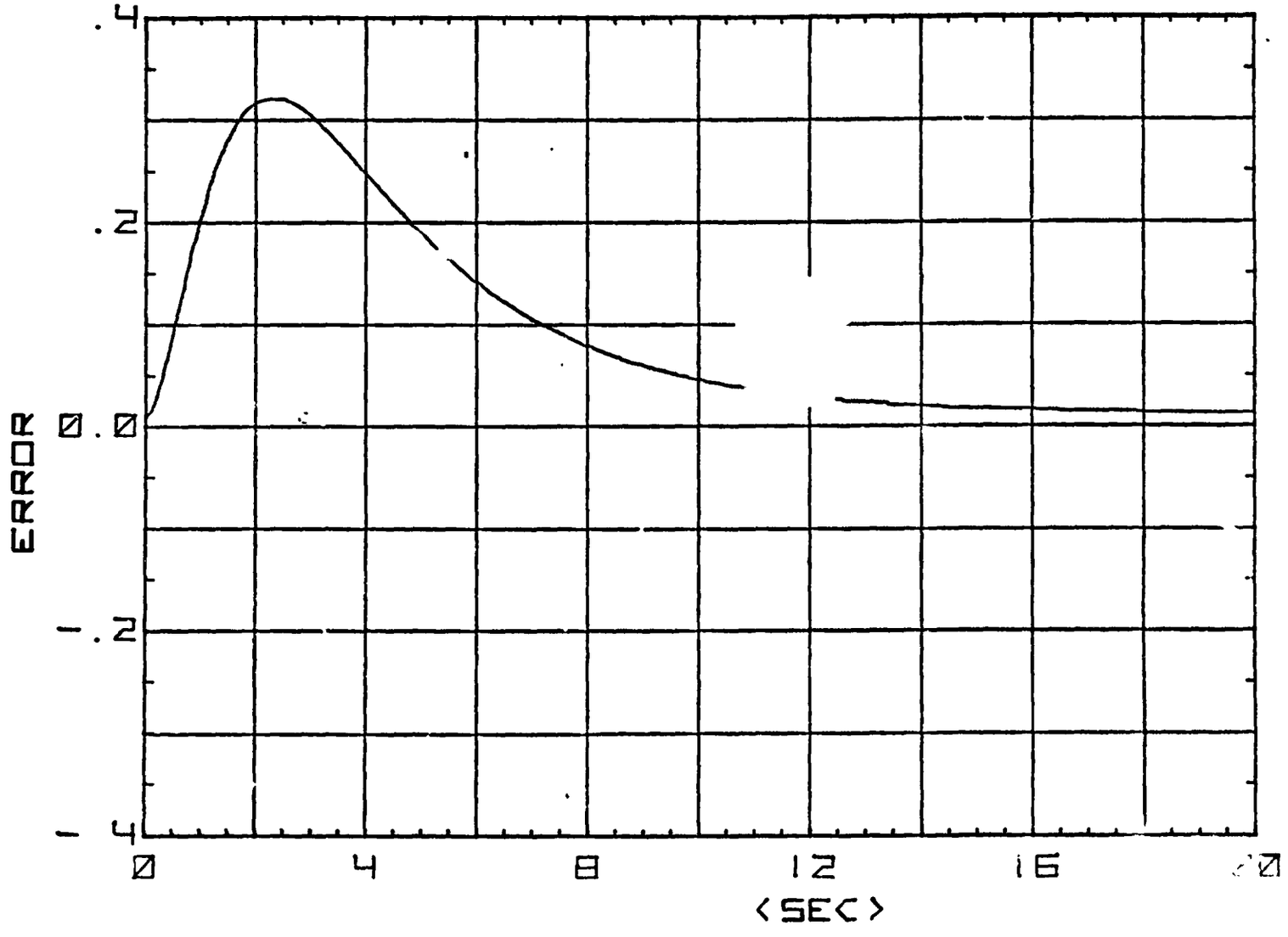


Figure 4.3.2.3-6. Response to Acceleration Step Input, Third Order PLL

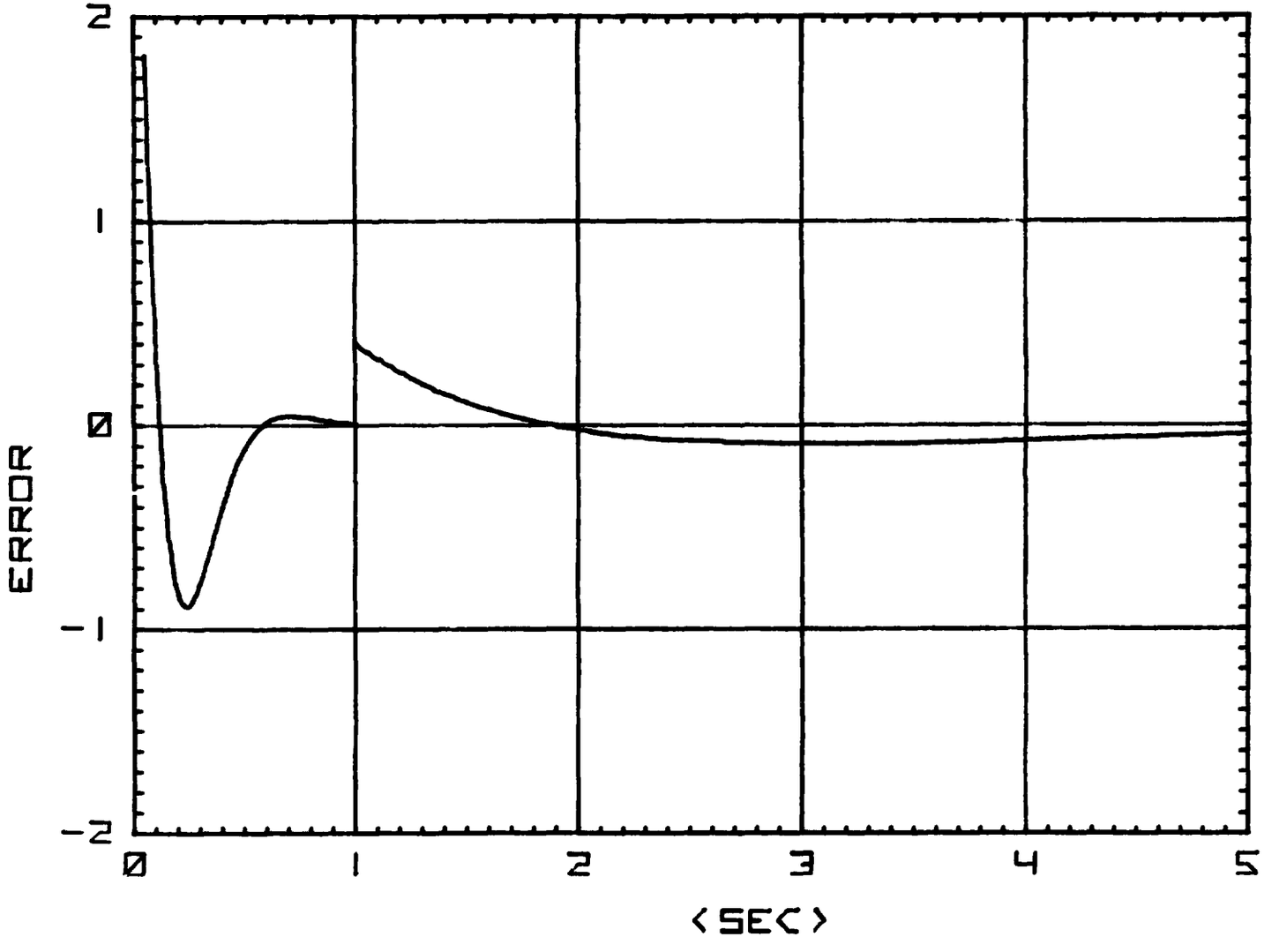


Figure 4.3.2.3-7. Response For Strong Signal, 500 kHz MRT

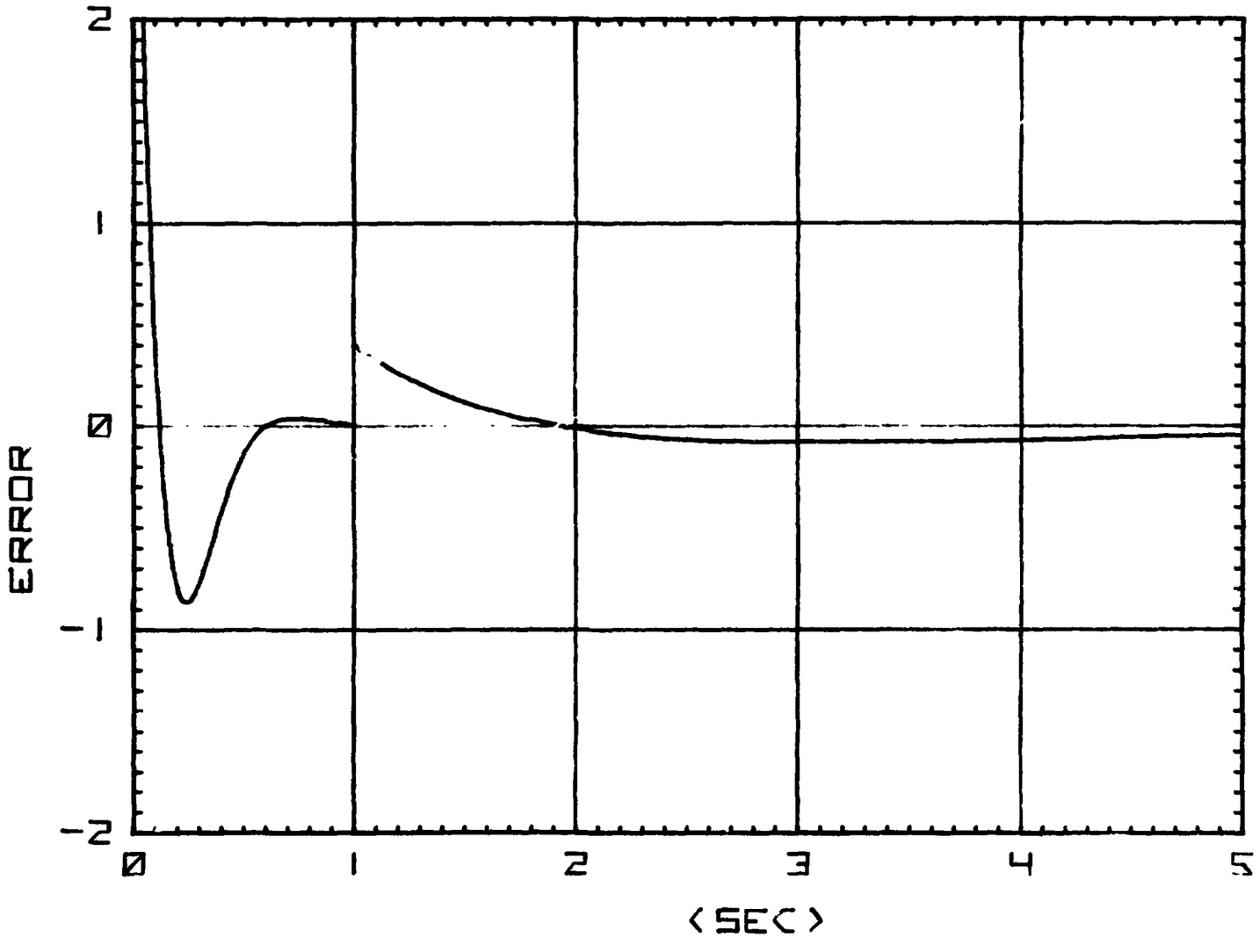


Figure 4.3.2.3-8. Response For Strong Signal, 100 kHz MRT

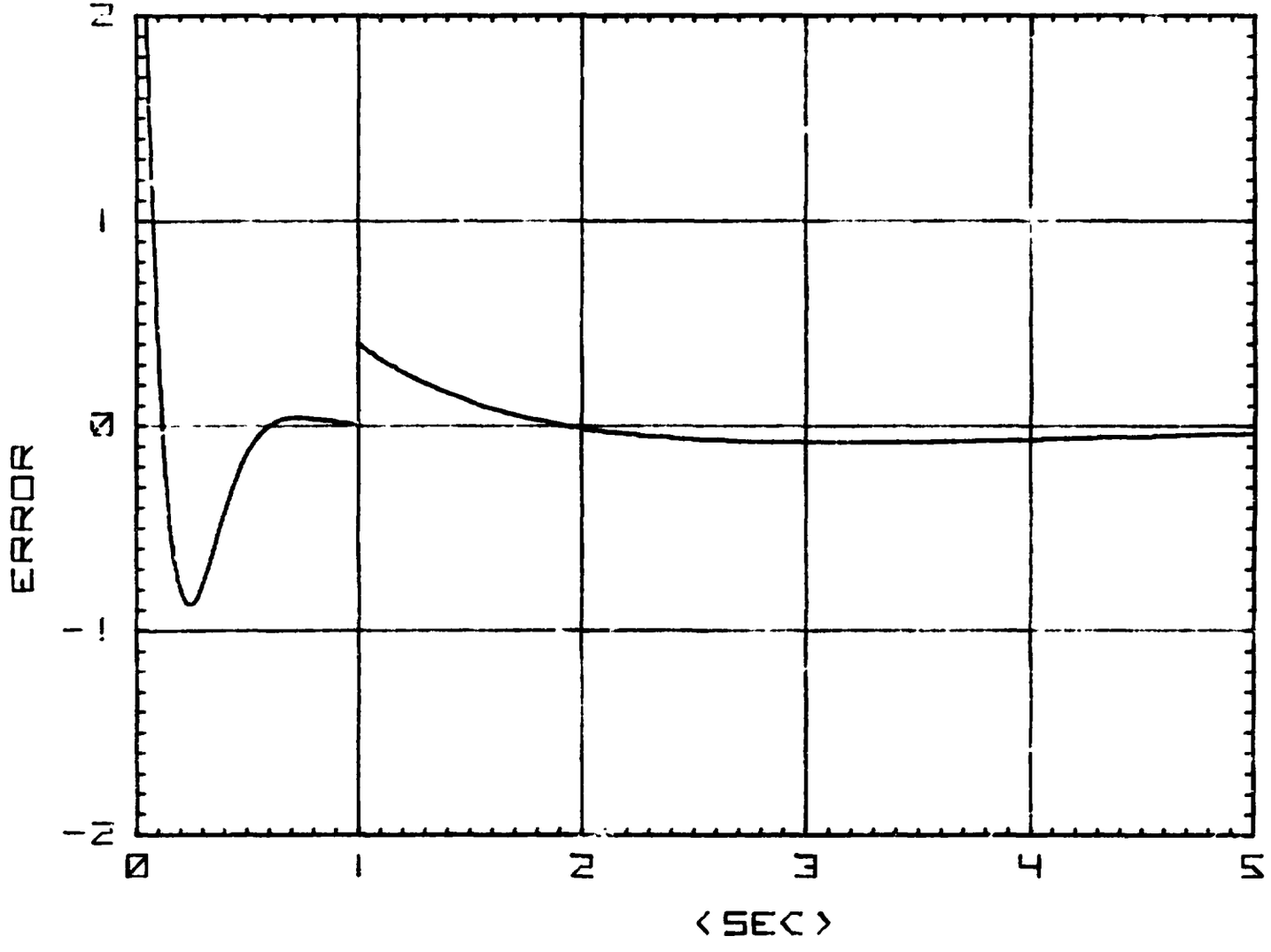


Figure 4.3.2.3-9. Response For Strong Signal, 20 kHz MRT

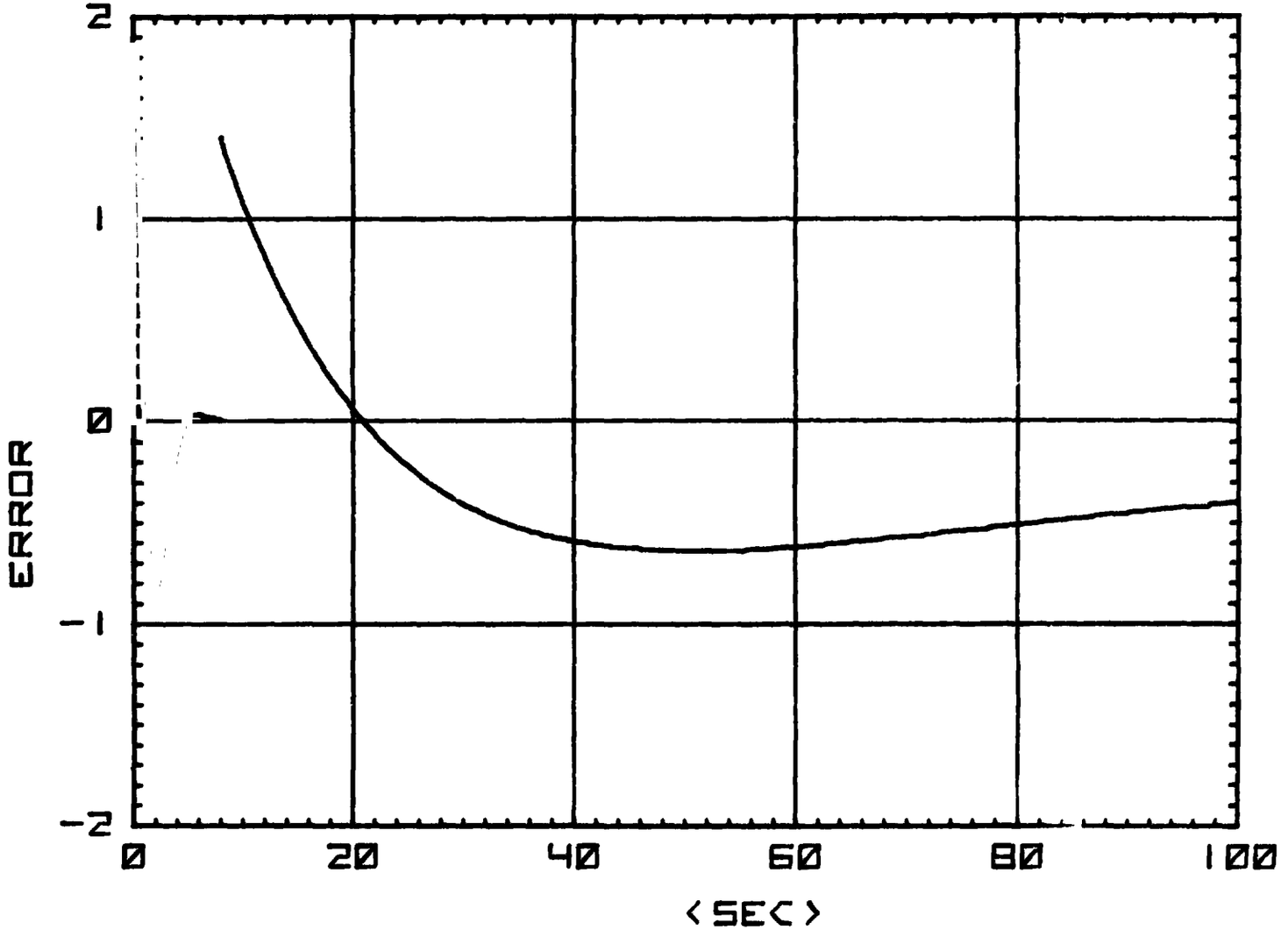


Figure 4.3.2.3-10(a). Response For Medium Signal, 500 kHz MRT, (positive)

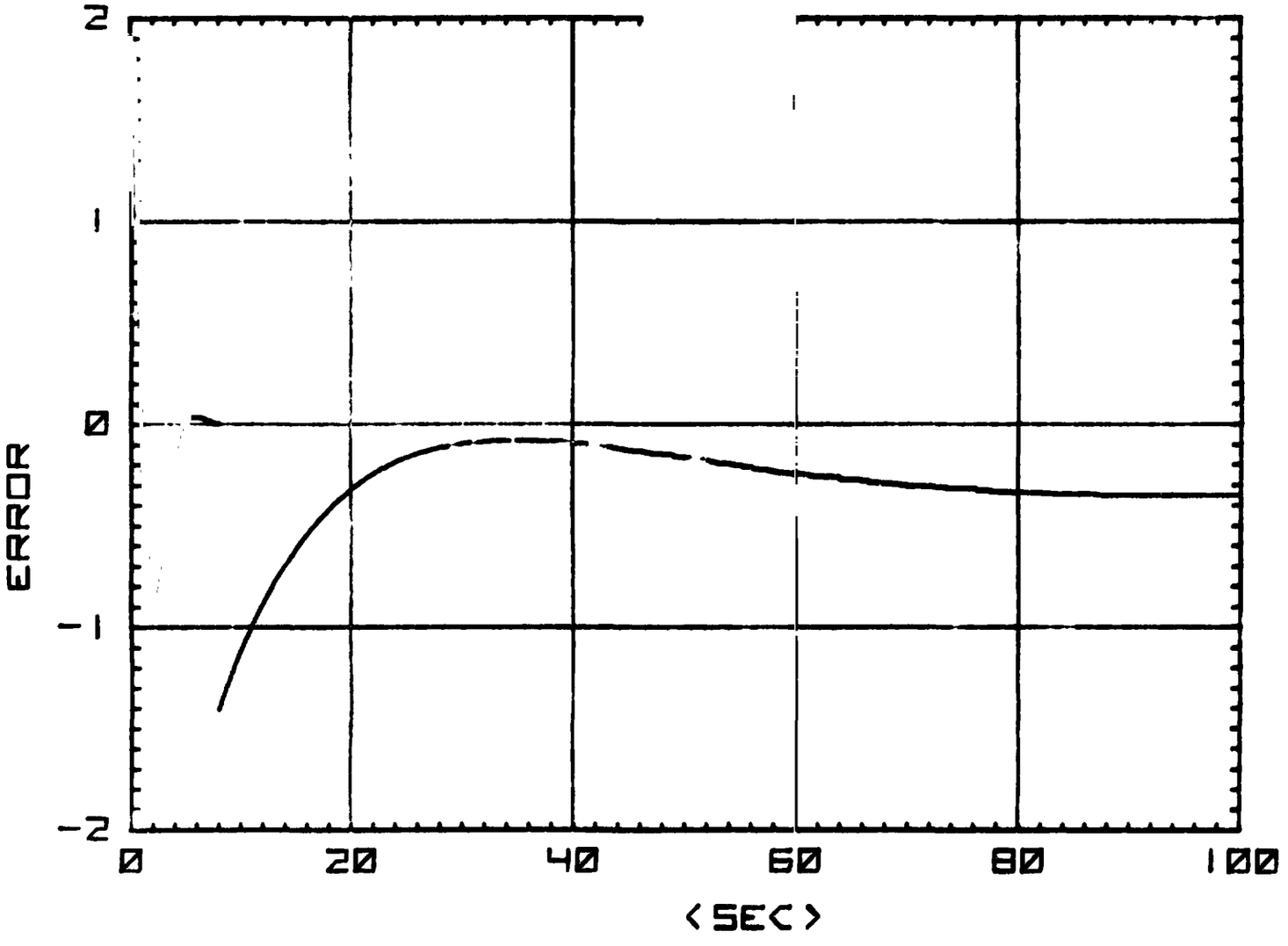


Figure 4.3.2.3-10(b). Response For Medium Signal, 500 kHz MRT, (negative)

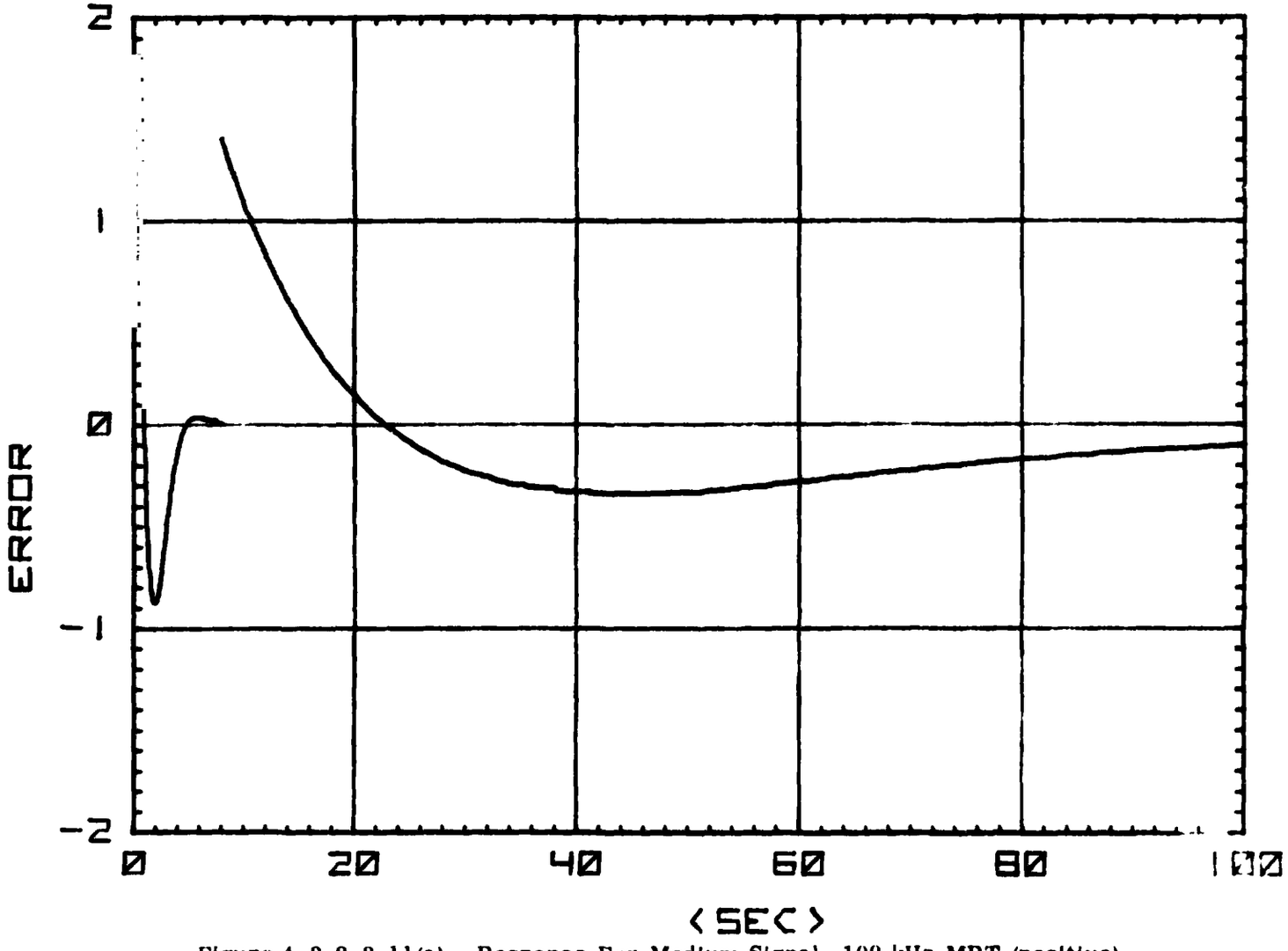


Figure 4.3.2.3-11(a). Response For Medium Signal, 100 kHz MRT (positive)

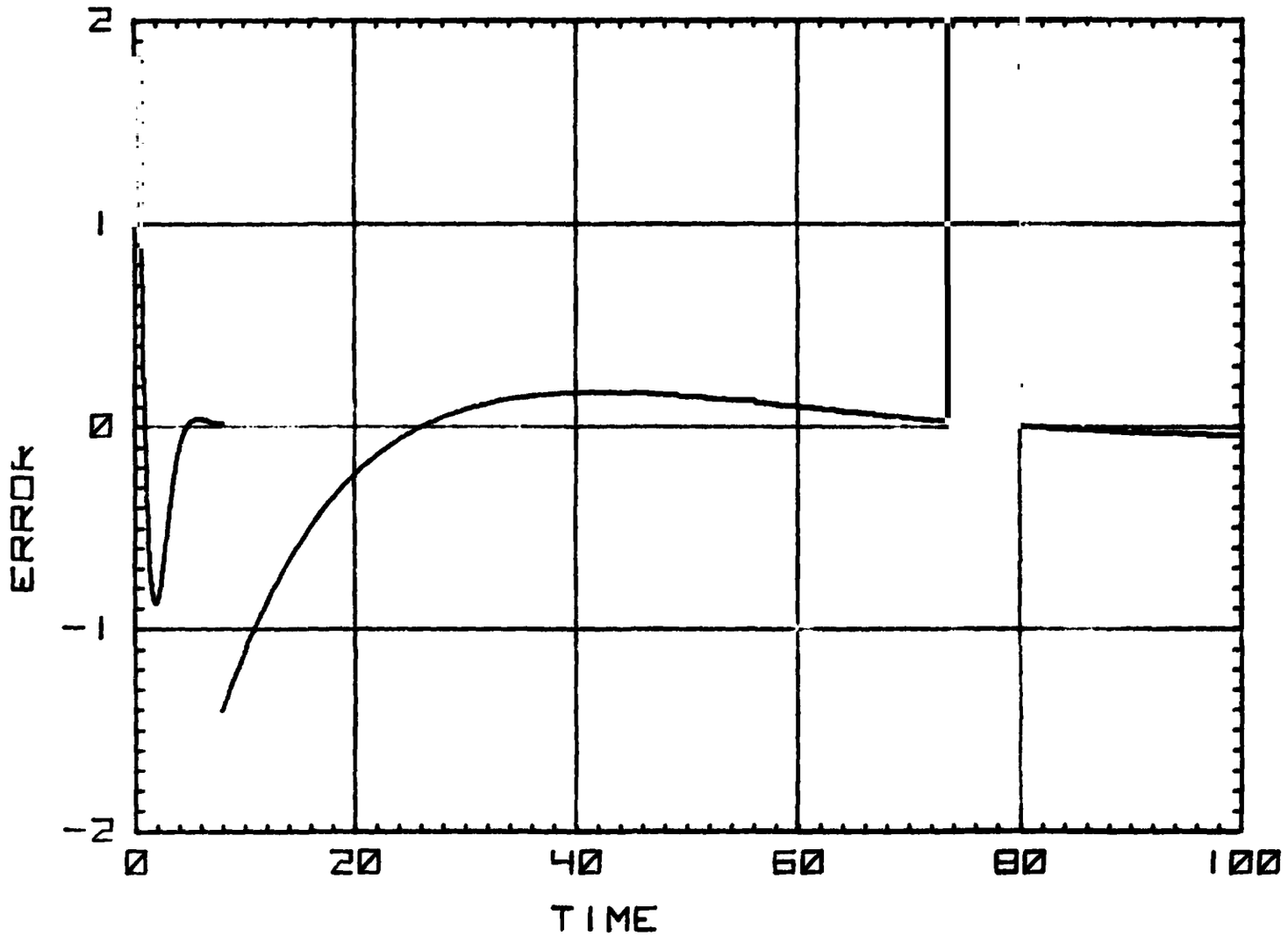


Figure 4.3.2.3-11(b). Response For Medium Signal, 100 kHz MRT (negative)

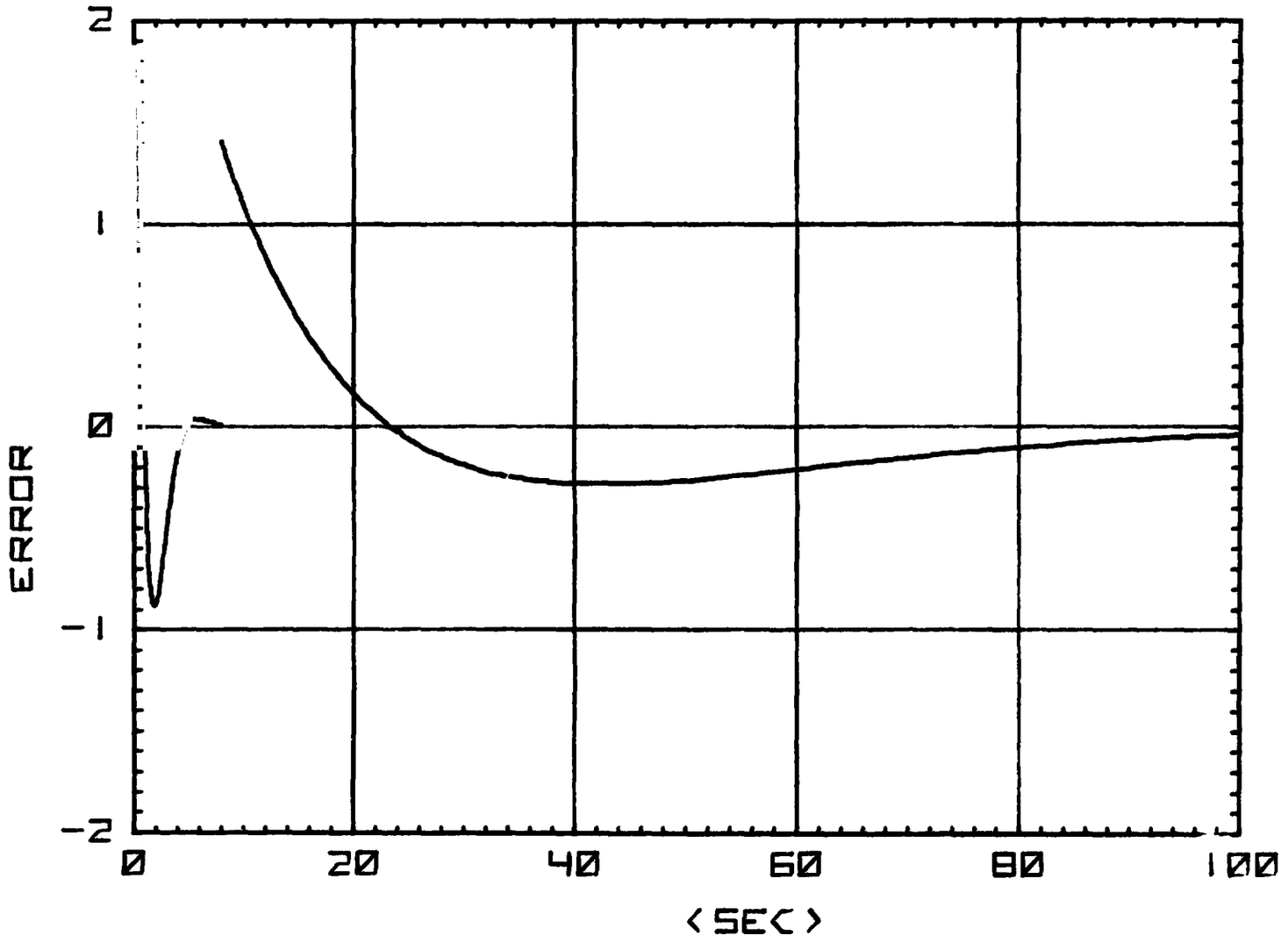


Figure 4.3.2.3-12(a). Response For Medium Signal, 20 kHz MRT, (positive)

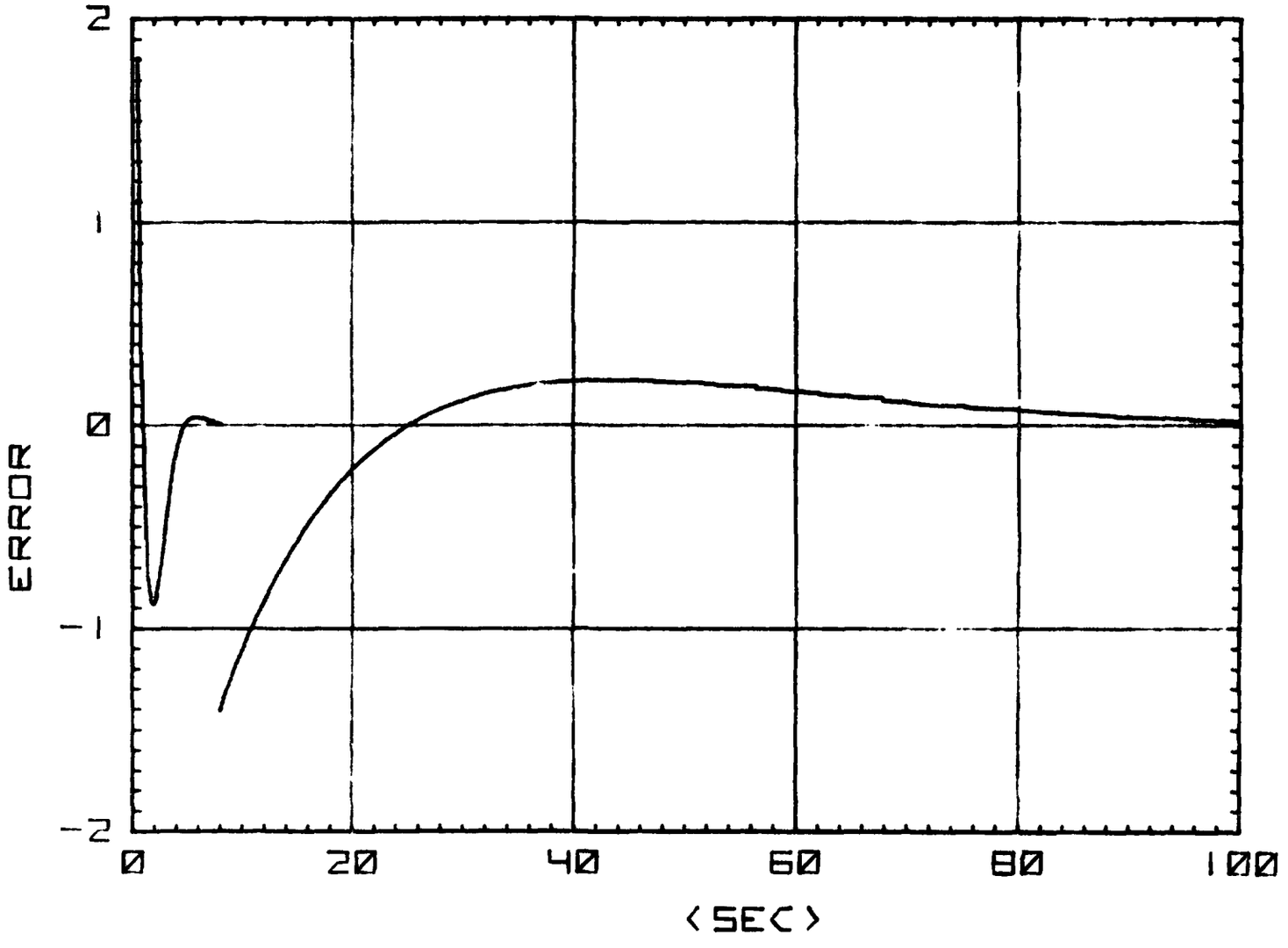


Figure 4.3.2.3-12(b). Response For Medium Signal, 20 kHz MRT, (negative)

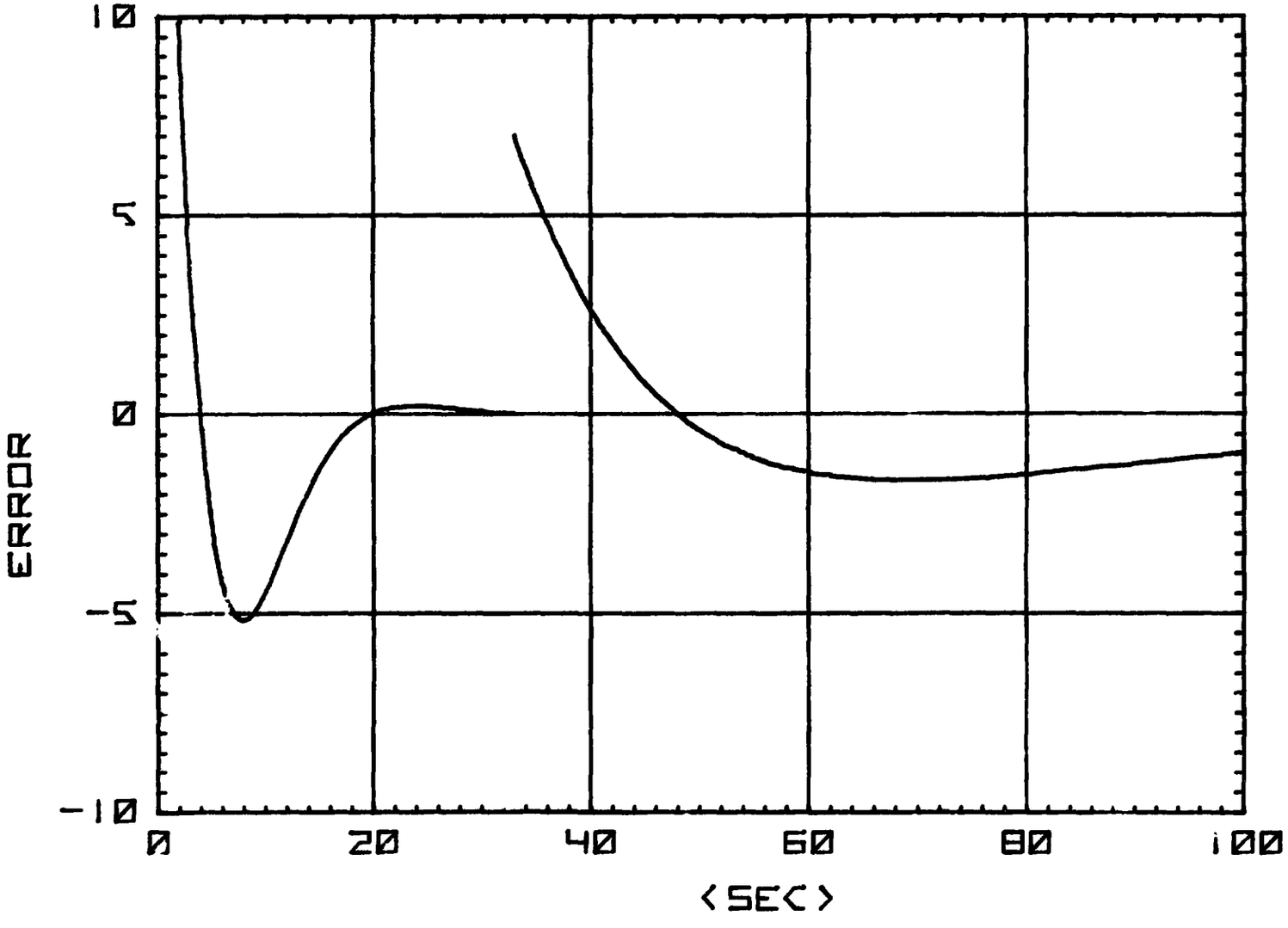


Figure 4.3.2.3-13(a) Response For Weak Signal, 500 kHz MRT, (positive)

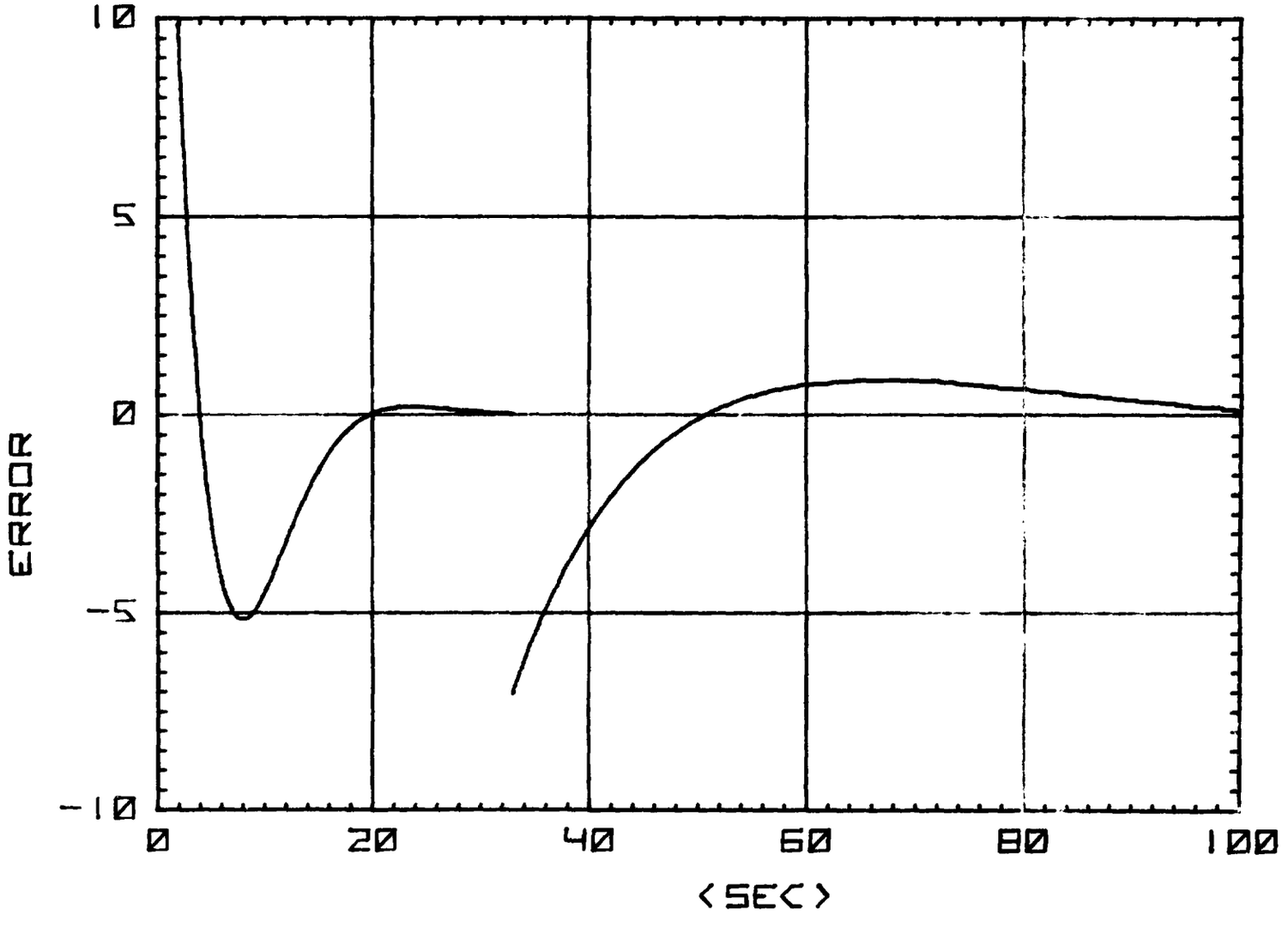


Figure 4.3.2.3-13(b). Response For Weak Signal, 500 kHz MRT, (negative)

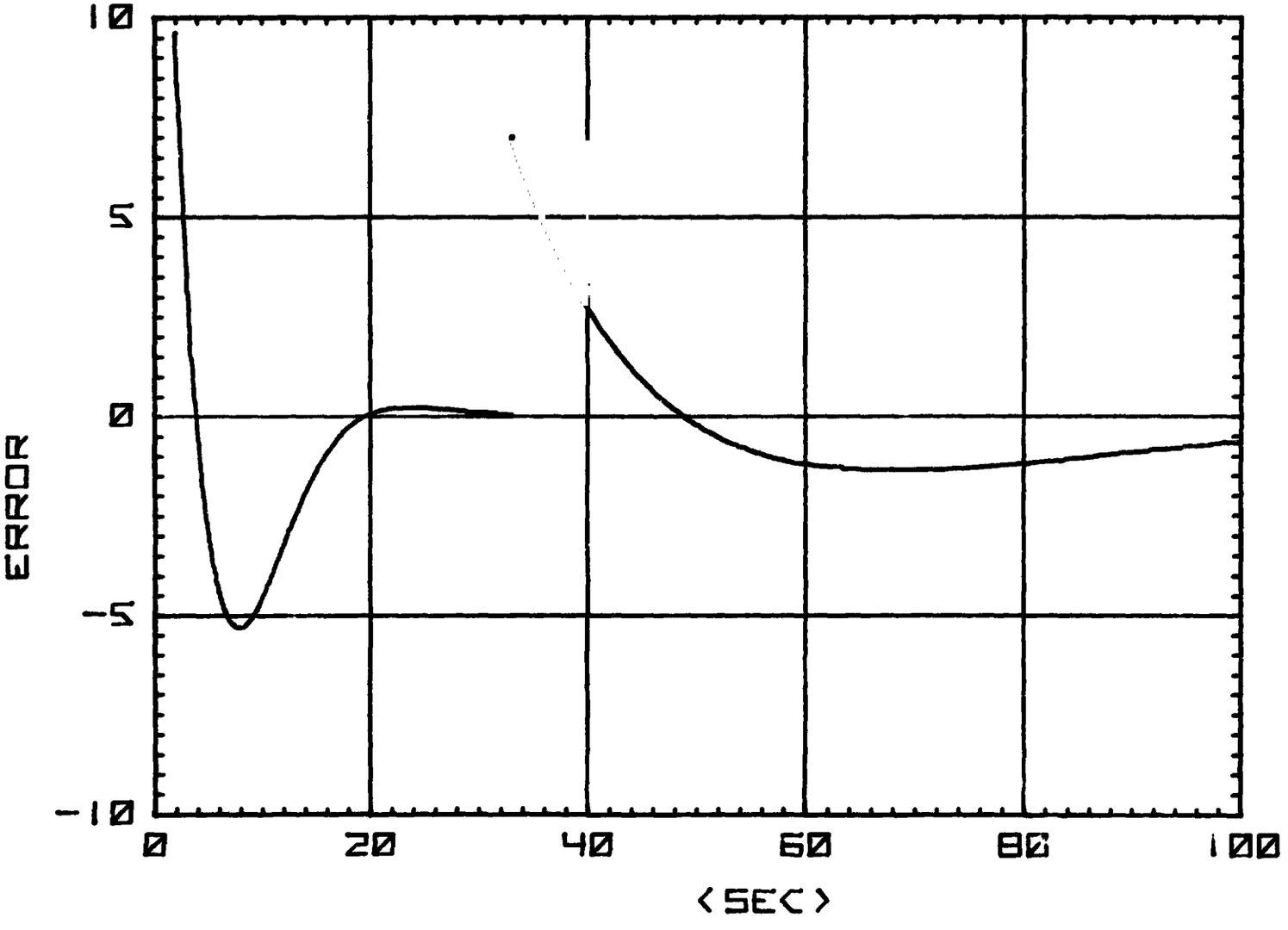


Figure 4.3.2.3-14(a). Response For Weak Signal, 100 kHz MRT, (positive)

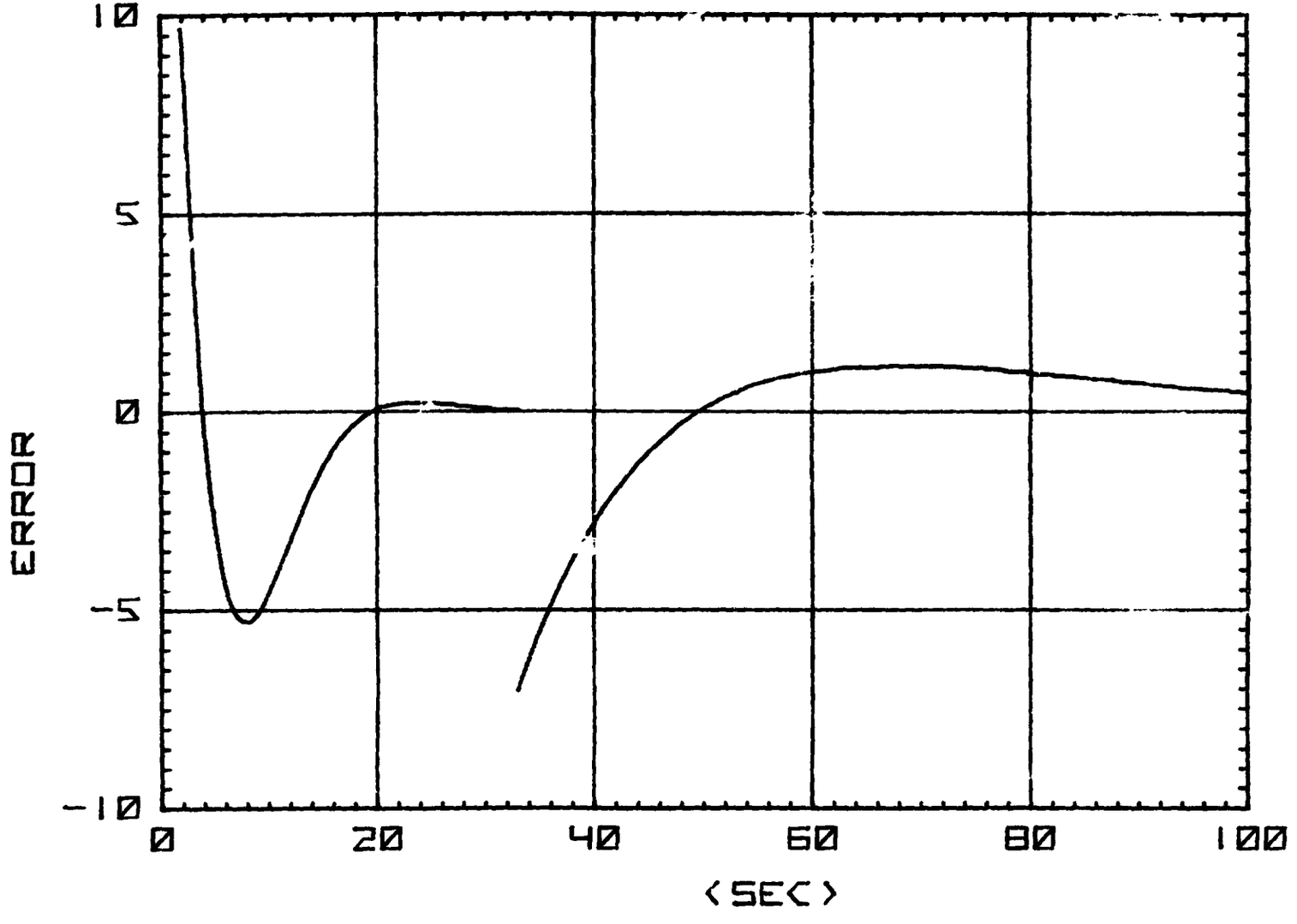


Figure 4.3.2.3-14(b). Response For Weak Signal, 100 kHz MRT, (negative)

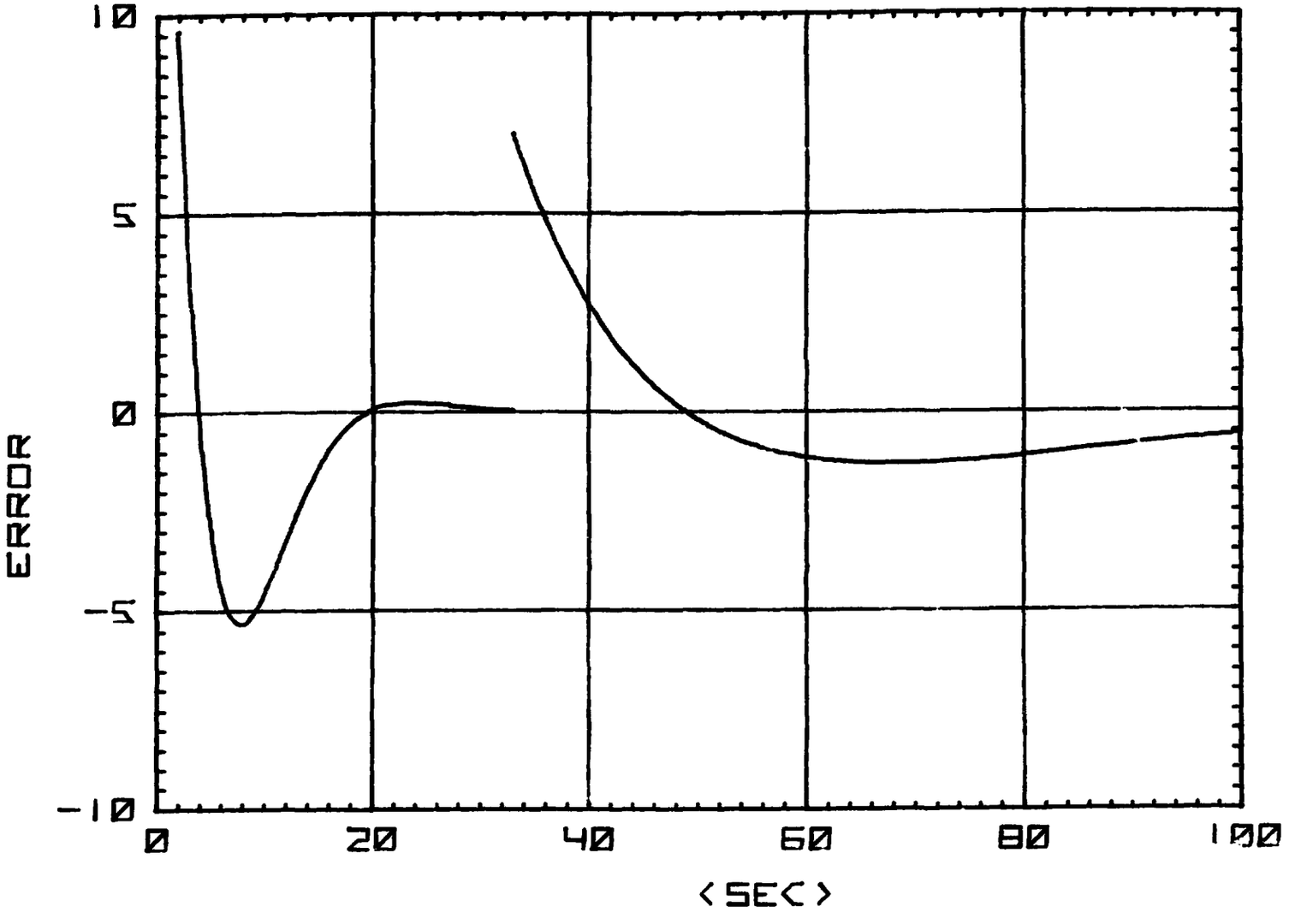


Figure 4.3.2.3-15(a). Response For Weak Signal, 20 kHz MRT, (positive)

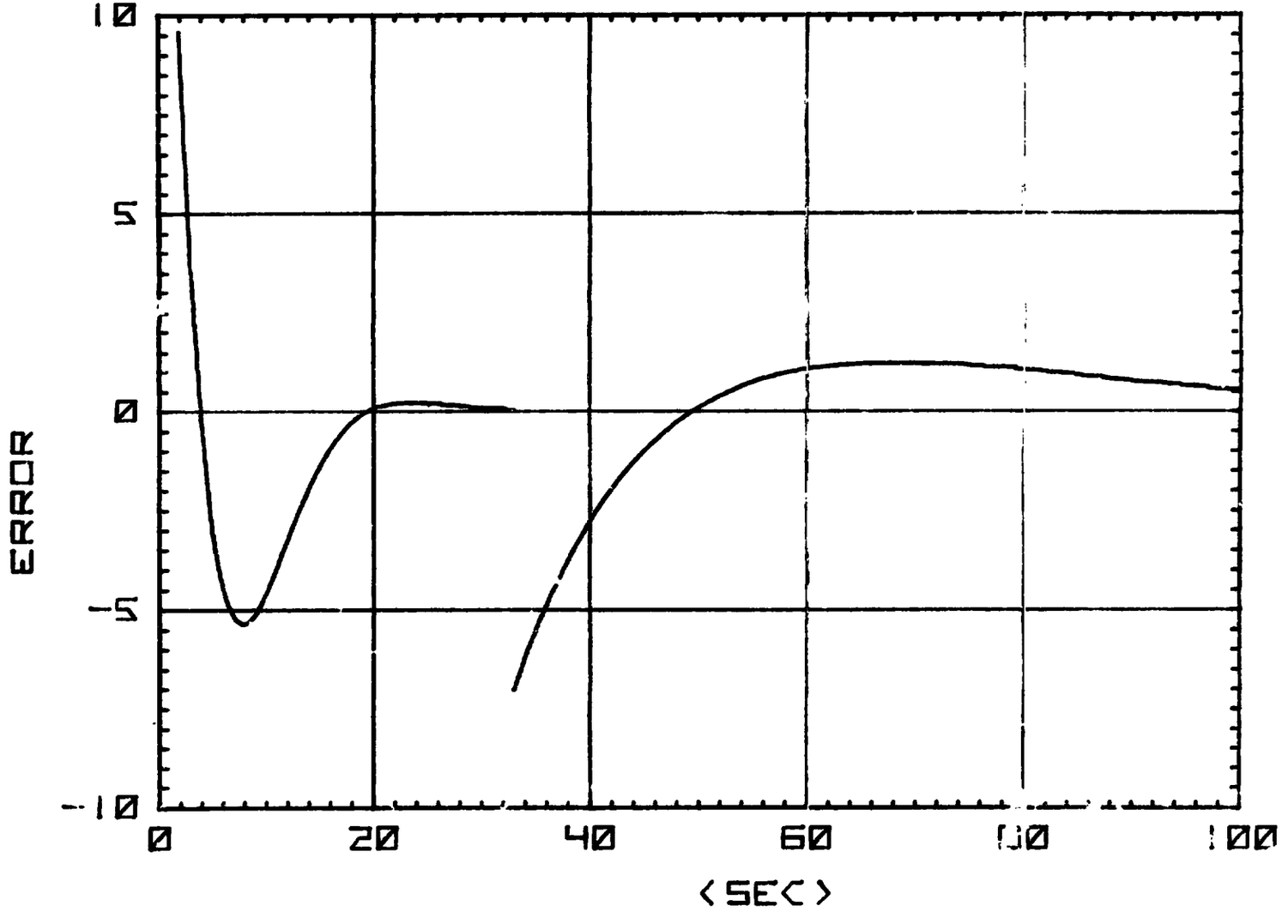


Figure 4.3.2 [illegible] Response For Weak Signal, 20 kHz MRT, (negative)

Table 4.3.2.3-2. Transient Response Summary

CONDITIONS	TOTAL ALLOWABLE ERROR (Degrees)	TRANSIENT ERROR ALLOCATION (Degrees)	TIME RQRD TO REACH ALLOCATION (Seconds)
S/φ = 50 dB - Hz			
500 kHz MRT	1.2	0.3	1.2
100 kHz MRT	0.32	0.16	1.5
20 kHz MRT	0.32	0.16	1.5
S/φ = 30 dB - Hz			
500 kHz MRT	1.2	0.8	13.0
100 kHz MRT	0.53	0.35	17.5
20 kHz MRT	0.53	0.35	17.5
S/φ = 12 dB - Hz			
500 kHz MRT	3.4	2.0	42
100 kHz MRT	3.4	2.0	42
20 kHz MRT	3.4	2.0	[illegible]

4.3.3 TRACKING PERFORMANCE

In all cases the MRT PLL will perform tracking in a third-order configuration with near perfect integrators. Thus, loop tracking phase errors due to velocity and constant acceleration dynamics will be near zero (less than 0.1°). Transient errors due to steps in velocity or acceleration dynamics can be predicted from Figures 4.3.2.3-5 and 4.3.2.3-6.

Other tracking errors, discussed in Paragraph 4.7.2, consist of systematic errors caused by phase detector and A/D converter drifts due to temperature, and random errors due to VCXO phase jitter and phase error digitizing.

Errors due to additive input thermal noise are discussed in Paragraph 4.7.3.

4.4 MINOR RANGE TONE CORRELATION

Operating together, the Range Tone Processor (RTP) and Digital Range Tone Extractor (DRTE) automatically synchronize the synthesized minor range tones with the received minor range tones in a prescribed sequence, starting with the highest minor tone and ending with the 10Hz tone.

The synchronization process for each tone consists of:

1. Correlation (phase comparison) of local tone with received tone
2. Deciding which of three possible levels the correlation function lies in
3. Correction of phase error in accordance with decision logic discussed in Paragraph 3.2.8, Table 3.2.8-1.
4. Repetition of steps (1) through (3) until agreement (peak correlation) is obtained.

In the absence of decision errors, at least two and not more than three correlations are required.

The correlation process is performed by a phase detector and an "integrate-and-dump" circuit.

For the 100 kHz through 800 Hz minor range tones, the correlation function is sinusoidal. For the 160 Hz through 10 Hz tones, the function is triangular.

This functional relationship between correlator output and the offset of phase match, θ_Δ, can be expressed as:

$$E_0 = (2/\pi)\, E_s \cos \theta_\Delta \qquad (100\ \text{kHz} \le \text{fm} \le 800\ \text{Hz})$$

$$= (2/\pi)\, E_s \left(1 - \left|\frac{\theta_\Delta}{90}\right|\right) \qquad \left\{\begin{array}{r} 160\ \text{Hz} \le \text{fm} \le 10\ \text{Hz} \\ |\theta_\epsilon| \le 180\ \text{deg} \end{array}\right\}$$

where

E_s = Amplitude of input range tone

Figure 4.4-1 is a graph of the two correlation functions normalized to unity. The possible correlator outputs (excluding any phase or amplitude error) for the various minor range tones are also indicated. The outputs for the 100 kHz through 800 Hz tones occur at one of five positions on the sinusoidal function and are separated in 72° (1/5-cycle) increments. The outputs for the 160 Hz tone also occur at one of five positions, but on the triangular transfer function. The outputs for the 40 Hz and 10 Hz tones occur at one of four positions on the triangular function and are separated in 90° (1/4-cycle) increments.

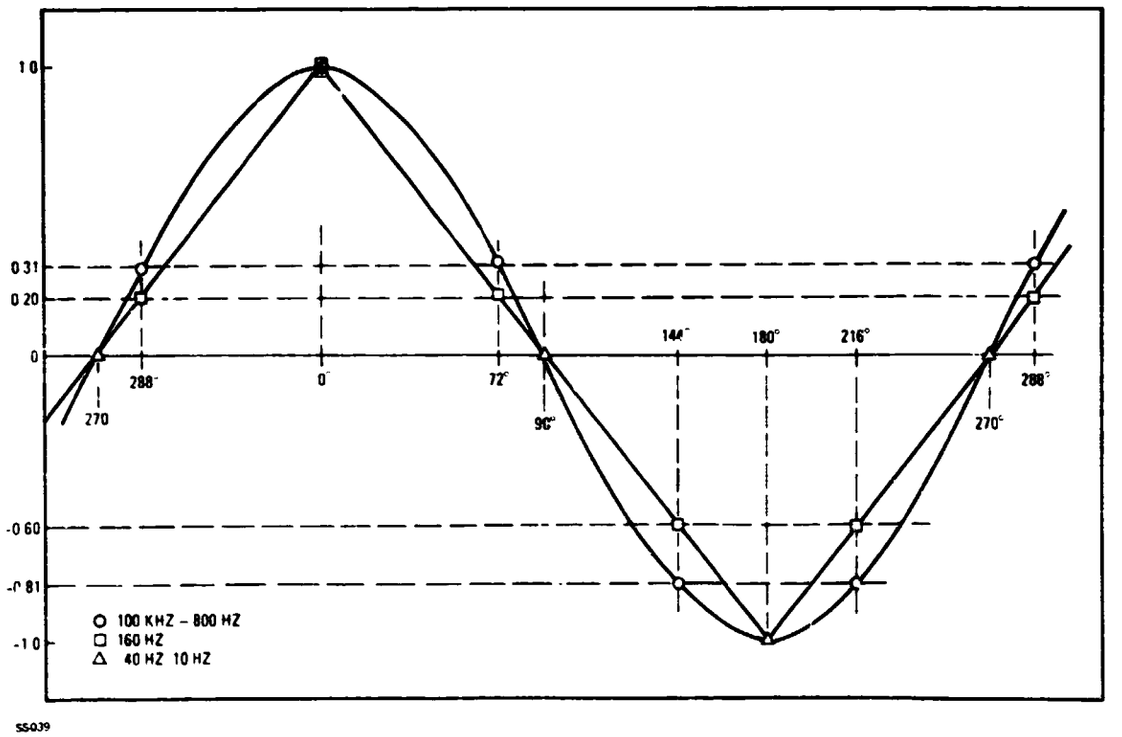


Figure 4.4-1. Correlator Outputs

The correlator output is compared to two different slicing (reference) levels and decisions made as to whether the correlator output is above or below the reference levels. These decisions provide information as to which of three states the apparent phase is in. These states correspond to:

State 1	0° (all tones)
State 2	±72° (100 kHz - 160 Hz) ±90° (40 Hz, 10 Hz)
State 3	±144° (100 kHz - 160 Hz) 180° (40 Hz, 10 Hz)

In the presence of a given noise level and with a given integration time, the difference in level between the slicing reference level and the nominal correlator output determines the probability of a decision error, P_e. Or contrarily, in the presence of a given noise level, and for a required decision error probability, the difference in levels determines the required integration time. This is stated mathematically as:

$$T = K/(S/\phi) \text{ sec}$$

where

T = Integration time

K = Function of error probability and level differences

S/ϕ = Signal-to-noise power density ratio

For $P_e = 10^{-3}$

$$K = 2.945/(a-b)^2$$

where

a = Limiting value of correlation output

b = Normalized value of slicing level

The nominal values for "a" are those corresponding to the various possible output levels shown in Figure 4.4-1. The limiting values, however, are different due to phase and amplitude drifts and other systematic errors which can occur. The ranges of "a" for the various tones are shown in Figure 4.4-2. These ranges correspond to phase errors of ±10° and amplitude errors of ±14%.

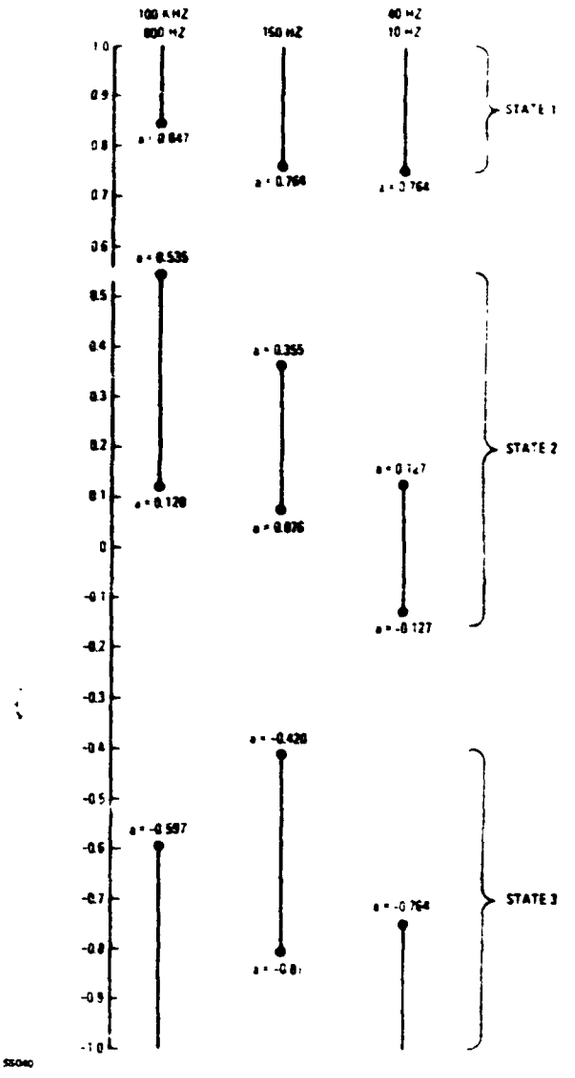


Figure 4.4-2. Normalized Correlation Output Limits

From the figure it can be seen that the worst-case situation occurs when making the decision as to State 1 or State 2 for the 100 kHz through 800 Hz tones. In this case the level limits are separated by 0.847 - 0.535 = 0.312. If the slicing level, "b", is set midway between the two values, then $|a-b| = 0.156$ and $(a-b)^2 = 0.0243$. Reference levels will be used in the Ranging Equipment such that this is the minimum value of $(a-b)^2$ in all cases. With this value, the maximum K is:

$$K = 2.945/0.0243 = 121$$

and the maximum required integration time is:

$$T = 121/(S/\phi) \text{ sec}$$

In all cases, the integration time used is at least this large and the $|a-b|$ value is at least 0.156. Thus, the decision error probability, P_e, will be less than 10^{-3}. In many situations the integration time used is longer and the $|a-b|$ value is considerably larger. Thus P_e will be considerably smaller.

Also, it should be noted that P_e is the probability of error for a single decision. With the phase matching logic used (Table 3.2.8-1), at least two decision errors are necessary to leave a tone improperly adjusted. Since the decisions are independent, the probability of that occurrence is:

$$(P_e)_1 = P_e^2 \leq 10^{-6}$$

Since as many as 7 tones are phase matched, the total probability of ambiguity error is:

$$(P_e)_T = 7(P_e)_1 \leq 7 \times 10^{-6}$$

The actual integration times selected for use are given in Table 4.4-1.

Table 4.4-1. Integration Times For Minor Range Tone Correlation

S/φ (dB-Hz)	INTEGRATION TIME (sec)
10 - 16	12.8
16 - 22	3.2
22 - 28	0.8
28 - 34	0.2
Above 34	0.05

4.5 CODE CORRELATION

Operating together, the Range Tone Processor, the Digital Range Tone Extractor and the Local ARC Generator automatically synchronize the local ARC with the received ARC. The synchronization process consists of:

1. Correlation (phase comparison) of local ARC with received ARC
2. Comparing apparent correlation level with decision level for decision that ARC is matched
3. Delaying local ARC by 16-bit position, if (2) is not satisfied
4. Repeating steps (1) through (3) until (2) is satisfied.

The correlation process is performed by a phase detector and an "integrate-and-dump" circuit. The input signals to the phase detector are the, (previously phase matched) received and local 4 kHz minor range tone pair which are bi-phase modulated with the received and local ARC respectively. The correlator integrates the phase detector output over an integral number of code bit periods, but over a time interval which in some cases is less than the code length.

The output of the correlator at each sample time, is:

$$E_0 = E_s (2/\pi) \text{ Cos } \theta_\Delta \qquad \text{Code Matched}$$

$$= E_s (2/\pi) C_{LR} \text{ Cos } \theta_\Delta \qquad \text{Code Not Matched}$$

where:

θ_Δ = Phase difference between local and received 4 kHz sub-carrier

E_s = Amplitude of input 4 kHz sub-carrier

C_{LR} = Cross-correlation between the local and received code when not matched

The value of C_{LR} depends on code position and the correlation interval. For the code selected, a digital computer was used to determine C_{LR} for a range of correlation intervals, expressed as the number of bits correlated. Results of that analysis are summarized in Figure 4.5-1 for intervals of interest; as can be seen $C_{LR} \leq 0.3125$ for an interval at least 0.2 second (32 bits). This has been chosen as the minimum integration time and will be the largest C_{LR}.

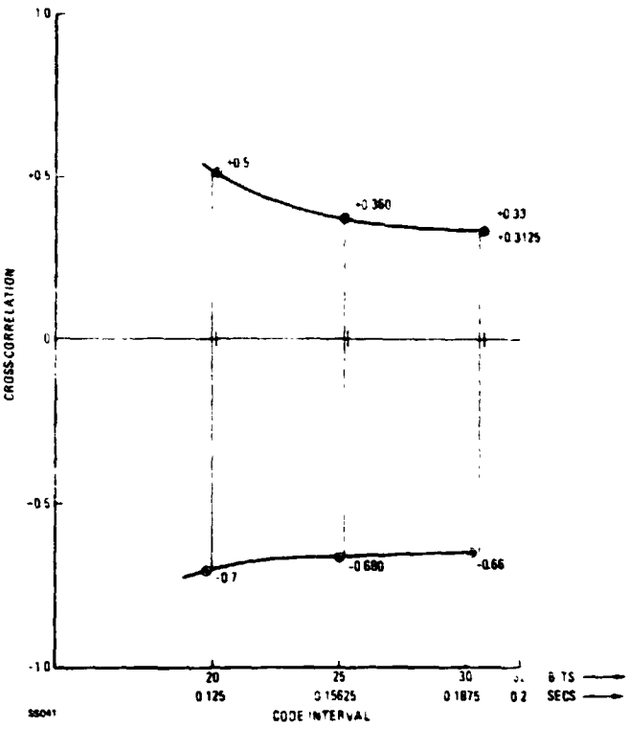


Figure 4.5-1. Bounds of Cross-correlation Between Unmatched Code

The required integration time, T, for a decision error probability of 10^{-6} is:

$$T = 6.96/(a-b)^2 \ (S/\phi)$$

Allowing ±10° error of sub-carrier phase match and ±14% signal amplitude error (same as for minor range tones), the boundary values of normalized E_0 ("a") are:

1. Code Matched
   Lower Limit = 0.86 Cos 10° = +0.847
2. Code Not Matched
   Upper Limit = (1.14 Cos 0°) (.3125) = +.356

Setting the slicing level, "b", at +0.601 gives a normalized separation value $|a-b| = 0.246$. Thus

$$K = \frac{6.96}{.246^2} = 115$$

and the required integration time is

$$T = 115/(S/\phi) \text{ sec}$$

for each code match decision.

In all cases, an integration time considerably longer than this is used and the decision error probability will be considerably less than 10^{-3}. (The actual integration times to be used are the same as the minor range tones. given in Table 4.4-1, except that the minimum time is 0.2 seconds.) For example at $S/\theta = 10$ dB, an integration time of 12.8 seconds will be used whereas the required minimum is:

$$T = 115/10 = 11.5 \text{ seconds}$$

Furthermore, for the relatively long integration times, the unmatched code cross-correlation factor, C_{LR}, will be much less than 0.3125 and the probability of deciding match — when actually unmatched — will be greatly improved.

For $S/\theta \geq 34$ dB, an integration time of 0.2 second will be used because this is the minimum value selected due to cross-correlation. The value required by noise considerations is, however, only

$$T = 115/2500 = 0.046 \text{ second}$$

Thus noise will cause decision errors with a probability much less than 10^{-6}.

4.6 RANGE DATA ACQUISITION

4.6.1 GENERAL PROCEDURE

The range data acquisition process comprises the execution of three separate sequences of action (Figure 4.6.1-1). The initial sequence of events starts with establishing level control of the MRT and ends with the major range tone PLL slewed to an approximate null error, with range tone AGC fully effective, and with the phase acquisition mode (FAST, MEDIUM, or SLOW) selected.

The other two sequences of events are executed in parallel; they separately culminate in:

1. Major range tone PLL operation in the appropriate bandwidth and 3rd order mode with major acquisition transient settled
2. Resolution of major range tone ambiguities with the minor range tones and the ARC

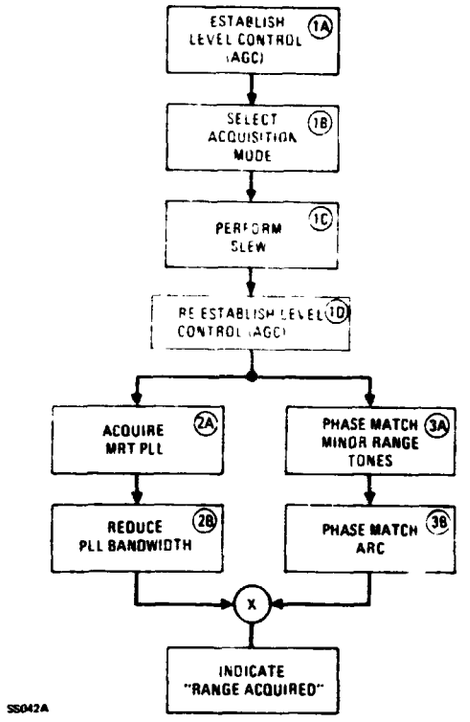


Figure 4.6.1-1. Acquisition Sequence

Manual control of operating mode (when effective during acquisition) deletes the S/ϕ determination action from the first sequence. After completion of acquisition, manual control results in change of PLL bandwidth (for change between FAST and MEDIUM).

The three sequences and their time schedule are discussed below.

4.6.2 AGC/SLEW SEQUENCE

The AGC/slew sequence sets up the initial conditions for the PLL acquire and ambiguity resolution sequences which follow. The actions which are completed during the AGC/slew sequence are:

1. Provide nominally correct major range tone power level into PLL and level sensing circuitry (establish AGC)
2. Determine the S/ϕ of the received major range tone and select the appropriate operating mode (FAST, MEDIUM, or SLOW) for the next sequences of data acquisition and for tracking
3. Slew PLL output signal to nominal null error with respect to input signal
4. Re-establish level control.

An acquisition mode selection of FAST, MEDIUM, or SLOW is made in accordance with:

Fast:	$S/\phi \geq 50$ dB - Hz
Medium:	50 dB - Hz $> S/\phi \geq 30$ dB - Hz
Slow:	30 dB - Hz $> S/\phi$

4.6.2.1 LEVEL CONTROL AND MODE SELECTION — The process of determining S/ϕ and selecting the operating mode is shown in Figure 4.6.2.1-1. Two basic decisions are made:

1. The major range tone is being received and is controlling amplifier gain
2. The S/ϕ value is above 50 dB - Hz, below 30 dB - Hz or between these two values.

The S/ϕ determination is made by comparison of the output of a wideband IF noise detector with two reference levels after AGC has had sufficient time to approach the final mean value.

4.6.2.2 SLEW — Slew of PLL output signal is initiated as soon as the operating mode is selected.

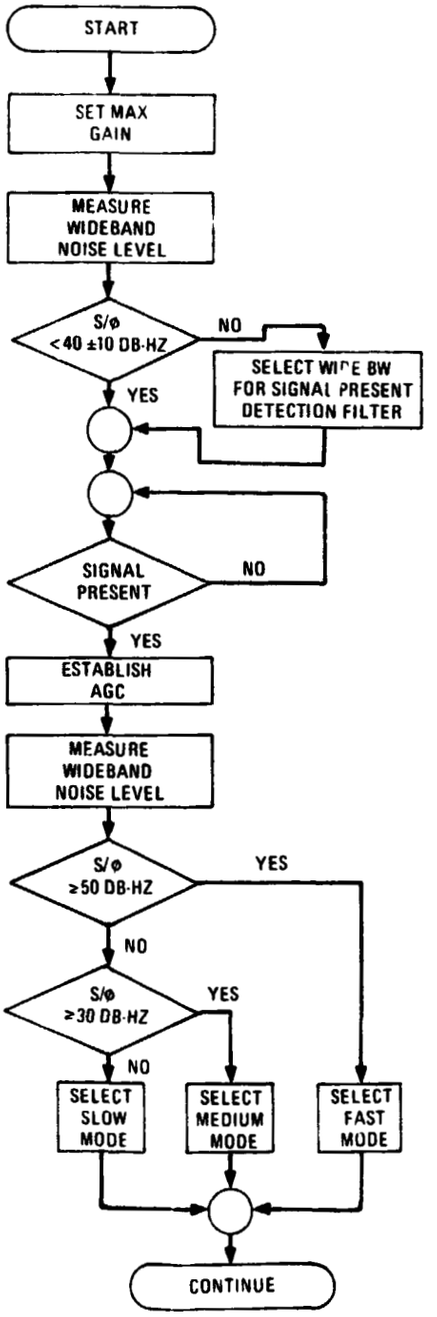
Digital logic (operating on filtered output signals of the coherent detectors which are used for PLL control and for AGC) controls a fast 180° digital slew and a slow analog slew of the PLL feedback signal. Filter bandwidths and slew rates are selected to minimize filter lag and S/N effect on phase error at end of slew consistent with the acquisition time requirements.

4.6.3 MRT PLL ACQUISITION

After slew is completed in the previous sequence, the MRT acquisition consists of:

1. Closing PLL in relatively wideband second-order configuration
2. Waiting for acquisition transients to sufficiently settle
3. Switching PLL to narrow bandwidth third-order configuration
4. Waiting for acquisition transients to sufficiently settle

The PLL performance and response to these steps are discussed in Paragraph 4.3.2.3.



SS043B

Figure 4.6.2.1-1. Automatic Mode Selection Process

4.6.4 AMBIGUITY RESOLUTION

Ambiguity resolution consists of phase matching all of the minor range tones and the ARC. These sequences are described in Paragraphs 4.4 and 4.5.

4.6.5 ACQUISITION TIME SUMMARY

4.6.5.1 GENERAL – The various steps required to achieve range data acquisition have been described; they consisted of:

1. AGC/Slew
2. MRT PLL Acquisition
3. Ambiguity Resolution

Steps (2) and (3) are conducted in parallel.

This section provides a summary of the total time to perform those steps for three key S/ϕ values. Not included in the acquisition time summaries are propagation delay times which will depend on range, and which can be substantial for very long ranges. For example, at lunar range, the round trip propagation time is approximately 2.47 seconds. Since there may be as many as 8 range tones plus the ARC transmitted sequentially, the total time lost due to propagation would be about 22.3 seconds.

4.6.5.2 AGC/SLEW – The initial AGC bandwidth is approximately 0.5 Hz (one-sided noise). Allowing about 2.5 time constants for settling of AGC, the signal will be properly level controlled in approximately 1.25 second at a modulation index of 0.2 rad. At $\beta = 0.5$ rad, the 1.25 second time is reduced to 0.75 second. At that time, the following actions can be taken:

1. Detect signal presence
2. Select acquisition mode (FAST, MEDIUM, SLOW)
3. Start slew

For all signal cases, slew will require 1.0 second at most.

After slew is completed the AGC bandwidth is reduced and the MRT PLL acquisition and ambiguity resolution processes are started in parallel. For strong signals, 0.5 seconds is required to re-establish the correct level of AGC; for $S/\phi \leq 50$ Db-Hz, 4 seconds is required.

4.6.5.3 MRT PLL ACQUISITION – The major range tone PLL is considered fully acquired when its acquisition transient errors have settled to an allowable value. The

allowable values and required maximum times were given in Table 4.3.2.3-2. In summary, the maximum required times were:

Strong Signal 1.5 secs
Medium Signal 17.5 secs
Weak Signal 42 secs

4.6.5.4 AMBIGUITY RESOLUTION – The ambiguity resolution process consists of a series of sequences:

1. Integrate and compare (correlation)
2. Dump and correct (correction)

The times for each event are determined by the S/ϕ values and the tone or ARC being operated upon; see Table 4.6.5.4-1.

Table 4.6.5.4-1. Schedule of Correlation and Correction Intervals

S/ϕ (dB - Hz)	Correlation (T_1) (secs)	Correction (T_2) (msecs)	Applicable Signals
10-16	12.8	50	All minor tones and ARC
16-22	3.2	50	All minor tones and ARC
22-28	0.8	50	All minor tones and ARC
28-34	0.2	50	All minor tones and ARC
> 34	0.05	1.25	800 Hz & above
> 34	0.05	6.25	160 Hz
> 34	0.05	25	40 Hz
> 34	0.05	50 to 100	10 Hz
> 34	0.2	50	ARC

If no decision errors are made during the process, at most 3 correlation and correction cycles are required for each minor range t For the strong signal case, the range should be within the 10 Hz ambiguity range and only one ARC correlation should be required to verify that fact. For the medium signal strength, it is assumed that the ARC can be preset so that, at most, 10 correlation and correction cycles are required. For the weak signal case, no preset knowledge is assumed.

Summaries of the ambiguity resolution times are given for the three signal strength cases in Tables 4.6.5.4-2 through 4.6.5.4-4.

Table 4.6.5.4-2. Correlation and Correction Time Summary for $S/\phi = 50$ dB - Hz

Signal	Time (msec)		
	Correlation (T_1)	Correction (T_2)	Total $n(T_1 + T_2)$*
100 kHz	50	1.25	153.75
20 kHz	50	1.25	153.75
4 kHz	50	1.25	153.75
800 Hz	50	1.25	153.75
160 Hz	50	6.25	168.75
40 Hz	50	25	225
10 Hz	50	50 to 100	450
ARC	200	50	250
Maximum Total Time 1.69 sec			

* n = 3 for all tones
n = 1 for ARC

Table 4.6.5.4-3. Correlation & Correction Time Summary for S/ϕ = 30 dB - Hz

Signal	Time (msec)		
	Correlation (T_1)	Correction (T_2)	Total $n(T_1 + T_2)$*
100 kHz	200	50	750
20 kHz	200	50	750
4 kHz	200	50	750
800 Hz	200	50	750
160 Hz	200	50	750
40 Hz	200	50	750
10 Hz	200	50 to 190	900
ARC	200	50	2500
Maximum Total Time (Sec) 7.9 Seconds			

* n = 3 for all tones
n = 10 for ARC

Table 4.6.5.4-4. Correlation & Correction Time Summary for S/ϕ = 12 dB - Hz

Signal	Time (msec)		
	Correlation (T_1)	Correction (T_2)	Total $n(T_1 + T_2)$*
100 kHz	12,800	50	38,550
20 kHz	12,800	50	38,550
4 kHz	12,800	50	38,550
800 Hz	12,800	50	38,550
160 Hz	12,800	50	38,550
40 Hz	12,800	50	38,550
10 Hz	12,800	50 to 100	38,700
ARC	12,800	50	539,700
Maximum Total Time 809.7 seconds (13.5 minutes)			

* n = 3 for all tones
n = 42 for ARC

4.6.5.5 TOTAL TIME – A summary of the total acquisition time for each of the three cases is given in Table 4.6.5.5-1. The total time consists of the AGC/Slew time plus the longer of the MRT PLL acquisition or the ambiguity resolution time.

Table 4.6.5.5-1. Total Acquisition Time Summary

Sequence	Time (Sec)		
	S/ψ = 50 dB	S/ϕ = 30 dB - Hz	S/ϕ = 12 dB - Hz
① AGC/Slew	2.25**	6.25	6.25
② MRT PLL Acquisitions	1.5	17.5	42
③ Ambiguity Resolution	1.69	7.90	809.7
Total Acq Time (Sec)*	3.94	21.75	841

*Larger of ① + ② and ① + ③

**At $\beta \geq 0.5$ rad.

4.7 RANGE MEASUREMENT ERROR

This error analysis of range measurement performance is consistent with the following definitions:

RANGE RESOLUTION — The smallest measurable quantity that will yield a deterministic output range value.

RANGE INSTRUMENTAL ACCURACY — Range instrumental accuracy includes all random and systematic errors due to the Ranging Equipment hardware in the presence of an infinitely high input S/N ratio.

RANGE ACCURACY — Consists of range instrumental accuracy plus the effect of receiver input thermal noise. Error due to uncertainty in initial zero-set and knowledge of the velocity of propagation is not included.

The unit used to express range measurement requirements and performance is the meter. Table 4.7-1 provides a set of conversion factors used in the range measurement error analysis.

Table 4.7-1. Range Measurement Conversion Factors

UNITS	FORMULA*	FREQUENCY, f		
		500 kHz	100 kHz	20 kHz
nsec/cyc	$10^9/f$	2,000	10,000	50,000
nsec/degree	$10^9/360f$	$5.5\overline{5}$	$27.\overline{7}$	$138.\overline{8}$
degrees/nsec	$360f/10^9$	0.18	0.036	0.0072
meters/cyc	c/2f	300	1500	7500
meters/degree	c/720f	$0.8\overline{3}$	$4.1\overline{6}$	$20.8\overline{3}$
degrees/meter	720f/c	1.2	0.24	0.048
meters/nsec	$c/(2 \times 10^9)$	0.15	0.15	0.15

*All factors for range are one way
Velocity of propagation c taken as 3×10^8 meters/sec.

4.7.1 RANGE RESOLUTION

The range resolution, as defined above, is set by the number of increments per cycle used in measuring phase delay of the major range tone; it is given by:

$$\Delta R = c / 2Mf_m$$

where,

ΔR = Resolution (increment size)

c = Velocity of propagation, 3×10^8 meters/second

M = Number of delay increments per cycle

f_m = Major range tone frequency

The value of the product Mf_m is the same for 500 kHz, 100 kHz, or 20 kHz and is (using the values of M and f_m for the 500 kHz range tone):

$$Mf_m = (2 \times 10^3)\ (5 \times 10^5) = 10^9.$$

Thus, the resolution is:

$$\Delta R \simeq 3 \times 10^8 / 2 \times 10^9 = 0.15 \text{ meter}$$

4.7.2 RANGE INSTRUMENTAL ACCURACY

Range instrumental accuracy is limited by systematic and random errors occurring within the Ranging Equipment. The errors of concern are those associated with the fine-range data signal processing. Intermediate- and coarse-range data is used only to resolve ambiguities in the fine-range data. The fine-range data signal processing and information flow is illustrated in Figure 4.7.2-1.* For reference purposes, some of the signal processing elements in the diagram have been arbitrarily numbered. The errors discussed below are those contributed by the Ranging Equipment. Errors contributed by sources outside the Ranging Equipment (part of the RF Link, Figure 4.7.2-1) are not included. For example, group delay variations in the Exciter, MFR, and Transponder will contribute error to the ranging measurement, but are not included in the analysis since they are not part of the Ranging Equipment. Ranging accuracy as discussed in Paragraph 4.7.2, however, does include input thermal noise error.

4.7.2.1 SYSTEMATIC ERRORS — Systematic errors result from modulation group delay and phase variations within the processing elements as a result of temperature

*For convenience bound in Appendix A.

change and signal frequency dynamics (doppler and doppler rate). Table 4.7.2-1 summarizes the errors by cause for elements shown in Figure 4.7.2-1. The errors are individually discussed below.

4.7.2.1.1 Temperature Change — The temperature variation within the cabinet is estimated to be ±12° F (see Paragraph 3.1.1). Most of the Ranging Equipment circuitry operates over that range and the following analyses and estimates are based on that temperature variation. Selected elements, however, are controlled through heater circuits to operate over smaller temperature variations. For those elements, the error analyses and estimates are based on the controlled temperature variation.

Filters 1A, 1B, and 1C are all 2-pole LC, bandpass filters with a Q of 2. Over the operating temperature range, the fractional detuning will be less than ±200 ppm resulting in a phase shift of less than ±0.1°.

Filters 2A, 2B, and 2C are all LC filters with a half-power bandwidth of 70 kHz. The 500 kHz and 100 kHz filters are 1-pole bandpass, and the 20 kHz filter is a 2-pole low-pass. Over the operating temperature range, (the 500 kHz filter is temperature controlled) the fractional detuning and resulting phase shift will be less than the following values:

Filter No.	Fractional Detuning	Phase Shift (degrees)
2A	±100 ppm	±0.08
2B	±500 ppm	±0.08
2C	±500 ppm	±0.016

Filter 6 is an LC, 2-pole low-pass filter with a cutoff frequency of 1 MHz. Detuning due to temperature variations will result in these phase delay variations:

Major Range Tone Frequency	Maximum Phase Shift (Degrees)
500 kHz	±0.05
100 kHz	±0.01
20 kHz	±0.002

Filter 3 is a 1-pole bandpass crystal filter with a half-power bandwidth of 100 Hz. Over its controlled temperature range, the phase shift will be less than ±0.15°.

Filter 4 is a 1-pole LC filter with a half-power bandwidth of 100 kHz; however, this filter, as well as the axis-crossing detector (ACD 3) which follows it, is within the major range tone PLL. Thus slowly varying phase shifts caused by temperature changes will be tracked out and not contribute error to the ranging measurement.

Table 4.7.2-1. Systematic Range Error Summary

ERROR SOURCE	MRT → / ERROR →	500 kHz DEG	500 kHz NSEC	100 kHz DEG	100 kHz NSEC	20 kHz DEG	20 kHz NSEC
TEMPERATURE CHANGE							
Filter 1		0.1	0.6	0.1	2.8	0.1	13.9
2		0.08	0.4	0.08	2.2	0.016	2.2
3		0.15	0.83	0.15	4.2	0.15	20.8
4		-	-	-	-	-	-
5		0.035	0.2	0.007	.2	0.002	0.2
6		0.05	0.3	0.01	.3	0.002	0.3
ACD 1		-	-	-	-	-	-
2		0.18	1.0	0.036	1.0	0.007	1.0
3		-	-	-	-	-	-
4		-	-	-	-	-	-
AGC & Demodulator		0.18	1.0	0.036	1.0	0.007	1.0
Rate Aid		-	-	-	-	-	-
Major Range Tone PLL		0.1	0.6	0.1	2.8	0.1	13.9
Phase Data Multiplier PLL		0.1	0.6	0.02	.6	0.004	0.6
RSS (Temperature)		0.36	2.0	0.23	6.4	0.21	28.8
SIGNAL FREQUENCY DYNAMICS							
Filter 1		-	-	-	-	-	-
2		0.08	0.4	.016	.4	0.003	0.4
3		0.003	0.02	.0007	.02	0.00013	0.02
4		-	-	-	-	-	-
5		-	-	-	-	-	-
6		0.05	0.28	0.01	0.28	.002	0.28
ACD 1		-	-	-	-	-	-
2		-	-	-	-	-	-
3		-	-	-	-	-	-
4		-	-	-	-	-	-
AGC & Demodulator		-	-	-	-	-	-
Rate Aid		-	-	-	-	-	-
Major Range Tone PLL		0.1	0.6	0.1	2.8	0.1	13.9
Phase Data Multiplier PLL		0.01	0.03	0.001	.03	0.0002	0.03
RSS (Dynamics)		0.14	0.77	0.10	2.84	0.10	13.9
RSS Total		0.38	2.14	0.25	7.0	0.23	32.0
RSS Total (Meters)		0.32		1.05		4.8	

Filter 5 is an LC, 1-pole bandpass filter with a half-power bandwidth of 3.2 MHz. Over the environmental temperature range the fractional detuning will be ±20% resulting in a 48 MHz phase shift of ±3.5°. However, this phase shift is divided by 100 prior to injection into the data processing signal path. Thus the error contribution is ±0.035° at 500 kHz. The equivalent errors for the 100 kHz and 20 kHz MRT are ±0.007° and ±0.0013° respectively. ACD 1 is common to the transmitted major range tone and reference signal paths; thus, slowly varying time delays are cancelled and do not contribute error to the ranging measurement.

ACD 2 operates at 48 MHz and has time delay variation due to temperature of less than 1 nanosecond. This results in a phase shift at 480 kHz and in the data signal path of less than ±0.18°. This is the error for the 500 kHz MRT. However, the equivalent error for the 100 kHz and 20 kHz MRT is divided by 5 and 25 respectively.

ACD 4 is within the Phase Data Multiplier PLL. Thus slowly varying drifts will be tracking out and not contribute to error in the ranging measurement.

Rate aid signals are employed in the data path in such a manner that slowly varying phase shifts in the rate aid circuitry will be cancelled and thus not contribute error to the ranging measurement.

The AGC and demodulator circuits are designed for low group delay variation over the range of operating temperature, noise, and signal levels. The variation is predicted at less than ±1 nanosecond.

Major range tone PLL tracking errors are caused by phase detector and A/D converter drifts. Due to noise handling requirements, these units have a large dynamic operating range and drifts are predicted at ±0.1° for the combined effect using temperature control.

For the phase data multiplier PLL, noise handling and dynamic range requirements are small. Thus phase detector drifts can be less than ±0.1° at the tracking frequency. The equivalent error at the MRT frequency is ±0.1° for the 500 kHz MRT, ±0.1/5 for the 20 kHz MRT, and ±0.1/25 for the 20 kHz MRT.

4.7.2.1.2 Signal Frequency Dynamics — Since there are no signal frequency dynamics on the reference signals, elements in the reference signal processing circuitry do not contribute error due to signal frequency dynamics. Elements in this category are ACD 1, ACD 2, Filter 1, and Filter 5.

Again, because of cancellation, the rate aid circuitry also does not contribute error. And again because of being within PLL's ACD 3, ACD 4, and Filter 4 do not contribute error. Because the demodulator operates at a constant 110 MHz, it also does not contribute error due to signal frequency dynamics.

The range tones passing through Filters 2A, 2B, and 2C have their full doppler since rate aid has not yet been injected. Phase shift through these filters (all of which have a 70 kHz half-power bandwidth) due to doppler is:

Filter No.	Maximum Doppler	Maximum Phase Shift (degrees)
2A	± 50 Hz	±0.08
2B	± 10 Hz	±0.016
2C	± 2 Hz	±0.003

Similarly the range tones passing through Filter 6 have full doppler. Phase shifts due to Doppler in this filter are:

Major Range Tone Frequency	Maximum Phase Shift (degrees)
500 kHz	±0.05
100 kHz	±0.01
20 kHz	±0.002

The range tone passing through Filter 3 has been rate aided; thus only residual doppler is present. This residual is only 1/17,600 times the original doppler. Phase shift due to doppler is:

Major Range Tone Frequency	Maximum Residual Doppler (Hz)	Maximum Phase Shift (degrees)
500 kHz	$\pm 2.84 \times 10^{-3}$	±0.0031
100 kHz	$\pm 5.68 \times 10^{-4}$	±0.0007
20 kHz	$\pm 1.14 \times 10^{-4}$	±0.00013

Because of its relatively wide tracking bandwidth (2 kHz) and large dc gain, the Phase Data Multiplier PLL has small tracking error due to signal frequency dynamics. When tracking, the error is a maximum of ±0.005° referred to the PLL input. This is the error for the case of the 500 kHz MRT. With 100 kHz and 20 kHz MRT frequencies, the equivalent phase error is divided by 5 and 25 respectively.

The Major Range Tone PLL tracking errors due to velocity and constant acceleration dynamics at strong signal are less than ±0.1°.

4.7.2.2 RANDOM ERRORS — Random errors result from phase jitter which is present on the output signal which is digitized as a measure of phase delay, from the quantizing error itself, and from sampling pulse jitter. Phase jitter may be caused by self-generated noise, spurious signal presence, power supply ripples or any other random fluctuations which result in rapid variations in axis crossings of the digitized waveform. Table 4.7.2-2 is a summary of random erros which are individually discussed below.

4.7.2.2.1 Reference Range Tone — Jitter appears on the transmitted major range tone due to jitter introduced by ACD 1 and by elements of the clocked divider chain in the Range Tone Generator. Very narrowband processing of the received tone by the major range tone (MRT), PLL, however, reduces this jitter to a negligible amount.

Table 4.7.2-2. Random Range Error Summary

ERROR SOURCE	MRT →	500 kHz		100 kHz		20 kHz	
	RMS ERROR →	DEG	NSEC	DEG	NSEC	DEG	NSEC
Reference Range Tone							
Rate Aid		0.4	2.2	0.08	2.2	0.016	2.2
MRT PLL Tracking		0.15	0.8	0.15	4.2	0.15	21
MRT PLL VCXO		0.1	0.6	0.02	0.6	0.004	0.6
500 kHz ACD		0.18	1.0	0.036	1.0	0.007	1.0
PDM Reference		0.18	1.0	0.036	1.0	0.007	1.0
PDM VCO		0.2	1.1	0.04	1.1	0.008	1.1
40 MHz ACD		—	—	—	—	—	—
Quantizing		0.05	0.3	0.01	0.3	0.002	0.3
Sampling Pulse		0.015	0.1	0.003	0.1	0.0006	0.1
RSS		0.54	3.0	0.19	5.1	0.16	21.2
RSS (Meters)		0.45		0.80		3.2	

4.7.2.2.2 Rate Aid — Jitter on the rate aid signal injected into mixers M1 and M3 are reduced to a negligible amount by the MRT PLL. Jitter on the 2.1$\bar{6}$ MHz rate aid signal injected into Mixer M2 however, is fully translated to the data signal. The jitter on the rate aid signal is due to axis-crossing detection, digital division, and spurious signal presence all developed in the Rate Aid Synthesizer. All of these effects will result in phase jitter on the 500 kHz data signal in the amount of 0.4° rms. The equivalent phase error for the cases of 100 kHz and 20 kHz MRT frequencies are 0.4/5° and 0.4/25° rms respectively.

4.7.2.2.3 MRT PLL Tracking — Because of the very narrow bandwidths required, the Major Range Tone PLL is partially implemented using digital techniques. The phase error signal is quantized using an A/D converter and then loop compensation (filtering) performed digitally. The digital output is then converted to analog form to control the PLL VCXO. Because the error signal is quantized into finite increments, random phase tracking errors will occur. The quantizing size will be such that the phase tracking error will be less than 0.15° rms referred to the PLL input.

4.7.2.2.4 MRT PLL VCXO — The VCXO used in the MRT PLL is a very stable oscillator, but operates in an extremely narrowband PLL. Phase fluctuations which are not tracked out appear as phase jitter on the 500 kHz data signal. This phase jitter will be less than 0.1° rms at the 500 kHz PLL output. The equivalent error for 100 kHz and 20 kHz MRT is 0.1/5° and 0.1/25° respectively.

4.7.2.2.5 500 kHz ACD — ACD 3 is in the feed forward path of the MRT PLL. Therefore, slowly varying time errors are tracked out. Rapid time variations, however, do appear as phase jitter on the 500 kHz data signal. The ACD time jitter will be less than 1 nanosec rms, corresponding to 0.18° rms on the 500 kHz data signal. The equivalent phase error for the cases of 100 kHz and 20 kHz MRT is 0.18/5° and 0.18/25° rms respectively.

4.7.2.2.6 PDM Reference — The 480 kHz Phase Data Multiplier reference signal introduces jitter into the data signal path. The jitter results from ACD 2 and the ÷100 scaler which are used to develop the 480 kHz reference. The time jitter will be less than 1 nanosecond rms, corresponding to 0.18° rms on the data signal. The equivalent phase error for the cases of 100 kHz and 20 kHz MRT are 0.18/5° and 0.18/25° rms respectively.

4.7.2.2.7 PDM VCO — Self-generated noise on the VCO used in the Phase Data Multiplier also introduces phase noise on the data signal. Although the VCO is relatively wideband and noisy, the PDM PLL is also relatively wideband and thus most of the noise is removed or reduced by feedback. The residual error will be less than 0.2° rms referenced to the PDM input. This corresponds to equivalent phase error of 0.2°, 0.2/5°, and 0.2/25° rms for MRT frequencies of 500 kHz, 100 kHz, and 20 kHz respectively.

4.7.2.2.8 40 MHz ACD — Errors introduced by ACD 4 time jitter are negligible because:

1. The basic time jitter is small
2. Referenced to the PDM input, the error is divided by 2000
3. The ACD is in the feed forward path of the PDM PLL, and most of the jitter is removed by feedback.

4.7.2.2.9 Quantizing Error — The quantizing error due to the use of a finite number of increments per cycle of the 500 kHz output signal of the PDM is the square root of the variance of an error function having a uniform distribution between zero and one-half increment. The rms equivalent time error due to sampling phase of a 500 kHz signal counted in 2000 increments is (1 nsec)/ $\sqrt{12}$ = 0.29 nanosecond which is equivalent to 0.05° rms at the PDM input. This corresponds to phase errors of 0.05°, 0.05/5° and 0.05/25° for MRT frequencies of 500 kHz, 100 kHz, and 20 kHz.

4.7.2.2.10 Sampling Pulse — The 10 PPS sampling pulse has time jitter due to ACD 1 and digital selection circuitry. The time jitter will be less than 2 nanoseconds rms. This time jitter translates to phase error at the 20 kHz translated data phase and is therefore equivalent to 0.0144° rms. The equivalent phase error for MRT frequencies of 500 kHz, 100 kHz, and 20 kHz is 0.0144°, 0.0144/5°, and 0.0144/25° respectively.

4.7.3 RANGE ACCURACY

As stated above, range accuracy consists of range instrumental accuracy plus the effect of receiver input thermal noise. The thermal noise error contribution is given by:

$$\sigma_R = \frac{c}{4\pi f_m} \sqrt{B_n} / \sqrt{S/\phi}$$

Where:

c = Velocity of propagation, 3×10^8 meters/sec

f_m = Range tone frequency

B_n = Tracking loop noise bandwidth (one sided)

S/ϕ = S/N power density for received range tone

Figure 4.7.3-1 depicts range accuracy for each major tone as a function of S/ϕ for each of the two possible final tracking bandwidths.

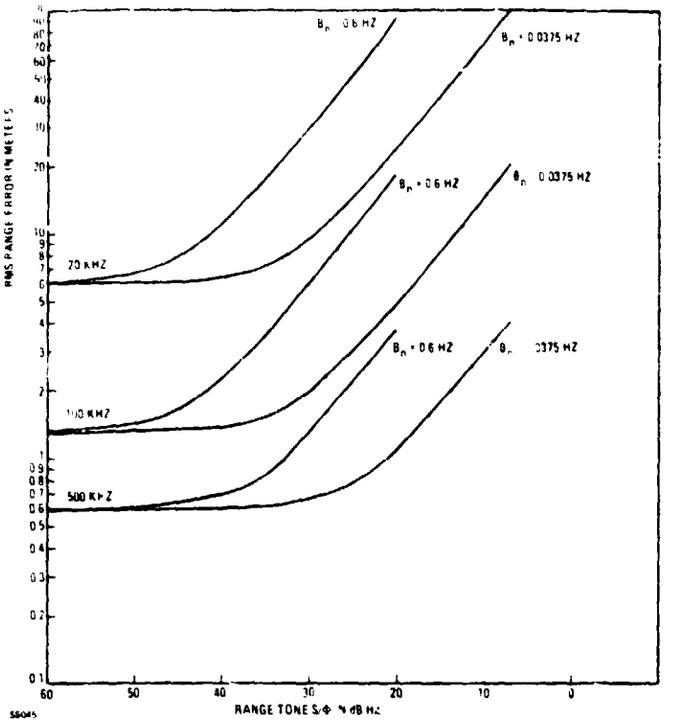


Figure 4.7.3-1. Range Accuracy for Major Tones

4.8 DOPPLER MEASUREMENT ERROR

This error analysis for doppler measurement performance is consistent with the following definitions:

DOPPLER RESOLUTION - The smallest measureable quantity that will yield a deterministic change of doppler cycle count.

DOPPLER INSTRUMENTAL ACCURACY - Includes all Ranging Equipment errors of cycle count measurement made during a 0.1 second interval.

DOPPLER ACCURACY - Doppler instrumental accuracy plus the effect of receiver VCXO phase noise.

The unit of measure used in expressing doppler measurement requirements and performance is the cycle.

4.8.1 DOPPLER RESOLUTION

The doppler resolution, as defined above, is set by the number of increments per cycle used in accumulating a count of elapsed cycles of the doppler (with bias) signal. The increment size is independent of the bias frequency.

Since the extracted doppler (plus bias) signal is multiplied by 1000 (with additional bias changes) before counting elapsed cycle increments, the doppler resolution is 0.001 cycle.

4.8.2 DOPPLER INSTRUMENTAL ACCURACY

Doppler instrumental accuracy is determined by Ranging Equipment random errors, since, by definition, a systematic error is slowly varying and does not appreciably affect short-term (0.1 second) measurements. (The doppler data signal flow within the Ranging Equipment is illustrated in Figure 4.1-1, Appendix A.) Ranging Equipment random error sources contributing to error-of-cycle count over a 0.1 second interval are summarized in Table 4.8.2-1 and discussed below. Errors contributed by sources outside the Ranging Equipment are not included. For example, phase noise present on the MFR VCO, the MFR Synthesizer reference, and the Exciter reference will contribute error, but are not included in the analysis since they are not part of the Ranging Equipment. Doppler accuracy, (discussed in Paragraph 4.9) does include error due to MFR VCO phase noise (due to additive input thermal noise), however.

Table 4.8.2-1. Random Doppler Instrumental Error Summary

ERROR SOURCE	RMS ERROR	
	DEGREES	CYCLE
DOPPLER EXTRACTOR		
Combined Processing	1.0	0.002
DOPPLER MULTIPLIER		
Reference Frequencies	1.0	0.0028
PLL VCO	1.8	0.0050
DOPPLER COUNTER		
Digital Circuitry	0.7	0.0020
Quantizing	0.1	0.0003
RSS Cycle Count Error	2.40	0.0067
RSS Interval Count Error	3.40	0.0094

4.8.2.1 DOPPLER EXTRACTOR PROCESSING. The Doppler Extractor (Figure 3.2.13-1) performs frequency multiplication, division, and mixing of various input signals to obtain the bias-plus-doppler-data signal. This signal processing can introduce phase noise, primarily due to imperfect suppression of undesired products (spurious signals). The Doppler Extractor has been designed to minimize these spurious and reduce the suppression problems. A combined error of 1.0° rms has been allowed for the Doppler Extractor. This is the error present at its output and corresponds to 2.8 counts rms error at the Doppler Counter output.

4.8.2.2 DOPPLER MULTIPLIER PROCESSING. The Doppler Multiplier (Figure 3.2.14-1) performs mixing and PLL frequency multiplication of the bias plus doppler data signal.

REFERENCE FREQUENCIES - Mixing (frequency translation) is performed using reference frequencies from the Fixed Frequency Synthesizer. As in the Doppler Extractor, these reference frequencies can introduce phase jitter into the doppler data due to spurious signal presence. A combined error of 1.0° rms, referred to the

Doppler Multiplier input, has been allowed. This corresponds to 2.8 counts rms at the Doppler Counter output.

PLL VCO - VCO phase jitter due to self-noise is a principal error source. This noise is reduced due to feedback, and will have a residual error (after feedback reduction) of less than 1.25 cycles rms at the Doppler Multiplier output. This corresponds to 1.25/250 = 5/1000 cycles (1.8°) error at the Doppler Multiplier input.

4.8.2.3 DOPPLER COUNTER

DIGITAL CIRCUITRY - The Doppler Counter accumulates a count which equals 250 times the number of whole cycles of input-bias-plus-doppler. In addition, the counter determines the number of 1/4-cycle increments at each sample time. This combines to give an increment the size of 1/1000 cycle of the input-bias-plus-doppler frequency. Ideally, the counter would contribute no error other than the quantizing error discussed below. To allow margin due to the high counting speeds, however, an error of 2 counts (2/1000 cycle) rms is arbitrarily assigned.

QUANTIZING - Data is sampled regularly at a 10 pps rate. The quantizing error due to the 1/1000 cycle increment size is:

$$\sigma_q = \left(\frac{1}{1000}\right)\left(\frac{1}{\sqrt{12}}\right) = 0.0003 \text{ cycle rms}$$

4.8.2.4 SUMMARY - The random errors discussed above are assumed to be uncorrelated over a 0.1 second or longer interval. The resultant cycle count error at any sample time is obtained as the RSS of the random errors and is given in Table 4.8.2-1.

The error in cycle measurement over any sampling interval of 0.1 second or greater is the RSS of the errors for each sample or:

$$\text{RSS Interval Count Error} = \sqrt{2} \text{ cycle count error}$$

This value is also given in Table 4.8.2-1.

As a matter of interest, the rms frequency and range rate measurement errors are

$$\sigma_f = \frac{\sqrt{2}\,\sigma_\phi}{\Delta t}$$

$$\sigma_{\dot{R}} = \frac{c}{2f_c}\,\sigma_f$$

where,

σ_f = RMS frequency measurement error

σ_ϕ = RMS phase measurement error (cycle count error)

Δt = Time interval of measurement

$\sigma_{\dot{R}}$ = RMS range rate measurement error

C = Velocity of propagation

f_c - Carrier frequency

If f_c = 2250 MH , Δt = 0.1 seconds and σ_ϕ = 0.0067 cycle, then

$$\sigma_f = 0.094 \text{ Hz}$$

and,

$$\sigma_{\dot{R}} = 0.0063 \text{ meter/sec.}$$

4.8.3 DOPPLER ACCURACY

Doppler accuracy consists of the Ranging Equipment Doppler instrumental accuracy plus the effects of receiver (MFR) VCO phase noise. The effects of VCO phase noise on cycle count, interval count, frequency, and range rate are:

$$(\sigma_\phi)_{VCO} \quad \frac{(\sigma_\theta)_{VCO}}{2\pi}$$

$$(\sigma_{IC})_{VCO} \quad \sqrt{2}\,(\sigma_\phi)_{VCO} = \frac{\sqrt{2}\,(\sigma_\theta)_{VCO}}{2\pi}$$

$$(\sigma_f)_{VCO} \quad \frac{(\sigma_{IC})_{VCO}}{\Delta t} = \frac{\sqrt{2}\,(\sigma_\theta)_{VCO}}{2\pi\,\Delta t}$$

$$(\sigma_{\dot{R}})_{VCO} \quad \frac{C}{2f_c}(\sigma_f)_{VCO} = \frac{\sqrt{2}\,C\,(\sigma_\theta)_{VCO}}{4\pi\,f_c\,\Delta t}$$

where,

$(\sigma_\phi)_{VCO}$ = RMS cycle count error (cycles)

$(\sigma_\theta)_{VCO}$ = VCO rms phase noise (radians)

$(\sigma_{IC})_{VCO}$ = RMS interval count error (cycles)

$(\sigma_f)_{VCO}$ = RMS frequency error (Hz)

Δt = Sampling interval (seconds)

$(\sigma_{\dot{R}})_{VCO}$ = RMS range rate error (meters/sec)

f_C = Carrier frequency (Hz)

C = Velocity of propagation

If

$(\sigma_\theta)_{VCO}$ = 1 radian

Δt = 0.1 second

f_c = 2250 MHz

c = 3×10^8 meters/sec

then,

$(\sigma_\phi)_{VCO}$ = 0.159 cyc

$(\sigma_{IC})_{VCO}$ = 0.225 cyc

$(\sigma_f)_{VCO}$ = 2.25 Hz

$(\sigma_{\dot{R}})_{VCO}$ = 0.15 meters/sec

A graph of range rate accuracy, which includes the Ranging Equipment instrumental errors, plus the effects of MFR VCO phase noise, is given in Figure 4.8.3-1. The graph is for a sampling interval of 0.1 seconds.

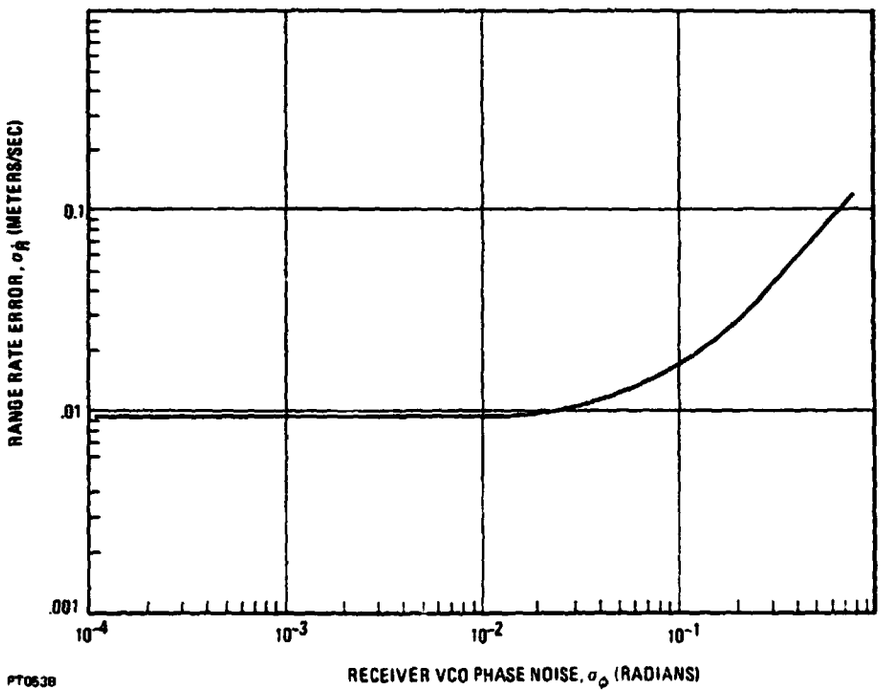


Figure 4.8.3-1. Range Rate Accuracy

5. DESIGN VERIFICATION TESTS

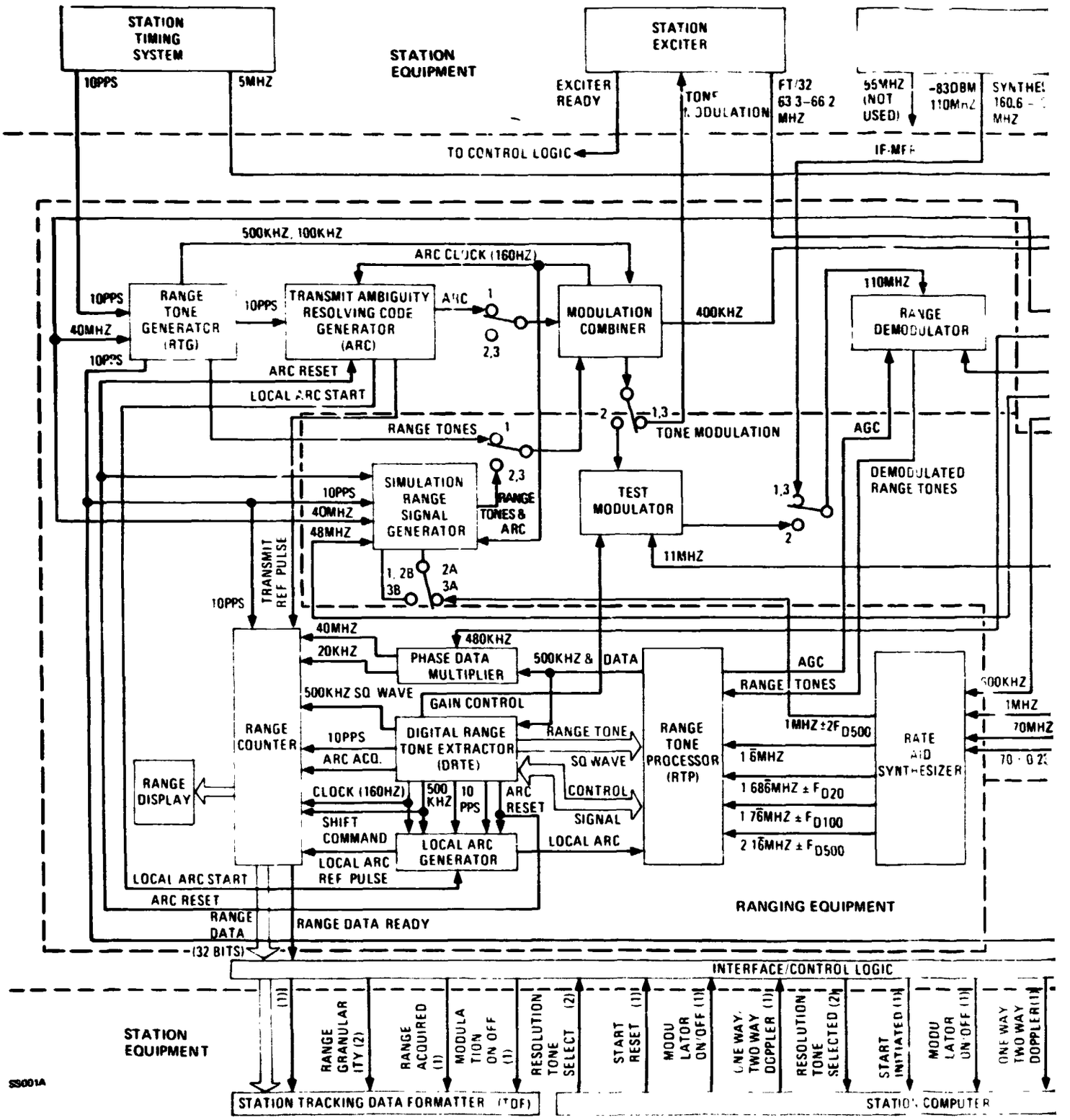
Design verification tests were accomplished on three units; S/N 1 (Engineering Model), S/N 2 (first production unit), and S/N 13 (random selected production unit).

These design verification tests were performed in the Bypass Simulate mode in accordance with the test procedure of Appendix B. The results are presented in Appendix C.

APPENDIX A

Foldout Diagrams

FOLDOUT FRAME 1



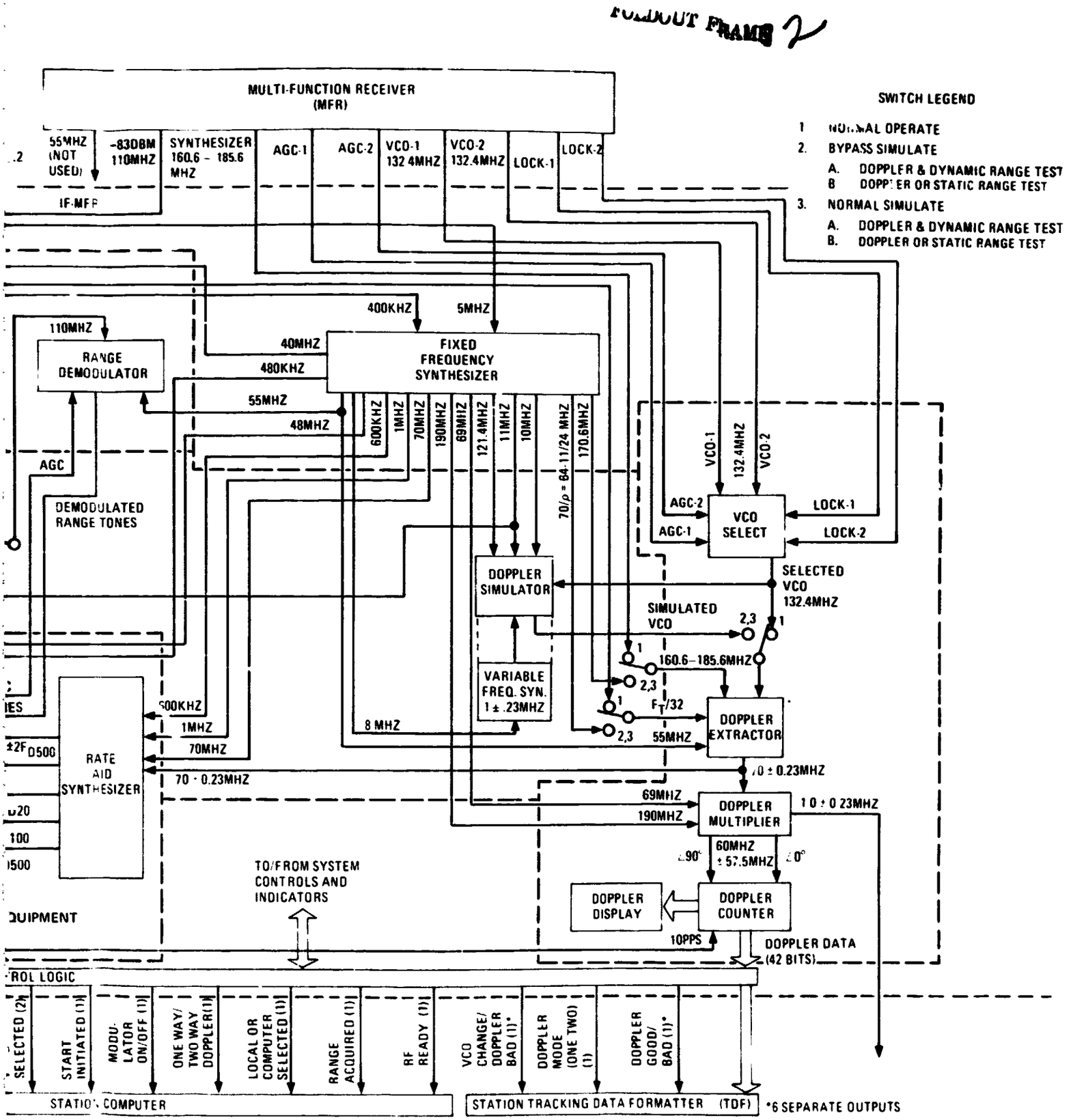
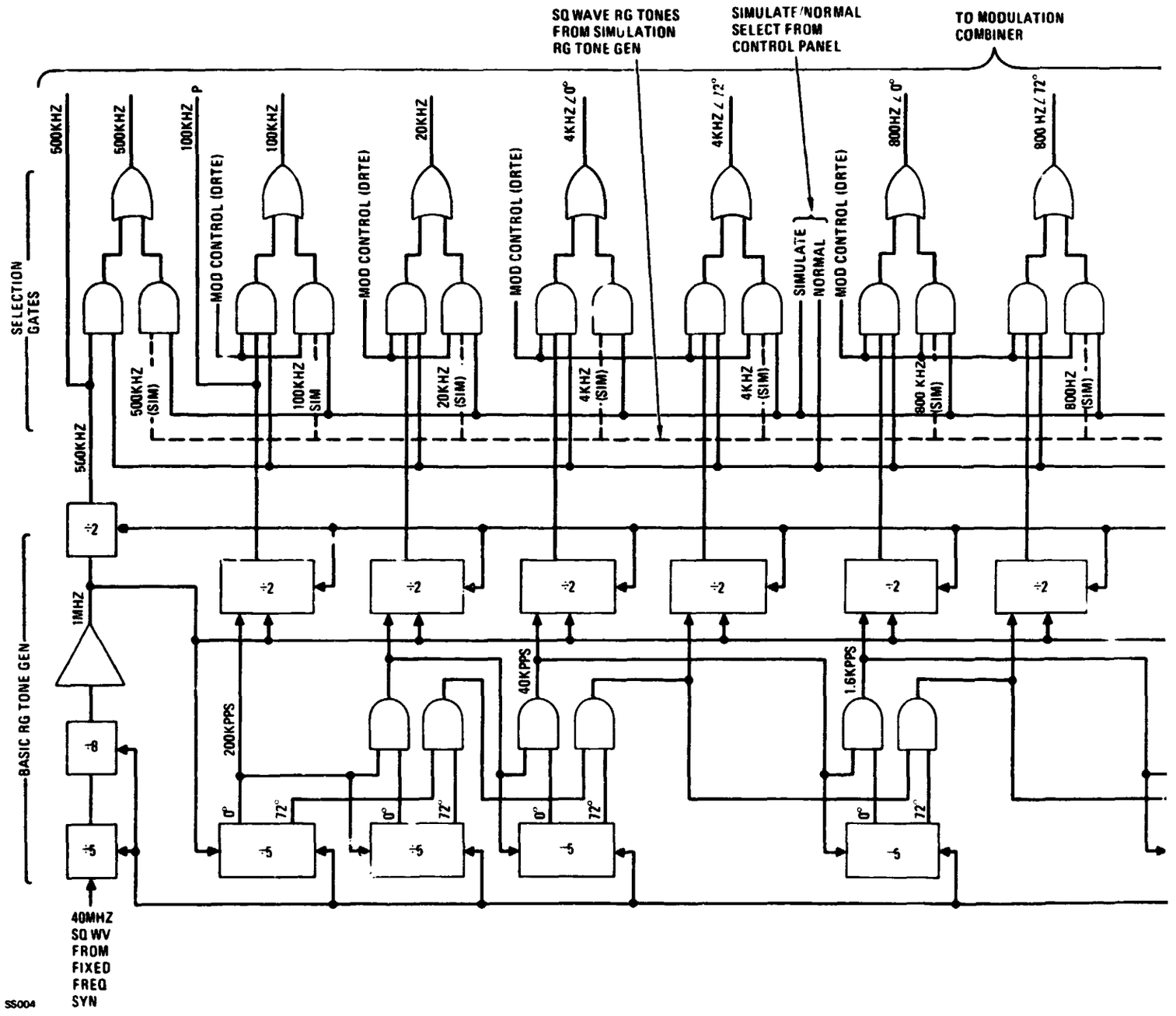


Figure 2.3-1. STDN Ranging Equipment, Functional Block Diagram

FOLDOUT FRAME /



FOLDOUT FRAME 2

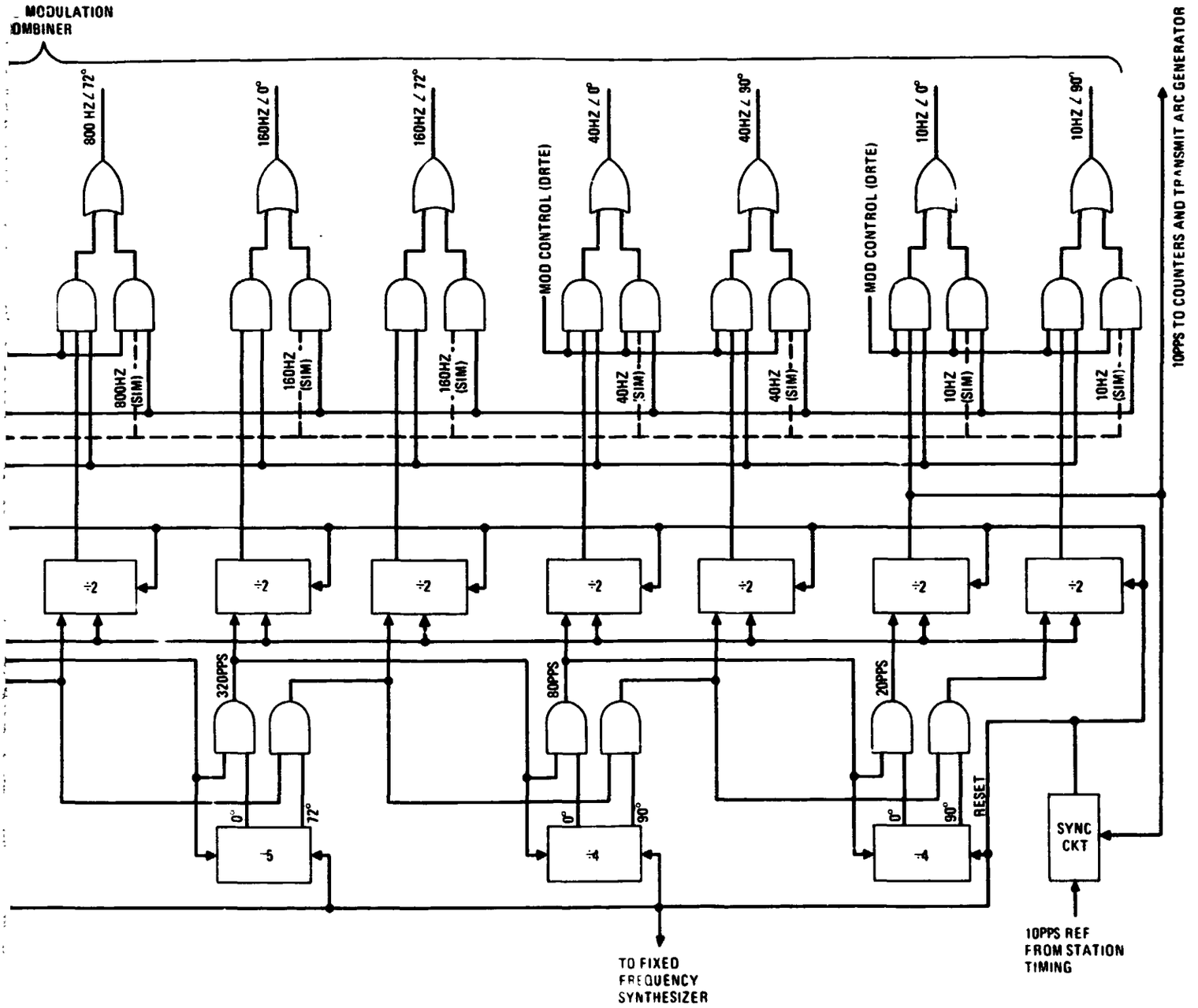
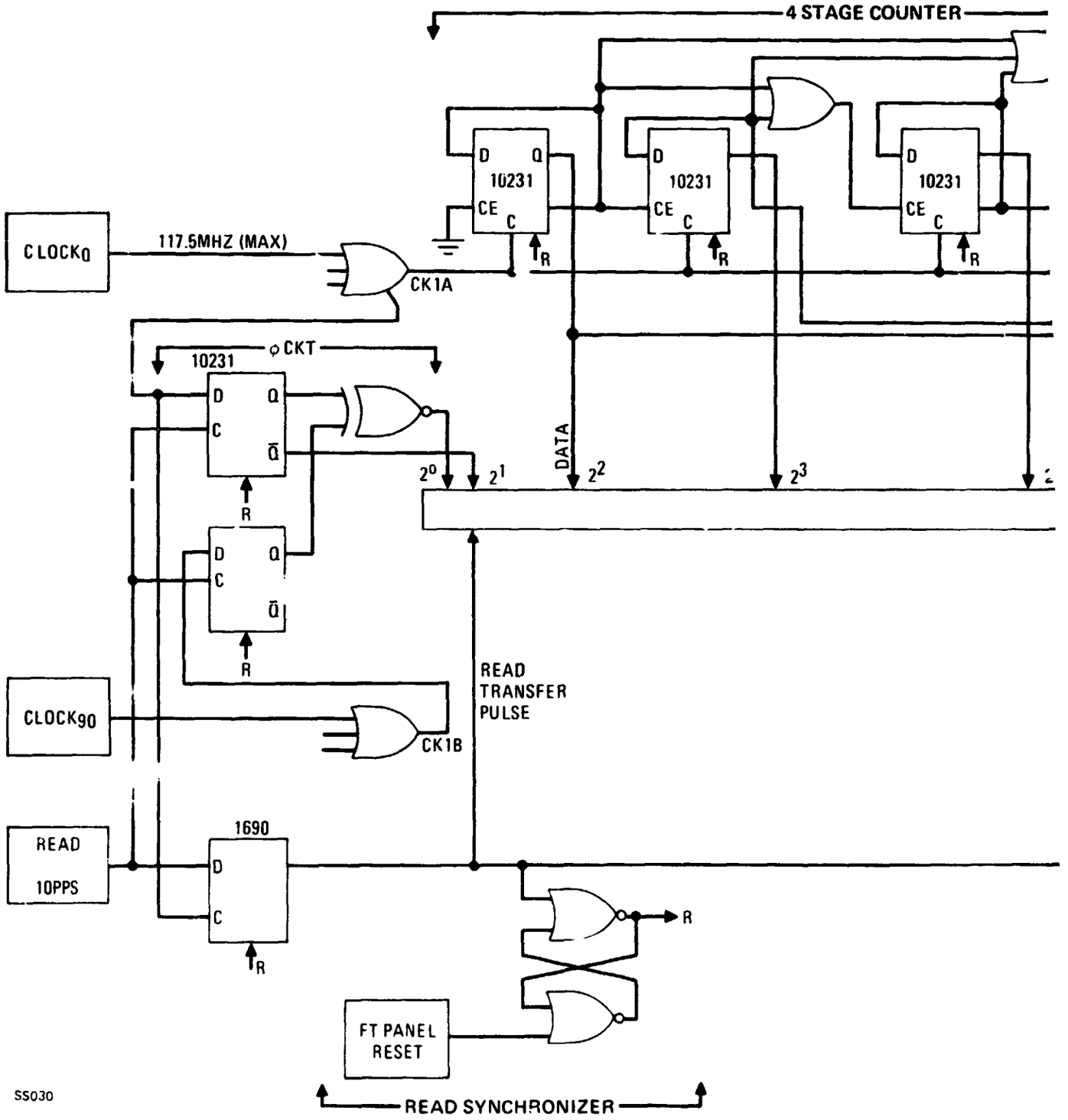
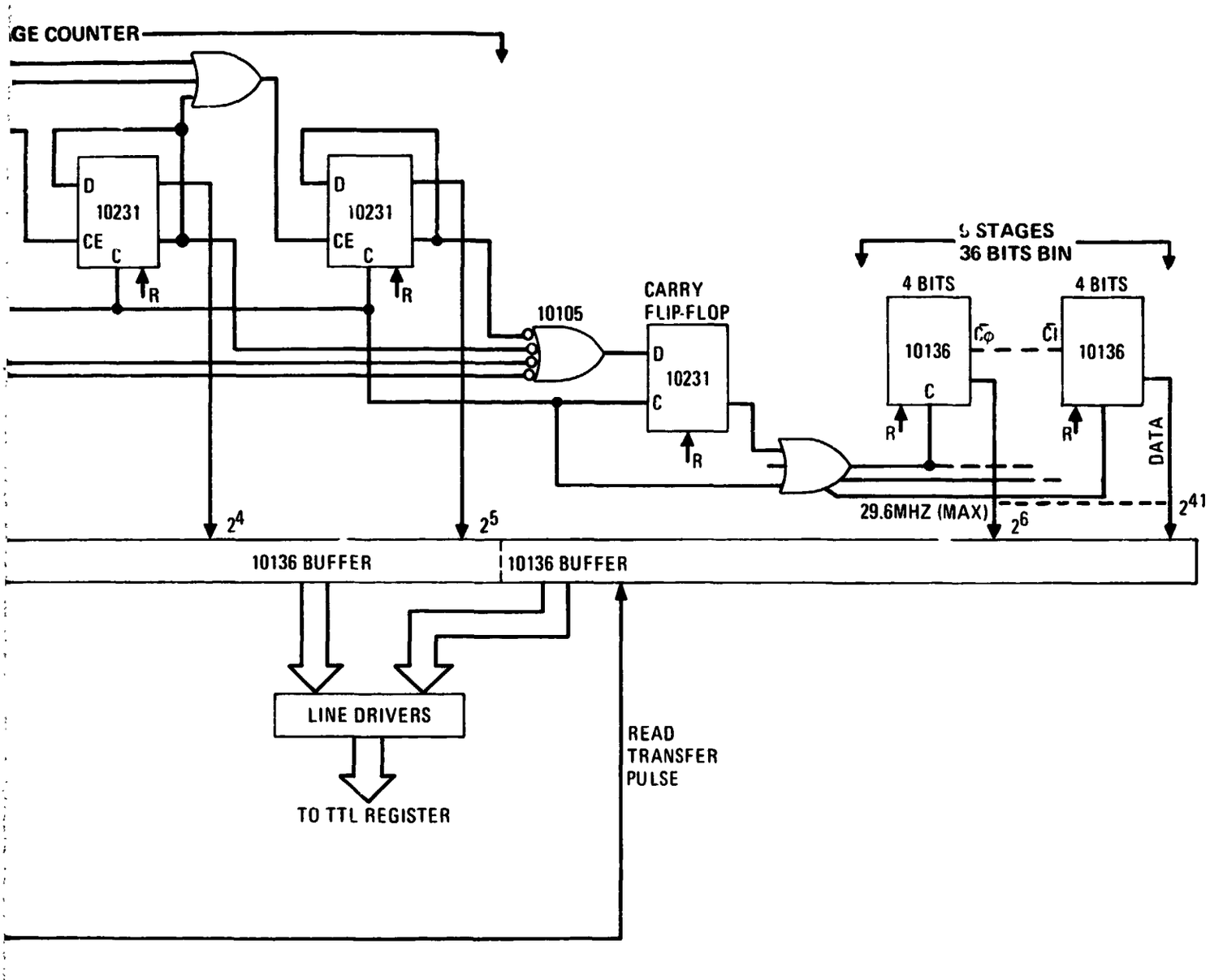


Figure 3.2.1-1. Range Tone Generator, Block Diagram

FOLDOUT FRAME 1



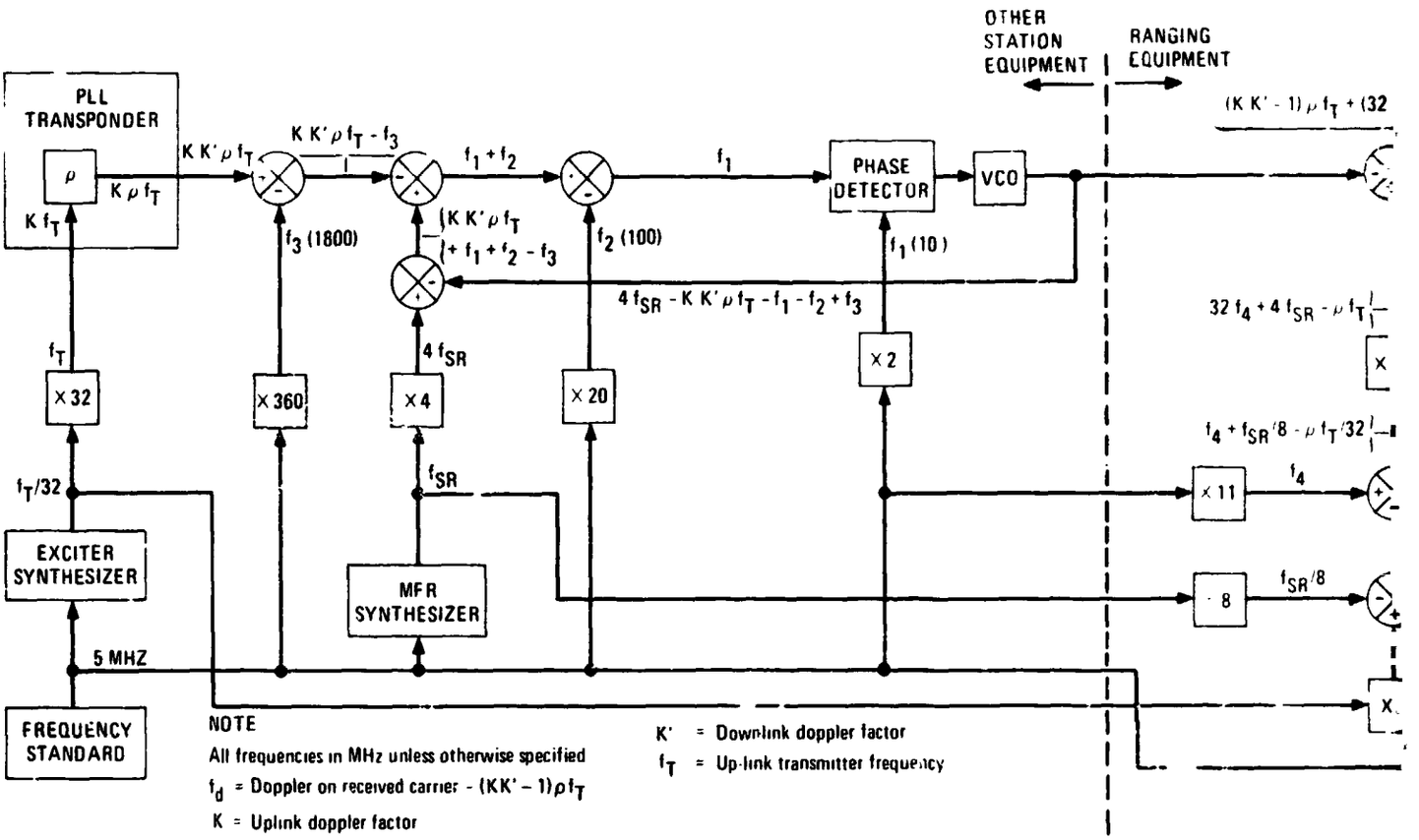
FOLDOUT FRAME 2



(ALL DEVICES ARE MECL)

Figure 3.2.15-2. Doppler Counter, High Speed Logic

FOLDOUT FRAME



SS037

FOLDOUT FRAME 2

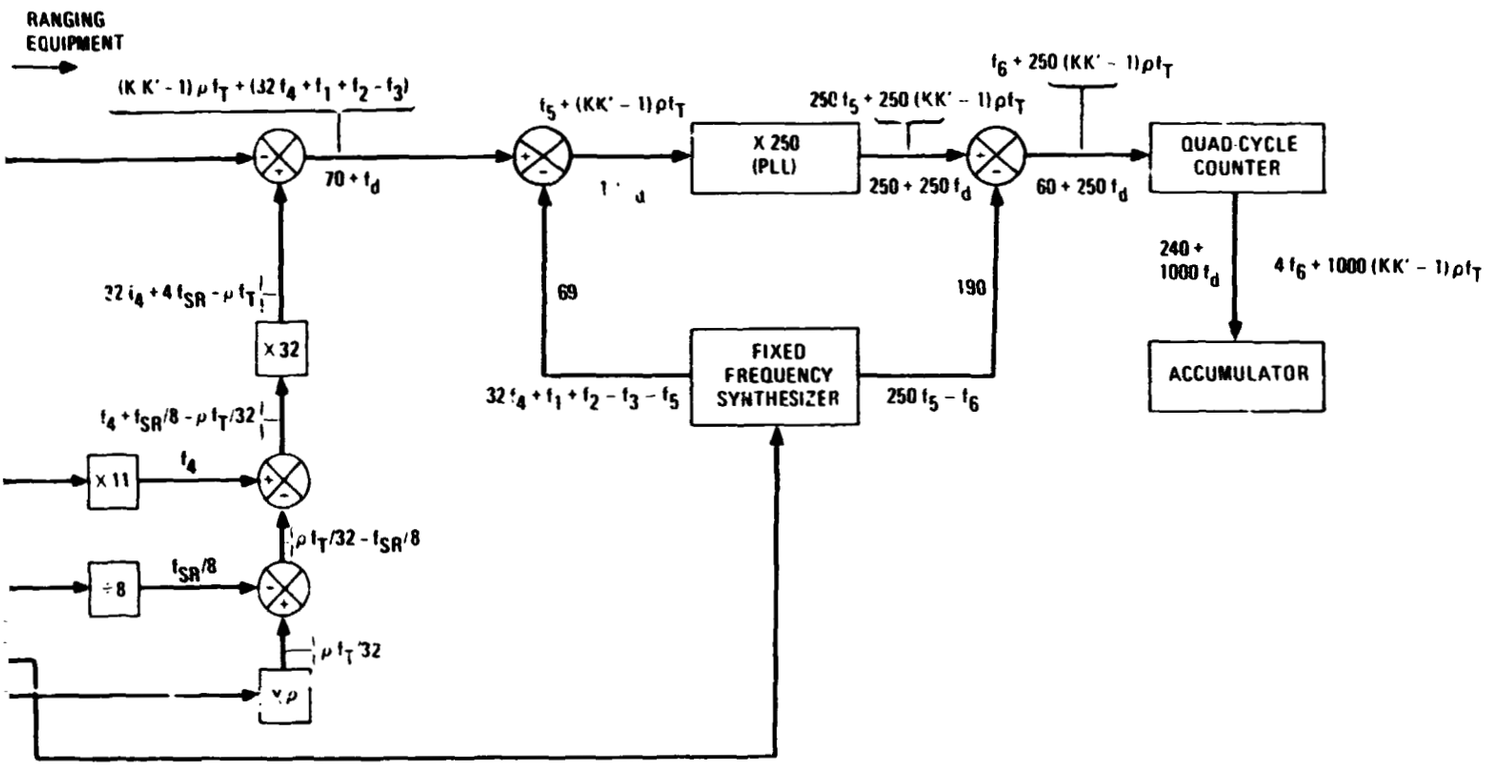
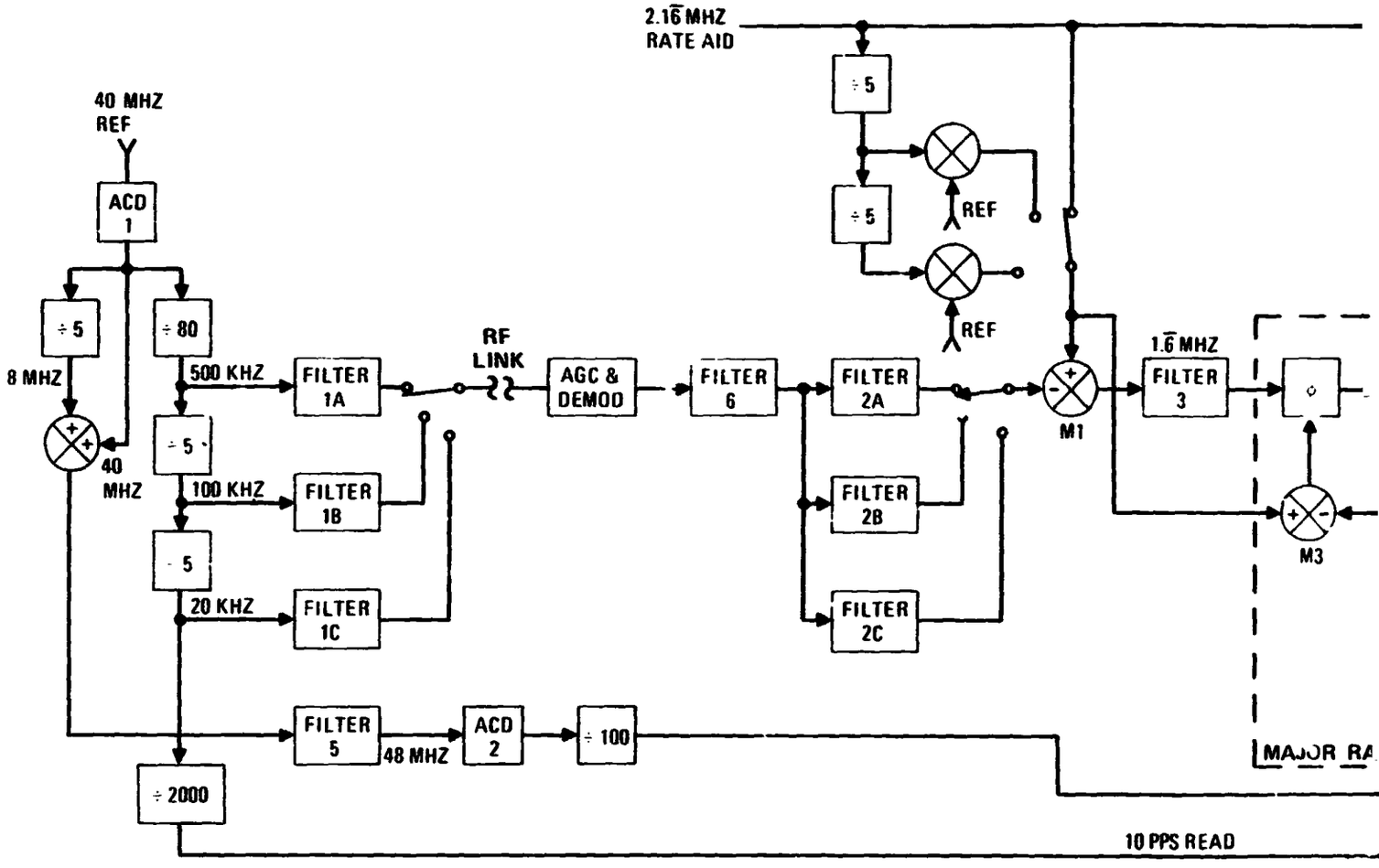


Figure 4.1-1. Doppler Extraction Coherence, Block Diagram

FOLDOUT FRAME 1



SS044

FOLDOUT FRAME 2

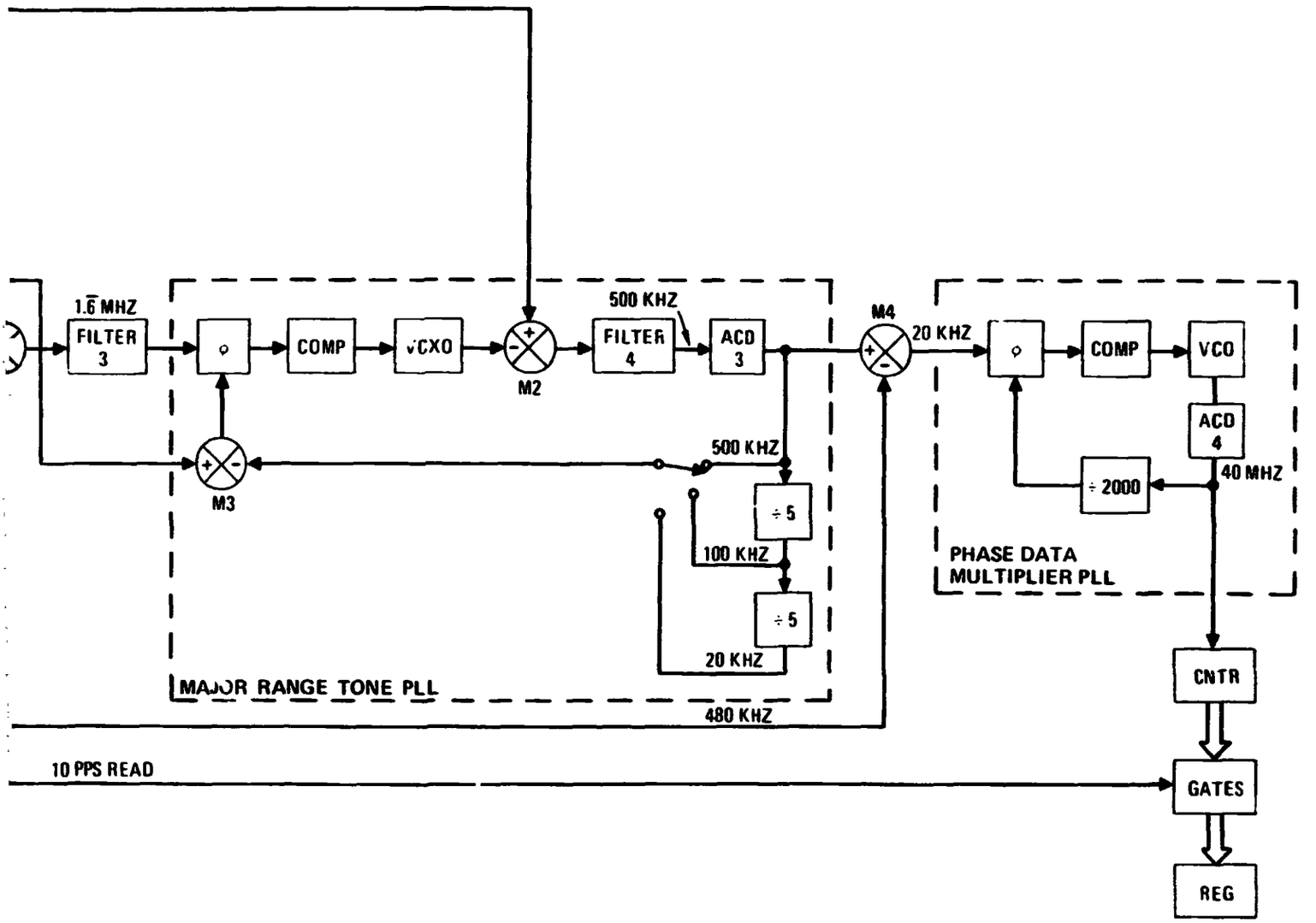


Figure 4.7.2-1. Fine-Range Data Signal Processing and Information Flow

APPENDIX B

STDN RANGING EQUIPMENT
DESIGN VERIFICATION
TEST PROCEDURE

GENERAL DYNAMICS
Electronics Division

REPORT NO. 2106015
MODEL 318
DATE April 22, 1974

2106015

TITLE

STDN RANGING EQUIPMENT DESIGN VERIFICATION TEST PROCEDURE

P/N 2106000

PREPARED BY E. J. Cekander

CHECKED BY H. A. Vasquez

REFERENCE NAS-5-20456

APPROVED BY C. E. Jones

APPROVED BY F. Herold, GSFC

NO. OF PAGES 35

NO. OF DIAGRAMS 7

CODE IDENT NO. 12436

FORM 5-050A

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
A	GENERAL REVISION	/20/74	
B	GENERAL REVISION	9/8/74	
C	REVISED SHEETS 1,5,6,8,10,11,12,13,15,16,17,18	9/24/74	
	REVISED SHEETS 12, 15, 16, 17, 25, 26, 18 REVISED DATA SHEETS 3, 4, 5, 6	10/7/74 (E) 3/26/75	

REV	SIZE	CODE IDENT NO.	DRAWING NO.
D	A	12436	2106015
	SCALE		SHEET 1

5-312-1

1.0 INTRODUCTION

1.1 PURPOSE OF TESTS

These tests are to demonstrate compliance of the equipment with the requirements of Goddard Space Flight Center specification S-813-P-19 as modified by Contract NAS5-20456, Amendment No. 1.

1.2 SIMULATED INTERFACE

Simulated interfaces are used for all signals furnished by, or distributed to, portions of the system not available at the place of test.

All signal interfaces will be provided by the built-in simulator of the system.

Logic level interfaces are provided by a special STDN Ranging Equipment test set General Dynamics par. number 2106960. For this reason, unless otherwise specified, the system will be in the STATIC, BYPASS SIMULATE mode under LOCAL control for the duration of the test.

Where it is necessary to record a large number of data points, the Range and Doppler data will be recorded on a Sangamo Model 3500 recorder and the recorded data will be analyzed by computer at a later time. The test set converts the parallel data to a serial stream suitable for recording.

1.3 RECORDING OF TEST RESULTS

All tests results will be recorded on a separate data sheet, with the exception of the TDF data which is recorded on tape. The reduced tape data will be recorded on the data sheet. A copy of the computer printout, from which the data is reduced, will be provided for NASA and Quality Assurance.

1.4 TEST EQUIPMENT

The following is a list of equipment needed to complete the tests. Equivalent items may be substituted:

ITEM	QTY	DESCRIPTION
1	1	Tape Recorder, Sangamo Model 3500
2	1	IRIG B Time Code Generator
3	1	Oscilloscope Tektronix 475 Oscilloscope
4	1	Computing Counter HP5360A
5	1	Time Interval Unit, HP5379A
6	1	RF Voltmeter, HP413A
7	1	Spectrum Analyzer, HP8551A/851A
8	1	Test Set, General Dynamics/Electronics P/N 2106960
9	3	Attenuator, Kay Model 30-0
10	1	Noise Generator, GD/Electronics P/N 2106988
11	A/R	Tape for Recorder, Scotch 871-1-3600 IRH
12	1	Frequency Synthesizer, HP5105A
13	1	Synthesizer Driver, HP5105B
14	1	Signal Generator, HP606A
15	1	Power Supply +5V, 7 Amps
16	1	Power Supply +5V, 3 Amps
17	1	Power Supply -7.4V, 250 mA
18	1	Ammeter, Weston 901
19	1	Wave Analyzer, HP310A
20	1	HP331A Distortion Analyzer
21	1	Signal Combiner, GD/Electronics P/N 2106987
22	1	Power Meter, HP431C

2.0 MECHANICAL REQUIREMENTS

2.1 CHASSIS SLIDES

Visually inspect all chassis and insure that they are equipped with quick-disconnect type chassis slides NOTE: The fixed frequency synthesizer is not equipped with chassis slides.

2.2 CABLE RETRACTORS

Visually inspect all chassis on slides and insure they are equipped with cable retractors.

2.3 GENERAL ADHERENCE TO SPECIFICATION

2.3.1 SWITCHES

Verify that all critical switches are guarded to prevent the accidental changing of state while not introducing an unusual burden in the normal operation of the switch. A critical switch is one which, if accidentally thrown, would require an extensive calibration of the system or interfere with the operation of the system.

2.3.2 MARKING

Verify that all front and rear chassis marking will be suitable to insure durability in the field.

3.0 FUNCTIONAL REQUIREMENTS

3.1 AC POWER INPUT

Verify that the equipment operates off a two (2) wire, 60 Hertz, 115 Volt AC line.

3.1.1 ELAPSED TIME INDICATOR

Verify the presence of an elapsed time indicator on the power control panel and that the meter increments in tenths of hours.

3.1.2 POWER ON INDICATOR

Verify the presence of an AC power on indicator on the power control panel. Also verify that the indicator illuminates when the master circuit breaker is on and extinguishes when the master circuit breaker is off.

3.2 POWER SUPPLIES

The following tests demonstrate that the power supply meets the requirement of the specification. For the majority of the cases, vendor data will be used to verify the power supply performance.

3.2.1 CURRENT DRAIN

In this test, the actual current on the supply is measured with an ammeter and is compared with the rated current of the supply as shown in the vendor data. The measured

value will be less than the 0.8 rated output value.

Supply	Rated Output	0.8 Rated Output
+15V	6 Amps	4.8 Amps
-15V	5 Amps	4.0 Amps
+5V *	45 Amps	36 Amps
-5.2V	15 Amps	12 Amps
+24V Relay & Lamps	10 Amps	8 Amps
+24V Signal	3 Amps	2.4 Amps

3.2.2 VOLTAGE INPUT

Demonstrates power supplies operate with an input voltage varying between 105V AC to 125V AC. See vendor data.

3.2.3 CURRENT LIMITNG & SHORT CIRCUIT PROTECTED

Demonstrates power supplies provide current limiting and short circuit protection. See vendor data.

3.2.4 ADJUSTABILITY

By visual inspection, verify that adjustment controls for the power supplies are screwdriver type adjustments.

3.2.5 REGULATION

Demonstrates that with worse case line and load regulation will be less than 0.1 percent of full load. See vendor data.

---

* On two lines. Measure each line separately and sum for measured output.

3.2.6 FUSING

By visual inspection, verify that each output is fused separately.

3.3 RANGE TONE GENERATOR

The following tests demonstrate that the Range Tone Generator meets the requirements of the specification. Simulated inputs for the Station Frequency Standard and Station Timing Signals are used.

3.3.1 STATION FREQUENCY STANDARD

The frequency standard for the test is simulated by a HP Model 5105A frequency synthesizer. Verify that the signal J 9 (System) has the following characteristics:

Frequency:	5.0 MHz as set on front panel of the synthesizer.
Output into 50 ohms:	2V peak-to-peak minimum.

3.3.2 STATION TIMING SIGNAL

A 10 PPS station timing signal is generated from the 1 MHz fixed frequency output of the H.P. synthesizer. Using an oscilloscope, verify the signal is as shown in Figure 1. The Station Timing Signal is available on J10 of the system.

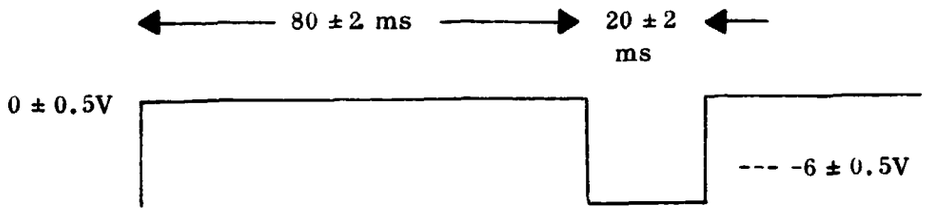


FIGURE 1.

In addition, using the HP5360A computing counter, verify that the pulse rise time is 10 nanoseconds or less. See Figure 2.

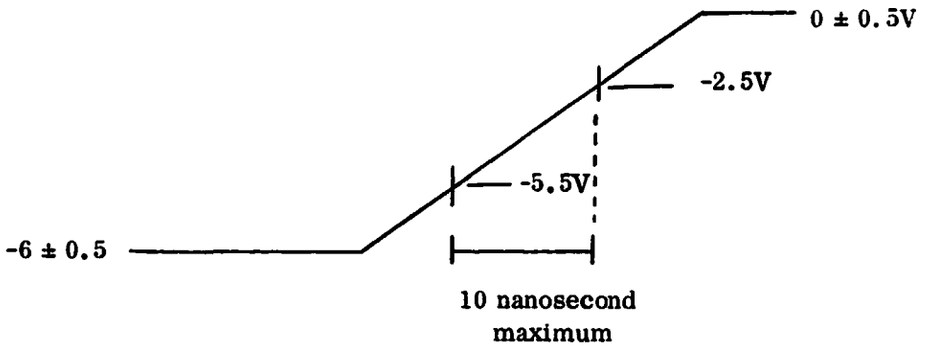


FIGURE 2.

NOTE: This signal is frequency coherent with the 5 MHz station frequency standard.

3.3.2.1 SYNCHRONIZATION OF REFERENCE PULSE TO TIMING SIGNAL

This test demonstrates that the internal 10 Hz reference is stable to the simulated station timing signal to within ± 25 nS. See Figure 3. The reference pulse is monitored at Block 48, IC U11 Pin 4. Record both the stability and average value of the delay.

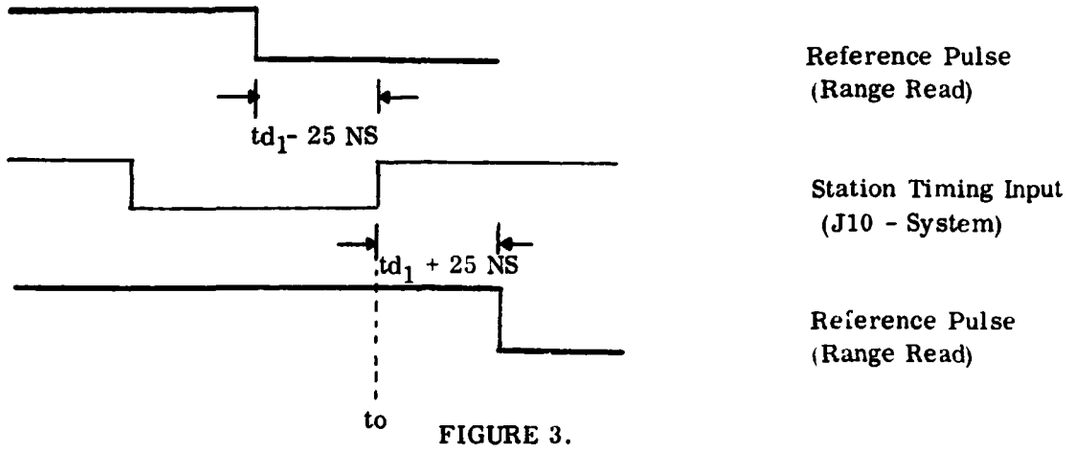


FIGURE 3.

3.3.2.2 LOSS OF SYNCHRONIZATION

This test demonstrates that if the reference pulse and station timing pulse are not synchronized, the SYNC LOSS indicator will illuminate. Loss of synchronization is demonstrated by shifting the Simulated Station timing signal.

To perform the test, the station timing signal is inserted into the t_1 input of the computing counter, and the reference pulse is inserted into the t_2 input of the counter. Vary the 5 MHz output of the frequency synthesizer by a small amount, and the time interval display will vary. When the time difference exceeds the tolerance, the SYNC LOSS light will illuminate. See Figure 4. The time stability should not exceed ± 25 NS.

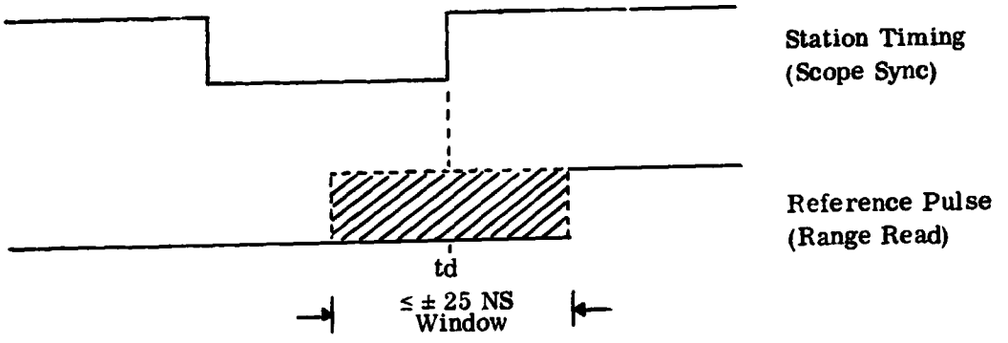


FIGURE 4.

Set the frequency synthesizer output to exactly 5 MHz. Press the SYNC LOSS button and observe that the SYNC LOSS light remains out, verifying that the system is re-synchronized. Disconnect the synthesizer output from J9. For all remaining tests, both the system and system test set will operate from the 5 MHz laboratory standard which is derived from an H.P. 107 AR quartz oscillator.

3.3.3 RANGE TONE OUTPUT

These tests demonstrate that the range tone outputs meet the requirements of the specification.

3.3.3.1 AMPLITUDE

Press the Modulation ON/OFF switch to "ON" and turn on the 20 kHz tone and the 100 kHz tone. Observe the output from the interface panel J17 on the oscilloscope terminated with 50Ω. Vary the Modulation Level control pot and check for level control from 4 Vpp to ≈0 Vpp. System is in the NORMAL of operation for this test and the following two tests.

3.3.3.2 HARMONIC CONTENT

With only the 20 kHz tone on, adjust the Modulation control pot for 1 Vpp. Switch the output from the oscilloscope to a HP331A distortion analyzer. Distortion will be less than 1%. Repeat for the 100 kHz and 500 kHz major tones. Repeat all readings with the Modulation Control pot set at 2 Vpp.

3.3.3.3 RESPONSE TO START COMMAND

This test demonstrates that the Range Tone Generator outputs signals upon receipt of a START command.

A. Select 500 kHz as a major tone; all minor tones are off.

B. Set START/RESET control to RESET.

C. Monitor the Range Tone Output (J17) with a scope and observe that no signal is present.

D. Depress START/RESET control and observe on the scope that a 500 kHz signal is now present.

3.3.3.4 AUTOMATIC SEQUENTIAL OPERATION OF MINOR TONES

This test demonstrates that once the major tone is selected, the minor tone, including ARC, will start at the next lowest frequency and automaticaliy sequence down until the ARC is locked. The test will demonstrate starting from each of the three (3) major tones. Note ARC USE/BYPASS control is in the "USE" position and the system is in the SIM mode of operation.

TABLE I.

MAJOR TONE SELECTED	MINOR TONE SEQUENCER
500 kHz	100 kHz ——→ ARC
100 kHz	20 kHz ——→ ARC
20 kHz	4 kHz ——→ ARC

Front panel lights are monitored to verify the operational sequence. Verify that the major tone selected remains on during the sequencing of the minor tones. Sequencing is complete when the RANGE ACQ COMP indicator illuminates.

3.3.3.5 MANUAL OPERATION OF MINOR TONES

This demonstrates the operation of the AUTO/MAN switch and verifies that in the MAN position, the minor tones do not automatically sequentially advance once the start button is depressed. Front panel lights are monitored to verify system performance.

A. Place the START/RESET control to the RESET position.

B. Place the AUTO/MAN control to the MAN position.

C. Select 500 kHz as the only tone on.

D. Place the START/RESET control to the START position.

E. Verify that the LOCK indication on the 500 kHz control illuminates and that no other tone illuminates.

3.3.3.6 ELIMINATION OF ARC IN MINOR TONE AUTOMATIC SEQUENTIAL OPERATION

This test demonstrates the ability of the system to delete the ARC as a minor tone during an otherwise normal automatic sequential system operation.

A. Place the START/RESET control to the RESET position.

B. Place the AUTO/MAN control to the AUTO position.

C. Place the ARC USE/BYPASS control to the BYPASS position.

D. Select 20 kHz as the major range tone.

E. Place the START/RESET control to the START positi

F. Observe that the 20 kHz LOCK indicator illuminates and that the 4 kHz, 800 Hz, 10 Hz LOCK indicator sequentially illuminate. Sequencing is completed when the RANGE ACQ COMP indicator illuminates.

3.3.3.7 MANUAL OPERATION OF MINOR TONES

With the AUTO/MAN Switch in the MAN position, verify that each of the minor tones can be selected and that after all of the minor tones have been acquired that the RANGE ACQ COMP indicator will illuminate when pressed.

3.4 RANGE DEMODULATOR

3.4.1 ANALYZER CALIBRATION

Perform a signal substitution procedure utilizing an HP-608 signal generator to calibrate a spectrum analyzer at a frequency of 110 MHz and a level of -53 dBm.

3.4.2 INDEX SETTING AT 1.5 RADIANS MODULATION INDEX

Disconnect the coax cable from the 30 dB attenuator, AT 1, within the H.F. Processor. Connect the cable to the spectrum analyzer. Operate in the Simulate/Bypass mode and modulate with a 500 kHz tone. Adjust R58 on A9 for each first order sideband at 0.75 dB above the 110 MHz carrier. Adjust R58 on A9 in the H.F. Processor for a 110 MHz carrier level at -53 dBm. NOTE: The front panel control may also be used to adjust the modulation index.

3.4.3 ALC CHECK AT 1.5 RADIANS

Reconnect the coax cable to attenuator, AT 1. Allow the tone tracking loop to lock (in the L.F. Processor). Measure and record the AC voltage at J5 of the L.F. Processor with a wave analyzer. Set the wave analyzer bandwidth to 1000 Hz.

3.4.4 INDEX SETTING AT 0.2 RADIANS MODULATION INDEX

Repeat 3.4.2 only adjust for each first order sideband to be 20 dB below the 110 MHz carrier and then adjust the 110 MHz carrier for a level of -53 dBm.

3.4.5 ALC CHECK AT 0.2 RADIANS

Reconnect the coax cable to attenuator, AT 1. Allow the tone tracking loop to lock. Measure and record the AC voltage at J5 in the L.F. Processor with the wave analyzer. Set the wave analyzer bandwidth to 1000 Hz.

3.5 RANGE DATA

This series of tests demonstrate that the Range Extractor meets all the requirements of the specification. The system is in the BYPASS SIMULATE mode for the duration of the test.

3.5.1 TEST MODULATOR CALIBRATION

Calibrate the Test Modulator as in paragraph 3.4, only adjust the front panel Modulation Level Control pot for each first order sideband 16.4 dB below the 110 MHz carrier (.3 radian modulation index). Adjust the 110 MHz carrier to a level of -53 dBm. Turn on a second tone 100 kHz and adjust R58 of A 9 within the H.F. Processor to bring the 110 MHz carrier back to -53 dBm. Reconnect the coax cable to attenuator AT 1 within the H.F. Processor.

3.5.2 RANGE SIMULATION CAPABILITY

3.5.2.1

Set the Static Range Select to 0 nS. Start the system to obtain range data while operating in the BYPASS SIMULATE Mode utilizing a 500 kHz major range tone. In small increments, adjust the Range Calibration to obtain 0 nS range display. Observe that the smallest increment on the display is 1 nS.

NOTE: The INSERT DATA CONTROL must be depressed to enter data into the system.

3.5.2.2 ADJUST RANGE SELECT FOR 3,333,330 nS

Set the Static Range Select to 3,333,330 and press INSERT DATA. Restart the system and after acquisition, observe a Range display of approximately 3,333,330 nS.

3.5.2.3 ADJUST RANGE SELECT FOR 1,698,333 nS

Set the Static Range Select to 1,698,333 and press INSERT DATA. Restart the system and after acquisition, observe a range display of approximately 1,698,333 nS.

3.5.3 STRONG SIGNAL DATA

3.5.3.1 500 kHz RESOLUTION

Connect the tape recorder equipment to the Data Out Jack, J26, on the test set. Start the system to obtain range data utilizing a 500 kHz major range tone while operating in the BYPASS SIMULATE mode. Select an initial range of 1,698,335 nS and record data for 30 seconds. After the data has been analyzed by computer, calculate and record the RSS system error using the following equation:

$$\text{error} = \left[(\text{Ideal Value} - \text{Average Value})^2 + (\text{Std. Dev.})^2\right]^{1/2}$$

3.5.3.2 100 kHz RESOLUTION

Repeat 3.5.3.1 only use a 100 kHz [illegible]ange tone. Change zero set calibration as necessary.

3.5.3.3 20 kHz RESOLUTION

Repeat 3.5.3.1 only use a 20 kHz major range tone. Change zero set calibration as necessary.

3.5.4 NOISE DATA

3.5.4.1 CALIBRATION OF THE NOISE GENERATOR

Set up the test modulator for an index of 0.2 radians. On the 21[illegible]6520 board in the L.F. Processor, remove relay K1 and place a jumper between pins [illegible]4. Set up test as shown in Figure 5. With maximum attenuation on the noise and using a [illegible] Hz BW on the wave analyzer at 500 kHz, read the voltage on the analyzer and record the value. Adjust R72 of A7 within the L.F. Processor for a reading of 0.56 mV. Place the system in the NORM SIM mode of operation.

3.5.4.1.1 Change the wave analyzer bandwidth to 3000 Hz and tune to 350 kHz then adjust the attenuator for a voltage reading of 97 mV (+50 dB - Hz) and record the attenuator setting.

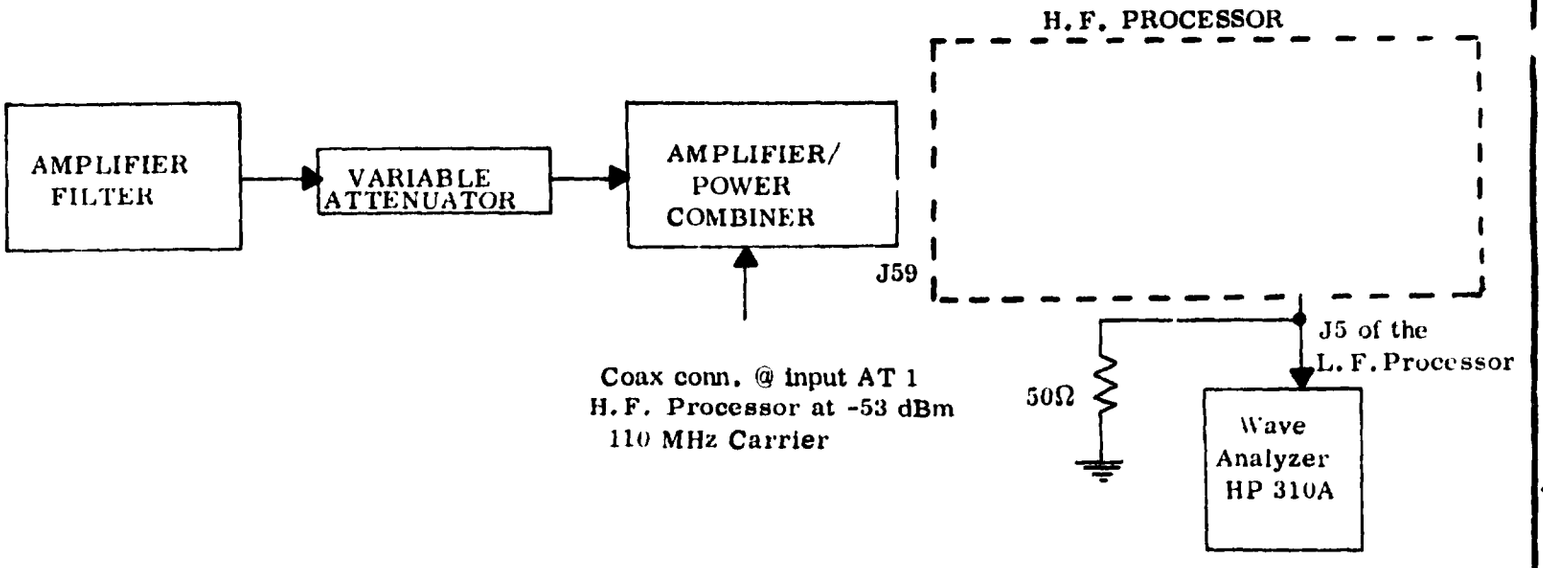


FIGURE 5. NOISE GENERATION TEST SETUP

3.5.4.1.2 Repeat 3.5.4.1.1 for readings of 0.17 mV (+45 dB - Hz), 0.31 mV (+40 dB - Hz), 0.55 mV (+35 dB - Hz), 0.97 mV (+30 dB - Hz), 1.73 mV (+25 dB - Hz), 3.08 mV (+20 dB - Hz), 5.47 mV (+15 dB - Hz), 7.72 mV (+12 dB - Hz) and 9.73 mV (+10 dB - Hz).

Record all attenuator settings. Readjust R 72 of A7 within the Low Frequency Processor for the initial reading in paragraph 3.5.4.1.

3.5.4.2 500 kHz RESOLUTION

3.5.4.2.1 +50 dB - Hz

Adjust the attenuator corresponding to +50 dB - Hz and reconnect the coax cable to the H.F. Processor. Insure that the tone loop locks and the range readout is approximately 1,698,333 nS. Record 30 seconds of range data.

3.5.4.2.2 +45 dB - Hz

Adjust the attenuator corresponding to +45 dB - Hz and record 30 seconds of range data.

3.5.4.2.3 +40 dB - Hz

Adjust the attenuator corresponding to +40 dB - Hz and record 30 seconds of range data.

3.5.4.2.4 +35 dB - Hz

Adjust the attenuator corresponding to +35 dB- Hz and record 30 seconds of range data.

3.5.4.2.5 +30 dB - Hz

Adjust the attenuator corresponding to +30 dB - Hz and record 30 seconds of range data.

3.5.4.2.6 +25 dB - Hz

Adjust the attenuator corresponding to +25 dB - Hz and record 30 seconds of range data.

3.5.4.2.7 -20 dB - Hz

Adjust the attenuator corresponding to -20 dB - Hz and record 30 seconds of range data.

3.5.4.2.8 +15 dB - Hz

Adjust the attenuator corresponding to +15 dB - Hz and record 30 seconds of range data.

3.5.4.2.9 +10 dB - Hz

Adjust the attenuator corresponding to +10 dB - Hz and record 30 seconds of range data. After the preceding range data has been analyzed by computer, calculate and record the error on the data sheet.

3.5.4.3 100 kHz RESOLUTION

Repeat paragraph 3.5. .2.

3.5.4.4 20 kHz RESOLUTION

Repeat paragraph 3.5.4.2.

3.5.5 ACQUISITION TIME

Using a time interval counter measure the acquisition time for a medium and a strong signal; the time for a weak signal is sufficiently long that a stopwatch must be used. The T1 input to the counter is the system start command at block 10 IC 8 pin 1 of the Digital Processor. The T2 input to the counter is the range acquisition complete signal at block 16 IC 4 pin 11 of the Digital Processor. Both signals are positive edge activated.
NOTE: The ARC USE/BYPASS switch will be in the USE position for all of the tests.

3.5.5.1 MEDIUM SIGNAL

Set the STATIC RANGE SELECT to 900,000. Adjust the attenuator corresponding to -40 dB - Hz. Operate in the BYPASS SIMULATE mode utilizing a 500 kHz major range tone. Record the time as read on the counter.

3.5.5.2 WEAK SIGNAL

Set the STATIC RANGE SELECT to 2,900,000. Adjust the attenuator corresponding to +12 dB - Hz and check to see that the system acquires, by monitoring the RANGE ACQ COMP indicator. There is no limit on the acquisition time for a weak signal. The acquisition process will take approximately 14 minutes.

3.5.5.3 STRONG SIGNAL

Reconnect the coax cable to attenuator AT1 within the H.F. Processor. Set the STATIC RANGE SELECT to 90,000. Change the modulation index to 0.5. Start the system and record the time it takes the system to acquire.

3.5.6 DYNAMIC ERROR

Select the dynamic range simulate mode with -225 kHz of doppler and record 30 seconds of data. The RAS thumbwheel should be set to 22500 for this test. Return the system to the STATIC range mode after this test. Calculate the error using the same equation used to determine the range error. The ideal value is 10,000 NS.

3.5.7 OUTPUTTING OF DATA

The signal that signifies that both the range and doppler information are ready for outputting to the TDF is called "DATA AVAILABLE". Monitor the "DATA AVAILABLE" signal from J27 on the test and synchronizing off the station timing signal, J10 (system), verify the waveform is as shown in Figure 6.

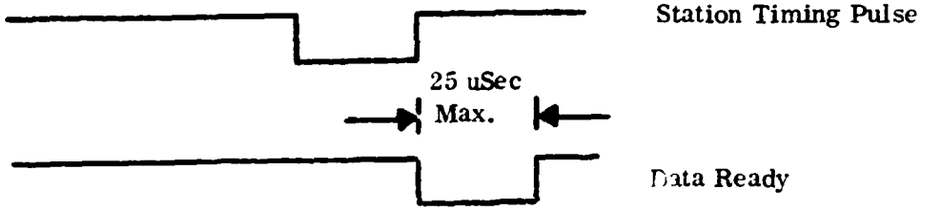


FIGURE 6.

3.5.8 AMBIGUITY INTERVAL

Using the ARC Generator, the code is 1023 bits clocked at a 160 Hz rate, giving a repetition rate of 6.39375 seconds. A code length of 6.39375 seconds provides an ambiguity resolving capability of 958,000 kM which far exceeds the 500,000 kM specification limit.

3.6 DOPPLER EXTRACTOR

This series of tests demonstrates that the system meets all the requirements of obtaining doppler data. The system will be in the BYPASS SIMULATE mode for the duration of the tests. Instantaneous range accuracy will be shown using the front panel readout of the system. Data at the TDF output will be placed on tape and analyzed later for accuracy requirements.

3.6.1 DOPPLER ACCURACY & RESOLUTION

Set in frequencies of 0, ± 115.775 kHz and ± 218.775 kHz. Record the output at each frequency for approximately 30 seconds. The front panel readout will be used to give the preliminary information that the system is functioning properly, the tape will be analyzed later to insure all of the requirements have been met. The same equation used to calculate range error will be used to calculate Doppler error.

3.6.2 CONTINUOUS COUNT CAPABILITY OF DOPPLER COUNTER

The maximum frequency into the Doppler counter is 117.5 MHz. If the counter were allowed to count for 10 minutes, the count would be:

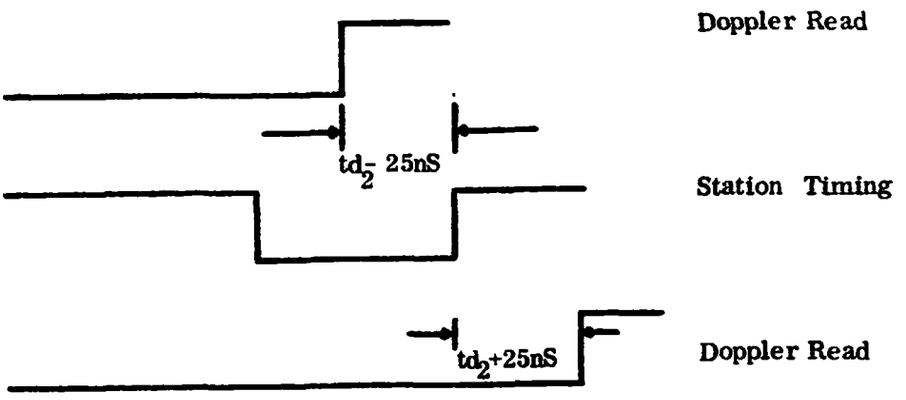
$$117.5 \times 10^6 \frac{\text{pulses}}{\text{sec}} \times 60 \frac{\text{seconds}}{\text{min.}} \times 10 \text{ minutes} = 7050 \times 10^7 \text{ pulses}$$

The TDF interface has 40 bits of binary information where $2^{39} = 54,975 \times 10^7$. Therefore, the counter could count for a maximum of 78 minutes which far exceeds the 10 minute minimum specification.

3.6.3 TIME TAGGING OF DATA

This test demonstrates that the doppler read pulse is stable to within ± 25 nS of the station timing signal. See Figure 7. The HP Computing Counter is used to determine the time interval between the two signals. Measure and record both the stability of the signal and the average value of the delay. NOTE: The DOPPLER SELECT switch must be set to -230 kHz.

FIGURE 7.



The Doppler Read pulse is 10 Hz squarewave located at Biock 23 IC U5 pin 5.

3.6.4 DIFFERENTIAL DELAY BETWEEN RANGE & DOPPLER READ SIGNALS

To obtain the differential delay between the Range and Doppler read signals perform the following calculation:

$$td_2 - td_1 = td$$

Where td_1 is the value recorded in step 3.3.2.1, and td_2 is the value recorded in step 3.6.3. Record the value for td on the data sheet.

3.6.5 DOPPLER RESET

This test demonstrates that depressing the DOPPLER RESET control sets the doppler counter to zero. Since the doppler is continuously counting and the reset is asynchronous, to observe the output at an exactly zero reading would be a matter of chance. Therefore, a sample of data will be taken after the system has been operating and then the reset control will be activated and the new count will be lower than the first count. A third reading will be taken which is higher than the second count to demonstrate that the counter is indeed advancing. The system will be in the SIM BYPASS mode and under MANUAL control for this test.

A. Set the DOPPLER SELECT frequency for 100 kHz.
B. Press the INSERT DATA control.

C. Press the DOP RESET control and allow the system to run for approximately two minutes.

D. Place the DOPPLER DSPL A/B switch on the test set to the DISPLAY A position.

E. Depress the DOPPLER READ control on the test set and record the doppler readout on the test set as N1. **

F. Depress the DOPPLER RESET control on the Digital Processor front panel, then quickly depress the DOPPLER READ control on the test set.

G. Record the doppler readout on the test set as N2. **

H. Place the DOPPLER DSPL A/B switch on the test set to the DISPLAY B position.

I. Record the doppler readout on the test set as N3.

Verify from the data sheet that N1 is much larger than N2 and that N3 is larger than N2. The N2 sample is the closest sample to the reset command and the N3 sample is the readout immediately proceeding the N2 sample.

3.7 EQUIPMENT INTERFACES

This section of the procedure verifies that the system fulfills all of the interface requirements specified in the specification. The system will be in the NORMAL mode for the duration of the test.

3.7.1 EXCITER INTERFACE

The following tests demonstrate that the system fulfills all of the exciter interface requirements. The modulation input interface has previously been tested in Section 3.3.

3.7.1.1 EXCITER READY STATUS

Place the EXCITER RDY switch on the test set to the "ON" position. Observe that the "RF READY" indicator on the Digital Processor is illuminated. Place the switch to the "OFF" position and observe that the light is extinguished.

** Data must be complemental.

3.7.1.2 EXCITER REFERENCE OUTPUT

Place the system in the BYPASS SIMULATE mode. Measure and record the voltage at A2 A15P3-2 (2106210 board of the High Frequency Processor).

Place the system in the NORMAL mode. Insert a 64.43 MHz signal having a level of -2 dBm into 50 ohms at J11 (System). Measure and record the voltage at A2 A15P3-2. The voltage will be within ± 2 dB of the level measured with the system in the BYPASS SIMULATE mode.

NOTE: Leave the signal generator connected to J11 until step 3.7.2 is completed.

3.7.2 MFR INTERFACE

3.7.2.1 VCXO INDICATOR, AGC, PHASE LOCK INTERFACE

The following test verifies the VCXO, AGC and Phase Lock outputs of the MFR. Verify that the results of the test are as shown in Table II.

TABLE II

SYSTEM TEST SET SWITCHES				MFR VCXO		
AGC 1	AGC 2	MFR LOCK 1	MFR LOCK 2	Man/Auto	VCXO 1	VCXO 2
--- **	---	---	---	MAN	ON	OFF
---	---	---	---	MAN	OFF	ON
⚠1 Max	Min	ON	ON	AUTO	ON	OFF
⚠1 Min	Max	ON	ON	AUTO	OFF	ON
Max	Max	ON	OFF	AUTO	ON	OFF
Max	Max	OFF	ON	AUTO	OFF	ON

⚠1 The system must be reset and returned to start after changing the AGC level.

** " --- " Indicates a "don't care" condition.

3.7.2.2 MFR IF OUTPUT

To verify proper connection between the non-simulated IF output and the input to the Range Demodulator, place the system in the NORMAL mode and insert a signal at 110 MHz with a level of 0 dB into 50 ohms at J13 (System). Measure the level at the input to the Range Demodulator and insure that the insertion loss is less than 3 dB. The input to the Range Demodulator is A2 J59 (J59 in the H.F. Processor).

3.7.2.3 VCXO SIGNAL INPUT

Place the system in the NORMAL mode and insert a signal at 132.4 MHz and +2 dBm into 50 ohms into the VCXO 1 input J14 (System). Place the MFR VCXO control on High Frequency Processor to MAN & VCXO 1. Measure the voltage at A2 A20P3-4 (2106320 board in the High Frequency Processor). The voltage will be 0 dBm minimum.

Check the operation for the VCXO 2 signal by placing the 132.4 MHz signal into J15 (System) and placing the VCXO 1/VCXO 2 switch to VCXO 2. Measure the voltage at A2 A20P3-4. The voltage will be 0 dBm minimum.

NOTE: The VCXO indicators were checked in Section 3.7.2.1.

3.7.2.4 MFR SYNTHESIZER INPUT

With the system in the BYPASS SIMULATE mode, measure and record the voltage at A2 A12P3-3 (2106230 board of the High Frequency Processor).

Place the system in the NORMAL mode and insert a signal into J16 (System) at 170.6 MHz with a level of +2 dBm into 50 ohms. Measure and record the voltage at A2 A12P3-3. The voltage will be within ± 2 dB of the level measured with the system in the BYPASS SIMULATE mode.

3.7.3 TRACKING DATA FORMATTER

These tests demonstrate that the system meets the interface requirements to the Tracking Data Formatter. The test simulator is used extensively during this test. The system shall be in the BYPASS SIMULATE, LOCAL CONTROL mode of operation during this test.

NOTE: For this test, only indicators in the TDF MONITOR section of the test set will be observed.

3.7.3.1 RANGE DATA

Data to demonstrate long term range accuracy is recorded and analyzed with a computer. For a visual check of the TDF output, the range can be readout on the test set range readout and compared to the front panel readout of the system.

3.7.3.2 DOPPLER DATA

Data to demonstrate long term doppler accuracy is recorded and analyzed with a computer. For a visual check of the TDF output, the doppler frequency can be read out on the test set doppler readout and compared to the front panel readout of the system.

3.7.3.3 RANGE GRANULARITY

Depending on the major tone selected, the following indicator on the test set shall illuminate. See Table III.

TABLE III.

MAJOR TONE SELECTED	TEST SET INDICATOR ON
500 kHz	500
100 kHz	100
20 kHz	20

3.7.3.4 RANGE ACQUIRED

When the range is acquired, the RANGE ACQ indicator on the test set will illuminate. The "RANGE ACQ COMPL" indicator on the Digital Processor will also illuminate.

3.7.3.5 DOPPLER GOOD/BAD

When doppler data is good, the DOPPLER GOOD indicator on the test set will illuminate. When the data is bad, the indicator will extinguish. The indicator can be forced to either condition by the LOCK 1, LOCK 2 switches on the test set. These switches simulate the MFR LOCK signal. When LOCK 1 and LOCK 2 are OFF, the DOPPLER BAD indicator will illuminate When LOCK 1 and LOCK 2 are ON, the DOPPLER GOOD indicator will illuminate.

3.7.3.6 DOPPLER ONE WAY/TWO WAY

When the "one-way/two way" switch on the Digital Processor front panel is in the "one-way" position, the 1-WAY indicator on the test set will illuminate. When the switch is in the "two-way" position, the 2-WAY indicator on the test set will illuminate.

3.7.3.7 MODULATION ON/OFF

When the modulation is OFF the MOD ON indicator on the test set will be extinguished. If the modulation switch is in the ON position, the indicator will illuminate.

3.7.3.8 DATA READY

When the Ranging Equipment is operating and data is available, the DATA READY indicator on the test set will flash on and off at a 10 Hz rate.

3.7.3.9 VCO CHANGE/DOPPLER BAD

Monitor J35 on the test set with a scope. Depress the RESET button on the DIGITAL PROCESSOR and then place the system in the START mode. Observe that the pulse is as shown in Figure 9.

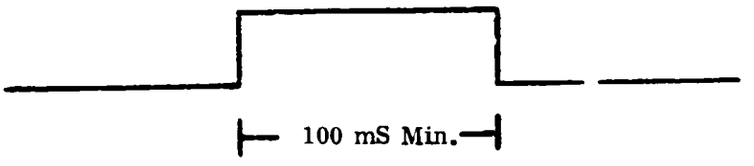


FIGURE 9.

3.7.4 COMPUTER INTERFACE

This test demonstrates that the system interface fulfills the requirement of the specification.

3.7.4.1 COMPUTER CONTROLLED & MONITORED FUNCTIONS

The following functions are both controlled and monitored by the computer. For these functions, the system test set will be used to place the system in a certain mode and indicators on the test set and system will monitor that the function has indeed been selected. Set switches and monitor indicators as shown in Table IV.

The system is in the Computer Control Mode for this test.

3.7.4.2 COMPUTER MONITORED FUNCTIONS

All of the Computer Monitored functions were checked in the computer mode of operation in Section 3.7.4.1. In this test, the system is placed in the LOCAL mode and the system is manually operated and outputs to the computer are monitored by indicators on the test set. Set switches and verify indicators as shown in Table V.

TABLE IV.

FUNCTION BEING TESTED	SYSTEM TEST SET SWITCH	SWITCH TO POS.	INDICATOR	SYSTEM INDICATOR
Start/Reset	Start/Reset	③	Start ON Start OFF	"START" ON "RESET" ON
Resolution Tone Selected	Resolution Tone	500 100 20	500 100 20	"500 kHz" ON "100 kHz" ON "20 kHz" ON
Modulation ON/OFF	Modulation ON/OFF	ON OFF	MOD ON MOD OFF	"MOD ON" ON "MOD OFF" ON
One-way/Two-way Doppler	Doppler 1-way/2-way	1-Way 2-Way	1-Way ON 2-Way ON	"1-Way" ON "2-Way" ON
Local Computer Selected	N/A	④	COMP Mode On Local Mode On	"COMP" ON "LOCAL" ON
ARC Use Bypass	N/A	⑤	USE ON BYPASS ON	"USE" ON "BYPASS" ON
RF Ready ②	N/A	N/A	RF READY ON	"RF READY" ON
Range Acquired ①	N/A	N/A	Range ACQ ON	"RANGE ACQ COMPL" ON

NOTE: ① Press reset button and insure that RANGE ACQ indicator on the test set and the RANGE ACQ COMP indicator on the system go out. Return button to START position. System must be in LOCAL SIM BYPASS mode for this test.

② Place the EXCITER READY switch on the test set to the DOWN position and insure that the RF READY indicators on the system and on the test set go out. Return the EXCITER READY switch to the UP position.

③ Momentary Switch. System changes state when switch is depressed.

④ LOCAL/COMP switch on the system must be activated.

⑤ ARC USE/BYPASS switch on system must be activated.

TABLE V.

FUNCTION BEING TESTED	SYSTEM SWITCH/INDICATOR	TEST SET INDICATOR (Computer Monitor Section)
Start/Reset	"START" ON "START" ON	START ON START OFF
Resolution Tone Selected	"500 kHz" ON "100 kHz" ON "20 kHz" ON	500 ON 100 ON 20 ON
Modulation ON/OFF (2)	"MOD ON" ON "MOD OFF" ON	MOD ON MOD ON
One-way Two-way Doppler	"One-way" ON "Two-way" ON	Doppler 1-Way ON Doppler 2-way ON
Local/Computer Selected	"LOCAL" ON "COMP" ON	LOCAL ON COMP ON
ARC Use/Bypass	"USE" ON "BYPASS" ON	USE ON BYPASS ON
Range Acquired (1)	"RANGE ACQ COMPL" ON	RANGE ACQ ON
RF Ready (1)	"RF READY" ON	RF READY ON

NOTE: (1) These functions previously tested in Table IV.

(2) System START/RESET control must be in the START position.

STDN RANGING EQUIPMENT

D.V.T. DATA SHEETS

SYSTEM S/N _____ DATE _____

OPERATOR _____

Q/A REPRESENTATIVE _____

SYSTEM ACCEPTED ☐

SYSTEM REJECTED ☐

LIST OF TEST EQUIPMENT

DESCRIPTION	S/N
Tape Recorder, Sangamo Model 3500	
IRIG B Time Code Generator	
Oscilloscope Tektronix 475 Oscilloscope	
Computing Counter, HP5360A	
Time Interval Unit, HP5379A	
RF Voltmeter, HP413A	
Spectrum Analyzer, HP8551A/851A	
Test Set, General Dynamics/Electronics P/N 2106960	
Attenuator, Kay Model 30-0	
Noise Generator, GD/Electronics P/N 2106988	
Tape for Recorder, Scotch 871-1-3600 IRH	
Frequency Synthesizer, HP5105A	
Synthesizer Driver, HP5105B	
Signal Generator, HP606A	
Power Supply +5V, 7 Amps	
Power Supply +5V, 3 Amps	
Power Supply -7.4V, 250 mA	
Ammeter, Weston 901	
Wave Analyzer, HP310A	
HP331A Distortion Analyzer	
Signal Combiner, GD/Electronics P/N 2106987	
Power Meter, HP431C	

APPENDIX C

STDN RANGING EQUIPMENT
DESIGN VERIFICATION
TEST RESULTS

SYSTEM S/N 001, 002, AND 013

SYSTEM S/N 001 -ENG model DATE 10-1-74

OPERATOR ENG.

Q/A REPRESENTATIVE U. BURKS D. OLSON

SYSTEM ACCEPTED ☐

SYSTEM REJECTED ☐

THE ENG UNIT WAS ACCP BY NASA, FRED HEROLD, WITH THE INDICATED OUT OF TOL. CONDITIONS. ALL OUT OF TOL CONDITION ON THE TAPE TEST WERE LISTED ON DD250. THESE CONDITIONS WERE ACCP'd ON ENG MODEL ONLY.

ENG MODEL WAS SHIPPED 10-2-74

D Olson

LIST OF TEST EQUIPMENT

DESCRIPTION ENG MODEL S/N 01

Tape Recorder, Sangamo Model 3500

IRIG B Time Code Generator

Oscilloscope Tektronix 475 Oscilloscope

Computing Counter, HP5360A

Time Interval Unit, HP5379A

RF Voltm.ter, HP413A

Spectru.n Analyzer, HP8551A/851A

Test Set, General Dynamics/Electronics P/N 2106960

Attenuator, Kay Model 30-0

Noise Generator, GD/Electronics P/N 2106988

Tape for Recorder, Scotch 871-1-3600 IRH

Frequency Synthesizer, HP5105A

Synthesizer Driver, HP5105B

Signal Generator, HP606A

Power Supply +5V, 7 Amps

Power Supply +5V, 3 Amps

Power Supply -7.4V, 250 mA

Ammeter, Weston 901

Wave Analyzer, HP310A

HP331A Distortion Analyzer

Signal Combiner, GD/Electronics P/N 2106987

Power Meter, HP431C

ENG MODEL - 19-1-74

STEP	TEST NO.	UNITS	MIN	MEASURED	MAX	ACCEPTED	REJECTED
2.1	---	Presence of Chassis Slides	Present	OK	Present		
2.2	---	Presence of Cable Retractors	Present	OK	Present		
2.3.1	---	Guards on Critical Switches	Present	OK	Present		
2.3.2	---	Durable Marking	Present	OK	Present		
3.1	---	Operation on AC Input	Yes	OK	Yes		
3.1.1	---	Presence of Time Meter	Present	OK	Present		
3.1.2	---	Operation of Power on Indicator	Proper	OK	Proper		
3.2.1 (+15V)	---	Amps	---		1.8		
3.2.1 (-15V)	---	Amps	---		4.0		
3.2.1 (+5V)	---	Amps	---		36		
3.2.1 (-5.2V)	---	Amps	---		12		
3.2.1 (+24V Relay)	---	Amps	---		8		
3.2.1 (+24V Signal)	---	Amps	---		2.4		
3.2.2	---	Operation at Var AC In	Yes		Yes		
3.2.3	---	Current Limit on Supply	Yes		Yes		
3.2.4	---	Power Supply Adjustability	Yes		Yes		
3.2.5	---	Line and Load Regulation	Yes		Yes		
3.2.6	---	Verification of Fuses	Present		Present		
			(1)				

STEP	TEST NO	UNITS	MIN	MEASURED	MAX	ACCEPTED	REJECTED
3.3.1	---	Hz V p-p	5,000,000 2	5,000,000 2.0	5,000,000 ---		
3.3.2	---	M.S. M.S. V p-p N.S.	78 18 -5.5 0	80 20 6.0 9.3	82 22 6.5 10		
3.3.2.1	---	N.S. (Stability)	-25	2-2.5	25		
3.3.2.1 td_1		N.S.	---	132	---		
3.3.2.2	---	N.S.	-25	[illegible]	+25		
3.3.3.1	---	V p-p	0	4.0	4		
3.3.3.2 (20) 1Vpp	---	%	---	.9	1		
3.3.3.2 (100) 1Vpp	---	%	---	1.0	1		
3.3.3.2 (500) 1Vpp	---	%	---	.78	1		
3.3.3.2 (500) 2Vpp	---	%	---	.80	1		
3.3.3.2 (1 0) 2Vpp	---	%	---	1.05 *	1 CONDITION ACCEPTED BY NASA		
3.3.3.2 (2) 2Vpp	---	%	---	.98	1		
3.3.3.3 (C)	---	500 kHz Tone	Not Present	NOT PRESENT	Not Present		
3.3.3.3 (D)	---	500 kHz Tone	Present	PRESENT	Present		
3.3.3.4 (500)	---	Range ACQ	---	ILLUMINATED	Illuminated	SIM LIGHT	CONDITION
3.3.3.4 (100)	---	Range ACQ	---	ILLUMINATED	Illuminated	BY NASA	ACCP
3.3.3.4 (20)	---	Range ACQ	---	ILLUMINATED	Illuminated		TO
3.3.3.5	---	500 kHz Minor Tones	--- ---	ILLUMINATED EXTINGUISHED	Illuminated Extinguished		NASA
3.3.3.6	---	ARC Range ACQ	--- ---	EXTINGUISHED ILLUMINATED	Extinguished Illuminated		
3.3.3.7 (100 kHz)	---	100 kHz IND	---	ILLUMINATED	Illuminated		
3.3.3. 0 kHz)	---	20 kHz IND	---	ILLUMINATED	Illuminated		
3.3.3.7 (4 kHz)	---	4 kHz IND	---	ILLUMINATED	Illuminated		
			(2)				

STEP	TEST NO	UNITS	MIN	MEASURED	MAX	ACCEPTED	REJECTED
3.3.3.7 (0 Hz)	---	800 Hz IND.	---	[illegible]	Illuminated		
3.3.3.7 (10 Hz)	---	10 Hz IND.	---	[illegible]	Illuminated		
3.3.3.7		Range Acq Comp Ind.	---	ILLUMINATE	Illuminated		
3.4.3	---	MV RMS	---	.5/MV	---		
3.4.5	---	MV RMS	---	.5 MV	---		
3.5.2.1	---	N.S.	1	1	1		
3.5.2.2	---	N.S.	3,333,300	3,333,331	3,333,360		
3.5.2.3	---	N.S.	1,698,303	1,698,331	1,698,363		
3.5.3.1	00	N.S.	--	1.26	~~3.3~~ 6.66		
3.5.3.2	01	N.S.	---	8.68	~~4.23~~ 8.43		
3.5.3.3	02	N.S.	---	0.93	~~21.9~~ 43.8		
3.5.4.1	---	M.V. (RMS)	---	1.43	---		
3.5.4.1.1 (,)	---	D.B.	---	62.0	---		
3.5.4.1.2 (+45)	---	D.B.	---	57.0	---		
3.5.4.1.2 (+40)	---	D.B.	---	52.0	---		
3.5.4.1.2 (+35)	--	D.B.	---	47.0	---		
3.5.4.1.2 (+30)	---	D.B.	---	42.0	---		
3.5.4.1.2 (+25)	---	D.B.	---	36.5	---		
3.5.4.1.2 (+20)	---	D.B.	---	31.5	---		
3.5.4.1.2 (+15)	---	D.B.	---	26.5	---		
3.5.4.1.2 (+12)	---	D.B.	---	23.0	---		
3.5.4.1.2 (+10)	---	D.B.	---	20.0	---		
			(3)				

STEP	TEST NO	UNITS	MIN	MEASURED	MAX	ACCEPTED	REJECTED
3.5.4.2.1 (500 kHz +50 dB)	03	N.S.	---	1.05	3.3		
3.5.4.2.2 (500 kHz +45 dB)	04	N.S.	---	1.01	3.3		
3.5.4.2.3 (500 kHz +40 dB)	05	N.S.	---	1.68	3.3		
3.5.4.2.4 (500 kHz +35 dB)	06	N.S.	---	1.75	3.3		
3.5.4.2.5 (500 kHz +30 dB)	07	N.S.	---	2.41	3.56		
3.5.4.2.6 (500 kHz +25 dB)	08	N.S.	---	3.24	4.1		
3.5.4.2.7 (500 kHz +20 dB	09	N.	---	7.04	4.86		
3.5.4.2.8 (500 kHz +15 dB)	10	N.S.	---	13.69	7.16		
3.5.4.2.9 (500 kHz +10 dB)	11	N.S.	---	37.13 *	11.7		
3.5.4.3.1 (100 kHz +50 dB)	12	N.S.	---	1.56	4.23		
3.5.4.3.2 (100 kHz +45 dB)	13	N.S.	---	2.0	4.23		
3.5.4.3.3 (100 kHz +40 dB)	14	N.S.	---	4.42	4.72		
3.5.4.3.4 (100 kHz +35 dB)	15	N.S.	---	5.09	5.43		
3.5.4.3.5 (100 kHz +30 dB)	16	N.S.	---	11.10	7.16 TAPE CHANNEL SHUT OFF OF RECEIVER CAUSED LOSS OF SYNC = RESET		
3.5.4.3.6 (100 kHz + 25 dB)	17	N.S.	---	17.48	10.9		
3.5.4.3.7 (100 kHz +20 dB)	18	N.S.	---	45.5 *	17.76		
3.5.4.3.8 (100 kHz +15 dB)	19	N.S.	---	71.46 *	31.06		
3.5.4.3.9 (100 kHz +10 dB)	20	N.S.	---	151.89 *	58.2		
3.5.4.4.1 (20 kHz +50 dB)	21	N.S.	---	7.28	21.9		

STEP	TEST NO	UNITS	MIN	MEASURED	MAX	ACCEPTED	REJECTED
3.5.4.4.2 (20 kHz +45 dB)	22	N.S.	---	11	21.9 43.8		
3.5.4.4.3 (20 kHz +40 dB)	23	N.S.	---	23.11	23.3 46.6		
3.5.4.4.4 (20 kHz +35 dB)	24	N.S.	---	28.84	27.9 55.8		
3.5.4.4.5 (20 kHz +30 dB)	25	N.S.	---	70.82	38.3 76.6		
3.5.4.4.6 (20 kHz +25 dB)	26	N.S.	---	150.72 *	58.23 116.46	PANEL 5-5-92	[illegible]
3.5.4.4.7 (20 kHz +20 dB)	27	N.S.	--	302.64 *	91.6 183.2		
3.5.4.4.8 (20 kHz +15 dB)	28	N.S.	---	464.3 *	166.6 333.2		
3.5.4.4.9 (20 kHz +10 dB)	29	N.S.	---	861.55 *	300 (PUT CURVE 666)		
3.5.5.1	---	Seconds	0	17.4	22		
3.5.5.2	---	Minutes	---	5MIN 24SEC	---		
3.5.5.3	---	Seconds	0	2.88	4		
3.5.6 (-225 kHz)	30	N.S.	-16.6	1,25	-16.6		
3.5.8	---	uSec	---	18.4	25		
3.6.1 (0 kHz)	31	Counts	---	20.22 *	10	[illegible]	[illegible]
3.6.1 (115 kHz)	32	Counts	---	31.38 *	10		
3.6.1 (-115 kHz)	33	Counts	---	19.9 *	10		
3.6.1 (218 kHz)	34	Counts	---	100.34 *	10		
3.6.1 (-218 kHz)	35	Counts	---	15.2 *	10		
3.6.3	---	N.S. (Stability)	-25	7.0	+25		
3.6.3 td	---	N.S.	---	102	---		
3.6.4	---	N.S.	-50	30	+50		

C-3

STEP	TEST NO	UNITS	MIN	MEASURED	MAX	ACCEPTED	REJECTED
3.6.4 (N1)	--	Hz	---	2.979219655XX	---		
3.6.4 (N2)	---	Hz	---	237347409	---		
3.6.4 (N3)	---	Hz	---	305849475	---		
3.7.1.1 (ON)	---	RF RDY IND	ON	ON	ON		
3.7.1.1 (OFF)	---	RF RDY IND	OFF	OFF	OFF		
3.7.1.2 (Simulate)	---	dB REF -10dB	---	-2dB	---		
3.7.1.2 (Normal)	---	dB (with respect to reading in 3.7.1.2 Simulate)	-2	0	+2		
3.7.2.1	---	Results per Table II	YES	YES	YES		
3.7.2.2	---	dB	-3	-1.1dB	+3		
3.7.2.3 (VCXO 1)	---	dBm	0	+2.3dBm	---		
3.7.2.3 (VCXO 2)	---	dBm	0	+3.2dBm	---		
3.7.2.4 (SIM)	---	dBm REF [illegible]	---	.1dBm	---		
3.7.2.4 (NORM)	---	dBm (With respect to reading in 3.7.2.4 SIM)	-2	0	+2		
3.7.3.3 (500 kHz)	---	500 Indicator	ON	ON	ON		
3.7.3.3 (100 kHz)	---	100 Indicator	ON	ON	ON		
3.7.3.3 (20 kHz)	---	20 Indicator	ON	ON	ON		
3.7.3.5 (Dopp Good)	---	Doppler Good Indicator	ON	ON	ON		
3.7.3.5 (Dopp Bad)	---	Doppler Bad Indicator	ON	ON	ON		
3.7.3.6 (1-way)	---	1-way Indicator	ON	ON	ON		
			(6)				

STEP	TEST NO	UNITS	MIN	MEASURED	MAX	ACCEPTED	REJECTED
3.7.3.6 (2-way)	---	2-way Indicator	ON	ON	ON		
3.7.3.7 (Mod Off)	---	Mod On Indicator	OFF	off	OFF		
3.7.3.7 (Mod On)	---	Mod On Indicator	ON	ON	ON		
3.7.3.8	---	Data RDY	Flashing	Flashing	Flashing		
3.7.3.9	---	MS	100	100	---		
3.7.4.1	---	Results per Table IV	Yes	yes	Yes		
3.7.4.2	---	Results per Table V	Yes	yes	Yes		
			(7)				

SYSTEM S/N 002 DATE 8 Jan 75

OPERATOR J. Bryson; W. A. MacBrayer

Q/A REPRESENTATIVE [illegible] D. Olson

DCAS: C. G. Adolph

SYSTEM ACCEPTED ☑

SYSTEM REJECTED ☐

Waiver (Ref Para 3.3.3.2.) 318-001

LIST OF TEST EQUIPMENT

DESCRIPTION	S/N 002
Tape Recorder, Sangamo Model 3500	7E01251
IRIG B Time Code Generator	001
Oscilloscope Tektronix 475 Oscilloscope	7E01565
Computing Counter, HP5360A	7E01481
Time Interval Unit, HP5379A	7E01482
RF Voltmeter, HP413A	7E00571
Spectrum Analyzer, HP3551A/851A	(Model 1415) 7093858
Test Set, General Dynamics/Electronics P/N 2106950	Tool No. 8M00143
Attenuator, Kay Model 30-0	(120-0) 0E08002
Noise Generator, GD/Electronics P/N 2106938	Tool No. 8M00156
Tape for Recorder, Scotch 871-1-3600 IRIG	No Serial Number (4 Rolls)
Frequency Synthesizer, HP5105A	(Model HP 5100A) 9E03851
Synthesizer Driver, HP5105B	(Model HP5100A) 9E03852
Signal Generator, HP606A	(Model 608D) 9E04162
Power Supply +5V, 7 Amps	0E04883
Power Supply +5V, 3 Amps	1E08925
Power Supply -7.4V, 250 mA	0E08595
Ammeter, Weston 931	1E09272 ~~7E08414~~
Wave Analyzer, HP310A	9E04578
HP331A Distortion Analyzer	9E04062
Signal Combiner, GD/Electronics P/N 2106963	Tool No. 8M00157
Power Meter, HP431C	(Model 432A) 1E11443

STEP	TEST NO.	UNITS	MIN	MEASURED	MAX	ACCEPTED	REJECTED
2.1	---	Presence of Chassis Slides	Present	Present	Present		
2.2	---	Presence of Cable Retractors	Present	Present	Present		
2.3.1	---	Guards on Critical Switches	Present	Present	Present		
2.3.2	---	Durable Marking	Present	Present	Present		
3.1	---	Operation on AC Input	Yes	Yes	Yes		
3.1.1	---	Presence of Time Meter	Present	Present	Present		
3.1.2	---	Operation of Power on Indicator	Proper	Proper	Proper		
3.2.1 (+15V)	---	Amps	---	4	1.8		
3.2.1 (-15V)	---	Amps	---	1	4.0		
3.2.1 (+5V)	---	Amps	---	28	36		
3.2.1 (-5.2V)	---	Amps	---	11.75	12		
3.2.1 (+24V Relay)	---	Amps	---	1.65	8		
3.2.1 (+24V Signal)	---	Amps	---	1.05	2.4		
3.2.2	---	Operation at Var AC In	Yes	Yes	Yes		
3.2.3	---	Current Limit on Supply	Yes	Yes	Yes		
3.2.4	---	Power Supply Adjustability	Yes	Yes	Yes		
3.2.5	---	Line and Load Regulation	Yes	Yes	Yes		
3.2.6	---	Verification of Fuses	Present	Present	Present		
			(1)				

STEP	TEST NO	UNITS	MIN	MEASURED	MAX	ACCEPTED	REJECTED
3.3.1	---	Hz V p-p	5,000,000 2	 2.8	5,000,000 ---		
3.3.2	---	M.S. M.S. V p-p N.S.	78 18 -5.5 0	80 20 6.0 8.5	82 22 6.5 10		
3.3.2.1	---	N.S. (Stability)	-25	± 1	25		
3.3.2.1 td1		N.S.	---	35	---		
3.3.2.2	---	N.S.	-25	± 7.5	+25		
3.3.3.1	---	V p-p	0	RANGE 0 TO 5.5	4		
3.3.3.2 (20) 1Vpp	---	%	---	.98	± 1.2		
3.3.3.2 (100) 1Vpp	---	%	---	1.1	± 1.2		
3.3.3.2 (500) 1Vpp	---	%	---	1.15	± 1.2		
3.3.3.2 (500) 2Vpp	---	%	---	1.45	± 1.5		
3.3.3.2 (100) 2Vpp	---	%	---	1.1	± 1.5		
3.3.3.2 (20) 2Vpp	---	%	---	1	± 1.5		
3.3.3.3 (C)	---	500 kHz Tone	Not Present	Not Present	Not Present		
3.3.3.3 (D)	---	500 kHz Tone	Present	Present	Present		
3.3.3.4 (500)	---	Range ACQ	---	ILL	Illuminated		
3.3.3.4 (100)	---	Range ACQ	---	ILL	Illuminated		
3.3.3.4 (20)	---	Range ACQ	---	ILL	Illuminated		
3.3.3.5	---	500 kHz Minor Tones	--- ---	ILL EXT	Illuminated Extinguished		
3.3.3.6	---	ARC Range ACQ	--- ---	EXT ILL	Extinguished Illuminated		
3.3.3.7 (100 kHz)	---	100 kHz IND	---	ILL	Illuminated		
3.3.3.7 (20 kHz)	---	20 kHz IND	---	ILL	Illuminated		
3.3.3.7 (4 kHz)	---	4 kHz IND	---	ILL	Illuminated		
			(2)				

Reference Winner 318-001

STEP	TEST NO	UNITS	MIN	MEASURED	MAX	ACCEPTED	REJECTED
3.3.3.7 (800 Hz)	---	800 Hz IND.	---	ON	Illuminated		
3.3.3.7 (10 Hz)	---	10 Hz IND.	---	ON	Illuminated		
3.3.3.7		Range Acq Comp Ind.	---	ON	Illuminated		
3.4.3	---	MV RMS	---	.6 MV	---		
3.4.5	---	MV RMS	---	.57M	---		
3.5.2.1	---	N.S.	1	1	1		
3.5.2.2	---	N.S.	3,333,300	3,333,317	3,333,360		
3.5.2.3	---	N.S.	1,698,303	1,698,349	1,698,363		
3.5.3.1	00	N.S.	--	.91	6.6		
3.5.3.2	01	N.S.	---	1.82	8.43		
3.5.3.3	02	N.S.	---	.81	43.8		
3.5.4.1	---	M.V. (RMS)	---	1.05 MV	---		
3.5.4.1.1	---	D.B.	---	70	---		
3.5.4.1.2 (+45)	---	D.B.	---	65	---		
3.5.4.1.2 (+40)	---	D.B.	---	60	---		
3.5.4.1.2 (+35)	---	D.B.	---	55	---		
3.5.4.1.2 (+30)	---	D.B.	---	50	---		
3.5.4.1.2 (+25)	---	D.B.	---	44	---		
3.5.4.1.2 (+20)	---	D.B.	---	39	---		
3.5.4.1.2 (+15)	---	D.B.	---	34	---		
3.5.4.1.2 (+12)	---	D.B.	---	31.5	---		
3.5.4.1.2 (+10)	---	D.B.	---	29	---		
			(3)				

STEP	TEST NO	UNITS	MIN	MEASURED	MAX	ACCEPTED	REJECTED
3.5.4.2.1 (500 kHz +50 dB)	03	N.S.	---	3.5	6.6		
3.5.4.2.2 (500 kHz +45 dB)	04	N.S.	---	12.36	6.6 Bad Data Point		
3.5.4.2.3 (500 kHz +40 dB)	05	N.S.	---	4.22	6.6		
3.5.4.2.4 (500 kHz +35 dB)	06	N.S.	---	2.63	6.6		
3.5.4.2.5 (500 kHz +30 dB)	07	N.S.	---	6.19	7.12		
3.5.4.2.6 (500 kHz +25 dB)	08	N.S.	---	8.32	8.2 O.K.		
3.5.4.2.7 (500 kHz +20 dB	09	N.S.	---	8.78	9.72		
3.5.4.2.8 (500 kHz +15 dB)	10	N.S.	---	12.78	14.32		
3.5.4.2.9 (500 kHz +10 dB)	11	N.S.	---	16.44	23.4		
3.5.4.3.1 (100 kHz +50 dB)	12	N.S.	---	1.06	8.46		
3.5.4.3.2 (100 kHz +45 dB)	13	N.S.	---	8.98	8.46 O.K.		
3.5.4.3.3 (100 kHz +40 dB)	14	N.S.	---	5.52	9.44		
3.5.4.3.4 (100 kHz +35 dB)	15	N.S.	---	5.47	10.86		
3.5.4.3.5 (100 kHz +30 dB)	16	N.S.	---	23.62	14.32 Bad Data Point		
3.5.4.3.6 (100 kHz + 25 dB)	17	N.S.	---	14.35	21.8		
3.5.4.3.7 (100 kHz +20 dB)	18	N.S.	---	18.35	35.52		
3.5.4.3.8 (100 kHz +15 dB)	19	N.S.	---	30.71	62.12		
3.5.4.3.9 (100 kHz +10 dB)	20	N.S.	---	107.7	116.4		
3.5.4.4.1 (20 kHz +50 dB)	21	N.S.	---	1.9	43.6		
			(4)				

STEP	TEST NO	UNITS	MIN	MEASURED	MAX	ACCEPTED	REJECTED
3.5.4.4.2 (20 kHz +45 dB)	22	N.S.	---	46.57	43.8 } Bad Data Point	SWA	
3.5.4.4.3 (20 kHz +40 dB)	23	N.S.	---	82.85	46.6 }		
3.5.4.4.4 (20 kHz +35 dB)	24	N.S.	---	38.42	55.8		
3.5.4.4.5 (20 kHz +30 dB)	25	N.S.	---	52.76	76.6		
3.5.4.4.6 (20 kHz +25 dB)	26	N.S.	---	61.47	116.46		
3.5.4.4.7 (20 kHz + 20 dB)	27	N.S.	---	134.0	183.2		
3.5.4.4.8 (20 kHz +15 dB)	28	N.S.	---	189.31	332.2		
3.5.4.4.9 (20 kHz +10 dB)	29	N.S.	---	542.77	600		
3.5.5.1	---	Seconds	0	17	22		
3.5.5.2	---	Minutes	---	1 MIN 13 SEC	---		
3.5.5.3	---	Seconds	0	2.5	4		
3.5.6 (-225 kHz)	30	N.S.	-16.6	1.9	+16.6		
3.5.7	---	uSec	---	24	25		
3.6.1 (0 kHz)	31	Counts	---	9.53	~~10~~ 35		
3.6.1 (115 kHz)	32	Counts	---	31.5	~~10~~ 30	SWA	
3.6.1 (-115 kHz)	33	Counts	---	22.88	~~10~~ 30	OK 1-8-95	
3.6.1 (218 kHz)	34	Counts	---	44.92	~~10~~ 45		
3.6.1 (-218 kHz)	35	Counts	---	7.99	~~10~~ 25		
3.6.3	---	N.S. (Stability)	-25	±35	+25		
3.6.3 td_2	---	N.S.	---	73	---		
3.6.4	---	N.S.	-50	58	+50		

STEP	TEST NO	UNITS	MIN	MEASURED	MAX	ACCEPTED	REJECTED
3.6.4 (N1)	---	Hz	---	332053433435	---		
3.6.4 (N2)	---	Hz	---	77060004	---		
3.6.4 (N3)	---	Hz	---	5772001115610	---		
3.7.1.1 (ON)	---	RF RDY IND	ON	On	ON		
3.7.1.1 (OFF)	---	RF RDY IND	OFF	off	OFF		
3.7.1.2 (Simulate)	---	dB	---	-5.5	---		
3.7.1.2 (Normal)	---	dB (w respect to reading in 3.7.1.2 Simulate)	-2	0	+2		
3.7.2.1	---	Results per Table II	YES	Yes	YES		
3.7.2.2	---	dB	-3	.8	+3		
3.7.2.3 (VCXO 1)	---	dBm	> -3dbm	-2dBm	---		
3.7.2.3 (VCXO 2)	---	dBm	> -3dbm	-2dBm	---		
3.7.2.4 (SIM)	---	dBm	---	-5	---		
3.7.2.4 (NORM)	---	dBm (With respect to reading in 3.7.2.4 SIM)	-2	0	+2		
3.7.3.3 (500 kHz)	---	500 Indicator	ON	On	ON		
3.7.3.3 (100 kHz)	---	100 Indicator	ON	On	ON		
3.7.3.3 (20 kHz)	---	20 Indicator	ON	On	ON		
3.7.3.4 (ON)	---	Range Acq. Ind.	ON	On	ON		
3.7.3.4 (OFF)	---	Range Acq. Ind.	OFF	off	OFF		
3.7.3.5 (Dop Good)	---	Doppler Good indicator	ON	On	ON		
3.7.3.5 (Dop Bad)	---	Doppler Bad Indicator	ON	On	ON		
3.7.3.6 (1-way)	---	1-Way Indicator	ON	On	ON		
			(6)				

STEP	TEST NO	UNITS	MIN	MEASURED	MAX	ACCEPTED	REJECTED
3.7.3.6 (2-way)	---	2-way Indicator	ON	on	ON		
3.7.3.7 (Mod Off)	---	Mod On Indicator	OFF	off	OFF		
3.7.3.7 (Mod On)	---	Mod On Indicator	ON	on	ON		
3.7.3.8	---	Data RDY	Flashing	flashing	Flashing		
3.7.3.9	---	MS	100	100	---		
3.7.4.1	---	Results per Table IV	Yes	yes	Yes		
3.7.4.2	---	Results per Table V	Yes	yes	Yes		
			(7)				

SYSTEM S/N 013 DATE 6 June 1975

OPERATOR W. A. McBrayer

Q/E REPRESENTATIVE [illegible] 6-9-75

SYSTEM ACCEPTED ☑ F. W. Herold

SYSTEM REJECTED ☐

DVT PERFORMED ON THIS UNIT IN LIEU OF SYSTEM ATP PER F. HEROLD, NASA TECH OFFICER

LIST OF TEST EQUIPMENT

DESCRIPTION S/N 013

Tape Recorder, Sangamo Model 3500 #7E01251

IRIG B Time Code Generator #132139

Oscilloscope Tektronix 475 Oscilloscope #7E01535

Computing Counter, HP5360A #9E04977

Time Interval Unit, HP5379A

RF Voltmeter, ~~HP413A~~ 3478A #0E09042

Spectrum Analyzer, ~~HP 141A/851A~~ 8554L/8552A #7E01195

Test Set, General Dynamics/Electronics P/N 2106960 8m00143

Attenuator, Kay Model 30-0 #1E05957

Noise Generator, GD/Electronics P/N 2106988 8m00136

.or Recorder, Scotch 871-1-3600 IRH

Frequency Synthesizer, HP5105A #7E00956

Synthesizer Driver, HP5105B #7E00918

Signal Generator, ~~HP606A~~ 606D #7E00519

Power Supply +5V, 7 Amps #1E16185

r Supply +5V, 3 Amps #9E04935

Supply -7.4V, 250 mA #0E08595

Ammeter, Weston 901 #0B10513

Wave Analyzer, HP310A #9E05080

HP331A Distortion Analyzer #9E04062

Signal Combiner, GD/Electronics P/N 2106987 8m00157

Power Meter, HP431C #9E03629

S/N 013

STEP	TEST NO.	UNITS	MIN	MEASURED	MAX	ACCEPTED	REJECTED
2.1	---	Presence of Chassis Slides	Present	Present	Present	✓	
2.2	---	Presence of Cable Retractors	Present	Present	Present	✓	
2.3.1	---	Guards on Critical Switches	Present	Present	Present	✓	
2.3.2	---	Durable Marking	Present	Present	Present	✓	
3.1	---	Operation on AC Input	Yes	Yes	Yes	✓	
3.1.1	---	Presence of Time Meter	Present	Present	Present	✓	
3.1.2	---	Operation of Power on Indicator	Proper	Proper	Proper	✓	
3.2.1 (+15V)	---	Amps	---	1.9	1.8	✓	
3.2.1 (-15V)	---	Amps	---	.94	4.0	✓	
3.2.1 (+5V)	---	Amps	---	28.5	36	✓	
3.2.1 (-5.2V	---	Amps	---	12	12	✓	
3.2.1 (+24V Relay)	---	Amps	---	1.2	3	✓	
3.2.1 (+24V Signal)	---	Amps	---	1	2.4	✓	
3.2.2	---	Operation at Var AC In	Yes	Yes	Yes	✓	
3.2.3	---	Current Limit on Supply	Yes	Yes	Yes	✓	
3.2.4	---	Power Supply Adjustability	Yes	Yes	Yes	✓	
3.2.5	---	Line and Load Regulation	Yes	Yes	Yes	✓	
3.2.6	---	Verification of Fuses	Present	Present	Present	✓	

STEP	TEST NO	UNITS	MIN	MEASURED	MAX	ACCEPTED	REJECTED
3.3.1	---	Hz V p-p	5,000,000 2	5,000,001 2 V p-p	5,000,000 ---		
3.3.2	---	M.S. M.S. V p-p N.S.	78 18 -5.5 0	80 20 -6.2 9.6	82 22 -6.5 10		
3.3.2.1	---	N.S. (Stability)	-25	1	25		
3.3.2.1 td_1		N.S.	---	24	---		
3.3.2.2	---	N.S.	-25	± 10	+25		
3.3.3.1	---	V p-p	0	5.8	4		
3.3.3.2 (20) 1Vpp	---	%	---	LT 1%	1.5		
3.3.3.2 (100) 1Vpp	---	%	---	LT 1%	1.5		
3.3.3.2 (500) 1Vpp	---	%	---	LT 1%	1.5		
3.3.3.2 (500) 2Vpp	---	%	---	LT 1%	1.5		
3.3.3.2 (100) 2Vpp	---	%	---	LT 1%	1.5		
3.3.3.2 (20) 2Vpp	---	%	---	LT 1%	1.5		
3.3.3.3 (C)	---	500 kHz Tone	Not Present	Not Present	Not Present		
3.3.3.3 (D)	---	500 kHz Tone	Present	Present	Present		
3.3.3.4 (500)	---	Range ACQ	---	ILL	Illuminated		
3.3.3.4 (100)	---	Range ACQ	---	ILL	Illuminated		
3.3.3.4 (20)	---	Range ACQ	---	ILL	Illuminated		
3.3.3.5	---	500 kHz Minor Tones	--- ---	ILL EXT	Illuminated Extinguished		
3.3.3.6	---	ARC Range ACQ	--- ---	EXT ILL	Extinguished Illuminated		
3.3.3.7 (100 kHz)	---	100 kHz IND	---	ILL	Illuminated		
3.3.3.7 (20 kHz)	---	20 kHz IND	---	ILL	Illuminated		
3.3.3.7 (4 kHz)	---	4 kHz IND	---	ILL	Illuminated		
			(2)				

STEP	TEST NO	UNITS	MIN	MEASURED	MAX	ACCEPTED	REJECTED
3.3.3.7 (800 Hz)	---	800 Hz IND.	---	ILL	Illuminated		
3.3.3.7 (10 Hz)	---	10 Hz IND.	---	ILL	Illuminated		
3.3.3.7		Range Acq Comp Ind.	---	ILL	Illuminated		
3.4.3	---	MV RMS	---	0.57 MV	---		
3.4.5	---	MV RMS	---	0.54 MV	---		
3.5.2.1	---	N.S.	1	1 none	1		
3.5.2.2	---	N.S.	3,333,300	3,33[illegible]	3,333,360		
3.5.2.3	---	N.S.	1,698,303	1,698,348	1,698,363		
3.5.3.1	00	N.S.	--	4.96	6.6		
3.5.3.2	01	N.S.	---	3.73	8.43		
3.5.3.3	02	N.S.	---	0.67	43.8		
3.5.4.1	---	M.V. (RMS)	---	0.96 MV	---		
3.5.4.1.1	---	D.B.	---	62	---		
3.5.4.1.2 (+45)	---	D.B.	---	57	---		
3.5.4.1.2 (+40)	---	D.B.	---	52	---		
3.5.4.1.2 (+35)	--	D.B.	---	47	---		
3.5.4.1.2 (+30)	---	D.B.	---	42	---		
3.5.4.1.2 (+25)	---	D.B.	---	37.1	---		
3.5.4.1.2 (+20)	---	D.B.	---	32	---		
3.5.4.1.2 (+15)	---	D.B.	---	27	---		
3.5.4.1.2 (+12)	---	D.B.	---	23.3	---		
3.5.4.1.2 (+10)	---	D.B.	---	21	---		

STEP	TEST NO	UNITS	MIN	MEASURED	MAX	ACCEPTED	REJECTED
3.5.4.2.1 (300 kHz +50 dB)	03	N.S.	---	0.54	6.6		
3.5.4.2.2 (300 kHz +45 dB)	04	N.S.	---	0.58	6.6		
3.5.4.2.3 (300 kHz +40 dB)	05	N.S.	---	0.57	6.6		
3.5.4.2.4 (300 KHz +35 dB)	06	N.S.	---	0.53	6.6		
3.5.4.2.5 (300 kHz +30 dB)	07	N.S.	---	0.96	7.12		
3.5.4.2.6 (300 kHz +25 dB)	08	N.S.	---	2.61	8.2		
3.5.4.2.7 (300 kHz +20 dB	09	N.S.	---	3.52	9.72		
3.5.4.2.8 (300 kHz +15 dB)	10	N.S.	---	7.97	14.32		
3.5.4.2.9 (300 kHz +10 dB)	11	N.S.	---	24.46	23.4		
3.5.4.3.1 (100 kHz +50 dB)	12	N.S.	---	0.94	8.46		
3.5.4.3.2 (100 kHz +45 dB)	13	N.S.	---	1.28	8.46		
3.5.4.3.3 (100 kHz +40 dB)	14	N.S.	---	1.81	9.44		
3.5.4.3.4 (100 kHz +35 dB)	15	N.S.	---	4.15	10.86		
3.5.4.3.5 (100 kHz +30 dB)	16	N.S.	---	12.38	14.32		
3.5.4.3.6 (100 kHz + 25 dB)	17	N.S.	---	26.77	21.8		
3.5.4.3.7 (100 kHz +20 dB)	18	N.S.	---	52.19	35.52		
3.5.4.3.8 (100 kHz +15 dB)	19	N.S.	---	53.71	62.12		
3.5.4.3.9 + 12 dB (100 kHz +10 dB)	20	N.S.	---	102.88	110.4		
3.5.4.4.1 (20 kHz +50 dB)	21	N.S.	---	0.90	43.8		
			(4)				

STEP	TEST NO	UNITS	MIN	MEASURED	MAX	ACCEPTED	REJECTED
3.5.4.4.2 (20 kHz +45 dB)	22	N.S.	---		43.8	OK / Init	
3.5.4.4.3 (20 kHz +40 dB)	23	N.S.	---	✓ 61.12	46.6	OK / Init	
3.5.4.4.4 (20 kHz +35 dB)	24	N.S.	---		55.8	OK	
3.5.4.4.5 (20 kHz +30 dB)	25	N.S.	---	✓ 60.41	76.6		
3.5.4.4.6 (20 kHz +25 dB)	26	N.S.	---	✓ 90.41	116.46		
3.5.4.4.7 (20 kHz + 20 dB)	27	N.S.	---	✓ 132.69	183.2		
3.5.4.4.8 (20 kHz +15 dB)	28	N.S.	---	✓ 322.56	332.2		
3.5.4.4.9 (20 kHz +10 dB)	29	N.S.	---	✓ 474.69	600		
3.5.5.1	---	Seconds	0	17.02 sec	22		
3.5.5.2	---	Minutes	---	4' 10"			
3.5.5.3 use 3.5.4 Proc	---	Seconds		4" - 2.38	+3 min		
3.5.6 (-225 kHz)	30	N.S.	-16.6	✓ 0.89	+16.6		
3.5.7	---	uSec	---	2 usec	25		
3.6.1 (0 kHz)	31	Counts	---	✓ 18.23	~~20~~ 25		
3.6.1 (115 kHz)	32	Counts	---	✓ 13.56	~~20~~ 30		
3.6.1 (-115 kHz)	33	Counts	---	✓ 9.12	~~20~~ 30		
3.6.1 (218 kHz)	34	Counts	---	✓ 131.17	~~40~~ 45	Check upchirp OK	
3.6.1 (-218 kHz)	35 36	Counts	---	✓ 11.29 ✓ 25.11	~~20~~ 25 10		
3.6.3	---	N.S. (Stability)	-25	4.5	+25		
3.6.3 td_2	---	N.S.	---	76.6	---		
3.6.4	---	N.S.	-50	48.5	+50		

STEP	TEST NO	UNITS	MIN	MEASURED	MAX	ACCEPTED	REJECTED
3.6.4 (N1)	---	Hz	---		---		
3.6.4 (N2)	---	Hz	---				
3.6.4 (N3)	---	Hz	---				
3.7.1.1 (ON)	---	RF RDY IND	ON	ON	ON		
3.7.1.1 (OFF)	---	RF RDY IND	OFF	OFF	OFF		
3.7.1.2 (Simulate)	---	dB	---	0 dB	---		
3.7.1.2 (Normal)	---	dB (with respect to reading in 3.7.1.2 Simulate)	-2	0dB	+2		
3.7.2.1	---	Results per Table II	YES	YES	YES		
3.7.2.2	---	dB	-3	-3	+3		
3.7.2.3 (VCXO 1)	---	dBm	~~0~~ -3	0	---		
3.7.2.3 (VCXO 2)	---	dBm	~~0~~ -3	0	---		
3.7.2.4 (SIM)	---	dBm	---	+1dBm	---		
3.7.2.4 (NORM)	---	dBm (With respect to reading in 3.7.2.4 SIM)	-2	+1dBm	+2		
3.7.3.3 (500 kHz)	---	500 Indicator	ON	ON	ON		
3.7.3.3 (100 kHz)	---	100 Indicator	ON	ON	ON		
3.7.3.3 (20 kHz)	---	20 Indicator	ON	ON	ON		
3.7.3.4 (ON)	---	Range Acq. Ind.	ON	ON	ON		
3.7.3.4 (OFF)	---	Range Acq. Ind.	OFF	OFF	OFF		
3.7.3.5 (Dop Good)	---	Doppler Good Indicator	ON	ON	ON		
3.7.3.5 (Dop Bad)	---	Doppler Bad Indicator	ON	ON	ON		
3.7.3.6 (1-way)	---	1-Way Indicator	ON	ON	ON		

STEP	TEST NO	UNITS	MIN	MEASURED	MAX	ACCEPTED	REJECTED
3.7.3.6 (2-way)	---	2-way Indicator	ON	ON	ON		
3.7.3.7 (Mod Off)	---	Mod On Indicator	OFF	OFF	OFF		
3.7.3.7 (Mod On)	---	Mod On Indicator	ON	ON	ON		
3.7.3.8	---	Data RDY	Flashing	FLASHING	Flashing		
3.7.3.9	---	MS	100	>100MS	---		
3.7.4.1	---	Results per Table IV	Yes	YES	Yes		
3.7.4.2	---	Results per Table V	Yes	YES	Yes		
3.7.3.4 (c)		RANGE ACQ IND	ON	ON	ON		
11		11	OFF	OFF	OFF		
			(7)				