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NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
WASHINGTON, D.C. 20546

REPLY TO
ATTN OF: GP

TO: USI/Scientific & Technical Information Division
Attention: Miss Winnie M. Morgan

FROM: GP/Office of Assistant General Counsel for
Patent Matters

SUBJECT: Announcement of NASA-Owned U. S. Patents in STAR

In accordance with the procedures agreed upon by Code GP and Code USI, the attached NASA-owned U. S. Patent is being forwarded for abstracting and announcement in NASA STAR.

The following information is provided:

U. S. Patent No. : 3,571,800

Government or
Corporate Employee : U.S. Government

Supplementary Corporate
Source (if applicable) :

NASA Patent Case No. : XLA-08799

NOTE - If this patent covers an invention made by a corporate employee of a NASA Contractor, the following is applicable:

Yes ☐ No ☒

Pursuant to Section 305(a) of the National Aeronautics and Space Act, the name of the Administrator of NASA appears on the first page of the patent; however, the name of the actual inventor (author) appears at the heading of Column No. 1 of the Specification, following the words ". . . with respect to an invention of . . ."

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Enclosure
Copy of Patent cited above

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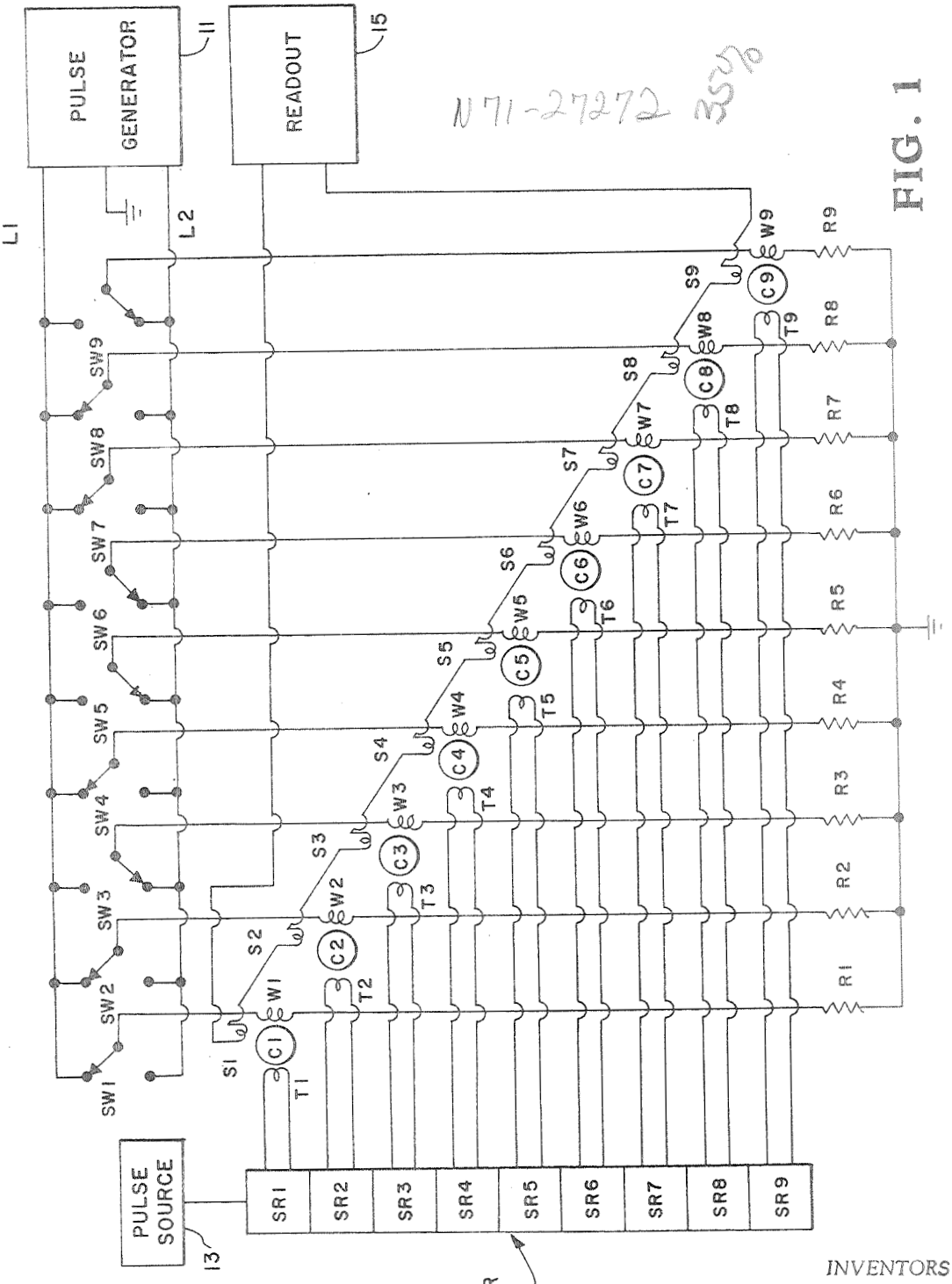

FIG. 1

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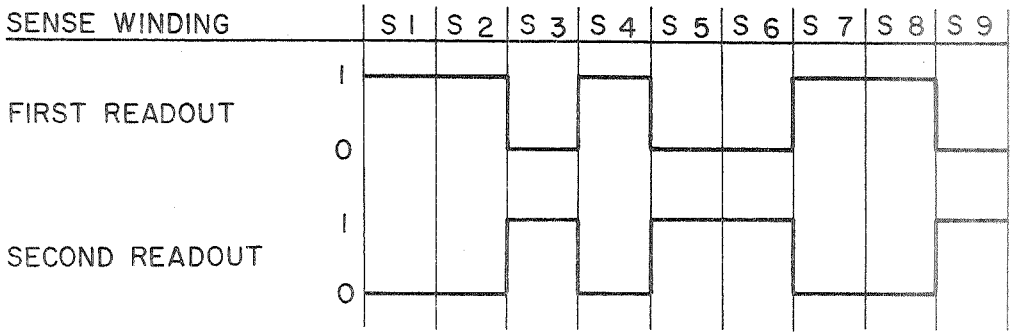

FIG. 2

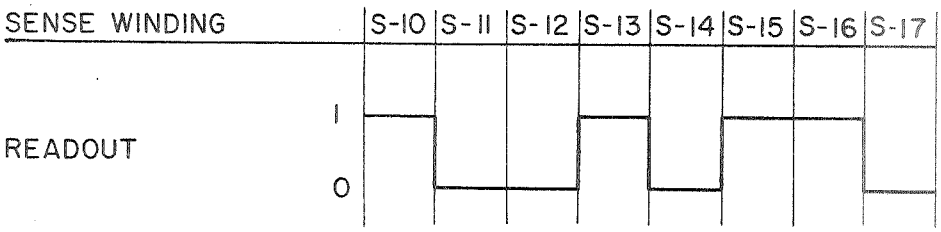

FIG. 4

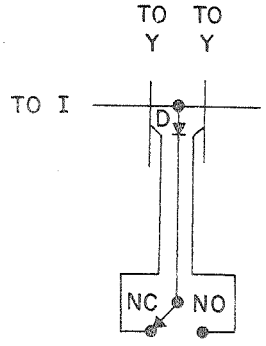

FIG. 6

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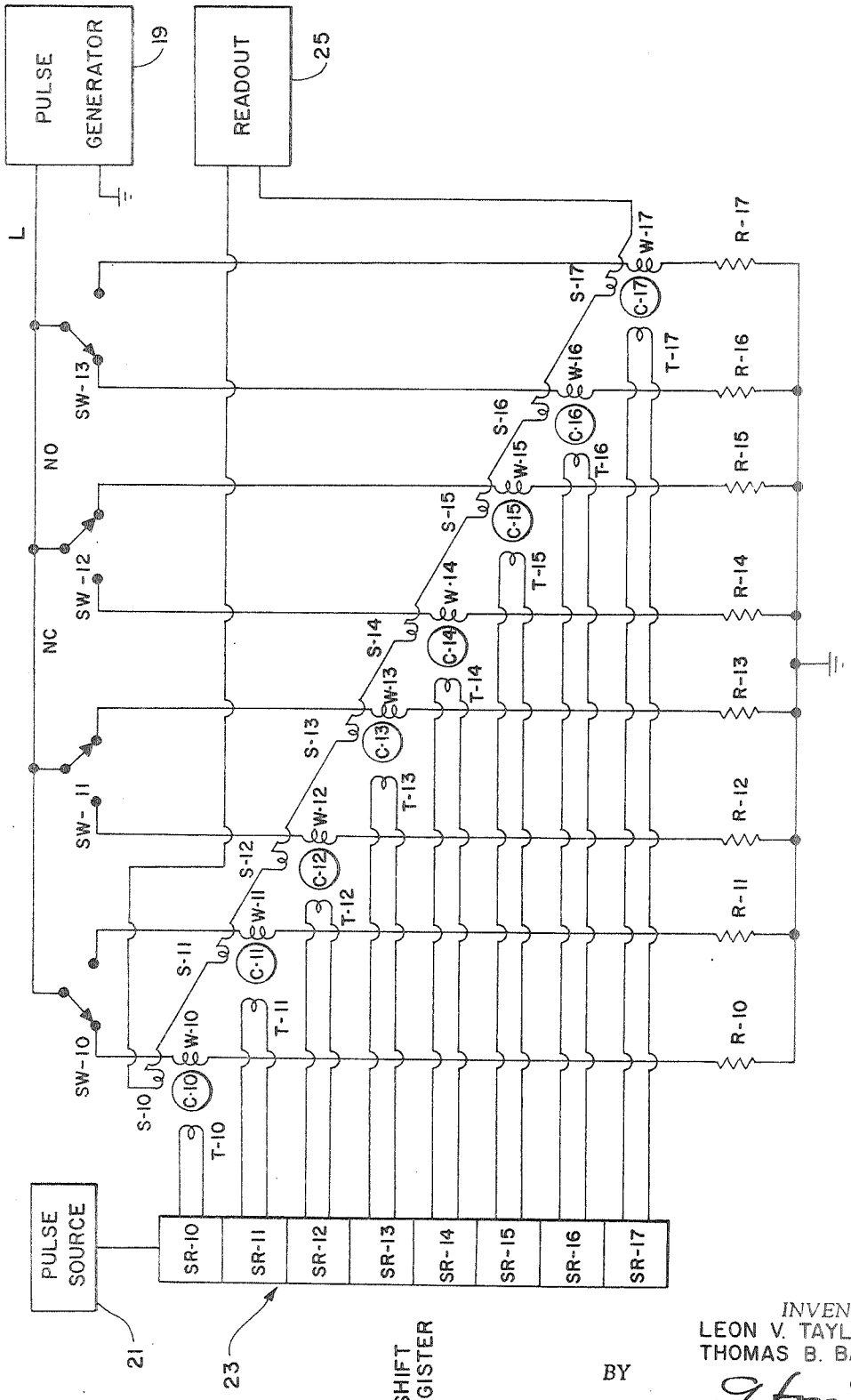

FIG. 3

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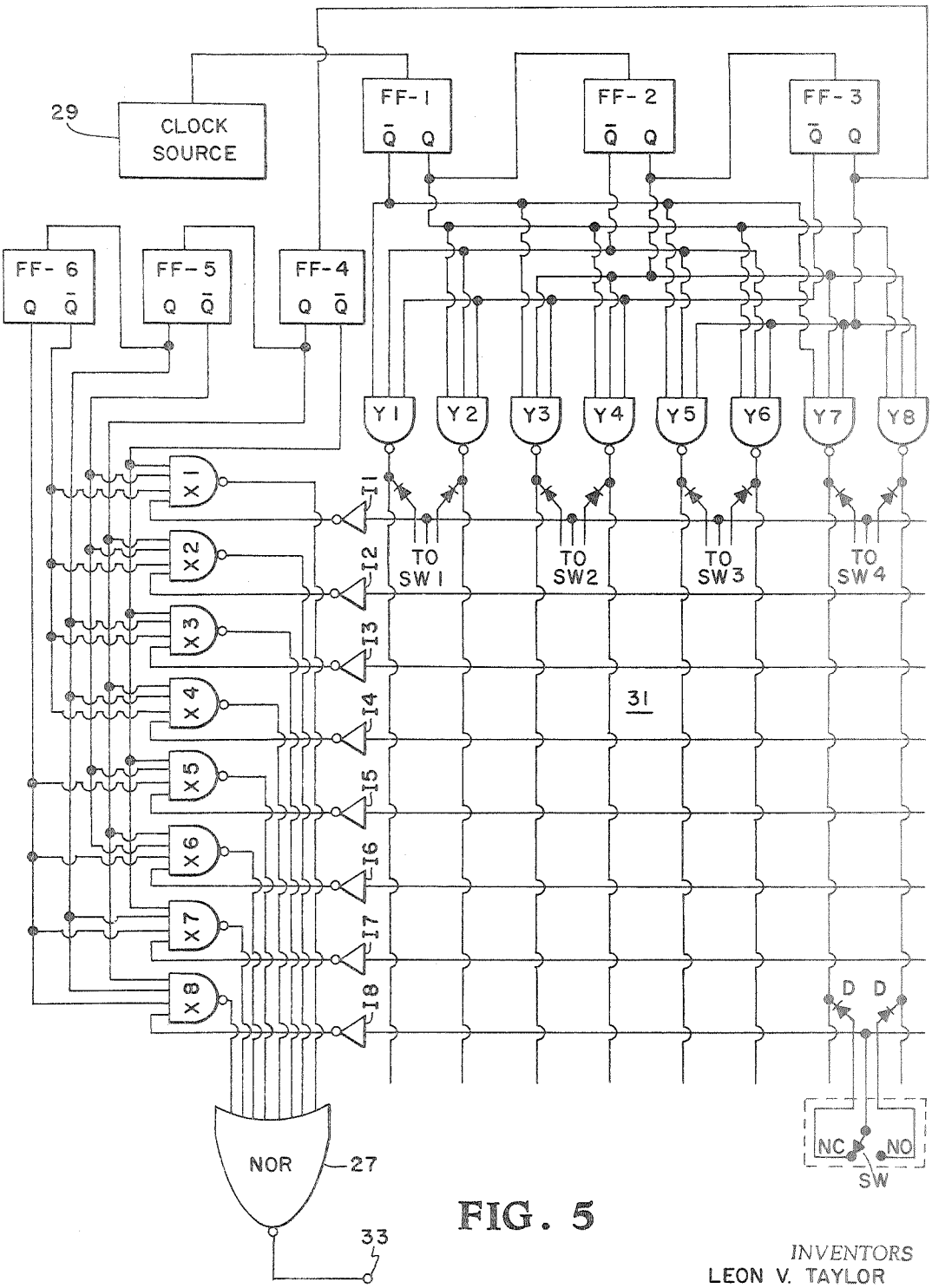

FIG. 5

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United States Patent

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[21] Appl. No. **668,242**
[22] Filed **Sept. 15, 1967**
[45] Patented **Mar. 23, 1971**

[73] Assignee **The United States of America as represented by the Administrator of the National Aeronautics and Space Administration**

[54] **PLURAL POSITION SWITCH STATUS AND OPERATIVENESS CHECKER**
4 Claims, 6 Drawing Figs.

[52] **U.S. Cl.** **340/166,** 340/150, 340/164, 340/213, 340/403
[51] **Int. Cl.** **H04g 1/00,** H04g 3/00, H04g 5/00
[50] **Field of Search** 340/166, 164, 150, 213, 403

[56] References Cited

UNITED STATES PATENTS

3,201,768	8/1965	Merz	340/166C
3,275,992	9/1966	Neumann	340/166C
3,327,290	6/1967	English	340/164X
3,387,264	6/1968	Budny	340/164X
3,012,240	12/1961	Klahn	340/166C
3,035,248	5/1962	Grose et al.	340/150X
3,205,486	9/1965	Crowley	340/413
3,391,305	7/1968	Bradwin	340/166X
3,475,750	10/1969	Howell	340/213X

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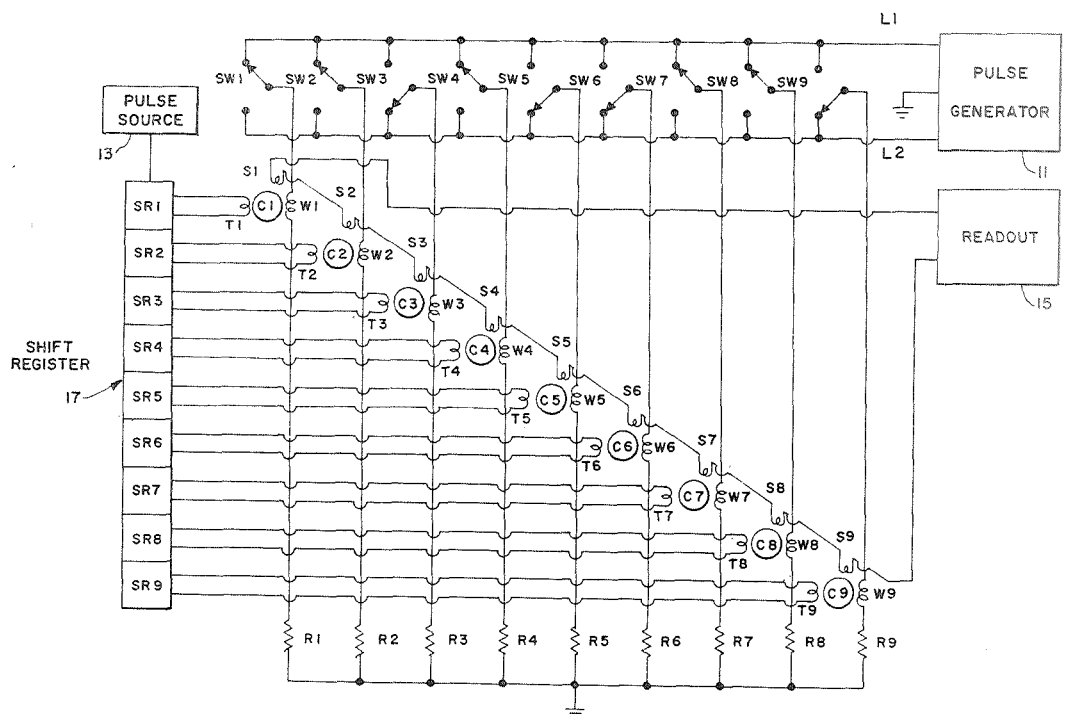
ABSTRACT: This invention is an apparatus for checking the status of a plurality of switches. In one embodiment, a matrix of magnetic cores are connected to the common terminals of a plurality of double-throw switches. A pulse is then applied to the normally closed side of the switches. This pulse energizes any of the cores that are connected to switches that are in the normally closed position. The matrix of magnetic cores is then read out. Following this, a pulse is applied to the normally open side of the switches. This second pulse energizes any of the cores that are connected to switches that are in the normally open position and the matrix is again read out. The readouts are then compared. If the readouts for any particular switch are complements, the status of the switch can be identified. If the readouts for any particular switch are the same, a defective switch condition or a defective switch wiring condition is indicated. Hence, the status and operativeness of the switches are both determined by the invention.



PLURAL POSITION SWITCH STATUS AND OPERATIVENESS CHECKER

BACKGROUND OF THE INVENTION

Pluralities of switches are utilized in numerous environments. They are utilized in telegraphy- and telephony-switching systems and in electronic sensing systems. For example, a plurality of switches are used on a spacecraft to sense micrometeoroid penetration. That is, a micrometeoroid-sensing satellite has large wings or appendages that are deployed when the spacecraft is in space. These wings are separated into separate regions and each region has a pressure sensitive cell that operates a switch. When a particular region is penetrated by a micrometeoroid, the switch for that region moves from its normally closed position to its normally open position.

Cyclically scanning a large number of switches on a spacecraft presents a number of problems. Not only must the switches be scanned, but they must be checked to determine if either they are defective or if their associated wiring is defective. In addition, the scanning system must be relatively uncomplicated so that it is reliable over an extended period of time.

Prior-art apparatus for detecting the status of a plurality of switches include mechanical means, line drivers, analogue summators, pulse counters, and pulse scanners. However, each of these prior-art systems has certain disadvantages. Specifically, mechanical means utilize a stepper switch or a relay matrix to form a scanning system and these devices are inherently unreliable and unable to withstand extreme environments such as the vibrations that occur when a spacecraft is launched into space.

Line drivers utilize flip-flops and a gating tree to sequentially generate pulses on a number of lines. The number of lines is equal to the number of switches being scanned; hence, one disadvantage of a line driver system is that for a large number of switches the gating tree places an unreasonable load on the driving flip-flops.

Analogue summators utilize voltage-dividing resistive networks. Individual resistors are shorted by switches to provide voltage changes and these changes are summed to provide an analogue signal. This summation of signals requires an analog-to-digital conversion to convert the signal prior to transmission from the spacecraft to a ground station. In addition, this system needs a multiplexer when more than 100 switches are involved. Hence, analogue summators are relatively complex.

Pulse counters count pulses each time a switch is closed. They are susceptible to transient noise pulses and there is no known way of rescanning the switches to eliminate the effects of noise.

Pulse scanners scan each switch and generate a pulse for each closed switch and store a total count equal to the number of closed switches. Pulse scanners do not permit the identification of individual switches and, to that extent, are unsatisfactory for use on a spacecraft.

From the foregoing, it will be appreciated that while there are numerous prior-art methods of scanning a plurality of switches, each of them has certain disadvantages which make them undesirable for scanning a large number of switches located in an extreme environment such as on a spacecraft, for example.

Therefore, it is an object of this invention to provide a new and improved apparatus for scanning a plurality of switches.

It is also an object of this invention to provide a new and improved apparatus for scanning a large plurality of switches that is reliable and suitable for use in an extreme environment.

It is another object of this invention to provide a new and improved switch scanning apparatus that scans a plurality of switches to determine their status and the status of their associated wiring thereby determining if they are operative.

It is a further object of this invention to provide a new and improved switch scanning apparatus that is simple and reliable and utilizes a minimum number of wires to connect the switches to the scanning apparatus.

SUMMARY OF THE INVENTION

In accordance with a principle of this invention, an apparatus for checking the status of a plurality of switches is provided. A sensing means for sensing the status of the switches is connected to the switches and an energizing means for selectively energizing the switches is also connected to the switches. The switches are selectively energized by the energizing means and their condition or status is sensed by the sensing means. The sensing means provides an indication of the status of the switches.

In accordance with another principle of this invention, the sensing means is a matrix of magnetizable cores which are connected to the common terminals of the switches. The energizing means is a pulse generator that is connected to both the normally closed and normally open contacts of the switches. When the pulse generator pulses the switches, the magnetic cores are selectively energized and their condition is subsequently read out by an appropriate readout means.

In accordance with a further principle of this invention, first the normally closed side of the switches and then the normally open side of the switches are energized. A first readout occurs after the energization of the normally closed side of the switches. A second readout occurs after energization of the normally open side of the switches and the two readouts are compared. When both readouts for any particular switch are the same, that switch and/or its associated wiring is defective. When the data for both readouts for any particular switch are complements, the status of the switch is determined.

In accordance with yet another principle of this invention, the sensing means may be a solid state matrix. The matrix is selectively energized and readout to detect and indicate the status and operativeness of the switches.

It will be appreciated that the invention provides a novel apparatus for checking the status of a plurality of switches. While the apparatus is useful for checking the status of a small number of switches, it becomes increasingly useful as the number of switches increases. The use of either a magnetic matrix or a solid state matrix substantially decreases the number of connecting wires necessary to check the status of the switches. Hence, the overall system is both uncomplicated and reliable.

It will also be appreciated that while the invention as herein described has particular utility in extreme environments, such as on a spacecraft for example, it can also be used in other environments. Generally, the invention is useful in any environment where the status of a large number of switches must be determined or where the presence of defective switches must be determined.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing object and many of the attendant advantages of this invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description when taken in conjunction with the accompanying drawings wherein:

FIG. 1 is a partially block and partially schematic diagram of one embodiment of the invention;

FIG. 2 is a waveform diagram of the readout for the embodiment of the invention illustrated in FIG. 1;

FIG. 3 is a partially schematic and partially block diagram of an alternate embodiment of the invention;

FIG. 4 is a waveform diagram of the readout of the embodiment illustrated in FIG. 3;

FIG. 5 is a logic diagram of a further embodiment of the invention; and

FIG. 6 is a variation of the embodiment illustrated in FIG. 5.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 is a partially schematic and partially block diagram of an embodiment of the invention utilizing a matrix of magnetizable core elements. The embodiment illustrated in FIG. 1 comprises: nine switches designated SW–1 to SW–9; nine magnetic core elements designated C–1 to C–9; nine core set windings designated W–1 to W–9; nine core interrogate windings designated T–1 to T–9; nine core sense windings designated S–1 to S–9; nine resistors designated R–1 to R–1 two lines designated L–1 and L–2; a pulse generator 11; a pulse source 13; and, a readout system comprising an address shift register 17 having nine stages designated SR–1 to SR–9 and a sensing circuit 15. Each switch is illustrated as a single-pole double-throw switch. For ease of discussion, the lower terminals of the switch are hereinafter designated the normally open (NO) terminals and the upper terminals are designated the normally closed (NC) terminals. The center terminals are designated the common terminals.

The pulse generator 11 has two outputs and a ground connection. One output of the pulse generator is connected by L–1 to the NC terminals of the nine switches and the second output is connected by L–2 to the NO terminals of the switches.

The common terminal of SW–1 is connected through W–1 in series with R–1 to ground. The common terminal of SW–2 is connected through W–2 in series with R–2 to ground and the common terminal of SW–3 is connected through W–3 in series with R-3 to ground. Similarly, the common terminal of SW–4 is connected through W–4 in series with R–4 to ground and the common terminal of SW–5 is connected through W–5 and R–5 to ground. The common terminal of SW–6 is connected through W–6 and R–6 to ground and the common terminal of SW–7 is connected through W–7 and R–7 to ground. Finally, the common terminal of SW–8 is connected through W–8 in series with R–8 to ground and the common terminal of SW–9 is connected through the series combination of W–9 and R–9 to ground.

The nine sense windings, S–1 to S–9, are connected in series to the input of the sensing circuit 15.

The pulse source 13 has its output connected to the input of the address shift register 17. The output of SR–1 is connected to T–1, the output of SR–2 is connected to T–2 and the output of SR–3 is connected to T–3. The output of SR–4 is connected to T–4, the output of SR–5 is connected to T–5 and the output of SR–6 is connected to T–6. Finally, the output of SR–7 is connected to T–7, the output of SR–8 is connected to T–8 and the output of SR–9 is connected to T–9.

At this point, it should be noted that the address system for reading out the information contained in the cores comprising the address shift register 17, the pulse source 13 and the sensing circuit 15 connected as described above and operative in the manner hereinafter described is merely by way of example. There are numerous other apparatus well known to those skilled in the art for serially reading out data from a core matrix. And, that apparatus can be used in lieu of the apparatus illustrated in FIG. 1 depending, of course, upon how the cores are energized.

Switches SW–1, SW–2, SW–4, SW–7 and SW–8 are indicated in FIG. 1 as having their common terminals connected to their normally closed terminals. Switches SW–3, SW–5, SW–6 and SW–9 are illustrated in FIG. 1 as having common terminals connected to their normally open terminals.

To clarify the following discussion, two terms are defined: (a) "set" implies going to a logical 1 state; and (b) "reset" implies going to a logical 0 state.

The embodiment of the invention illustrated in FIG. 1 operates as follows. The pulse generator 11 applies the first pulse along L–1. The first pulse sets all of the cores that are connected to switches that are in their normally closed positions. Specifically, with the switch configuration illustrated in FIG. 1, the circuits of set windings W–1, W–2, W–4, W–7 and W–8 are completed to set the cores C–1, C–2, C–4, C–7 and C–8. After the first pulse, the cores are read out by the readout system and their logical states are determined.

The readout operation occurs as follows. After the occurrence of the pulse on L–1, pulse source 13 is energized. Pulse source 13 sequentially applies pulses to the shift register 17 so that each state of the shift register sequentially operates. That is, the first stage, SR–1 generates an output pulse upon the occurrence of the first pulse from the pulse source 13, the second state SR–2 generates an output pulse upon the occurrence of the second pulse from the pulse source 13 and so on through the nine stages of the shift register.

When SR–1 generates an output pulse, it resets core C–1. Specifically, because W–1 had previously set C–1, a pulse is induced on the sense winding S–1 due to the transition of C–1 from the set to the reset state. However, if W–1 had previously not set C–1, a pulse would not be induced on S–1 because the core was already in the reset state and no transition would occur. Hence, when SR–1 generates a pulse, the sense winding S–1 generates an output pulse, i.e., it generates a 1, and applies it to the sense circuit 15. A similar situation occurs for sense winding S–2 because W–2 had previously set it. However, W–3 has not set C–3 because SR–3 is not in its normally closed position. Hence, when SR–3 generates an output pulse, it does not cause a transition of core C–3 and S–3 does not generate an output pulse. Rather, S–3 generates a 0 during this readout. This serial readout occurs through the nine stages of the shift register for the nine cores to generate a complete readout waveform of the type illustrated on the line entitled FIRST READOUT of FIG. 2. That is, sense windings S–1, S–2, S–4, S–7 and S–8 generate 1's while sense windings S–3, S–5, S–6 and S–9 generate 0's. Hence, the waveform of the serial readout is identical to the setting of the nine switches.

As a result of the first readout, all cores have been reset to a 0 state. Thereafter, the pulse generator 11 applies a pulse to L–2. This second pulse sets all of the cores that are connected to switches that are in their normally opened position. That is, cores C–3, C–5, C–6 and C–9 are set by the second pulse. After the second pulse sets these cores, the pulse source 13, the address shift register 17 and the sensing circuit 15 perform a second readout in the same manner as the first readout is performed. The second readout is illustrated in FIG. 2 on the SECOND READOUT line. Specifically, sense windings S–3, S–5, S–6 and S–9 generate 1's and sense windings S–1, S–2, S 4, S–7 and S–8 generate 0's.

It will be appreciated that the second readout should be the complement of the first readout if all of the switches and the wiring of the switches are operative. These first and second readouts can be compared by any suitable comparison means to determine if they are exact complements. For the embodiment illustrated in FIG. 1, as illustrated by the waveforms of FIG. 2, the readouts are exact complements. However, if one of the switches was defective either because it set a core for each readout or because it did not set a core for either readout, the waveform readouts would not be exact complements. And, the position of the noncomplementary condition in the waveforms designates which switch is inoperative. Hence, the invention, in addition to checking the status of the switches, also detects inoperative switches and switch wiring.

It will be appreciated that the system illustrated in FIG. 1 provides an uncomplicated and reliable means for checking the status of a plurality of switches. A pulse generator sequentially applies pulses to two limes—one line is connected to the normally open terminals of the switches and the second line is connected to the normally closed terminals. The common terminals of the switches are separately connected to magnetic cores. One group of magnetic cores are set when the first pulse occurs; thereafter, the cores are read out. Following the first readout the second pulse occurs. The second pulse sets the remaining cores and a second readout occurs. The two readouts are then compared to determine if any of the switches are defective.

While the embodiment illustrated in FIG. 1 only discloses use of the invention illustrated in FIG. 1 as hereinabove

described is merely by way of example. The invention can be utilized with a small number of switches, such as nine or with a large number such as 1,000, for example.

It will be appreciated, that the operation of the embodiment of the invention illustrated in FIG. 1 as hereinabove described is merely by way of example. Alternatively, a positive pulse could be applied to L–1 while a negative pulse is applied to L–2. All cores connected to switches in the NC position are then set to 1 state while all cores connected to switches in the NO position are reset to the 0 state. The core plane is then read out by any conventional technique. Thereafter, a positive pulse is applied to L–2 and a negative pulse is applied to L–1. All cores connected to switches in the NO position are now set to the 1 state while all cores connected to NC switches are reset to the 0 state. Thereafter, the core plane is again read out. As hereinabove described, the readouts can then be compared by any conventional means to determine the status of the switches. If the compared bits are not complementary, an operative switch condition or an inoperative switch wiring condition is indicated.

FIG. 3 illustrates an alternative embodiment of the invention that comprises: four switches designated SW–10 to SW–13; eight magnetic cores designated C–10 to C–17; eight resistors designated R–10 to R-17; eight set windings designated W–10 to W–17; eight interrogate windings designated T–10 to T–17; eight sense windings designated S–10 to S–17; a line designated L; a pulse generator 19; a pulse source 21; an address shift register 23; and a sensing circuit 25. The shift register 23 has eight stages designated SR–10 to SR–17. The switches are single-pole double-throw switches and for purposes of discussion the normally closed terminals are on the left and the normally open terminals are on the right.

The common terminals of all of the switches are connected by the line L to the pulse generator 19. The normally closed terminal of SW–10 is connected through W–10 in series with R–10 to ground the normally open terminal of SW–10 is connected through W–11 in series with R–11 to ground. The normally closed terminals of SW–11 is connected through W–12 in series with R–12 to ground and the normally open terminal of SW–11 is connected through W–13 in series with R–13 to ground. Similarly, the normally closed terminal of SW–12 is connected through W–14 in series with R–4 to ground and the normally open terminal of SW–12 is connected through W-15 in series with R–15 to ground. Finally, the normally closed terminal of SW–13 is connected through W-16 in series with R–16 to ground and the normally open terminal of SW–13 is connected through W–17 in series with R–7 to ground. S–10 through S–17 are connected in series and to the sensing circuit 25.

The output of the pulse source 21 is connected to the address shift register 23. SR–10 is connected to T–10, SR–22 is connected to T–11, and SR–12 is connected to T–12. SR–13 is connected to T–13, SR–14 is connected to T–14 and SR–15 is connected to T–15. Finally, SR–16 is connected to T–16 and SR–17 is connected to T–17.

SW–10 has its common terminal connected to its normally closed terminal, SW–11 has its common terminal connected to its normally open terminal, and SW–13 has its common terminal connected to its normally open terminal, and SW–13 has its common terminal connected to its normally closed terminal.

The embodiment illustrated in FIG. 3 operates similarly to the embodiment illustrated in FIG. 1 except that there is only one pulse energization and only one readout. Specifically, line L is pulsed by the pulse generator and sets all cores that form a complete circuit. More specifically, core C–10 is set because it is connected to the normally closed side of SW–10 and because SW–10 is in its normally closed position, similarly, SW–11 causes C–13 to be set, SW–1 2 causes C–15 to the set and SW–13 causes C–16 to be set, cores C–11, C–12, C–14 and C–17 are not set and remain in a reset state because the sides of the switches to which these cores are connected are open. The cores are now read out in a manner similar to the readout of the cores of FIG. 1; that is, the pulse source 21 generates a series of pulses that sequentially operate the shift register. And, the readout occurs during this sequential operation.

The readout for the switch setting of the embodiment illustrated in FIG. 3 is illustrated by the waveform of FIG. 4. A completed circuit is readout as a 1 and an open circuit is readout as a 0. The first two sections of the wave, S–10 and S–11, are the status of SW–10, the second two sections, S–12 and S–13, are the status of SW–11, the third two sections, S–14 and S–15, are the status of SW–12 and the fourth two sections, S–16 and S–17, are the status of SW–13. The first half of each section is the status of the normally closed terminals and the second half is the status of the normally open terminal.

In addition to checking the status of the switches, the waveform of FIG. 4 can be used by an appropriate electronic circuit to determine if any of the switches or their associated wiring are defective. That is, each switch must have a 1 section and a 0 section in the readout. If the readout for a switch is 0 for both sections, it designates that the switch is completely open, i.e., the common terminal is not in contact with either the normally closed or the normally open side. Or, if the readout is 1 for both sections, it indicates that the switch is shorted between all three terminals. Hence, the waveform of the embodiment of the invention illustrated in FIG. 3 determines both the status and the operativeness of the switches.

FIG. 5 illustrates a second alternative embodiment of the invention wherein a solid state matrix is utilized to scan the switches to determine their status. The embodiment illustrated in FIG. 5 comprises: six flip-flops designated FF–1 to FF–6; eight Y–axis NAND gates designated Y–1 to Y–8; eight X–1 axis NAND gates designated X–1 to X–8; eight inverters designated I–1 to I–8; a NOR gate 27; and a clock source 29. Each flip-flop has a true output designated Q and a false output designated $\overline{Q}$. Each Y–axis NAND gate has three inputs and each X–axis NAND gate has four inputs. The NOR gate 27 has eight inputs.

The clock source 29 is connected to the trigger input of FF–1. The $\overline{Q}$ output of FF–1 is connected to one input of Y–1, Y–3, Y–5 and Y–7. The Q output of FF–1 is connected to one input of Y–2, Y–4, Y–6 and Y–8 and to the trigger input of FF–2.

The $\overline{Q}$ output of FF–2 is connected to one input of Y–1, Y–2, Y–5 and Y–6. The Q output of FF–2 is connected to one input of Y–3, Y–4, Y–7, Y–8 and to the trigger input of FF–3. The $\overline{Q}$ output of FF–3 is connected to one input of Y–1, Y–2 Y–3 and Y–4. The Q output of FF–3 is connected to one input of Y–5, Y–6, Y–7, Y–8 and to the trigger input of FF–4.

The $\overline{Q}$ output of FF–4 is connected to one input of X–1, X–3, X–5 and X–7. The Q output of FF–4 is connected to input of X–2, X–4, X–6, X–8 and to the trigger input of FF–5. The $\overline{Q}$ output of FF–5 is connected to one input of X–1, X–2, X–5 and X–6 and the Q output of FF–8 is connected to one input of X–3, X–4, X–7 X–8 and to the trigger input of FF–6. The $\overline{Q}$ output of FF–6 is connected to one input of X–1, X–2, X–3 and X–4 and the Q output of FF–6 is connected to one input of X–5, X–6, X–7 and X–8.

The outputs of Y-axis NAND gates are connected to the vertical lines of a matrix arrangement 31 illustrated in FIG. 5 from left to right for Y–1 to Y–8, respectively. And, the inputs of I–1 to I–8 are connected to the horizontal lines of the matrix from top to bottom, respectively.

The output of I–1 is connected to one input of X–1, the output of I–2 is connected to one input of X–2 and the output of I–3 is connected to one input of X–3. The output of I–4 is connected to one input of X–4, the output of I–5 is connected to one input of X–5 and the output of I–6 is connected to one input of X–6. Finally, the output of I–7 is connected to one input of X–7 and the output of I–8 is connected to one input of X–8. The eight outputs of X–1 to X–8 are connected to the eight inputs of the NOR gate 27. The output of the NOR gate 27 is connected to an output terminal 33.

Each vertical line of the matrix is connected to the cathodes of eight diodes designated D. Each horizontal line of the matrix is connected to the common terminal of four switches. Further, the anodes of the diodes are connected to the sides of the switches. For ease of illustration only one diode matrix switch connection is illustrated in FIG. 5, that connection being shown at the lower right-hand side of the FIG.

From the foregoing description of the circuit connections of FIG. 5, it will be appreciated that the flip-flops comprise a ripple counter wherein the first three flip-flops operate the vertical lines of the matrix and the second three flip-flops operate the horizontal lines of the matrix. Because of this arrangement, all of the Y NAND gates are sequentially operated before the device switches from one X NAND gate to a second X NAND gate. Specifically, all of the vertical lines are scanned for one horizontal line before a second horizontal line is scanned.

Turning now to a description of the operation of the embodiment of the invention illustrated in FIG. 5, assume that the first two diodes in the upper left-hand corner are connected to switch S–1, and assume that S–1 is in the configuration of the switch illustrated in the switch in the lower right-hand corner of the matrix. That is, the normally closed contacts are closed and normally open contacts are open. The first clock pulse triggers FF–1 and creates a condition where all of the inputs to Y–1 are energized, i.e., Y–1 is turned on. In addition, X–1 has all of its inputs except the input from I–1 energized. Now, when Y–1 passes the first pulse, it continues to pass through I–1, X–1 and the NOR gate because the normally closed side of the switch is closed.

A second pulse from the clock source turns Y–1 off and Y–2 on. However, no pulse passes through I–1 and X–1 because the normally open side of the switch is open. The third pulse energizes Y–3 to check the normally closed side of S–2; if that side is closed, X–1 passes a pulse and if it is open, X–1 does not pass a pulse. Thereafter, Y–4 is energized and so on through Y–8. After Y-8 has been energized, the ripple counter arrangement triggers FF–4 so that X–2 is made operative and X–1 is made inoperative. Thereafter, Y–1 to Y–8 are sequentially operated to scan the second horizontal line of the X–axis. In this manner, each X–axis or horizontal line is sequentially scanned with a sequential or vertical Y–axis scan occuring for each line. The diodes are included to prevent ambiguous data paths from existing in the matrix-switch wiring.

The output from the system illustrated in FIG. 5 can be electronically checked to determine if any of the switches are defective. That is, the waveform of the output will be similar to the waveform illustrated in FIG. 4. Hence, by sequentially testing the first and second outputs for each switch, the existence and location of defective switches can be determined. That is, if two 0's occur for a particular switch or two 1's occur, a defective switch is indicated. Consequently, the matrix arrangement of FIG. 5 operates in a manner similar to the magnetic core arrangements of FIGS. 1 and 3 to scan a plurality of switches to determine both their status and their operativeness.

FIG. 6 illustrates a slight modification of the embodiment of the invention illustrated in FIG. 5. Specifically, FIG. 6 illustrates a switch connection wherein a single diode is utilized with each switch. That is, the NC side of the NO side of the switches are directly connected to the Y lines of a matrix and a diode D is connected between the common terminals of the switch and the X line. As discussed above, the modification illustrated in FIG. 6 utilizes the diode in the same manner as the embodiment illustrated in FIG. 5; that is, the diode prevents ambiguous data passage through the matrix-switch wiring.

It will be appreciated that the invention has numerous advantages over the prior art. It has the ability to rescan switches, to identify individual switches and to reduce the effect of transient noise as well as to maintain a history of switch status. All these functions can be easily accomplished by applying the output from the scanning devices to suitable electronic means.

The invention also has the ability to detect the abnormal operation of the switches. In addition, the invention utilizes a minimum number of sensing wires to connect the various switches to magnetic or solid state matrices. This minimum connection results in a considerable weight and cost savings in large systems. Further, if it is not desired to detect defective switches the status checking capacity of all embodiments can be doubled. For example, 18 rather than nine switches can be status checked by the FIG. 1 embodiment if only the status of one side of each switch is sensed.

It will also be appreciated that while the invention has been illustrated as connected to only a small number of switches, it can be utilized with a large number of switches. In fact, the benefits of the invention become much greater when it is used with a large rather than a small number of switches.

It will further be appreciated that the invention can be varied in numerous ways. The inventive embodiments illustrated in FIGS. 1 and 2 describe two types of core arrangements for connection to switches; however, other types of core arrangements and connections can also be utilized. Moreover, the sensing arrangement can be utilized with other than single-pole, double-throw switches. Hence, the invention can be practiced other than as specifically described herein.

I claim:

1. Apparatus for checking the status of the positions of a plurality of multiple-position switches and for locating open and short circuits in the switches, said switches each having a common terminal, another terminal for each of its positions and an armature connected to said common terminal which can be selectively positioned to contact either of said another terminals comprising:

a plurality of magnetic pulse sensing means with each including first and second inputs and an output on which a pulse is produced when a pulse is applied to said second input only if a pulse has previously been applied to said first input;

said first input of each of said plurality of magnetic pulse sensing means connected in an electrical circuit with one terminal of one of said plurality of switches;

means for applying pulses to corresponding terminals of said plurality of switches other than said one terminal;

scanning means for successively applying pulses to the second inputs of said plurality of magnetic pulse sensing means after each pulse is applied to said first inputs of said magnetic pulse sensing means; and

means synchronous with said scanning means and to the pulse waveform from said magnetic pulse sensing means for determining which of said outputs of said magnetic pulse sensing means produce a pulse when a pulse is applied to its second input.

2. Apparatus according to claim 1 wherein said one terminal is said common terminal.

3. Apparatus according to claim 1 wherein said one terminal is one of said another terminals and said corresponding terminals of said plurality of switches other than said one terminal is said terminal.

4. Apparatus for checking the status of the position of a plurality of multiple-position switches arranged in a matrix and for locating open and short circuits in the switches said switches each having a common terminal, another terminal for each of its positions and an armature connected to said common terminal which can be selectively positioned to contact either of said another terminals comprising:

a plurality of logic circuit means with each associated with a different row in said matrix and with each connected to receive one input from all of said common terminals in its corresponding row, each of said logic circuit means producing a predetermined signal if and only if said predetermined signal is applied to said one input and all of its other inputs have another signal applied to them;

means for successively applying said another signal to said plurality of logic circuit means said another signal being applied simultaneously to all inputs other than said one; and

means for successively applying said predetermined signal to all of said another terminals of the switches in each column of said matrix each time and while said another signal is being applied to said logic circuit means whereby the outputs of said logic circuit means are indicative of the status of the positions of said switches and of the open and short circuits in said switches.