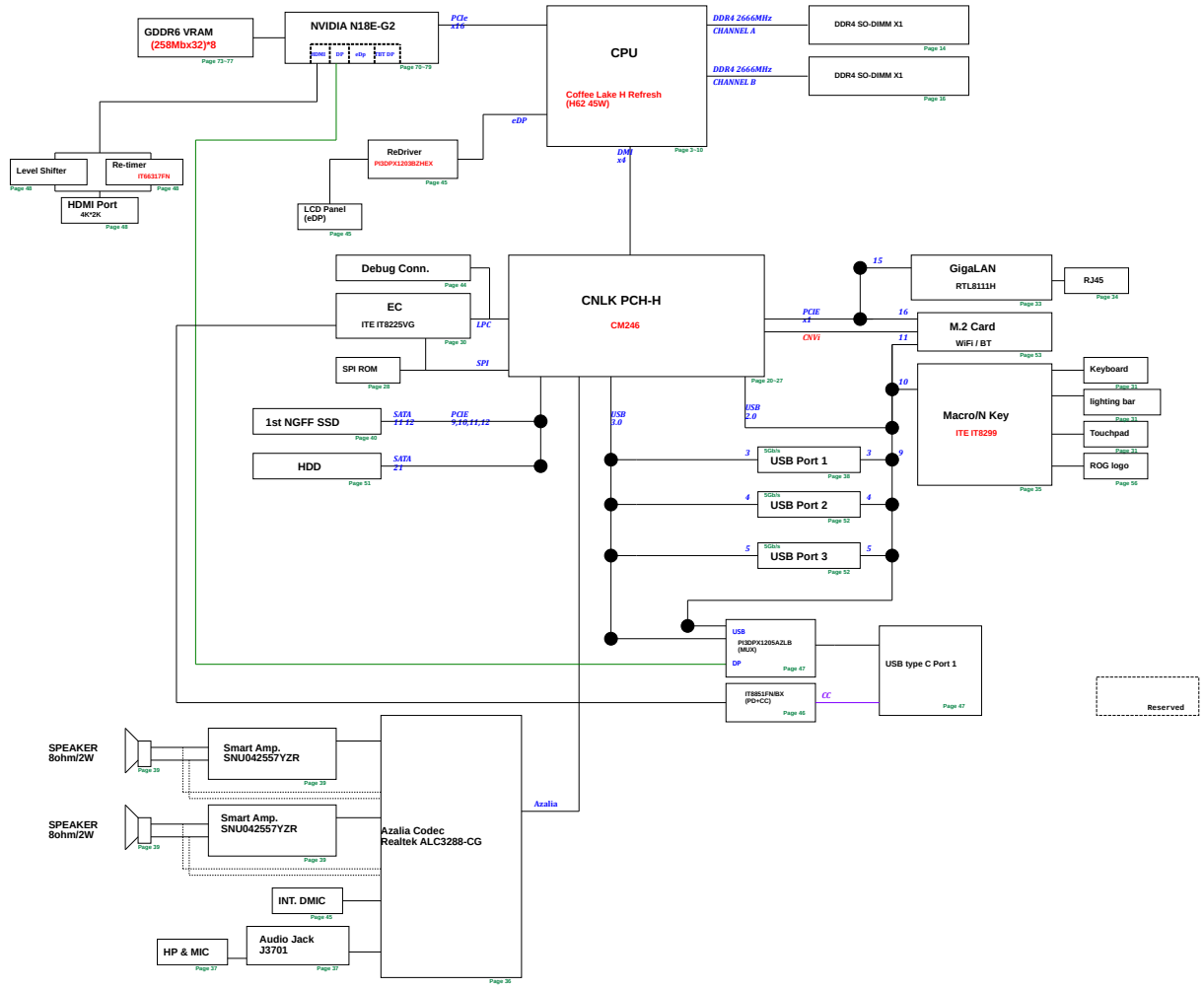
G531GW Block Diagram

Coffee Lake H Refresh Platform



Project Name	G711GW
Rev	91.1
Title :	Block Diagram
Size	D
Dept.	ASUSTeK COMPUTER
Engineer	Gaming RD
Date	Tuesday, April 16, 2019
Sheet	1 of 103

PCH_CPU GPIO

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_A0	RCIN#	Native	RC_IN#		PU 10K	+3VS
GPP_A1	LAD0	Native	LPC_AD0			
GPP_A2	LAD1	Native	LPC_AD1			
GPP_A3	LAD2	Native	LPC_AD2			
GPP_A4	LAD3	Native	LPC_AD3			
GPP_A5	LFRAME#	Native	LPC_FRAME#			
GPP_A6	SERIRQ	Native	INT_SERIRQ		PU 10K	+3VS
GPP_A7	PIRQA#	Native	PCI_INTA#		PU 10K	+3VS
GPP_A8	CLKRUN#	Native	PM_CLKRUN#		PU 8.2K	+3VS
GPP_A9	CLKOUT_LPC0	Native	CLK_KBCPCI_PCH_X1			
GPP_A10	CLKOUT_LPC1	Native	CLK_DEBUG_X1			
GPP_A11	PME#	Native	PCI_PME#			
GPP_A12	GPI	GPI	PCH_GPP_A12			
GPP_A13	SUSWARN#/	Native	PE_SusPwrDnAck		PU 10K(@)	+3VSUS
GPP_A14	SUS_STAT#	Native	PCH_SUS_STAT#			
GPP_A15	SUS_ACK#	Native	PM_SUSACK#			
GPP_A16	Native/GPI	GPI	GPP_A16			
GPP_A17	GPI	GPI	(N.C)			
GPP_A18	GPI	GPI	(N.C)			
GPP_A19	GPI	GPI	(N.C)			
GPP_A20	GPI	GPI	(N.C)			
GPP_A21	GPI	GPI	(N.C)			
GPP_A22	GPI	GPI	(N.C)			
GPP_A23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_B0	GPO	GPO	(N.C)			
GPP_B1	GPO	GPO	(N.C)			
GPP_B2	GPI	GPI	(N.C)			
GPP_B3	GPI	GPI	(N.C)			
GPP_B4	GPI	GPI	(N.C)			
GPP_B5	GPI	Native	CLK_PEGA_REQB#_X1		PU 10K	+3VSUS
GPP_B6	GPI	Native	CLK_REQ1#		PU 10K	+3VSUS
GPP_B7	GPI	Native	CLK_REQ2#		PU 10K	+3VSUS
GPP_B8	GPI	Native	CLKREQ3_WLAN#_X1		PU 10K	+3VSUS
GPP_B9	GPI	Native	CLKREQ4_GLAN#_X1		PU 10K	+3VSUS
GPP_B10	GPI	Native	CLKREQ5_TBT#_X1		PU 10K	+3VSUS
GPP_B11	GPO	GPO	MPHY_PWREN		PU 10K	+3VSUS
GPP_B12	SLP_S0#	Native	SLP_S0#			
GPP_B13	PLTRST#	Native	PLT_RST#			
GPP_B14	GPO	Strap	PCH_GPP814	PD		
GPP_B15	GPI	Native	GSPI0_CS#			
GPP_B16	GPI	Native	GSPI0_CLK			
GPP_B17	GPI	Native	GSPI0_MISO			
GPP_B18	GPO	Strap	PCH_GPP818	PD		
GPP_B19	GPI	GPO	PCH_GPP819/BT_ON_PCH		PD 10K(@)	
GPP_B20	GPI	GPO	PCH_GPP820/NV_GPU_EVENT#		PU 10K(@)	+3VSUS
GPP_B21	GPI	GPI	PCH_GPP821/NV_GC6_FB_EN		PU 10K(@)	+3VS
GPP_B22	GPO	Strap	PCH_GPP822	PD		
GPP_B23	GPO	GPO	SMLALERT#	PD	PU 150K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_C0	SMBCLK	Native	SMB_CLK		PU 2.2K	+3VSUS
GPP_C1	SMBDATA	Native	SMB_SDA		PU 2.2K	+3VSUS
GPP_C2	GPO	Strap	PCH_GPPC2			
GPP_C3	SMLOCLK	Native	SML0_CLK		PU 2.2K	+3VSUS
GPP_C4	SMLODATA	Native	SML0_DAT		PU 2.2K	+3VSUS
GPP_C5	GPO	Strap	PCH_GPPC5	PD		
GPP_C6	GPI	Native	SML1_CLK		PU 2.2K	+3VSUS
GPP_C7	GPI	Native	SML1_DAT		PU 2.2K	+3VSUS
GPP_C8	GPI	GPI	PCH_GPPC8			
GPP_C9	GPI	GPI	PCH_GPPC9			
GPP_C10	GPI	GPI	PCH_GPPC10			
GPP_C11	GPI	GPI	PCH_GPPC11			
GPP_C12	GPI	GPI	DIMM_SEL0		PD 10K	
GPP_C13	GPI	GPI	DIMM_SEL1		PD 10K	
GPP_C14	GPI	GPI	DIMM_SEL2		PD 10K	
GPP_C15	GPI	GPI	NFC_ID		PU 10K	+3VSUS
GPP_C16	GPI	GPO	ADAC_WLANLED		PU 10K(@)	+3VSUS
GPP_C17	GPI	GPO	PCH_GPPC17		PU 10K(@)	+3VS
GPP_C18	GPI	Native	I2C1_SDA		PU 2.2K	+3VS
GPP_C19	GPI	Native	I2C1_SCL		PU 2.2K	+3VS
GPP_C20	GPI	GPI	PCH_GPPC20/DGPU_PWROK		PD 10K(@)	
GPP_C21	GPI	GPO	PCH_GPPC21/GPU_RST#		PD 10K	
GPP_C22	GPI	GPO	PCH_GPPC22/DGPU_PWR_EN#		PD 1K	
GPP_C23	GPI	GPI	CPAD_INT#		PU 10K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_D0	GPI	GPI	CIO_PLUG_EVENT		PU 10K	+VCC3V3_Sx
GPP_D1	GPO	GPIO	GPIO_3_FORCE_PWR		PD 10K	
GPP_D2	GPI	GPI	EXT_SMI#		PU 10K	+3VS
GPP_D3	GPI	GPI	EXT_SCI#		PU 10K	+3VS
GPP_D4	GPI	GPI	(N.C)			
GPP_D5	GPI	GPI	(N.C)			
GPP_D6	GPI	GPI	(N.C)			
GPP_D7	GPI	GPO	WLAN_ON#			
GPP_D8	GPI	GPI	(N.C)			
GPP_D9	GPI	Strap	PCB_ID0		PD 10K	
GPP_D10	GPI	Strap	PCB_ID1		PD 10K	
GPP_D11	GPI	Strap	TOUCHPAD_ID			
GPP_D12	GPI	Strap	TOUCH_PANEL_ID			
GPP_D13	GPI	GPI	PCH_GPP_D13		PU 10K(@)	+3VSUS
GPP_D14	GPI	GPO	PCH_GPP_D14/WLAN_LED		PD 100K	
GPP_D15	GPI	GPO	PCH_GPP_D15/WLAN_BT_LED		PD 100K	
GPP_D16	GPI	GPI	(N.C)			
GPP_D17	GPI	GPI	(N.C)			
GPP_D18	GPI	GPI	(N.C)			
GPP_D19	GPI	GPI	(N.C)			
GPP_D20	GPI	GPI	(N.C)			
GPP_D21	GPI	GPO	LED_Record			
GPP_D22	GPI	GPI	(N.C)			
GPP_D23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_E0	GPI	GPI	SATAPCIE_DET0		PU 10K	+3VS
GPP_E1	GPI	GPI	SATAPCIE_DET1		PU 10K	+3VS
GPP_E2	GPI	GPI	SATAPCIE_DET2		PU 10K	+3VS
GPP_E3	GPI	GPI	(N.C)			
GPP_E4	GPI	Native	NGFF0_DEVSLP			
GPP_E5	GPI	Native	(N.C)			
GPP_E6	GPI	Native	NGFF2_DEVSLP			
GPP_E7	GPI	GPI	(N.C)			
GPP_E8	GPI	Native	SATA_LED#		PU 10K(@)	+3VS
GPP_E9	GPI	Native	USB_OC#0	PD	PU 10K	+3VSUS
GPP_E10	GPI	Native	USB_OC#1	PD	PU 10K	+3VSUS
GPP_E11	GPI	Native	USB_OC#2	PD	PU 10K	+3VSUS
GPP_E12	GPI	Native	USB_OC#3	PD	PU 10K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_F0	GPI	GPI	SATAPCIE_DET3		PU 10K	+3VS
GPP_F1	GPI	GPO	(N.C)			
GPP_F2	GPI	GPI	(N.C)			
GPP_F3	GPI	GPI	(N.C)			
GPP_F4	GPI	GPI	(N.C)			
GPP_F5	GPI	Native	(N.C)			
GPP_F6	GPI	Native	(N.C)			
GPP_F7	GPI	GPI	(N.C)			
GPP_F8	GPI	GPI	(N.C)			
GPP_F9	GPI	GPI	(N.C)			
GPP_F10	GPI	GPI	(N.C)			
GPP_F11	GPI	GPI	(N.C)			
GPP_F12	GPI	GPI	(N.C)			
GPP_F13	GPI	GPI	(N.C)			
GPP_F14	GPI	GPI	(N.C)			
GPP_F15	GPI	Native	USB_OC#4		PU 10K	+3VSUS
GPP_F16	GPI	Native	USB_OC#5		PU 10K	+3VSUS
GPP_F17	GPI	Native	USB_OC#6		PU 10K	+3VSUS
GPP_F18	GPI	Native	USB_OC#7		PU 10K	+3VSUS
GPP_F19	GPI	Native	L_VDDEN_PCH_X1			
GPP_F20	GPI	Native	LCD_BACKEN_PCH_X1			
GPP_F21	GPI	Native	L_BKLTCTL_PCH_X1			
GPP_F22	GPI	GPI	(N.C)			
GPP_F23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_G0	GPI	GPI	(N.C)			
GPP_G1	GPI	GPO	SATA_ODD_PWRGT			
GPP_G2	GPI	GPI	SATA_ODD_DA#			
GPP_G3	GPI	GPI	(N.C)			
GPP_G4	GPI	GPI	(N.C)			
GPP_G5	GPI	GPI	(N.C)			
GPP_G6	GPI	GPI	(N.C)			
GPP_G7	GPI	GPI	(N.C)			
GPP_G8	FAN_PWM_0	Native	(N.C)			
GPP_G9	FAN_PWM_1	Native	(N.C)			
GPP_G10	FAN_PWM_2	Native	(N.C)			
GPP_G11	FAN_PWM_3	Native	(N.C)			
GPP_G12	GPI	GPI	(N.C)			
GPP_G13	GPI	GPI	(N.C)			
GPP_G14	GPI	GPI	(N.C)			
GPP_G15	GPI	GPI	(N.C)			
GPP_G16	GPI	GPI	(N.C)			
GPP_G17	GPI	GPI	(N.C)			
GPP_G18	GPI	GPI	PCH_GPP_G18			
GPP_G19	GPI	GPI	PCH_GPP_G19			
GPP_G20	GPI	GPI	(N.C)			
GPP_G21	GPI	GPI	(N.C)			
GPP_G22	GPI	GPI	(N.C)			
GPP_G23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_H0	GPI	Native	CLKREQ0_NGFF1#_X1		PU 10K	+3VSUS
GPP_H1	GPI	Native	CLKREQ7_USB31#_X1		PU 10K	+3VSUS
GPP_H2	GPI	Native	CLK_REQ8#		PU 10K	+3VSUS
GPP_H3	GPI	Native	CLK_REQ9#		PU 10K	+3VSUS
GPP_H4	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H5	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H6	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H7	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H8	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H9	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H10	GPI	GPI	(N.C)			
GPP_H11	GPI	GPI	(N.C)			
GPP_H12	GPO	GPO	(N.C)	PD		
GPP_H13	GPI	GPI	(N.C)			
GPP_H14	GPI	GPI	(N.C)			
GPP_H15	GPI	GPI	(N.C)			
GPP_H16	GPI	GPI	(N.C)			
GPP_H17	GPI	GPI	(N.C)			
GPP_H18	GPI	GPI	(N.C)			
GPP_H19	GPI	GPI	(N.C)			
GPP_H20	GPI	GPI	(N.C)			
GPP_H21	GPI	GPI	(N.C)			
GPP_H22	GPI	GPI	(N.C)			
GPP_H23	GPI	GPO	WLAN_WAKE_CTRL_CRB			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_I0	GPI	Native	(N.C)		PD 100K	
GPP_I1	GPI	Native	(N.C)		PD 100K	
GPP_I2	GPI	GPI	(N.C)			
GPP_I3	GPI	Native	(N.C)			
GPP_I4	GPI	Native	GPP_I4		PD 100K	
GPP_I5	GPI	Native	(N.C)		PU 2.2K	+3VS
GPP_I6	GPO	Native	(N.C)	PD	PU 2.2K	+3VS
GPP_I7	GPI	Native	(N.C)		PU 2.2K	+3VS
GPP_I8	GPO	Native	(N.C)	PD	PU 2.2K	+3VS
GPP_I9	GPI	Native	(N.C)		PU 2.2K(@)	+3VS
GPP_I10	GPO	Native	(N.C)	PD	PU 2.2K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPD0	BATLOW#	Native	PM_BATLOW#		PU 8.2K	+3VA_DSW
GPD1	ACPRESENT	Native	ME_AC_PRESENT_X1		PU 100K	+3VA_DSW
GPD2	LAN_WAKE#	Native	LAN_WAKE#		PU 10K	+3VA_DSW
GPD3	PWRBTN#	Native	PWRBTN#/PM_PWRBTN#		PU 10K(@)	+3VSUS
GPD4	SLP_S3#	Native	SLP_S3#/PM_SUSB#		PD 100K	
GPD5	SLP_S4#	Native	SLP_S4#/PM_SUSC#		PD 100K	
GPD6	SLP_A#	Native	SLP_A#			
GPD7	RSVD	GPO	(N.C)			
GPD8	SUSCLK	Native	SUS_CLK#/SUS_CLK			
GPD9	SLP_WLAN#	Native	SLP_WLAN#		PU 10K(@)	+3VA_DSW
GPD10	SLP_S5#	Native	SLP_S5#			
GPD11	LANPHYPC	Native	LAN_PWREN		PU 10K	+3VA_DSW

EC IT8995 GPIO

	Default	Use As	Signal Name	EXT PU/PD	Power
GPA0	0	GPO	PWR_LED	PD 1M	
GPA1	OD	GPO	CHG_LED#	PU 10K (@)	+3VA_EC
GPA2	OD	GPO	CHG_FULL_LED#	PU 10K (@)	+3VA_EC
GPA3	Alt	PWM	FAN1_PWM		
GPA4	0	GPO	EC_GPA4		
GPA5	Alt	PWM	FAN0_PWM		
GPA6	Alt	PWM	KB_LED_PWM		
GPA7	0	GPO	OS_LED#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPB0	Alt	GPI	AC_IN_DC#	PU 100K	+3VA
GPB1	I	GPI	LID_SW#	PU 100K	+3VA
GPB2	OD	GPO	NUM_LED#		
GPB3	Alt	GPO	EC_GPB3/PWR_SW#	PU 100K	+3VA
GPB4	I	GPO	PS_ON_EC		
GPB5	O	GPO	MAry_WPST	PD 10K	
GPB6	OD	GPO	RC_IN#	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPC0	O	GPO	PM_EXTTS#0	PU 10K (@)	+3VA_EC
GPC1	Alt	SMBus	SMB1_CLK	PU 4.7K	+3VA_EC
GPC2	Alt	SMBus	SMB1_DAT	PU 4.7K	+3VA_EC
GPC3	O	GPO	PM_PWRBTN#	PU 10K (@)	+3VSUS
GPC4	I	GPI	EC_SPC4/INT8#	PU 10K	+3VSUS
GPC5	I	GPI	PM_SUSC#	PD 100K	
GPC6	Alt	GPI	BAT1_IN_DC#	PD 100K	
GPC7	O	GPO	EC_SPC7		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPD0	I	GPI	EC_GPD0/PCH_SLP_S0#		
GPD1	O	GPO	EC_GPD1/ME_AC_PRESENT	PU 100K	+3VA_DSW
GPD2	Alt	GPI	BUF_PLT_RST#	PD 100K	
GPD3	OD	GPO	EXT_SCI#	PU 10K	+3VS
GPD4	OD	GPO	EXT_SMI#	PU 10K	+3VS
GPD5	O	GPO	EC_GPD5/GP_SI#		
GPD6	Alt	GPI	FAN0_TACH	PU 10K	+3VS
GPD7	Alt	GPI	FAN1_TACH	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPE0	O	GPO	EC_GPE0/SUSB_EC#	PD 4.7K	
GPE1	O	GPO	EC_GPE1/SUSC_EC#	PD 4.7K	
GPE2	O	GPO	1.2V_ON		
GPE3	O	GPO	SUSWARN#_vCC		
GPE4	O	GPO	USB_BC1.2_OFF#		
GPE5	I	GPI	PM_SUS0#	PD 100K	
GPE6	OD	GPO	CAP_LED#		
GPE7	OD	GPO	THRO_CPU#	PU 10K(@)	+3VA_EC

	Default	Use As	Signal Name	EXT PU/PD	Power
GPF0	O	GPO	5VSUS_ON	PU 100K&PD 1M	+3VA_EC
GPF1	O	GPO	VSUS_ON	PU 100K&PD 1M	+3VA_EC
GPF2	Alt	SMBus	P_SMB0_CLK	PU 4.7K	+3VA_EC
GPF3	Alt	SMBus	P_SMB0_DAT	PU 4.7K	+3VA_EC
GPF4	Alt	PS2	TP_CLK	PU 4.7K	+3VS
GPF5	Alt	PS2	TP_DAT	PU 4.7K	+3VS
GPF6	Alt	PECI	EC_GPF6/PECI_EC		
GPF7	O	GPO	PCH_SPI_0V		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPG0	O	GPO	DGPU_LIMIT		
GPG1	O	GPO	PCH_SUSACK#		
GPG2	I	GPI	EC_GPG2/PWRLIMIT_EC#	PU 100K	+3VA_EC
GPG3	GPI		EC_SCE0#/EC_SCE#_PCH		
GPG4	GPI		EC_S1/EC_S1_PCH		
GPG5	GPI		EC_S0/EC_S0_PCH		
GPG6	O	GPO	USB30_SYBUS		
GPG7	GPI		EC_SCK_PCH	PD 10K (@)	

	Default	Use As	Signal Name	EXT PU/PD	Power
GPH0	Alt	PCI	PM_CLKRUN#	PU 8.2K	+3VS
GPH1	Alt	SMBus	P_SMB3_CLK	PU 4.7K	+3VA_EC
GPH2	Alt	SMBus	P_SMB3_DAT	PU 4.7K	+3VA_EC
GPH3	O	GPO	PM_RSMRST#	PD 10K(@)	
GPH4	O	GPO	DPWROK_EC	PD 10K	
GPH5	O	GPO	PM_PWROK	PD 10K	
GPH6	O	GPO	PM_SYSPWROK	PD 10K	
GPH7	O	GPO	LCD_BACKOFF#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPI0	I	GPI	PM_SLP_SUS#		
GPI1	I	GPI	3VSUS_PWRGD		
GPI2	I	GPI	ALL_SYSTEM_PWRGD	PU 10K	+3VS
GPI3	I	GPI	IMVP8_PWRGD	PU 100K	+3VS
GPI4	I	GPI	3VA_DSW_PWRGD	PU 100K	+3VA_DSW
GPI5	I	GPI	SUSWARN#		
GPI6	Alt	AD	A/D_MAX_POWER	PD 0	+3VACC
GPI7	Alt	AD	MB_MAX_POWER	PU 100K & PD 56K	+3VACC

	Default	Use As	Signal Name	EXT PU/PD	Power
GPJ0	O	GPI	EC_GPJ0/USB31_5VBUS#	PU 10K	+3VSUS
GPJ1	O	GPO	3VAOSW_ON	PU 100K	+3VA_EC
GPJ2	Alt	DA	FL_REF_EC		
GPJ3	O	GPO	EC_GPJ3 / PCH_SUS_STAT#		
GPJ4	Alt	DA	IBAT_REF_EC		
GPJ5	O	GPO	EC_GPJ5		
GPJ6	I	GPI	KB_WAKE#	PU 100K	+3VA_DSW
GPJ7	O	GPO	USB_CHARGE_ON#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPM0	LAD0/EIO0		LPC_AD0_R/LPC_AD0		
GPM1	LAD1/EIO1		LPC_AD1_R/LPC_AD1		
GPM2	LAD2/EIO2		LPC_AD2_R/LPC_AD2		
GPM3	LAD3/EIO3		LPC_AD3_R/LPC_AD3		
GPM4	LPCLK/ECSCK		CLK_KBCPCI_PCH		
GPM5	LFRAME#/ECS#		LPC_FRAME#		
GPM6	SERIRQ/ALERT#		INT_SERIRQ	PU 10K	+3VS

N501VW Setting

SM_BUS ADDRESS :

PCH Master	
SM-Bus Device	**SM-Bus Address**
on board memory CHA	
SO-DIMM B(0)	A4h

EC Master (SMB1)	SM-Bus Address
SM-Bus Device	
VGA Thermal Sensor	90h
CPU Thermal Sensor	98h
Power Thermal Sensor	70h

Device Identification

CPU Thermal Sensor		
1st	0x0023218010	MCT77771U
2nd		

GX501VIP\CIE & USB Function define

Kabylake HM175

SSID	HSIO Capabilities	Function	SRC
	PCIEG (From GPU)	dGPU	SRC0
01	USB3#01	USB3.0 MB Port1(Charger)	
02	USB3#02 / SSIC#01	USB3.0 Port2	
03	USB3#03 / SSIC#02	USB3.0 Port3	
04	USB3#04	USB3.0 Port4	
05	USB3#05		
06	USB3#06		
07	USB3#07 / PCIE#01	CardReader_USB3(RSV)	
08	USB3#08 / PCIE#02		SRC2
09	PCIE#03	WLAN	SRC3
10	PCIE#04 / GBE		
11	PCIE#05 / GBE	Thunderbolt	SRC5
12	PCIE#06		
13	PCIE#07		
14	PCIE#08		
15	PCIE#09 / SATA#0 / GBE	SATA*1 SSD port0	
16	PCIE#10 / SATA#1	PCIE*4 SSD	SRC6
17	PCIE#11		
18	PCIE#12 / GBE		
19	PCIE#13 / SATA#0 / GBE		
20	PCIE#14 / SATA#1		
21	PCIE#15 / SATA#2		
22	PCIE#16 / SATA#3		
23			
24			
25			
26			

USB 2.0	Function
USB2_01	USB3.0 MB Port1(Charger)
USB2_02	USB3.0 MB Port2
USB2_03	USB3.0 MB Port3
USB2_04	Camera
USB2_05	USB3.0 MB Port4
USB2_06	
USB2_07	Card Reader
USB2_08	N key
USB2_09	BT
USB2_10	
USB2_11	
USB2_12	

SKL PCH-H Z170 HSIO

1	USB3 #1 (OTG)					
2	USB3 #2	SSIC #1				
3	USB3 #3	SSIC #2				
4	USB3 #4					
5	USB3 #5					
6	USB3 #6					
7	USB3 #7	PCIE #1	x 2	x 4	NA	
8	USB3 #8	PCIE #2				
9	PCIE #3		x 2			
10	USB3 #10	PCIE #4	GbE			
11	PCIE #5		GbE	x 2	x 4	NA
12	PCIE #6					
13	PCIE #7			x 2		
14	PCIE #8					
15	PCIE #9	SATA #0	GbE	x 2	x 4	Intel IRST PCIE Storage Device #1
16	PCIE #10	SATA #1				
17	PCIE #11			x 2		
18	PCIE #12		GbE			
19	PCIE #13	SATA #0*	GbE	x 2	x 4	Intel IRST PCIE Storage Device #2
20	PCIE #14	SATA #1*				
21	PCIE #15	SATA #2		x 2		
22	PCIE #16	SATA #3				
23	PCIE #17	SATA #4		x 2	x 4	Intel IRST PCIE Storage Device #3
24	PCIE #18	SATA #5				
25	PCIE #19	SATA #6		x 2		
26	PCIE #20	SATA #7				

SKL PCH-H H170 HSIO

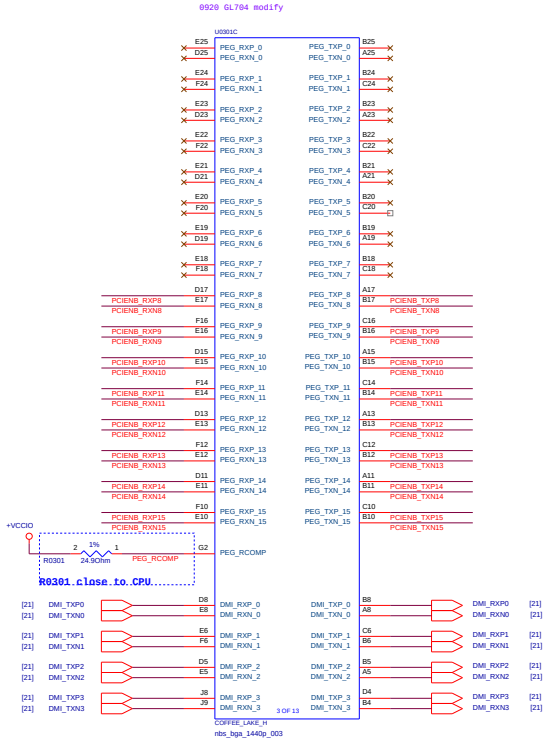
1	USB3 #1 (OTG)					
2	USB3 #2	SSIC #1				
3	USB3 #3	SSIC #2				
4	USB3 #4					
5	USB3 #5					
6	USB3 #6					
7	USB3 #7					
8	USB3 #8					
9	PCIE #3		x 2	NA	NA	
10	PCIE #4	GbE				
11	PCIE #5	GbE	x 2	x 4	NA	
12	PCIE #6					
13	PCIE #7		x 2			
14	PCIE #8					
15	PCIE #9	SATA #0	GbE	x 2	x 4	Intel IRST PCIE Storage Device #1
16	PCIE #10	SATA #1				
17	PCIE #11			x 2		
18	PCIE #12		GbE			
19	PCIE #13	SATA #0*	GbE	x 2	x 4	Intel IRST PCIE Storage Device #2
20	PCIE #14	SATA #1*				
21	PCIE #15	SATA #2		x 2		
22	PCIE #16	SATA #3				
23	SATA #4			NA	NA	NA
24	SATA #5					
25	PCIE #19			x 2		
26	PCIE #20					

SKL PCH-H HM170 HSIO

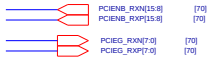
1	USB3 #1 (OTG)					
2	USB3 #2	SSIC #1				
3	USB3 #3	SSIC #2				
4	USB3 #4					
5	USB3 #5					
6	USB3 #6					
7	USB3 #7	PCIE #1	x 2	x 4	NA	
8	USB3 #8	PCIE #2				
9	PCIE #3		x 2			
10	PCIE #4	GbE				
11	PCIE #5	GbE	x 2	x 4	NA	
12	PCIE #6					
13	PCIE #7		x 2			
14	PCIE #8					
15	PCIE #9	SATA #0	GbE	x 2	x 4	Intel IRST PCIE Storage Device #1
16	PCIE #10	SATA #1				
17	PCIE #11			x 2		
18	PCIE #12		GbE			
19	PCIE #13	SATA #0*	GbE	x 2	x 4	Intel IRST PCIE Storage Device #2
20	PCIE #14	SATA #1*				
21	PCIE #15	SATA #2		x 2		
22	PCIE #16	SATA #3				
23				NA	NA	NA
24						
25				x 2		
26						

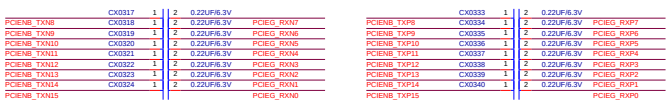
ASUS	Project Name: G711GW		Rev: 1.0
Title : System Setting			
File:	Date:	Engineer: Gaming RD	
Size: Custom	Document Number:	Sheet:	of:

PCIEG



CFG2=0 -> Reversed
CFG5=0 -> PCIEG 2x8





Display

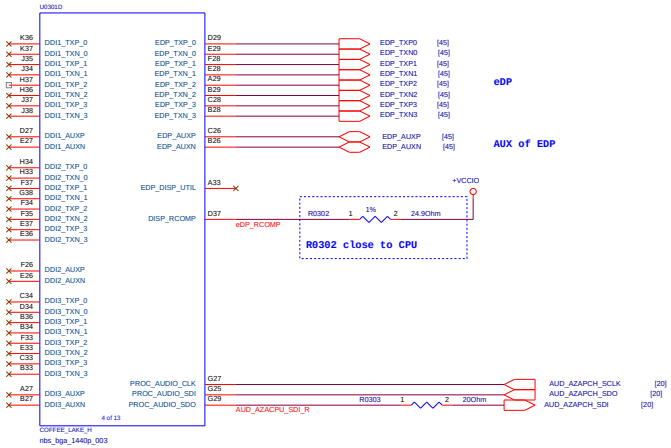


Table 8-3. Few Supported Normal and Lane-reversed Bifurcation Configurations

x16 Controller Negotiated Width	x8 Controller Negotiated Width	x4 Controller Negotiated Width	Processor	Physical Lanes															
				0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x16	Off	Off	Direct	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x8	x8	Off	Direct	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
x8	x4	x4	Direct	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
x16	Off	Off	Reverse	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x8	x8	Off	Reverse	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
x8	x4	x4	Reverse	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

Notes:
1. Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
2. In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
   — Connect lane 0 of 1st device to lane 0.
   — Connect lane 0 of 2nd device to lane 8.
   — Connect lane 0 of 3rd device to lane 12.
   For example:
   a. When using 1x8 + 2x4, the 8 lane device must use lanes 0:7.
   b. When using 1x4 + 1x2, the 4 lane device must use lanes 0:3, and other 2 lanes device must use lanes 8:9.
   c. When using 1x4 + 1x2 + 1x1, 4 lane device must use lanes 0:3, two lane device must use lanes 8:9,one lane device must use lane12.

Refer to CFL-H PDG P.363 (Doc.571391)

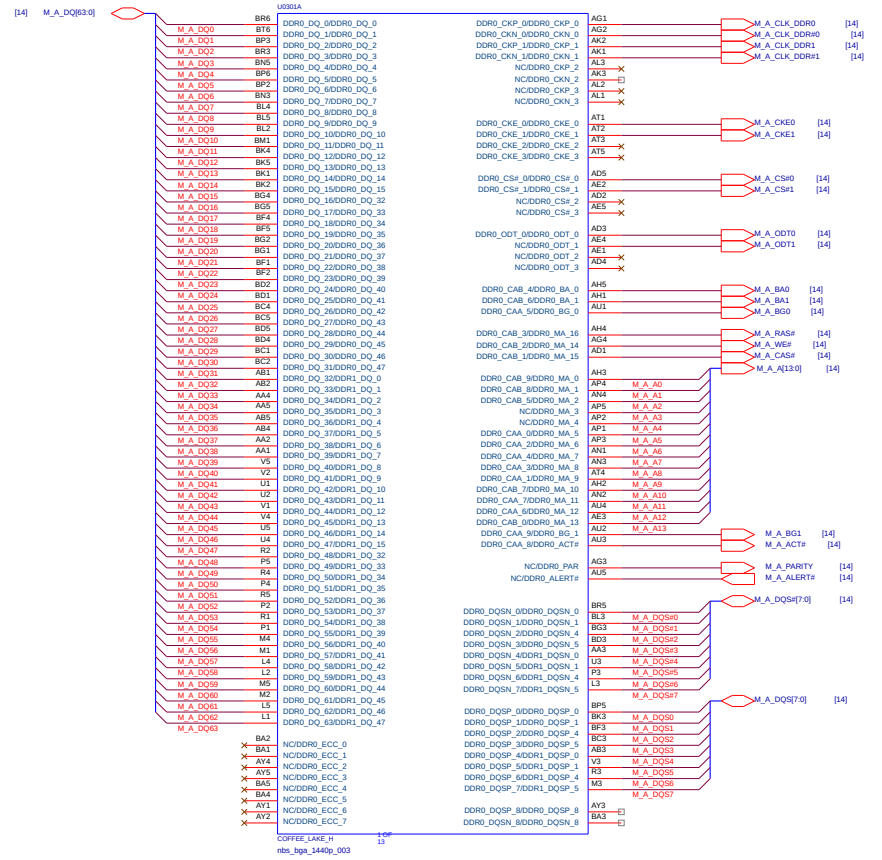
31.1.4 Disabling and Termination Guidelines for the Intel® High Definition Audio Interface

When HDA_SDIN[1:0], DISPA_SDIN interface is not implemented on the platform the signal pin(s) may be left unconnected.

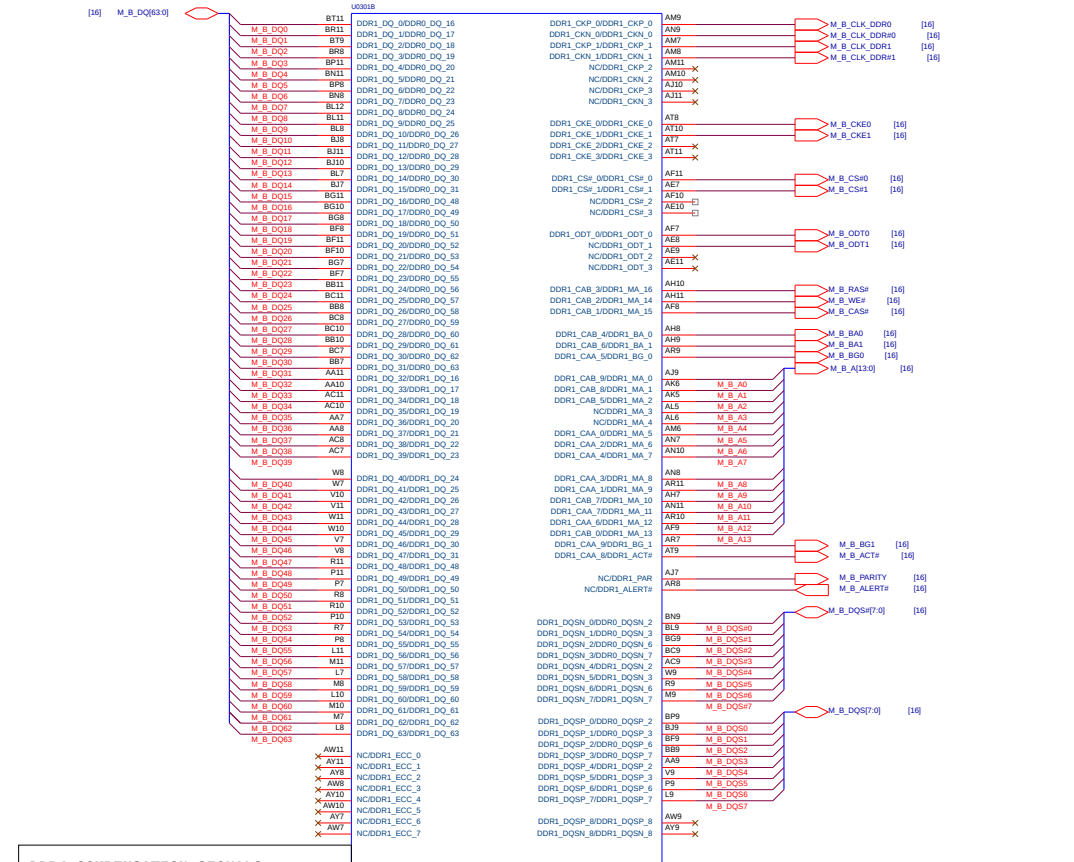
When the Intel® Display Audio interface is not implemented, PROC_AUDIO_CLK and PROC_AUDIO_SDI need to be terminated to GND via a weak pull-down resistor (i.e. ~2KΩ), PROC_AUDIO_SDO can be left unconnected.

ASUS	Project Name: G711GW	Rev: R1.1
Title : CPU_DMI,PEG,FDI,eDP,DDI		
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD
Date: Tuesday, April 16, 2019	Sheet 3 of 103	

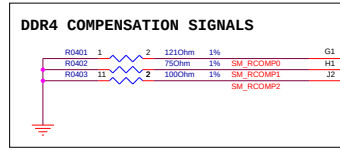
Memory Channel A



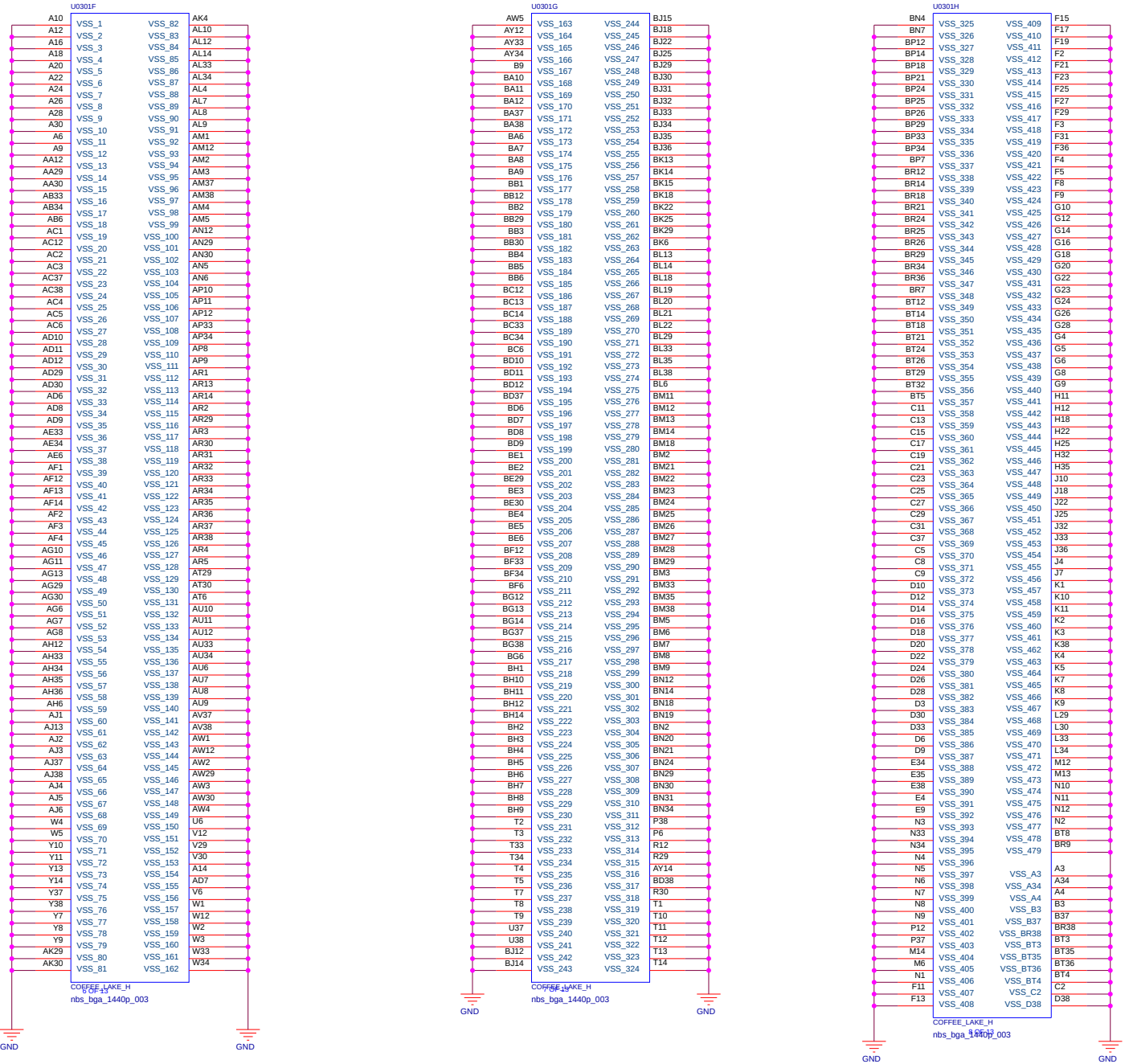
Memory Channel B



DDR4 COMPENSATION SIGNALS

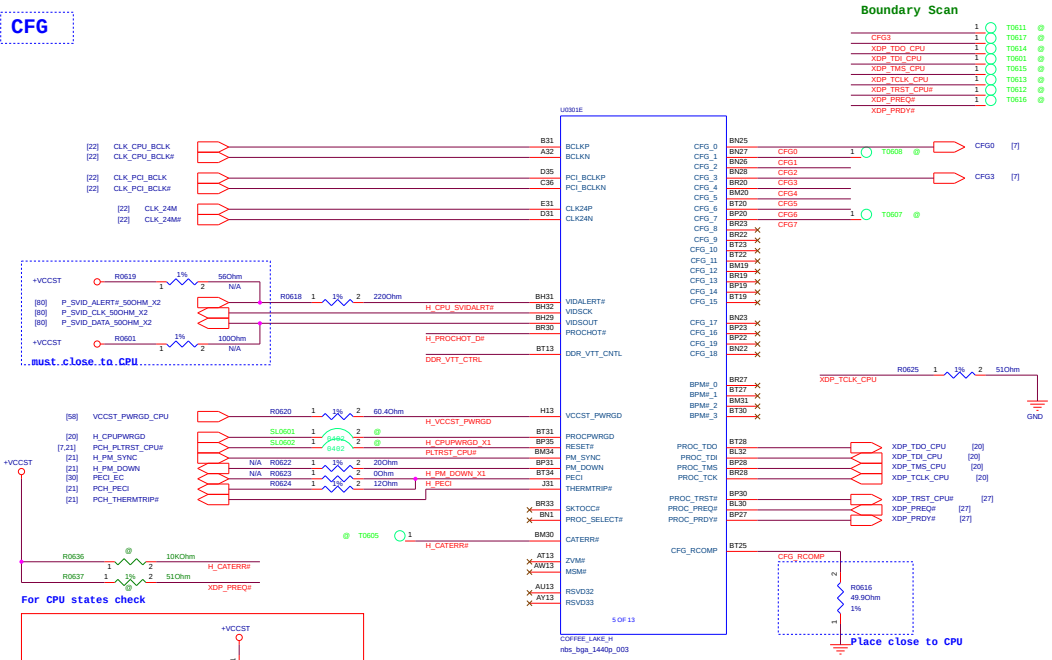


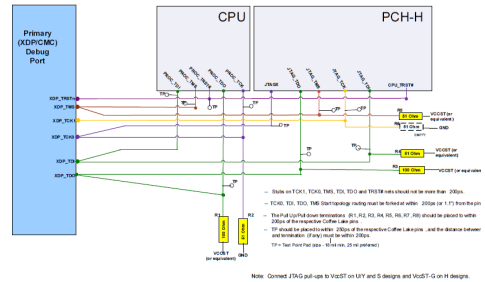
Project Name	G711GW	Rev	1.0
Title :	CPU_DDR4		
Size	Custom	Dept.:	ASUSTeK COMPUTER
Engineer:	Gaming RD		
Date:	Tuesday, April 16, 2019	Sheet	4 of 103



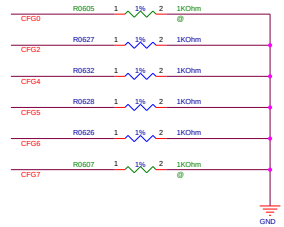
ASUS	Project Name: G711GW		Rev: 1.0
Title :	CPU_CFG,RSVD,GND		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Tuesday, April 16, 2019	Sheet 5 of 103		

CFG





CFG Straps



CFG Straps for Processor

ref : Intel 570805_Coffeelake_EDS_Vol_1_Rev1.4 P.121

CFG[0] : Stall reset sequence after PCU PLL lock until de-asserted

- 1 : (Default) Normal Operation; No stall
- 0 : Stall

CFG[1] : Reserved Configuration Lane

Reserved Configuration Lane

CFG[2] : PCI Express* Static x16 Lane Numbering Reversal

- 1 : (Default) Normal Operation
- 0 : Lane Numbers Reversed

CFG[3] : Reserved configuration lanes

Reserved Configuration Lane

CFG[4] : eDP Enable

- 1 : Disabled
- 0 : Enabled

CFG[6:5] : PCI Express* Bifurcation

- 00 : 1 x8 , 2 x4 PCI Express*
- 01 : Reserved
- 10 : 2 x8 PCI Express*
- 11 : 1 x16 PCI Express*

CFG[7] : PEG Training

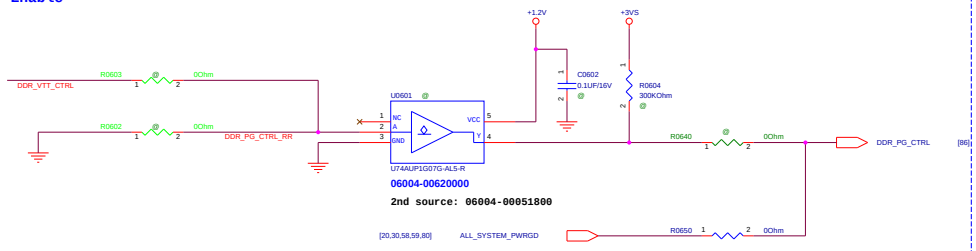
- 1 : (Default) PEG Train Immediately Following RESET# de-assertion
- 0 : PEG Wait for BIOS for Training

CFG[19:8] : Reserved Configuration Lanes

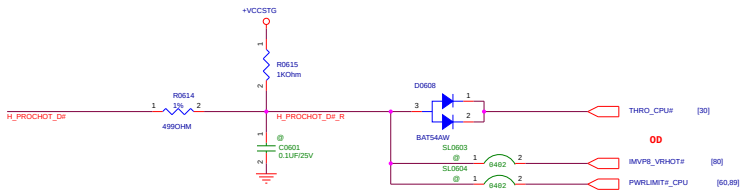
Reserved Configuration Lanes

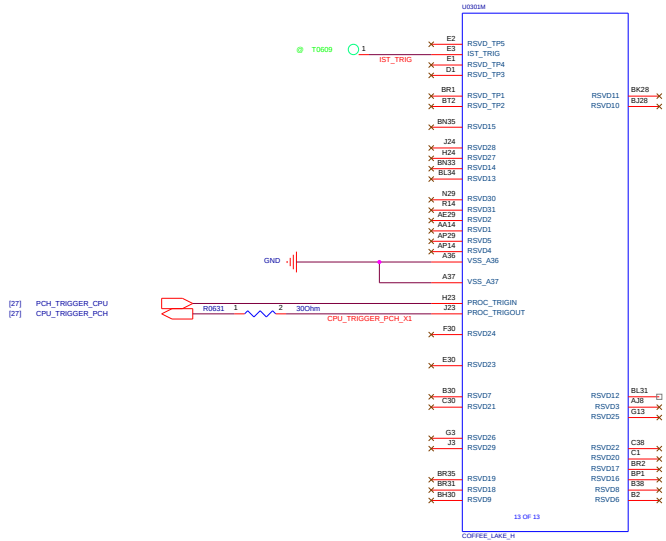
DDR_VTT_CTRL:
System Memory Power Gate Control:
Disables the platform memory VTT regulator
in C8 and deeper and S3.
Ref: Intel 570805_Coffeelake_EDS_Vol_1_Rev1.5 P.116

VTT Enable



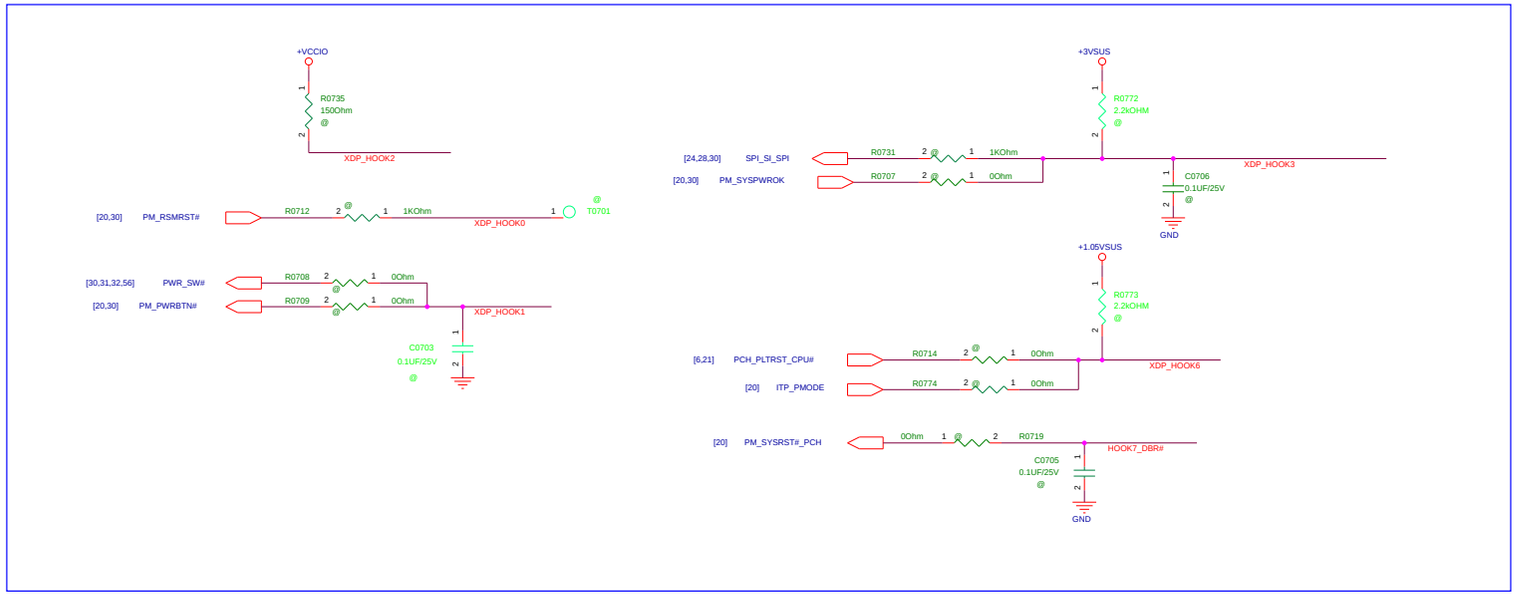
CPU SIDEBAND SIGNALS



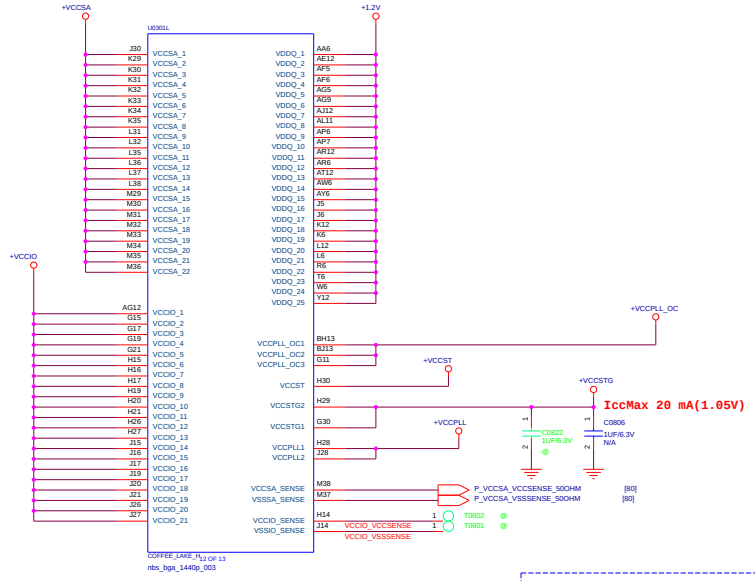


ASUS	Project Name: G711GW		Rev: 1.0
Title :	CPU_CFG,RSVD		
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Tuesday, April 16, 2019	Sheet 6 of 103		

CPU XDP



Project Name: G711GW			Rev: 1.0
Title : CPU XDP			
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Tuesday, April 16, 2019	Sheet 7 of 103		



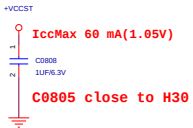
Main Source	1th PWR	2nd PWR	3rd PWR
AC_BAT_SYS	+1.05VSUS	+VCCST	
		+VCCSTG	
	+1.2V	+VTT	
		+VCCPLL_OC	
	+VCCSA		
	+VCCIO	+VCCSTG	

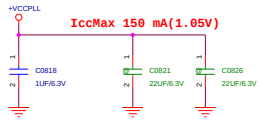
Configuration		Estimated SoC Power Delta from Config #1 to #2
Config #1 (Premium)	Config #2 (Volume)	CFL H
VccST off in S3	On in S3	+25-30mW
VccPLL_OC off in S0/C10	On in S0/C10	+3-10mW
VccPLL_OC off in S0ix	On in S0ix	+3-10mW

Other than what is documented in the table above, there is no expected SoC power delta in Sx states between Volume and Premium configurations. Independently, implementing Deep Sx (also known as DSW) may lower platform power over traditional Sx.

CPU_C10_GATE# is a signal from the Coffee Lake SoC that can be used for gating off VccSTG, VccPLL_OC and VccIO (CFL-H) in the S0/C10 system state in order to save power.

+VCCST/+VCCPLL DECAPS Place Back Side (TOP)





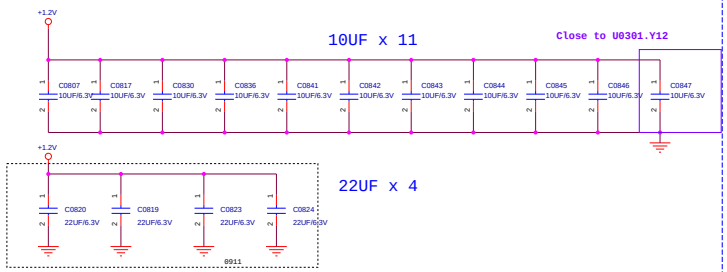
CFL U/H PDG Update for VCCPLL Power Rail Design Guidelines

Due to Display PLL lock issues observed on systems with high noise level on VCCPLL, CFL-H (BP#571391 and CFL-U (BP#571021 Platform design guidelines has been updated with new recommendation for VCCPLL power rail.

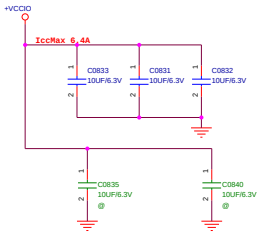
An additional capacitor 0805 size placeholder near CPU BGA ball is recommended for better power delivery, this should be stuffed when encountered a noisy VCCPLL power rail.

This new recommendation not required for systems that follows the PDG Power Integrity guidance and kept low noise level on VCCPLL.

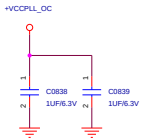
+VDDQ DECAPS Place Back Side (TOP)



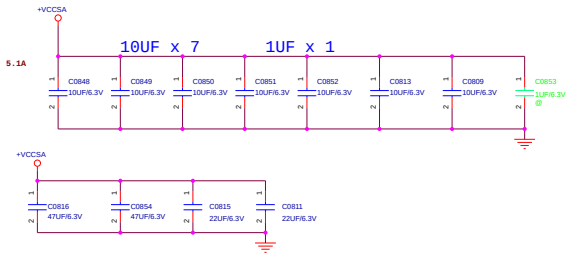
+VCCIO DECAPS Place Back Side (TOP)



+VCCPLL_OC DECAPS Place Back Side (TOP)

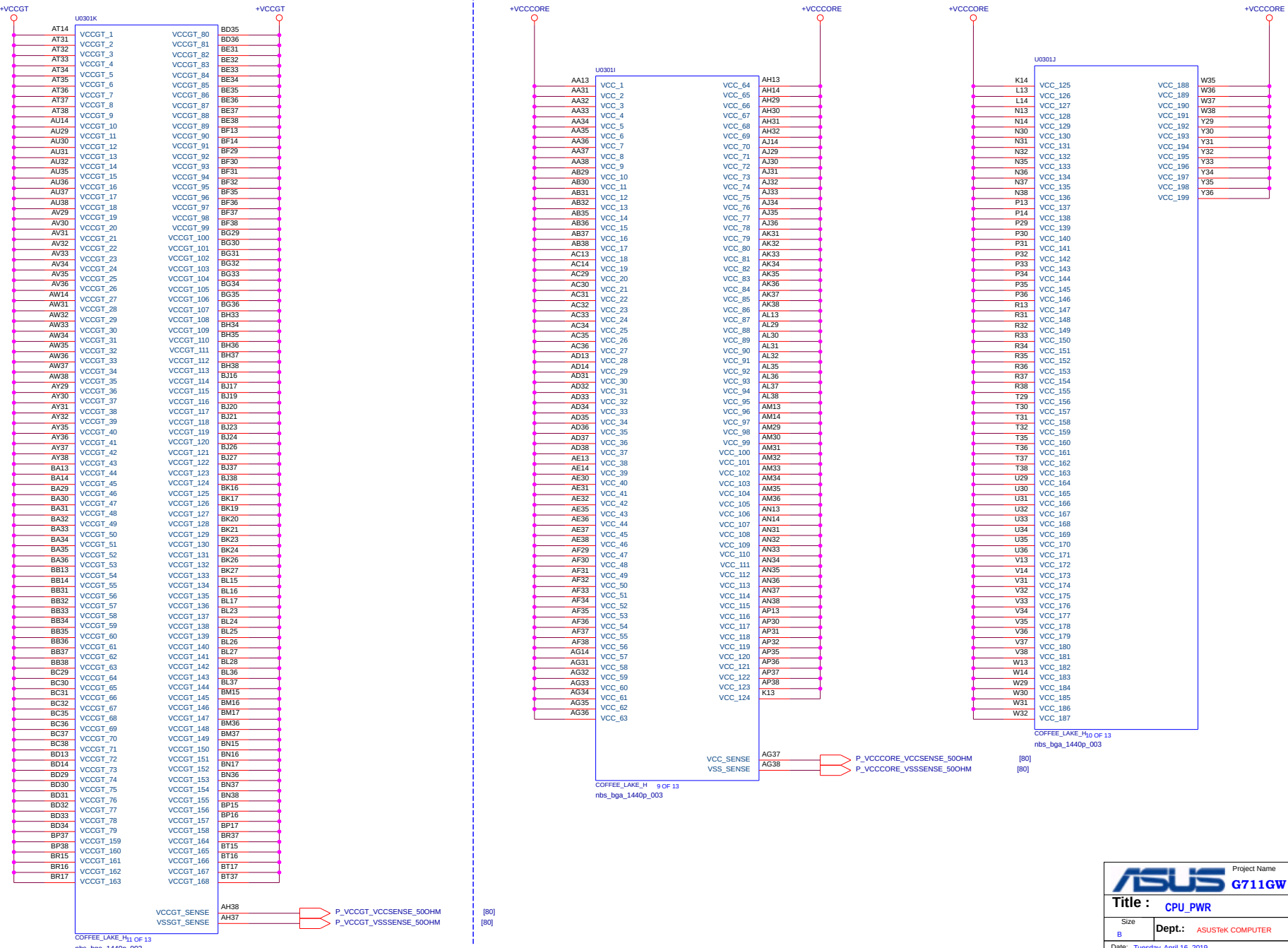


+VCCSA DECAPS Place Back Side (TOP)



+VCCSA near CPU

ASUS	Project Name: G711GW		Rev: 1.0
Title : CPU_PWR			
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Tuesday, April 16, 2019	Sheet 8 of 103		


Main Board
+VCCGT
+VCCGT
U0301K
VCCGT_1
VCCGT_2
VCCGT_3
VCCGT_4
VCCGT_5
VCCGT_6
VCCGT_7
VCCGT_8
VCCGT_9
VCCGT_10
VCCGT_11
VCCGT_12
VCCGT_13
VCCGT_14
VCCGT_15
VCCGT_16
VCCGT_17
VCCGT_18
VCCGT_19
VCCGT_20
VCCGT_21
VCCGT_22
VCCGT_23
VCCGT_24
VCCGT_25
VCCGT_26
VCCGT_27
VCCGT_28
VCCGT_29
VCCGT_30
VCCGT_31
VCCGT_32
VCCGT_33
VCCGT_34
VCCGT_35
VCCGT_36
VCCGT_37
VCCGT_38
VCCGT_39
VCCGT_40
VCCGT_41
VCCGT_42
VCCGT_43
VCCGT_44
VCCGT_45
VCCGT_46
VCCGT_47
VCCGT_48
VCCGT_49
VCCGT_50
VCCGT_51
VCCGT_52
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VCCGT_55
VCCGT_56
VCCGT_57
VCCGT_58
VCCGT_59
VCCGT_60
VCCGT_61
VCCGT_62
VCCGT_63
VCCGT_64
VCCGT_65
VCCGT_66
VCCGT_67
VCCGT_68
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VCCGT_70
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VCCGT_87
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VCCGT_90
VCCGT_91
VCCGT_92
VCCGT_93
VCCGT_94
VCCGT_95
VCCGT_96
VCCGT_97
VCCGT_98
VCCGT_99
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VCCGT_101
VCCGT_102
VCCGT_103
VCCGT_104
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VCCGT_118
VCCGT_119
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VCCGT_121
VCCGT_122
VCCGT_123
VCCGT_124
VCCGT_125
VCCGT_126
VCCGT_127
VCCGT_128
VCCGT_129
VCCGT_130
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VCCGT_135
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VCCGT_153
VCCGT_154
VCCGT_155
VCCGT_156
VCCGT_157
VCCGT_158
VCCGT_164
VCCGT_165
VCCGT_166
VCCGT_167
VCCGT_168
VCCGT_SENSE
VSSGT_SENSE
P_VCCGT_VCCSENSE_50OHM
P_VCCGT_VSSSENSE_50OHM
[80]
[80]
COFFEE_LAKE_H 11 OF 13
nbs_bga_1440p_003
+VCCCORE
+VCCCORE
U0301I
VCC_1
VCC_2
VCC_3
VCC_4
VCC_5
VCC_6
VCC_7
VCC_8
VCC_9
VCC_10
VCC_11
VCC_12
VCC_13
VCC_14
VCC_15
VCC_16
VCC_17
VCC_18
VCC_19
VCC_20
VCC_21
VCC_22
VCC_23
VCC_24
VCC_25
VCC_26
VCC_27
VCC_28
VCC_29
VCC_30
VCC_31
VCC_32
VCC_33
VCC_34
VCC_35
VCC_36
VCC_37
VCC_38
VCC_39
VCC_40
VCC_41
VCC_42
VCC_43
VCC_44
VCC_45
VCC_46
VCC_47
VCC_48
VCC_49
VCC_50
VCC_51
VCC_52
VCC_53
VCC_54
VCC_55
VCC_56
VCC_57
VCC_58
VCC_59
VCC_60
VCC_61
VCC_62
VCC_63
VCC_64
VCC_65
VCC_66
VCC_67
VCC_68
VCC_69
VCC_70
VCC_71
VCC_72
VCC_73
VCC_74
VCC_75
VCC_76
VCC_77
VCC_78
VCC_79
VCC_80
VCC_81
VCC_82
VCC_83
VCC_84
VCC_85
VCC_86
VCC_87
VCC_88
VCC_89
VCC_90
VCC_91
VCC_92
VCC_93
VCC_94
VCC_95
VCC_96
VCC_97
VCC_98
VCC_99
VCC_100
VCC_101
VCC_102
VCC_103
VCC_104
VCC_105
VCC_106
VCC_107
VCC_108
VCC_109
VCC_110
VCC_111
VCC_112
VCC_113
VCC_114
VCC_115
VCC_116
VCC_117
VCC_118
VCC_119
VCC_120
VCC_121
VCC_122
VCC_123
VCC_124
VCC_SENSE
VSS_SENSE
P_VCCCORE_VCCSENSE_50OHM
P_VCCCORE_VSSSENSE_50OHM
[80]
[80]
COFFEE_LAKE_H 9 OF 13
nbs_bga_1440p_003
+VCCCORE
+VCCCORE
U0301J
VCC_125
VCC_126
VCC_127
VCC_128
VCC_129
VCC_130
VCC_131
VCC_132
VCC_133
VCC_134
VCC_135
VCC_136
VCC_137
VCC_138
VCC_139
VCC_140
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VCC_187
VCC_188
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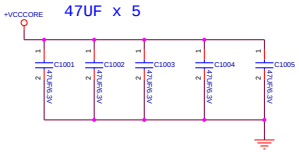
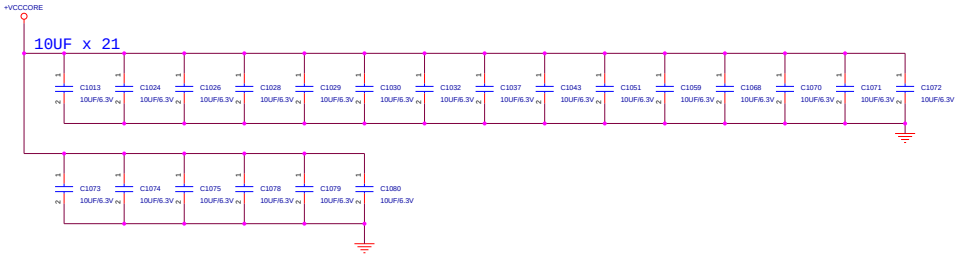
VCC_190
VCC_191
VCC_192
VCC_193
VCC_194
VCC_195
VCC_196
VCC_197
VCC_198
VCC_199
COFFEE_LAKE_H 10 OF 13
nbs_bga_1440p_003
Project Name
G711GW
Rev
1.0
Title : CPU_PWR
Size
B
Dept.: ASUSTeK COMPUTER
Engineer: Gaming RD
Date: Tuesday, April 16, 2019
Sheet 9 of 103

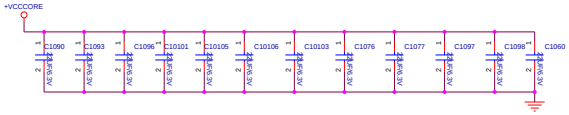
Domain	Board Edge cap	Backside cap	Notes
Vcc	5x 47uF 0805		
		12x 22uF 0603	
		21x 10uF 0402	
		24x 1uF 0201	
		24x 0201 (placeholder)	
Vcc_{GT}	3x 47uF 0805		Place as close to the BGA as possible
	7x 22uF 0603		
		10x 10uF 0402	
		12x 1uF 0201	

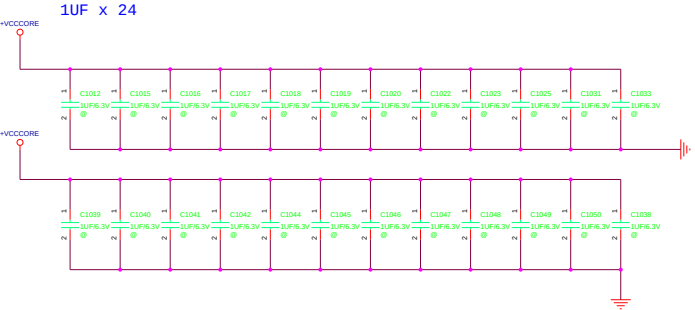
+VCCORE near CPU



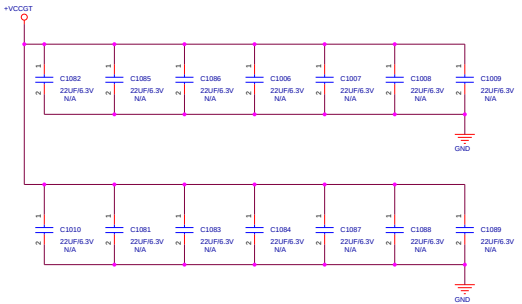
+VCCORE DECAPS Place Back Side (TOP)







+VCCGT cap near CPU **22uF x14**



ASUS	Project Name: G711GW		Rev: 1.0
Title : 010_CPU_POWER_CAP			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Tuesday, April 16, 2019	Sheet 10 of 103		

	Project Name G711GW	Rev R1.0

Title : TBT_Alpine-Ridge

Size	Dept.:	Engineer:
C	ASUSTeK COMPUTER	Gaming RD

Date: Tuesday, April 16, 2019	Sheet 11 of 103

Project Name

G711GW

Rev

R1.3

Title : CYPRESS CCG4

Size	Dept.:	Engineer:
D	ASUSTeK COMPUTER	Gaming RD

Date: Tuesday, April 16, 2019

<Variant Name>

	Title :	**DDR4_TERMINATION**
ASUSTeK COMPUTER	**Engineer:**	**Gaming RD**

Size	Project Name	Rev
Custom	**G711GW**	1.0

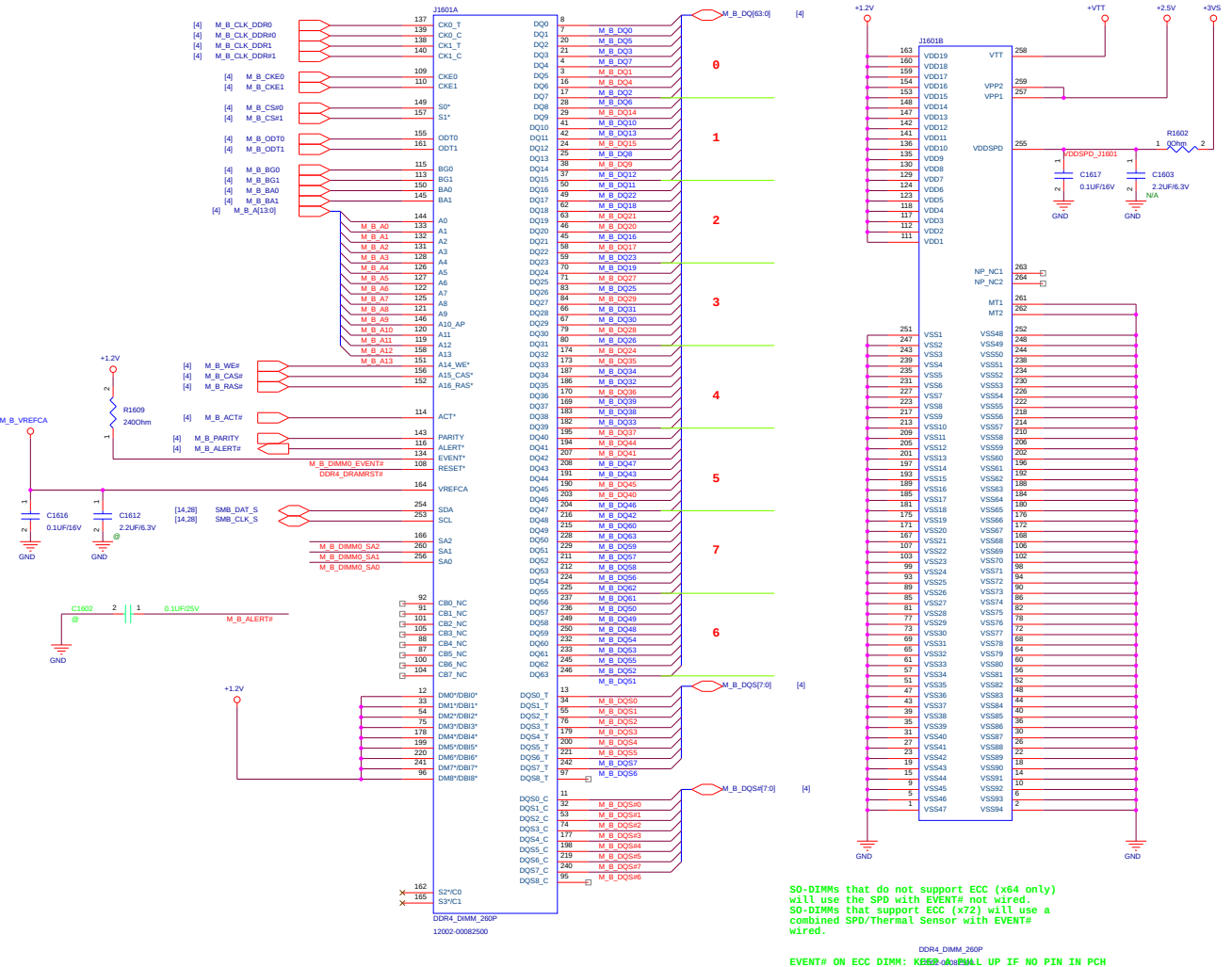
Date:	Tuesday, April 16, 2019	Sheet	13	of	103

<Variant Name>

ASUSTeK COMPUTER	Title : DDR4_ON-BOARD_A2	
	Engineer: Gaming RD	
Size: C	Project Name: G711GW	Rev: 1.0
Date: Tuesday, April 16, 2019	Sheet 15 of 103	

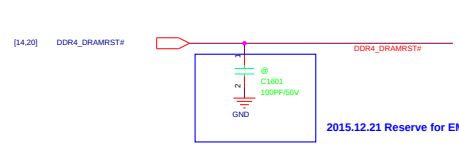
SODIMM CHB-DIMM0
TOP H4.0mm STD (J1601)

Main Board

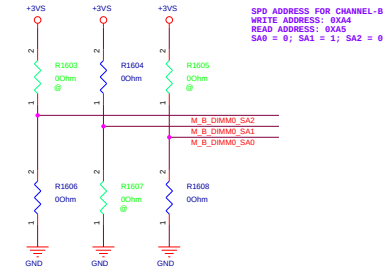


SO-DIMMs that do not support ECC (x64 only)
will use the SPD with EVENT# not wired.
SO-DIMMs that support ECC (x72) will use a
combined SPD/Thermal Sensor with EVENT#
wired.

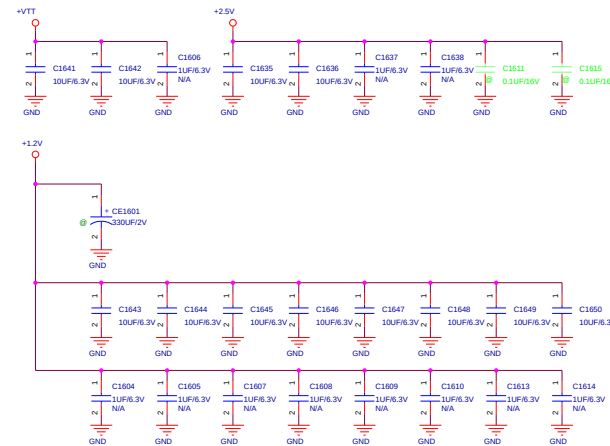
EVENT# ON ECC DIMM: KEEP PULL UP IF NO PIN IN PCH



2015.12.21 Reserve for EMI



SPD ADDRESS FOR CHANNEL-B
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA5
SA0 = 0; SA1 = 1; SA2 = 0



ASUS	Project Name: G711GW		Rev: 1.0
Title :	DIM_DDR4 SO-DIMM B1		
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Tuesday, April 16, 2019	Sheet 16 of 103		

<Variant Name>

ASUSTeK COMPUTER	Title : NB_****	
	Engineer: Gaming RD	
Size: A	Project Name: G711GW	Rev: 1.0
Date: Tuesday, April 16, 2019	Sheet 17 of 103	

Figure 4-23. CFL H DDR4 x16 Memory Down V_{REF-CA} Overview

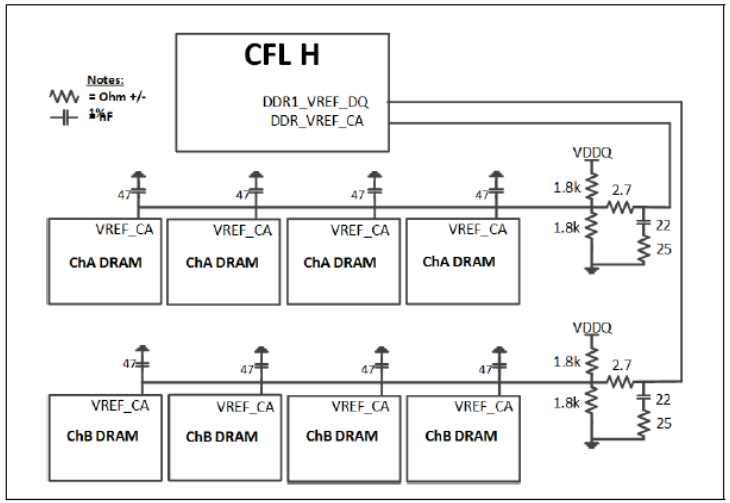
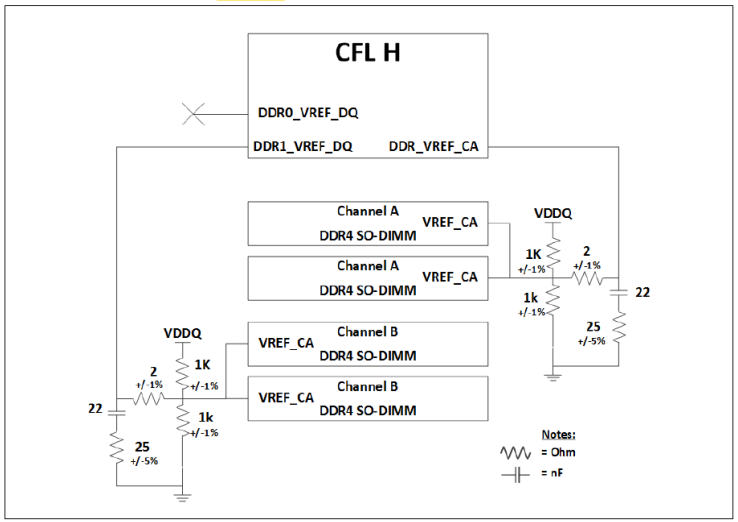
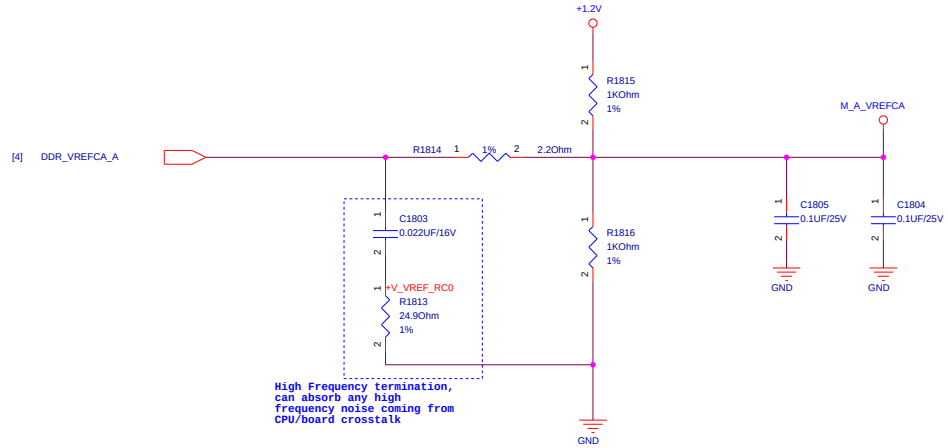


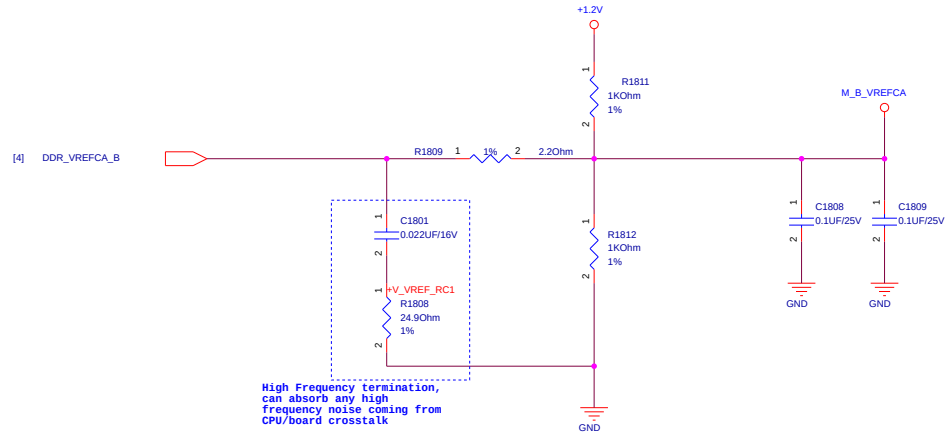
Figure 4-22. CFL-H DDR4 SO-DIMM V_{REF-CA} Overview



Vref for CHA_DIMM0



Vref for CHB_DIMM0



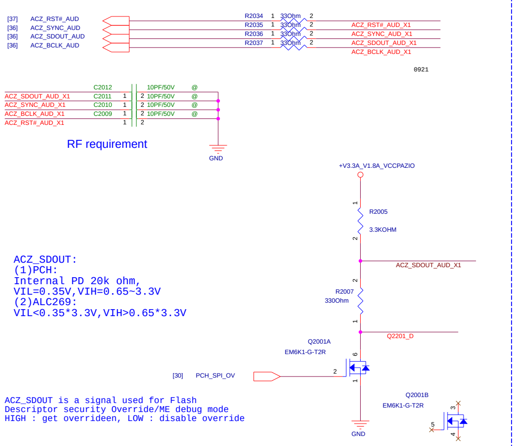
Main Board

ASUS	Project Name: G711GW	Rev: 1.0
Title : DIM_CA/DQ Voltage		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD
Date: Tuesday, April 16, 2019	Sheet 18 of 103	

<Variant Name>

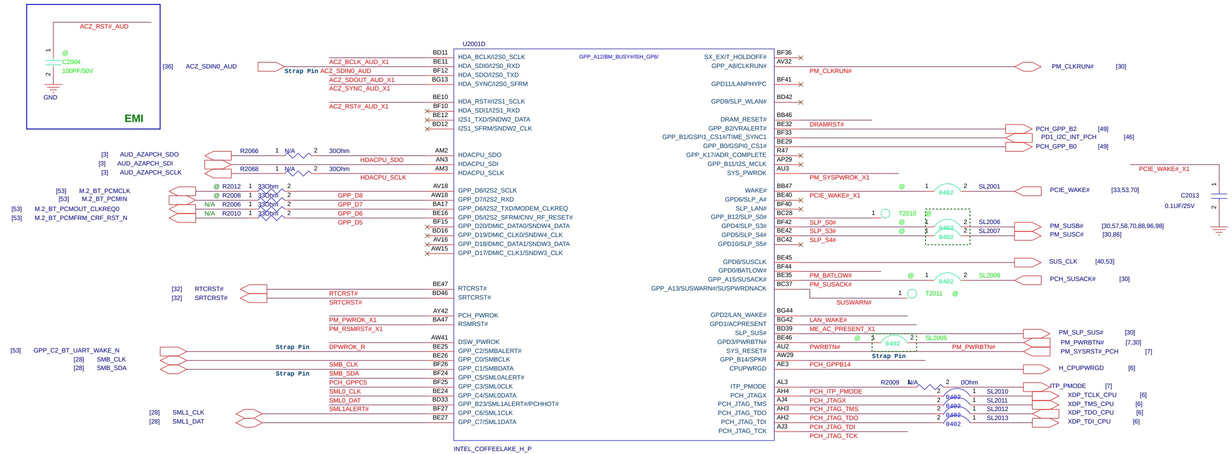
ASUSTeK COMPUTER	**Title :** *****	
	Engineer: Gaming RD	
Size: C	Project Name: **G711GW**	Rev: 1.0
Date: Tuesday, April 16, 2019	Sheet 19 of 103	

HD Audio



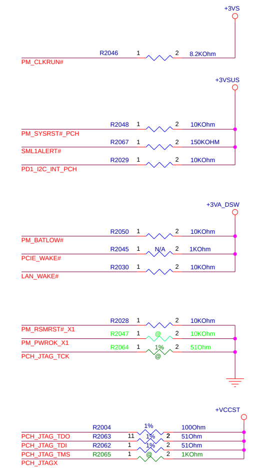
ACZ_SDOUT:
(1)PCH:
Internal PD 20k ohm,
VIL=0.35V,VIH=0.65~3.3V
(2)ALC269:
VIL<0.35*3.3V,VIH>0.65*3.3V

ACZ_SDOUT is a signal used for Flash Descriptor security Override/ME debug mode
HIGH : get overridden, LOW : disable override



Power failure solution (S0-->G3,S5-->G3):

Main Board

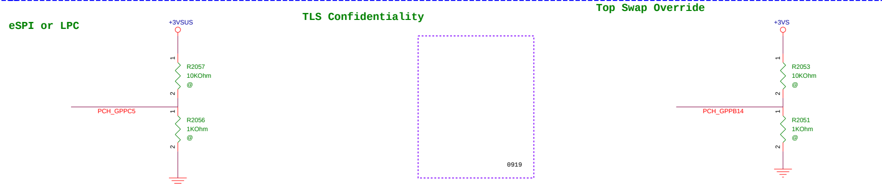


Main Source	1th PWR	2nd PWR	3rd PWR	4th
+RTCBAT	+RTC_BAT	+3VA_RTC		
AC_BAT_SYS	+1.05VSUS	+VCCST		
	+1.2V			
	+3VAO	+3VA	+3VA_EC	
	+3VA_DSW	+3VSUS	+3VSUS_PCH	+V3.3A_V1.8A_VCCPAZIO
		+3VS		

eSPI or LPC

TLS Confidentiality

Top Swap Override

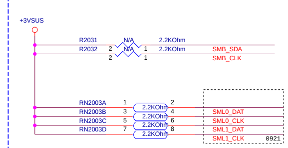


PCH_GPPC5: weak internal pull down	
PU	eSPI
PD	LPC (default)

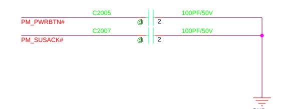
PU	Enable
PD	Disable (default)

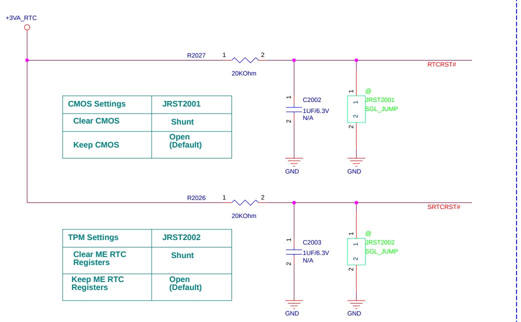
PCH_GPPB14: weak internal pull down	
PU	Enable
PD	Disable (default)

SMBUS



EMI-GX501GI

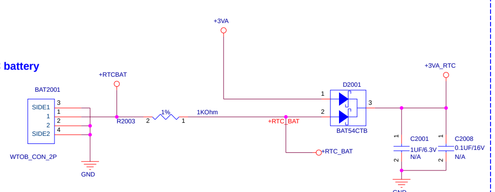




CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)

TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)

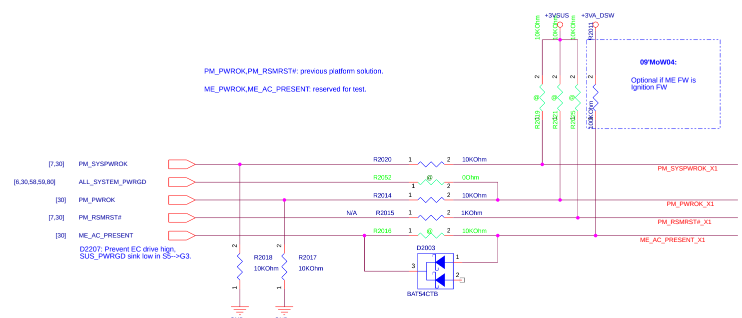
RTC battery



1st :12017-00020200
2nd :12G17100002C
USE RTC Battery:
P/N: 0B100-00040500 BATT-LI CR1220 3V

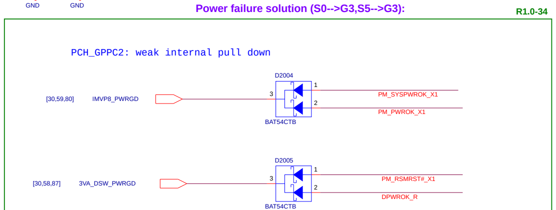
PM_PWROK,PM_RSMRST#: previous platform solution.

ME_PWROK,ME_AC_PRESENT: reserved for test.

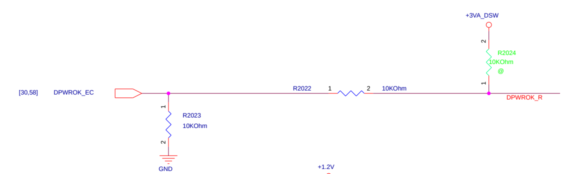


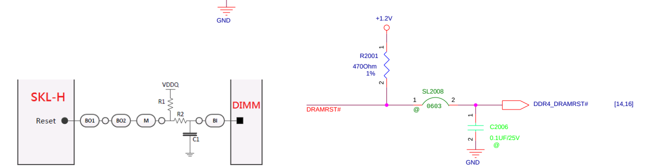
Power failure solution (S0-->G3,S5-->G3):

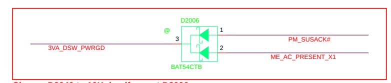
R1.0-34



Power failure solution (S0-->G3,S5-->G3):







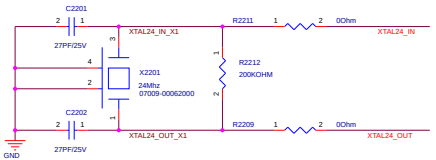
Change D2040 to 10Kohm if mount D2006

R1.1-03

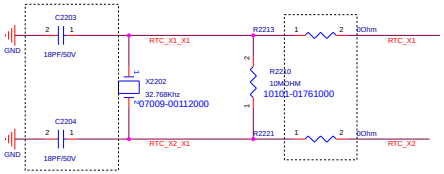
Deep SX discharge (S0-->DSX,S5-->DSX)

Project Name	G711GW	Rev 1.0
Title :	PCH-CPT(1)SATA,IHDA,RTC,JTAG	Size Custom
Dept.:	ASUSTeK COMPUTER	Engineer: Gaming RD
Date:	Tuesday, April 16, 2019	Sheet 20 of 103

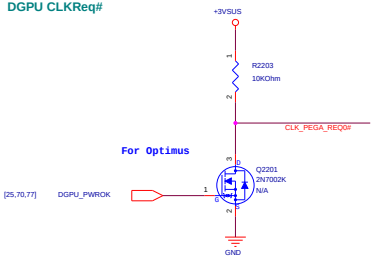
XTAL 24MHz



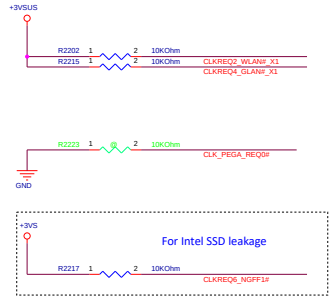
RTC CRYSTAL 32.768KHz

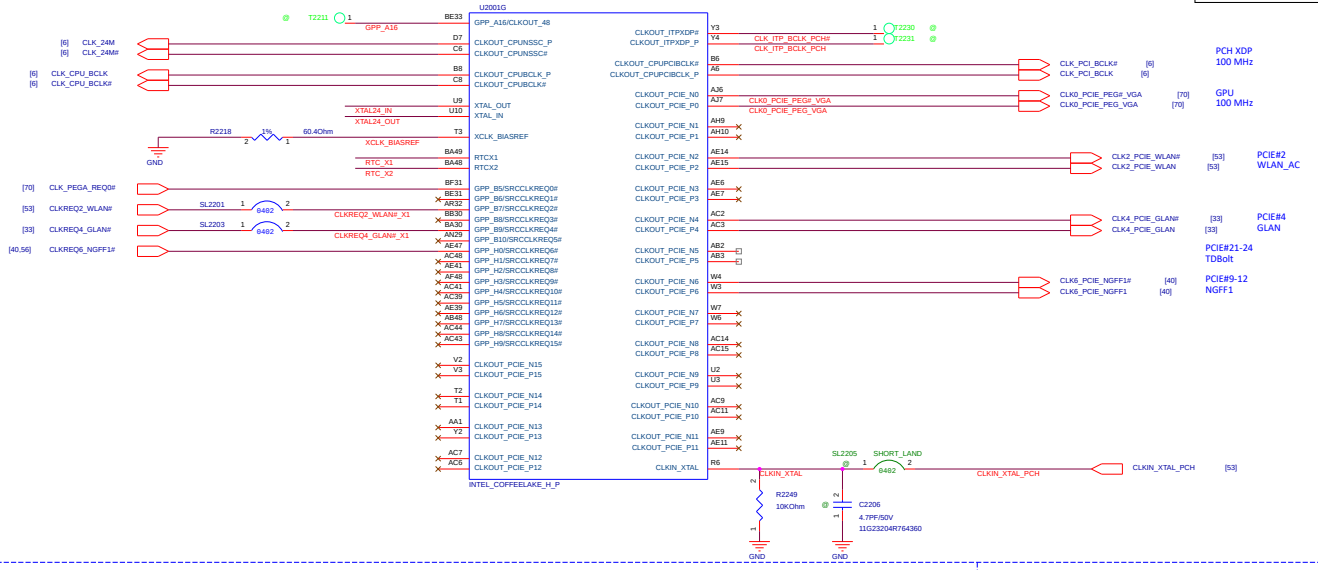


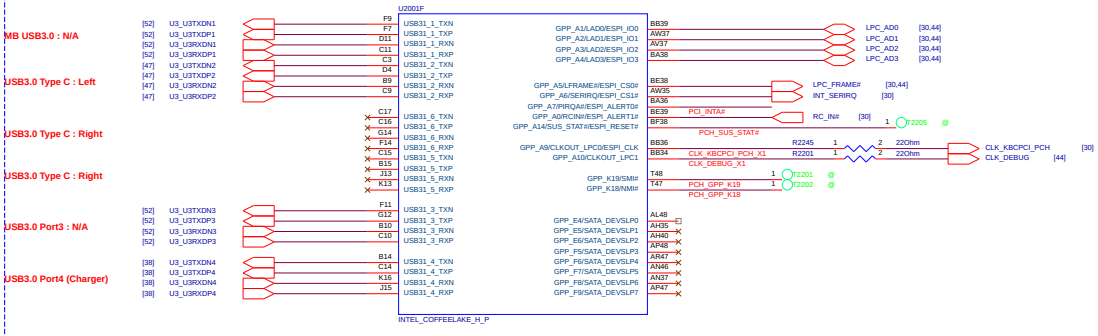
DGPU CLKReq#



PCH CLKREQ Setting:







ASUS	Project Name: G711GW		Rev: 1.0
Title :	PCH-CPT(3)_FDI,DMI,SYS PWR		
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer:	Gaming RD
Date: Tuesday, April 16, 2019	Sheet 22 of 103		

HPD0 to DP

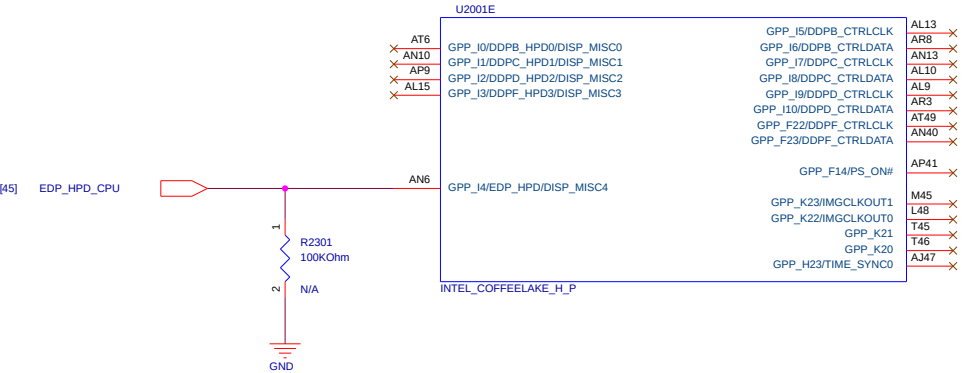
HPD1 to HDMI

HPD2 to TBT

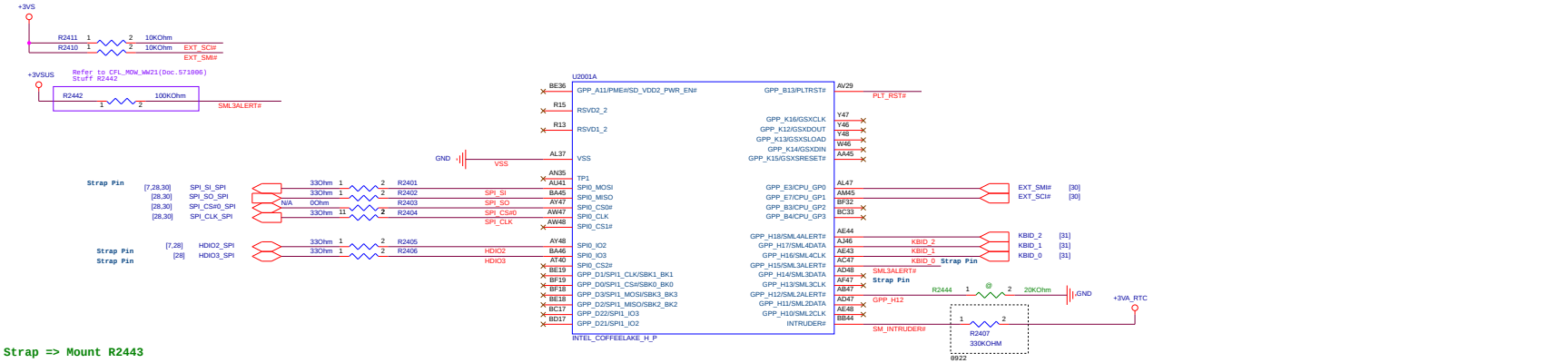
HPD3 to VGA

HPD4 to EDP Panel

DDP Strap Setting Update：
0 = Port is not detected (Default)
1 = Port is detected

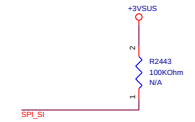


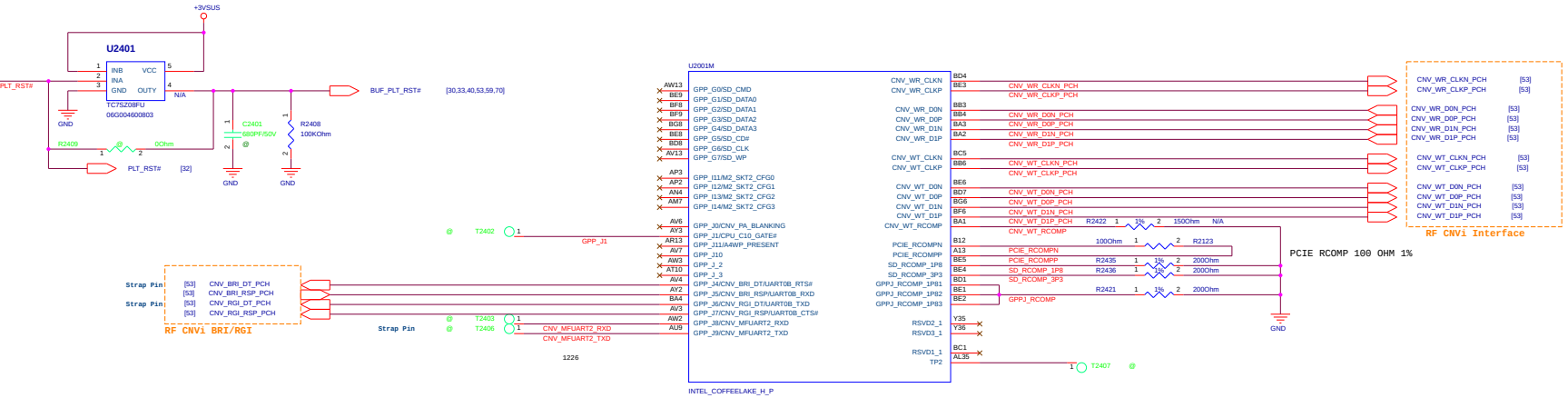
ASUS	Project Name: G711GW		Rev: 1.0
Title : PCH-CPT(4)_eDP,PCI,DP			
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Tuesday, April 16, 2019	Sheet 23 of 103		



Strap => Mount R2443

This strap should sample high,
if sample low will cause boot up fail.





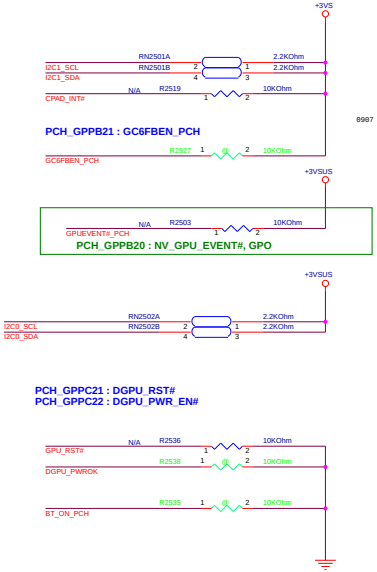
GPP_J6:
Do not leave this pin float,
if CNVi is not used, it still need a 20K ohm PU.

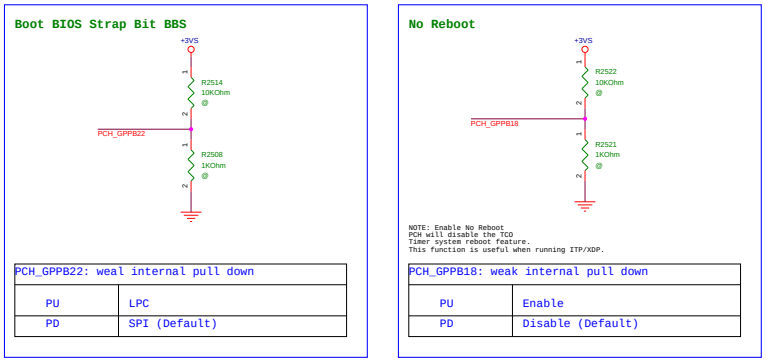
[CNV Mode Select] CNV_RGI_DT_PCH
An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.

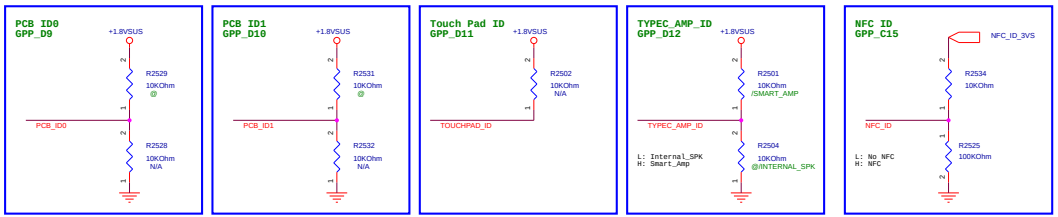
GPP_J6(CNV_RGI_DT):
An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.
[Intel PAE]
RGI_DT has an automatic detect CNVi mechanisim,
please do not use external PD.
The CRF has an internal strong 1K PD already.
Do not leave this pin float,
if CNVi is not used, it still need a 20K ohm PU

GPP_J9:
The signal has a weak internal pull-down
0 = VCCSPI is connected to 3.3V rail
1 = VCCSPI is connected to 1.8V rail

ASUS	Project Name: G711GW		Rev: 1.0
Title : PCH-CPT(5)_LPC,SPI,SMBUS			
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Tuesday, April 16, 2019	Sheet 24 of 103		







X-tal Frequency Select

Cannon Lake PCH-LP

- XTAL_Freq_Select = GPP_H21
- Pin Strap for XTAL frequency selection
- An external 4.7k to 10k Ohm +/-5% pull-up to VCC (1.8V or 3.3V) is required on this strap for PCH 24 MHz XTAL operation

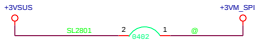
Cannon Lake PCH-H

- XTAL_Freq_Select = GPP_J4
- Pin Strap for XTAL frequency selection
- An external 4.7k to 10k Ohm +/-5% pull-up to VCC (1.8V or 3.3V) is required on this strap for PCH 24 MHz XTAL operation

Project Name	G711GW		Rev 1.0
Title :	PCH-CPT(6)_GPIO,MISC		
Size Custom	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Tuesday, April 16, 2019	Sheet 25 of 103		

Project Name: G711GW		Rev: 1.0
Title : PCH-CPT(8)_POWER,GND		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD
Date: Tuesday, April 16, 2019	Sheet 27 of 103	

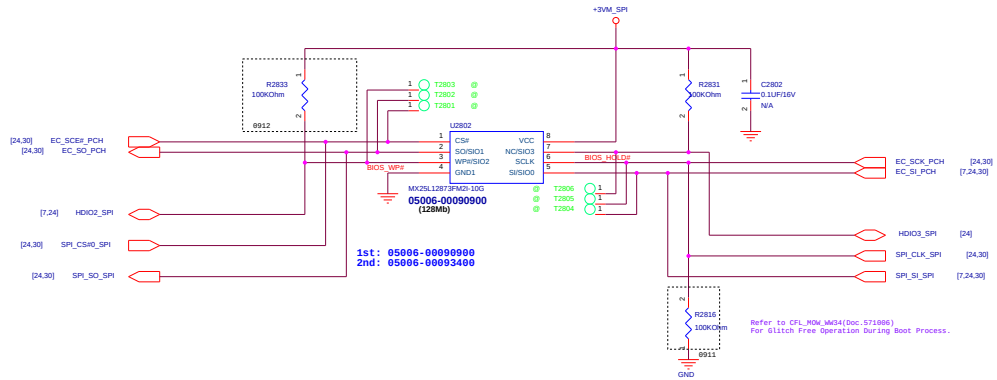
SPI Power



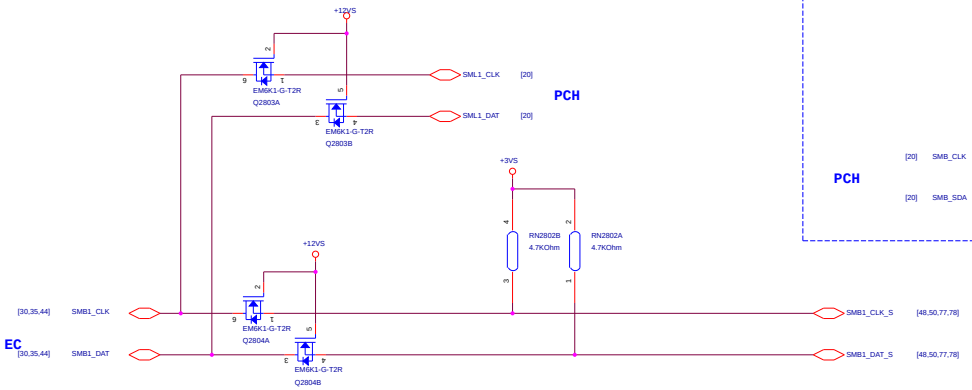
1st SPI ROM

1st: 05006-00090900 FLASH MXIC MX25L12873FM2I-10G 128M SOP-8L
2nd: 05006-00093100 FLASH GD25B127DSIGG IGADEVICE 128MB SOP8

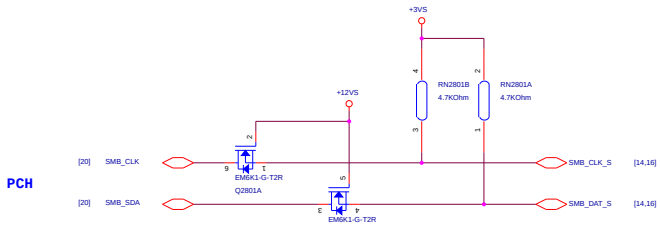
Main Board

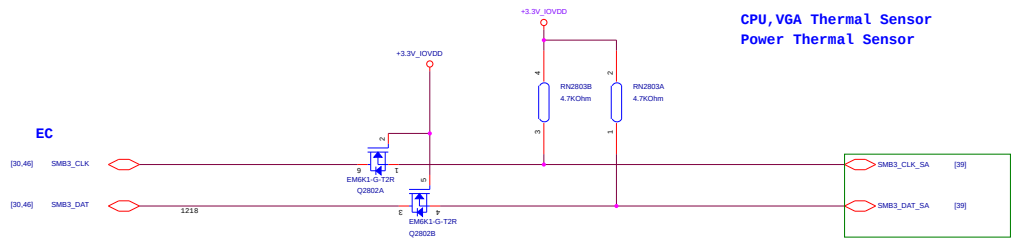


System Management Interface



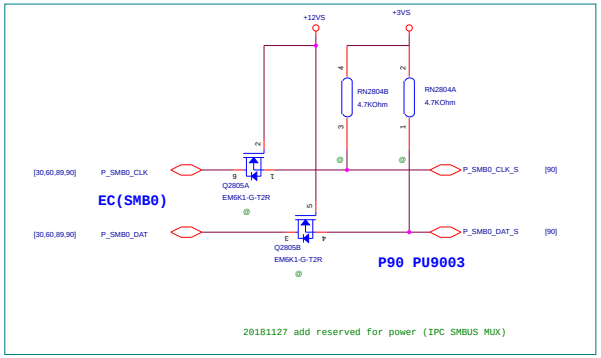
SMBus Interface





CPU,VGA Thermal Sensor
Power Thermal Sensor

for smart amp



20181127 add reserved for power (IPC SMBUS MUX)

ASUS	Project Name: G711GW		Rev: 1.0
Title : PCH-SPI ROM,OTH			
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Tuesday, April 16, 2019	Sheet 28 of 103		

ASUS	Project Name: G711GW	Rev: 1.0
Title : PCH-XDP		
Size: A	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD
Date: Tuesday, April 16, 2019	Sheet 29 of 103	

EC 8995

Only 3V Torlence

GPB[0,1,2,3,4,5,6]
GPC[3,4,5,6,7]
GPD[0,4,6,7]
GPE[4]
GPF[6,7]
GPH[7]
GPI [0 :7]
GPJ[0:7]

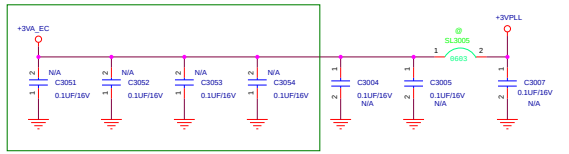
Can be adjusted to Open-Drain for port:

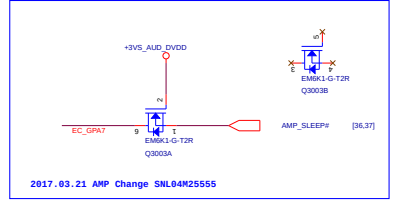
GPA0~GPA3
GPB0~GPB7
GPD0~GPD7
GPE0~GPE7
GPF0~GPF7
GPH0~GPH6
GPJ0~GPJ5

EC Require

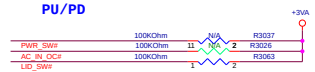
Power

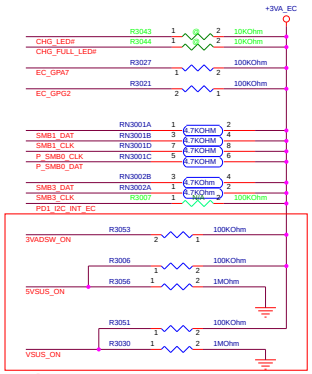
R1.0-29



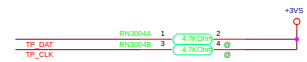


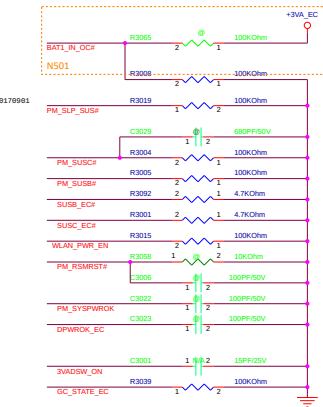
PU/PD



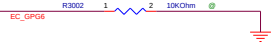


for load code





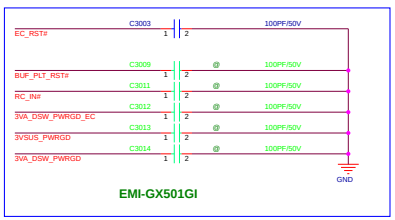
N key



Battery

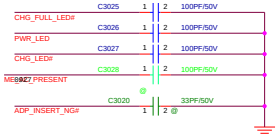
Thermal sensor

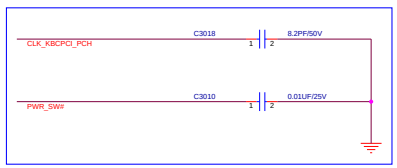
ITE Version	ASUS P/N
IT8225VG/BX	06037-00260000



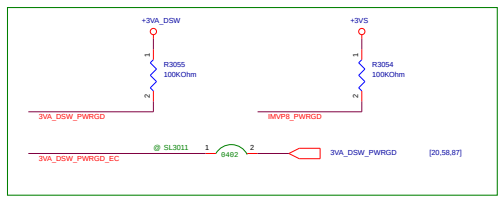
EMI-GX501GI

For EMI





R1.0-34

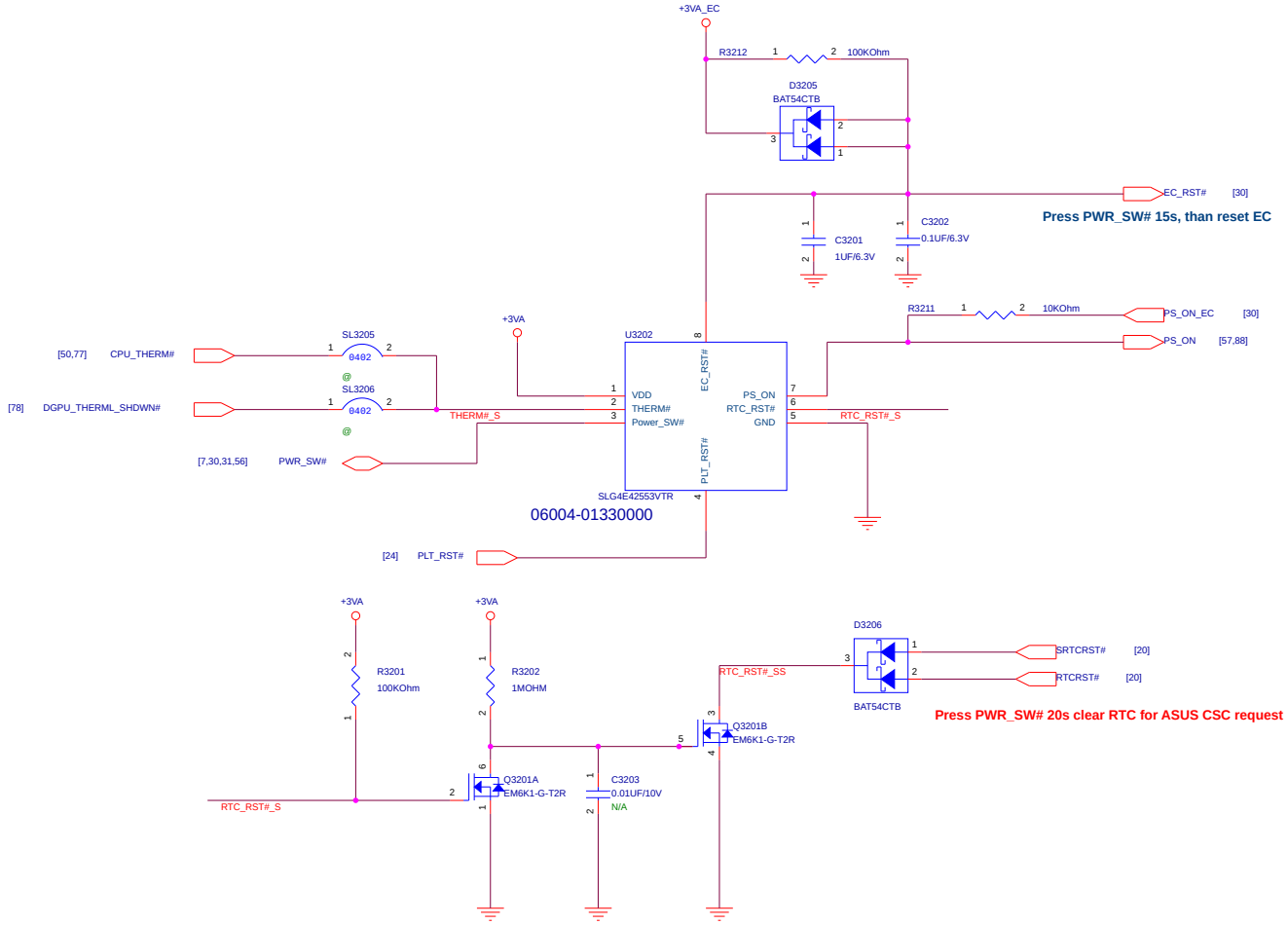


Modern standby project should use Silego solution for EC/RTC reset (Microsoft hardware requirements)

6.6.2 Power button behavior

https://docs.microsoft.com/en-us/windows-hardware/design/minimum/minimum-hardware-requirements-overview#section-60---shared-minimum-hardware-requirements-for-components

UX362FA R1.3 board will verify this circuit 7/E



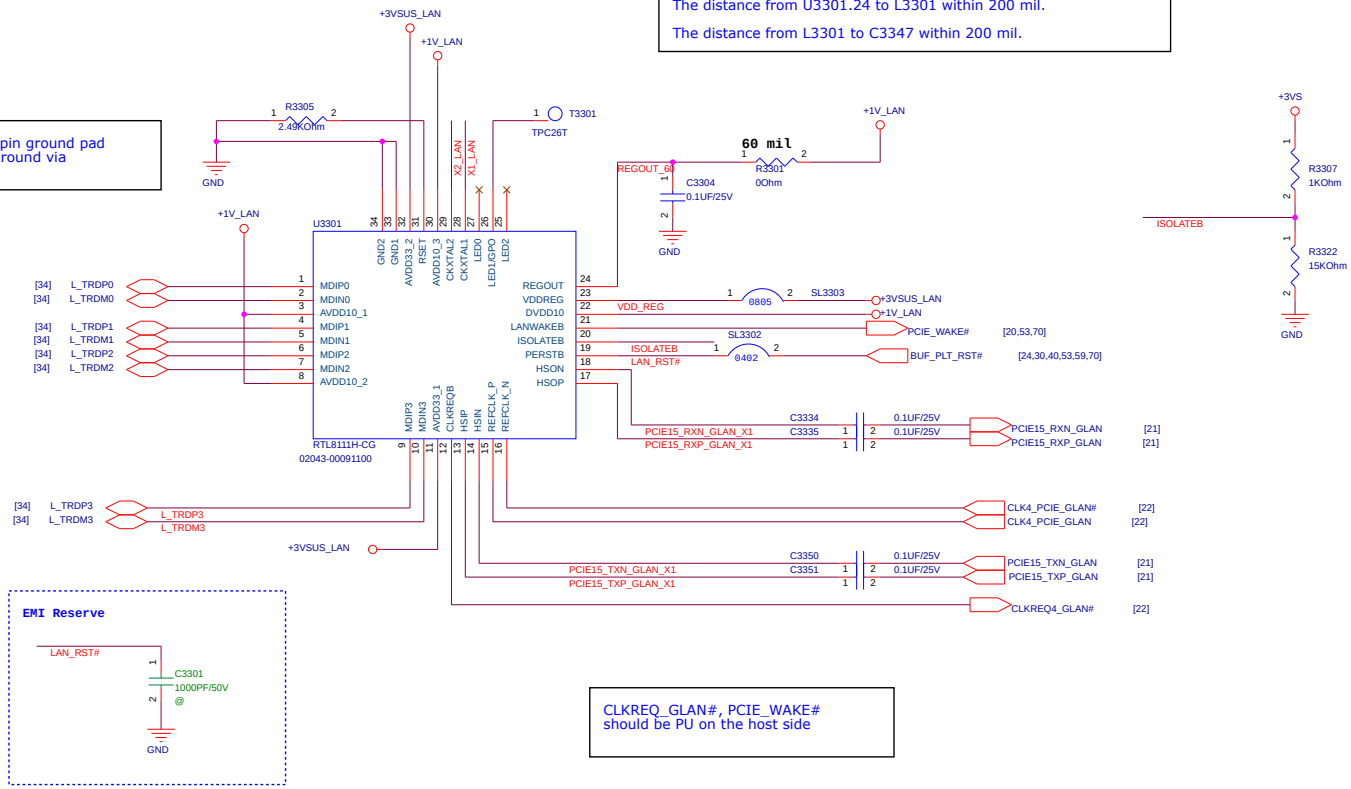
<Variant Name>

ASUSTeK COMPUTER	Title : RST_Reset Circuit	
	Engineer: Gaming RD	
Size: B	Project Name: G711GW	Rev: 1.0
Date: Tuesday, April 16, 2019	Sheet 32 of 103	

The distance from U3301.24 to L3301 within 200 mil.

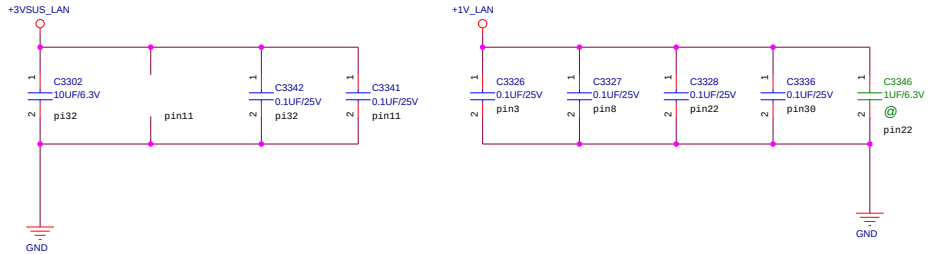
The distance from L3301 to C3347 within 200 mil.

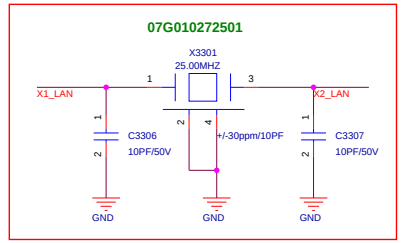
33/34 pin ground pad
need ground via



EMI Reserve

CLKREQ_GLAN#, PCIE_WAKE#
should be PU on the host side



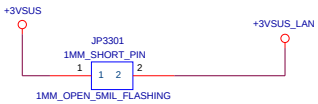


X3301: 25MHZ +/-30ppm/10pF (3225)

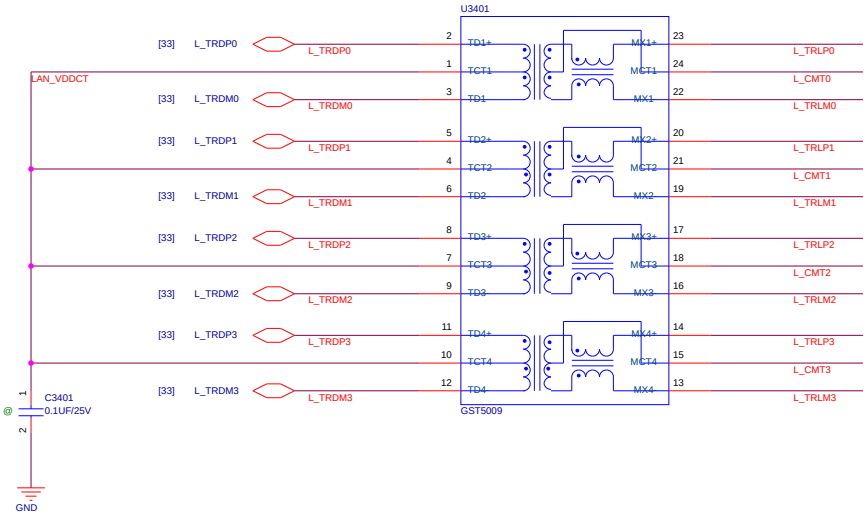
1st: P/N:07G010272501 TXC/7V25000011

2nd: P/N:07G010952500 HOSONIC/E3FB25

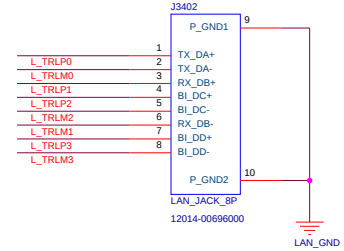
Realtek suggests 3V_LAN raise time >1ms

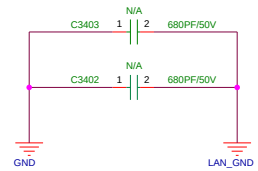


ASUS	Project Name: GX502GX	Rev: 1.0
Title : LAN RTL8111GUX-CG		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: NB1 RD2 EE1
Date: Tuesday, April 16, 2019	Sheet 33 of 103	

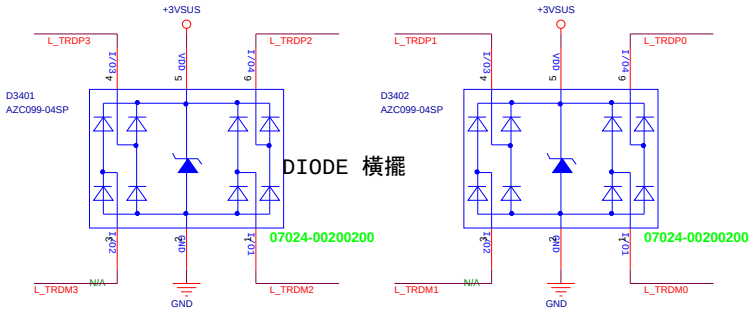


LAN Connector





Place near chassis GND



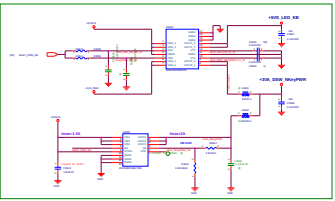
D3401,D3402 ESD Diode

1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

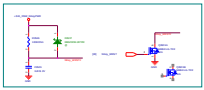
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

ASUS	Project Name: GX502GX	Rev: 1.0
Title : LAN_RJ45_CON		
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: NB1 RD2 EE1
Date: Tuesday, April 16, 2019	Sheet 34 of 103	

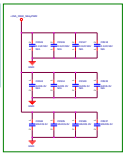
N_KEY_IT8299E

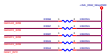


For EC Reset N_key



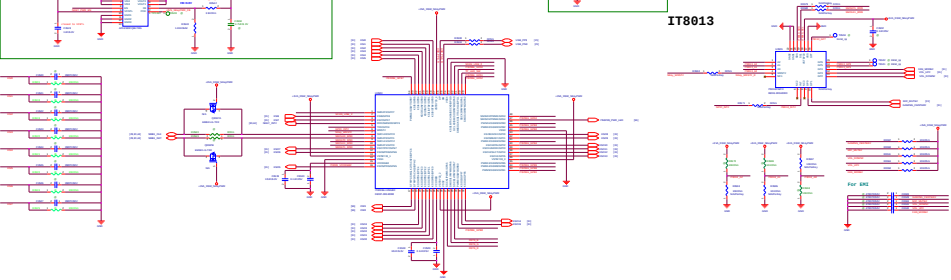
Nkey_Power



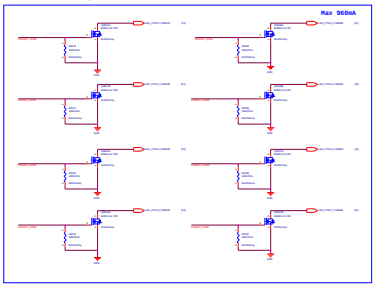


IT8299E

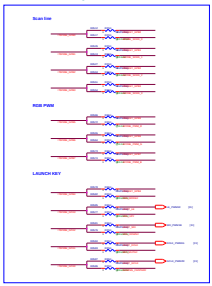
IT8013



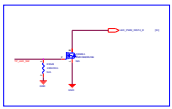
KB RGB Per Key LED



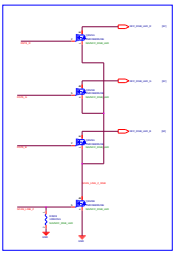
KB RGB co-layout



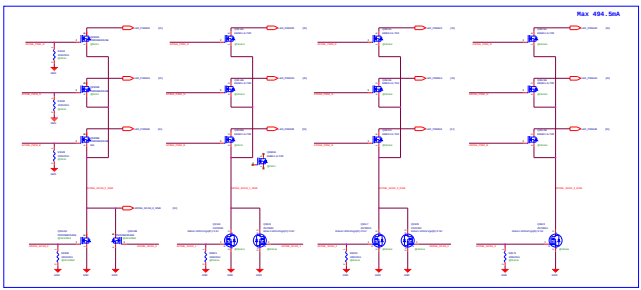
TP LED



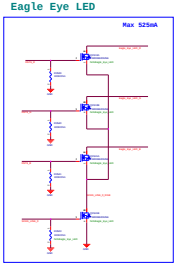
NFC RGB LED



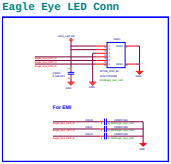
KB RGB 4Zone and 1Zone LED

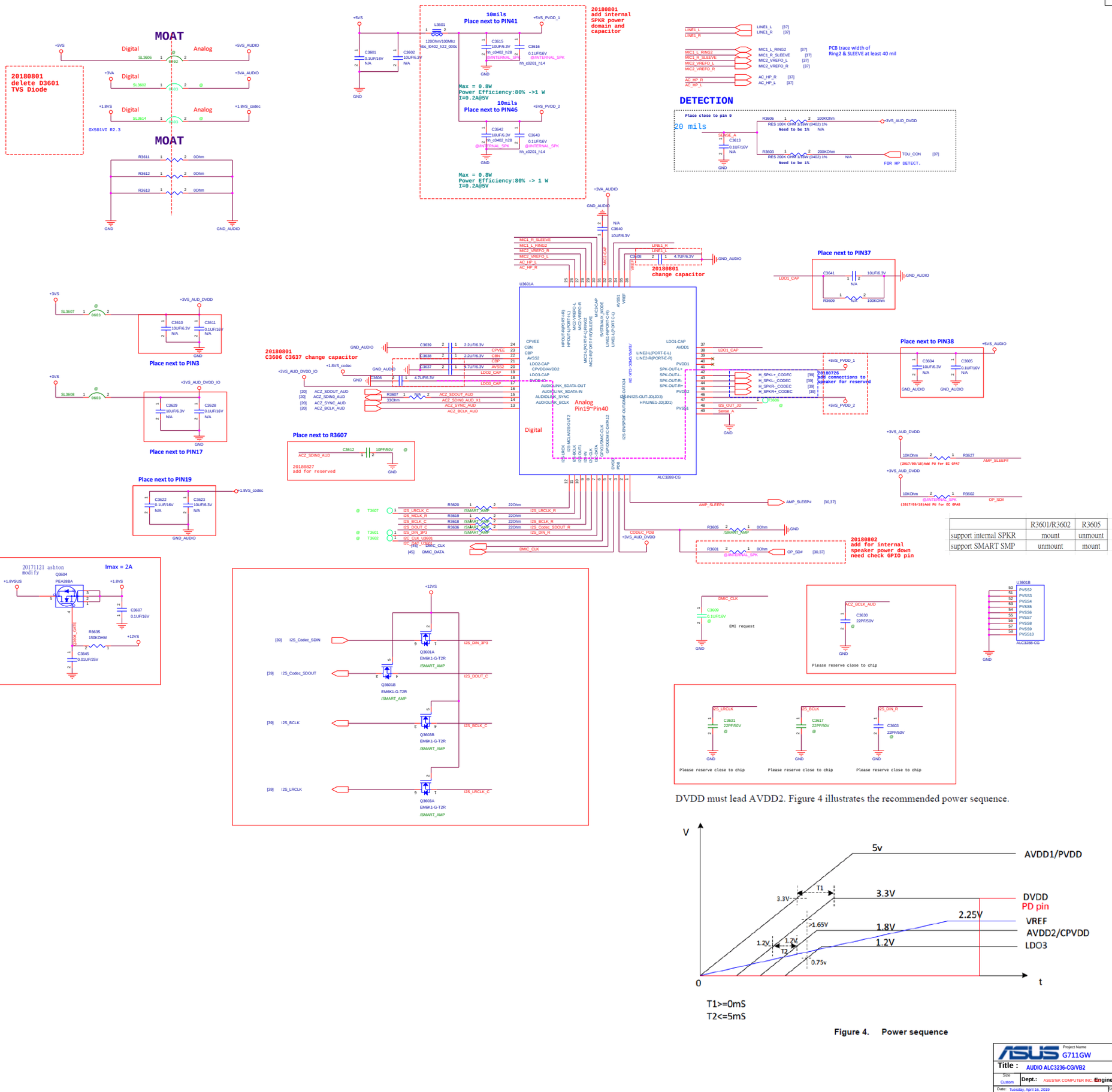


Eagle Eye LED



Eagle Eye LED Conn



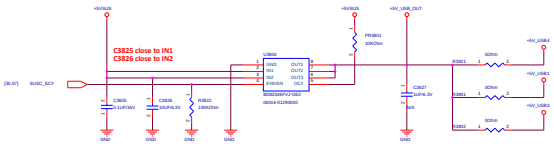


	R3601/R3602	R3605
support internal SPKR	mount	unmount
support SMART SMP	unmount	mount

DVDD must lead AVDD2. Figure 4 illustrates the recommended power sequence.

Figure 4. Power sequence

Project Name	G711GW		Rev 1.0
Title :	AUDIO ALC3236-CG/VB2		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Marshall Li	
Date: Tuesday, April 16, 2019	Sheet 36 of 103		



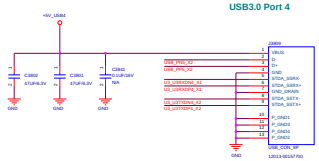
USB3.0_PORT4 (Support USB Charge Circuit)

J3809 USB3.0 Connector

1st Source: P/N:12013-00018300 FOXCONN/UEA1111-N40AM2-7H

2nd Source: P/N:12013-00080400 SINGATRON/2UB4006-310101F

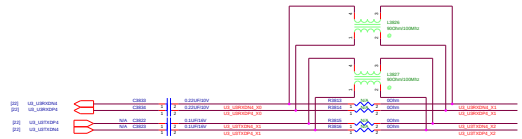
USB3.0 Port 4

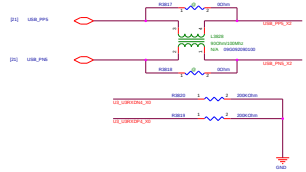


USB3.0 Pin define	
1	VBUS
2	D-
3	D+
4	GND
5	RX-
6	RX+
7	GND
8	TX-
9	TX+

USB Charge Circuit (For PORT 4)

USB3.0_PORT4

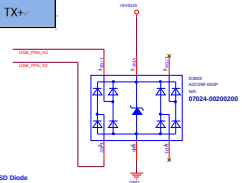




USB3.0 ESD-Protection

1st : 07G028076030
ESD PROTECTION AZ1045-04F

2nd : 07G028153010
ESD PROTECTION IP4284CZ10-TB

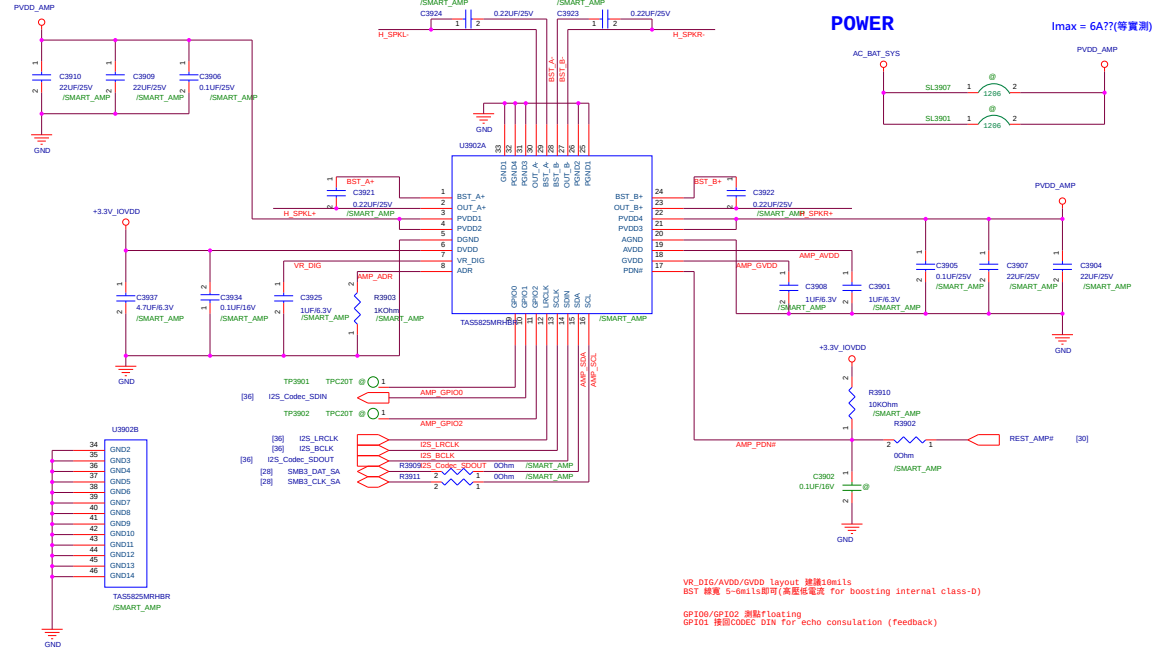


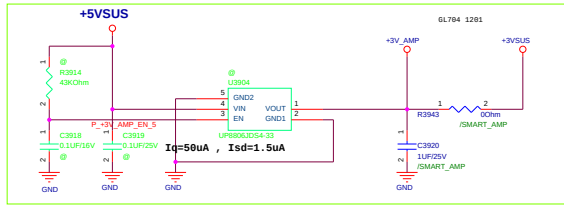
D3802 ESD Diode

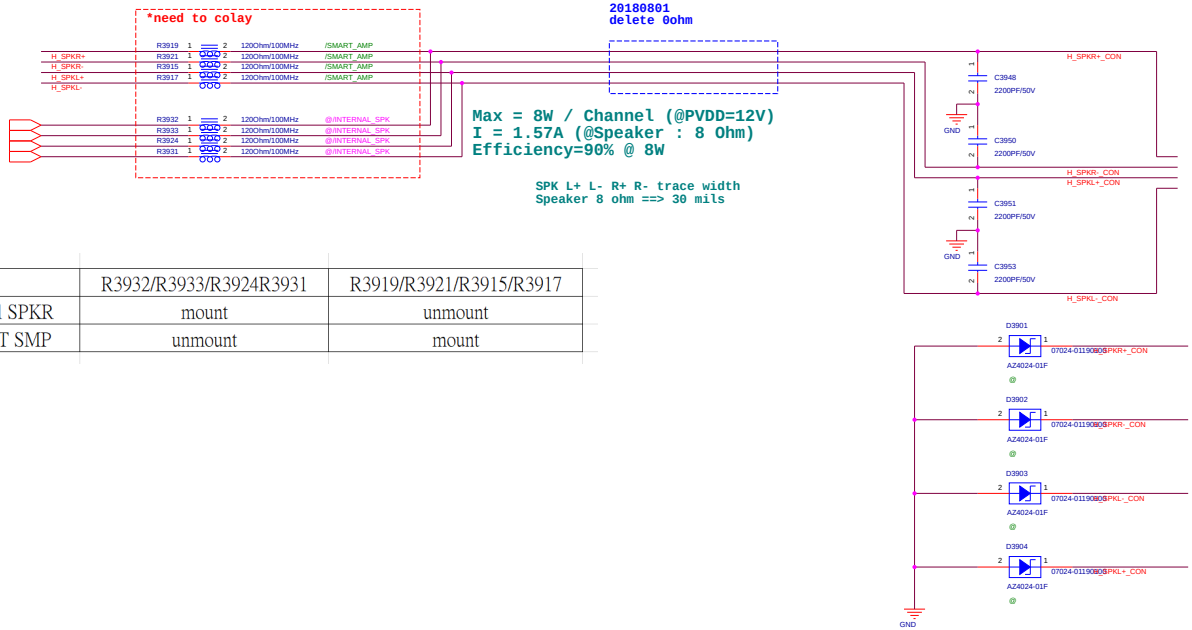
1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

ASUSTeK COMPUTER	Title :	Aud_HP Jack_MIC	
	Engineer:	Gaming RD	
Size: D	Project Name: G711GW		Rev: 1.0
Date: Tuesday, April 09, 2019	Sheet 38 of 45		





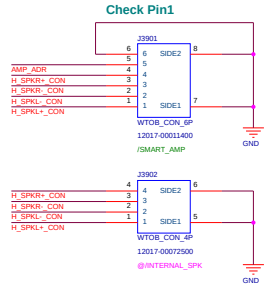


	R3932/R3933/R3924R3931	R3919/R3921/R3915/R3917
support internal SPKR	mount	unmount
support SMART SMP	unmount	mount

20180823
add

INTERNAL SPK Conn.

Speaker = 1.5W / channel



<Variant Name>

ASUSTeK COMPUTER INC. NB1

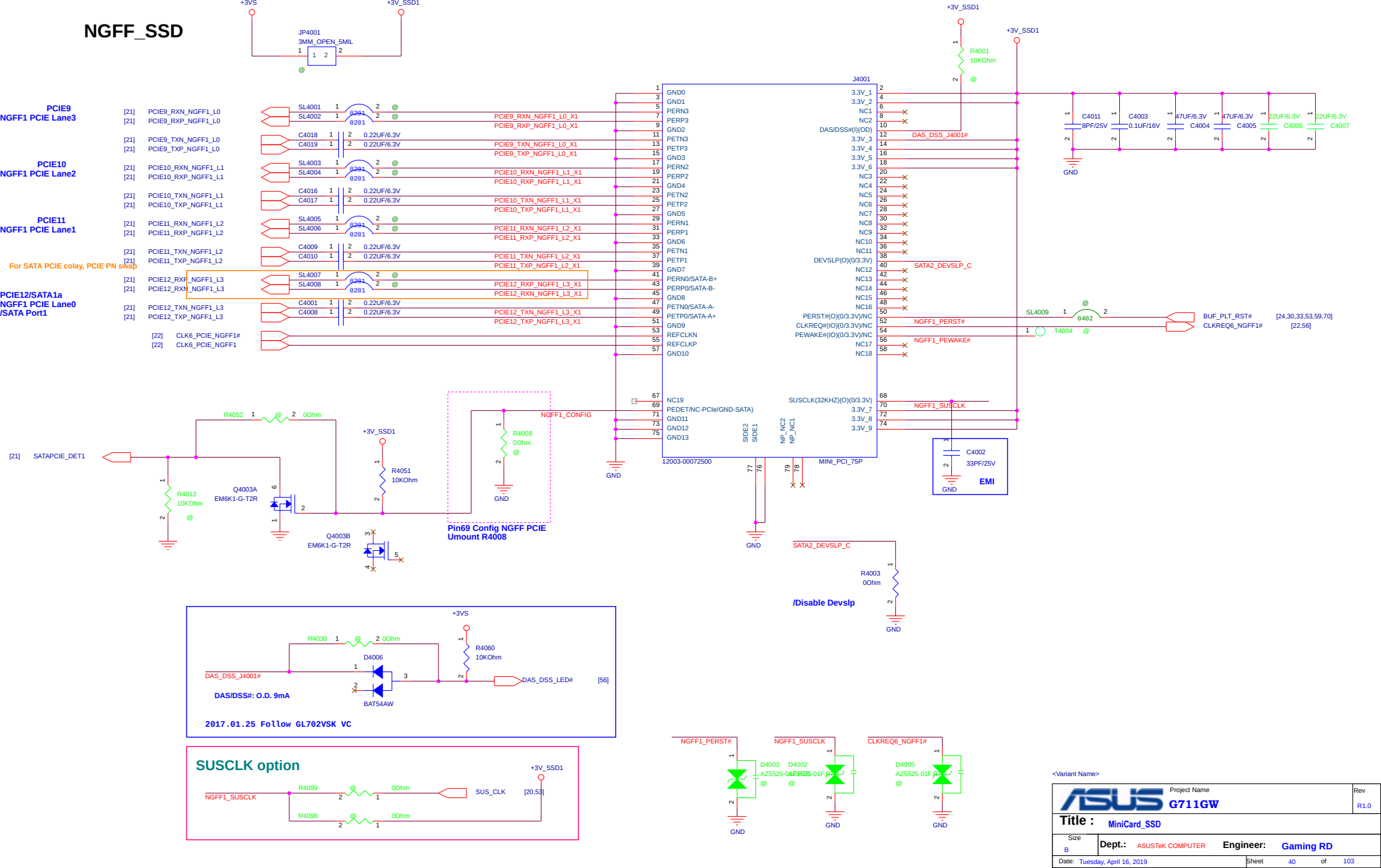
Title : Aud_Woofer_**

Engineer: EE

Size	Project Name	Rev
C	G711GW	1.0

Date: Tuesday, April 16, 2019 Sheet 39 of 103

NGFF_SSD



<Variant Name>

Project Name: G711GW		Rev: R1.0
Title : MiniCard_SSD		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD
Date: Tuesday, April 16, 2019	Sheet 40 of 103	

<Variant Name>

Title : CB_*****

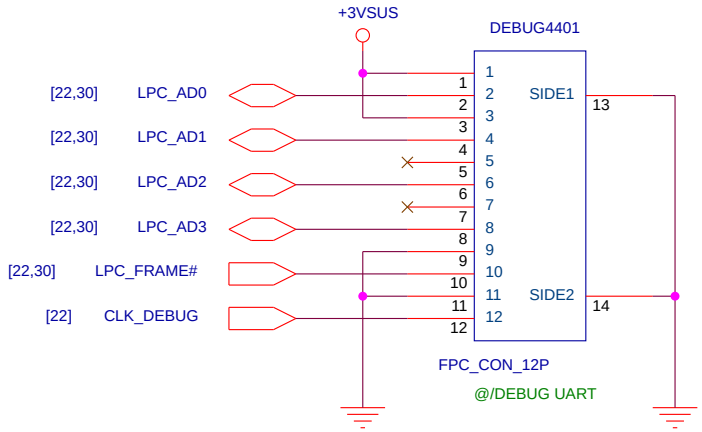
ASUSTeK COMPUTER

Engineer: Gaming RD

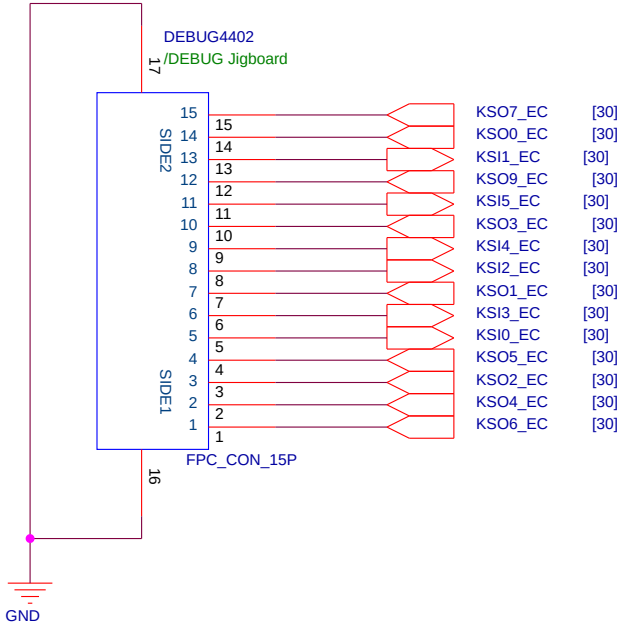
Size	Project Name	Rev
C	**G711GW**	1.0

Date:	Tuesday, April 16, 2019	Sheet	41	of	103

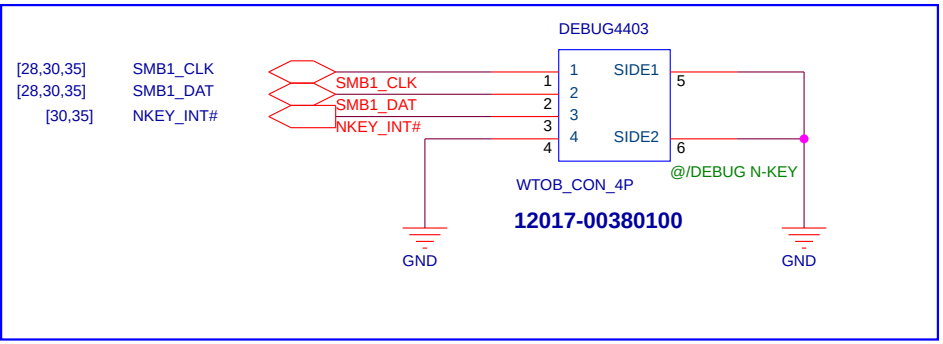
LPC Debug Port



ER2 stuff



N-KEY Debug Connector



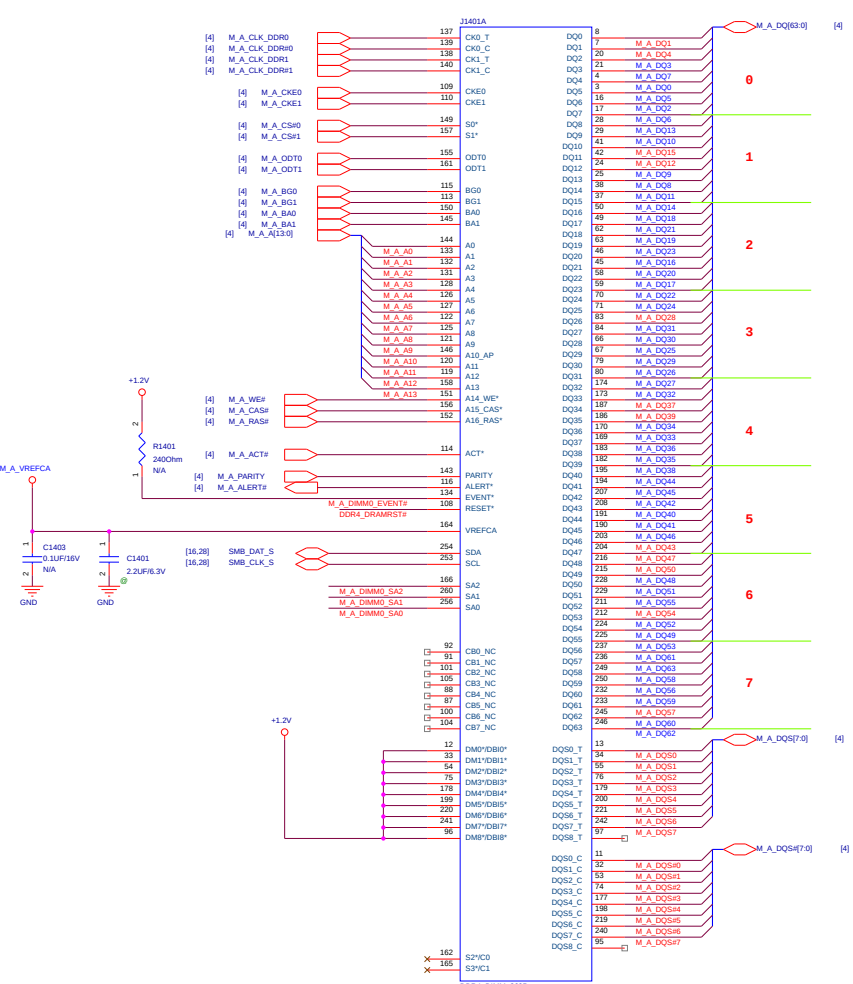
<Variant Name>

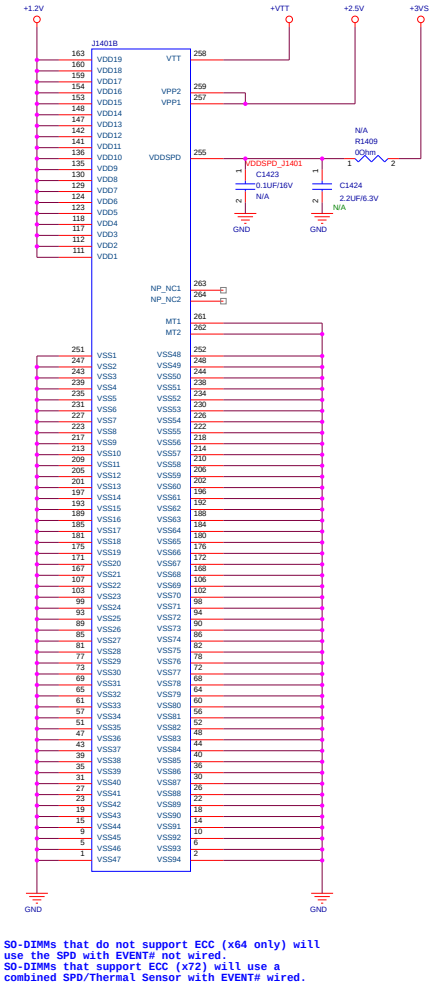
ASUSTeK COMPUTER	Title : DEBUG_LPC	
	Engineer: Gaming RD	
Size: A	Project Name: G711GW	Rev: 1.0
Date: Tuesday, April 16, 2019	Sheet 44 of 103	

Chris

SODIMM CHA-DIMM0
TOP H4.0mm REV (J1401)

Main Board

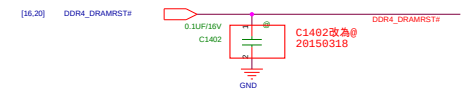


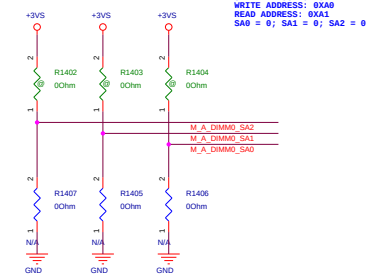


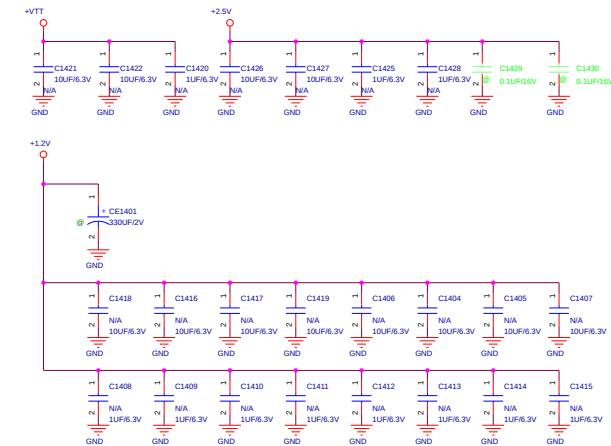
SO-DIMMs that do not support ECC (x64 only) will use the SPD with EVENT# not wired.
SO-DIMMs that support ECC (x72) will use a combined SPD/Thermal Sensor with EVENT# wired.

DDR4_DIMM_260P

EVENT# ON ECC DIMM: KEEP A PULL UP IF NO PIN IN PCH







ASUS	Project Name: G711GW		Rev: R1.0
Title :	DIM_DDR4 SO-DIMM A1		
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Tuesday, April 16, 2019	Sheet 14 of 103		

Max:200mA

+3VSUS_MUX

From GPU
90 ohm

To Type C Connector
90 ohm

U4703_29

Table 4-7. EN is the channel enable pin

EN	Channel Enable Setting
0	Disabled
1	Enabled (Default)

06113-00340000

20180727
modify net name

Slave address : 0xA0

20180723
change to unmount

USB EMI-Protection

20180726
delete L4705/4706/4707

20180803
change VBUS capacitor

20180726
add type-c 5V VBUS power switch

C4710 close to VDD
C4711 close to VIN

CC pin
OVP Protection

20180727
delete CC pin OVP because do not support PD 20V

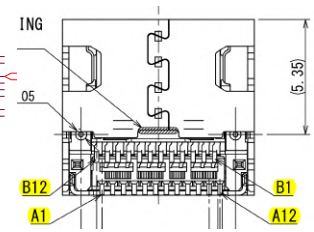
USB3.0
ESD-Protection

NOTE 8. PIN ASSIGNMENT (FRONT VIEW)

Pin No.	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
	GND	TX1+	TX1-	V_{BUS}	CC1	D+	D-	SBU1	V_{BUS}	RX2-	RX2+	GND
Pin No.	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1
	GND	RX1+	RX1-	V_{BUS}	SBU2	D-	D+	CC2	V_{BUS}	TX2-	TX2+	GND

NOTE 9. LASER WELD POINTS MAY BE DISCOLORED.

TYPE-C Connector



USB2.0
ESD-Protection

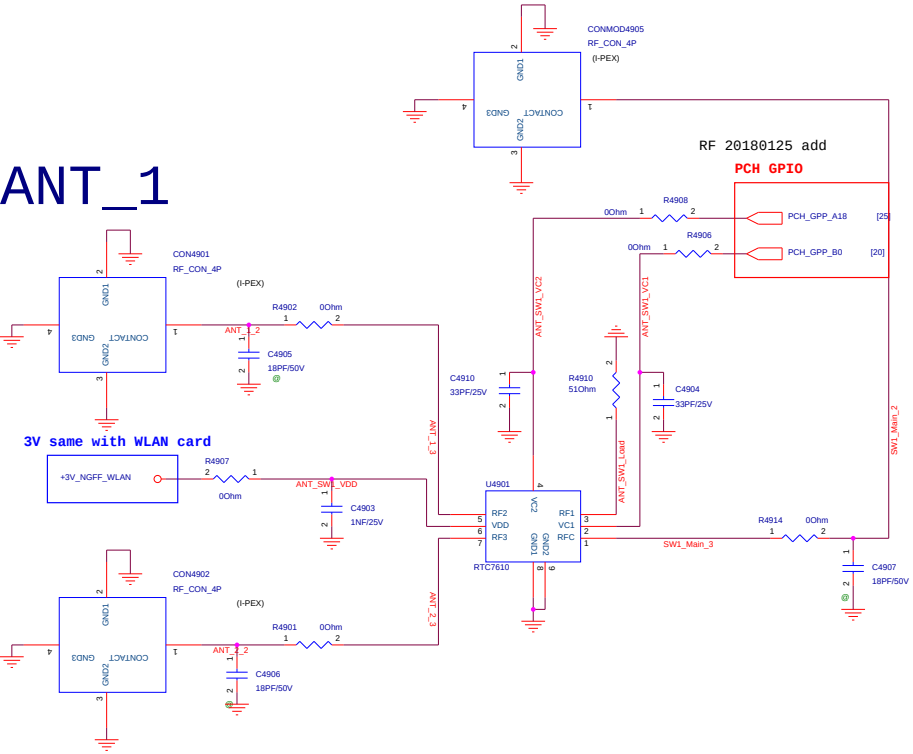
PD Discharging

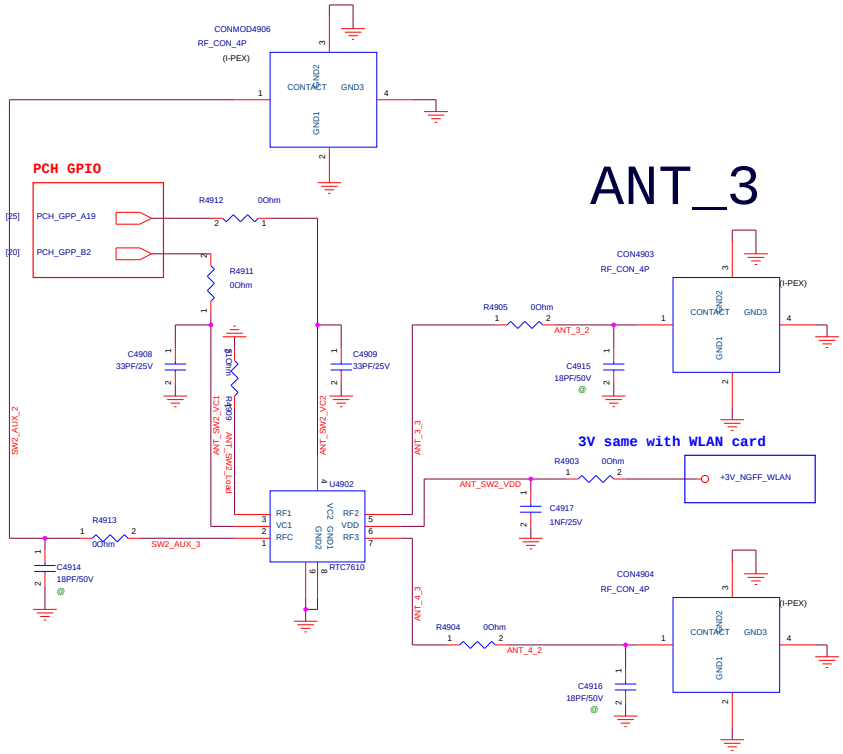
20180801
no PD function, delete discharging circuit

ASUS	Project Name: G711GW		Rev: 2.0
Title :	TYPE-C USB3.1_R1.5_4		
Dept.:	ASUSTeK COMPUTER INC.	Engineer: Ashton_yang	
Date: Tuesday, April 16, 2019	Sheet: 47 of 103		

Module_AUX

Module_MAIN





U4901 RTC7610			
ANT	Port	VC1 GPP_B0	VC2 GPP_A18
50 Ω	RF1	1	0
ANT_1	RF2	X	1
ANT_2	RF3	0	0

X: don't care
0: -0.2v~0.3v
1: 1.6v~3.6v

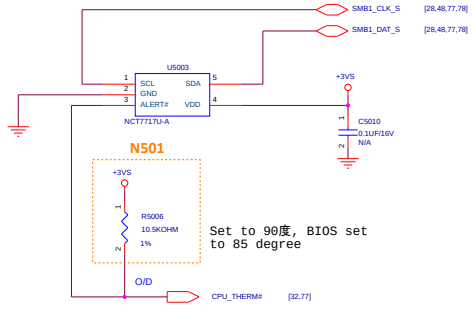
U4902 RTC7610			
ANT	Port	VC1 GPP_B2	VC2 GPP_A19
50 Ω	RF1	1	0
ANT_3	RF2	X	1
ANT_4	RF3	0	0

X: don't care
0: -0.2v~0.3v
1: 1.6v~3.6v

<Core Design>

ASUS	Project Name GX502GX	Rev 1.0
Title : ANT		
Size C	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Tuesday, April 16, 2019	Sheet 49 of 103	

CPU Thermal Sensor

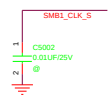


Set to 90度, BIOS set to 85 degree

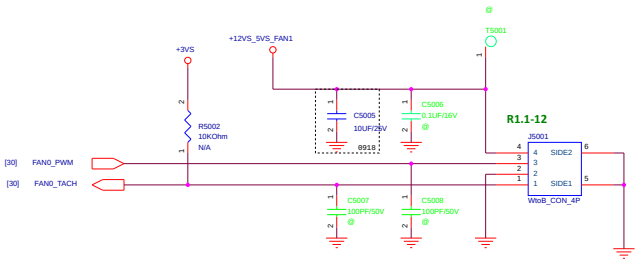
SMBUS address=10010000 (90)

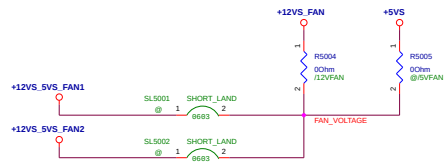
Temp.	Resistor
75	2kOhm
90	7.5kOhm
100	10.5kOhm
105	14kOhm
110	18.7kOhm

Reserve for powr noise



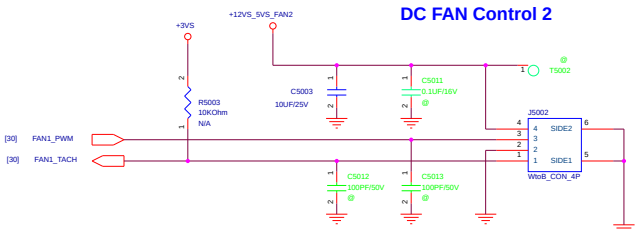
DC FAN Control 1





1st: 12017-00330300
2nd :12G171010049

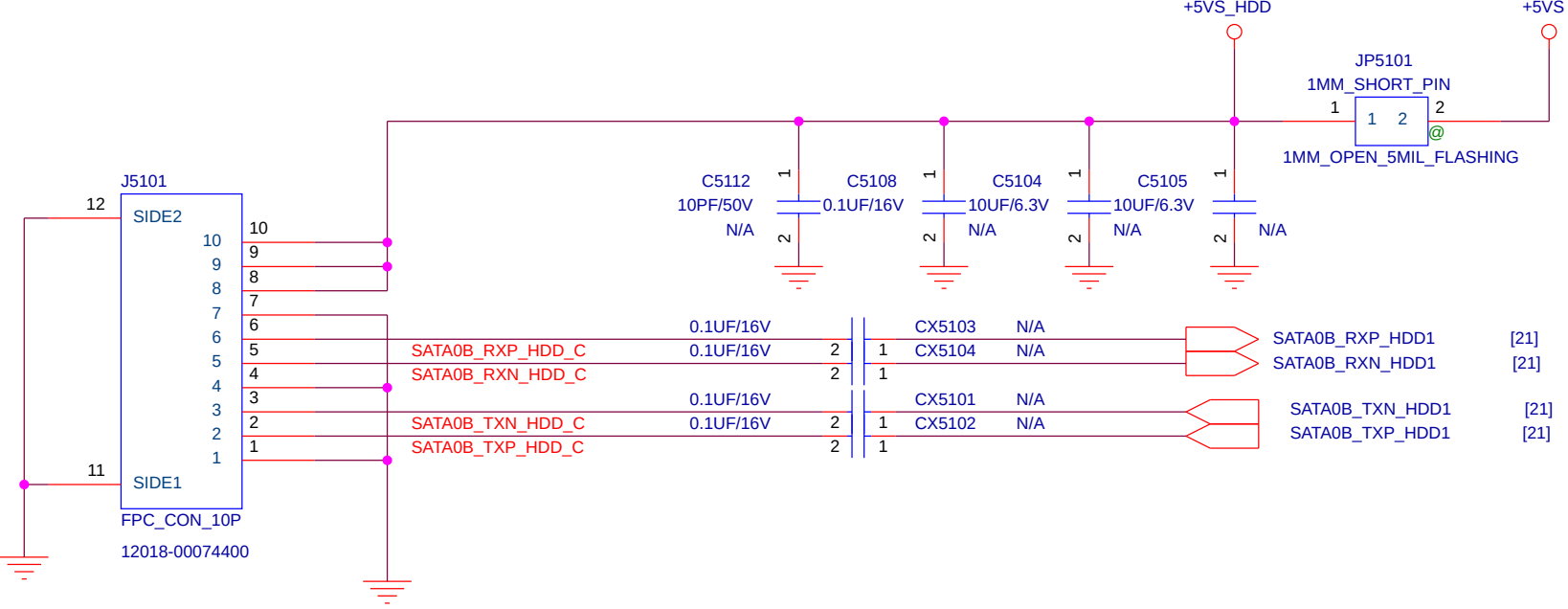
DC FAN Control 2



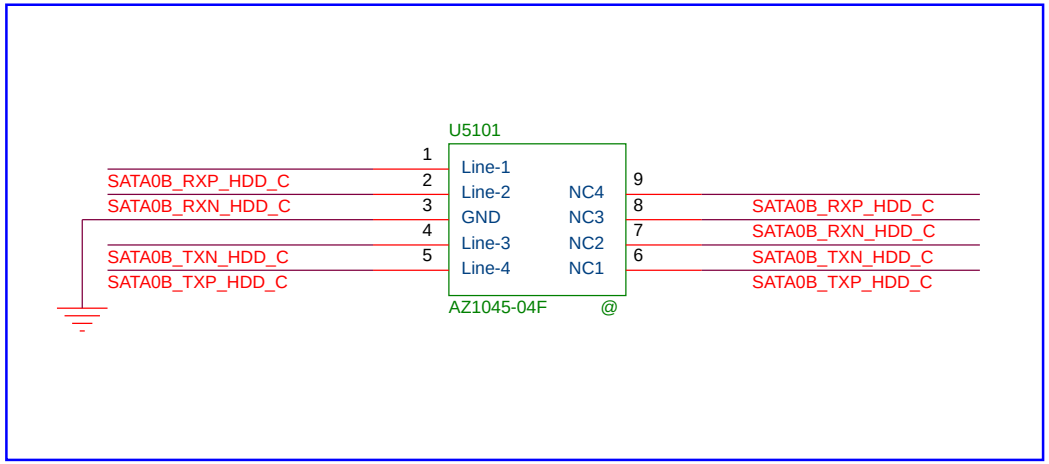
1st: 12017-00330300
2nd :12G171010049

<Variant Name>

ASUSTeK COMPUTER	Title : FAN_Thermal Sensor & Fan	
	Engineer: Gaming RD	
Size: C	Project Name: G711GW	Rev: 1.0
Date: Tuesday, April 16, 2019	Sheet 50 of 103	



PIN #	Description
1	5V
2	5V
3	5V
4	GND
5	RX+
6	RX-
7	GND
8	TX-
9	TX+
10	GND



<Variant Name>

ASUSTeK COMPUTER

Title : XDD_HDD & ODD CON

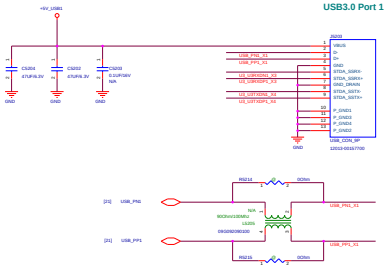
Engineer: Gaming RD

Size	Project Name	Rev
A	G711GW	R1.0

Date: Tuesday, April 16, 2019 Sheet 51 of 103

Main Board

USB3.0 Port 1



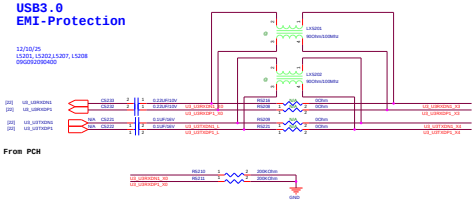
USB3.0 ESD-Protection

1st : 07G028076030
ESD PROTECTION AZ1045-04F

2nd : 07G028153010
ESD PROTECTION IP4284CZ10-TB

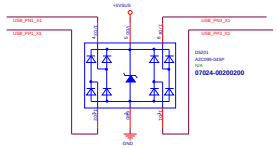
USB3.0 EMI-Protection

12/10/25
LS201, LS202,LS207, LS208
09G093209040O



From PCH

USB2.0 ESD-Protection

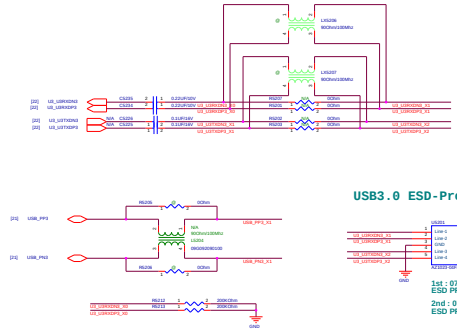


D5301 ESD Diode

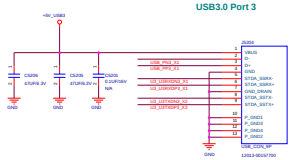
1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

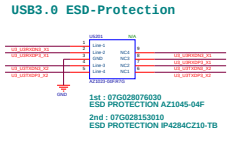
USB3.0_PORT3



USB3.0 Port 3



USB3.0 ESD-Protection



1st : 07G028076030
ESD PROTECTION AZ1045-04F

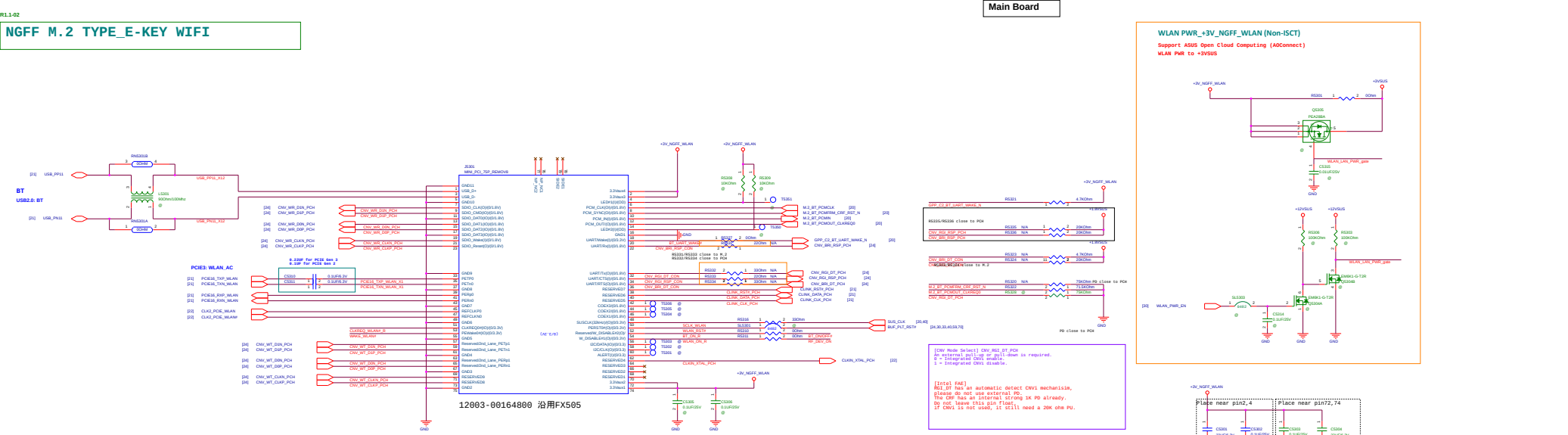
2nd : 07G028153010
ESD PROTECTION IP4284CZ10-TB

ASUSTeK COMPUTER	Title :	USB Charger
	Engineer:	Gaming RD
Size: D	Project Name: G711GW	Rev: 1.0
Date: Tuesday, April 28, 2026	Sheet: 52 of 69	

R1.1-02

NGFF M.2 TYPE_E-KEY WIFI

Main Board



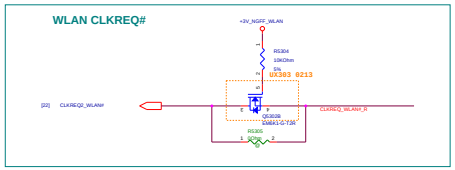
J5301_NGFF E-KEY WLAN Connector H=2.0mm

1st Source: P/N:12003-00076000 ARGOSYINASE0-S6701-TP20

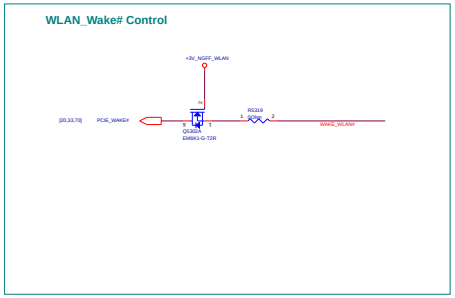
2nd Source: P/N:12003-00075200 DRAGONSTATE/213EBAA2FFB

3rd Source: P/N:12003-00075800 LOTES/APCI0062-P001A

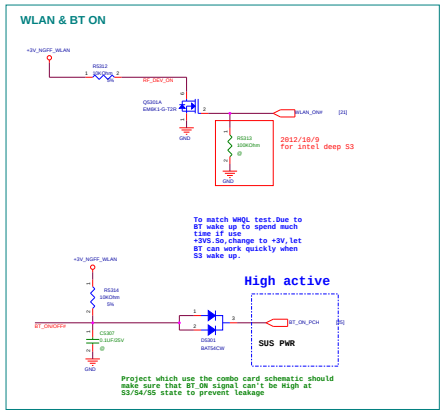
WLAN CLKREQ#



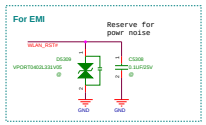
WLAN_Wake# Control



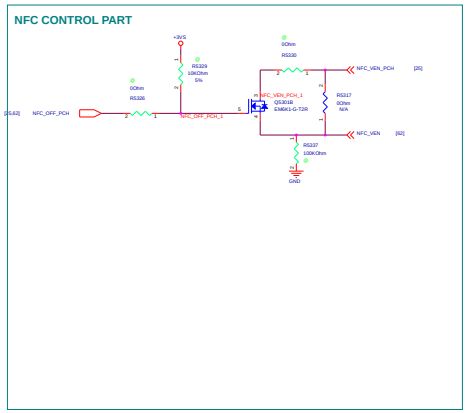
WLAN & BT ON



For EMI



NFC CONTROL PART



Title :	WiFi/WiMax		
Engineer:	EE		
Size	Project Name		Rev
D	GX502GX		0.0
Date: Tuesday, April 16, 2019	Sheet 53 of 105		

<Variant Name>

ASUSTeK COMPUTER

Title : USB3_*****

Engineer: Gaming RD

Size	Project Name	Rev
Custom	G711GW	1.0

Date: Tuesday, April 16, 2019 Sheet 54 of 103

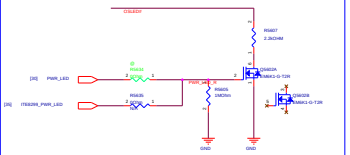
<Variant Name>

	Title :	**IO Con. to MB**
ASUSTeK COMPUTER	**Engineer:**	**Gaming RD**

Size	Project Name	Rev
Custom	**G711GW**	1.0

Date:	Tuesday, April 16, 2019	Sheet	55	of	103

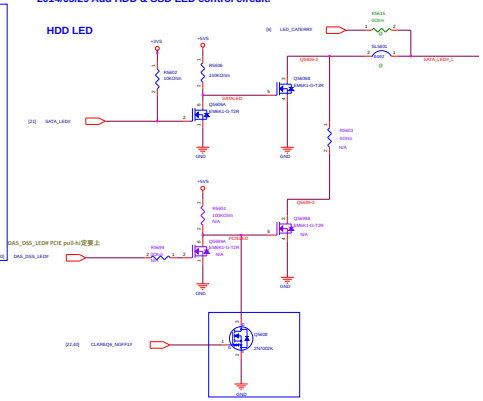
OS LED



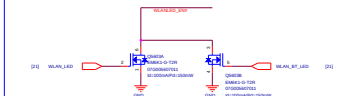
Charger LED

2014/05/29 Add HDD & SSD LED control circuit.

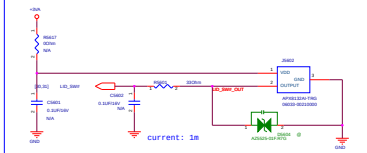
HDD LED



BT/WLAN LED

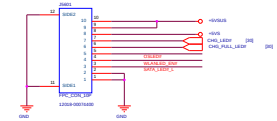


HALL SENSOR

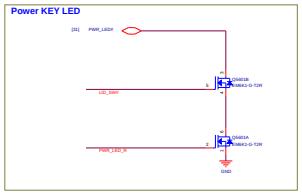


CAP LED

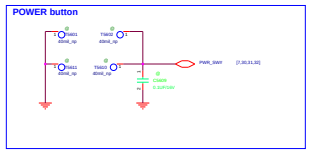
LED Board



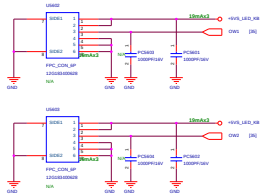
Power KEY LED



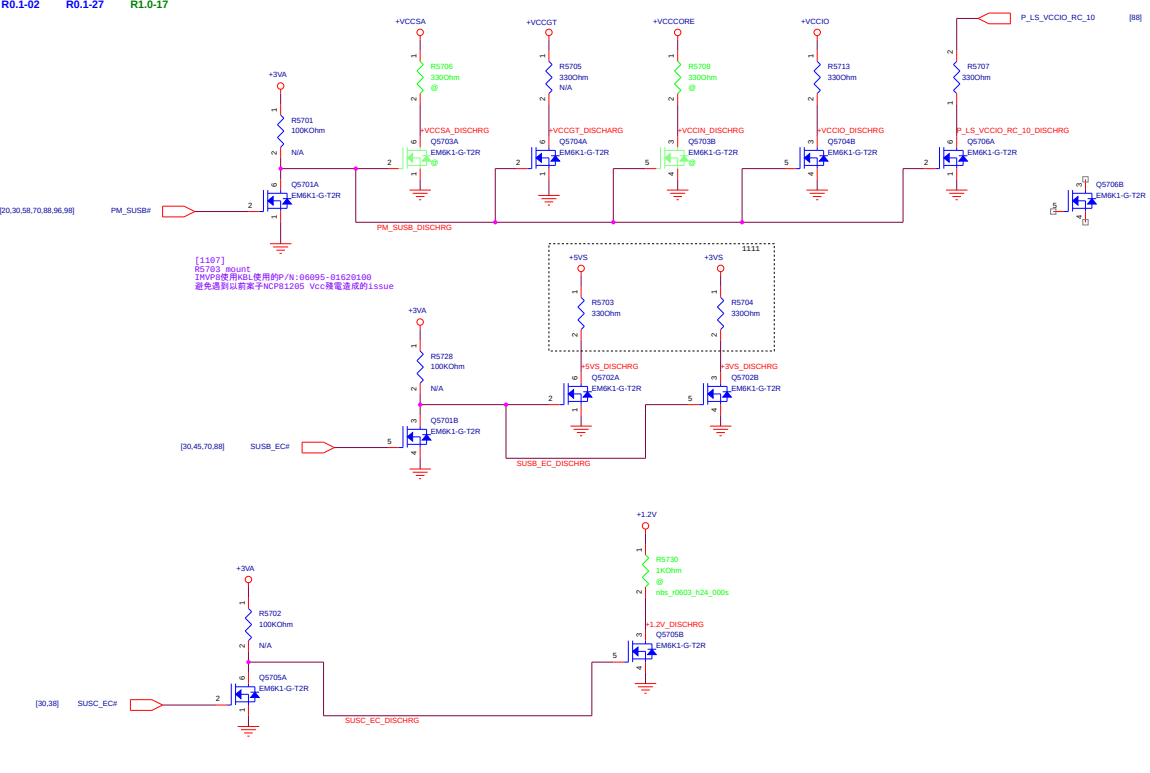
POWER button

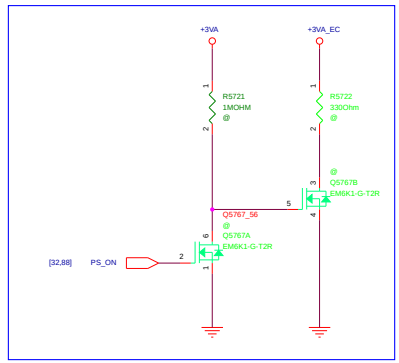


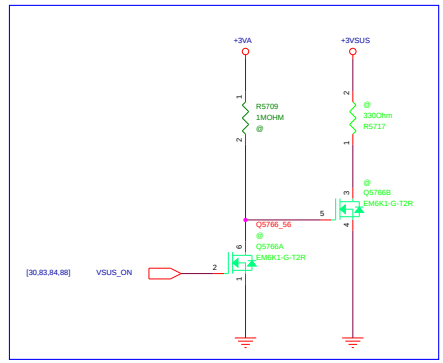
One-wire Connect to LED

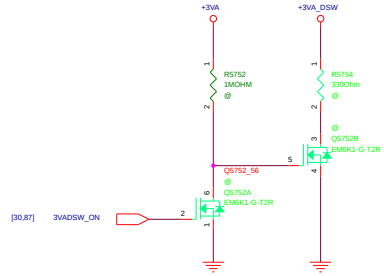


R0.1-02 R0.1-27 R1.0-17



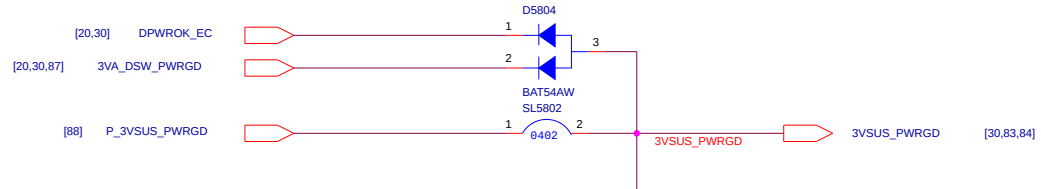


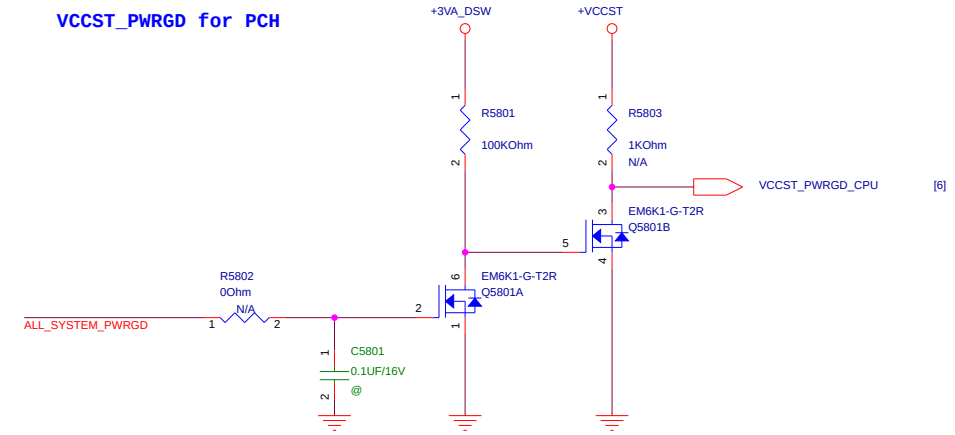


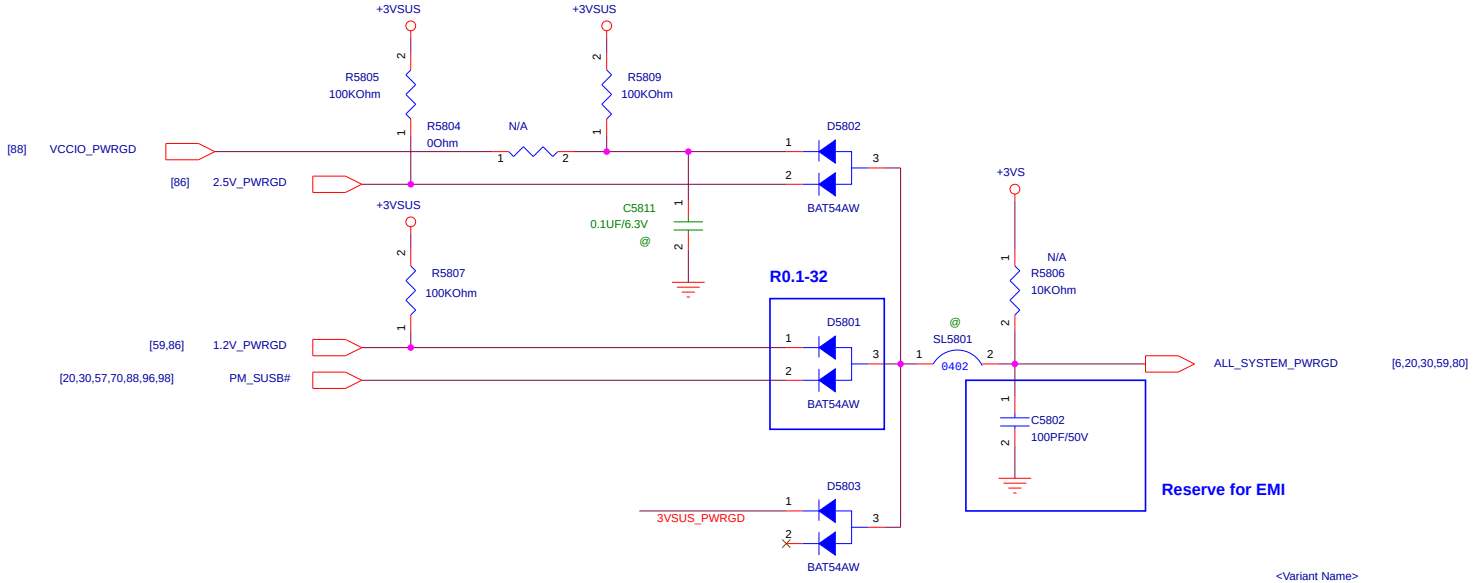


<variant_name>

ASUSTeK COMPUTER	Title : DSG_Discharge	
	Engineer: Gaming RD	
Size: C	Project Name: G711GW	Rev: 1.0
Date: Tuesday, April 16, 2019	Sheet 57 of 103	



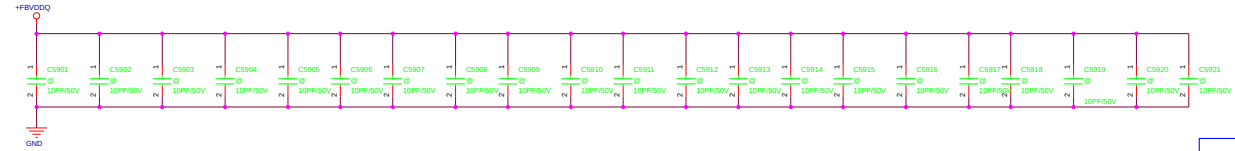


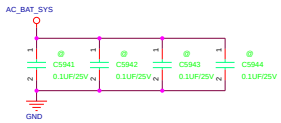


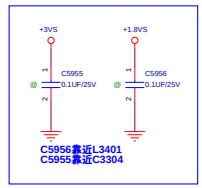
<Variant Name>

ASUSTeK COMPUTER	Title : Power Protect	
	Engineer: Gaming RD	
Size: Custom	Project Name: G711GW	Rev: 1.0
Date: Tuesday, April 16, 2019	Sheet 58 of 103	

EMI

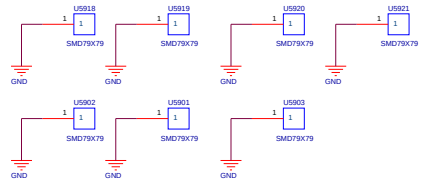






CLIP

13NB0I40T01011



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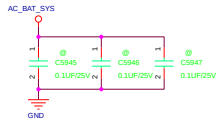

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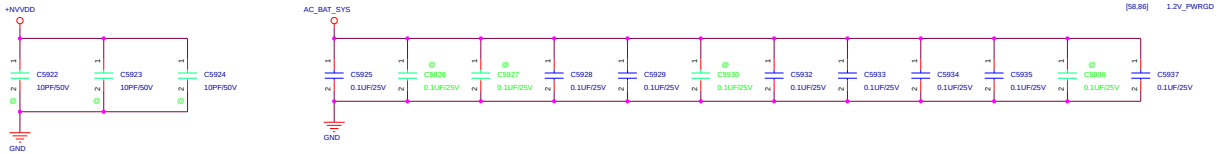
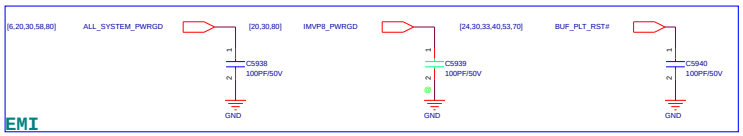
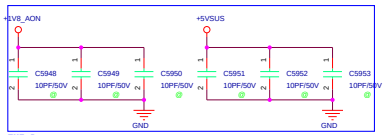
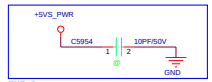








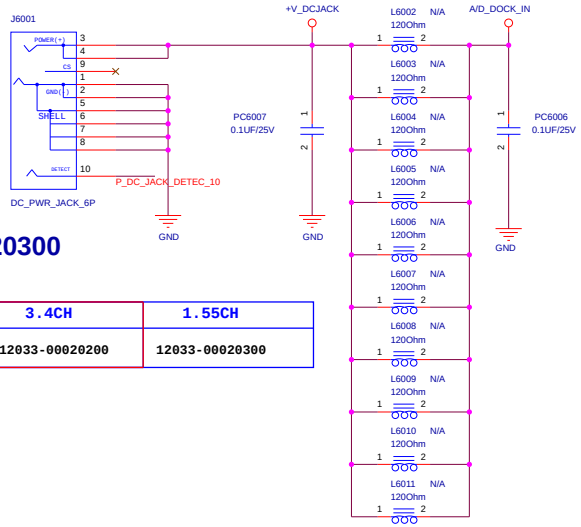
<Variant Name>

ASUSTeK COMPUTER	Title : I/O_Main board Conn.	
	Engineer: Gaming RD	
Size: C	Project Name: G711GW	Rev: 1.0
Date: Tuesday, April 16, 2019	Sheet 59 of 103	

DC-IN Connector

DC Jack使用請詢用River_Hsu

New 6 Phi 4 Pin DC_Jack

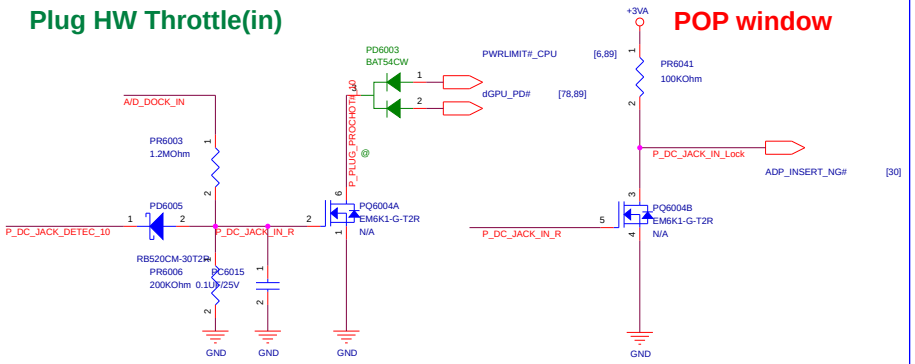


12033-00020300

J6001	3.4CH	1.55CH
	12033-00020200	12033-00020300

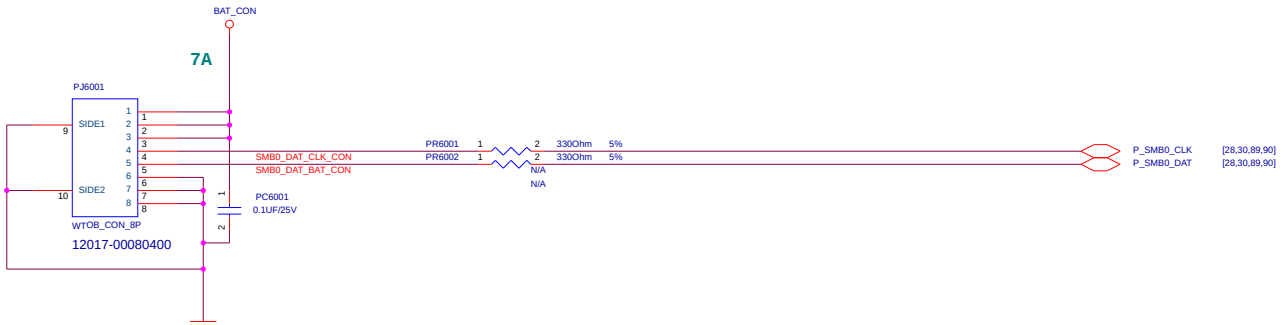
Mode	ADP_INSERT_NG#	AC_IN_OC#
AC Mode	0 (POP,throttling, stop charging)	0
	1	

Plug HW Throttle(in)



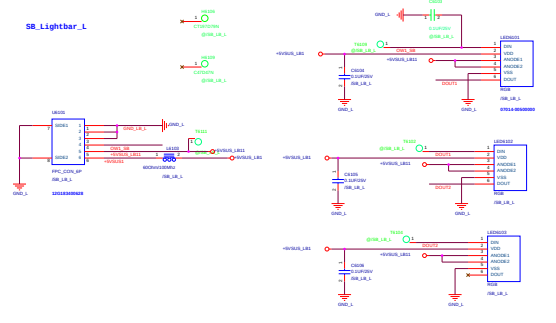
POP window

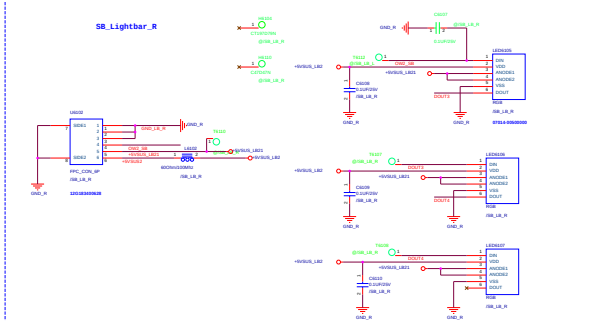
Battery Connector

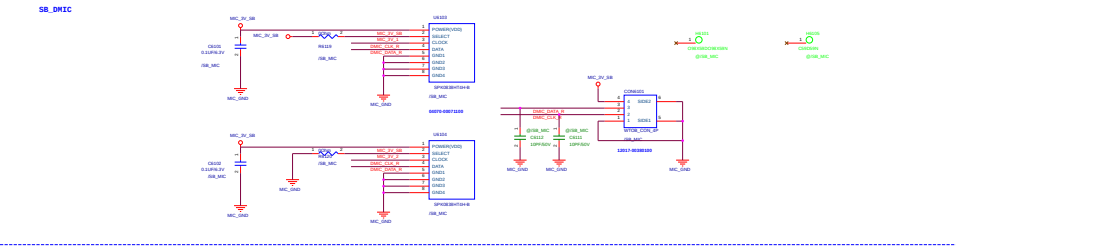


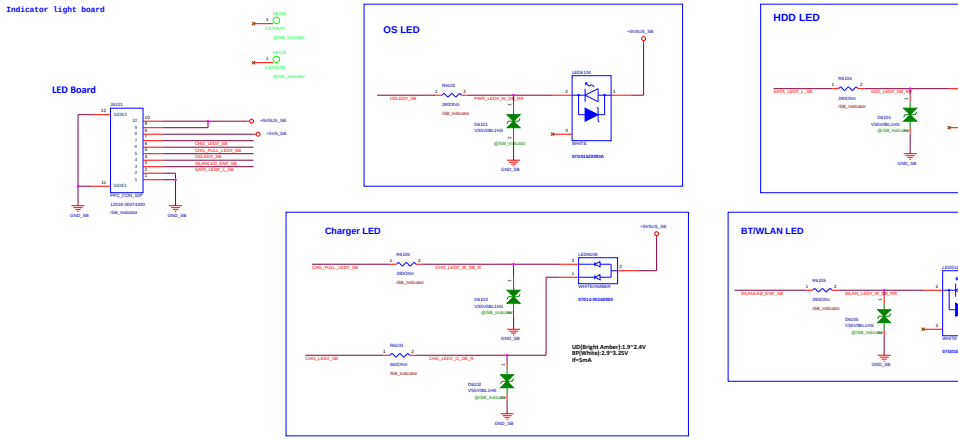
Note:Battery Connector 正確性與BAT1_IN_OC#是否預留!

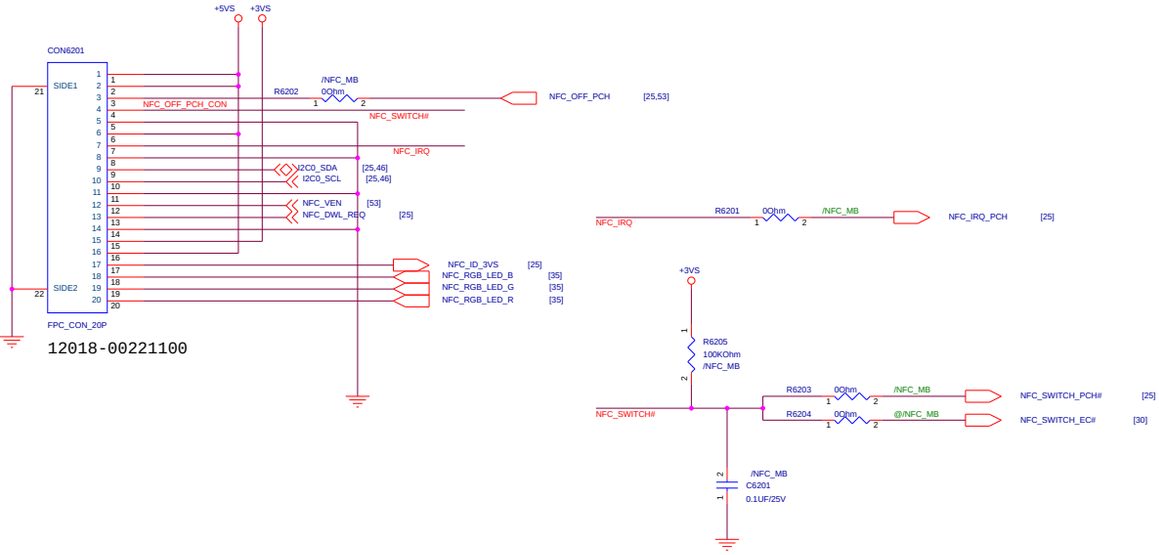
Project Name: GX700			Rev: R1.0
Title: DC & BAT IN			
Size: A3	Dept.: NB_Power team	Engineer: Benson	
Date: Tuesday, April 16, 2019	Sheet 60 of 103		


SB_Lightbar_L


SB_Lightbar_R

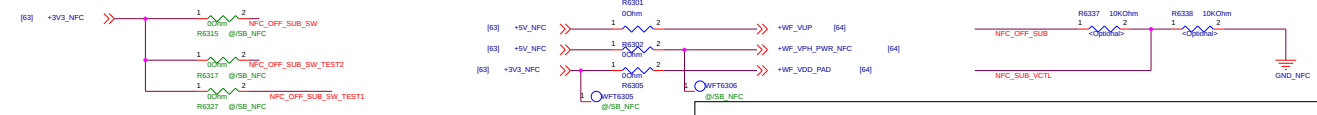

SB_DMIC

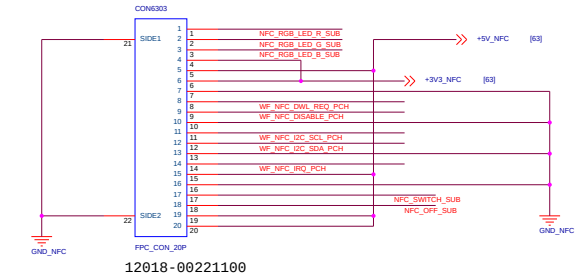

Indicator light board
LED Board
OS LED
HDD LED
Charger LED
BT/WLAN LED
UD(Bright Amber):1.0~2.4V
BY(White):2.9~3.25V
IF=5mA


+5VS
+3VS
CON6201
SIDE1
SIDE2
21
22
FPC_CON_20P
12018-00221100
/NFC_MB
R6202
0Ohm
NFC_OFF_PCH_CON
NFC_OFF_PCH [25,53]
NFC_SWITCH#
NFC_IRQ
I2C0_SDA [25,46]
I2C0_SCL [25,46]
NFC_VEN [53]
NFC_DWL_REQ [25]
NFC_ID_3VS [25]
NFC_RGB_LED_B [35]
NFC_RGB_LED_G [35]
NFC_RGB_LED_R [35]

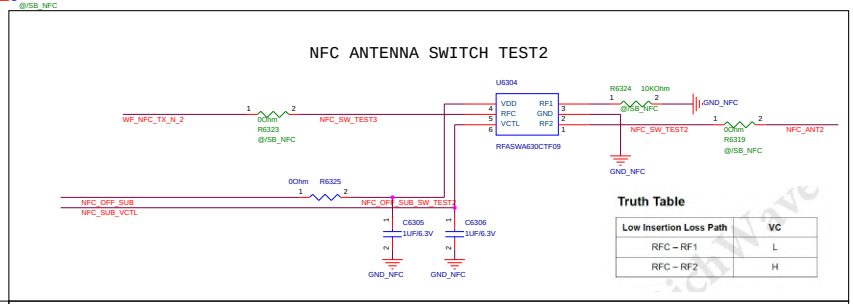
NFC_IRQ
R6201
0Ohm
/NFC_MB
NFC_IRQ_PCH [25]

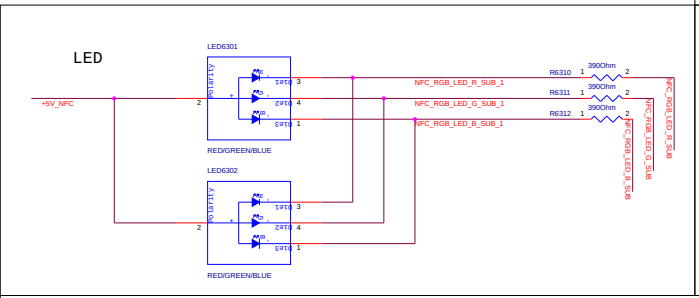
+3VS
R6205
100KOhm
/NFC_MB
NFC_SWITCH#
R6203
0Ohm
/NFC_MB
NFC_SWITCH_PCH# [25]
R6204
0Ohm
@/NFC_MB
NFC_SWITCH_EC# [30]
/NFC_MB
C6201
0.1UF/25V

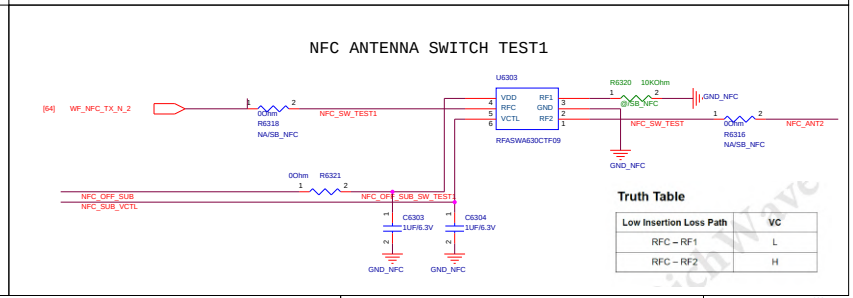


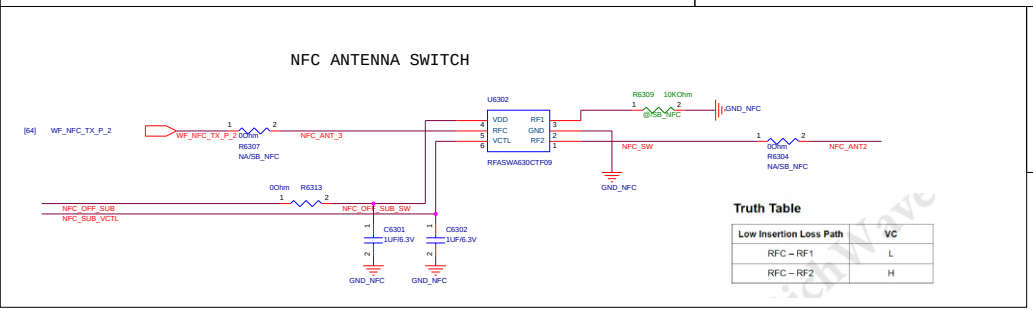


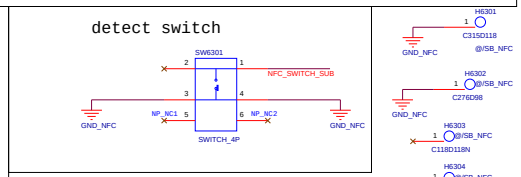
12018-00221100

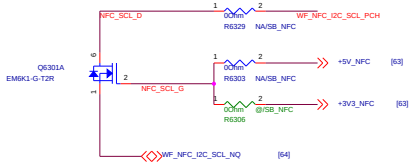


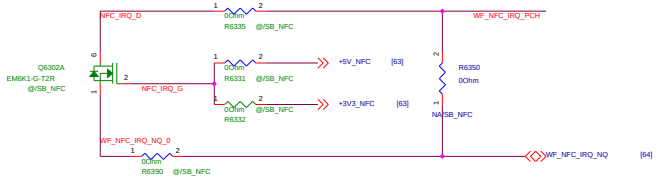


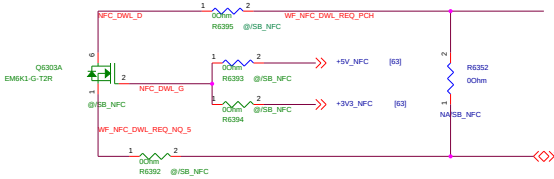


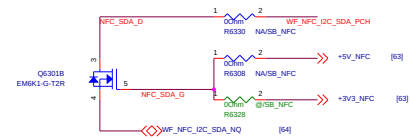


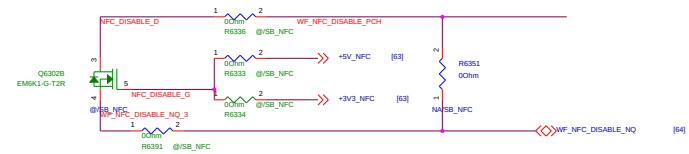


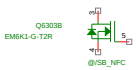


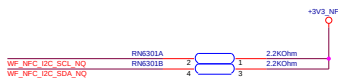












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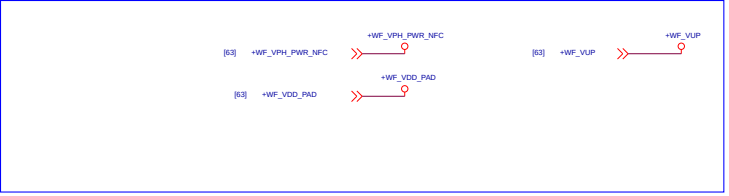
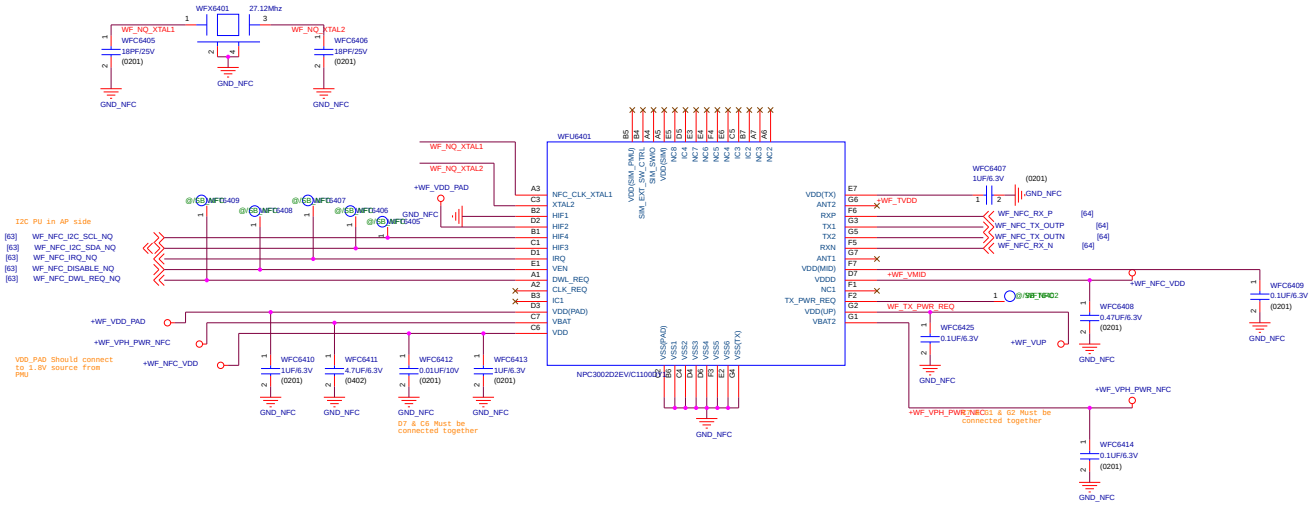
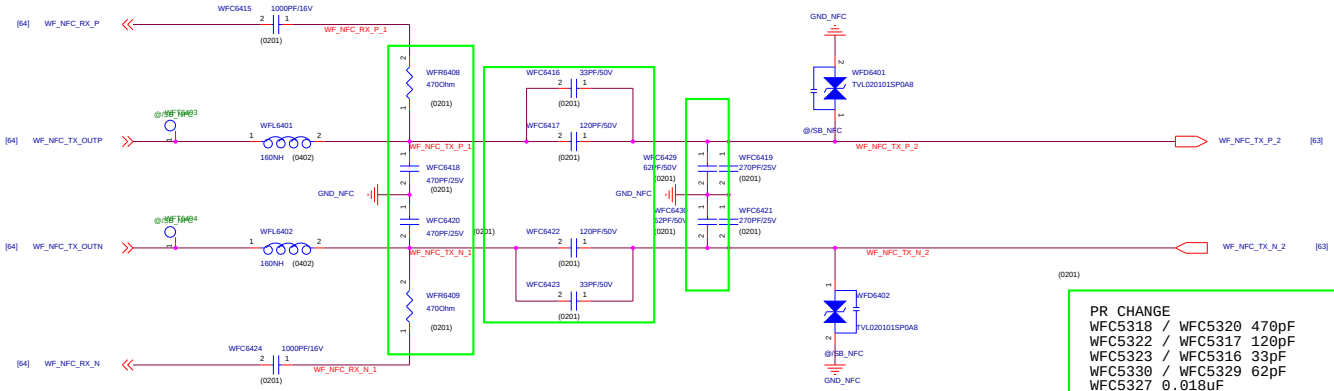
ASUSTeK COMPUTER	Title :	
	Engineer:	Gaming RD
Size: C	Project Name: G731GX	Rev: 1.0
Date: Tuesday, April 16, 2019	Sheet 63 of 103	





NFC Matching

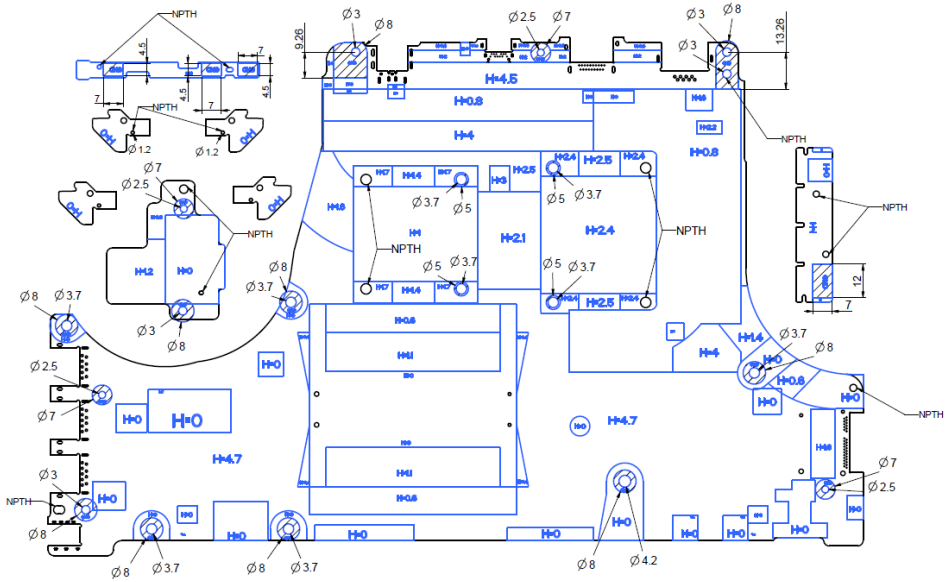


PR CHANGE
WFC5318 / WFC5320 470pF
WFC5322 / WFC5317 120pF
WFC5323 / WFC5316 33pF
WFC5330 / WFC5329 62pF
WFC5327 0.018uF
WFR5308 /WFR5309 470 Ohm

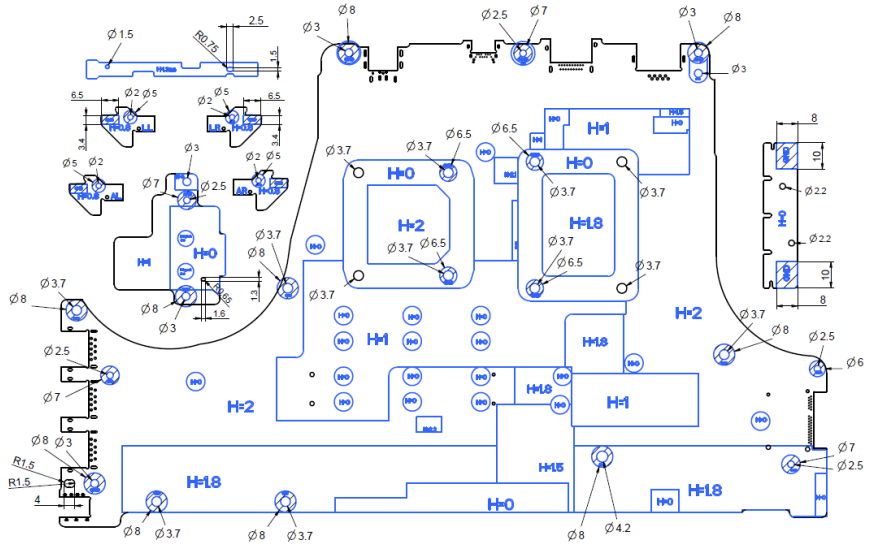
<Variant Name>

ASUSTeK COMPUTER	Title :	USB3_*****	
	Engineer:	Gaming RD	
Size: C	Project Name: G731GX		Rev: 1.0
Date: Tuesday, April 16, 2019	Sheet 64 of 103		

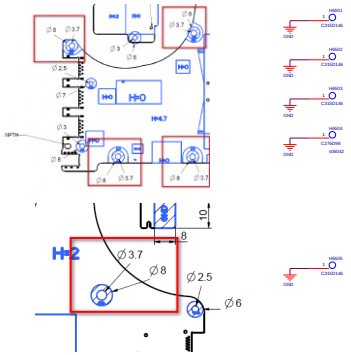
BOTTOM



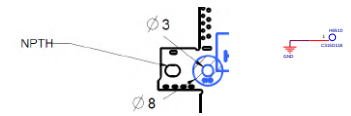
TOP



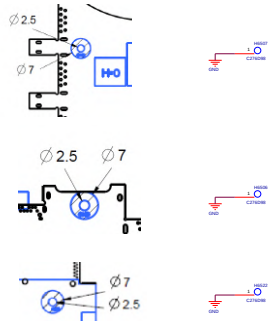
PTH 8 /3.7mm



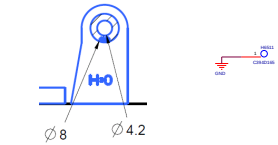
PTH 8 /3 mm



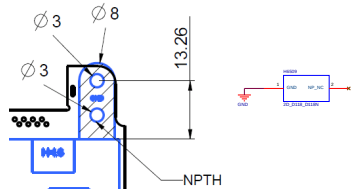
PTH 7 /2.5mm



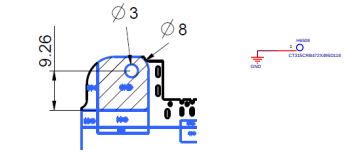
PTH 8 /4.2 mm



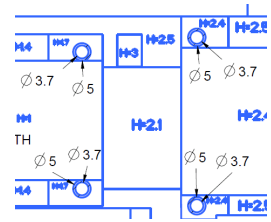
PTH 8 /3mm+ NPTH 3mm



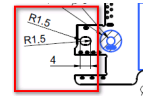
PTH 8/3mm (Ext.)



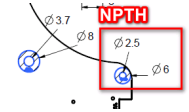
PTH 6.5 /5 /3.7 mm



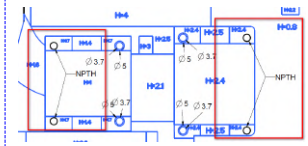
NPTH 1.5/ 4mm



NPTH 6/ 2.5 mm



NPTH 3.7 mm



Title :	ME_Screw Hole & Nut
Engineer:	Gaming RD
Project Name	G711GW

Main Board

PCIE Setting

GX501GI PCIE/SATA Function define

CNL HM370

HSIO Capabilities	Function
PCIEG (From GPU)	
PCIE#01 - USB3.1#07	
PCIE#02 - USB3.1#08	
PCIE#03 - USB3.1#09	
PCIE#04 - USB3.1#10	
PCIE#05	
PCIE#06	
PCIE#07	
PCIE#08	
PCIE#09	PCIE*4 SSD
PCIE#10	
PCIE#11- SATA-0a	
PCIE#12- SATA-1a	
PCIE#13- SATA-0b	
PCIE#14- SATA-1b	
PCIE#15 / SATA#2	
PCIE#16 / SATA#3	WLAN
PCIE#17 / SATA#4	
PCIE#18 / SATA#5	
PCIE#19 / SATA#6	
PCIE#20 / SATA#6	
PCIE#21	TBT (x4)
PCIE#22	
PCIE#23	
PCIE#24	

	Function
CLKREQ-0	GPU
CLKREQ-1	
CLKREQ-2	CR
CLKREQ-3	WLAN
CLKREQ-4	
CLKREQ-5	TBT AR
CLKREQ-6	PCIE SSD
CLKREQ-7	
CLKREQ-8	
CLKREQ-9	
CLKREQ-10~15	

USB Setting

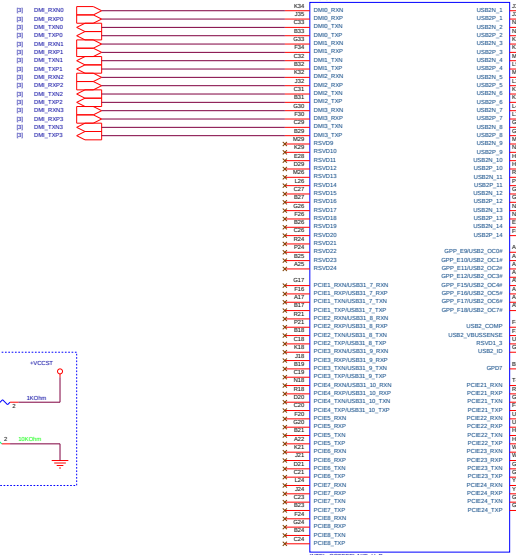
GX501GI USB Function define

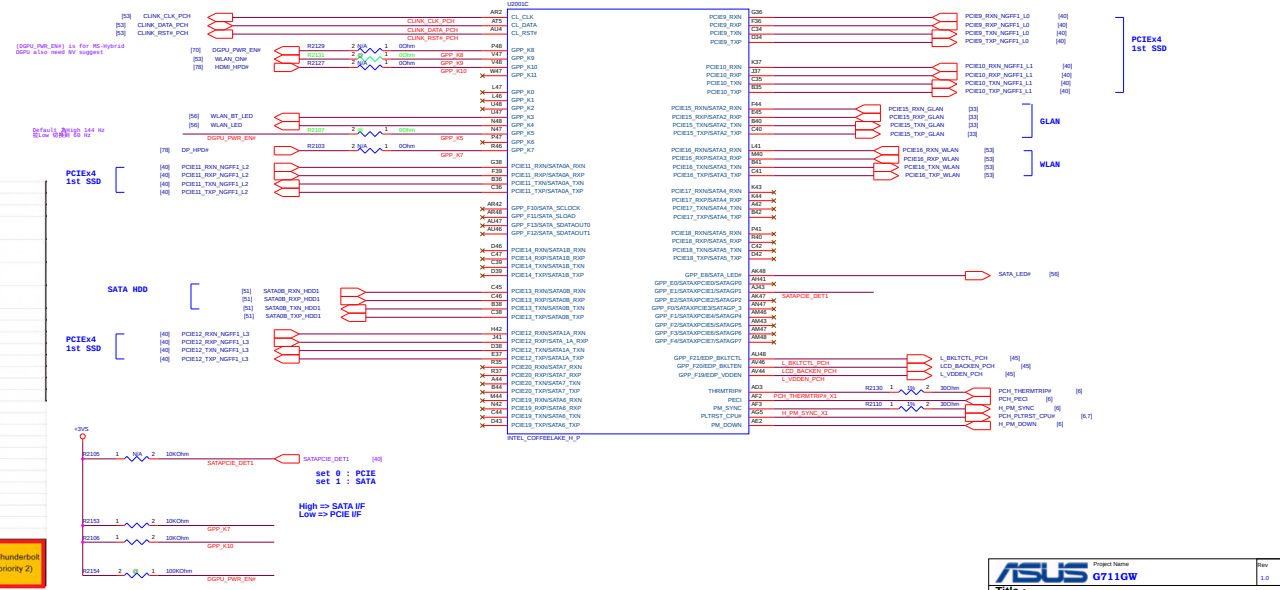
CNL HM370

USB 2.0	Function
USB2_01	USB3.0 MB Port1
USB2_02	USB3.0 MB Port2
USB2_03	USB3.0 MB Port3
USB2_04	Camera
USB2_05	USB3.0 MB Port4(Charger)
USB2_06	TBT
USB2_07	
USB2_08	N key
USB2_09	BT
USB2_10	
USB2_11	
USB2_12	

USB 3.0	Function
USB3.1#01	USB3.1MB Port1 (Support Gen2)
USB3.1#02	USB3.0 MB Port2 (Support Gen2)
USB3.1#03	USB3.0 MB Port3 (Support Gen2)
USB3.1#04	USB3.0 MB Port4 (Support Gen2)
USB3.1#05	
USB3.1#06	
USB3.1#07	
USB3.1#08	

HSIO	HM370	QM370	CM246	IRST			Devices Assign
0	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #1				(port1) USB3.1 Type C
1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #2				(port2) USB3.1 Type C
2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #3				(port1) USB3.0 Type A USB3.1 Type A
3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #4				(port2) USB3.0 Type A USB3.1 Type A
4	USB3.1 Gen1 #5	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #5				(port3) USB3.0 Type A USB3.1 Type A only for QM370 / CM246
5	USB3.1 Gen1 #6	USB3.1 Gen1/Gen2 #6	USB3.1 Gen1/Gen2 #6				(port4) USB3.0 Type A USB3.1 Type A only for QM370 / CM246
6	USB3.1 Gen1 #7	USB3.1 Gen1 #7	USB3.1 Gen1 #7	PCIE #1			CR (USB3.0 / PCIE)
7	USB3.1 Gen1 #8	USB3.1 Gen1 #8	USB3.1 Gen1 #8	PCIE #2	NO	x2	
8	NA	USB3.1 Gen1 #9	USB3.1 Gen1 #9	PCIE #3		x2	
9	NA	USB3.1 Gen1 #10	USB3.1 Gen1 #10	PCIE #4			
10	NA GbE	PCIE #5 GbE	PCIE #5 GbE	PCIE #5 GbE	NO	x4	
11	NA	PCIE #6	PCIE #6	PCIE #6		x2	Thunderbolt (priority 1)
12	NA	PCIE #7	PCIE #7	PCIE #7		x2	
13	NA	PCIE #8	PCIE #8	PCIE #8			
14	PCIE #9 GbE	PCIE #9 GbE	PCIE #9 GbE	PCIE #9 GbE	Yes	x2	1st M.2 SSD (PCIE*4 / SATA#1a) 1st M.2 SSD (PCIE*2, optane)
15	PCIE #10	PCIE #10	PCIE #10	PCIE #10		x2	(PCIE*4, optane)
16	PCIE #11 SATA #0a	PCIE #11 SATA #0a	PCIE #11 SATA #0a	PCIE #11 SATA #0a			
17	PCIE #12 SATA #1a GbE	PCIE #12 SATA #1a GbE	PCIE #12 SATA #1a GbE	PCIE #12 SATA #1a GbE			
18	PCIE #13 SATA #0b GbE	PCIE #13 SATA #0b GbE	PCIE #13 SATA #0b GbE	PCIE #13 SATA #0b GbE	NO	x4	HDD (SATA#0b)
19	PCIE #14 SATA #1b	PCIE #14 SATA #1b	PCIE #14 SATA #1b	PCIE #14 SATA #1b		x2	ODD (SATA#1b)
20	PCIE #15	PCIE #15	PCIE #15	SATA #2		x2	GLAN
21	PCIE #16	PCIE #16	PCIE #16	SATA #3			WLAN
22	PCIE #17 SATA #4	PCIE #17 SATA #4	PCIE #17	SATA #4		x2	2nd M.2 SSD (PCIE*2, optane)
23	PCIE #18 SATA #5	PCIE #18 SATA #5	PCIE #18	SATA #5	Yes	x4	2nd M.2 SSD (PCIE*4 / SATA#4)
24	PCIE #19	PCIE #19	PCIE #19	SATA #6		x2	(PCIE*4, optane)
25	PCIE #20	PCIE #20	PCIE #20	SATA #7			
26	PCIE #21	PCIE #21	PCIE #21			x2	3rd M.2 SSD (PCIE*4) 3rd M.2 SSD (PCIE*2, optane) 10G LAN (PCIE*4) optional Thunderbolt (priority 2)
27	PCIE #22	PCIE #22	PCIE #22		Yes	x4	
28	PCIE #23	PCIE #23	PCIE #23			x2	(PCIE*4, optane)
29	PCIE #24	PCIE #24	PCIE #24				





Project Name	G711GW	Rev 1.0
Title :	PCH-CPT(2)_PCIE,CLK,USB	
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD
Date: Tuesday, April 16, 2019	Sheet 21 of 103	

<Variant Name>

Title :

ASUSTeK COMPUTER

Engineer: Gaming RD

Size	Project Name	Rev
D	**G711GW**	1.0

Date:	Tuesday, April 16, 2019	Sheet	66	of	103

<Variant Name>

	Title :	I/O board FUNC key
ASUSTeK COMPUTER	**Engineer:**	Gaming RD

Size	Project Name	Rev
E	**G711GW**	1.0

Date:	Tuesday, April 16, 2019	Sheet	67	of	103

<Variant Name>

	Project Name G711GW	Rev R1.0

Title : Thunderbolt

Size		
Custom	**Dept.:** ASUSTeK COMPUTER	**Engineer:** Gaming RD

Date: Tuesday, April 16, 2019	Sheet 68	of	103

<Variant Name>

Title : OTH_EMI

ASUSTeK COMPUTER

Engineer: Gaming RD

Size	Project Name	Rev
C	**G711GW**	1.0

Date:	Tuesday, April 16, 2019	Sheet	69	of	103

Main Board

GPU POWER GOOD Signal

PCH_GPIO17

NVVDD POWER GOOD LOOPBACK

remove NVVDD Loop back circuit
Nvidia FAE Suggestion, add loopback circuit for protect NVVDD/NVDDS

GPU POWER SEQUENCE CONTROL

PCH_GPPK8

inverter inside

Page 98 need up high

20180719 follow NC CRB schematic Logic add

Optimus

DGPU_PWR_EN#	FUNCTION
H	GC OFF
L	GC ON

iGPU_dGPU_switch	FUNCTION
H	dGPU Mode
L	iGPU Mode

PCI EXPRESS_Graphics

REVERSED Type PCIE X16

Reverse PCIE6 x 8

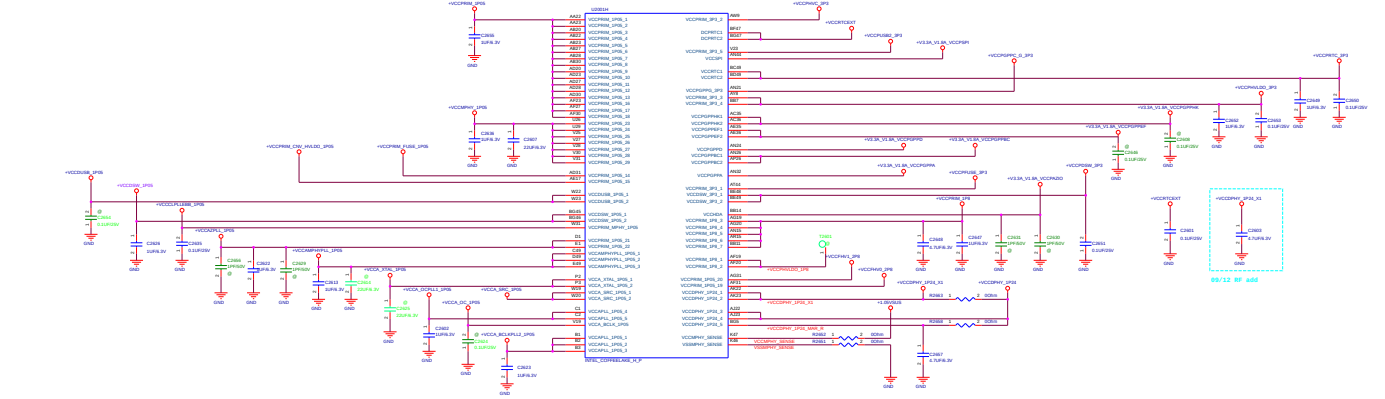
For EMI

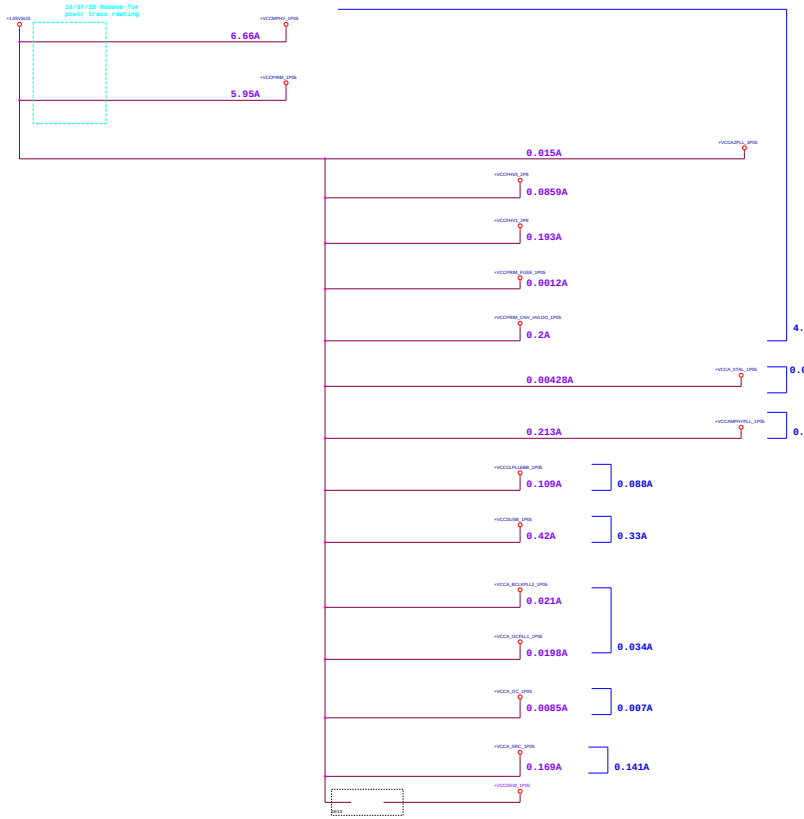
GL504GW	GS31GW(ORI)	GS31GW(NEW)
+PEX_VDD	+PEX_VDD	+PEX_VDD
22uF x2	22uF x2	22uF x2
10uF x3	10uF x3	10uF x3
4.7uF x3	4.7uF x3	4.7uF x3
0.47uF x16	0.47uF x14	0.47uF x16
+3VS_MAIN	1uF x1	1uF x1
22uF x2	+1VB_MAIN	+1VB_MAIN
10uF x4	22uF x2	22uF x2
4.7uF x4	10uF x4	10uF x4
0.47uF x13	4.7uF x1	4.7uF x5
	0.47uF x7	0.47uF x13
	1uF x2	1uF x2

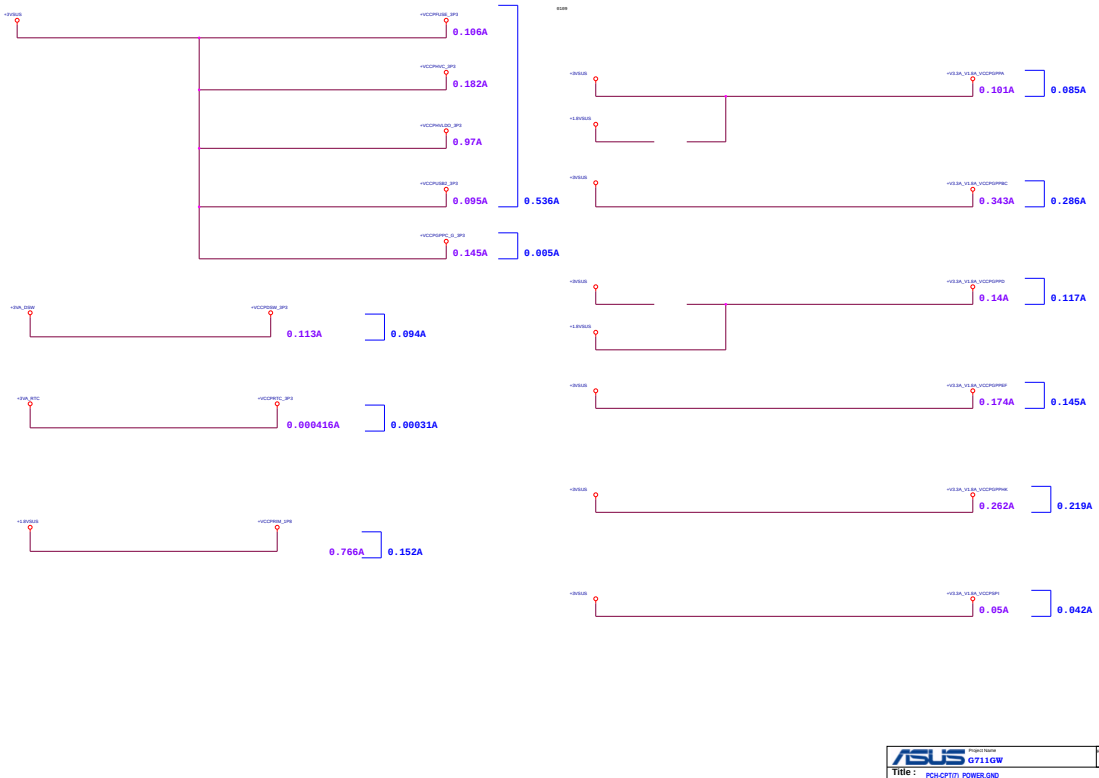
Project Name	G711GW
Title :	GPU_PCIE I/F
Size	D
Dept. :	ASUSTeK COMPUTER
Engineer:	Gaming RD
Date:	Tuesday, April 24, 2018
Sheet	70 of 103

Table 8-1. Power Descriptions for PCH in CNL-H

Name	Description
VCCPHVLDO_1P8	**1.8V Primary Well.** On the motherboard, this power pin must be connected to VCCPRIM_1P8 rail in Internal 1.8 V VRM Mode and left as no-connect in External 1.8V VRM Mode.
VCCPGPPA	1.8V or 3.3V for GPP_A group.
VCCPGPPBC	1.8V or 3.3V for GPP_B and GPP_C groups.
VCCPGPPD	1.8V or 3.3V for GPP_D group.
VCCPGPPEF	1.8V or 3.3V for GPP_E and GPP_F groups.
VCCPGPPG_3P3	3.3V for GPP_G group.
VCCPGPPHK	1.8V or 3.3V for GPP_H and GPP_K groups.
VCCMPHY_SENSE	1.05V Sense Line.
VSSMPHY_SENSE	0V (Ground) Sense Line.
VSS	Ground.

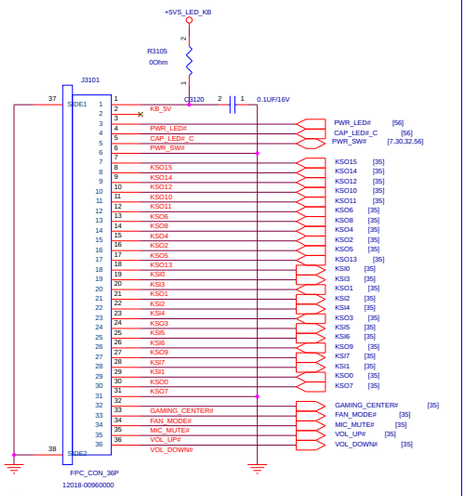




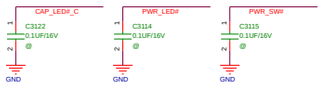


ASUS	Project Name: G711GW		Rev: 1.0
Title : PCH-CPT(7)_POWER,GND			
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Tuesday, April 28, 2020	Sheet 26 of 103		

Keyboard Connector

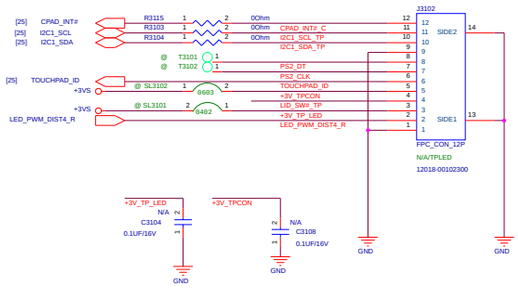


Reserved for EMI

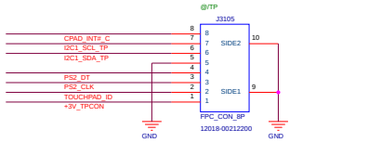


Touch Pad Connector

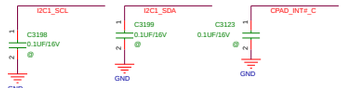
2019 RGB Logo 12PIN

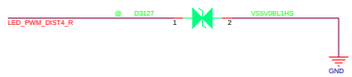


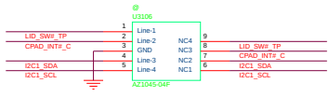
SA555D-2400 8PIN

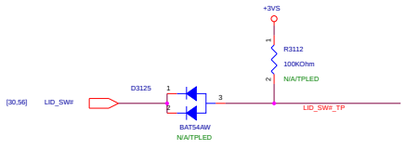


Reserved for EMI

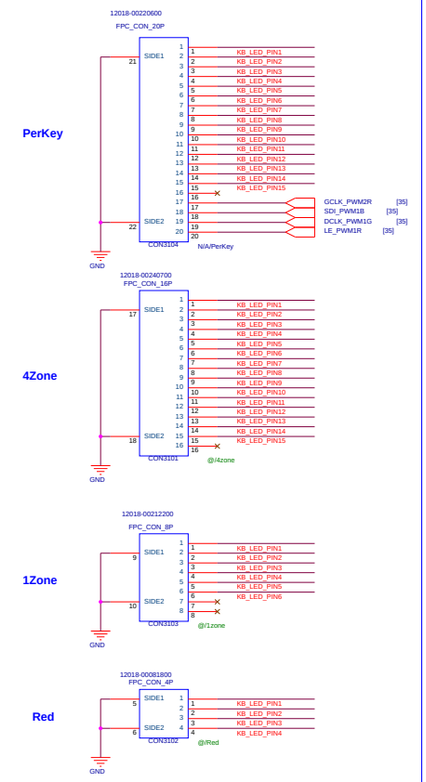




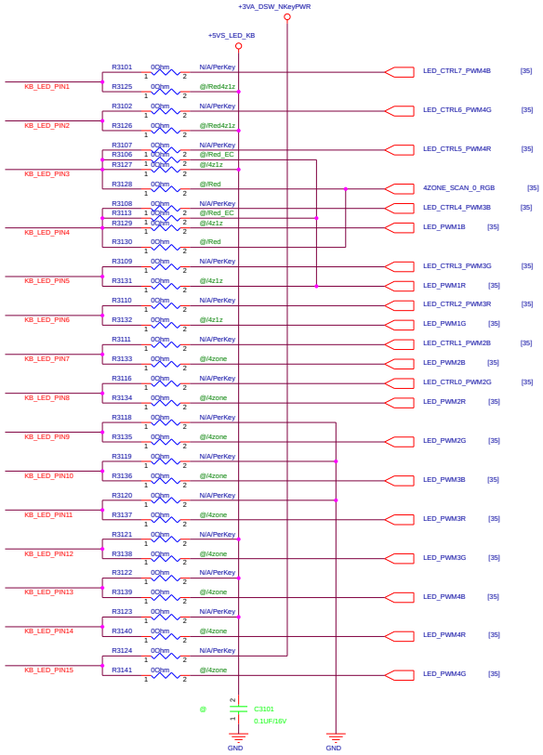




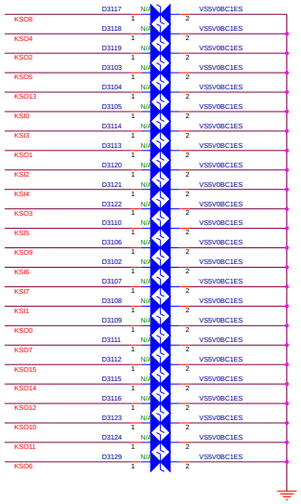
Keyboard Backlight

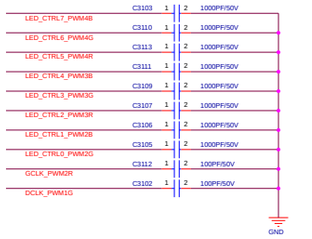


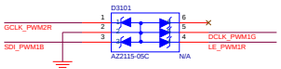
RED, 4zone,1zone, PerKey Co-layout



For EMI

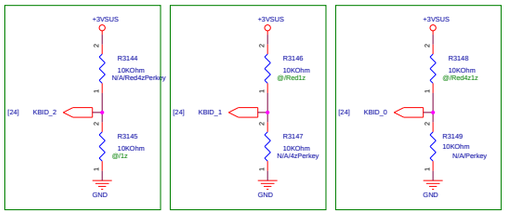






	RED-4pin	1zone RGB_8pin	4zone-16pin	per key-20pin
pin1	VCC	VCC green	VCC green	COM7
pin2	VCC	VCC red	VCC red	COM6
pin3	GND	VCC blue	VCC blue	COM5
pin4	GND	LED1 blue	LED1 blue	COM4
pin5		LED1 red	LED1 red	COM3
pin6		LED1 green	LED1 green	COM2
pin7		NC	LED2 blue	COM1
pin8		NC	LED2 red	COM0
pin9			LED2 green	GND
pin10			LED3 blue	GND
pin11			LED3 red	GND
pin12			LED3 green	VCC
pin13			LED4 blue	VCC
pin14			LED4 red	VCC
pin15			LED4 green	VDD-33
pin16			NC	NC
pin17				GCLK
pin18				SDI
pin19				DCLK
pin20				LE

Keyboard ID



KB ID PCH Side(HW請依照此表格做設計判斷) *BIOS會再反向				
Code	ROG RGB KB Type	KBID 2 (GPP_H18)	KBID 1 (GPP_H17)	KBID 0 (GPP_H16)
0x00	Normal Keyboard	H	H	H
0x01	QWERASD Partition Keyboard	H	H	L
0x02	4 Zone RGB Keyboard	H	L	H
0x03	Per Key RGB Keyboard	H	L	L
0x04	1 Zone RGB Keyboard	L	H	H

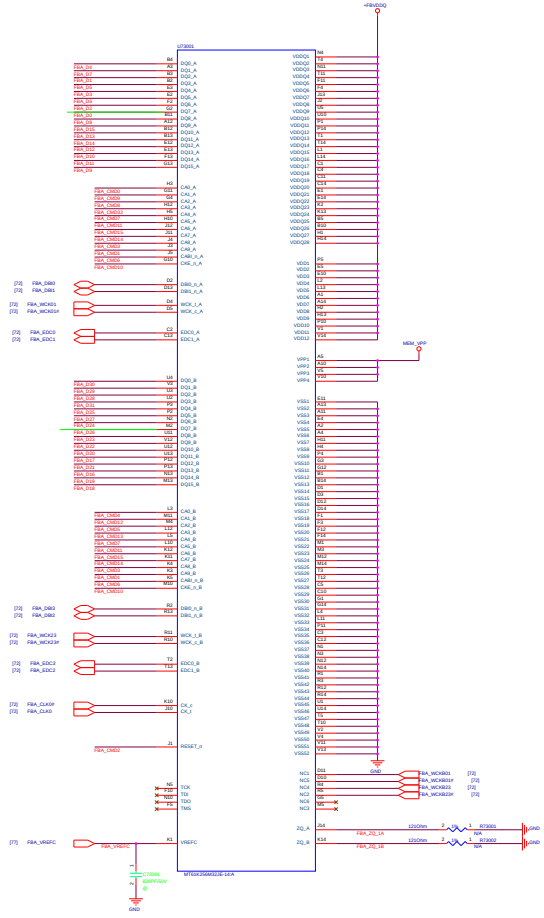
[72] FBA_D[63..32]

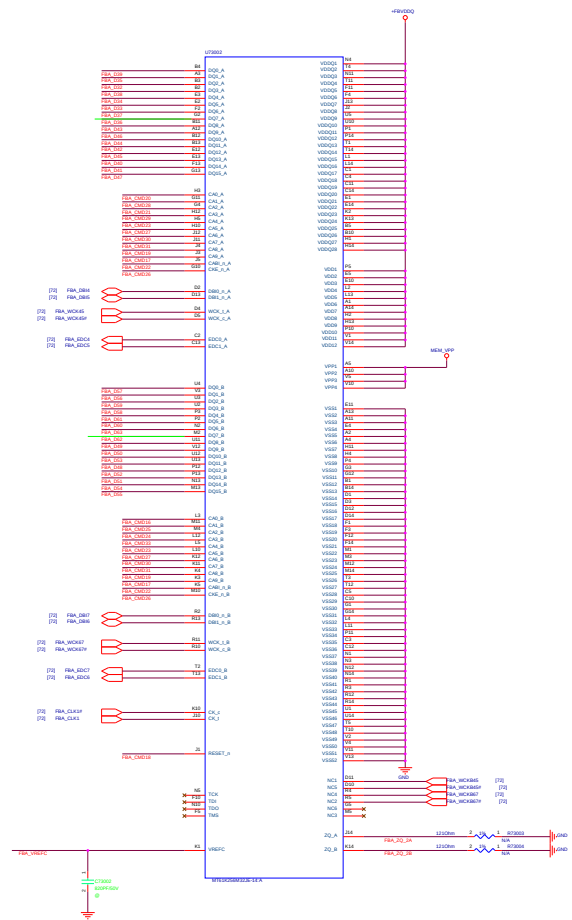
40 OHm_NET
FBA Partition 64..32
MF=0 Normal

[72] FBA_D[31..0]

[73] FBA_CMD[33..0]

40 OHm_NET
FBA Partition 31..0
MF=1 Mirror





<variant_name>

Title	<Title>		
Size: A3	Document Number: G710GW		Rev: R1.0
Date: Tuesday, April 16, 2019	Sheet: 73	of: 100	

G731GX SKU Table

			CPU	Power	DIMM	VRAM			
Option	PCB	SKU							
60NB0H10-MB1030	R2.0	GX501VSK SKU1	/I7-7700HQ	/230W	8G_Hynix	V8G_Samsung			
60NB0H10-MB2000	R2.0	GX501VSK SKU2	/I5-7300HQ	/230W	8G_Hynix	V8G_Samsung			

1. CPU: INT I7-7700HQ 2.8G/6M SR32Q BGA 01001-01380600
CPU: INT I5-7300HQ 2.5G/6M SR32S BGA 01001-01380500

2. dGPU: nVidia N17E-G2-A1 FCBGA2152 02004-00480500

4. EC: ITE IT8995VG-128/DX --06037-00050800

5.onboard menory
8G_ Hynix 03012-00030400

9. Card Reader: AU6435--02G630002400 (Page42)

10. USB Charger IC: (Page52) Silego SLG55584AVTR -- 06016-00040000
MAXIM MAX14566AEETA+ -- 06G016196011

11. USB3.0 Repeater IC:(Page67)
Parade : PS8710B -- 06053-00200000
Maxim : MAX14972CTG+ -- 06053-00030000

13. Audio Codec : 02043-00130000 (663-VA4)

Title : UX362_SKU Table_R1.0
Engineer: Gaming RD
Size: C
Project Name: G711GW
Rev: R1.0
Date: Tuesday, March 28, 2017
Sheet of

Rev	Date	Description
1.0	2017.03.03 P21	Remove CR
	2017.03.04 Q5602, Q5601 change for DXF Limitation	
	2017.03.10 +1V8_MAIN, +3VS_NV Follow G753 Power sequence setting	
	2017.03.11 R7821 Follow GL702 GPU Power seq	
	2017.03.11 +PEX_VDD GPU Sequence update	
	2017.03.14 PCE8104, PCE8107, PCE8106 update Cap for DXF Limit	
	2017.03.14 GX501VIK Remove useless nut in P67	
	2017.03.15 J5301 Connector list update	
	2017.03.15 H6716, H6706, H6724, H6723 Screw Hole update	
	2017.03.16 J5602 change LID SW for Angle Simulation	
	2017.03.17 EMI Reserve C5606, C5607 Cap	
	2017.03.17 RN3002, L4512, L4513, L4504, L4515, L4505 SWAP for Layout	
1.1	2017.03.21 P30、P37, P39 AMP Change SNL04M25555	
	2017.03.21 EMI Reserve P30 C77360 Cap and P69 Caps and Spring	
	2017.03.23 AMP Change Remove P37 MUTE CONTROL schematic	
	2017.03.23 AMP Change Reserve Q3701	
	2017.03.27 P71 +FBVDDQ Discharge setting Follow G753 Power sequence setting	
	2017.03.29 P12 Remove TBT Power Low Switch for Layout	
1.2	2017.03.30 Change Cap C7105, C7101 for thermal request	
	2017.03.30 Thermal Request for H6728	
	2017.04.05 EMI Reserve Cap and Spring in P69	
	2017.04.06 Reserve C2601 for +VCCPGPP_EF Ripple	
	2017.04.07 25.00MHZ Cap C1126, C1124 change for Vendor Suggest	
	2017.04.07 27MHz Cap C7811, C7801 change for Vendor Suggest	
2.0	2017.04.11 P48 Reserve 0 ohm for SDA and SCL	
	2017.04.17 P71 Add Caps for NVVDD Ripple	
	2017.04.18 Q5704 Chnage MOS for DXF Limitation	
	2017.04.20 P71 Add Caps for NVVDD Ripple	
	2017.04.21 P67 Screw Hole H6705 update	
	2017.04.21 P71 Add Caps for NVVDD Ripple C71119~C71122	
	2017.04.25 P71 C7122, C7123, C7127, C7135, C7143, C7144, C7156, C7164, C7166,, C7186, C7187 change to 10UF	
	2017.04.25 P70 C7007, C7002 change to 4.7UF	
	2017.04.25 P70 C7020, C7024 change to 22UF	
	2017.05.02 EMI Reserve C6948, C6949, C6950, C6951, C6952, C6953, C6954 and remove U6913	
	2017.05.02 H6711, H6712 change screw hole type fot EMI Solution	
	2017.05.03 Remove J4502 Pin 36 GND fot Factory Issue	
	2017.05.05 P88、P58 Remove VCCST_PWRGD signal	
	2017.05.05 P79、P45 Remove eDP Lan2 and Lan3 Signal	
	2017.08.10 P31 R3121,R3122 change to unmount	

Rev	Date	Description

Rev	Date	Description

Rev	Date	Description

ASUSTeK COMPUTER INC.

Title : Revision History

Engineer: Gaming RD

Size: D | Project Name: G711GW | Rev: 1.0

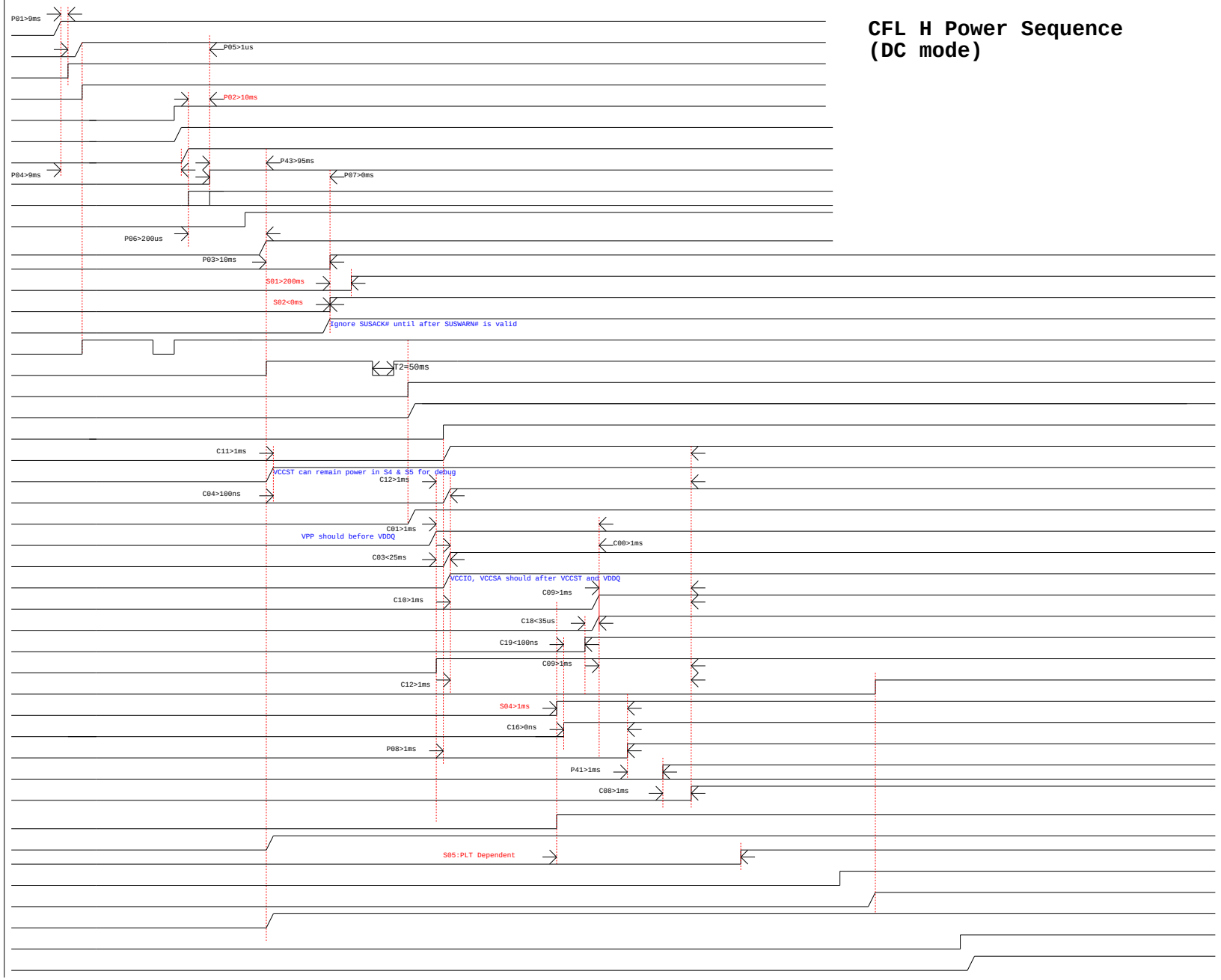
Date: Tuesday, April 04, 2017 | Sheet 102 of 103

CFL H Power Sequence (DC mode)

DC-IN Mode

C:CPU
P:PCH
S:PLT
Power
Signal

(+RTCBAT)+3VA_RTC
(AC_BAT_SYS)+3VA/+5VA
(+3VA_RTC)RTCRST#(PCH)
(Power)AC_IN_OC#(EC)
(EC)PS_ON(+3VA_EC)
(PS_ON)+3VA_EC(EC)
(3VADSW_ON)+3VA_DSW(3VA_DSW_PWRGD)
(EC)DPWROK_EC(PCH)
(+3VA_DSW)PM_BATLOW#(PCH)
(PCH)PM_SLP_SUS#(EC)
(VSUS_ON)+1.0VSUS_VCCPRIM(1.0VSUS_PWRGD)
(EC)PM_RSMRST#_PCH(PCH)
(PCH)SUSWARN#(EC)
(EC)ME_AC_PRESENT_PCH(PCH)
(EC)PCH_SUSACK#(PCH)
(PWR Switch)PWR_SW#(EC)
(EC)PM_PWRBTN#(PCH)
(EC)SUSC_EC#(Power)
(SUSC_EC#)+12V/+5V/+3V
(EC)SUSB_EC#(Power)
(SUSB_EC#)+12VS/+5VS/+3VS
(VSUS_ON)+1.0V_VCCST,VCCPLL(VCCST_PWRGD)
(+VCCIO)+VCCSTG
(1.2V_ON)+2.5V(2.5V_PWRGD)
(1.2V_ON)+VDDQ_CPU(1.2V_PWRGD)
(+12VS)+VCCPLL_OC
(SUSB_EC#)+VCCIO(VCCIO_PWRGD)
(ALL_SYSTEM_PWRGD)+VCCSA(IMVP8_PWRGD)
(DDR_VTT_CTRL)+0.6V
(CPU)DDR_VTT_CTRL(Power)
(Power)1.2V_PWRGD(AND)
(Power)IMVP8_PWRGD
(AND)ALL_SYSTEM_PWRGD(CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD)VCCST_PWRGD_CPU(CPU)
(EC)PM_PWROK_PCH(PCH)
(PCH)CLK_PCH_BCLK(CPU)
(PCH)H_CPUPWRGD(CPU)
(ALL_SYSTEM_PWRGD)P_IMVP8_EN_10(Power)
(CPU)P_SVID_DATA_X2(Power)
(EC)PM_SYSPWROK_PCH(PCH)
(PCH)PLT_RST#(CPU/EC/Device)
(P_IMVP8_DRVON)+VCCCORE(IMVP8_PWRGD)
(CPU)H_THERMTRIP#(PCH)
(PCH)DDR4_DRAMRST#(Memory)
+VCCGT

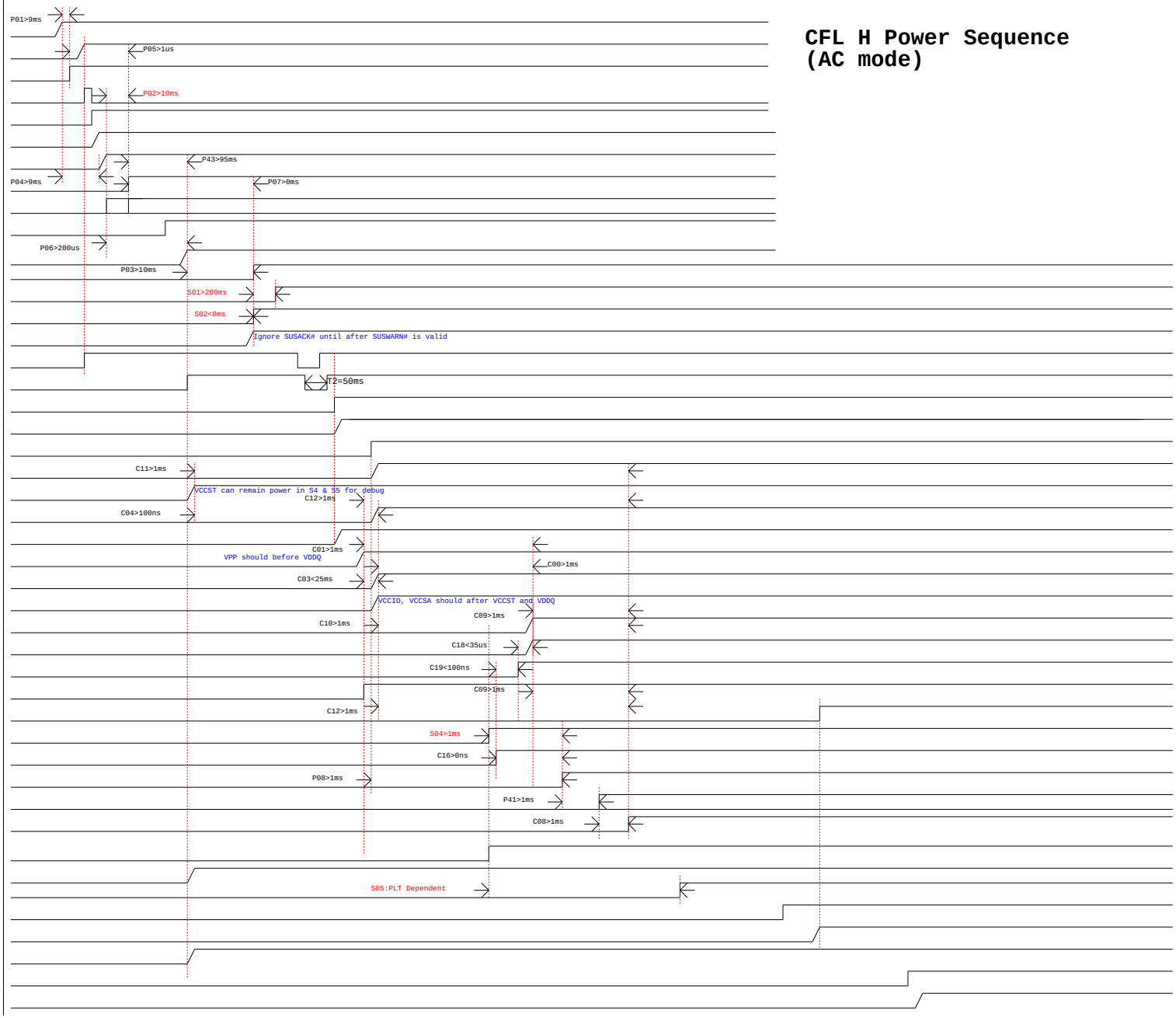


ASUS	Project Name: G711GW		Rev: R1.0
Title : Power On Timing--DC mode			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Tuesday, April 16, 2019	Sheet 101 of 103		

AC-IN Mode

C:CPU
P:PCH
S:PLT
Power
Signal

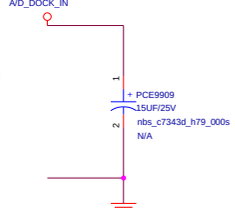
(+RTCBAT)+3VA_RTC
(AC_BAT_SYS)+3VA/+5VA
(+3VA_RTC)RTCRST#(PCH)
(Power)AC_IN_OC#(EC)
(EC)PS_ON(+3VA_EC)
(PS_ON)+3VA_EC(EC)
(3VADSW_ON)+3VA_DSW(3VA_DSW_PWRGD)
(EC)DPWROK_EC(PCH)
(+3VA_DSW)PM_BATLOW#(PCH)
(PCH)PM_SLP_SUS#(EC)
(VSUS_ON)+1.0VSUS_VCCPRIM(1.0VSUS_PWRGD)
(EC)PM_RSMRST#_PCH(PCH)
(PCH)SUSWARN#(EC)
(EC)ME_AC_PRESENT_PCH(PCH)
(EC)PCH_SUSACK#(PCH)
(PWR Switch)PWR_SW#(EC)
(EC)PM_PWRBTN#(PCH)
(EC)SUSC_EC#(Power)
(SUSC_EC#)+12V/+5V/+3V
(EC)SUSB_EC#(Power)
(SUSB_EC#)+12VS/+5VS/+3VS
(SUSB_EC#)+1.0V_VCCST,VCCPLL
(SUSB_EC#)+VCCIO,(+12VS)+VCCSTG
(1.2V_ON)+2.5V(2.5V_PWRGD)
(1.2V_ON)+VDDQ_CPU(1.2V_PWRGD)
(+12VS)+VCCPLL_OC
(SUSB_EC#)+VCCIO(VCCIO_PWRGD)
(ALL_SYSTEM_PWRGD)+VCCSA(IMVP8_PWRGD)
(DDR_VTT_CTRL)+0.6V
(CPU)DDR_VTT_CTRL(Power)
(Power)1.2V_PWRGD(AND)
(Power)IMVP8_PWRGD
(AND)ALL_SYSTEM_PWRGD(CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD)VCCST_PWRGD_CPU(CPU)
(EC)PM_PWROK_PCH(PCH)
(PCH)CLK_PCH_BCLK(CPU)
(PCH)H_CPUPWRGD(CPU)
(CPU)P_SVID_DATA_X2(Power)
(EC)PM_SYSPWROK_PCH(PCH)
(PCH)PLT_RST#(CPU/EC/Device)
(P_IMVP8_DRVON)+VCCCORE(IMVP8_PWRGD)
(CPU)H_THERMTRIP#(PCH)
(PCH)DDR4_DRAMRST#(Memory)
+VCCGT



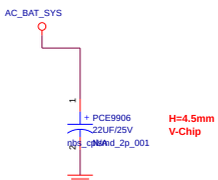
CFL H Power Sequence (AC mode)

ASUS	Project Name: G711GW	Rev: R1.0
Title : Power On Timing–AC mode		
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD
Date: Tuesday, April 16, 2019	Sheet 100 of 103	

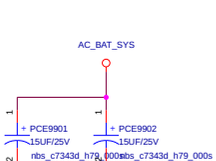
A/D_DOCK_IN



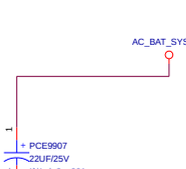
5VSUS



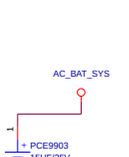
VCORE



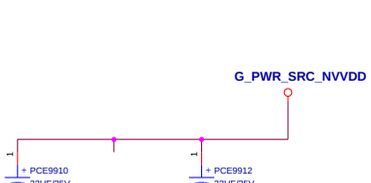
Charger



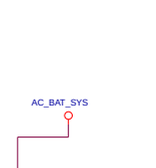
GT



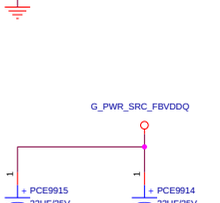
NVVDD(X70)



1.05



FBVDDQ



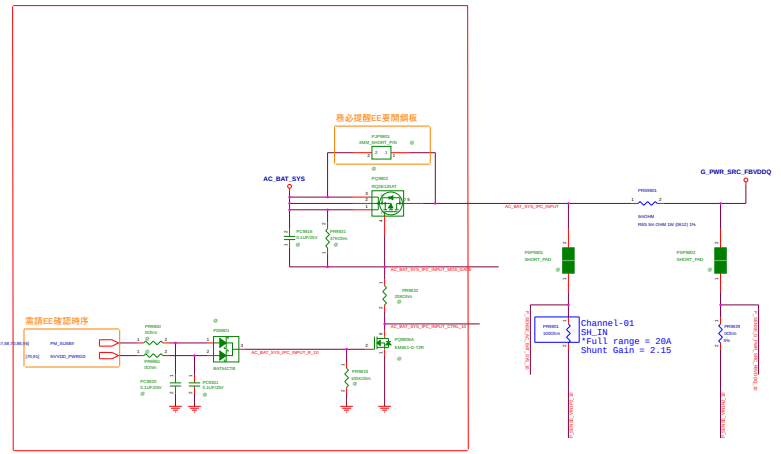
1.2

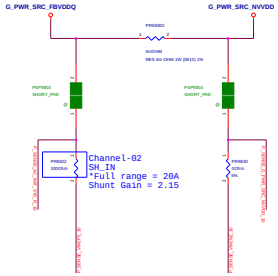
*共12顆
*請將對應電容放置對應PWR VRM輸入端

<Variant Name>

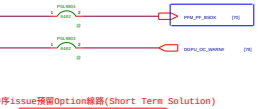
ASUS	Project Name: GM531GX	Rev: R1.0
Title : PW_Input CAP		
Size: Custom	Dept.: Power Team	Engineer: Joe
Date: Tuesday, April 16, 2019	Sheet 99 of 102	

UPI / ON 時序issue預留Option線路(Short Term Solution)
SS : 103us ~ 275us
OFF : 8.1ms ~ 12.4ms



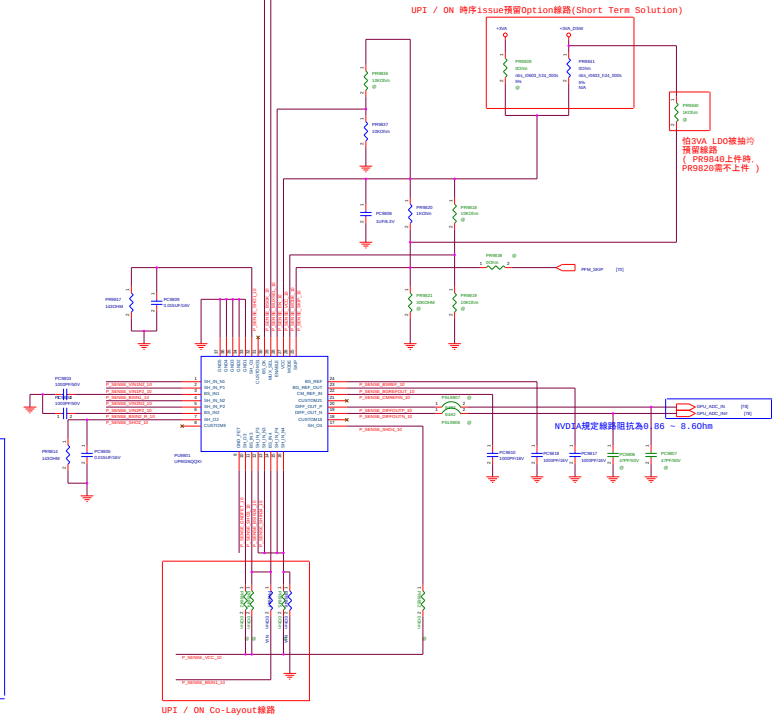


請和EE確認EE端是否有畫對應線路、pull high



UPI / ON 時序issue預留Option線路(Short Term Solution)

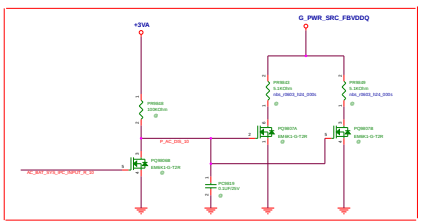
怕3VA LDO被抽均
預留線路
(PR9840上件時,
PR9820需不上件)



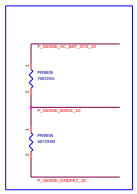
NVDIA規定線路阻抗為0.86 ~ 8.60hm

UPI / ON Co-Layout線路

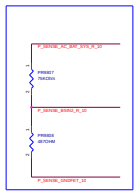
AC_BAT_SYS Discharge線路
T-Discharge : 0.626s(Worst case 10 Phase)



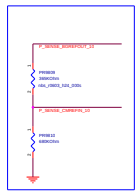
Channel-01
BS_IN
*Full range = 19V
Bus Gain = 6.4514m



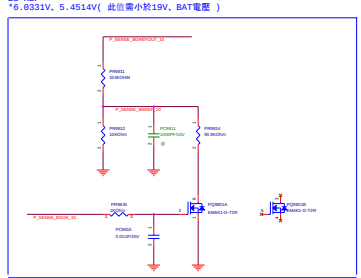
Channel-02
BS_IN
*Full range = 19V
Bus Gain = 6.4514m



CM REF IN
*0.85V(實際0.8459V)



BS REF
*6.0331V、5.4514V(此值需小於19V、BAT電壓)



N18E

150W+

	UP9026PQKI(UPI)	NCP45491(ON)
PR9801	100□(10G212100014010)	
PR9817	127□(10G212127014010)	169□(10G212169014010)
PR9822	100□(10G212100014010)	
PR9814	127□(10G212127014010)	169□(10G212169014010)
PR9805	75k□(10G212750214010)	
PR9806	487□(10G212487014010)	649□(10G212649014010)
PR9807	75k□(10G212750214010)	
PR9808	487□(10G212487014010)	649□(10G212649014010)
PR9811	324k□(10G212324314010)	243k□(10G212243314010)
PR9812	10k□(10G212100214010)	
PR9834	90.9k□(10G212909214010)	

115W ~ 130W

	UP9026PQKI(UPI)	NCP45491(ON)
PR9817	143□(10G212143014010)	191□(10G212191014010)
PR9814	143□(10G212143014010)	191□(10G212191014010)

100W ~ 110W

	UP9026PQKI(UPI)	NCP45491(ON)
PR9817	165□(10G212165014010)	221□(10G212221014010)
PR9822		
PR9814	165□(10G212165014010)	221□(10G212221014010)

75W ~ 90W

	UP9026PQKI(UPI)	NCP45491(ON)
PR9817	215□(10102-00571000)	287□(10G212287014010)
PR9822		
PR9814	215□(10102-00571000)	287□(10G212287014010)

75W-

	UP9026PQKI(UPI)	NCP45491(ON)
PR9817	357□(10G212357014010)	475□(10G212475014010)
PR9822		
PR9814	357□(10G212357014010)	475□(10G212475014010)

N18P

75W-

	UP9026PQKI(UPI)	NCP45491(ON)
PR9801	100□(10G212100014010)	
PR9817	357□(10G212357014010)	475□(10G212475014010)
PR9822	100□(10G212100014010)	
PR9814	357□(10G212357014010)	475□(10G212475014010)
PR9805	75k□(10G212750214010)	
PR9806	487□(10G212487014010)	649□(10G212649014010)
PR9807	75k□(10G212750214010)	
PR9808	487□(10G212487014010)	649□(10G212649014010)
PR9811	324k□(10G212324314010)	243k□(10G212243314010)
PR9812	10k□(10G212100214010)	
PR9834	90.9k□(10G212909214010)	

150w+

	UP9026PQKI(UPI)	NCP45491(ON)
PR9801	200□(10G212200014010)	
PR9817	127□(10G212127014010)	
PR9822	200□(10G212200014010)	
PR9814	127□(10G212127014010)	
PR9805	33k□(10G212330214010)	
PR9806	431□(10102-00581000)	
PR9807	33k□(10G212330214010)	
PR9808	431□(10102-00581000)	
PR9811	324k□(10G212324314010)	
PR9812	10k□(10G212100214010)	
PR9834	90.9k□(10G212909214010)	

115W ~ 130W

	UP9026PQKI(UPI)	NCP45491(ON)
PR9801	200□(10G212200014010)	
PR9817	143□(10G212143014010)	
PR9822	200□(10G212200014010)	
PR9814	143□(10G212143014010)	
PR9805	33k□(10G212330214010)	
PR9806	431□(10102-00581000)	
PR9807	33k□(10G212330214010)	
PR9808	431□(10102-00581000)	
PR9811	324k□(10G212324314010)	
PR9812	10k□(10G212100214010)	
PR9834	90.9k□(10G212909214010)	

75W ~ 90W

	UP9026PQKI(UPI)	NCP45491(ON)
PR9801	200□(10G212200014010)	
PR9817	215□(10102-00571000)	
PR9822	200□(10G212200014010)	
PR9814	215□(10102-00571000)	
PR9805	33k□(10G212330214010)	
PR9806	431□(10102-00581000)	
PR9807	33k□(10G212330214010)	
PR9808	431□(10102-00581000)	
PR9811	324k□(10G212324314010)	
PR9812	10k□(10G212100214010)	
PR9834	90.9k□(10G212909214010)	

Project Name

GX531GM

Rev

R1.0

Title : Type C LDO 3V3

Size	Dept.:	Engineer:
Custom	ASUSTeK COMPUTER INC.	Joe

Date:	Sheet		
Tuesday, April 16, 2019	97	of	103

<Variant Name>

	Project Name **GX531GM**	Rev R1.0

Title : PW_PEX_VDD/+1.8V_GPU

Size			
Custom	**Dept.:** NB Power Team	**Engineer:** Joe	
Date: Tuesday, April 16, 2019	Sheet 95	of 117	

+FBVDDQ [For VRAM]

DVS Setting		
REM_VDD_CTL	H	L
Voltage	1.35V	1.25V
PR9404	10KOhm	
PR9409	21.5KOhm	
PR9423	75KOhm	

Imax= 63A
OCP= 100A

PT940* 請放置 PU9401旁;並請放置Trace 上!

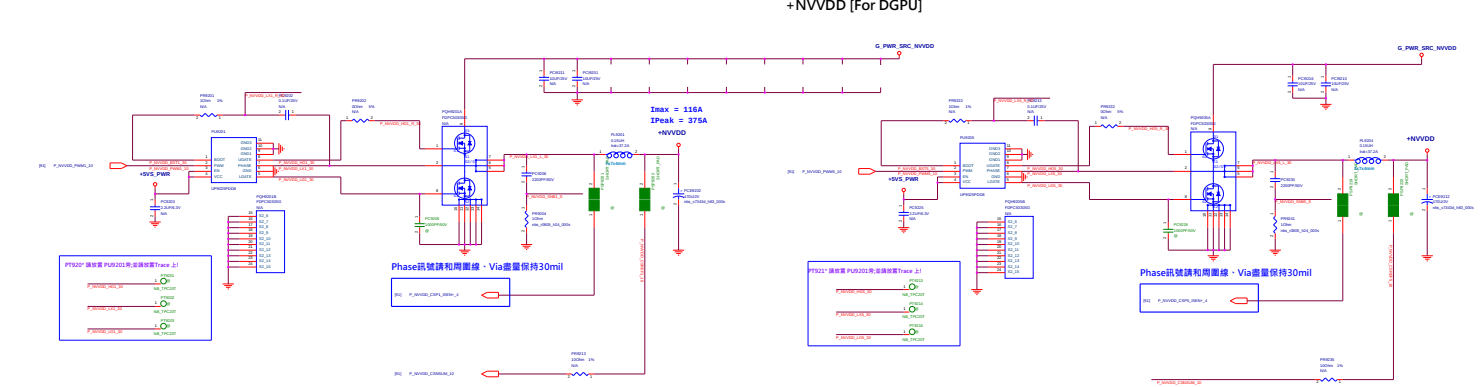
Project Name	GM531GX	Rev
Title :	PW_+FBVDDQ	R1.0
Size: Custom	Dept.: NB Power Team	Engineer: Joe
Date: Tuesday, April 16, 2019	Sheet 94 of 103	

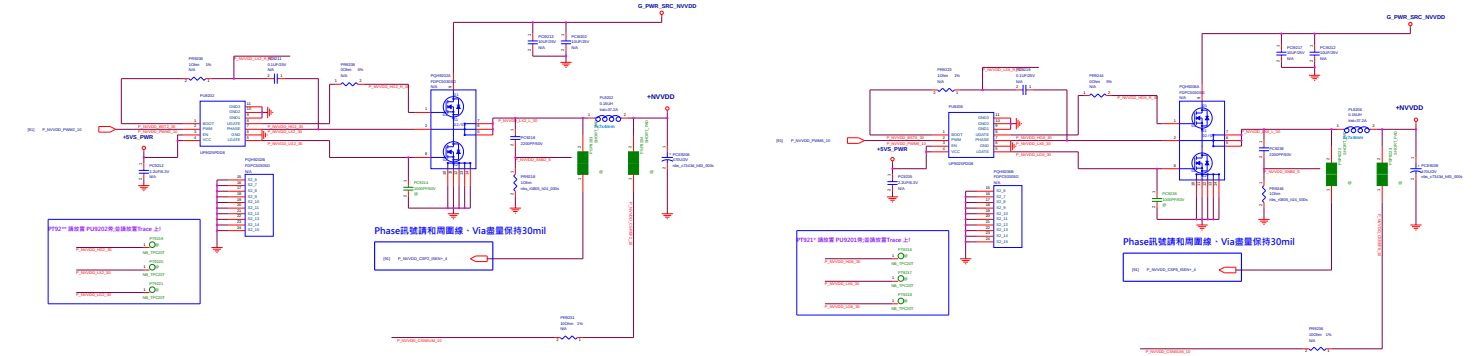
<Variant Name>

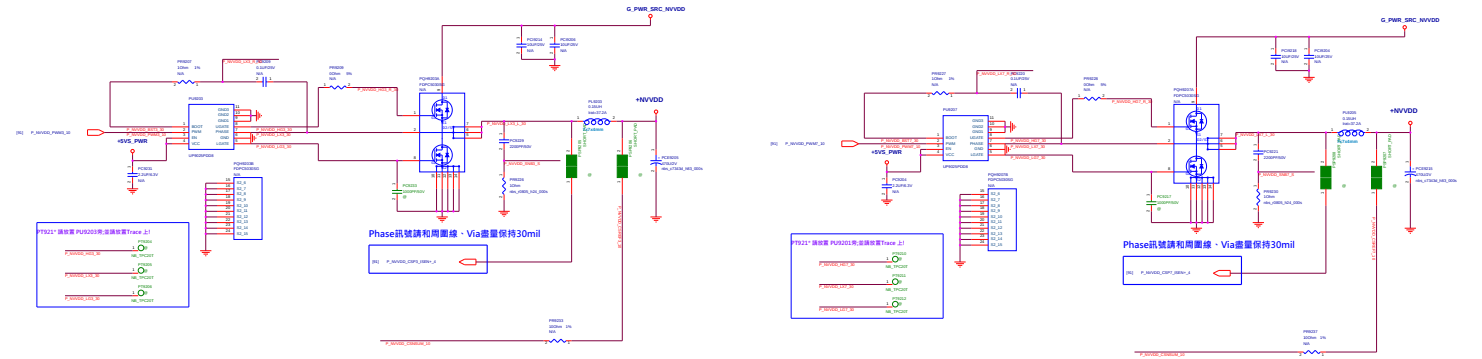
	Project Name **GX531GM**	Rev R1.0

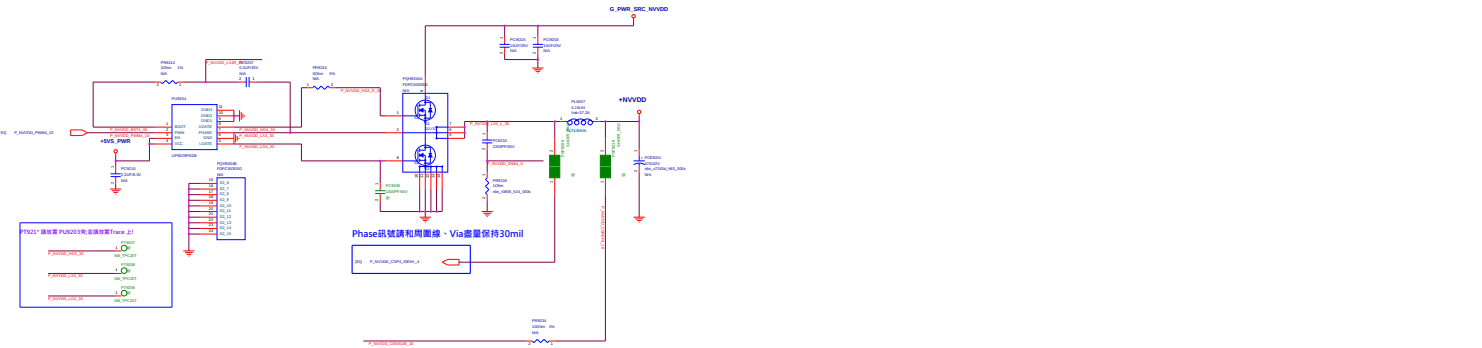
Title : PW_PEX_VDD/+1.8V_GPU

Size			
Custom	**Dept.:** NB Power Team	**Engineer:** Joe	
Date: Tuesday, April 16, 2019	Sheet 93	of 117	









+NVVDD [For DGPU]

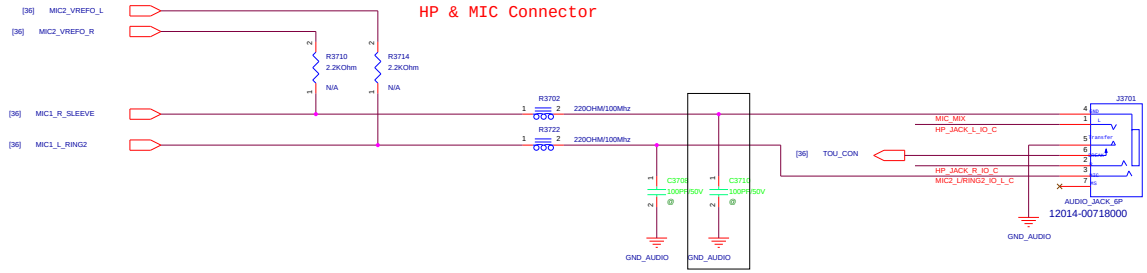
<Core Design>

Project Name	G711GW	Rev R1.0
Title :	PW_+NVVDD (2)	
Size A0	Dept.: NB Power team	Engineer: Neil
Date: Tuesday, April 16, 2019	Sheet 92	of 103

Headphone&MIC

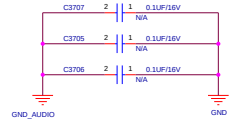
Main Board

HP & MIC Connector

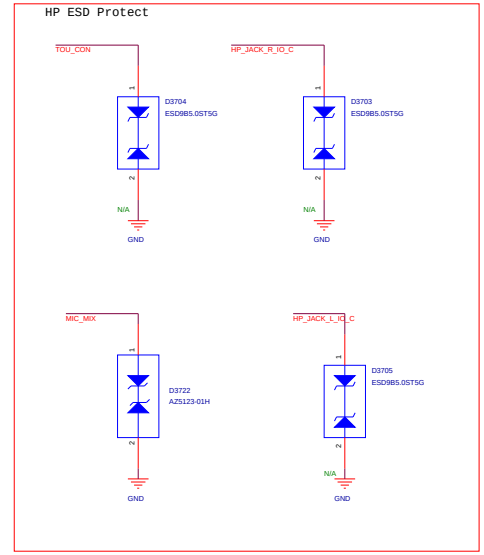


A_GND / GND

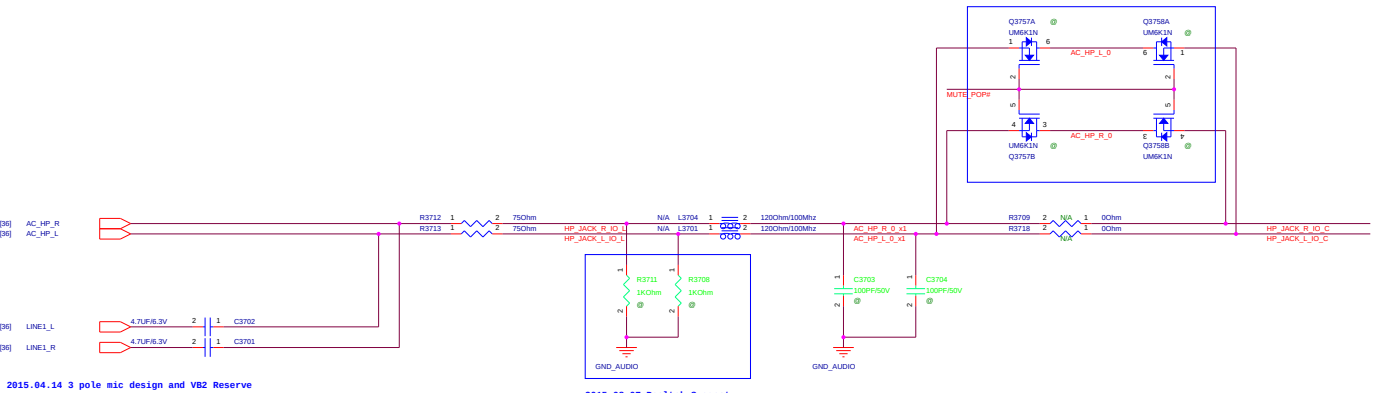
FOR EMI



HP ESD Protect

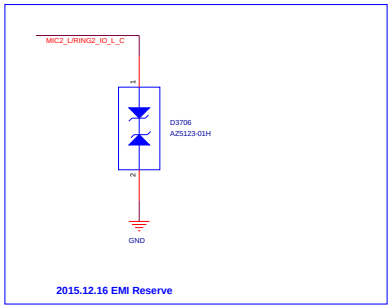


2016.09.06 Add DEPOP solution



2015.04.14 3 pole mic design and VB2 Reserve

2015.08.07 Realtek Suggest



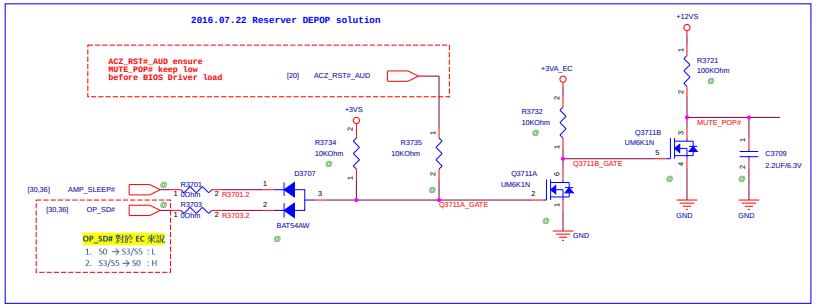
2015.12.16 EMI Reserve

MUTE CONTROL

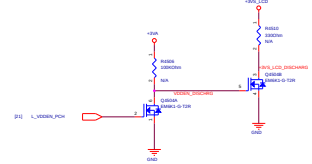
2017.03.23 AMP Change Remove

MUTE CONTROL new solution for 1.8V HDA BUG 0318

2016.07.22 Reserver DEPOP solution



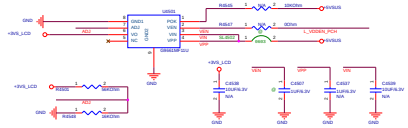
ASUS	Project Name G711GW		Rev 1.0
Title : AUDIO ALC3236-CG/VB2 Jack			
Size C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Marshall Li	
Date: Tuesday, April 16, 2019	Sheet 37	of 103	

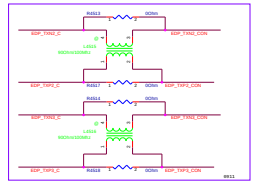


R4510 is selected by Panel spec

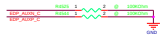
Current Limit vs. R_{ILIM} Values

R_{ILIM} (Ω)	Min. Current Limit (mA)	Typ. Current Limit (mA)	Max. Current Limit (mA)
6.65k	2730	3000	3300
7.68k	2430	2700	2970
8.25k	2230	2500	2750
9.53k	1999	2200	2420
10.5k	1830	2000	2200
11.5k	1620	1800	1980
14.3k	1330	1500	1650
17.4k	1090	1250	1320
21k	900	1000	1100

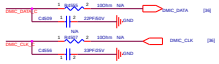




eDP from CPU

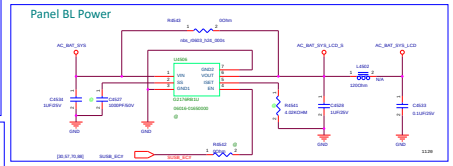


MIC

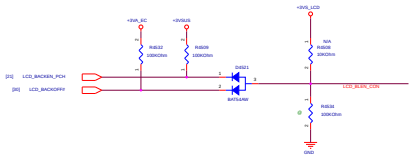


MIC module

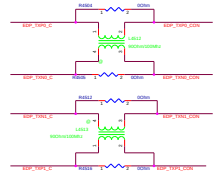
Panel BL Power



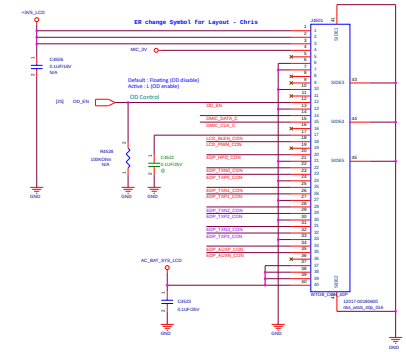
Panel

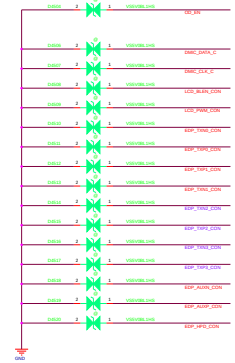


For EMI



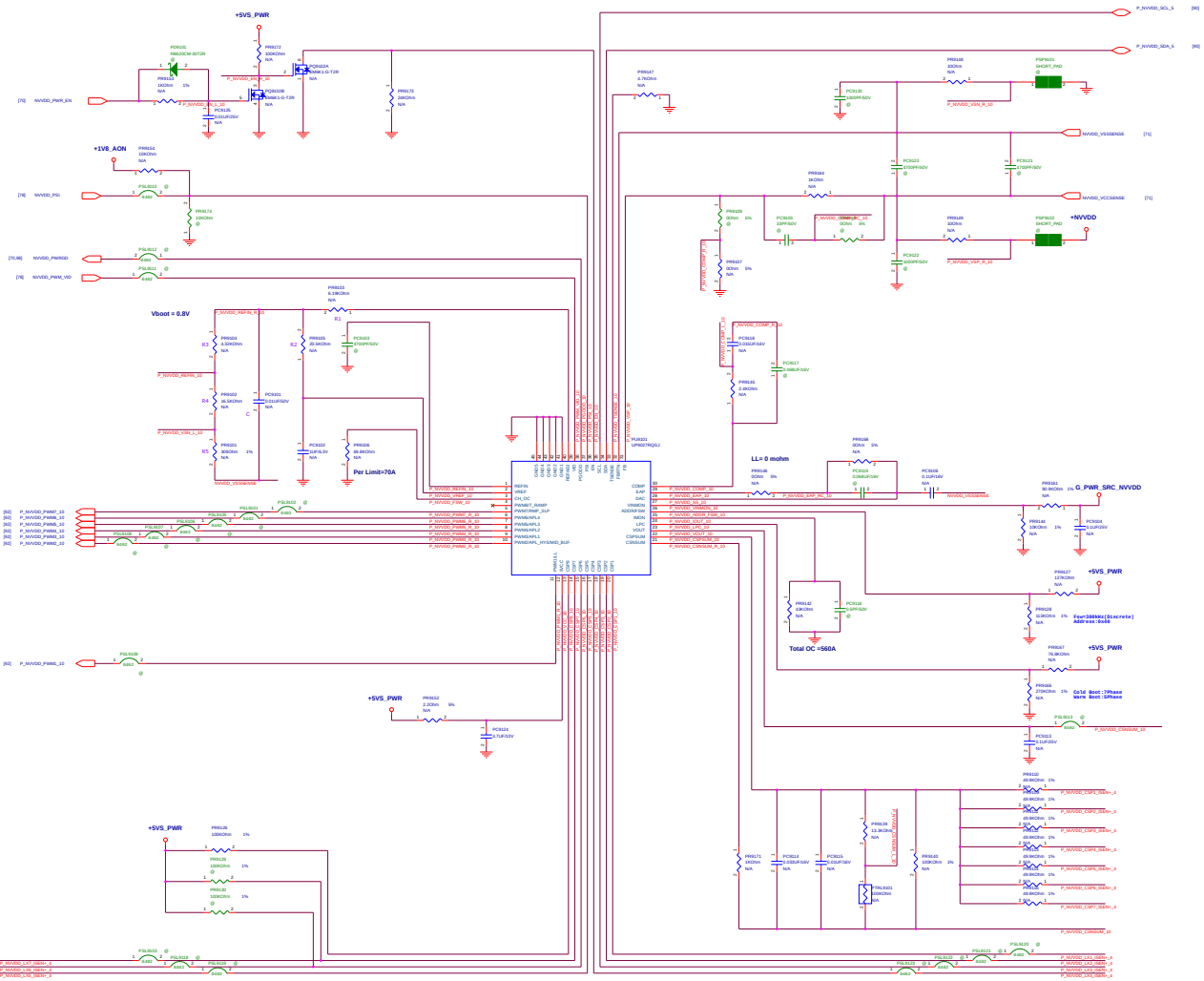
eDP Panel Conn.



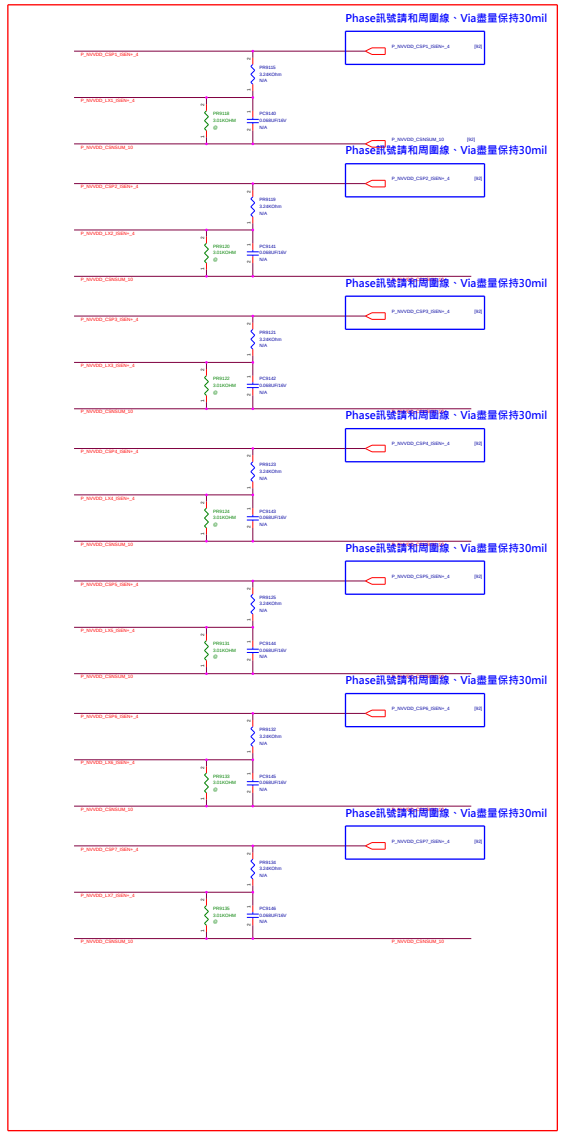


ASUSTeK COMPUTER	Title :	CRT_eDP	
	Engineer:	Gaming RD	
Size: D	Project Name: G711GW		Rev: 1.0
Date: Tuesday, April 09, 2019	Sheet: 65	of: 100	

+NVVDD [For DGPU]



請放靠近PU9101



ASUS	Project Name: G711GW		Rev: R1.0
Title :	PW_NVVDD (0)		
Size: A1	Dept.: NB Power team	Engineer: Neil	
Date: Tuesday, April 09, 2019	Sheet 91 of 103		

Address Selection Table

Address	0x78	0x7C	0x7A	0x7E	0x76	0x72	0x7A	0x7E
PR9801	10k	1.5k	2k	2.5k	3.9k	6.3k	9.1k	4k
PR9802	Open	6.2k	6.2k	6.8k	8.7k	9.6k	2.7k	2k

Register Address

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06
R/W	W	W	W	R	R	R	R
Function	Temp. alert threshold setting		Sensed temp. data				bit 4 = 0 bit 3 = 0 bit 2 = 0 bit 1 = 0 bit 0 = 0 When ALERT# asserted

PROTECTION

Cost-down不開

Cost-down不開

Cost-down不開

Cost-down不開

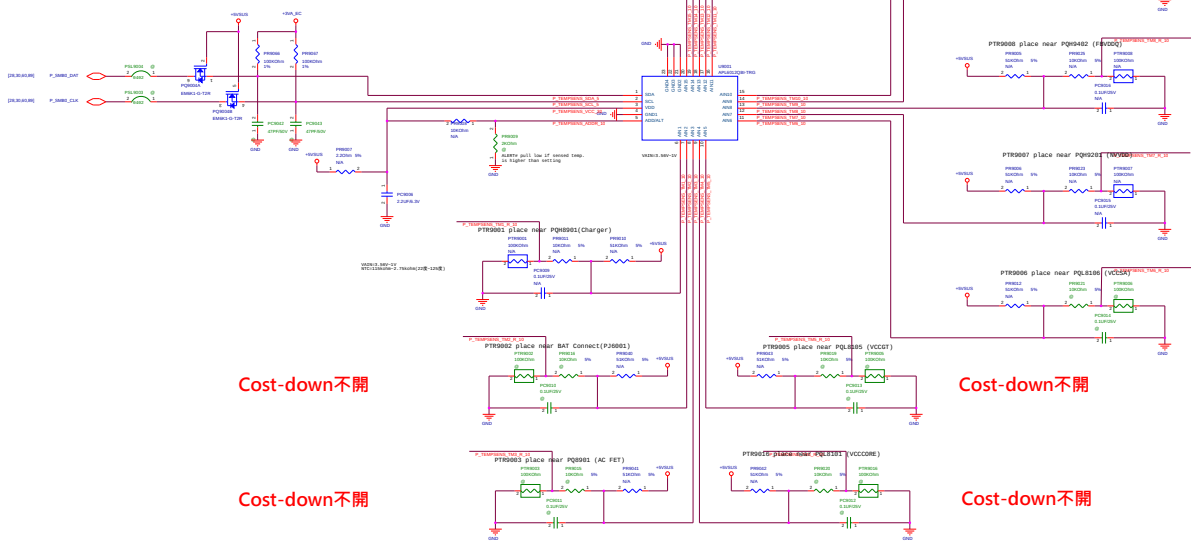
Cost-down不開

Cost-down不開

Cost-down不開

Cost-down不開

Cost-down不開



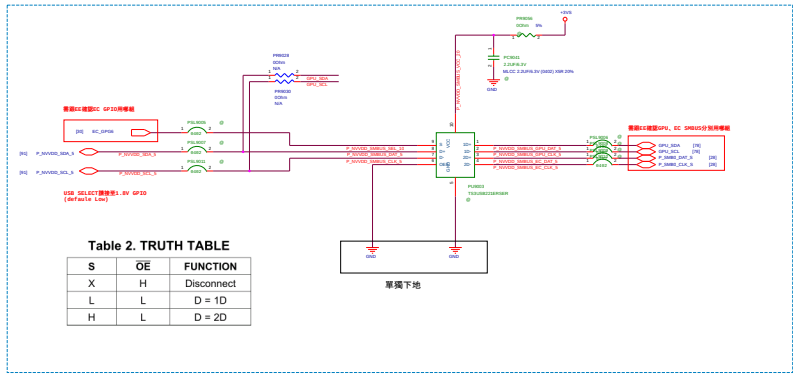
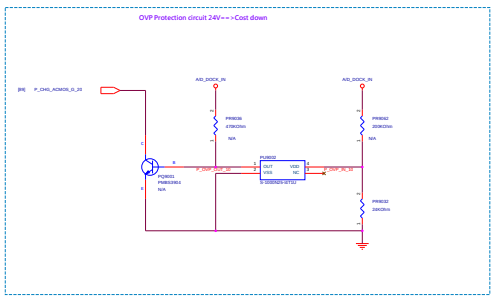
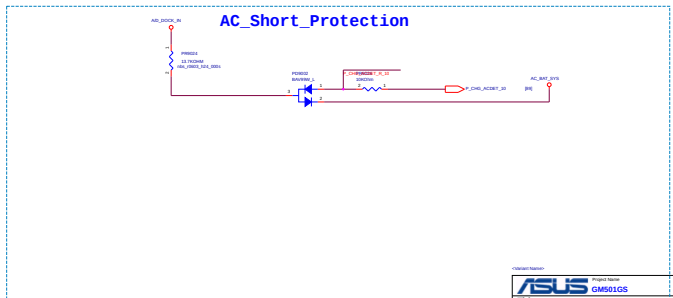


Table 2. TRUTH TABLE

S	$\overline{OE}$	FUNCTION
X	H	Disconnect
L	L	D = 1D
H	L	D = 2D





ASUS GM501GS

Title : Net Inspection

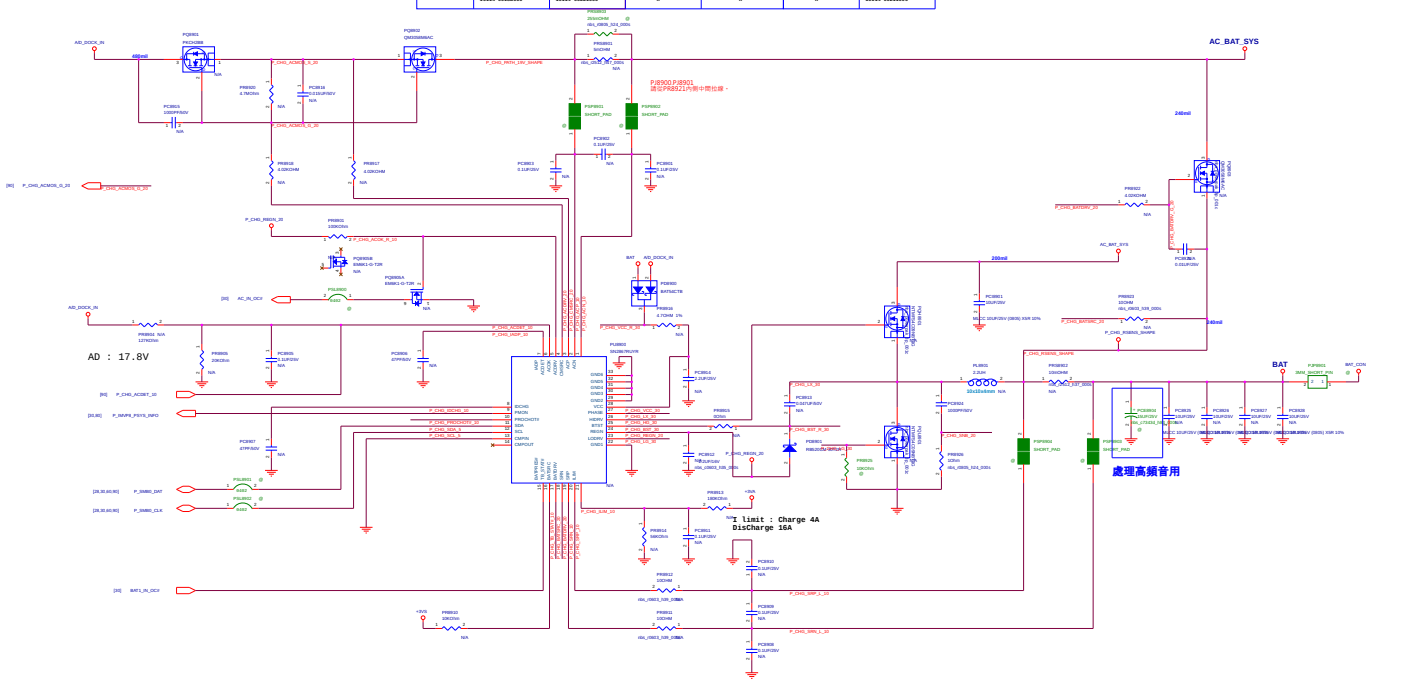
Dept.: NB Power Team

Engineer: Edison

Date: Tuesday, April 16, 2019

PRS8901	ADP<120W	ADP<=230W	ADP>230W	ADP>330W
	TBD	5m	5m	2m
	TBD	10125-00008100	10108-00008000	10103-00008000

PRS8903	ADP<120W	ADP<=150W	ADP<180W	ADP<230W	ADP<280W	ADP<330W
	200m	255m	X	X	X	560m
	10114-00108000	10114-00221000	X	X	X	10114-00211000

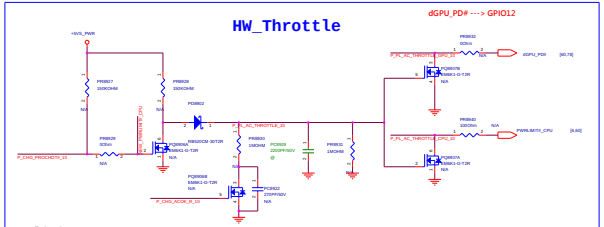


Adaptor select
total power = 90% ADP

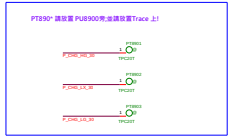
Adaptor select

	N Series	6 Series
PR8921	10m	5m
PR8936		
14K	0.4V	30W	120W
31.6K	0.8V	40W	150W
56K	1.2V	45W	180W
93.1K	1.6V	65W	230W
150K	2.0V	75W	280W
270K	2.4V	90W	330W
560K	2.8V	120W	400W

HW_Throttle



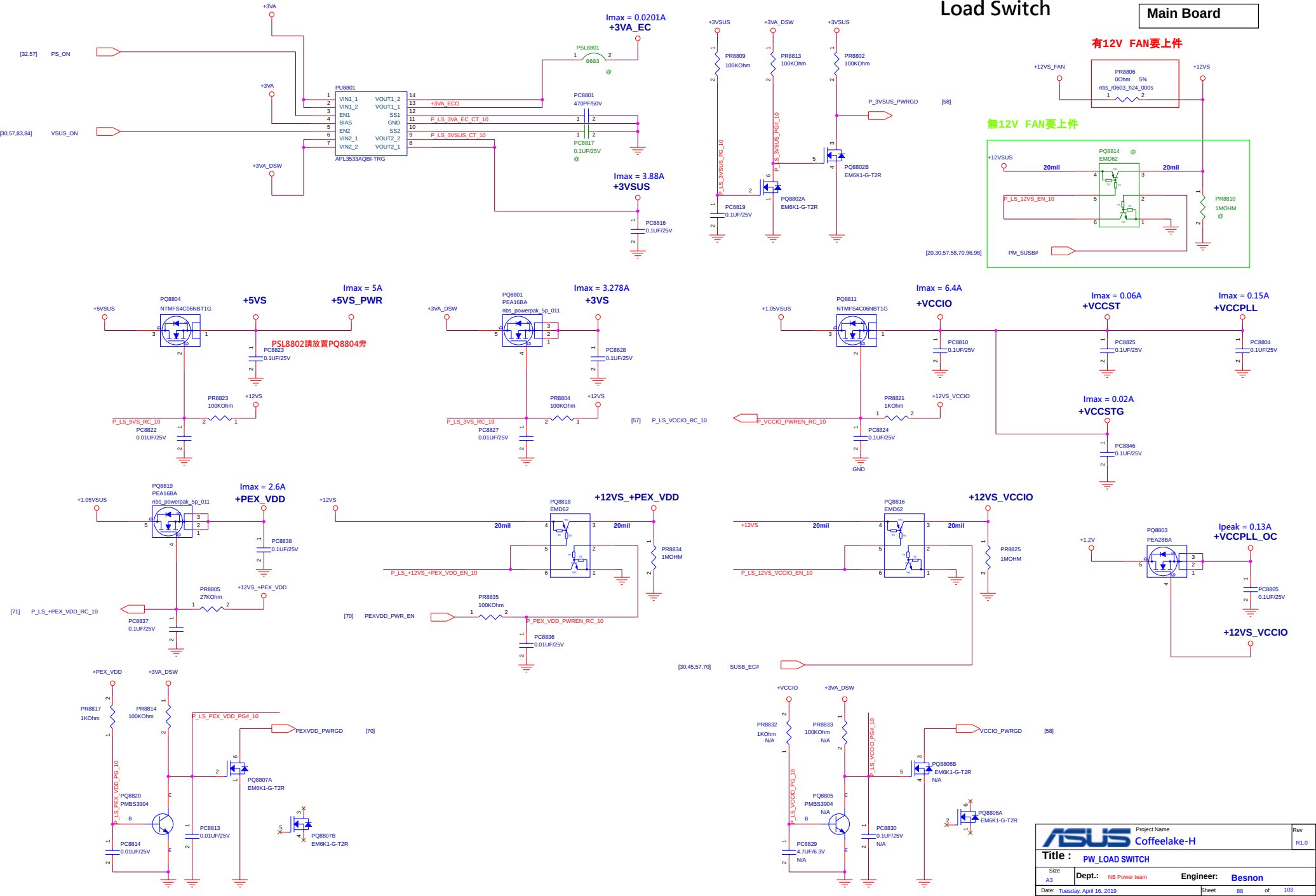
AC limit = 100% ADP
Bat limit = byte 7 x 1.7



ASUS	Project Name: Coffee lake-H	Rev: R1.0
Title :	PW_CHARGER	
Size: A2	Dept.: MB Power Team	Engineer: Benson
Date: Tuesday, April 09, 2019	Sheet: 85 of 103	

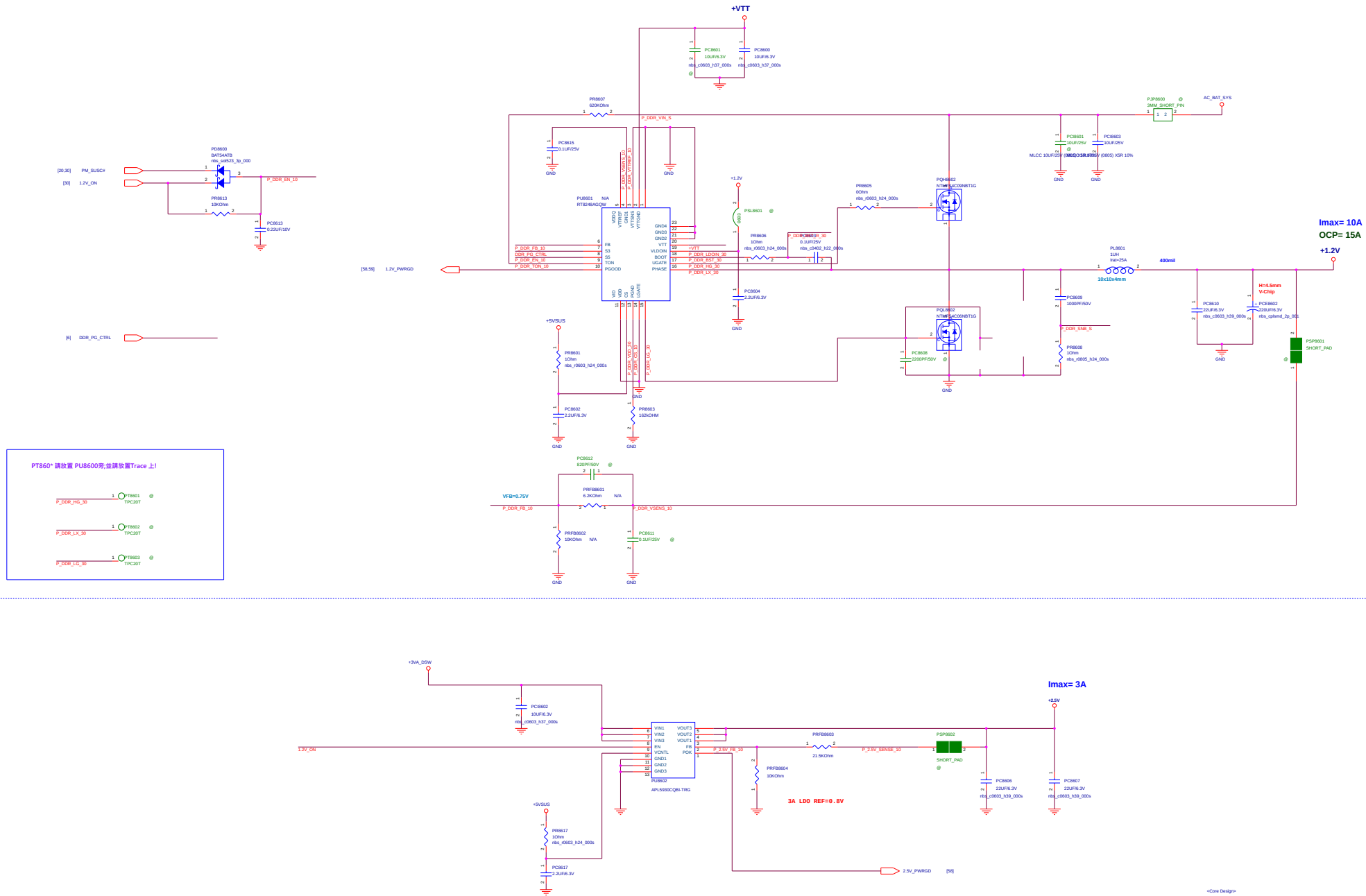
Load Switch

Main Board



Project Name: Coffeelake-H			Rev: R1.0
Title : PW_LOAD SWITCH			
Size: A3	Dept.: NB Power team	Engineer: Besnon	
Date: Tuesday, April 16, 2019	Sheet 88 of 103		

+1.2V / +VTT / +2.5V[For Memory]



<Core Design>

ASUS	Project Name: G711GW		Rev: R1.0
Title : PW_+1.2V/+VTT/+2.5V			
Size: A2	Dept.: NB Power team	Engineer: Neil	
Date: Tuesday, April 16, 2019	Sheet 86 of 103		

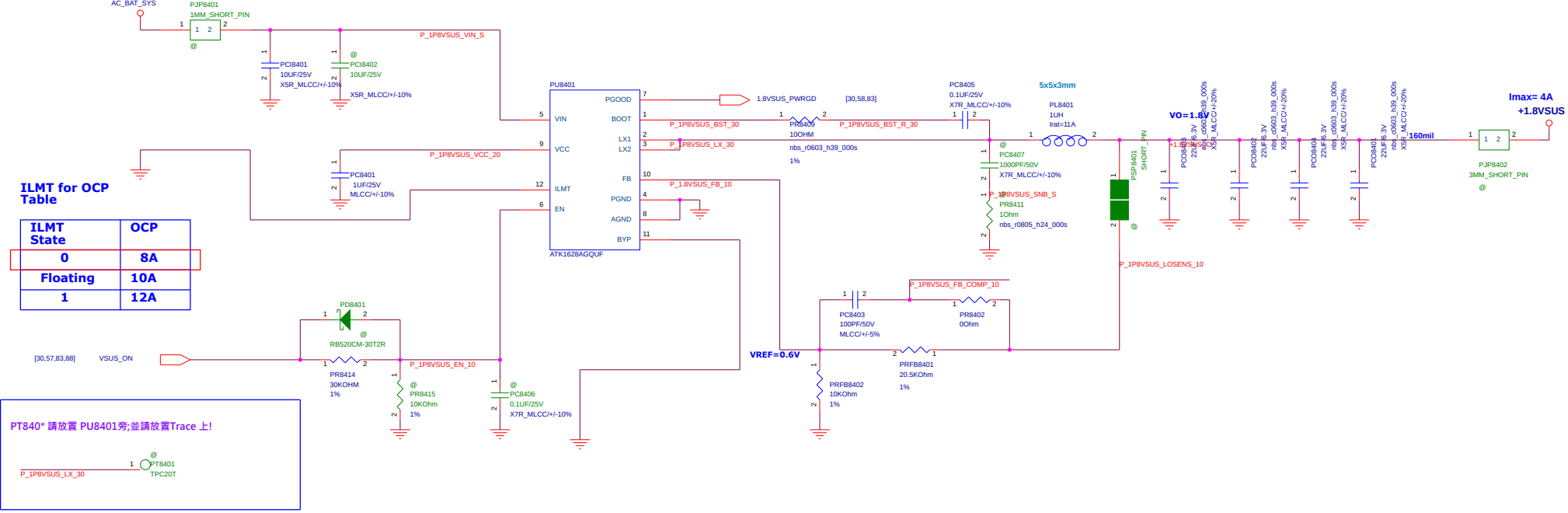
<Variant Name>

	Project Name GM531GX	Rev R1.0

Title : Thunderbolt

Size	Dept.:	Engineer:
Custom	ASUS Power Team	Joe

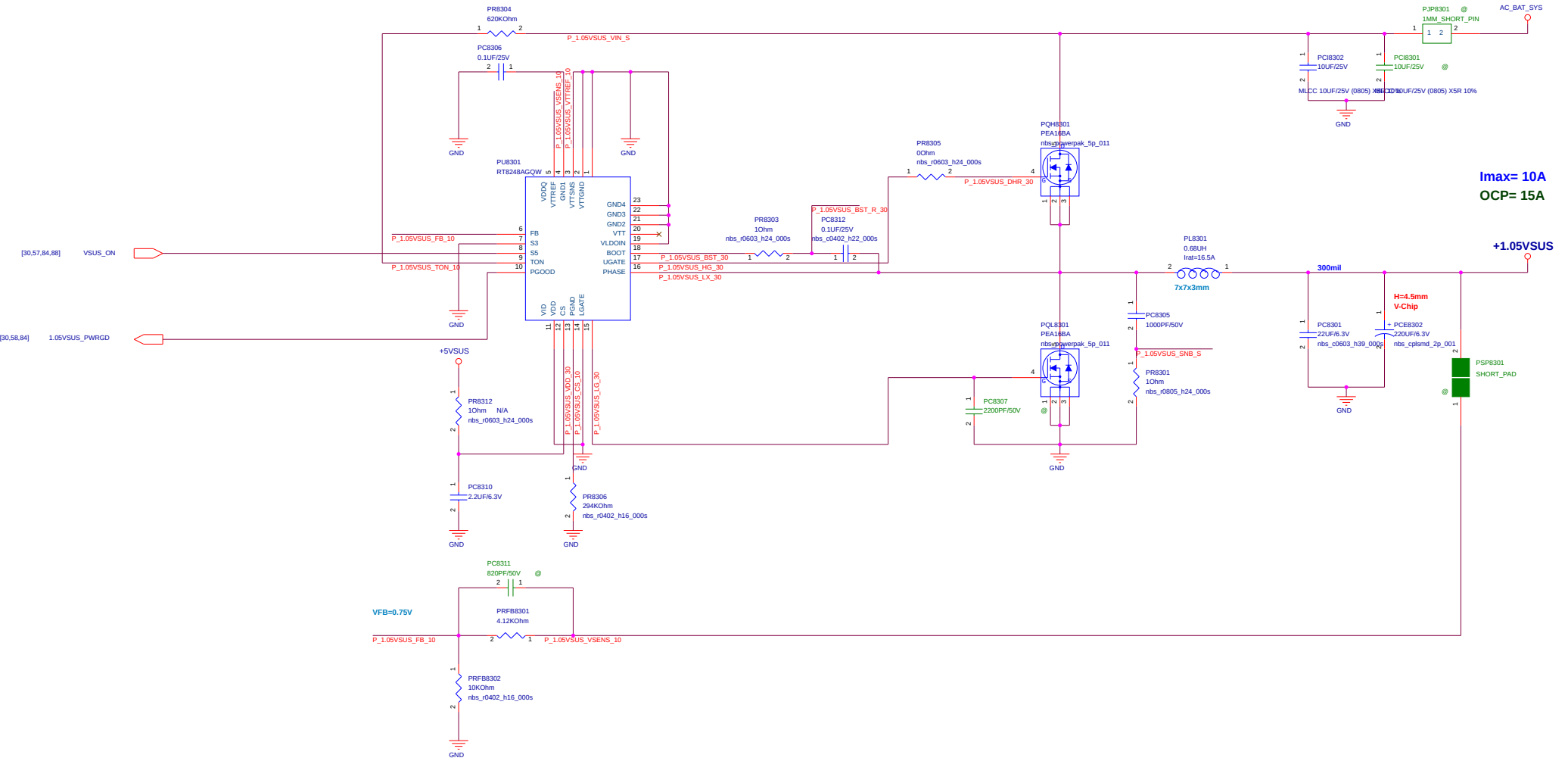
Date: Tuesday, April 16, 2019	Sheet	85	of 103



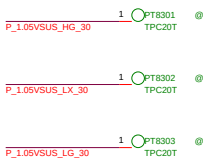
<Variant Name>

Project Name: FX505DY		Rev: R1.0
Title : PW_+1.8VSUS		
Size: A3	Dept.: NB Power team	Engineer: CS Lin
Date: Tuesday, April 16, 2019	Sheet 84 of 103	

+1.05VSUS [For PCH]



PT830* 請放置 PU8301旁;並請放置Trace 上!



Project Name: G711GW			Rev: R1.0
Title : PW_+1.0VSUS			
Size: A3	Dept.: NB Power team	Engineer: Neil	
Date: Tuesday, April 16, 2019	Sheet 83 of 103		

<Core Design>

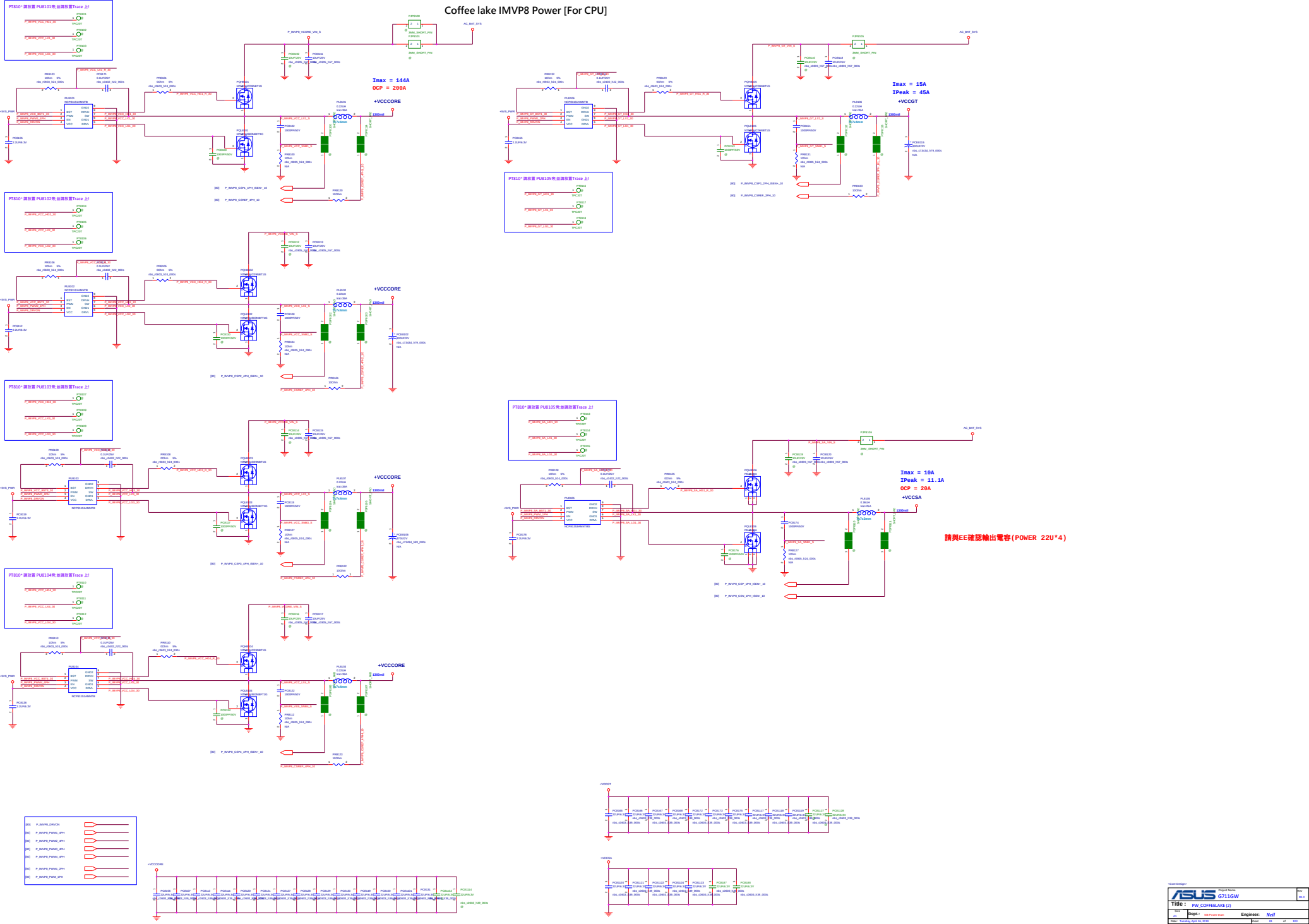
	Project Name GM531GM	Rev R1.0

Title : PW_+VCCIO

Size A3	**Dept.:** NB Power team	**Engineer:** *Joe*

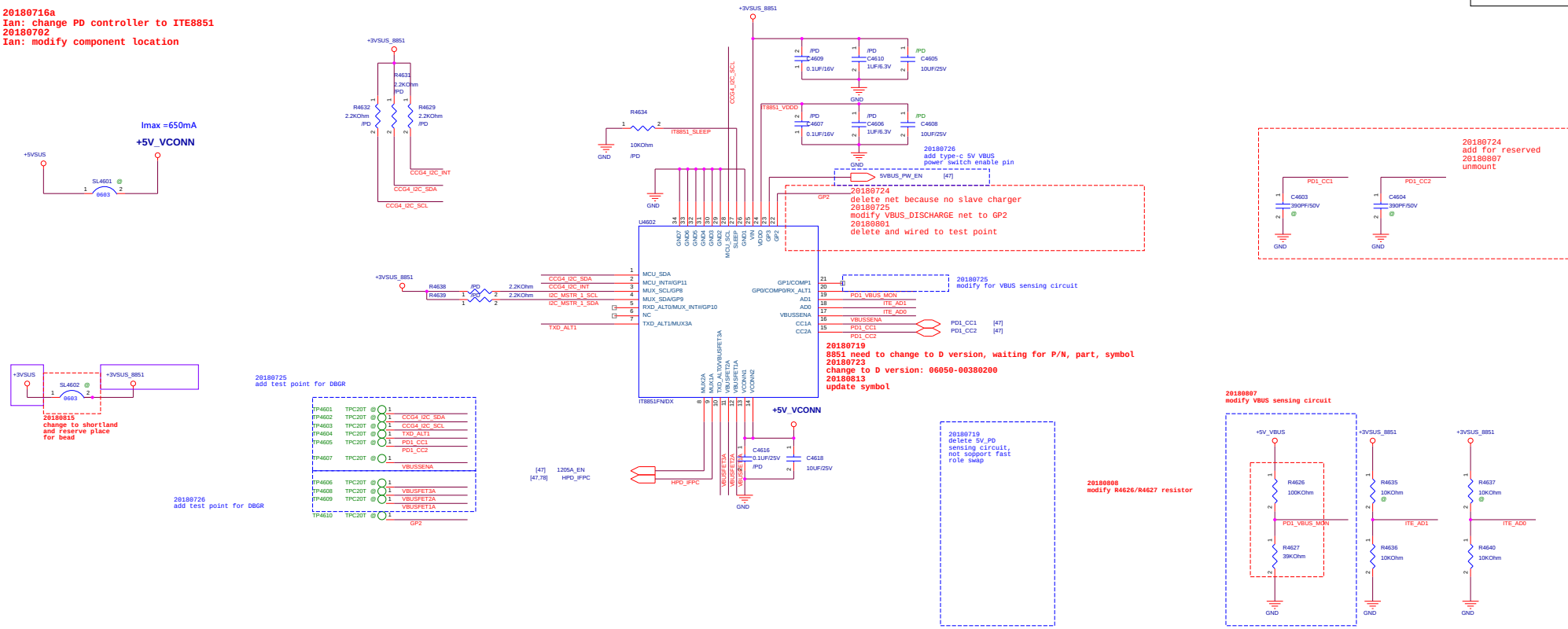
Date: Tuesday, April 16, 2019	Sheet	82	of	103

Coffee lake IMVP8 Power [For CPU]

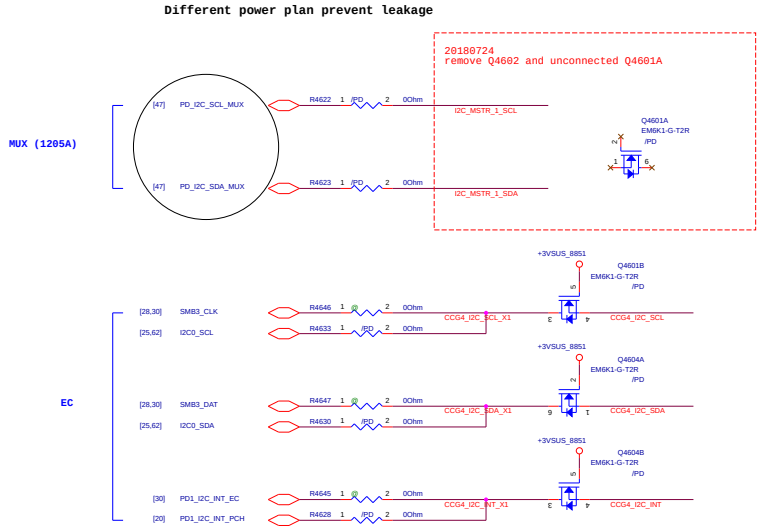


ASUS	Project Name: G711GW		Rev: X01.0
Title :	PW_COFFELAKE (2)		
Size: A3	Dept.: NB Power Team	Engineer: Neil	
Date: Tuesday, April 10, 2018	Sheet 91 of 103		

20180716a
Ian: change PD controller to ITE8851
20180702
Ian: modify component location



Different power plan prevent leakage



6.3 I2C0 Slave ID Decode

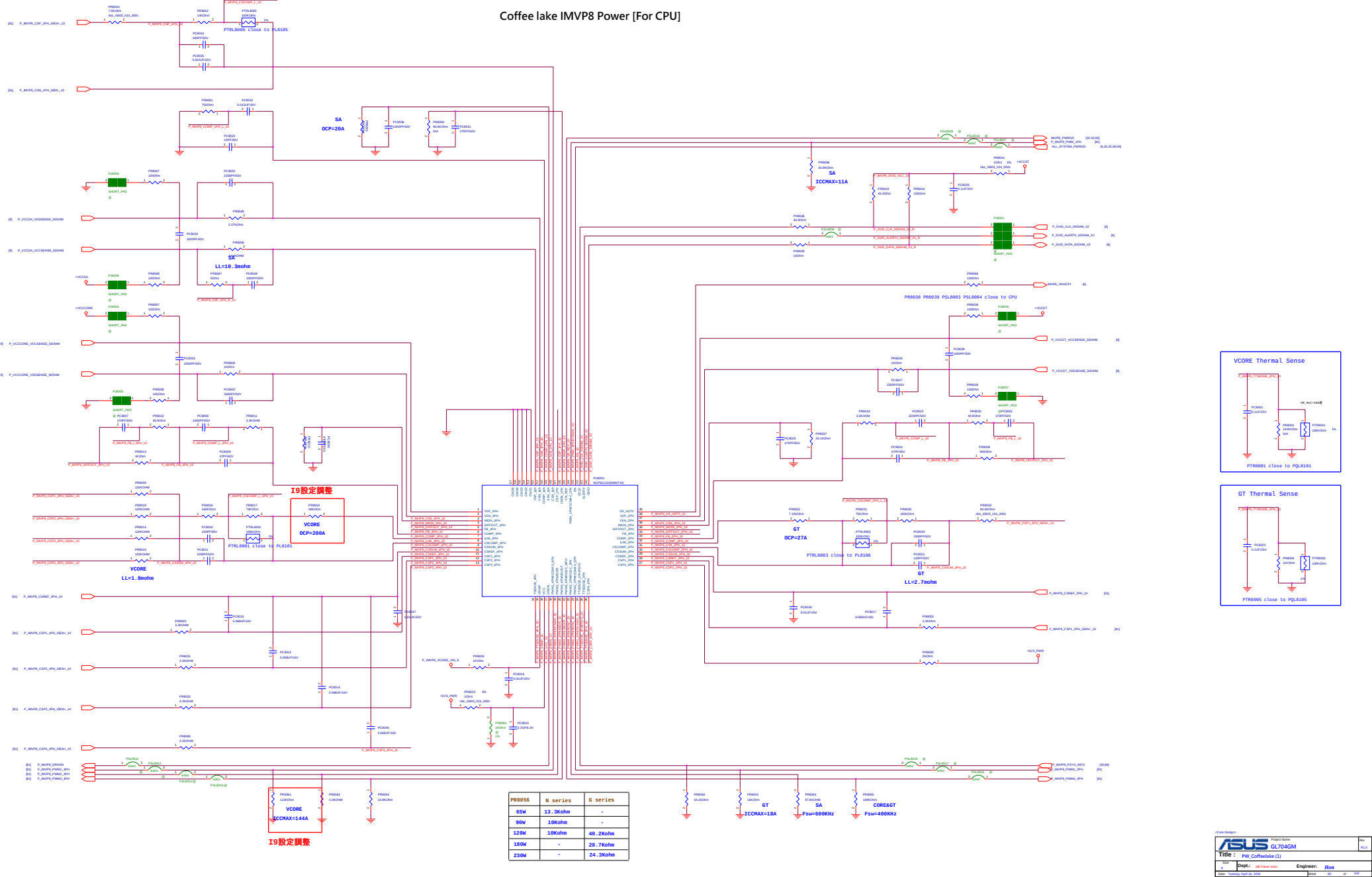
IT8851 provides one I2C slave interface, I2C0, for communication and four different slave ID decodes for I2C0 slave.

Table 6-1. I2C0 Slave ID Decode

AD1	AD0	Slave ID
0	0	7'h40
0	1	7'h42
1	0	7'h50
1	1	7'h52

Project Name	G711GW	Rev 1.0
Title :	PD_IT8851FN	
Size C	Dept.: ASUSTeK COMPUTER	Engineer: Wendell_Lo
Date: Tuesday, April 16, 2019	Sheet 46 of 103	

Coffee lake IMVP8 Power [For CPU]



PR8056	N series	G series
65W	13.3Kohm	-
90W	10Kohm	-
120W	10Kohm	40.2Kohm
180W	-	28.7Kohm
230W	-	24.3Kohm

Main Board

Internal Regulator option

LDO OUT

LDO IN

20180813
change to +1.8VS for improving transfer efficiency

20180815
SL4801: bead change to shortland

20180815
delete short land

HDMI Active-Level Shift

FW update path

20180814
上件, HP那改不上件

20180813
最高边层此IC應用不同
原為應用在Cable/box才需接TX

20180731
change HDMI retimer to IT66317

Output Swing	GPIO	URDBG
Level 1 (Lowest)	0	0
Level 2 (Default)	0	1
Level 3	1	0
Level 4 (Highest)	1	1

20180810
add 10K pull-up

PCADR:
Control of serial programming device address
0:0x78 (defaul , internal pull down)
1:0x7A

20180807
add for output swing HW control

HDMI PWR_+5VS_HDMI

HDMI Conn.

ER change to 4.7K ohm
for HDMI protocol

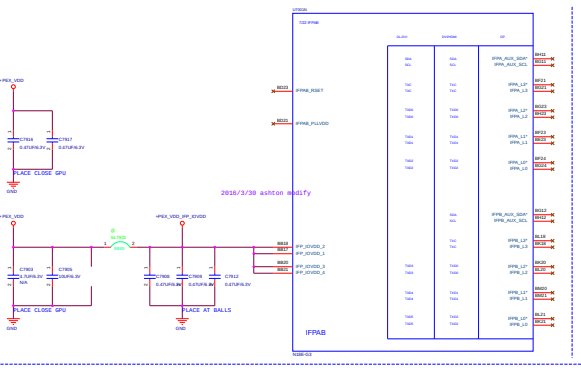
20180810
R4816 change to 47kohm

20180810
delete dcma

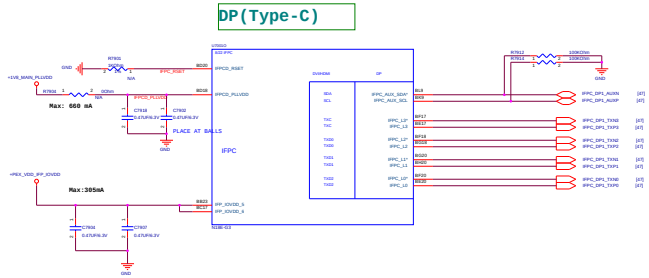
HDMI EMI

Project Name	G711GW
Rev	1.3
Title :	HDMI
Size	Custom
Dept.:	ASUSTeK COMPUTER INC.
Engineer:	EE1_RD3
Date:	Tuesday, April 16, 2019
Sheet	48 of 103

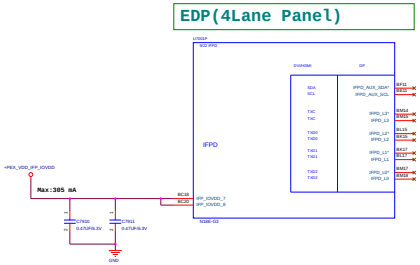
Main Board



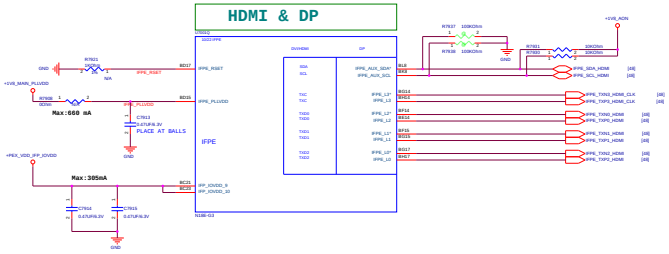
DP(Type-C)

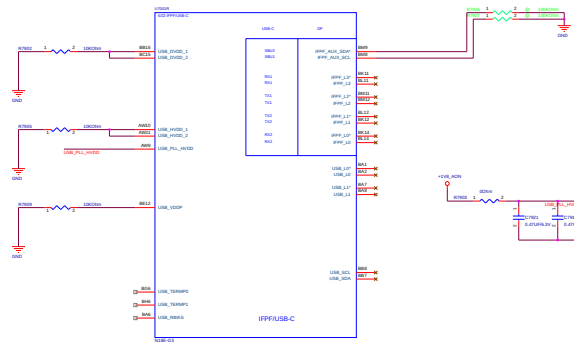


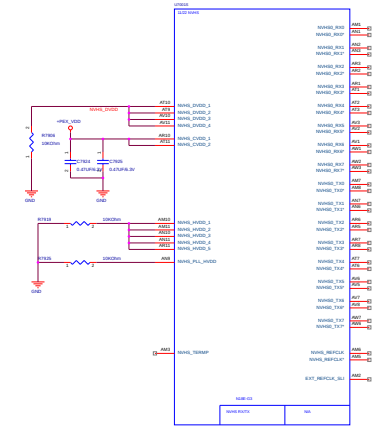
EDP(4Lane Panel)



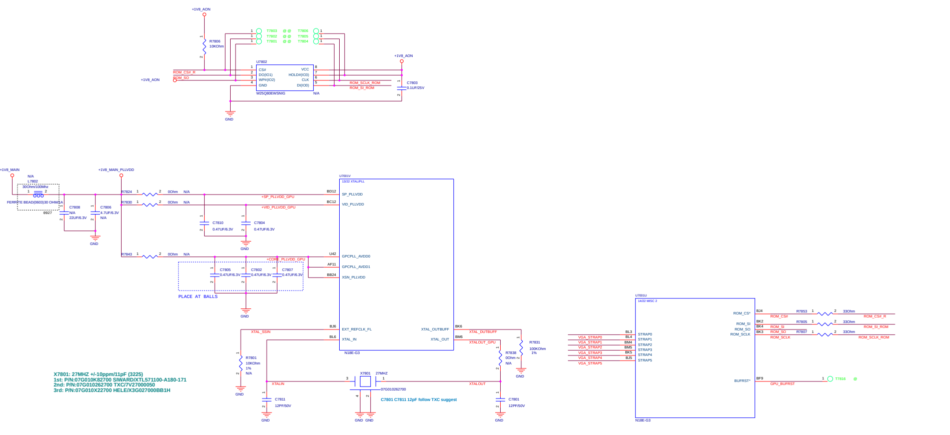
HDMI & DP

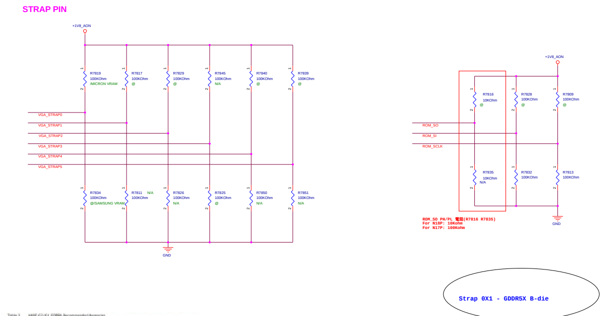






ASUS	Project Name: G711GW		Rev: 2.0
Title: GPU_DP&EDP&HDMI			
Size: D	Dept.: Abyssmal COMPUTER	Engineer: Gaming RD	
Date: Tuesday, April 16, 2019	Sheet: 79	of: 103	





Level Option	Physical Configuration: Pull-Up to 1.8V via resistor (see Note 1). (Notebook designs also see Note 2.)	Pull-Down to GND via resistor Note 1
1.8V ("HIGH") Level	Populate	No Stuff
0.9V ("MIDDLE") Level	Populate	Populate
GND ("LOW") Level	No Stuff	Populate

Note 1: Resistor should be 100K Ohms. 5% tolerance is acceptable.
Note 2: Notebook graphics circuit designs should pull up to the 1V8_AON rail rather than to 1V8_MAIN.

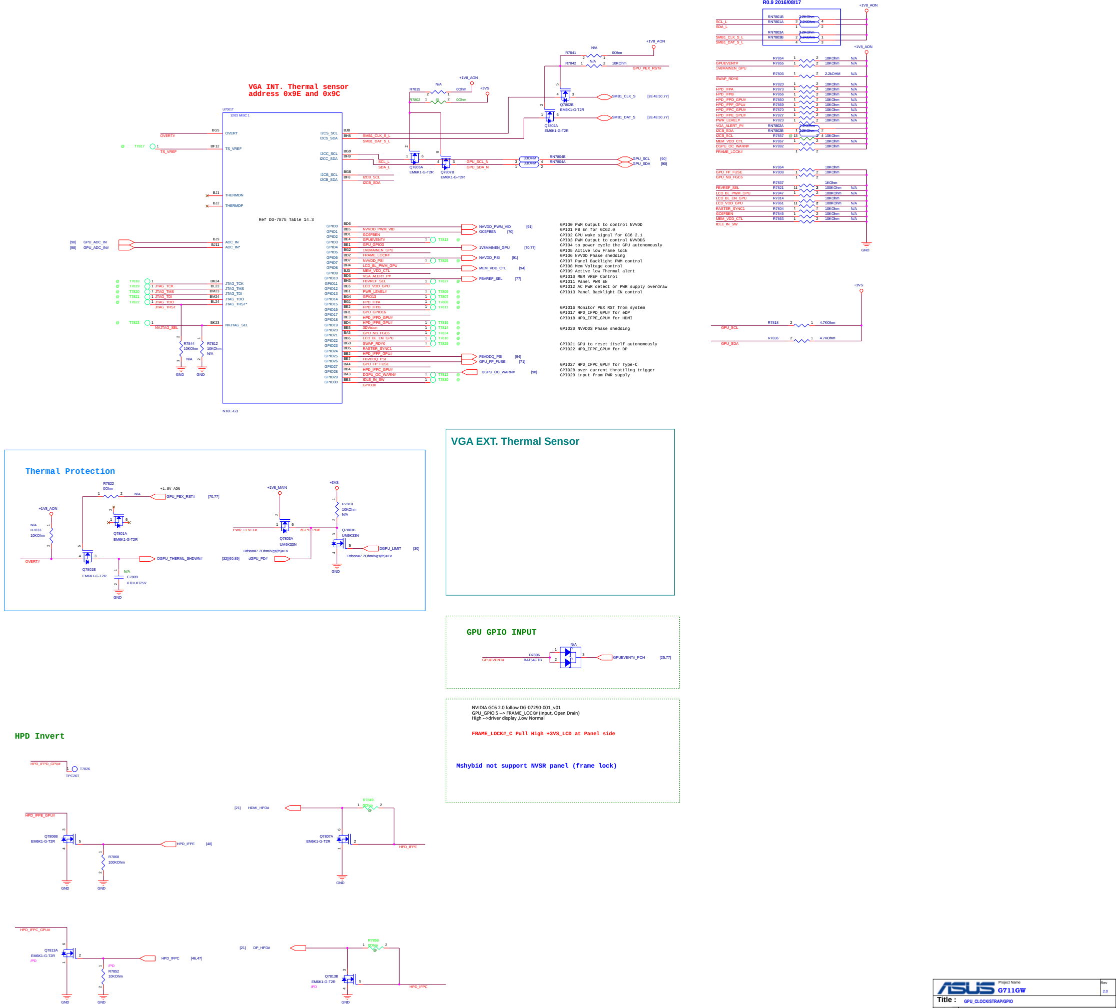
Assorted Configuration Straps:
1. SMB_ALT_ADDR Enable: [illegible]
2. DEVID_SEL: G-sync function→"0"normal GPU ID, "1" support G-sync GPU ID
3. PCIE_CFG: PCIE Swing→"0" PCIE Swing default, "1" PCEI swing reduce
4. VGA_DEVICE: Graphics circuit→"0" MS-Hybrid, "1" Discrete

Strap Pins see Note: ROM_SO	ROM_SI	ROM_SCLK	FS_OVERT* Function
L	L	L	FS_OVERT* function ENABLED
L	L	H	FS_OVERT* function DISABLED (Reserved; do not configure)
all other configurations			(Invalid; do not configure)

Strap Pins see Note: STRAP2	STRAP1	STRAP0	RAMCFG Setting Number (see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)
M	H	L	14 (0x000E)
M	H	H	15 (0x000F)
H	L	M	16 (0x0010)
H	M	L	17 (0x0011)
H	M	H	18 (0x0012)
H	H	M	19 (0x0013)
L	M	M	20 (0x0014)
M	L	M	21 (0x0015)
M	M	L	22 (0x0016)
M	M	H	23 (0x0017)
M	H	M	24 (0x0018)
H	M	M	25 (0x0019)
M	M	M	26 (0x001A)

Strap Pins see Note: STRAP5	STRAP4	STRAP3	Functions Selected by This Strapping: SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0

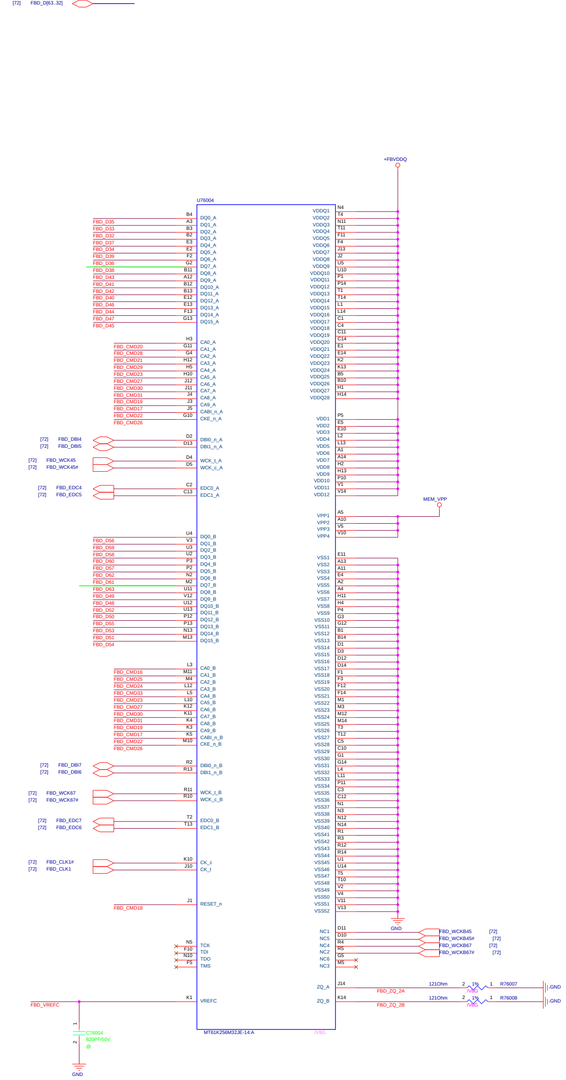
Total Display Links (HDMI, DP or DVI)	Total Enabled for Audio (HDMI, DP or DVI)	Is eDP Supported on: IFPA or IFPB?	IFPC or IFPD?	IFPE or IFPF?	See This Row of Table 5.4
4	4	--	--	--	15
4	3	yes	--	--	14
4	3	--	yes	--	13
4	3	--	--	yes	12
3	3	--	--	--	[illegible]
3	2	yes	--	--	[illegible]
3	2	--	yes	--	12
3	2	--	--	yes	10
2	2	--	--	--	[illegible]
2	1	yes	--	--	8
2	1	--	yes	--	8
2	1	--	--	--	8
1	1	--	--	--	8
1	0	yes	--	--	8
1	0	--	--	--	8
1	0	--	--	yes	8



Project Name: G711GW
Rev: 2.0
Title: GPU_CLOCK/STRAP/GPIO
Size: Custom
Dept.: ASUSTeK COMPUTER
Engineer: Gaming RD
Date: Tuesday, April 16, 2019

40 OHm_NET
FBD Partition 31..0
MF=1 Mirror

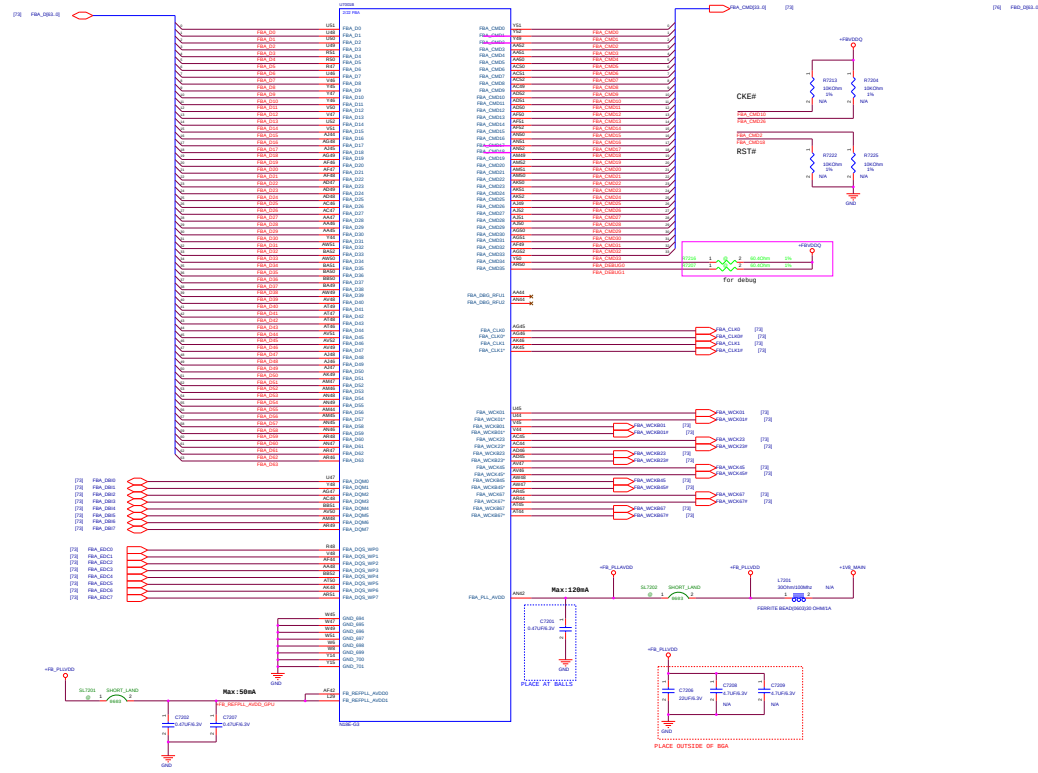
40 OHm_NET
FBDPartition 64..32
MF=0 Normal



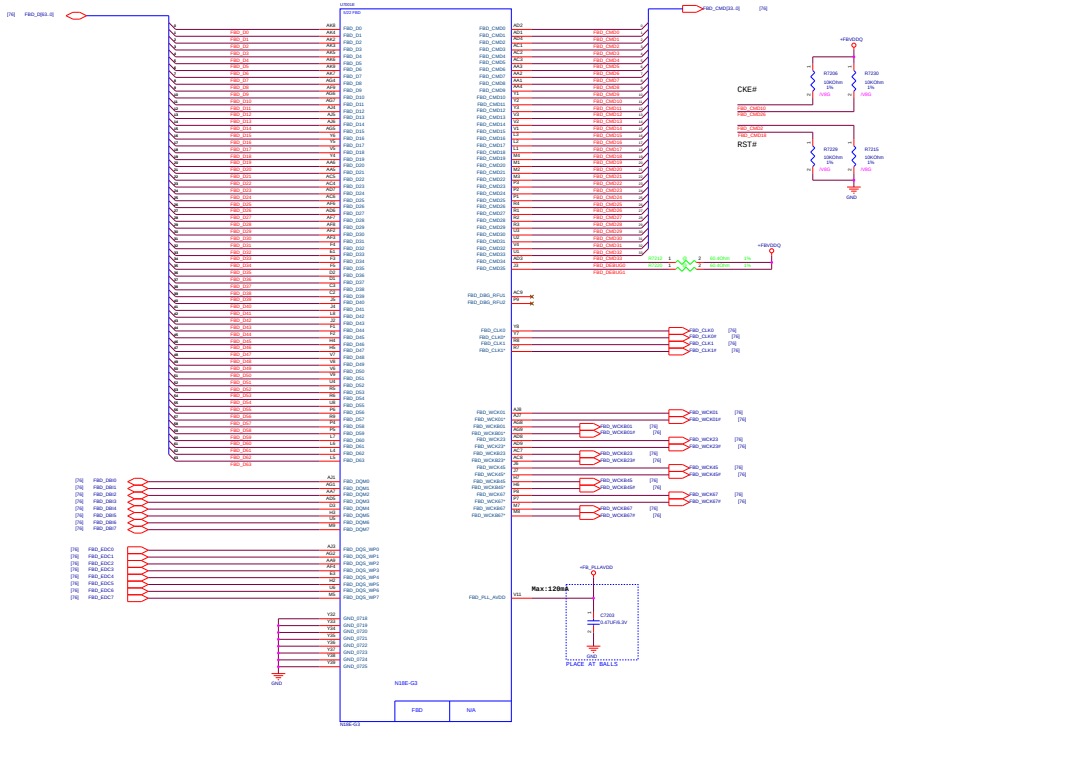
<Variant Name>

Title	<Title>	
Size A1	Document Number G711GW	Rev R1.0
Date: Tuesday, April 16, 2019	Sheet 76 of 103	

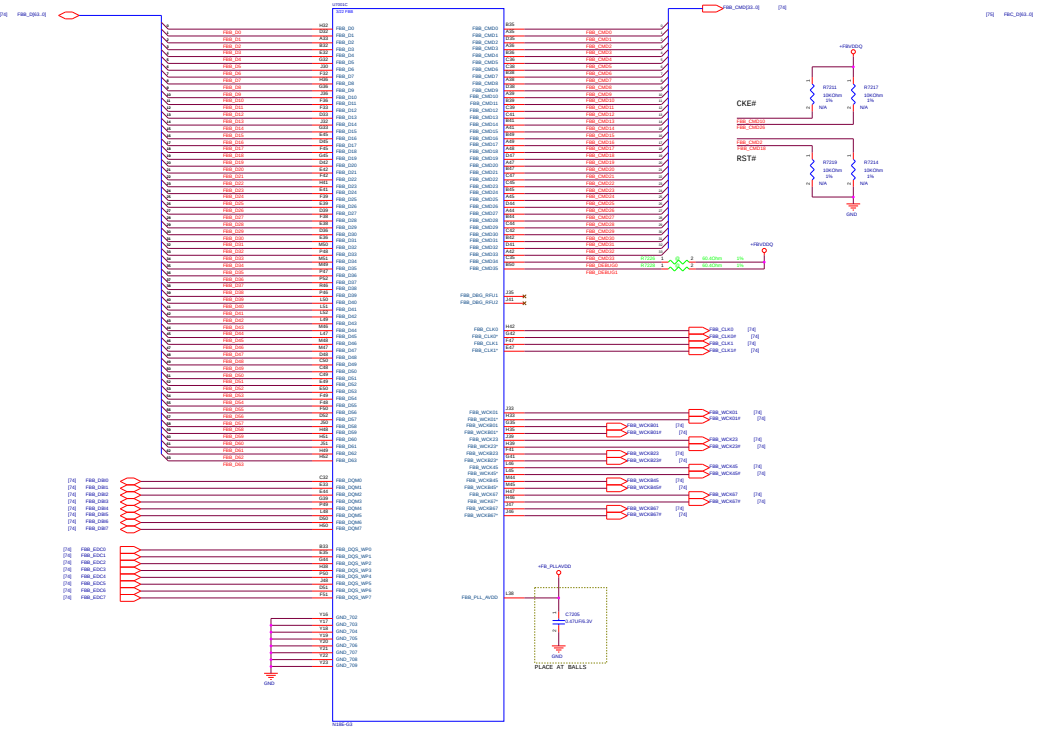
MEMORY: GPU FB Partition A



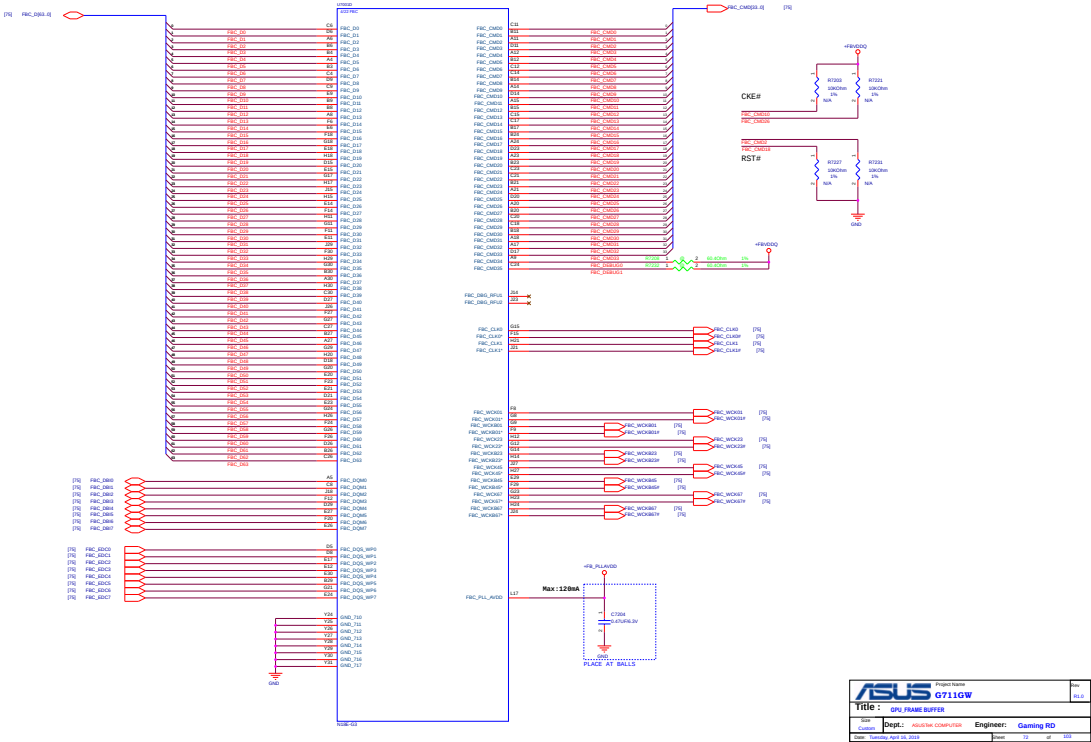
MEMORY: GPU FB Partition D



MEMORY: GPU FB Partition B



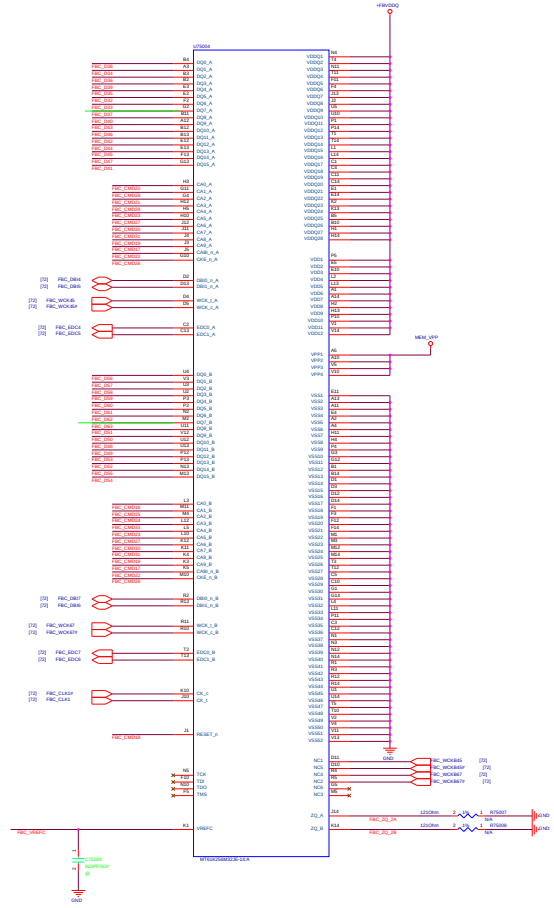
MEMORY: GPU FB Partition C



ASUS	Project Name: G711GW		Rev: 81.0
Title :	GPU_FRAME BUFFER		
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Tuesday, April 16, 2019	Sheet: 72 of 103		

40 OHm_NET
FBC Partition 31..0
MF=1 Mirror

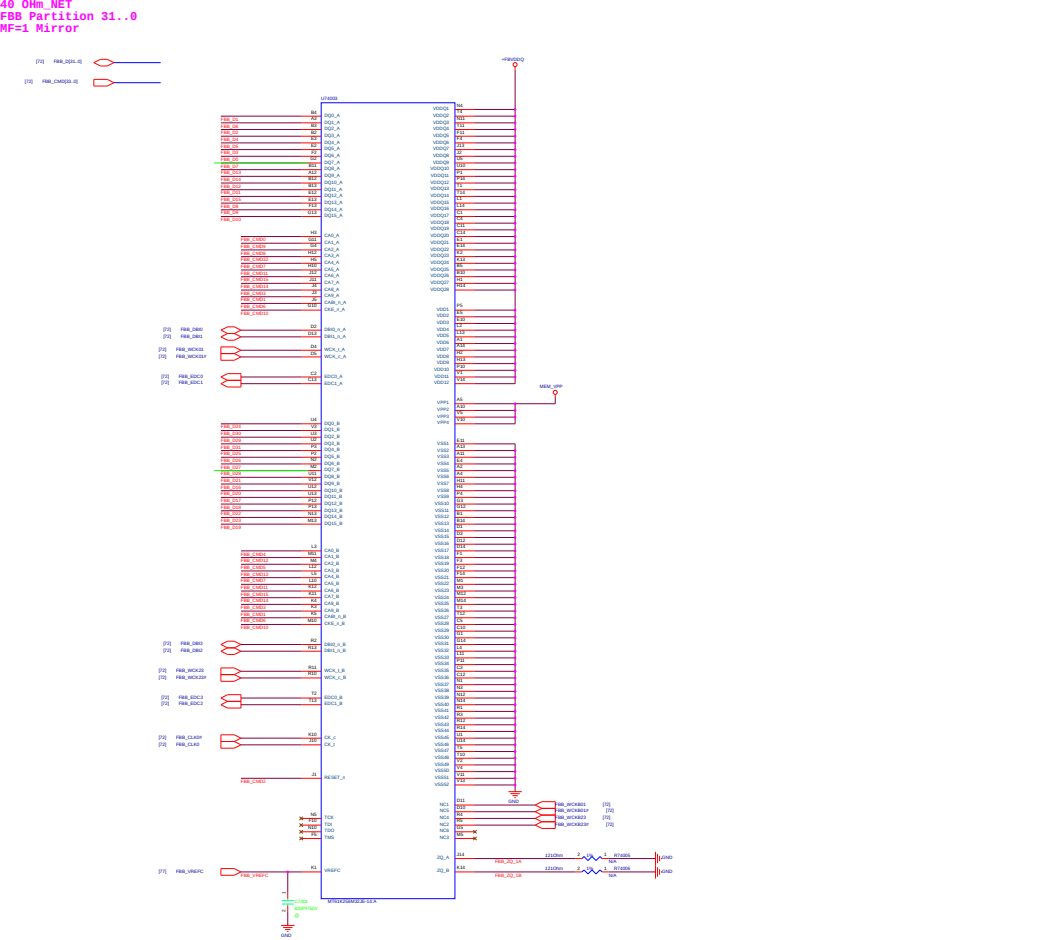
40 OHm_NET
FBC Partition 64..32
MF=0 Normal



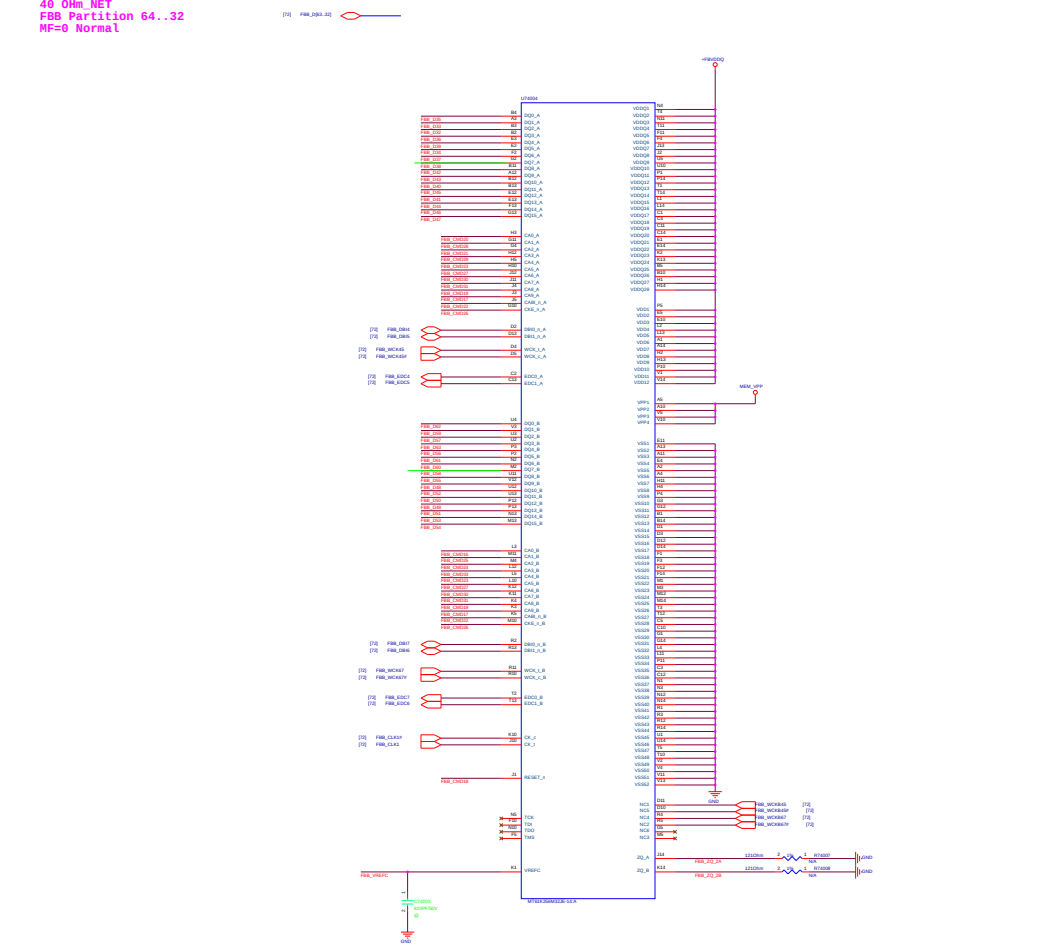
<variant_name>

Title:	<Title>		
Size: A1	Document Number: 07710234		Rev: R1.0
Date: Tuesday, April 16, 2019	Sheet: 75	of:	103

40 OHm_NET
FBB Partition 31..0
MF=1 Mirror



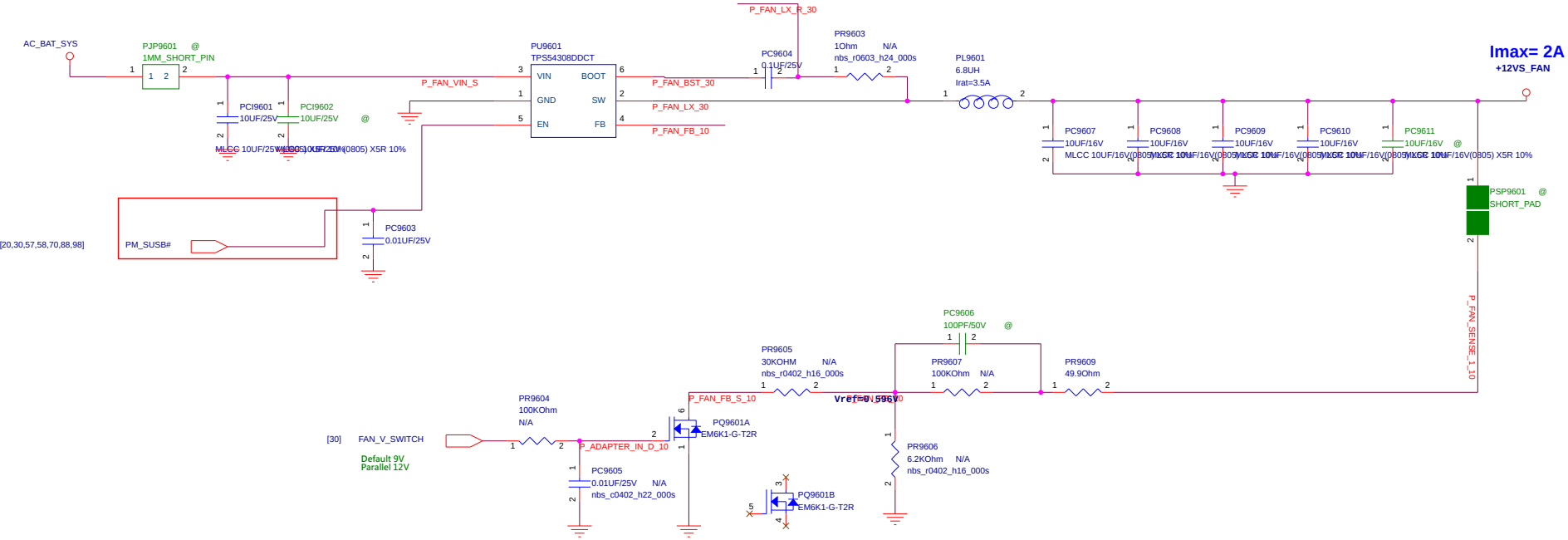
40 OHm_NET
FBB Partition 64..32
MF=0 Normal



<Variant Name>

Title:	<Title>
Size: A4	Document Number: 0710230
Rev: 01.0	
Date: Tuesday, April 16, 2019	Sheet: 11 of 120

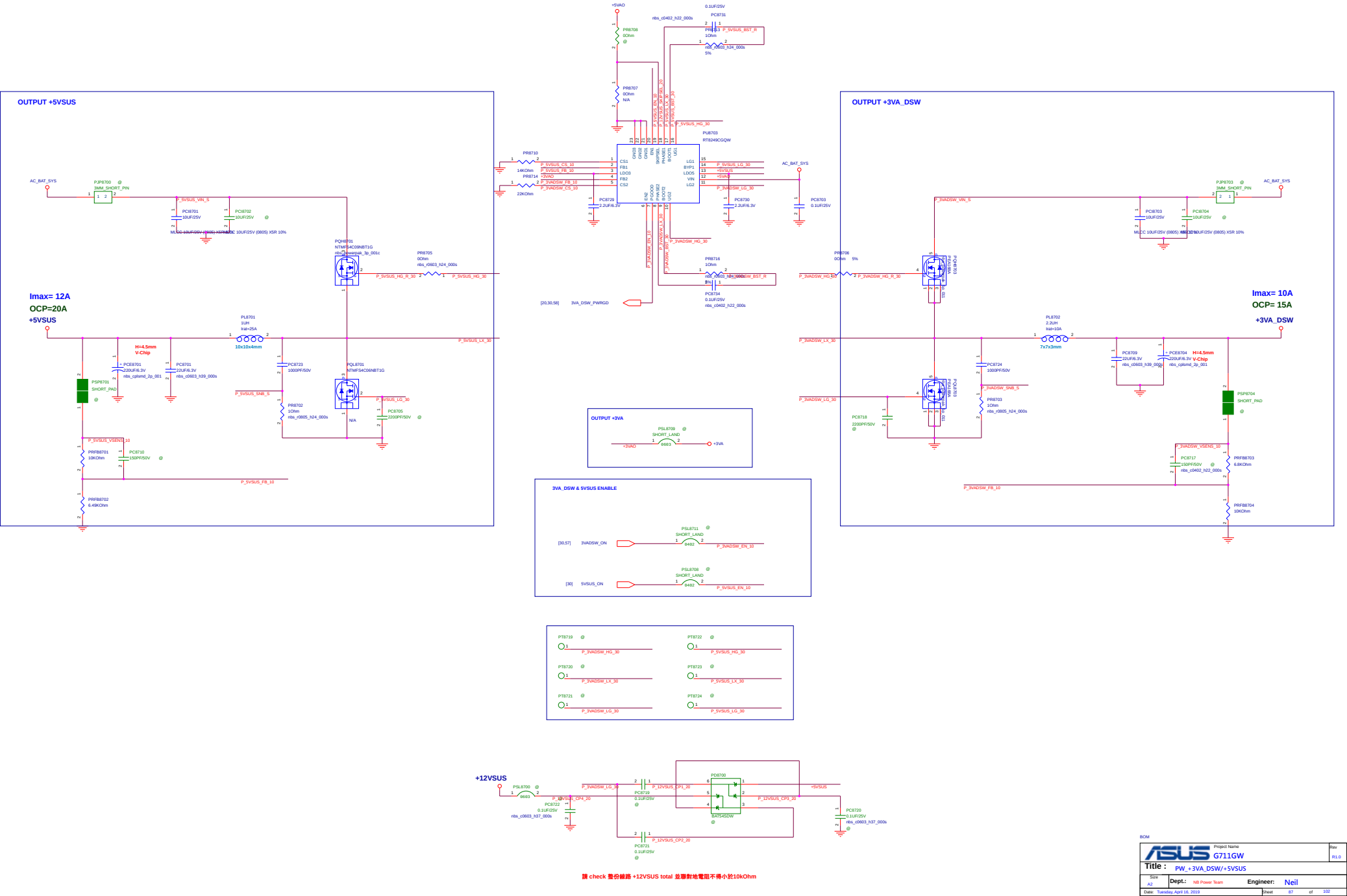
+12VS_FAN [For FAN]

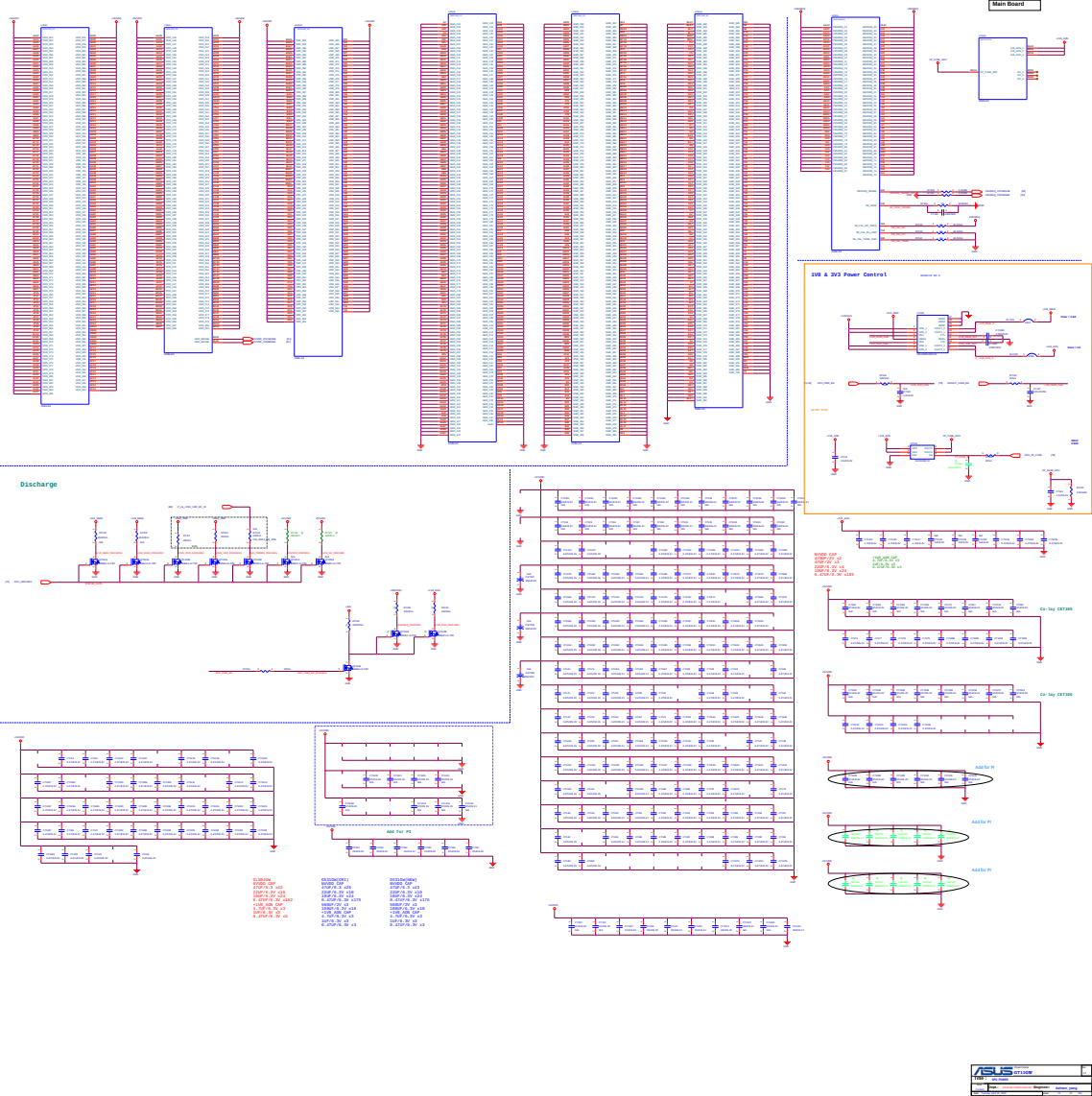


<Variant Name>

ASUS	Project Name: Coffeelake-H	Rev: R1.0
Title : PW_+12VS_FAN		
Size: B	Dept.: NB Power team	Engineer: Hon
Date: Tuesday, April 16, 2019	Sheet 96 of 103	

+3VA_DSW / +5VSUS [System Power]




Main Board
IVB & 3V3 Power Control
Discharge
Add for PI
Co-lay CE738S
Co-lay CE738E
Add for PI
Add for PI
Add for PI

Channel A

Close to DRAM
0.47uF x 36pcs
10uF x 4pcs

Around DRAM
22uF x 6pcs
10uF x 2pcs

Close to DRAM
0.47uF x 4pcs
4.7uF x 1pcs

Close to DRAM
0.47uF x 36pcs
10uF x 4pcs

Around DRAM
22uF x 6pcs
10uF x 2pcs

Channel C Add
22UF/6.3V x3
10UF/6.3V x4
0.47UF/6.3V x49

Close to DRAM
0.47uF x 4pcs
4.7uF x 1pcs

Channel B

Close to DRAM
0.47uF x 36pcs
10uF x 4pcs

Around DRAM
22uF x 6pcs
10uF x 2pcs

Close to DRAM
0.47uF x 4pcs
4.7uF x 1pcs

Close to DRAM
0.47uF x 36pcs
10uF x 4pcs

Around DRAM
22uF x 6pcs
10uF x 2pcs

Channel C Add 0.47UF/6.3V *36

Close to DRAM
0.47uF x 4pcs
4.7uF x 1pcs

Channel C

Close to DRAM
0.47uF x 36pcs
10uF x 4pcs

Around DRAM
22uF x 6pcs
10uF x 2pcs

Close to DRAM
0.47uF x 4pcs
4.7uF x 1pcs

Close to DRAM
0.47uF x 36pcs
10uF x 4pcs

Around DRAM
22uF x 6pcs
10uF x 2pcs

Channel D Add 0.47UF/6.3V *36

Close to DRAM
0.47uF x 4pcs
4.7uF x 1pcs

Channel D

Close to DRAM
0.47uF x 36pcs
10uF x 4pcs

Around DRAM
22uF x 6pcs
10uF x 2pcs

Close to DRAM
0.47uF x 4pcs
4.7uF x 1pcs

Close to DRAM
0.47uF x 36pcs
10uF x 4pcs

Around DRAM
22uF x 6pcs
10uF x 2pcs

Channel D Add 0.47UF/6.3V *18

Close to DRAM
0.47uF x 4pcs
4.7uF x 1pcs

VRAM PWR_FBVDDQ

Partition A under GPU
0.47uF x 12pcs
10uF x 2pcs

Partition B under GPU
0.47uF x 12pcs
10uF x 1pcs

Partition C under GPU
0.47uF x 12pcs
10uF x 1pcs

Partition D under GPU
0.47uF x 12pcs
10uF x 1pcs

Close GPU
10uF x 7pcs
22uF x 9pcs

Close GPU

Near U76001

Add for PI

For power sequence measurement

GODRSX VPP power +1.8V

GL504GW	G531GW(ORI)	G531GW(NEW)	G531GW(NEW ADD)
VRAM PWR	VRAM PWR	VRAM PWR	Channel A
330UF/2V x1	330UF/2V x1	330UF/2V x1	22UF/6.3V x3
22UF/6.3V x6	22UF/6.3V x17	22UF/6.3V x17	10UF/6.3V x4
10UF/6.3V x12	10UF/6.3V x12	10UF/6.3V x12	0.47UF/6.3V x49
0.47UF/6.3V x45	0.47UF/6.3V x48	0.47UF/6.3V x48	Channel B
Channel A	Channel A	Channel A	0.47UF/6.3V x36
22UF/6.3V x15	22UF/6.3V x12	22UF/6.3V x15	Channel C
10UF/6.3V x16	10UF/6.3V x12	10UF/6.3V x16	0.47UF/6.3V x36
4.7UF/6.3V x2	4.7UF/6.3V x2	4.7UF/6.3V x2	Channel D
0.47UF/6.3V x83	0.47UF/6.3V x34	0.47UF/6.3V x83	0.47UF/6.3V x18
Channel B	Channel B	Channel B	
22UF/6.3V x11	22UF/6.3V x12	22UF/6.3V x12	
10UF/6.3V x12	10UF/6.3V x12	10UF/6.3V x12	
4.7UF/6.3V x2	4.7UF/6.3V x2	4.7UF/6.3V x2	
0.47UF/6.3V x80	0.47UF/6.3V x44	0.47UF/6.3V x80	
Channel C	Channel C	Channel C	
22UF/6.3V x10	22UF/6.3V x12	22UF/6.3V x12	
10UF/6.3V x10	10UF/6.3V x12	10UF/6.3V x12	
4.7UF/6.3V x2	4.7UF/6.3V x2	4.7UF/6.3V x2	
0.47UF/6.3V x80	0.47UF/6.3V x44	0.47UF/6.3V x80	
Channel D	Channel D	Channel D	
22UF/6.3V x12	22UF/6.3V x12	22UF/6.3V x12	
10UF/6.3V x10	10UF/6.3V x12	10UF/6.3V x12	
4.7UF/6.3V x2	4.7UF/6.3V x2	4.7UF/6.3V x2	
0.47UF/6.3V x80	0.47UF/6.3V x62	0.47UF/6.3V x80	

ASUS	Project Name: G711GW			Rev: REV_0
Title : VARM				
Issued Date: Tuesday, April 09, 2019	Dept.: MB/PRM COMPUTER	Engineer: Gaming RD	Sheet: 37	of: 103