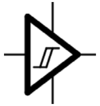
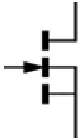
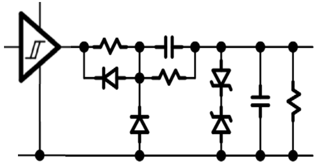
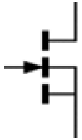
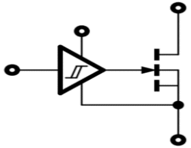
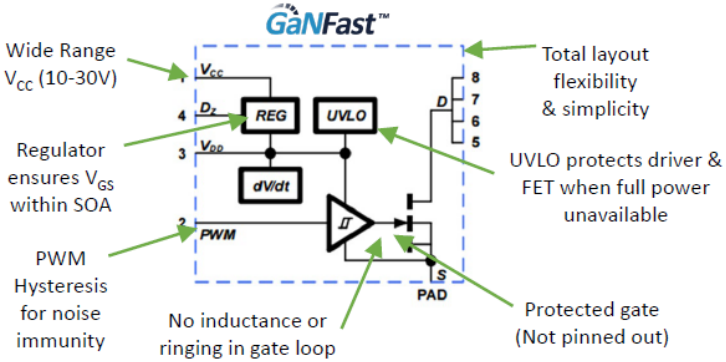
Advancements in GaN Power IC System Integration

Victor Sinow, Sr. Principal Design Engineer
Marco Giandalia, VP IC Design
Navitas Semiconductor
victor.sinow@navitassemi.com , marco.giandalia@navitassemi.com

The Integration Journey

	Driver Drive, control & protection	Parasitics Limit speed & efficiency	Power Device Si or GaN	Speed Switching Frequency	Power Density Faster Charging, Smaller Size	
Silicon Discrete	 *(in system controller)*			**< 100 kHz**		**<0.5 W/cc**
GaN Discrete	 *(complex circuit)*			**< 200 kHz**		**<1 W/cc**
GaNFast™ GaN IC				**Up to 2 MHz** *(3-10x faster)*		**>>1 W/cc**

Navitas Generation 2 - GaNFast



Excellent Reliability!

As of December 31st, 2021

35M+ GaNFast power ICs shipped

116B+ Device Hours In the Field

0 Failures

0 ppm

0.16 FIT Rate

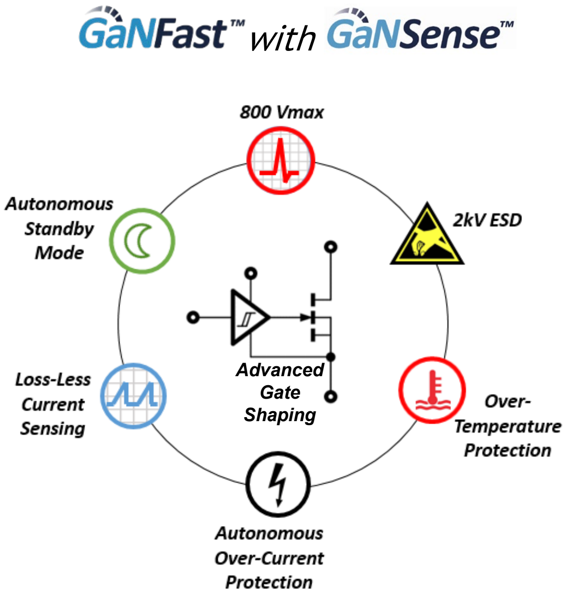
5.8B Equivalent Device Hours Tested

Enables Industry Leading Power Density!

OPPO “Cookie” 50W, 34 cc, 1.5 W/cc

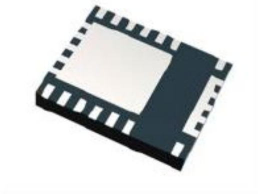
Xiaomi 65W, 53 cc, 1.2 W/cc

Navitas Generation 3 - GaNSense

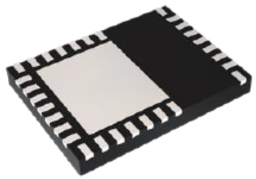


18mΩ ←→ 600mΩ

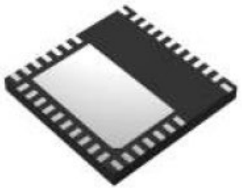
Wide Available R_{dson} and Package Array!



QFN 5 x 6 mm

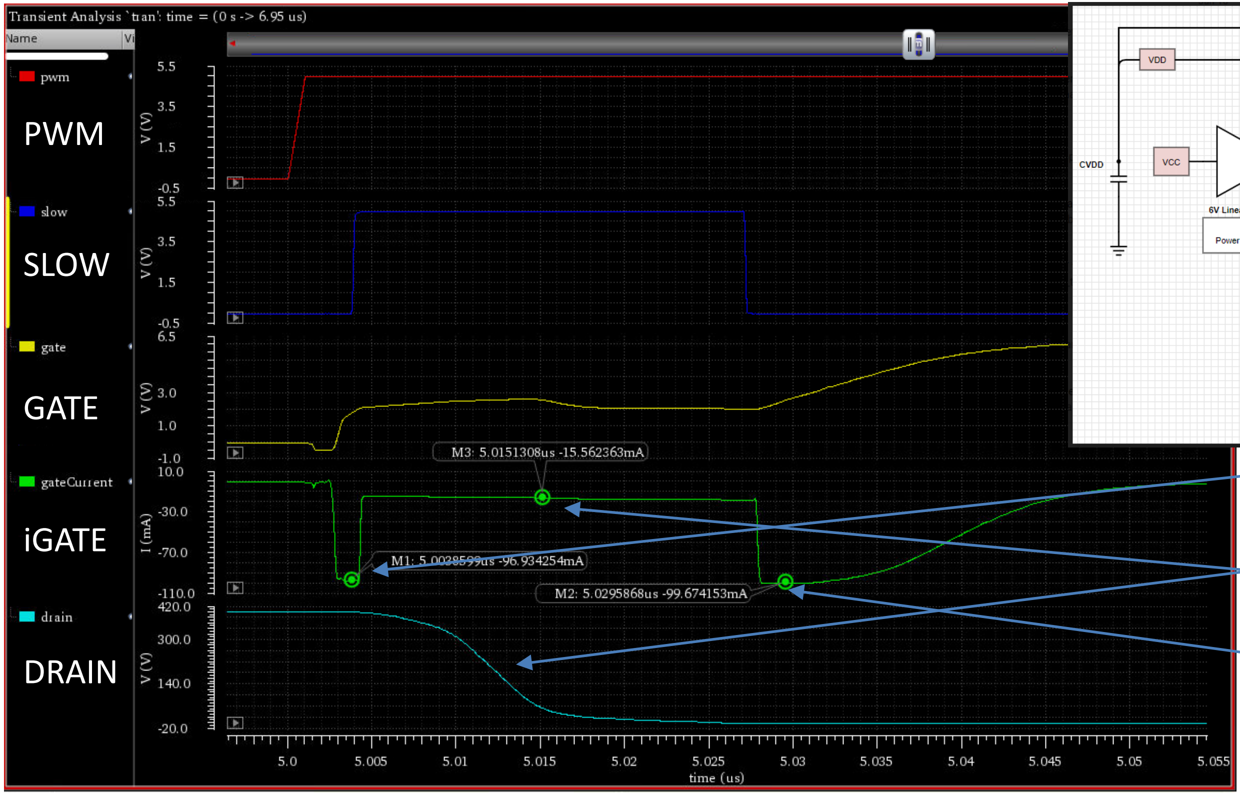


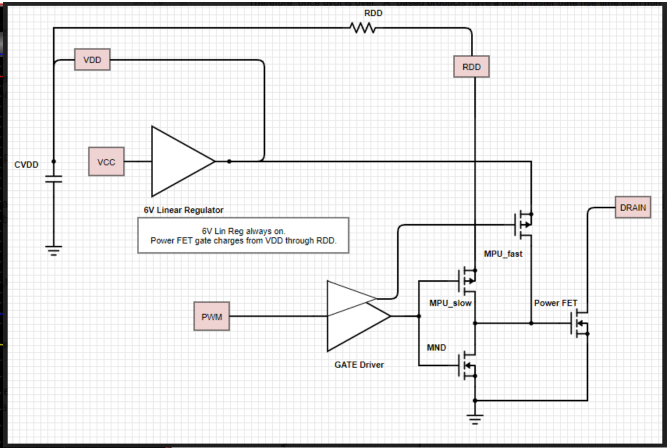
QFN 6 x 8 mm



QFN 8 x 8 mm

Advanced Gate Shaping

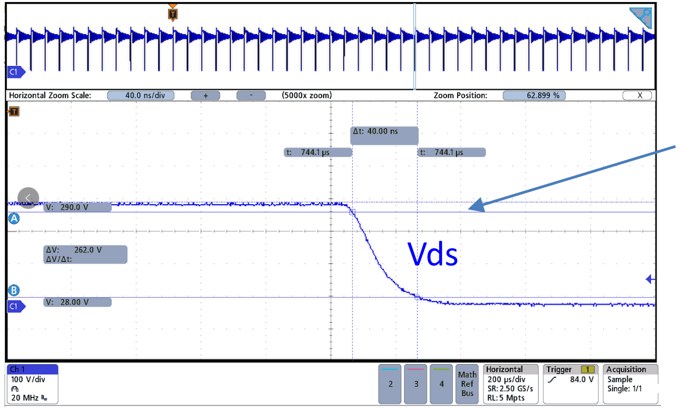




- Full power gate charge current until drain starts to fall.
- Gate current set by external dvdt control resistor while drain falls.
- Full power gate charge current re-activated once drain reaches ~0V.

Advanced Gate Shaping - Effect

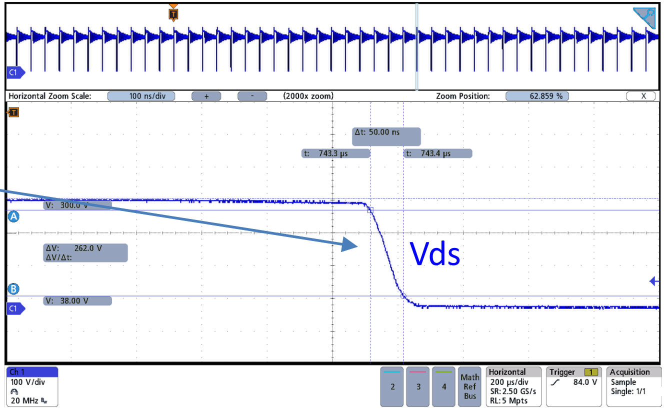
Vo(V)	Vin(Vac)	Io(A)	Efficiency		Gap
			GaNFast	GaNSense	
12V	90V/60Hz	2.75	91.48%	91.68%	0.20%
	115V/60Hz	2.75	92.77%	92.94%	0.17%
	230V/50Hz	2.75	92.86%	93.07%	0.21%
	264V/50Hz	2.75	92.44%	92.62%	0.18%



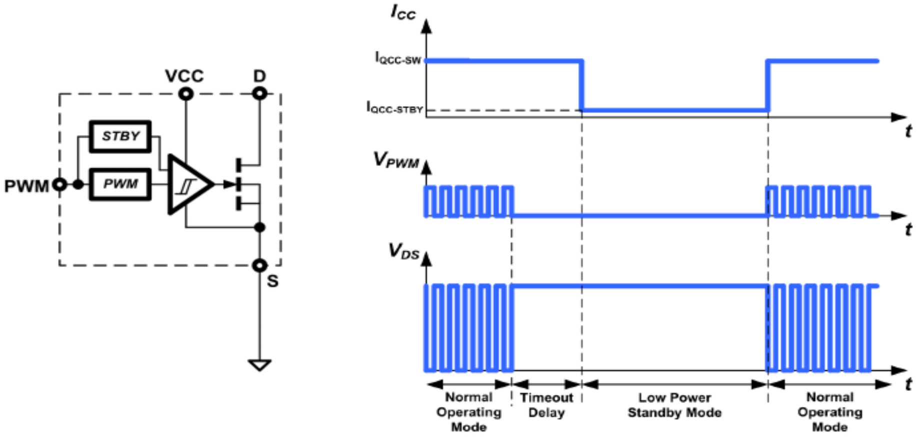
Same 33W HFQR:

GaNFast: **6.55v/ns**
GaNSense: **5.24v/ns**

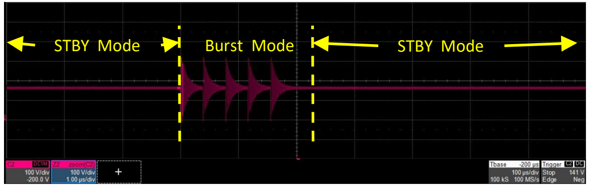
Advanced Gate Shaping yields .2% efficiency improvement for all input line conditions!



Autonomous Standby Mode



Autonomous low-power standby mode simplified circuit and timing diagram



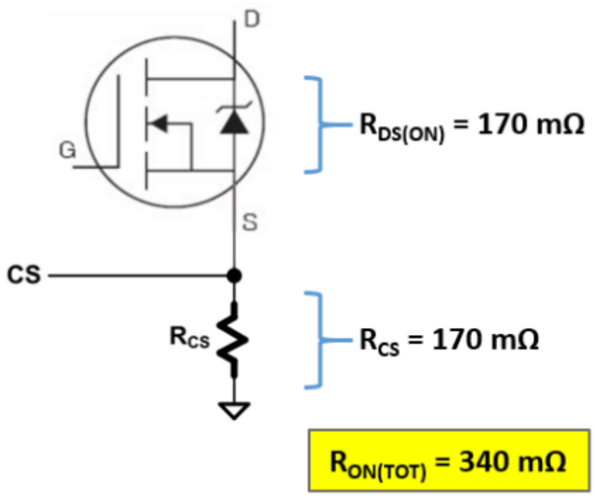
HFQR, no load

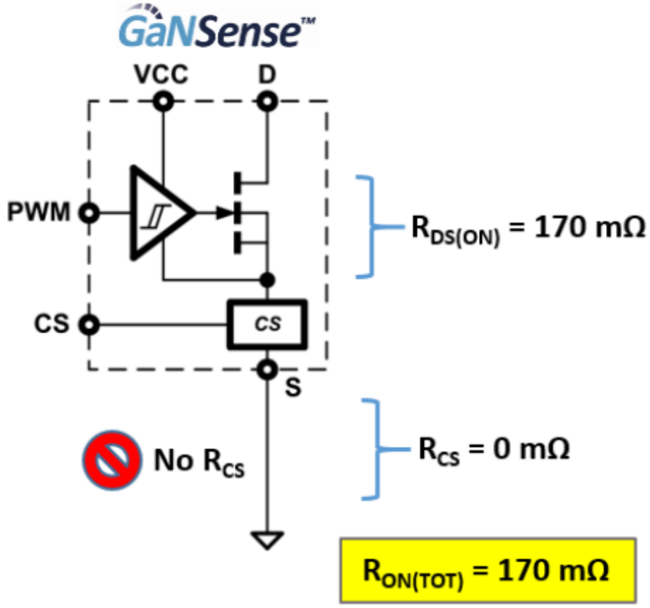
P_{IN} (no load)	115 V_{AC}	230 V_{AC}
NV6125	39 mW	40 mW
NV6136	33 mW	33 mW

- GaN IC autonomously enters standby mode in the absence of PWM signals.
- Super fast wakeup at next PWM rising edge.
  - No discernable effect on propagation delay, current sense performance, etc…
- In the High Frequency QR Flyback no load example above, **full system standby losses are reduced 17%**
  - NV6125 Gen 2 GaNFast part (175mΩ typical).
  - NV6136 Gen 3 GaNSense part (170mΩ typical).

Lossless Current Sensing – What Is It?

External Resistor Sensing Method



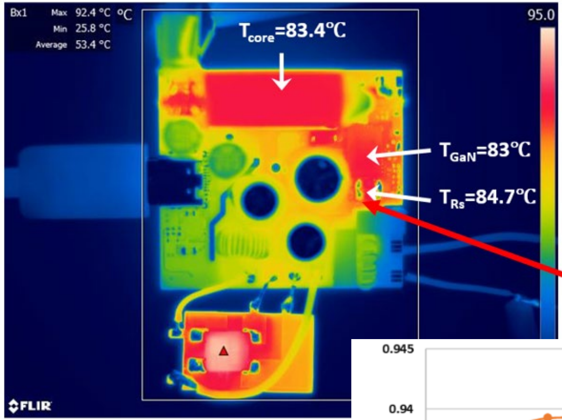


- Reduce $R_{DS(ON)\_TOTAL}$ by 50%
- Efficiency increased +0.5%

- No R_{CS} PCB hotspot (-85°C)
- No R_{CS} PCB footprint (-30 mm²)

Lossless Current Sensing – Does It Work?

GaNFast™



NV6125

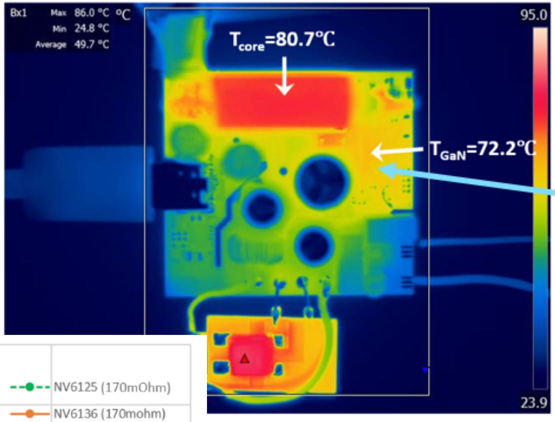
$R_{DS(ON)}$ = 170 mΩ

R_{CS} = 170 mΩ

$R_{ON(TOT)}$ = 340 mΩ

R_{CS} = 85°C

GaNFast™ with GaNSense™



NV6136

$R_{DS(ON)}$ = 170 mΩ

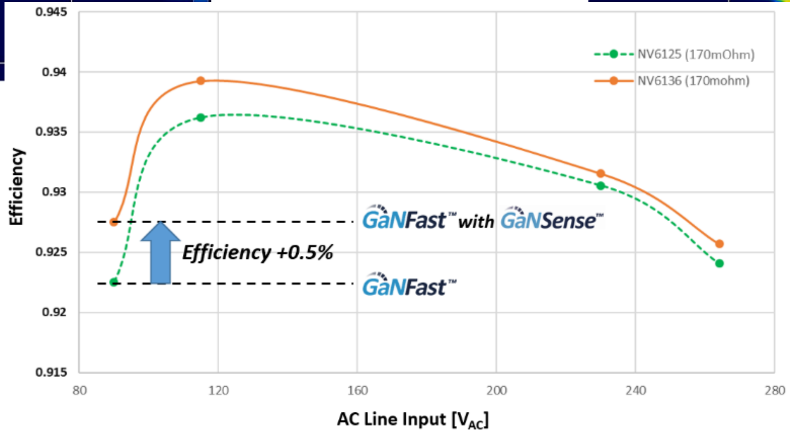
R_{CS} = 0 mΩ

$R_{ON(TOT)}$ = 170 mΩ

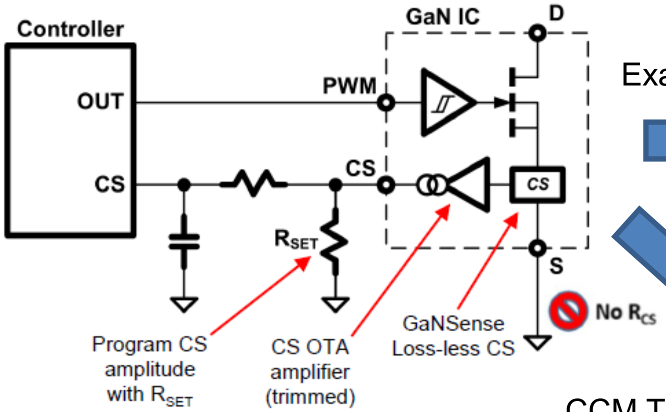
NO R_{CS}

NO HOT-SPOT

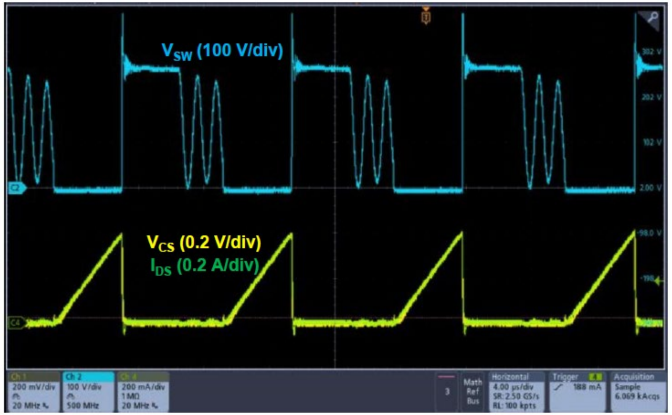
T_{GaN} = -10°C



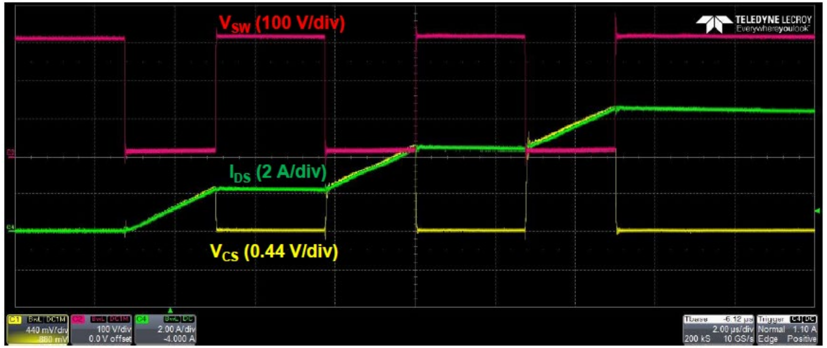
Lossless Current Sensing – Details

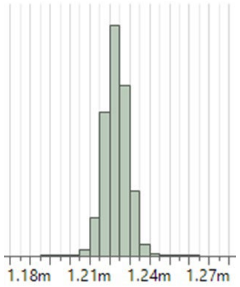


DCM Tracking Example @ 192KHz

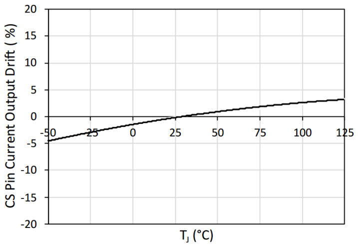


CCM Tracking Example @ 200KHz



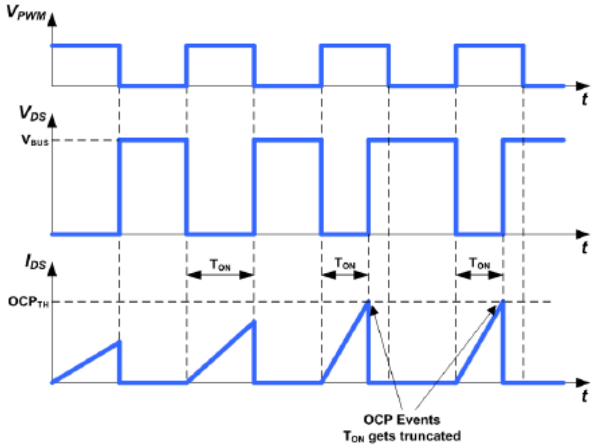


+/- 2% 3σ @ 25C (post trim)

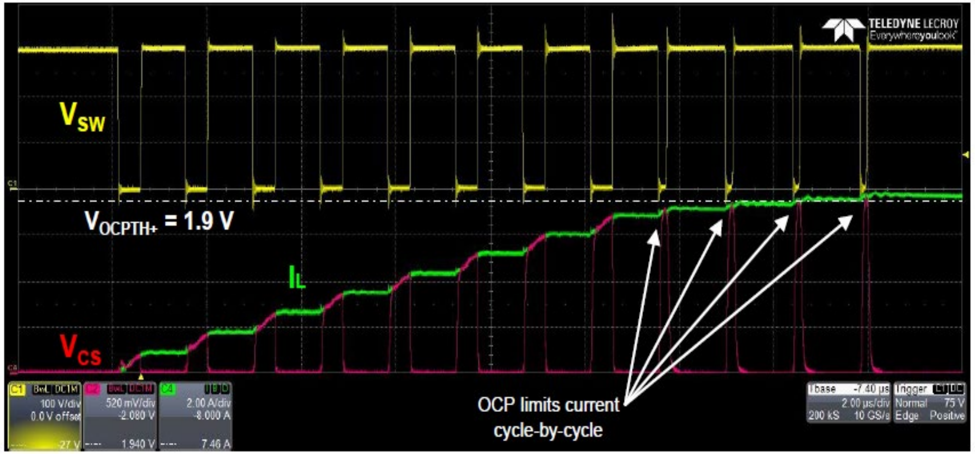


Temp Drift

Autonomous Over Current Protection (OCP)



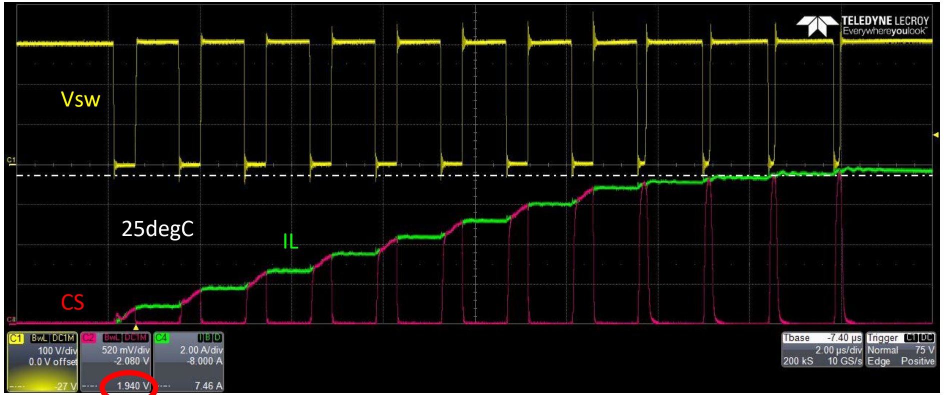
Over Current Protection DCM Timing Diagram

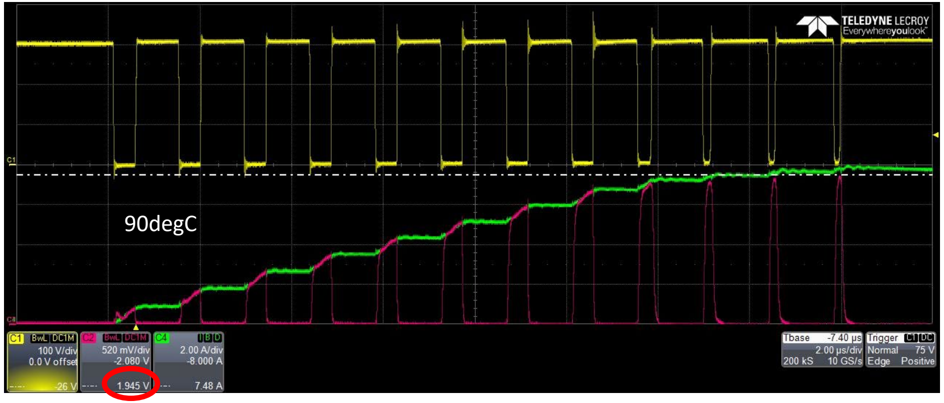


Cycle by cycle over current protection in CCM boost configuration

- On any given cycle, if the CS output voltage exceeds 1.9V, the internal gate driver will turn off the GaN IC and truncate the on-time.
  - **OCP response time 30ns!** Compare to ~200ns response if relying on most conventional controllers.
- The current at which the IC protects is dependent on the I_{DRAIN}→ I_{CS} ratio and the value of R_{SET}.
- Turn-on OCP blanking time prevents noise from triggering the fault and is optimized for GaN FET protection.
- This protection mechanism is designed to be accurate and user programmable via R_{SET}.

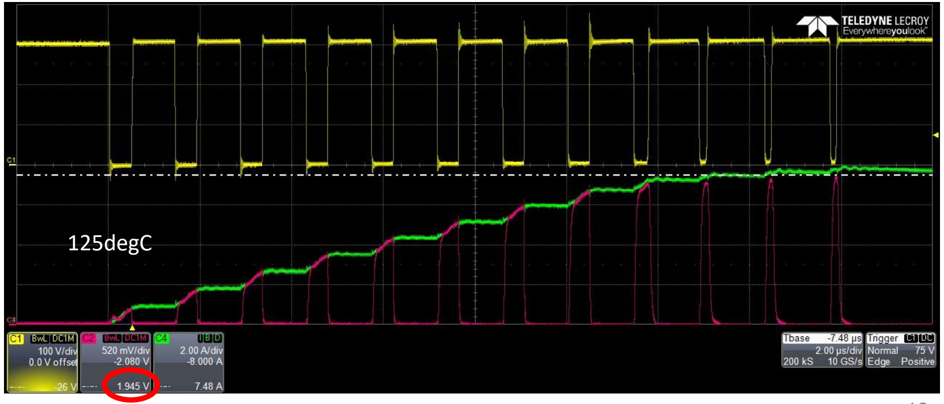
Autonomous OCP Over Temperature



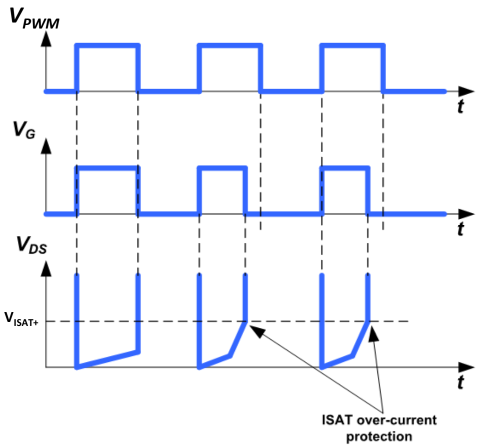


GaNSense 260mΩ in double pulse tester:

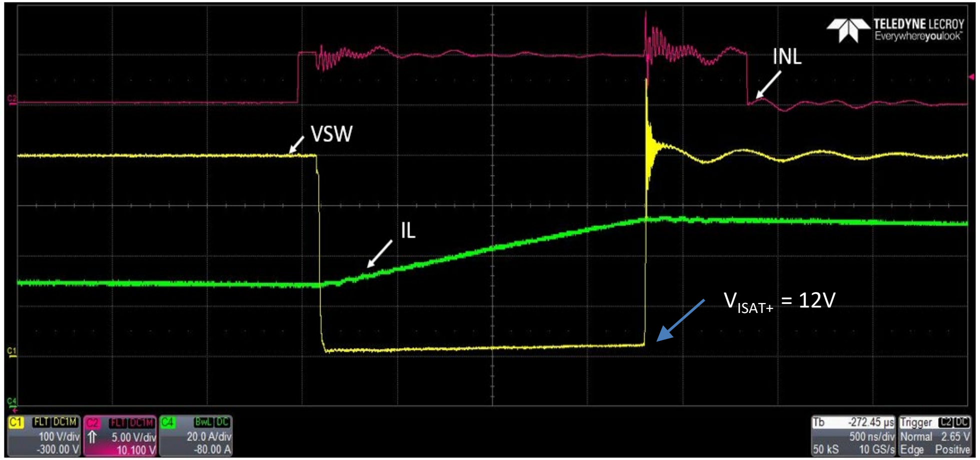
- CS signal matches I_{DS} current, independent of temperature.
- OCP uses CS signal, and the trip point is consistent over temperature.
- OCP is cycle by cycle, and limits inductor current.
- Conduction time when turning on into an OCP condition is equal to the optimized blanking interval.



Saturation Detection for Short Circuit Protection



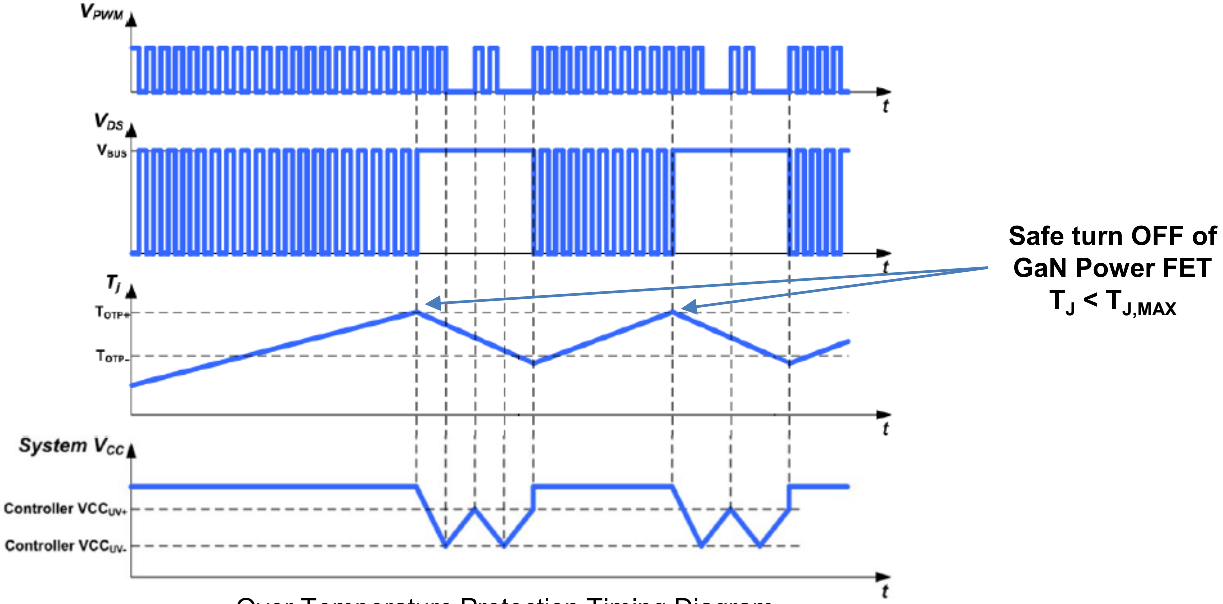
ISAT Protection Timing Diagram



ISAT protection example @ 78A

- On any given cycle, if V_{DS} of the GaN FET exceeds V_{ISAT+}, the internal gate driver will turn off the GaN IC and truncate the on-time.
- Turn-on ISAT blanking time prevents noise from triggering the fault and is optimized for GaN FET protection.
- This protection mechanism is designed for ***catastrophic events*** such as input to drain shorts, half bridge shoot through failure, saturated power inductance, etc…

Over Temperature Protection (OTP)



Over Temperature Protection Timing Diagram

- Should T_J exceed the internal T_{OTP+} threshold (165 ℃, typical) then the IC will latch off safely.
- When T_J decreases again and falls below the internal T_{OTP-} threshold (105 ℃, typical), the OTP latch will be reset.

GaNSense In Mass Production (1)

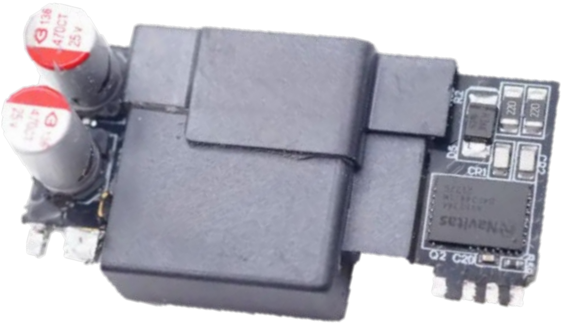
Lenovo YOGA

Charger Power, Output(s)	65W 2CA	65W 2C		
				
Powertrain	Discrete GaN	NV6134 GaNFast with GaNSense		
Size (cc)	105	75	30%	Smaller
Power Density (W/cc)	0.6	0.9	50%	Higher
Efficiency (%) [(1)]	89.15%	92.50%	3.4%	Higher
Loss (W)	7.1	4.9	30%	Energy Savings
Drive, Protection Components	19	5	75%	Fewer
PCB Area (mm^2)	83	15	80%	Smaller
T_{CASE} max (°C) [(1)]	85°C	<77°C	8°C	Cooler

GaNSense In Mass Production (2)

- DCM boost PFC:
  - Silergy SY5072B
  - NV6134 GaNFast with GaNSense
- HFQR DC-DC
  - Onsemi NCP1342
  - NV6134 GaNFast with GaNSense
  - Planar transformer (shown)

Power density = 1.4W/cc



Presenter Bios

- Victor Sinow is a Senior Principal Engineer at Navitas Semiconductor and serves as the Lead Power IC Architect for the company. Victor has been in the power semiconductor / systems space for more than 12 years and holds both a BS EE and an MS EE from MIT.
- Victor's previous experience includes (1) designing and bringing to market the Dart 65W power adapter in his roles first as a Principal Engineer and then as the Director of the Power Engineering group at FINsix Inc; (2) designing various control ICs for offline power converters while working as an IC design engineer in the Power Supply Control group at Texas Instruments.
- Victor has been granted patents for innovations in circuit topologies, power system solutions, and semiconductor devices.

- Marco Giandalia serves as Vice President IC Design for Navitas Semiconductor and has 25 years experience in the field of Power IC products and technology development in Si and GaN since he received is MSEE in 1996.
- Before joining Navitas, Marco led the Energy Saving Product - Design Center at International Rectifier developing innovative products for Off-Line application like motor drive, AC/DC, DC/DC converters. Earlier he was in charge as IC Design Engineer at STMicroelectronics for Smart Power IC product line.
- He has been granted several patents for Power IC design solutions and has been author of multiple papers and conferences presentations.