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Battery Charger Based on a Resonant Converter for High-Power LiFePO₄ Batteries

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Abstract: A new battery charger, based on a multiphase resonant converter, for a high-capacity 48 V LiFePO₄ lithium-ion battery is presented. LiFePO₄ batteries are among the most widely used today and offer high energy efficiency, high safety performance, very good temperature behavior, and a long cycle life. An accurate control of the charging current is necessary to preserve the battery health. The design of the charger is presented in a tight correlation with a battery model based on experimental data obtained at the laboratory. With the aim of reducing conduction losses, the general analysis of the inverter stage obtained from the parallel connection of N class D LC_pC_s resonant inverters is carried out. The study provides criteria for proper selection of the transistors and diodes as well as the value of the DC-link voltage. The effect of the leakage inductance of the transformer on the resonant circuit is also evaluated, and a design solution to cancel it is proposed. The output stage is based on a multi-winding current-doubler rectifier. The converter is designed to operate in open-loop operation as an input voltage-dependent current source, but in closed-loop operation, it behaves as a voltage source with an inherent maximum output current limitation, which provides high reliability throughout the whole charging process. The curve of efficiency of the proposed charger exhibits a wide flat zone that includes light load conditions.

Keywords: lithium-ion battery; battery modeling; battery chargers; power supplies; resonant inverters; phase control



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1. Introduction

Lithium iron phosphate (LiFePO₄) batteries have a great electrochemical performance and a good thermal stability, which makes them safer and more robust. This lithium-based technology exhibits a very low internal resistance offering a high current rating. Their cycle life is significantly longer compared to other technologies [1,2]. The applications of LiFePO₄ batteries are, among others, for storage systems in renewable energy facilities, powering electric vehicles and uninterruptible power supplies (UPS) in data centers, telecommunications, and hospitals. A battery model is an important tool for designing the charger allowing the study of the dynamic response of the battery-charger system along the whole charging process, wherein the converter load, i.e., the equivalent resistance of the battery, varies from almost short-circuit to open-circuit values. Most of the battery models are aimed to improve the battery management system (BMS) performance, providing information about important parameters of the battery such as the state of charge (SOC) [3]. The estimation of the battery SOC and power capacity is usually solved by applying three methods, i.e., the look-up table method, the model-based method, and the artificial intelligence method [4–7]. In addition to that, the BMS is responsible for ensuring the battery operation within safety margins of temperature and sets the overvoltage and

under voltage protection limits. In this work, the battery modeling is presented in a tight correlation with the battery charger design.

The technology of resonant converters is chosen to implement the proposed battery charger. The advantages of the resonant conversion of energy, such as high frequency of operation, sinusoidal waveforms, and low switching losses are well known [8]. Among all possible configurations of resonant converters, the series resonant converter and the *LLC* converter have been widely used [9–12]. Usually, the converter is designed to operate as a voltage source with some kind of control to limit the charging current. In this work, the converter is designed as a voltage-dependent current source. In this approach, the circuit presents an inherent maximum current limitation, which is a safer operation mode. The LiFePO_4 technology reaches current rates as high as hundreds of amps. In circuit design for high-current applications, conduction losses are a major design limitation [13,14]. In high-current resonant converters, increasing the dc-link voltage, V_{dc} , and using a step-down transformer ($n > 1$) reduces the amplitude of the resonant currents in the inverter stage, minimizing the conduction loss in transistors and resonant inductors. New Wide Band Gap (WBG) devices enable the operation at an 800 V to 1700 V dc-link voltages range [15]. WBG devices achieve high performance at high current levels with important simplifications in the power circuit. However, the cost of WBG devices limits their use for certain applications.

In this work, a generalized design method aimed at minimizing the conduction loss is presented for multiphase resonant converters [16]. The number of parallel branches and therefore phases, N , in the inverter stage is calculated according to the maximum output power and the expected efficiency. This alternative offers another degree of freedom for achieving efficiencies higher than 90% even at relatively low values of V_{dc} and using low-cost transistors. Moreover, the multi-phase structure makes it possible to regulate the charging current at constant switching frequency by shifting the phase of the output voltages of each class D section of the inverter.

This paper is organized as follows: After the introduction, Section 2 describes the charging profile of the target LiFePO_4 battery, which is oriented to obtain a fast charge without reducing its lifetime. The battery model is presented in Section 3. The analysis of the proposed charger and main design equations are developed in Section 4. The efficiency of the charger is studied in Section 5. A detailed step-by-step design sequence of the proposed charger is explained in Section 6. In Sections 7 and 8, the results obtained for the modeling of the battery and experimental waveforms to verify the performance of the prototype are presented, ending with a discussion about Si vs. SiC solutions and concluding remarks.

2. Charging Method

The main characteristics of the commercial 48NPFC50 LiFePO_4 battery (Narada Power Source Co., Ltd., Hangzhou, China) [17] used in this work are 48 V nominal voltage and 50 Ah nominal capacity (C_n) i.e., 2.4 kWh of power capacity. The battery consists of fifteen ($N_s = 15$) stacked cells in series and incorporates a BMS that guarantees the right balance-of-charge of all cells. Thus, the voltage across each cell is assumed identical to any other. The battery charger is designed to meet all operational limits settled by the BMS.

The charging protocol recommended for LiFePO_4 batteries is the well-known [18] constant current (CC)–constant voltage (CV) method (i.e., CC–CV). During the CC stage, the battery is charged at the maximum current rate, which depends on the battery capacity and technology. Once the battery voltage reaches its maximum charging voltage specified in the battery data sheet, the CV stage begins. At this point, the power drawn from the charger is the maximum, which happens at 90% of the SOC approximately. During the CV stage, the charging current diminishes. Three experimental charging profiles are carried on at the battery laboratory facility shown in Figure 1. They are evaluated at room temperature (25 °C) using the battery test equipment PEC SBT-10050 (PEC, Leuven, Belgium) and taking into account that the battery is fully discharged as the initial condition.



Figure 1. (Left) Laboratory facility for battery testing. (Right) Battery connected to SBT-10050 test equipment.

Those profiles correspond to the battery charge at current rates equal to $C_n/5$, $C_n/2$, and C_n during the CC stage. The results are shown in Figure 2.

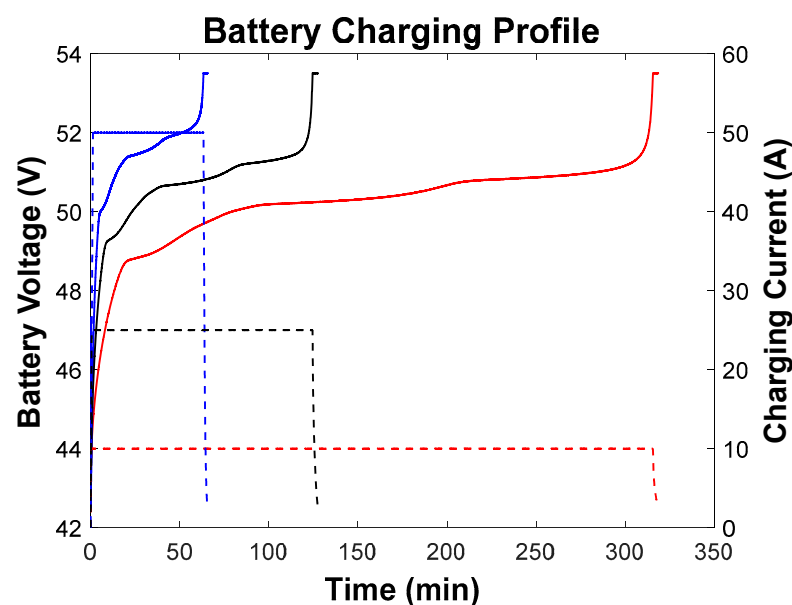


Figure 2. Experimental charging profiles at 10, 25, and 50 A for a 48NPFC50 LiFePO₄ battery.

The temperature is observed by the BMS during the whole charging process, and it implements the corresponding protection (maximum value 55 °C for charging) to prevent the battery aging. Electro-thermal models for studying the temperature of a lithium-ion cell as a function of the charging/discharging current have been reported in [19,20]. The user manual recommends a conservative value, $C_n/5$, for the charging current rate; however, LiFePO₄ technology tolerates fast-charging protocols [21–24]. In this work, in order to shorten the charging time, a maximum charging current rate of 20 A (approximately $C_n/2$) is chosen the charger design. According to the experimental characterization of the battery, charging at $C_n/2$ keeps the temperature of the battery well below 55 °C.

3. Battery Model

Although the LiFePO₄ cell is a complex physical system with several variables involved, a good trade-off among simplicity, accuracy, and insight information is obtained with the electrical parameters-based models [25], as shown in Figure 3. The single cell

model is generalized by affecting all parameters by the total number of cells, N_s , under the assumption that all cells are identical, as shown in Figure 3.

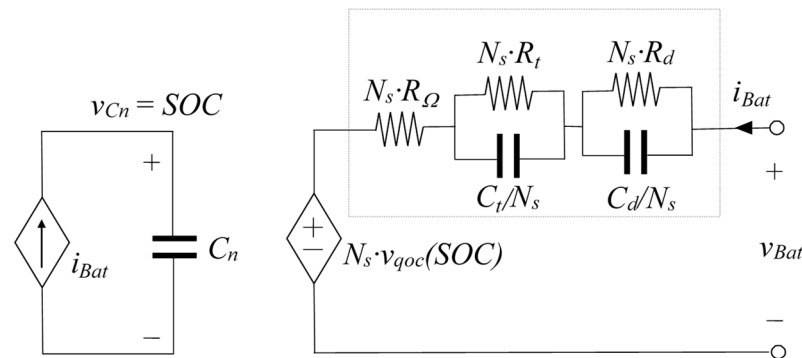


Figure 3. Battery model considering N_s stacked cells in series.

The state of charge (SOC) [26] of the battery is defined as the ratio of the battery charge, Q , to the nominal capacity, C_n .

$$SOC = \frac{Q}{C_n} \cdot 100\% \tag{1}$$

The model calculates the SOC [26], integrating the battery current-dependent current source, i_{bat} , which charges/discharges the capacitor C_n . The SOC is equal to the voltage across the capacitor C_n , v_{Cn} varying from zero to one corresponding to exhausted to fully charged battery, respectively.

$$SOC(t) = SOC(t_0) + \frac{1}{C_n} \int_{t_0}^t i_{bat}(t) dt \tag{2}$$

The voltage-controlled voltage source, $N_s v_{qoc}(SOC)$, dependent on the voltage v_{Cn} , represents the quasi-open-circuit battery voltage, where v_{qoc} , is the quasi-open-circuit voltage across one single cell. The experimental measurement of v_{qoc} as a function of the SOC is a time-consuming task because it should be obtained while keeping the cell in electrochemical equilibrium [27], charging and discharging the cell at a very low current rate. From the experimental study of one single cell, the v_{qoc} as a function of the SOC was obtained by charging and discharging the cell at $C_n/50$. This test required 100 h. The result is shown in Figure 4.

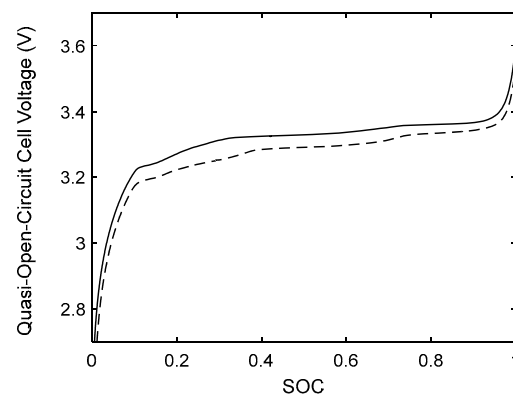


Figure 4. Quasi-open-circuit voltage of the cell as a function of the state of charge (SOC) obtained at $C_n/50$ for a complete charge/discharge cycle. Solid line: Charge trajectory. Dashed line: Discharge trajectory.

As it is observed in Figure 4, the quasi-open-circuit cell voltage, v_{qoc} , incorporates the effect of the voltage hysteresis caused by the battery structure [27]. The maximum hysteresis is about ≈ 40 mV within the 30% SOC region, and the average is ≈ 20 mV within the 40% to 80% SOC region. The experimental test results show a cell capacity $C_n = 50$ Ah, which is represented in the model by a capacitance $C_n = 180,000$ F.

The electrolyte and electrode resistance are modeled by R_Ω . In addition to that, the model also includes two time constants, which are modeled by networks $R_t C_t$ and $R_d C_d$. The time constant $R_t C_t$ is associated to chemical reactions and charge transportation phenomenon in the electrodes. This time constant is within the range from milliseconds to a few seconds. In contrast, the time constant $R_d C_d$ governs the mass diffusion in the electrolyte and electrodes and is within the tens of seconds range [27]. From the point of view of the battery charger design, the electrical parameters of the battery at the end of the CC stage are of interest. At this point, the power supplied by the charger is the maximum. For a given SOC, the battery model can be simplified to a resistance, r_{Bat} , in series with a voltage source equal to the quasi-open-circuit voltage $N_s V_{qoc}$. Assuming the battery is in steady state, r_{bat} is obtained from the model shown in Figure 3 as

$$r_{Bat} = N_s \cdot (R_\Omega + R_t + R_d). \tag{3}$$

The specific values R_t and R_d for a given SOC should be obtained from the dynamic study of the battery, once the time constants associated with transport and diffusion phenomena were obtained. Finally, the battery voltage is obtained as:

$$V_{Bat} = N_s V_{qoc} + I_{Bat} r_{Bat}. \tag{4}$$

4. Multiphase $LC_p C_s$ Resonant Converter

The proposed battery charger is a multiphase resonant converter. The general form of the circuit is shown in Figure 5, where the battery is modeled in steady state by its internal impedance, r_{Bat} , in series with the quasi-open-circuit battery voltage $N_s V_{qoc}$.

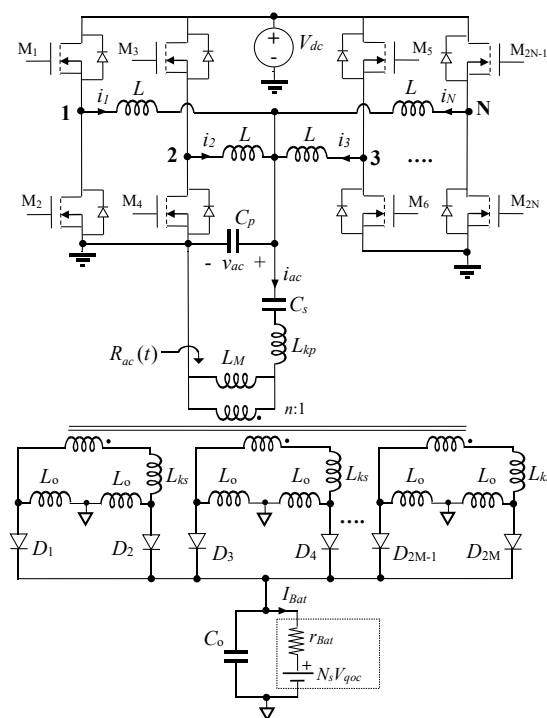


Figure 5. General architecture of the battery charger based on an N -phase $LC_p C_s$ resonant inverter with an M -winding current-doubler rectifier as output stage. Multiple configurations are possible according to the N and M values.

The AC side is a multiphase resonant inverter, which consists of N paralleled LC_pC_s class D sections [16,28]. Among the possible configurations of the resonant network, the configuration LC_pC_s of the LCC family is chosen to achieve a current source behavior while preserving the zero voltage switching (ZVS) mode of transistors [8,29]. Unlike the LLC converter, the proposed LC_pC_s does not require a gapped-core transformer [30], so the magnetizing inductance, L_M , is high enough to neglect its impact in the later analysis.

The DC side consists of an M -winding current multiplier, which is derived from the parallel connection of an M current-doubler rectifier [31,32]. The low output voltage of this application recommends the use of Schottky diodes without any control circuit in the secondary side, which is a simplification in comparison to solutions based on synchronous rectification (SR).

4.1. Resonant Inverter Stage

The converter is analyzed considering the general case, where each midpoint voltage v_i of all class D sections has associated a phase-angle $\Psi_0, \Psi_1, \dots, \Psi_{i-1}$. To illustrate this assumption, the midpoint voltages, v_i , are shown in Figure 6.

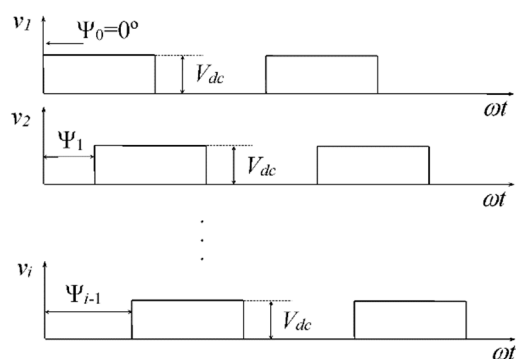


Figure 6. Output voltages of each inverter section obtained in the midpoint of the transistors leg.

Using the fundamental approximation, the input voltages, v_i , are represented with the exponential form given in (5),

$$V_i = \frac{2V_{dc}}{\pi} \cdot e^{-j\Psi_{i-1}}, \tag{5}$$

where $i \in [1, 2, \dots, N]$ is the phase number. In steady state and using the low ripple approximation, the M -winding output rectifier is reduced to an equivalent impedance R_{ac} [8,29]. The resonant inverter stage is analyzed using the simplified circuit model shown in Figure 7.

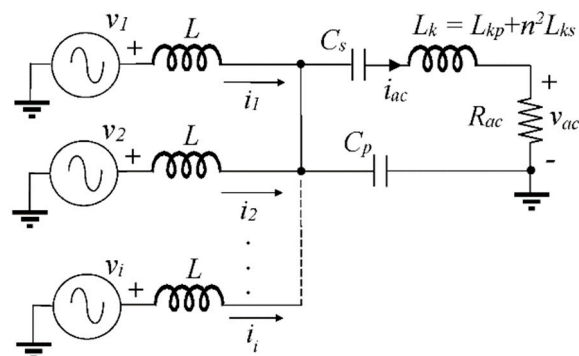


Figure 7. Simplified model using the fundamental approximation for circuit analysis purposes of the inverter stage.

The parallel parameters of the resonant inverter are defined in Table 1.

Table 1. Parameters of the LC_pC_s resonant inverter.

Parallel Resonant Frequency	Parallel Characteristic Impedance	Parallel Quality Factor
$\omega_p = \frac{1}{\sqrt{LC_p/N}}$	$Z_p = \omega_p L = \frac{N}{\omega_p C_p}$	$Q_p = \frac{NR_{ac}}{Z_p}$

4.1.1. AC Side Output Current

During the CC stage of the charging process, the converter provides an inherent current limitation, protecting the battery and extending its life. The current source behavior of the resonant converter is achieved by fixing the switching frequency at $\omega = \omega_p$, where ω_p is the parallel resonant frequency, as given in Table 1. Once the switching frequency is fixed at $\omega = \omega_p$, the output current, seen from the primary side of the transformer, i.e., through C_s , I_{ac} , is calculated by (6).

$$I_{ac} = -\frac{2V_{dc}}{\pi Z_p} \left\{ \sum_{m=1}^N \sin \Psi_{m-1} + j \sum_{m=1}^N \cos \Psi_{m-1} \right\} \tag{6}$$

From (6), the current source behavior is verified, given that I_{ac} has no dependence on the load.

4.1.2. Switching Mode

The switching losses are minimized by ensuring the zero voltage switch (ZVS) on the primary side of the converter [8,29]. The ZVS mode requires sufficient phase-delay of the resonant current with respect to the input voltage. A high value of Q_p reduces the reactive energy in the resonant converter, which is beneficial from the point of view of reducing the conduction loss. However, some reactive energy must be accepted for ensuring the ZVS mode of all transistors. The complex form, I_i , of each resonant current is given in (7) as a function of the angles $\Psi_0, \Psi_1, \dots, \Psi_{N-1}$.

$$I_i = \frac{2V_{dc}}{\pi Z_p} \times \left\{ \begin{array}{l} \frac{Q_p}{N} \sum_{m=1}^N \cos \Psi_{m-1} - \left(\frac{C_p}{NC_s} - \frac{L_k}{L} \right) \sum_{m=1}^N \sin \Psi_{m-1} - \sin \Psi_{i-1} \\ -j \left[\frac{Q_p}{N} \sum_{m=1}^N \sin \Psi_{m-1} + \left(\frac{C_p}{NC_s} - \frac{L_k}{L} \right) \sum_{m=1}^N \cos \Psi_{m-1} + \cos \Psi_{i-1} \right] \end{array} \right\} \tag{7}$$

In order to determine the power factor angle, ϕ_i , of each transistor’s leg, the input impedance $Z_i = V_i/I_i$, of each phase is calculated. The power factor angle, ϕ_i is obtained using $\phi_i = \text{angle}(Z_i)$ as a function of the control angles, $\Psi_0, \Psi_1, \dots, \Psi_{N-1}$, the number of phases, N , and the quality factor, Q_p . Upon substitution of $\Psi_0 = \Psi_1 = \dots = \Psi_{N-1} = 0^\circ$ in (5) and (7), ϕ_i at the maximum output current is obtained:

$$\phi_i = \arctan \left(\frac{1 + \frac{C_p}{C_s} - N \frac{L_k}{L}}{Q_p} \right). \tag{8}$$

From (8), it can be observed that the effect of leakage inductance referred to the primary side of the transformer, L_k , is more significant for high-power as well as for high-frequency designs, where the value of inductance of the resonant circuit, L , is usually low, and a high value of leakage inductance could produce the loss of the ZVS mode. However, the series disposition of L_k and C_s enables the cancelation of the L_k effect on the AC side by calculating C_s to achieve, at the switching frequency, the series resonance with L_k . According to this proposal, C_s is obtained from (9).

$$C_s = \frac{L}{NL_k} C_p \tag{9}$$

With the cancellation of the L_k effect, the value of the power factor angle, ϕ_i , depends essentially on the value of the quality factor Q_p , which is set during the design process of the converter. The minimum value of power factor angle for achieving ZVS, ϕ_{zvs} , depends on the dead time, t_d , of the transistors' driver and the switching frequency ω_p [33].

$$\phi_{zvs} = \frac{t_d \omega_p}{2\pi} \cdot 360^\circ \quad (10)$$

As design criteria, a value of power factor angle $\phi_i = 2\phi_{zvs}$ is assumed at nominal conditions for achieving a reliable operation of the converter. This is the most restrictive design condition for operating in ZVS mode for the whole range of variation of the control angle Ψ . From (8) to (10), the value of the quality factor at nominal conditions, Q_{pN} , is obtained:

$$Q_{pN} = \frac{1}{\tan 2\phi_{zvs}} \quad (11)$$

4.1.3. Variation of the Quality Factor and Transformer Turns Ratio

During the charging process, the equivalent impedance of the battery, R_{Bat} , changes depending on V_{Bat} and I_{Bat} , whose relationship is given by the charging profile of the battery, as shown in Figure 1. At the end of the CC stage, $V_{Bat} = V_{Bat(Max)}$ and the power supplied to the battery reaches the maximum, $P_{Bat} = V_{Bat(Max)} I_{Bat(Max)}$. The specifications of the point of maximum output power are used for defining the nominal value of the quality factor, Q_{pN} . Thus, during the CC stage of the charging profile, the converter works with a quality factor lower than the nominal one, which strengthens the inductive behavior of the resonant tank, assuring the ZVS mode.

During the CV stage, the reduction of the charging current leads to a significant increment in the equivalent resistance R_{Bat} and consequently, the reflected impedance on the AC side, R_{ac} , and the quality factor Q_p also increase. Assuming that $V_{Bat(Max)}$ is constant and working with (6), the quality factor as a function of Ψ is obtained in (12),

$$Q_p = \frac{n\pi^2 V_{Bat(Max)}}{2V_{dc}} \frac{N}{\sqrt{\left(\sum_{m=1}^N \sin \Psi_{m-1}\right)^2 + \left(\sum_{m=1}^N \cos \Psi_{m-1}\right)^2}} \quad (12)$$

The increment of Q_p , as a consequence of the reduction of the charging current during the CV stage could put at risk the ZVS mode of the transistors of the converter. However, it is beneficial from the point of view of achieving waveforms with low distortion and increases the converter efficiency. The nominal value of quality factor is obtained by evaluating (12) for $\Psi_0 = \Psi_1 = \Psi_{N-1} = 0^\circ$.

$$Q_{pN} = \frac{n\pi^2 V_{Bat(Max)}}{2V_{dc}} \quad (13)$$

From (13) and (11), the transformer's turns ratio ($n:1$) can be obtained:

$$n = \frac{2V_{dc}}{\pi^2 V_{Bat(Max)} \tan 2\phi_{zvs}} \quad (14)$$

4.2. Output Current Multiplier

In order to analyze the output current multiplier stage, first, a single-winding current-doubler rectifier with an ideal transformer, as seen in Figure 8, is considered. The quasi-sinusoidal voltage v_{ac} at parallel capacitor C_p drives the current multiplier stage. The diodes D_1 and D_2 turn on alternatively according the positive or negative cycle of v_{ac} , respectively.

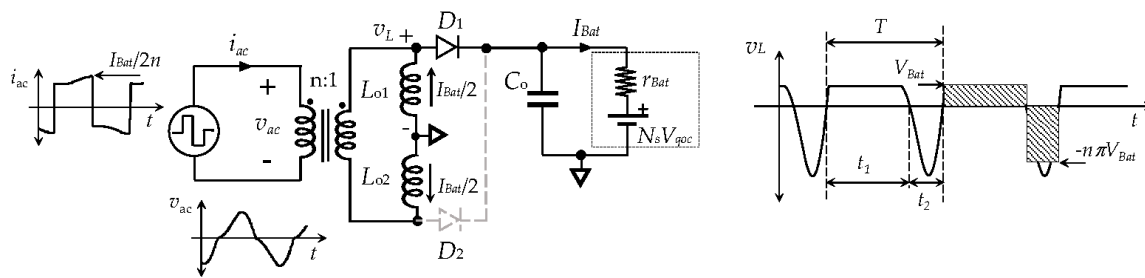


Figure 8. (Left) Current-doubler rectifier considering the positive semi-cycle of the drive voltage v_{ac} . (Right) Theoretical voltage waveform at the filter inductors.

The diodes conduction time, t_1 , is obtained from the volts–seconds balance across the inductors. The areas are calculated according to the approximation shown in Figure 8 right.

$$t_1 = \frac{n\pi}{1 + n\pi} T \tag{15}$$

The average current through each inductor, $L_{o1,2}$, is equal to one-half of the charging current I_{Bat} . The amplitude of the current ripple in each inductor is determined by

$$\Delta i_L = \frac{n\pi^2 V_{Bat(Max)}}{(1 + n\pi)\omega_p L_o} \tag{16}$$

The total ripple current through the filter capacitor C_o is calculated considering M parallel rectifiers and taking into account the ripple cancellation effect due to the 180° phase displacement between the current through each inductor [31,32] in the current-doubler structure; thus,

$$\Delta i_C = \frac{n\pi^2 M V_{Bat(Max)}}{2(1 + n\pi)\omega_p L_o} \tag{17}$$

The output voltage ripple is

$$\Delta v_{Bat} = \frac{n\pi^3 M V_{Bat(Max)}}{16(1 + n\pi)\omega_p^2 L_o C_o} \tag{18}$$

From (18), the ripple of the charging current is a function of the switching frequency, output filter components, and battery parameters.

$$\Delta i_{Bat} = \frac{n\pi^3 M V_{Bat(Max)}}{16(1 + n\pi)r_{Bat}\omega_p^2 L_o C_o} \tag{19}$$

The limitation of the output current ripple, Δi_{Bat} , is mandatory in order to avoid the battery degradation [12].

Reflected Impedance on the Primary Side of the Transformer

Since the output filter removes the high-frequency ripple, the low ripple approximation [29] is used to study the proposed rectifier in steady state. Considering the total current in the primary side and using the first harmonic of the square waveform, the relationship between the AC and DC currents is given in (20).

$$\hat{i}_{ac} = \frac{2I_{Bat}}{n\pi} \tag{20}$$

where \hat{I}_{ac} is the amplitude of the transformer’s primary current. From (20) and (6), the charging current is obtained as a function of the angles $\Psi_0, \Psi_1, \dots, \Psi_{N-1}$,

$$I_{Bat} = \frac{nV_{dc}}{Z_p} \sqrt{\left(\sum_{m=1}^N \sin\Psi_{m-1}\right)^2 + \left(\sum_{m=1}^N \cos\Psi_{m-1}\right)^2} \tag{21}$$

The normalized amplitude of the charging current, I_{Bat} , is depicted in Figure 9 as a function of the control angle, Ψ , and considering the modulation pattern where all phases are evenly shifted.

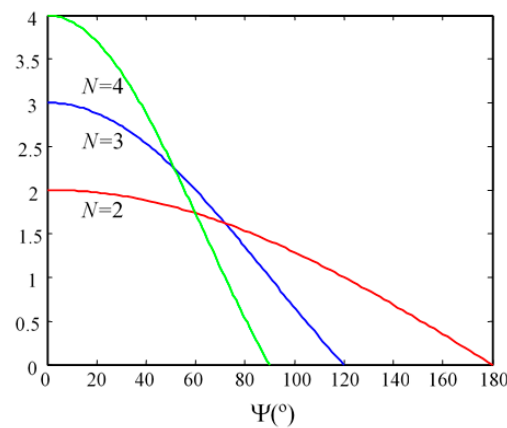


Figure 9. Amplitude of the normalized charging current, I_{Bat} , as a function of the control angle, Ψ , for $N = 2, 3$, and 4 . All phases are evenly shifted, $\Psi_0 = 0^\circ, \Psi_1 = \Psi, \Psi_2 = 2\Psi, \dots, \Psi_{N-1} = (N-1)\Psi$.

Working with (21), the maximum charging current is achieved at $\Psi_0 = \Psi_1 = \Psi_{N-1} = 0^\circ$ and is given by

$$I_{Bat(Max)} = \frac{nV_{dc}}{Z_p} \cdot N \tag{22}$$

From (22), it can be observed that the output current capability of the multiphase converter is enhanced by increasing the number, N , of paralleled phases. An accurate acquisition of the modulation angle, covering the whole range over the entire battery charging process, facilitates the computation of ampere-hours in order to calculate the supplied capacity.

The amplitude of the voltage in the primary side of the transformer is obtained from the power balance in the windings. Assuming a lossless transformer,

$$P_{ac} = P_{Bat} = \frac{\hat{I}_{ac} \hat{V}_{ac}}{2} = I_{Bat} V_{Bat} \tag{23}$$

and substituting (20) into (23),

$$\hat{V}_{ac} = n\pi V_{Bat} = n\pi r_{Bat} \cdot I_{Bat} + n\pi \cdot V_{Bat} \tag{24}$$

From (20) and (24), the battery is modeled from the AC side by

$$\hat{V}_{ac} = \frac{n^2 \pi^2}{2} r_{Bat} \cdot \hat{I}_{ac} + n\pi \cdot V_{Bat} \tag{25}$$

The reflected impedance of the current multiplier and load, R_{ac} , into the AC side of the converter defines important characteristics of the resonant inverter, such as the switching

mode of the transistors, the distortion of the waveforms, and the efficiency [11]. From (25), the rectifier stage is reflected into the AC side as the equivalent resistance R_{ac} in (26),

$$R_{ac} = \frac{\pi^2}{2} n^2 R_{Bat} = \frac{\pi^2}{2} n^2 \left(r_{Bat} + \frac{V_{Bat}}{I_{Bat}} \right) \tag{26}$$

Assuming an ideal transformer, where the leakage inductance reflected in the secondary side is $L_{ks} = 0$, the maximum voltage across the diodes is $V_B = -n\pi V_{Bat}$. However, in practice, L_{ks} is in series with the junction capacitance of the reverse-biased diode, C_j , causing a high-frequency oscillation or ringing. The selection of the Schottky devices takes into account the minimization of this effect.

5. Efficiency of the Multiphase $LC_p C_s$ Resonant Converter

The overall efficiency of the converter is calculated by

$$\eta = \eta_I \cdot \eta_R, \tag{27}$$

where η_I is the efficiency of the resonant inverter stage and η_R is the efficiency of the output current multiplier stage.

5.1. Efficiency of the Inverter Stage

Taking into account the ZVS mode operation of the converter, the switching loss is considered negligible in comparison to the conduction loss. The efficiency of the resonant inverter stage, η_I , considering the conduction loss only [16] is

$$\eta_I = \frac{1}{1 + \frac{r}{R_{ac}} \cdot \frac{\sum_{k=1}^N \hat{I}_i^2}{\hat{I}_{ac}^2}} \tag{28}$$

where \hat{I}_i is the amplitude of each resonant current given in (7). The resistance r represents the $r_{ds_{on}}$ of the transistors as well as the ESR of the inductors. The highest efficiency, $\eta_{I(Max)}$, is achieved with $\Psi_0 = \Psi_1 = \dots = \Psi_{N-1} = 0^\circ$. Upon substitution of $\Psi_0 = \Psi_1 = \dots = \Psi_{N-1} = 0^\circ$ in (28) and under the assumption that C_s is calculated according to (9), the maximum efficiency as a function of the ratio r/R_{ac} , the nominal value of the quality factor, Q_{pN} , and the number of phases, N , is obtained.

$$\eta_{I(Max)} = \frac{1}{1 + \frac{r}{NR_{ac}} \cdot [1 + Q_{pN}^2]} \tag{29}$$

From (28), it is observed that $\eta_{I(Max)}$ is improved by increasing R_{ac} . The straightforward way to increase R_{ac} is through the larger transformer turns ratio, n . However, it should be considered that Q_{pN} increases with n , according to (12), which could jeopardize the ZVS mode of the converter transistors. Taking into account the tight correlation among, N , Q_{pN} , n , and r/R_{ac} , the design process oriented to find a suitable value of these parameters involves iterative cycles. Upon the substitution of (12) and (20) into (29), $\eta_{I(Max)}$ is obtained as a function of the converter parameters,

$$\eta_{I(Max)} = \frac{1}{1 + \frac{\pi^2 r I_{Bat(Max)} V_{Bat(Max)}}{2N V_{dc}^2} + \frac{2r I_{Bat(Max)}}{n^2 \pi^2 N V_{Bat(Max)}}} \approx \frac{1}{1 + \frac{2r I_{Bat(Max)}}{n^2 \pi^2 N V_{Bat(Max)}}} \tag{30}$$

The maximum efficiency of the resonant inverter stage, $\eta_{I(Max)}$, improves, approaching one asymptotically as the number of phases, N , increases.

5.2. Efficiency of the Output Current Multiplier

Limiting the current level through the output rectifier stage is a major design challenge oriented to reduce the conduction loss. The proposed M -windings output current multiplier

lowers the amplitude of the current through diodes by a factor M and the average current through filter inductors by a factor $2M$. An expression for the rectifier efficiency, η_R , only including the conduction loss, is obtained from the analysis of the current paths shown in Figure 7. Considering a lossless transformer, the total power, P_T , in the secondary side of the current multiplier is

$$P_T = P_{Bat} + M \left(\frac{V_D I_{Bat}}{M} + \frac{I_{Bat}^2 r_D}{M^2} + \frac{I_{Bat}^2 r_{LF}}{4M^2} \right), \quad (31)$$

where P_{Bat} is the output power, $P_{Bat} = V_{Bat} \cdot I_{Bat}$, V_D and r_D are the voltage and dynamic resistance of the linear model of the diode, and r_{LF} is the ESR of the filter inductor L_o . The efficiency, η_R , is calculated with $\eta_R = P_{Bat} / P_T$,

$$\eta_R = \frac{1}{1 + \frac{V_D}{V_{Bat}} + \frac{\left(\frac{r_D}{M} + \frac{r_{LF}}{2M}\right) I_{Bat}}{V_{Bat}}}. \quad (32)$$

The efficiency of the output current multiplier, η_R , is improved by increasing the number of secondary windings, M . The theoretical limit $\eta_{R(Max)}$ of η_R is obtained letting $M \rightarrow \infty$,

$$\eta_{R(Max)} = \frac{1}{1 + \frac{V_D}{V_{Bat(Max)}}}. \quad (33)$$

From (32) and (33), it can be observed that the ratio $V_D / V_{Bat(Max)}$ should be minimized, which confirms the benefit of using Schottky diodes or sync rectifiers to improve the efficiency of the rectifier stage.

5.3. Optimum N and M of Parallelized Stages

The expressions (30) to (33) are used as a criterion to define the appropriate number of phases, N , of the resonant inverter stage as well as the number of secondary windings, M , of the output current multiplier. The maximum efficiency of the inverter section, $\eta_{I(Max)}$, and the efficiency of the current multiplier, η_R , are depicted in Figure 10 as a function of N and M .

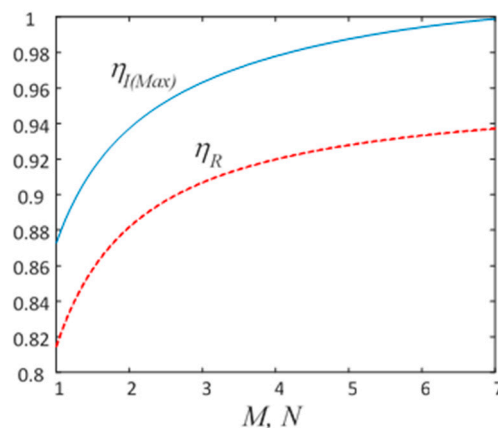


Figure 10. Maximum efficiency of the resonant inverter stage, $\eta_{I(Max)}$, and efficiency of the output current multiplier, η_R , as a function of the number of phases, N , and secondary windings M . The following typical values are assumed: $n = 2$, $r = 1.7 \Omega$, $I_{Bat(Max)} = 20 \text{ A}$, $2rI_{Bat(Max)} / \pi^2 V_{Bat(Max)} = 0.5$, $V_D / V_{Bat(Max)} = 0.05$ and $r_D = r_{LF} = 0.1$.

From a practical point of view, the asymptotic variation of η_R and $\eta_{I(Max)}$, shown in Figure 10, limits the maximum values of M and N . The criterion for choosing the suitable values of M and N is a tradeoff between the increment of the efficiency and the circuit complexity. It is assumed that if the increment of efficiency achieved is barely 1%, a higher number of secondary windings M or phases, N , is not justified.

6. Design of the Multiphase $LC_p C_s$ Resonant Converter

- (1) The maximum battery voltage is set at $V_{Bat(Max)} = 53.5$ V, which is below the overvoltage protection limit (54.7 V) defined by the BMS. The output current capability of the circuit is set to $I_{Bat} = 20$ A in order to shortening the charging time. The equivalent impedance of the battery is $R_{Bat} = 2.67$ Ω . The peak power that must be supplied by the charger is $P_{Bat} = 1.07$ kW. The converter supply voltage is $V_{dc} = 400$ V, which is the output voltage of a previous front-end PFC stage. The switching frequency is set at $\omega_p = 2\pi(125$ kHz).
- (2) The drive signals of the transistors are obtained from an integrated circuit IR2111 with a dead time, $t_d = 650$ ns. From (10), the minimum value of the power factor angle for each class D section is $\phi_{zvs} = 29.25^\circ$. Using the design constrain $\phi_i = 2\phi_{zvs} = 58^\circ$ from (11), the nominal value of the quality factor is obtained, $Q_{pN} = 0.624$. The transformer turns ratio, n , is calculated from (14), approximating to the nearest entire value, $n = 1$.
- (3) The number of phases, N , is calculated taking into account that transistors are low-cost CoolMOS™ SPA11N60C3 (Infineon, Neubiberg, Germany) with $r_{ds(on)} = 0.38$ Ω . Considering the equivalent series resistant (ESR) of the resonant inductors and tracks of the printed circuit board (PCB), a worst case of $r = 1$ Ω is assumed. Upon substitution in (30), the pair $n = 1$ and $N = 4$ yields $\eta_{I(Max)} = 0.98$. This value of efficiency means 21 W power loss in the resonant inverter stage at full load conditions.
- (4) The expected efficiency of the rectifier stage is calculated using the conduction loss model of the Schottky diode STPS30M60S (STMicroelectronics, Geneva, Switzerland) from ST with $V_D = 0.395$ V and $r_D = 0.0047$ Ω . The filter inductors are Vishay IHLP–8787MZ (Vishay Intertechnology, Malvern, USA) with $L_o = 75$ μ H and $r_{LF} = 30$ m Ω at 25° C. Taking into account the temperature effect, the value $r_{LF} = 90$ m Ω is assumed. Upon substitution of V_D , r_D , $V_{Bat(Max)}$, r_{LF} , and $I_{Bat} = 20$ A in (32), the value $M = 1$ yields an efficiency of the rectifier stage at maximum load, $\eta_R = 0.97$. This value of efficiency means 32 W power loss in the current-doubler rectifier at full load. In this way, the configuration of a four-phases ($N = 4$) resonant inverter with a single ($M = 1$) current-doubler rectifier as output stage achieves an overall efficiency at full load equal to $\eta = \eta_I \cdot \eta_R = 0.95$.
- (5) From (16), the amplitude of the current ripple in each inductor is $\Delta i_L = 2.16$ A. The r_{Bat} is estimated at 40 m Ω . The output capacitor, C_o , is calculated to achieve a maximum current ripple equal to 0.1% of the charging current, $\Delta i_{Bat} = 20$ mA. From (19), $C_o = 680$ μ F.
- (6) The characteristic impedance is obtained from (22), $Z_p = 80$ Ω . In Table 1, the reactive components are $L = Z_p / \omega_p = 100$ μ H and $C_p = 4 / \omega_p Z_p = 64$ nF.
- (7) The transformer has been built with an ETD49 core of material N87. The primary and secondary are 16 single-layer turns of 40 strands of litz wire. The resulting magnetizing inductance is $L_M = 800$ μ H and the leakage inductance from the primary and secondary sides are $L_{kp} = L_{ks} = 1.4$ μ H. The total leakage inductance is $L_k = L_{kp} + n^2 \cdot L_{ks} = 2.8$ μ H.
- (8) Once L_k is known, the series capacitor C_s is calculated with (9) to cancel out the effect of L_k , $C_s = 571$ nF.

7. Control Circuit and Battery Modeling

During the CV stage, the charging current must be regulated to avoid the voltage of the battery exceeding $V_{Bat(Max)}$. The current is modulated through the phase-angles Ψ_0 , Ψ_1 , and Ψ_{N-1} , while keeping the switching frequency constant. Different patterns are possible for adjusting Ψ_1 , Ψ_2 , and Ψ_{N-1} . For any value of N , the full control of the charging current is achieved if the phase shift is evenly distributed among all N phases, e.g., $\Psi_0 = 0^\circ$, $\Psi_1 = \Psi$, $\Psi_2 = 2\Psi \dots \Psi_{N-1} = (N-1)\Psi$. In this case, the minimum current $I_{Bat} = 0$ A is achieved at $\Psi = 360^\circ / N$. This pattern requires N control signals. For this design, where $N = 4$, the control angles are adjusted as follows: $\Psi_0 = \Psi_1 = 0^\circ$ and $\Psi_2 = \Psi_3 = \Psi$. For this approach, the minimum $I_{Bat} = 0$ A is achieved at $\Psi = 180^\circ$, and only two control signals are required, which implies a simplification of the control circuit.

Once the converter is designed, the battery-charger system is completed with a control loop to limit the output voltage of the charger to the maximum value recommended for the battery. The action of the control loop transforms the circuit’s open-loop current source behavior into a voltage source. A type I error amplifier is enough for this action. The scheme of the charger-battery system, modeled in Simulink, is shown in Figure 11. In the voltage mode, the battery imposes the dynamic response of the converter-battery system [27].

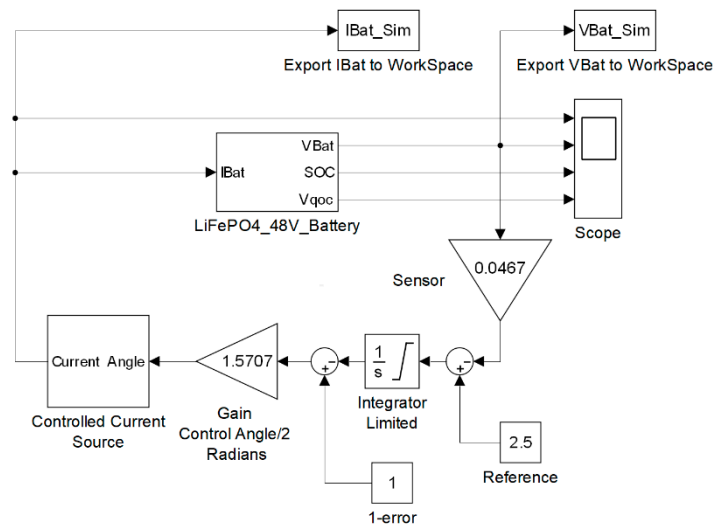


Figure 11. Control loop for limiting the maximum battery voltage, $V_{Bat(Max)}$.

The Simulink® model of the battery [34,35] is shown in Figure 12. The look-up tables include the quasi-open circuit voltage of a basic cell for the charge and discharge trajectories as a function of the SOC.

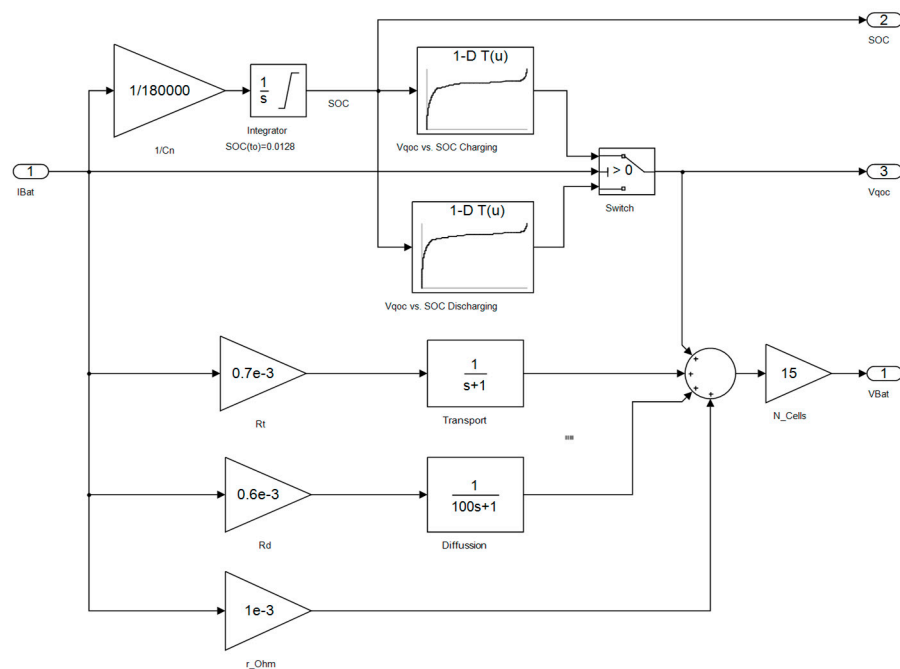


Figure 12. Simulink® model of the battery.

The different parameters of the model can be tuned using curve fitting. The data used as reference for adjusting the model were obtained from the experimental characterization of the battery charging at 25 A, which has been shown in Figure 1. The time constant for charge transportation and diffusion phenomena are 1 s and 100 s, respectively. The

impedance for the charge transport is $R_t = 0.7 \text{ m}\Omega$ and the capacitance is $C_t = 1428 \text{ F}$. The impedance of the diffusion is $R_d = 0.6 \text{ m}\Omega$ and the corresponding capacitance is $C_d = 166,000 \text{ F}$. The impedance due to electrodes and electric connections is $R_\Omega = 1 \text{ m}\Omega$. The impedance of the battery pack is obtained from (4), $r_{bat} = 34.5 \text{ m}\Omega$. This value of r_{Bat} includes the impedance of connectors and cables, which is used to conform to the battery by the series connection of the 15 cells.

The variation of the battery voltage, obtained from the simulation of the system in Figure 11, is shown in Figure 13. It can be observed that simulation and experimental results are in good agreement for the three charging profiles in Figure 2 that were evaluated experimentally.

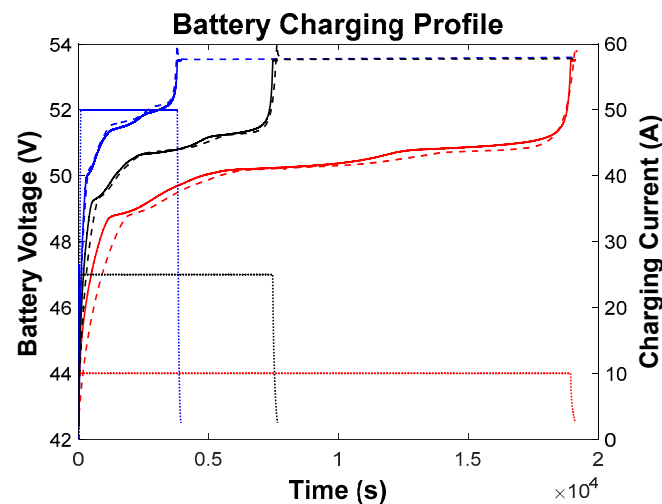


Figure 13. Charging profiles at 10, 25, and 50 A. Solid lines: Experimental battery voltage. Dashed lines: Simulation result. Dot lines: Charging current.

8. Results of the Experimental Prototype

An experimental prototype, shown in Figure 14, has been built to validate the theoretical proposal.

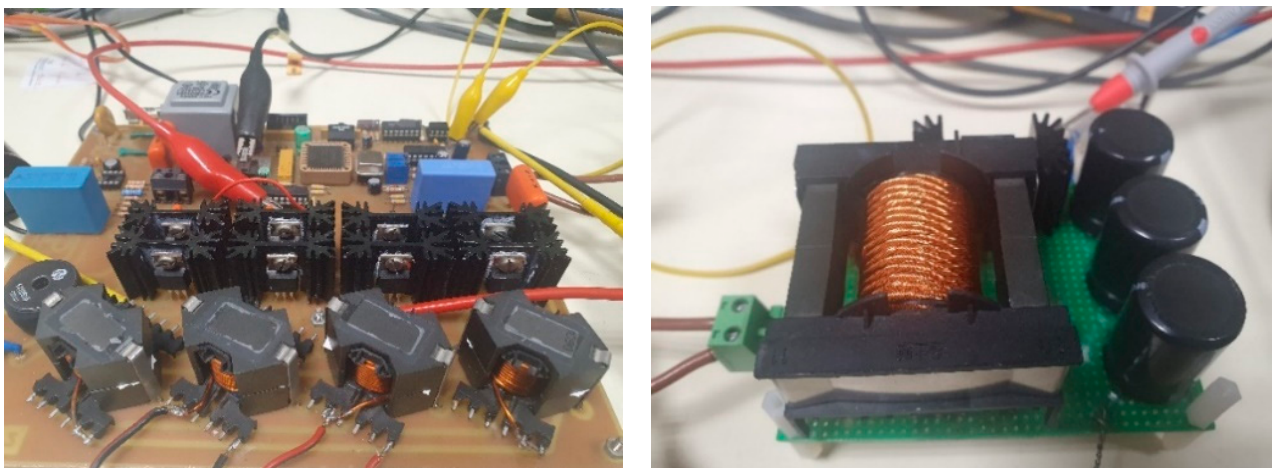


Figure 14. Details of the experimental prototype of the charger. (Left) Four-phase resonant inverter stage. (Right) Current-doubler rectifier.

When connecting the battery to the charger, an initial frequency sweep is programmed to ensuring the gradual growth of the charging current to prevent the occurrence of an overvoltage across the discharged battery. The experimental waveforms in different circuit sections are shown in Figures 15–17. In order to demonstrate the charger performance at different operation points, the waveforms for full load and 70% of full load operation are

shown. In Figure 15, it is observed that the resonant current has a phase lag with respect to the input voltage. At full load condition, $\varphi_{i_{1,2}} = \varphi_{i_{3,4}} = 54^\circ$, which is in good agreement with the theoretical value, and at 70% of the full load condition, $\varphi_{i_{1,2}} = 54^\circ$, $\varphi_{i_{3,4}} = 72^\circ$. The ZVS mode operation was verified for all phases of the resonant inverter section.

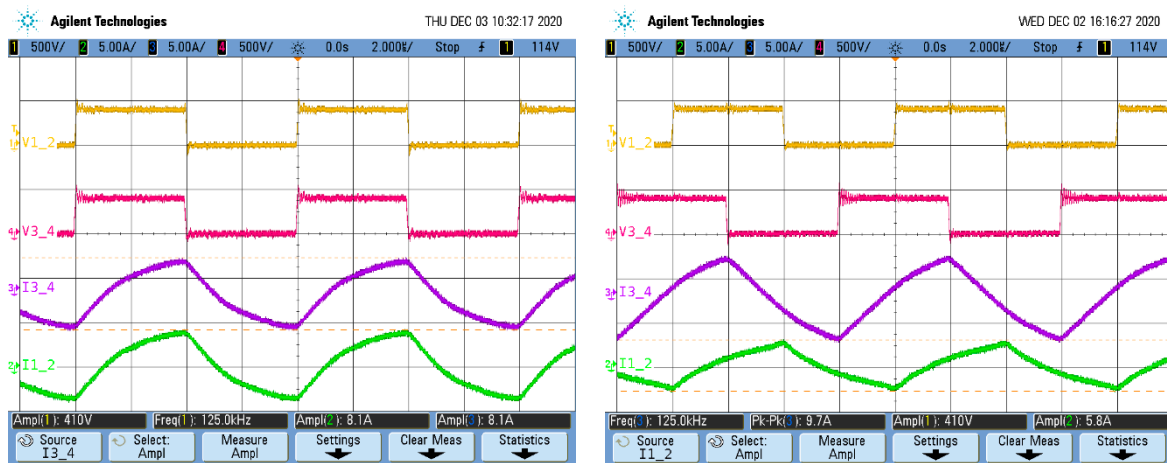


Figure 15. From top to bottom: Midpoint voltages of phases 1 and 2, $v_{1,2}$. Midpoint voltages of phases 3 and 4, $v_{3,4}$. Resonant current of phases 1 and 2, $i_{1,2}$. Resonant current of phases 3 and 4, $i_{3,4}$. (Left) Full load condition ($\Psi_0 = \Psi_1 = \Psi_2 = \Psi_3 = 0^\circ$). (Right) 70% of full load condition ($\Psi_0 = \Psi_1 = 0^\circ$, $\Psi_2 = \Psi_3 = 90^\circ$).

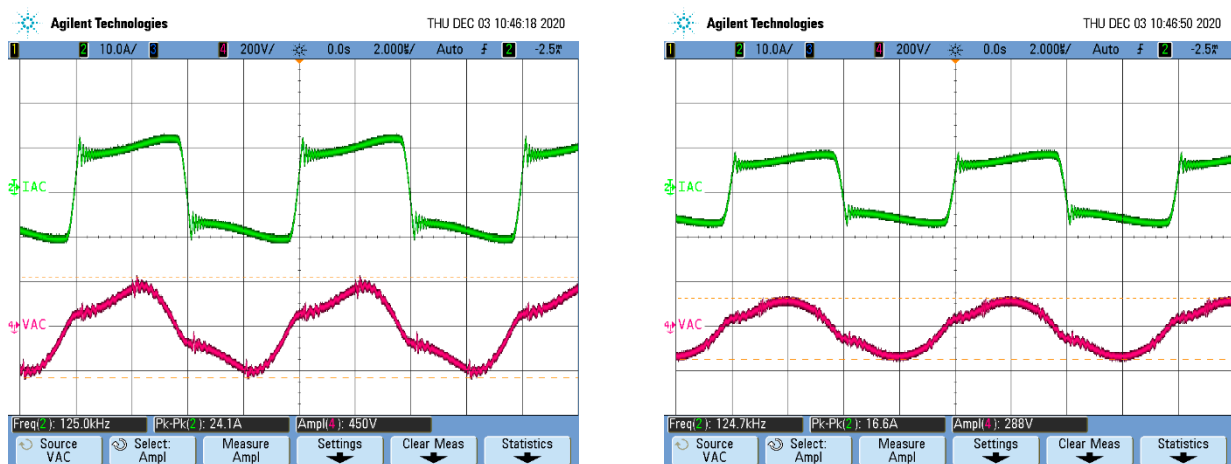


Figure 16. From top to bottom: Output current through the primary side of the transformer, i_{ac} . Output voltage applied to the primary side of the transformer, v_{ac} . (Left) Full load condition ($\Psi_0 = \Psi_1 = \Psi_2 = \Psi_3 = 0^\circ$). (Right) 70% of full load condition ($\Psi_0 = \Psi_1 = 0^\circ$, $\Psi_2 = \Psi_3 = 90^\circ$).

In Figure 16, the current and voltage at the primary side of the transformer are shown. The amplitude of the current square waveform is half (10 A) of the battery charging current. In Figure 17, the charging current at full load (20 A) and at 70% of full load are shown. The results are in good agreement with the theoretical value according to the control angle Ψ . It can be observed that the charging current ripple is negligible as it is required for this application. The experimental efficiency of the prototype measured at the point of maximum load ($I_{Bat} = 20 \text{ A}$, $P_{Bat} = 1.07 \text{ kW}$) was $\eta = 91.3\%$. The efficiency at 70% and 50% of the full load was $\eta = 90.2\%$ and $\eta = 88\%$, respectively. The experimental efficiency is slightly lower than the theoretical due to the switching losses, the power dissipation at the transistors drive circuit, and the auxiliary power supply loss.

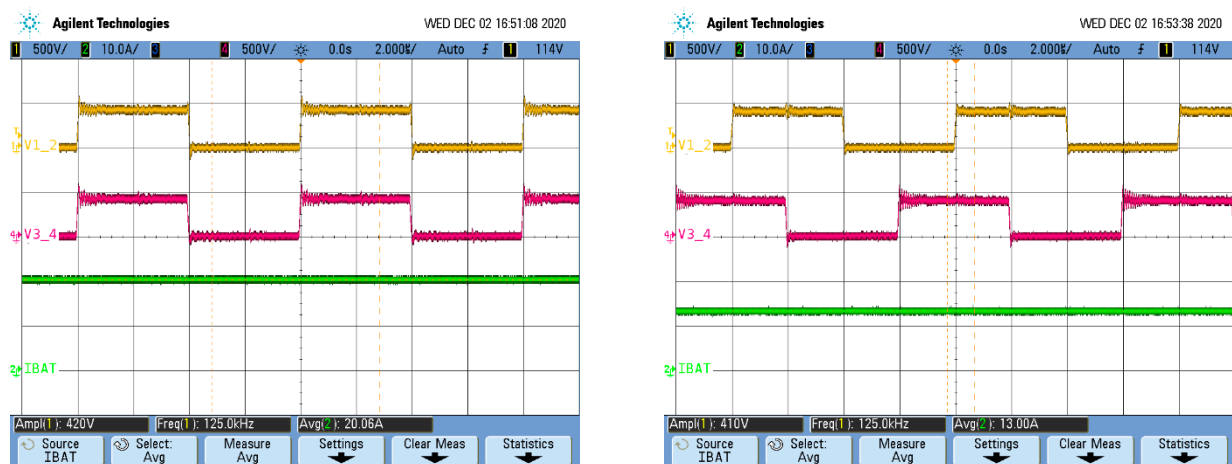


Figure 17. From top to bottom: Midpoint voltages of phases 1 and 2, $v_{1,2}$. Midpoint voltages of phases 3 and 4, $v_{3,4}$. Charging current i_{Bat} . **(Left)** Full load condition ($\Psi_0 = \Psi_1 = \Psi_2 = \Psi_3 = 0^\circ$). **(Right)** 70% of full load condition ($\Psi_0 = \Psi_1 = 0^\circ$, $\Psi_2 = \Psi_3 = 90^\circ$).

9. Discussion

In this work, the general design method of the proposed charger has been explained, but the particular configuration of the final solution depends on the chosen technology. One key decision is the most suitable value of the dc-link voltage. The solution for an dc-link voltage $V_{dc} = 400$ V, which was obtained from a single-phase power factor corrector (PFC) based on a Boost Converter, and using the CoolMOS™ SPA11N60C3 MOSFET transistor and the STPS30M60S Schottky diode has been fully developed. As alternative, a solution with $V_{dc} = 800$ V, obtained from a three-phase PFC and using silicon carbide (SiC) components is also assessed. For this case, the third-generation C3M0065100K MOSFET transistor (Wolfspeed, Research Triangle Park, USA) with the CGD15SG00D2 driver (Wolfspeed, Research Triangle Park, USA) is used in the inverter section. As the voltage, current, and power at the circuit output are the same, the silicon (Si) Schottky diode STPS30M60S is used in both cases. For a better comparison, both designs are summarized in Table 2.

Table 2. Designs comparison.

V_{dc}	n	N	M	Z_p	Q_{pN}	η	$I_{Bat(Max)}$	$P_{Bat(Max)}$
400 V	1	4	1	80 Ω	0.624	0.95	20 A	1.07 kW
800 V	2	2	1	160 Ω	0.624	0.966	20 A	1.07 kW

As it can be seen in Table 2, both designs achieve a similar theoretical efficiency, but the SiC technology uses only two phases for the resonant inverter stage.

Considerations about the Solution Cost

SiC technology for power devices is becoming more competitive in technical performance and cost. Important advances have been reported in terms of increasing the wafer diameter and minimization of the defect density [36], which contribute to lowering the cost of the devices, so it is worth comparing the cost of the proposed alternatives. Focusing on the inverter section of the described designs, i.e., $V_{dc} = 400$ V for the four-phase Si inverter and $V_{dc} = 800$ V for the two-phase SiC inverter, the cost assessment reveals that at present, the solution based on SiC components is more expensive despite requiring fewer transistors. The cost of the third-generation SiC MOSFET C3M0065100K is five times ($5 \times$) that of the SPA11N60C3 Si MOSFET. On the other hand, in contrast to the simplicity of the half-bridge driver, based on the integrated circuit IR2111, the complexity and cost of the selected driver CGD15SG00D2 for SiC MOSFETS are also significantly higher [37]. In addition, the PFC section adds a cost difference in favor of the $V_{dc} = 400$ V four-phase Si

design. For illustrating the analysis, in Tables 3 and 4, the cost of the SiC components and its Si counterparts are summarized [38]. Differences in the magnetic elements, capacitors, and control circuit have less impact on cost.

Table 3. SiC resonant inverter.

Component	Quantity	Cost (Retail Sale)
MOSFET C3M0065100K	4	40€
Driver CGD15SG00D2	4	200€

Table 4. Si resonant inverter.

Component	Quantity	Cost (Retail Sale)
MOSFET SPA11N60C3	8	16€
Driver IR2111	4	8€

Nowadays, for a given architecture, the use of SiC MOSFETs could be recommended if the maximum current, voltage, and temperature limits of the Si MOSFETs are compromised, e.g., for charging currents and powers higher than 50 A and 2.5 kW, respectively.

10. Conclusions

The general design procedure of a multiphase resonant converter for battery charger applications has been presented. Since the output current on the AC side is shared among N equal inverter sections, the circuit presents high output current capability using low-cost power MOSFETs, and the design of the resonant inductors is simplified. The proposed output rectifier is based on an M -winding current-doubler rectifier that also diminishes the conduction loss by using passive components. The efficiency curve of the proposed charger exhibits a wide flat zone, assuring a constant value of efficiency even at light load conditions. This feature is very interesting for the battery charger applications, taking into account that high efficiency is desirable along the whole charging process, despite the heavy load variation. The effect on the AC side of the leakage inductance of the transformer L_k is canceled out by the series capacitor C_s . The maximum charging current is limited by the circuit in an inherent manner, without the necessity of any control. However, the output voltage is limited to the maximum value recommended for the battery by a voltage control loop with a type I error amplifier. The control action is performed keeping constant the switching frequency by adjusting the control angle, Ψ , while maintaining the ZVS mode at any operation point. The general proposal has been validated by implementing an experimental prototype for charging a commercial 48 V LiFePO₄ battery with 50 Ah of capacity. The achieved efficiency of the $N = 4$ inverter with $V_{dc} = 400$ V using Si MOSFETs is similar to the predicted with an $N = 2$ inverter with $V_{dc} = 800$ V using SiC MOSFETs.

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