

UNIT-6

PROGRAMMABLE INTERRUPT CONTROLLERS

8259A-PROGRAMMABLE INTERRUPT CONTROLLER (PIC)

INTRODUCTION

Microcomputer system design requires that I/O devices such as keyboards, displays, sensors and other components receive servicing in an efficient manner so that large amounts of the total system tasks can be assumed by the microcomputer with little or no effect on throughput.

The most common method of servicing such devices is the Polled approach. This is where the processor must test each device in sequence and in effect "ask" each one if it needs servicing.

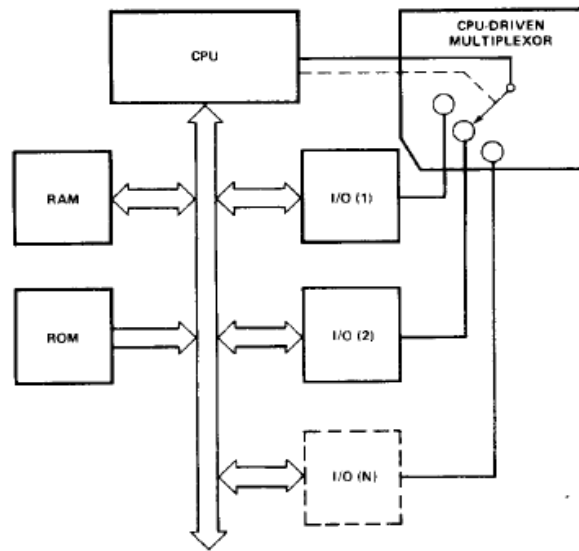


Fig. Polled method

A more desirable method would be one that would allow the microprocessor to be executing its main program and only stop to service peripheral devices when it is told to do so by the device itself. In effect, the method would provide an external asynchronous input that would inform the processor that it should complete whatever instruction that is currently being executed and fetch a new routine that will service the requesting device. Once this servicing is complete, however, the processor would resume exactly where it left off. This method is called Interrupt method.

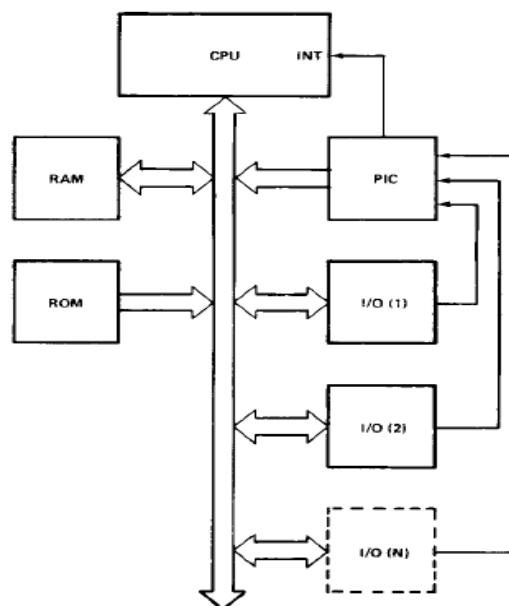


Fig. Interrupt method

NEED OF 8259-PIC

If we are working with an 8086, we have a problem here because the 8086 has only two interrupt inputs, NMI and INTR. If we save NMI for a power failure interrupt, this leaves only one interrupt for all the other applications. For applications where we have interrupts from multiple sources, we use an external device called a *priority interrupt controller* (PIC) to the interrupt signals into a single interrupt input on the processor.

The Programmable Interrupt Controller (PIC) functions as an overall manager in an Interrupt-Driven system environment. It accepts requests from the peripheral equipment, determines which of the incoming requests is of the highest importance (priority), ascertains whether the incoming request has a higher priority value than the level currently being serviced, and issues an interrupt to the microprocessor based on this determination.

FEATURES OF 8259A

The Intel 8259A Programmable Interrupt Controller handles up to eight vectored priority interrupts for the microprocessor. It is cascadable for up to 64 vectored priority interrupts without additional circuitry. It is packaged in a 28-pin DIP, uses NMOS technology and requires a single +5V supply. Circuitry is static, requiring no clock input. The 8259A is designed to minimize the software and real time overhead in handling multi-level priority interrupts. It has several modes, permitting optimization for a variety of system requirements. The 8259A is fully upward compatible with the Intel 8259. Software originally written for the 8259 will operate the 8259A in all 8259 equivalent modes.

- It is a tool for managing the interrupt requests.
- Compatible with 8-bit as well as 16-bit microprocessors.
- It provides 8 priority interrupt request levels.
- Be expanded to 64 priority levels by cascading additional 8259As.
- The interrupts can be masked or unmasked individually.
- Programmable interrupt modes.
- Available in 28-pin DIP.
- It requires a single +5v supply.

ARCHITECTURE OF 8259A-PIC

The 8259A is a device specifically designed for use in real time, interrupt driven microcomputer systems. It manages eight levels or requests and has built-in features for expandability to other 8259A's (up to 64 levels). It is programmed by the system's software as an I/O peripheral. A selection of priority modes is available to the programmer so that the manner in which the requests are processed by the 8259A can be configured to match his system requirements. The internal block diagram of 8259A is shown below.

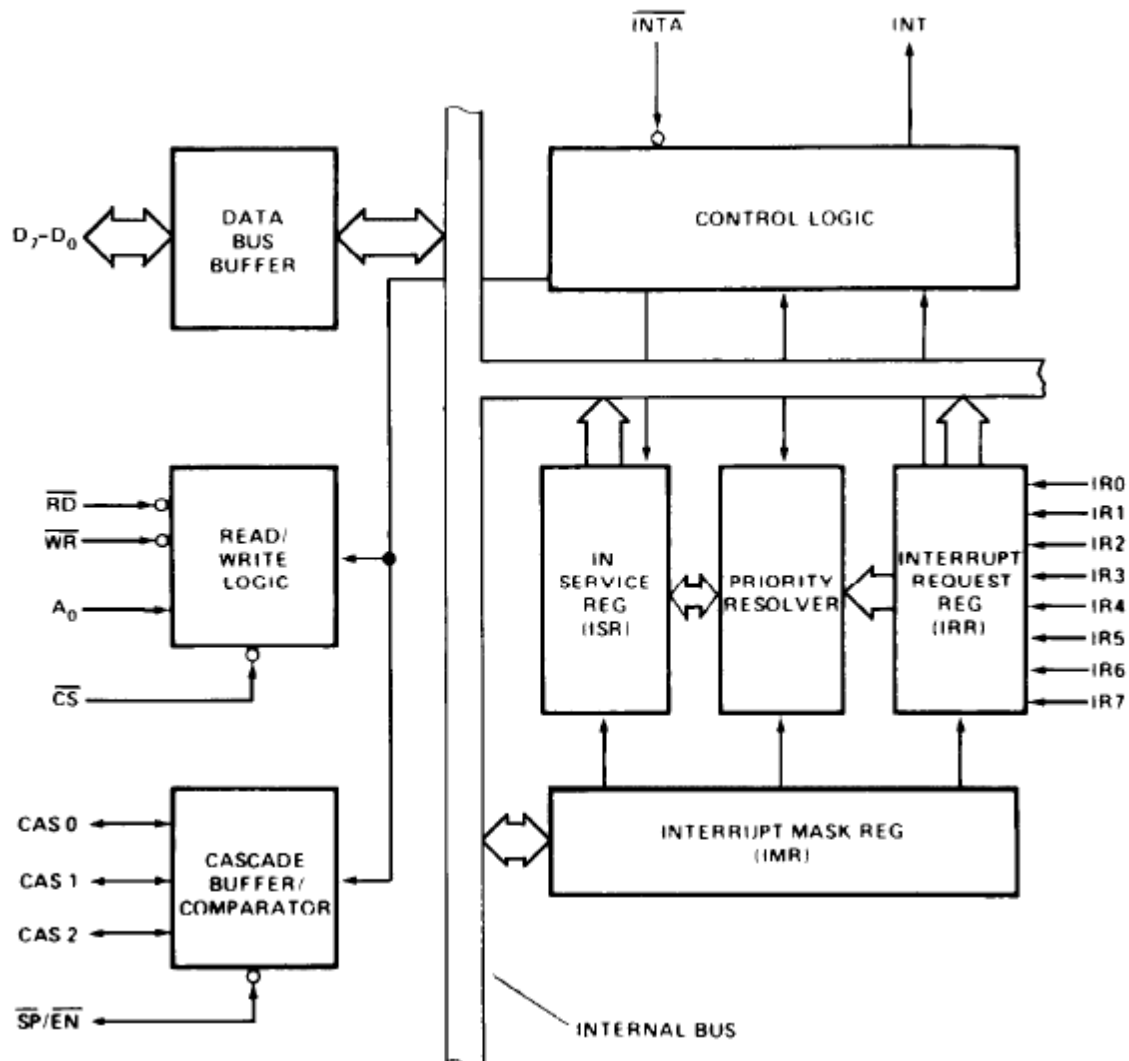
Control logic: Control logic has two signals.

INT (Interrupt): This output goes directly to the microprocessor interrupt input.

INTA (Interrupt Acknowledge): INTA pulses will cause the 8259A to release vectoring information onto the data bus.

Interrupt Request Register (IRR) and In-Service Register (ISR): The interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In-Service (ISR). The IRR has eight input lines (IR0-IR7) for interrupts. When these lines go high, the request is stored in IRR in order to serve them one by one on the priority basis. Normally IR0 has highest priority and IR7 has the lowest priority. The priorities of the interrupt request input are also programmable.

The IRR is used to store all the interrupt levels which are requesting service; and the ISR is used to store all the interrupt levels which are being serviced.



Priority Resolver: This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during INTA pulse.

Interrupt Mask Register (IMR): The IMR stores the bits which mask the interrupt lines to be masked. The IMR operates on the IRR.

Data Bus Buffer: This bidirectional 8-bit buffer is used to interface the 8259A to the system Data Bus. Control words and status information are transferred through the Data Bus Buffer.

Read/Write Control Logic: The function of this block is to accept output commands from the microprocessor. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store the various control formats for device operation. This function block also allows the status of the 8259A to be transferred onto the Data Bus.

The Cascade Buffer/Comparator: This function block stores and compares the IDs of all 8259A's used in the system. The associated three I/O pins (CAS0-2) are outputs when the 8259A is used as a master and are inputs when the 8259A is used as a slave. As a master, the 8259A sends the ID of the interrupting slave device onto the CAS0-2 lines.

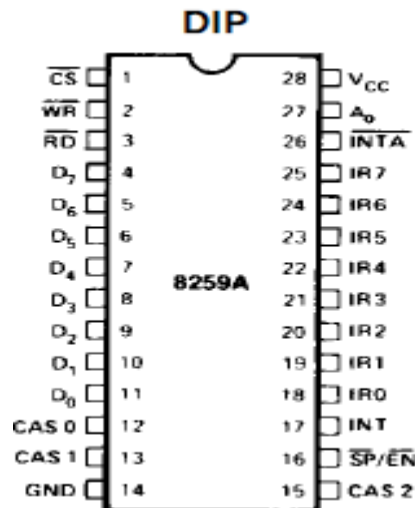
INTERRUPT SEQUENCE IN 8086 SYSTEM

The events occur as follows in an 8086-8259A system:

1. One or more of the INTERRUPT REQUEST lines (IR7 – IR0) are raised high, setting the corresponding IRR bit(s).
2. The 8259A evaluates these requests, and sends an INT to the CPU, if appropriate.
3. The CPU acknowledges the INT and responds with an \overline{INTA} pulse.

4. Upon receiving an \overline{INTA} from the CPU group, the highest priority ISR bit is set, and the corresponding IRR bit is reset. The 8259A will also release a CALL instruction code (11001101) onto the 8-bit Data Bus through its D7 - D0 pins.
5. This CALL instruction will initiate second INTA pulses to be sent to the 8259A from the CPU group.
6. This \overline{INTA} pulse allows the 8259A to release an 8-bit preprogrammed subroutine address onto the Data Bus.
7. ISR bit is reset at the end of the 2nd \overline{INTA} pulse if automatic EOI mode is programmed

PIN DIAGRAM OF 8259A



V_{CC}: +5V Supply.

GND: Ground.

\overline{CS} : A LOW on this input enables the 8259A. No reading or writing of the chip will occur unless the device is selected.

\overline{WR} : A LOW on this input enables the microprocessor to write control words (ICWs and OCWs) to the 8259A.

\overline{RD} : A LOW on this input enables the 8259A to send the status of the Interrupt Request Register (IRR), In Service Register (ISR), the Interrupt Mask Register (IMR), or the Interrupt level onto the Data Bus.

A₀: This input signal is used in conjunction with WR and RD signals to write commands into the various command registers, as well as reading the various status registers of the chip. This line can be tied directly to one of the address lines.

D₇-D₀: Control, status and interrupt-vector information is transferred via this bus.

CAS₀-CAS₂: The CAS lines form a private 8259A bus to control a multiple 8259A structure. These pins are outputs for a master 8259A and inputs for a slave 8259A.

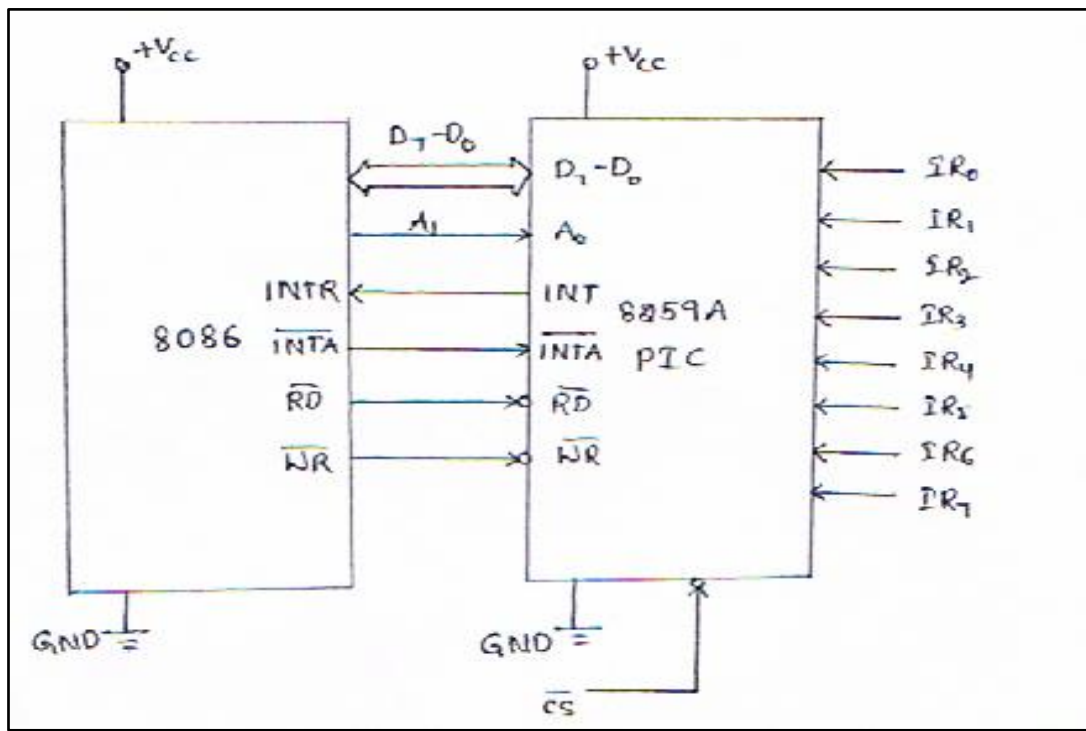
$\overline{SP/EN}$: This is a dual function pin. When in the Buffered Mode it can be used as an output to control buffer transceivers (EN). When not in the buffered mode it is used as an input to designate a master (SP=1) or slave (SP=0).

INT: This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the microprocessor, thus it is connected to the microprocessor's interrupt pin.

\overline{INTA} : This pin is used to enable 8259A interrupt-vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the microprocessor.

IR7-IR0: Asynchronous inputs. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged (Edge Triggered Mode), or just by a high level on an IR input (Level Triggered Mode).

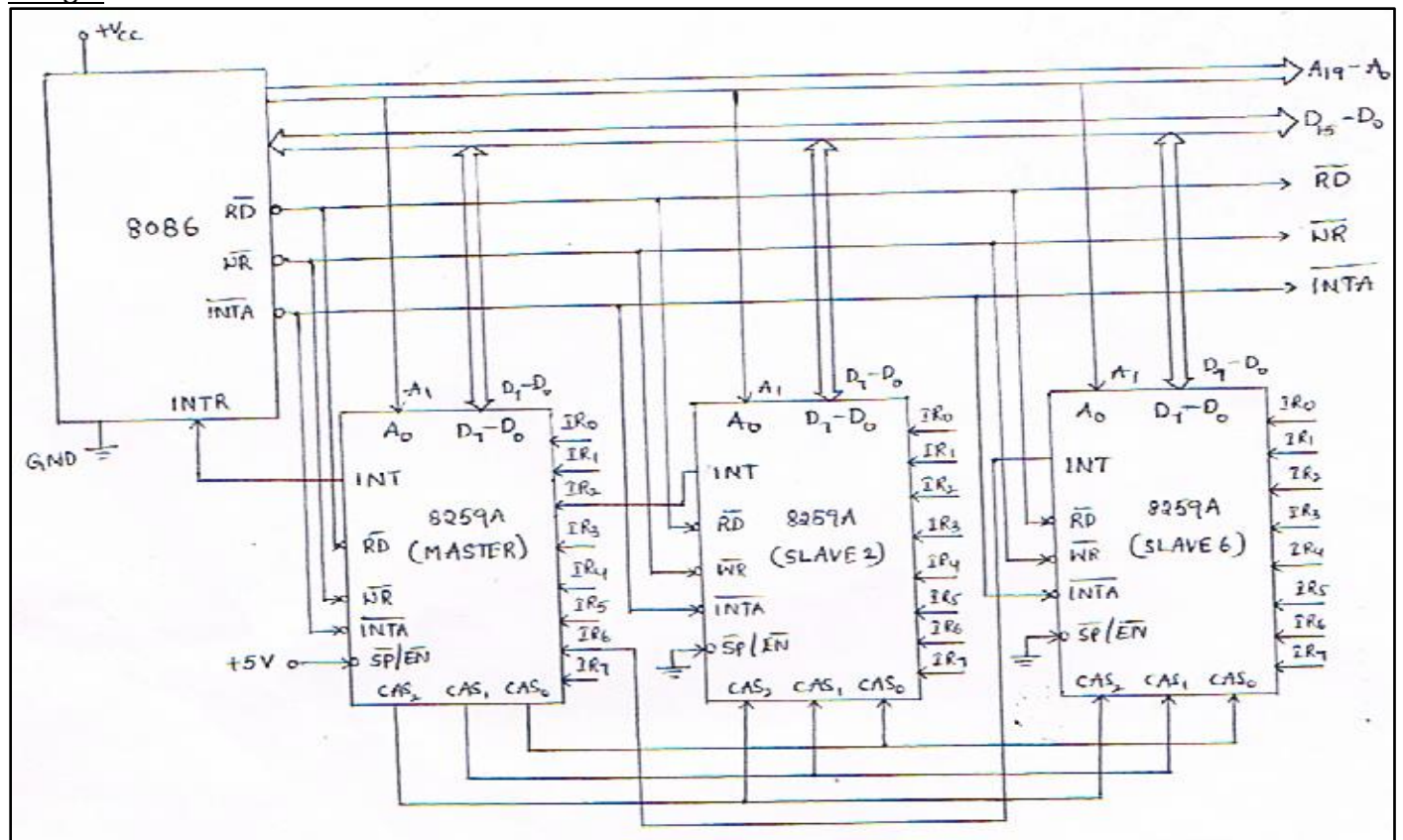
8259A PIC INTERFACING WITH 8086



CASCADED INTERFACING OF 8259A

Example: Interface 3 IC's of 8259A PIC with 8086 in such way that one is master and rest two are slaves connected at IR2 and IR6 interrupt request level of the master.

Design:



OPERATING MODES OF 8259A PIC

The different modes of operation of 8259A can be programmed by setting or resting the appropriate bits of the ICW or OCW as discussed previously. The different modes of operation of 8259A are explained in the following.

Fully Nested Mode: This is the default mode of operation of 8259A. IR0 has the highest priority and IR7 has the lowest one. When interrupt request are noticed, the highest priority request amongst them is determined and the vector is placed on the data bus. The corresponding bit of ISR is set and remains set till the microprocessor issues an EOI command just before returning from the service routine or the AEOI bit is set.

End of Interrupt (EOI): The ISR bit can be reset either with AEOI bit of ICW1 or by EOI command, issued before returning from the interrupt service routine. There are two types of EOI commands specific and non-specific.

Automatic Rotation: This is used in the applications where all the interrupting devices are of equal priority. In this mode, an interrupt request IR level receives priority after it is served while the next device to be served gets the highest priority in sequence. Once all the device are served like this, the first device again receives highest priority.

Automatic EOI Mode: Till AEOI=1 in ICW4, the 8259A operates in AEOI mode. In this mode, the 8259A performs a non-specific EOI operation at the trailing edge of the last INTA pulse automatically. This mode should be used only when a nested multilevel interrupt structure is not required with a single 8259A.

Specific Rotation: In this mode a bottom priority level can be selected, using L2, L1 and L0 in OCW2 and R=1, SL=1, EOI=0. The selected bottom priority fixes other priorities. If IR5 is selected as a bottom priority, then IR5 will have least priority and IR4 will have a next higher priority. Thus IR6 will have the highest priority.

Specific Mask Mode: In specific mask mode, when a mask bit is set in OCW1, it inhibits further interrupts at that level and enables interrupt from other levels, which are not masked.

Edge and Level Triggered Mode: This mode decides whether the interrupt should be edge triggered or level triggered. If bit LTIM of ICW1=0 they are edge triggered, otherwise the interrupts are level triggered.

Special Fully Nested Mode: This mode is used in more complicated system, where cascading is used and the priority has to be programmed in the master using ICW4. This is somewhat similar to the normal nested mode.

Buffered Mode: When the 8259A is used in the systems where bus driving buffers are used on data buses. The problem of enabling the buffers exists. The 8259A sends buffer enable signal on $\overline{SP}/\overline{EN}$ pin, whenever data is placed on the bus.

Cascade Mode: The 8259A can be connected in a system containing one master and eight slaves (maximum) to handle upto 64 priority levels. The master controls the slaves using CAS0-CAS2 which act as chip select inputs (encoded) for slaves.

PROGRAMMING THE 8259A PIC

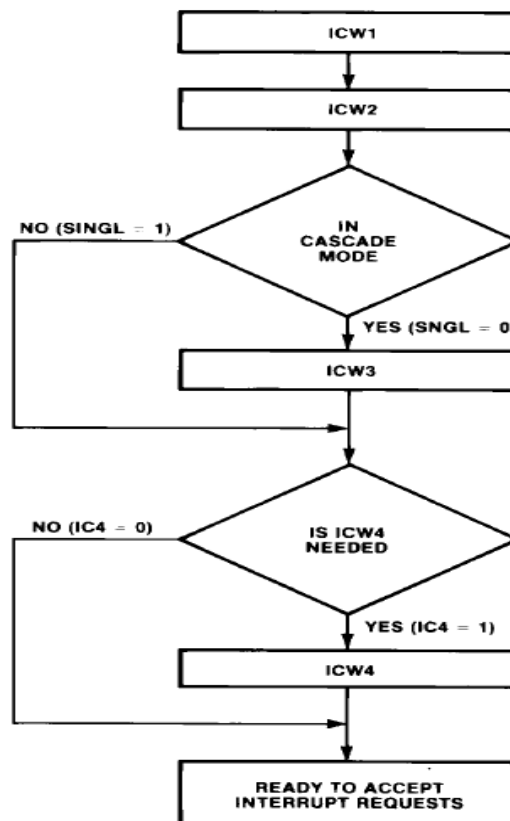
The 8259A accepts two types of command words generated by the microprocessor.

1. Initialization Command Words (ICWs)
2. Operation Command Words (OCWs)

Initialization Command Words (ICWs)

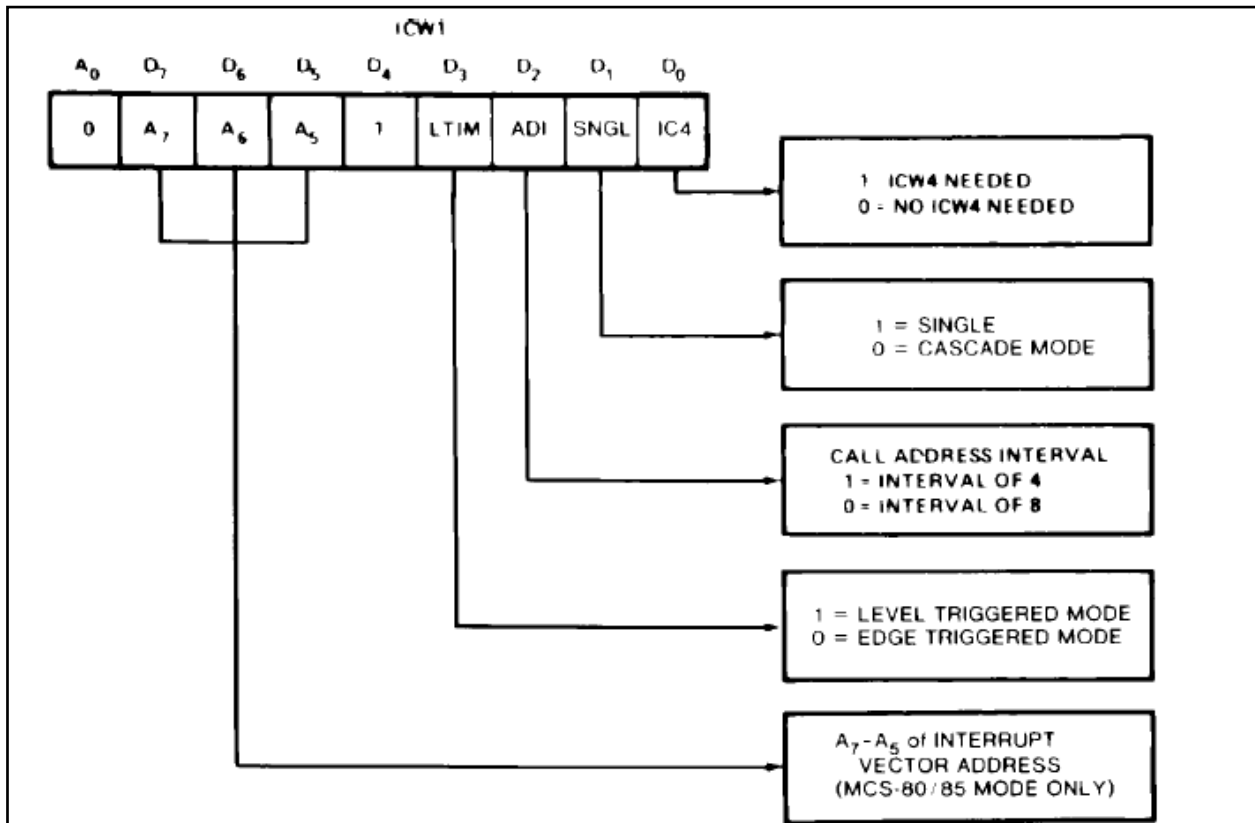
Before it starts functioning, the 8259A must be initialized by writing two to four command words into the respective command word registers. These are called as initialized command words.

- If A0= 0 and D4= 1, the control word is recognized as ICW1. It contains the control bits for edge/level triggered mode, single/cascade mode, call address interval and whether ICW4 is required or not.
- If A0=1, the control word is recognized as ICW2. The ICW2 stores details regarding interrupt vector addresses.
- ICW1 and ICW2 are compulsory command words in initialization sequence of 8259A as is evident from fig, while ICW3 and ICW4 are optional. The ICW3 is needed only when there are more than one 8259A in the system, cascading is used.
- The initialization sequence of 8259A is described in form of a flow chart in fig below.

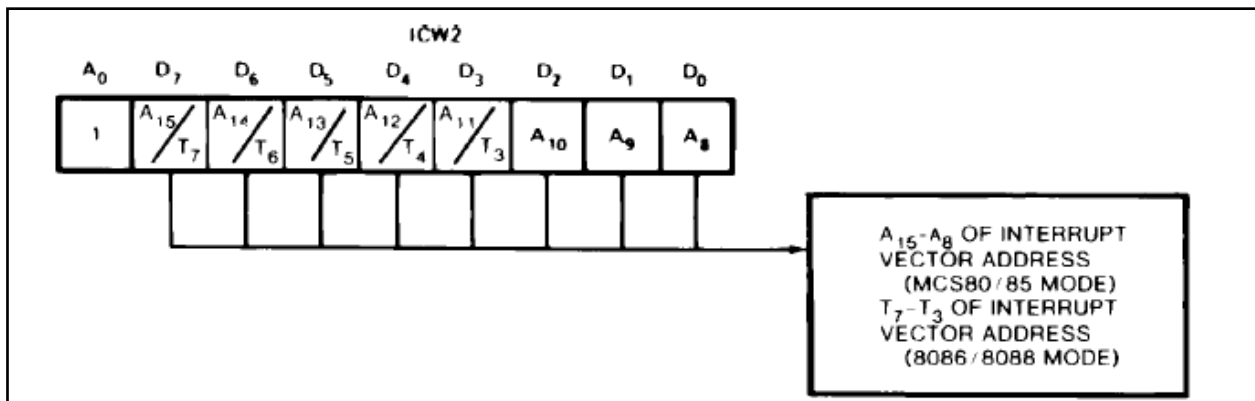


- The bit functions of the ICW1 and ICW2 are self explanatory as shown in fig below.

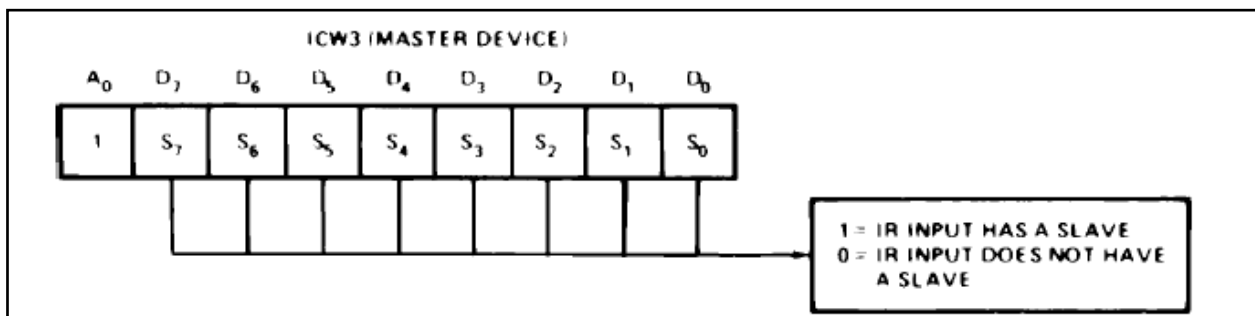
Initialization Command Word 1 (ICW 1)

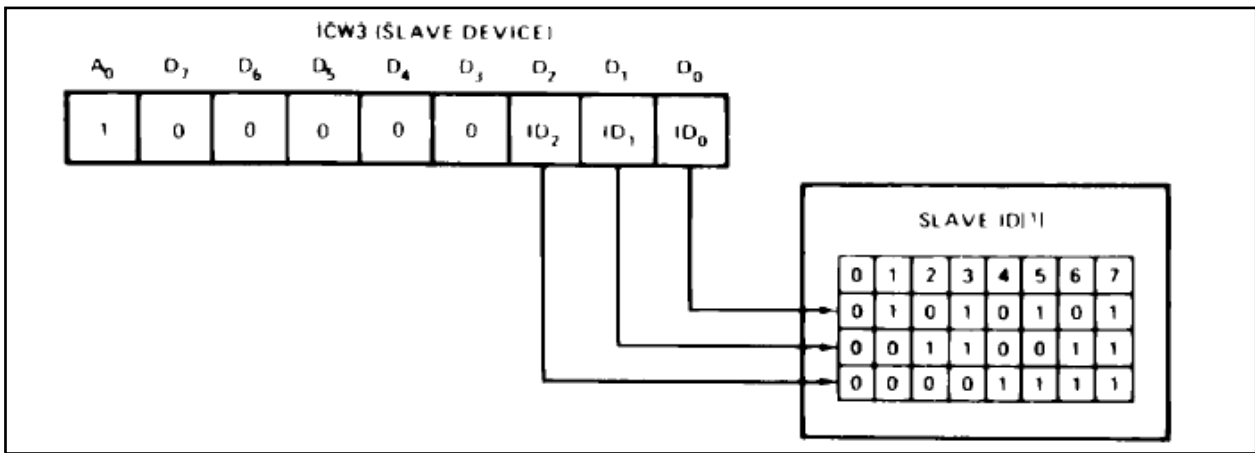


Initialization Command Word 2 (ICW 2)

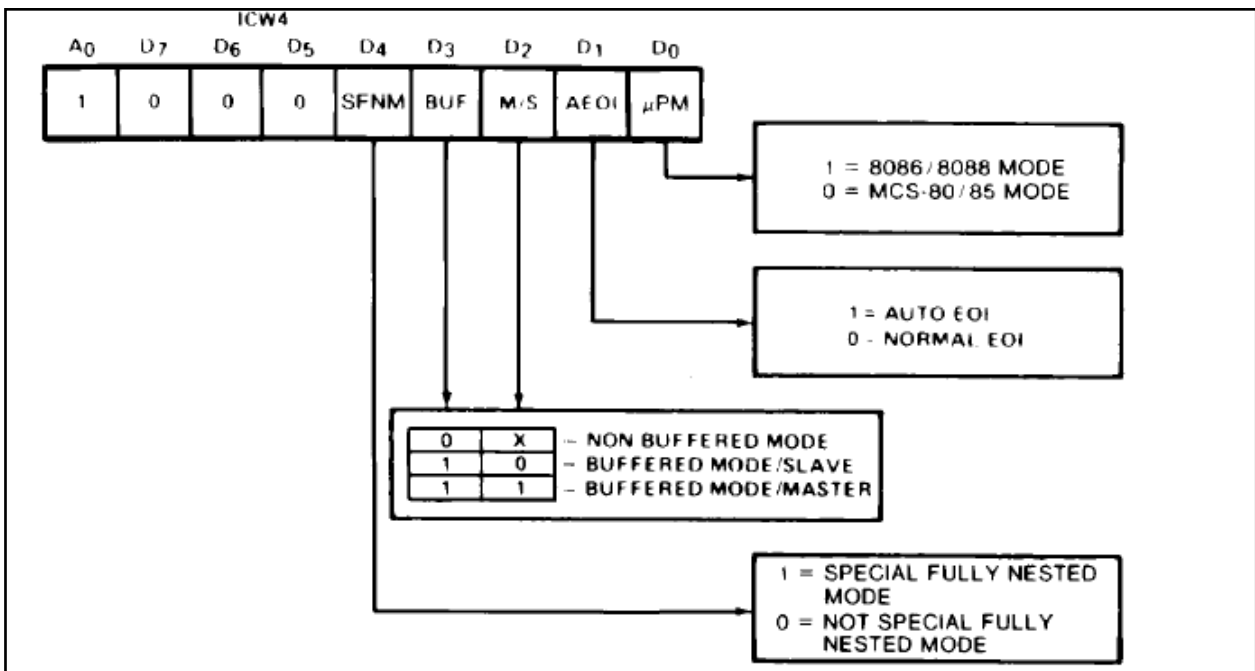


Initialization Command Word 3 (ICW 3)





Initialization Command Word 4 (ICW 4)



Operation Command Words (OCWs)

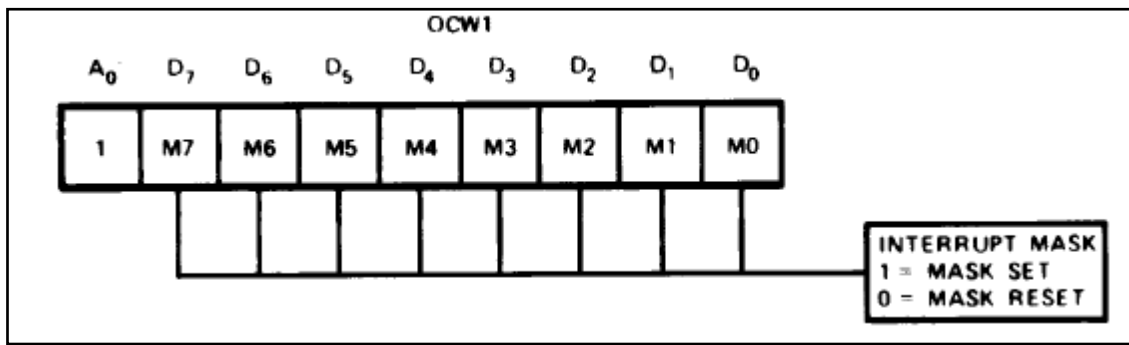
Once 8259A is initialized using the previously discussed command words for initialization, it is ready for its normal function, i.e. for accepting the interrupts but 8259A has its own way of handling the received interrupts called as modes of operation. These modes of operations can be selected by programming, i.e. writing three internal registers called as operation command words.

In the three operation command words OCW1, OCW2 and OCW3 every bit corresponds to some operational feature of the mode selected, except for a few bits those are either 1 or 0. The three operation command words are shown in fig with the bit selection details.

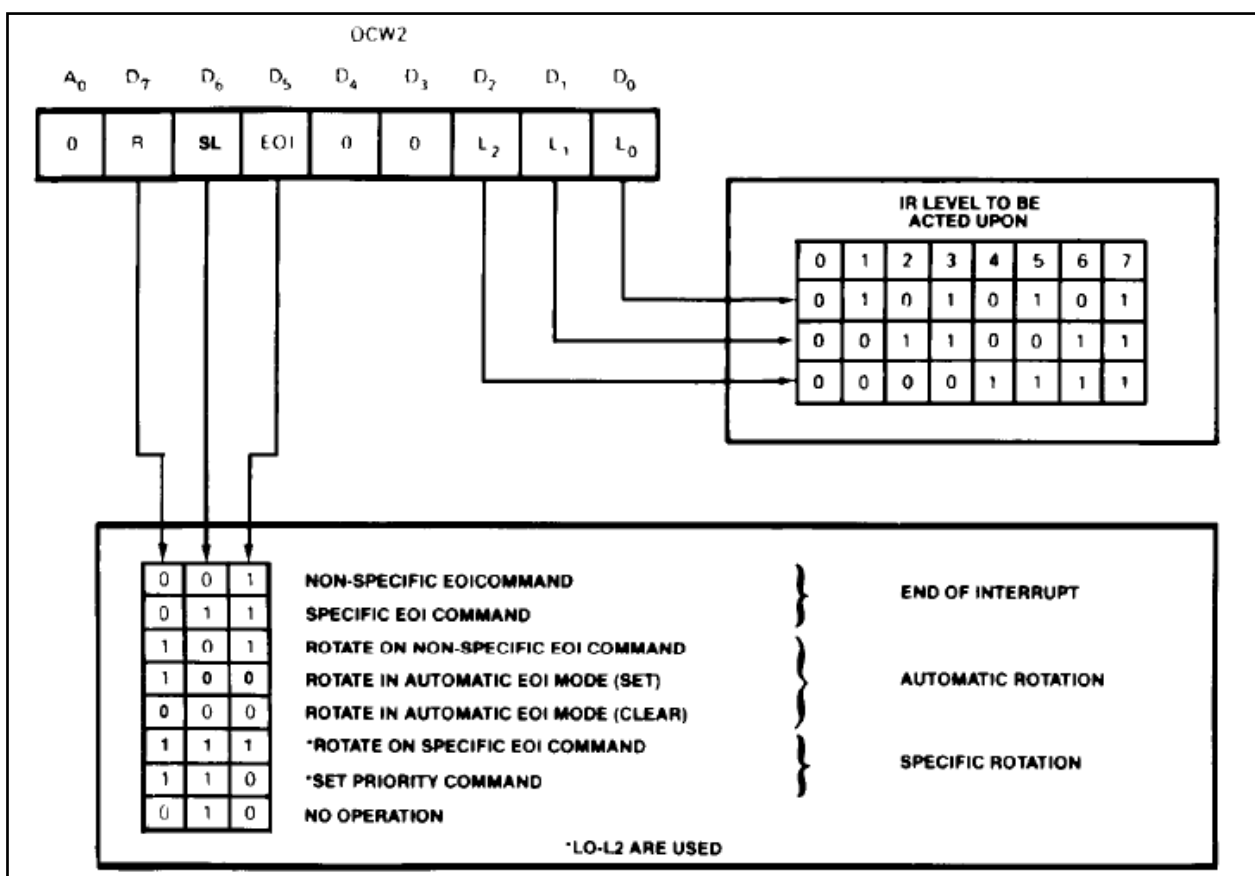
- OCW1 is used to mask the masked and if it is 0 the request is enabled.
- In OCW2 the three bits, R, SL and EOI control the end of interrupt, the rotate mode and their combinations as shown in fig below. The three bits L2, L1 and L0 in OCW2 determine the interrupt level to be selected for operation, if SL bit is active i.e. 1. The details of OCW2 are shown in fig.
- In operation command word 3 (OCW3), if the ESMM bit, i.e. enable special mask mode bit is set to 1, the SMM bit is neglected. If the SMM bit, i.e. special mask mode. When ESMM bit is 0 the SMM bit is neglected. If the SMM bit, i.e. special mask mode bit is 1, the 8259A will enter special mask mode provided ESMM=1. If ESMM=1 and SMM=0, the 8259A will return to the normal mask mode. The details of bits of OCW3 are given in fig along with their bit definitions.

The OCWs can be written into the 8259A anytime after initialization.

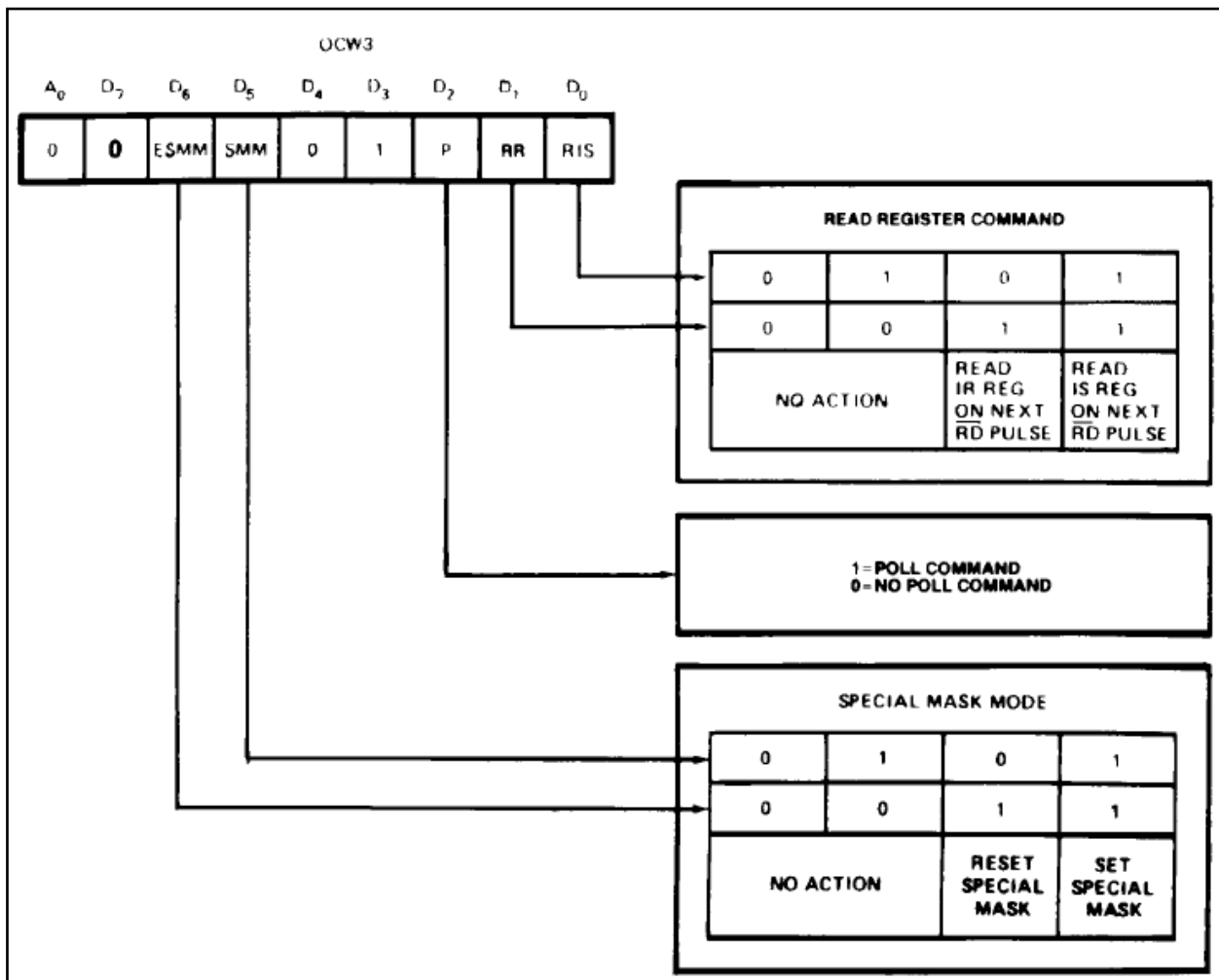
Operation Command Word 1 (OCW 1)



Operation Command Word 2 (OCW 2)



Operation Command Word 3 (OCW 3)



8253-PROGRAMMABLE INTERVAL TIMER/COUNTER (PIT)

NECESSITY AND INTRODUCTION

The 8253/54 solves one of most common problem in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in system software, the programmer configures the 8253/54 to match his requirements, initializes one of the counters of the 8253/54 with the desired quantity, then upon command the 8253/54 will count out the delay and interrupt the CPU when it has completed its tasks. It is easy to see that the software overhead is minimum and that multiple delays can be easily be maintained by assignment of priority levels.

The 8253/54 includes three identical 16 bit counters that can operate independently. To operate a counter, a 16-bit count is loaded in its register and, on command, it begins to decrement the count until it reaches 0. At the end of the count, it generates a pulse that can be used to interrupt the CPU. The counter can count either in binary or BCD. In addition, a count can be read by the CPU while the counter is decrementing. The 8254 is a superset of 8253. The functioning of these two ICs is almost similar along with the pin configuration. Only the differences are:

8253	8254
Operating frequency 0 - 2.6 MHz	Operating frequency 0 - 10 MHz
Uses N-MOS technology.	Uses H-MOS technology.
Read-Back command not available.	Read-Back command available

FEATURES OF 8253

- Compatible with all Intel and most other microprocessors.
- It has three independent 16-bit down counters.
- Each counter with a count rate up to 2.6 MHz
- Three counters are identical presettable, and can be programmed for either binary or BCD count.
- Counter can be programmed in six different modes.
- It is available in 24 pin DIP
- It uses N-MOS technology with +5v single power supply.

ARCHITECTURE OF 8253

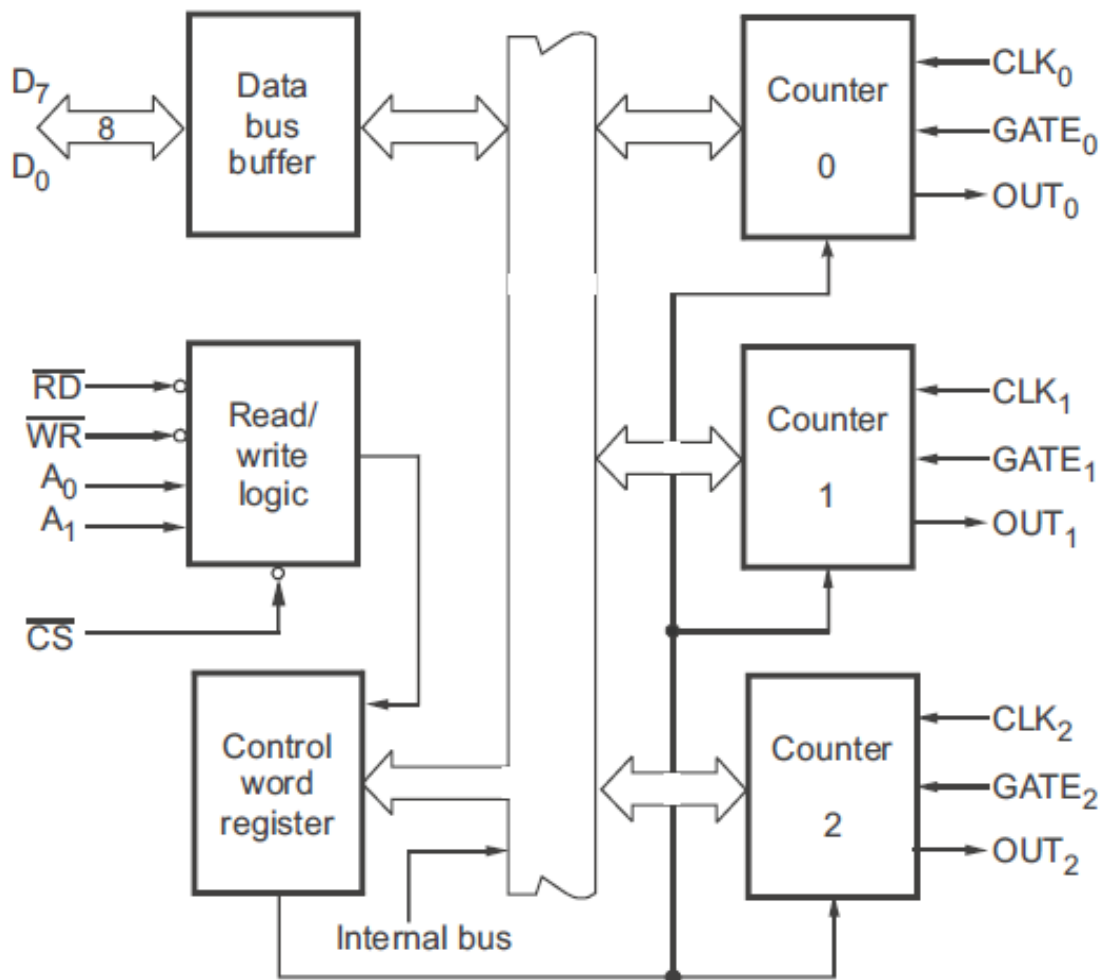


Fig. Internal block diagram of 8253

Fig. shows the block diagram of 8253. It includes three counters, a data bus buffer, Read/Write control logic, and a control register. Each counter has two input signals CLOCK and GATE and one output signal OUT.

Data Bus Buffer: This tri-state, bi-directional, 8-bit data bus is used to interface the 8253 to the system data bus. The Data bus buffer has three basic functions.

1. Programming the modes of 8253.
2. Loading the count registers.
3. Reading the count values.

Read/Write Logic: The Read/Write logic has five signals: RD, WR, CS and the address lines A0 and A1. Address lines A1 and A2 of the microprocessor are usually connected to lines A0 and A1 of the 8253, and

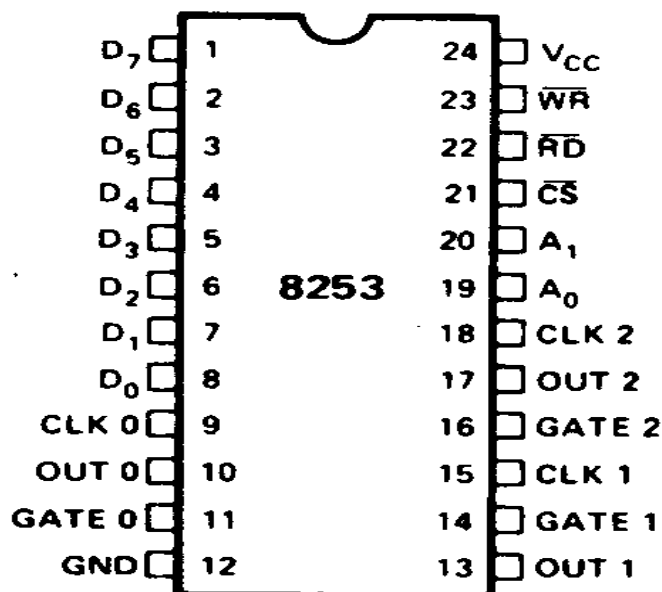
CS is tied to a decoded address. The control word register and counters are selected according to the signals on lines A0 and A1.

\overline{CS}	\overline{RD}	\overline{WR}	A ₁	A ₀	
0	1	0	0	0	Load Counter No. 0
0	1	0	0	1	Load Counter No. 1
0	1	0	1	0	Load Counter No. 2
0	1	0	1	1	Write Mode Word
0	0	1	0	0	Read Counter No. 0
0	0	1	0	1	Read Counter No. 1
0	0	1	1	0	Read Counter No. 2
0	0	1	1	1	No-Operation 3-State

Control Word Register: This register is accessed when lines A0 and A1 are at logic 1. It is used to write a command word which specifies the counter to be used (binary or BCD), its mode, and either a read or write operation.

Counters: These three functional blocks are identical in operation. Each counter consists of a single, 16 bit, pre-settable, down counter. The counter can operate in either binary or BCD and its input, gate and output are configured by the selection of modes stored in the control word register. The counters are fully independent.

PIN DIAGRAM OF 8253



D7-D0 (Data bus) : This tri-state, bi-directional, 8-bit data bus is used to interface the 8253 to the system data bus. The Data bus has three basic functions.

1. Programming the modes of 8253.
2. Loading the count registers.
3. Reading the count values.

CLK 0,1,2: Input clock signal for Counter-0, Counter-1 and Counter-2 respectively.

A1 & A0: These inputs are normally connected to the address bus. Their function is to select one of the three counters to be operated on and to address the control word register for mode selection.

A ₁	A ₀	Selection
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control word Register

\overline{CS} : A LOW on this input enables the 8253. No reading or writing of the chip will occur unless the device is selected.

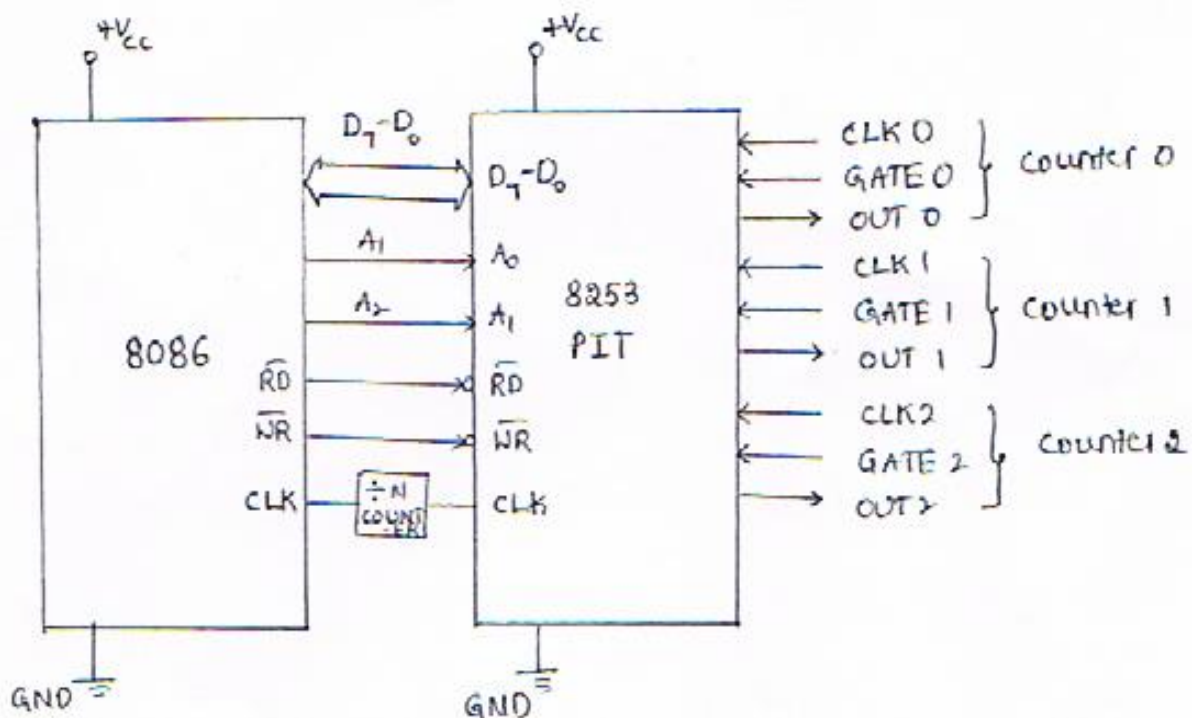
\overline{WR} : A LOW on this input informs the 8253 that the microprocessor is outputting data in the form of mode information or loading counter value.

\overline{RD} : A LOW on this input informs the 8253 that the microprocessor is inputting data in the form of counters value.

V_{cc}: +5v supply.

GND: Ground.

8253 INTERFACING WITH 8086



OPERATING MODES OF 8253-PIT

Each of the three counters of 8253 can be operated in one of the following six modes of operation.

1. Mode 0 (Interrupt on terminal count)
2. Mode 1 (Programmable monoshot)
3. Mode 2 (Rate generator)
4. Mode 3 (Square wave generator)
5. Mode 4 (Software triggered strobe)
6. Mode 5 (Hardware triggered strobe)

Mode 0 (Interrupt on terminal count): Mode 0 is used for the generation of accurate time delay under software control. In this mode, the counter will start counting from the initial COUNT value loaded into it, down to 0. Counting rate is equal to the input clock frequency. The OUT pin is set low after the Control Word is written, and counting starts one clock cycle after the COUNT programmed. OUT remains low until the counter reaches 0, at which point OUT will be set high until the counter is reloaded or the Control Word is written.

Mode 1 (Programmable monoshot): In this mode 8253 can be used as monostable multivibrator. GATE input is used as trigger input. OUT will be initially high. OUT will go low on the CLK pulse following a trigger to begin the one-shot pulse, and will remain low until the Counter reaches zero. OUT will then go high and remain high until the CLK pulse after the next trigger.

Mode 2 (Rate generator): In this mode, the device acts as a divide-by-n counter, which is commonly used to generate a real-time clock interrupt. Like other modes, counting process will start the next clock cycle after COUNT is sent. OUT will then remain high until the counter reaches 1, and will go low for one clock pulse. OUT will then go high again, and the whole process repeats itself.

The time between the high pulses depends on the preset count in the counter's register, and is calculated using the following formula: Value to be loaded into counter = $\frac{f_{input}}{f_{output}}$.

Mode 3 (Square wave generator): This mode is similar to mode 2. However, the duration of the high and low clock pulses of the output will be different from mode 2.

Suppose n is the number loaded into the counter, the output will be

- high for $\frac{n}{2}$ counts, and low for $\frac{n}{2}$ counts, if n is even.
- high for $\frac{n+1}{2}$ counts, and low for $\frac{n-1}{2}$ counts, if n is odd.

Mode 4 (Software triggered strobe): After Control Word and COUNT is loaded, the output will remain high until the counter reaches zero. The counter will then generate a low pulse for 1 clock cycle (a strobe) – after that the output will become high again.

Mode 5 (Hardware triggered strobe): This mode is similar to mode 4. However, the counting process is triggered by the GATE input.

After receiving the Control Word and COUNT, the output will be set high. Once the device detects a rising edge on the GATE input, it will start counting. When the counter reaches 0, the output will go low for one clock cycle – after that it will become high again, to repeat the cycle on the next rising edge of GATE.

PROGRAMMING THE 8253-PIT

Each counter of the 8253 is individually programmed by writing a control word into the Control Word Register. The Control Word Register format of 8253 is shown below.

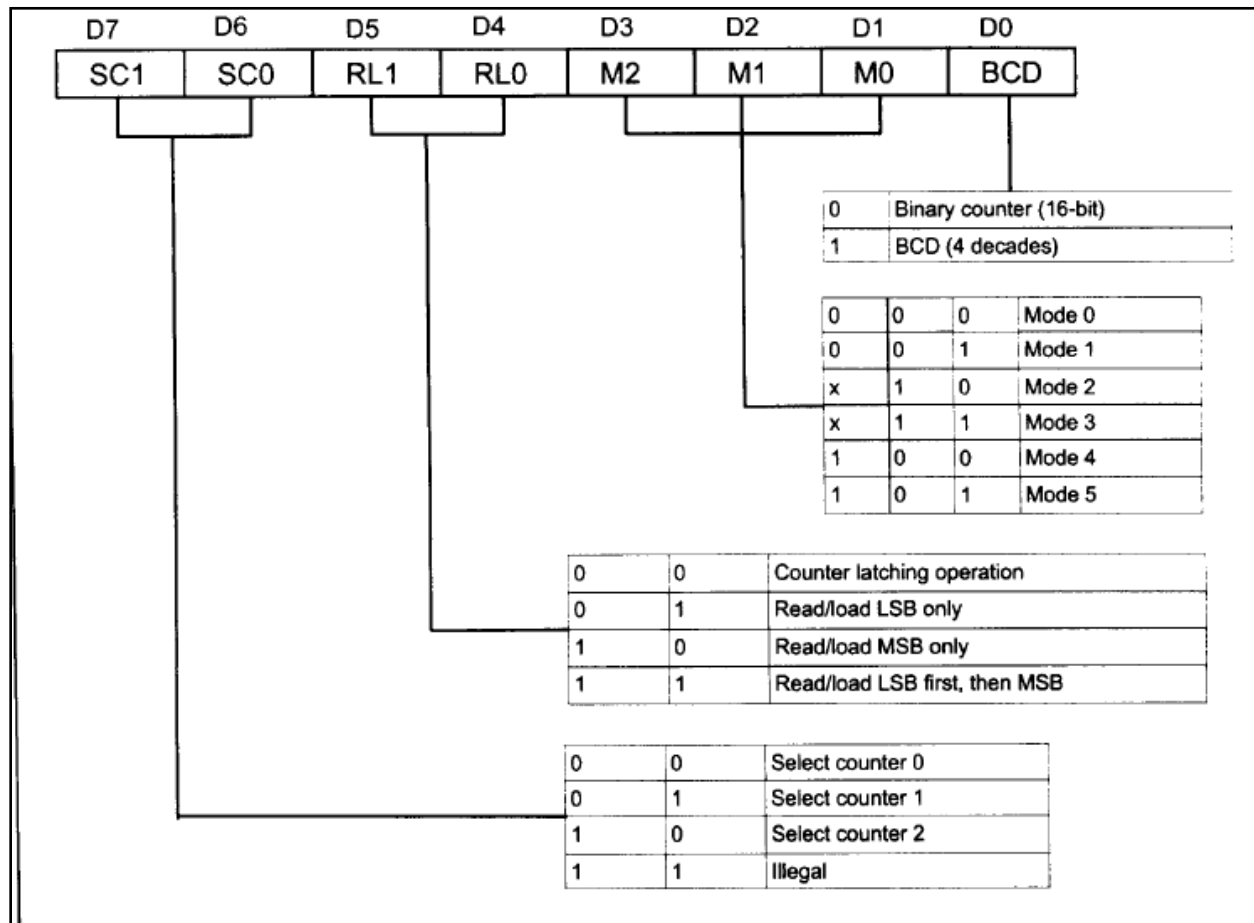


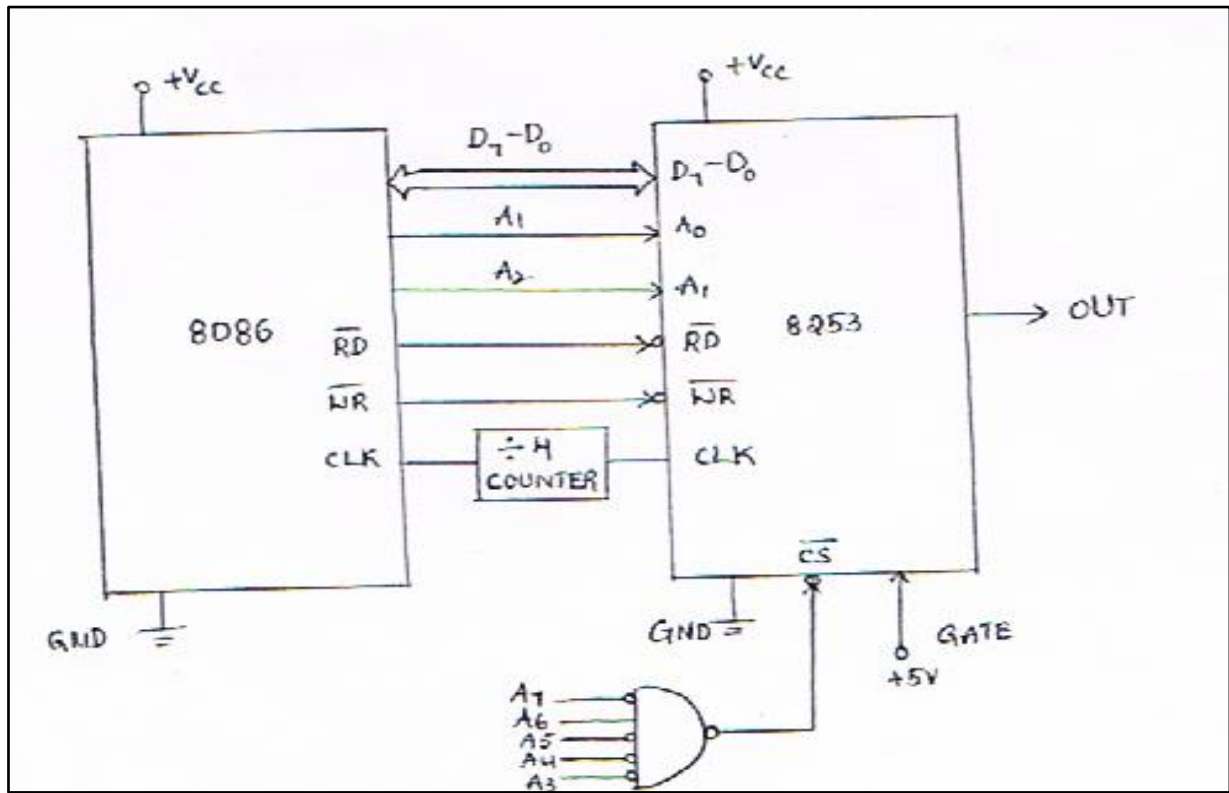
Fig. Control Word Format and Bit definitions

Example: Design a programmable interval timer using 8253 and 8086. Interface 8253 at an address 0040H for counter-0. The 8086 and 8253 run at 6 MHz and 1.5 MHz respectively. Write an ALP to generate a square wave of period 1ms.

Design: Neglecting the higher order address lines (A15-A8), the address of the counter-0 is 40H. Address lines A0 and A1 in 8253 are connected to the A1 and A2 of the 8086. These address lines are the selection lines for counters and control word register. The addresses of the counters are as follows.

A7	A6	A5	A4	A3	A2	A1	A0	Address
0	1	0	0	0	0	0	0	40H → Conter-0
0	1	0	0	0	0	1	0	42H → Counter-1
0	1	0	0	0	1	0	0	44H → Counter-2
0	1	0	0	0	1	1	0	46H → Control Word Register

Interfacing diagram



Control Word

0	0	1	1	0	1	1	1
---	---	---	---	---	---	---	---

Control word= 37H

The running frequency of 8253 is $f = 1.5 \text{ MHz}$

$$T = \frac{1}{f} = \frac{1}{1.5 \times 10^6} = 0.66 \mu\text{s}$$

$$N = \frac{\text{Required Time period}}{T}$$

$$N = \frac{1 \times 10^{-3}}{0.66 \times 10^{-6}} = 1500 \text{ states}$$

Program

```

ASSUME CS: CODE
CODE SEGMENT
ORG 3000H
MOV AL, 37H
OUT 46H, AL
MOV AL, 00
OUT 40H, AL
MOV AL, 15
OUT 40H, AL
INT 03H
CODE ENDS
END
    
```