US/GR BK/VLBA/

VLBA Technical Report No. 45
THE VLBA CORRELATOR
MAC and LTA SUB-SYSTEMS
VOLUME 2 of 2

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Chuck Broadwell

Ray Escoffier

January 1, 1999

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Volume 2 Section 1

Master Control Card Drawings

Drawing Number and/or Filename	Title	Nr of Sheets
56000L027 (L027D01.SCH - L027D04.SCH)	MCC Schematics	4
56000Z012 (Z012D01.LAY - Z012D02.LAY)	MCC IC Layouts	2
MCC.BLK	MCC Block Diagram	1
MCCTOP.PAL, PAL*.SCH (1F,2C,3B,4B,5B,5C,6B,6C,7B,8C, 9B,11C,13B,14G,15B,16E,16F, 16G,16I,19B,19F,20B,20F,21I, 22F,23B,23F,25F,28F,28H,29J,30C, 30E,32H)	PAL drawings	35

TEST FRAME GENERATOR

FRAME SEQUENCER

39 BIT RANDOM DATA GENERATOR

RAM DATA GENERATOR

FORMATER

HEADER DATA GENERATOR

FS4	FS3	FS2	FS1	FUNCTION
X	X	X	1	CWE FOR CRCC CHIP (VLBA)
X	1	X	X	CWE FOR CRCC CHIP (MKIII)
X	X	1	X	CRCC CHIP CLOCK ENA (VLBA)
1	X	X	X	CRCC CHIP CLOCK ENA (MKIII)

FS7	FS6	FS5	FUNCTION
1	X	X	DATA OUT
0	0	0	HEADER OUT
0	1	0	HEADER (MKIII), CRC (VLBA)
0	1	1	CRC OUT
1	0	1	EVEN PARITY OUT
1	0	1	ODD PARITY OUT
1	1	0	RESET SEQUENCER/CRC (VLBA)
1	1	1	RESET SEQUENCER/CRC (MK III)

uP1	uP0	FUNCTION
X	0	RANDOM DATA
X	1	RAM DATA
0	X	VLBA FRAME FORMAT
1	X	MARK III FRAME FORMAT

VLBA TAPE FORMAT

22,680 BITS 2.5 MSEC

22,500 TOTAL BITS 20,000 DATA BITS

HEADER | DATA FIELD

MK III TAPE FORMAT

22,500 BITS 2.5 MSEC

22,320 TOTAL BITS 19,840 DATA BITS

HEADER | DATA FIELD

REV	DATE	DESCRIPTION
REV A	1/24/90	PUT INVERTER IN WR11\ PUT IN FRAME CHART PUT IN 28H
REV B	7/06/92	MAKE 16I A 22V10 MAKE 6B A 22V10 ADD TEST, CYC ENA2 AND 3 CHANGE TEST FRAME PLL CHANGE 33A-34E TO 74ALS540
REV C	2/25/93	ADD upRESET\, R15 CHANGE 34A - WAS ALS541, NOW ALS540 ADD FS\0 TO 28F, 30F,30G, 31F, 31G

23F-6,5,2	23F DIVIDE	PLL FREQ	COMMENT
0,0,0	485	9.001600 MHZ	DEFAULT VLBA (0.00083% LOW)
0,0,1	487	9.038720 MHZ	SPARE
0,1,0	484	8.983040 MHZ	VLBA, SELF TEST (0.18% HIGH)
0,1,0	484	8.983040 MHZ	VLBA, NO SELF TEST (0.20% LOW)
0,1,1	486	9.020160 MHZ	VLBA, NO SELF TEST (0.20% HIGH)
1,0,0	482	8.945920 MHZ	VLBA, SELF TEST (0.23% LOW)
1,0,0	482	8.945920 MHZ	MKIII, NO SELF TEST (0.17% HIGH)
1,0,1	483	8.964480 MHZ	SPARE
1,1,0	480	8.908800 MHZ	MKIII, NO SELF TEST (0.24% LOW)
1,1,0	480	8.908800 MHZ	MKIII, SELF TEST (0.15% HIGH)
1,1,1	478	8.871680 MHZ	MKIII, SELF TEST (0.27% LOW)

VLBA CORRELATOR PROJECT

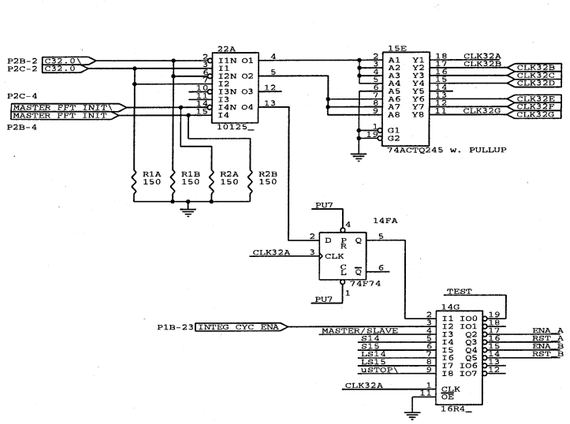
NATIONAL RADIO ASTRONOMY OBSERVATORY

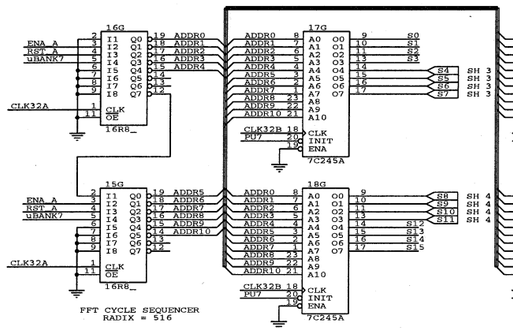
CHARLOTTESVILLE, VA

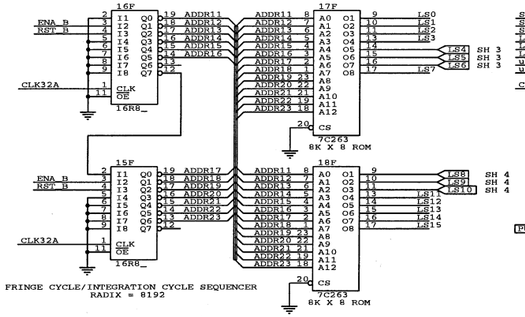
Title: MASTER CONTROL CARD

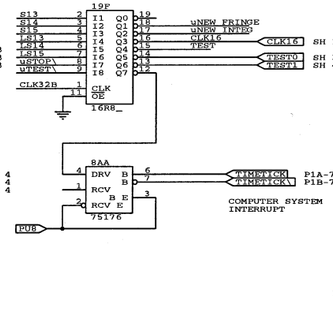
Size: D | Document Number: 56000L027 (L027D01.SCH) | REV: C

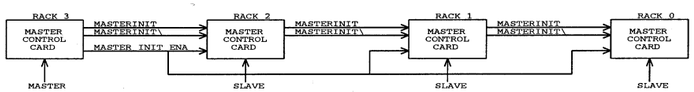
Date: December 30, 1998 | Sheet 1 of 4

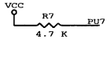


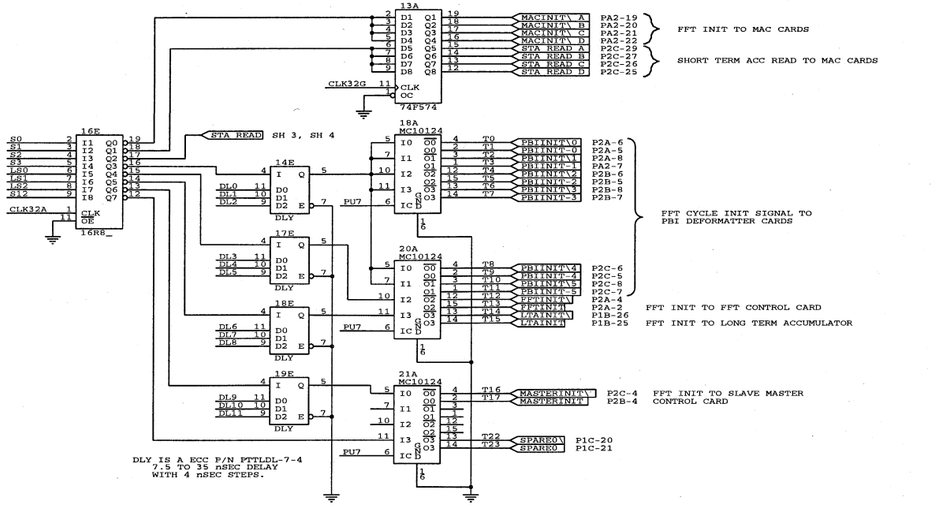




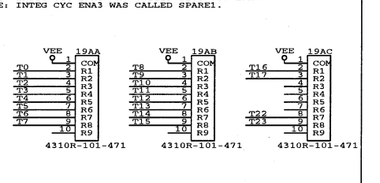




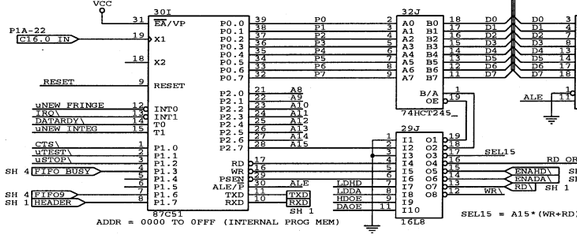




TEST	LS2-LS0	R12	S3-S0	FUNCTION
X	X	0	X	SHORT TERM ACC READ LOW
X	X	1	X	SHORT TERM ACC READ HIGH
X	0	X	0	IDLE
X	0	X	1	FFT INIT TO SLAVE CONTROL CARDS
X	0	X	2	FFT INIT TO DEFORMATER CARDS
X	0	X	3	FFT INIT TO FFT CONTROL CARD
X	0	X	4	FFT INIT TO MAC CARDS
X	0	X	5	FFT INIT TO LONG TERM ACCUMULATOR
X	1	X	1,2	FRINGE ENA TO DEFORMATER
X	1	X	3,4	FRINGE ENA TO FFT CONTROL CARD
X	1	X	5,6	TEST CYCLE ENA TO DEFORMATER CARD
X	1	X	7,8	TEST CYCLE ENA TO LONG TERM ACCUMULATOR
X	2	X	1,2	INTERGATION CYCLE ENA TO SLAVE CONTROL CARD
X	2	X	3,4	INTERGATION CYCLE ENA TO LONG TERM ACCUMULATOR
X	2	X	5,6	
X	2	X	7,8	

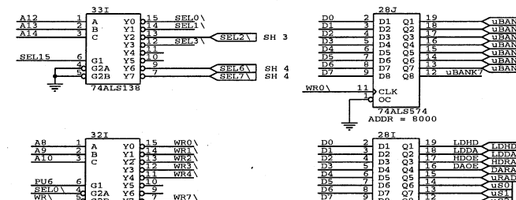


MICROPROCESSOR

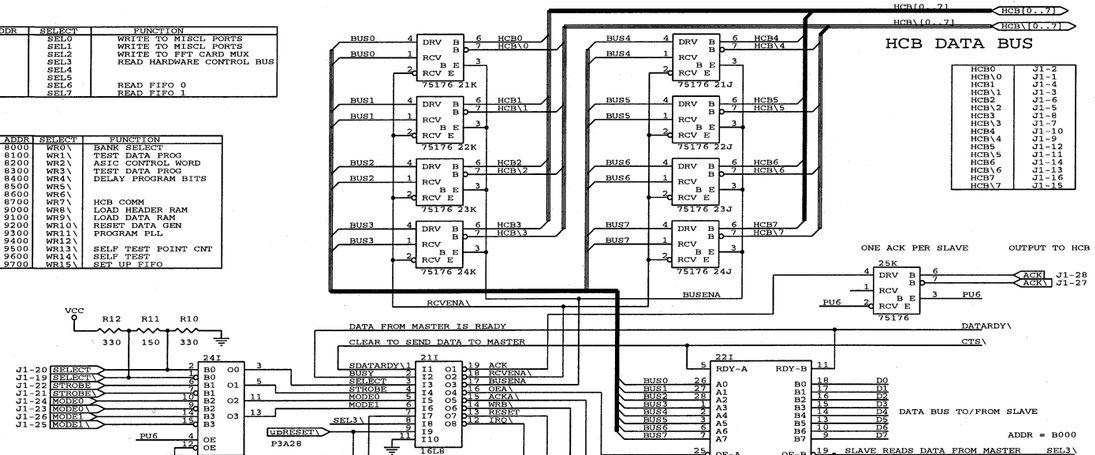


MICRO ADDR	SELECT	FUNCTION
8X00	SEL0	WRITE TO MISCL PORTS
9X00	SEL1	WRITE TO MISCL PORTS
A00X	SEL2	WRITE TO FFT CARD MUX
B000	SEL3	READ HARDWARE CONTROL BUS
	SEL4	
	SEL5	
E000	SEL6	READ FIFO 0
F000	SEL7	READ FIFO 1

ADDR	SELECT	FUNCTION
8000	WR0\	BANK SELECT
8100	WR1\	TEST DATA PROG
8200	WR2\	ASIC CONTROL WORD
8300	WR3\	TEST DATA PROG
8400	WR4\	DELAY PROGRAM BITS
8500	WR5\	
8600	WR6\	
8700	WR7\	HCB COMM
9000	WR8\	LOAD HEADER RAM
9100	WR9\	LOAD DATA RAM
9200	WR10\	RESET DATA GEN
9300	WR11\	PROGRAM PLL
9400	WR12\	
9500	WR13\	SELF TEST POINT CNT
9600	WR14\	SELF TEST
9700	WR15\	SET UP FIFO

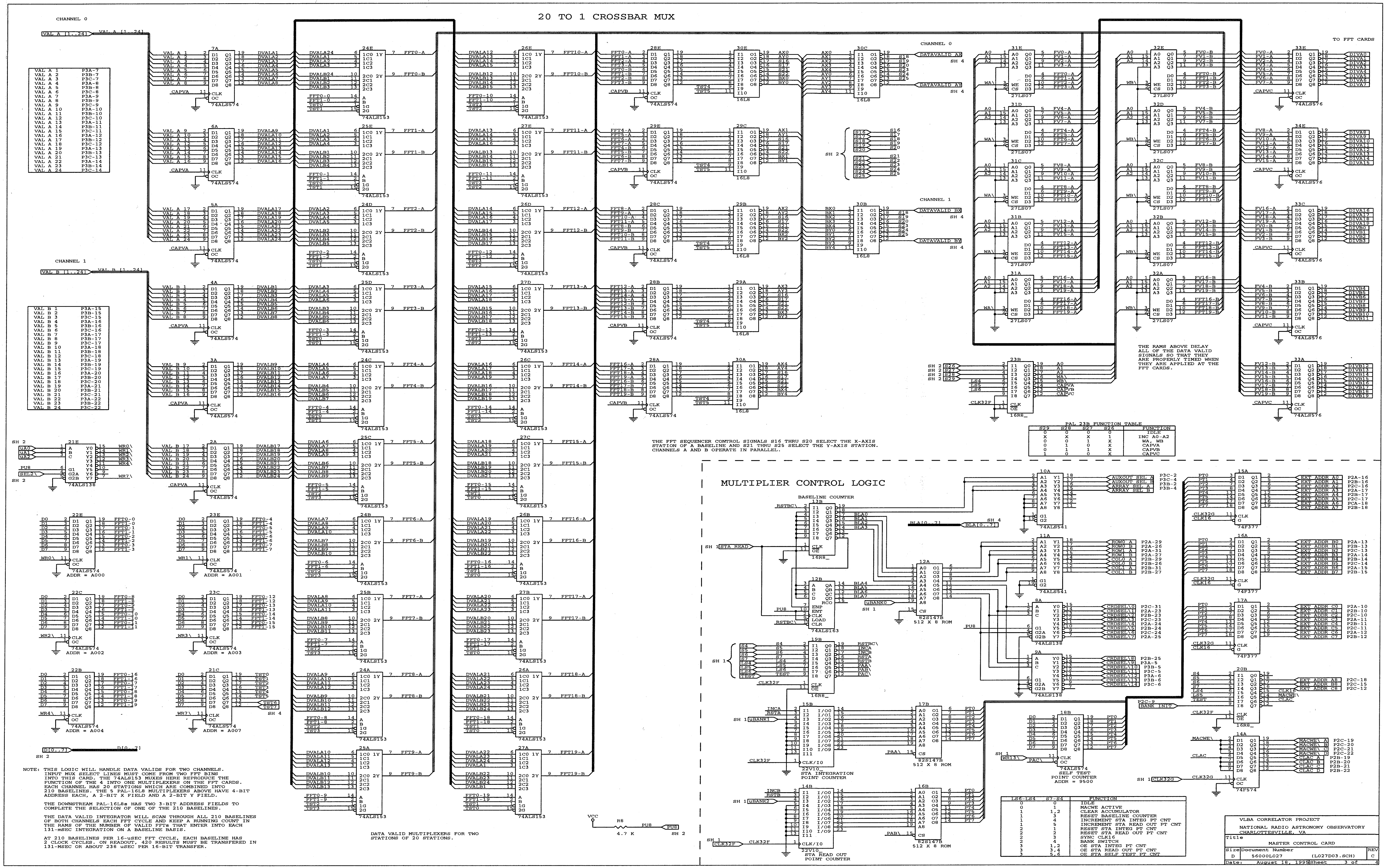


NOTE: C16.0 OFF GOES OFF THE CARD AND BACK AS C16.0 IN FOR THE 87C51.



SELECT	STROBE	MODE1	MODE0	FUNCTION	ACK	RCVENA\	BUSENA	OEA\	ACKA\	WRB\	RESET	IRQ\
0	X	0	0	ALLOW SLAVE TO ASSERT ATT'N	SDATARDY\	1	0	1	1	1	0	1
0	X	0	1	IDLE	1	1	0	1	1	1	0	1
0	X	1	0	IDLE	1	1	0	1	1	1	0	1
0	X	1	1	IDLE	1	1	0	1	1	1	0	1
1	⎍	0	0	MASTER SENDS IRQ TO SLAVE	1	1	1	1	STROBE\	1	0	STROBE\
1	⎍	0	1	MASTER WRITES TO SLAVE	BUSDY\	0	0	1	STROBE\	STROBE\	0	1
1	⎍	1	0	MASTER READS FROM SLAVE	SDATARDY\	1	STROBE\	STROBE\	STROBE\	1	0	1
1	⎍	1	1	MASTER RESETS SLAVE	1	1	0	1	STROBE\	1	STROBE	1

VLBA CORRELATOR PROJECT	
NATIONAL RADIO ASTRONOMY OBSERVATORY	
CHARLOTTESVILLE, VA	
Title	MASTER CONTROL CARD
Size	Document Number: 560001L027 (L027D02.SCH) — REV: C
D	
Date: November 19, 1997	Sheet 2 of 4



NOTE: THIS LOGIC WILL HANDLE DATA VALIDS FOR TWO CHANNELS. INPUT MUX SELECT LINES MUST COME FROM TWO FFT BINS INTO THIS CARD. THE 74ALS153 MUXES HERE REPRODUCE THE FUNCTION OF THE 4 INTO ONE MULTIPLEXERS ON THE FFT CARDS. EACH CHANNEL HAS 20 STATIONS WHICH ARE COMBINED INTO 210 BASELINES. THE 5 PAL-16L8 MULTIPLEXERS ABOVE HAVE 4-BIT ADDRESS EACH, A 2-BIT X FIELD AND A 2-BIT Y FIELD.

THE DOWNSTREAM PAL-16L8s HAS TWO 3-BIT ADDRESS FIELDS TO COMPLETE THE SELECTION OF ONE OF THE 210 BASELINES.

THE DATA VALID INTEGRATOR WILL SCAN THROUGH ALL 210 BASELINES OF BOTH CHANNELS EACH FFT CYCLE AND KEEP A RUNNING COUNT IN THE RAMS OF THE NUMBER OF VALID FFTs THAT ENTER INTO EACH 131-mSEC INTEGRATION ON A BASELINE BASIS.

AT 210 BASELINES PER 16-uSEC FFT CYCLE, EACH BASELINE HAS 2 CLOCK CYCLES. ON READOUT, 420 RESULTS MUST BE TRANSFERED IN 131-MSEC OR ABOUT 238 uSEC PER 16-BIT TRANSFER.

THE FFT SEQUENCER CONTROL SIGNALS S16 THRU S20 SELECT THE X-AXIS STATION OF A BASELINE AND S21 THRU S25 SELECT THE Y-AXIS STATION. CHANNELS A AND B OPERATE IN PARALLEL.

PAL 23B FUNCTION TABLE

S29	S28	S27	S26	FUNCTION
0	0	0	0	IDLE
X	X	X	1	INC A0-A2
0	0	1	X	WA, WB
0	1	0	X	CAPVA
0	1	1	X	CAPVB
1	0	0	X	CAPVC

LS6-LS4	S7-S4	FUNCTION
0	0	IDLE
0	1	MACWE ACTIVE
1	1,2	CLEAR ACCUMULATOR
1	3	RESET BASELINE COUNTER
1	4	INCREMENT STA INTEG PT CNT
1	5	INCREMENT STA READ OUT PT CNT
2	1	RESET STA INTEG PT CNT
2	2	RESET STA READ OUT PT CNT
2	3	SYNC CLK16
2	4	BANK SWITCH
3	1,2	OE STA INTEG PT CNT
3	3,4	OE STA READ OUT PT CNT
3	5,6	OE STA SELF TEST PT CNT

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Date: August 18, 1995 Sheet 3 of 4

BASELINE 210

BASELINE 211

BASELINE 212

NOTE: THE 22V10 BELOW PROVIDES A LATCH FOR THE TWO FIFO 9TH BITS.

COUNTS THRU 210 BASELINES AND 256 PULSAR GATE STATES AND KEEPS RUNNING SUMS OF DATA VALID IN A uPROC SELECTED BANK.

OUTPUT ENABLED DURING THE 4-BIT PAUSE BETWEEN FFT CYCLES FOR READOUT INTO LTA.

uPROC SELECTED READOUT ADDRESS FROM SECONDARY STORAGE BANK FOR SELF TEST.

CHANNEL A DATA VALID INTEGRATOR ARRAY 0 (OR 2 OR 4 OR 6)

CHANNEL B DATA VALID INTEGRATOR ARRAY 1 (OR 3 OR 5 OR 7)

CHANNEL A PULSAR GATE INTEGRATOR FFT PIPELINE 0 (OR 4)

CHANNEL C PULSAR GATE INTEGRATOR FFT PIPELINE 2 (OR 6)

CHANNEL B PULSAR GATE INTEGRATOR FFT PIPELINE 1 (OR 5)

CHANNEL D PULSAR GATE INTEGRATOR FFT PIPELINE 3 (OR 7)

DATA VALID DELAY LINE

PULSAR GATE DELAY LINE

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Date: July 28, 1998	Sheet 4 of 4

32 MHZ CLOCK RUNS

Z012D02.LAY

WIREWRAP
PIN 140094

WIREWRAP
PIN 001094

J2

J1

11.01 inches

PIN 1

RX
CX

WIREWRAP
PIN 001001

WIREWRAP
PIN 140001

14.43 inches

9U x 280 mm EUROCARD

P3

P2

P1

SEE NRAO DRAWING # 56000M002 FOR
MECHANICAL DETAILS OF CARD.

THIS SKETCH DETAILS THE APPROXIMATE
LOCATIONS OF ALL COMPONENTS.

ALL COMPONENTS WILL BE ON GRID UNLESS OTHERWISE NOTED.

REV B	2/25/93	ADDED R15

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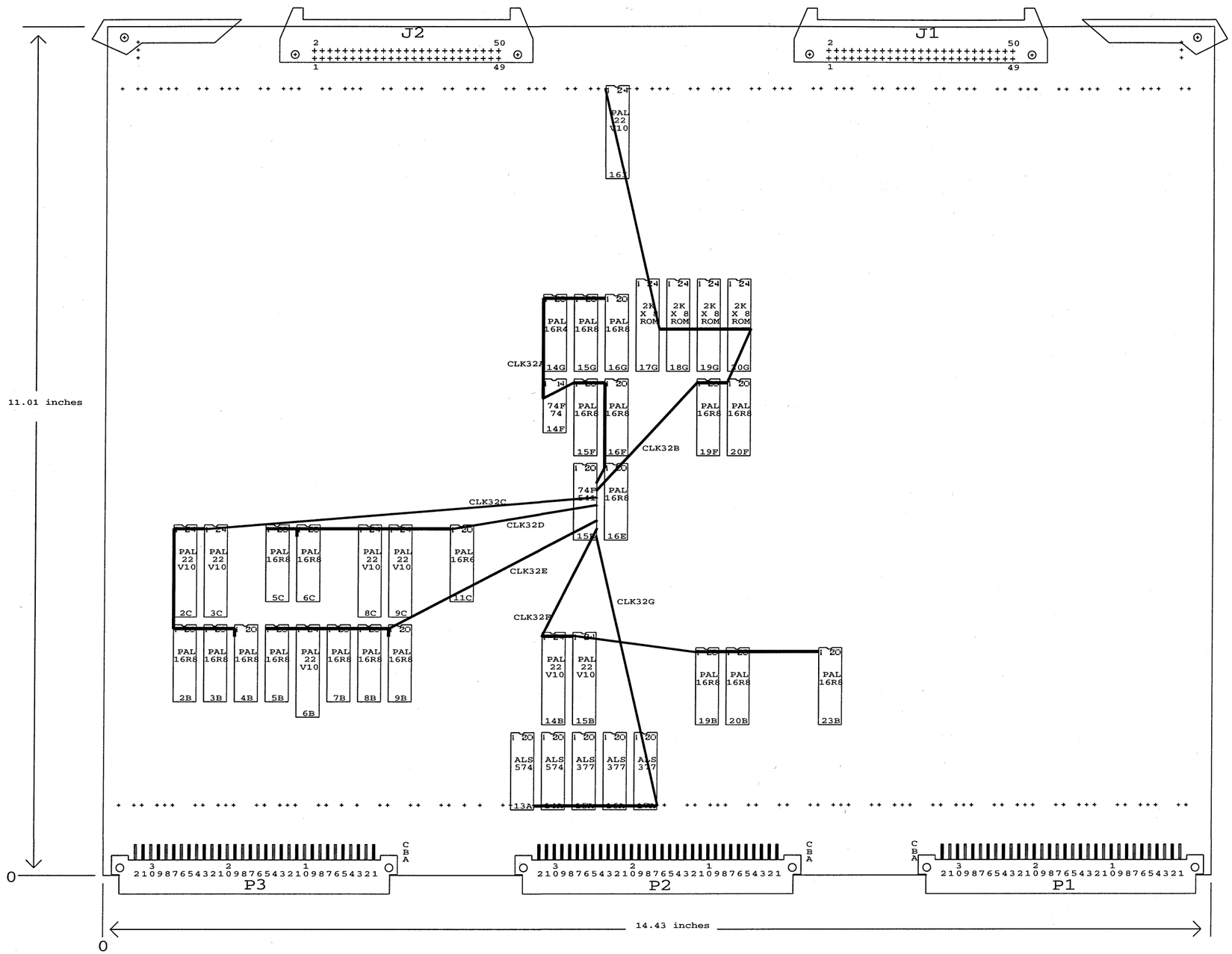
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: MASTER CONTROL CARD IC LAYOUT

Size	Document Number	REV
C	56000Z012 (Z012D01.LAY)	B

Date: November 19, 1997 Sheet 1 of 2

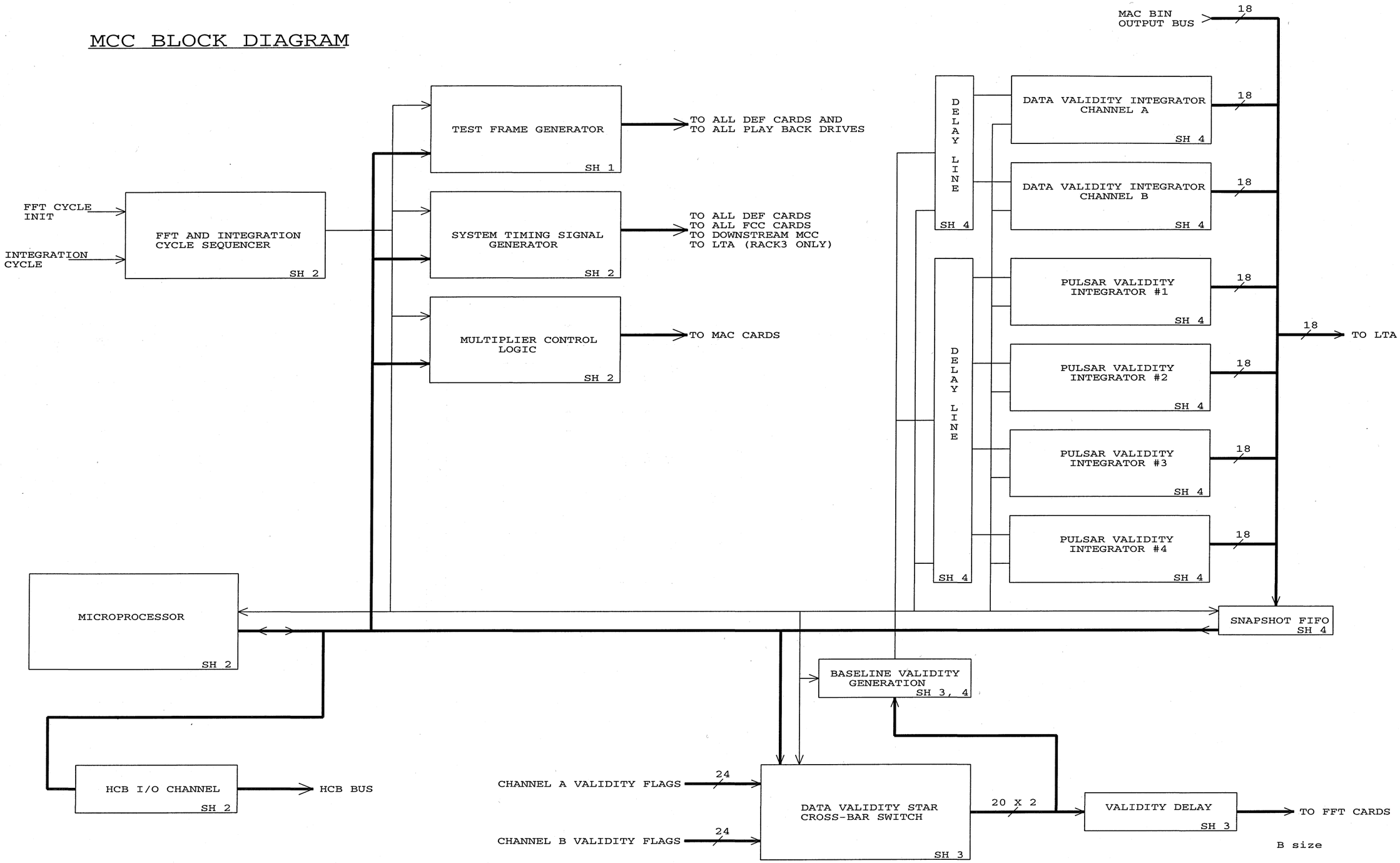


32 MHz CLOCK DISTR

9U x 280 mm EUROCARD

VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title MASTER CONTROL CARD IC LAYOUT		
Size C	Document Number 560002012 (Z012D02.LAY)	REV
Date: July 19, 1991	Sheet 2 of 2	

MCC BLOCK DIAGRAM



B size

MCC.BLK

15 BIT DATA VALID ADDER
SHEET 1 — PAL1F.ABL, PAL2F.ABL
PAL1F.SCH — PALS 1F,2F,2G, 3F,4F,4G 5F,6F,6G, 7F,8F,8G 9F,10F,10G, 11F,12F,12G

VALIDITY STORAGE ADR CNTRS
SHEET 2 — PAL2C.ABL, PAL3C.ABL
PAL2C.SCH — PALS 2C AND 3C

DATA VALID DELAY LINE CONTROL
SHEET 3 — PAL2B.ABL, PAL3B.ABL
PAL3B.SCH — PALS 3B AND 2B

DECODER PAL
SHEET 4 — PAL4B.ABL
PAL4B.SCH

DECODER PAL
SHEET 5 — PAL5B.ABL
PAL5B.SCH

DATA VALID INTEGRATOR BANK SEL
SHEET 6 — PAL5C.ABL
PAL5C.SCH

DECODER PAL
SHEET 7 — PAL6B.ABL
PAL6B.SCH

DECODER PAL
SHEET 8 — PAL6C.ABL
PAL6C.SCH

PULSAR GATE DELAY LINE CONTROL
SHEET 9 — PAL7B.ABL, PAL8B.ABL
PAL7B.SCH — PALS 7B AND 8B

VALIDITY STORAGE ADR CNTRS
SHEET 10 — PAL8C.ABL
PAL8C.SCH — PALS 8C AND 9C

PULSAR GATE DELAY LINE CONTROL
SHEET 11 — PAL9B.ABL
PAL9B.SCH

DECODER PAL
SHEET 12 — PAL11C.ABL
PAL11C.SCH

BASELINE COUNTER PAL
SHEET 13 — PAL13B.ABL
PAL13B.SCH

SEQUENCER COUNTER CONTROL PAL
SHEET 14 — PAL14G.ABL
PAL14G.SCH

8-BIT COUNTER PAL
SHEET 15 — PAL15B.ABL
PAL15B.SCH — PALS 15B AND 14B

FFT CYCLE CONTROL SIGNAL DECODER
SHEET 16 — PAL16E.ABL
PAL16E.SCH

FRINGE & INT CYCLE SEQ ADR CNTR
SHEET 17 — PAL15F.ABL, PAL16F.ABL
PAL16F.SCH — PALS 16F AND 15F

FFT CYCLE SEQ ADR CNTR
SHEET 18 — PAL15G.ABL, PAL16G.ABL
PAL16G.SCH — PALS 16G AND 15G

FIFO CONTROL PAL
SHEET 19 — PAL16I.ABL
PAL16I.SCH

DECODER PAL
SHEET 20 — PAL19B.ABL
PAL19B.SCH

TIMING SIGNAL DECODER PAL
SHEET 21 — PAL19F.ABL
PAL19F.SCH

DECODER PAL
SHEET 22 — PAL20B.ABL
PAL20B.SCH

FRINGE AND INT CYCLE DECODE PAL
SHEET 23 — PAL20F.ABL
PAL20F.SCH

HCB CONTROLLER PAL
SHEET 24 — PAL21I.ABL
PAL21I.SCH

PHASE LOCK LOOP REFERENCE DIVIDER
SHEET 25 — PAL22F.ABL
PAL22F.SCH

DATA VALID DELAY RAM CONTROL PAL
SHEET 26 — PAL23B.ABL
PAL23B.SCH

PHASE LOCK LOOP VARIABLE RADIX CNTR
SHEET 27 — PAL23F.ABL
PAL23F.SCH

TEST FRAME FORMATTER PAL
SHEET 28 — PAL25F.ABL
PAL25F.SCH

HEADER RAM ADDRESS COUNTER
SHEET 29 — PAL28F.ABL
PAL28F.SCH

CRC CONTROL SIGNAL GENERATOR PAL
SHEET 30 — PAL28H.ABL
PAL28H.SCH

MISC UP LOGIC PAL
SHEET 31 — PAL29J.ABL
PAL29J.SCH

DUAL 5 INTO 1 MUX
SHEET 32 — PAL30C.ABL
PAL30C.SCH — PALS 30C AND 30B

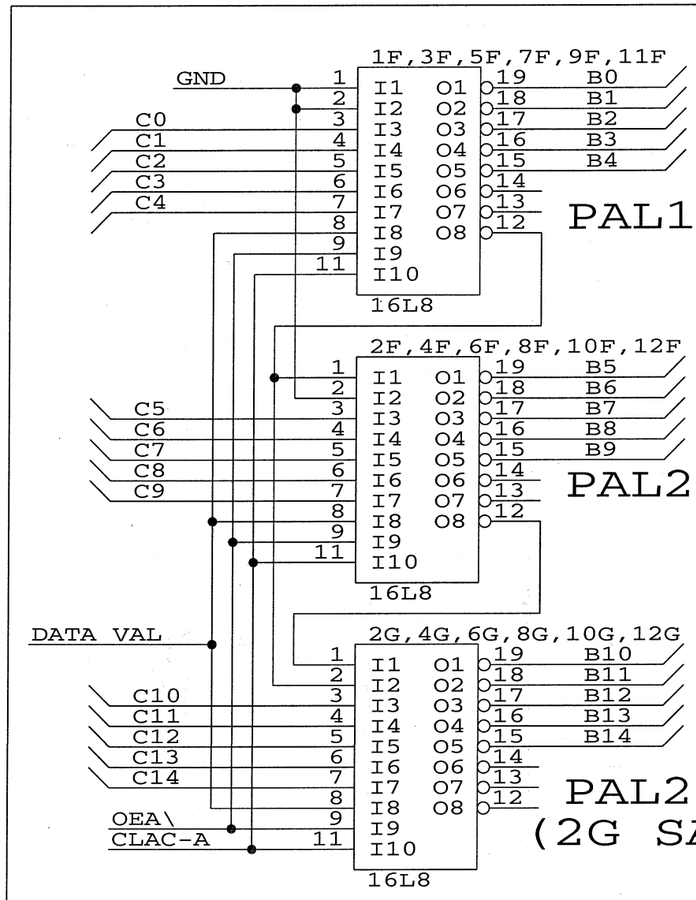
DUAL 4 INTO 1 MUX
SHEET 33 — PAL30E.ABL
PAL30E.SCH — PALS 30E, 29A, 29B, 29C AND 30A

RANDOM DATA GENERATOR PAL
SHEET 34 — PAL32H.ABL
PAL32H.SCH

63 PHYSICAL PALS
ON MCC

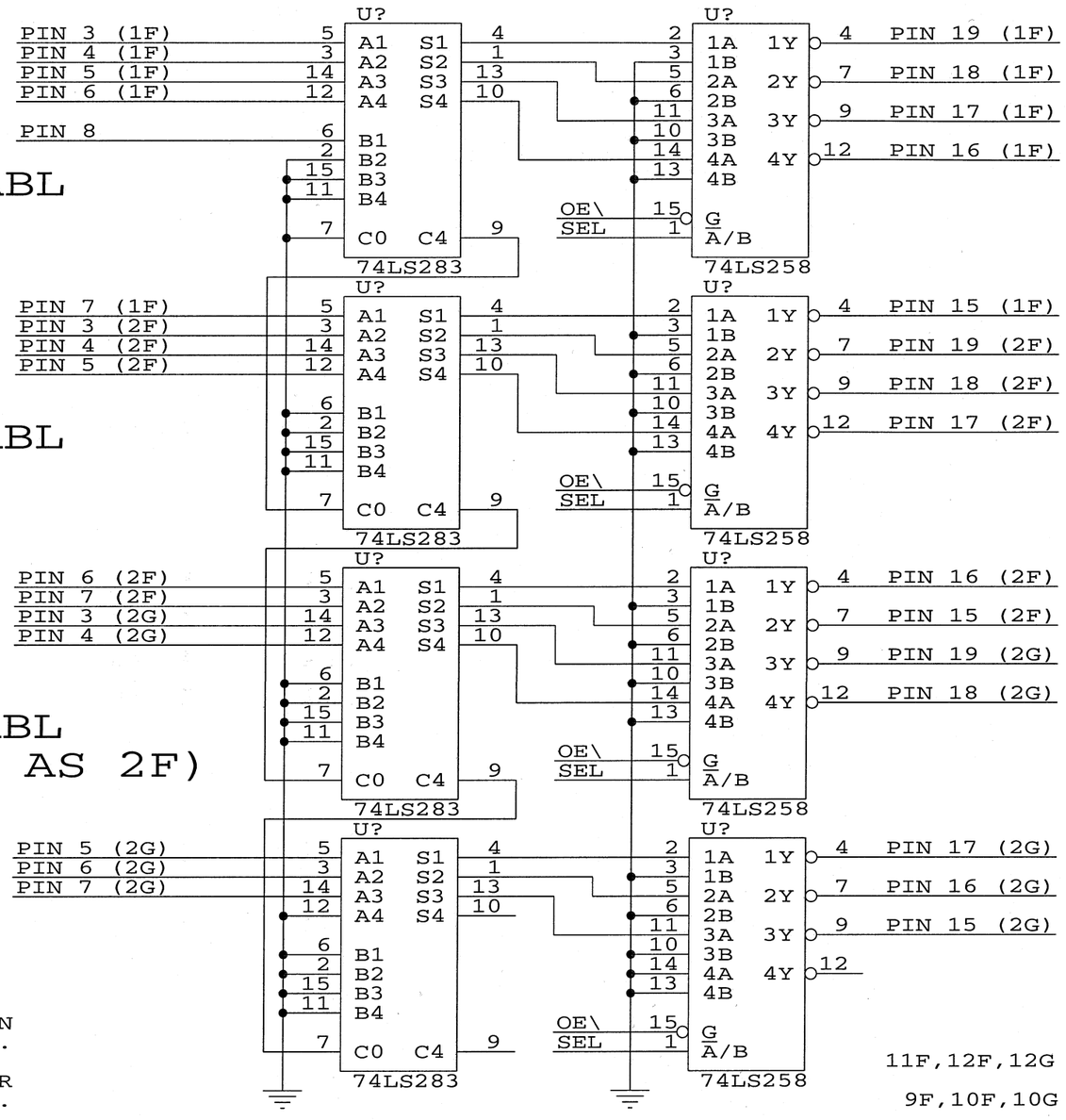
40 DISTINCT ABEL SOURCE FILES

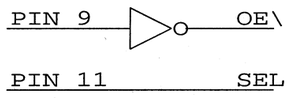
Title: MCC PALS		
Size: B	Document Number: MCCTOP.PAL	REV
Date: December 30, 1998	Sheet 1 of 1	



PALS 1F, 2F, AND 2G
15-BIT DATA VALID ADDER

THESE PALS TOGETHER FORM A 15-BIT ADDER.
A RUNNING SUM ON C(0..14) IS READ FROM
THE RAMS AND A ONE OR ZERO (ON DATA VAL)
IS ADDED TO IT. THE NEW RUNNING SUM IS WRITTEN
BACK INTO THE RAM ON THE 3-STATE BUS B(0..14).
NOTE THAT THE OUTPUT ENABLE LINE OEA\ IS HIGH
TRUE. IT WILL OUTPUT ENABLE THE 1F/2F/2G ADDER
WHEN HIGH AND OUTPUT ENABLE THE RAMS WHEN LOW.

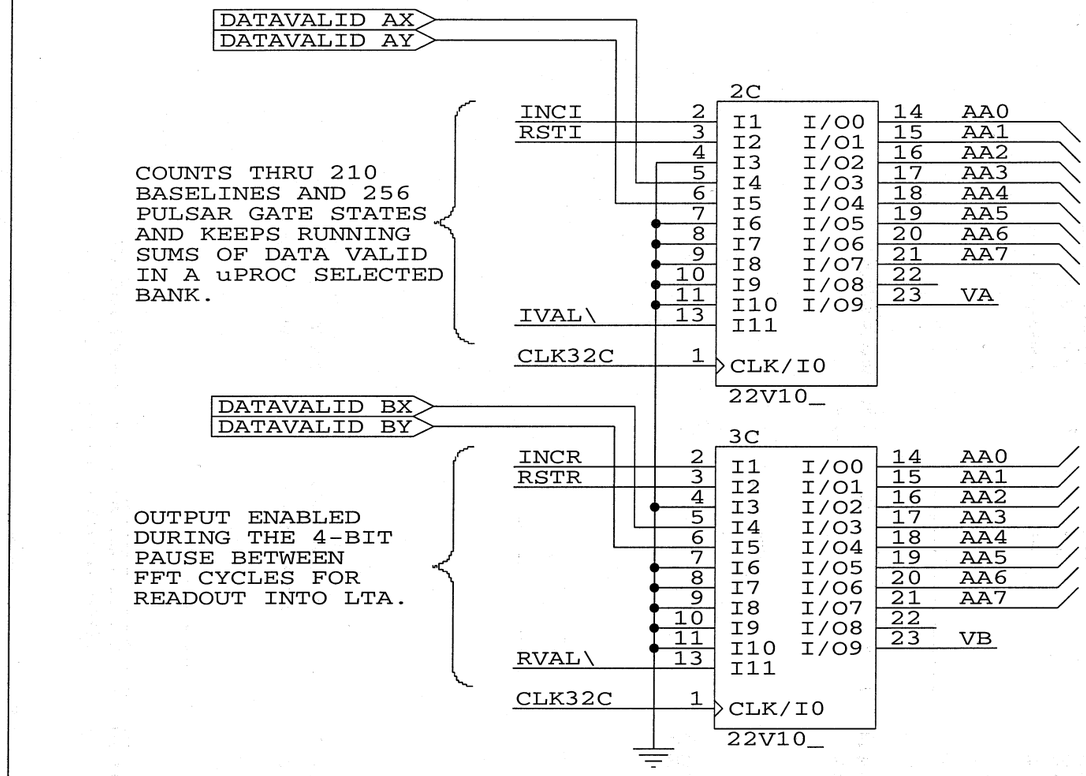




11F,12F,12G
9F,10F,10G
7F, 8F, 8G
5F, 6F, 6G
3F, 4F, 4G

Title
15 BIT DATA VALID ADDER: PALS 1F, 2F, 2G

Size	Document Number	REV
A	PAL1F.SCH	
Date: December 30, 1998	Sheet 1 of 34	



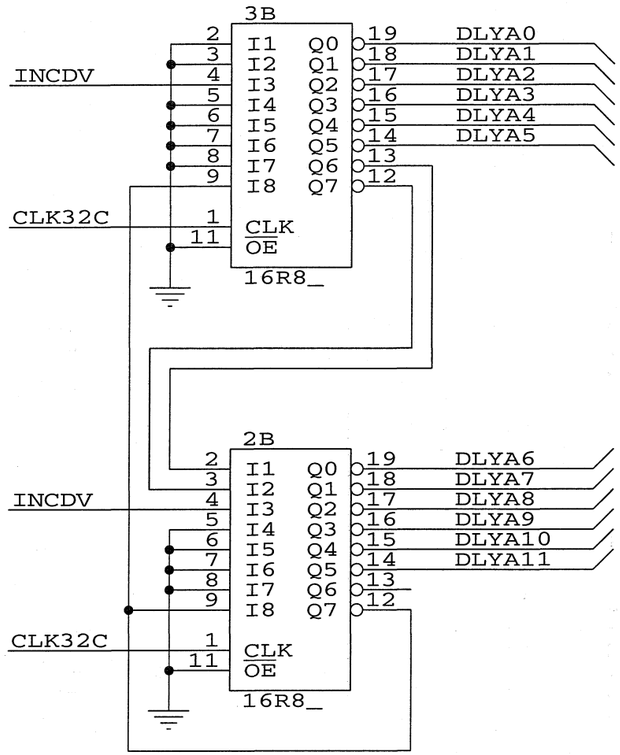
*** IN PAL 2C THIS IS PIN 2.
IN PAL 3C THE 16-MHz IS INTERNALLY GENERATED BUT SYNCHRONIZED BY PIN 2.

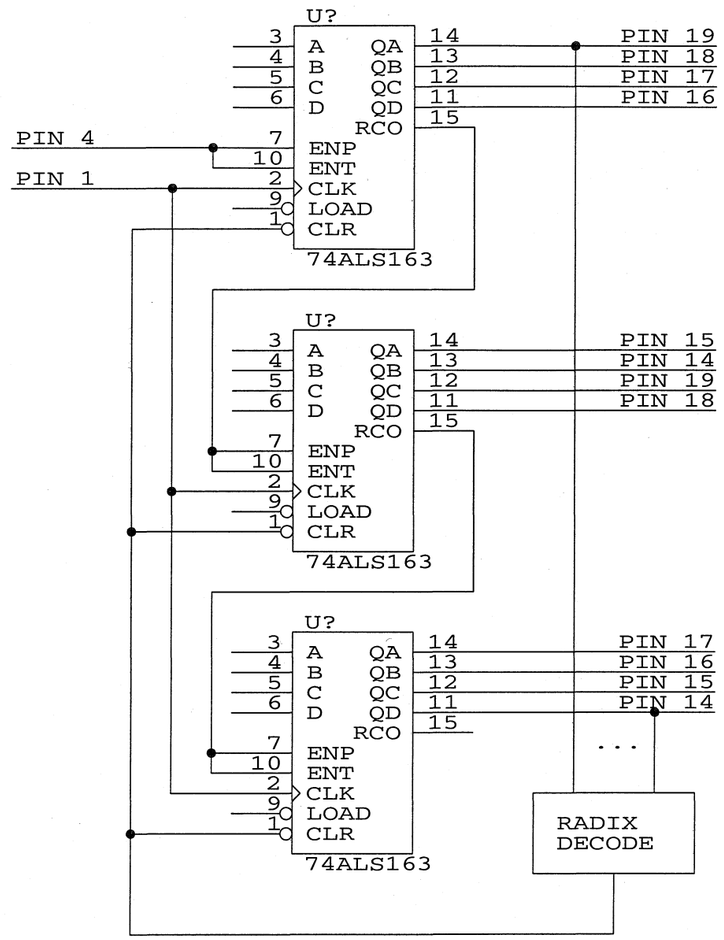
PALS 2C AND 3C
VALIDITY STORAGE ADDRESS COUNTERS

THESE 2 PALS GENERATE THE ADDRESS FOR THE DATA VALID INTERGATION RAMS. THEY ARE ALMOST IDENTICAL AND DIFFER ONLY IN THE AUX FUNCTION OF LOGICALLY ANDING THE 2 STATION DATA VALIDS TO OBTAIN A BASELINE DATA VALID.

```
COUNT = [CNT7,CNT6,CNT5,CNT4,CNT3,CNT2,CNT1,CNT0]        ;

COUNT       :=     COUNT        & !INC   &   !RST
                # (COUNT + 1)   &  INC   &   !RST          ;

CNT7.OE      =     OE                                     ;
CNT6.OE      =     OE                                     ;
CNT5.OE      =     OE                                     ;
CNT4.OE      =     OE                                     ;
CNT3.OE      =     OE                                     ;
CNT2.OE      =     OE                                     ;
CNT1.OE      =     OE                                     ;
CNT0.OE      =     OE                                     ;

VAL_A       :=     DV_AX  &  DV_AY    &    INC
                #   VAL_A  &                !INC          ;
```

Title: VALIDITY STORAGE ADR CNTRS: PALS 2C AND 3C		
Size: A	Document Number: PAL2C.SCH	REV:
Date: May 7, 1997	Sheet 2 of 34	

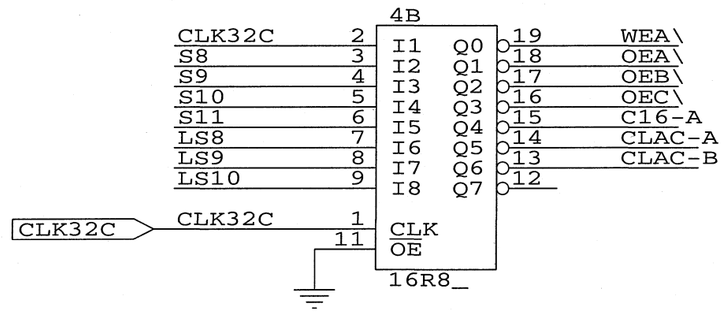




PALS 3B AND 2B
DATA VALID DELAY LINE CONTROL PALS

THESE PALS FORM A RADIX ???? COUNTER TO SET THE DELAY BETWEEN THE DEFORMATER DATA VALID OUTPUT LINES AND THE DATA VALID INTEGRATION INPUT. THIS DELAY MUST MATCH THE THRU PUT OF THE MAC SYSTEM.

Title: DATA VALID DELAY LINE CTRL: PALS 3B AND 2B		
Size: A	Document Number: PAL3B.SCH	REV:
Date: May 7, 1997	Sheet 3 of 34	

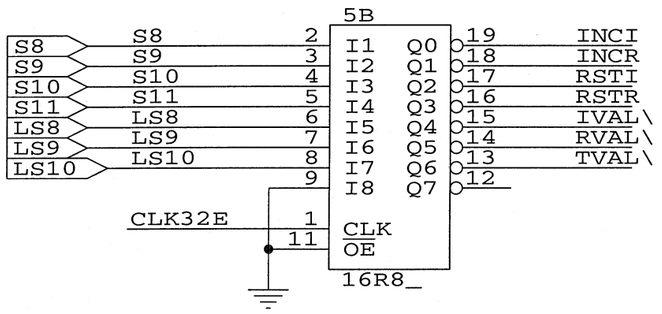


PAL 4B
DECODER PAL

THIS PAL DECODES STATES OF THE FFT CYCLE AND INTEGRATION CYCLE SEQUENCERS TO PROVIDE TIMING SIGNALS FOR THE DATA VALID INTEGRATOR. THE EQUATIONS BELOW GIVE THE PAL FUNCTIONS.

```
MODE   = [S11,S10,S9,S8]          ;
LMODE  = [LS10,LS9,LS8]           ;


WEA         :=     C16   &   ((MODE != [0,0,1,1])   &   (MODE != [0,1,0,1]))   ;

OEA         :=    !C16   #   (MODE == [0,0,1,1])                    ;

OEB         :=    !C16   #   (MODE == [0,0,1,1])                    ;

OEC         :=    !C16   #   (MODE == [0,0,1,1])                    ;

C16         :=    !C16   &   (MODE != [0,0,0,1])                    ;

CLAC_A      :=     (MODE == [0,1,1,0])   &   (LMODE == [0,1,0])
               #    CLAC_A   &   (MODE != [0,0,1,1])               ;

CLAC_B      :=     (MODE == [0,1,1,0])   &   (LMODE == [0,1,0])
               #    CLAC_B   &   (MODE != [0,0,1,1])               ;
```

Title: DECODER PAL		
Size: A	Document Number: PAL4B.SCH	REV:
Date: May 7, 1997	Sheet 4 of 34	

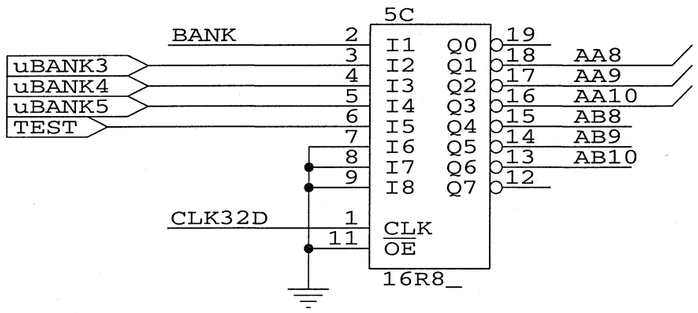


PAL 5B
DECODER PAL

THIS PAL DECODES STATES OF THE FFT CYCLE AND INTEGRATION CYCLE SEQUENCERS TO PROVIDE TIMING SIGNALS FOR THE DATA VALID INTEGRATOR. THE EQUATIONS BELOW GIVE THE PAL FUNCTIONS.

```
MODE  = [S11,S10,S9,S8]          ;
LMODE = [LS9,LS8]                ;


INCI        :=  !INCI  #  (MODE == [0,0,0,1])                    ;

INCR        :=  (MODE == [0,1,1,1])  &  (LMODE == [0,1])         ;

RSTI        :=  (MODE == [0,1,0,1])                              ;

RSTR        :=  (MODE == [0,0,1,1])  &  (LMODE == [1,0])         ;

IVAL        :=  (MODE == [0,1,1,0])
              # IVAL &  (MODE != [0,0,1,0])                      ;

RVAL        :=  (MODE == [0,0,1,1])  &  (LMODE == [0,1])
              # RVAL &  (MODE == [0,1,0,0])                      ;

TVAL        :=  (MODE == [0,0,1,1])  &  (LMODE == [1,1])
              # TVAL &  (MODE == [0,1,0,0])                      ;
```

Title: DECODER PAL		
Size: A	Document Number: PAL5B.SCH	REV:
Date: May 7, 1997	Sheet 5 of 34	

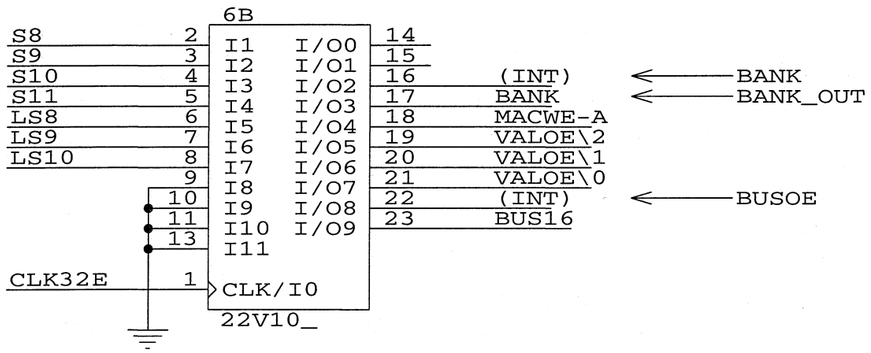


PAL 5C
DATA VALID INTEGRATOR BANK SELECTOR PAL

THIS PAL PROVIDES THE BANK SIGNALS FOR THE DATA VALID INTEGRATION RAMS. THE EQUATIONS BELOW SHOW THE PALS FUNCTION.

```
AA8      :=    BANK                    ;
AA9      :=    uBANK3                  ;
AA10     :=    uBANK4                  ;
AB8      :=    BANK                    ;
AB9      :=    uBANK3                  ;
AB10     :=    uBANK4                  ;
```

Title: DATA VALID INTEGRATOR BANK SELECTOR		
Size: A	Document Number: PAL5C.SCH	REV:
Date: May 7, 1997	Sheet 6 of 34	

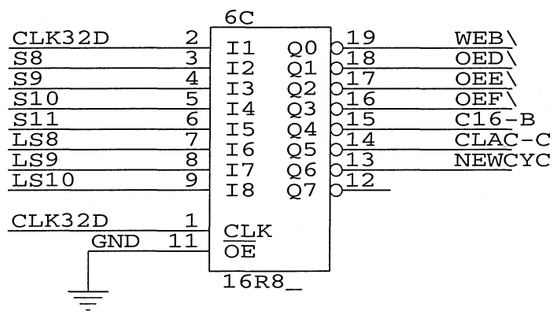


PAL 6B
DECODER PAL

THIS PAL DECODES STATES OF THE FFT CYCLE AND INTEGRATION CYCLE SEQUENCERS TO PROVIDE TIMING SIGNALS FOR THE DATA VALID INTEGRATOR. THE EQUATIONS BELOW GIVE THE PAL FUNCTIONS.

```
MODE   = [S11,S10,S9,S8]                ;
LMODE  = [LS10,LS9,LS8]                 ;


BUS16        =    0                                                    ;

BUSOE        :=    (MODE == [1,0,1,0])   &   (LMODE == [1,0,0])
                #   (MODE == [1,0,1,1])   &   (LMODE == [1,0,0])
                #   (MODE == [1,1,0,0])   &   (LMODE == [1,0,0])
                #   (MODE == [1,1,0,1])   &   (LMODE == [1,0,0])
                #   (MODE == [1,1,1,0])   &   (LMODE == [1,0,0])
                #   (MODE == [1,1,1,1])   &   (LMODE == [1,0,0])
                #    BUSOE    &   (MODE != [1,0,0,1])                  ;

BUS16.OE     =    BUSOE                                                ;

VALOE0       :=    (MODE == [1,0,1,0])   &   (LMODE == [1,0,0])
                #    VALOE0   &   (MODE != [1,0,0,1])                  ;

VALOE1       :=    (MODE == [1,1,0,0])   &   (LMODE == [1,0,0])
                #    VALOE1   &   (MODE != [1,0,0,1])                  ;

VALOE2       :=    (MODE == [1,1,1,0])   &   (LMODE == [1,0,0])
                #    VALOE2   &   (MODE != [1,0,0,1])                  ;

MACWE        :=    (MODE == [0,1,0,0])   &   LS8                       ;

BANK         :=     BANK   $ ((MODE == [0,1,0,0]) & (LMODE == [0,1,0]))   ;

BANK_OUT     :=     BANK
     $ (((MODE == [0,0,1,0]) # (MODE == [0,0,1,1])) & (LMODE == [0,0,1]))   ;
```

DECODER PAL		
Size A	Document Number PAL6B.SCH	REV
Date: May 7, 1997	Sheet 7 of 34	

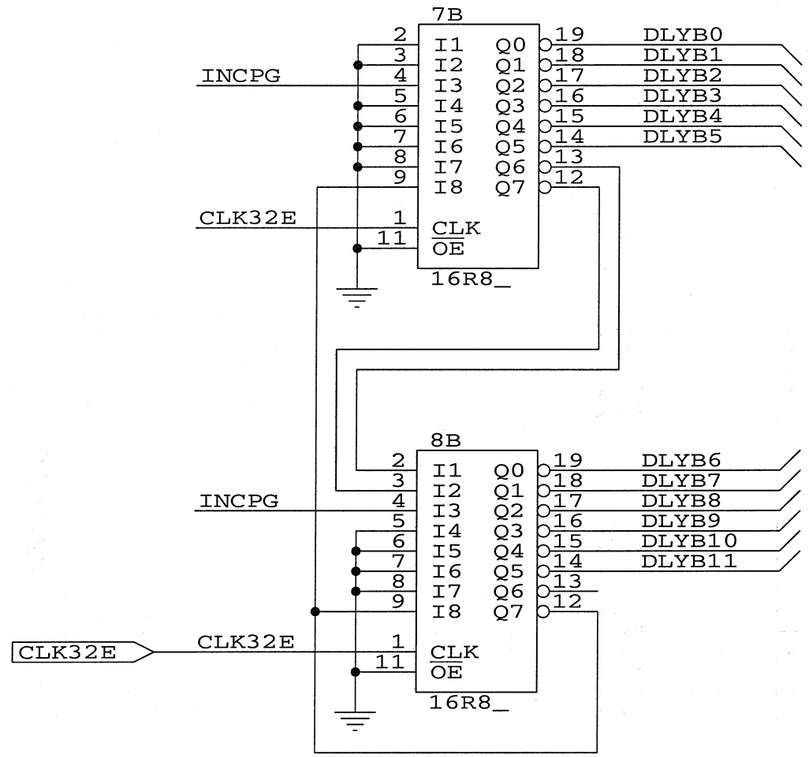


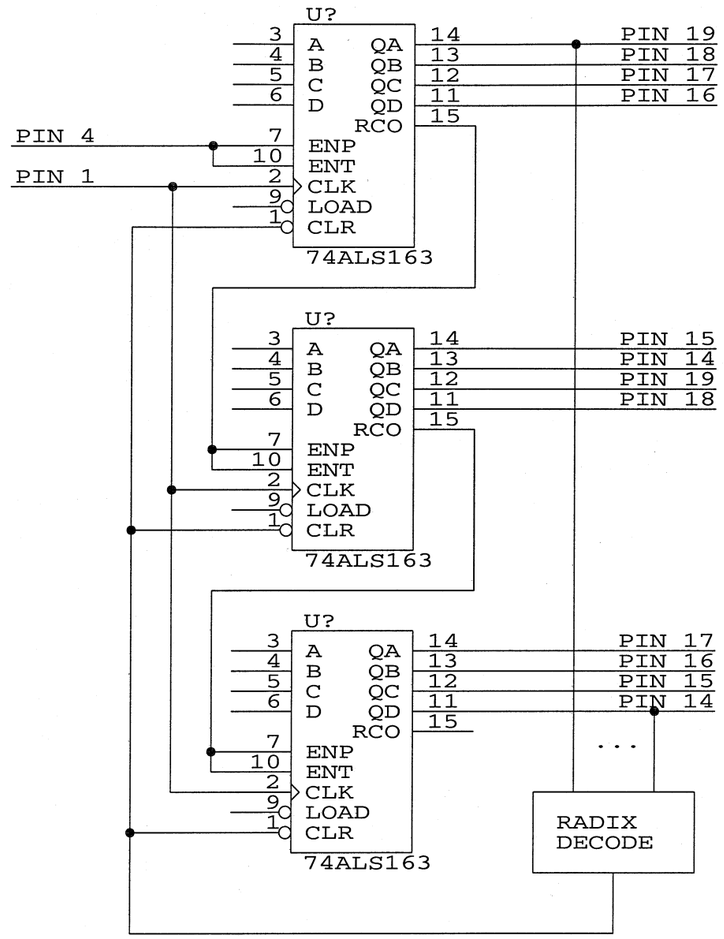
PAL 6C
DECODER PAL

THIS PAL DECODES STATES OF THE FFT CYCLE AND INTEGRATION CYCLE SEQUENCERS TO PROVIDE TIMING SIGNALS FOR THE DATA VALID INTEGRATOR. THE EQUATIONS BELOW GIVE THE PAL FUNCTIONS.

```
MODE  = [S11,S10,S9,S8]          ;
LMODE = [LS10,LS9,LS8]           ;


WEB       :=    C16  &  ((MODE != [0,0,1,1])  &  (MODE != [0,1,0,1]))  ;
OED       :=   !C16  #  (MODE == [0,0,1,1])                            ;
OEE       :=   !C16  #  (MODE == [0,0,1,1])                            ;
OEF       :=   !C16  #  (MODE == [0,0,1,1])                            ;
C16       :=   !C16  &  (MODE != [0,0,0,1])                            ;
CLAC_C    :=   (MODE == [0,1,1,0])  &  (LMODE == [0,1,0])
           #   CLAC_C  &  (MODE != [0,0,1,1])                          ;
NEWCYC    :=   (MODE == [0,1,0,1])  &  (LMODE == [0,0,1])
           #   NEWCYC  &  !(S8     &  (LMODE == [0,1,0]))              ;
```

Title: DECODER PAL		
Size: A	Document Number: PAL6C.SCH	REV:
Date: May 7, 1997	Sheet 8 of 34	

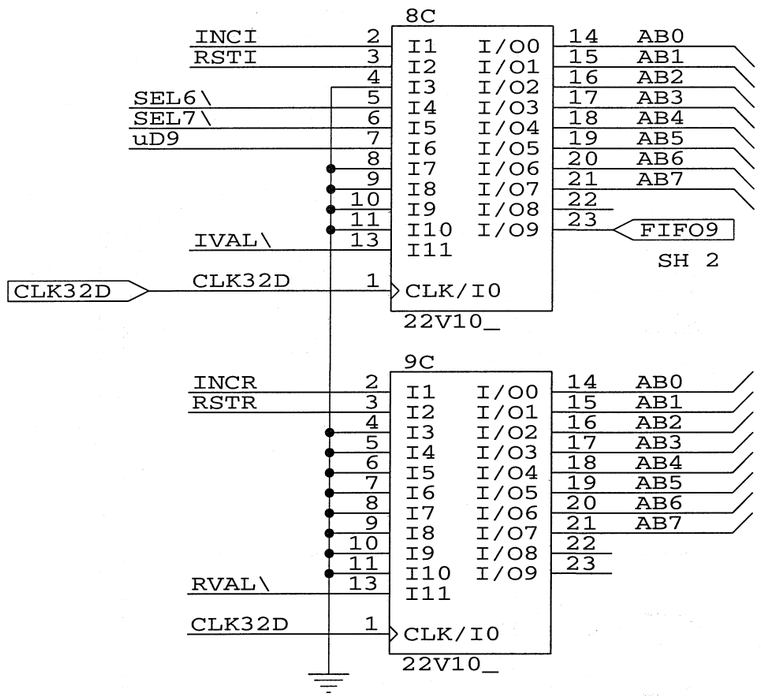


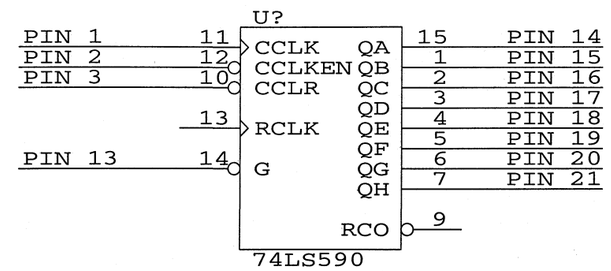


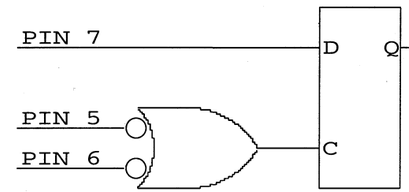
PALS 7B AND 8B
PULSAR GATE DELAY LINE CONTROL PALS

THESE PALS FORM A RADIX ???? COUNTER TO SET THE DELAY BETWEEN THE PULSAR GATE GENEARTOR
AND THE DATA VALID INTEGRATION INPUT. THIS DELAY MUST MATCH THE THRU PUT OF THE MAC SYSTEM.

Title: PULSAR GATE DELAY LINE CTRL: PALS 7B AND 8B		
Size: A	Document Number: PAL7B.SCH	REV:
Date: May 7, 1997	Sheet 9 of 34	





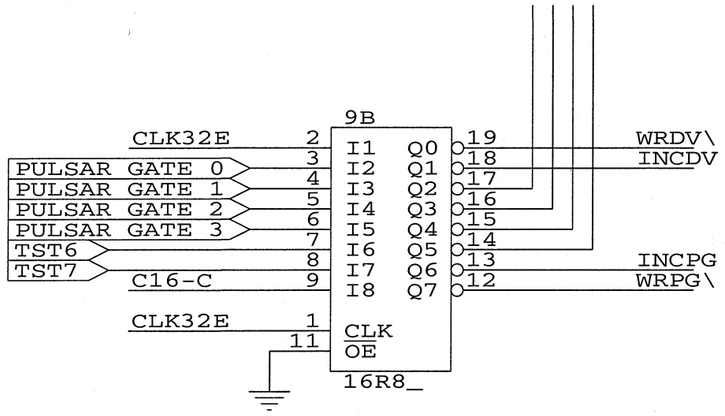


PALS 8C AND 9C
VALIDITY STORAGE ADDRESS COUNTERS

THESE 2 PALS GENERATE THE ADDRESS FOR THE DATA VALID INTERGATION RAMS.
THEY ARE ALMOST IDENTICAL AND DIFFER ONLY IN THE AUX FUNCTION OF STORING
FIFO MS DATA BIT FOR THE MICROPROCESSOR.

```
COUNT = [CNT7,CNT6,CNT5,CNT4,CNT3,CNT2,CNT1,CNT0]       ;


COUNT       :=    COUNT        & !INC   &   !RST
                # (COUNT + 1)   &  INC   &   !RST              ;

CNT7.OE      =    OE                                          ;
CNT6.OE      =    OE                                          ;
CNT5.OE      =    OE                                          ;
CNT4.OE      =    OE                                          ;
CNT3.OE      =    OE                                          ;
CNT2.OE      =    OE                                          ;
CNT1.OE      =    OE                                          ;
CNT0.OE      =    OE                                          ;

FIFO9        =    uD9     &  (SEL6  #  SEL7)
                #  FIFO9   & !(SEL6  #  SEL7)                 ;
```

Title: VALIDITY STORAGE ADR CNTRS: PALS 8C AND 9C		
Size: A	Document Number: PAL8C.SCH	REV:
Date: May 7, 1997	Sheet 10 of 34	



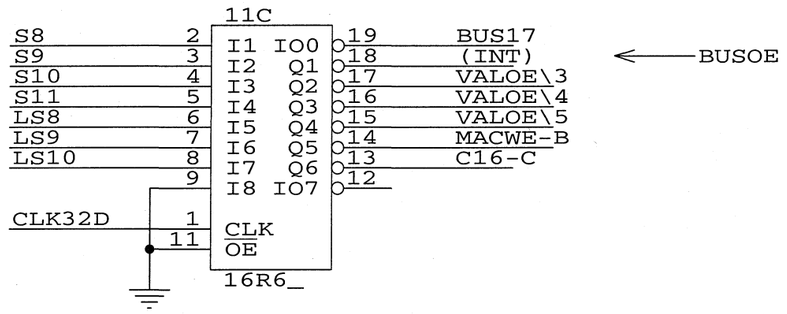
PAL 9B

PULSAR GATE DELAY LINE CONTROL PAL

THIS PAL PROVIDES SOME CONTROL SIGNALS FOR THE PULSAR AND DATA VALID DELAY LINES. IT ALSO CAPTURES THE PULSAR GATE SIGNALS AND CAN PUT TEST SIGNALS INTO THE PULSAR DELAY RAM.

```
TST = [TST7,TST6]                                                    ;

WRDV        :=      C16                                              ;

INCDV       :=      C16                                              ;

GATE0       :=    PULSAR0   &   C16   &   (TST == [0,0])
                #   GATE0   & !C16    &   (TST == [0,0])
                #   0       &         &   (TST == [0,1])
                #   1       &         &   (TST == [1,0])
                # !GATE0    &   C16   &   (TST == [1,1])
                #   GATE0   & !C16    &   (TST == [1,1])              ;

GATE1       :=    PULSAR1   &   C16   &   (TST == [0,0])
                #   GATE1   & !C16    &   (TST == [0,0])
                #   0       &         &   (TST == [0,1])
                #   1       &         &   (TST == [1,0])
                # !GATE1    &   C16   &   (TST == [1,1])
                #   GATE1   & !C16    &   (TST == [1,1])              ;

GATE2       :=    PULSAR2   &   C16   &   (TST == [0,0])
                #   GATE2   & !C16    &   (TST == [0,0])
                #   0       &         &   (TST == [0,1])
                #   1       &         &   (TST == [1,0])
                # !GATE2    &   C16   &   (TST == [1,1])
                #   GATE2   & !C16    &   (TST == [1,1])              ;

GATE3       :=    PULSAR3   &   C16   &   (TST == [0,0])
                #   GATE3   & !C16    &   (TST == [0,0])
                #   0       &         &   (TST == [0,1])
                #   1       &         &   (TST == [1,0])
                # !GATE3    &   C16   &   (TST == [1,1])
                #   GATE3   & !C16    &   (TST == [1,1])              ;

INCPG       :=      C16                                              ;

WRPG        :=      C16                                              ;
```

Title: PULSAR GATE DELAY LINE CONTROL PAL		
Size: A	Document Number: PAL9B.SCH	REV:
Date: May 7, 1997	Sheet 11 of 34	

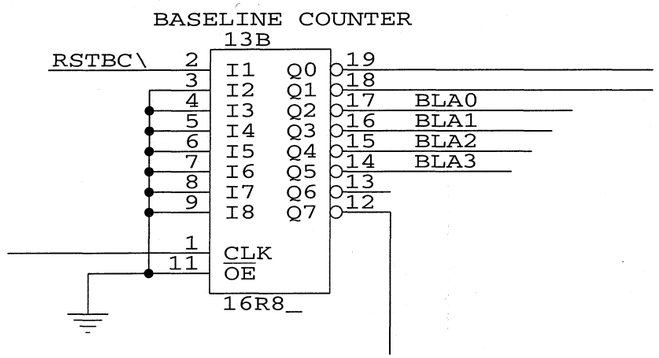


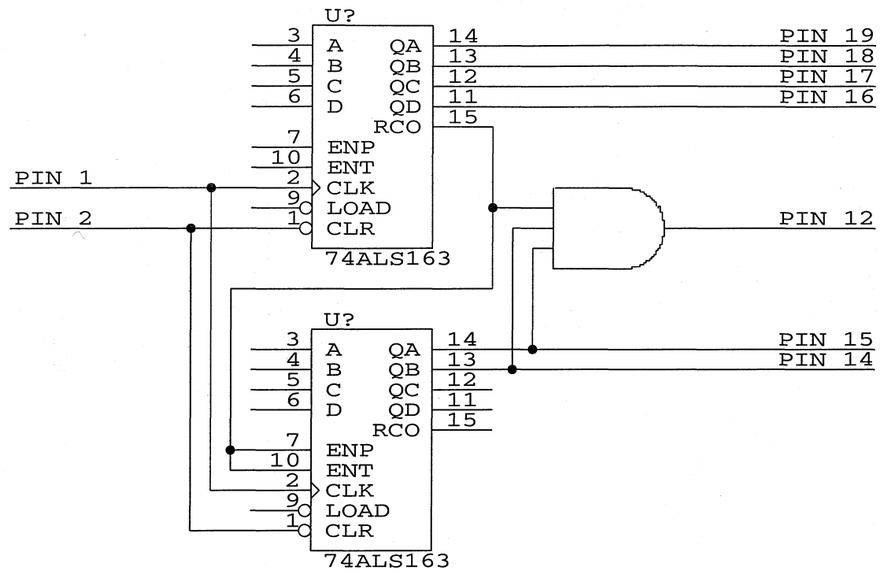
PAL 11C
DECODER PAL

THIS PAL DECODES STATES OF THE FFT CYCLE AND INTEGRATION CYCLE SEQUENCERS TO PROVIDE TIMING SIGNALS FOR THE DATA VALID INTEGRATOR. THE EQUATIONS BELOW GIVE THE PAL FUNCTIONS.

```
MODE   = [S11,S10,S9,S8]                ;
LMODE  = [LS10,LS9,LS8]                 ;


BUS17        =    0                                                    ;

BUSOE        :=    (MODE == [1,0,1,0])   &   (LMODE == [1,0,0])
                 #   (MODE == [1,0,1,1])   &   (LMODE == [1,0,0])
                 #   (MODE == [1,1,0,0])   &   (LMODE == [1,0,0])
                 #   (MODE == [1,1,0,1])   &   (LMODE == [1,0,0])
                 #   (MODE == [1,1,1,0])   &   (LMODE == [1,0,0])
                 #   (MODE == [1,1,1,1])   &   (LMODE == [1,0,0])
                 #    BUSOE    &   (MODE != [1,0,0,1])                 ;

BUS17.OE     =    BUSOE                                                ;

VALOE3       :=    (MODE == [1,0,1,1])   &   (LMODE == [1,0,0])
                 #    VALOE3   &   (MODE != [1,0,0,1])                 ;

VALOE4       :=    (MODE == [1,1,0,1])   &   (LMODE == [1,0,0])
                 #    VALOE4   &   (MODE != [1,0,0,1])                 ;

VALOE5       :=    (MODE == [1,1,1,1])   &   (LMODE == [1,0,0])
                 #    VALOE5   &   (MODE != [1,0,0,1])                 ;

MACWE        :=    (MODE == [0,1,0,0])   &   LS8                        ;

C16          :=    !C16   &   (MODE != [0,0,0,1])                       ;
```

DECODER PAL		
Size A	Document Number PAL11C.SCH	REV
Date: May 7, 1997	Sheet 12 of 34	



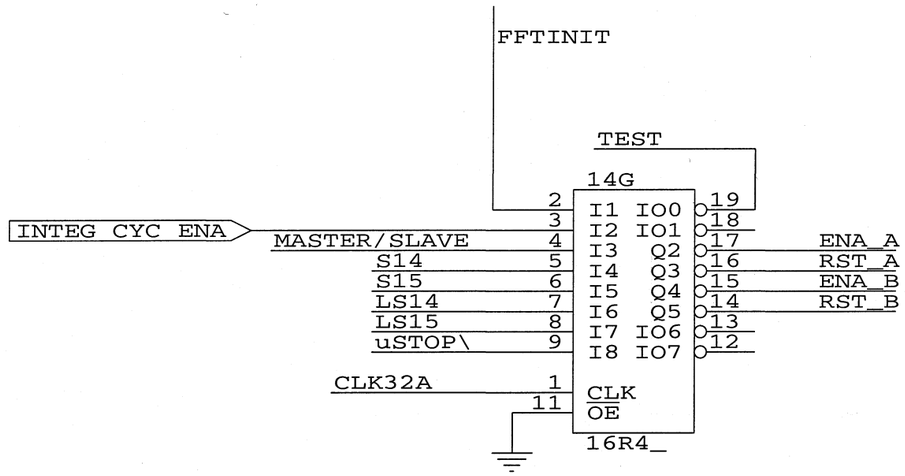


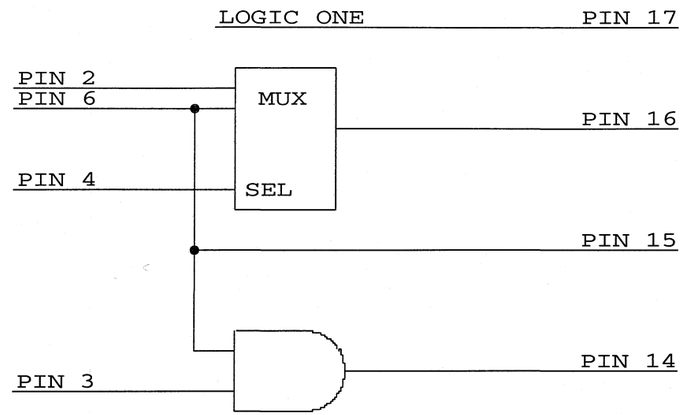
PAL 13B
BASELINE COUNTER PAL

THIS PAL IS A 6-BIT BINARY COUNTER USED TO READ THRU THE MULTIPLIER RESULTS. THE FIRST 2 BIYS OF THE COUNTER ADDRESS THE REAL/IMAG AND CHANNEL 0/CHANNEL 1 PRODUCTS ON A MAC CARD. THE LAST 4-BITS ARE THE LOWER BITS OF THE 8-BIT BASELINE ADDRESS. THE EQUATIONS BELOW GIVE THE PAL FUNCTION.

```
COUNT = [CNT5,CNT4,CNT3,CNT2,CNT1,CNT0]          ;


COUNT    :=    (COUNT + 1)   &   !RST             ;
CARRY    :=    (COUNT == [1,1,1,1,1,0])           ;
```

Title: BASELINE COUNTER PAL		
Size: A	Document Number: PAL13B.SCH	REV:
Date: May 7, 1997	Sheet 13 of 34	



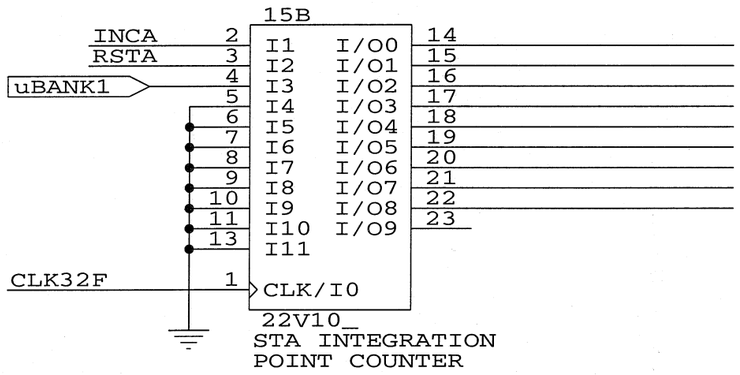


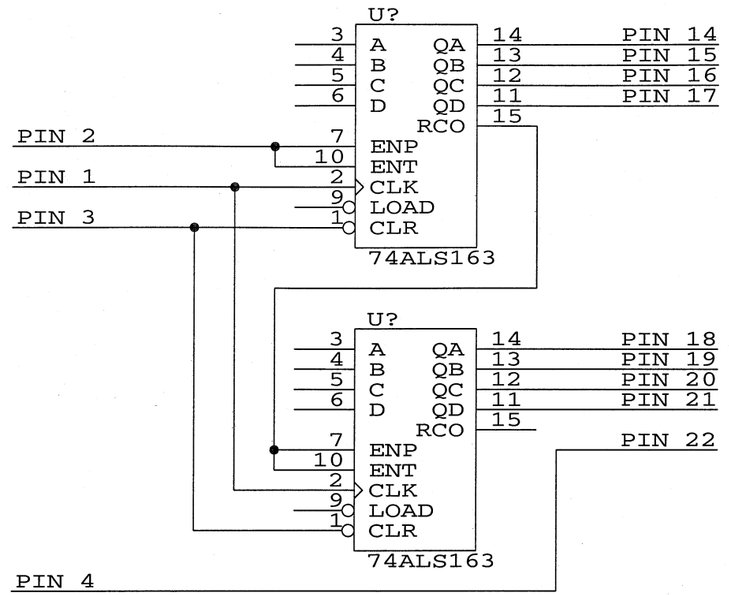
PAL 14G
SEQUENCER COUNTER CONTROL PAL

THIS PAL GENERATES THE COUNT ENABLE AND RESET SIGNALS FOR THE FFT CYCLE AND FRINGE CYCLE SEQUENCER COUNTERS.

```
ENA_A    :=    1                                   ;

RST_A    :=    FFTINIT  &  !MASTER
           #   S15      &   MASTER                  ;

ENA_B    :=    S15                                 ;

RST_B    :=    S15      &   INTCYCENA               ;
```

Title: SEQUENCER COUNTER CONTROL PAL		
Size: A	Document Number: PAL14G.SCH	REV:
Date: May 7, 1997	Sheet 14 of 34	



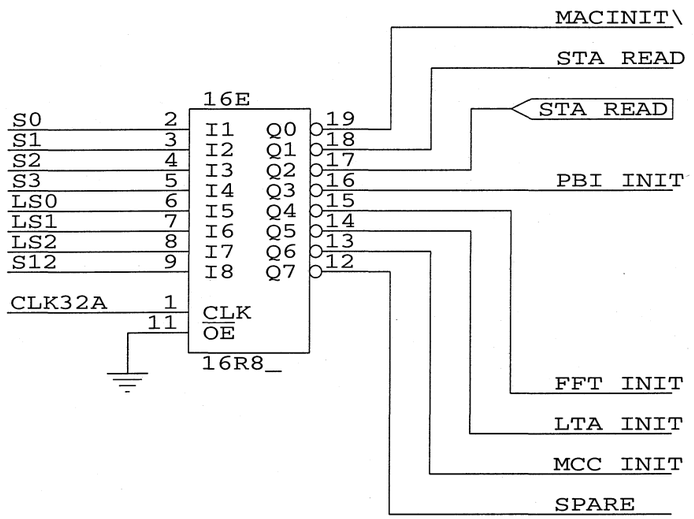


PAL 15B (ALSO PAL 14B)
8- BIT COUNTER PAL

THIS PAL IS AN 8-BIY COUNTER USED IN READING THE MAC RESULTS.

```
COUNT = [CNT7,CNT6,CNT5,CNT4,CNT3,CNT2,CNT1,CNT0]      ;

COUNT       :=    COUNT         & !INC  &  !RST
                # (COUNT + 1)   &  INC  &  !RST          ;

CNT8        :=    BANK                                  ;
```

Title: 8-BIT COUNTER: PALS 15B AND 14B		
Size: A	Document Number: PAL15B.SCH	REV:
Date: May 7, 1997	Sheet 15 of 34	

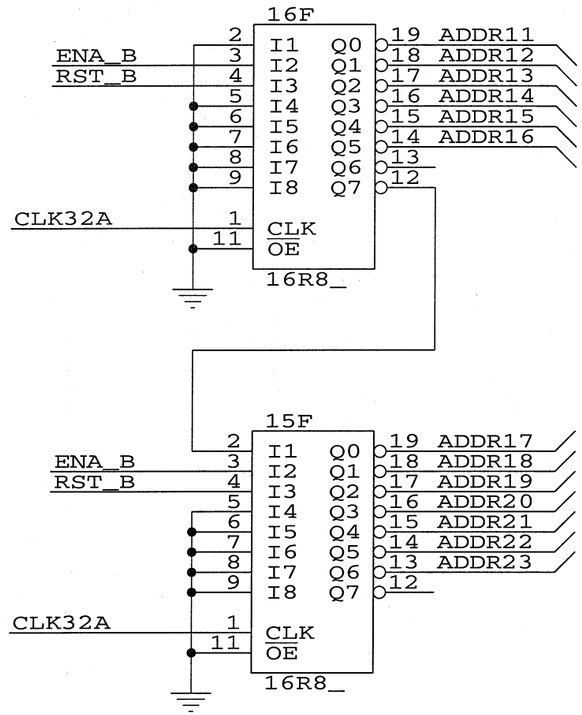


PAL 16E
FFT CYCLE CONTROL SIGNAL DECPDER PAL

THIS PAL DECODES THE FFT CYCLE SEQUENCES TO GENERATE CONTROL SIGNALS FOR THE SYSTEM. THE EQUATIONS BELOW DEFINE THE PAL.

```
MODE    = [S3,S2,S1,S0]          ;

MACINIT     :=     (MODE == [0,1,0,0])                    ;
STA_READ    :=      STA__READ                             ;
STA__READ   :=      S12                                   ;
PBIINIT     :=     (MODE == [0,0,1,0])  &  (LS0 == 1)     ;
FFTINIT     :=     (MODE == [0,0,1,1])                    ;
LTAINIT     :=     (MODE == [0,1,0,1])                    ;
MCCINIT     :=     (MODE == [0,0,0,1])                    ;
SPARE0      :=     (MODE == [0,1,0,0])                    ;
```

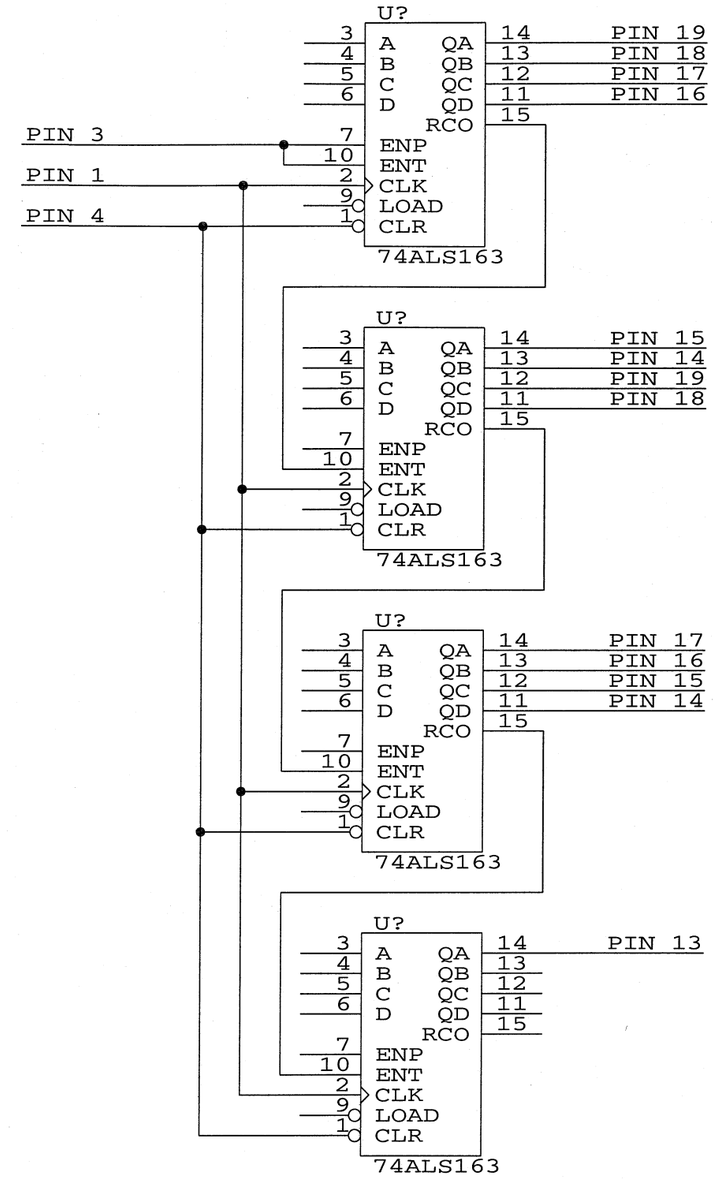
Title: FFT CYCLE CONTROL SIGNAL DECODER		
Size: A	Document Number: PAL16E.SCH	REV:
Date: May 7, 1997	Sheet 16 of 34	



FRINGE CYCLE/INTEGRATION CYCLE SEQUENCER
RADIX = 8192

PALS 16F AND 15F
FRINGE CYCLE/INTEGRATION CYCLE SEQUENCER ADDERSS COUNTER PALS

THESE PALS PROVIDE A 13-BIT BINARY COUNTER FOR THE ADDRESS INPUTS OF THE FRINGE CYCLE/INTEGRATION CYCLE SEQUENCER.



FRINGE & INT CYCLE SEQUENCER ADR CNTR		
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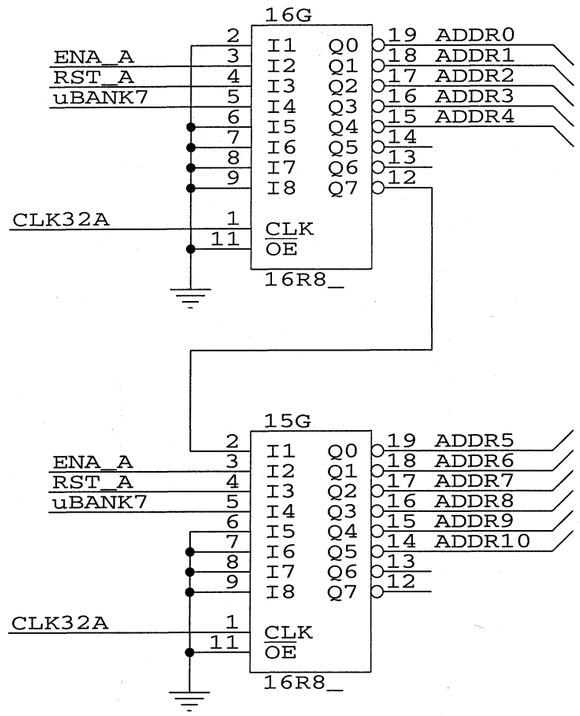
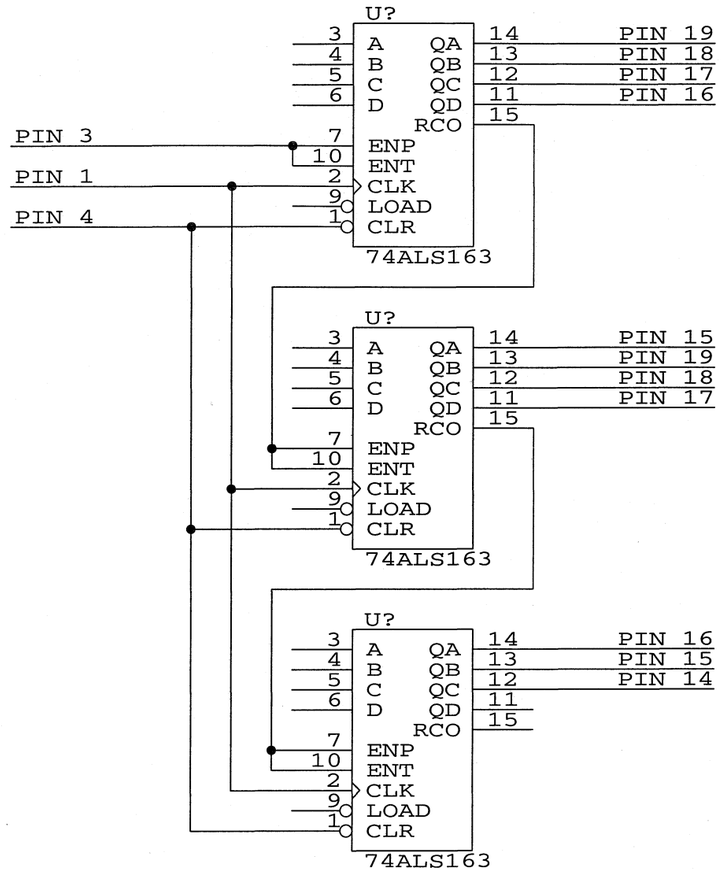


FFT CYCLE SEQUENCER
RADIX = 516



PALS 15G AND 16G
FFT CYCLE SEQUENCER ADDRESS COUNTERS

THESE TWO PALS (THEY HAVE SLIGHTLY DIFFERENT PERSONALITIES) CONSTITUTE AN 11-BIT ADDRESS COUNTER. IN USE, THE ENABLE LINE IS ALWAYS PERMISSIVE AND THE RESET LINE MAKES THE COUNTER A RADIX 516 COUNTER.

Title: FFT CYCLE SEQ ADR CNTR		
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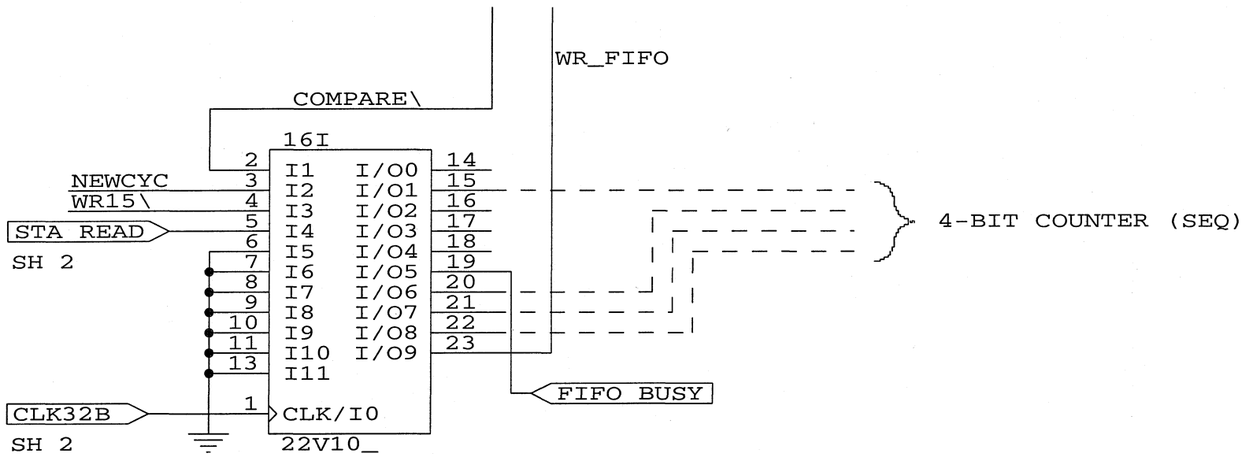

PAL 16I
FIFO CONTROL PAL

THIS PAL PROVIDES THE WRITE PULSE FOR THE FIFOs. IT CONTAINS A 4-BIT COUNTER SCHRONIZED BY THE STA_READ SIGNAL WHICH IS USED TO TIME THE FIFO WRITE DURING A MAC READOUT CYCLE. THE FIFO BUSY (ACTIVE) LINE TELLS THE MICROPROCESSOR WHEN THE FIFO IS THRU STORING A BASELINES WORTH OF RESULTS AND IT CAN READ THE FIFO. THE COMPARE SIGNAL COMES FROM A COMPARATOR AND IS LOW WHEN THE BASELINE BEING READ BY THE LTA IS = TO THE BASELINE PROGRAMED FOR STORAGE IN THE FIFO.

```
SEQ = [SEQ3,SEQ2,SEQ1,SEQ0]                                    ;


WR_FIFO     :=    (SEQ == [1,0,0,0])   &  DLYCOMP   &  ACTIVE
                # WR_FIFO   &   (SEQ != [1,1,0,0])                          ;

SEQ         :=    (SEQ + 1)   &   (SEQ != [1,1,0,1])
                # (SEQ     )   &   (SEQ == [1,1,0,1]) &   !STA_READ        ;

ACTIVE      :=     CAP15    &    NEWCYC    &   !DLYNEWCYC
                #   ACTIVE   &    NEWCYC                                   ;

CAP15       :=     WR15     #   (CAP15     &   !ACTIVE)                    ;

DLYCOMP     :=     COMPARE &   (SEQ == [1,1,0,0])
                #   DLYCOMP & !(SEQ == [1,1,0,0])                         ;

DLYNEWCYC   :=     NEWCYC                                                  ;
```

	Title: FIFO CONTROL PAL	
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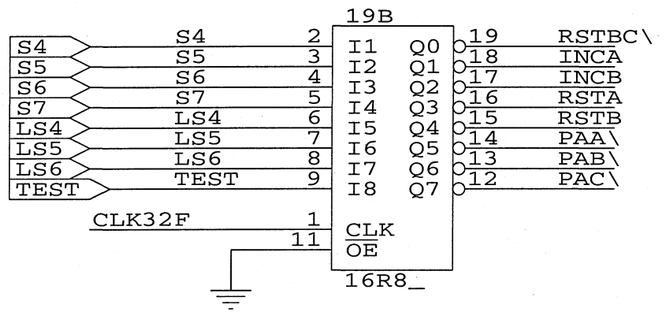

PAL 19B
DECODER PAL

THIS PAL DECODES STATES OF THE FFT CYCLE AND INTEGRATION CYCLE SEQUENCERS TO PROVIDE TIMING SIGNALS FOR THE MAC RESULTS READOUT. THE EQUATIONS BELOW GIVE THE PAL FUNCTIONS.

```
MODE   = [S7,S6,S5,S4]                ;
LMODE  = [LS5,LS4]                    ;


RSTBC       :=     (MODE == [1,0,1,0])   &   (LMODE == [0,1])      ;

INCA        :=    !INCA    &   (MODE != [0,0,0,1])                 ;

INCB        :=     (MODE == [0,1,1,1])   &   (LMODE == [0,1])      ;

RSTA        :=     (MODE == [0,1,0,0])                             ;

RSTB        :=     (MODE == [0,0,1,1])   &   (LMODE == [1,0])      ;

PAA         :=     (MODE == [0,1,0,0])
                #    PAA   & !(MODE == [1,1,1,1])                  ;

PAB         :=     (MODE == [1,1,1,1])   &   (LMODE == [0,1])
                #    PAB   &   (MODE == [0,0,0,1])
                #    PAB   &   (MODE == [0,0,1,0])                 ;

PAC         :=     (MODE == [1,1,1,1])   &   (LMODE == [1,1])
                #    PAC   &   (MODE == [0,0,0,1])
                #    PAC   &   (MODE == [0,0,1,0])                 ;
```

Title: DECODER PAL		
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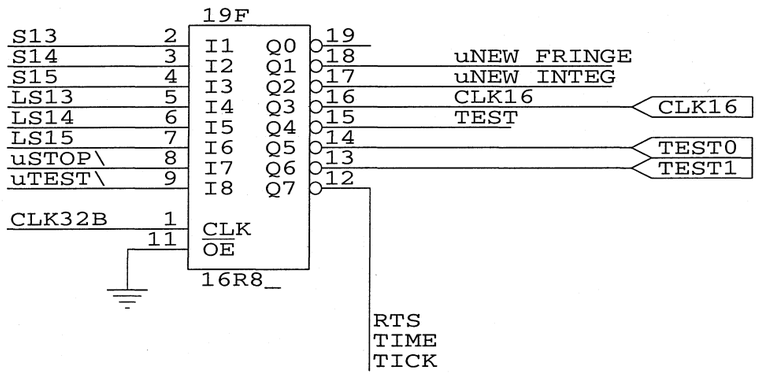

PAL 19F
TIMING SIGNAL DECODE PAL

THIS PAL DECODES THE FFT CYCLE SEQUENCER AND INTEGRATION CYCLE SEQUENCER TO GENERATE VARIOUS TIMING SIGNALS NEED IN THE CORRELATOR. THE EQUATIONS BELOW GIVE THE PAL FUNCTIONS.

```
  LMODE   =   [LS15,LS14,LS13]                ;


NEWFRINGE   :=    ((LMODE == [0,1,0])   #   (LMODE == [0,1,1]))   &   S15
              #    NEWFRINGE   &   !S15                                    ;

NEWINTEG    :=     (LMODE == [0,1,0])   &   S15
              #    NEWINTEG             &   !((LMODE == [0,1,1])   &   S15)   ;

CLK16       :=     !CLK16   &   !S15                                       ;

TEST        :=      TST     & (LMODE == [0,1,0])    &   S15
              #     TEST    &   !(LMODE == [0,1,0]   &   S15)              ;

TEST0       :=      TST     & (LMODE == [0,1,0])    &   S15
              #     TEST    &   !(LMODE == [0,1,0]   &   S15)              ;

TEST1       :=      TST     & (LMODE == [0,1,0])    &   S15
              #     TEST    &   !(LMODE == [0,1,0]   &   S15)              ;

TIMETICK    :=     (LMODE == [0,0,1])   &   S15
              #     TIMETICK             &   !((LMODE == [0,1,1])   &   S15)   ;
```

TIMING SIGNAL DECODER PAL		
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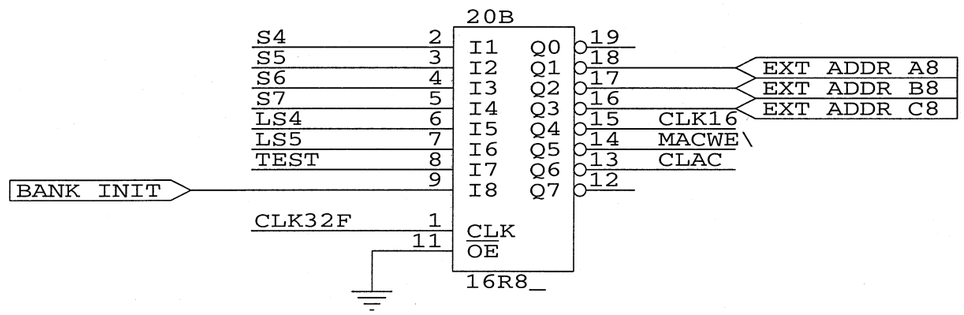

PAL 20B
DECODER PAL

THIS PAL DECODES STATES OF THE FFT CYCLE AND INTEGRATION CYCLE SEQUENCERS TO PROVIDE TIMING SIGNALS FOR THE MAC RESULTS READOUT AND OPERATION . THE EQUATIONS BELOW GIVE THE PAL FUNCTIONS.

```
MODE   = [S7,S6,S5,S4]              ;
LMODE  = [LS5,LS4]                  ;


BANK      :=     BANK  $  ((MODE == [0,1,1,0])  &  (LMODE == [1,0]))     ;
ADDR8A    :=     BANK  $  ((MODE == [0,0,1,1])  &  !TEST)                ;
ADDR8B    :=     BANK  $  ((MODE == [0,0,1,1])  &  !TEST)                ;
ADDR8C    :=     BANK  $  ((MODE == [0,0,1,1])  &  !TEST)                ;
CLK16     :=    !CLK16  &   (MODE != [0,0,0,1])                          ;
MACWE     :=    (MODE == [0,0,1,1])  &   LS4                             ;
CLAC      :=    (MODE == [0,1,0,1])  &  (LMODE == [1,0])
             #   CLAC  &   (MODE != [0,0,1,0])                           ;
```

DECODER PAL		
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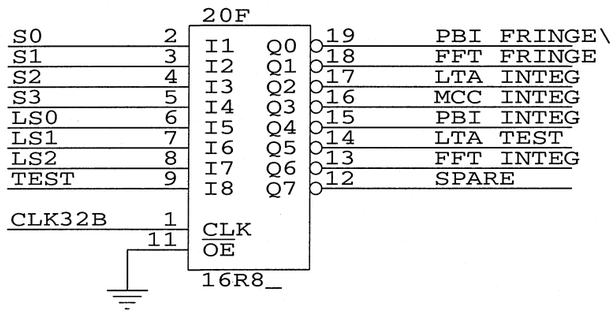

PAL 20F
FRINGE CYCLE AND INTEGRATION CYCLE DECODE PAL

THIS PAL DECODES STATES OF THE FFT CYCLE AND INTEGRATION CYCLE SEQUENCERS TO PROVIDE CYCLE INIT SIGNALS TO VARIOUS PARTS OF THE SYSTEM. THE FUNCTION OF THE PAL IS BEST SEEN IN THE EQUATIONS BELOW.

```
                MODE    = [S3,S2,S1,S0]           ;
                LMODE   = [LS2,LS1,LS0]           ;

PBIFRINGE   :=  (MODE == [0,1,1,0]) & ((LMODE == [1,0,1]) # (LMODE == [1,1,1]))
              #  PBIFRINGE  &  (MODE != [0,1,1,0])                              ;

FFTFRINGE   :=  (MODE == [0,1,1,0]) & ((LMODE == [1,0,1]) # (LMODE == [1,1,1]))
              #  FFTFRINGE  &  (MODE != [0,1,1,0])                              ;

PBIINTEG    :=  (MODE == [0,1,1,0]) &  (LMODE == [1,1,1])
              #  PBIINTEG   & !((MODE == [0,1,1,0]) & (LMODE == [1,0,1]))       ;

FFTINTEG    :=  (MODE == [0,1,1,0]) &  (LMODE == [1,1,1])
              #  FFTINTEG   & !((MODE == [0,1,1,0]) & (LMODE == [1,0,1]))       ;

MCCINTEG    :=  (MODE == [0,1,1,0]) &  (LMODE == [0,1,1])
              #  MCCINTEG   &  (MODE != [0,1,1,0])                              ;

LTAINTEG    :=  (MODE == [0,1,1,0]) &  (LMODE == [0,1,1])
              #  LTAINTEG   &  (MODE != [0,1,1,0])                              ;

LTATEST     :=  (MODE == [0,1,1,0]) &  (LMODE == [0,1,1])  &  TEST
              #  LTATEST    &  (MODE != [0,1,1,0])                              ;

SPARE2      :=  (MODE == [0,1,1,0]) &  (LMODE == [0,0,1])
              #  SPARE2     &  (MODE != [0,1,1,0])                              ;
```

FRINGE AND INT CYCLE DECODE PAL		
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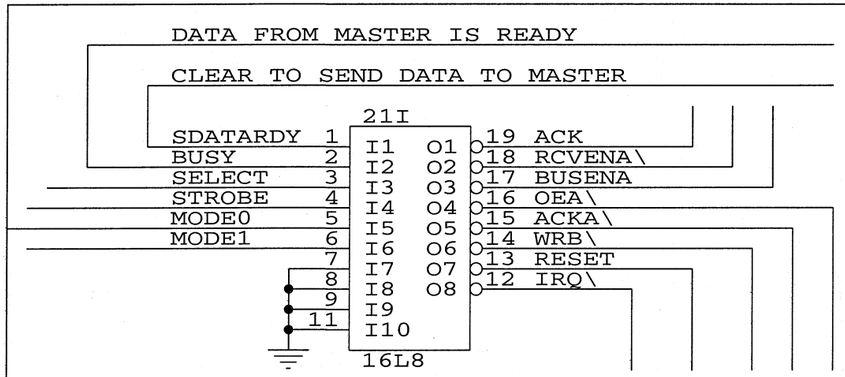


PAL 21I
HCB CONTROLLER PAL

ACK: FOR WRITES FROM MASTER TO 2950, ACK GOES LOW WHEN 2950 IS BUSY, GOES HIGH WHEN 2950 IS READY FOR MORE DATA.

FOR READS OF 2950 BY MASTER, ACK GOES LOW WHEN 2950 HAS NEW DATA, HIGH WHEN MASTER HAS READ THE DATA.

FOR ATTENTION REQUEST FROM SLAVE TO MASTER, ACK GOES LOW; CLEARS WHEN MASTER INTEROGATES SLAVE.

RCVENA\: ENABLE DATA FROM HCB BUS TO LOCAL BUS

BUSENA: ENABLE DATA FROM LOCAL BUS TO HCB BUS

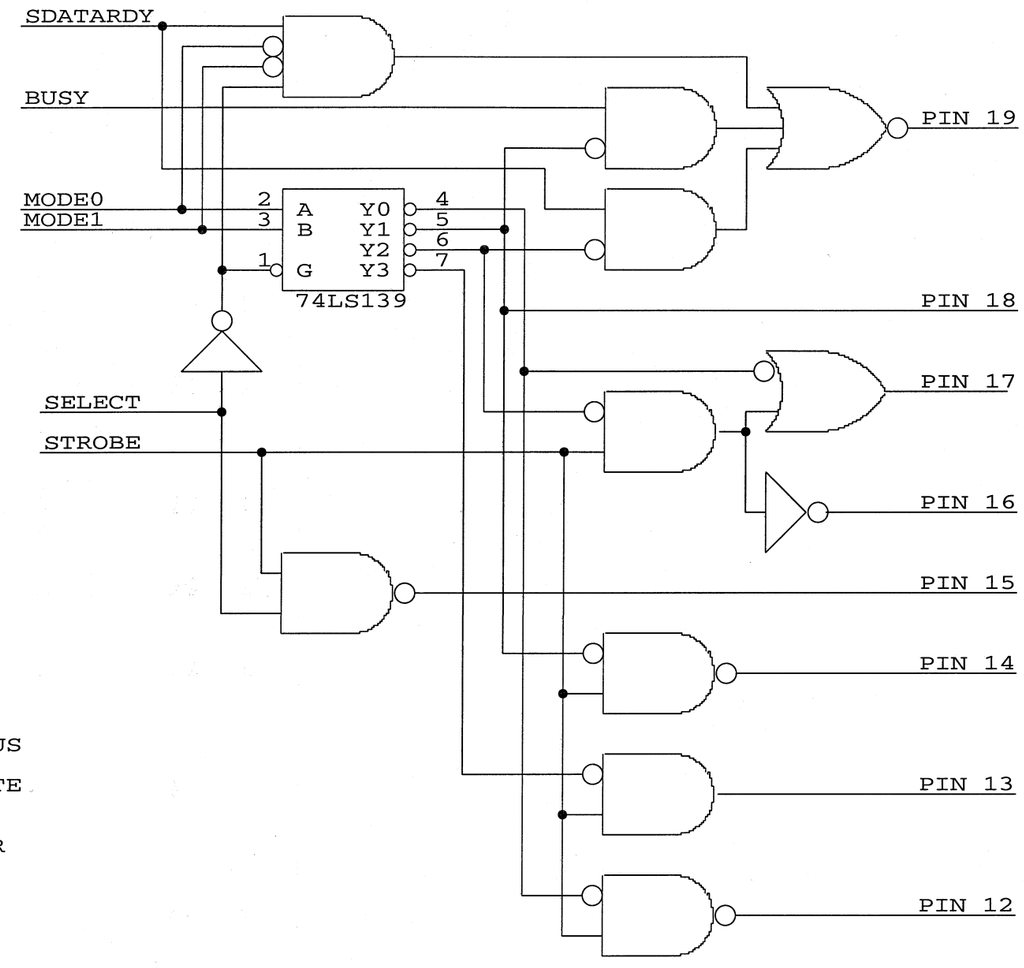
OEA\: ENABLE DATA FROM 2950 PORT A TO LOCAL BUS

ACKA\: ACK PULSE TO 2950 FOR BOTH READ AND WRITE (PULSES LOW, TRAILING EDGE IS ACTIVE)

WRB\: WRITE PULSE TO 2950 FOR WRITES BY MASTER (PULSES LOW, TRAILING EDGE IS ACTIVE)

RESET: HIGH TRUE RESET PULSE

IRQ\: LOW TRUE INTR RQST PULSE TO SLAVE INDICATES NEXT BYTE IS FIRST BYTE OF A TRANSFER FROM MASTER TO SLAVE.



SELECT	STROBE	MODE1	MODE0	FUNCTION	ACK	RCVENA\	BUSENA	OEA\	ACKA\	WRB\	RESET	IRQ\
0	X	0	0	ALLOW SLAVE TO ASSERT ATTN	SDATARDY\	1	0	1	1	1	0	1
0	X	0	1	IDLE	1	1	0	1	1	1	0	1
0	X	1	0	IDLE	1	1	0	1	1	1	0	1
0	X	1	1	IDLE	1	1	0	1	1	1	0	1
1	_⎍_	0	0	MASTER SENDS IRQ TO SLAVE	1	1	1	1	STROBE\	1	0	STROBE\
1	_⎍_	0	1	MASTER WRITES TO SLAVE	BUSY\	0	0	1	STROBE\	STROBE\	0	1
1	_⎍_	1	0	MASTER READS FROM SLAVE	SDATARDY\	1	STROBE	STROBE\	STROBE\	1	0	1
1	_⎍_	1	1	MASTER RESETS SLAVE	1	1	0	1	STROBE\	1	STROBE	1

HCB CONTROLLER PAL		
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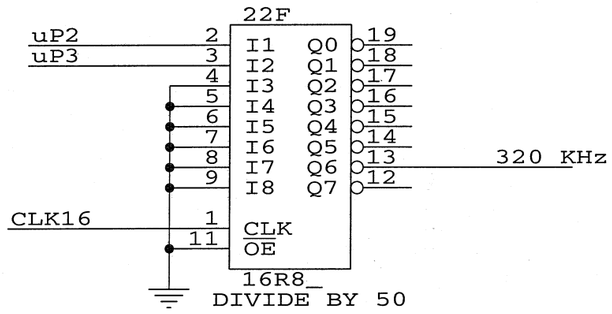
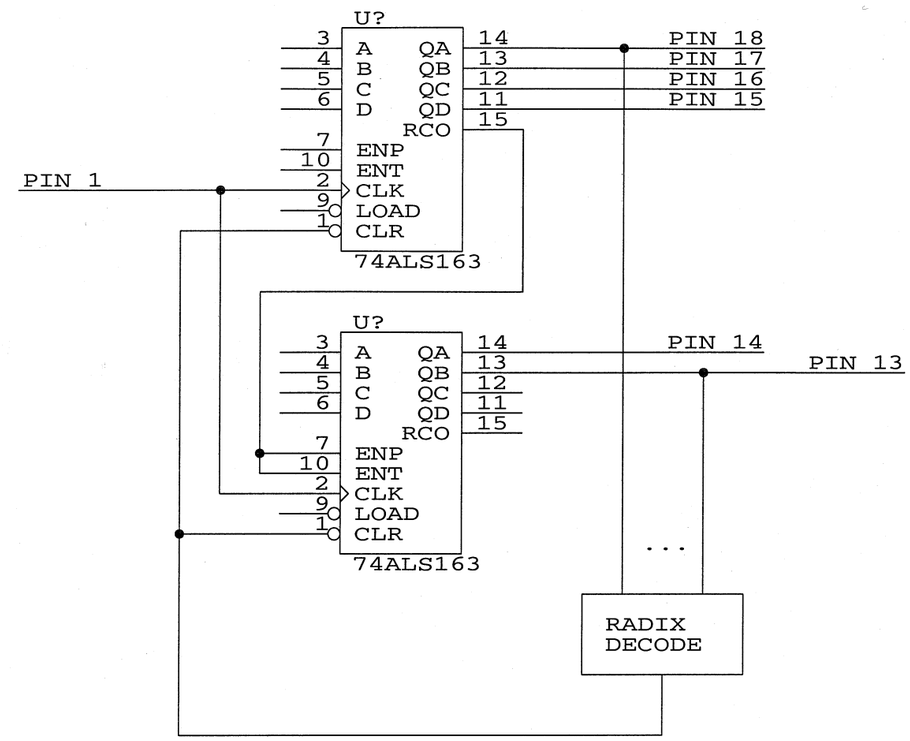


PAL 22F
PHASE LOCK LOOP REFERENCE DIVIDER

THE CLOCK ON PIN 1 IS DIVIDED BY 50 TO YIELD THE OUTPUT ON PIN 13. PINS 2 AND 3 ARE NOT USED.



Title: PHASE LOCK LOOP REFERENCE DIVIDER		
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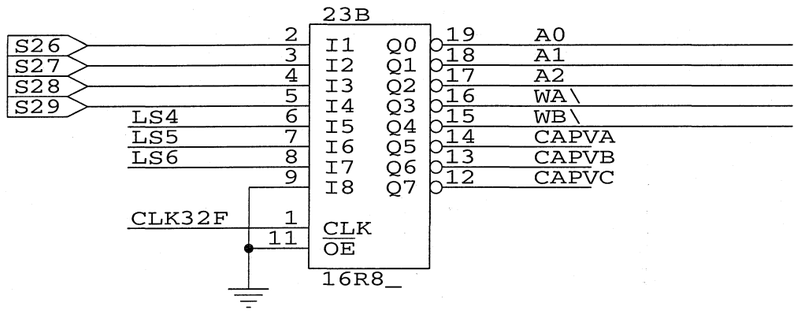
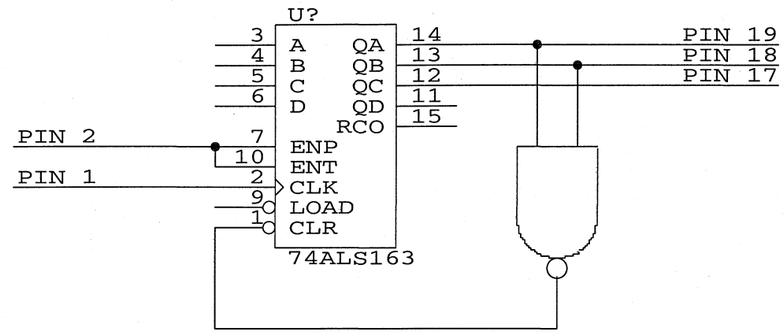
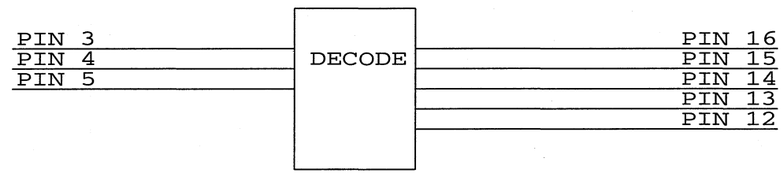


PAL 23B
DATA VALID DELAY RAM CONTROL PAL





THIS PAL PROVIDES THE ADDRESS COUNTER FOR THE DATA VALID DELAY RAMS.
THE DATA VALIDS FROM THE DEFORMATERS MUST BE DELAYED 5 FFT CYCLES
TO COMPENSATE FOR THE PIPELINING OF THE FFT ENGINE. THE PAL ALSO DECODES
THE MCC CARD SEQUENCERS TO GENERATE THE RAM WRITE SIGNALS AND THE SIGNALS
NEEDED TO CAPTURE THE DATA VALIDS AT 3 STAGES ON THE MCC CARD.

```
ADDR   = [A2,A1,A0]                ;
MODE   = [S29,S28,S27]             ;


ADDR    :=    (ADDR + 1)   &    S26   &   (ADDR != [0,1,1])
           # (ADDR     )   &   !S26                          ;

WA      :=     (MODE == [0,0,1])                            ;

WB      :=     (MODE == [0,0,1])                            ;

CAPVA   :=     (MODE == [0,1,0])                            ;

CAPVB   :=     (MODE == [0,1,1])                            ;

CAPVC   :=     (MODE == [1,0,0])                            ;
```

Title: DATA VALID DELAY RAM CONTROL PAL		
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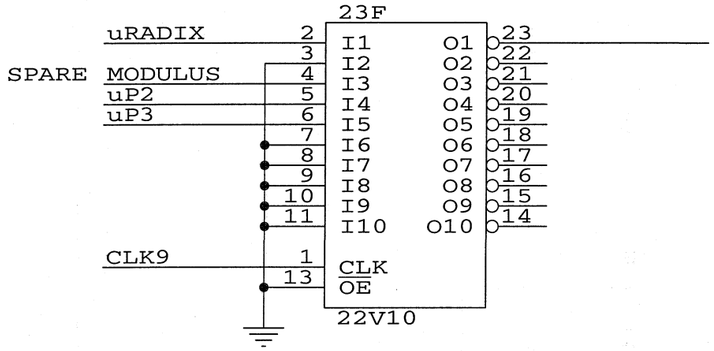
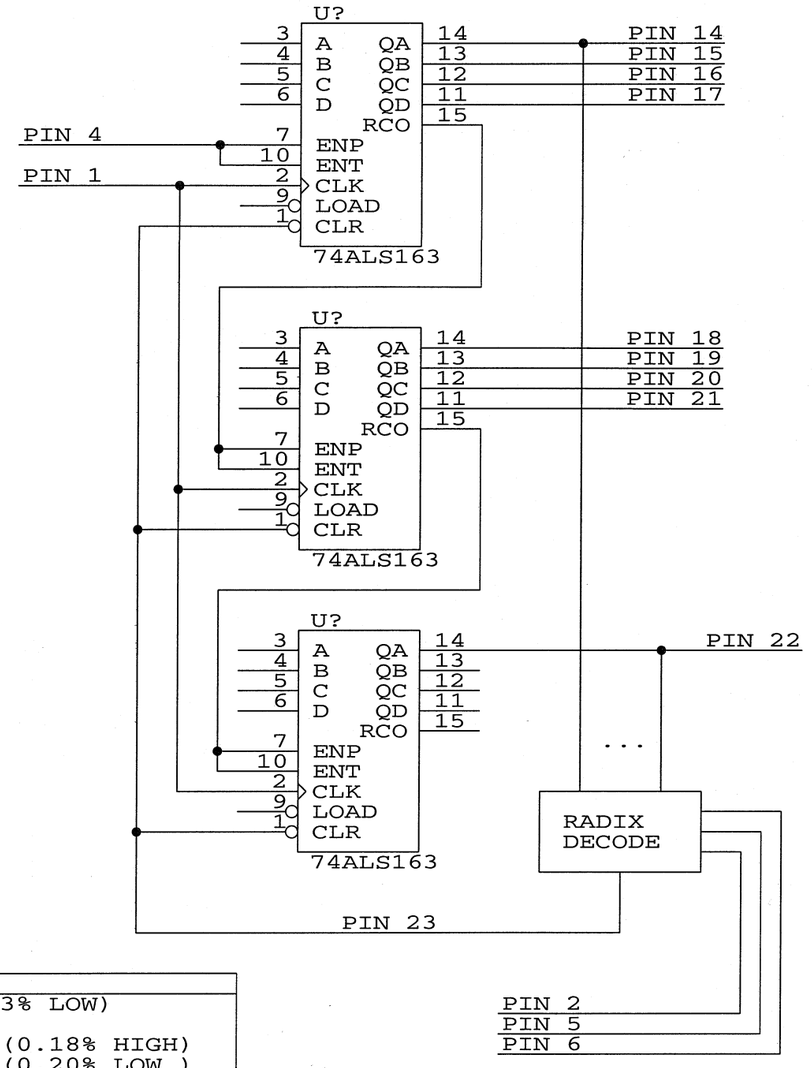


PAL 23F
PHASE LOCK LOOP VARIABLE RADIX COUNTER

PAL 23F DIVIDES THE OUTPUT OF THE 23G VFO BY A PROGRAMMABLE RADIX AND SUPPLIES THE FREQ IN TO PLL CHIP 22G. THE DIVIDE RADIX IS SUPPLIES BY THREE INPUTS FROM THE MCC MICRO (uRADIX, uP2, AND uP3). THE FUNCTION TABLE BELOW GIVES THE EXACT DIVISION RATIOS AVALIABLE.



23F-6,5,2	23F DIVIDE	PLL FREQ	COMMENT
0,0,0	485	9.001600 MHZ	DEFAULT VLBA (0.00083% LOW)
0,0,1	487	9.038720 MHZ	SPARE
0,1,0	484	8.983040 MHZ	VLBA, SELF TEST (0.18% HIGH)
0,1,0	484	8.983040 MHZ	VLBA, NO SELF TEST (0.20% LOW)
0,1,1	486	9.020160 MHZ	VLBA, NO SELF TEST (0.20% HIGH)
1,0,0	482	8.945920 MHZ	VLBA, SELF TEST (0.23% LOW)
1,0,0	482	8.945920 MHZ	MKIII, NO SELF TEST (0.17% HIGH)
1,0,1	483	8.964480 MHZ	SPARE
1,1,0	480	8.908800 MHZ	MKIII, NO SELF TEST (0.24% LOW)
1,1,0	480	8.908800 MHZ	MKIII, SELF TEST (0.15% HIGH)
1,1,1	478	8.871680 MHZ	MKIII, SELF TEST (0.27% LOW)

PHASE LOCK LOOP VARIABLE RADIX CNTR

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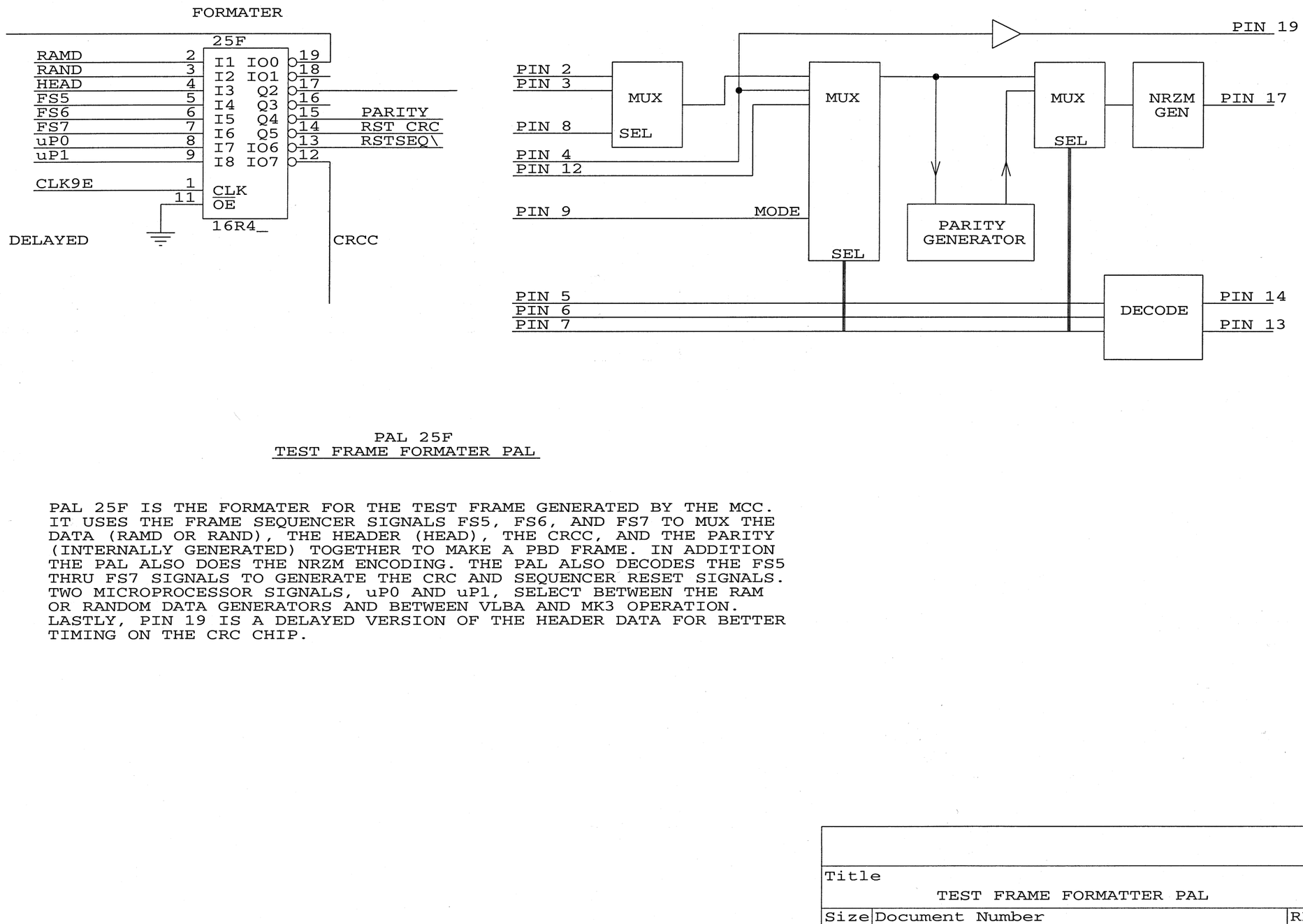

PAL 25F
TEST FRAME FORMATER PAL

PAL 25F IS THE FORMATER FOR THE TEST FRAME GENERATED BY THE MCC. IT USES THE FRAME SEQUENCER SIGNALS FS5, FS6, AND FS7 TO MUX THE DATA (RAMD OR RAND), THE HEADER (HEAD), THE CRCC, AND THE PARITY (INTERNALLY GENERATED) TOGETHER TO MAKE A PBD FRAME. IN ADDITION THE PAL ALSO DOES THE NRZM ENCODING. THE PAL ALSO DECODES THE FS5 THRU FS7 SIGNALS TO GENERATE THE CRC AND SEQUENCER RESET SIGNALS. TWO MICROPROCESSOR SIGNALS, uP0 AND uP1, SELECT BETWEEN THE RAM OR RANDOM DATA GENERATORS AND BETWEEN VLBA AND MK3 OPERATION. LASTLY, PIN 19 IS A DELAYED VERSION OF THE HEADER DATA FOR BETTER TIMING ON THE CRC CHIP.

Title: TEST FRAME FORMATTER PAL		
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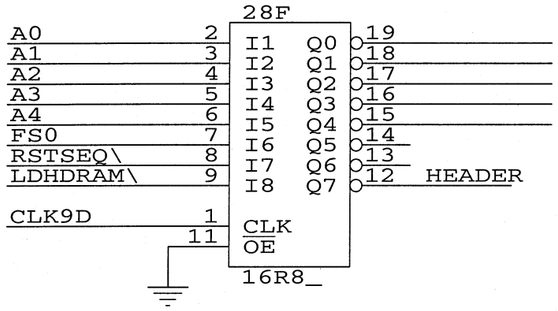
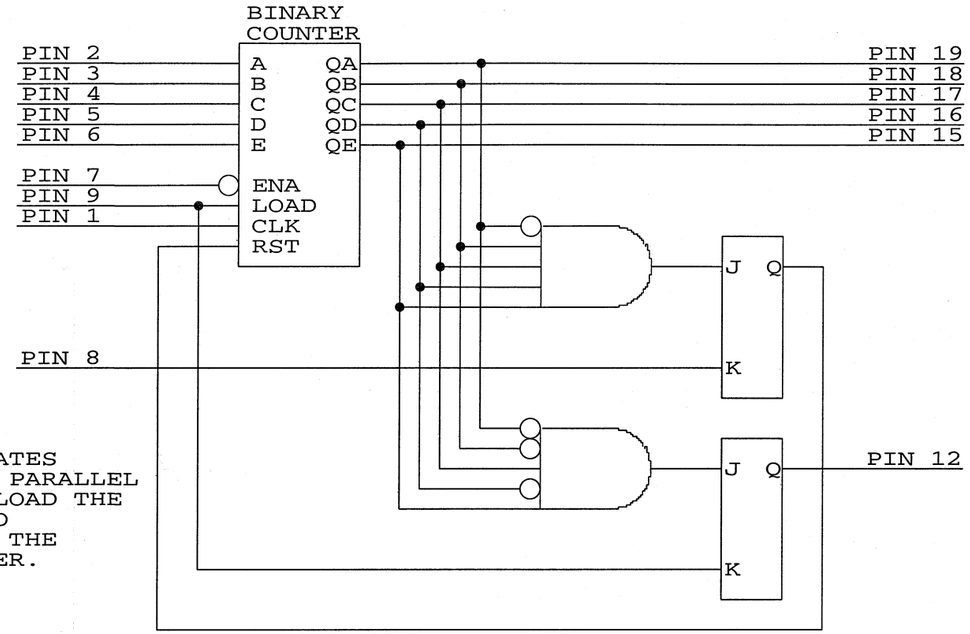


PAL28F
HEADER RAM ADDRESS COUNTER



PAL 28F IS THE ADDRESS COUNTER FOR THE RAM THAT GENERATES THE HEADER IN THE MCC TEST FRAME. THIS COUNTER CAN BE PARALLEL LOADED FROM THE MICROPROCESSOR SO THAT THE MICRO MAY LOAD THE RAM DURING THE DATA PORTION OF THE FRAME. THE PAL ALSO GENERATES A DISCRETE SIGNAL FOR THE MICRO (HEADER) SO THE MICRO WILL KNOW WHEN IT IS SAFE TO LOAD THE NEXT HEADER.

NOTE: LOAD WINS OVER RST

Title: HEADER RAM ADDRESS COUNTER		
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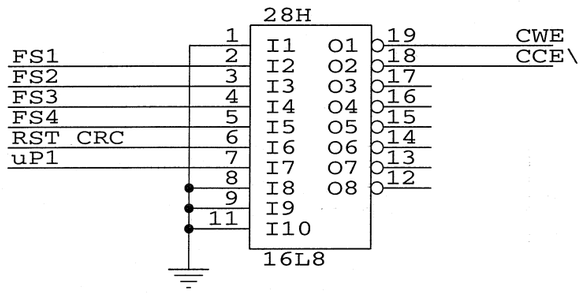
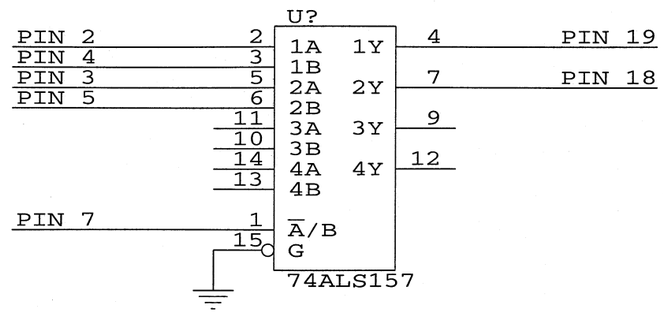


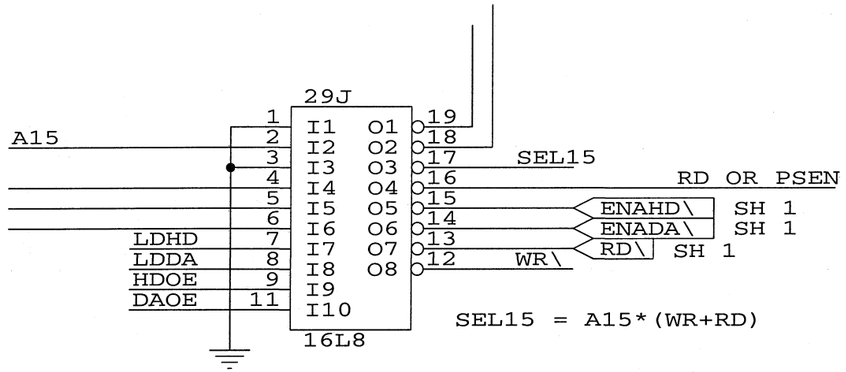


PAL 28H
CRC CONTROL SIGNAL GENERATOR PAL

PAL 28H SWITCHES THE CRC CHIP CWE AND CCE CONTROL SIGNALS BETWEEN VLBA AND MKIII OUTPUTS FROM THE MCC TEST FRAME SEQUENCER. (uP1 = 0 FOR VLBA, = 1 FOR MKIII)

```
CWE     =    FS1  &  !uP1
          #  FS3  &   uP1      ;

CCE     =    FS2  &  !uP1
          #  FS4  &   uP1      ;
```

Title: CRC CONTROL SIGNAL GENERATOR PAL		
Size: A	Document Number: PAL28H.SCH	REV:
Date: May 7, 1997	Sheet 30 of 34	



SEL15 = A15*(WR+RD)

PAL 29J
MISCELLANEOUS MICROPROCESSOR LOGIC PAL

THIS PAL CONTAINS MISCELLANEOUS LOGIC IN THE MICROPROCESSOR PORTION OF THE FFT CONTROL CARD:

PIN 19. THIS PIN IS THE LS245 OUTPUT ENABLE. IT IS ACTIVE (LOW) ALL THE TIME EXCEPT FOR READ OPERATIONS.

PIN 18. THIS PAL OUTPUT SUPPLIES THE DIRECTION SIGNAL FOR THE DATA BUS LS245.

PIN 17. THIS PAL OUTPUT SUPPLIES A GLITCHLESS A15 SIGNAL FOR THE 74LS138 DECODERS.

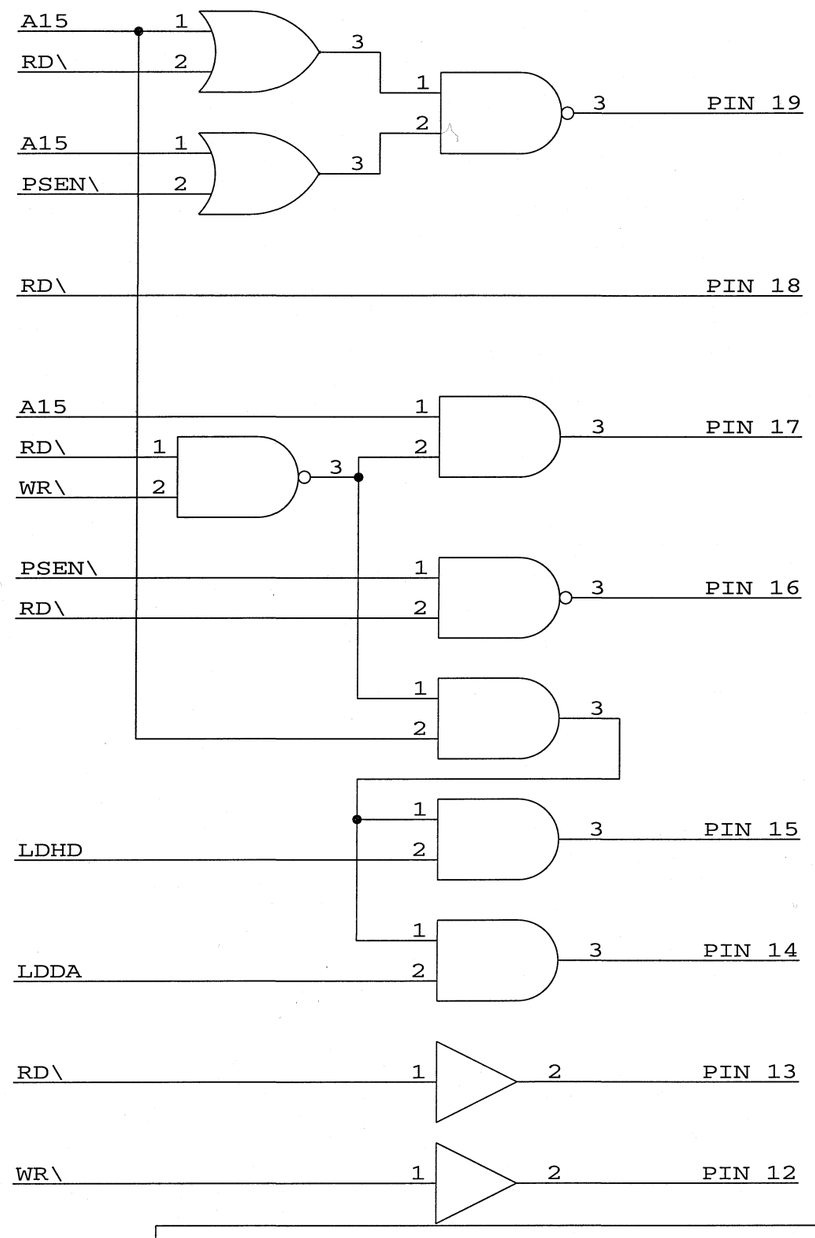
PIN 16. THIS PAL OUTPUT PROVIDES THE RAM MEMORY OUTPUT ENABLE SIGNAL FOR EITHER DATA MEMORY ACCESS (RD) OR FOR PROGRAM MEMORY ACCESS (PSEN).

PIN 15. THIS PAL OUTPUT PROVIDES A DECODE SIGNAL THAT GIVES THE MICRO ASSESS TO THE TEST FRAME HEADER RAM 27F.

PIN 14. THIS PAL OUTPUT PROVIDES A DECODE SIGNAL THAT GIVES THE MICRO ASSESS TO THE TEST FRAME DATA RAM 29F.

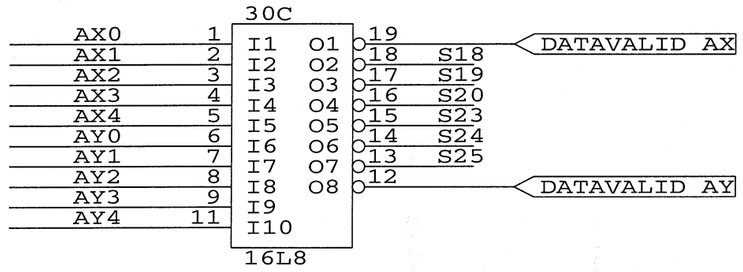
PIN 13. THIS PAL OUTPUT BUFFERS THE MICRO RD\ LINE FOR HIGH FANOUT.

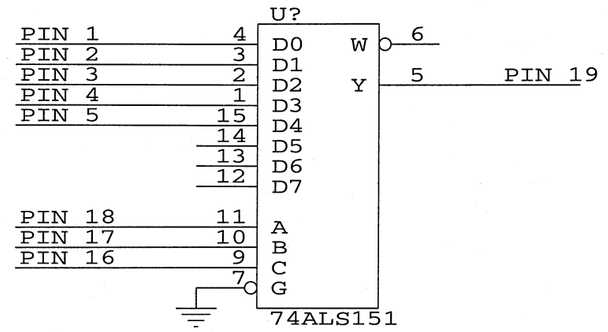
PIN 12. THIS PAL OUTPUT BUFFERS THE MICRO WR\ LINE FOR HIGH FANOUT.



MISC uP LOGIC PAL

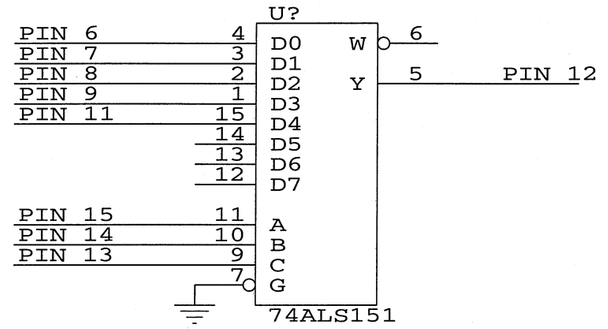
Size	Document Number	REV
A	PAL29J.SCH	
Date: May 7, 1997	Sheet 31 of 34	





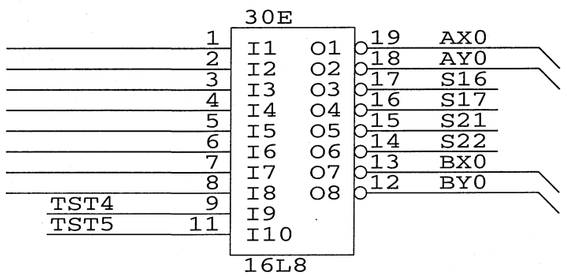
PAL 30C
(ALSO USED FOR PAL 30B)
DUAL 5 INTO 1 MUX

THIS PAL PROVIDES 2 INDEPENDENTLY PROGRAMMABLE 5 INTO 1 MUXES. THESE PALS ALONG WITH THE 30E/29C/29B/29A/30A PALS ARE A DUAL 20 INTO 1 MUX. THE 2 20 INTO 1 MUXES SELECT 2 DATA VALIDS IN ORDER TO FORM A BASELINE DATA VALID BY ANDING THEM TOGETHER.




```
MODE_X = [S20,S19,S18]          ;
MODE_Y = [S25,S24,S23]          ;


VAL_AX  =     AX0  &  (MODE_X == [0,0,0])
          #   AX1  &  (MODE_X == [0,0,1])
          #   AX2  &  (MODE_X == [0,1,0])
          #   AX3  &  (MODE_X == [0,1,1])
          #   AX4  &  (MODE_X == [1,0,0])          ;

VAL_AY  =     AY0  &  (MODE_Y == [0,0,0])
          #   AY1  &  (MODE_Y == [0,0,1])
          #   AY2  &  (MODE_Y == [0,1,0])
          #   AY3  &  (MODE_Y == [0,1,1])
          #   AY4  &  (MODE_Y == [1,0,0])          ;
```

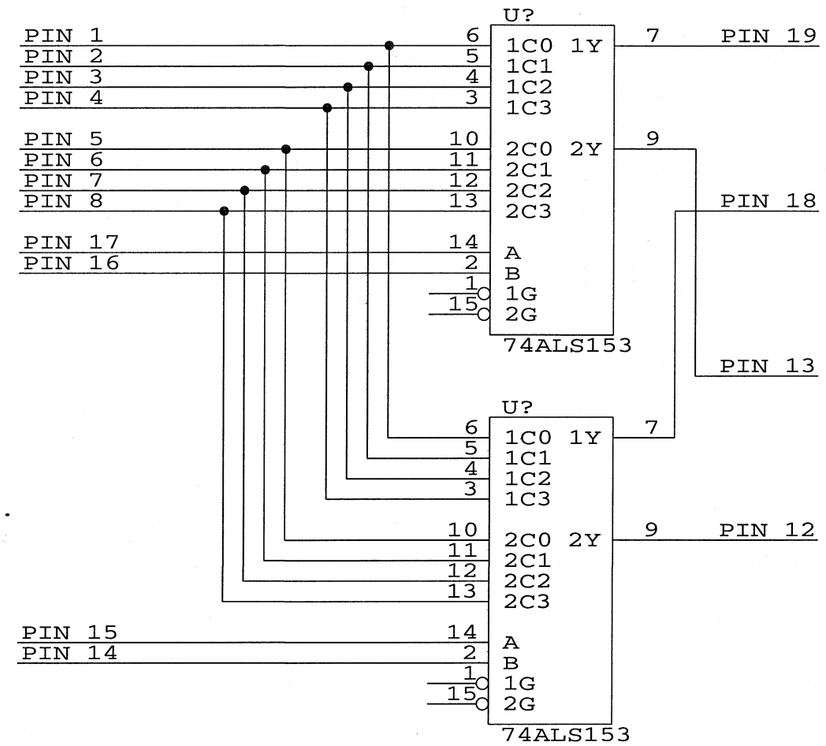
Title: DUAL 5 INTO 1 MUX: PALS 30C AND 30B		
Size: A	Document Number: PAL30C.SCH	REV
Date: May 7, 1997	Sheet 32 of 34	



PAL 30E
(ALSO USED FOR PAL 29C, 29B, 29A ,AND 30A)
DUAL DUAL 4 INTO 1 MUX

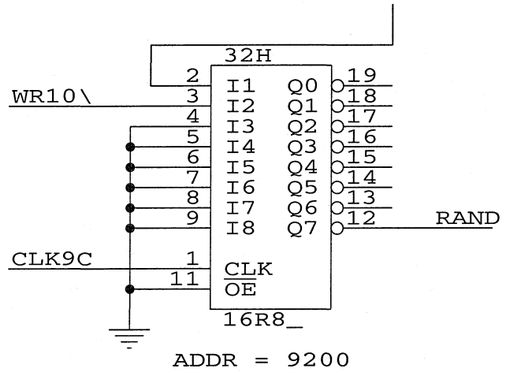
THIS PAL PROVIDES 2 INDEPENDENTLY PROGRAMMABLE DUAL 4 INTO 1 MUXES. ONE OF THE DUAL' ABOVE PRETAINS TO THE 2 CHANNELS (A AND B) OF VALIDS PROVIDED FOR ON AN MCC CARD. THE OTHER DUAL IS FOR THE 2 COORDINATES OF A BASELINE (X AND Y) NEEDED TO GET THE BASELINE VALIDITY. A AND B GET THE SAME MUX SELECT BITS WHILE X AND Y GET DIFFERENT MUX SELECT BITS. THE EQUATIONS BELOW ILLUSTRATE THE PAL FUNCTION.

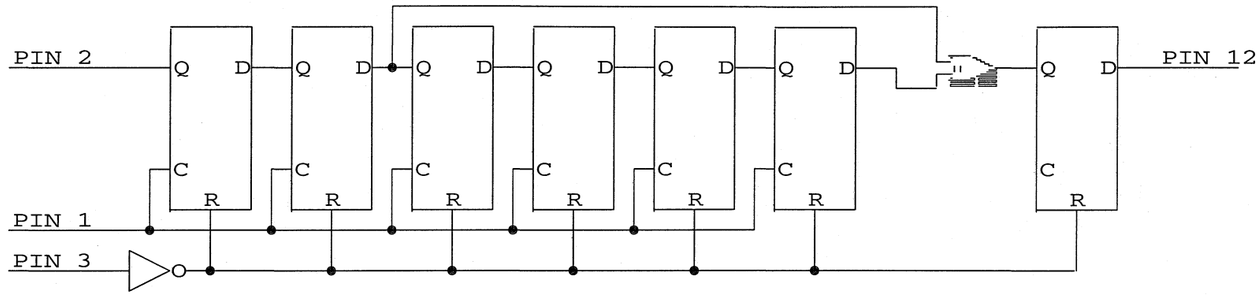
```
MODE_X = [S17,S16]          ;
MODE_Y = [S22,S21]          ;
TEST   = [TST5,TST4]        ;


AX0   =    V0A  &  (MODE_X == [0,0])  &  (TEST == [0,0])
         #  V1A  &  (MODE_X == [0,1])  &  (TEST == [0,0])
         #  V2A  &  (MODE_X == [1,0])  &  (TEST == [0,0])
         #  V3A  &  (MODE_X == [1,1])  &  (TEST == [0,0])
         # (TEST == [1,1])  #  (TEST == [1,0])                ;

AY0   =    V0A  &  (MODE_Y == [0,0])  &  (TEST == [0,0])
         #  V1A  &  (MODE_Y == [0,1])  &  (TEST == [0,0])
         #  V2A  &  (MODE_Y == [1,0])  &  (TEST == [0,0])
         #  V3A  &  (MODE_Y == [1,1])  &  (TEST == [0,0])
         # (TEST == [1,1])                                   ;

BX0   =    V0B  &  (MODE_X == [0,0])  &  (TEST == [0,0])
         #  V1B  &  (MODE_X == [0,1])  &  (TEST == [0,0])
         #  V2B  &  (MODE_X == [1,0])  &  (TEST == [0,0])
         #  V3B  &  (MODE_X == [1,1])  &  (TEST == [0,0])
         # (TEST == [1,1])  #  (TEST == [1,0])                ;

BY0   =    V0B  &  (MODE_Y == [0,0])  &  (TEST == [0,0])
         #  V1B  &  (MODE_Y == [0,1])  &  (TEST == [0,0])
         #  V2B  &  (MODE_Y == [1,0])  &  (TEST == [0,0])
         #  V3B  &  (MODE_Y == [1,1])  &  (TEST == [0,0])
         # (TEST == [1,1])                                   ;
```



NOTE: THE TEST FUNCTION NOT SHOWN ABOVE.

Title: DUAL 4 INTO 1 MUX 30E, 29A, 29B, 29C, 30A		
Size: A	Document Number: PAL30E.SCH	REV:
Date: December 30, 1998	Sheet 33 of 34	





PAL 32H
RANDOM DATA GENERATOR PAL

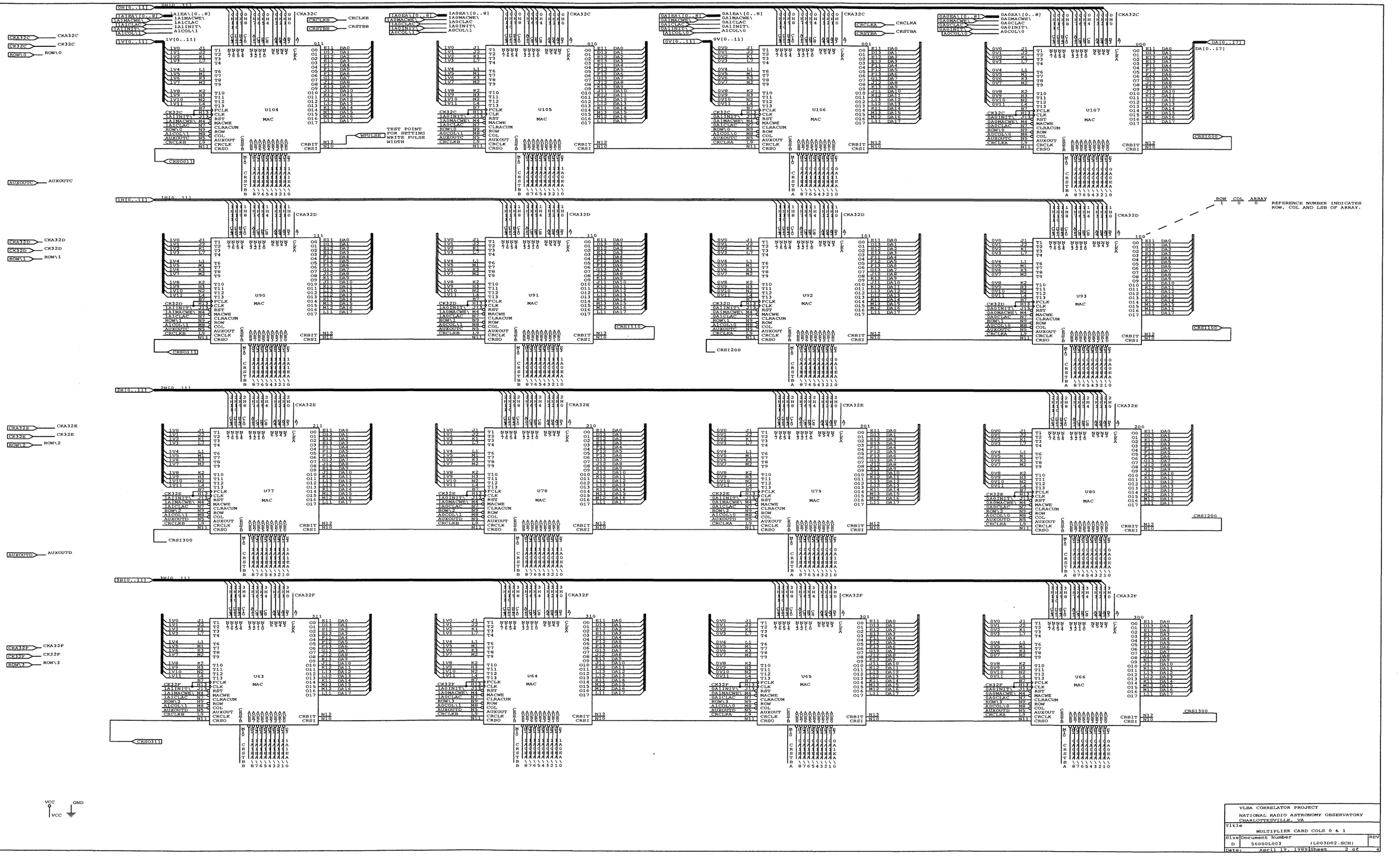
PAL 32H PROVIDES 7 BITS OF A 39 BIT RANDOM DATA GENEARTOR. A MICROPROCESSOR SIGNAL, WR10\, CAN RESET THE DATA GENERATOR TO GET IT OUT OF THE HANG UP STATE.

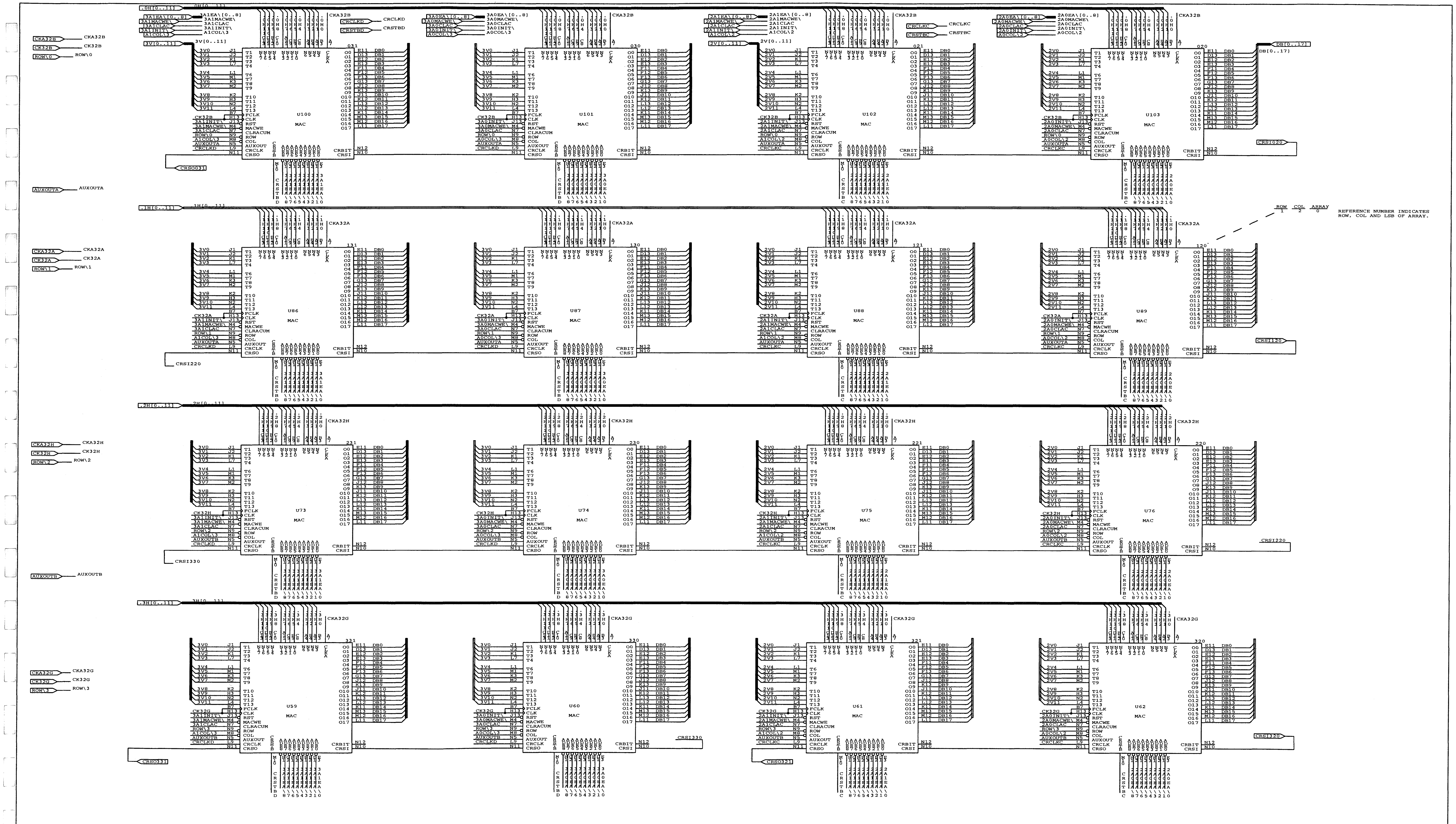
Title: RANDOM DATA GENERATOR PAL		
Size: A	Document Number: PAL32H.SCH	REV:
Date: May 7, 1997	Sheet 34 of 34	

Volume 2 Section 2

Multiply Accumulate Card Drawings

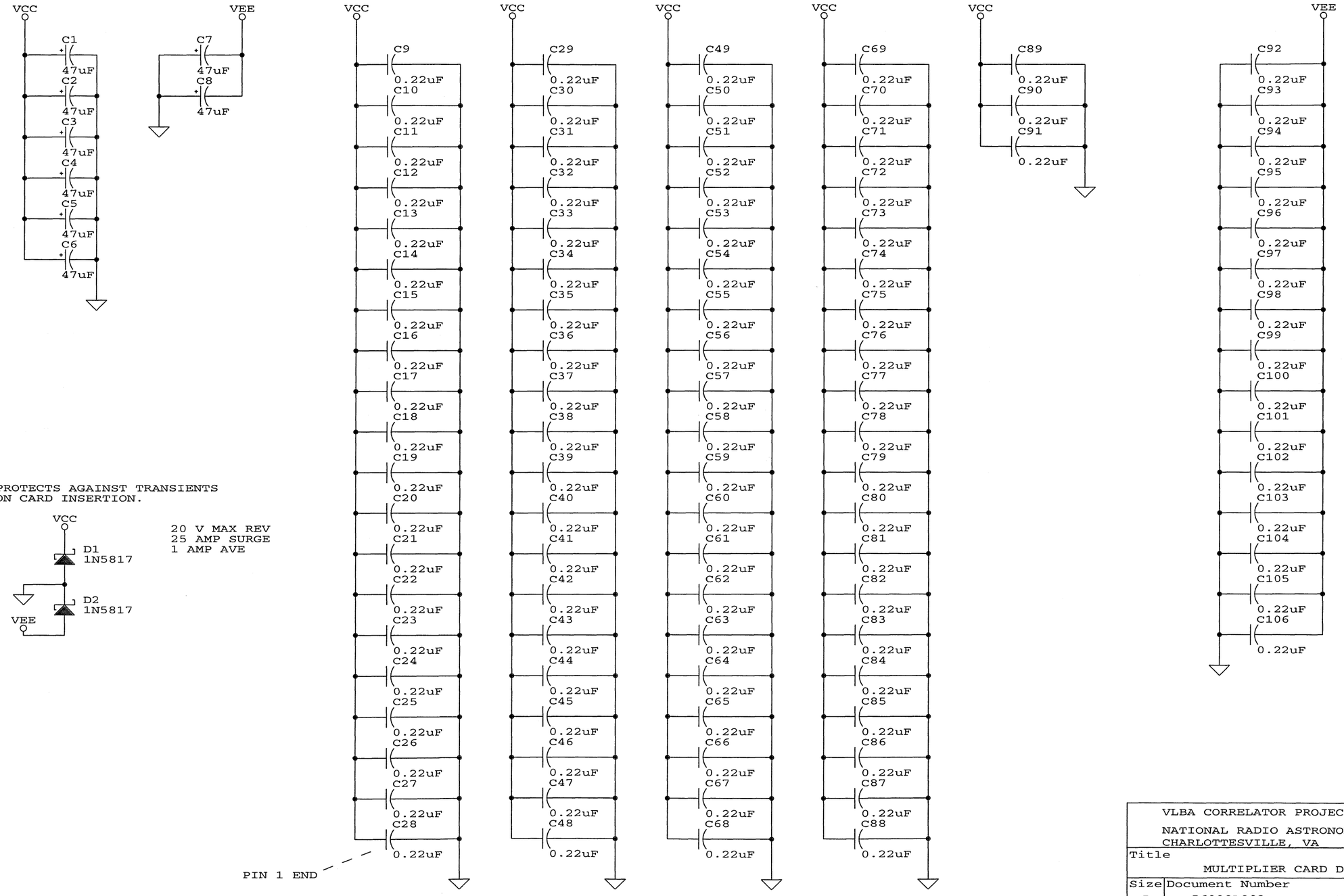
Drawing Number and/or Filename	Title	Nr of Sheets
56000L003 (L003D01.SCH - L003D04.SCH)	MAC Schematics	4
56000Z003 (Z003D01.LAY - Z003D02.LAY)	MAC IC Layouts	2
K029D01.BLK	FFT to MAC interface	1
K030D01.BLK	MAC Block Diagram	1
V009D01.TIM	MAC card edge timing	1


CKA32C
CK32C
ROW\0
AUXOUTC
CKA32D
CK32D
ROW\1
CKA32E
CK32E
ROW\2
AUXOUTD
CKA32F
CK32F
ROW\3
VCC
GND
TEST POINT FOR SETTING WRITE PULSE WIDTH
ROW COL ARRAY
1 0 0
REFERENCE NUMBER INDICATES ROW, COL AND LSB OF ARRAY.
VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA
Title
MULTIPLIER CARD COLS 0 & 1
Size D
Document Number 56000L003 (L003D02.SCH)
REV
Date: April 19, 1989
Sheet 2 of 4



VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title MULTIPLIER CARD COLS 2 & 3		
Size D	Document Number 56000L003 (L003D03.SCH)	REV
Date: April 19, 1989	Sheet 3 of 4	

47 uF VCC BYPASSES 47uF VEE BYPASSES



PROTECTS AGAINST TRANSIENTS
ON CARD INSERTION.

20 V MAX REV
25 AMP SURGE
1 AMP AVE

VLBA CORRELATOR PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title

MULTIPLIER CARD DECOUPLING

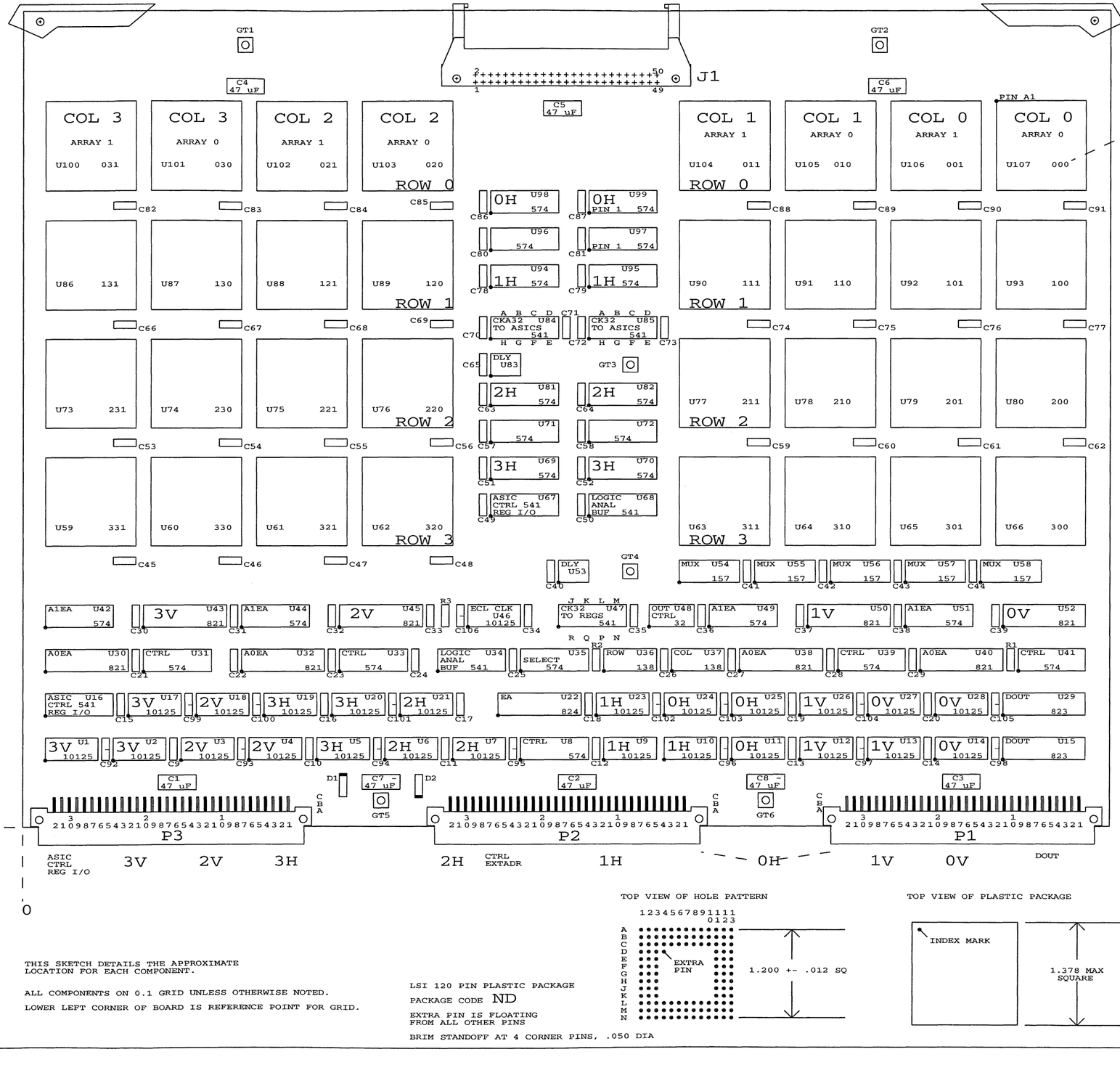
Size	Document Number	REV
B	56000L003 (L003D04.SCH)	
Date: June 12, 1989	Sheet 4 of 4	

NOTE:
CHIP OUTLINES REPRESENT THE IC PIN FOOTPRINT, NOT THE PHYSICAL CASE OR SOCKET OUTLINES.

VIEW IS OF COMPONENT SIDE

50 PIN "3M" TYPE CONN, 3433-5303
FOR TEST POINTS

SCANBE S-217 INJECTOR/EJECTOR



ROW COL ARRAY
0 0 0

DIP TYPE MONOLITHIC BYPASS CAPACITORS

PIN ORIENTATIONS:

PIN 1 OF "HORIZONTAL" DIPS IN LOWER LEFT CORNER.

PIN A1 OF ASICS IN UPPER LEFT CORNER.

PIN 1 OF DISCRETE RESISTORS AND BYPASS CAPACITORS IS AT TOP OR LEFT:

PIN 1 END

PIN 1 END

MINUS SIGN INDICATES -5.2V BYPASS

UNMARKED INDICATES +5V BYPASS

ALL ICs ARE SOCKETED

THIS REPRESENTS MOUNTING PAD FOR KEYSTONE TURET #1593-3
6 TOTAL, EACH CONNECTED TO GROUND

ALL DIP ICs SOCKETED:
TI C93xx FAMILY

ALL PGA USE SOCKET PINS:
ADVANCED INTERCONNECTIONS
KD-121-33TG

9U x 280 mm EUROCARD

SEE NRAO DRAWING # 56000M003 FOR MECHANICAL DETAILS OF CARD.

SEE NRAO DRAWING # A56000B003 FOR BILL OF MATERIALS

REV B: 8-31-89 CMB
SWAPPED C15 WITH C99
SWAPPED C18 WITH C102
REVERSED D2
ADDED PIN 1 DOTS AT U1-U15

REV C: 8-10-90 CMB
COPIED SHEET 1 TO SHEET 2 AND REVISED SHEET 2 SPECIFICALLY FOR BOARD ASSEMBLY DETAILS.
ADDED GT1-GT6 REFERENCE DESIGNATIONS.

THIS SKETCH DETAILS THE APPROXIMATE LOCATION FOR EACH COMPONENT.

ALL COMPONENTS ON 0.1 GRID UNLESS OTHERWISE NOTED.

LOWER LEFT CORNER OF BOARD IS REFERENCE POINT FOR GRID.

LSI 120 PIN PLASTIC PACKAGE

PACKAGE CODE ND

EXTRA PIN IS FLOATING FROM ALL OTHER PINS

BRIM STANDOFF AT 4 CORNER PINS, .050 DIA

TOP VIEW OF HOLE PATTERN

TOP VIEW OF PLASTIC PACKAGE

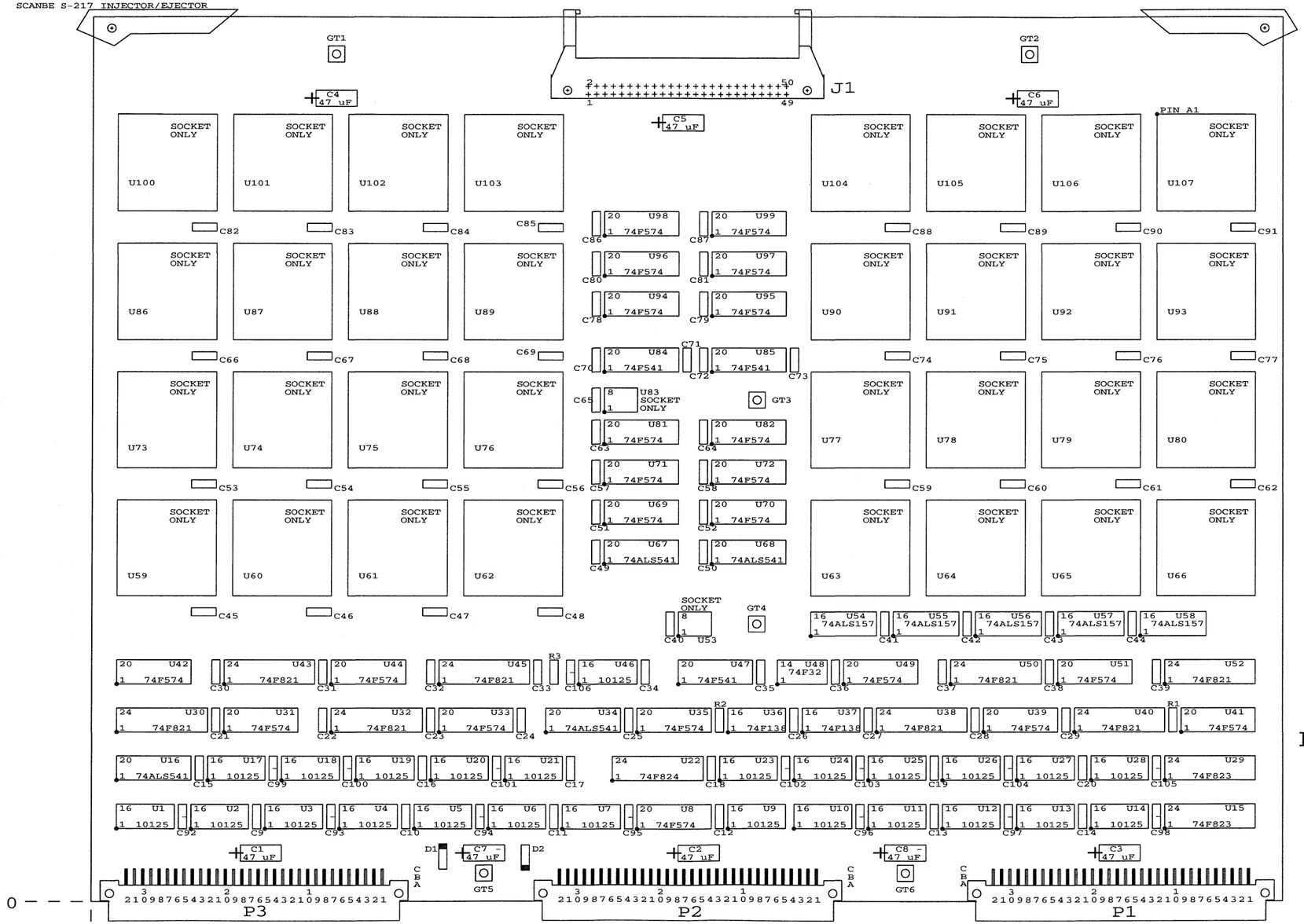
VLBA CORRELATOR PROJECT		
NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title: MULTIPLIER CARD COMPONENT LAYOUT SKETCH		
Size: C	Document Number: 56000Z003 (Z003D01.LAY)	REV: C
Date: August 21, 1990	Sheet 1 of 2	

NOTE:
CHIP OUTLINES REPRESENT THE
IC PIN FOOTPRINT, NOT THE PHYSICAL
CASE OR SOCKET OUTLINES.

J1 IS A 50 PIN "3M" TYPE CONN, 3433-1403.
THE TWO MOUNTING HOLES FOR J1 ON THE PC BOARD
ARE NOT CORRECTLY LOCATED.
THE CONNECTORS SUPPLIED BY NRAO TO THE BOARD ASSEMBLER
WILL HAVE THE MOUNTING HOLES DRILLED OUT SO THAT
THEY MAY BE MOUNTED.

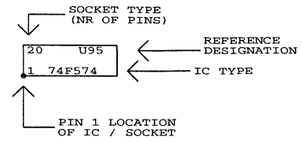
VIEW IS OF COMPONENT SIDE

SCANBE S-217 INJECTOR/EJECTOR



0 — — —
|
|
.
0

EXAMPLE OF DIP IC DETAILS:



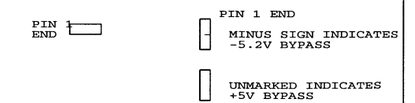
DIP TYPE MONOLITHIC
BYPASS CAPACITORS

PIN ORIENTATIONS:

PIN 1 OF "HORIZONTAL" DIPS
IN LOWER LEFT CORNER.

PIN A1 OF ASICS IN UPPER LEFT CORNER.

PIN 1 OF DISCRETE RESISTORS AND
BYPASS CAPACITORS IS AT TOP OR LEFT:



ALL ICs ARE SOCKETED

THIS REPRESENTS MOUNTING PAD FOR
KEYSTONE TURRET #1593-3
6 TOTAL, EACH CONNECTED TO GROUND

ALL DIP ICs SOCKETED:
TI C93xx FAMILY

ALL PGA USE SOCKET PINS:
ADVANCED INTERCONNECTIONS
KD-121-33TG

THE NOTATION "SOCKET ONLY" INDICATES THAT
THE BOARD ASSEMBLER WILL INSTALL THE
IC SOCKET, BUT NRAO WILL INSTALL THE IC.

ALL OTHER IC's WILL BE INSTALLED BY THE
ASSEMBLER.

NOTE:

BOARD ASSEMBLER DOES
NOT NEED SHEET 1 OF
THIS DRAWING

9U x 280 mm EUROCARD

SEE NRAO DRAWING # 56000M003 FOR
MECHANICAL DETAILS OF CARD.

SEE NRAO DRAWING # A56000B003 FOR
BILL OF MATERIALS

REV B: 8-31-89 CMB
SWAPPED C15 WITH C99
SWAPPED C18 WITH C102
REVERSED D2
ADDED PIN 1 DOTS AT U1-U15

REV C: 8-10-90 CMB
COPIED SHEET 1 TO SHEET 2 AND REVISED
SHEET 2 SPECIFICALLY FOR BOARD
ASSEMBLY DETAILS.
ADDED GT1-GT6 REFERENCE DESIGNATIONS.

THIS SKETCH DETAILS THE APPROXIMATE
LOCATION FOR EACH COMPONENT.

ALL COMPONENTS ON 0.1 GRID UNLESS OTHERWISE NOTED.

LOWER LEFT CORNER OF BOARD IS REFERENCE POINT FOR GRID.

SILK SCREEN IDENTIFIES EXACT PHYSICAL LOCATION OF PARTS

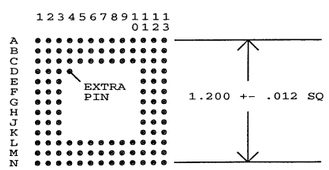
LSI 120 PIN PLASTIC PACKAGE

PACKAGE CODE ND

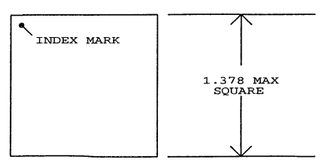
EXTRA PIN IS FLOATING
FROM ALL OTHER PINS

BRIM STANDOFF AT 4 CORNER PINS, .050 DIA

TOP VIEW OF HOLE PATTERN

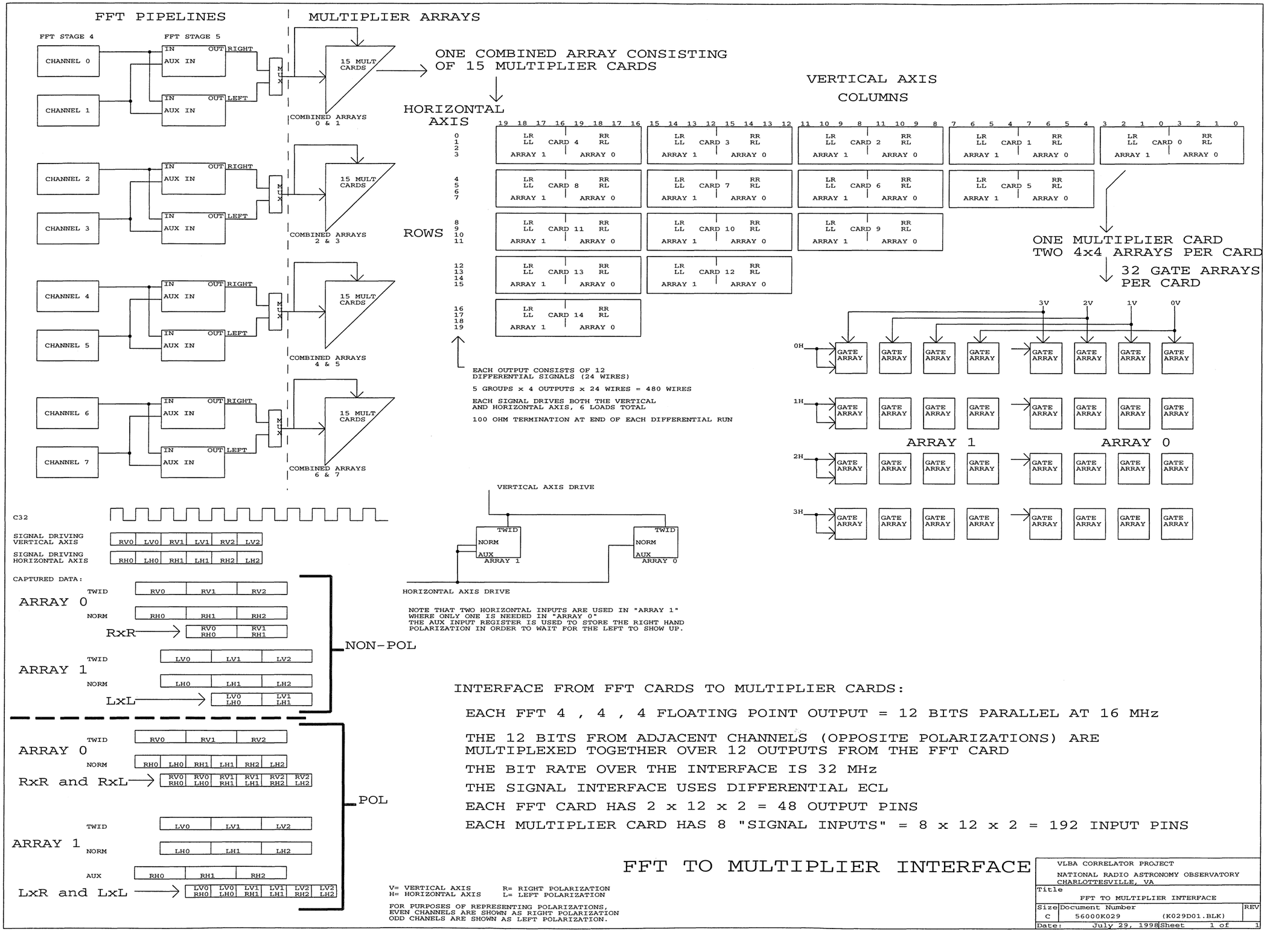


TOP VIEW OF PLASTIC PACKAGE



VLBA CORRELATOR PROJECT		
NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title: MULTIPLIER CARD ASSEMBLY DETAILS		
Size: C	Document Number: 560002003 (Z003D02.LAY)	REV: C
Date: August 21, 1990	Sheet 2 of 2	

FFT TO MULTIPLIER INTERFACE



INTERFACE FROM FFT CARDS TO MULTIPLIER CARDS:

EACH FFT 4 , 4 , 4 FLOATING POINT OUTPUT = 12 BITS PARALLEL AT 16 MHz

THE 12 BITS FROM ADJACENT CHANNELS (OPPOSITE POLARIZATIONS) ARE MULTIPLEXED TOGETHER OVER 12 OUTPUTS FROM THE FFT CARD

THE BIT RATE OVER THE INTERFACE IS 32 MHz

THE SIGNAL INTERFACE USES DIFFERENTIAL ECL

EACH FFT CARD HAS 2 x 12 x 2 = 48 OUTPUT PINS

EACH MULTIPLIER CARD HAS 8 "SIGNAL INPUTS" = 8 x 12 x 2 = 192 INPUT PINS

V= VERTICAL AXIS
H= HORIZONTAL AXIS
R= RIGHT POLARIZATION
L= LEFT POLARIZATION

FOR PURPOSES OF REPRESENTING POLARIZATIONS, EVEN CHANNELS ARE SHOWN AS RIGHT POLARIZATION ODD CHANELS ARE SHOWN AS LEFT POLARIZATION.

VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA	
Title	FFT TO MULTIPLIER INTERFACE
Size: C	Document Number: 56000K029 (K029D01.BLK) — REV:
Date: July 29, 1998	Sheet 1 of 1

MULTIPLIER CARD BLOCK DIAGRAM

ENLARGED VIEW
OF MAIN I/O SIGNALS
FOR VLBA1 USED IN MAC MODE

TWID
4,4,4
4,4,4
15,15,6
ROW
COL
AUXOUT
(9 BITS)
CTRL EXTADR

NOTE: THE PHYSICAL LAYOUT OF VLBA1 CHIPS ON THE CARD IS NOT THE SAME AS THE LOGICAL ARRANGMENT BELOW. SEE L003D01.SCH (MAC SCHEMATIC SHEET 1) FOR THE PHYSICAL LAYOUT

ANTENNAS 0-3, VERTICAL AXIS (COLUMNS 0-3)

12 BITS PER ANTENNA BUS * 4 BUSES * 2 WIRES EACH (DIFFERENTIAL) = 96 INPUT PINS

96

ECL TO TTL TRANSLATORS AND REGISTERS

ANT 3 VERT AXIS | ANT 2 VERT AXIS | ANT 1 VERT AXIS | ANT 0 VERT AXIS

12 3V | 12 2V | 12 1V | 12 0V

(CLOCKS OUT REG)
STAREAD

ARRAYS 0 AND 1 COLUMNS 2 AND 3
ARRAYS 0 AND 1 COLUMNS 0 AND 1
18 BIT 2 TO 1 MUX
OUT REG
18
CARD OUTPUT DATA
CARD OUT ENABLE

18 BIT TRI-STATE BUS (TWO BUSES TOTAL ON CARD)

ANTS 0-3 HORIZ AXIS
96
ROWS 0-3
ECL TO TTL AND REGS

0H 12
1H 12
2H 12
3H 12

CARDS ON THE ARRAY DIAGONAL ARE PARTIALLY POPULATED

SERIAL CONTROL WORD DAISY CHAIN

ARRAY 1

L*L and L*R

ONE BIT DELAY TO ARRAY 1

REGS

ARRAY 0

R*R and R*L

EXTADR (9 BITS)
INIT
CLAC
MACWE
STAREAD
CARDSEL
ROW 0-3
COL 0-3
ARRAY
AUXOUT
CLK

REGS
REGS
REGS

EXTADR
INIT
CLAC (CLEAR ACCUMULATOR)
MACWE (READOUT STROBE)
CAPTURED STAREAD (SHORT TERM ACCUM READ CYCLE)
CARD OUT ENABLE

ROW & COL DECODE FOR RESULT READOUT

ROW AND COL DECODES SELECT A SINGLE VLBA1 ASIC IF THIS CARD IS SELECTED

AUXOUT SELECTS THE 18 BIT PORTION OF THE 36 BIT RESULT

HIGH FOR ONE 32 MHz PERIOD
LOW FOR SEVEN PERIODS

IF SELECTED HERE
ASIC ENA HERE
CARD ENA HERE

IF AN 18 BIT RESULT FROM A SINGLE ASIC IS SELECTED AT THE RISING EDGE OF STAREAD THEN THAT ASIC IS ENABLED ON THE CARD DURING THE FOLLOWING LOW PORTION OF THE STAREAD CYCLE, AND CLOCKED INTO THE OUTPUT REGISTER ON THE NEXT RISING EDGE. THE RESULT IS ENABLED AT THE CARD OUTPUT DURING THE NEXT LOW PORTION OF STAREAD

3V 2V 1V 0V

0H 12 bits per input
1H 24 pins per input
2H 192 pins total
3H for V & H inputs

CK32ECL\
CK32ECL 2 PINS

INIT\ 4 PINS
CLAC
MACWE\
STAREAD

CARDSEL\
ROW0
ROW1
COL0 7 PINS
COL1
ARRAY
AUXOUT

EXTADR[0..8] 9 PINS
CRCLK
CRSI 3 PINS
CRSTB
CRSO
18 PINS
DOUT[0..17]

236 I/O PINS
7 SPARE PINS
18 GND PINS
18 VCC PINS
9 VEE PINS
288 TOTAL PINS

I/O PIN SUMMARY

VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

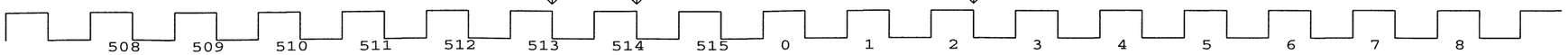
Title: MULTIPLIER CARD BLOCK DIAGRAM

Size	Document Number	REV
C	56000K030 (K030D01.BLK)	
Date: July 29, 1998	Sheet 1 of 1	

ADR FOR READOUT ACCESS AT ASIC EDGE HERE

MACWE AT ASIC EDGE HERE.

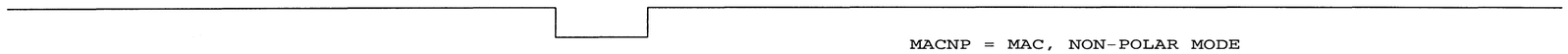
INIT\ AT ASIC EDGE HERE.



VERT AXIS AT TWID INPUT	RV254	LV254	RV255	LV255	X	X	X	X	RV0	LV0	RV1	LV1	RV2	LV2	RV3	LV3	
MACNP A0 & A1																	
HORIZ AXIS AT NORM INPUT	RH254	LH254	RH255	LH255	X	X	X	X	RH0	LH0	RH1	LH1	RH2	LH2	RH3	LH3	
VERT AXIS AT TWID INPUT	F0RV127	F0LV127	F1RV127	F1LV127	X	X	X	X	F0RV0	F0LV0	F1RV0	F1LV0	F0RV1	F0LV1	F1RV1	F1LV1	
MACP A0 & A1																	
HORIZ AXIS AT NORM INPUT	F0RH127	F0LH127	F1RH127	F1LH127	X	X	X	X	F0RH0	F0LH0	F1RH0	F1LH0					
READ ADR AT ASIC INPUT MACNP ARRAY 0	254	RD254	255	RD255	X	ACCESS	X	X	0	RD0	1	RD1	2	RD2	3	RD3	4
READ ADR AT ASIC INPUT MACP ARRAY 0	254	RD254	RD255	255	X	ACCESS	X	X	0	RD0	RD1	1	2	RD2	RD3	3	4

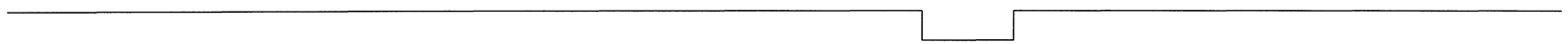
NOTE: SAME ADR SEQUENCE FOR BOTH MACNP AND MACP.
"RD" IS USED TO INDICATE WHEN THE ADR IS USED FOR AN ACTUAL READ IN EACH CASE.

MAC WE\ AT ASIC INPUT A0



ADR FOR MAC WE\ INJECTED INTO EXT ADR STREAM HERE A0 — ACCESS

INIT\ AT ASIC INPUT A0



MACNP = MAC, NON-POLAR MODE

MACP = MAC, POLAR MODE

THIS SECTION IS THE TIMING AT THE ASIC PINS

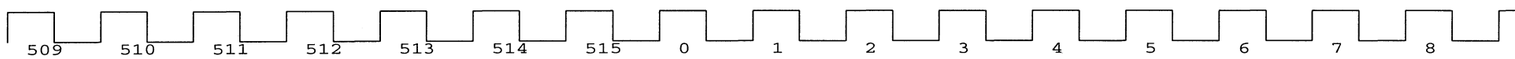
RV254 = RIGHT POLARIZATION VERTICAL AXIS SPECTRAL POINT NUMBER 254

LH254 = LEFT POLARIZATION HORIZONTAL AXIS SPECTRAL POINT NUMBER 254

F0RV127 = FFT #0 RIGHT POLARIZATION VERTICAL AXIS SPECTRAL POINT NUMBER 127

POLAR MODE REQUIRES FFT SIZE <= 256 SO THERE ARE "ADJACENT FFTS" FFT #0 AND #1 IN THIS EXAMPLE

CLK CYCLES COUNTED AT CARD EDGE

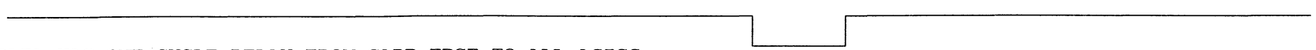


VERT AXIS AT CARD EDGE	LV254	RV255	LV255	X	X	X	X	RV0	LV0	RV1	LV1	RV2	LV2	RV3	LV3	
MACNP																
HORIZ AXIS AT CARD EDGE	LH254	RH255	LH255	X	X	X	X	RH0	LH0	RH1	LH1	RH2	LH2	RH3	LH3	
VERT AXIS AT CARD EDGE	F0LV127	F1RV127	F1LV127	X	X	X	X	F0RV0	F0LV0	F1RV0	F1LV0	F0RV1	F0LV1	F1RV1	F1LV1	
MACP																
HORIZ AXIS AT CARD EDGE	F0LH127	F1RH127	F1LH127	X	X	X	X	F0RH0	F0LH0	F1RH0	F1LH0					
EXT ADR SEQUENCE AT CARD EDGE	255	255	X	ACCESS	X	X	0	0	1	1	2	2	3	3	4	4

MAC WE\ AT CARD EDGE

ADR FOR MAC WE\ INJECTED INTO EXT ADR STREAM HERE — ACCESS

INIT\ AT CARD EDGE



THIS SECTION IS THE CARD EDGE TIMING DERIVED FROM THE ASIC PIN TIMING ABOVE

NOTE:
ADR SEQ IS 0-255 FOR BANK 0
256-511 FOR BANK 1

MSB OF ADR IS BANK SWITCH BIT

IN GAP, X INDICATES ADR IS DON'T CARE, EXCEPT FOR MSB WHICH MUST BE SAME AS IN REST OF CYCLE.

NOTE: DATA HAS ONE CYCLE DELAY FROM CARD EDGE TO ALL ASICS.

INIT\, EXTADR, MAC WE\, AND CL ACC ALL HAVE TWO CYCLE DELAY FROM CARD EDGE TO ASICS IN ARRAY 0, AND THREE CYCLE DELAY TO ARRAY 1.

Title: MAC CARDEDGE TIME		
Size: B	Document Number: V009D01.TIM	REV
Date: August 4, 1998	Sheet 1 of 1	

Volume 2 Section 3

Long Term Accumulator Card Drawings

Drawing Number and/or Filename	Title	Nr of Sheets
56000L024		
(L024D01.SCH - L024D04.SCH)	LTA Schematics	4
(L024D05.DOC - L024D10.DOC)	LTA blk diag & timings	6
(L024D11.XIL - L024D15.XIL)	LTA Xilinx dwgs	5
56000Z015		
(Z015D01.LAY - Z015D06.LAY)	LTA IC layout & adapters	6

FFT CYCLE SEQUENCER

FRINGE CYCLE/INTEGRATION CYCLE SEQUENCER

HCB
TARGET INTERFACE

ubeFPMD HAS HIGHEST PRIORITY
TO USE THE BACKEND ACCESS
WINDOW TO LOAD THE FP CHIP
MODE REGISTER
ultaoE\ USED FOR 8751
BACKEND WRITE AND FOR
FP CHIP MODE LOAD

S[40..42] & ROST	ADR SELECT	ASEL[0..2]
0	ROW fe RD/WR	0 (default)
1	COL fe READ	1
2	COL fe WRITE	2
3	ROW be READ	3
4	COL be READ	4
5	ube RD/WR	5
6	ube RD/WR	6
7	neither ROW refresh	7
4	neither ROW refresh	7
5	RFRSH RQST ON	0
6	spare	0
7	spare	0

S36	S35	S34	FUNCTION
0	0	0	IDLE
1	0	1	WR FOR BSLINES 0-7
0	1	0	WR FOR BE ACCESS
1	0	1	MAC FIFO RST, RNDRST & SO INH
1	0	0	MACFIFOSO UN-INHIBIT
0	1	1	LAST WINDOW ON
0	1	0	LAST WINDOW OFF
1	1	1	MAC FIFO RST, RNDRST, SO INH AND WR FOR BE

rfrshR	beR	ubeR	lastWINDOW	RQST HONORED
1	X	X	1	REFRESH
0	1	X	1	BACKEND RQST
0	0	1	1	8751
0	0	0	1	REFRESH

beR	rfrshR	ubeR	lastWINDOW	RQST HONORED
1	X	X	0	BACKEND RQST
0	1	X	0	REFRESH
0	0	1	0	8751
0	0	0	0	REFRESH

S23	S22	
0	0	IDLE
0	1	RSTa
1	0	ENBb or RSTb
1	1	spare

LS2	LS1	LS0	FFT CYCLE TYPE
0	0	0	NO ACCUMULATIONS
0	0	1	NORMAL RESULTS
0	1	0	SELF TEST RESULTS
0	1	1	NORMAL or SELF TEST RESULTS
1	0	0	NO ACCUMULATIONS, RESET MAC FIFO
1	0	1	spare
1	1	0	spare
1	1	1	spare

LS15	LS14	FUNCTION
0	0	IDLE
0	1	RST LTA & FIR IF SELF TEST
1	0	(spare)
1	1	RST FIR

PAL AT 15C WILL DECODE
(SELFTEST & STATE 1) TO
SPECIFY RESET OF BOTH LTA AND FIR.
IF LTA AND FIR NEED THIS IN DIFFERENT
FFT CYCLES, THE PAL WILL BE CHANGED
TO ALSO USE STATE 2.
STATE 3 WILL ONLY OCCUR WHEN NOT
SELFTEST.

LS4	LS3	COUNTER FUNCTION
0	0	IDLE
0	1	RESET RESULT AND HBL
1	0	INCR RESULT AND RESET HBL
1	1	spare

HBL IS INCREMENTED EVERY FFT CYCLE
EXCEPT WHEN BEING RESET

I5 FP27	I4 FP26	I3 FP25	I2 FP24	I1 FP23	I0 FP22	
0	0	0	0	0	0	F' = P
0	0	0	0	0	1	F' = P' + T'
X	1	0	1	1	1	LOAD MODE REG

OE\ FOR WRITING TO DRAM OR FP MODE ultaOE\

CLK\ FOR DATA FROM DRAM ultaWRSTB\

FP CHIP LOAD MODE INSTRUCTION IS CLOCKED INTO THE CHIP ON THE SAME FPCLK THAT CLOCKS THE MODE BITS INTO THE CHIP.

SELFTEST FORCES CLAC TO OCCUR

ADDRESSES TO be RAMS:

ADDRESSES TO fe RAMS:

64 BIT PATH FOR WRITING TO DRAM OR FP CHIP MODE

64 BIT PATH FOR READING DRAM

20 BIT ADR FOR 8751 TO READ/WRITE DRAM

FP[0..38] CONFIGURES THE 29C327 CHIPS.

RAM WRITE ENABLES AND CHIP SELECTS

BE, FE, SUBARRAY AND BASELINE RAM ADDRESSES

TARGET WRITES TO MASTER WR\HCB (WR\8405)

TARGET READS FROM MASTER RD\HCB (RD\8405)

MASTER RESETS TARGET HCBRST

MASTER INTERUPTS TARGET HCBIRQ\

OUTPUT TO HCB

DATA FROM MASTER IS RDY (LOW TRUE)

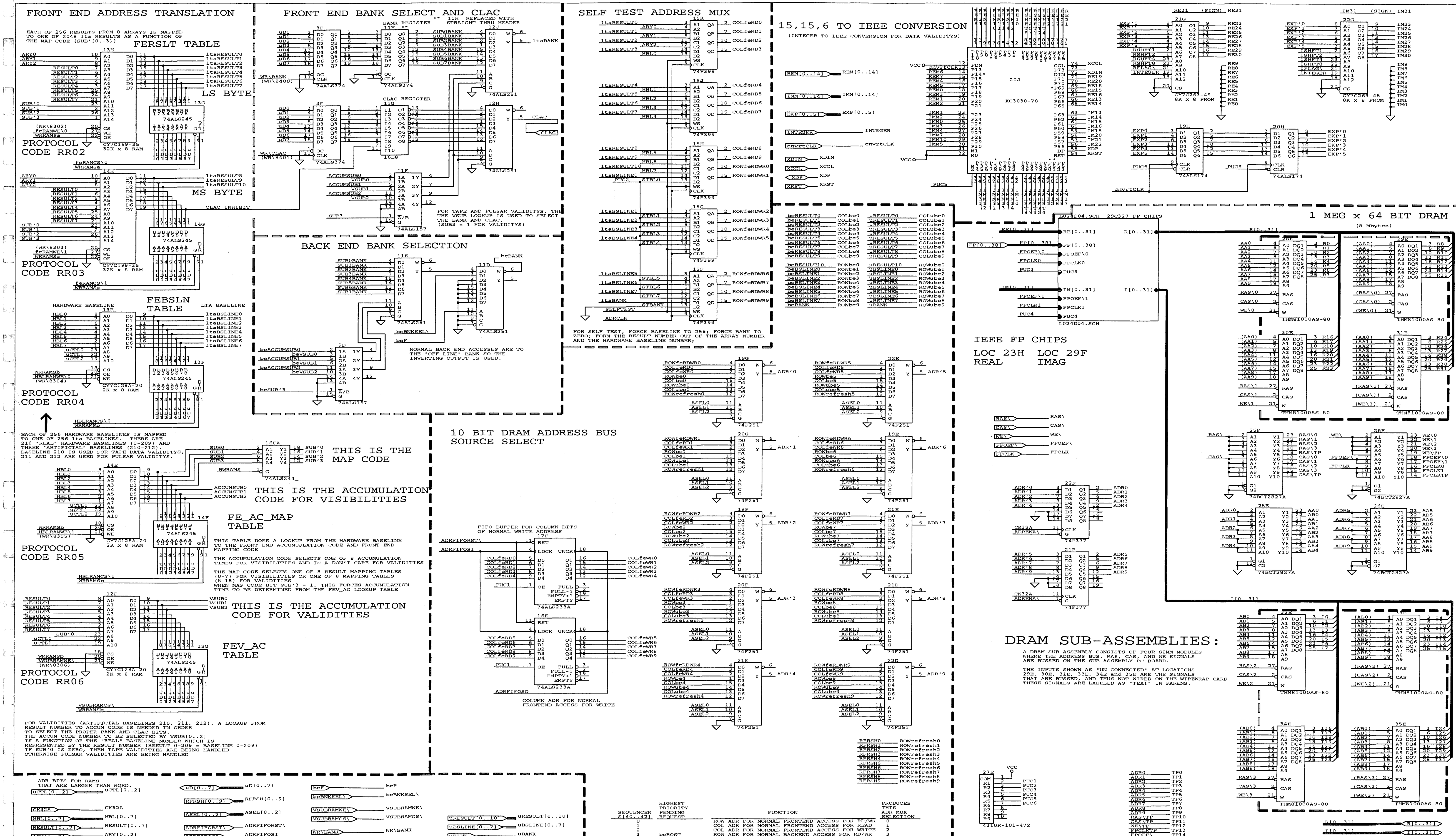
CLR TO SEND TO MASTER (LOW TRUE)

VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: LTA 8751 AND SEQUENCERS

Size: D | Document Number: 56000L024 (L024D02.SCH) | REV:

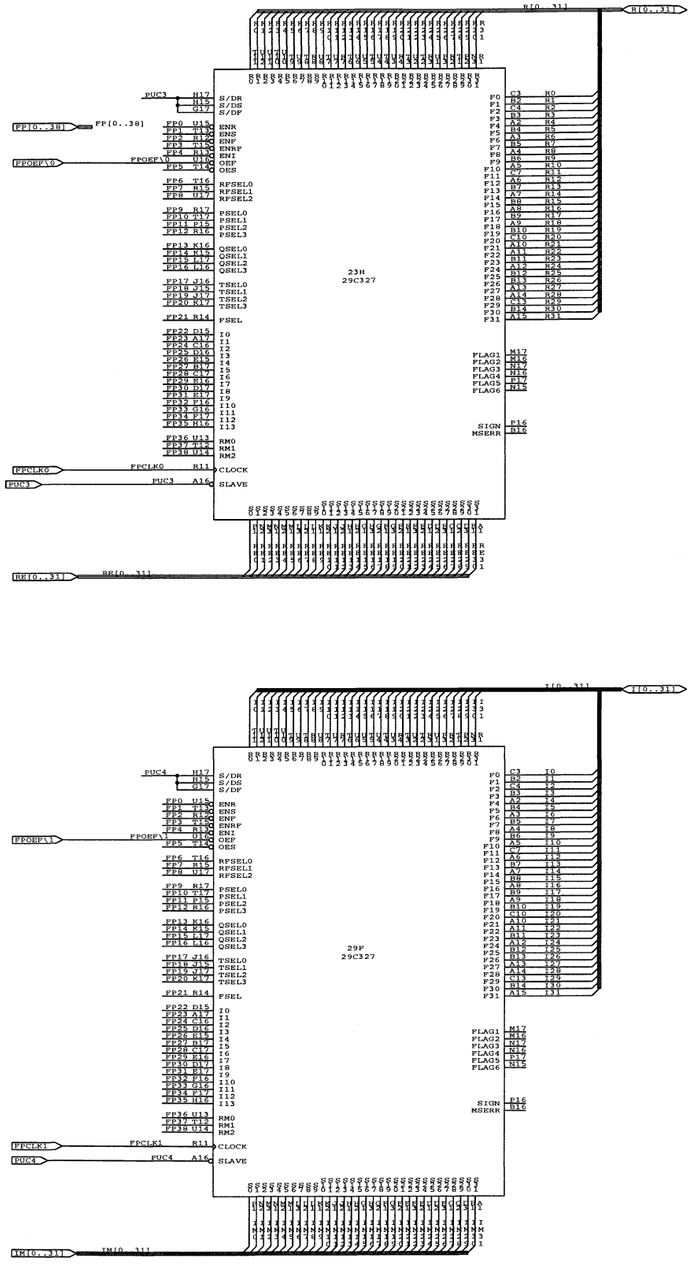
Date: November 19, 1997 | Sheet 2 of 15

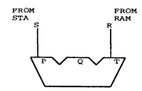


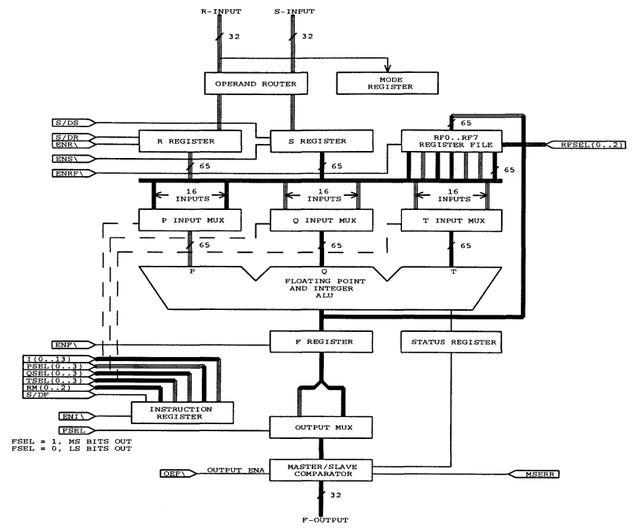
VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: LTA ADR CTRL, IEEE CNVRT, FP CHIPS, DRAM

Size	Document Number		REV
D	56000L024	(L024D03.SCH)	
Date: November 5, 1998	Sheet 3 of 15		





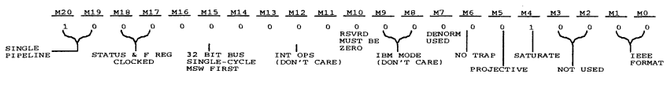


I5	I4	I3	I2	I1	I0	HEX	OPERATION (FLOATING POINT)
0	0	0	0	0	0	00	P
0	0	0	0	0	1	01	P + T
0	0	0	0	1	0	02	P * Q
0	0	0	0	1	1	03	COMPARE P AND T
0	0	0	1	0	0	04	MAX P, T
0	0	0	1	0	1	05	MIN P, T
0	0	0	1	1	0	06	CONVERT T TO INTEGER
0	0	0	1	1	1	07	SCALE T TO INTEGER BY Q
0	0	1	0	0	0	08	(P * Q) + T
0	0	1	0	0	1	09	ROUND T TO INTEGRAL VALUE
0	0	1	0	1	0	0A	RECIPROCAL SEED OF P
0	0	1	0	1	1	0B	CONVERT T TO ALTERNATE F, P FORMAT
0	0	1	1	0	0	0C	CONVERT T FROM ALTERNATE F, P FORMAT
0	0	1	1	0	1	0D	
0	0	1	1	1	0	0E	
0	0	1	1	1	1	0F	
I5	I4	I3	I2	I1	I0		OPERATION (INTEGER)
1	0	0	0	0	0	20	F
1	0	0	0	0	1	21	P + T
1	0	0	0	1	0	22	P - T
1	0	0	0	1	1	23	COMPARE P AND T
1	0	0	1	0	0	24	MAX P, T
1	0	0	1	0	1	25	MIN P, T
1	0	0	1	1	0	26	CONVERT T TO INTEGER
1	0	0	1	1	1	27	SCALE T TO INTEGER BY Q
1	0	1	0	0	0	28	
1	0	1	0	0	1	29	
1	0	1	0	1	0	2A	
1	0	1	0	1	1	2B	
1	1	0	0	0	0	30	F OR T
1	1	0	0	0	1	31	P AND T
1	1	0	0	1	0	32	F EXOR T
1	1	0	0	1	1	33	LOGICAL SHIFT P Q PLACES
1	1	0	1	0	0	34	ARITHMETIC SHIFT P Q PLACES
1	1	0	1	0	1	35	FUNNEL SHIFT P-T Q PLACES
1	1	0	1	1	0	36	
1	1	0	1	1	1	37	
X	1	1	0	0	0	18	MOVE P
X	1	1	1	1	1	1F	LOAD MODE REGISTER

SEL3	SEL2	SEL1	SEL0	HEX	P, Q, T INPUT SELECTED
0	0	0	0	00	R REGISTER
0	0	0	1	01	S REGISTER
0	0	1	0	02	ZERO (0000 0000 0000 0000)
0	0	1	1	03	0.5 * (3FE0 0000 0000 0000)
0	1	0	0	04	1 (3FF0 0000 0000 0000)
0	1	0	1	05	2 (4000 0000 0000 0000)
0	1	1	0	06	3 (4080 0000 0000 0000)
0	1	1	1	07	PI ** (4009 21FB 5444 2D18)
1	0	0	0	08	REGISTER FILE 0
1	0	0	1	09	REGISTER FILE 1
1	0	1	0	0A	REGISTER FILE 2
1	0	1	1	0B	REGISTER FILE 3
1	1	0	0	0C	REGISTER FILE 4
1	1	0	1	0D	REGISTER FILE 5
1	1	1	0	0E	REGISTER FILE 6
1	1	1	1	0F	REGISTER FILE 7

* 0.5 (FLOATING POINT) OR -1 (INTEGER)
** PI (FLOATING POINT) OR MAX NEG (INTEG)

MODE WORD FOR LTA:



	VLBA CORRELATOR PROJECT
	NATIONAL RADIO ASTRONOMY OBSERVATORY
	CHARLOTTESVILLE, VA
Title	LTA FP CHIPS
Size	Document Number / REV
D	56000L024 (L024D04.SCH)
Date:	June 19, 1996 Sheet 4 of 15

LTA BLK DIAG

L024D06.DOC

MAC TO IEEE INFO

L024D07.DOC

DRAM TIMING

L024D08.DOC

FULL CYCLE SEQUENCE

L024D09.DOC

INIT SEQ STATES

L024D10.DOC

XILINX INTERNALS

L024D11.XIL

COMPLETE XILINX LCA LEVEL SCHEMATIC

74148 PRIORITY ENCODER

L024D12.XIL

FUNCTIONAL SCHEMATIC OF 74148 PRIORITY ENCODER

XILINX HIGHER PRIORITY

L024D13.XIL

ADAPTATION OF 74148 TO XILINX IMPLEMENTATION HIGHER PRIORITY SECTION

XILINX LOWER PRIORITY

L024D14.XIL

ADAPTATION OF 74148 TO XILINX IMPLEMENTATION LOWER PRIORITY SECTION

XILINX DISCRETE VERSION

L024D15.XIL

FUNCTIONAL SCHEMATIC REPRESENTATIVE OF THE XILINX INTERNAL FUNCTIONS

Title	ROOT FOR LTA DOCUMENTATION FILES	
Size	Document Number	REV
D	56000L024 (L024D05.DOC)	
Date:	June 19, 1996 Sheet 5 of 15	

LOGIC ANAL

TP SUFFIX INDICATES BUFFERED VERSION

HCB I/O CONNECTOR

RS-485 RCVRS

18 DIFFERENTIAL BITS FROM EACH OF FOUR QUADRANTS

INPUT REGISTERS

(INCUDES PSEUDO RANDOM DATA SOURCE FOR TEST)

INPUT FIFOs

BACKEND INTERFACE

8751 MICRO FFT & INTEGRATION CYCLE SEQUENCERS

FP CHIP CONTROL AND INSTRUCTION BITS

15,15,6 TO IEEE CONVERSION IEEE ADDITION, ADR CTRL 1 MEG x 64 BIT DRAM

IF THE REQUESTED BASELINE IS 210, 211 OR 212, THEN THE RESULT OF THIS beSUB LOOKUP IS USED TO DETERMINE WHICH BANK TO READ FROM.

FOR TAPE VALIDITY, beSUB IS A FUNCTION OF beRSLT[13..10] WHICH COUNTS BASELINES 0-209.

FOR PULSAR VALIDITY, beSUB IS A FUNCTION OF beRSLT[1..2] WHICH COUNTS RACKS 0-3.

ALL OF THE ABOVE BASED ON A TRANSPARENT RESULT NUMBER TRANSLATION FOR VALIDITY0.

ROOT FOR DOCUMENTATION FILES

SHEETS 5 THROUGH 15

(STILL PART OF L024dxx SERIES)

ALL D SIZE

L024D05.DOC

ROOT FOR LAYOUTS

SEPARATELY NUMBERED

SHEETS 1 THROUGH 6

ALL C SIZE

Z015D01.LAY

SHEETS 1-4 ARE THE SCHEMATIC

SHEETS 5-15 ARE DOCUMENTATION

VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: LONG TERM ACCUMULATOR (LTA) TOP LEVEL

Size: D | Document Number: 56000L024 (L024D01.SCH) | REV:

Date: June 20, 1996 | Sheet 1 of 15

256 MACWE ACCESSES ARE REQUIRED TO READOUT ALL 430,080 RESULTS
FOR EACH MACWE, THERE ARE 1680 RESULTS TO BE READ.
64 RESULTS ARE READ IN 512 CLOCK CYCLES IN A SINGLE FFT CYCLE.
26.25 FFT CYCLES ARE REQUIRED TO READ ALL 1680 RESULTS FROM
A SINGLE MACWE. (WITH VALIDITY RESULTS, THE TOTAL IS 1704
RESULTS IN 26.625 FFT CYCLES.)
THE 64 RESULTS IN A FFT CYCLE ARE READ IN 8 SETS OF 8.
EACH SET REPRESENTS A SINGLE BASELINE
THUS THE BASELINE NUMBER STARTS AT ZERO AND INCREMENTS 8 TIMES
EVERY FFT CYCLE (ONCE FOR EACH SET OF EIGHT).

QUAD 0 / QUAD 1 / QUAD 2 / QUAD 3

0 1 2 3 4 5 6 7

18 → MULT CONTROL CARD → RS-485 18 → 18 BIT REG → OE\0 OE\1 OE\2 OE\3

144 INPUT PINS TOTAL
MAY USE 4 40 PIN 3M CONNS
AT TOP EDGE OF CARD

18 → HDWR BASE LINE (0-212)

FFT SEQUENCER INCREMENTS
THIS 8 TIMES PER FFT
WHEN APPROPRIATE

CY7C409A-25 64 x 9 FIFOs, 25 MHz (MIDDLE SPEED)

FIFOSO

REALSI → 18 BIT WIDE FIFO REAL → 18 → 36 → REAL MAG[0..14] 15 → CONVERT TO IEEE → 32 REAL

IMAGSI → 18 BIT WIDE FIFO IMAG → 18 → IMAG MAG[0..14] 15 → CONVERT TO IEEE → 32 IMAG

6 → EXP[0..5] 15

TAPE DATA VALIDS AND PULSAR VALIDITY
PASSED OVER SAME BUS AS MAC RESULTS

VALIDITY (FROM SEQUENCER)

MODE WORD

CPU → CPU READS OR WRITES LTA.

SIN AM29C327 FP CHIP
RIN INSTRUCTION OUT

32 REAL → IN/OUT
32 IMAG → IN/OUT

LTA DRAM
1 MEG x 64
(8 Mbytes)
2048 COMPLEX SINGLE PREC IEEE RESULTS FOR EACH OF 210 BASELINES DOUBLE BUFFERED

10 BIT ADR

CPU → INSTRUCT FOR FP CHIPS ← SELF TEST

64 BIT OUTPUT REG BI-DIRECT

210 HARDWARE BASELINES (0-209) PLUS 3 "ARTIFICIAL" BASELINES FOR VALIDITYS, RESULTS IN 213 "BASELINES", 0-212.

BASELINE # 210 IS TAPE DATA VALIDITY,
#211 AND #212 ARE PULSAR VALIDITY.

(NEED DIFFERENT CONVERSION FOR INTEGERS)

ARRAY SELF TEST

HARDWARE BASELINE

CPU → RAM 256 x 12

GROUP ALL BASELINES IN SAME SUB-ARRAY TOGETHER

8 → LTA BASELINE

BASELINE

FOR SELF TEST:
FORCE LTA BASELINE TO 255
USE HARDWARE BASELINE AND ARRAY TO GENERATE RESULT FIELD

BASE LINE
BANK
RESULT

10 BIT ADR BUS

20 BIT ADR FOR ACCUM

MUXING FOR DRAM ADDRESS
NEED READ/WRITE STREAM CONTROL (WR= DLYD READ)
ROW/COL AND ONE OF THREE SOURCES

20 BIT ADR FOR BACK END ACCESS

REFRESH ADR → REFRESH COUNTER BITS 0-8

8 SUB-ARRAY # (0-7)

SUB-ARRAY GREATER THAN 7 USED AS A FLAG FOR VALIDITY.

THE TERM SUB-ARRAY IS USED HERE TO INDICATE A DISTINCT DUMP RATE/DATA REDUCTION COMBINATION.

A MAXIMUM OF 8 DISTINCT SUB-ARRAYS ARE PROVIDED FOR.

IF THE SUB-ARRAY NUMBER IS GREATER THAN 7, THIS INDICATES THAT TAPE OR PULSAR DATA VALIDITYS ARE BEING HANDLED.

THE BASELINE AND SUB-ARRAY NUMBERS USED AS FLAGS ARE:

BASELINE	SUB-ARRAY	FUNCTION
210	8	TAPE DATA VALIDITY
211	9	PULSAR VALIDITYS (FIRST HALF)
212	10	PULSAR VALIDITYS (OTHER HALF)
255		SELF TEST

CPU → 8 BIT REG BANK 8 → 8 BIT TO 1 BIT MUX AND MORE → 1 BANK

CPU → 8 BIT REG CLAC 8 → 8 BIT TO 1 BIT MUX AND MORE → 1 CLEAR ACCUM

FFT SEQUENCER COUNTS
0,2,4,6,1,3,5,7
FOR EACH SET OF 8.

CPU → RAM 32K x 11

SUB-ARRAY GREATER THAN 7 FORCES BYPASS OR WHATEVER
PROVIDE DATA REDUCTIONS

ARRAY (8) 3
RESULT (256) 8

INTEGRATOR CYCLE SEQUENCER INCREMENTS THIS FOR EVERY MACWE

11 → LTA RESULT (2048)

BANK SWITCH AND CLR ACCUM FOR VALIDITYS NEED THE RESULT NUMBER IN ORDER TO KEEP TRACK OF PROPER BANKS.
A LOOKUP FROM RESULT TO SUB-ARRAY WILL PROBABLY BE NEEDED IN THE BANK SWITCH AND CLAC MUXES.

BANK FOR EACH SUB-ARRAY 10 → 16 BIT TO 1 BIT MUX

BACK END ACCESSES ARE TO OPPOSITE BANK SO MUX IS INVERTING

CPU → 1K x 3 RAM LOOKUP

RESULT 8
LOWER 2 BITS OF SUB-ARRAY 2

VALIDITY SUB-ARRAY NUMBER

IF SUB-ARRAY NUMBER IS > 7, THE RESULT OF THIS LOOKUP IS USED AS THE SOURCE FOR THE BANK SWITCH AND CLAC MULTIPLEXORS.

THIS TRANSLATES THE RESULT NUMBER TO SUB-ARRAY NUMBER FOR THE TAPE DATA VALIDS AND THE PULSAR VALIDITYS.

THIS BIT ONLY GOES TO THE BANK SWITCH MUX
THIS BIT ONLY GOES TO THE RAM

SUB ARRAY NUMBER	4 (16)	3 (8)	2 (4)	1 (2)	0 (1)	
0	0	0	0	0	0	NORMAL RESULTS
7	0	0	1	1	1	
8	0	1	0	0	0	TAPE VALID WEIGHTS, SUB-ARRAY LOWER 3 BITS STILL DETERMINE BANK; RAM LOOKUP IS BYPASSED
F	0	1	1	1	1	
10	1	0	0	0	0	NOT USED
17	1	0	1	1	1	
18	1	1	0	0	0	FORCE BANK 0
19	1	1	0	0	1	FORCE BANK 1

RAM LOOKUP IS BYPASSED
BANK SELECT MUX IS FORCED

INTEGRATION CYCLE SEQUENCER (8192 FFT CYCLES)

FULL FFT CYCLE ACCUM
PARTIAL FFT CYCLE ACCUM
RESULT NR
FULL FFT CYCLE ACCUM SELF TEST
PARTIAL FFT CYCLE ACCUM SELF TEST

FFT CYCLE SEQUENCER

REPEATS FIFO SHIFT IN, ACCUM TO RAM, BACKEND ACCESS, AND REFRESH SEQUENCES EVERY FFT CYCLE.

ACTUAL WRITES TO RAM ENABLED ONLY AT APPROPRIATE TIMES. (FOR 26.25 FFT CYCLES AT A TIME)

RAS\
CAS\
WE\
FFCLOCK
FF OE\
REALSI
IMAGSI
FIFOSO
OE\[0..3]
HARDWARE BASELINE[0..7]
ARRAY[0..2]

1/8192 FFT CYCLES
1/516 CLK CYCLES

INTEG SEQ RESET ENA
DIFF ECL FFT INIT
INCREMENT
INCREMENT INTEG SEQUENCER
INTERRUPT 8751

8751 MICRO

CONFIGURES RAMS

UPDATES CURRENT BANK FOR EACH SUB-ARRAY EVERY 131ms

SELF TEST

(MASTER CONTROLLER ALSO KEEPS TRACK OF SELF TEST CYCLES.)

HCB INTERFACE → INTERRUPT

131ms TIC → INTERRUPT

REAL TIME SYSTEM NEEDS A 131ms TIC ALSO.

LTA 8751 NEEDS TO KEEP TRACK OF BANK SWITCHING.
SEEMS LIKE NEED SOME SORT OF MASTER INIT TO SAY WE ARE STARTING AT INTEGRATION CYCLE #0 AND ALL BANK SWITCHING IS DETERMINED WITH REFERENCE TO THIS POINT??
PROBABLY A COMMAND OVER THE HCB CAN DO THIS?

ADR, SUB-ARRAY, & DATA — 19 BITS OF ADR, 5 BITS SUB-ARRAY TO CONTROL BANK SWITCH BIT — 64 BITS DATA

READ

beRD/WR
beWRSTB\ INITIATES READ CYCLE
DUMMY DATA WRITTEN TO 2950's IN ORDER TO CAUSE BERQST TO ASSERT
beRQST
SYNCHRONIZE TO NEXT BACKEND ACCESS CYCLE AND READ THE REQUESTED ADDRESS
ltaACK\
ltaWRSTB\
ltaSTATUS → STATUS TO BACKEND
beRDSTB\
TERMINATES READ CYCLE

ADR, SUB-ARRAY, & DATA — 19 BITS OF ADR, 5 BITS SUB-ARRAY TO CONTROL BANK SWITCH BIT — 64 BITS DATA

WRITE

beRD/WR
INITIATES WRITE CYCLE
beWRSTB\
SYNCHRONIZE TO NEXT BACKEND ACCESS CYCLE AND WRITE THE REQUESTED ADDRESS
beRQST & ltaSTATUS → STATUS TO BACKEND
TERMINATES WRITE CYCLE
ltaACK\
ltaOE\

11 → RESULT MAPPING HERE CAN BE USED TO OVERCOME ANY NON-STANDARD ORDERING REQUIRED BY THE FAST PAGE MODE RESTRICTION

CPU → 32K x 11 RAM (UPPER HALF PBLY BY-PASS)

BITS 3, 2, 1, 0 GO TO RAM
BITS 4, 2, 1, 0 GO TO BANK SWITCH MUX
BIT 3 FORCES RAM BYPASS (OR WHATEVER)
BIT 4 FORCES BANK SWITCH BIT

RESULTS HOLDER WEIGHT TAG

BASELINE COUNTER
PRE-LOAD
TAG, WEIGHT, PLACE HOLDER, RESULTS
ITEM COUNTER 0-2047 MAX

CPU → MODULUS CONTROL

WHEN WEIGHT FLAG ASSERTED, BASELINE IS FORCED TO 210, SUBARRAY BIT 3 IS FORCED HIGH SO RAM LOOKUP IS BYPASSED, RESULT FIELD IS FORCED TO USE A FROM LOOKUP FROM BASELINE TO RESULT NR.

TAPE DATA VALIDS ARE THUS DISPERSED OUT WITH EACH BASELINE OF RESULTS.
PULSAR VALIDITYS ARE PROBABLY READ OUT AS FOUR SETS, ONE PER POSSIBLE PULSAR SUBARRAY.

THIS AREA NEEDS UPDATING

START BASELINE SUB-ARRAY

DR-11W EMULATOR

FOR INTERFACE TO VME SYSTEM

VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA

Title: LTA BLOCK DIAGRAM

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D	56000L024 (L024D06.DOC)	

Date: June 19, 1996 Sheet 6 of 19

ONE'S COMP VALUES FROM MAC CHIP

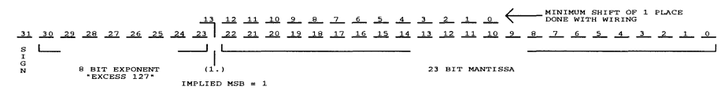
AT LEAST ONE MANTISSA IS NORMALIZED TO HAVE MSB=1, BUT THE OTHER MAY NOT HAVE THE MSB = 1.

	6 BIT 2's COMP EXPONENT						15 BIT 1's COMPLEMENT MANTISSAS															
	5	4	3	2	1	0	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	32	16	8	4	2	1							8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1
	S	E	E	—	—	—	—	S.	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I
				E	E	E	—	S.	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

UNSIGNED DATA VALID COUNTER RESULTS
MAX COUNT= 8192

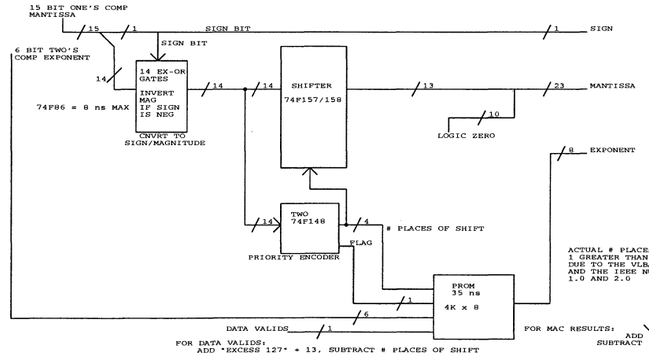
0	0	0						0	DV	DV	DV	DV	DV	DV	DV	DV	DV	DV	DV	DV	DV	DV	DV	← DECIMAL POINT
						0	0	0	0	DV	DV	DV	DV	DV	DV	DV	DV	DV	DV	DV	DV	DV	DV	.

THE LOWER 14 BITS OF THE 16 BIT DATA VALID COUNTER ARE SENT OVER THE 18 BIT MAC OUTPUT BUS. THE EXPONENT BITS ARE FORCED TO ZERO SOMEWHERE. TWO DIFFERENT RESULTS COULD BE SENT, ONE IN PLACE OF REAL AND ONE IN PLACE OF IMAG, SO TWO RESULTS ARE HANDLED IN PARALLEL, AND STORED TOGETHER IN DRAM. OR ONLY ONE PATH MIGHT BE USED.



IF BIASED EXPONENT = 0 AND MANTISSA = 0: VALUE IS ZERO

IF BIASED EXPONENT = 0 AND MANTISSA != 0: VALUE IS DENORMALIZED



RANGE OF UNBIASED EXPONENT	+ BIAS	=	RANGE OF BIASED EXPONENT	
+128	127	=	255	± INF and NaN
+127	127	=	254	
⋮	⋮		⋮	
-126	127	=	1	
-127	127	=	0	± 0 and DENORM

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Title: MAC TO IEEE INFO

Size	Document Number	REV
D	56000L024 (L024D07.DOC)	

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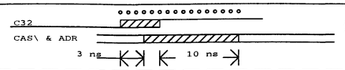
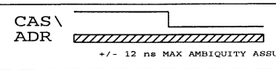
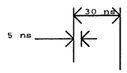
CAS\, RAS\ FP CLK FP OE\ AND BACKEND ACCESS CLOCK ARE FROM THE SAME FROM AND THUS ASSUMMED TO HAVE NO RELATIVE SKEW. C32 IS SHOWN ONLY FOR REFERENCE, AND ADDRESSES ARE SHOWN TO INCLUDE A +/- 12 ns MAX AMBIGUITY W.R.T. CAS\.

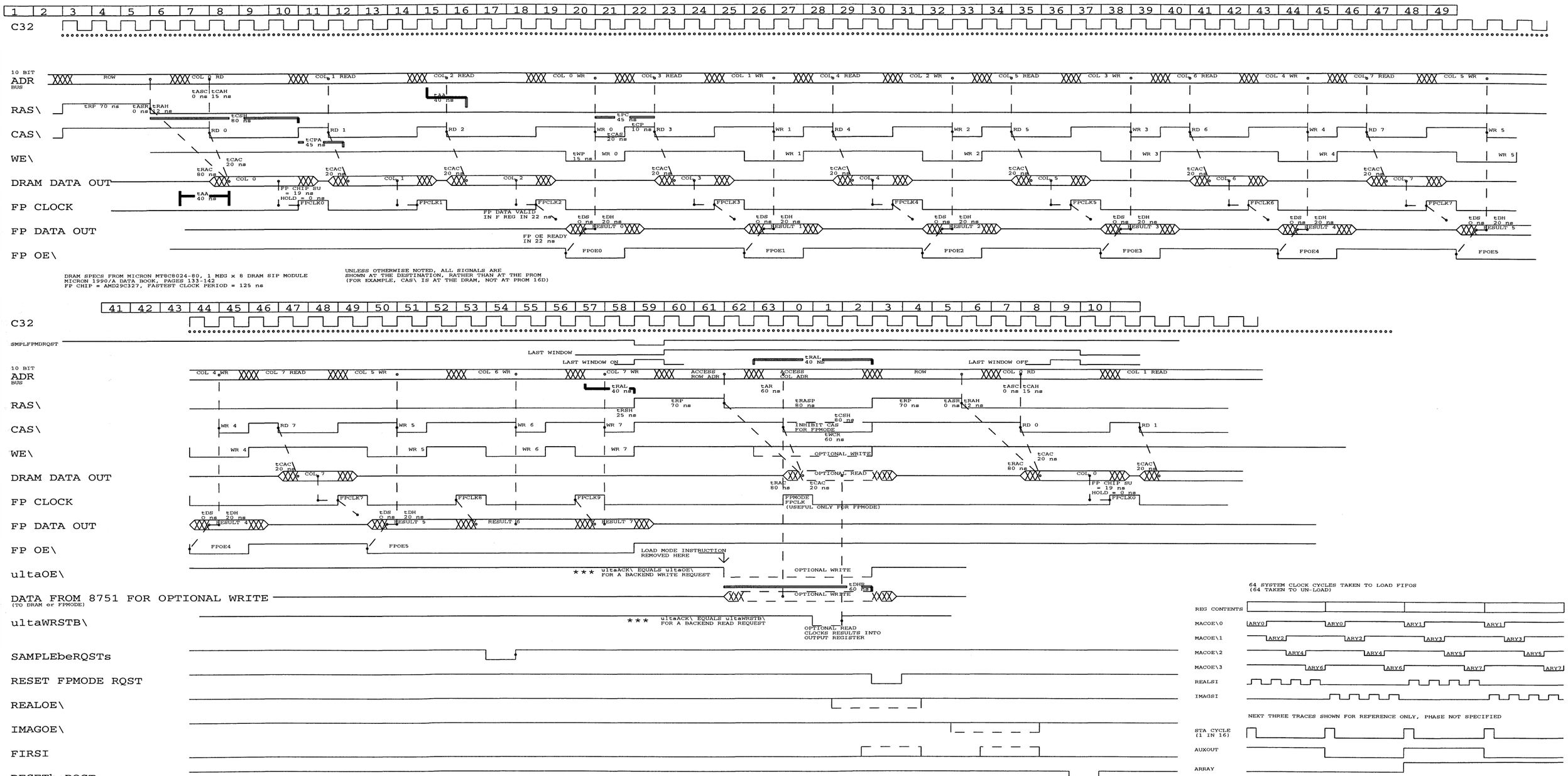
ALL CONTROL AND ADDRESS LINES ASSUMMED TO BE DRIVEN WITH REASONABLY MATCHED BUS DRIVERS.



5 ns MAX CLOCK SKEW ASSUMMED
ASSUME NO OUTPUT CHANGES FASTER THAN 3 ns.
ASSUME NO OUTPUT IS SLOWER THAN 10 ns.

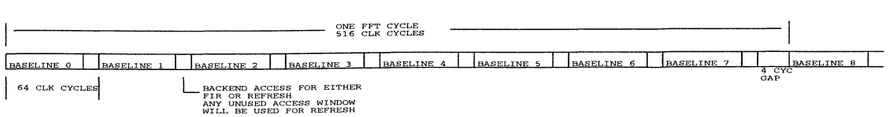






DRAM SPECS FROM MICRON MT8C8024-80, 1 MEG x 8 DRAM SIP MODULE
MICRON 1990/A DATA BOOK, PAGES 133-142
FP CHIP = AMD29C327, FASTEST CLOCK PERIOD = 125 ns

UNLESS OTHERWISE NOTED, ALL SIGNALS ARE SHOWN AT THE DESTINATION, RATHER THAN AT THE PROM (FOR EXAMPLE, CAS\ IS AT THE DRAM, NOT AT PROM 16D)



EIGHT SETS OF 8 RESULTS X 64 CYCLES PER SET = 512 CYCLES TOTAL.
THUS 64 RESULTS PER FFT CYCLE CAN BE ACCUMULATED.
1680 RESULTS PER MAC ACCESS / 64 = 27 FFT CYCLES.
430,080 / 1680 = 256 MAC ACCESSES

A SINGLE SET OF 8 RESULTS ARE ALL FROM THE SAME BASELINE, ONE RESULT PER ARRAY.
THUS ONE RESULT FROM EACH ARRAY FOR 8 BASELINES ARE READOUT IN ONE FFT CYCLE

64 SYSTEM CLOCK CYCLES TAKEN TO LOAD FIFOS
(64 TAKEN TO UN-LOAD)

NOTE CONCERNING ACCURACY:

THIS DRAWING SHOULD BE CLOSE TO REALITY, BUT MAY NOT BE TOTALLY ACCURATE.
AS OF 26 JUNE 1997, THERE ARE TWO OLD BLUEPRINTS WITH CONFLICTING DATES, RELATED TO THIS SHEET. ONE WITH THE SAME TITLE AND DATED MAY 21, 1991 HAD THE PRELIMINARY DRAWING NUMBER OF L024D50.TIM. IT APPEARS TO BE THE SAME AS THIS CURRENT SHEET BEFORE THESE NOTES WERE ADDED TODAY (26 JUNE).
THE SECOND ONE WITH THE SAME TITLE IS DATED AUGUST 7, 1990 WITH THE PRELIMINARY DRAWING NUMBER OF L024D50.SCH.
THE OLDER TIME STAMP DRAWING SEEMS TO HAVE MORE DETAILS THAN THE NEWER ONE.
SOME OF THE ITEMS FROM THE OLDER BLUEPRINT DATE WILL BE INCLUDED IN THIS SHEET TODAY.

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CHARLOTTESVILLE, VA

Title: LTA DRAM & FP CHIP TIMING

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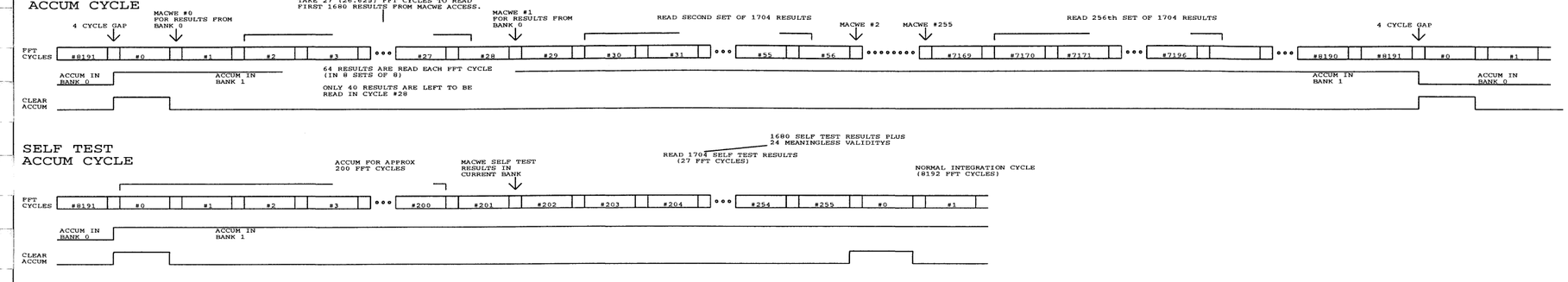
D	560001024 (L024D08.DOC)	

Date: June 26, 1997 Sheet 8 of 15

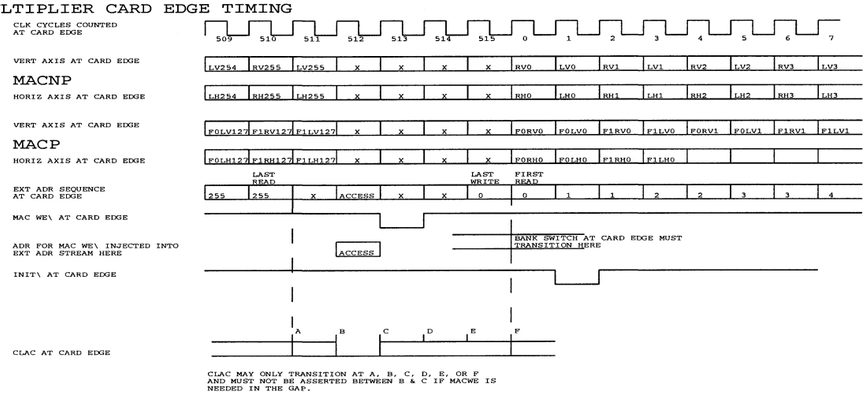
NORMAL ACCUM CYCLE



SELF TEST ACCUM CYCLE

NOTE:
NORMAL MACWE'S ACCESS A RESULT FROM
THE IN-ACTIVE BANK.
MACWE FOR SELF TEST ACCESSES A RESULT
FROM THE CURRENT BANK.

MULTIPLIER CARD EDGE TIMING



CLAC MAY ONLY TRANSITION AT A, B, C, D, E, OR F
AND MUST NOT BE ASSERTED BETWEEN B & C IF MACWE IS
NEEDED IN THE GAP.

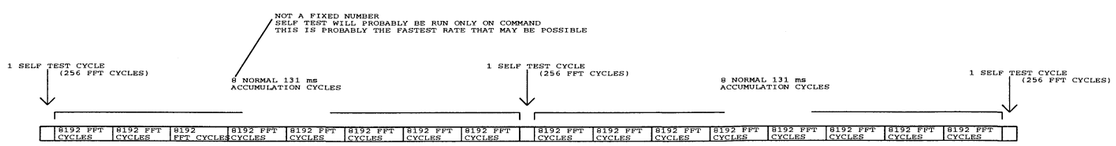
NOTE: IN ORDER TO BE ABLE TO SET UP MODELS FOR SELF TEST,
THE PRI DELAY BUFFER WILL BE USED TO ABSORB
ONE FRINGE CYCLE (4ms) EVERY 8 INTEGRATION CYCLES
(APPROX EVERY 1.05 SECONDS).

THUS A SPECIAL SHORT INTEGRATION CYCLE WILL OCCUR FOR SELF TEST,
WHICH LASTS FOR ONE FRINGE CYCLE (256 FFT CYCLES).

FOR SELF TEST, WE WILL ACCUMULATE FOR APPROX 200 FFT CYCLES,
AND USE APPROX 27 FFT CYCLES FOR READING OUT THE RESULTS.

NOTE: DATA HAS ONE CYCLE DELAY FROM CARD EDGE TO ALL ASICS.

INIT\, EXTADR, MAC WE\, AND CL ACC ALL HAVE TWO CYCLE DELAY FROM CARD EDGE
TO ASICS IN ARRAY 0, AND THREE CYCLE DELAY TO ARRAY 1.



VLBA CORRELATOR PROJECT			
NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA			
Title: LTA FULL CYCLE SEQUENCE			
Size: D	Document Number: 56000L024 (L024D09.DOC)		REV
Date: June 19, 1996	Sheet 9 of 15		

MCC CLK CYCLES

SHOWN FOR REFERENCE ONLY
ACTUAL RELATION NOT PRESENTLY KNOWN

CARD EDGE MAC DATA FROM MCC

BSLINE 0, REAL 18 BITS, ARYS 0,2,4,6 | BSLINE 0, IMAG 18 BITS, ARYS 0,2,4,6 | BSLINE 0, REAL 18 BITS, ARYS 1,3,5,7 | BSLINE 0, IMAG 18 BITS, ARYS 1,3,5,7 | BSLINE 1, REAL 18 BITS, ARYS 0,2,4,6 | BSLINE 1, IMAG 18 BITS, ARYS 0,2,4,6 | BSLINE 1, REAL 18 BITS, ARYS 1,3,5,7 | BSLINE 1, IMAG 18 BITS, ARYS 1,3,5,7 | BSLINE 2, REAL 18 BITS, ARYS 0,2,4,6

FIRST VALID DATA OF INTEGRATION PERIOD

FSTa STATE

FFT CYCLE MODULUS (0-515)

LTA CLK CYCLES

CARD EDGE MAC DATA

STACLK

CAPTURED MAC DATA

MACOE\0

MACOE\1

MACOE\2

MACOE\3

REALSI

IMAGSI

AN ASSUMPTION IS MADE THAT THE IMAGSI MAY OCCUR INSIDE THE FIFORST AS SHOWN. IF THIS IS WRONG, THEN IMAGSI NEEDS TO GO THRU THE PAL AT 20C.

MACFIFORST\ AT FIFO

S[34..36] AT PROM 0 1 0 3 7 2

MACFIFORST\ AT PROM

← MACFIFORST\ OVERLAPS WE\ AS SHOWN
3= MACFIFORST\ /= OVERLAP 2= BE WE\

ENAb AT PROM

ENAb AT COUNTER

THE OUTPUTS FROM THE INTEGRATION CYCLE SEQUENCER NEED THREE SYSTEM CLOCK CYCLES BEFORE THEY CAN BE CONSIDERED STABLE AFTER THE INCREMENT.

RNDRST AT PROM

RNDRST AT DATA REGS

FFT CYCLE COUNTER STATES — FFT CYCLE # 255 — FFT CYCLE # 256

MACFIFOSO AT PROM

MACFIFOSO INHIBITED BY MACFIFORST\ RELEASED BY S[36..34] = 4

MACFIFOSO AT FIFO

MAC FIFO OUTPUT DATA

BSLINE 0 ARY 0 1st VALID DATA OF INT PERIOD | BSLINE 0 ARY 2 | BSLINE 0 ARY 4 | BSLINE 0 ARY 6 | BSLINE 0 ARY 1 | BSLINE 0 ARY 3 | BSLINE 0 ARY 5 | BSLINE 0 ARY 7 | BSLINE 0 ARY 0 | BSLINE 1 ARY 0 | BSLINE 1 ARY 2

RELEASE MACFIFOSO AT PROM

envfeCLK AT PROM

envfeCLK AT PAL OUTPUT

1ST PIPELINE REG OUTPUT IN IEEE CONV

BSLINE 0 ARY 0 | BSLINE 0 ARY 2 | BSLINE 0 ARY 4 | BSLINE 0 ARY 6 | BSLINE 0 ARY 1 | BSLINE 0 ARY 3 | BSLINE 0 ARY 5 | BSLINE 0 ARY 7 | (BSLINE 1 ARY 0) | BSLINE 1 ARY 2

FINAL IEEE OUTPUT (INPUT TO FP CHIP)

BSLINE 0 ARY 0 | BSLINE 0 ARY 2 | BSLINE 0 ARY 4 | BSLINE 0 ARY 6 | BSLINE 0 ARY 1 | BSLINE 0 ARY 3 | BSLINE 0 ARY 5 | BSLINE 0 ARY 7 | (BSLINE 1 ARY 0) | BSLINE 1 ARY 2

FPCLK AND ENVFECLK ARE TREATED AS BEING FULLY SYNCHRONOUS WITH EACH OTHER, COMING FROM THE SAME PAL (17E), THUS THE 2ONO NS HOLD SPEC AT FP INPUT IS ASSUMMED TO BE MET.

FPCLK AT PROM

FPCLK AT FP CHIP

FP MODE

THIS EDGE OF FPCLK CAPTURES RNDRST AT DATA REGS, SO IT MAY BE USED FOR LOGIC ANALYZER TRIGGER

LAST WINDOW

LAST WIND ON

LAST WIND OFF

DATA IN FP CHIP OUTPUT REGISTER

ADRCLK AT PROM

SAMPLE beRQSTs

RESETbeRQSTs

RESET FPMD RQST

CNTR POS (S15)

SMPLFPMDRQST

rfrshR ASSERTS

HBL NR

ARRAY NR

19 BIT ADR AT SEQ OUTPUT

R & COL0 | ROW & COL1 | R & COL2 | ROW & COL3 | ROW & COL4 | ROW & COL5 | ROW & COL6 | ROW & COL7

ADRCLK AT 'F399s

ADRFIFOSO

ADRFIFORST\

ADRFIFOSI

20 BIT ADR IN REG

ROW & COL0 | ROW & COL1 | ROW & COL2 | ROW & COL3 | ROW & COL4 | ROW & COL5 | ROW & COL6 | ROW & COL7

S[40..42] AT PROM

ASEL[] AT MUX

3,5 OR 4,6 OR

10 BIT MUX OUT

COL7 WR | BE ROW | BE COL | ROW | COL0 RD | COL1 RD | COL2 RD | COL0 WR | COL3 RD | COL1 WR | COL4 RD | COL2 WR | COL5 RD | COL3 WR | COL6 RD | COL4 WR | COL7 RD | COL5 WR | COL6 WR | COL7 WR | BE ROW | BE COL | ROW | COL0 RD | COL1 RD | COL2 RD | COL0 WR | COL3 RD | COL1 WR | COL4 RD | COL2 WR | COL5 RD | COL3 WR | COL6 RD | COL4 WR | COL7 RD | COL5 WR | COL6 WR | COL7 WR | BE ROW | BE COL

ADR ENA\

RAS\ AT DRAM

PAGE

10 BIT ADR BUS AT DRAM

BE | RD 0 | RD 1 | RD 2 | W0 | RD 3 | W1 | RD 4 | W2 | RD 5 | W3 | RD 6 | W4 | RD 7 | W5 | W6 | W7 | BE | (4 CY GAP) | RD0 | RD1 | RD2 | W0 | RD3 | W1 | RD4 | W2 | RD5 | W3 | RD6 | W4 | RD7 | W5 | W6 | W7 | BE | RD 0

CAS\ AT DRAM

WE\ AT DRAM

BACKEND | W0 | W1 | W2 | W3 | W4 | W5 | W6 | W7 | BACKEND

FPOE\ AT FP CHIP

WE\ AT 20C OUT

RAS\ AT PROM

CAS\ AT PROM

FPOE\ AT PROM

WE\ AT PROM

S[34..36] AT PROM 0 1 0 3 7 2 0 1 0 1 0 1 0 1 0 1 0 4 0 1 0 1 0 1 0 5 0 2 0 6 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 2

LAST WIND ON

LAST WIND OFF

OE\ AT PROM

WRSTB\ AT PROM

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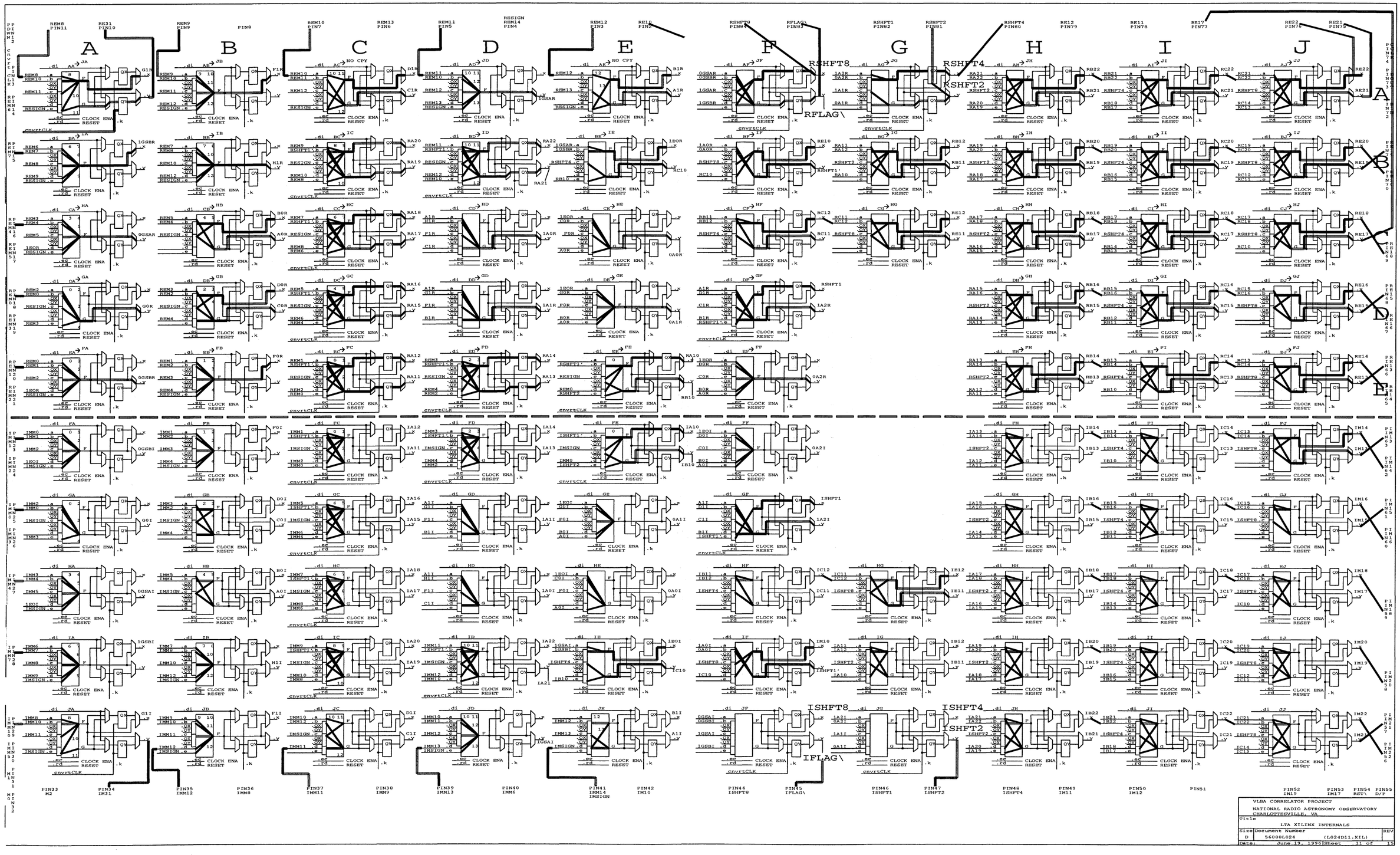
Title: LTA INITIAL SEQUENCER STATES

Size	Document Number	REV
D	56000L024 (L024D10.TIM)	

Date: June 19, 1996 Sheet 10 of 15



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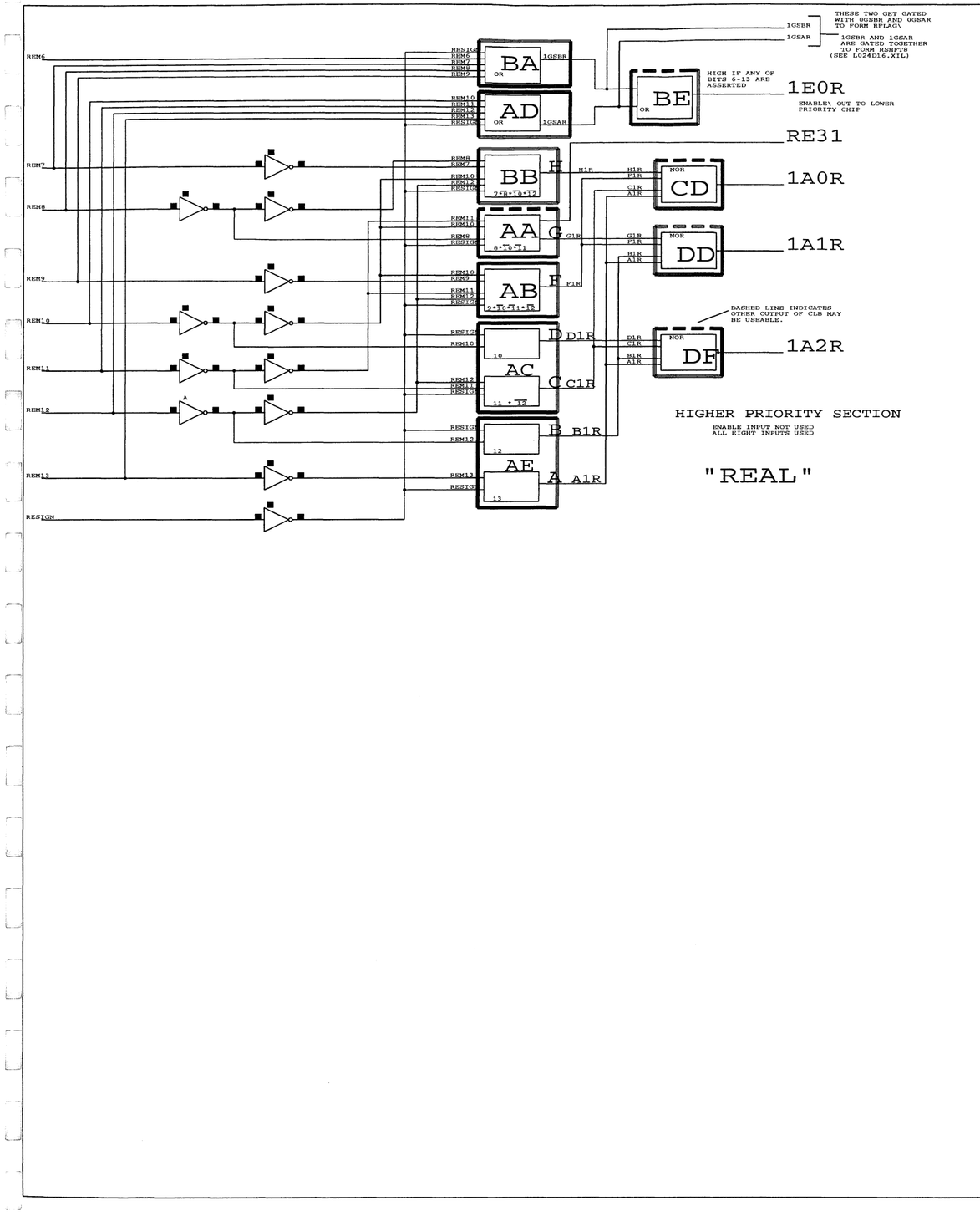
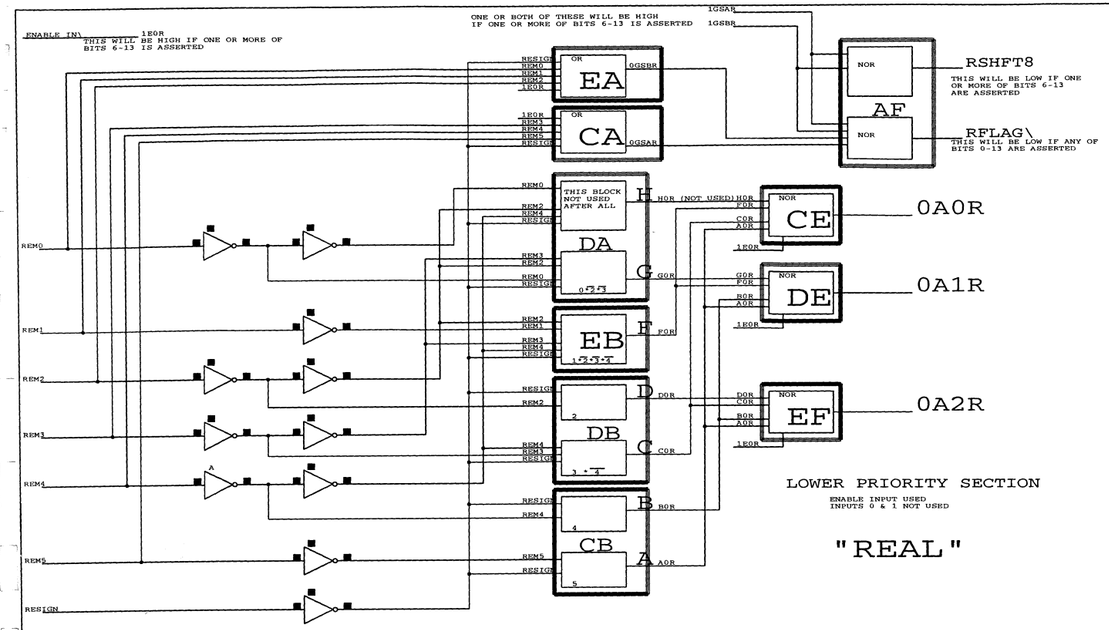
Title
LTA XILINX INTERNALS
Size D | Document Number 56000L024 (L024D11.XIL) | REV
Date: June 19, 1996 | Sheet 11 of 15



VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title 15,15,6 CONVERSION TO IEEE: PRIORITY ENCODER		
Size D	Document Number 56000L024 (L024D13.XIL)	REV
Date: June 19, 1996	Sheet 13 of 15	



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Title	
15,15,6 CONVERSION TO IEEE; PRIORITY ENCODER	
Size: D	Document Number: 560001024 (L024D14.XIL) — REV:
Date: June 19, 1996	Sheet 14 of 15

15,15,6 TO IEEE CONVERSION

(INTEGER TO IEEE CONVERSION FOR DATA VALIDITY5)

XILINX INPUT REGISTERS USED
ONE STAGE OF PIPELINE USED INTERNALLY
AT OUTPUT OF FIRST MUX STAGE.

LS SHIFT BIT NEEDED UN-PIPELINED AT INPUT
TO FIRST MUX.

INDICATES CLB AT WHICH
OUTPUT(S) ARE GENERATED

ONE'S COMPLEMENT
CONVERSION IS DONE
IN PRIORITY ENCODER AND
IN 1ST MUX STG

ORIGINAL DISCRETE VERSION
MODIFIED TO BE REPRESENTATIVE OF XILINX INTERNALS
(BUT NOT INTENDED TO BE EXACT)

IMAG SECTION NOT KEPT AS CURRENT AS REAL SECTION

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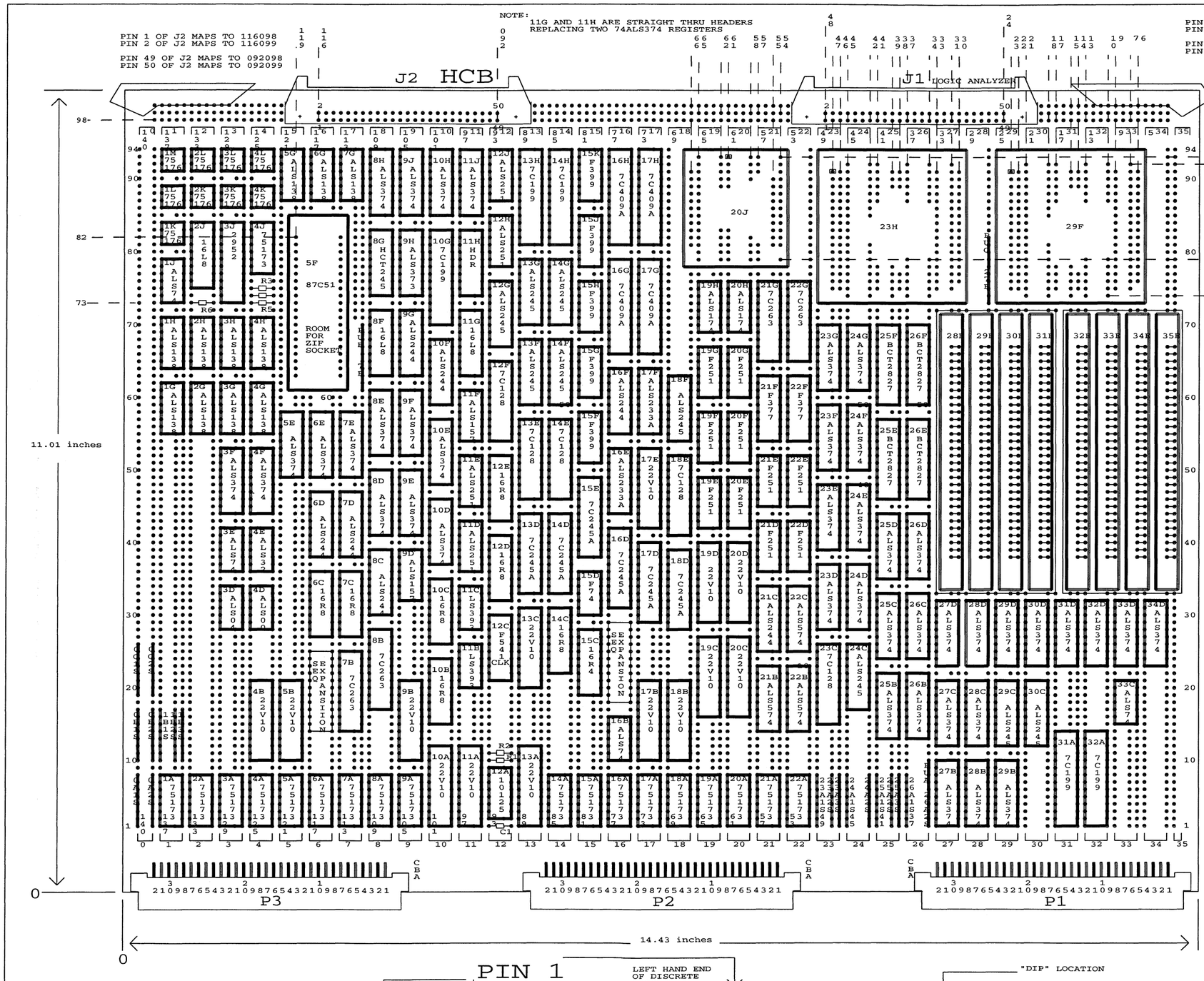
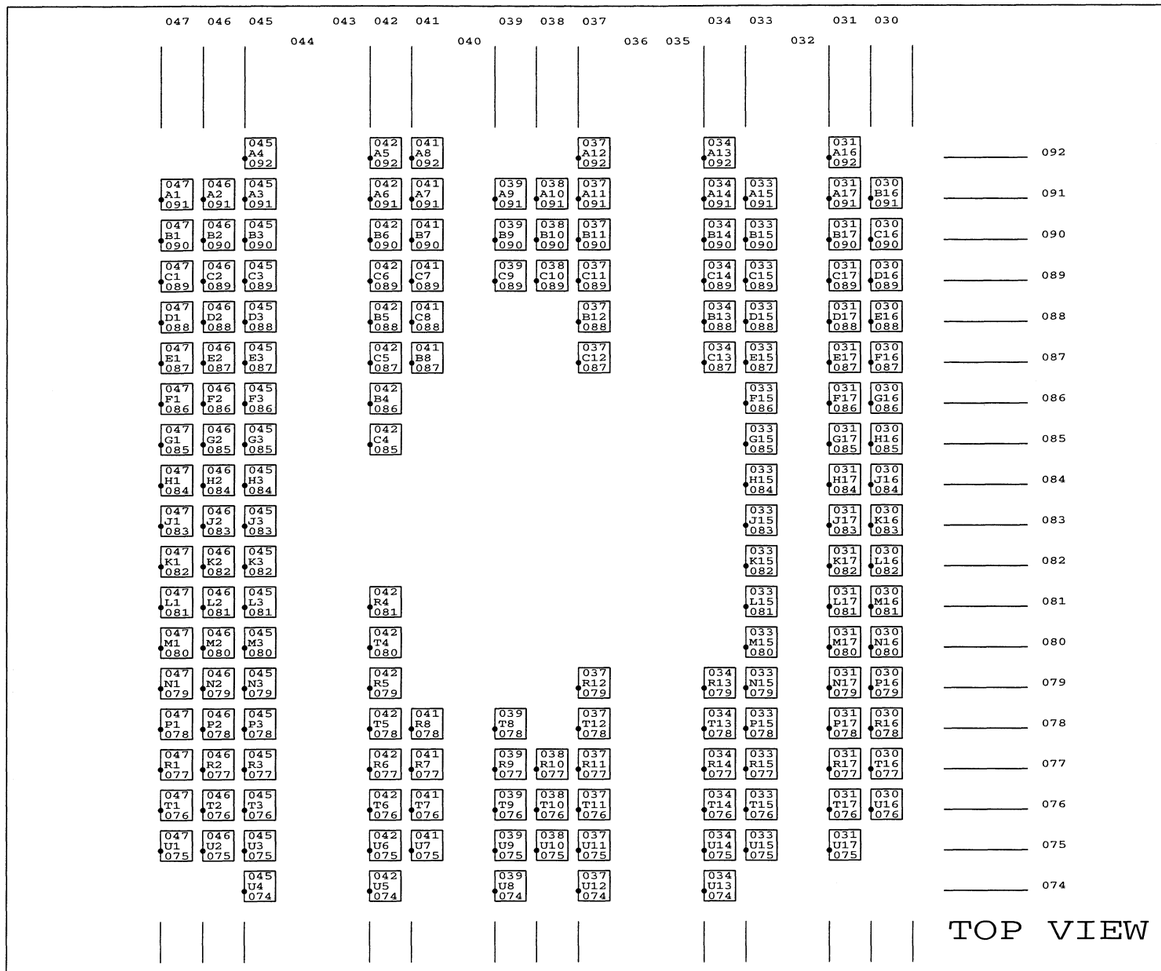
CHARLOTTESVILLE, VA	
Title	15,15,6 TO IEEE DISCRETE VERSION
Size: D	Document Number: 56000L024 (L024D15.XIL) REV
Date: June 19, 1996	Sheet 15 of 15


NOTE:
11G AND 11H ARE STRAIGHT THRU HEADERS
REPLACING TWO 74ALS374 REGISTERS
PIN 1 OF J2 MAPS TO 116098
PIN 2 OF J2 MAPS TO 116099
PIN 49 OF J2 MAPS TO 092098
PIN 50 OF J2 MAPS TO 092099
J2 HCB
J1 LOGIC ANALYZER
PIN 1 OF J1 MAPS TO 048098
PIN 2 OF J1 MAPS TO 048099
PIN 49 OF J1 MAPS TO 024098
PIN 50 OF J1 MAPS TO 024099
11.01 inches
14.43 inches
5F 87C51
ROOM FOR ZIF SOCKET
20J
23H
29F
SEXPANSION
P3
P2
P1
TOP VIEW
9U x 280 mm EUROCARD
PIN 1
TOP PIN OF ALL SIPS
UPPER LEFT CORNER OF ALL DIPS
LEFT HAND END OF DISCRETE RESISTORS
RESISTOR PINS: PIN 1
PIN 2
WW PINS:
125075 122075 R3 330 1/8w
125074 122074 R4 150 1/8w
125073 122073 R5 330 1/8w
133073 130073 R6 4.7K 1/8w
093011 090011 R2 100 1/8w
093010 090010 R1 100 1/8w
093001 090001 C1 0.22uF DIP CAP
"DIP" LOCATION
SIP # FROM LEFT TO RIGHT
INDICATES "SIP"
23A1S
23A2S
23A3S
REFERENCE DESIGNATORS FOR SIPS WHEN MORE THAN ONE SIP IS PLACED IN A "DIP" LOCATION:
REV A: 8-28-91 ADDED 74ALS374 AT 29E
SIMM SOCKET PINS
ADAPTOR PINS PLUG INTO WW CARD
PIN 1
BOARD COORDINATE WIREWRAP PIN DESIGNATIONS ARE IN XXYYY FORM
IN THE FIELD OF WIREWRAP PINS:
XXX GOES FROM 001 TO 140
YYY GOES FROM 001 TO 094
FOR PURPOSES OF LOCATING THE J1 and J2 CONNECTORS, THE YYY DESIGNATION IS EXTENDED TO INCLUDE ROWS 098, 099 and 100 FOR THE FIELD OF HOLES BETWEEN THE EJECTORS
X AXIS
Y AXIS
29C327 ADAPTOR, 23H
Z015D02.LAY
29C327 ADAPTOR, 29F
Z015D03.LAY
84 PIN PLCC ADAPTOR, 20J
Z015D04.LAY
LAYOUT CHECK, WITH VCC AND GND
Z015D05.LAY
LTA DRAM ADAPTOR
Z015D06.LAY
VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA
Title
LTA IC LAYOUT WITH SIMMs
Size C
Document Number 56000Z015 (Z015D01.LAY)
REV A
Date: November 19, 1997 Sheet 1 of 6

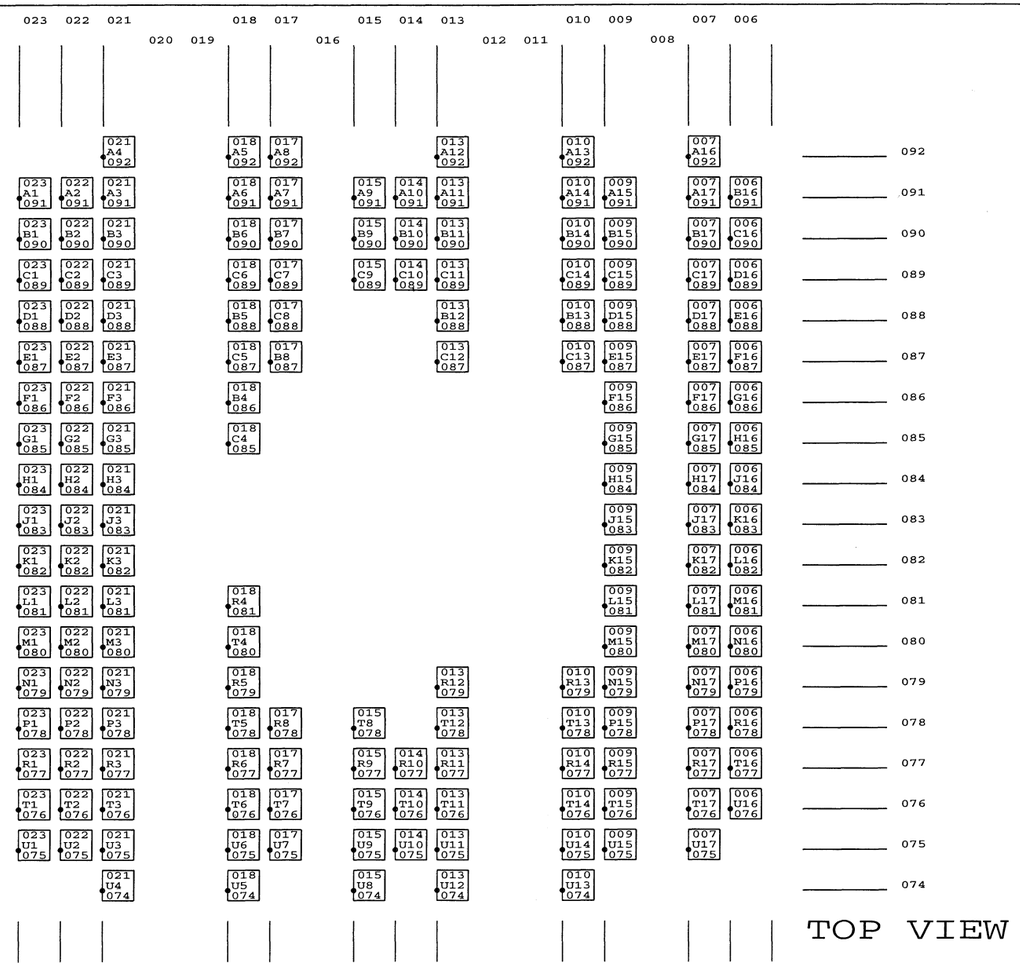


L0C 23H

PIN A1 MAPS TO 047091

THIS LAYOUT USED TO CREATE THE TEXT FILE
W013T03.PIN, L0C 23H PGA ADAPTOR PIN MAPPING

VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA				
Title LTA 29C327 ADAPTOR PIN MAPPINGS: 23H				
Size C	Document Number 560002015 (Z015D02.LAY)			REV
Date: June 20, 1996		Sheet 2 of 6		

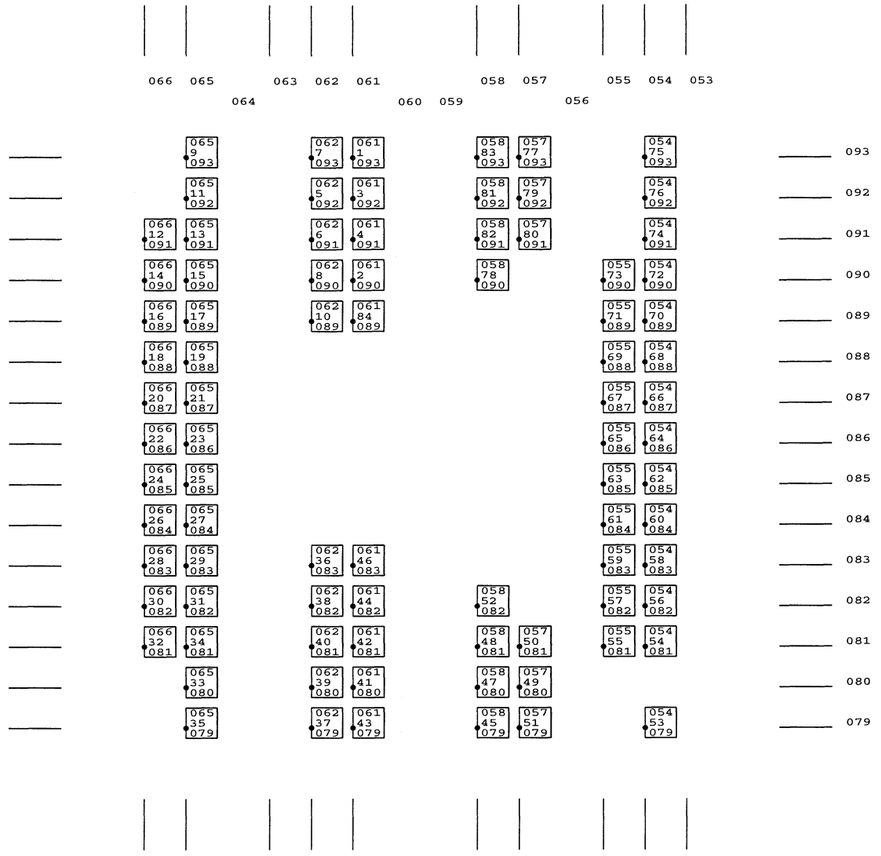


LOC 29F

PIN A1 MAPS TO 023091

THIS LAYOUT USED TO CREATE THE TEXT FILE
W013T04.PIN, LOC 29F PGA ADAPTOR PIN MAPPING

VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title LTA 29C327 ADAPTOR PIN MAPPINGS: 29F		
Size C	Document Number 560002015 (Z015D03.LAY)	REV
Date: June 20, 1996	Sheet 3 of 6	



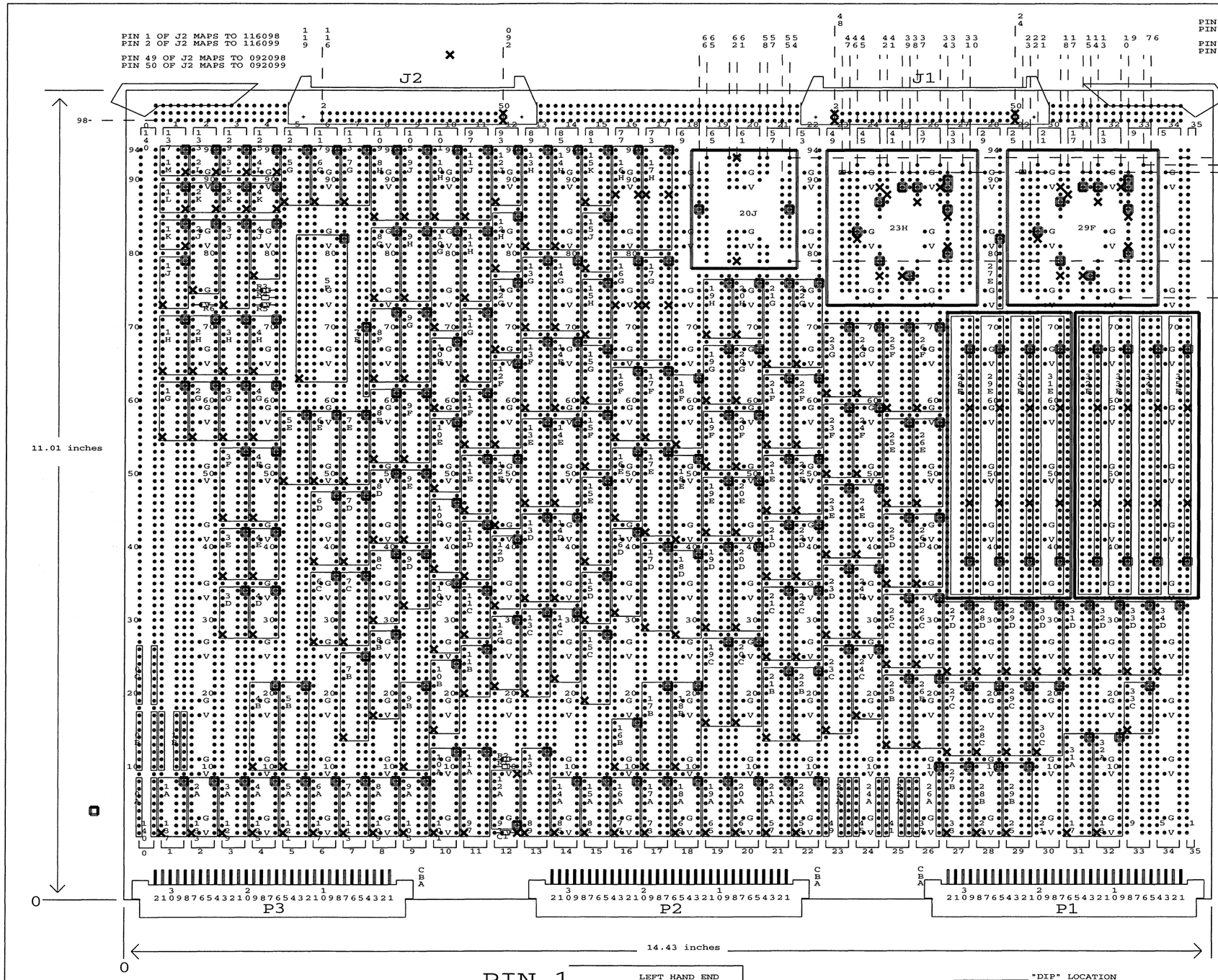
TOP VIEW

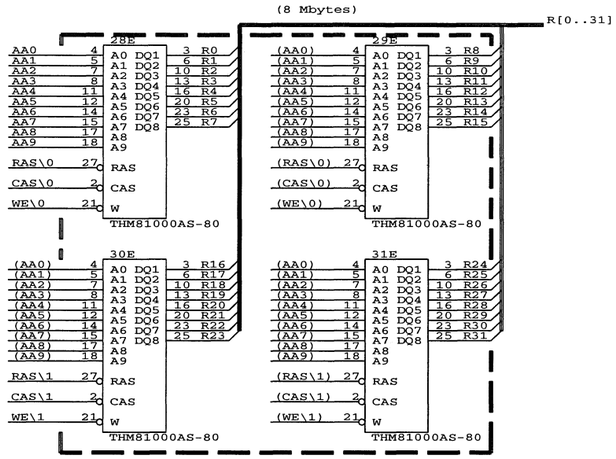
LOC 20J

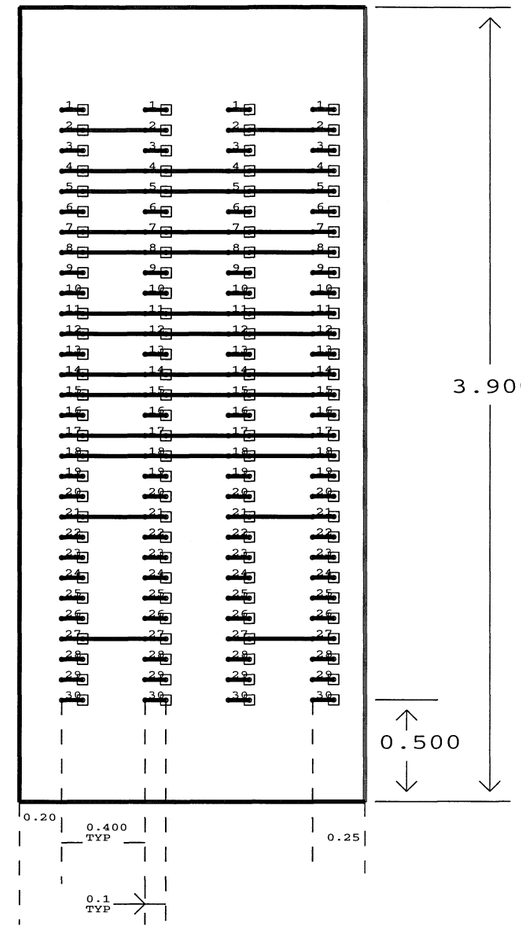
PIN 1 MAPS TO 061093

THIS LAYOUT USED TO CREATE THE TEXT FILE
W013T05.PIN, LOC 20J PLCC ADAPTOR PIN MAPPING

VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title LTA 84 PIN PLCC ADAPTOR PIN MAPPINGS: 20J		
Size C	Document Number 560002015 (Z015D04.LAY)	REV
Date: June 20, 1996	Sheet 4 of 6	


PIN 1 OF J2 MAPS TO 116098
PIN 2 OF J2 MAPS TO 116099
PIN 49 OF J2 MAPS TO 092098
PIN 50 OF J2 MAPS TO 092099
J2
J1
PIN 1 OF J1 MAPS TO 048098
PIN 2 OF J1 MAPS TO 048099
PIN 49 OF J1 MAPS TO 024098
PIN 50 OF J1 MAPS TO 024099
20J
23H
29F
093
092
091
079
074
11.01 inches
P3
P2
P1
14.43 inches
0
TOP VIEW
9U x 280 mm EUROCARD
PIN 1
TOP PIN OF ALL SIPS
UPPER LEFT CORNER OF ALL DIPS
LEFT HAND END OF DISCRETE RESISTORS
RESISTOR PINS: PIN 1
PIN 2
125075
122075
WW PINS:
"DIP" LOCATION
SIP # FROM LEFT TO RIGHT
INDICATES "SIP"
23A1S
23A2S
23A3S
REFERENCE DESIGNATORS FOR SIPS WHEN MORE THAN ONE SIP IS PLACED IN A "DIP" LOCATION:
SIMM SOCKET OUTLINE
PC BOARD EDGE
PIN 1 SIMM SOCKET
PIN 1 ADAPTOR PIN LOCATION
OUTLINE AROUND ADAPTOR PINS 1 THROUGH 30
ADAPTOR PINS ARE OFFSET 0.1 INCH TO RIGHT OF SIMM SOCKET PINS
PC BOARD MOUNTS FOUR SIMM SOCKETS
BOARD COORDINATE WIREWRAP PIN DESIGNATIONS ARE IN XXXYYY FORM
IN THE FIELD OF WIREWRAP PINS:
XXX GOES FROM 001 TO 140
YYY GOES FROM 001 TO 094
FOR PURPOSES OF LOCATING THE J1 and J2 CONNECTORS, THE YYY DESIGNATION IS EXTENDED TO INCLUDE ROWS 098, 099 and 100 FOR THE FIELD OF HOLES BETWEEN THE EJECTORS
X AXIS
Y AXIS
IC OUTLINES PLACED W.R.T. PIN 1 AND NR OF PINS AS LISTED IN W013T02.IC AS A CHECK OF THAT LIST.
"X" INDICATES GROUND TIE
INDICATES VCC PIN OF IC
REV A: 8-28-91 ADDED 74ALS374 AT 29B
REV B: 9-16-92 ADDED R6
VLBA CORRELATOR PROJECT
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA
Title
LTA LAYOUT CHECK, WITH VCC & GND
Size C
Document Number 56000Z015 (Z015D05.LAY)
REV B
Date: June 20, 1996
Sheet 5 of 6





DRAM SUB-ASSEMBLIES

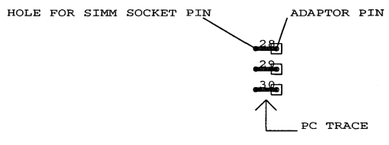
A DRAM SUB-ASSEMBLY CONSISTS OF FOUR SIMM MODULES WHERE THE ADDRESS BUS, RAS, CAS AND WE SIGNALS ARE BUSSED ON THE SUB-ASSEMBLY PC BOARD.

THE INPUTS SHOWN AS "UN-CONNECTED" AT LOCATIONS 29S, 30S, 31E, 33E, 34E AND 35E ARE THE SIGNALS THAT ARE BUSSED, AND THUS NOT WIRED ON THE WIREWRAP CARD. THESE SIGNALS ARE LABELED AS "TEXT" IN PARENS.

SIMM SOCKETS ARE AMP # 643930-1

ADAPTOR PINS ARE PROBABLY:

ADVANCED INTERCONNECTIONS P/N 1364-1G



ORIGINAL VERSION OF THIS LAYOUT WAS L039D01.SCH

AS OF JUNE 1996, THE ORIGINAL FILE COULD NOT BE FOUND

THE DRAWING WAS RE-DRAWN FROM A HARDCOPY IN THIS PRESENT FORM, AS Z015D06.LAY

VLBA CORRELATOR PROJECT NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA		
Title: LTA DRAM ADAPTOR		
Size: C	Document Number: 560002015 (Z015D06.LAY)	REV
Date: June 20, 1996	Sheet 6 of 6	