Scan Test of Die Logic in 3D ICs Using TSV Probing*

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Abstract— **Pre-bond testing of TSVs and die logic is a significant challenge and a potential roadblock for 3D integration. BIST solutions introduce considerable die area overhead. Oversized probe pads on TSVs to provide pre-bond test access limit both test bandwidth and TSV density. This paper presents a solution to these problems, allowing a probe card to contact TSVs without the need for probe pads, enabling both TSV and pre-bond scan test. Two possible pre-bond scan test configurations are shown—they provide varying degrees of test parallelism. HSPICE simulations are performed on a logic-on-logic 3D benchmark. Results show that the ratio of the number of probe needles available for test access to the number of pre-bond scan chains determines which pre-bond scan configuration results in the shortest test time. Maximum pre-bond scan-in and scan-out shift-clock speeds are determined for dies in a benchmark 3D design. These clock speeds show that pre-bond scan test can be performed quickly, at a speed that is comparable to scan testing of packaged dies. The maximum clock speed can also be tuned by changing the drive strength of the probe and on-die drivers of the TSV network. Estimates are also provided for peak and average power consumption during pre-bond scan test. On-die area overhead for the proposed method is estimated to be between 1.0% and 2.2% for three dies in the 3D stack.**

I. Introduction

As semiconductor technology continues to scale, interconnect delay and power consumption threaten to limit the benefits of further scaling. To overcome these bottlenecks, the semiconductor industry is exploring 3D integration e.g., through die stacking and through-silicon-vias (TSVs) [1]–[3]. In a 3D stacked IC (SIC), two or more dies with their own active device and metal layers are bonded together, with vertical TSVs connecting metal layers of adjacent dies. Figure 1 shows an example of a two-die 3D stack. 3D SICs lead to a decrease in interconnect length, power consumption, and footprint.

Dies in a 3D SIC can be tested both pre-bond, i.e., before the dies are assembled onto a stack, or post-bond [4], [5]. An example manufacture and test flow is shown in Figure 2 for a 3-die stacked IC. Pre-bond testing has the potential to significantly increase stack yield. Pre-bond test allows dies to be screened for manufacturing defects both in internal logic and TSVs. Dies can also be matched for performance and power. If a single faulty die is bonded to a stack of otherwise good dies, the whole stack may need to be discarded when a fault is detected during post-bond test. In this paper, we focus on pre-bond testing with access to TSVs or the microbumps deposited on them, and we assume that dies have been thinned to ensure TSV access.

Contacting TSVs with probes prior to bonding is difficult due to the small pitch and density of TSVs. Modern cantilever probes can reach a pitch of 35 μm, but TSVs have pitches of 4.4 μm or smaller [32]. Previous techniques have introduced large probe pads to TSVs for probe needles [7], but these limit test access and TSV placement. Built-in self-test (BIST) techniques have also been proposed for TSV testing [8], [9] and BIST methods for 2D circuits can be extended to pre-bond dies [10], but they require a relatively large amount of die area, and on-chip analog BIST logic is subject to process variations.

To address the above challenges, this paper presents a new method for pre-bond testing of die logic using probe technology. It extends recent work on pre-bond TSV testing through probing [11], [13]. The probing technique in [11] focused only on TSV test; pre-bond testing of die logic remains a challenge, especially since logic on a die takes up more area than the TSVs. This work is focused on scan-test of die logic utilizing scan chains that can be reconfigured for pre-bond test to allow scan-in and scan-out through TSVs. This method does not require probe pads except for a few critical signals, such as power, ground, and test/functional clocks. Two different scan configurations are examined in this paper, each providing varying degrees of test parallelism. Simulations are presented that demonstrate the feasibility of the proposed test method, including area overhead, power/current delivery needs, current density in TSVs, and scan clock frequencies.

The rest of this paper is organized as follows. Section II provides an overview of related prior work. It also includes a review of the pre-bond TSV probing method from [11]. Section III introduces the proposed scan architecture for pre-bond scan test of the die logic. Section IV presents HSPICE simulation results for three dies with TSVs in a logic-on-logic 3D benchmark, highlighting the feasibility of the method presented in this paper. Finally, Section V concludes the paper.

II. Related Prior Work

A TSV is a metal pillar that connects to a metal layer and is embedded in the device substrate. To expose the TSV pillar,

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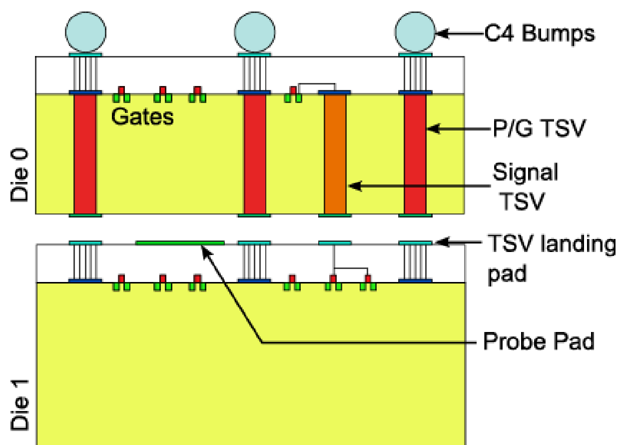

Fig. 1: An example of a back-to-face two-die 3D IC.

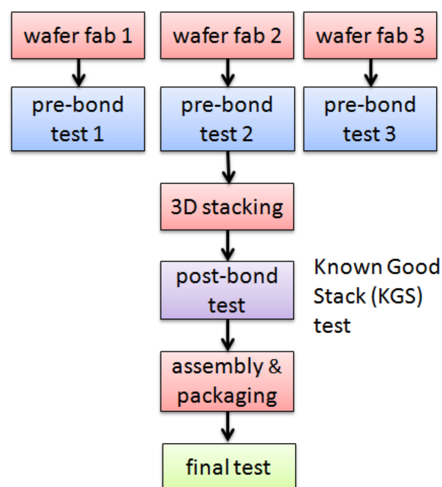

Fig. 2: A potential manufacture and test flow for a 3-die stacked IC.

much of the substrate is ground away in a process called "thinning". After thinning, metal balls called "microbumps" are added to the end of the TSV for use in bonding. Probing can be performed either on the microbumps, the bare TSV pillar, or added probe pads [11], [16], [29]. The thinned wafers are significantly more fragile than standard wafers, so they must be mounted on a carrier before probing. Probe cards that use low contact forces may also be required, as in [29]. To prevent mechanical damage to the microbump or TSV surface, the number of probe touchdowns on the same TSV must be limited.

As 3D IC testing has emerged as a considerable challenge, test architecture optimizations been proposed in the literature [7], [17]–[21]. Many of these solutions are limited to post-bond test. In [7], pre-bond test access is provided through a few oversized landing pads added to TSVs for probe needle touchdown. In [16], the authors present a die wrapper based on the IEEE 1500 standard. This die wrapper includes a wrapper boundary register for post-bond TSV testing and a switch box in the wrapper to change to a reduced pin-count pre-bond test mode. The pre-bond test also relies on oversized landing pads placed on a few TSVs for test access. There are a number of drawbacks to using large probe pads. The first is that it reduces the spacing and density of those TSVs that require pads. Second, pre-bond test requires significantly more time since test access is only available through a small number of TSVs with landing pads. Finally, pre-bond TSV test is not addressed in these methods.

Recent research has therefore been targeted at pre-bond TSV test. In [6], methods for resistance and capacitance test, such as testing TSV chains, are introduced. These tests remain conceptual, though, and no results are provided regarding their feasibility. BIST techniques for TSV testing are presented in [8], [9], [22]. However, these methods tend to use large on-die components such as voltage dividers per TSV and tuned sense amplifiers which, along with wiring complexity, require significant die area. This problem is exacerbated by the fact that a chip can have thousands of TSVs with densities of 10000/mm^2 or more [5]. Moreover, these BIST architectures do not support pre-bond die logic testing, and in many cases they may interfere with standard techniques such as a boundary scan chain on a logic die.

A. *TSV Probing*

Surface planarity of TSV microbumps impacts not only the quality of connection between a TSV and a probe needle, but also the quality of TSV contacts after bonding. It is therefore desirable not only to planarize microbumps before bonding and TSV test, but also for probes and test methods to be tolerant of non-planarity. Recently published research [27], [28] address methods for planarizing microbumps to reduce non-planarity between TSVs. The basic technology behind "springloaded" probe technologies has been available for decades [23]–[26], since good contact between a probe and a wafer or die is important in testing 2D ICs as well. These probe cards provide varying degrees of actuation between probe needs and include membrane probe cards, thermally-actuated probe needles, and probe needles with electrostatic actuators.

Recent research [29] has highlighted the promise of using low-contact force spring-loaded probe cards to make good contact between probe needles and TSVs with minimal damage to the TSVs themselves. In [29], contact was made between probe needles and microbumps on TSVs, and worst-case contact resistances of only 13 Ω were obtained. Damage was shown to be nearly non-existent until the contact force was increased to much higher levels than what is needed for a good contact. Microbumps were used as probe pads, bringing the size and pitch of TSVs on par with the probe card. This requirement limits TSV placement and density to ensure alignment with the probe card, and research shows that microbumps are scaling faster than probe cards [15].

In [11], a measurement and DFT technique was introduced to enable the pre-bond test of TSVs through probing. This method utilized a die wrapper similar to [16] but replaced the boundary scan flops with gated scan flops (GSFs), a simplified example of which is shown in Figure 3. Figure 3(a) shows the gate level design of a GSF and Figure 3(b) shows the transistor-level implementation. As in a normal scan flop,

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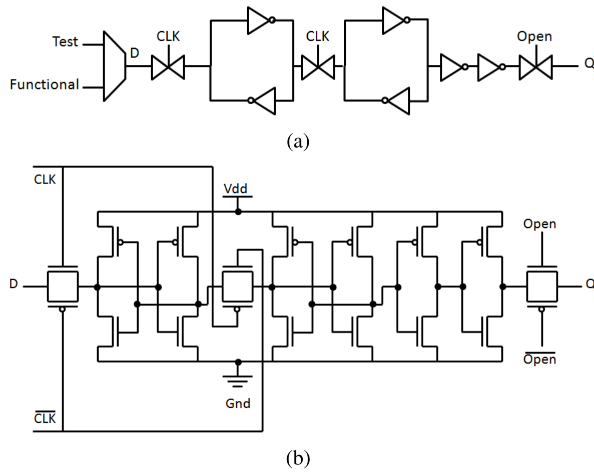


Fig. 3: An example design of a gated scan flop: (a) gate level; (b) transistor level.

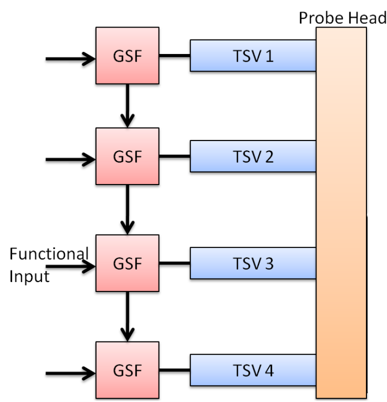
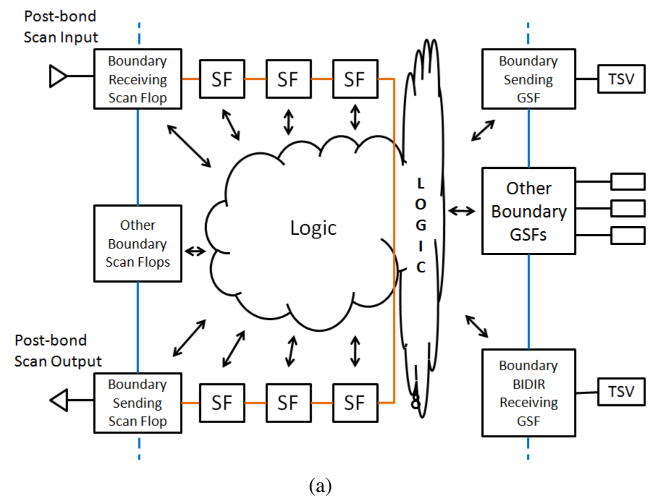
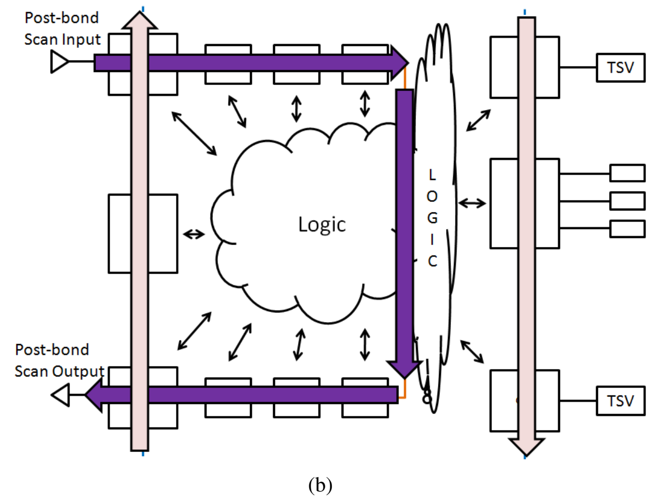


Fig. 4: A TSV network created by shorting together TSVs through a probe needle.



(a)



(b)

Fig. 5: The assumed post-bond scan architecture: (a) scan chains and logic; (b) movement of test data.

a GSF multiplexes between a test and functional input and can be connected to other GSFs to form a scan chain. The difference is that the GSFs include a buffer of two inverters and a transmission gate at the output of the flop, which accepts a new 'open' signal to switch between a low- and a high-impedance output. This design effectively allows the TSV to be driven by the GSF or to be left floating. GSFs on receiving TSVs, or those TSVs that would be driven by another die in the stack, are bidirectional in that the GSF can drive the TSV during test.

In [11], the GSFs were included before each TSV to enable pre-bond probing of TSVs. It was shown how using probe needles larger than an individual TSVs, groups of TSVs can be deliberately shorted together to form a single circuit called a network, as shown in Figure 4. Using the GSFs, the resistance of each TSV could be accurately determined, along with the average capacitance of each TSV. Contact force, and variations in contact between TSVs, were shown to have little effect on the ability to accurately characterize TSVs. Recent work in [12] shows that even in TSV networks where contact is poor or non-uniform between a probe needle and the outer TSVs in a TSV network, accurate measurement can be achieved through the aggregation method described in this paper.

A drawback of [11] is that it is limited to TSV testing. It does not support the pre-bond testing of die logic, even though the die area devoted to logic is much more than that for TSVs. This paper extends the test method introduced in [11] to enable pre-bond scan test of die logic. Scan chains are reconfigured into a pre-bond test mode in which scan inputs and scan outputs are connected to TSV networks. This allows the probe station to apply test patterns to the die and read test responses through the scan chains. A key advantage of the proposed method over [11] is that not all TSVs need to be contacted for die logic test. It is necessary to contact only those TSVs that are required for pre-bond scan. Results for a 3D benchmark in Section IV show that for 100 scan chains for pre-bond test, as few as 10.7% of the TSVs need to be contacted. Probing techniques that can be used for pre-bond test are being extensively researched [29]–[31]. The proposed pre-bond test approach is synergistic with the advances in probing that are likely to therefore emerge soon.

III. Pre-bond Scan Test

In this section, we first describe the test architecture. We assume a post-bond scan architecture similar to that proposed

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with die wrappers [16], as shown in Figure 5. Figure 5(a) shows a single scan chain and a number of boundary scan flops. The scan chain consists of typical scan flops (SFs), while boundary scan registers at the TSV interface are GSFs. As with die wrappers, some landing pads must be supplied for providing essential signals to the die, such as power, ground, and clocks. The post-bond scan input and scan output for a scan chain enter the die through the boundary register. In the bottom die in a stack, this interface is through external test pins or a JTAG test-access port. For other dies in the stack, scan I/Os are connected to the dies below it in the stack. Parallel loading of the boundary registers decreases test time, but serial scan test is also available by shifting through the boundary scan chain. This is illustrated in Figure 5(b), which shows the post-bond movement of test data. Test data can be shifted not only through the internal scan chain, but also around the boundary registers. All scan flops interact with die logic.

Multiplexers are added to the scan path to allow scan chains to be reconfigured to a pre-bond mode in which their scan-in and scan-out connections are through TSVs, as shown in Figure 6(a). A receiving GSF is chosen for the reconfigured scan-in and a sending GSF is chosen for the scan-out. Since many boundary scan registers are logically separated from internal scan chains in the post-bond mode, they need to be stitched to the scan path in pre-bond mode to enable testing. Multiplexers are added in as few places as possible to achieve access to all internal and boundary scan flops in order to minimize hardware overhead.

In Figure 6(a), we examine the multiplexers added to a single scan chain. The receiving GSF, which now acts as the pre-bond scan input, is enabled to accept its functional input driven through the TSV. Its scan output is then multiplexed into the boundary scan chain. This is done such that the sending GSF used as a pre-bond scan output and the receiving GSF used as a pre-bond scan input interface with scan flops that are adjacent to one another in the post-bond scan chain. The output of the boundary scan flop that is used to feed the pre-bond scan input is then multiplexed into the scan chain. The post-bond scan output, post-bond scan input, and other boundary registers are stitched into the scan chain. Finally, the sending GSF used as a pre-bond scan output is multiplexed to the end of the scan chain. The pre-bond movement of test data is shown in Figure 6(b). The combinational logic is not shown to retain clarity; it is the same as in Figure 6(a). Arrow color changes in the figure so as not to confuse the overlapping arrows.

The reconfigured pre-bond scan chain in Figure 6 demonstrates one of two possible pre-bond scan configurations. In this example, the pre-bond scan chain's scan-in and scan-out terminals are part of the same TSV network. Under these conditions, the scanning in of test data and the scanning out of test responses must be done separately. This is because, in order to scan in test data, the transmission gate on the receiving GSF must be set to its low-impedance state while all other gates must be set to their high-impedance states. Likewise, while scanning out, the sending GSF's gate must be set to low impedance while all others are set to high impedance. Since scan-in and scan-out occur on the same network, the maximum number of scan chains that can be tested in a single touchdown is equal to the number of TSV networks formed. In other words, the number of scan chains can at most be equal to the number of probe needles. Furthermore, if current or power limits cause the maximum scan clock frequency to be different for scan input and scan output, then the appropriate frequency must be used for the corresponding operation.

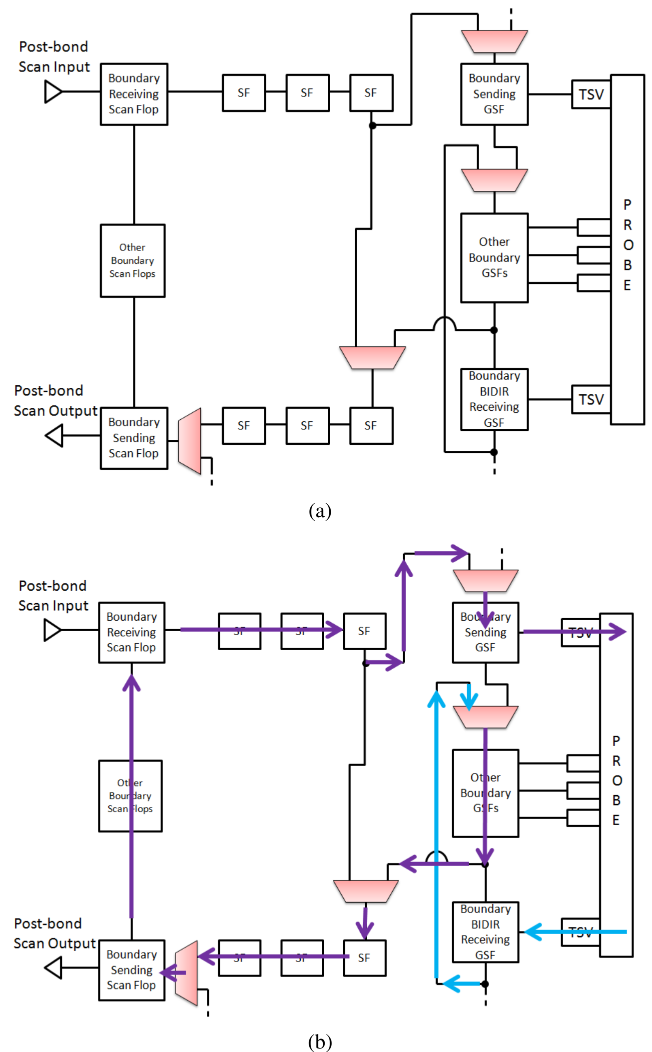

Fig. 6: Reconfigurable scan chains for pre-bond test: (a) added multiplexers; (b) movement of test data.

The other possible pre-bond scan configuration involves the scan input and scan output being on separate TSV networks, an example of which is shown in Figure 7. In this case, test responses can be scanned out while while test patterns are scanned in. The maximum number of scan chains that can be tested per touchdown is reduced to half of the number of probe needles (or half of the number of TSV networks). Both scan input and scan output operations must occur at the lower of the possible scan frequencies, since both operations occur simultaneously. It should be noted that pre-bond functional test cannot be conducted while using TSV networks, since it is not possible to supply individual inputs to TSVs within a network at the same time.

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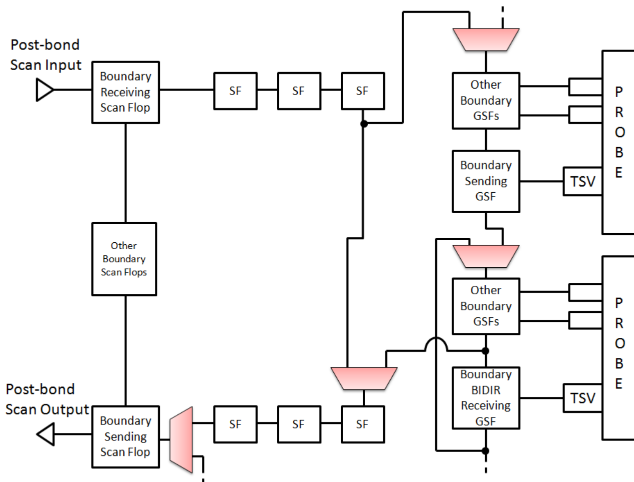

Fig. 7: A reconfigurable scan chain with pre-bond scan input and scan output on different TSV networks.

IV. Discussion and Results

In this section, we address a number of key criteria needed to demonstrate the feasibility of the proposed method:

- The current needed to be delivered to the device under test during pre-bond scan test must fall within the current-carrying capacities of TSVs and probe needles.
- The speed at which TSV networks are charged and discharged must be reasonable such that the pre-bond scan test time is low.
- The area overhead of the proposed method must be small.
- That boundary scan registers are necessary to achieve high coverage in pre-bond scan test.

We next present simulation results demonstrating the feasibility of the methods given in this paper. Simulations were conducted in HSPICE on a 3D logic-on-logic benchmark. The resistance and capacitance used for each TSV of 5 μm diameter were 1 Ω and 20 fF, respectively [9], [33]. Transistors were modeled using a predictive low-power 45 nm model [34]. Transmission-gate transistor widths were set to 540 nm for PMOS and 360 nm for NMOS. These larger widths were chosen such that the gate, when open, would have little impact on signal strength. For each GSF, a strong and weak inverter were used, with the strong inverter having widths of 270 nm for PMOS and 180 nm for NMOS, and the weak inverter having 135 nm for PMOS and 90 nm for NMOS. These were chosen such that the majority of transistor W/L ratios were 2/1 for NMOS and 3/1 for PMOS. The power supply voltage for both the probe and the circuit was taken to be 1.2 V.

A. 3D IC Benchmark

Since 3D IC benchmarks are not available in the public domain, we created a benchmark from a Fast Fourier Transform (FFT) circuit chosen from the OpenCores set of benchmarks [35]. It is synthesized using the Nangate open cell library at the 45nm technology node [36]. The total gate count after synthesis is 299,273, with 19,962 flip-flops. The design

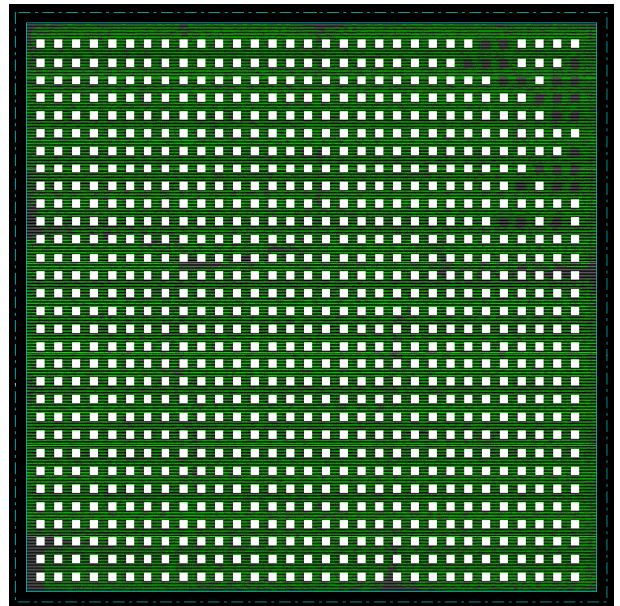

Fig. 8: Layout of die 0 of the 4-die FFT benchmark, with standard cells in green and TSVs in white.

was partitioned into 4 dies, with the gate counts in each die being 78,752, 71,250, 78,367, and 70,904, respectively. The logic gates in each die are placed using Cadence Encounter, and TSVs are inserted in a regular fashion, using a minimum spanning tree approach [37]. Back-to-face bonding is assumed, which means that TSVs are present only in the first three dies. The TSV counts are 936, 463, and 701, respectively. The TSV diameters in this chip are 5 μm. The circuit was routed such that each TSV has a small microbump sized at 7 μm, and the total TSV cell size including keep out zone is 8.4 μm, which corresponds to six standard cell rows. Each die is then routed separately in Cadence Encounter. The bottom die of the 4-die layout is shown in Figure 8, with TSVs in white and standard cells in green.

Boundary scan cells were added at the TSV interface. We motivate the need for inserting boundary registers at the TSV interface by examining die 0 of the 4-die FFT benchmark. Without boundary scan registers, the pre-bond stuck-at fault coverage is only 44.76%. With boundary registers added, the coverage increases to 99.97%. This is a significant increase, especially considering that the die only contains 936 TSVs, and an industry design may contain tens of thousands of TSVs. The area overhead of the boundary scan GSFs and scan chain reconfiguration circuits was 2.2% of the total number of gates.

B. Simulation Results

We first examine the feasibility of performing scan test through probe needles in terms of sourcing and sinking currents. To determine an upper limit on the current drawn, scan chains were inserted into the benchmark. In order to manage the complexity of circuit-level HSPICE simulation, scan chains were limited to a length of 8 (6 internal scan cells and two boundary scan cells for pre-bond scan I/O per chain). Stuck-at and transition test patterns for this design were

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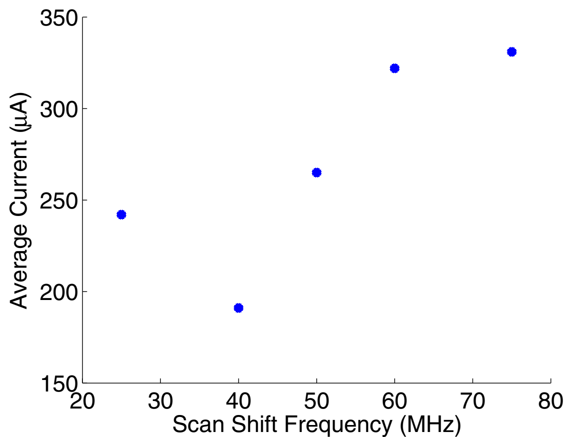

Fig. 9: Average current drawn at 25, 40, 50, 60, and 75 MHz scan shift frequency.

Test Parameter	Die 0	Die 1	Die 2
Peak Current	1 mA	1 mA	1.1 mA
Avg. Current (stuck-at)	300 μA	294 μA	327 μA
Avg. Current (transition)	432 μA	341 μA	383 μA
Area Overhead	2.2 %	1.0 %	1.2 %

TABLE I: A comparison of the results of three dies with TSVs in the 3D stack.

Number of Scan Chains	% of TSVs to be Contacted	
	Configuration A	Configuration B
25	2.7	5.3
50	5.3	10.7
75	8.0	16.0
100	10.7	21.4

TABLE II: Percentage of TSVs that must be contacted for Die 0, as a function of the number of scan chains and scan configuration.

generated using a commercial ATPG tool and ordered based on toggle activity. Test generation yielded the toggle activity per pattern and fault coverage of 99.97% for stuck-at patterns and 97.65% for transition patterns. For the pattern with highest peak toggle activity, we simulated the scan chain that had the largest number of transitions for that pattern.

Figure 9 shows the current drawn for shifting in the stuck-at pattern and shifting out test responses at 25, 40, 50, 60, and 75 MHz shift frequency. At 50 MHz, current drawn averaged at around 300 μA and, at all frequencies, peaked at almost 1 mA for about a tenth of a nanosecond. For a high toggle-activity transition fault pattern using launch-off-shift and a 1 GHz functional clock, an average current of 432 μA is drawn during capture and peak current is similar as for stuck-at patterns.

It has been reported in the literature that a TSV can handle a current density higher than 70,000 A/cm^2 [38]. Published work on TSV reliability screening indicates that a sustained current density of 15,000 A/cm^2 is possible through a TSV without damage [39]. To sustain a peak current of 1 mA through a single 5 μm TSV in the pre-bond test method would require the TSV to be capable of handling a current density of 5093 A/cm^2. To handle a 300 μA average current, a TSV must be capable of sustaining a current density of 1528 A/cm^2. Both these numbers are well below the maximum allowable current density.

In addition to the current density limits of the TSVs, we also need to consider the amount of current that the probe needles can deliver. It has been shown in the literature that a 3 mil (76.2 μm) cantilever probe tip is capable of supplying 3 A of current for a short pulse time (less than 10 ms) [40], [41]. In the worst case, assuming that all scan chains and logic in the benchmark draw the peak current at once, the probe tip would have to supply 3 A of current for less than 0.1 ns. This falls within the probe current-supply specification. If current supply from the probe is an issue, a variety of well-known methods can reduce peak and average test power on die during test, including partitioning the circuit into separate test modules, clock gating, and low-power patterns [42]–[44].

We can also examine the feasibility of the proposed method from a test-time perspective. The frequency at which scan-in and scan-out can take place depends on a number of factors. Scan-in speed depends on the strength of the probe-needle driver while scan-out depends on the strength of the TSV driver in the sending GSF used as a scan output. Both of these drivers must be able to charge and discharge the TSV network capacitance fast enough to meet the setup and hold times of the scan flops given the test clock frequency. Therefore, the number and capacitance of TSVs in a network also influences maximum scan clock frequency.

Simulations were performed assuming a probe card with 100 probe needles [29]. The design contains 936 TSVs and we assume that TSV networks are roughly balanced, so we simulated a worse-case network of 11 TSVs. This results in a network capacitance of 220 fF. For scan-out, we examined two separate buffers with W/L ratios of 4 and 6 to drive the TSV. Maximum scan-out frequencies were determined to be 50 MHz for the 4 W/L buffer and 98 MHz for the 6 W/L buffer. The probe driver is limited by the maximum current rating of the probe tip, delay of internal transmission gates to switch between driving and receiving, and probe-needle resistance. The maximum scan-in frequency was determined to be 185 MHz. These frequencies reflect typical scan shift frequencies, which tend to be significantly lower than functional clock frequencies.

Table I compares results between Die 0, Die 1, and Die 2. The worst-case stuck-at pattern current drawn was taken at 50 MHz. Since neither the driver strength nor the TSV network size were changed for these simulations, maximum scan-in and scan-out frequencies were equal for the dies.

We next examine the effect of scan configuration on test time. In Section III, we described two possible scan configurations—one in which the scan I/Os for a scan chain are on the same TSV network (Configuration A) and one in which they are on separate networks (Configuration B). The scan frequency, scan chain length, number of scan chains, and number of TSV networks determine which configuration results in a lower test time. We present two examples to highlight this issue.

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For Die 0 of the 4-layer FFT benchmark (Die A in Table I), if we create 50 scan chains, the result is a maximum scan chain length of 402 cells and 633 stuck-at test patterns. We assume a probe card with 100 probe needles for contacting TSV networks. We further assume that Configuration A utilizes the maximum scan-in (185 MHz) and scan-out (98 MHz) clock frequencies. Configuration A can use different scan-in and scan-out frequencies because these two shift operations are not performed in parallel. However, scan-in and scan-out are not overlapped. In this case, configuration A requires 4.0 ms to complete stuck-at scan test. Configuration B, operating only at 98 MHz only, requires 2.6 ms since it can scan out test responses while scanning in the next test pattern.

If on the other hand, the die has 100 scan chains, the maximum scan chain length is 202 cells and ATPG results in 640 stuck-at patterns. Since Configuration A can handle a maximum of 100 scan chains in a single touchdown, it needs to contact the die only once. This results in a test time of 2.0 ms. Configuration B requires two touchdowns; each time it is only capable loading and unloading 50 scan chains. We assume that the die is partitioned into separate test modules each of 50 scan chains such that coverage remains high. In this case, Configuration B requires 2.6 ms for test plus the time required align the probe card and for the second touchdown.

As stated in Section II, not all TSVs need to be contacted for die logic testing. This is an important advantage, especially if TSV or microbump damage due to probing is a concern. Table II shows what percentage of TSVs must be contacted depending on the number of scan chains present on the die and the scan configuration used. If oversize probe pads are used with the same number of scan chains, significant overhead must be incurred due to the large number of probe pads (even with test compression solutions), If the number of probe pads is limited, the test time will be higher because of constraints on the number of scan chains.

V. Conclusions

We have shown how TSV probing can be used not only for pre-bond TSV test, but also for full-scan pre-bond die logic test. We have shown that scan chains can be reconfigured into a pre-bond state to use TSV networks for scan I/O while preserving significant test parallelism and not requiring many oversized probe pads. We have presented HSPICE simulation results to highlight the feasibility and effectiveness of this approach. We have shown that the current needed for testing can be supplied through TSVs and probe needle tips. We have also shown that test clock frequencies remain relatively high even with the increased TSV network capacitance and that the frequency can be tuned by adjusting the strength of drivers of the TSV network. The area overhead was estimated to be between 1.0% and 2.2% for three dies with TSVs in a 4-die logic-on-logic 3D stack.

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