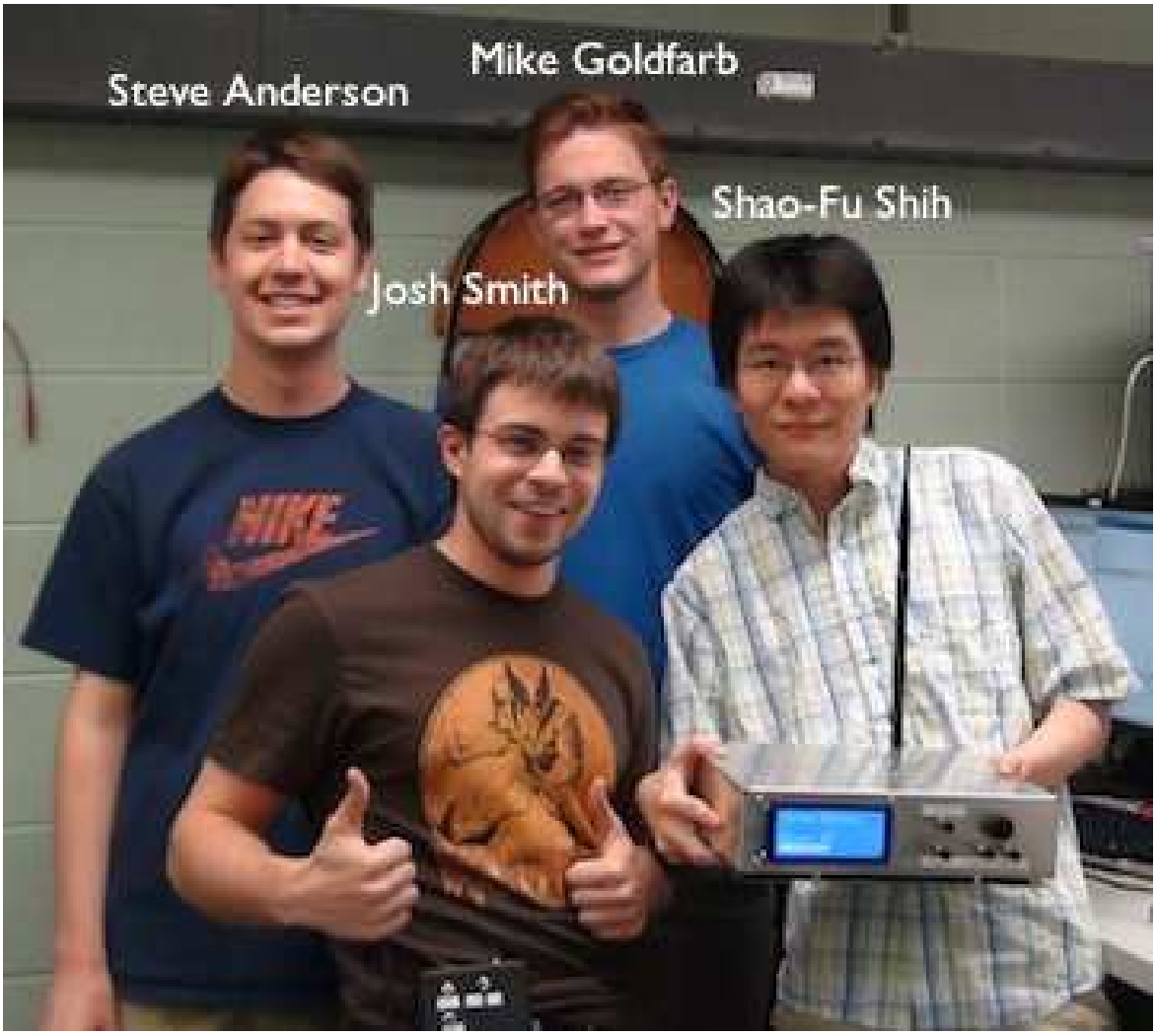
ECE 477 Final Report – Spring 2010
Team 6 – Digital Sound Projection



Team Members:

#1: Steve Anderson	**Signature: _____**	**Date:** 05/05/2010
#2: Mike Goldfarb	**Signature: _____**	**Date:** 05/05/2010
#3: Shao-Fu Shih	**Signature: _____**	**Date:** 05/05/2010
#4: Josh Smith	**Signature: _____**	**Date:** 05/05/2010

CRITERION	SCORE	MPY	PTS
Technical content	0 1 2 3 4 5 6 7 8 9 10	3	
Design documentation	0 1 2 3 4 5 6 7 8 9 10	3	
Technical writing style	0 1 2 3 4 5 6 7 8 9 10	2	
Contributions	0 1 2 3 4 5 6 7 8 9 10	1	
Editing	0 1 2 3 4 5 6 7 8 9 10	1	
Comments:		**TOTAL**	

TABLE OF CONTENTS

Abstract

Digital Sound Projection is a high quality audio transceiver for use in music or lecture hall venues and personal settings. A portable transmitter accepts a microphone or line input and transmits the audio signal wirelessly to the receiver base station. From the receiver the user can adjust audio characteristics with equalization controls or enhance vocal components with Digital Mute. An LCD interface simplifies the user controls for adjusting the different audio settings. An EQ screen allows the user to adjust the amplitudes of 11 frequency bands from 20Hz up to 24kHz. The digital mute function allows the user to enhance vocal harmonics in order to selectively amplify human voice.

1.0 Project Overview and Block Diagram

1.1 Project Overview

Digital Sound Projection consists of a transmitter and a receiver unit. The transmitter accepts an analog stereo line or microphone input. Each signal is converted into a differential signal through the DRV134, amplified using the PGA2505 microphone preamplifier, buffered with the OPA1611 op-amp, and finally converted into a digital signal by the PCM4202. The digital signal is then modulated by the nRF24Z1 transceiver and sent to the receiver via a 2.4GHz wireless channel.

The receiver takes an input audio signal from either the transmitter or directly from an analog line-in. Equalizer effects are then applied digitally through the SHARC ADSP-21262 DSP chip. The user is capable of defining the EQ effects through an LCD user interface controlled by the ATmega168 microcontroller. The UI also enables the user to apply a voice enhancement algorithm implemented by the SHARC and select the input signal source. After signal processing, the digital audio signal is converted back to analog through the PCM1792A DAC and output to speakers.

1.2 System Level Diagram

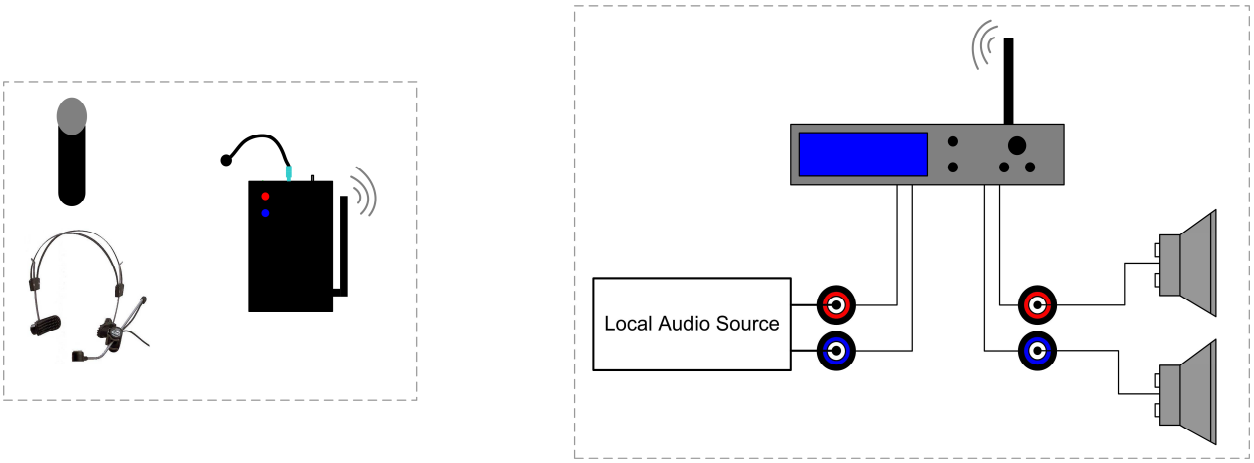


Figure 1-1: System Level Diagram

1.3 Transmitter Block Diagram

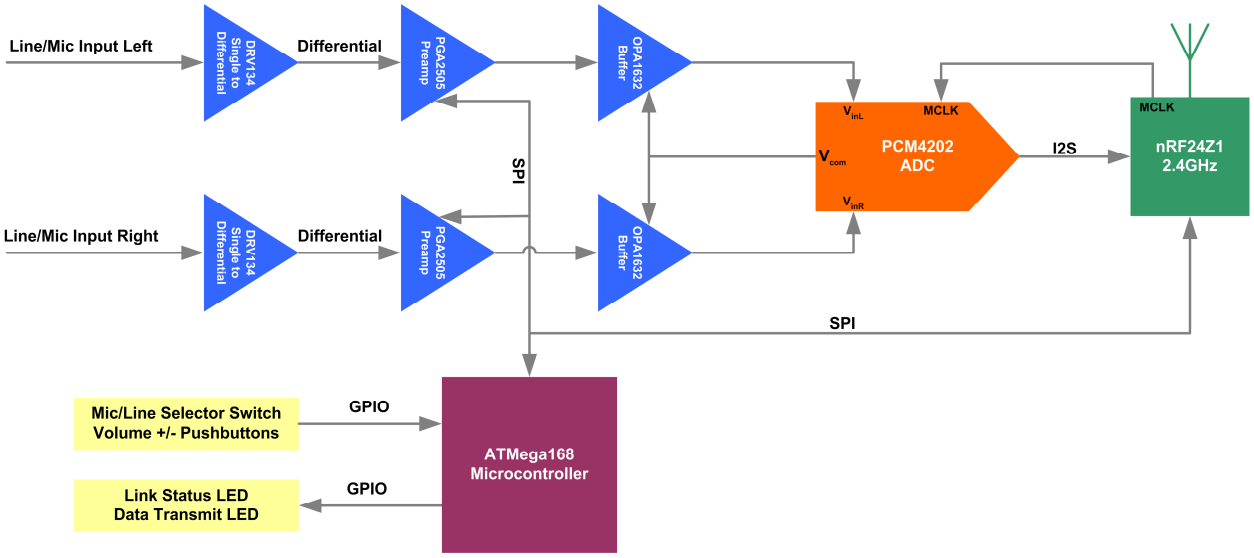


Figure 1-2: Transmitter Block Diagram

1.4 Receiver Block Diagram

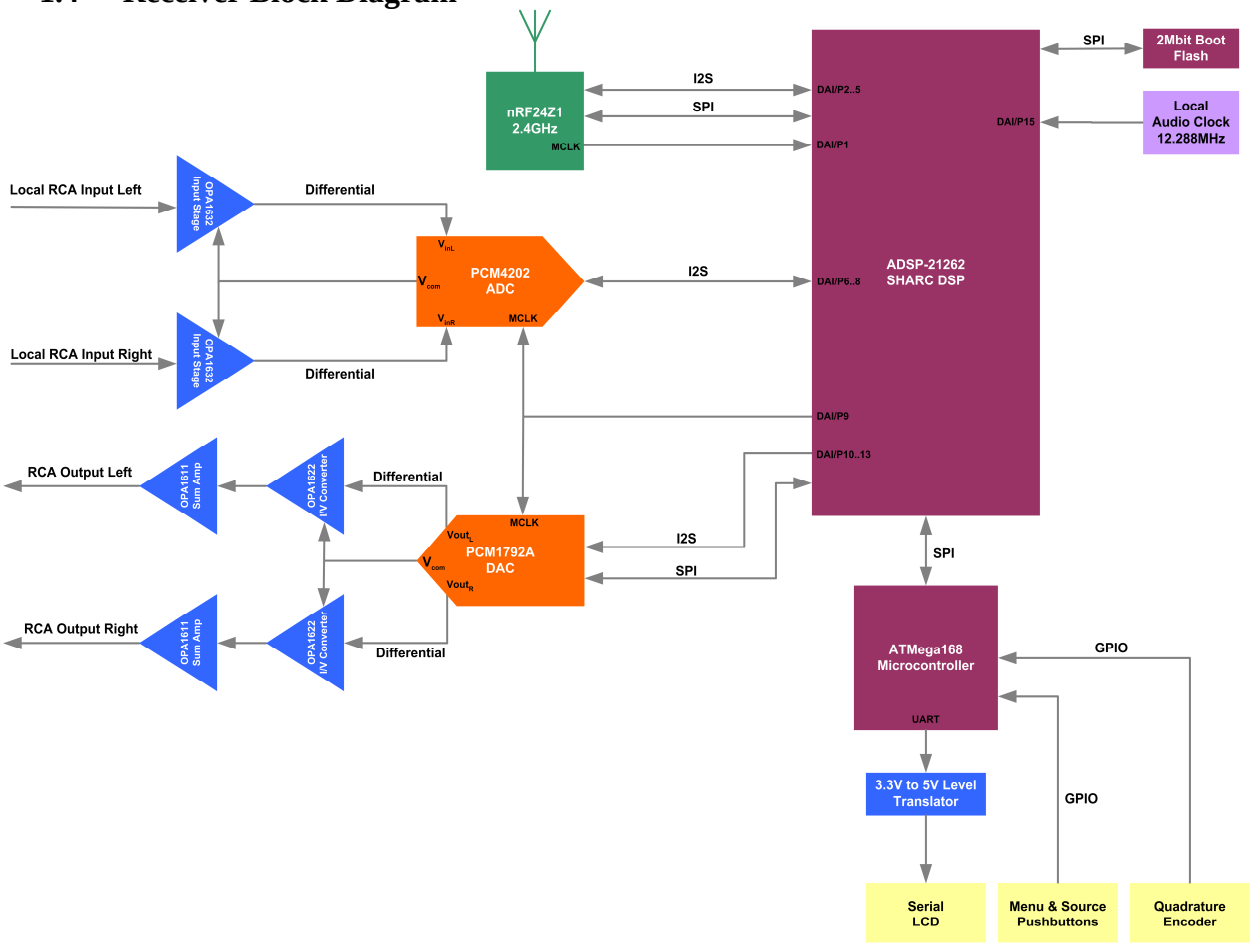


Figure 1-3: Transmitter Block Diagram

1.5 Photograph of Digital Sound Projection System

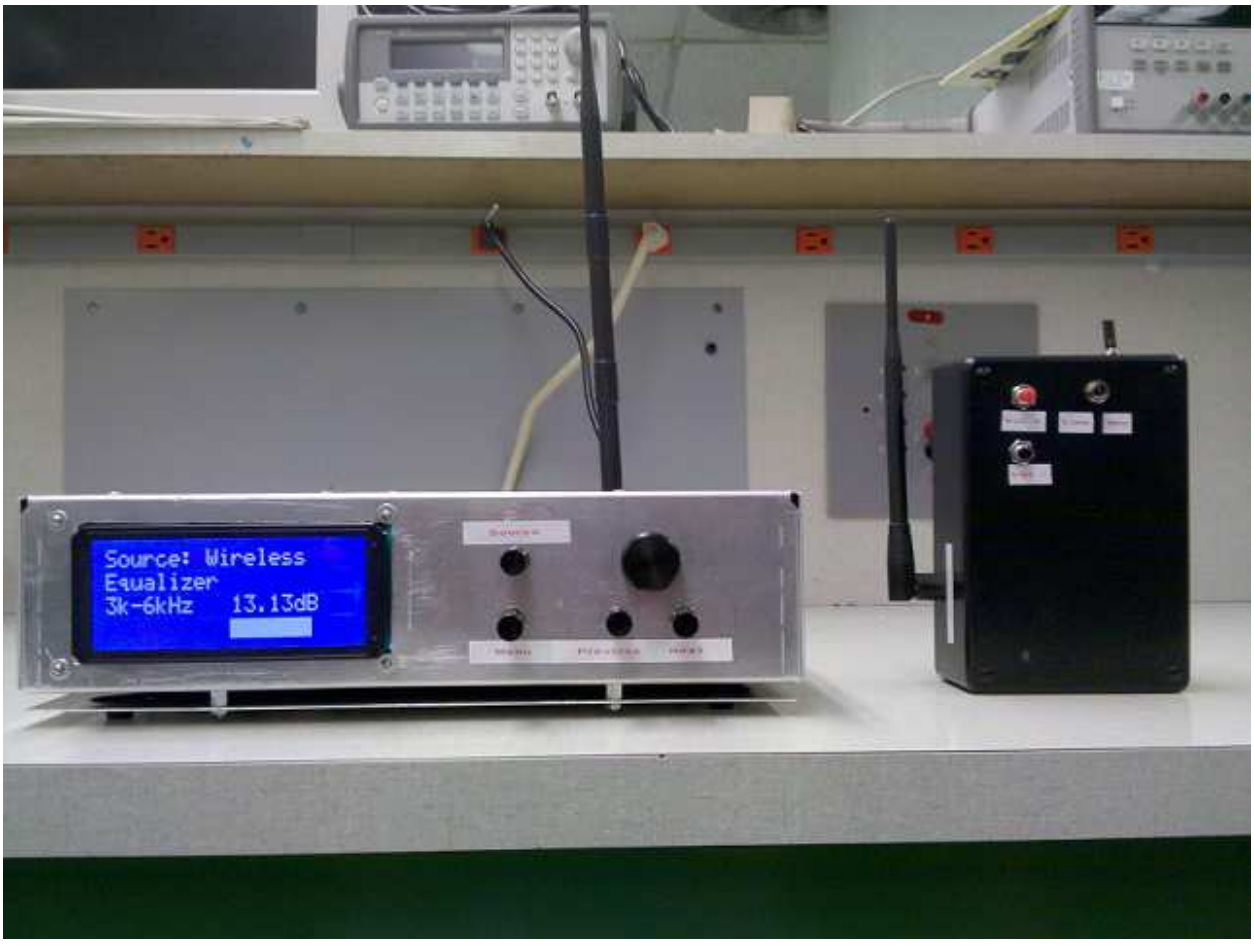


Figure 1-4: Digital Sound Projection

2.0 Team Success Criteria and Fulfillment

2.1 Project-Specific Success Criteria

1. An ability to wirelessly transmit and receive a digital audio signal.
2. An ability to display information to the user on an LCD about the status of the device.
3. An ability to apply digital mute to the audio signals based on a threshold.
4. An ability to allow the user to adjust EQ effects applied to audio signals.
5. An ability to control output volume wirelessly from the transmitter.

2.2 Assessment of PSSC Fulfillment

All PSSC's have been satisfied by the Digital Sound Projection design.

1. The unit successfully transmits a digital audio signal between the transmitter unit and receiver base.
2. The unit successfully displays information regarding the system to the user via an LCD interface. Separate menus are provided for the three major adjustable settings on the receiver: volume, EQ, digital mute. The rotary encoder and push buttons allow the user to manipulate settings on each screen of the user interface.
3. Digital mute based on a threshold is successfully implemented in Digital Sound Projection. A user can selectively boost or reduce harmonic components of human voice by setting the upper and lower frequency boundary and specifying a gain value.
4. The user can apply EQ effects to audio by adjusting the gain of 11 separate frequency bands.
5. The user can increase or decrease the output volume wirelessly from the transmitter using pushbutton controls.

3.0 Constraint Analysis and Component Selection

3.1 Introduction

Processing digital audio in real-time is computationally expensive and requires a microprocessor that executes fast enough to maintain the necessary level of throughput without dropping audio samples or degrading audio quality. High quality analog to digital and digital to analog converters with high dynamic range and low harmonic distortion are necessary to ensure undistorted audio input and output. This section will address the constraints that must be met to produce a successful design along with the rationale for major component selection based upon the constraint analysis.

3.2 Design Constraint Analysis

In this section, the major design constraints will be addressed. As the most critical design challenges, computational, interfacing, and peripheral requirements will be emphasized. Important power, packaging, and cost constraints will also be covered.

3.3 Computation Requirements

The device will require a high-performance digital signal processor to perform real-time digital audio processing. Equalizer effects and digital mute will be applied to large blocks of 2048 audio samples using the method of FFT convolution. FFT convolution takes advantage of the property that multiplication in the frequency domain is equivalent to convolution in time domain. Performing signal processing in the frequency domain is conceptually simple and provides greater software flexibility. The digital signal processor must compute the FFT, process frequency domain data, and compute the inverse FFT within the maximum amount of time required to collect the next set of audio samples. Audio will be sampled at a rate of 48kHz, limiting the maximum processing time to 42.7ms per 2048 sample block. After this amount of time passes the next sample block will have been filled, not processing this block in time would require the entire sample blocks to be skipped.

All signal processing algorithms will be carried out using 32-bit floating-point arithmetic. Floating-point representation is preferable because quantization noise is thousands of times

smaller [1] when compared to fixed-point. The total amount of RAM required for storing and processing input samples, not including program space, (i.e. stack, heap, and program) is given by: $M = 15 * 32 * N$, where N is the number of sample points per block, and M is the number of bits required to perform the FFT convolution. The DSP requires at least 983,040 bits of data memory for a block size of 2048 floating point samples.

3.4 Interface Requirements

General purpose I/O is split between user interface components and SPI chip selects signals for off-chip slave peripherals. The receiver's user interface contains a LCD, a rotary encoder, and several push buttons. A CFA634-TMC-KS serial character LCD requires a UART capable of a minimum 9600 baud with a TTL voltage swing of 0 to 5V [2]. A 3.3V to 5V level translator will be required to interface with the LCD data lines with microcontroller's UART pins. The EVEG rotary encoder requires two digital I/O pins for quadrature pulses. [12] Four to five push buttons will be used to select between several user interface displays and to move between on screen selections. The DSP requires four general-purpose I/O pins for SPI chip select signals used for off-chip slave peripherals.

3.5 On-Chip Peripheral Requirements

The transmitter's microcontroller is responsible for configuring the microphone pre-amp and wireless transmitter through a serial peripheral bus. A minimum of one SPI controller is required to initialize and control these components. A microcontroller also is used to control the user interface on the receiver. The user interface microcontroller requires at least one SPI peripheral to communicate with the DSP. Both the transmitter and receiver microcontrollers SPI peripherals must be capable of 1MHz clock speed and have configurable modes. Each microcontroller should also include an I2C capable interface to plan for unforeseen peripheral requirements or an additional SPI controller.

The DSP requires at most three I2S capable serial ports for interfacing with the wireless audio transceiver, an ADC, and a DAC. It may be possible to use two serial ports if the clock, frame sync and bit clock can be shared between the ADC and DAC. A dedicated serial port must be used to interface with the wireless audio transceiver due to the mismatch in data word sizes.

The DSP also requires at least one SPI controller to configure the DAC, wireless transceiver chip, and to communicate with the user interface microcontroller. The DSP SPI controller should also be capable of operating in either master or slave mode.

3.6 Off-Chip Peripheral Requirements

The device requires both analog to digital and digital to analog converters capable of 24-bit resolution at a sampling rate of 48kHz. The ADC and DAC must also implement the I2S serial audio interface to connect with the DSP and the wireless transceiver. To ensure the best possible audio signal quality the DAC and ADC should have a very high dynamic range and low total harmonic distortion. An external wireless transceiver is required to stream audio data from the ADC on the transmitter to the DSP on the receiver. The wireless transceiver should be capable of interfacing directly with the DSP and the ADC using I2S. Configuration of the ADC, DAC and wireless transceiver should be performed through a common peripheral bus such as SPI or I2C.

3.7 Power Constraints

The wireless transmitter should be battery powered with NiMH rechargeable batteries to enable the user to carry the device without additional wires that restrict movement. An estimated 200mA (based off datasheets) is required to power the transmitter components. On the receiver a +15V and -15V supply is required to power high quality operational amplifiers on the audio output stage.

3.8 Packaging Constraints

The wireless transmitter is designed to be small and light enough to clip to a users belt or pocket. Care must be taken when considering antenna size and placement to ensure the best possible reception while not making the transmitter awkward to wear. Analog and digital components should be separated and possibly shielded on the PCB of both the receiver and transmitter to ensure minimal RF contamination of the analog audio signal.

3.9 Cost Constraints

The device should be competitive with other wireless audio systems on the market while providing additional features not present in existing products. The freePORT Presentation Set, a wireless audio system with wireless microphone from Sennheiser, retails for $375.95. [3] Another system, the Shure ULX Standard Series – Instrument System, also provides quality wireless audio transmission, for $759.00. [4] Both of these products provide more wireless channels than our device will support, however, our device will provide additional audio capabilities without the need for additional audio processing hardware.

3.10 Component Selection Rationale

Component selection is based on the constraints covered in the previous section with special consideration given to performance, ease of use, and interface flexibility. Two floating-point DSPs are compared: TMS320C6711D (TMS320) from Texas Instruments and ADSP-21262 from Analog Devices. The PCM4202 ADC and PCM1792A DAC from Texas Instruments are compared against the Analog Devices AD1936 audio codec. For wireless audio transmission, the nRF24Z1 wireless audio transceiver from Nordic Semiconductor is compared with the DARR80 digital baseband processor from STS.

The DSP that best meets the computational and interfacing constraints is the ADSP-21262 (SHARC) from Analog Devices. The SHARC is a high-performance (1200 MFLOPs), DSP supporting 32-bit floating-point and 32-bit fixed-point computation with two independent computational units. An I/O processor provides 22 separate DMA channels, a dedicated SPI port, six serial ports and configurable general-purpose I/O pins. The I/O processor includes a software programmable signal routing unit (SRU) that allows any I/O processor port to be connected to any of the 20 external processor pins. [5] The TMS320 is a 32-bit floating point, high-performance (1500 MFLOPs) DSP with 512Kbits of RAM, and eight independent computational units. The TMS320 includes 16 independent DMA channels, two multi-purpose serial ports, and five general-purpose I/O pins. The SHARC meets all computational, memory, and interfacing requirements and includes several desirable features not present in the TMS320. While comparable to the SHARC in computational speed, the TMS320 lacks the I/O flexibility provided by the SHARC's signal routing unit. The SHARC also includes a larger amount on on-chip RAM, avoiding the need to interface to slower external memory.

High quality ADC and DAC channels with high dynamic range and low total harmonic distortion (THD) are essential for ensuring high quality audio. The AD1936 audio codec from Analog Devices provides four ADC channels with a dynamic range of 109dB and -98dB THD. Eight DAC channels with 107dB dynamic range and -98dB THD are packaged with the DAC channels for an all-in-one chip solution. [7] While the AD1936 performs well, most of the DAC and ADC channels would be unused, especially on the transmitter where only two ADC channels are required. The PCM4202 from Texas Instruments is a two channel ADC with 118dB dynamic range and -105dB THD. [8] The PCM4202 has higher performance characteristics and fewer channels which better meets the interfacing requirements of both the receiver and transmitter. The PCM1792A two-channel DAC from Texas Instruments has a 127dB dynamic range and -108dB THD [9] also outperforms the AD1936 and better meets the interfacing requirements of the receiver.

The wireless audio transceiver must be capable of interfacing directly with the DSP and ADC peripherals using an I2S audio serial interface. A glueless digital audio interface is required to maintain the necessary throughput of high quality audio. The nRF24Z1 from Nordic Semiconductor transmits 16-bit CD quality audio on the 2.4GHz ISM radio band. Audio data is transferred into and out of the nRF24Z1 using an I2S audio interface. [10] The DARR80 from STS implements all of the features found in the nRFZ241 but includes support for up to eight audio channels. Unlike the nRF24Z1, the DARR80 requires an external 802.11 frontend radio and only supports I2C bus for configuration and initialization. [11] The nRF24Z1 was selected due to the availability of documentation, smaller pin count, an on-chip radio interface, and its inclusion of an SPI port for configuration.

3.11 Summary

In this section, several major components were selected based on key design constraints. The ADSP-21262 digital signal processor was chosen for its 2Mbit and I/O flexibility. Separate high-performance DACs and ADCs from Texas Instruments were selected over a single integrated audio codec because of their superior performance characteristics and lower channel count. Lastly, the nRF24Z1 wireless audio transceiver provides the necessary audio interfacing and RF stack in a single-chip package.

4.0 Patent Liability Analysis

4.1 Introduction

Digital Sound Projection (DSP) is a wireless audio system for a microphone or direct line input. The user then is able to modify the audio signal on the receiver by adjusting the Equalization (EQ) effects shown on an LCD screen. After these effects have been applied by a digital signal processor, the signal is then sent to speakers through a 2 channel stereo output. Two of the main functions for DSP are the wireless transmission of the input microphone signal from the transmitter to the receiver and the ability for the user to apply EQ effects on the received signal to their preference. DSP's design, specifically the two prior functions listed, must be designed in a manner as to not infringe on any prior patents or product designs.

4.2 Results of Patent and Product Search

The patent database was searched in order to analyze the patent liability associated with Digital Sound Projection's major functions. In addition to the patent search, products that perform similar functions were investigated in order to determine if any ideas or designs were infringed upon in DSP's design. Some of the major functions that DSP performs that are of concern involve the implementation of the wireless system and the signal processing done on the input signal in order to improve quality.

The first patent that was investigated for the design of a wireless audio system is Patent 7,680,465. [1] This patent was filed on July 31, 2006, and involves a wireless audio device and improving the sound quality based on user-specific audio parameters. This audio device receives its input from a wireless source, and then allows the user to adjust the gain of individual frequency bands and does this processing using a digital signal processor. It then outputs the audio signal directly to speakers or transmits it wirelessly to another device. The patent covers basically any wireless scheme and allows for an operating frequency range of any MHz or GHz as shown in the detailed description section of the patent.

Another product that shared similar functionality as the DSP is the Shure line of wireless microphone systems. [2] An example device shows that Shure has designed a body pack that receives a microphone input and outputs at a specific frequency to a tuned receiver that outputs to some speakers or another audio device. This devices' wireless operation frequency is around

700 MHz and is tuned/selected based on the user's input from the base receiver and transmitter. The transmitters have automatic frequency selection and offer the choice of using a microphone input or a direct line input.

Technical-pro also has a product that performs a similar function as Digital Sound Projection. [3] The RX-B32 is a home audio receiver that has the capability of accepting 3 RCA inputs and 2 microphone inputs. The receiver also has built-in antennas that receive AM and FM radio. This receiver has the ability to choose whether to use the microphone input or the RCA inputs and allows the user to input some parameters in order to improve the quality of the input signal to their preference. The output is then sent to 2 main speakers or through surround sound if selected by the user.

4.3 Analysis of Patent Liability

Digital Sound Projection has many similarities with other products and existing patents. [1] For example, Patent 7,680,465 and Digital Sound Projection both accept an audio signal from an RF source and allow for the user to input different audio parameters into the system to generate a user-specific audio signal. For both products this involves determining the coefficients for different frequency bands and using these coefficients to adjust the signal in a digital signal processor. Both systems then output this new audio signal to speakers. Also, each device uses a controller to manage the user input along with the rest of the system on the receiver. The patent uses a description of a general "controller" managing the devices in the system, but DSP specifically uses the ATmega168 microcontroller to manage the user input and ICs on the transmitter and receiver. Digital Signal Projection is similar enough to the patent's design that it could potentially infringe under the doctrine of equivalents. DSP performs the same overall functions, but it would depend on how the software is structured in the design within the patent. The patent does not list how it performs the user specific input on the audio source using the processor. However, DSP analyzes the incoming audio signal by taking the FFT and then uses the amplitude coefficients for the frequency bands to perform the Equalization effects on the audio signal. Another difference may apply with the circuitry involved in outputting the signal from the digital signal processor to the speakers. Again the patent does not explain how it is done, but for DSP the data output from the processor passes through a digital to analog converter and then through a IV-conversion stage to produce a 2-channel stereo output.

The designs in Patent 7,680,465 and that of DSP also receive the inputs to their systems from a wireless RF source. [1] The patent is designed to accept an audio input from any wireless link; specifically it will be able to operate in the 2.4 GHz frequency range. DSP, on the other hand, only is designed to receive its input from the matching wireless transmitter. This RF signal also is transmitted in the 2.4 GHz range, but the nRF24Z1 uses a frequency shifting algorithm in order to find an unused frequency for transmission in the 2.4-2.45 GHz range, and the patent does not describe the wireless modulation scheme that is implemented in their design. The wireless transceiver used in DSP is designed specifically for transmitting/receiving high fidelity audio signals where the patent does not make this distinction.

The Shure wireless microphone systems are other products that perform the same general function as Digital Sound Projection. For both systems, a user connects either a microphone or a direct audio line into the transmitter, and then the signal transmits wirelessly to the base receiver. The major differences in operation occur in the receiver. [2] The Shure systems receive the signal from the transmitter and then output the signal to the speakers, whereas DSP allows the user to modify the signal before outputting to the speakers. For Shure's design, the only major UI on the receiver involves selecting the frequency of operation for the wireless transmission. There are enough differences in the receiver portion of the designs after the signal is received that there is no possibility that DSP infringes on Shure's designs. The potential for infringement comes from the transmitter and the wireless transmission. The Shure system transmits at around 700 MHz whereas DSP transmits at 2.4 GHz. Again, DSP's wireless transceiver uses GPSK which is not a common modulation scheme. This and the fact that transmitting a signal through RF is non-trivial enough that DSP's design would not be infringing on Shure's wireless designs. There is also no specific software being written in DSP's transmission that would potentially infringe on Shure's designs.

Technical-Pro's RX-B32 audio receiver is another product that performs the same overall function as the Digital Sound Projection. [3] Both receivers can accept either a microphone input or a stereo (RCA) input. Each product then allows the user to change the settings of the audio signal given some parameters and then outputs the signal to speakers. However, the purpose of the UI is different for both devices. The RX-B32 has a limited interface of only being able to adjust bass, treble, echo, and volume; whereas the DSP design allows for adjustments of the amplitude for different frequency bands and allows for an overall volume modification and

mute, with these adjustments output on an LCD screen. The RX-B32 also allows for AM/FM radio from the antenna input. DSP allows for a wireless input as well, but it is from the matching transmitter of the receiver that accepts a microphone or line input. Even though these two products achieve the same general function of improving an audio signal based on a user's input, there are enough differences so that DSP does not infringe on the RX-B32's design.

4.4 Action Recommended

Even though Patent 7,680,465 covers many of the same functions and ideas in Digital Sound Projection's design, the specific claims of the patent are obvious enough for DSP to not infringe on the patent's design. The patent does not explain how any of the claims are implemented or even give any idea of what kind of algorithm or software is used. Because of the generality of the claims, DSP would not have any significant potential for infringing under the doctrine of equivalents. However, if a lawyer interpreted that the design of DSP was actually infringing on this patent, then DSP would most likely have to pay a licensing fee in order to produce the wireless system.

Shure's wireless microphone systems were also a potential for infringement; however, the receivers of the Shure's systems and DSP are significantly different and the audio signal passes through more user influence in DSP before outputting to the speakers. The potential of infringement would occur with the transmitters. However, since the transmitter's hardware can be considered "obvious", there are enough differences in the wireless scheme that no actions need to be taken with DSP's design in order to avoid infringing on Shure's wireless systems. DSP's design was also very similar to Technical-Pro's RX-B32 receiver involving the user interface to adjust the audio signal to the user's specifications before being output to speakers. However, the kind of functions that DSP uses are significantly different than the RX-B32 and the source of the wireless input is also notably different. With these differences in design, DSP does not have the potential for infringing upon the design of the RX-B32 and no action needs to be taken to change the design of DSP.

4.5 Summary

Two products and one patent were analyzed in order to determine the possibility of infringement if Digital Sound Projection were to be produced and sold. Patent 7,680,465 described a wireless system that receives an audio signal and allows the user to adjust the amplitude of different frequency bands. One company's products, the Shure wireless microphone systems, are products that perform the same function of transmitting a microphone input to a base receiver and outputting the signal to speakers. However, the Shure wireless systems do not allow the user to adjust the audio signal to the user's preferences before outputting to the speakers. The Technical-Pro RX-B32 receiver is another product that does the same function as DSP's receiver unit by accepting an audio signal and allowing the user to change some settings to their preference and outputs the adjusted signal. These products and the patent all share some similarities with the design of Digital Sound Projection, although the main similarities are considered "obvious" designs and do not risk any infringement of ideas. DSP also applies enough differences in execution of the design that the potential for infringement, both literal and under the doctrine of equivalents, does not exist and no other actions need to be taken.

5.0 Reliability and Safety Analysis

5.1 Introduction

In the case of device failure, because the transmitter board contains only one microcontroller and three other digital components, it is unlikely a safety critical event will arise. The receiver consists of a set of digital and analog boards. In the case of device failure on the analog board, one of the critical safety issues is if the two 1mF power supply filter capacitors malfunction. A critical safety issue on the receiver station can be a failure of the 5V/4A switching power supply module. A malfunction will damage all the digital components on the digital board. To prevent the user from being harmed when critical failure occurs, the receiver is packaged with an aluminum casing. Other non-critical failures such as digital components malfunctioning or analog components decaying over time will only create inconvenience without resulting physical harm to the user.

5.2 Reliability Analysis

The failure rate of Digital Sound Projection is most likely to be determined by the digital signal processor, SHARC ADSP-21262, since it has the most die complexity and current load. The SHARC DSP performs 32-bit computations on the digital audio signal and routes the input and output signals for DAC and ADC. The SHARC draws around 800mA of current under full load which is relatively high in comparison to all other components on the board. The next set of digital components expected to fail after the ADSP-21262 are the PCM4202, the PCM1792A, and the ATmega168. The PCM4202 is chosen because it continuously converts the analog input signal to an I2S output signal with 24-bit precision. This operation involves a series of logic gate switching and draws approximately 20mA from Vdd and 65mA from Vcc. The PCM1792A is chosen because it continuously converts the I2S input signal from the SHARC into differential current outputs. This operation involves an internal voltage to current converter in addition to the 24-bit digital to analog conversion and draws approximately 10mA from Vdd and 65mA from Vcc. The ATmega168 is expected to fail because it holds the input values for various audio effects that are constantly scanned by the SHARC and is responsible for generating the user interface on the LCD display module when the device is turned on.

The Military Handbook for Reliability Prediction of Electronic Equipment predict the expected amount of device failures in 10^6 hours can be calculated as $\boldsymbol{\lambda_P = (C1*\pi_T + C2*\pi_E) *\pi_Q*\pi_L}$ for microcircuits, gate/logic arrays, and digital processors where C1 is the die complexity, π_T is the temperature coefficient, C2 is the packaging failure rate, π_E is the environment factor, π_Q is the fabrication quality factor, and π_L is the manufacture learning factor.

Table 5-1: ADSP-21262 MTTF Calculation Chart

Parameter name	**Description**	**Value**	**Comments**
C1	Die complexity	0.560	32-bit MOS micro
π_T	Temperature coeff.	0.630	$T_j = T_C + (\theta_{JC} * P) = 69.90°$ C $T_c = 30$ $\theta_{JC} = 27.9$ P =1.27
C2	Package Failure Rate	0.060	$N_p = 144$ Hermetic SMT
π_E	Environment Factor	2.0	Ground Fixed
π_Q	Quality Factors	1.0	Commercial Product
π_L	Learning Factor	1.0	In production for more than 2 years
Entire Design		$\lambda_P = .484$	MTTF ≅ 235.9 years

Table 5-2: ATmega168 MTTF Calculation Chart

Parameter name	**Description**	**Value**	**Comments**
C1	Die complexity	0.140	8-bit MOS micro
π_T	Temperature coeff.	0.140	$T_j = T_C + (\theta_{JC} * P) = 32.5°$ C $T_c = 30$ $\theta_{JC} = 25$ P =.10
C2	Package Failure Rate	0.012	$N_p = 32$ Hermetic SMT
π_E	Environment Factor	2.0	Ground Fixed
π_Q	Quality Factors	1.0	Commercial Product
π_L	Learning Factor	1.0	In production for more than 2 years
Entire Design		$\lambda_P = .0374$	MTTF ≅ 4397 years

Table 5-3: PCM4202 MTTF Calculation Chart

Parameter name	Description	Value	Comments
C1	Die complexity	0.160	10001-30000 gates
π_T	Temperature coeff.	0.431	$T_j = T_C + (\theta_{JC} * P) = 60.8°$ C $T_c = 30$ $\theta_{JC} = 100$ P =.308
C2	Package Failure Rate	0.013	$N_p = 28$ Non-hermetic SMT
π_E	Environment Factor	2.0	Ground Fixed
π_Q	Quality Factors	1.0	Commercial Product
π_L	Learning Factor	1.0	In production for more than 2 years
Entire Design		$\lambda_P = .0950$	MTTF ≅ 1202 years

Table 5-4: PCM1792A MTTF Calculation Chart

Parameter name	Description	Value	Comments
C1	Die complexity	0.080	3001 – 10000 Gates
π_T	Temperature coeff.	0.293	$T_j = T_C + (\theta_{JC} * P) = 50.50°$ C $T_c = 30$ $\theta_{JC} = 100$ P =.205
C2	Package Failure Rate	0.013	$N_p = 28$ Non-hermetic SMT
π_E	Environment Factor	2.0	Ground Fixed
π_Q	Quality Factors	10	Commercial Product
π_L	Learning Factor	1.0	In production for more than 2 years
Entire Design		$\lambda_P = .0494$	MTTF ≅ 2309 years

In summary, the Digital Sound Projection has a relatively low failure rate and all of the digital components have $\lambda_P < 1$. One critical factor of the failure rate is the thermal dissipation of surface mount ICs. To further improve the MTTF rate, additional heatsinks can be attached to reduce the thermal junction coefficient. Applying extra cooling fans to reduce the ambient casing temperature is also a possible solution to extend the MTTF.

5.3 Failure Mode, Effects, and Criticality Analysis

The Digital Sound Projection consists of one transmitter unit and one receiver unit. The following two subsections will discuss each individual subsystem for both the transmitter and the receiver. In Appendix F of the report, there is a FMECA table that includes the criticality of each failure for each subsystem for both the transmitter and the receiver.

The criticality levels are stated as High, Medium, and Low. A High criticality failure is a failure that could physically harm the user. For this kind of failure, the failure rate λ_P must be below 10^{-9} failures/hour. A Medium criticality failure is a failure that can cause the Digital Sound Projection unit to malfunction. These failures are less dangerous to users but the failure rate should be lower than 10^{-6} failures/10^6 hours. A Low criticality failure is a failure that affects the Digital Sound Projection's overall performance. These failures should not stop the functionality of the Digital Sound Projection but should be limited to 10^{-5} failures/10^6 hours.

5.4 FMECA on the Transmitter Board

The transmitter board can be divided into five individual functional subsystems. These blocks include NiMH battery packs connected with linear voltage regulators, analog inputs, the PCM4202 ADC, the nRF24Z1 wireless transmitter with antenna, and the ATmega168 microcontroller with device status indicators.

5.5 FMECA on the Receiver Board

The Receiver board can be divided into six individual functional subsystems. These blocks include digital/analog power supply modules with noise filters, analog inputs and outputs, the PCM4202 ADC and the PCM1792A DAC, the nRF24Z1 wireless receiver with antenna, the ATmega168 microcontroller with LCD display module, and the SHARC DSP with JTAG interface.

5.6 Summary

Digital Sound Projection is a relatively safe and reliable product based on the failure rate calculations. In the event of critical failures, the aluminum casing would provide protection from physical harm; however, there is no failure protection in the circuitry. Therefore, if any of the digital components are damaged, the Digital Sound Projection will most likely stop functioning. In addition, heatsinks and current limiters could be implemented to improve the MTTF rate.

6.0 Ethical and Environmental Impact Analysis

6.1 Introduction

Ethical and environmental issues with respect to the transmitter include frequency sniffing, proper battery and circuit board disposal, and user warning labels. Finally, the receiver takes the digital signal from the transmitter and performs user defined equalizer effects through the use of the SHARC digital signal processor. Ethical and environmental concerns include shock hazard user warnings, harmful materials disposal, and noise pollution.

6.2 Ethical Impact Analysis

6.2.1 Transmitter Analysis

The ethical challenges facing the transmitter design include operating conditions, user warnings, and possibly adding safety mechanisms. First, the transmitter design must be tested in a suite of different operating conditions. As DSP is meant to be used in lectures, speeches, and/or concert settings, there is the possibility of outdoor use. To ensure the DSP functions as marketed, the system will be tested for both indoor and outdoor operating conditions. Testing will include the standard "shake and bake" consisting of extreme temperature change and vibration testing. Products akin to the Thermotron Accelerated Stress Test (AST) Chamber will be used for this process [1]. Also, Radio Frequency (RF) and Electromagnetic Compatibility (EMC) Testing will be completed to ensure no FCC regulations are broken and background noise, especially in the outdoor application, does not negatively affect the system. Lastly, spill testing will be performed on the transmitter to ensure working condition in the case of a rain storm in an outdoor setting.

Secondly, while nickel metal hydride (NiMH) is not technically dangerous, it is a skin irritant and can be dangerous if ingested or comes into contact with the eye [2]. As NiMH rechargeable batteries are used in the transmitter, a warning label will be located inside the package to warn the user of dangers associated with the battery packs. The warning label will be placed next to the battery connections giving the user an easily visible caution not to use the batteries in any configuration that may cause a rupture. No other warning labels are necessary for the transmitter as there are no shock hazards or high temperatures associated with the transmitter circuit board.

Lastly, there is a possible ethical issue of frequency sniffing and subsequent remote recording of the audio signals transmitted by DSP. These illegal recordings could lead to pirated live music tracks; however, this occurrence is very unlikely. The Nordic nRF24Z1 Transceiver used in the DSP design utilizes frequency hopping in the range of 2.4 to 2.45GHz [3] making it exceedingly difficult to successfully lock onto and demodulate the transmitted signal.

6.2.2 Receiver Analysis

Like the transmitter, the receiver unit will be placed through a suite of tests. The receiver circuit boards will be placed through temperature change and vibration testing [1] identical to the transmitter circuit board. The receiver will also be tested for RF, EMC, and spill tested in case the receiver station is exposed to rain.

Next, the receiver requires two warning labels to be placed on the rear face of the unit. The first label will be a generic electric shock warning to caution the user from tampering with the wall socket and power input to the receiver base. Also, a warning label cautioning against operating the receiver with the cover off will be placed on the rear face of the unit. Chance of shock hazards and potential hearing loss caused by capacitor explosions are drastically reduced with a closed package; therefore, it is important to caution the user from operating the unit with no cover.

In the user documentation, volume control warnings will be placed to caution the user from operating the system at an extremely high volume. This will help prevent hearing loss to the user or any passerby in close proximity to the speakers connected to DSP. Also, all warnings provided on the receiver unit itself will be reiterated in the user documentation.

Lastly, there are a few safety mechanisms that could be added to the receiver station. A surge protector in the form of a circuit breaker could be added to the receiver power input to protect the circuit board and capacitors. This would prevent any chance, with the exception of a short circuit, of electrical shock or capacitor explosions that could potentially harm the user if operated with an open case. With regards to the receiver packaging, the prototype will be placed in a simple aluminum sheet metal box. To decrease the chance of the unit falling off a shelf and onto the user, the package could be changed to a securable rack mount.

6.3 Environmental Impact Analysis

6.3.1 Transmitter Analysis

First, while NiMH rechargeable batteries do not pose a serious environmental problem, recycling is the best course of action. Documentation in the user manual will urge the user to properly dispose of the battery packs and point them to the United States Environmental Protection Agency (EPA) battery informational page [4] which contains resources for proper battery disposal. Also, the current circuit board design contains lead. To reduce the chance of environmental lead contamination, the circuit board must be disposed of properly upon design obsolescence or circuit board failure. The EPA provides guidelines on proper disposal and recycling locations for consumer electronics [5]. The EPA also suggests using the Earth911 website to conveniently search for recycling centers for both batteries and consumer electronics on a zip code basis [6]. Both the EPA and Earth911 websites will be cited in user documentation to ensure proper disposal of both the rechargeable NiMH batteries and transmitter circuit board.

Secondly, the manufacturing process could be improved to reduce the environmental impact of DSP. A printed circuit board (PCB) manufacturer with Restriction of the Use of Certain Hazardous Substances (RoHS) compliance [7] would be chosen to ensure no lead or other environmentally harmful materials are present in the circuit board. Advanced Circuits, the PCB manufacturer used for DSP, is one such manufacturer capable of producing a RoHS compliant circuit board [8]. Although a majority of components on the circuit board are currently RoHS compliant, RoHS compliant equivalent parts would be chosen to replace the current components containing lead. Lead-free solder will also be used to ensure a RoHS compliant design. Lastly, copper pours could be added to the transmitter circuit board design to reduce the amount of copper wasted in the etching process. This, in turn, will reduce the amount of etchant waste that must be disposed of.

6.3.2 Receiver Analysis

Like the transmitter circuit board, both receiver PCB's contain lead. Components containing lead must also be replaced by RoHS compliant parts to reduce any possible contamination to the environment. In addition to the circuit boards, a liquid crystal display (LCD) is used to display the equalizer effects user interface. LCD's are known to contain environmentally harmful

materials; however, a RoHS compliant LCD from CystalFontz was chosen for the DSP design reducing the environmental impact of the design. The user documentation will, however, still urge the user to recycle the LCD with the receiver unit. The same informational resources as mentioned for the transmitter PCB and batteries in Section 3.1 will be utilized in the user documentation.

Power consumption is also an environmental concern with the receiver unit as it uses significantly more power than the transmitter. The receiver requires several different voltage levels: ±15V, 5V, 3.3V, and 1.2V. A power supply providing 19V was chosen to achieve each required voltage level. The lower level voltages are supplied through linear regulators for the ±15V and a power module supplying 5V to the remaining linear regulators. While there is inherent wasted power, the power module, whom draws the most current, is 83% efficient.

Lastly, there is the environmental problem of noise pollution. In the outdoor setting, noise pollution may be a viable issue if DSP is used to play music or lectures at extremely high volume levels. Again, this could not only damage the user's hearing, but also passerby's hearing in the process. This could also lead to public nuisance reports requiring police intervention. Documentation will be added to ensure the user is aware of this environmental issue and warns against playing audio signals at extreme levels. The extreme solution would be to digitally limit the volume levels output by the receiver unit; however, the signal output by DSP could then be amplified by the user making this solution ineffective. The best course of action is to document the potential for noise pollution to ensure the user is aware of this issue.

6.4 Summary

All in all, the DSP design has possible ethical and environmental issues. Ethical issues associated with the design including frequency sniffing, safety issues, and design functionality will be addressed through frequency hopping, user warnings and cautions, and a suite of testing, respectively. Noise pollution and proper battery and electronics disposal are potential environmental issues of the design; however, user documentation warning against operating at high volume levels and providing information resources for environmentally friendly disposal will reduce the environmental impact of the design.

7.0 Packaging Design Considerations

7.1 Introduction

The transmitter packaging constraints include size, ergonomic shape, and interfacing capabilities. The package must be small and light enough to clip onto the user's belt or fit in a pocket. The transmitter must be ergonomically designed as not to create discomfort for the user. Openings in the package will be required for a microphone connector, user interface (UI), and antenna.

At the receiving end, interfacing capabilities, UI considerations, and electromagnetic interference (EMI) shielding are all potential packaging issues. The receiver base must have openings for an antenna, external power source, audio output, and analog input connectors. Package openings will also be required for the UI's LCD, rotary encoder, and push buttons to display and change EQ levels and other pertinent information. EMI shielding is also a packaging constraint as to minimize exterior noise influx and radiation within the circuit.

7.2 Commercial Product Packaging

Although there were no package designs exactly like DSP's, several professional wireless audio systems exist with similar packages. This analysis will focus on two professional wireless audio systems, the Shure ULX Wireless System [1] and the Sennheiser freePORT Presentation Set [2], and how they are both similar and different to DSP's packaging scheme.

7.2.1 Shure ULX Wireless System

Figure 7-1: Shure ULX Wireless System Packaging [1]

The Shure ULX Wireless System comes in a package consisting of two separate devices. A transmitter, either the ULX1 Body-Pack Transmitter or ULX2 Hand-Held Microphone Transmitter, complimented by the ULXS4 Standard Diversity Receiver comprises the system packaging. Please note the transmitter packaging analysis will focus on the ULX1 as it closely fits the design for the DSP transmitter.

First, the transmitter package of the ULX1 is compromised of a plastic injection mold with seamless openings for antenna, audio input connector, and user interface components. A metal clip is provided on the reverse side for placement on a user's belt [1]. The package is compact and ergonomically shaped for comfort when worn by the user. All connectors and LED indicators are conveniently located on top of the unit [1]. A display and push buttons located on the ULX1's face enable the user to easily switch frequency bands [1]. Overall, the packaging design is excellent providing both user comfort and easy access to all functions. The packaging design of the DSP transmitter will be similar to that of the ULX1. The package will be small, light weight, include a metal clip, and provide easy access to connectors and buttons. Unlike the ULX1, however, the DSP package requires no considerations for a UI display.

Next, the receiving ULXS4 station package consists of a sheet metal box providing space for the UI and antennas. The package is compact and provides the user with an ability to turn the power on or off, adjust the frequency band, and volume level [1]. Connector jacks and antennas are conveniently located in the rear of the unit [1]. Like the ULXS4, the receiver's LCD UI will be placed on the front of the unit; however, as DSP's UI is more robust, more real estate is required necessitating a larger package. Also, similar to the ULXS4, the DSP receiver's connector jacks and antennas will be located at the rear face as to avoid physically interfering with the UI.

7.2.2 Sennheiser freePORT Presentation Set

Figure 7-2: Sennheiser freePORT Presentation Set Packaging [2]

The Sennheiser freePORT Presentation Set has a similar packaging scheme to that of DSP's. The package includes a compact transmitter unit and a sleek receiver box. First, the transmitter box is small, light weight at three ounces without batteries [2], and has a simple power button. Located on the front face is a power button and simple sliding plastic piece to protect the battery bay [2]. The top face includes the antenna and microphone input connector [2]. The Sennheiser transmitter package is a very close fit to DSP's. The design fits the size and ergonomic constraints of the DSP packaging. The only planned difference for the DSP design will be the volume control interface.

Secondly, the Sennheiser receiver package is a sleek, metal enclosure. The front face includes two antennas, LED's indicating system status, and a dial to switch frequency bands. Power and audio connectors are located in the rear of the unit [2]. The antenna located in the front of the unit do not pose any issues for the Sennheiser design [2]; however, in DSP's case, the antenna must be located in the rear of the unit as the antenna would physically impede the user from interacting with the LCD and push button interface located on top of the unit.

7.3 Project Packaging Specifications

The packaging will consist of a separate transmitter and receiver base. The transmitter package will be small, light weight, and ergonomically shaped as the user will wear the transmitter on his/her belt. A RadioShack ABS, plastic injection molded, 6 x 4 x 2 inch project enclosure will be used to encase the design [3]. To minimize packaging envelope size, the antenna will be located on the left side of the transmitter. Power and wireless data link LED indicators, microphone input connector, and power switch will be placed on top of the unit for

easy viewing and access, respectively. Volume control push buttons and gain flag switch will be located on the front face to allow the user to adjust volume or adjust the gain of the transmitter while wearing the device.

Next, the receiver base must be large enough to accommodate the LCD, rotary encoder, and push button user interface, and satisfy the EMI shielding constraint. The package will be the Bud Industries 12 x 10 x 3" aluminum sheet metal enclosure [4]. For easy accessibility, the user interface will be located on the front of the unit. The power input, audio input, and antenna will all be located in the rear of the unit as not to impede access to the UI. Four rubber pads will be added to the bottom of the unit to decrease the chance of the unit slipping off of a surface. Also, the aluminum case will effectively shield the circuit from electromagnetic interference. Copper tape will be used to fill gaps at connecting interfaces to completely EMI shield the system if necessary. Refer to Appendix B for detailed CAD drawings of packaging design and Appendix B for materials, tooling, weight, and unit cost details.

7.4 PCB Footprint Layout

For the components selected in the Design Constraints Analysis, most had either only one or a few footprints available. For the components with multiple footprints, two major characteristics were considered, overall footprint area and lead or pad solderability. Using these criteria, it was determined that PDIP packages were to be avoided as the through-hole leads effectively double the footprint of the chip. Next, extremely small packages such as QFN were avoided as soldering these components is difficult with the exception of the nRF24Z1 transceiver chip as QFN was the only available package. SOIC and TQFP were the packages of choice as they provide small footprints and reasonable solderability.

Next, the PCB dimension estimates will be 5 x 3", 7.446 x 3.833", and 6.499 x 4.555" for the transmitter board, receiver analog board, and receiver digital board respectively. For the transmitter, all active components fit on one side of the board leaving space for passive components and UI push button connectors. For the receiver, all active components easily fit onto the analog and digital circuit boards. This layout effectively isolates the analog and digital circuitry and allows for easy routing.

7.5 Summary

Overall, the packaging design will be very similar to that of the Shure and Sennheiser commercial systems. The ABS transmitter package will be small at 3 x 2 x 1 inch, lightweight, and user friendly. The aluminum receiver package will be large enough to accommodate the UI at 7.4 x 4.75 x 3.2 inches, provide EMI shielding, and provide easy access to the UI on the top face. The transmitter and receiver PCB layouts at 2.8 x 1.8 inches and 7.0 x 4.2 inches, respectively, are large enough for all active components and will fit within the chosen package designs.

8.0 Schematic Design Considerations

8.1 Introduction

Digital Sound Projection consists of a transmitter and a receiver base station for transmitting digital audio through the air. Since the transmitter is battery based, there will be a tradeoff between SNR and power consumption. The receiver station was designed to either receive the digital audio wirelessly or to accept analog input from the analog to digital converter. The base station will then perform an N point Fast Fourier Transformation (FFT) to get a rough estimation of the frequency domain. By adjusting the frequency bands, users will be able to apply EQ effects by interacting with a user interface. After all the computations are done, the digital signal processor will then send the reconstructed digital audio signal to the digital to analog converter. On the PCB, left and right channels are laid out separately to reduce the effect of inter-channel contamination. The digital circuitry is also separated from analog components to reduce electromagnetic interference effects.

8.2 Theory of Operation

The transmitter contains three major subsections which include the microphone input, unit control, and wireless transmitter. The microphone input section uses a pair of Texas Instruments PGA2505s, one for each channel. The PGA2505 has a serial control interface, gain up to one thousand, and accepts small differential signal inputs. The PGA2505 output is set to a voltage swing of 0 to 5V on V_{out+} and V_{out-} with a common reference voltage (V_{com}) equal to 2.5V. The PGA2505 common voltage reference is set to match the PCM4202 ADC reference voltage (V_{ref}). To further process the input, the signal is passed to the PCM4202 that quantizes the analog input into I2S output with 48kHz/24bit bit rate.

The Nordic Semiconductor nRF24Z1 wireless transceiver receives I2S input from the PCM4202 and performs bit truncation to compress the input down to 16-bit. The nRF24Z1 also provides channel coding to guarantee quality of service between transmitter and receiver; it generates protection codes and a CRC checksum to correctly receive data. To modulate the digital audio for transmission, the nRF24Z1 passes data to a Gaussian filter and then multiplies its output with 38 different carrier frequencies between 2.4GHz to 2.45GHz simultaneously to select an optimal transmission frequency. In order to transmit at 2.4GHz, a high frequency

capacitor is used between antenna ground and digital ground to prevent interference. A 12.288MHz is used to drive the I2S clocks between the nRF24Z1, PCM1792a DAC and PCM4202 ADC.

An ATmega168 microcontroller handles the control of the user interface on the transmitter and receiver. The clock speed of 4MHz for is sufficient to operate the user interface and control the nRF24Z1. The microcontroller debounces external pushbutton inputs and decodes the quadrate encoder signals.

On the transmitter, the analog output is driven between +5V and -5V and the digital components operate at 3.3V. All of the above voltages are generated from two 6V battery packs and regulated separately by low drop-off linear voltage regulators.

On the receiver, inputs can come from either the wireless input or analog line-in from the RCA stereo jack. The nRF24Z1 receives digital audio from an antenna and the chip then utilizes a Phase Lock Loop (PLL) with self-clock regeneration to decode Gaussian Phase Shift Keying (GPSK) back to I2S with additional checksum and error corrections. From the RCA analog line-in port, the analog audio is first converted into differential pair with 2.5V DC offset by OPA1632 then is sent to PCM4202 to quantize the $0V<Vin<5V$ analog signal to an I2S digital audio signal. Since mic-in is not implemented, a PGA2505 is not necessary on receiver side.

The I2S signal from either the wireless or line-in input is then sent to Analog Devices' SHARC ADSP-21262 for EQ and digital mute processing. The SHARC takes the I2S input and saves the sample points into two separate N (N = 1024 or 2048) real number floating point buffers with a fill time of 20ms or 40ms, respectively, for the left and right channels. Since the user will be able to adjust the input signal's behavior in the frequency domain, a Short Time Fourier Transformation (STFT) is needed to convert time domain into frequency domain. An optimized FFT function provided by the Virtual DSP library from Analog Device is used. In order to FFT each individual channel, one complex N point and one real N point buffer is allocated; N twiddle coefficients (complex points) are generated and saved into memory. After the FFT calculation and frequency convolutions (EQ effects and other frequency based operations), an inverse FFT (IFFT) of length N is used to convert the frequency domain back to time domain in order to reconstruct the digitized signal. The entire computation should not exceed the time required to build N samples input buffers based on the 200MHz clock frequency of the SHARC, which is insignificant compared to the 20ms to 40ms required sampling time.

The PCM1792A reconstructs the processed digital audio sent from the SHARC to analog current driven differential outputs, Iout+ and Iout-. A set of bi-amp I/V current integrators are implemented to convert Iout to Vout with Vavg of 2V and Vpp of 4V. To generate RCA output, another bi-amp configuration is used to combine differential output into singled RCA output.

The receiver uses a 19V, 3.15A wall wart with one +19V to +5V power module for the digital board power and +15V to -15V power module for the analog board negative supply reel. The +15V and -15V on the analog board are first filtered with two LC filters in series (Fc_1 = 400Hz and Fc_2 = 2000Hz then filtered again by bypass and decouple capacitors to ensure the clearness of the power supply for OPA1611 op-amps, +5V for Vcc on PCM1792 and PCM4202, and +3.3 for Vdd on our digital devices. The SHARC requires 1.2V supply for its internal core voltage which will be generated from a +3.3V to +1.2Vlinear voltage regulator to prevent overheating.

8.3 Hardware Design Narrative

On the transmitter, three pins on ATmega168 microcontroller will be utilized for SPI: serial clock, master out slave in, and slave devices master in slave out. Two additional pins are used to select between the PGA2505 and nRF24Z1. To give user control of output volume on the receiver from the transmitter, two pins are used for reading from push buttons. Also there will be two additional pins on the ATmega168 to read the user input regarding analog input gain selection. On ATmega168, all the unused pins are tied to ground through resistors to avoid EMI effects.

The PGA2505 communicates with the ATmega168 using SPI to adjust gain between 0dB to 60dB. In order to generate 0-5V differential output for the PCM4202, the PGA2505 reads Vref from PCM4202, uses it as an output common ground (Vcom), and generates voltage outputs accordingly.

The PCM4202 is set to PCM mode with 12.288MHz clock signal from the nRF24Z1. After the PCM4202 digitizes the analog input, it then sends the digital audio to the nRF24Z1. I2S with word length of 24bits is selected for this operation; it uses three pins for I2S data, I2S bit clock, and I2S frame-sync. On the PCM4202, all the unused modes, including DSD and multi-bit modulator mode, are disabled.

The nRF24Z1 is configured by the ATmega168 with one mode select (either Tx or Rx) pin, two volume control inputs de-bounced by the ATmega168, and the SPI bus. The nRF24Z1 reads I2S input from the PCM4202 and adds additional volume reading to the end of the audio bit stream. This signal is then transmitted via a 2.4GHz channel. On the nRF24Z1, the "antenna 2" output is tied to ground and all other unused pins are tied to ground to prevent EMI effects.

On the receiver, the PCM4202 is set to have the same data output format as the one on the transmitter. Chip select pins are set to source digital audio between the nRF24Z1 and the PCM4202. All the unused I/O are tied to ground and all the unused functions are disabled for both the nRF24Z1 and the PCM4202.

The SHARC Digital Signal Processor receives an I2S signal from either the PCM4202 or the nRF24Z1 and buffers the input data stream in internal RAM to perform digital signal processing on the digital audio. Since the SHARC has the most of GPIO pins and fastest clock speed, it is used as the master SPI device to select between different SPI controlled subsystems and sends out a reset flag to each subsystem every time the receiver restarts. Also, the SHARC requires an additional SPI based flash chip to store its boot-image.

An ATmega168 microcontroller is also used to show user device status, to read user inputs, and to drive the LCD display. The microcontroller is driven by the SHARC over SPI buses and reads user input from push buttons and rotary knobs. Analog rotary encoders and push buttons will take eight pins on the microcontrollers. The LCD display module is driven by the ATmega168 with two serial port pins, two LCD read/write pins, and one LCD chip select pin.

8.4 Summary

The transceiver is designed with low power consumption. A minimum amount of chips are used to reduce power consumption and pin connections. The transmitter uses the ATmega168 as a central processing unit to control the PGA2505, PCM4202, and nRF24Z1. The PGA2505 is connected to a single input to differential output converter and generates high gain voltage output. The PCM4202 reads the voltage s from both the positive and negative of the differential input and output I2S digital audio to the nRF24Z1. The nRF24Z1 accepts the I2S signal and performs input compression and channel coding before sending the modulated signal via a 2.4GHz wireless channel.

On the receiver, the nRF24Z1 receives an input signal from an external antenna and decodes the modulated input to an I2S digital audio. An additional PCM4202 is used on the receiver to read analog line-in input. The SHARC DSP has a chip select function to select the input source between the nRF24Z1 and PCM4202. The SHARC performs frequency analysis and applies frequency convolution to the digital audio signal. After frequency operations, the SHARC then sends the processed digital audio signal to the PCM1792. The PCM1792 takes the I2S data and converts it back to current driven differential outputs. The ATmega168 is used on the receiver to show device status, to read user inputs, and to drive the LCD display. The ATmega168 reads user inputs from a rotary encoder and push buttons. All the subsystems on the receiver side, with the exception of the PCM4202, are controlled by the SHARC using SPI buses. The entire system is powered by a 19V DC input and is sent to one +19V to +5V power module and one +19V to -15V power module with linear voltage regulators to acquire desired voltage outputs.

9.0 PCB Layout Design Considerations

9.1 Introduction

As a design consideration, the transmitter circuit board will have to be small in order to retain the portability of a handheld device; however, there are specific limitations with some of the chip layouts that will require additional space on the board. However, there are limitations on how small the circuit boards can be due to noise considerations, placement of chips for convenient traces, and also based on the manufacturers' data sheets for each chip.

9.2 PCB Layout Design Considerations – Overall

The project requires two separate printed circuit board designs: one transmitter and one receiver. The transmitter and receiver boards both have very similar requirements; however, the transmitter has the additional requirement of small size. As a benefit, the transmitter requires fewer physical chips and external connections, which will allow for less circuitry.

The nRF24Z1 transceiver is a major imitation on the size of the circuit boards, specifically the transmitter. This chip requires that the nRF24Z1 be placed alone on the board with no components or traces running underneath. The transceiver must also be placed close to the edge of the board where the SMA antenna connector is located so that traces are short. This is done to avoid the EMI radiation of the received wireless signal from the antenna, because if the trace is longer than a specific value depending on the frequency, then the electromagnetic fields could radiate off the trace as if it was an antenna itself. Keeping the antenna connection close to the nRF24Z1 chip will also help retain the characteristics of the 50 ohm matched output circuit without having to meet additional requirements concerning the physical trace as outlined in the layout application note. If there is a reason for the nRF24Z1 impedance matching network to require more board space, then the design must use a 50-ohm micro strip line to carry the signal [1]. In order to place the nRF24Z1 at the side of the board near the edge, the chip should be situated such that the I/O pins face the interior of the board in order to eliminate inefficient trace design.

A major concern for the layout is the risk of noise contamination between the chips themselves. This specifically is a consideration of the noise contribution that the analog devices on the circuit boards would have with the digital components. The first part of the solution for

this problem is simple by creating two separate boards for the receiver: one board for the analog components and one board for the digital components. This will also help separate the analog and digital grounds, which will reduce noise between the two different types of components. A header will then be needed to connect the two boards with the important signal and power/ground traces that are common between the two boards. With two separate boards, it is preferred that the sizes are kept to a minimum in order to fit the receiver into the chosen receiver package. To minimize the size some planning is needed to draw out, by hand, the orientation and placement of the chips to most efficiently use the board space. The transmitter design will only be placed on one board and due to size constraints the only solution is to separate the analog and digital chips on opposite sides of the board. There will not be much space in between the chips, but this could possibly help reduce noise contamination between the components.

Each printed circuit board for the receiver will be a four layer board and the transmitter will be a two layer board. This will require strategic routing and placement of the off-chip circuitry. In order to use as much board space as possible while maintaining minimum size, careful planning will be needed to place traces, passive, and active components on both sides of the board. To prevent further noise contamination, no traces or noisy components should be placed underneath the chips themselves. The multiple layers will also allow for bypass and decoupling capacitors to be placed right next to the pins on one side of the board without interfering with any of the traces between chips. The Op-Amps (OPA1632, DRV134, PGA2505) will require as short of a trace as possible in order to prevent small signal oscillation while operating at the expected values, which can be done by taking advantage of the two layers. The maximum current draw for any of the chips' signal pins does not exceed 100mA, which means the width of the signal traces can be at the minimum 10-12 mil width. This will help in routing because there will be less space on the PCB used to route these thin traces.

One other consideration for the layout of the project's circuit boards will be the off board peripherals. The antennas, microphone input, RCA input, and RCA output will all be connected using surface mount or through-hole connectors on the boards. These connectors will have to be placed on the edge of the board but also close to the respective chips for which they are inputs or outputs. The boards will also require several headers for programming chips like the ATmega168 microcontroller and the ADSP-21262 DSP. These headers will also give an opportunity to make use of extra unused pins of chips to provide alternatives in case of pins

burning out. Space will need to be allocated for these headers, which will increase the size of the board, specifically for the SHARC's 26 pin DAI header and 16 pin JTAG header, and also require additional planning for the placement with respect to the chips that they are connected to so that there is no risk of crossing traces. The user interface including the LCD, pushbuttons, batteries, and LEDs will also require some header connections since these devices will not be connected to the PCBs directly but will be placed on the project casing. The other decision with the headers is whether to use surface mount or through-hole. Any through-hole mounting will essentially eliminate possible trace routing on both sides of the board where these headers are located while surface mount would only take up space on one side of the board. If any through-hole components are used, then these should be placed such that they would not interfere with any traces on either side of the board.

9.3 PCB Layout Design Considerations – Microcontroller

The circuit board layouts for the ATmega168 Microcontroller and the SHARC ADSP-21262 DSP are similar to the rest of the chips on the boards. Bypass and decoupling capacitors need to be placed as close to the pins as possible to reduce noise on the supply pin. The same aspect applies with the oscillator circuit that must be placed close to the pins of the nRF24Z1 transceiver, ATmega168 microcontroller, and SHARC ADSP-21262. With several components that need to be placed next to these chips, then both sides of the board will need to be taken advantage of. This is important for the SHARC due to its large number of power and ground pins. These power traces will need to be larger than the signal traces (around 60-100 mils in width), but will need to gradually decrease in width to match the width of the pins so they do not interfere with the rest of the connections to the chip. This reduces the amount of resistance for the large current ratings from the power supplies and prevents burning out traces. In addition, both the SHARC and the ATmega168 will require large headers and extra space on the board in order to program the chips and to access unused pins as a back up to any burned pins.

9.4 PCB Layout Design Considerations - Power Supply

The placement of the voltage regulators for each circuit board is a major concern for the design because of the noise that these devices produce. A solution to this problem is to place the

regulators on a side of the board that is as far from the other chips. These regulators also generate lots of heat (around 5W of power dissipation for the 15V to 10V 1A regulator) and this will require connecting the thermal pads to heat sinks to handle the amount of heat generated while not taking up too much room on the PCB. However, these heat sinks will take up additional space that can be take advantage of with placement and orientation. Placing these regulators on a separate side of the board also causes the power traces to be longer and might cause problems when routing due to interference with other traces and could block possible signal traces.

In order to effectively reduce the input ripple voltage, the input ceramic capacitors must be as close to the input pins as possible [3]. In order to preserve the value of any inductors and to not degrade their characteristics, inductors must not be placed over ground planes. When designing the PCB, copper pours must be omitted in the areas including and immediately around any inductors.

Both the transmitter and receiver PCBs will be separated into analog and digital components on either side of the boards. This will allow for the analog and digital grounds to be separated easily without having to create complicated copper pour designs. Then the ground planes can simply be connected by a zero ohm resistor and creating a solder bridge between the two connections to give a common ground for the analog and digital grounds. Each voltage regulator for the boards will also need a capacitor connected to the common ground to help eliminate noise in the system.

The transmitter's power supply will consist of a pack of batteries which will be connected to the board through a header. This will require some additional space, but it will allow the connection to be placed any place on the board to be most efficient for routing the supply to the rest of the components. The power supply for the receiver will be a DC wall wart that will be converted into the appropriate voltages needed using several regulators. The output of the regulators and the battery pack should be situated so that star routing can be used. Each chip or pairs of chips will have their own power supply trace that begin as close to the regulators as possible. This should eliminate noise between the input supplies of the chips. These traces should be large in width (around 60-100 mils) when leaving the supplies to compensate for the large amounts of current. When each trace is approaching the power pin of a chip, the width should gradually decrease so that it is the appropriate size when reaching the chip. The gradual

decrease will depend on the distance and number of traces next to these power traces. The goal is to keep the sizes of the PCBs as small as possible. This will help reduce the traces' resistance to the large amounts of current and the chance of burning out a trace.

9.5 Summary

Digital Sound Projection's transmitter is designed to be a wireless handheld device. This emphasizes the fact that the main consideration is the printed circuit board must be as small as possible. Although, the quality of the transmitted signal being must also be preserved, which limits just how small the board can be due to trace placement and manufacturer requirements. The receiver PCB, however, does not need to meet the same requirements as the transmitter. The main concern when designing the PCB will be maintaining the signal quality throughout the system. This requires following the manufacturers requirements and avoiding any noise between chips and the traces connecting the pins.

10.0 Software Design Considerations

10.1 Introduction

This section will address the major software design considerations such as memory organization, peripheral initialization and settings and device driver requirements. A complete overview of major software components and their current development status will also be provided. A complete listing of all source code developed for Digital Sound Projection can be found on our team website.

10.2 Software Design Considerations

This section describes the software design considerations specific to the ATmega168 microcontroller and ADSP-21262 SHARC floating-point DSP. Constraints differ greatly between the real-time signal processing performed by the SHARC and user interface control provided by the ATmega168. A detailed overview of memory organization for each processor is presented. Considerations for the utilization of on-chip peripherals with an emphasis on software implementation will also be discussed. A depiction of each main software loop is provided in Appendix G.

10.2.1 ADSP-21262 SHARC

Audio processing is computational and memory intensive but also bound by real-time constraints of live playback. Excessive time spent processing audio samples or waiting for processor resources will add unacceptable delay or skipping to the output. These constraints require careful software implementation particularly for the SPI and serial port (SPORT) device drivers. Considerations must also be made when handling clock signal generation to drive off-chip ADC and DAC devices and deriving the I2S bit and word clock signals.

The SPI bus is used to control off-chip peripherals and communicate with the ATmega168 user interface microcontroller. SPI drivers are implemented using very simple device drivers which poll the SPI status register (SPISTAT) for an SPI finished (SPIF) flag. [1] An SPI clock of 1MHz is derived from the core clock by specifying the SPI baud rate divisor register (SPIBAUD). 1MHz was chosen to maintain a reasonably fast bit rate while not exceeding the maximum possible SPI clock speed of the slowest SPI slave, the ATmega168. The SHARC

automatically handles the clock and data signals once a transfer is started. SPI transfers are initiated by writing data to the transmit data buffer register (TXSPI). Slave select signals may also be controlled using the SPI flag control register (SPIFLG) to automatically select a particular slave device when a transfer starts. [1] Automatic slave select lacks the necessary timing control needed to interface with several peripherals. Manual control of these signals will be performed using the signal routing unit to route digital HIGH and LOW to an external processor pin. Specific SPI timing requirements are listed in Appendix C.

Table 10-1: ADSP-21262 SPI Peripheral Registers [1]

Register	Memory Address	Description
SPICTL	0x00001000	Enables and configures the SPI peripheral.
SPIBAUD	0x00001005	Clock divisor to generate the SPI clock $f_{SPI} = f_{core}/(2*SPIBAUD)$
SPIFLG	0x00001001	Enables SPI slave select signals on the FLAG pins
SPISTAT	0x00001002	Contains the status of the last SPI transfer. Can be polled to detect when an SPI cycle is complete.
TXSPI	0x00001003	32-bit transmit data buffer register
RXSPI	0x00001004	32-bit receive data buffer register

Digital audio is transferred between the SHARC and external audio peripherals using the I2S interface via the SPORT peripheral. I2S is a serial data bus used to transfer multi-channel digital audio between devices. Each I2S bus has a frame/word sync clock, bit clock, and data signal. A typical I2S interface can act as either master or slave mode, where master I2S mode specifies that the device is responsible for driving the bit and frame sync clock. [1] The SHARC acts as the I2S master of the PCM4202 ADC and PCM1792a DAC. A separate 12.288MHz clock is used to derive the 3.072MHz bit clock and 48kHz frame sync clock using the precision clock generator (PCG) peripheral. The source of the 12.288MHz clock depends on the user selected audio source, either the nRF24Z1 wireless transceiver or an external 12.288MHz clock oscillator is used. Both clock sources are input into the SHARC via external processor pins and routed to internal peripherals using the signal routing unit. Two separate clock sources are necessary because the nRF24Z1 must generate its own 12.288MHz clock when receiving wireless audio. This clock is recovered directly from the wireless audio transmitter to ensure the transmitter and receiver clocks are synchronized. [4] Additional requirements that must be met are the differences in I2S word length of the nRF24Z1 and the PCM4202. The nRF24Z1 supports an I2S word length of 24-bits [7] on the audio transmitter but on the receiver I2S output is fixed at 16-

bits. [4] Both the PCM4202 and the PCM1792a I2S word length is fixed at 24-bits. [2, 7] It is important to correctly set the I2S word length during SPORT initialization to prevent invalid bits from begin shifted into the data receive register (RXSPxA and RXSPxB).

Table 10-2: ADSP-21262 Serial Port (SPORT0-2) Registers [1]

Register	Memory Address	Description
SPCTLx	0x00000C00 0x00000C01 0x00000400	Serial port x control register enables and configures the SPORT
TXSPxA	0x00000C60 0x00000C64 0x00000460	Serial port x transmit data buffer A, 32-bit
TXSPxB	0x00000C62 0x00000C66 0x00000462	Serial port x transmit data buffer B, 32-bit
RXSPxA	0x00000C61 0x00000C63 0x00000461	Serial port x receive data buffer A, 32-bit
RXSPxB	0x00000C63 0x00000C67 0x00000463	Serial port x receive data buffer B, 32-bit

The PCG accepts an input clock signal and generates two clock output signals, typically used as bit and frame sync clocks, by specifying CLKDIV in PCG_CTLA1 and FSDIV divisors in PCG_CTLA0 registers. A subtle but important setting is the phase of the frame sync output clock signal specified by the FSPHASEA_HI in PCG_CTLA0 and FSPHASEA_LO in PCG_CTLA1. [1] The I2S protocol requires the frame sync clock signal transition after one bit clock cycle of the current frame. All PCG input and output clock signals can be routed to external processor pins or other on-chip peripherals using the signal routing unit. A visual depiction of proper I2S clock and data format is provided in Appendix C.

Table 10-3: ADSP-21262 Precision Clock Generator Registers [1]

Register	Memory Address	Description
PCG_CTLAx	0x000024C0 0x000024C1	Precision clock generator A control register x
PCG_CTLBx	0x000024C2 0x000024C3	Precision clock generator B control register x

The SHARC has two, on-chip, dual-ported, single-cycle, memory blocks that are addressable in long (64-bit), normal (32-bit) and short (16-bit) word formats and instructions are stored in 48-

bit words. All of the four word sizes are stored in the same physical memory block. The SHARC uses a simple virtual addressing scheme to separate these spaces. Each block contains 1Mbit of SRAM and 2Mbit of mask-programmable ROM, on-chip ROM is factory programmable and cannot be used. RAM on the SHARC is effectively divided into two types: program and data. Program memory is typically reserved for executable code, but space may be allocated for additional data storage. Data memory is used to store global variables, and to provide stack and heap space. Access to on-chip memory is provided via three memory bus elements: PM, DM and IO. Each bus is capable of accessing memory concurrently in a single cycle to reduce memory latency but requires explicit organization of program code and data. The SHARC implements a flat memory model with internal CPU registers occupying the lowest address space, internal RAM and ROM occupying the middle address space, and external memory occupying the highest address space. [1] Memory space is further organized into logical segments to assist in organization. By default all global variable, stack, and heap space is placed into the data memory segment seg_dmda. The entire 1Mbit of SRAM of memory block 1 is reserved for this segment. Additional space will be used to store intermediate frequency domain data in the program data memory segment seg_pmda.

Table 10-4: ADSP-21262 Long, Normal, Short and Instruction Word Memory Addresses [1]

Long Word (64-bit)	Normal Word (32-bit)	Short Word (16-bit)	Instruction (48-bit)
	IOP Registers 0x00000000 – 0x0003FFFF		
Block 0 SRAM 0x00040000 - 0x00043FFF	Block 0 SRAM 0x00080000 - 0x00087FFF	Block 0 SRAM 0x00100000 - 0x0010FFFF	Block 0 SRAM 0x00080000 - 0x00085555
Block 0 ROM 0x00058000 - 0x0005FFFF	Block 0 ROM 0x000B0000 - 0x000BFFFF	Block 0 ROM 0x00160000 - 0x0017FFFF	Block 0 ROM 0x000A0000 - 0x000AAAAA
Block 1 SRAM 0x00060000 - 0x00063FFF	Block 1 SRAM 0x000C0000 - 0x000C7FFF	Block 1 SRAM 0x00180000 - 0x0018FFFF	Block 1 SRAM 0x000C0000 - 0x000C5555
Block 1 ROM 0x00078000 - 0x0007FFFF	Block 1 ROM 0x000F0000 - 0x000FFFFF	Block 1 ROM 0x001E0000 - 0x001FFFFF	Block 1 ROM 0x000E0000 - 0x000EAAAA

Table 10-5: ADSP-21262 Memory Segments

Segment	Start Address	End Address	Description
seg_rth	0x00080000	0x000800FF	Program memory. Contains interrupt vector table and reset vector.
seg_int_code/seg_pmco	0x00080100	0x00080E17	Program memory. Contains main program code.
seg_int_code/seg_int_code	0x00080100	0x00080E17	Program memory. Contains library initialization code.
seg_pmda	0x00081525	0x00087FFF	Data memory. Contains additional space for variable data.
seg_dmda	0x000C0000	0x000C7FFF	Data memory. Contains variable data, heap and stack space.

Lastly, all signals must be correctly routed from external digital audio interface (DAI) pins to internal on chip-peripherals. The signal routing unit (SRU) is responsible for connecting internal peripheral signals with external processor pins. Signal routing remains relatively static while the SHARC is operating, with the exception of clock source signals. Depending on the audio source, the 12.288MHz clock must be routed to the PCG from either the nRF24Z1 clock output or the external 12.288MHz oscillator. With the exception of slave select signals that are routed to digital HIGH and LOW, all routing must be performed before audio data can be processed. Also any output signals must have their pin buffers enabled to drive an internal signal out of a DAI pin.

Table 10-6: DAI Pin Mapping

DAI Pin #	Signal Name	Notes
1	MCLK_NRF	12.288MHz master clock output from nRF24Z1.
2	NRF_DATA	I2S data from nRF24Z1, driven by nRF24Z1
3	NRF_LRCLK	I2S LR clock from nRF24Z1, driven by nRF24Z1
4	NRF_BCLK	I2S bit clock from nRF24Z1, driven by nRF24Z1
5	NRF_SS	SPI slave select for the nRF24Z1
6	ADC_LRCLK	I2S LR clock to the PCM4202, driven by the SHARC
7	ADC_BCLK	I2S bit clock to the PCM4202, driven by the SHARC
8	ADC_DATA	I2S data from the PCM4202, driven by the PCM4202
9	MCLK_DSP	12.288MHz master clock output from the SHARC. Connected to PCM4202 and PCM1792a.
10	DAC_BCLK	I2S bit clock to the PCM1792a, driven by the SHARC
11	DAC_DATA	I2S data to the PCM1792a, driven by the SHARC
12	DAC_LRCLK	I2S LR clock to the PCM1792a, driven by the SHARC
13	DAC_SS	SPI slave select for the PCM1792a
14	ATMEGA_SS	SPI slave select for the ATmega168
15	AUDIO_OSC	12.288MHz master clock input to the SHARC.

10.2.2 ATmega168

The processes controlled by the microcontroller differ greatly from the audio processing tasks of the SHARC. To separate the concerns of interacting with users from real-time signal processing the ATmega168 was chosen. An ATmega168 on the transmitter handles the basic user interfacing and controls the PGA2505 audio input preamp and nRF24Z1 wireless transceiver peripherals via an SPI interface. The receiver includes an ATmega168 to handle user interface control and LCD.

The ATmega168 includes one SPI peripheral that can operate in both slave and master modes. [5] On the transmitter, the SPI bus is used configure and initialize off-chip peripherals using a polling device driver. Because the user interface software requirements are non-real time, polling provides a very simple but effective means of driving the SPI bus. The transmitter SPI peripheral is initialized in master mode with a clock rate of 1MHz by setting the SPI control register (SPCR) with the proper value. A transfer is initiated by writing the SPI data register (SPDR). Then the program will wait for completion by polling the SPI flag bit (SPIF) in the SPI status register (SPSR). [6] The receiver SPI operates in slave mode and relies on an interrupt driven state machine to handle communication with the SHARC. An interrupt driven approach was taken to prevent unnecessary blocking of the main program while a transfer is in progress or not initiated. Because the receiver ATmega168 operates its SPI peripheral in slave mode a polling based method would consume an unacceptable amount of processor cycles while waiting for a transmission to occur. Configuration of the SPI peripheral is very similar to that of the transmitter, except, the MSTR bit in the SPCR register will be cleared to select slave mode operation. In slave mode the SPI slave select (SS) input pin is used to indicate the slave may drive its SPI slave out signal. [6] This pin also provides an additional synchronization capability to ensure the SPI driver never remains in an invalid state for more than a single SPI cycle. An external pin-change interrupt is used perform this reset immediately before an SPI transfer commences. Data transferred between the SHARC and the ATmega168 is mostly configuration and user settings to display on the LCD or apply to audio samples during processing. To ensure the settings are associated with the correct values a simple addressing scheme is used where each value is given a specific address that can be read from or written to.

Table 10-7: ATmega168 SPI Peripheral Registers [6]

Register	Memory Address	Description
SPCR	0x002C	SPI control register. Enables and configures the SPI peripheral.
SPSR	0x002D	SPI status register. Can be polled to detect when an SPI cycle is complete.
SPDR	0x002E	SPI data buffer register. 8-bit
DDR_SPI	0x0004	Data direction register for SPI pins.
PORT_SPI	0x0005	Input data port register for SPI.

Other user interfacing requirements include push-button de-bouncing and rotary encoder decoding. A simple de-bounce routine is implemented using the 8-bit timer module to periodically sample the input pins. The timer is initialized to interrupt every 2ms by setting the clock pre-scalar in the timer/counter control register (TCCR0B) and corresponding value in the output compare register (OCR0B). When the timer runs the value stored in the counter register (TCNT0) is compared with the value in OCR0B, if they are equal an interrupt occurs. [6] Rotary encoder decoding is also performed using the timer interrupt to filter out spurious pulses on the input pins.

Table 10-8: ATmega168 Timer/Counter Peripheral Registers [6]

Register	Memory Address	Description
TCCR0B	0x0025	Timer/count control register
TIMSK0	0x006E	Timer interrupt mask register
OCR0B	0x0028	Output-compare register 0
TCNT0	0x0026	Timer/counter count register 0

The ATmega168 has three separate memory spaces: data, program and EEPROM. Program space is provided by 16K of on-chip in-system programmable flash memory. [5] Instructions are fetched directly out of this flash memory space therefore program memory may not be used to store variable data. Data memory consists of 32 general purpose CPU registers, 64 I/O registers, 160 extended I/O (peripheral) registers and 1K of SRAM. Internal registers are mapped to the lowest part of this address space and SRAM is mapped to the remaining addresses. SRAM is used to store volatile program data and provide stack and heap space. 4K of on-chip EEPROM provides non-volatile data memory which can be programmed during normal program execution. [5, 6]

Table 10-9: ATmega168 Memory Organization [6]

Data Memory		EEPROM		Program Memory	
32 CPU Registers	0x0000 0x001F	4K Data EEPROM	0x0000	Application Flash Section	0x0000
64 I/O Registers	0x0020 0x005F				
160 Extended I/O Registers	0x0060 0x00FF				
1K SRAM	0x0100 0x04FF		0x0FFF	Boot Flash Section	0x1FFF

10.3 Software Design Narrative

Software for both the ATmega168 microcontroller and SHARC DSP is organized into several modules. At the highest level, device independent interfaces provide the necessary abstraction to simplify the software development and separate the concerns of lower-level peripheral interaction. This approach works well with most of the software but care is taken when including additional abstraction that adds unnecessary overhead. In this section the major software modules/components will be presented with a short description and their functional interface. A hierarchical view of these software components is presented in Appendix H.

The transmitter ATmega168 microcontroller is responsible for configuring the PGA2505 and the nRF24Z1. A simple state machine controls the process of initializing the nRF24Z1 and ensuring the wireless link remains active. The microcontroller must also act on the user input events: volume increment, volume decrement and enable input pre-amp. Flags for each user input event indicate when action needs to be taken. On the receiver, an ATmega168 microcontroller is responsible for maintaining EQ, digital mute and volume settings for the SHARC and controlling the user interface. Much of the work performed on the receiver microcontroller is to update the LCD display and respond to push button and encoder events. All of the SPI communication and user input handling is performed using interrupts, which leaves the main loop free to update the LCD.

The SHARC main loop performs device initialization and audio block processing. Immediately after startup the nRF24Z1, the PCM1792a and the ATmega168 are initialized. By default the auxiliary (receiver) PCM4202 DAC is set as the audio source. Once initialization completes, audio is buffered into large blocks for processing. A “block ready” flag indicates that the buffer is full and ready for processing. While the main loop waits for the audio buffer to fill the processor is free to perform housekeeping communication with the ATmega168 and

nRF24Z1. The SHARC will always update its local set of audio settings during this time. If the nRF24Z1 is set as the audio source then the SHARC will also query for link status and volume increment and decrement flags from the nRF24Z1. If the wireless link is lost the SHARC will instruct the nRF24Z1 to re-establish the wireless link. The main loop will also check for an audio source change flag to re-initialize the signal routing unit and serial port interrupts.

10.3.1 PGA2505 Device Interface

The PGA2505 preamplifier is used to apply variable gain to audio input on the transmitter. Underneath the hood of the interface a SPI device driver sends configuration to the PGA2505 serial control port. The user specifies GPIO and gain values and then calls the configure function to commit new settings to the PGA2505. Only the initialize, set and configure functions need to be called from the top-level software.

Table 10-10: PGA2505 Device Interface

Function	Description
void PGA2505_Init(void)	Initializes the interface and internal state information.
void PGA2505_SetGPIO(unsigned char)	Set the value of the GPIO bits.
void PGA2505_SetGain(unsigned char)	Set the value of the gain constant.
void PGA2505_Configure(void)	Sends all configuration data to the PGA2505.
void PGA2505_Enable(void)	Selects the PGA2505 slave.
void PGA2505_Disable(void)	Deselects the PGA2505 slave.

10.3.2 PCM1792a Device Interface

The PCM1792a digital to analog converter accepts digital PCM coded I2S audio and outputs current driven differential signals. PCM1792a configuration data is stored in a set of on-chip registers and is programmed via an SPI interface. Since configuration is static, only the initialize function needs to be called from top-level code. Raw configuration data is written by constructing a single 16-bit word that contains the address and write flag in the upper byte and data in the lower byte.

Figure 10-11: PCM1792a Device Interface

Function	Description
void PCM1792_Init(void)	Initializes the interface and sends configuration data to the PCM1792.
void PCM1792_SPIEnable(void)	Initializes the underlying SPI peripheral and selects the PCM1792a slave.
void PCM1792_SPIDisable(void)	Deselects the PCM1792a slave.

int PCM1792_SPIWrite(int)	Reads and writes a single word to the PCM1792a over the SPI bus.

10.3.3 nRF24Z1 Device Interface

The nRF24Z1 is a complex wireless audio transceiver that accepts I2S audio input for transmission over a 2.4GHz channel. The nRF24Z1 device interface exposes the necessary functions to initialize both the receiver (ARX) and transmitter (ATX). When power is applied, the nRF24Z1 is initialized as either a transmitter or receiver. Common RF settings are also set on both the receiver and transmitter. Once initialized the nRF24Z1 will maintain the wireless audio link. Common tasks such as polling link status are provided by the interface for convenience. Internally the nRF24Z1 interface calls SPI driver routines to read and write data to internal registers.

Table 10-12: nRF24Z21 Device Interface

Function	Description
void nRF24Z1_InitSlaveInterface(void)	Initialize the underlying SPI interface.
unsigned char nRF24Z1_Read(unsigned char)	Read a single byte from the nRF24Z1 at the specified address.
void nRF24Z1_Write(unsigned char, unsigned char)	Write a single byte to the nRF24Z1 to the specified address.
unsigned char nRF24Z1_HasLink(void)	Return 1 if the nRF24Z1 has an RF link established with another device.
void nRF24Z1_ForceRelink(void)	Force the nRF24Z1 to re-establish the RF link.
void nRF24Z1_SetAddress(unsigned char, unsigned char, unsigned char, unsigned char, unsigned char)	Set the five address bytes of the nRF24Z1.
void nRF24Z1_InitARXRegisters(void)	Initialize the nRF24Z1 as an audio receiver.
void nRF24Z1_InitATXRegisters(void)	Initialize the nRF24Z1 as an audio transmitter.
void nRF24Z1_InitRFCHRegisters(void)	Initialize common nRF24Z1 RF settings.

10.3.4 SHARC Communication

Communication between the SHARC and ATmega168 is implemented using an SPI bus. A simple state machine and interrupt routine handles SPI communication on the ATmega168. The slave select pin triggers a pin-change interrupt that resets the state machine. An interrupt occurs each time a complete byte is shifted into the SPI receive buffer. Each read or write requires an 8-bit address which contains a read or write flag in the most significant bit. Once an address is received, a byte is either placed into the transmit buffer to send to the SHARC or the state machine waits for the next by to be received from the SHARC. There is no functional interface for this component because all operations are performed in the SPI interrupt handler.

10.3.5 ATmega168 Device Interface

Communication between the SHARC and ATmega168 is implemented using an SPI bus. The SHARC implements a polling based SPI routine to read or write from the ATmega168 slave. While the polling based method blocks the main loop the amount of time needed for an individual transfer is very small. Each read or write requires an 8-bit address and that contains an optional write flag in the most significant bit. An address is followed by an additional SPI cycle to send the byte to write or receive the byte to read.

Table 10-13: ATmega168 Device Interface

Function	Description
void ATmega168_WriteByte(unsigned char, unsigned char)	Write a single byte to the ATmega168 at the specified address.
unsigned char ATmega168_ReadByte(unsigned char)	Read a single byte from the ATmega168 from the specified address.
void ATmega168_SlaveEnable(void)	Initialize the underlying SPI interface and select the ATmeg168 slave.
void ATmega168_SlaveDisable(void)	Deselect the ATmega168 slave.
unsigned char ATmega168_SPIByte(unsigned char)	Perform a single SPI byte transfer.

10.3.6 LCD Device Interface

The LCD interface provides convenient means of displaying information on the LCD. Communication is implemented using the USART module of the ATmega168 using a simple polling based device driver. Since the LCD display routines are the only functions called from the microcontrollers main loop an interrupt driven approach was not necessary. Complex commands are simplified by wrapping the necessary USART transfers into functions. The interface provides a means of controlling major LCD functions such as writing characters to specific locations, adjusting the backlight, and setting contrast levels.

Table 10-14: LCD Device Interface

Function	Description
void LCD_InitPort(void)	Initialize the LCD communication port (USART)
void LCD_InitDisplay(void)	Initialize the LCD display with common settings
void LCD_SendByte(char)	Send a byte of data to the LCD
void LCD_SetBootScreenMode(char)	Set the boot screen display mode of the LCD.
void LCD_SetBacklight(char)	Set the backlight level (0-100)
void LCD_SetContrast(char)	Set the contrast level (0-100)
void LCD_SetCursorPosition(char, char)	Moves the LCD cursor to the specified row and column
void LCD_PutChar(char, char, char)	Puts a character at the specified location
void LCD_PutString(char*, char, char)	Puts a string at the specified location

10.3.7 ATmega168 SPI Peripheral Interface

Provides initialization and transmit functions for the ATmega168 SPI peripheral. The interface provides both initialization and communication using master or slave mode in both interrupt and non-interrupt driven modes.

Table 3-6: ATmega168 SPI Peripheral Interface

Function	Description
void SPI_InitMaster(void)	Initialize the SPI peripheral in master mode with no interrupts.
void SPI_InitMasterWithInterrupts(void)	Initialize the SPI peripheral in master mode with interrupts.
void SPI_InitSlave(void)	Initialize the SPI peripheral in slave mode with no interrupts.
void SPI_InitSlaveWithInterrupts(void)	Initialize the SPI peripheral in slave mode with interrupts.
unsigned char SPI_TransmitByte(unsigned char)	Performs an SPI transfer by polling the SPI status register

10.3.8 Audio Serial Ports Interface

This module contains initialization functions and interrupts for the serial port (SPORT) and the precision clock generator peripherals. The serial ports are used to communicate with off-chip audio devices using the I2S serial audio interface. Interrupt handlers are used to send and receive individual samples and to perform initial processing such as converting fixed point samples to floating point and scaling to a normalized range. Separate interrupt handlers are required to accommodate differences in the nRF24Z1 and the PCM4202 word size. The nRF24Z1 can only output 16-bit PCM digital audio while the PCM4202 supports 24-bit words. The interrupt handlers are also responsible for maintaining the buffer pointers so that the correct sample buffer is accessed in the main processing loop.

Table 10-16: Audio Serial Port Peripheral Interface

Function	Description
void InitSPORT(void)	Initialize all SPORT peripherals.
void InitPCG(void)	Initialize the precision clock generator.
void OnSample_nRF24Z1(void)	Interrupt handler for nRF24Z1 audio source.
void OnSample_Auxillary(void)	Interrupt handler for PCM4202 auxiliary audio source.

10.3.9 Audio Block Processing Interface

This module contains audio block processing functions that apply EQ effects, digital mute and volume to sample blocks. EQ effects are applied in frequency domain by first computing the FFT of each sample block, multiplying the EQ constants to the respective frequency bin and then computing the inverse FFT. Digital mute examines the sample of each block and mutes any sample that is below the set volume threshold. To mute a sample it is simply set to a value of 0.

Volume is applied by multiplying every sample by a specified constant between 0 and 1. These functions are implemented within the main loop and do not have separate function declarations.

10.4 Summary

In this report major software design considerations were presented along with the rationale for particular design choices or implementations. A complete listing of the major software module functions and a discussion of the overall software organization was also covered. Most of the software challenges are meeting the timing requirements of the various off-chip peripherals and ensuring correct initialization of on-chip signal routing. Clever use of available processing time reduces the need to implement interrupt driven device drivers.

11.0 Version 2 Changes

Version 2 would implement many changes to improve Digital Sound Projection. Changes would be employed in both the transmitter and receiver designs. Revisions on the transmitter include a reduction in size and increasing the range for the wireless transmission. The receiver changes include implementing a more solid power supply, adjusting the user input, and upgrading some components.

For the transmitter the main revision includes decreasing the size of the device to attempt to make the device handheld. One solution includes using an on-chip antenna in order to eliminate the need for a large antenna and corresponding connection. The size of the board would also reduced by using smaller passive components, preferably using 0402 packages instead of the 1206 that are currently in the design. Smaller battery packs would also decrease the thickness and length of the required package for the transmitter. However, some version 2 changes would increase the size of the board design. In order to increase the range of the wireless transmission, a power amplifier IC would be included in the design to increase the output power of the transmitted signal. Some additional circuitry would also be needed for an on board battery charger. This would allow the user to charge the transmitter without having to open the case to remove the batteries. This will increase reliability of the transmitter and ease of use for the user.

The receiver changes for version 2 are also to improve the functionality of Digital Sound Projection. One change includes adjusting the receiver package to eliminate the gap between the bottom and top of the package used for heat dissipation. The case would be designed with gaps cut in the top of the case or sides in order to provide air flow dissipation. This will improve the look of the receiver and secure the mechanical connection of the top and bottom of the case.

The receiver board design would also include a power amplifier IC for the antenna. Unlike the transmitter, an on-chip antenna will not be needed and the existing antenna can be used. The power amplifier will only be needed to increase the power of the incoming signal to increase the effective range. The board design for the receiver will also include better circuitry for the 19V to 5V voltage regulation. This circuitry will remove the need for the power module in the current implementation and the required “fly-wire” to connect the module to the receiver.

Another change for the receiver in version 2 will include replacing the SHARC ADSP-21262 DSP chip with a newer version of the SHARC. This will increase the memory in the system and allow for the implementation of more functions in Digital Sound Projection. The current version

of Digital Sound Projection is limited in the amount of functions available to the user due to the amount of on-chip memory. An example of another function that would be available to the user is the ability to save current EQ settings into memory so that the user can recall these settings even after the system is powered off. Version 2 would also include a more robust user interface. The current LCD would be replaced with a graphical LCD to implement a more user friendly and more involved display. The amount of actions involved to switch between displays on the LCD would also be dramatically reduced improve the user's experience.

12.0 Summary and Conclusions

DSP successfully accomplished all of the PSSC's. The transmitter successfully transmits digital audio which is output at the receiver base station. The user is also able to adjust the volume of the system wirelessly from the transmitter. At the receiver, the user can implement EQ effects or digital mute through the LCD user interface. The LCD also displays information about the device including volume level, input source, EQ levels, and digital mute settings.

The team learned how to implement a design from start to finish under severe time constraints. This applies to each stage of the design process from preliminary design, prototyping through bread-boarding, capturing circuitry in schematics, designing the PCB's, populating components and debugging PCB's, and software / hardware interfacing. The team learned how to identify and solve problems throughout the design process.

13.0 References

13.1 Section 3 References

[1] S. Smith. The Scientists and Engineers Guide to Digital Signal Processing. California Technical Publishing, 1997. [Online]. Available: http://www.dspguide.com/ch29/5.htm

[2] CrystalFontz America Inc., CFA-634 Serial LCD Datasheet, Oct. 2005. [Online]. Available: http://www.crystalfontz.com/product/CFA634-TMC-KS.html

[3] Sennheiser USA, freePORT Presentation Product Page. [Online]. Available: http://www.sennheiserusa.com/professional_wireless-microphone-systems_wireless-instrument-systems_freeport_502808

[4] Shure Inc., ULX Wireless Microphone Systems Specification Sheet, 2009.

[5] Analog Devices Inc., ADSP-21261/21262/21266 Processor Datasheet, Jul. 2009. [Online]. Available: http://www.analog.com/static/imported-files/data_sheets/ADSP-21261_21262_21266.pdf

[6] Texas Instruments Inc., TMS320C6711D Processor Datasheet, Oct. 2005. [Online]. Available: http://www.ti.com/lit/gpn/tms320c6711d

[7] Analog Devices Inc., AD1935/1936/1937/1938/1939 Audio Codec Datasheet.

[8] Texas Instruments Inc., PCM4202 Analog-to-Digital Converter Datasheet, Mar. 2007. [Online]. Available: http://www.ti.com/lit/gpn/pcm4202

[9] Texas Instruments Inc., PCM1792A Digital-to-Analog Converter Datasheet, Nov. 2006. [Online]. Available: http://www.ti.com/lit/gpn/pcm1792a

[10] Nordic Semiconductor, nRF24Z1 2.4GHz Wireless Audio Streamer Datasheet, Jun. 2006. [Online]. Available: http://www.nordicsemi.com/index_popup.cfm?obj=misc&act=download&pro=86&prop=607

[11] STS, DARR80 Product Brief. [Online]. Available: http://www.sts.sg/products.asp?product=1

[12] Panasonic Corp., EVEG/H/K/L Square GS Encoder Datasheet, Apr. 2008.

13.2 Section 4 References

[1] Free Patents Online, Sound Enhancement for Audio Devices Based on User-Specific Audio Processing Parameters, July 2006. [Online]. Available: http://www.freepatentsonline.com/7680465.html

[2] Shure Incorporated, ULX Wireless Microphone Systems Specification Sheet, 2009. [Online]. Available: http://www.shure.com/stellent/groups/public/@gms_gmi_web_ug/documents/web_resource/us_pro_ulx-specsheet.pdf

[3] J & R Electronics, Technical Pro RX-B32 Stereo Home Receiver, [Online]. Available: http://www.jr.com/technical-pro/pe/TAE_RXB32/#productTabDetails

13.3 Section 5 References

[1] United States of America. Department of Defense. *Military Handbook: Reliability Prediction of Electronic Equipment.* Washington D.C.: Department of Defense, 1991.

[2] Analog Devices Inc., ADSP-21261/21262/21266 Processor Datasheet, Jul. 2009. [Online]. Accessed: http://www.analog.com/static/imported-files/data_sheets/ADSP-21261_21262_21266.pdf

[3] Texas Instruments Inc., PCM1792A Digital-to-Analog Converter Datasheet, Nov. 2006. [Online]. Accessed: http://www.ti.com/lit/gpn/pcm1792a

[4] Nordic Semiconductor, nRF24Z1 2.4GHz Wireless Audio Streamer Datasheet, Jun. 2006. [Online]. Accessed: http://www.nordicsemi.com/index_popup.cfm?obj=misc&act=download&pro=86&prop=607

[5] AVR ATmega168, 8-bit Microcontroller Datasheet, Jul. 2009. [Online]. Accessed: http://www.atmel.com/dyn/resources/prod_documents/doc2545.pdf

[6] Texas Instruments Inc., PCM4202 Analog-to-Digital Converter Datasheet, Nov. 2006. [Online]. Accessed: http://www.ti.com/lit/gpn/pcm4202

13.4 Section 6 References

[1] Thermotron, "Accelerated Stress Testing," *Thermotron – Products: Accelerate Stress Test (AST) Environmental Test Chamber*. [Online]. Available: http://www.thermotron.com/products/ast.html [Accessed: Apr. 11, 2010].

[2] "Product Safety Datasheet – Nickel Metal Hydride Batteries," *Energizer – Product Safety Datasheet.* Jan, 2010. [Online]. Available: http://data.energizer.com/PDFs/nickelmetalhydride_psds.pdf [Accessed: Apr. 15, 2010].

[3] Nordic Semiconductors, "2.4GHz Wireless Audio Streamer – nRF24Z1," *Preliminary Product Specification – Nordic Semiconductor.* [Online]. Available: http://www.nordicsemi.com/files/Product/data_sheet/nRF24Z1_PPS_rev3_1.pdf [Accessed: Apr. 15, 2010].

[4] Environmental Protection Agency, "Wastes – Resources Conservation – Wastes and Materials – Batteries," *Batteries | Common Wastes and Materials | USA EPA*. [Online]. Available: http://www.epa.gov/epawaste/conserve/materials/battery.htm [Accessed: Apr. 11, 2010].

[5] Environmental Protection Agency, "Wastes – Partnerships – Plug-In To e-Cycling – Reuse & Recycle – eCycle," *Reuse and Recycle – eCycle | Plug-In To eCycling | US EPA.* [Online]. Available: http://www.epa.gov/epawaste/partnerships/plugin/reuse.htm [Accessed: Apr. 12, 2010].

[6] Earth 911, "Earth911.com," *Earth911.com – Find Recycling Centers and Learn How to Recycle.* [Online]. Available: http://earth911.com/ [Accessed: Apr. 12, 2010].

[7] RoHS, "Working with EEE producers to ensure RoHS compliance through the European Union," *RoHS Compiance in the EU – WEEE / REACH legislation.* [Online]. Available: http://www.rohs.eu/english/index.html [Accessed: Apr. 12, 2010].

[8] Advanced Circuits, "RoHS Compliance Printed Circuit Boards," *Advanced Circuits RoHS prototype printed circuit board manufacturer, RoHS Compliant Circuit Board.* [Online]. Available: http://4pcb.com/index.php?load=content&page_id=17 [Accessed: Apr. 12, 2010].

13.5 Section 7 References

[1] Shure Incorporated, "Shure ULX Wireless System User Guide," *Shure – Wireless Systems – ULX Standard Wireless Systems*, 2001. [Online]. Available: http://www.shure.com/ProAudio/Products/WirelessMicrophones/us_pro_ULXS_content [Accessed: Jan. 30, 2010].

[2] Sennheiser Electronic Corporation, "freePORT Presentation Set, Article No. 502808," *Sennheiser USA – wireless presentation receiver Set, freePORT, clip microphone, wireless*. [Online]. Available: http://www.sennheiserusa.com/professional_wireless-microphone-systems_wireless-instrument-systems_freeport_502808 [Accessed: Jan. 30, 2010].

[3] Radioshack Corporation, "Project Enclosure (6x4x2")," *Project Enclosure (3x2x1") – RadioShack.com*, 2010. [Online]. Available: http://www.radioshack.com/product/index.jsp?productId=2062283 [Accessed: Apr. 25, 2010].

[4] Bud Industries, "Aluminum Chassis, Part Number AC-401 through AC-1431," *http://www.budind.com/pdf*, 2010. [Online]. Available: http://www.budind.com/pdf/hb401.pdf [Accessed: Apr. 25, 2010].

13.6 Section 8 References

[1] Analog Devices Inc., ADSP-21261/21262/21266 Processor Datasheet, Jul. 2009. [Online]. Available: http://www.analog.com/static/imported-files/data_sheets/ADSP-21261_21262_21266.pdf

[2] Texas Instruments Inc., PCM4202 Analog-to-Digital Converter Datasheet, Mar. 2007. [Online]. Available: http://www.ti.com/lit/gpn/pcm4202

[3] Texas Instruments Inc., PCM1792A Digital-to-Analog Converter Datasheet, Nov. 2006. [Online]. Available: http://www.ti.com/lit/gpn/pcm1792a

[4] Texas Instruments Inc., PGA2505 Digital Controlled Microphone Preamplifier Datasheet, Jun. 2009. [Online]. Available: http://www.ti.com/lit/gpn/pga2505

[5] Nordic Semiconductor, nRF24Z1 2.4GHz Wireless Audio Streamer Datasheet, Jun. 2006. [Online]. Available: http://www.nordicsemi.com/index_popup.cfm?obj=misc&act=download&pro=86&prop=607

[6] AVR ATmega168, 8-bit Microcontroller Datasheet, Jul. 2009. [Online]. Available: http://www.atmel.com/dyn/resources/prod_documents/doc2545.pdf

13.7 Section 9 References

[1] Nordic Semiconductor, nRF24Z1 Design-in of RF Circuits, Nov. 2002. http://www.nordicsemi.com/files/Product/white_paper/RF-design-in.pdf

[2] Nordic Semiconductor, nRF24Z1 2.4GHz Wireless Audio Streamer Datasheet, Jun. 2006. http://www.nordicsemi.com/index_popup.cfm?obj=misc&act=download&pro=86&prop=607

[3] Texas Instruments Inc., SLTA055 Input and Output Capacitor Selection, February 2006. http://focus.ti.com/lit/an/slta055/slta055.pdf

[4] Analog Devices Inc., ADSP-21261/21262/21266 Processor Datasheet, Jul. 2009. http://www.analog.com/static/imported-files/data_sheets/ADSP-21261_21262_21266.pdf

13.8 Section 10 References

[1] Analog Devices Inc., ADSP-21261/21262/21266 Processor Datasheet, Jul. 2009. [Online]. Accessed: http://www.analog.com/static/imported-files/data_sheets/ADSP-21261_21262_21266.pdf

[2] Texas Instruments Inc., PCM1792A Digital-to-Analog Converter Datasheet, Nov. 2006. [Online]. Accessed: http://www.ti.com/lit/gpn/pcm1792a

[3] Texas Instruments Inc., PGA2505 Digital Controlled Microphone Preamplifier Datasheet, Jun. 2009. [Online]. Accessed: http://www.ti.com/lit/gpn/pga2505

[4] Nordic Semiconductor, nRF24Z1 2.4GHz Wireless Audio Streamer Datasheet, Jun. 2006. [Online]. Accessed: http://www.nordicsemi.com/index_popup.cfm?obj=misc&act=download&pro=86&prop=607

[5] AVR ATmega168, 8-bit Microcontroller Datasheet, Jul. 2009. [Online]. Accessed: http://www.atmel.com/dyn/resources/prod_documents/doc2545.pdf

[6] AVR ATmega168, 8-bit Microcontroller Processor Manual, Jul. 2009. [Online]. Accessed: http://www.atmel.com/dyn/resources/prod_documents/doc2545.pdf

[7] Texas Instruments Inc., PCM4202 Analog-to-Digital Converter Datasheet, Nov. 2006. [Online]. Accessed: http://www.ti.com/lit/gpn/pcm4202

Appendix A: Individual Contributions

A.1 Contributions of Steve Anderson:

One major contribution involved drawing up the schematics in PADS for the individual chips and different stages for Digital Sound Projection's receiver. I created the PCB decals for the ICs, various connectors, and special parts that PADS did not already have decals created for. The schematics were fine tuned after testing the different circuits in order to get accurate schematics for the PCB layouts. In order to make sure that the individual schematics were designed correctly in the complete system, an overall schematic was put together to link the individual schematics together. This assured that all the chips had the correct I/Os between one another and correct powers supplied to them.

Another major contribution was the completion of the PCB for the receiver device by drawing the traces in PADS by hand to assure proper design. Originally a single two layer board was being designed, but after several revisions it was found that the required size by Purdue was not achievable with the use of a two layer board. This required a redesign of the receiver board for the use of a four layer board. The top and bottom layers were used as signal layers, the second inner layer was used for the different power traces, and the third inner layer was used for the ground traces. Two boards were created in order to meet Purdue's size requirement for the four layer board. One board was designed to contain the digital components and the other board contained the analog components. After these new four layer boards were designed, another check was made before submission to assure the correct connections were made and there were no discrepancies between the schematic and PCB layout.

After the PCBs were returned by the fabrication house, I checked all the connections on the two receiver boards with an ohmmeter. This was to make sure there were no errors in the manufacturing of the boards before soldering anything onto the PCBs. After a thorough check, the boards were verified except for one mistake with an op-amp design in PADS. This fix was made in the PADS schematic for future use and reference. I also helped solder on many of the components on the receiver digital board and transmitter board. After various stages of soldering, I assisted in testing the functionality of the boards and components. When we ran into a problem, such as too much current passing through our regulators, I helped come up with different solutions.

I also helped with the design and completion of the packaging for both the receiver and transmitter. Also, when it was realized that the range of the wireless transmission was not as expected, I then diagnosed why we were experiencing power loss and where it was occurring within our system.

Two technical documents were designated to me: the PCB layout considerations and the Patent Liability Analysis. Research was completed in order to determine if the major functions of Digital Sound Projection infringed on any existing patents or products. It was determined that there were no patents or products infringed upon under the doctrine of equivalents. The PCB layout consideration document illustrated the considerations taken in order to design the circuit boards for both the receiver and digital.

A.2 Contributions of Michael Goldfarb:

As the groups only Computer Engineer and member with substantive experience and background in embedded systems, I assumed all software development and digital hardware interfacing tasks. In the early stages of the project I guided the group members in component selection ensuring all interfacing requirements could be met with our selected microprocessors. I feel that I was also responsible for setting the overall pace of work. By the beginning of the second week I was looking ahead to ensure the group was in the best possible position to meet the major deadlines.

My initial work focused on becoming an expert on the ADSP-21262 SHARC DSP processor so that we could quickly prototype our system on the development board. I was able to get a good grounding in some important DSP concepts while working with Shao-Fu on some basic audio block processing programs. During the component selection stage my background in embedded systems was critical in ensuring we selected compatible components so that we could move forward with system development and prototyping without running into major roadblocks.

Once our design constraint analysis was complete and all major components were selected I began delving into the specific digital circuitry and interfacing necessary for our system. I would designate the correct pin mappings or required interface circuitry so that schematic and PCB layout could proceed concurrently with prototyping.

I worked with Shao-Fu to prototype every major component with our SHARC development kit. This work was invaluable to ensure all interfacing circuitry was correct before PCB fabrication. While prototyping I was able to develop and debug a majority of the software for the receiver and transmitter. This work culminated with a nearly flawless PCB layout and not need to flywire major bus connections or interfaces and very few bugs in critical device driver code.

With the system and all components operating correctly on the PCB I was able to focus on perfecting the user interface and DSP software without having to constantly debug the physical hardware. Our DSP algorithms were first implemented in MATLAB and then ported over to C code and optimized for the ADSP-21262.

A.3 Contributions of Shao-Fu Shih:

I designed the analog differential circuitry needed to interact with Texas Instrument's ADC and DAC. The differential circuitry input is generated by the OPA1632 singled to differential driver with Vcom of 2.5V. The differential to singled stereo RCA output is generated by six OPA1611 audio operational amplifiers in two tri-amp configurations for left and right channels. The DAC outputs differential current outputs, four of the OPA1611's are used as I/V converters for V+ and V-, and the two remaining OPA1611's are used as summing amplifiers to convert differential pairs to singled RCA outputs. To ensure a high SNR on the power rails in an high speed embedded environment, I implemented two cascaded LC low pass filters on the analog board to filter the digital switching noises on both +15V and -15V rails.

I also developed and simulated the digital audio signal processing algorithm (1D orthogonal transform) in Matlab. The algorithms include Short Time Fourier Transformation (STFT), Overlap-Save method, FFT Convolution, and time dependent frequency operations. To utilize the SHARC's memory, I coded the algorithms with minimum memory consumption. Also, to improve the time variant performance of the sample blocks, I customized the existing Overlap-Save method to be more sensitive to the time domain without sacrificing too much resolution in the frequency domain.

Since I have the most experience in soldering SOIC's on the team, I soldered the majority of the chips on the boards. For each of the IC's soldered, I double checked the connections and its general functionality. To connect the external components such as RCA connections and rotary encoder, I made custom bus wires and ensured they had stable connections to prevent unnecessary rewiring.

I also packaged the transmitter into the plastic project box. To secure the transmitter board in the box, I drilled six mounting holes and loaded the board with aluminum spacers and nuts. I mounted the power switch and LEDs in the front with custom bus wires and loaded the rechargeable NiMH batteries onto the plastic case using fasteners.

On the receiver aluminum casing, I used aluminum spacers and nuts to mount and secure both the digital and analog boards. To ventilate the aluminum casing for additional heat dissipation, I added six additional aluminum spacers to allow air flow through the aluminum

enclosure. To fly wire the RCA connectors to the analog board, I also soldered the insulated audio wire to the analog board for both singled input and output ports.

A.4 Contributions of Josh Smith:

For the Digital Sound Projection project, my main contributions to the project included the Packaging Design Considerations document, the Ethical and Environmental Impact Analysis document, the Final Report document, the schematic, layout, and routing of the transmitter circuit board, populating components onto the transmitter circuit board, and the general testing of the circuit board.

First, for the Packaging Design Considerations document, the packaging constraints were determined before researching possible packaging solutions. Taking into account the size constraints of the transmitter and EMI shielding constraints of the receiver, packaging to fit requirements was found and updated as the design evolved. Also, in order to complete CAD drawings of the packaging scheme, I learned how to use the AutoCAD program. The drawings were also updated as the packaging needs changed.

Next, I completed the Ethical and Environmental Impact Analysis document. I researched possible ethical and environmental issues that could result from Digital Sound Projection's design and solutions to these problems. Major ethical issues included the possibility of frequency sniffing, user safety warnings, and design testing to ensure the product is what the user expects. Solutions included the use of frequency hopping, warning labels, and a suite of planned tests for the design. Major environmental issues found included possible noise pollution, disposal of hazardous materials, and power consumption. Solutions included warnings against playing music at high volume levels, providing disposal resources, and using efficient power modules.

For the Final Report document, I was responsible for bringing together the report, ensuring accuracy of prewritten reports inserted into the final, and completing the remaining sections of the report.

I was also responsible for the schematic, layout, and routing of the transmitter circuit board. In order to complete this task, I learned how to utilize the PADS program through the course website resources and learning through using the program. After this, I created the schematics for a majority of the transmitter circuits. Another responsibility included creating custom footprints and logic decals for IC's, connectors, and through-hole capacitors, and other miscellaneous components used on both the transmitter and receiver circuit boards. Using the transmitter schematic created in PADS Logic, the transmitter circuit board was laid out and

routed. This process took several different approaches and multiple iterations in order to satisfy the small physical size requirement with all the desired circuitry. A final design was agreed upon with a size of 5 x 3", verified for accuracy, and submitted for manufacture to Advanced Circuits by Chuck.

Upon receiving the manufactured transmitter circuit board, I was responsible for testing connections, populating the circuit board, and testing for general circuit functionality. All circuit board connections were tested and only one mistake was found. The digital ground for the two PGA2505 microphone pre-amplifiers was floating; the issue was easily corrected with a single fly wire to the main digital ground trace. After testing connectivity, the board was populated with components one circuit section at a time starting with the power, followed by the microcontroller, the two audio channels, the ADC, and finally the 2.4GHz audio transceiver and antenna matching circuit. After each section was populated, the circuit was tested to ensure it functioned as expected. Upon completing the circuit and the software was loaded, the transmitter worked as expected.

Appendix B: Packaging

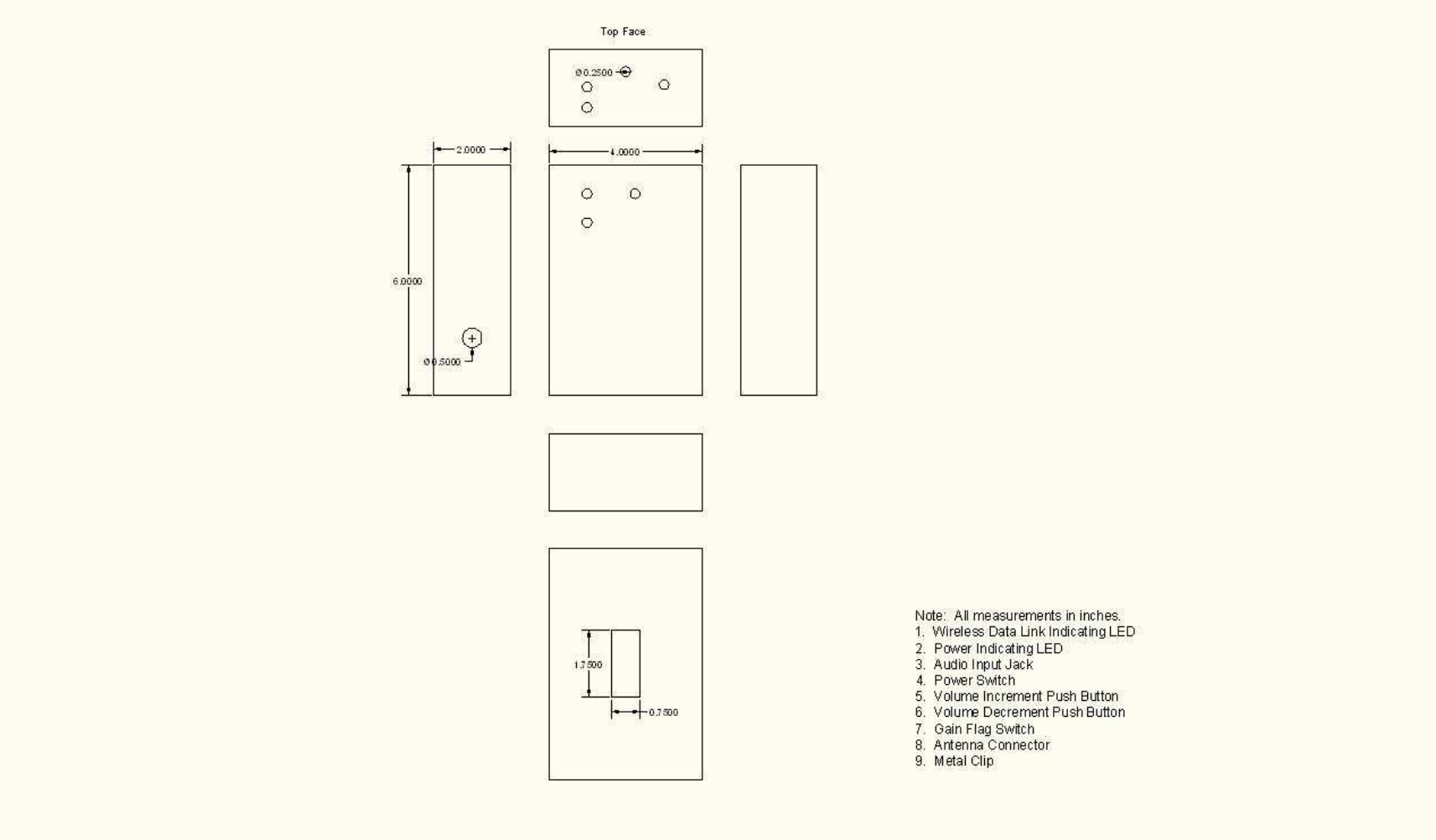


Figure B-1: Transmitter Packaging Illustration

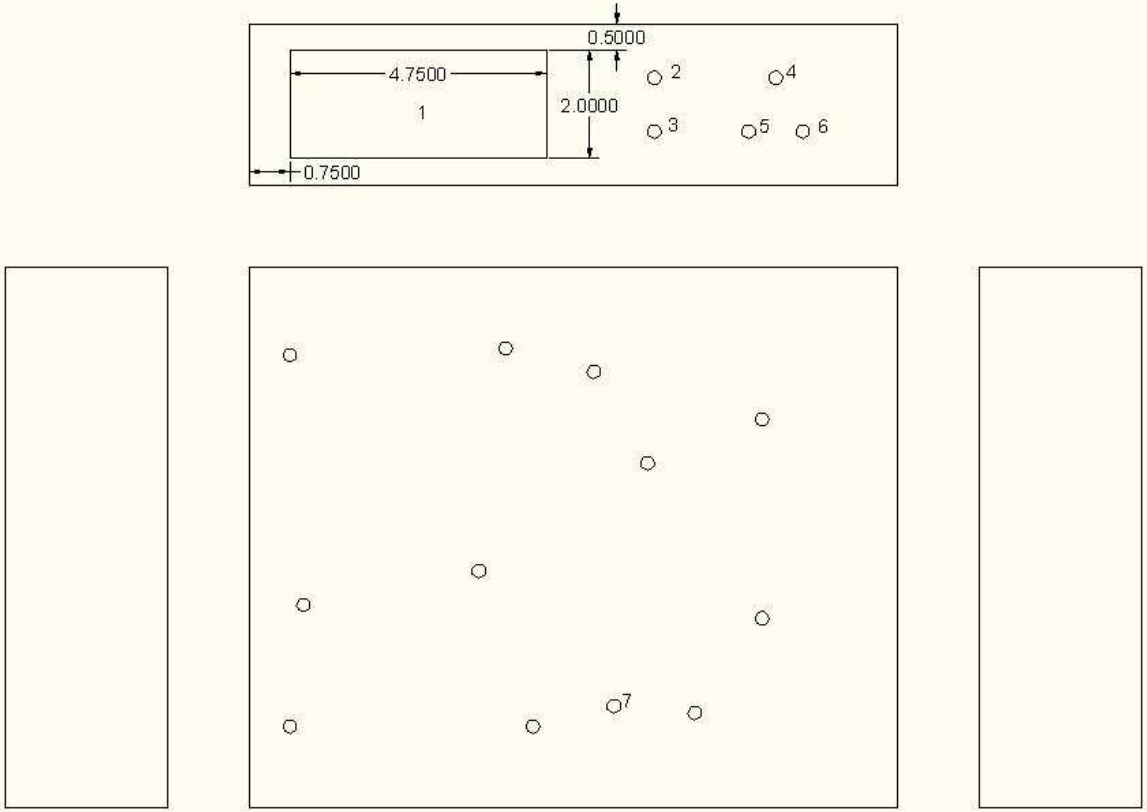
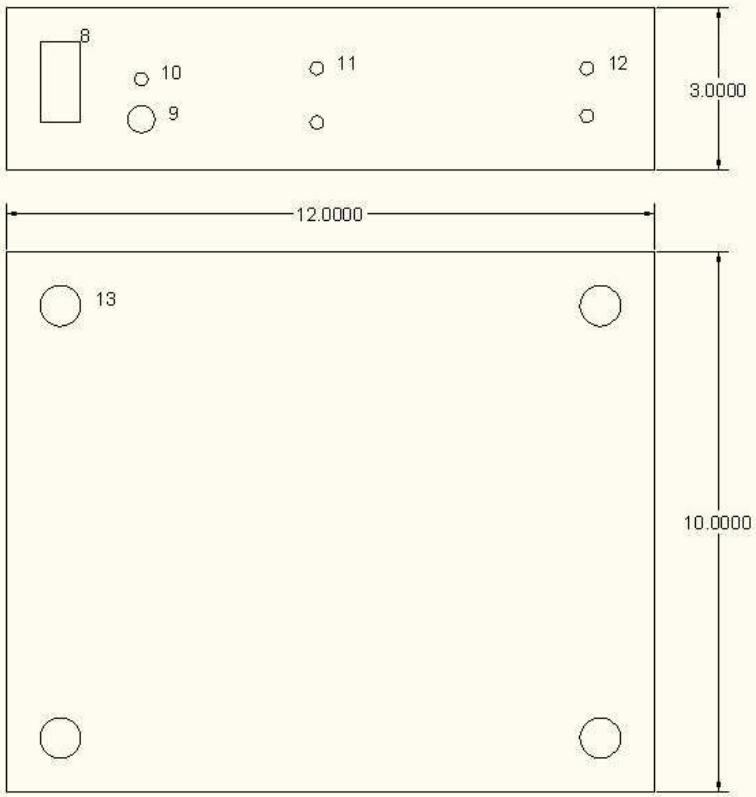


Figure B-2.1: Receiver Packaging Illustration: Top, Left, Front, and Right Faces



Note: All measures are in inches.
1. LCD Screen
2. Source Button
3. Menu Button
4. Rotary Encoder
5. Previous Button
6. Next Button
7. PCB Mounting Holes
8. Power Switch
9. Power Input
10. Antenna Input
11. RCA Input
12. Output
13. Rubber Pads

Figure B-2.2: Receiver Packaging Illustration: Rear and Bottom Face

Appendix C: Schematic

C.1 Receiver Schematics

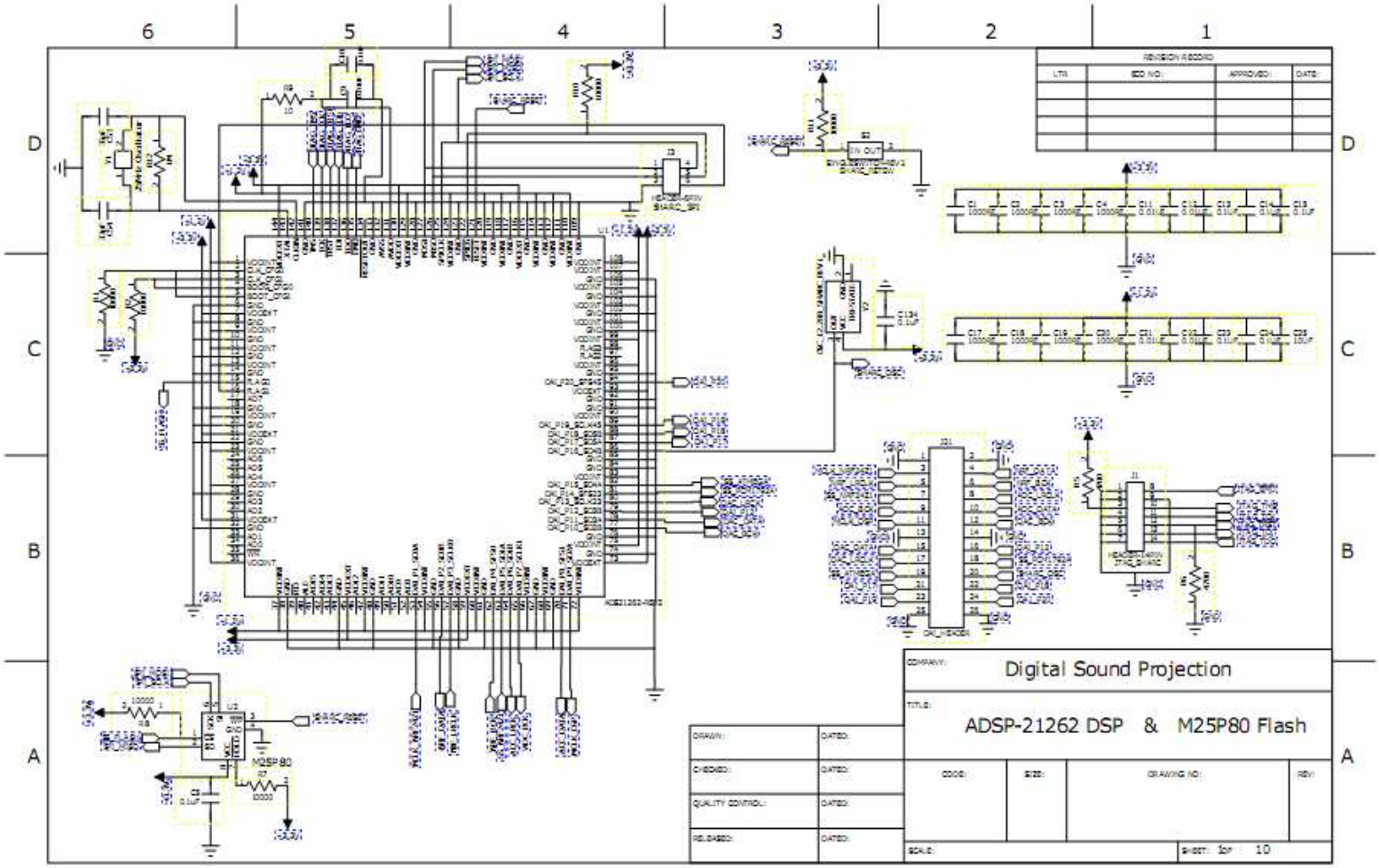


Figure C-1.1: SHARC ADSP-21262 and M25P80 Flash Schematic

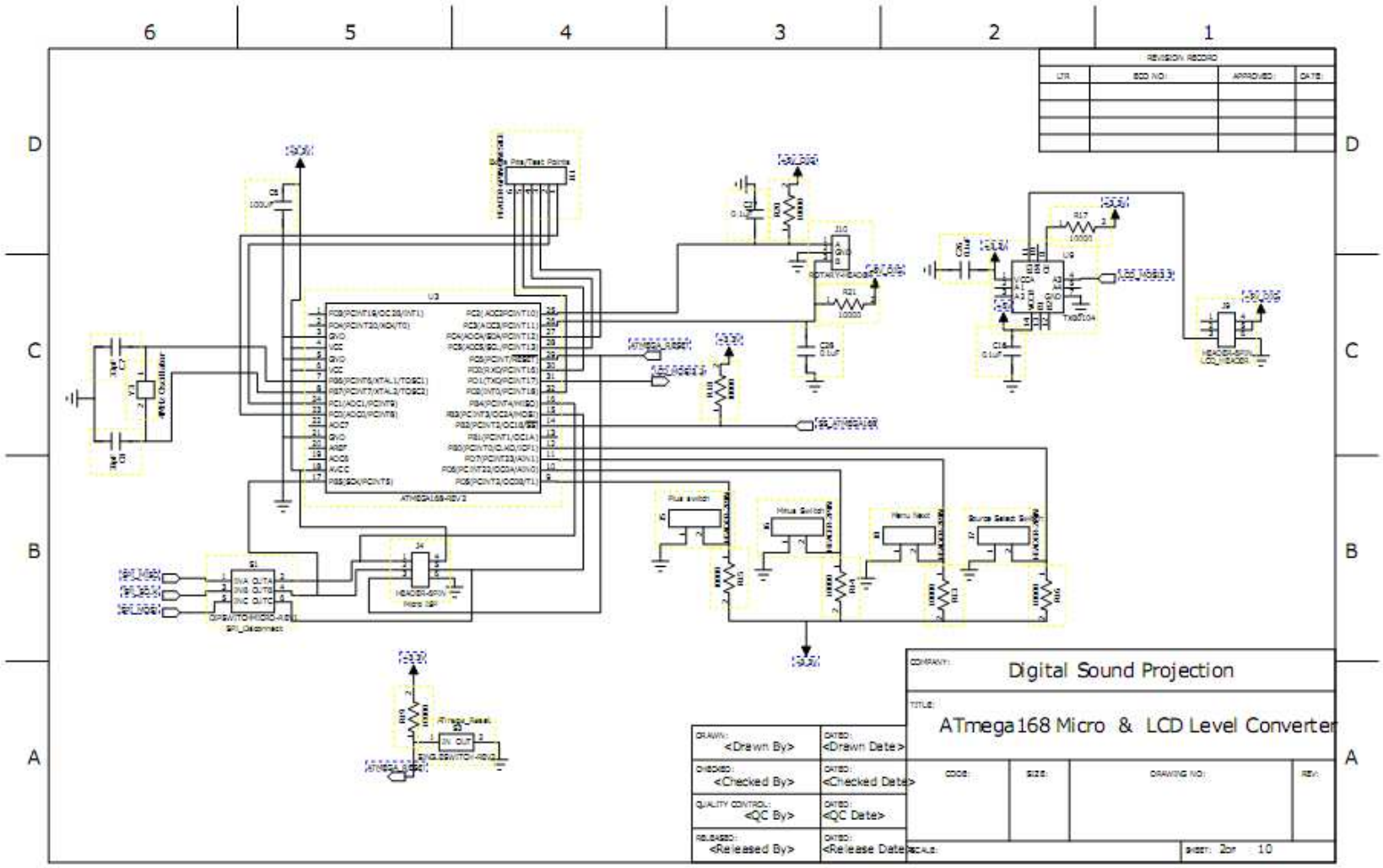


Figure C-1.2: ATmega168 Microcontroller and Voltage Level Translator Schematic

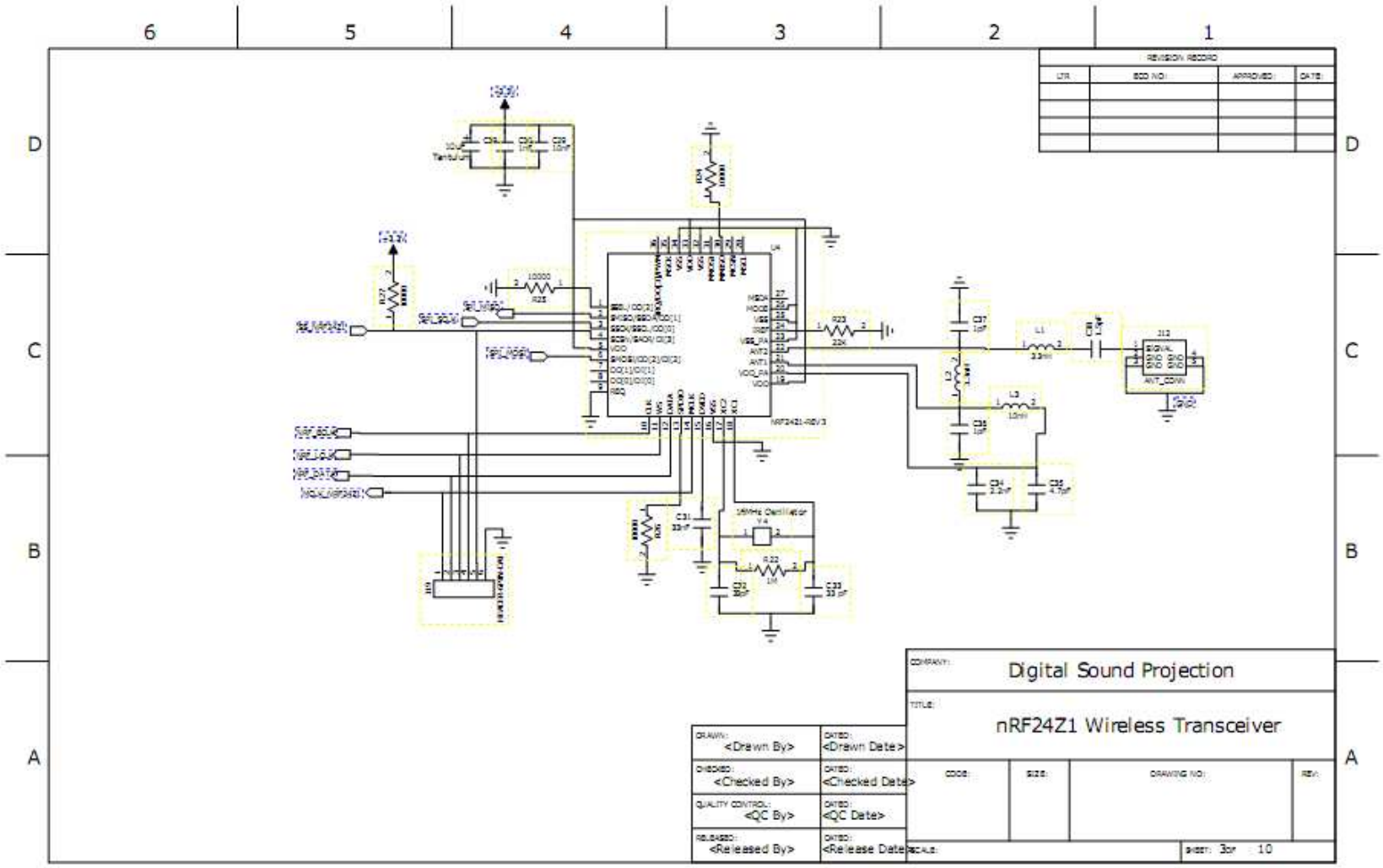


Figure C-1.3: nRF24Z1 Transceiver Schematic

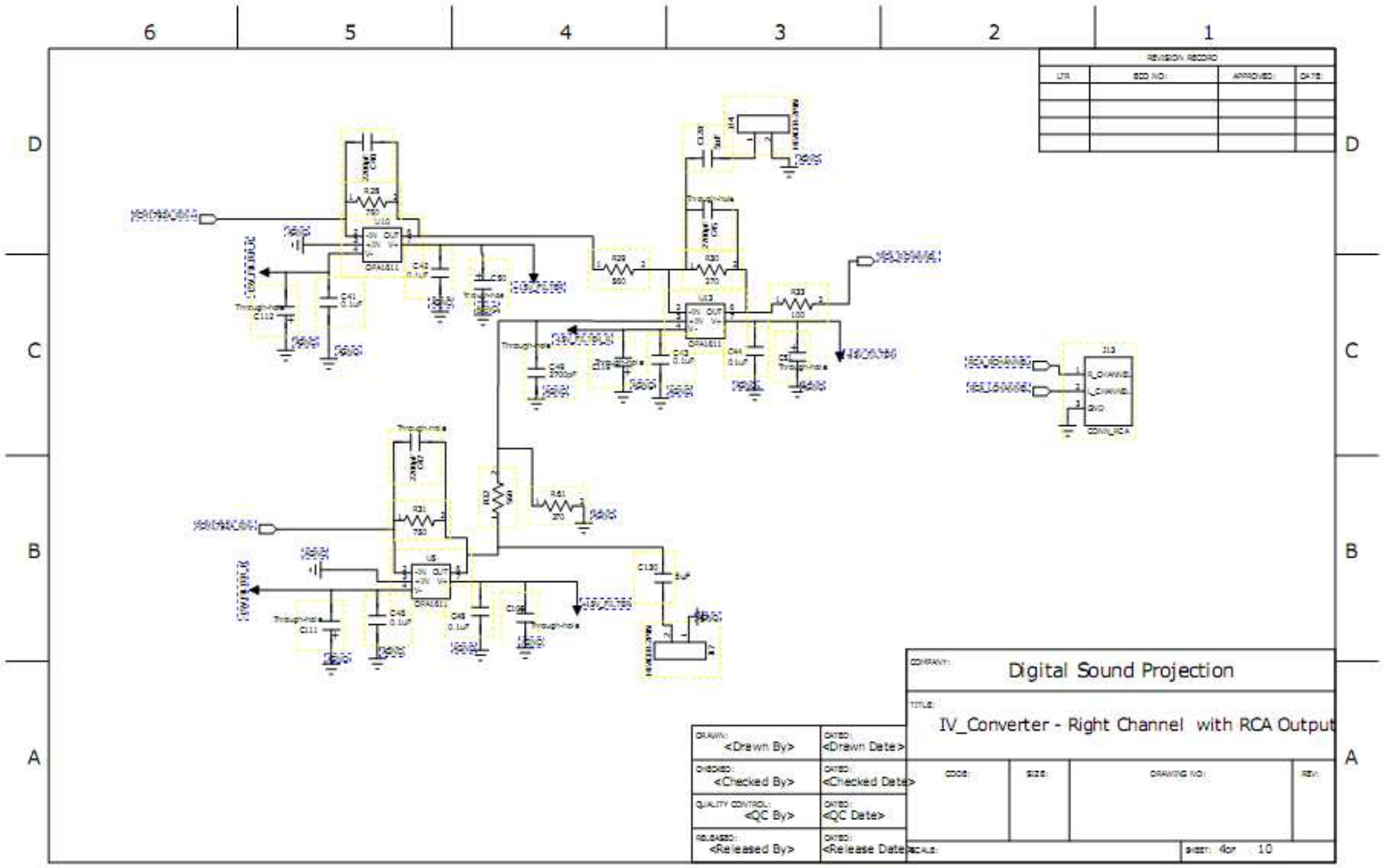


Figure C-1.4: IV Converter Output Stage – Right Channel Schematic

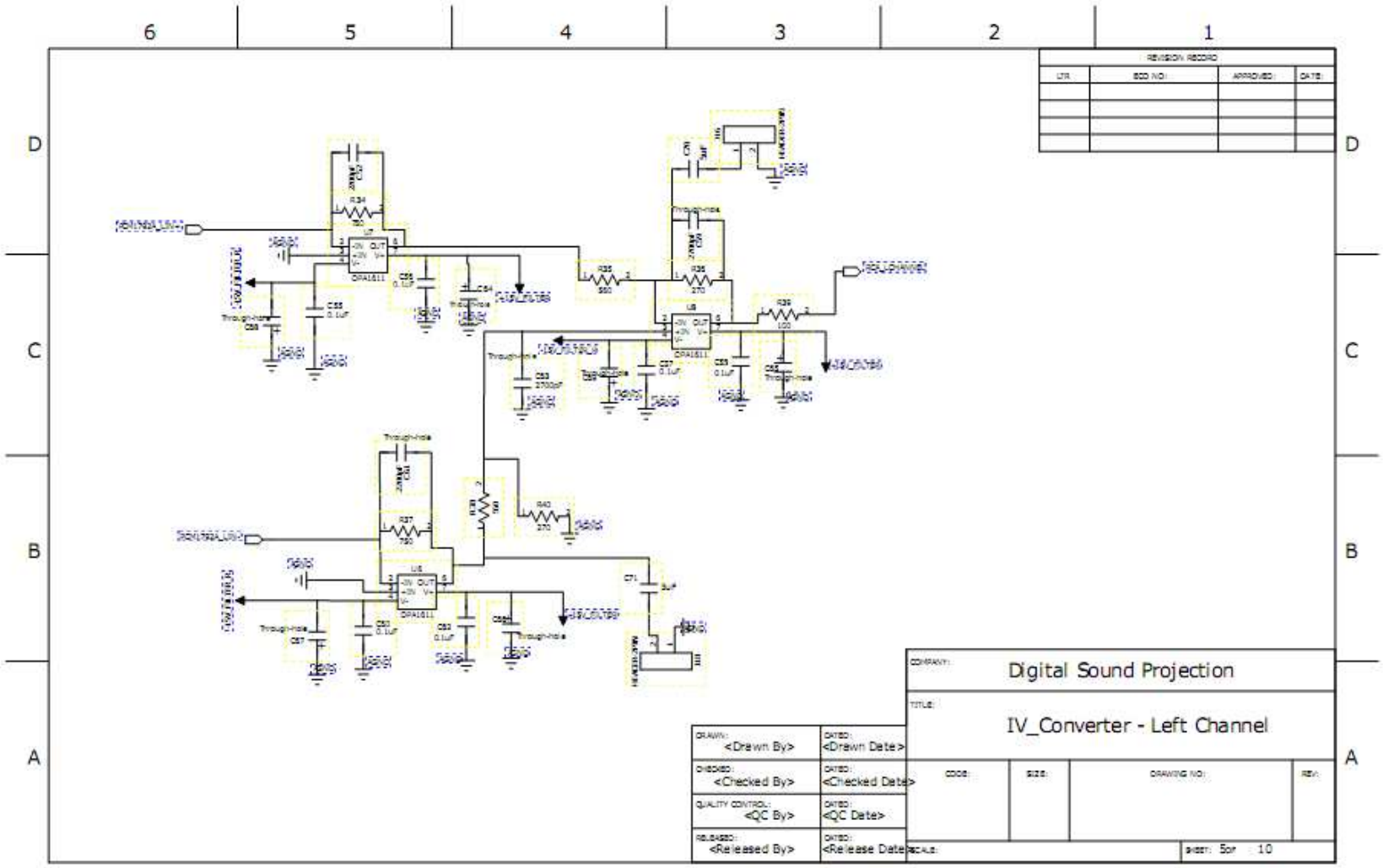


Figure C-1.5: IV Converter Output Stage – Left Channel Schematic

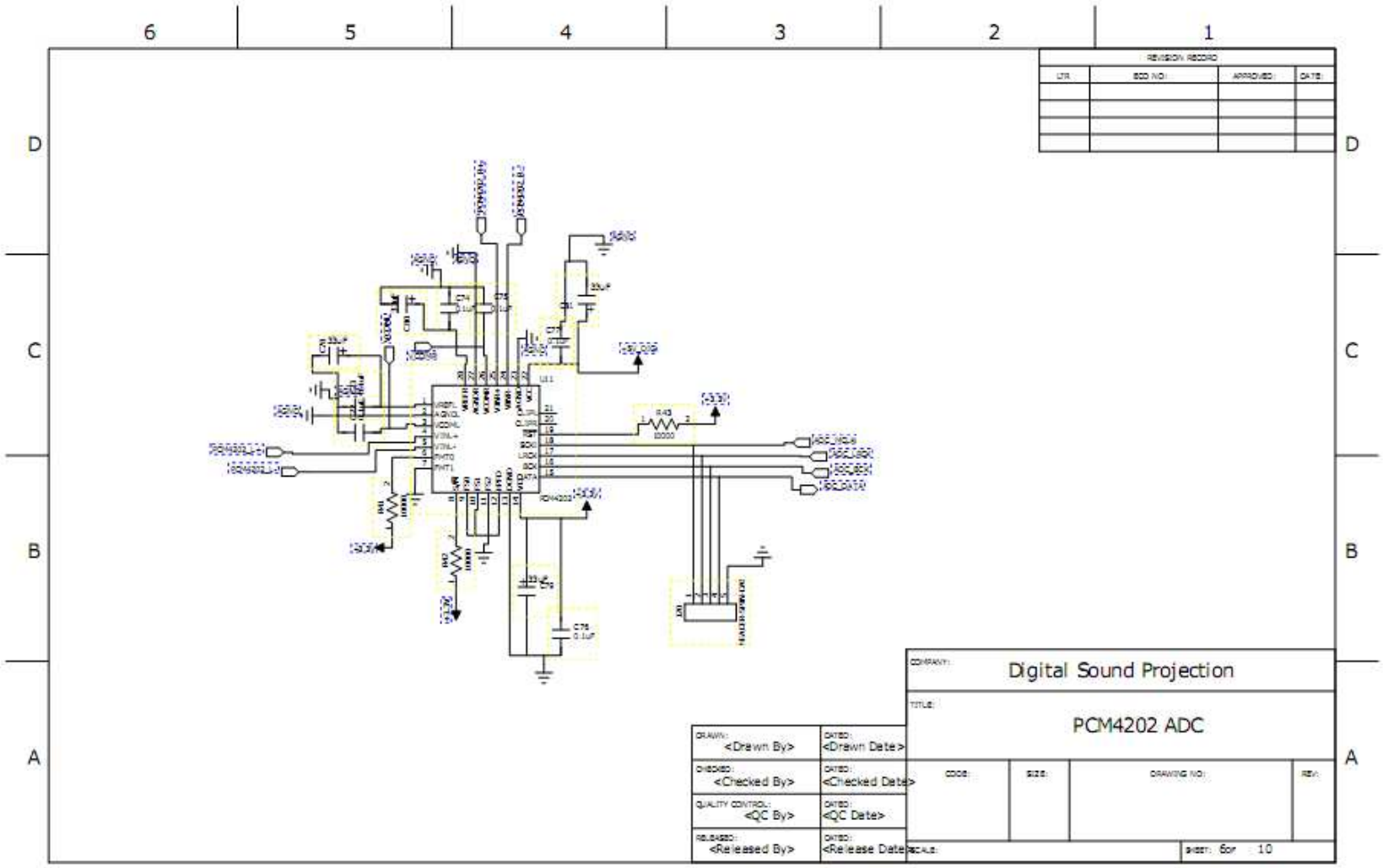


Figure C-1.6: PCM4202 Analog to Digital Converter Schematic

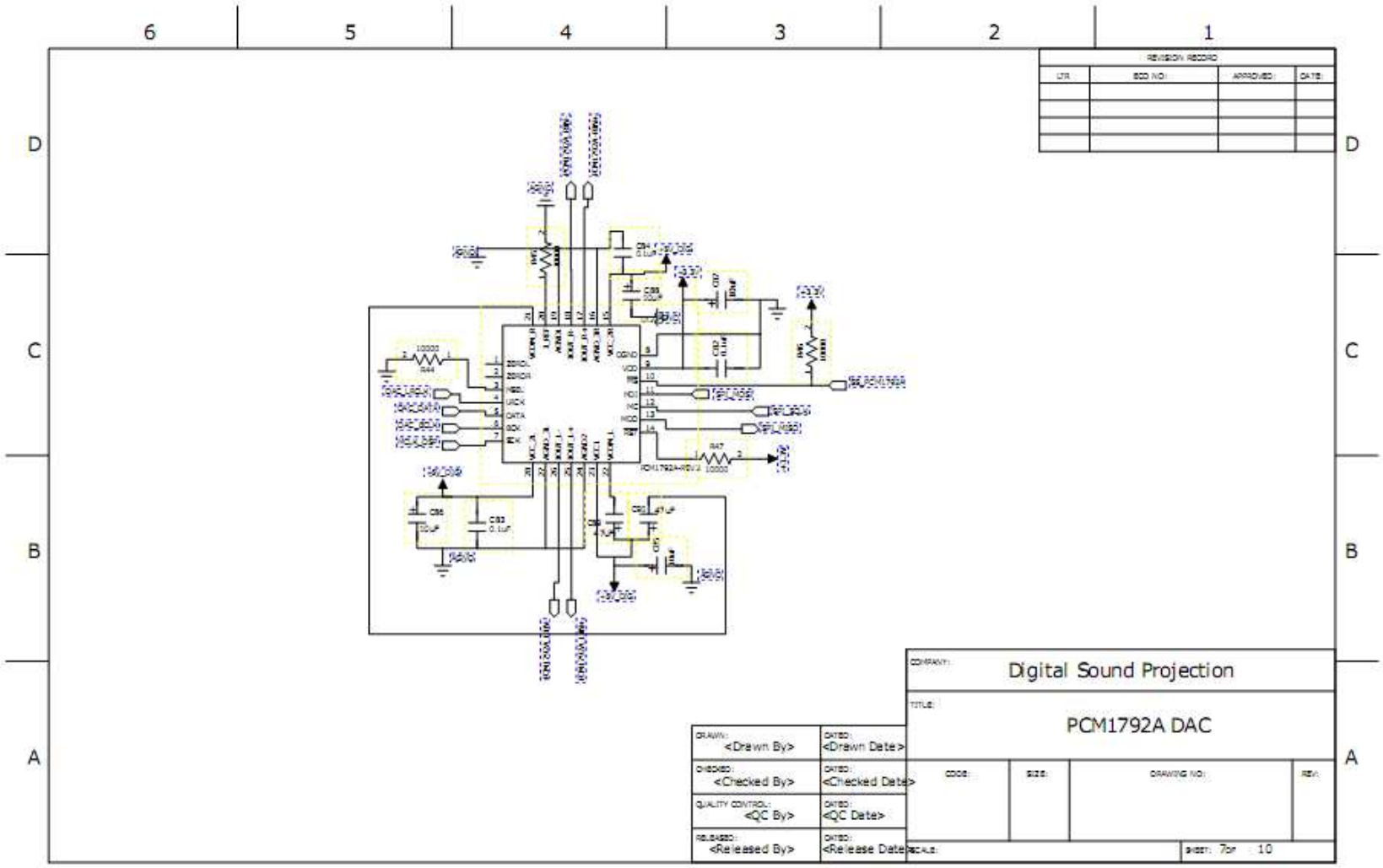


Figure C-1.7: PCM1792A Digital to Analog Converter Schematic

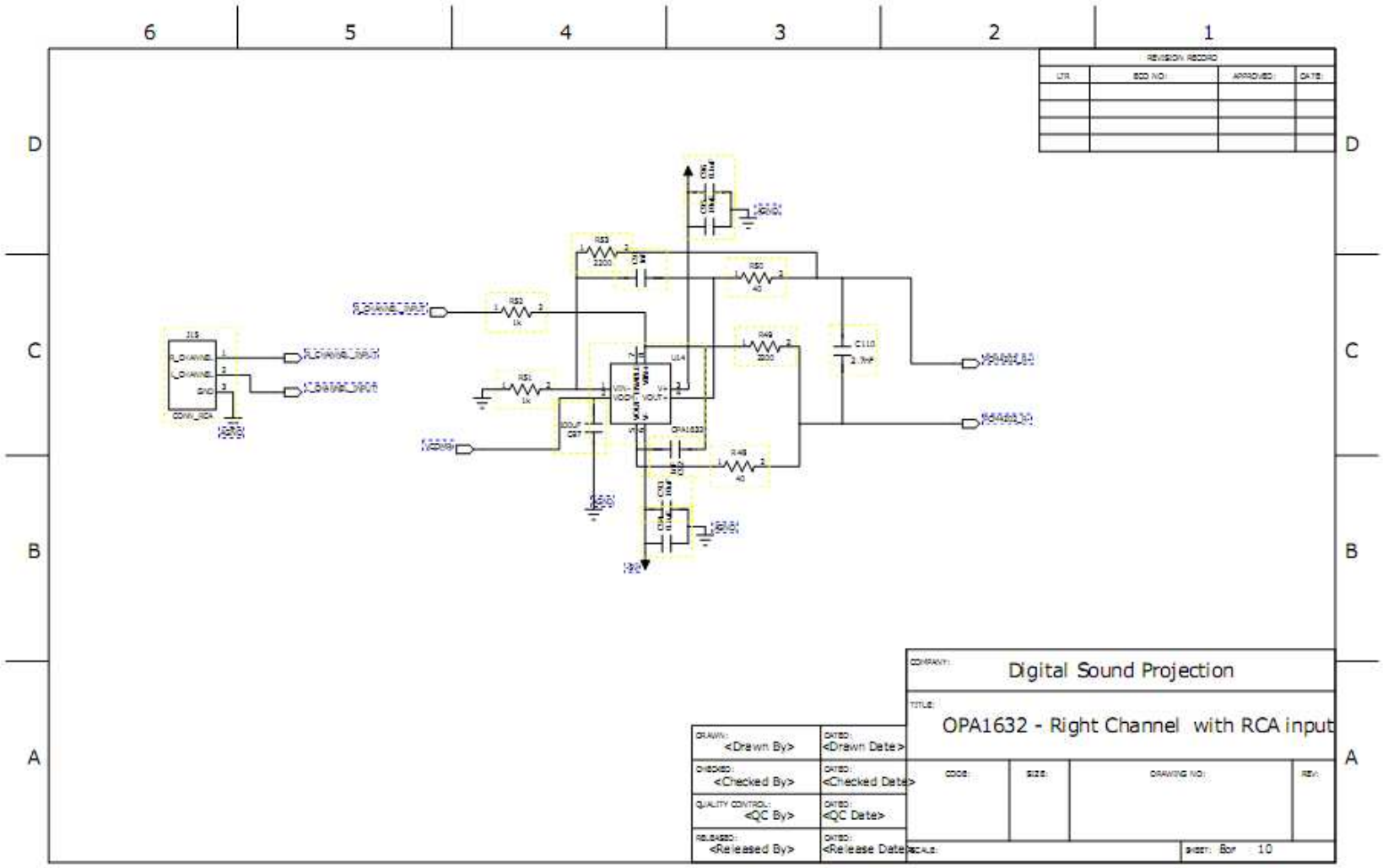


Figure C-1.8: OPA1632 Input Stage – Right Channel Schematic

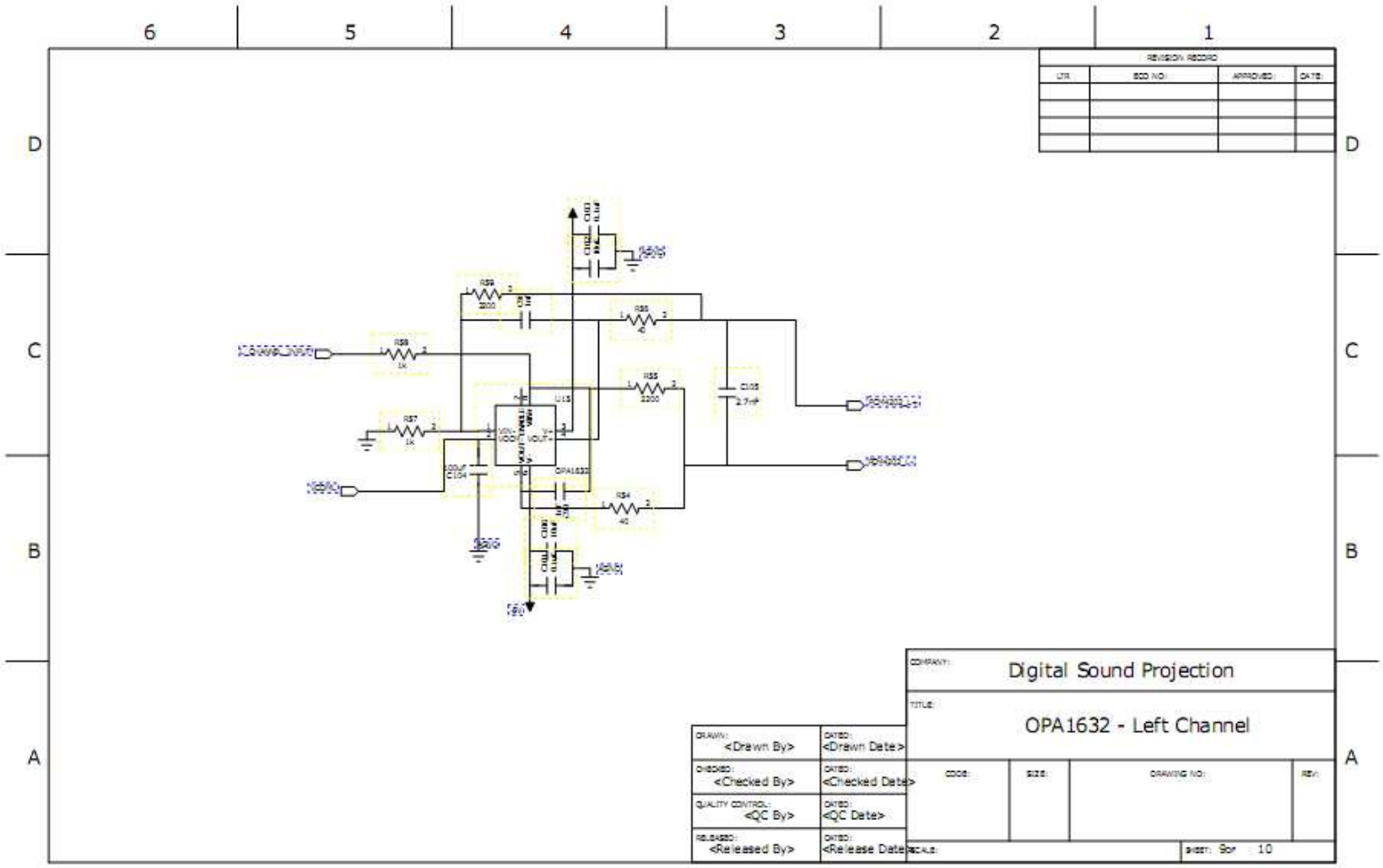


Figure C-1.9: OPA1632 Input Stage – Left Channel Schematic

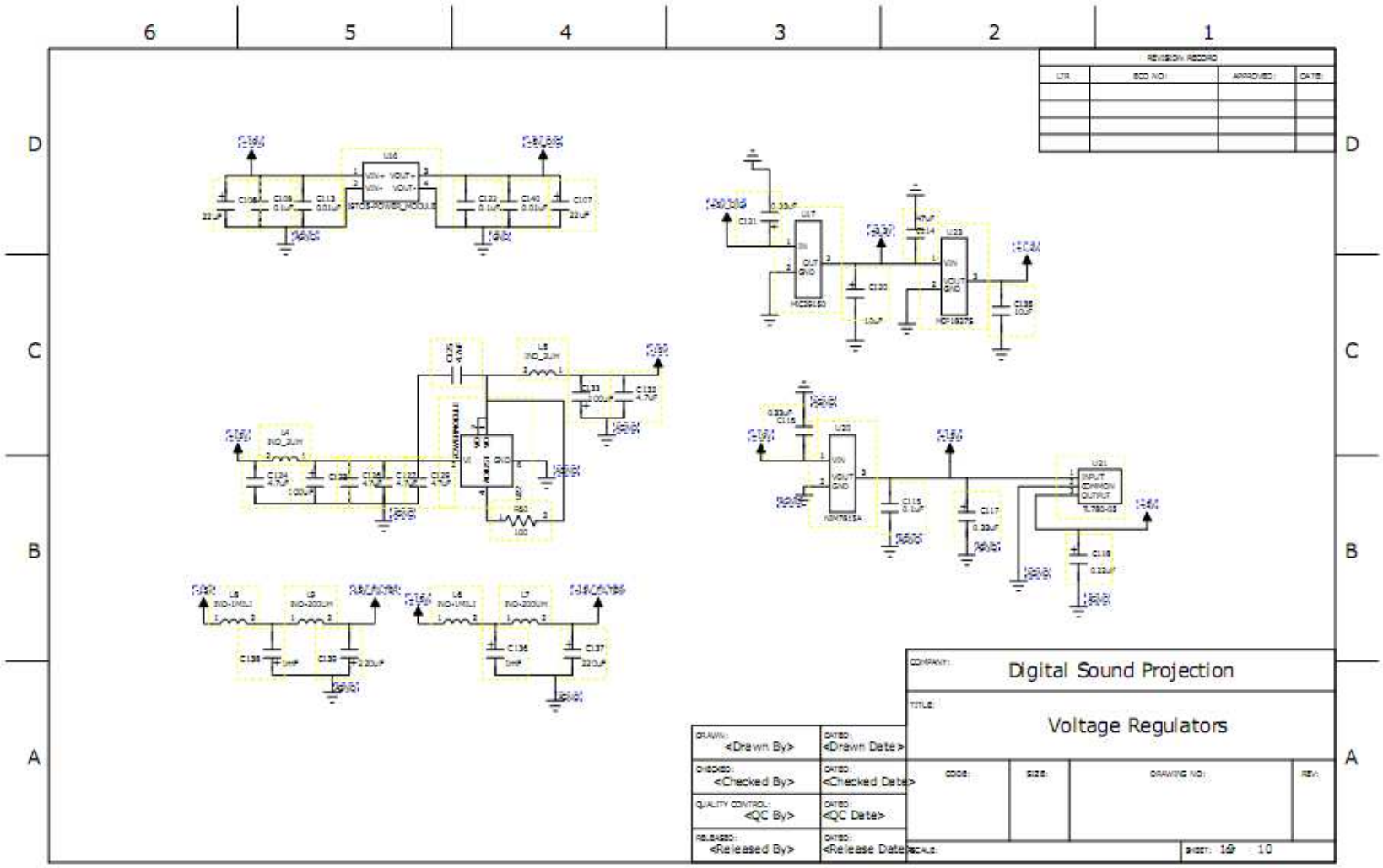


Figure C-1.10: Voltage Regulators Schematic

C.2 Transmitter Schematics

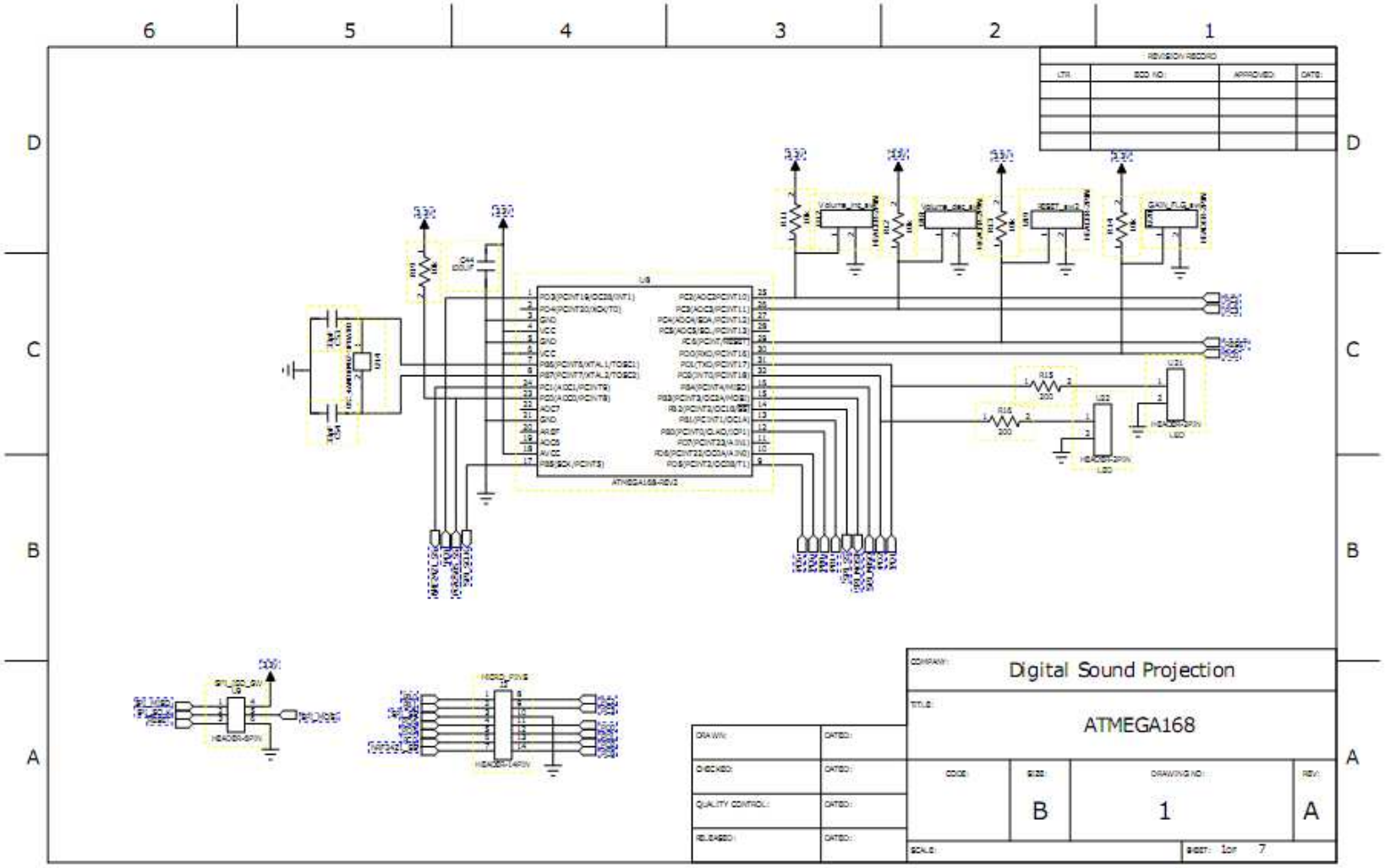


Figure C-2.1: ATmega168 Microcontroller Schematic

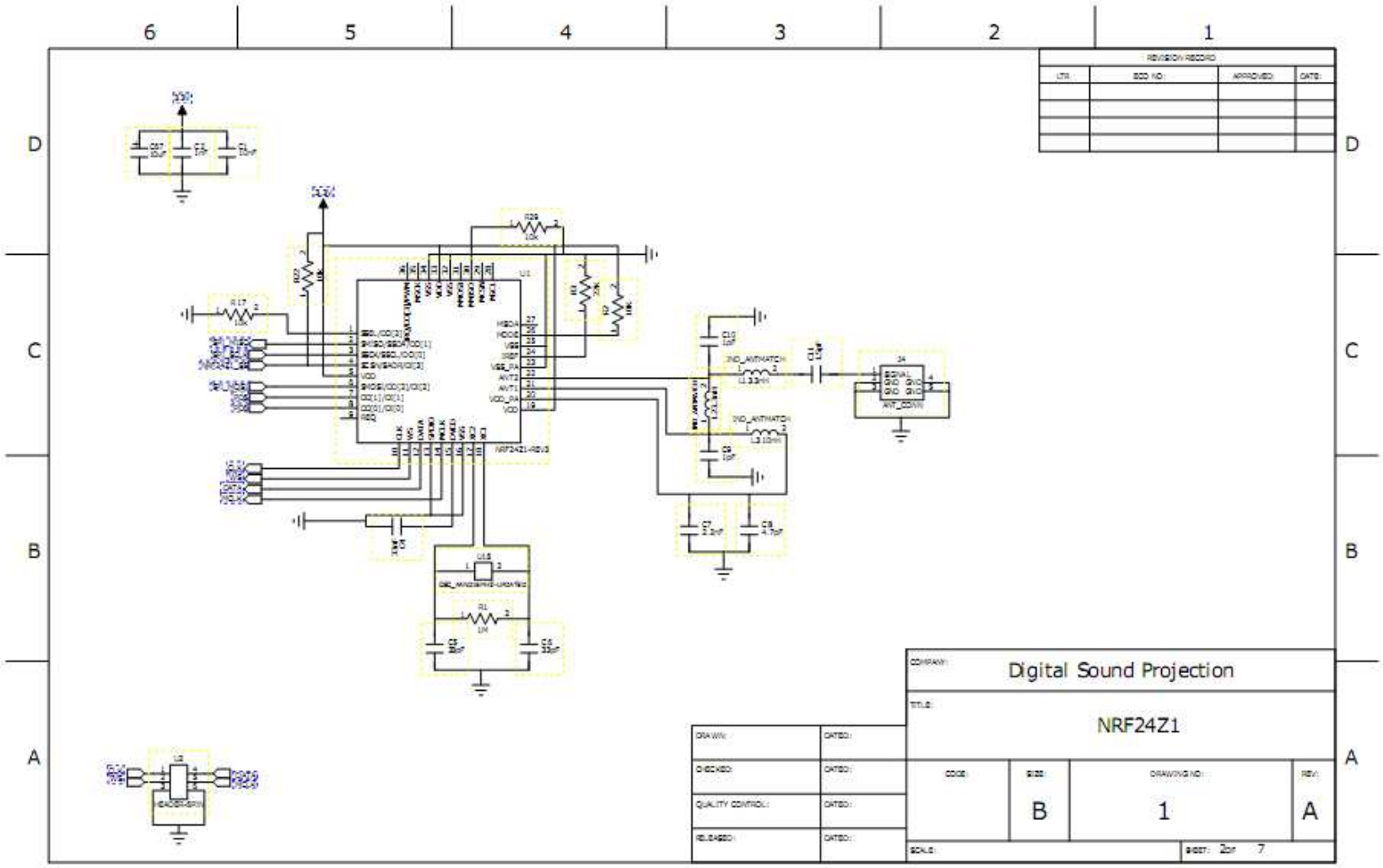


Figure C-2.2: nRF24Z1 Transceiver Schematic

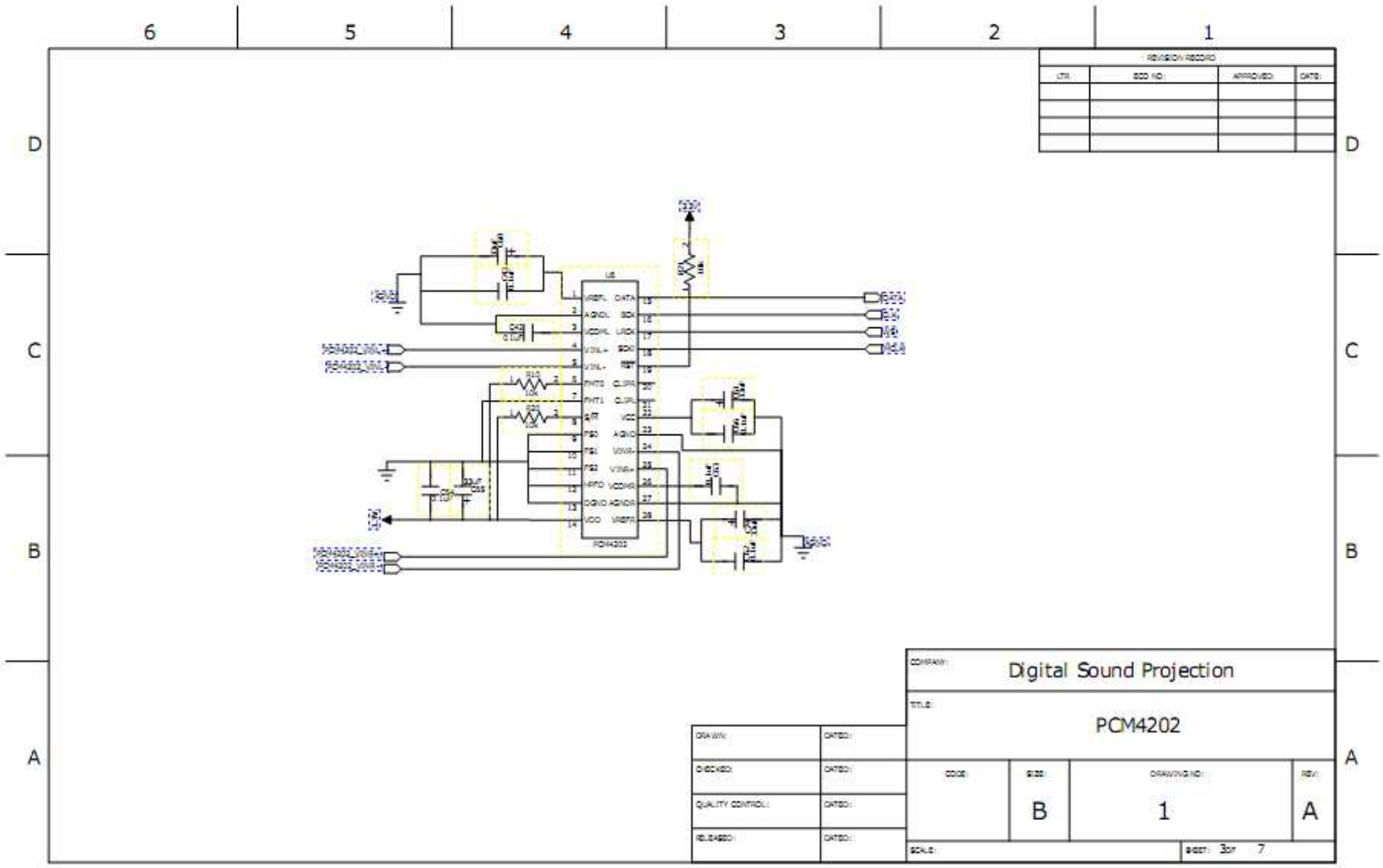


Figure C-2.3: PCM4202 Analog to Digital Converter Schematic

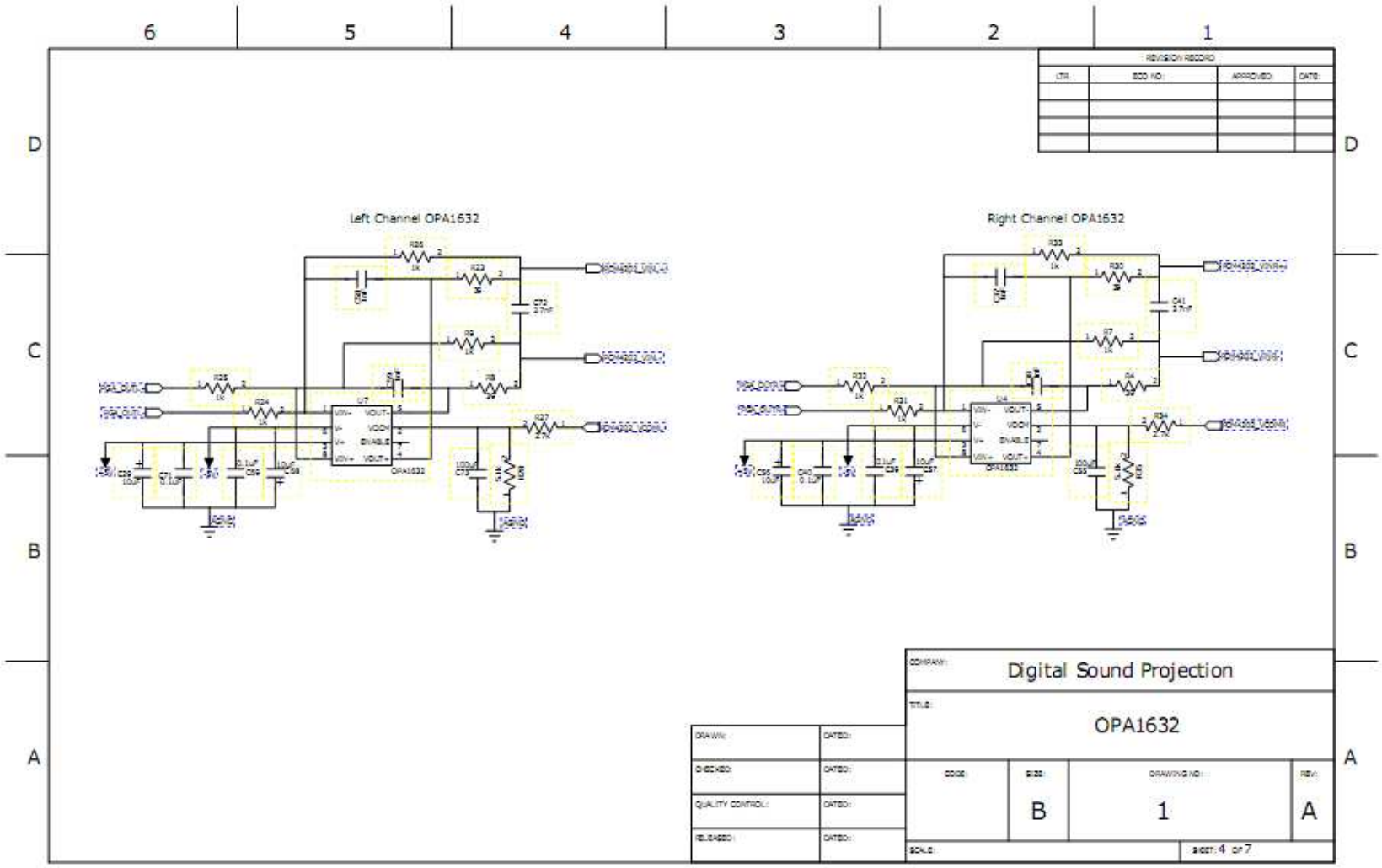


Figure C-2.4: OPA1632 Operational Amplifier Schematic

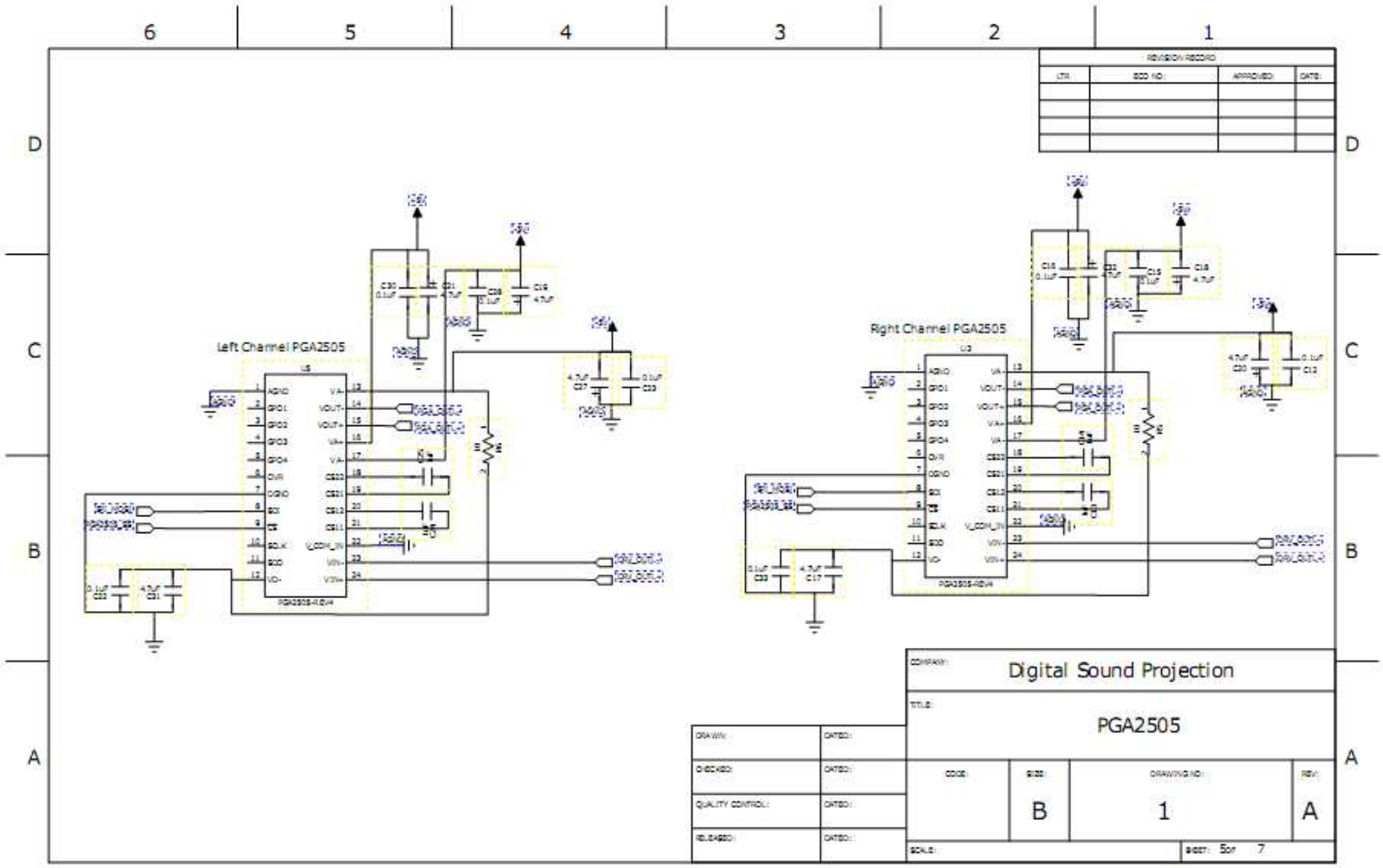


Figure C-2.5: PGA2505 Microphone Preamplifier Schematic

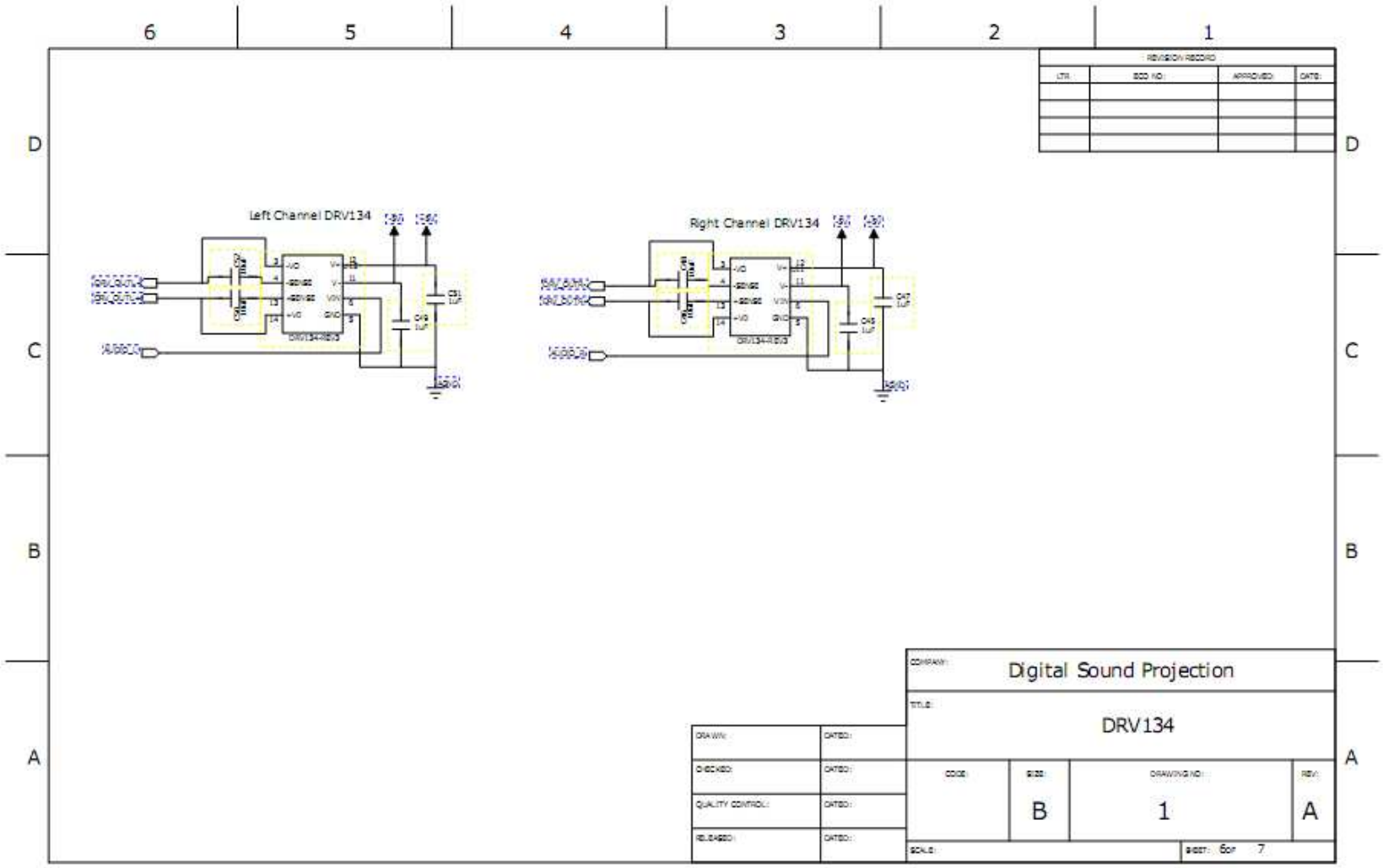


Figure C-2.6: DRV134 Differential Generator Schematic

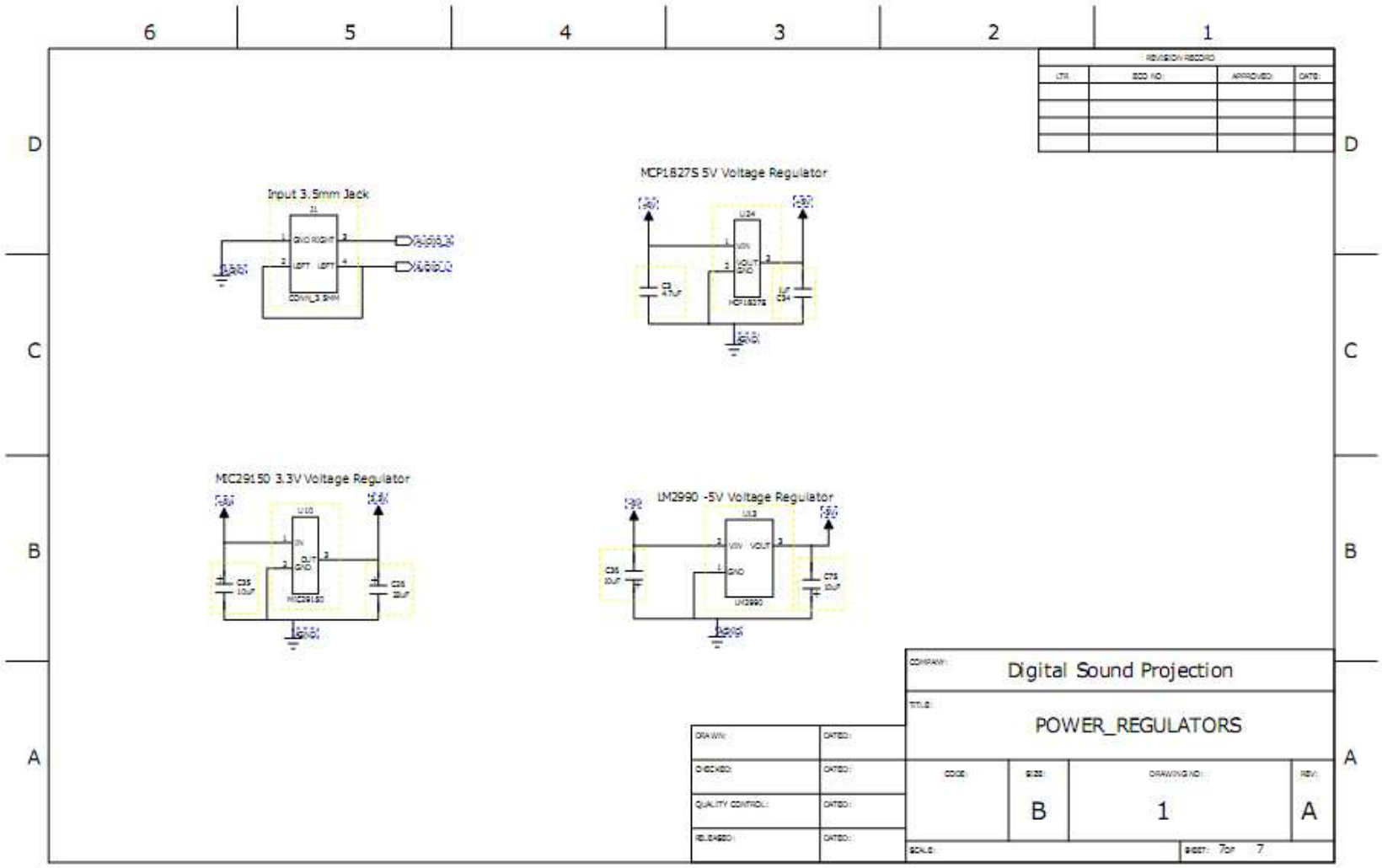


Figure C-2.7: Linear Voltage Regulators Schematic

Appendix D: PCB Layout Top and Bottom Copper

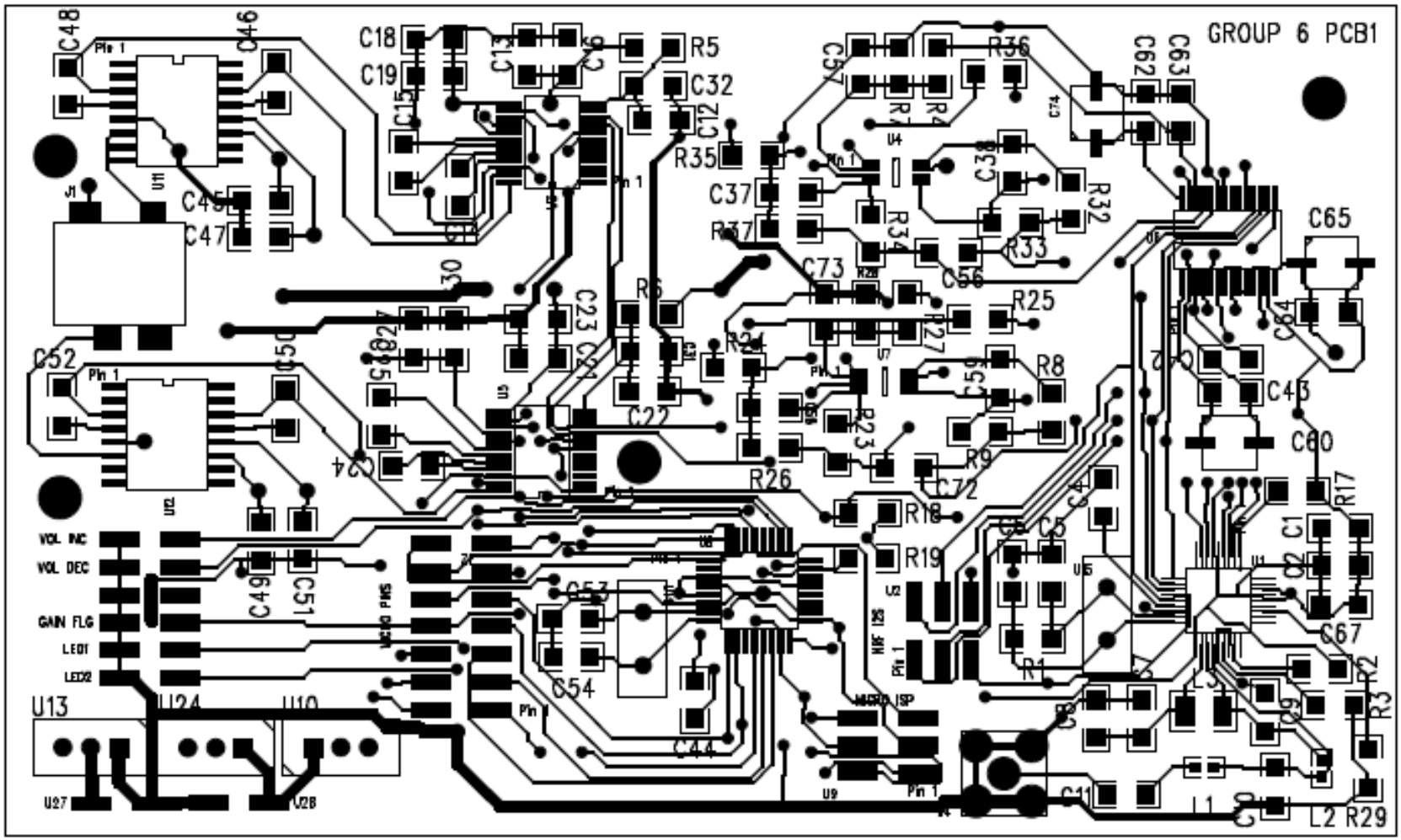


Figure D-1: Transmitter Top Copper and Silkscreen Layout

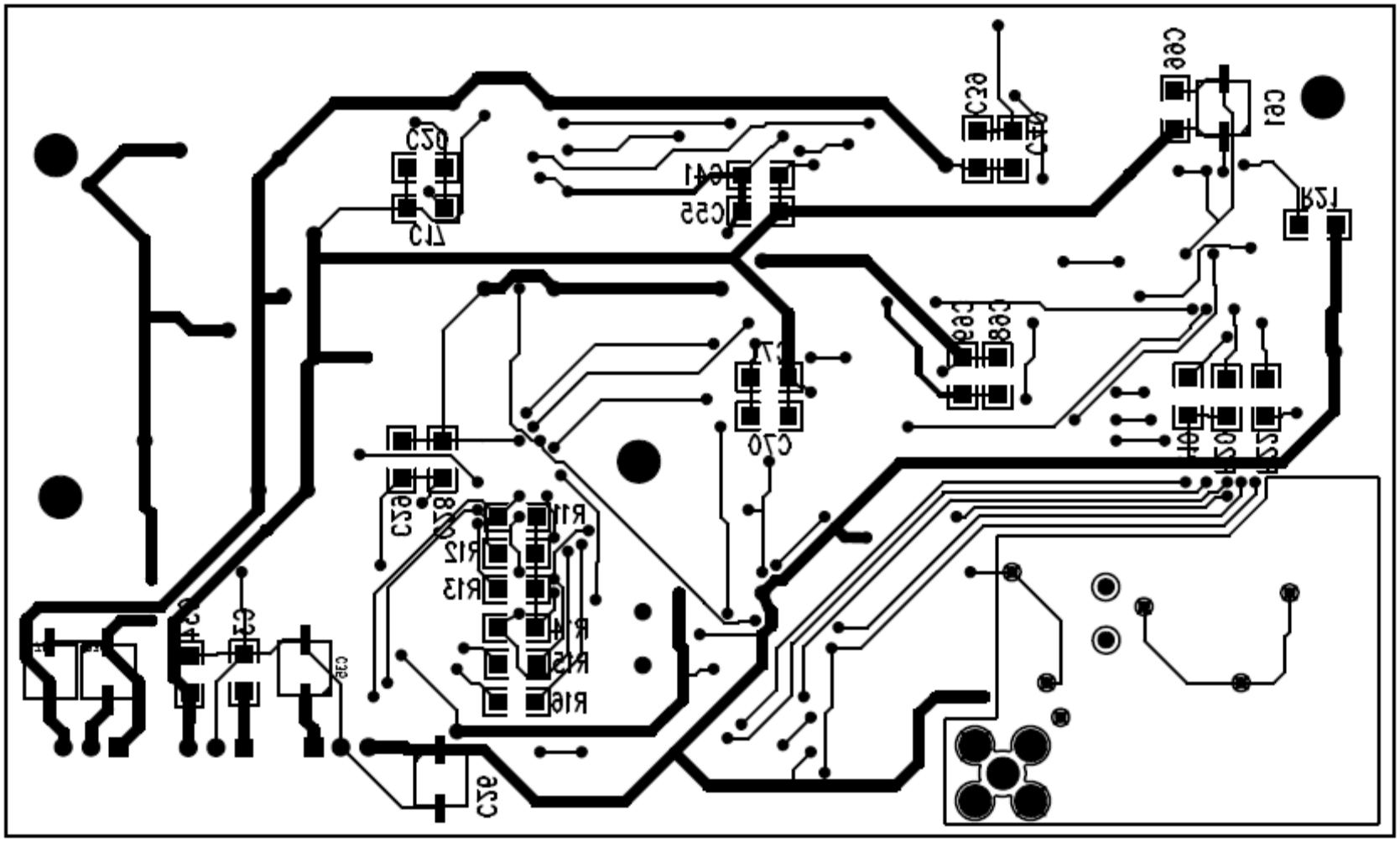


Figure D-2: Transmitter Bottom Copper and Silkscreen Layout

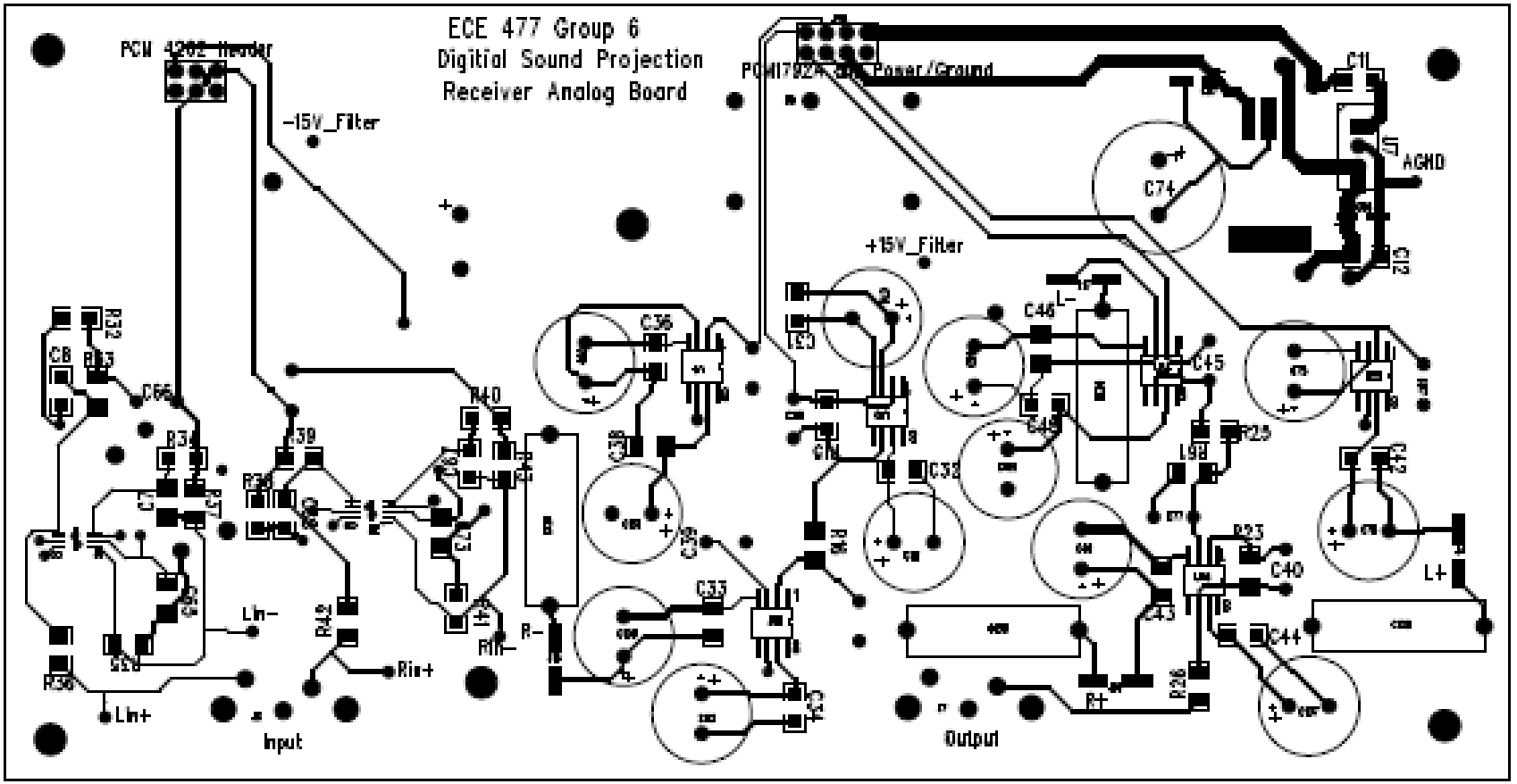


Figure D-3: Receiver Analog Board Top Copper and Silkscreen Layout

Figure D-4: Receiver Analog Board Power Layer Copper Layout

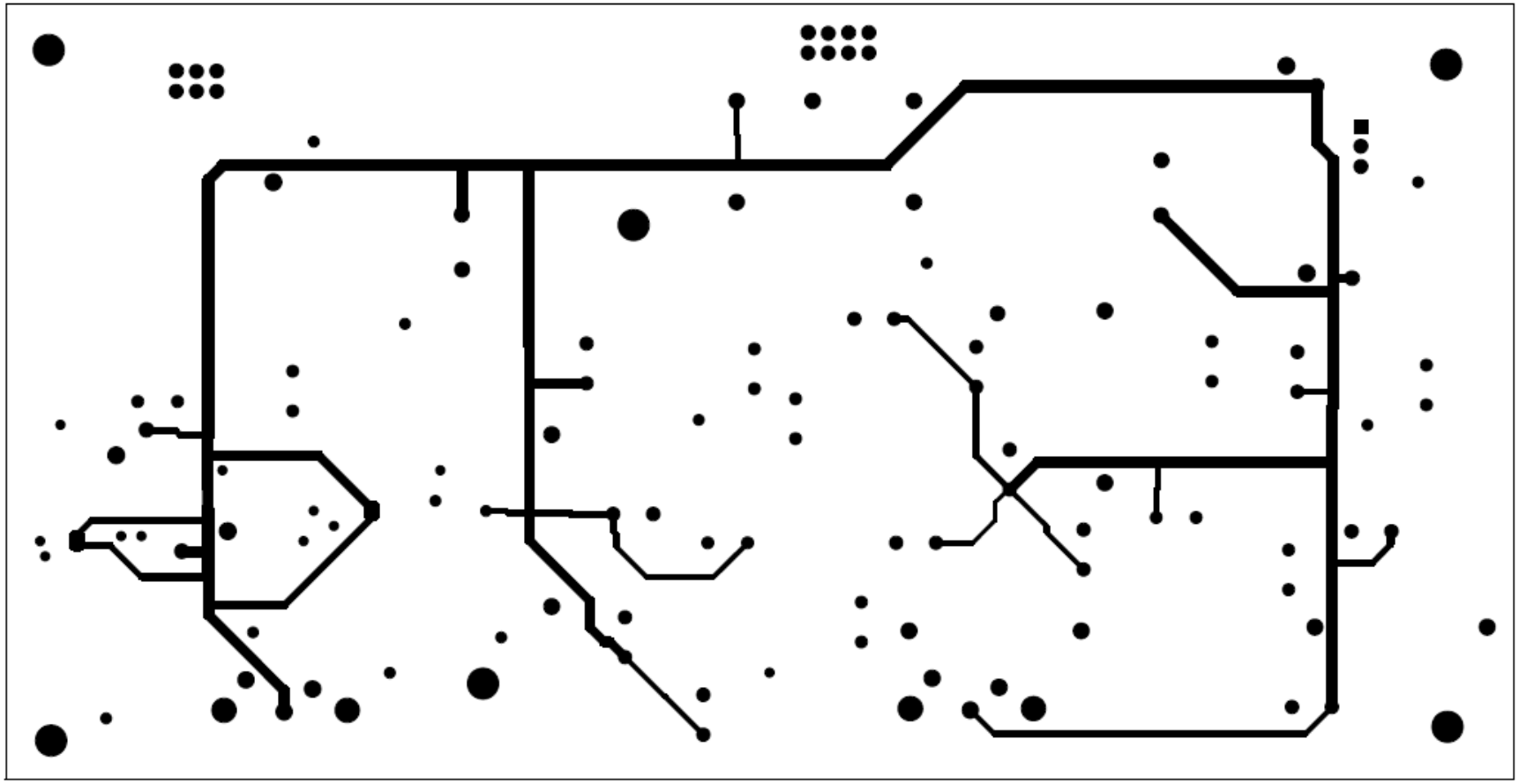


Figure D-5: Receiver Analog Board Ground Layer Copper Layout

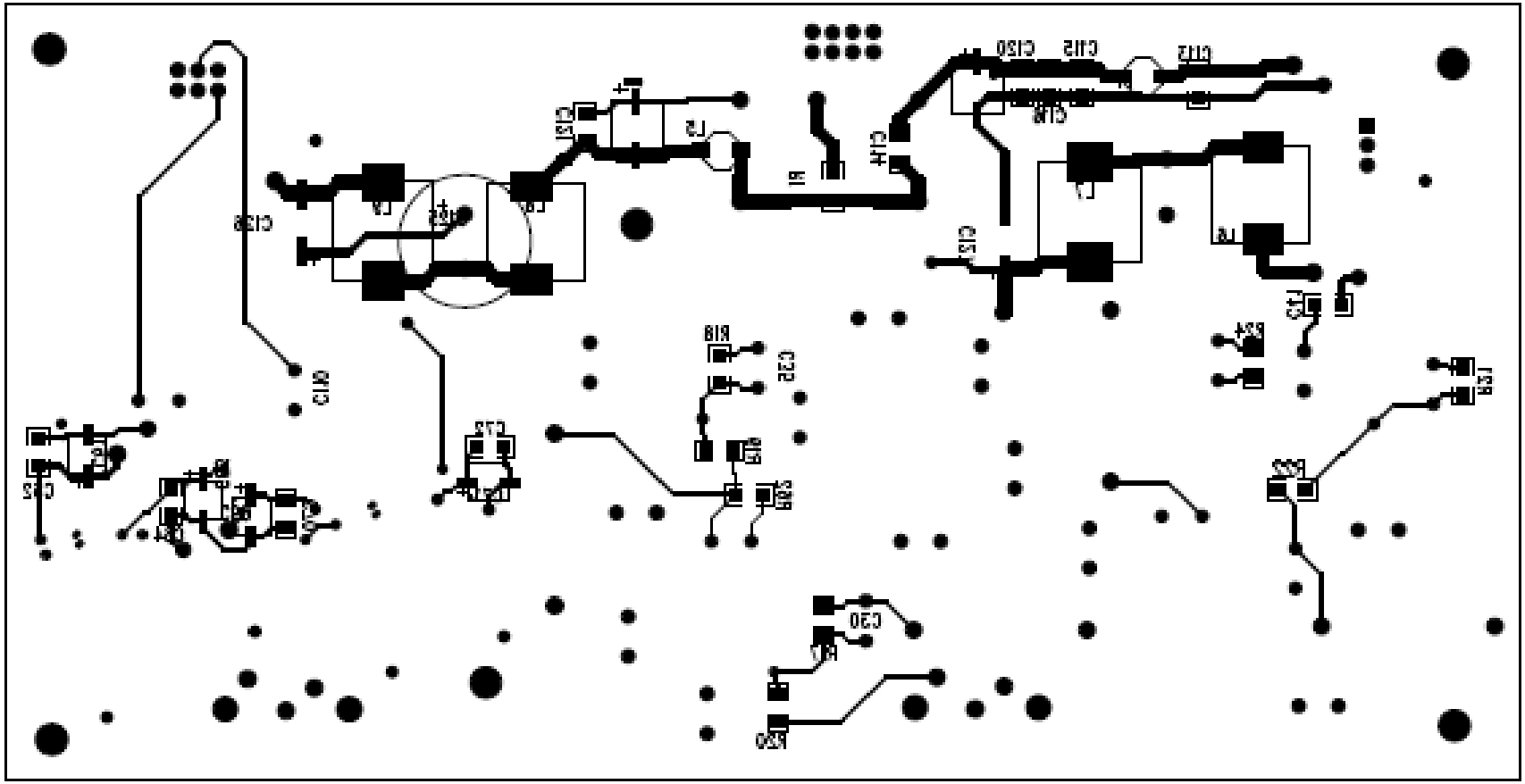


Figure D-6: Receiver Analog Board Bottom Copper and Silkscreen Layout

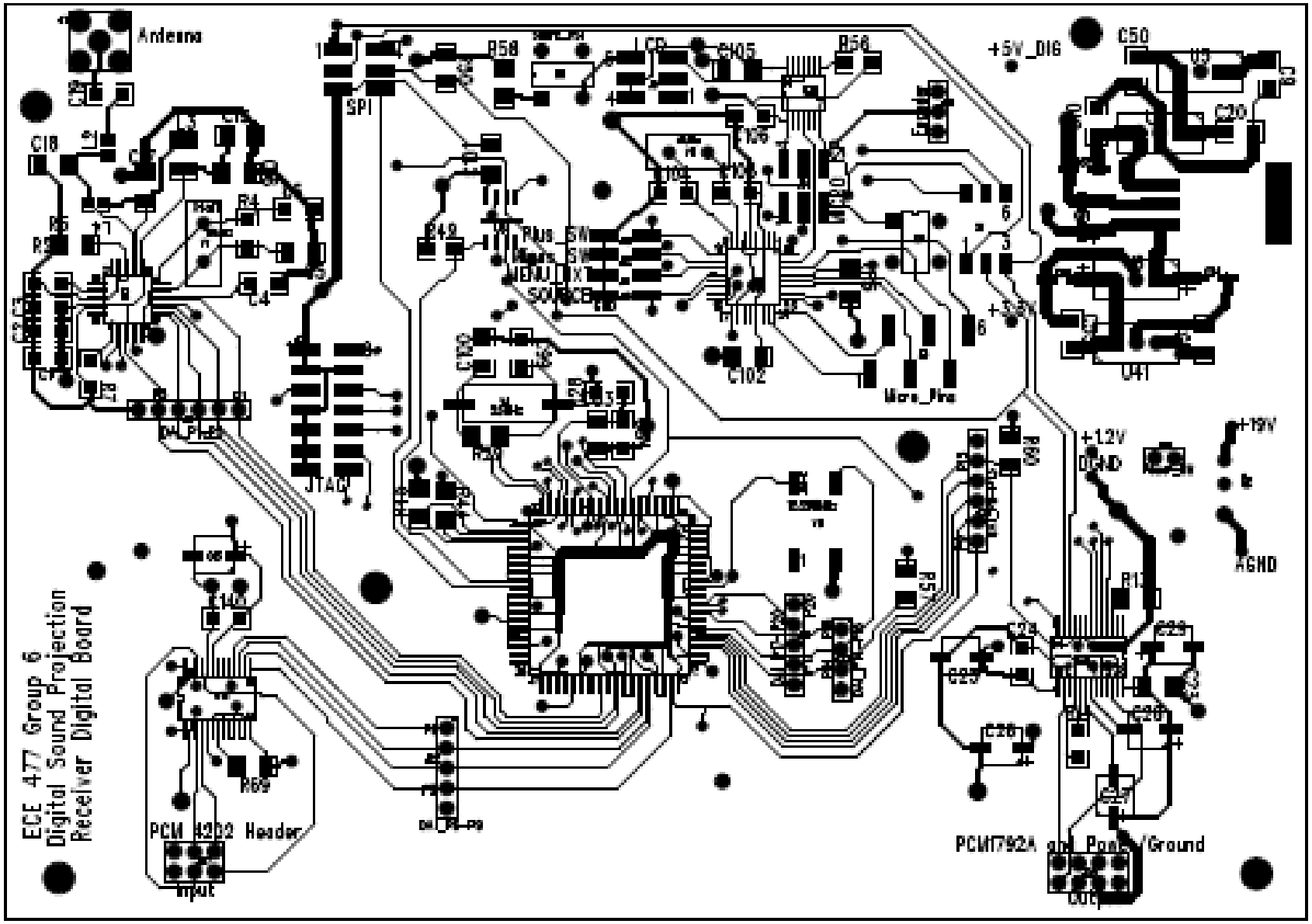


Figure D-7: Receiver Digital Board Top Copper and Silkscreen Layout

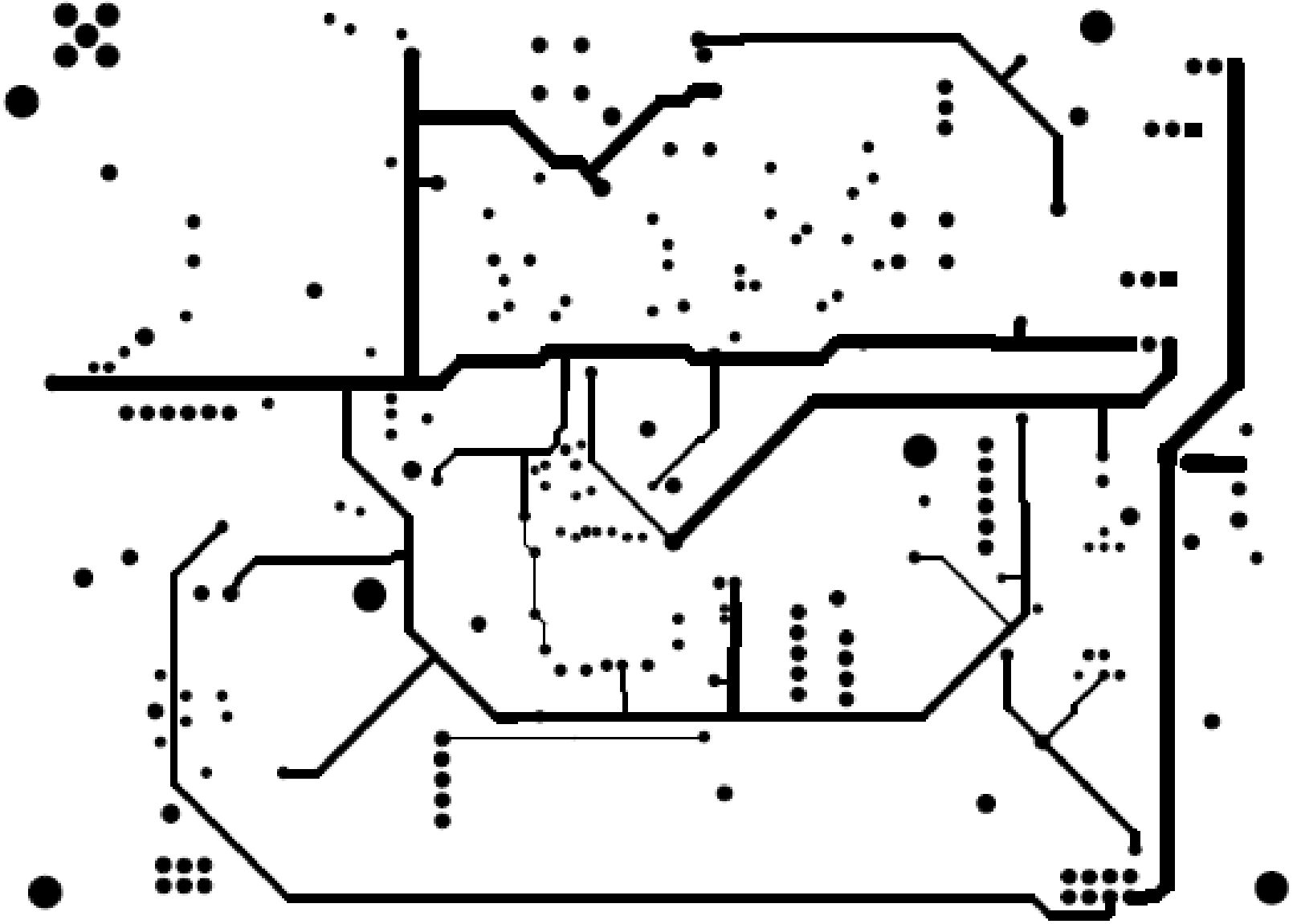


Figure D-8: Receiver Digital Board Power Layer Copper Layout

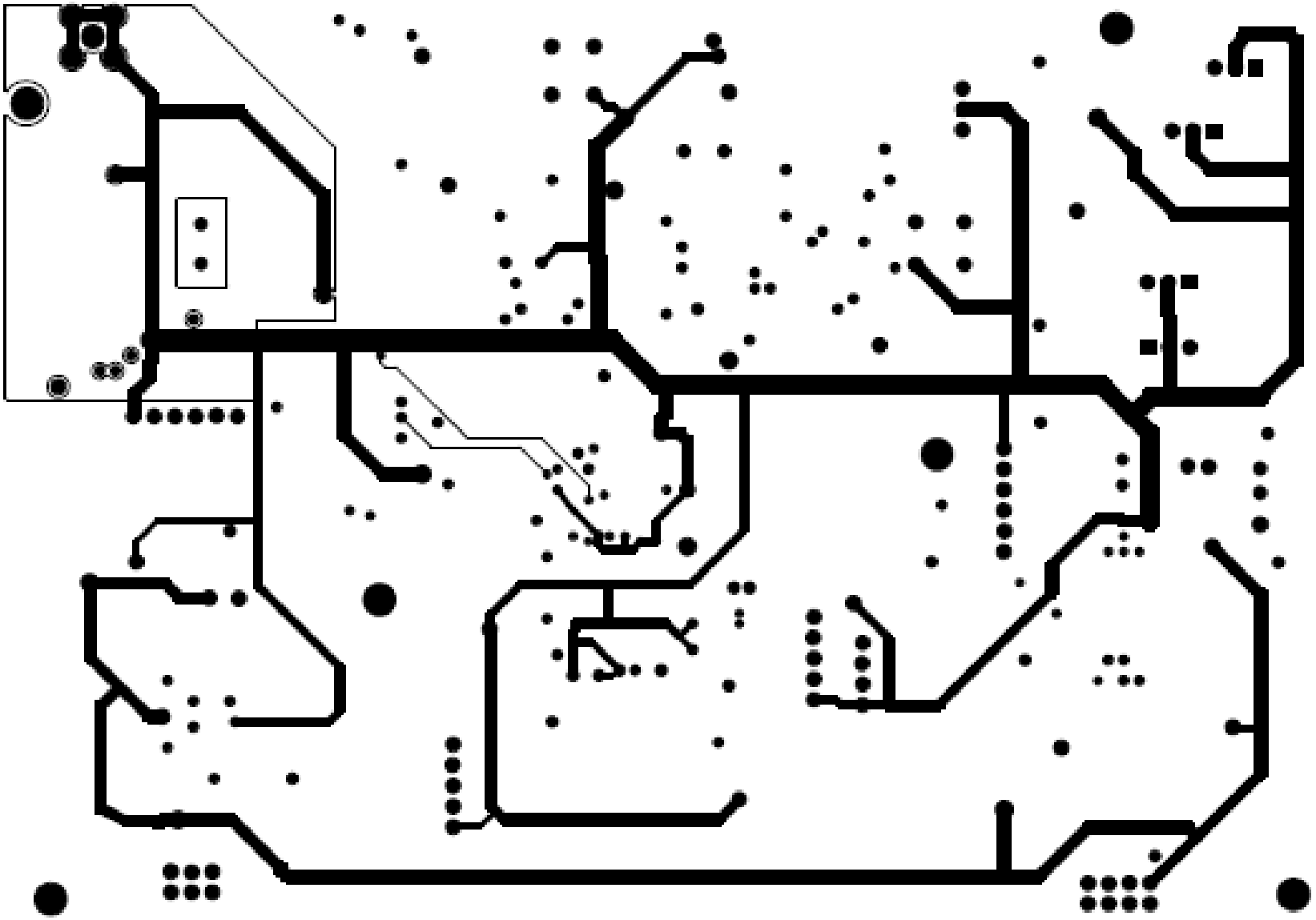


Figure D-9: Receiver Digital Board Ground Layer Copper Layout

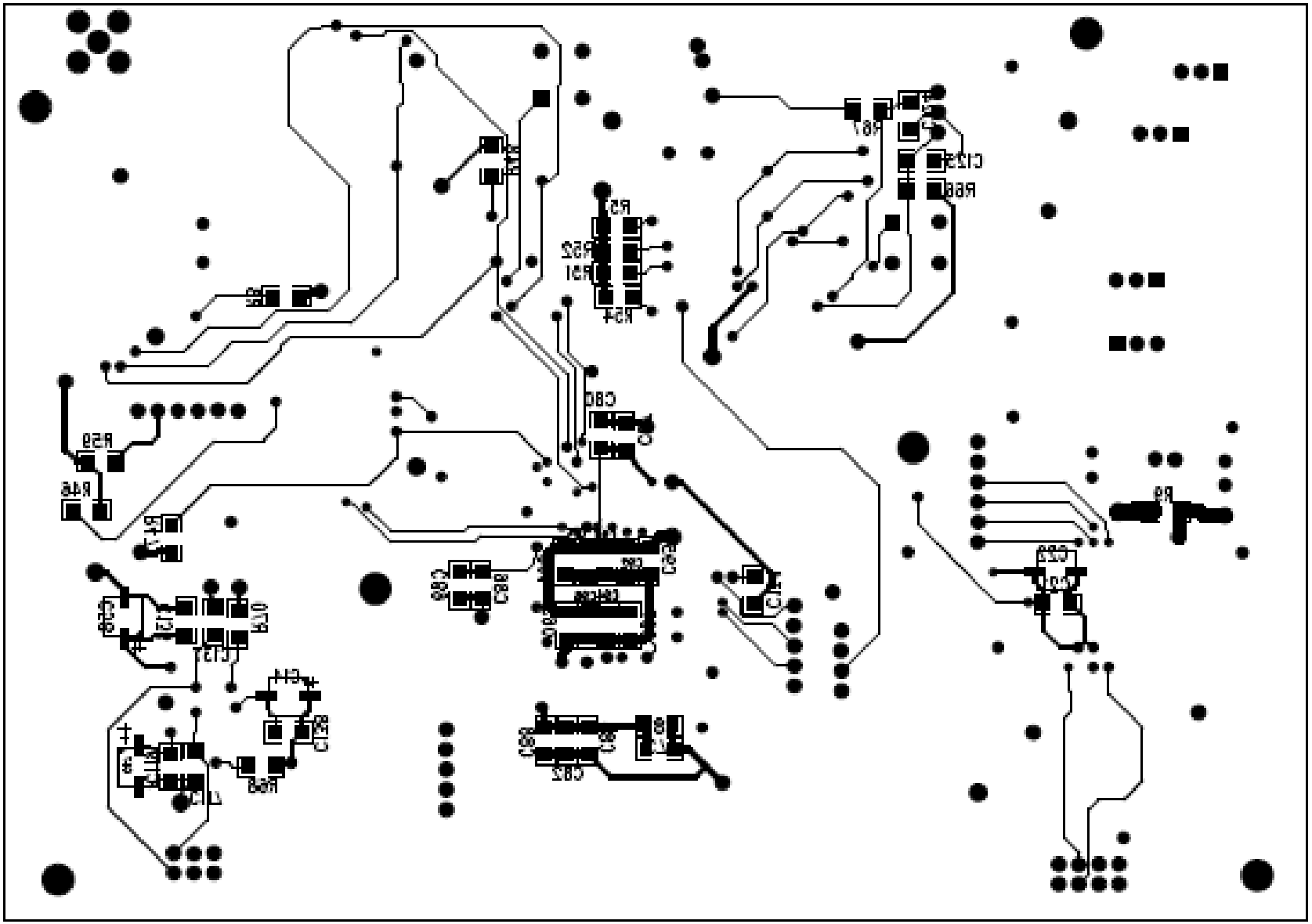


Figure D-10: Receiver Digital Board Bottom Copper and Silkscreen Layout

Appendix E: Parts List Spreadsheet

Table E-1: Transmitter Parts List

Vendor	*Manufacturer*	*Part No.*	*Description*	*Unit Cost*	*Qty*	*Total Cost*
Digi-Key	Texas Instruments	DRV134	Single to Differential Generator	$5.46	2	$10.92
Digi-Key	Texas Instruments	PGA2505	Microphone Pre-amplifier	$11.99	2	$23.98
Digi-Key	Texas Instruments	OPA1632	Fully Differential I/O Audio Amplifier	$5.46	2	$10.92
Digi-Key	Texas Instruments	PCM4202	118dB SNR Stereo Audio ADC	$17.25	1	$17.25
Digi-Key	Atmel Corporation	ATmega168-20AU	General Purpose Microcontroller	$4.32	1	$4.32
Semiconductor Store	Nordic Semiconductor	nRF24Z1	Wireless Audio Transceiver	$6.00	1	$6.00
Digi-Key	Microchip	MCP1827S	Low Voltage LDO 5V Regulator	$1.50	1	$1.50
Digi-Key	National Semiconductor	LM2990	Negative LDO -5V Regulator	$3.58	1	$3.58
Digi-Key	Micrel	MIC29150	High-Current LDO 3.3V Regulator	$3.13	1	$3.13
All-Battery	Tenergy	11106	NiMH Rechargeable Battery Pack	$7.99	2	$15.98
Radioshack	Radioshack	270-1806	ABS Project Enclosure 6x4x2”	$4.99	1	$4.99
Digi-Key	Panasonic	P1.00KFTR-ND	1206 Resistors, Miscellaneous	$0.01	34	$0.34
Digi-Key	CTS	CTX402-ND	Oscillator, 4MHz	$0.78	2	$1.56
Digi-Key	TDK Corporation	445-1592-2-ND	1206 Capacitors, Miscellaneous	$0.03	64	$1.92
Digi-Key	Panasonic	PCE3849TR-ND	Aluminum Surface Mount Capacitors, Miscellaneous	$0.05	12	$0.60
Digi-Key	CUI	CP1-3514SJCT-ND	3.5mm Audio Jack Connector	$0.65	1	$0.65
Semiconductor Store	Semiconductor Store	CON-RPSMA-RA	SMA Connector	$2.32	1	$2.32
L-Com	L-Com	HG2402RD-RSF	2.4GHz Antenna	$5.99	1	$5.99
Digi-Key	Panasonic	PCD1910CT-ND	0402 Inductor	$0.12	2	$0.24
Digi-Key	TDK Corp	445-1505-1-ND	1210 Inductor	$0.29	1	$0.29
Digi-Key	Molex	WM17435-ND	Surface Mount Header, 2 Pin	$0.53	15	$7.95
Radioshack	Radioshack	275-1548	Push Buttons, SPST	$0.87	2	$1.74
Radioshack	Radioshack	275-664	DPDT Switch	$4.99	2	$9.98
Transmitter Total Cost						**$136.35**

Table E-2: Receiver Parts List

Vendor	*Manufacturer*	*Part No.*	*Description*	*Unit Cost*	*Qty*	*Total Cost*
Digi-Key	Analog Devices	ADSP-21262	Digital Signal Processor	$27.30	1	$27.30
Digi-Key	Texas Instruments	PCM4202	Analog to Digital Converter	$17.25	1	$17.25
Digi-Key	Texas Instruments	PCM1792A	Digital to Analog Converter	$12.68	1	$12.68
Digi-Key	Atmel Corporation	ATMEGA168-20AU	General Purpose Microcontroller	$4.32	1	$4.32
Semiconductor Store	Nordic Semiconductor	nRF24Z1	Wireless Audio Transceiver	$6.00	1	$6.00
Digi-Key	Texas Instruments	OPA1611	Audio Operational Amplifier	$5.46	6	$32.76
Digi-Key	Texas Instruments	OPA1632	Audio Operational Amplifier	$5.46	2	$32.76
Digi-Key	Panasonic	EVE-GA1F2024B	12mm Square GS Encoder	$1.52	1	$1.52
Digi-Key	Atmel Corporation	M25P80	8Mb SPI Flash	$1.82	1	$1.82
Digi-Key	Microchip	MCP1827S	3.3V to 1.2V Linear Regulator	$1.50	1	$1.50
Digi-Key	Micrel	MIC29150	5V to 3.3V Linear Regulator	$3.13	1	$3.13
Digi-Key	National Semiconductor	LM340T-15-ND	19V to 15V Linear Regulator	$1.07	1	$1.07
Digi-Key	Texas Instruments	PT4142A	19V to 5V Power Module	$55.17	1	$55.17
Digi-Key	Texas Instruments	TXB0104	Voltage Level Translator	$0.89	1	$0.89
Digi-Key	Texas Instruments	296-20518-ND	15V to -15V Power Module	$27.50	1	$27.50
Digi-Key	Molex	WM17435-ND	Surface Mount Header, 2 Pin	$0.53	45	$23.85
Digi-Key	E-Switch	EG4422-ND	DIP Switch, Micro	$0.78	1	$0.78
Digi-Key	Panasonic	P12354S-ND	Single Switch	$1.82	1	$1.82
Digi-Key	CTS	CTX402-ND	Oscillator, 4MHz	$0.78	2	$1.56
Digi-Key	Abracon	535-10219-1-ND	Oscillator, 12.288MHz	$0.41	1	$0.41
Digi-Key	ECS Inc.	ECS-8FX	Oscillator, 25MHz	$1.50	1	$1.50
Semiconductor Store	Semiconductor Store	CON-RPSMA-RA	SMA Connector	$2.32	1	$2.32
The Cable Company	DH Labs Silver Sonic	CM-R1 RCA Socket (pair)	RCA Connector	$24.00	2	$48.00
Digi-Key	Panasonic	ECQ-P1H272GZ	Capacitor, ECQP 2.7nF	$0.39	6	$2.34
Digi-Key	Nichicon	493-3194-ND	KZ-Series Capacitors	$0.50	20	$10.00
Digi-Key	TDK Corporation	445-1592-2-ND	1206 Capacitors, Miscellaneous	$0.03	98	$2.94

Digi-Key	Panasonic	PCE3849TR-ND	Aluminum Surface Mount Capacitors, Miscellaneous	$0.05	19	$0.95
Digi-Key	Panasonic	P1.00KFTR-ND	1206 Resistors, Miscellaneous	$0.01	59	$0.59
Digi-Key	Panasonic	PCD1910CT-ND	0402 Inductor	$0.12	2	$0.24
Digi-Key	TDK Corp	445-1505-1-ND	1210 Inductor	$0.29	1	$0.29
Digi-Key	Coiltronics	513-1453-1-ND	Inductor, 2uH	$0.99	2	$1.98
Digi-Key	Bourns	SRR1240-221KCT-ND	Inductor, 200uH	$1.09	2	$2.18
Digi-Key	TDK	445-3826-1-ND	Inductor, 1mH	$1.80	2	$3.60
Crystal Fontz	Crystal Fontz	CFA634-TMC-KS	LCD	$65.00	1	$65.00
Digi-Key	Panasonic	P10860-ND	Rotary Encoder	$1.52	1	$1.52
Radioshack	Radioshack	275-1549	Push Button, SPDT	$3.99	3	$11.97
Digi-Key	Tyco Electronics	450-1666-ND	Power Switch	$4.46	1	$4.46
Digi-Key	Bud Industries	AC-413	Aluminum Sheet Metal Box	$32.20	1	$32.20
Digi-Key	Bud Industries	BPA-1523	Aluminum Sheet Metal Bottom	$10.70	1	$10.70
Receiver Total Cost						**$392.62**

Appendix F: FMECA Worksheet

Table F-1: FMECA Worksheet for the Transmitter Power Supply

Failure No.	Failure Mode	Possible Causes	Failure Effects	Method of Detection	Criticality	Remarks
A1	No voltage output	Linear regulator failure	Device does not turn on	No display on LCD screen	Medium	
A2	Excessive voltage output	Linear regulator failure	Overdrives digital components	Input/output malfunction	High	Overheating
A3	Noisy voltage	Filtering capacitors malfunctioning	Noisy audio input	Observation.	Low	Probe the +-5V outputs

Table F-2: FMECA Worksheet for the Transmitter Audio Input

Failure No.	Failure Mode	Possible Causes	Failure Effects	Method of Detection	Criticality	Remarks
B1	No sound input	Singled to differential Op-Amp malfunctioning	No sound input	Observation	High	excessive heat from OPA1632
B2	Irregular sound input	Singled to differential Op-Amp malfunctioning	Differences in loudness on left and right channels	Observation	High	excessive heat from OPA1632

Table F-3: FMECA Worksheet for the Transmitter Analog to Digital Converter

Failure No.	Failure Mode	Possible Causes	Failure Effects	Method of Detection	Criticality	Remarks
C1	No sound input	Power failure, Damaged IC	No digital audio sent	Observation	Medium	Check the output data from nRF24Z1 buffer
C2	Irregular sound input	Damaged IC, I2S misbehavior	Distorted data input	Observation	Medium	Check the output data from nRF24Z1 buffer

Table F-4: FMECA Worksheet for the Transmitter Transceiver

Failure No.	Failure Mode	Possible Causes	Failure Effects	Method of Detection	Criticality	Remarks
D1	Discontinuous digital data	Low wireless signal strength due to passive components	Discontinuous Audio output	Observation	Low	Change current transmitter location, improve antenna strength
D2	Fail to establish connection	Same as above, Damaged IC	No data transmitted from nRF24Z1	LED indicator	Medium	Change current transmitter location, improve antenna strength
D3	No reading from nRF24Z1	Software error, Damaged IC	Unable to communicate to nRF24Z1	Observation	Medium	Damaged IC

Table F-5: FMECA Worksheet for the Transmitter Microcontroller and LED Indicators

Failure No.	Failure Mode	Possible Causes	Failure Effects	Method of Detection	Criticality	Remarks
E1	Fail to accept volume adjustments	Software error, ATmega168 malfunctioning	User interface malfunctioning	Observation	Low	
E2	Devices indicator malfunctioning	LED malfunctioning, ATmega168 malfunctioning	User lose the indication of the transmitter status	Observation	Medium	
E3	No output from ATmega168	ATmega168 malfunctioning	No digital audio output, no LED indicator	Observation	Medium	Transmitter malfunctioning

Table F-6: FMECA Worksheet for the Receiver Power Supply

Failure No.	Failure Mode	Possible Causes	Failure Effects	Method of Detection	Criticality	Remarks
F1	No voltage output	Linear voltage regulator failure	Device does not turn on	No display on LCD screen	Medium	
F2	Excessive voltage output	Voltage control resistor failure	Overdrives digital components, potential of damaging IC	Input/output malfunction	High	Overheating, switching power module malfunctioning
F3	Noisy voltage	Filtering capacitors malfunctioning	Noisy audio output	Observation.	Low	Probe the +-15V and filter outputs

Table F-7: FMECA Worksheet for the Receiver Audio Input and Output

Failure No.	Failure Mode	Possible Causes	Failure Effects	Method of Detection	Criticality	Remarks
G1	No sound output	I/V tri-amp converter malfunctioning	No sound output	Observation	Medium	Check 7-pin bus data
G2	Distorted sound output	I/V tri-amp converter malfunctioning	Distorted sound effect	Observation	Medium	Check 7-pin bus data
G3	No sound input	Singled to differential Op-Amp malfunctioning	No sound input	Observation	High	excessive heat from OPA1632, Check 6-pin bus data
G4	Irregular sound input	Singled to differential Op-Amp malfunctioning	Differences in loudness on left and right channels	Observation	High	excessive heat from OPA1632, Check 6-pin bus data

Table F-8: FMECA Worksheet for the Receiver Analog to Digital Converter and Digital to Analog Converter

Failure No.	Failure Mode	Possible Causes	Failure Effects	Method of Detection	Criticality	Remarks
H1	No sound output	Power failure Damaged IC	Current output remains constant	Observation	Medium	Check DAI pins
H2	Distorted sound output	I2S misbehavior	Distorted current output	Observation	Medium	Restart the device and reset the SHARC
H3	No sound input	Power failure Damaged IC	No digital audio data generated	Observation	Medium	Plot the input from SHARC
H4	Irregular sound input	I2S misbehavior	Distorted data input	Observation	Medium	Plot the input from SHARC

Table F-9: FMECA Worksheet for the Receiver Transceiver

Failure No.	Failure Mode	Possible Causes	Failure Effects	Method of Detection	Criticality	Remarks
I1	Discontinuous digital data	Low wireless signal strength from passive components	Discontinuous Audio output	Observation	Low	Change current transmitter location, improve antenna strength
I2	Fail to establish connection	Same as above, Damaged IC	No data received from nRF24Z1	LED indicator	Medium	Change current transmitter location, improve antenna strength
I3	No reading from nRF24Z1	Software error Damaged IC	Unable to communicate to nRF24Z1	Observation	Medium	Damaged IC, try to reboot then reset SHARC

Table F-10: FMECA Worksheet for the Receiver Microcontroller and LCD

Failure No.	Failure Mode	Possible Causes	Failure Effects	Method of Detection	Criticality	Remarks
J1	No backlight on LCD	LCD reaches lifecycle	Display failure	Observation	Medium	Replace the LCD display module
J2	Display error on LCD	ATmega168 is trapped in a particular state	Display random characters on the screen	Observation	Low	Reset the ATmega168
J3	Fail to accept user inputs	Software error, ATmega168 malfunctioning	User interface malfunctioning	Observation	Medium	
J4	LCD lights up but no display	ATmega168 malfunctioning	User interface malfunctioning	Observation	Medium	SHARC will not be able to read input parameters from the microcontroller

Table F-11: FMECA Worksheet for the Receiver SHARC DSP with Flash Programmer

Failure No.	Failure Mode	Possible Causes	Failure Effects	Method of Detection	Criticality	Remarks
K1	SHARC does not load startup program	Reset circuitry malfunction	No Sound input/output	Observation	Medium	Manually press the reset button
K2	SHARC malfunctioning	Power issue Broken pins	No or distorted sound output	Observation	High	Might cause the power supply section to overheat
K3	Flash does not send programmed data to SHARC on startup	Software error, flash programmer is damaged	No Sound input/output	Observation	Medium	Program the SHARC with JTAG programmer to troubleshoot

Appendix G: Flowchart for Main Program

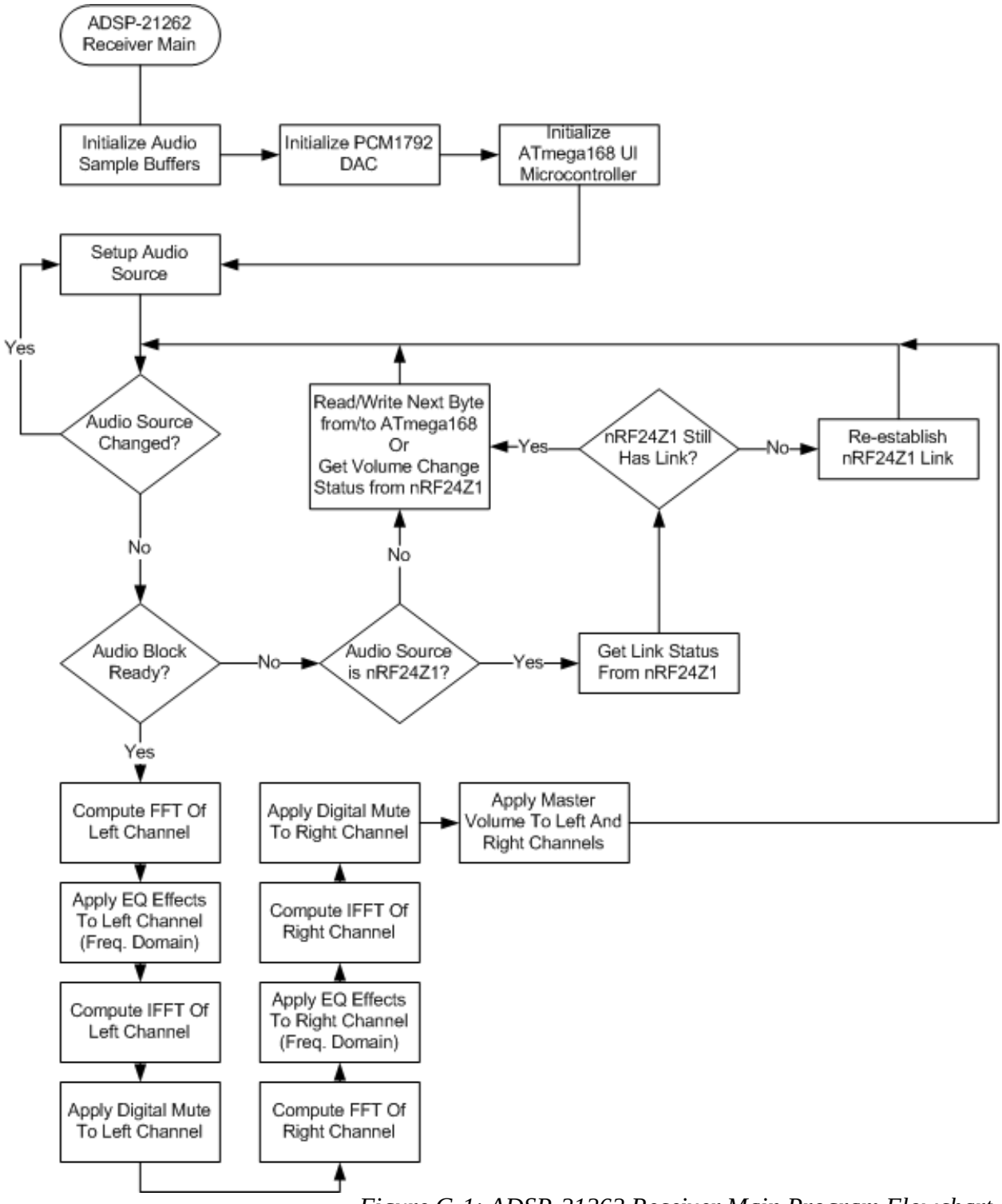


Figure G-1: ADSP-21262 Receiver Main Program Flowchart

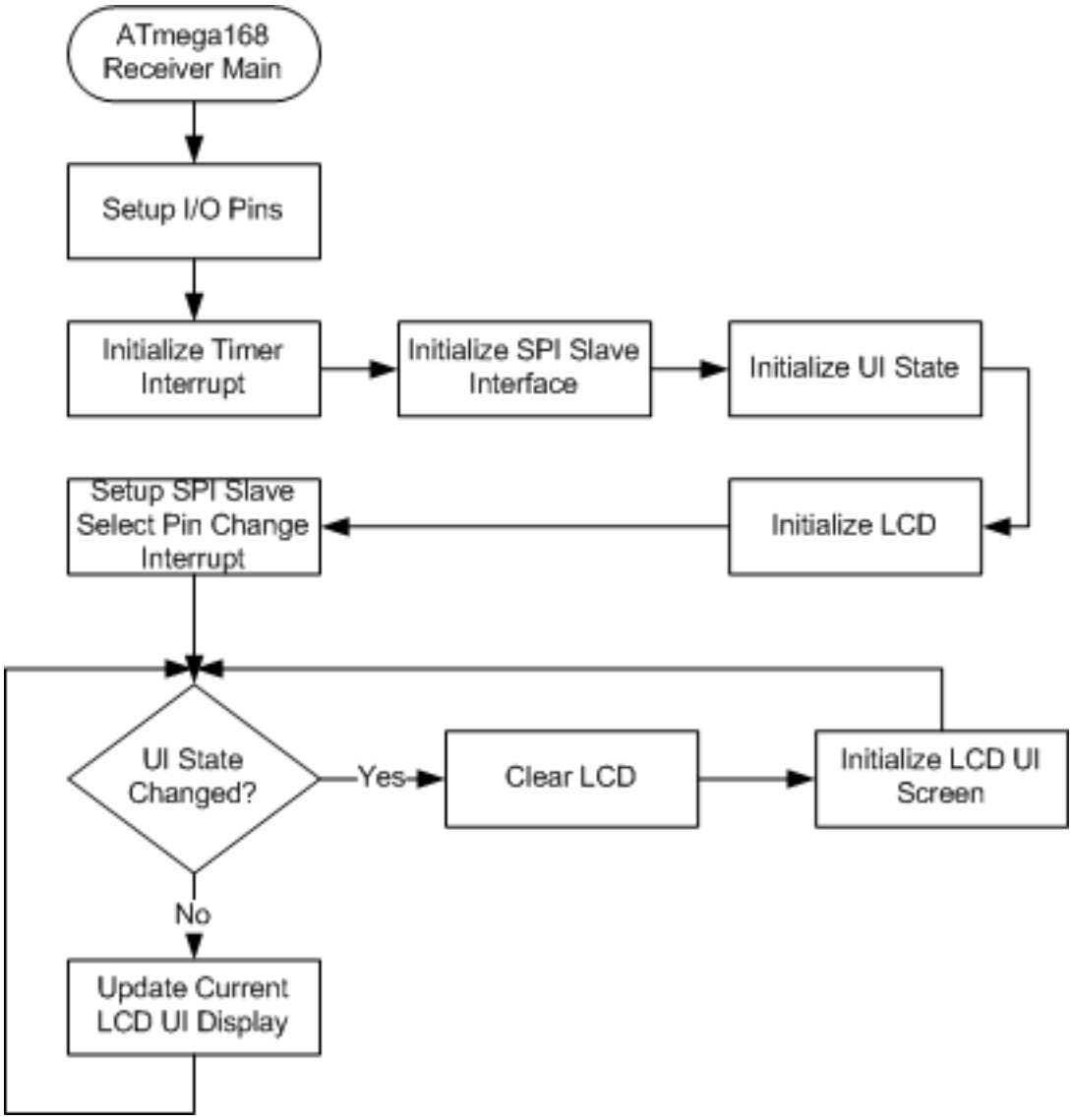


Figure G-2: ATmega168 Receiver Main Program Flowchart

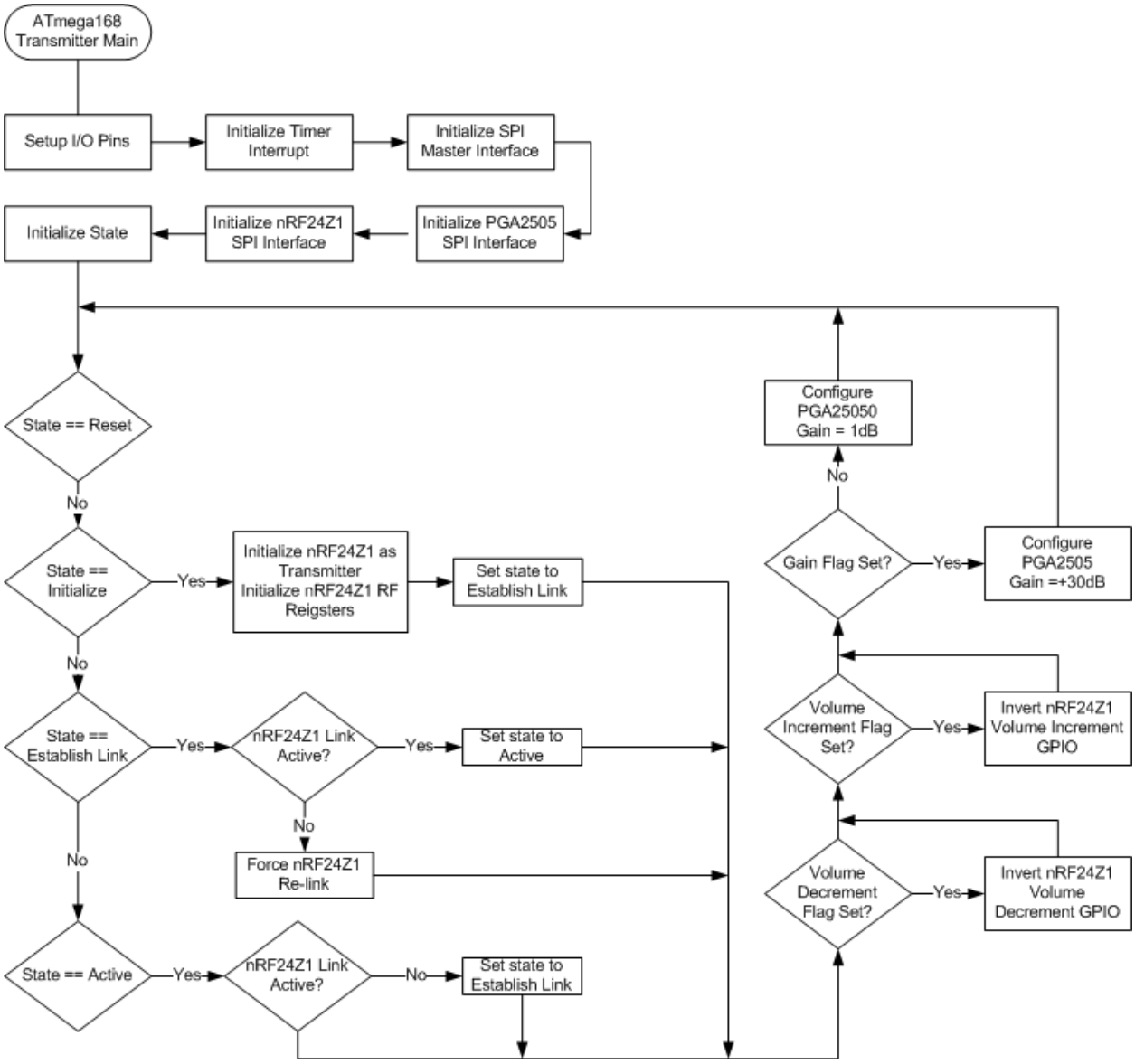


Figure G-3: ATmega168 Transmitter Main Program Flowchart

Appendix H: Hierarchical Block Diagram of Code Organization

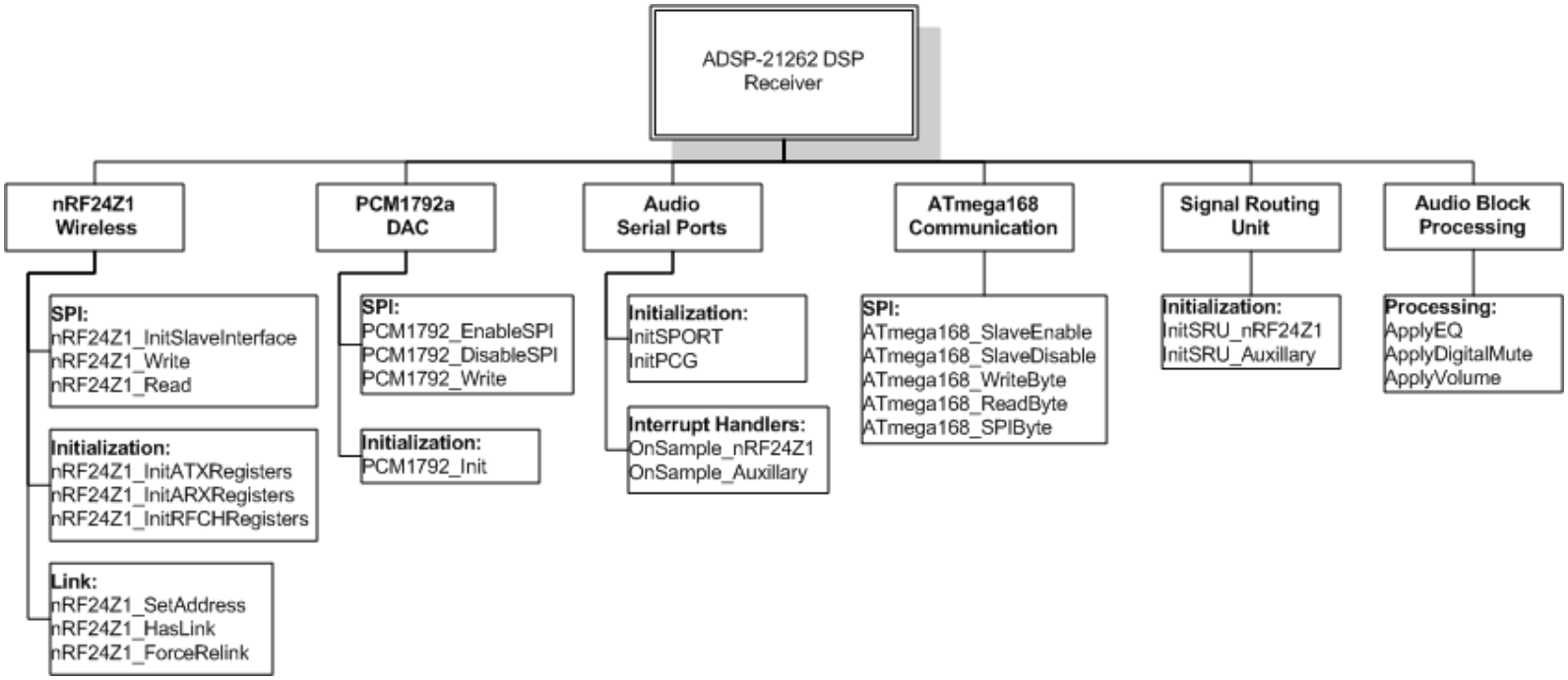


Figure H-1: ADSP-21262 Receiver Software Hierarchy

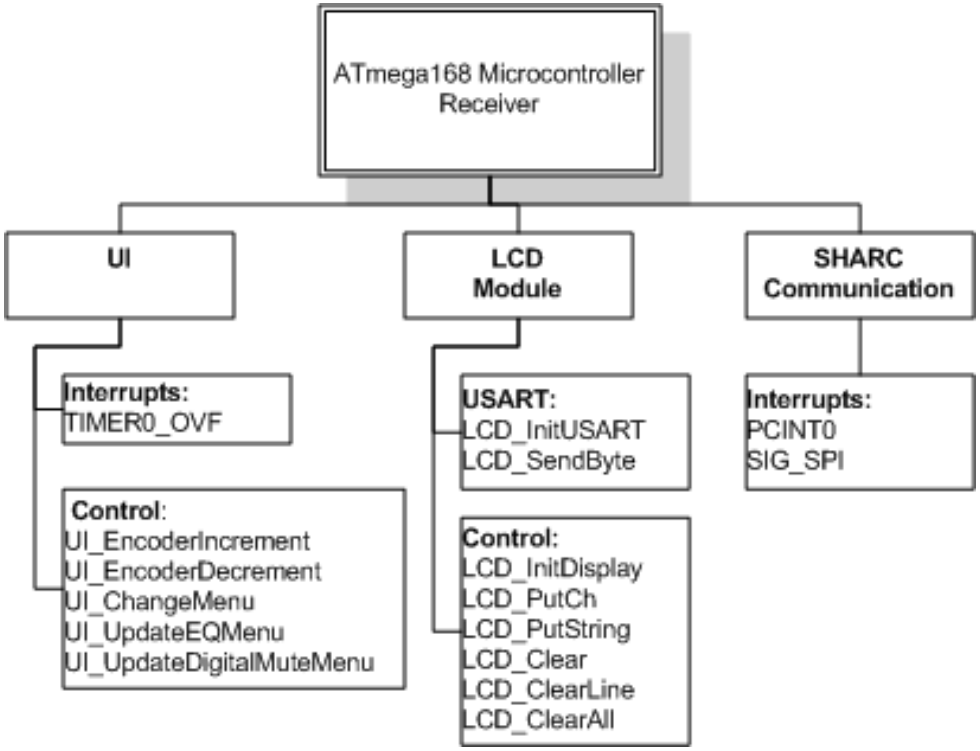


Figure H-2: ATmega168 Receiver Software Hierarchy

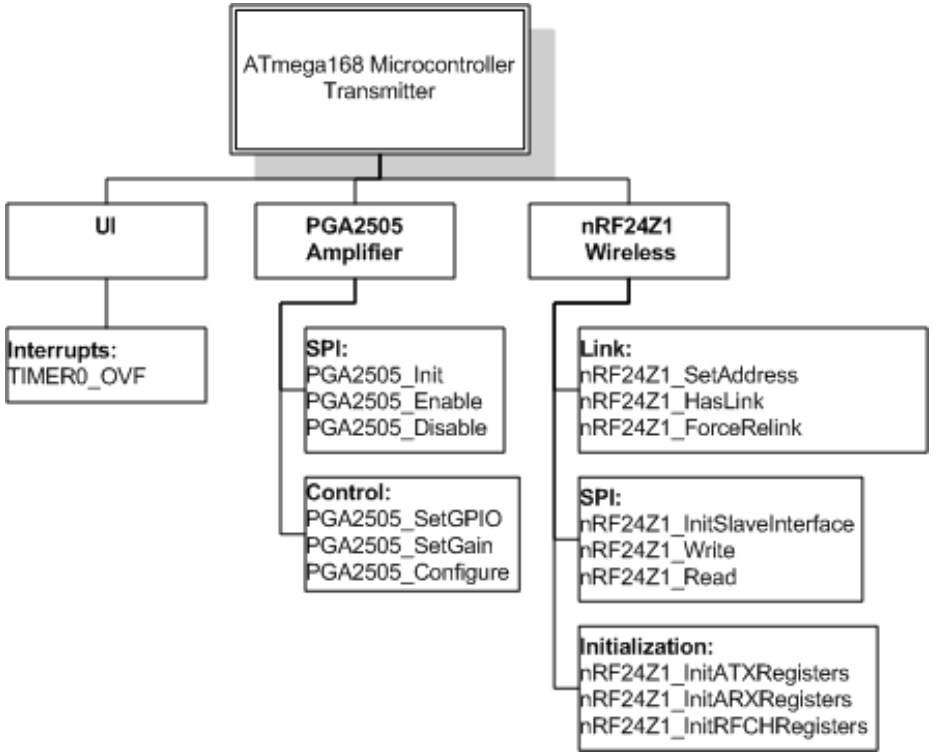
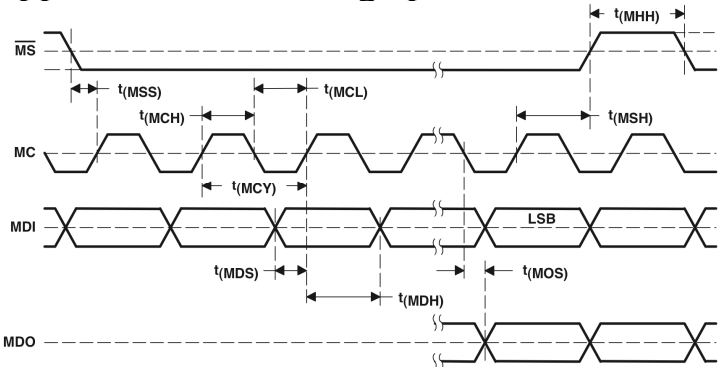


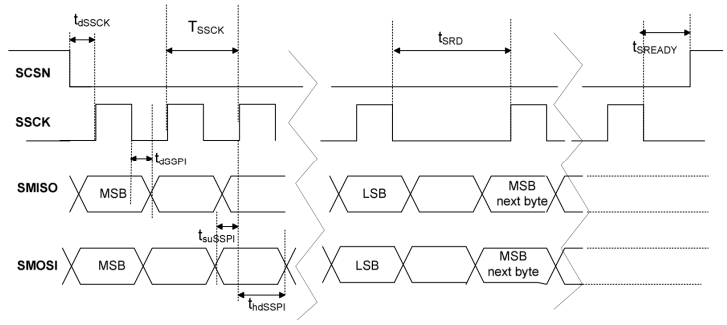
Figure H-3: ATmega168 Transmitter Software Hierarchy

Appendix I: SPI Timing Specifications and I2S Protocol



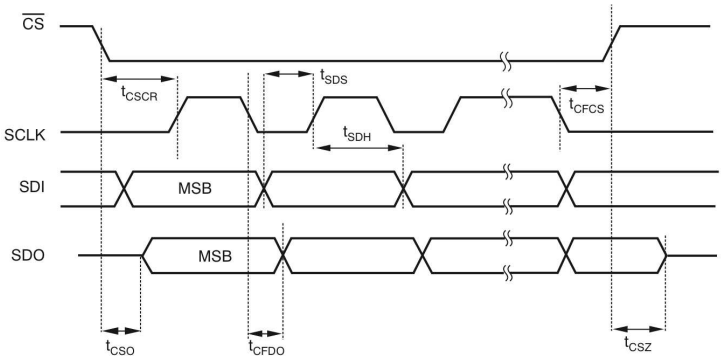
Parameter	Min	Max	Units
$t_{(MCY)}$	100		ns
$t_{(MCL)}$	40		ns
$t_{(MCH)}$	40		ns
$t_{(MHH)}$	80		ns
$t_{(MSS)}$	15		ns
$t_{(MSH)}$	15		ns
$t_{(MDH)}$	15		ns
$t_{(MDS)}$	15		ns
$t_{(MOS)}$		30	ns

Figure I-1: PCM1792a SPI Timing Diagram
Table I-1: PCM1792a SPI Timing Parameters



Parameter	Min	Max	Units
$t_{(SSCK)}$	62		ns
$t_{(suSSPI)}$	10		ns
$t_{(hdSSPI)}$	10		ns
$t_{(dSSPI)}$		55	ns
$t_{(dSSCK)}$	500		us
$t_{(SRD)}$	500		us
$t_{(SREADY)}$	500		us

Figure I-2: nRF24Z1 SPI Timing Diagram
Table I-2: nRF24Z1 SPI Timing Parameters



Parameter	Min	Max	Units
$t_{(SDS)}$	20		ns
$t_{(SDH)}$	20		ns
$t_{(CSCR)}$	90		ns
$t_{(CFCS)}$	35		ns
$t_{(CSO)}$		35	ns
$t_{(CFDO)}$		60	ns
$t_{(CSZ)}$		100	ns

Figure I-3: PGA2505 SPI Timing Diagram
Table I-3: PGA2505 SPI Timing Parameters

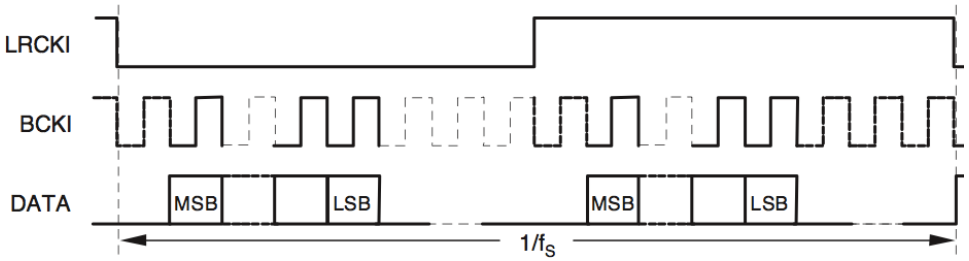


Figure I-4 I2S Clock and Data Format