DIGITAL TECHNIQUES IN DELTA MODULATION

BY

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SUMMARY

During the last twenty years delta modulation has received considerable attention as a simple but inefficient method of coding analogue signals into binary signals. Companding is used to improve the efficiency of the delta modulation process, but it gives added complexity to the hardware, so that a compromise is usually made between the performance and complexity of the delta modulator.

Recently, with the advent of integrated circuit (IC) technology it became apparent that firstly, the hardware was becoming cheaper and secondly, the cost of the IC was not strictly related to the complexity of the IC, but rather to the number of IC's made.

Because the input to the demodulator is a binary signal, delta modulation is ideally suited to the use of digital techniques in the demodulation process. Further advantages of digital techniques are; stability, noise immunity, tolerance to power supply and temperature variations, a higher yield during the manufacture of the IC and the ability to reproduce exactly the same signal at two different locations.

An efficient and therefore complex delta modulator, using digital techniques, will thus in the near future be an economical proposition.

This thesis is mainly concerned with the developement of delta modulators using the above features. Furthermore

the delta modulators are specifically designed for speech transmission in telephone applications.

Two delta modulators are described in the thesis, one using instantaneous companding, the other using syllabic companding. It will be shown that the use of digital techniques in instantaneous companding can achieve a better transmission error performance, an improved stability, a wider dynamic range and a better matching of the companding laws at the transmitter and the receiver than can be obtained by using analogue methods.

The use of digital techniques in syllabic companding enables the dynamic range to be chosen at will. The syllabic companded delta modulator described in this thesis has a 60dB companding ratio which is far more than can be obtained using analogue methods. Furthermore, digital techniques enable the modulation depth to be determined accurately, so that the companding takes place at the optimum performance of the modulator.

Computer simulation was used to optimize the delta modulators when speech is used as input.

STATEMENT OF ORIGINALITY

This thesis contains no material which has been accepted for the award of any other degree or diploma in any University and that, to the best of my knowledge and belief the thesis contains no material previously published or written by another person, except when due reference is made in the text of the thesis.

Cornelis Jan Kikkert.

AKNOWLEDGEMENTS

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Finally I would like to thank my wife Maxine for her encouragement, patience and for typing this thesis

LIST OF ABBREVIATIONS

DIDM	-	double integration delta modulation
ΔM or DM	-	delta modulation
ΔPCM	-	delta pulse code modulation
ΔΣM	-	delta sigma modulation
IC	-	integrated circuit
NDDM	-	nonlinear digital delta modulation
PCM	-	pulse code modulation
RTL	-	resistor transistor logic
SIDM	-	single integration delta modulation
SNR	-	signal to (quantization) noise ratio
TTL	-	transistor transistor logic

The graphical representation of the logic symbols used in the figures is shown in Appendix 2 in fig A2.1.

CHAPTER 1

INTRODUCTION

1.1 Code Modulation

Code modulation is a group of modulation processes where an analogue signal is coded into a binary signal. In order for this process to be possible, the analogue waveform must be sampled. These samples are then approximated to the nearest standard signal, this process is known as quantization. The standard signal is then represented by a certain binary coded word. These code words are then transmitted and at the receiver they are decoded into standard signals, giving a demodulated output which is an approximation of the input.

Because the analogue input is sampled, the sampling rate must be larger than the Nyquist rate, i.e. at least twice the bandwith of the input signal.

1.1.1 Pulse Code Modulation

In pulse code modulation, (PCM) the range of amplitude over which the input signal is to operate is divided into n regions. In each region a standard level is chosen, which is usually the middle of the region. These regions are numbered 0 to n-1. At each sampling interval, the region in which the input signal falls is determined, and the number corresponding to this region is transmitted. At the receiver this information is decoded into the standard level for the

particular region. It is clear that all the input signals in one region are represented by the standard level and approximations of the input are involved.

From information theory it is clear that the most information about the signal will be transmitted if we choose the regions such that each of the regions has an equal probability of containing the input signal.

The most common spacings between the standard levels are linear and logarithmic, neither of which necessarily gives the best performance, depending on the signal being used.

The linear standard level division is often used in computer interfaces, where the pulse code modulation is known as analogue to digital conversion and the demodulation as digital to analogue conversion.

1.1.2 Differential Pulse Code Modulation

In differential pulse code modulation (ΔPCM), the change of level is transmitted, instead of the absolute level as in PCM.

Because in ΔPCM the change of input is transmitted it is more suitable to input signals which have a spectrum that decreases with frequency, so that the rate of change of input is constant.

Both linear and logarithmic spacing between the standard levels can be used as for PCM.

1.1.3 Delta Modulation

Delta modulation is a special name for unity bit ΔPCM. At each sampling interval we will thus send the information "increase output" or "decrease output". Because so little information is transmitted at each sampling interval, it can be seen that in order to transmit sufficient information to reconstruct the input signal accurately the sampling frequency must be many times the Nyquist rate.

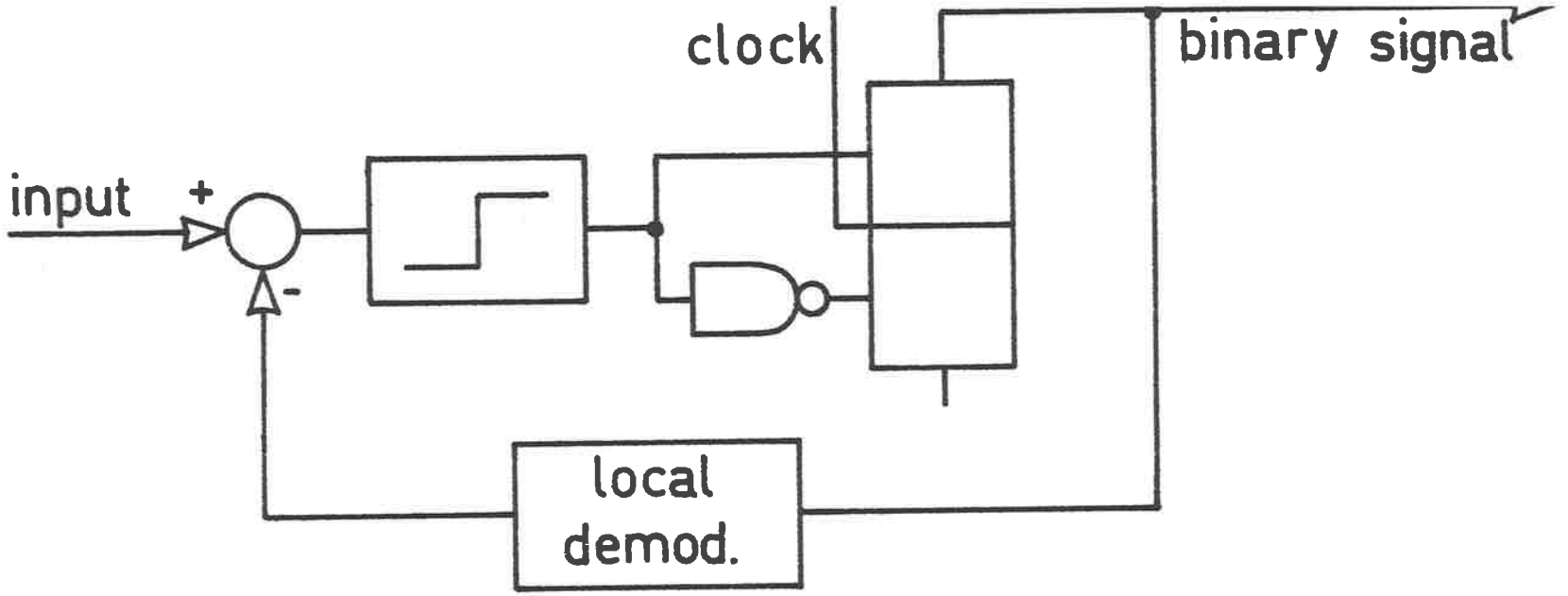
Typical values for the sampling rate are between two and twelve times the Nyquist rate, depending on the accuracy required.

Furthermore because only one bit of information is transmitted at each sampling interval, the basic delta modulator is very simple. The block diagram for the system is shown in fig 1-1 and the input and unfiltered demodulated output waveform for the case where the demodulator is simply an integrator are shown in fig 1-2.

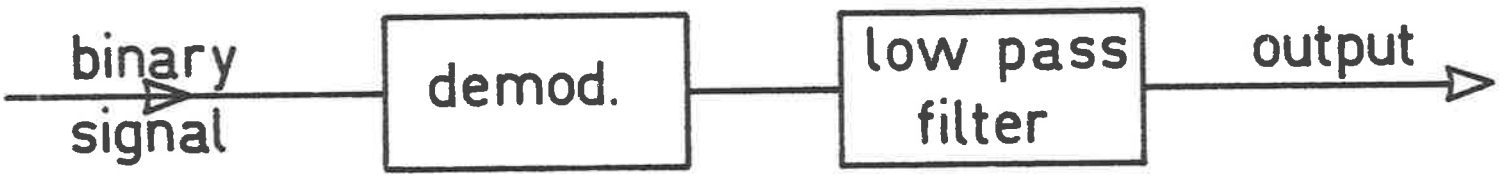
The low pass filter in the demodulator removes those frequency components of the unfiltered demodulated output signal that are outside the signal bandwidth, giving an output signal that closely resembles the input signal.

1.2 Quantization Noise

In section 1.1 it was stated that in code modulation, the input signal is converted into a standard signal, which is then coded and transmitted. The distortion introduced by



(a)modulator



(b)demodulator

FIG.1.1

Delta modulator block diagram.

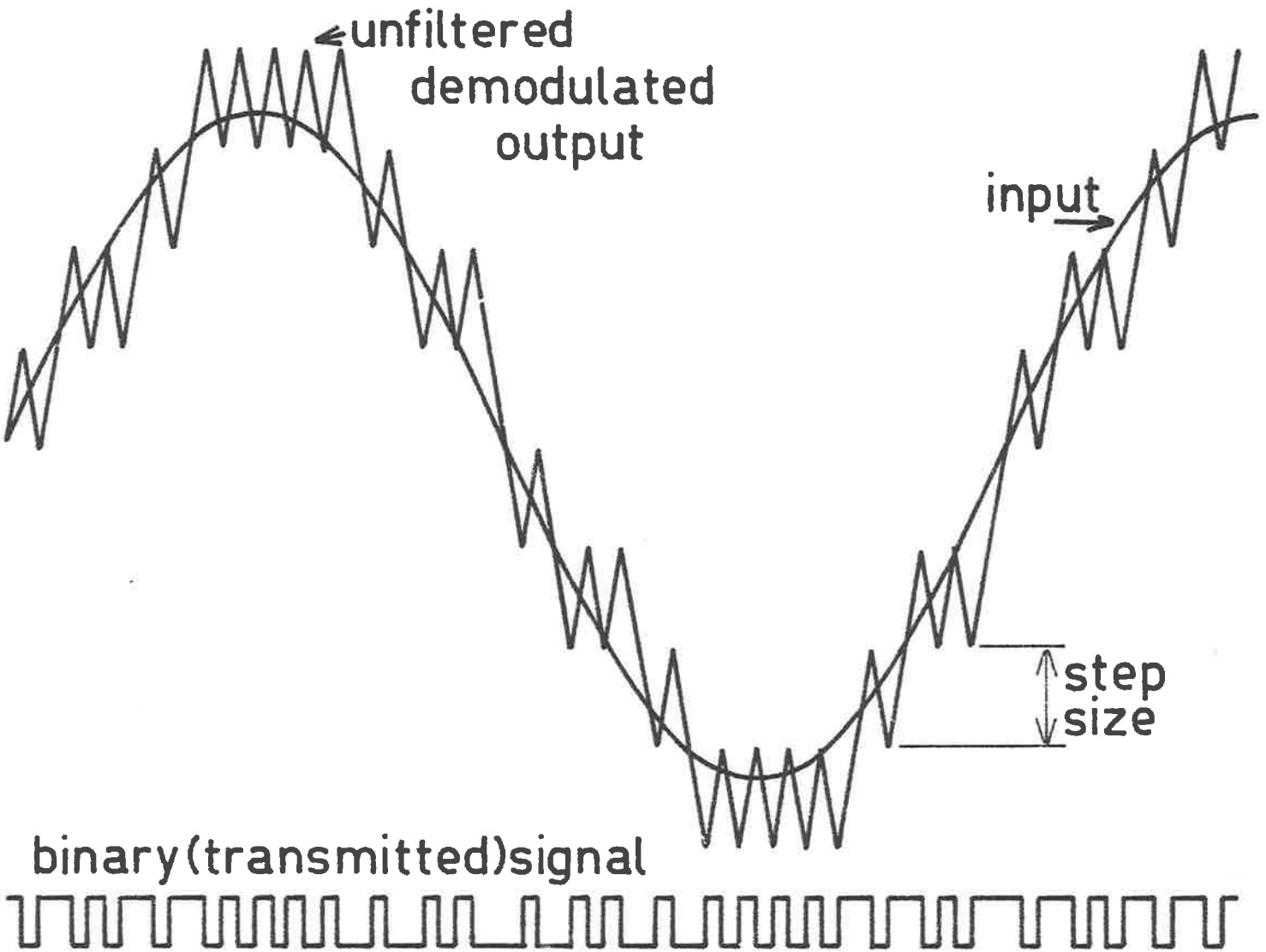


FIG.1.2
Delta modulator waveforms.

converting the input signal into the standard signal is known as the quantization noise. The quantization noise can thus be defined as the difference between the input and quantized waveforms. Furthermore, usually one is only interested in those frequency components of the quantization noise that lie inside the signal bandwidth, so that generally the term quantization noise only refers to those frequency components. It should be noted that the definition allows for a delay or amplitude change, introduced by the quantization process, since neither will affect the waveshape.

1.3 Historical Review

1.3.1 The Developement of Delta Modulation

The principle of delta modulation was first described in a French patent [1], issued in 1946. The first description of delta modulation in the English language was given by de Jager [2] in 1952. He originated the following intuitive concepts: Firstly, de Jager assumed that speech could be represented by an 800Hz sinewave. Secondly, he empirically derived formulae for the maximum SNR for both single integration delta modulation (SIDM) and double integration delta modulation (DIDM) as :

$$SNR_{max} = C_1 \frac{f_s^{3/2}}{f.f_o^{1/2}} \qquad \text{for SIDM}$$

$$SNR_{max} = C_2 \frac{f_s^{5/2}}{f.f_o^{3/2}} \qquad \text{for DIDM}$$

where C_1 and C_2 are constants, f_s is the sampling frequency, f is the audio signal frequency and f_o is the audio bandwidth. The constants C_1 and C_2 were determined experimentally as $C_1 = 0.2$ and $C_2 = 0.026$. The maximum SNR's obtained using these formulae are indicated in fig 5.5, together with a comparison of the results obtained by others.

Zettenberg [3] obtained a mathematical model for speech and used this to analyse the performance of SIDM. Syllabic variations of power were however not included in the model for speech. The results obtained agreed reasonably well with the results obtained by de Jager, seemingly justifying de Jager's assumptions for evaluating the performance of SIDM. Zettenberg did however notice that the peak SNR occurred at an input power which was 6dB less than predicted by de Jager's assumptions.

In 1962 Inosi et.al. [4] proposed integrating the input signal to obtain a delta modulator capable of handling a uniform spectrum. By re-arranging the block diagram as is shown in fig 1.3 only one integrator needs to be used. The resulting system is known as delta sigma modulation. They [4] found that the maximum SNR is independant of the audio frequency and is given by:

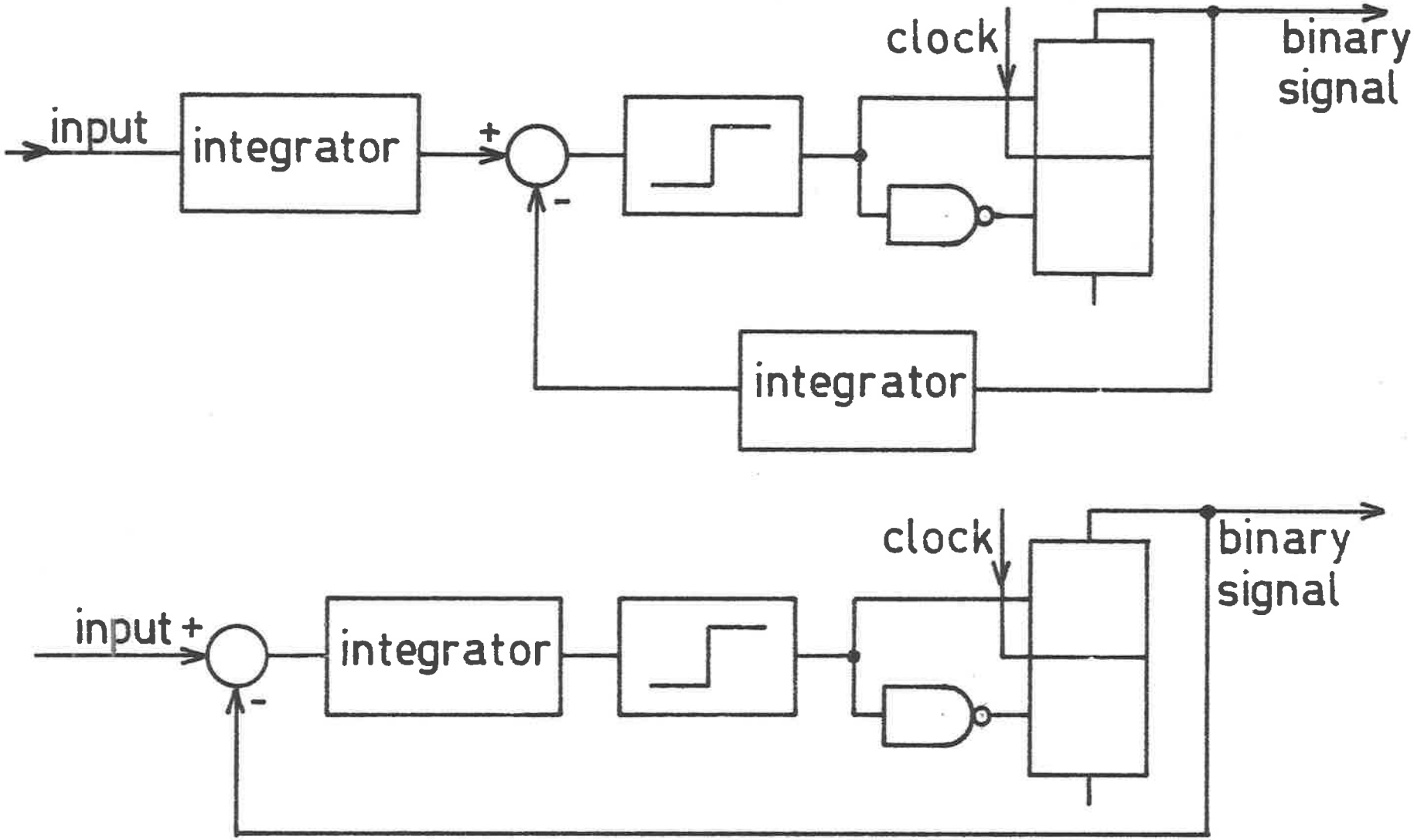


FIG.1.3
Delta-sigma modulator block diagrams.

$$SNR_{max} = \frac{3}{4\pi} \left(\frac{f_s}{f_o}\right)^{3/2} \approx 0.2 \left(\frac{f_s}{f_o}\right)^{3/2}$$

The three systems mentioned above namely SIDM, DIDM and $\Delta\Sigma M$ are the basic delta modulation systems. The dynamic range of each of these systems can be extended by companding (compressing at the modulator and expanding at the demodulator).

The quantization step size, normally referred to as the step size, is defined as the increment in the unfiltered demodulated output during one clock period, as shown in fig 1.2.

The companding process varies the step size, to adapt the modem to the input signal.

1.3.2 Instantaneous Companding

Instantaneous companding has the property that the step size is varied rapidly.

Winkler [5], in 1963, proposed a system known as high information delta modulation. In her system the step size is doubled when three consecutive one's or zero's are detected. The step size is halved when a transition in the binary output occurs. A variation of this rule was developed by Montgomery [6] and has been used by the Weapons Research Establishment for their studies for project Mallard [7].

With this variation, known as binary variable slope delta (type A), the step size is halved only if a transition has occurred and the previous two bits were the same.

In 1967 Abate [8] described a system where the step size is increased if a sequence of ones or zero's occur and decreased if a transition occurs. It was however not stated how long the sequence of ones or zeros must be before the step size is increased. It is presumed that at least 3 bits are used since if the step size is increased on the second consecutive bit, oscillations can take place, as is indicated in section 4.4.3. Abate found by using computer simulation and a bandlimited Gaussian input signal that a linear increment in step size gave the best performance.

In 1969 Bosworth and Candy [9] produced an instantaneous companded delta modulation system. The step size is increased if the transmitted bit is the same as the previous bit. The step size is varied according to the following sequence 1,1,2,3,5. When a transition occurs, the step size is reduced to the smallest step.

All the above systems can be represented by the block diagram in fig 1.4. In practice satisfactory results can be obtained by using only a small number of different step sizes. Bosworth and Candy for example use 4 step sizes only. However, the companding achieved by the last 2 systems is small. (12dB in the system proposed by Abate)

The author developed an instantaneous companded delta

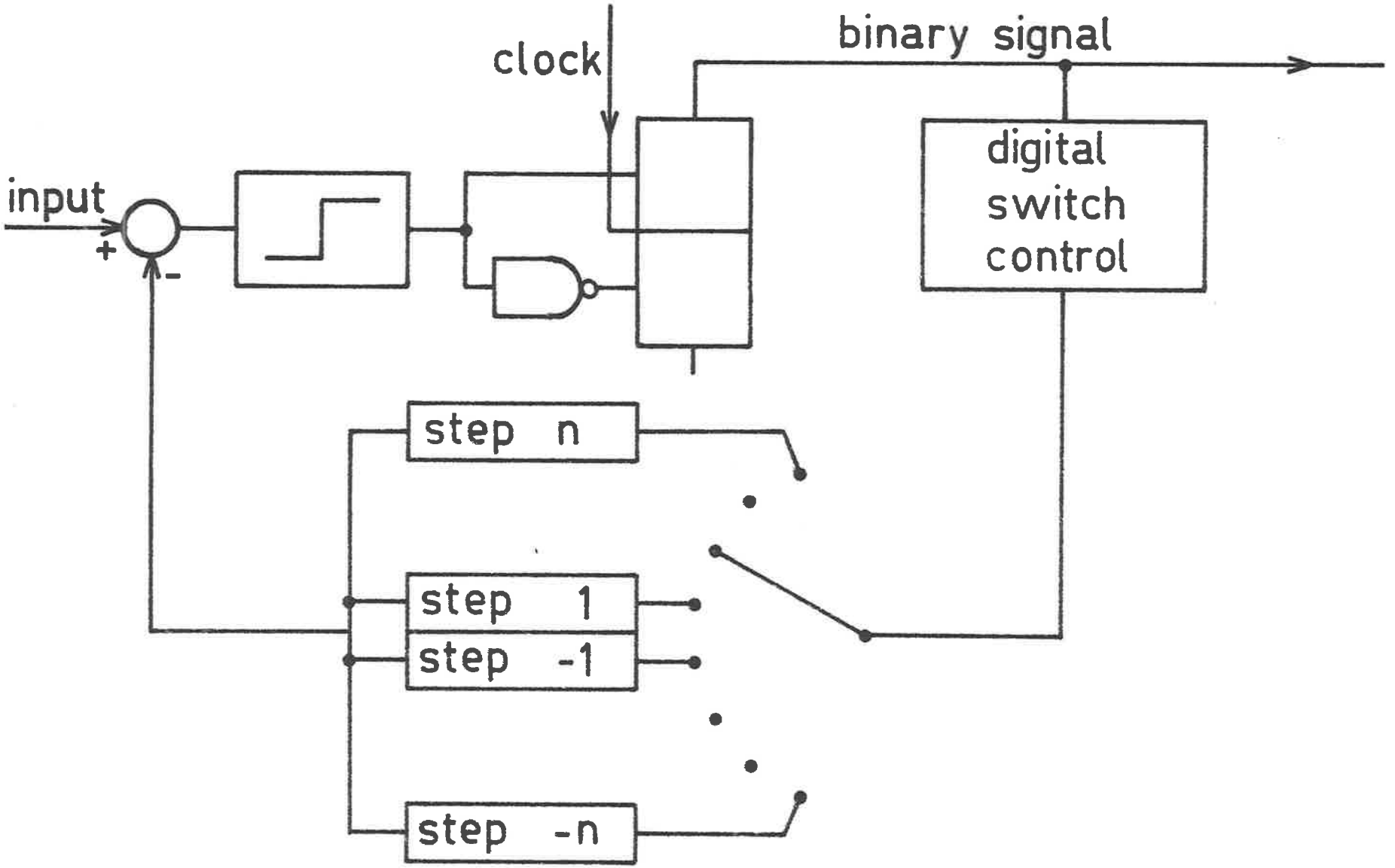


FIG.1.4
Delta modulator with instantaneous companding.

modulation system which has a companding ratio of 43dB and is described in chapter 3. (The companding ratio is the ratio of the largest to the smallest step size) This companding ratio is far more than has been achieved by other workers [5-9].

1.3.3 Syllabic Companding

In syllabic companding the step size is varied slowly and in general the system can be represented by the block diagram shown in fig 1.5 The companding should ideally vary the step size in such a way that the modulator always operates at the maximum SNR. A detailed theory of the companding is presented in the sections 4.2 and 4.3. The companding can only stretch the horizontal axis of the SNR versus input power curve, but it cannot alter the maximum SNR's at all. If one compares the maximum SNR's obtained from the following systems one can see that the results are similar, the only difference being the dynamic range over which the companding can be obtained.

Tomozawa and Kaneko [10,11] described a system using syllabic companding in 1966. The normalized input power detection block in fig 1.5 consists of an integrator followed by a half wave rectifier. The filtering consists of a low pass RC network. Their hardware has a companding ratio of 20dB.

Hosokawa et.al. [12] devised a system where the output

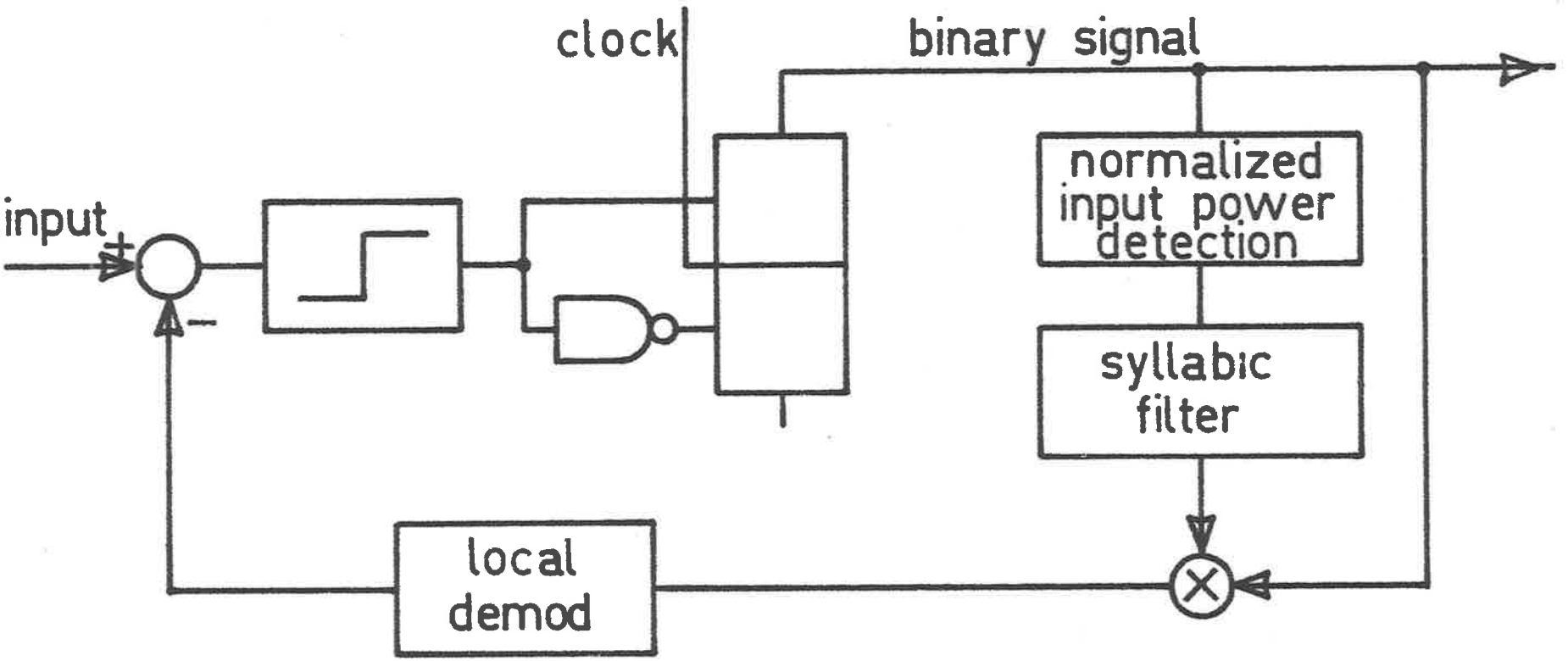


FIG.1.5

Delta modulator with syllabic companding.

of the local demodulator is used to control the amplitude of the input to the modulator. In principle this is nearly the same as the incomplete companding proposed in the late thirties [13]. A description of complete and incomplete companding is given in section 4.2.

Brolin and Brown [14] used two delta modulators, one for audio signal coding, the other to transmit information about the amplitude of the signal. This amounts to trans transmitting a separate pilot signal containing the amplitude of the signal. This is again one of the techniques used to obtain complete companding in the late thirties [13].

The system described by Greefkes and de Jager [15] in 1968 uses the bandwidth below 200Hz to code the amplitude information, by adding a DC level, proportional to the signal power to the input signal. In this system the pilot signal containing the amplitude information is transmitted in the bandwidth below 200Hz. Only incomplete companding was achieved however and the companding ratio was about 20dB.

In 1968 Hosokawa and Yamashita [16] used logic circuitry for the normalised input power detection block in fig 1.5. Hauser and Zarda [17] produced a similar system, but the binary signal required to initiate a change of step size is different.

In 1970 Shindler [18] described a system which uses logarithmic companding. This system will be discussed further in section 4.3.3.

None of the above systems have been able to achieve a companding ratio of more than 35dB. In chapter 4 a system developed by the author, is described where the companding ratio can be chosen at will and results are presented for a hardware model incorporating a companding ratio of 60dB.

CHAPTER 2

THE MEASUREMENT OF THE PERFORMANCE OF DELTA MODULATION AND RELATED SYSTEMS

2.1 Introduction

Present indications are that delta modulation if it is to be used in the telephone network will mainly be used for speech applications. In order to develop better delta modulators and to compare the relative performances of different delta modulation systems, a precise measure of the performance must be obtained. Furthermore as shown in this chapter, the performance of a delta modulator when subject to sinewaves is not directly related to its performance when subject to speech as input, so that the performance should be evaluated for speech inputs, eliminating conventional measuring techniques. The author developed a technique enabling the exact performance of a delta modulator to be determined for any input signal. This technique and the resulting hardware are discussed in this chapter.

The discussion applies to related systems such as pulse code modulation (PCM) as well as delta modulation.

2.2 Review

There are many methods for determining the performance of a delta modulator.

Since some of the methods mentioned in this section are

not commonly used, all these methods are described in Appendix 1.

The methods can be grouped into two classes namely subjective methods and nonsubjective methods.

The subjective methods are:

1) Intelligibility tests, which evaluate how good one can understand speech subjected to the delta modulation process.

2) Equivalent white noise methods, which tests for the quality of the demodulated signal by comparing it with the input signal degraded by white noise.

Both these tests are useful when the delta modulator has an SNR of less than 20dB. Once the SNR becomes better than 20dB it becomes difficult to distinguish between the input and demodulated output so that the intelligibility score would be nearly 100%, regardless of whether the SNR is 40dB or 20dB. Because these tests are subjective, care should be taken to eliminate or allow for the learning that the subjects may develop. Weapons Research Establishment (7) found that the subjects developed a skill at understanding the test words and the intelligibility score improved as time went on. The Australian Post Master General's Department Subjective Evaluation Group found that their test team developed a dislike to quantization distortion as time went on.

The nonsubjective methods include methods used for

distortion measurements in audio equipment such as the Notch Filter method, the Frequency Analysis method and the Cancellation method. These methods are described in Appendix 1.

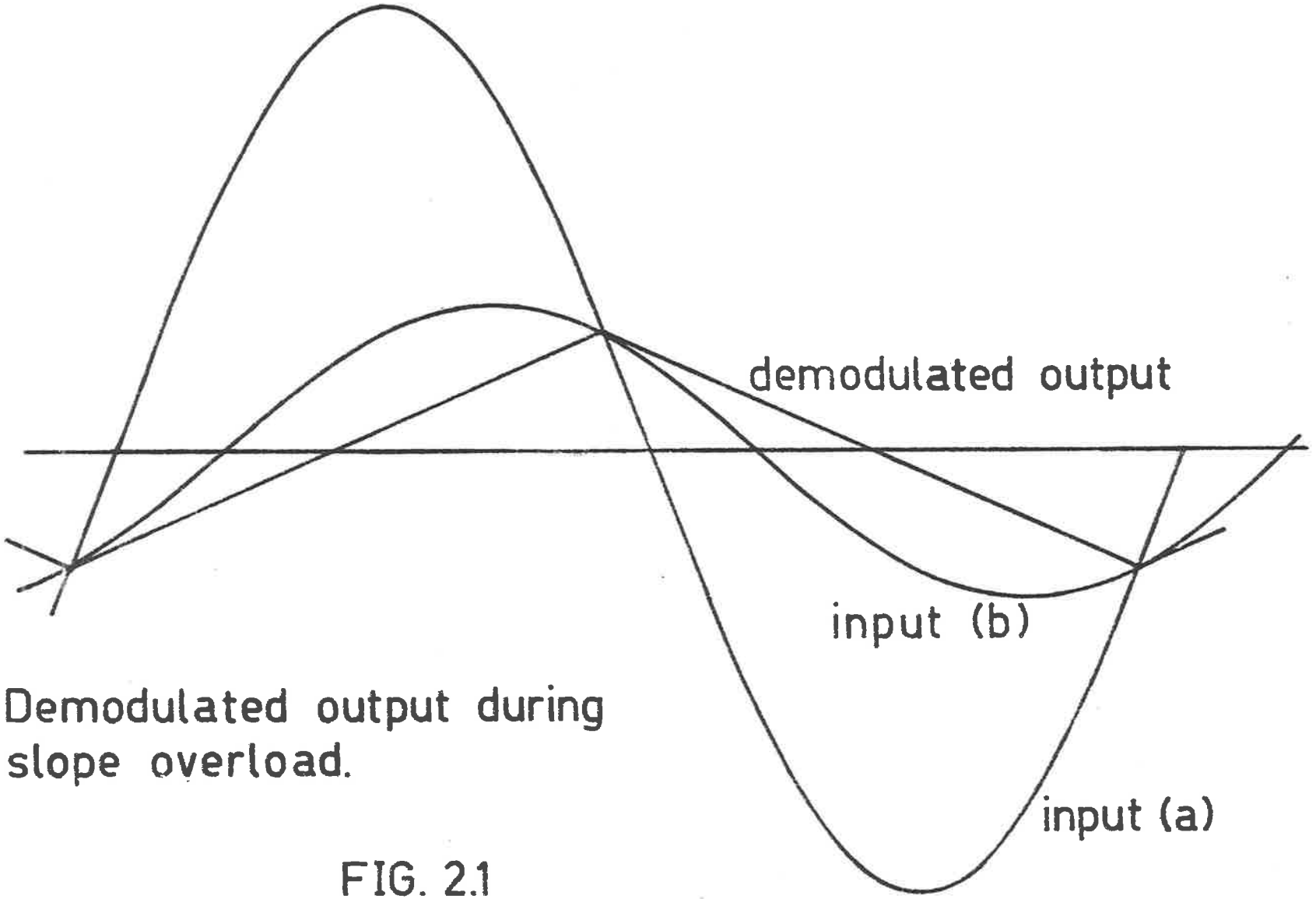
Since these methods measure distortion, they are also capable of measuring quantization distortion in delta modulation.

It should be pointed out that these methods are designed for equipment where limiting does not normally occur. It will be shown directly that these methods no longer give an indication of the performance of the equipment when limiting occurs.

In delta modulation the dynamic range is normally small and slope overload occurs during a significant part of the useful operating range. When overload occurs the output signal is no longer proportional to the input signal, as is shown in fig 2.1.

Since the above methods use the output of the delta modulator to obtain a measure of the distortion, the quantization distortion will be the same for both input signals in fig 2.1. In one case the system is only just limiting, while in the other, severe overload occurs, and obviously the performance of the modulator is not the same.

When overload occurs, the above methods will no longer indicate a measure of the performance of the delta modulator.



Demodulated output during slope overload.

FIG. 2.1

2.3 Measurements of signal to quantization noise ratio for random input signals

Some of the work described in this section is also described elsewhere by the author [19]. A copy of this publication is included in the thesis.

2.3.1 Definition of quantization noise

There are several definitions of quantization noise, each of which have their own merits.

The definition used in this thesis is as follows: Quantization noise is the difference between the input and demodulated output waveforms.

The gain and delay of a delta or pulse code modulator is independant of the amplitude and frequency of the input signal under non-overload conditions. If the gain and delay are assumed to be amplitude and frequency independant under overload conditions as well, one will obtain a different measure of the performance for both input signals in fig 2.1 as required.

The definition can thus be modified as follows: Quantization noise is the difference between the input and demodulated output waveforms, provided the gain and delay of the delta or pulse code modulator are assumed to be independant of the amplitude and frequency of the input signal and the values of the gain and delay of the modulator are those corresponding to non-overload conditions.

It should be noted that the conventional methods mentioned in Appendix 1 do not assume the gain and delay of the delta modulator to be constant.

Fig 2.2 indicates which areas contribute to the distortion when the distortion is measured according to:

(1) the above definition

(2) the notch filter method

It can be seen that by using the above defintion, an indication of performance can be obtained even when the system is overloading.

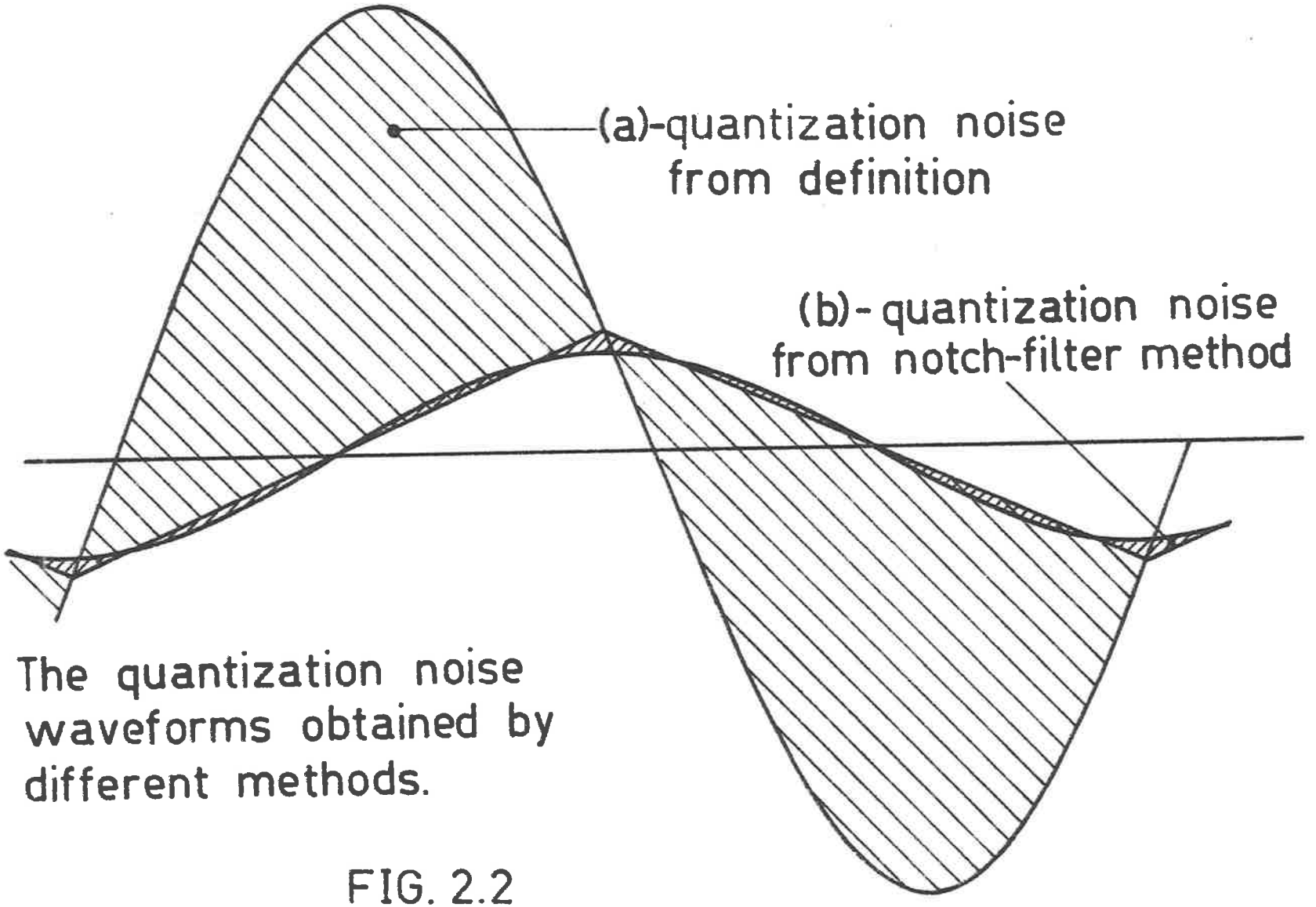
2.3.2 Disadvantages of using sinewaves for measurements

The delta modulators investigated in this thesis are designed for use with speech.

Since there are differences in the performance of a delta modulator when it is subject to an 800Hz sinewave input or a speech input, as is shown in fig 2.3 for SIDM, the testing should be done with speech as input. The results in fig 2.3 are obtained by computer simulation as discussed in chapter 5.

Furthermore the SNR of a nonlinear system such as a delta or pulse code modulator when subject to sinewaves need not be related to its performance when it is subjecj to speech, as is illustrated by the following 3 examples:

(a) A digital coder measures the frequency, and amplitude of a sinewave input, transmits this information in binary



The quantization noise waveforms obtained by different methods.

FIG. 2.2

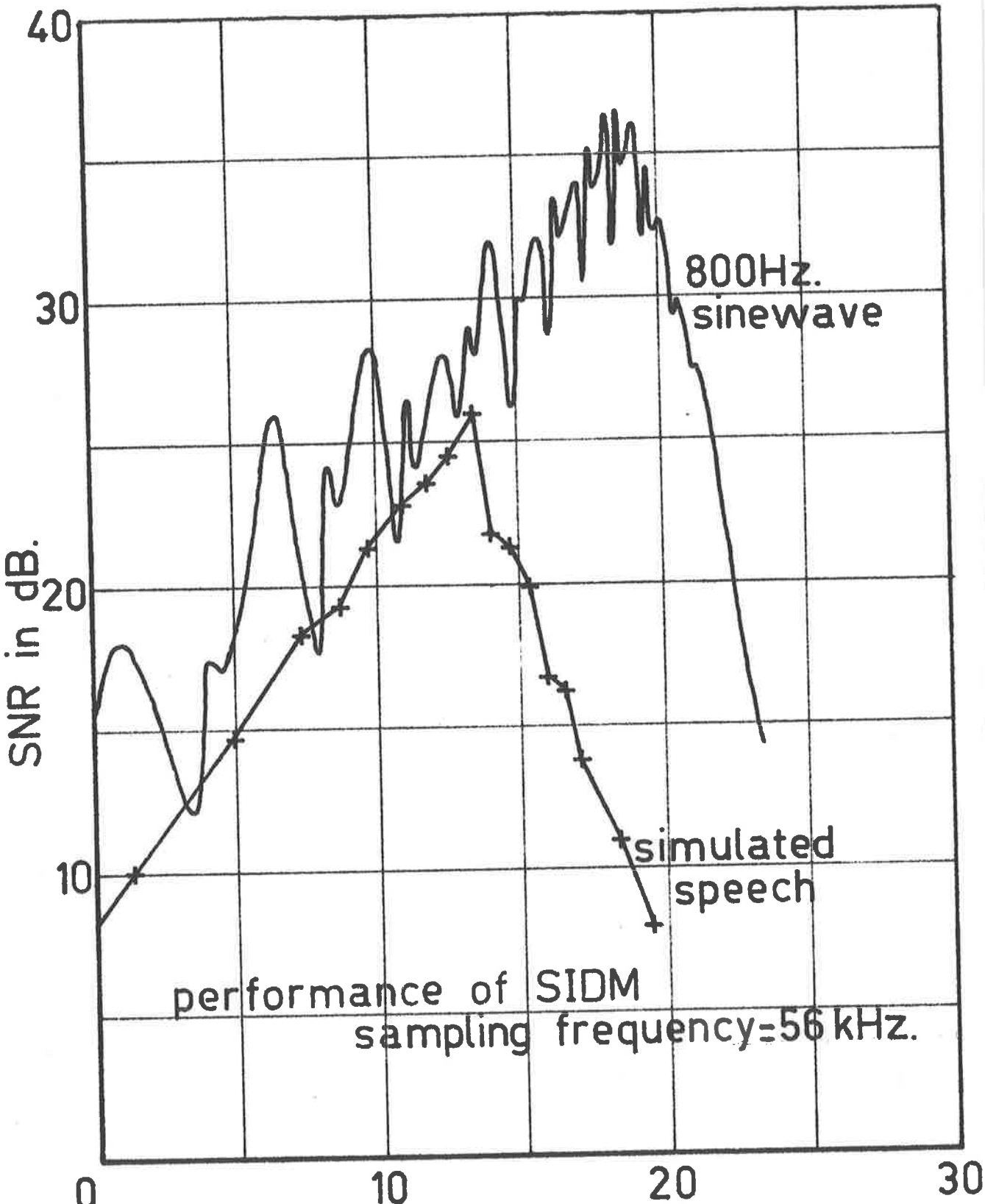

40
30
20
10
0
10
20
30
SNR in dB.
Relative input in dB.
800Hz.
sinewave
simulated
speech
performance of SIDM
sampling frequency=56 kHz.

FIG.2.3

form and at the receiver this information is used to set the amplitude and frequency of an oscillator. This system will have an excellent signal to quantization distortion ratio for sinewaves, but the performance when the system is subject to speech will not be good.

The example given above is extreme, it does however illustrate one of the differences between speech and sinewaves.

(b) A delta modulator, employing syllabic companding has attack and decay time constants which are far too long so that when speech is used as input, the companding cannot follow the input power variations and the system is either overloading or operating near threshold. (i.e. at a small normalized input power) The performance of the system, when subject to sinewaves, will be good because the companding has sufficient time to adjust itself to the proper level. Schindler [18] indicates that the continuous delta modulation scheme used in France has this defect of improperly designed companding response times.

(c) As shown in section 4.5.2 and fig 4.13 the normalized input power (which is defined in chapter 4 and [20]) at which the companding should operate is different for speech and sinewaves. This means that one can only obtain the best performance from a companded delta modulation system to be used with speech, if its companding is designed for speech. It is impossible to obtain the relevant information required

to design the companding from measurements using sinewaves. This point is further discussed and illustrated in chapter 4.

None of the non-subjective methods previously mentioned can be used when a random input signal such as speech is used. The subjective methods require a team of listeners and normally the results cannot be repeated, due to the changing subjective standards of the team. Because of this and other practical and financial limitations, subjective methods have not been used in this thesis to evaluate the performance of delta modulators.

It is however possible to obtain a method for evaluation of the performance by either using control theory techniques related to nonlinear systems, or using the previous definition of quantization noise.

2.4 Measurement equipment description

2.4.1 Theory

The quantization noise is defined previously as the difference between the input and output waveforms.

A frequency independant time delay will not affect the waveform. Since the delta modulator may introduce a delay, this delay has to be allowed for.

A gain, independant of frequency and amplitude will not affect the waveform and hence any amplification in the delta modulator must thus be allowed for also.

The block diagram in fig 2.4 shows equipment which will

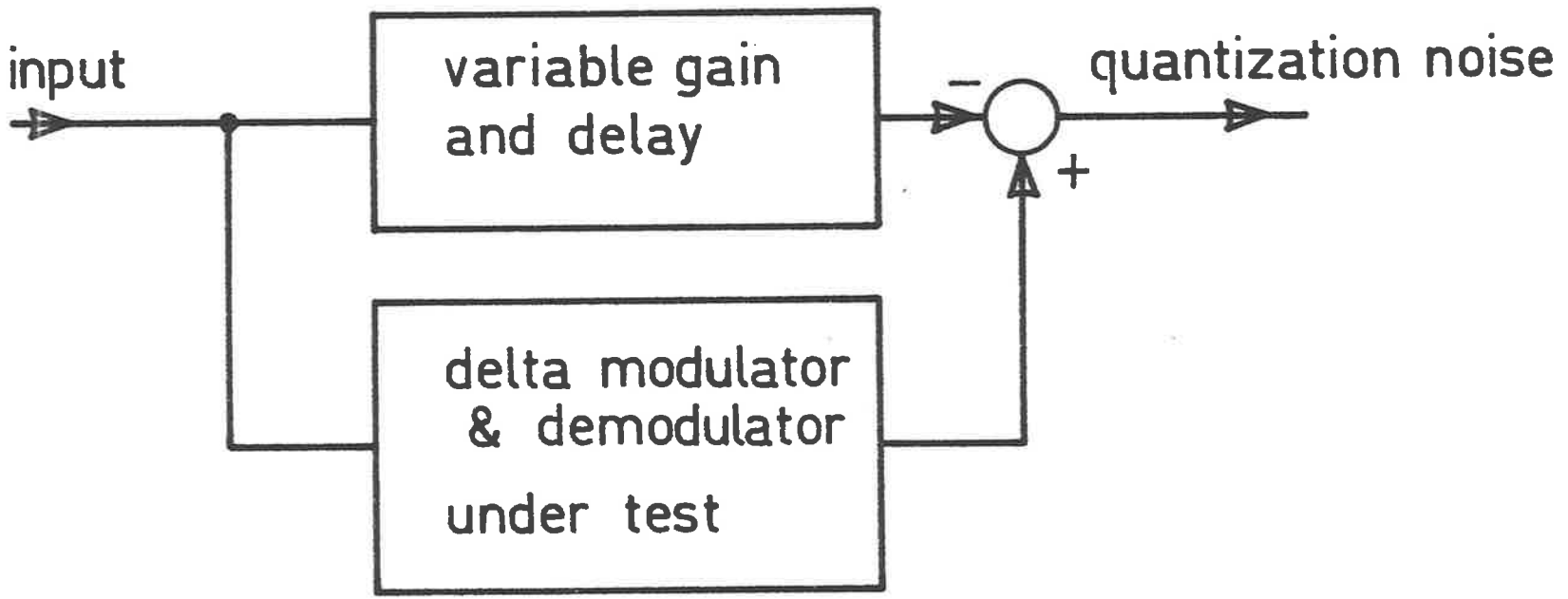


FIG. 2.4
Method for obtaining the quantization noise.

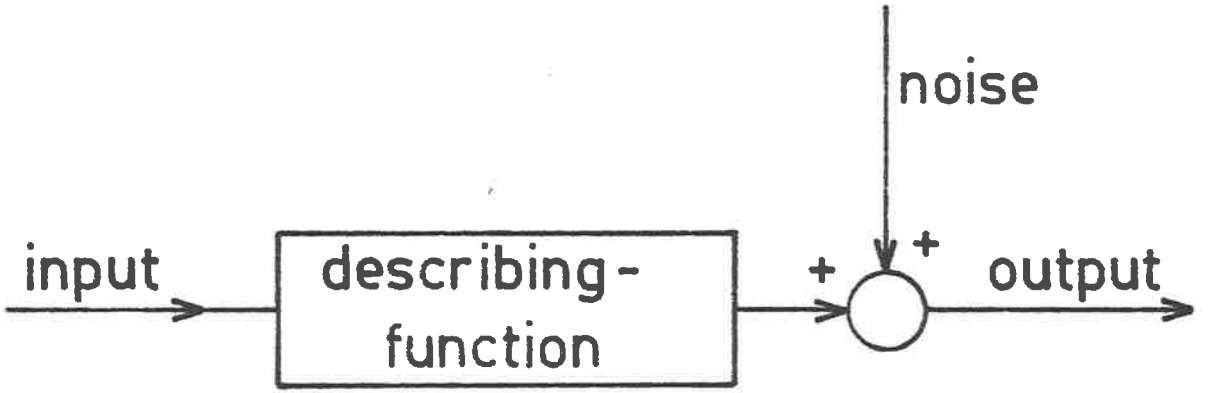
evaluate the quantization noise as defined previously. In order to obtain the quantization noise, the gain and delay are adjusted such that the minimum difference signal is obtained when the delta modulator is not limiting. These then remain fixed for the rest of the measurements.

It should be realized that if sinewaves are used as input and no limiting occurs, the results obtained by this method will be exactly the same as those obtained by the cancellation method. There are however the following differences:

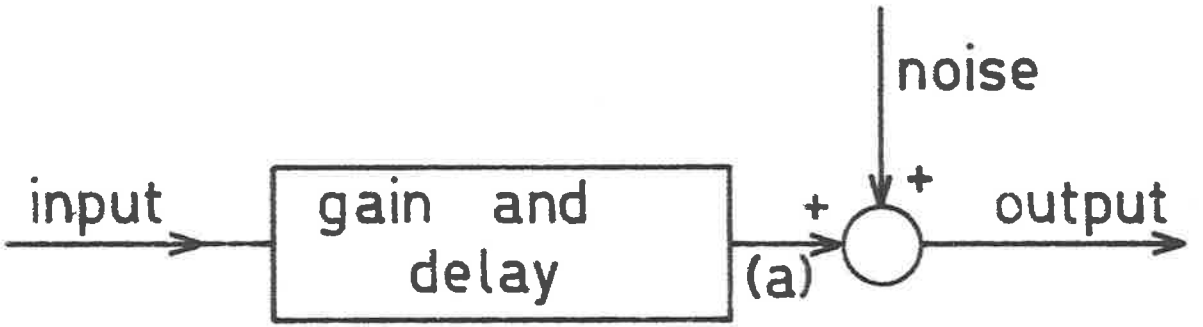
(1) In the cancellation method, the gain and delay are adjusted continuously, while for the proposed method the gain and delay of the cancellation network are kept constant, so that when the modulator is limiting, the difference signal in fig 2.4 remains the quantization noise as indicated in fig 2.2 (a).

(2) The cancellation network is frequency independant and any input signal, including speech, can be used.

A second approach to the problem is as follows:
In control theory, a nonlinear element is usually represented by a linear describing function[21], plus a noise source as shown in fig 2.5 (a). A delta modulator contains nonlinearities, and can thus be represented similarly. A gain and delay which are independant of both frequency and amplitude, will not affect the waveshape. Since the object of the delta modulator is to reproduce the input waveform as



(a) block diagram of a nonlinear element



(b) block diagram of a delta modulator

FIG.2.5

closely as possible, the describing function should not alter the waveshape and the deviations from the input waveshape will will be due to the noise source. This noise is the quantization noise, according to the definition in section 2.3.1. The delta modem can thus be represented by the block diagram in fig 2.5 (b).

If we want to obtain the quantization noise, this can be done by using a cancellation network with a transfer function identical to the describing function of the delta modem, subjecting this to the same input signal as the delta modulator and subtracting the respective output signals, as is shown in fig 2.6.

Since the gain and delay of the delta modulator are not known in advance the gain and delay of the test equipment must be made variable.

2.4.2 Measurement of Power

The ultimate aim of the test equipment is to obtain a measure of the performance of the delta modulator under test which is hopefully indicated by the signal to quantization noise ratio. The SNR is normally expressed as a power ratio and in dB.

In the previous section a method was described which enables one to obtain the quantization noise. From this one can obtain the quantization noise power.

The signal power can be obtained from the input signal.

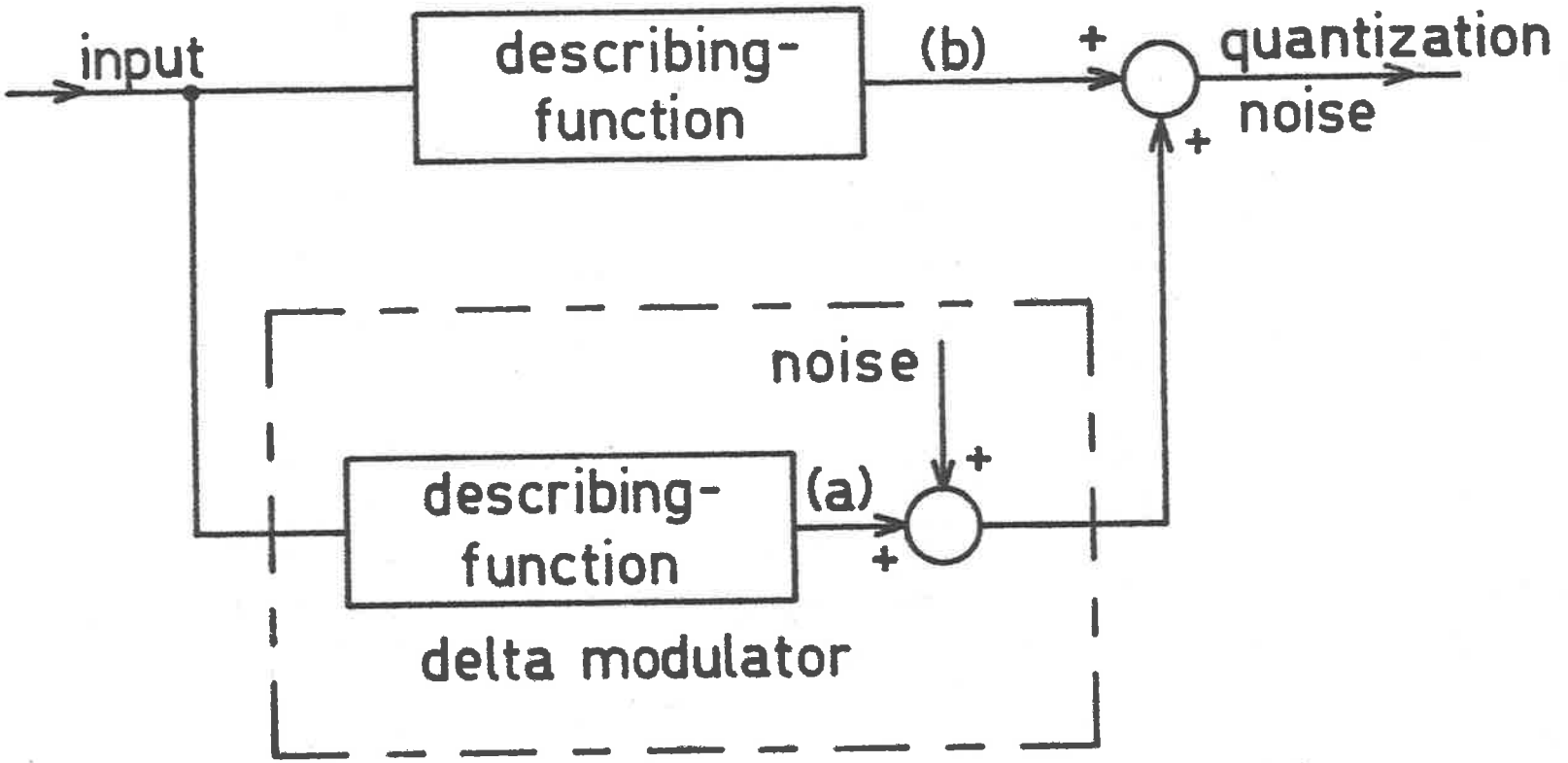


FIG. 2.6
Using the describing function to obtain the quantization noise

However since one is interested in the signal to noise ratio the gain of the delta modulator has to be allowed for.

The signal to be used for calculating the signal to noise ratio is the output signal from the describing function (i.e. at point (a) in fig 2.5 and 2.6). Unfortunately this signal is ficticious and thus unobtainable. When the test equipment is adjusted properly however the signal at point (b) in fig 2.6 is identical to the signal at point (a) which is the desired signal. The output of the cancellation network can thus be used to obtain the signal power.

The signal and quantization noise powers can be obtained by squaring and averaging the signal and noise voltages. The squaring can be achieved by using IC multipliers with the two inputs tied together. If speech is used as input signal, in order to minimise the effect of different power levels due to each syllable, a long averaging time typically between 10 and 100 seconds should be used.

2.5 Hardware Description

The following section describes some aspects of the practical realization of the ideal concepts expressed in the previous section.

Since the details of the circuitry will vary depending on the availability of certain IC's, no circuit details will be discussed in the main text. They are however presented in Appendix 2.1.

Some of the techniques used to obtain the required functions are worth mentioning. The block diagram of the equipment is shown in fig 2.7.

2.5.1 Tapped Delay Line

The easiest method of obtaining a variable delay is by the use of a tapped delay line. The delay line can either use:

1) analogue elements, such as a series of Bessel filters or a series of allpass networks. The time delay obtained by a series of RC networks is discussed in Appendix 4.3.
2) digital elements, such as a series of flipflops. The digital elements have the advantages that the per stage delay can easily be controlled. The disadvantage is however that the analogue input signal must be converted to binary signal.

The easiest way to convert the binary signal into an analogue signal is by delta modulation, or delta sigma modulation [4]. This modulation process produces quantization distortion which must be allowed for. Fig 2.8 shows a block diagram of a system where 2 waveforms are produced, the relative delay of which can be varied. Furthermore since both the waveforms are obtained by the same process, the waveforms will be identical if the demodulators are matched properly, eliminating the effect of quantization distortion. The quantization distortion in each waveform is minimized by a high sampling frequency for

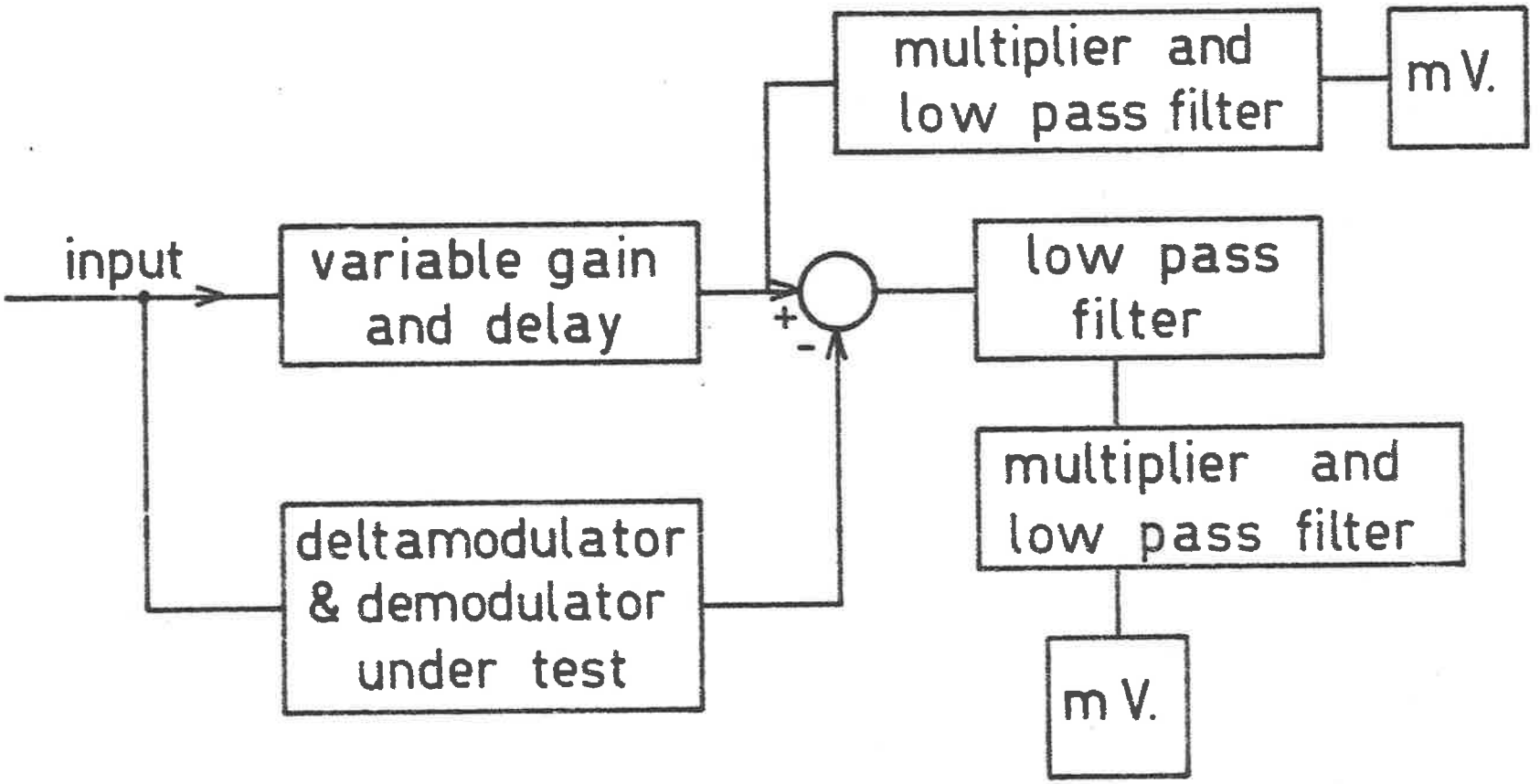


FIG.2.7
Block diagram of the measuring equipment.

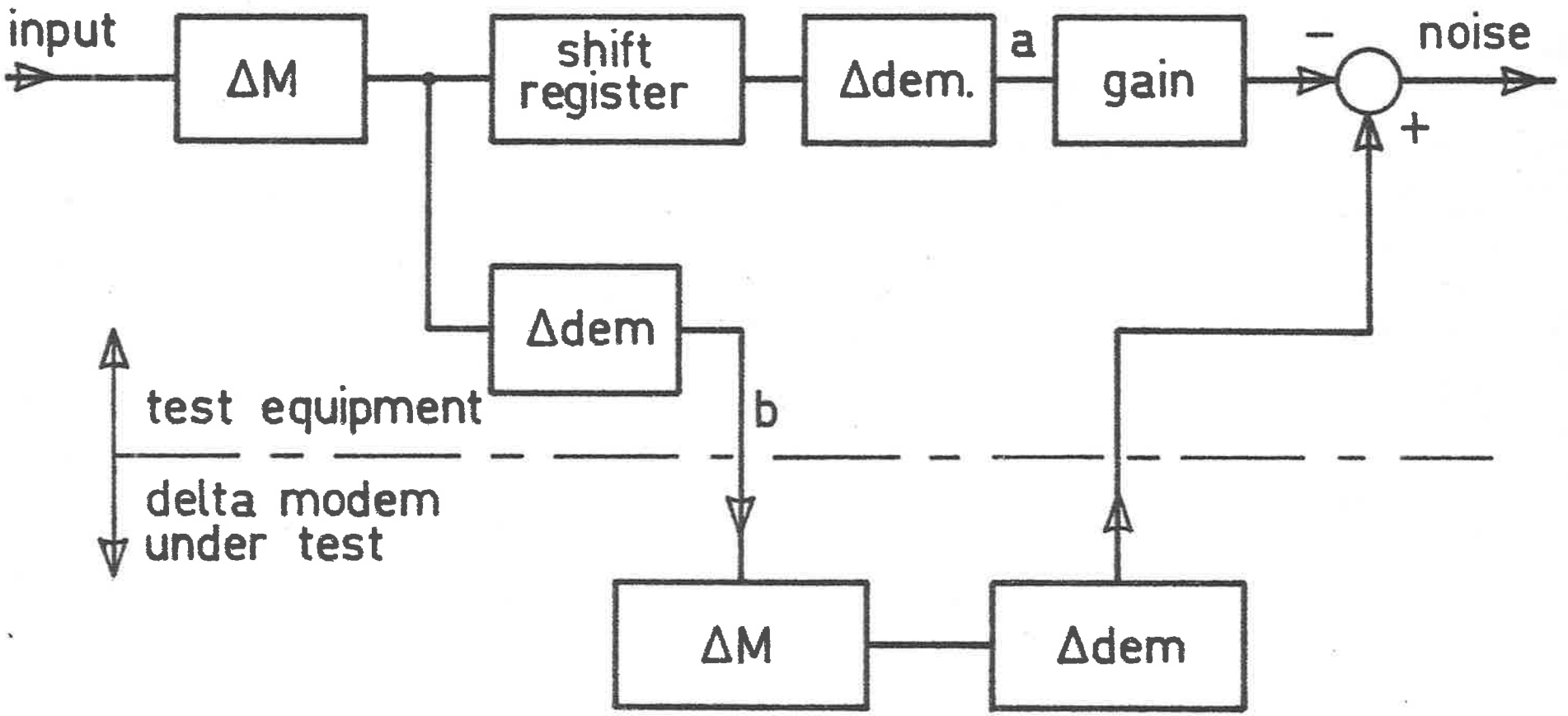


FIG.2.8
Method for obtaining a variable time delay.

the delta modulator in the delay line. The undelayed output of the delay line can be used as input to the delta modulator or pulse code modulator under test and the delayed output can be used to compare with the demodulated output.

The resultant system will thus produce two identical waveforms, the time delay between which is variable and independant of frequency.

The above method was used in the construction of the test equipment. By careful matching of the delta demodulators and the lowpass filters, the difference between the waveforms at points (a) and (b) in fig 2.8 can be made less than 50dB below the signals at point (a) and (b), enabling SNR's of up to 50dB to be measured.

2.5.2 Power Measurement

When the research described in this thesis was started analogue multipliers were not readily available, so that the SNR was computed from the average rectified values rather than the RMS values. The results presented in [19] were obtained this way. (Obviously in order to compare the calculated and measured results, the SNR was evaluated by both methods during the computer simulation, but the error was found to be less than 1.5dB)

Recently IC analogue multipliers became available and test equipment was reconstructed using these in order to measure the actual signal and noise powers.

The output of these multipliers is filtered by the use of an RC network with a time constant of 25 seconds, giving the mean square voltage. This long time constant is necessary in order to eliminate variations of power due to pauses and syllabic variations in speech.

2.5.3 Accuracy Considerations

In order to reduce the effect of the quantization noise due to the delta modulator in the tapped delay line, this delta modulator is operated at nearly constant power, corresponding to the optimum performance. Any variation of signal power required for input to the delta modulator under test is obtained by the use of operational amplifiers after the delay line delta demodulators.

The gain of these amplifiers can be varied in approxim approximately 6dB steps over an 80dB range.

The quantization noise can also be amplified, so that the multipliers can be operated at a constant power level to obtain the most accurate results and to minimize the effects of drifts. The resultant block diagram is shown in fig 2.9.

Knowing the multiplier outputs and the gain of the amplifiers, the signal and noise powers and hence the signal to quantization noise ratio can be calculated.

2.5.4 Results

The results obtained with the measurement equipment are

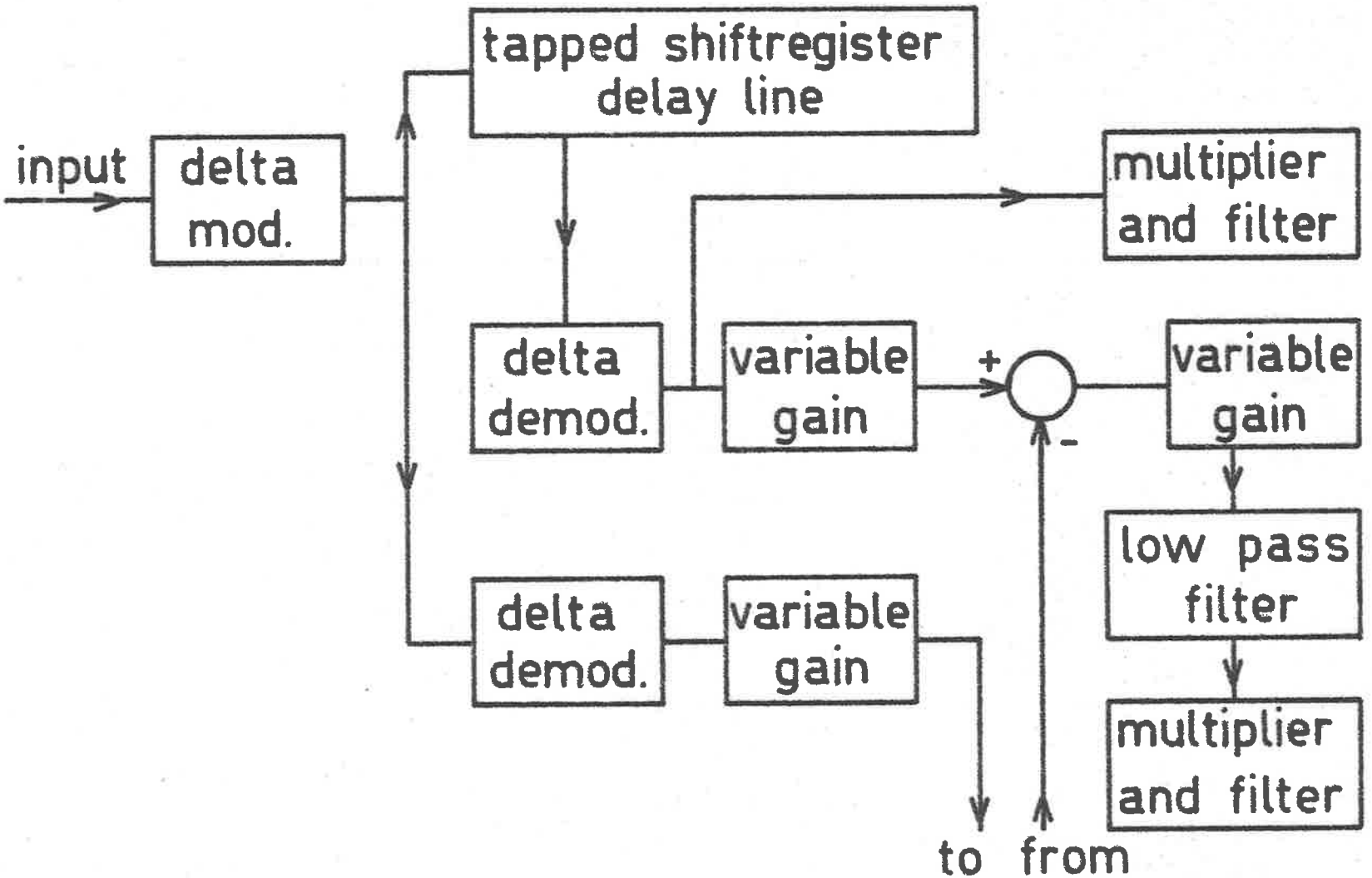


FIG.2.9 Final block diagram of the measuring equipment.

discussed in chapters 3 and 4, where the delta modulators developed during the research are discussed, together with a comparison with the calculated performance.

Fig 2.10 shows a comparison between the performance of NDDM which is described in the next chapter, obtained from:

(a) the notch filter method and

(b) the measuring equipment.

The results can be seen to agree closely except for large input power, where the notch filter method gives optimistic results.

The differences at small input power are due to the background noise (switching spikes and thermal noise) causing a reduction in accuracy of the measurements.

2.6 Conclusions

This chapter has shown the desirability of testing a delta modulator or pulse code modulator, under actual operating conditions. If, as is common practice, a delta modulator to be used with speech is tested by using sinewaves, a misleading estimate of its performance can result.

Equipment has been developed which will enable the SNR of a delta modulator to be determined when this delta modulator is subject to random inputs such as speech. This equipment enables one to assess the performance of a delta modulator or pulse code modulator under actual operating conditions.

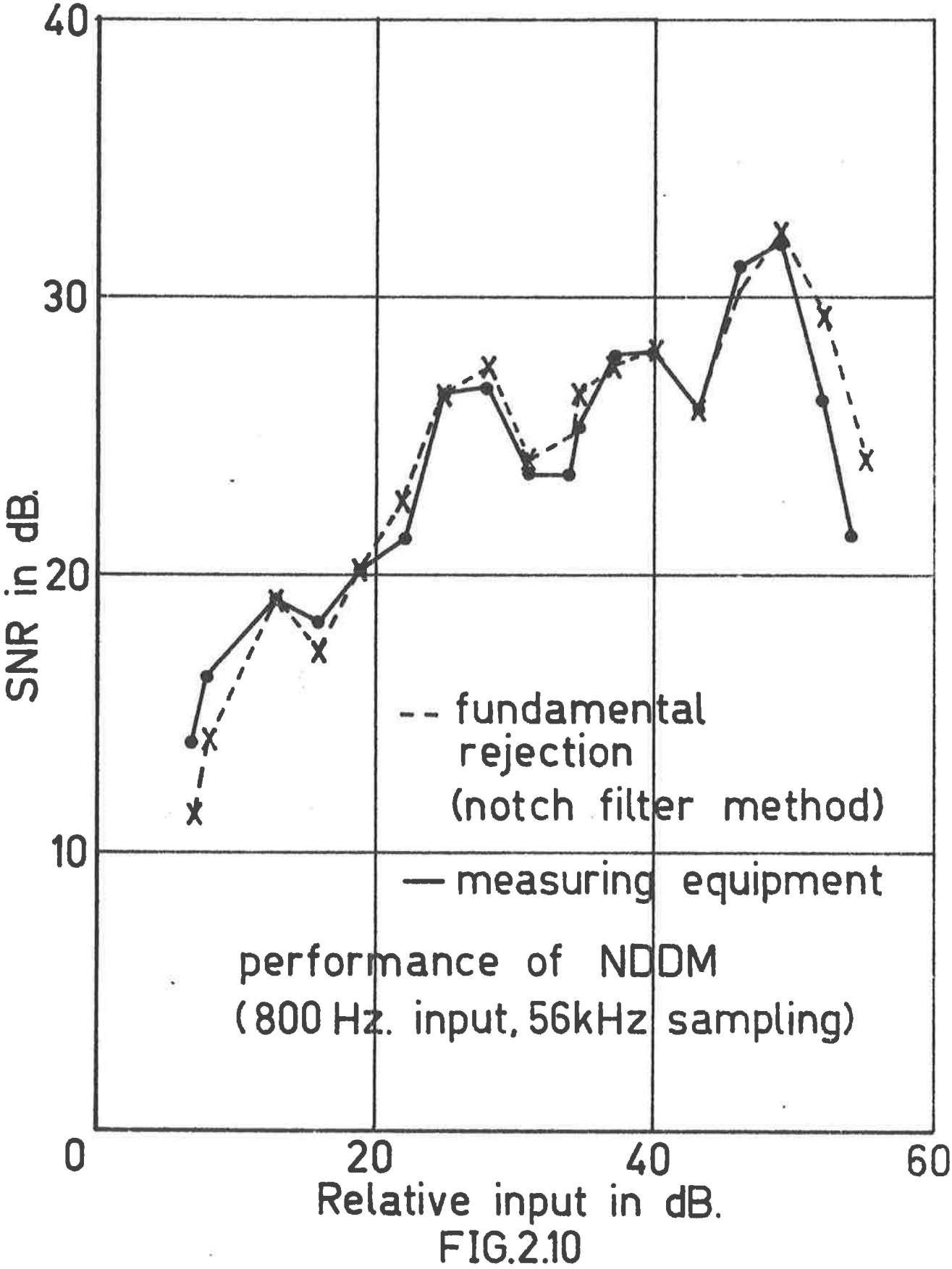

40
30
20
10
0
SNR in dB.
20
40
60
Relative input in dB.
-- fundamental rejection (notch filter method)
— measuring equipment
performance of NDDM
(800 Hz. input, 56kHz sampling)

FIG.2.10

CHAPTER 3

THE DEVELOPMENT OF NONLINEAR DIGITAL DELTA MODULATION

3.1 Introduction

In this chapter the development, design criteria and the performance of nonlinear digital delta modulation (NDDM) are discussed.

Instantaneous companding is used in double integration delta modulation (DIDM) [2]. However this makes the system less stable, causing a deterioration of the performance due to large amounts of overshoot. The use of digital techniques, together with nonlinear counting procedures enables instantaneous companding with good stability to be obtained.

Because the stability can be increased by the nonlinear counting developed by the author, the companding ratio and thus the dynamic range of NDDM is 30dB larger than those for the systems described by Abate [8] and Bosworth and Candy [9].

3.2 Instantaneous Companding

3.2.1 Principles of Instantaneous Companding

The dynamic range of a delta modulator can be increased by altering the gain of the local demodulator, to suit the input signal. This is known as companding.

Depending on the rate of change of gain of the local demodulator, the companding can be divided into 2 classes,

namely instantaneous companding and syllabic companding. In instantaneous companding, the gain is changed rapidly. For NDDM, the gain can change 40dB in 5 clockpulses and the delta modulator can thus track instantaneous variations of the input signal.

With syllabic companding, the gain is changed more slowly, so that the delta modulator can track variations of the average power.

Referring to fig 1.2 it can be seen that for single integration delta modulation (SIDM) which uses no companding, the change of demodulated output per clockpulse is fixed. This change in demodulated output is called the step size. Companding changes the step size. The step size is usually normalised to make the smallest step size unity.

A simple form of companding is used in DIDM [2], by the use of 2 integrators in the feedback loop. However because the 2 integrators produce a 180° phase shift and a further delay is produced by the sampling process, oscillations can occur over a wide range of frequencies, often resulting in an audible output.

The stability can be improved by the use of what is known as "prediction", where the network in fig 3.1 replaces the 2 integrators in the feedback loop. The network no longer has a phase of 180° and by the proper choice of Rp, stable operation can be obtained.

From the description of DIDM it can thus be seen that

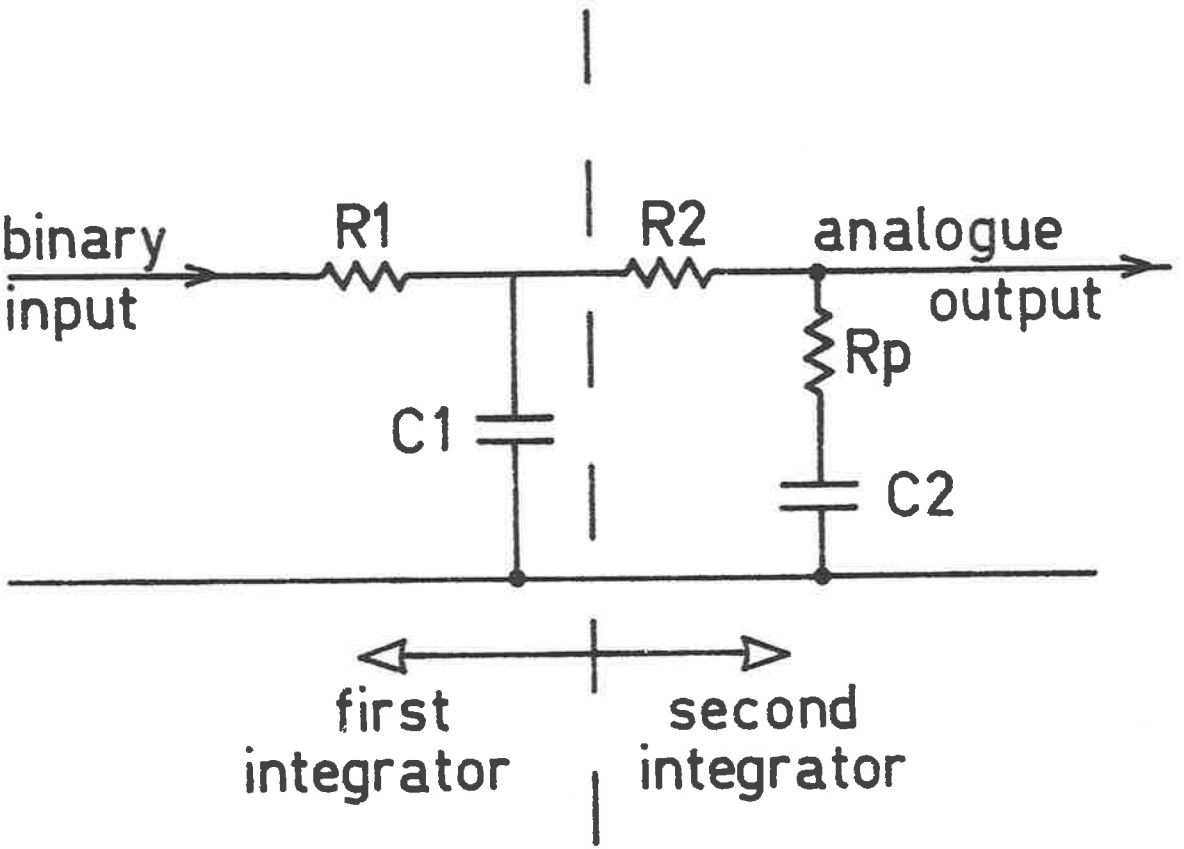


FIG.3.1
Double integration network with prediction

the usefulness of instantaneous companding is sometimes limited by a decrease in stability and the consequently large amounts of overshoot.

Other systems using instantaneous companding are described in section 1.2.2, but since NDDM was developed from DIDM in an attempt to overcome some of the disadvantages of DIDM, the principles of operation of NDDM will be compared with those of DIDM.

3.2.2 Dynamic Range Considerations

The step size of DIDM changes linearly with time as can be seen by comparing different step sizes in table 3.1. (The change in step size is related to the magnitude of the input voltage of the first integrator, which is the magnitude of the binary transmitted signal, which is constant. The step size is normalized to make the smallest step sizes plus and minus one, the difference between them is two.)

Consider an 800Hz input signal to a delta modulator with a sampling frequency of 56KHz. There will be about 18 clockpulses per quarter cycle and the maximum step size will be 36 (= 2 x 18). The companding ratio, which is defined as the ratio of the largest to the smallest step size, is thus approximately 30dB for an 800Hz input signal. The companding ratio is related to the dynamic range and if an extension of the dynamic range is required the companding ratio has to be increased.

TABLE 3.1

Step Number	SIDM	Step Size DIDM	NDIM
-6		-11	-320
-5		-9	-130
-4		-7	- 44
-3		-5	- 15
-2		-3	- 5
-1	-1	-1	- 1
1	1	1	1
2		3	5
3		5	15
4		7	44
5		9	130
6		11	320

(The step sizes for NDDM are discussed in section 3.3.2)

3.2.3 Nonlinear Instantaneous Companding

The dynamic range can be increased by increasing the change of step size for large step sizes. This can however not be done by adding a third integrator, since this would give a phase shift of more than 180° and instability would result. Thus nonlinear methods must be used, as is indicated in fig 3.2.

The required nonlinearities can be generated by either analogue methods or digital methods. With analogue methods, diodes or other nonlinear devices are used to produce voltage dependant transfer functions, so that the change of step size can be made dependant on the step size. If the demodulated output from the local demodulator and the receiver demodulator are to be the same, the nonlinearities in the transmitter and receiver must be closely matched. Any mismatch will create distortion. Since diode characteristics depend on temperature and the transmitter and receiver are likely to be at different temperatures, a mismatch of nonlinearities will normally occur. Furthermore, supply voltage variations and a spread of component values will aggravate the problem.

These problems can be overcome by the use of digital techniques, where digital circuitry selects the step size to be used. Normally the information indicating an increase or decrease in step size is obtained from the binary signal. Since this binary signal is available at both the transmitter and receiver, the step size will be identical at the

The use of a nonlinear element to obtain instantaneous companding.

FIG.3.2

transmitter and receiver, provided no transmission errors have occurred.

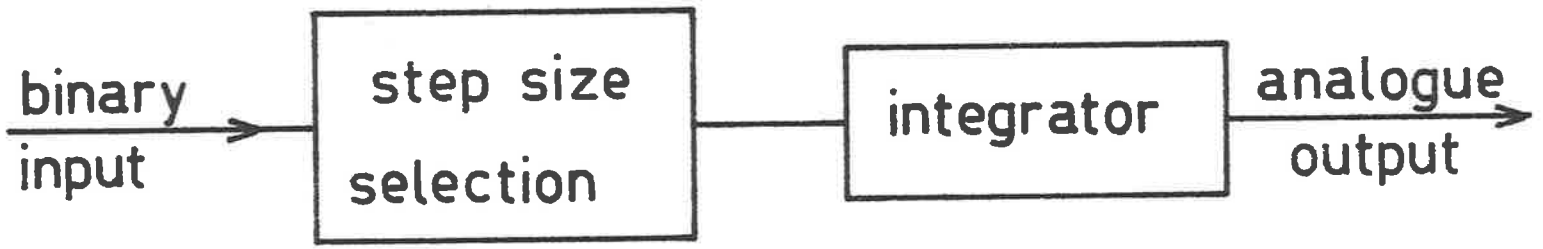
Because digital circuitry is used to select the step size, only a limited number of step sizes can be used. For DIDM at 800Hz and maximum amplitude, only 36 different step sizes are used, 18 positive step sizes and 18 negative step sizes, so that a finite number of step sizes can be used in practice. The local cemodulator can now be represented by the block diagram in fig 3.3.

There are many practical ways by which this block diagram can be realized, 3 different methods are shown in fig 3.4. Referring to fig 3.4 (b) it can be seen that the step size is represented by a resistor, which is switched to either the positive or negative rail. Since each step size is represented by a resistor there are no limitations on step size and the step sizes can be optimized for the normal operating signal of the delta modulator, which is speech in this thesis.

Prediction will however generally no longer be sufficient to maintain stability. The stability of the delta modulator must thus be improved if the dynamic range is to be extended by this method.

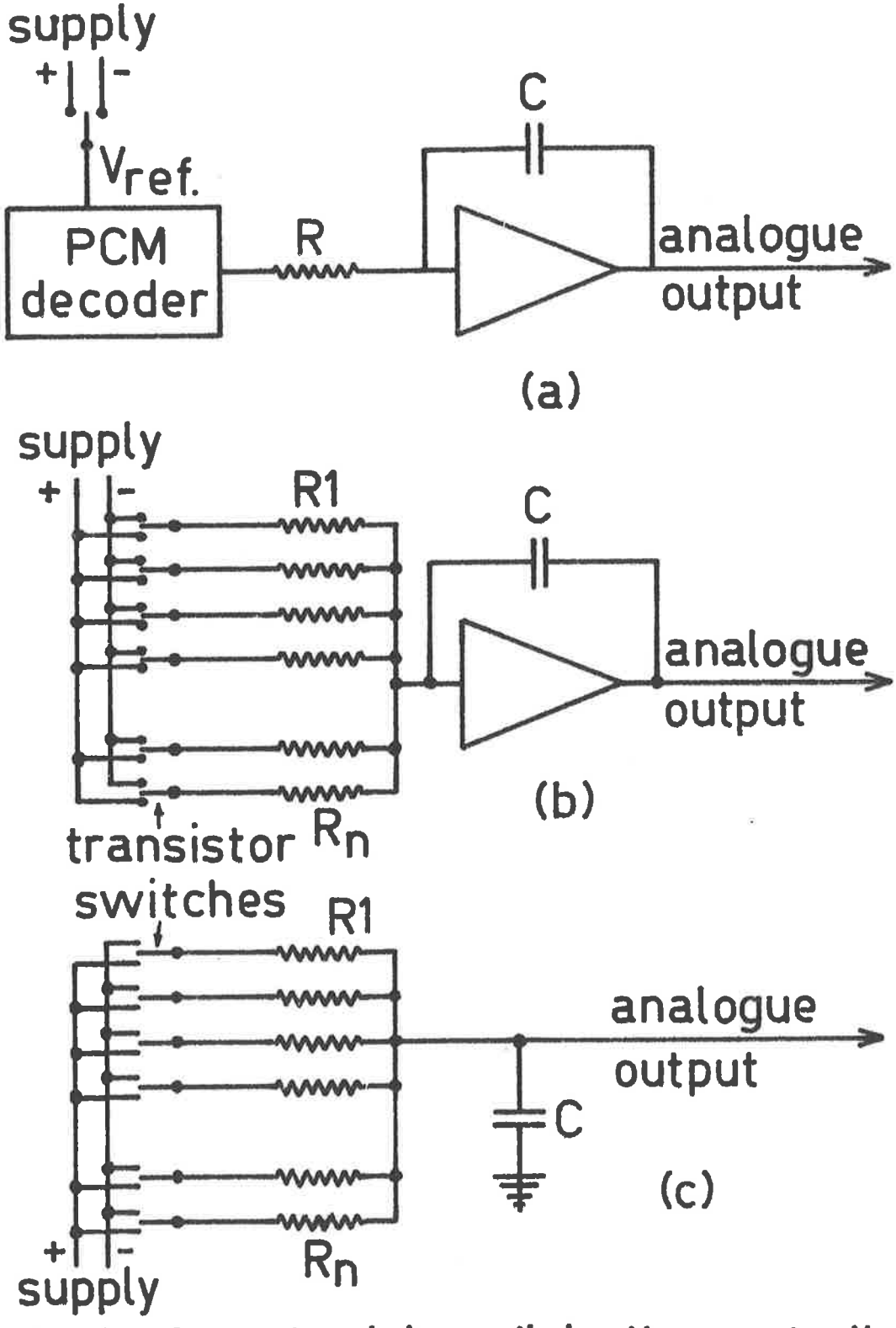
3.2.4 Improvement of Stability

In section 3.2.1 it was stated that DIDM without prediction was unstable. A good test for stability is to



Block diagram of a demodulator with digital companding

FIG.3.3



Methods for obtaining digitally controlled companding FIG.3.4

apply a step input to the delta modulator and observe the resulting demodulated output. Fig 3.5 (a) shows the step response of DIDM without prediction. It can be seen that the system is unstable. Fig 3.5 (b) shows the step response of DIDM with prediction. Oscillations can however still occur, as is shown in fig 3.5 (c)

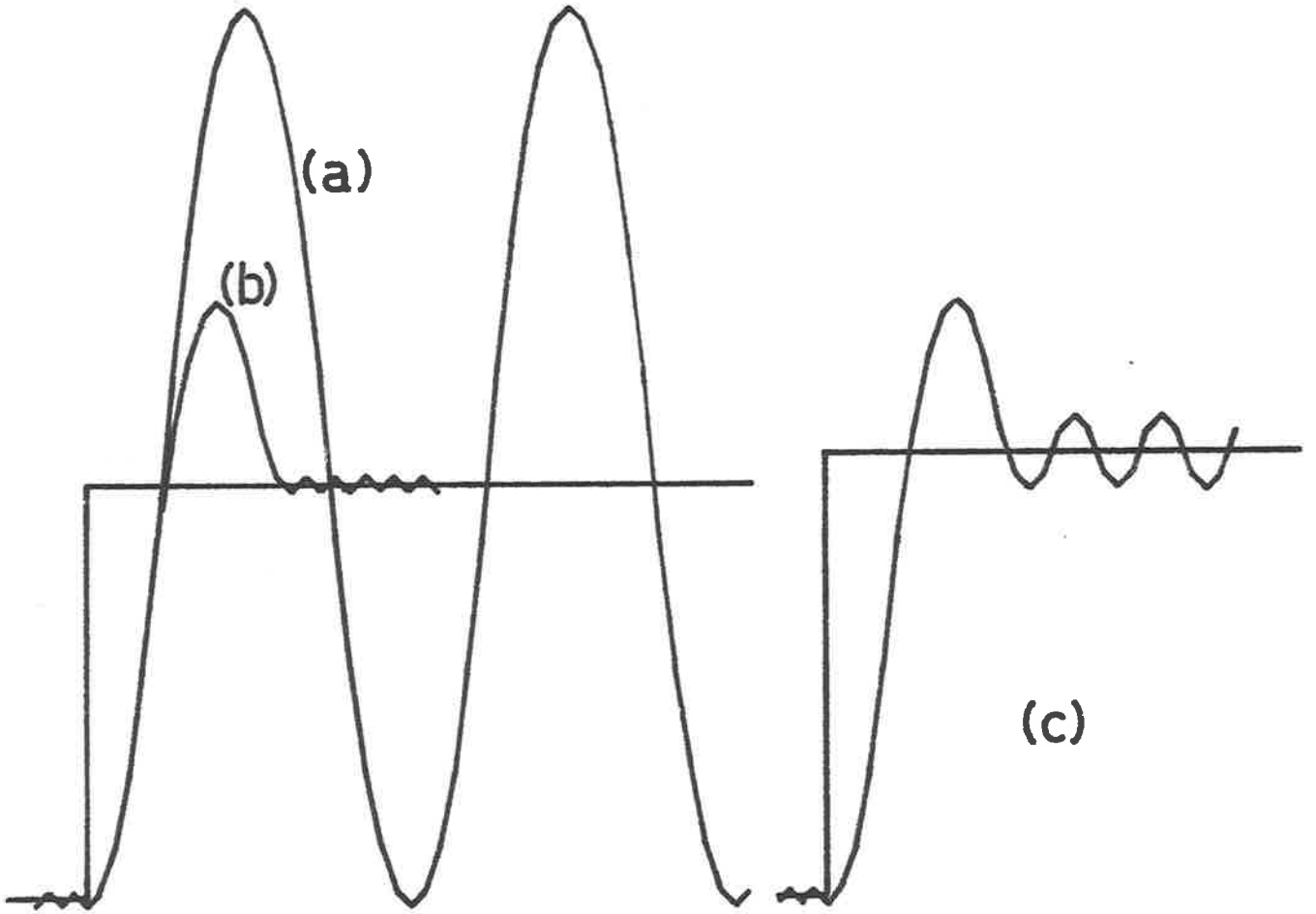
In DIDM the step size is changed by a fixed amount during each sampling interval. The stability can be improved by changing the step size more than the normal 2 units when certain conditions occur.

From fig 3.5 (a) it can be seen that if the step size is reduced more quickly after the desired output voltage is obtained, i.e. after a change of the binary transmitted signal has occurred, the overshoot will be reduced. In other words if the step size is changed by X units, instead of 2 units, when a change of binary transmitted signal occurs, the stability of the delta modulator will be improved.

The idling pattern (10101010 etc.) has a change of binary signal occurring at every clockpulse. In order to minimize the quantization error, it is desirable to make this idling pattern correspond to the minimum step size, i.e. $\pm$ 1.

If the step size is changed by X units at every change in binary transmitted signal, the idling pattern will correspond to the step sizes $\pm$ X/2 while the required step size is $\pm$ 1.

A further condition must thus be satisfied namely: If



Step response of double integration delta modulation,(a)-without prediction and,(b)and (c)-with prediction

FIG.3.5

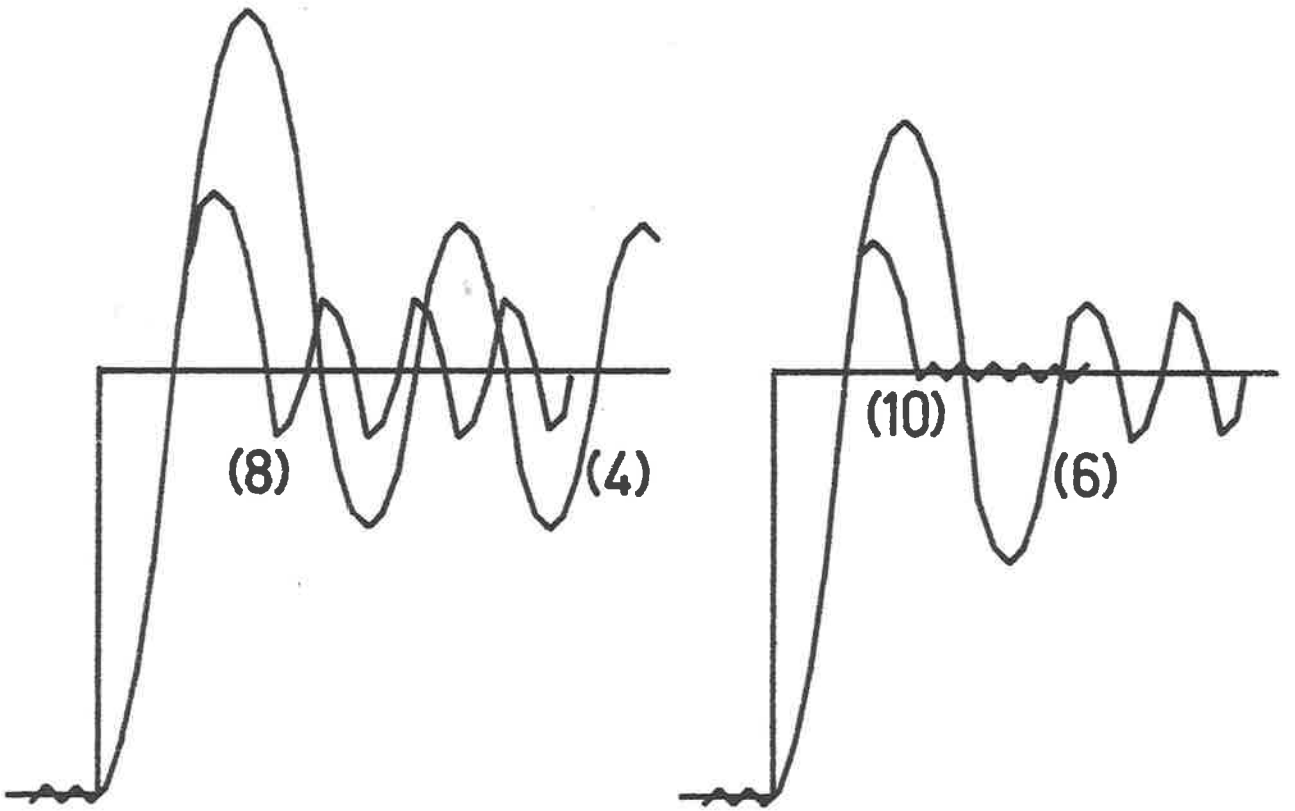
the change in step size results in a step size of opposite sign to the previous step size, the new step size is the smallest step size of opposite sign to the previous step size. size.

If for instance the step size is + Y units and it is reduced by X units, where X>Y, a negative step size results and the step size used is not Y-X units but -1. This rule will achieve the required idling pattern.

Fig 3.6 shows the step response of DIDM with conditional nonlinearities when the step size is changed by 4,6,8 and 10 units when the previously mentioned conditions are satisfied. Comparing fig 3.6 with fig 3.5 (a) it can be seen that the stability has been increased. The step response in fig 3.6 is evaluated for nonlinear counting without prediction and oscillations can still occur. Absolute stability will be obtained if prediction is incorporated as well, enabling the companding described in section 3.2.3 to be implemented.

3.2.5 Error Performance

In a practical delta modulator system, transmission errors will occur. It is desirable to minimize the effect of transmission errors. A compromise must however always be made. As the performance of the delta modulator is improved, the information contained in the binary signal must increase, so that the redundancy in the binary signal will decrease



Step response of DIDM with conditional nonlinearities. The conditional change is indicated by the numbers

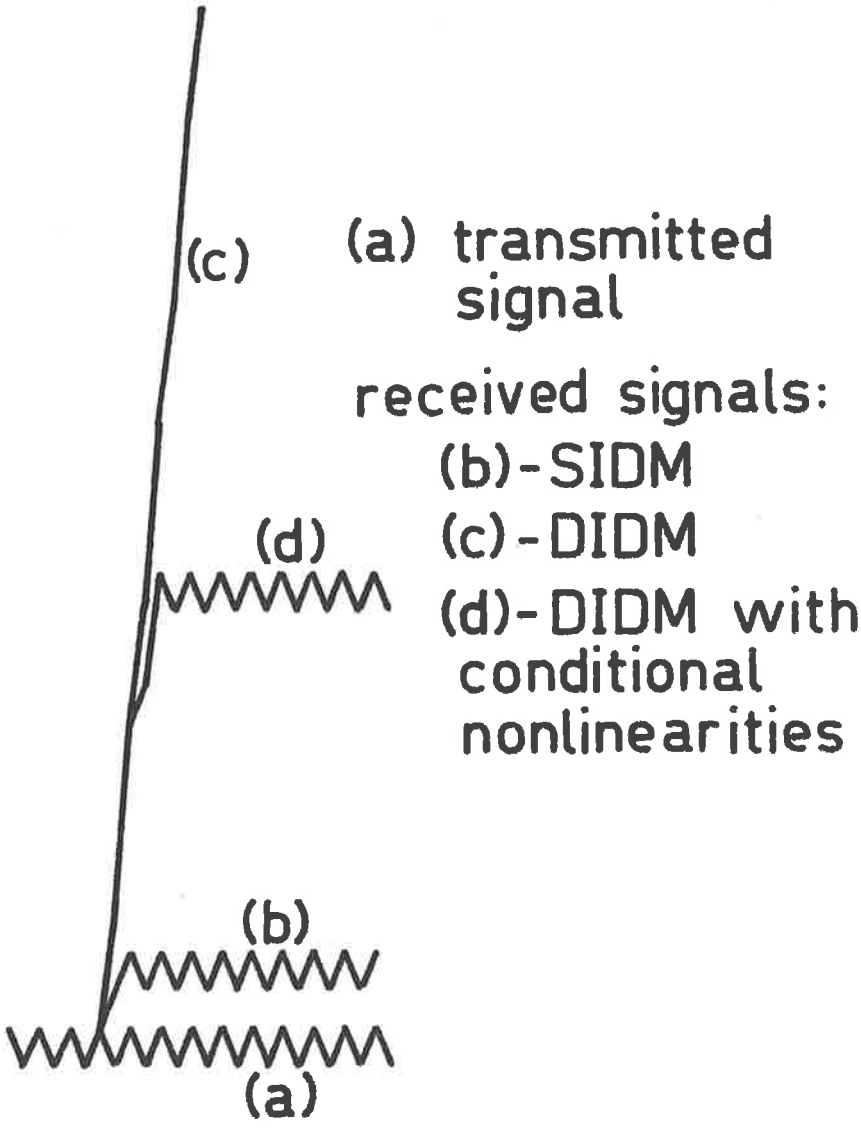
FIG.3.6

and the effect of errors will increase.

For the delta modulator to be useful however, the effect of a transmission error must diminish with time, i.e. the error caused by a single transmission error must not persist indefinitely. Fig 3.7 (b) shows the effect of a single transmission error on ideal SIDM and DIDM systems.

For SIDM the error causes a DC shift in the output signal, which will not produce a lasting audible effect since the ear is not sensitive to absolute pressure even if the reproducing system were capable of responding to it. For DIDM the error causes a bias on the step size, which causes the output to increase until limiting occurs in the hardware, making the system useless. The first integrator in the DIDM system must be leaky, so that the effect of errors diminish with time. Since it is intended to replace the first integrator with digital circuitry, leakyness must also be incorporated in the digital circuitry. Leakyness causes a gradual decrease in magnitude of the step size if a 1010 etc. binary pattern is applied, until the step size $\pm$ 1 are obtained. The required leakyness can be achieved by changing the step size by X units only when the magnitude of the step size is decreased as well as satisfying the previous requirement of a change in binary signal. This further requirement will not change the step response indicated in fig 3.6.

Fig 3.7 (b) shows that the effect of a transmission error decreases with time, as required. The resultant DC offset



Effect of a transmission error

FIG.3.7

does not effect the performance markedly since firstly, the ear is insensitive to absolute pressure and secondly, the DC error will decay if analogue integrators are used for the second integrator, since all analogue integrators have a finite leakyness and thus a finite memory. Comparing fig 3.7 (b) and fig 3.7 (a) it can be seen that because each transmitted bit carries more information due to the companding, the effect of a transmission error for NDDM is worse than for SIDM.

The resulting system, incorporating the features mentioned in sections 3.2.3, 3.2.4 and 3.2.5 is called Nonlinear Digital Delta Modulation (NDDM).

3.2.6 Summary of Companding Strategy

The requirements outlined in sections 3.2.4 and 3.2.5 can also be written in terms of step numbers instead of step sizes and it can be seen from table 3.1 that this has some advantages when the step sizes are varied as proposed in section 3.2.3. Changing the step size by X units now corresponds to changing the step number by N_X units.

The companding strategy will now become as follows:

(1) The step number is controlled by the binary transmitted signal.

The step number is increased if the binary signal is a one and decreased if the binary signal is a zero.

(2) The magnitude step number is increased by one if no

change in binary transmitted signal occurs at the clockpulse concerned.

(3) The step number is changed by N_x units if a change in binary signal occurs and the magnitude of the step size is decreased as a consequence of this change, provided that if a change in the sign of the step size occurs, the new step size becomes the smallest step size of the opposite sign to the previous step size.

3.3 Optimization

3.3.1 Aims of Optimization

In the previous section a new type of delta modulator denoted as NDDM was proposed, removing some of the restrict restrictions placed on DIDM. There are 4 basic variables that must be chosen, each of these will have an effect on the performance. The following questions must be answered:

1) Prediction: Is prediction to be used and if so how much?
2) Stabilization: By how much does the step number have to change on a change of binary signal to obtain the best performance?
3) Step sizes: Which step sizes give the best performance?
4) Leakyness in the Integrator: How much leakyness is required for the best performance?

It is difficult to optimize all of these quantities, since each one will affect the other. For example if a large change in step size occurs, more stabilization is required to keep the system stable.

The relative ratio of the step sizes will depend on the specific application of the delta modulator.

A compromise between SNR and dynamic range must be made and the optimization must then be carried out to maximize the performance according to the criteria specified.

For NDDM it was decided to use simulated speech and to optimize the step sizes such that a flat SNR curve is obtained over as wide a range as possible. Alternatively it is possible to select the step sizes such that the highest possible SNR is obtained from the delta modulator.

3.3.2 Selection of Parameters

1) Prediction

Since prediction increases the stability of the delta modulator, without significantly affecting the performance of the delta modulator, prediction was used in NDDM. A prediction of one clockpulse was used, which is the same amount of prediction as is usually used in DIDM and means that the voltage across the prediction resistor corresponds to the step size, so that the output from the local demodulator is a stepsize more than the output from the demodulator at the receiver.

2) Stabilization

Increasing the stabilization by increasing the change in step number when a change in binary signal occurs, normally increases the grannulation noise i.e. the quantization noise. The increase in stabilization will however reduce the overshoot due to rapid changes of the slope of the input signal and will thus reduce the slope overload noise. A compromise must thus be made between slope overload and grannulation noise. For the optimization, a change of 2 steps on a change of binary sign was chosen since this gives sufficient stabilization without increasing the grannulation noise too much. After optimization of the step sizes, the above assumption can be checked to make sure that the best performance has been obtained.

3) Step Size

The step sizes were obtained by successive optimization.

If the required step sizes are $\pm$ 1, $\pm$ A, $\pm$ B, $\pm$ C, $\pm$ D, $\pm$ E, etc., one must find A,B,C,D, etc. such that the best performance is obtained. The constants A,B,C,D etc. are obtained by successive optimizations. This optimization was carried out using computer simulation, as described in chapter 5, with simulated speech, without syllabic variations of power, as input. A flat SNR curve over as wide a dynamic range as possible was aimed for. This optimization resulted in the step sizes indicated in table 3.1. From the computer simulation it was found that each step size affected the

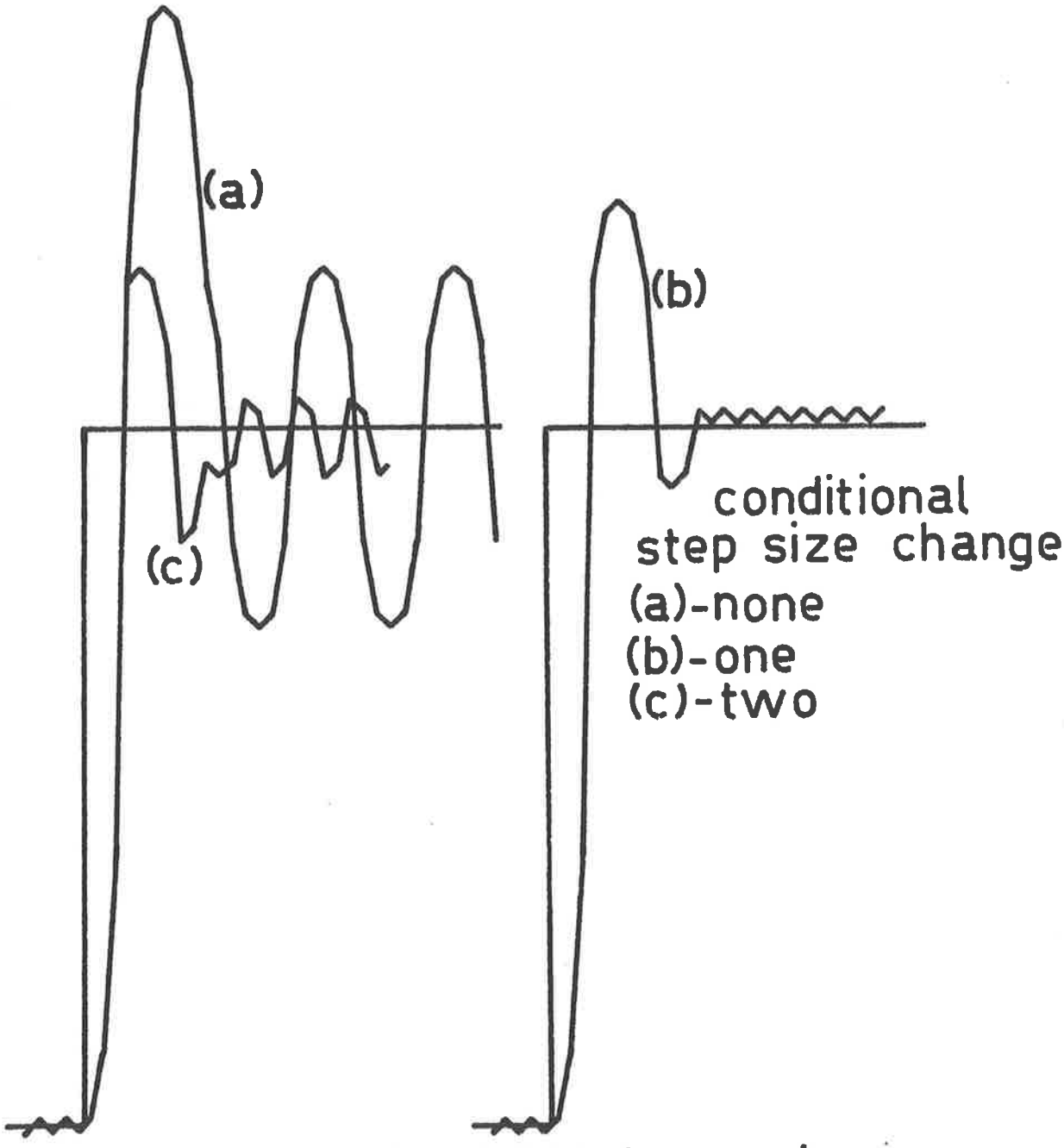
performance of the modulator only over a narrow range of input power and that there is little interaction between the step sizes, so that the optimum performance can be obtained by successive optimization. No improvement in performance could be obtained by using more than the 12 step sizes indicated. The step sizes ± 320 only resulted in a marginal increase in dynamic range (2dB) and were not incorporated in the hardware, because the extra complexity was not justified by the marginal increase in performance.

After the step sizes are obtained, one can check whether the correct stabilization is chosen. Fig 3.8 shows different stabilization applied to NDDM with the step sizes as in table 3.1. It can be seen that adequate stability is obtained if the step size is changed by two steps instead of one for a conditional nonlinearity, so that the initial assumption is correct.

4) Leakyness in the Second Integrator

The optimum amount of leakyness in the analogue integrator must now be determined. This again must be a compromise. As leakyness is increased the performance will decrease but the tolerance to errors will increase. Fig 3.9 shows the effect of the leakyness on the performance.

The leakyness is expressed as a percentage, indicating the percentage decay during one sampling interval. A leakyness of 3% was chosen since this gives a good SNR and also a reasonable tolerance to errors.



Step response of NDDM for various nonlinearities FIG.3.8

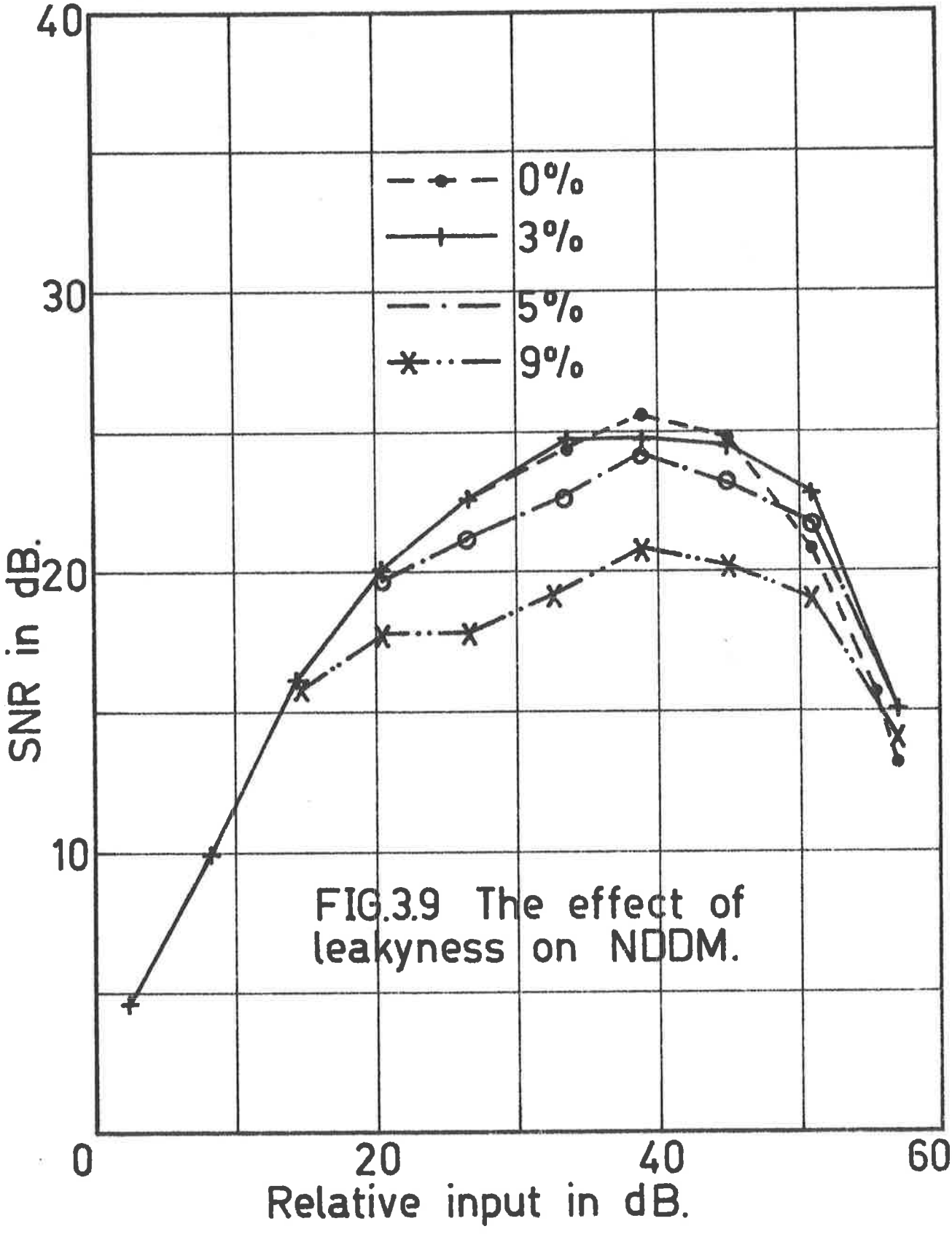


FIG.3.9 The effect of leakyness on NDDM.

3.3.3 Accuracy Considerations

The optimization was carried out by means of computer simulation using the Control Data Corporation (CDC) 6400 at the University of Adelaide. Because of cost limitations, the program time was kept as short as possible. The simulation was carried out in the time domain, so that only a relatively small number of sampling intervals could be studied and from the performance of the delta modulator during this interval a judgement on the overall performance of the delta modulator could be made.

A compromise was necessary between the cost of running a longer program and the inaccuracy of the performance that a shorter program would give.

The program time can be split up in 2 sections, firstly, a period for initialisation, to allow the steady state performance to be obtained and secondly, the period during which the performance is evaluated. Fig 3.10 shows the effect of different intervals during which the performance is evaluated. It can be seen that 3000 clockpulses enable the performance to be evaluated with reasonable accuracy. Since 3000 clockpulses at 56 KHz sampling frequency corresponds to approximately 0.05 sec., one can expect variations of the SNR to occur.

Fig 3.11 shows the variations in SNR that can be obtained when using 3000 clockpulses to calculate each point. It can be seen that for most of the dynamic range the results

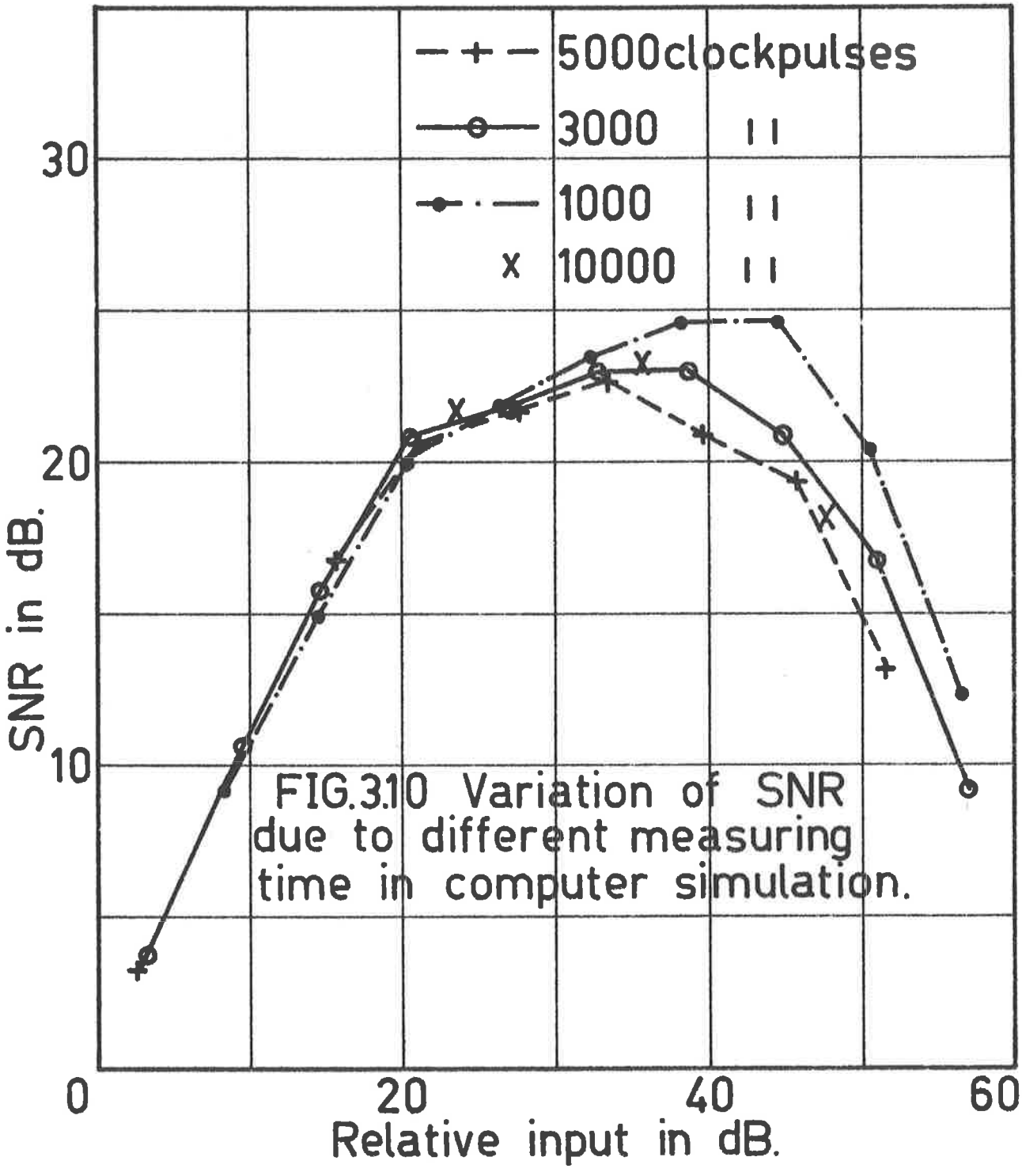


FIG.3.10 Variation of SNR due to different measuring time in computer simulation.

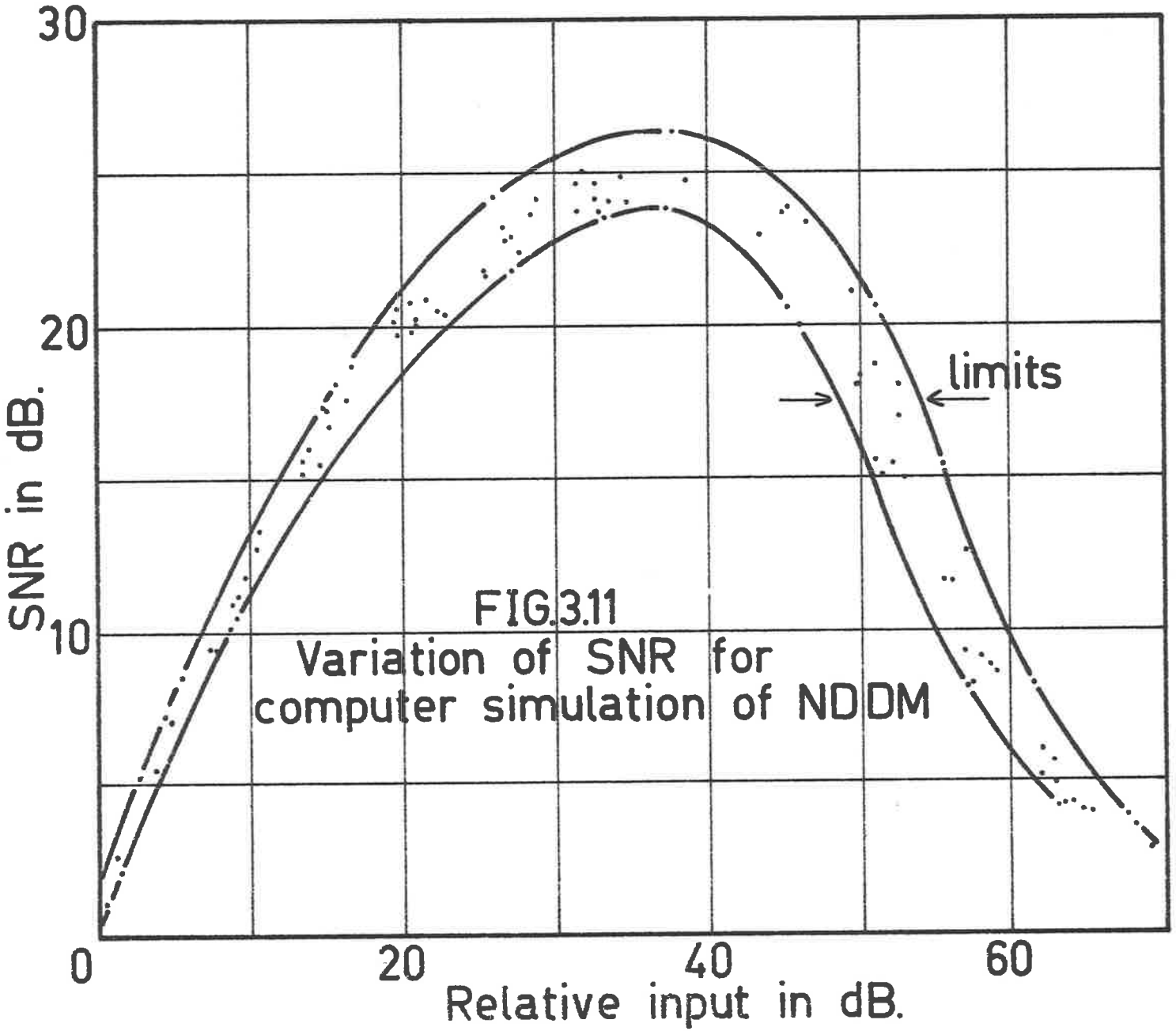


FIG.3.11
Variation of SNR for
computer simulation of NDDM

are within ± 1dB of the mean SNR curve, while all points are within ± 2.5dB of the mean SNR curve.

From this wide variation in SNR due to different signal conditions it is apparent that no exact optimization can be carried out, since the optimization for one particular time segment will be different from the optimization for another time segment. It can however be seen that the optimization is sufficiently accurate to give a good performance over a wide dynamic range.

Fig 3.12 shows a comparison between SIDM and HDDM, obtained by computer simulation, when simulated speech is used as input for both. It can be seen that by using the instantaneous companding the dynamic range has been increased.

3.4 Practical Realisation

3.4.1 Hardware

In the previous section the required switching strategy was stated as follows:
The step number is changed by 2 units instead of the normal one unit when a change in binary signal occurs and the magnitude of step size is reduced as a consequence of this, provided no change in sign of the step number occurs. The step number will be changed by one unit, if the above conditions are not fulfilled.

The block diagram of the digital circuitry is shown in

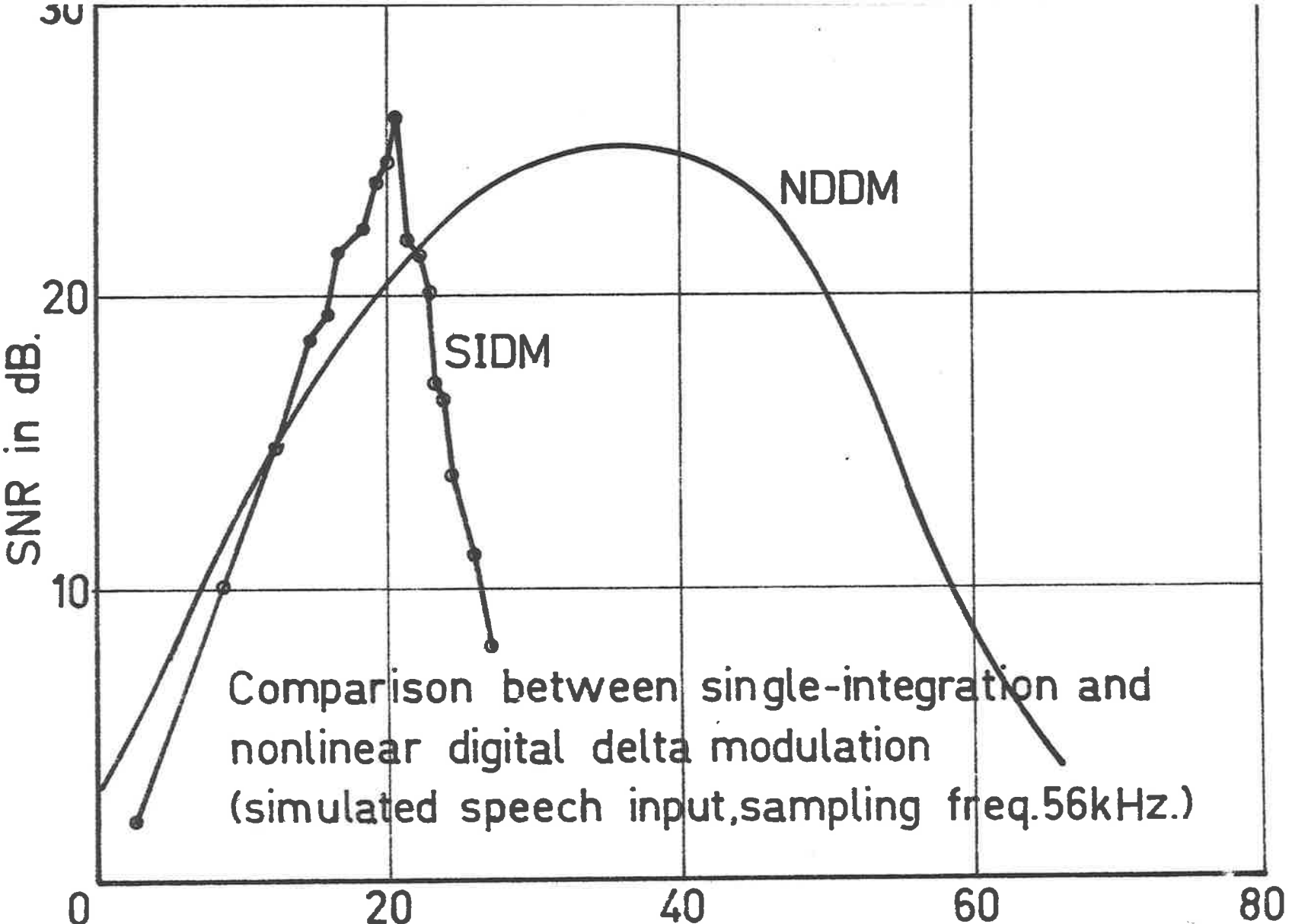

30
20
10
0
SNR in dB.
NDDM
SIDM
Comparison between single-integration and
nonlinear digital delta modulation
(simulated speech input, sampling freq. 56kHz.)
20
40
60
80
Relative Input in dB.

FIG.3.12

fig 3.13. The following action occurs at the sampling instant:

1) The binary transmitted signal is compared with the previous binary transmitted signal and a signal is produced if a change has occurred. The new binary transmitted signal also sets the counter to either forward or reverse counting.

2) A decision is made whether one or two step changes are required, this information is then stored in a flipflop.

3) Two pulses are generated and depending on the condition of the flipflop mentioned in (2) one or both are passed into the counter, setting the new step size.

The decoders control the step sizes by means of transistor switches as indicated in fig 3.4(c). For proper operation, the time taken to do steps (1) to (3) above should be much smaller than the sampling interval.

The complete circuit diagram is given in Appendix 2.3. Fig 3.14 shows a photograph of the hardware for the modulator. The demodulator is of similar complexity.

3.4.2 Results

Fig 3.15 shows the measured performances when speech is used as input, obtained with the equipment described in chapter 2, together with the results obtained by computer simulation. It can be seen that the calculated and measured results agree remarkably well. Fig 2.10 shows the measured performance of NDDM for an 800Hz sinewave input. These

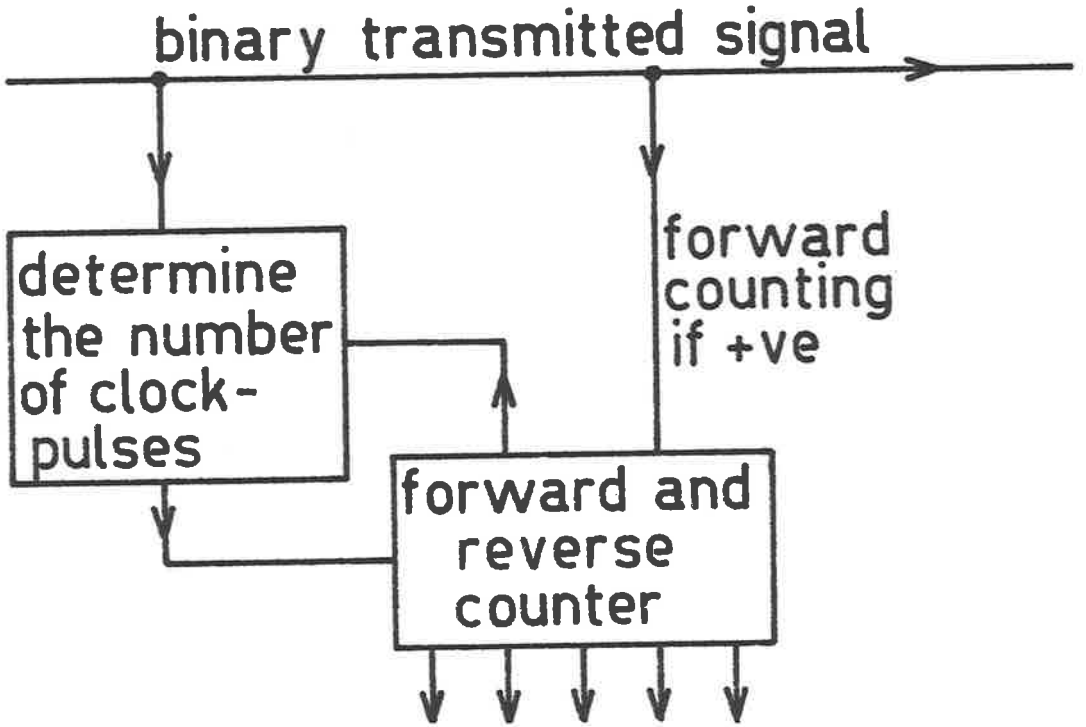


FIG.3.13 Digital circuitry of NDDM.

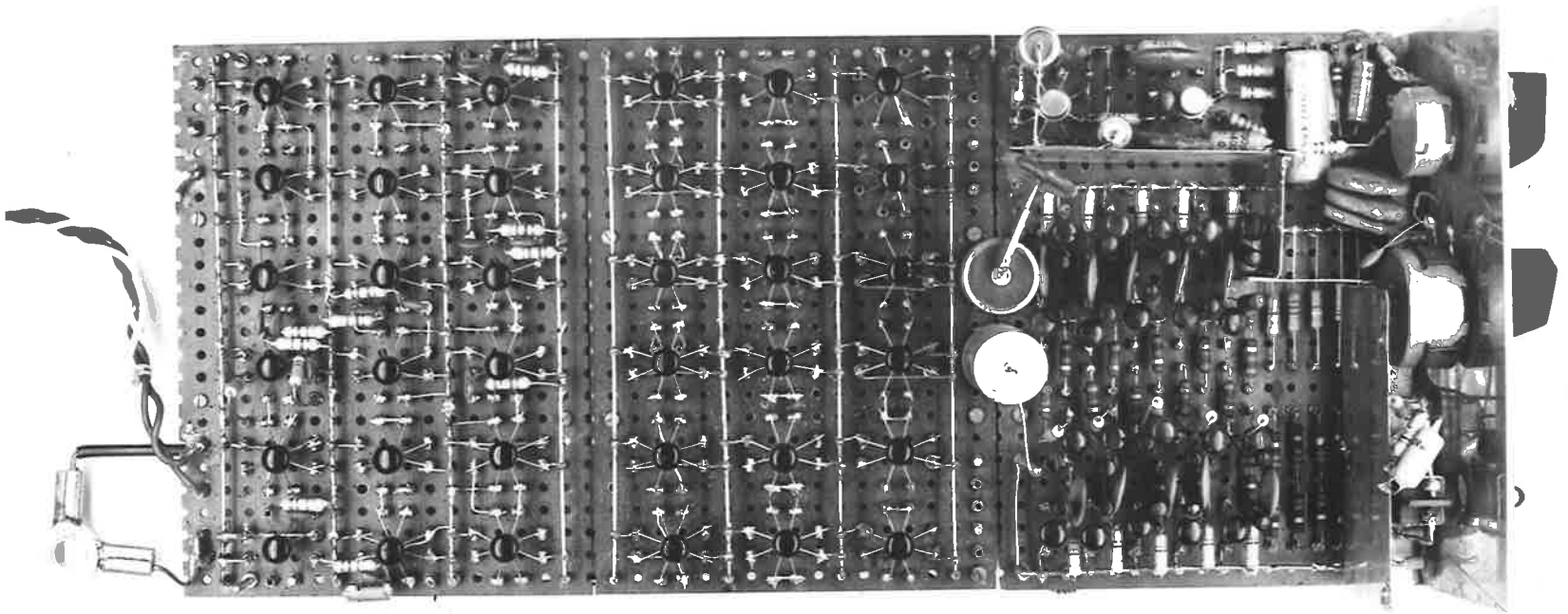


FIG.3.14 NDDM Hardware

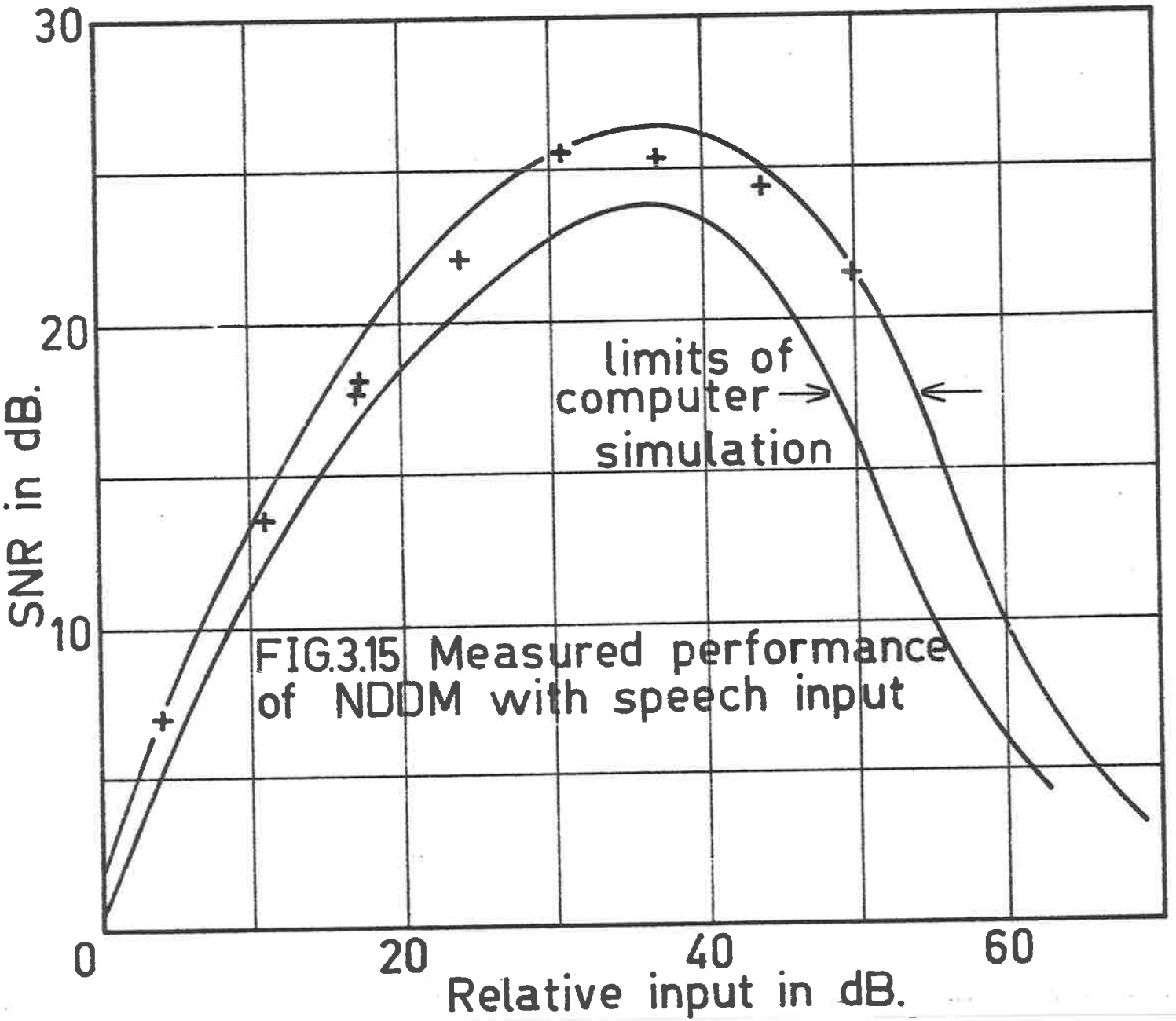


FIG.3.15 Measured performance of NDDM with speech input

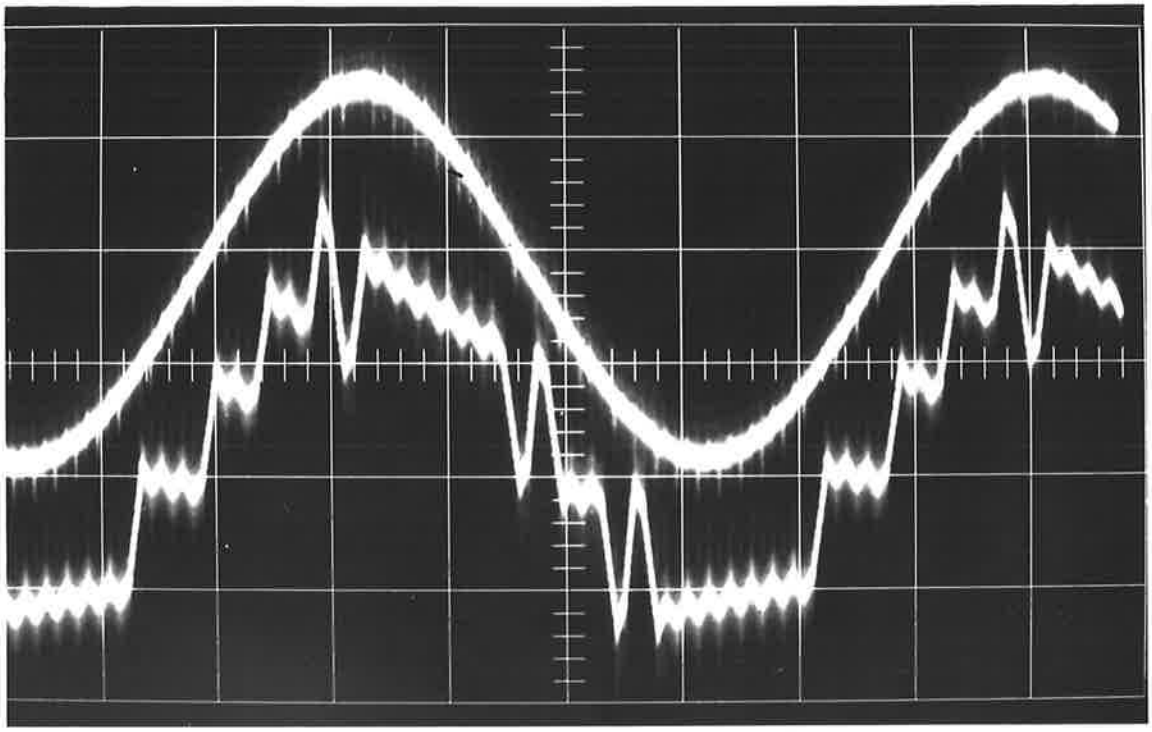
diagrams show that the SNR for speech is quite different from the SNR for an 800Hz sinewave.

Fig 3.16 shows oscilloscope traces of the input and demodulated output waveforms, when an 875Hz sinewave is used as input. In order to obtain stationary oscilloscope traces, the input frequency was synchronised with the 56KHz sampling frequency.

3.5 Extensions

The NDDM system described in section 3.3 was optimized to give as flat a SNR over as wide a dynamic range as possible. With the development of Digital Syllabic Companded Delta Modulation (DSCDM) as described in the next chapter, it is possible to obtain a wide dynamic range. Instantaneous companding can then be used to obtain a high SNR. A possible extension of this thesis is thus the optimization of NDDM to give a high SNR and combining this with syllabic companding to obtain a wide dynamic range as well. Such a delta modulator will have a better performance than any delta modulator developed previously, but it will however also be more complex.

A second extension which can be investigated is the further improvement of the stability. DIDM has a low quantization noise if no overshoot occurs but from the step responses in fig 3.6 it can be seen that a large oscillation results from a step response. When this overshoot occurs, a



20mV/cm

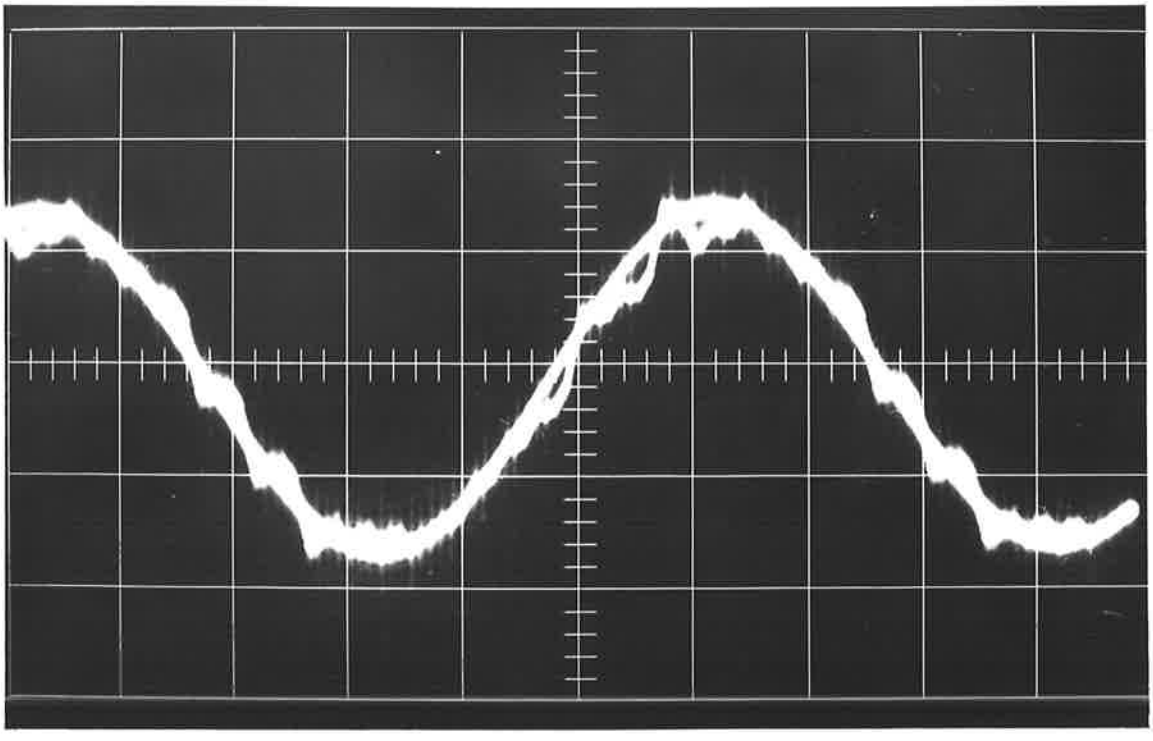
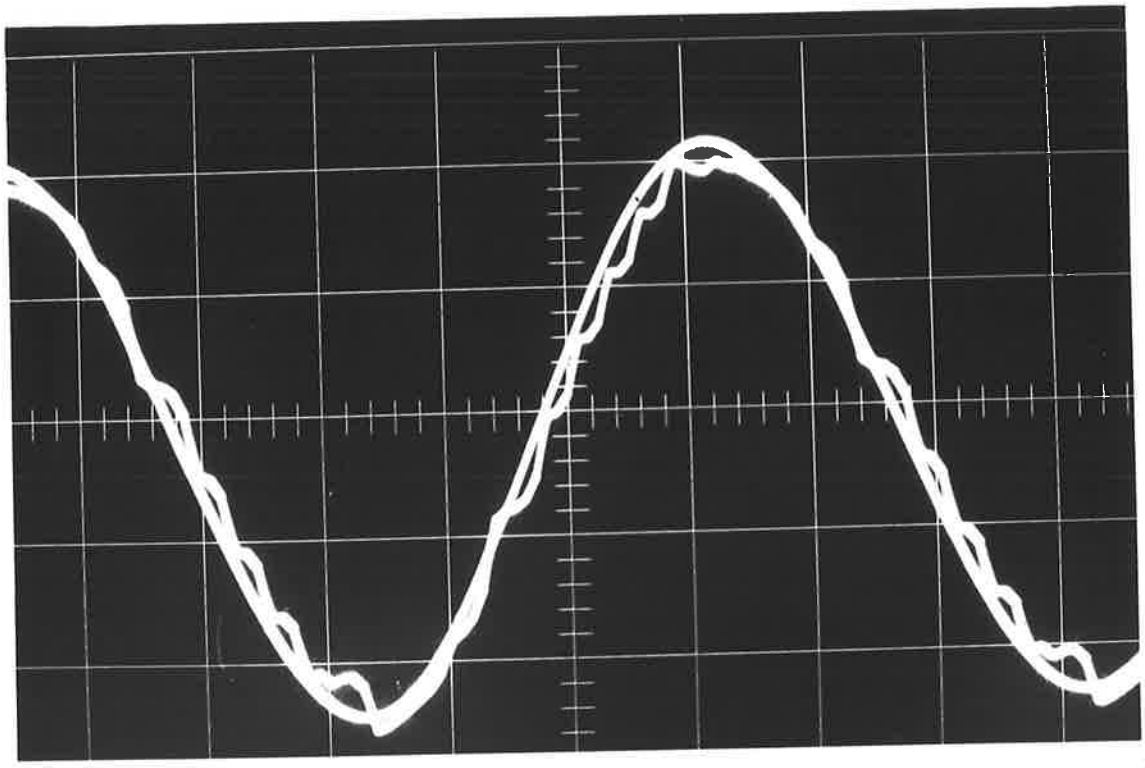


FIG.3.16(a) 100mV/cm



1V/cm

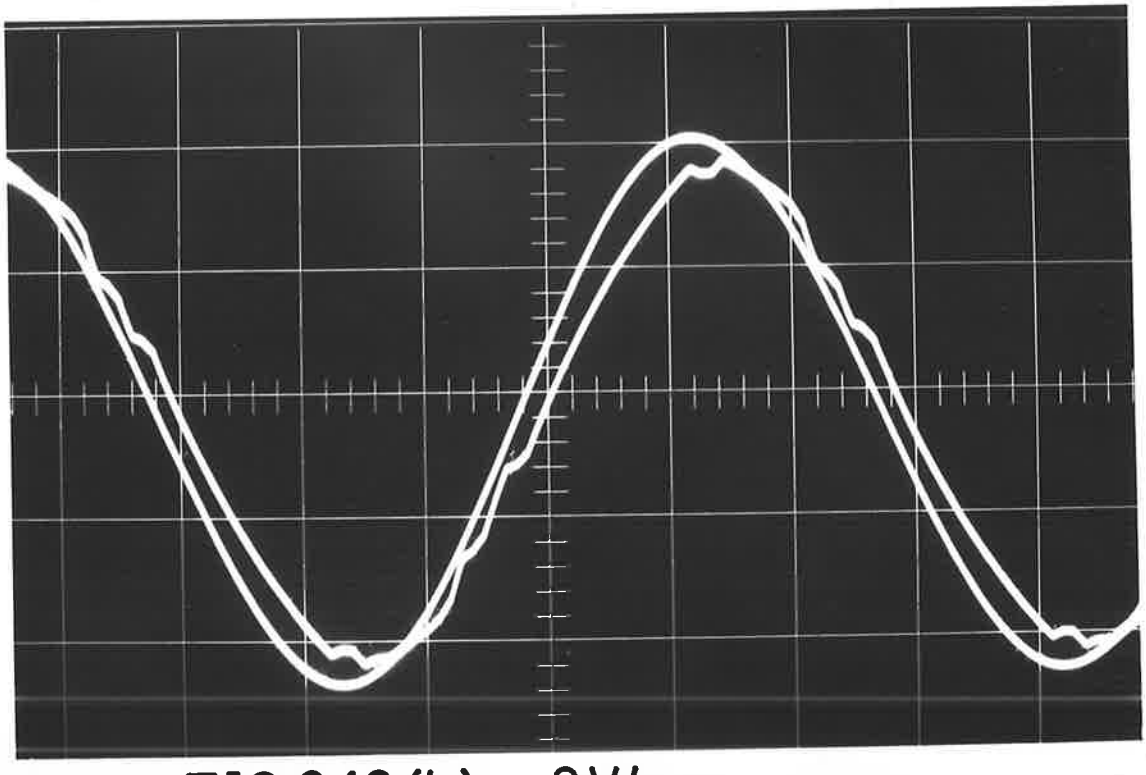


FIG.3.16 (b) 2V/cm

large series of consecutive ones or zero's are produced. These sequences can be detected and the stability can be increased by changing the step size by more than one step as indicated for NDDM. The above proposal gives yet another degree of freedom which can be optimized to obtain the best performance from the delta modulator.

3.6 Conclusions

The investigation in instantaneous companding of delta modulation and the optimization of NDDM has shown that by using a nonlinear conditional companding law, excellent stability and a wide dynamic range can be obtained. The use of digital techniques to obtain this companding law makes the companding characteristic independant of temperature and supply voltage variations, enabling identical demodulated waveforms to be obtained at the transmitter and receiver.

CHAPTER 4

DIGITAL COMPANDED DELTA MODULATION

4.1 Introduction

This chapter deals with the development, design criteria and the performance of digital syllabic companded delta modulation.

As indicated in chapter 1, many systems using syllabic companding have been designed by other workers. None of these have advantages that digital techniques can offer. It will be shown that the delta modulator using the digital syllabic companding developed by the author and described in this chapter has a companding ratio which exceeds that of previously known systems by about 25dB.

4.2 Syllabic Companding

A substantial improvement in performance of any modulation system can be obtained if the modulating signal is of such a power level that the modulator works at the optimum performance. This can be obtained by two different methods:

(1) A reduction of the dynamic range by means of controlling the gain of the modulator and demodulator. This is known as companding with incomplete control.

(2) Splitting the input signal into two components, firstly, a signal with a constant power indicating the waveform of the input signal and secondly, a signal denoting the average

power of the input signal. This is known as companding with complete control.

Each of these two types will later be described in more detail.

If speech is used, the average power varies with each syllable and the companding must be capable of following this variation, hence the name "syllabic companding".

Many of the principles of syllabic companding were investigated during the late thirties [13] when the Atlantic telephone cables were installed.

4.2.1 Companding with Incomplete Control

The block diagram of a modulator using companding with incomplete control is shown in fig 4.1. By means of gain control circuitry, the gain of the compressor is varied such that the dynamic range of the modulating signal is reduced. For incomplete control an increase in the input power will still provide a small increase in the modulating signal power so that there is a one to one relationship between the modulating signal power and the input signal power. Fig 4.2(a) shows a typical relationship between the power levels of the input and the modulating signals. Since there is 1:1 correspondence between the average input and output power levels at the compressor, the inverse relationship at the expander will restore the original power levels. There will however still be variations in modulation depth which means

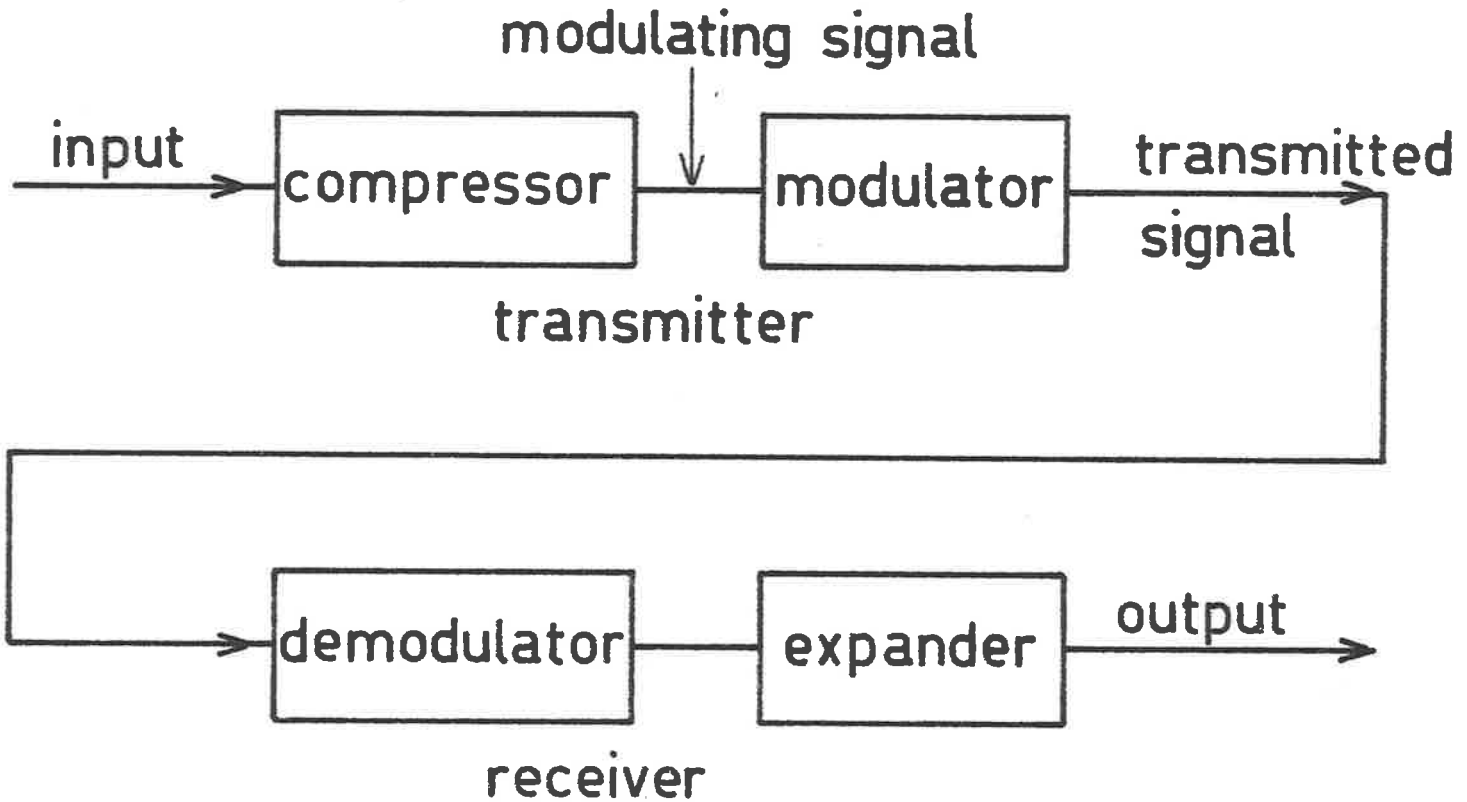
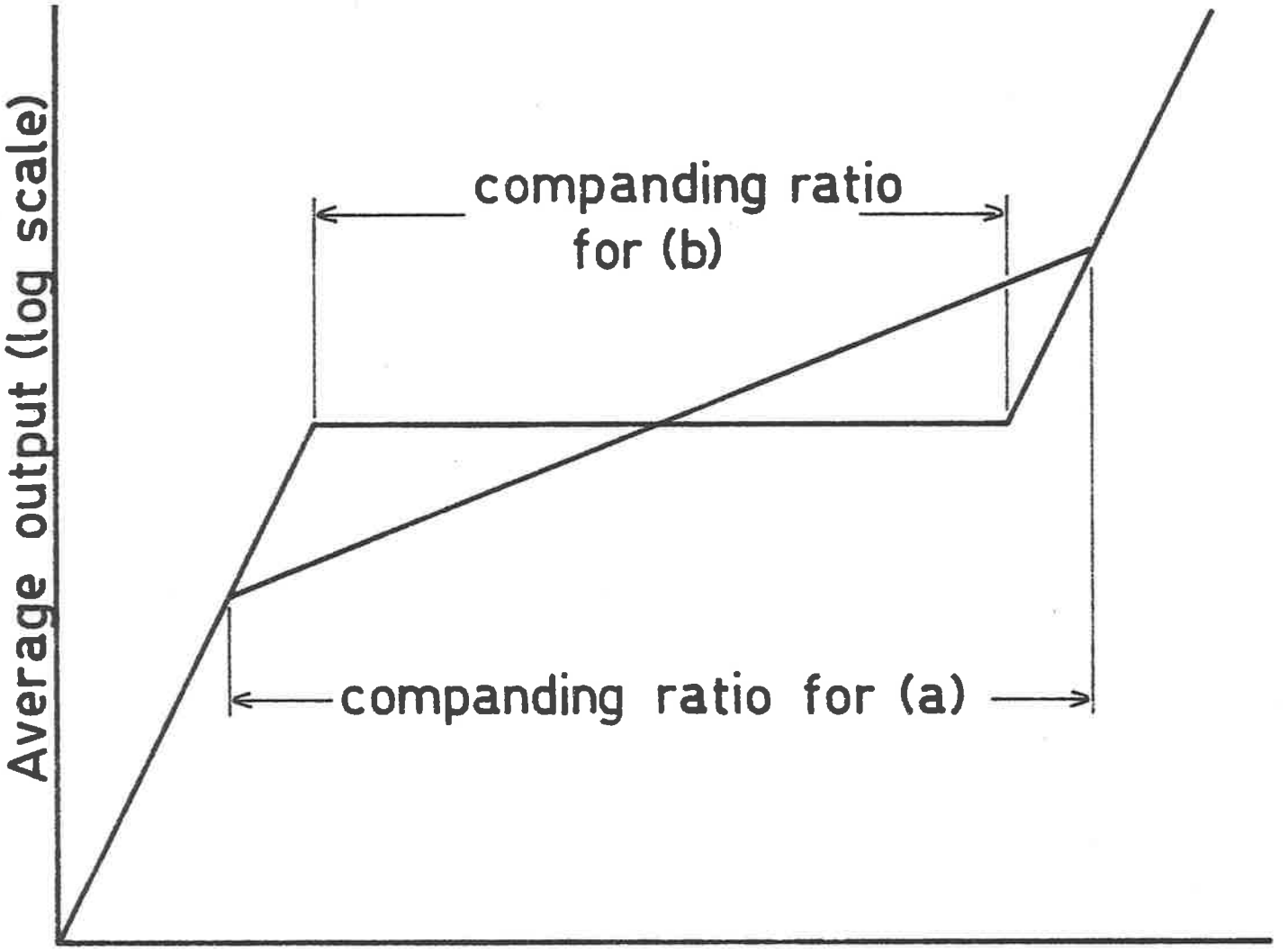


FIG.4.1 Block diagram of a modulator with incomplete companding


companding ratio
for (b)
companding ratio for (a)
Average output (log scale)
Average input (log scale)
FIG.4.2

that the modem will not always operate at its best performance. For example from fig 2.3 and fig 4.3 it can be seen that the peak performance of an uncompanded delta modulator occurs over a very narrow range of input signals. If the delta modulator is to work at its peak performance, the input power must be kept within narrow limits. For this reason companding with complete control is advantageous for delta modulation.

4.2.2 Companding with Complete Control

If the gain of the compressor is varied such that the modulating signal power is kept constant, companding with complete control is obtained. Since however there is no longer a one to one correspondence between the input power and modulation depth it is not possible to use the inverse characteristics to obtain the required output power at the expander. The information about the input power level must thus be transmitted separately as shown in fig 4.4. The companding characteristics of a compander with complete control is shown in fig. 4.2(b).

Since the rate of change of gain is normally small the bandwidth of the channel transmitting the gain does not have to be wide. In some cases the two channels are combined into one by means of frequency division multiplexing. In speech applications the bandwidth below 150Hz can easily be used to transmit the gain information.

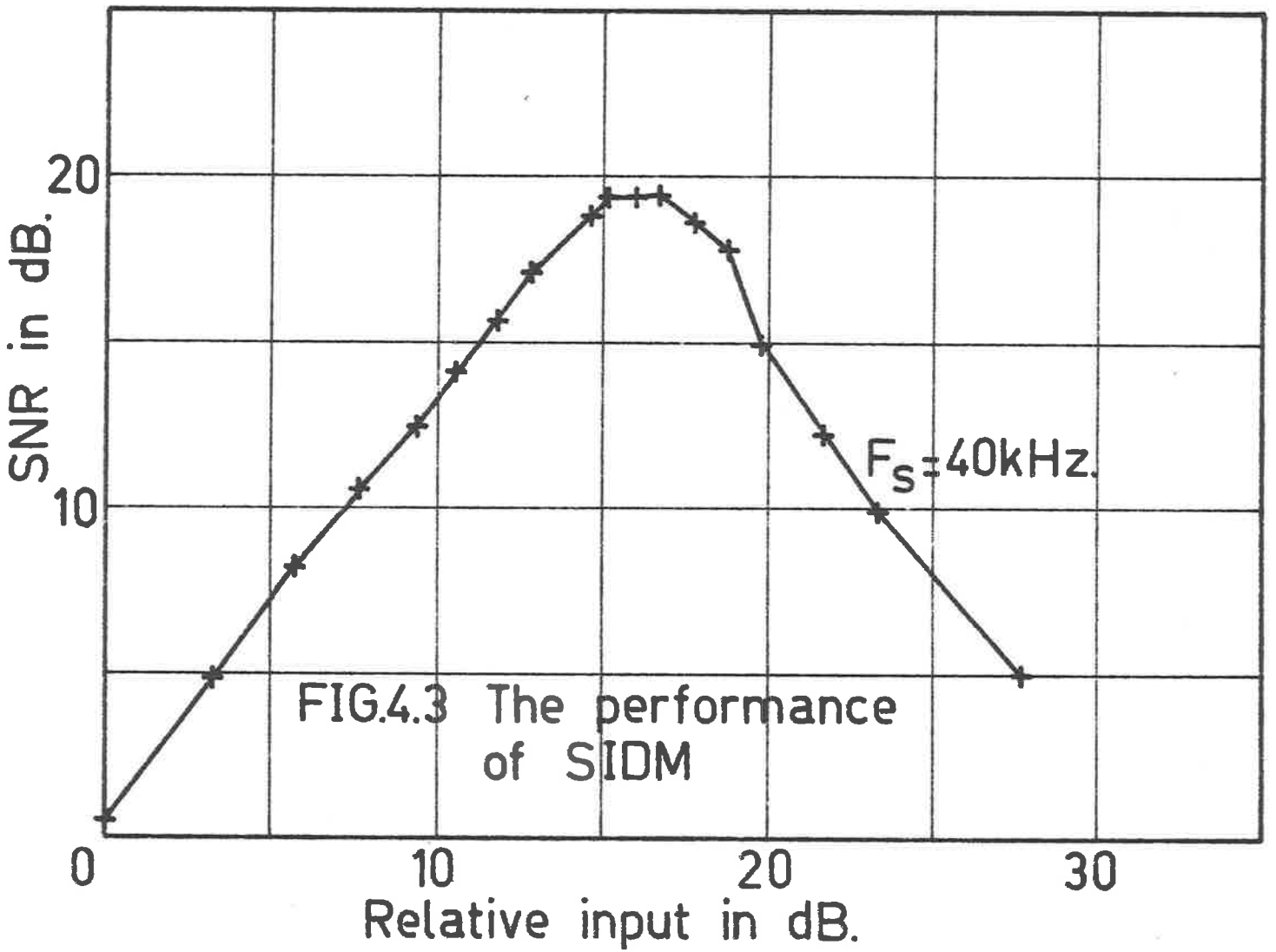


FIG.4.3 The performance of SIDM

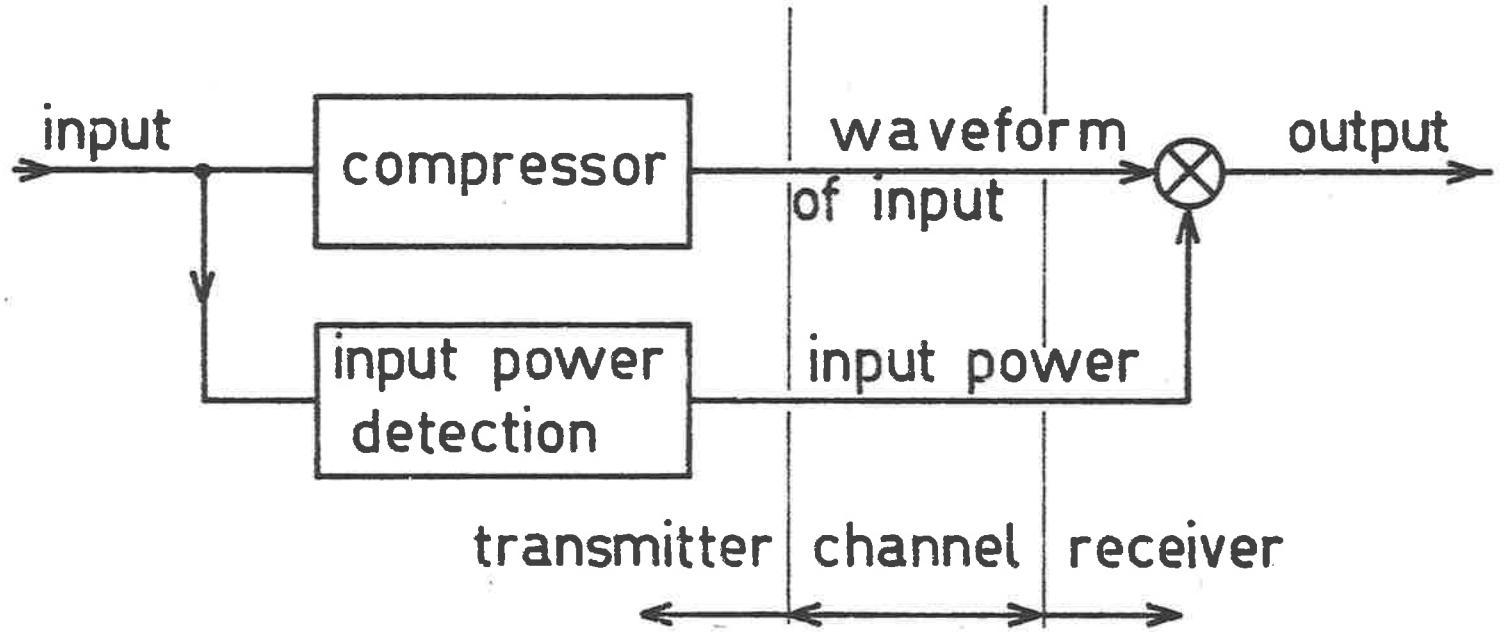


FIG.4.4 Method by wich complete companding can be obtained

The system proposed by Greefkes and de Jager [15] applies this principle to delta modulation. Some of the other systems mentioned in chapter 1 [10,11,12,16] use incomplete control, so that both complete and incomplete control of companding have been used in delta modulation in an attempt to restrict the modulation depth to the narrow range required to give the optimum SNR.

Fig 4.5 shows the difference in the performance of a delta modulator when complete or incomplete control of the companding is used. For incomplete control a region of the SNR curve of the uncompanded system is expanded, while for complete control a single point of the SNR curve is expanded horizontally. From fig 4.5 it can be seen that complete companding will give a better performance for delta modulation.

4.3 Companding with Complete Control, applied to Delta Modulation

The following section describes the theoretical principles involved in the design of digital syllabic companded delta modulation (DSCDM). These principles are also described in the Australian Patent No.C349663/71 and the U.S. Patent No. 193,410 [20] taken out by the author and the University of Adelaide. A copy of this patent is included in the thesis as Appendix 5.1

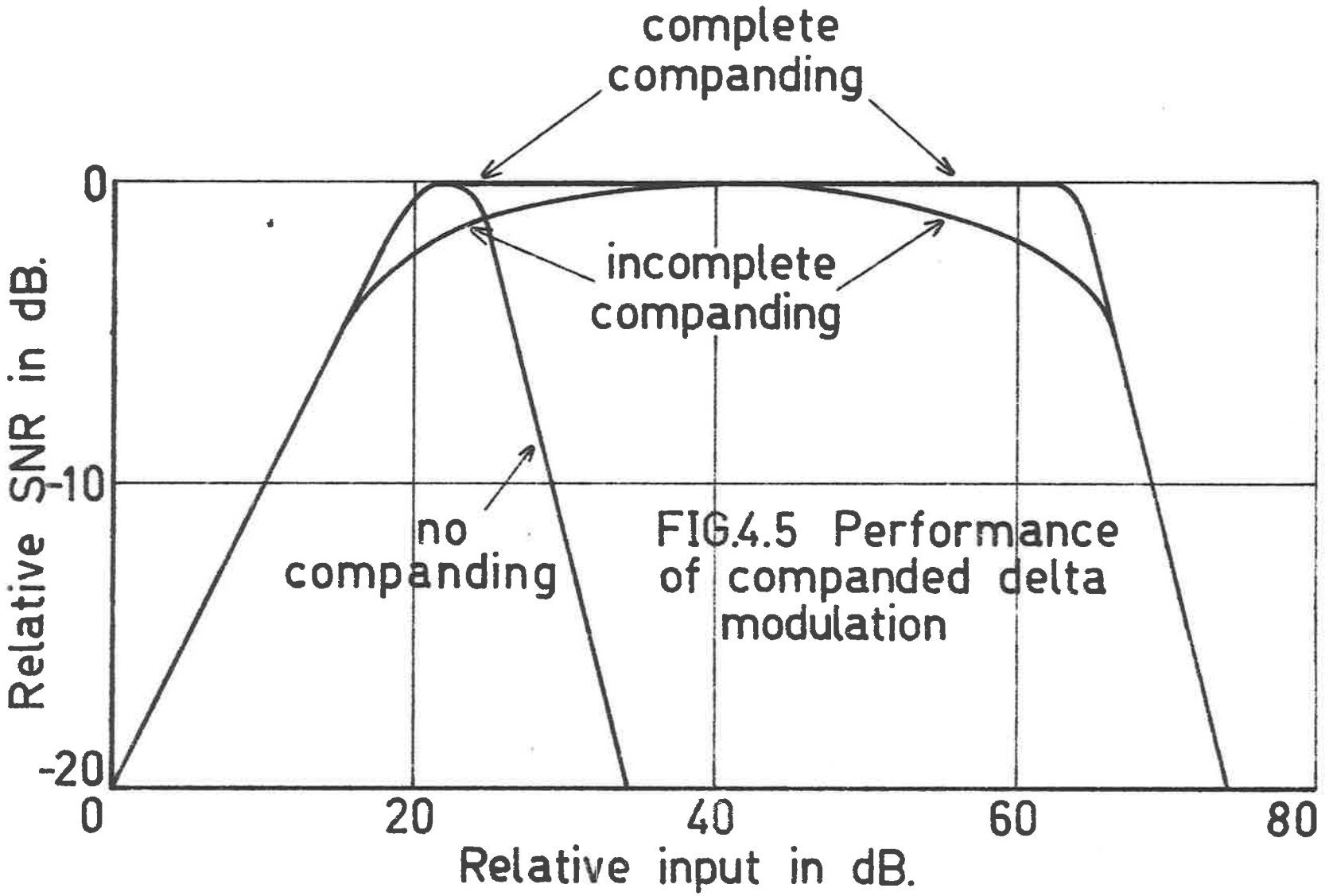


FIG.4.5 Performance of companded delta modulation

4.3.1 Detection of Normalised Input Power

Fig 4.3 indicates the performance of SIDM for a variation of input power. From fig 1.2 it can be seen that if the step size is increased, the amount of input power required to obtain the optimum SNR will increase as well.

Similarly for a given input power, the optimum performance can be obtained from the delta modulator, by selecting a suitable step size. The ratio of input power to step size is thus an important parameter and is called the normalised input power.

The normalised input power is similar to the term modulation depth, used in amplitude modulation. For delta modulation the term modulation depth does not have a strict meaning, so that the term normalised input power will be used in this thesis.

A measure of the normalised input power can be derived from the binary (transmitted) signal and since the binary signal is present at both the modulator and demodulator, the same measure of the normalised input power can be obtained at both the modulator and demodulator, provided no transmission errors have occurred.

In order to obtain a measure of the normalised input power from the binary transmitted signal, one must select one or more binary patterns, or control words, the relative occurrence of which vary with the input power. In order to prevent ambiguities in the measure of the normalised input

power, the functions of the relative occurrence of the control words versus normalised input power must be monotonic increasing or decreasing functions as shown in fig 4.6.

At each sampling interval, a test is made to determine whether a control word is present or not, from this information the normalised input power can be determined and the step size corrected to give the required normalised input power.

Consider the case where the relative occurrence of control word decreases with normalised input power as shown in fig 4.6(a), and that the relative occurrence at the normalised input power corresponding to the peak SNR is X.

If the relative occurrence of the control word is less than X, the normalised input power is too high and the step size must thus be increased in order to obtain the correct normalised input power. Similarly if the relative occurrence is more than X we want to decrease the step size to obtain the correct normalised input power. The manner in which the step size is changed will determine the type of companding. Three types of companding, namely linear, logarithmic and semilogarithmic companding will be dealt with in this thesis but the principles can apply to other companding laws as well.

4.3.2 Linear Companding

For linear companding the change of step size is independant of the step size, although the increase and

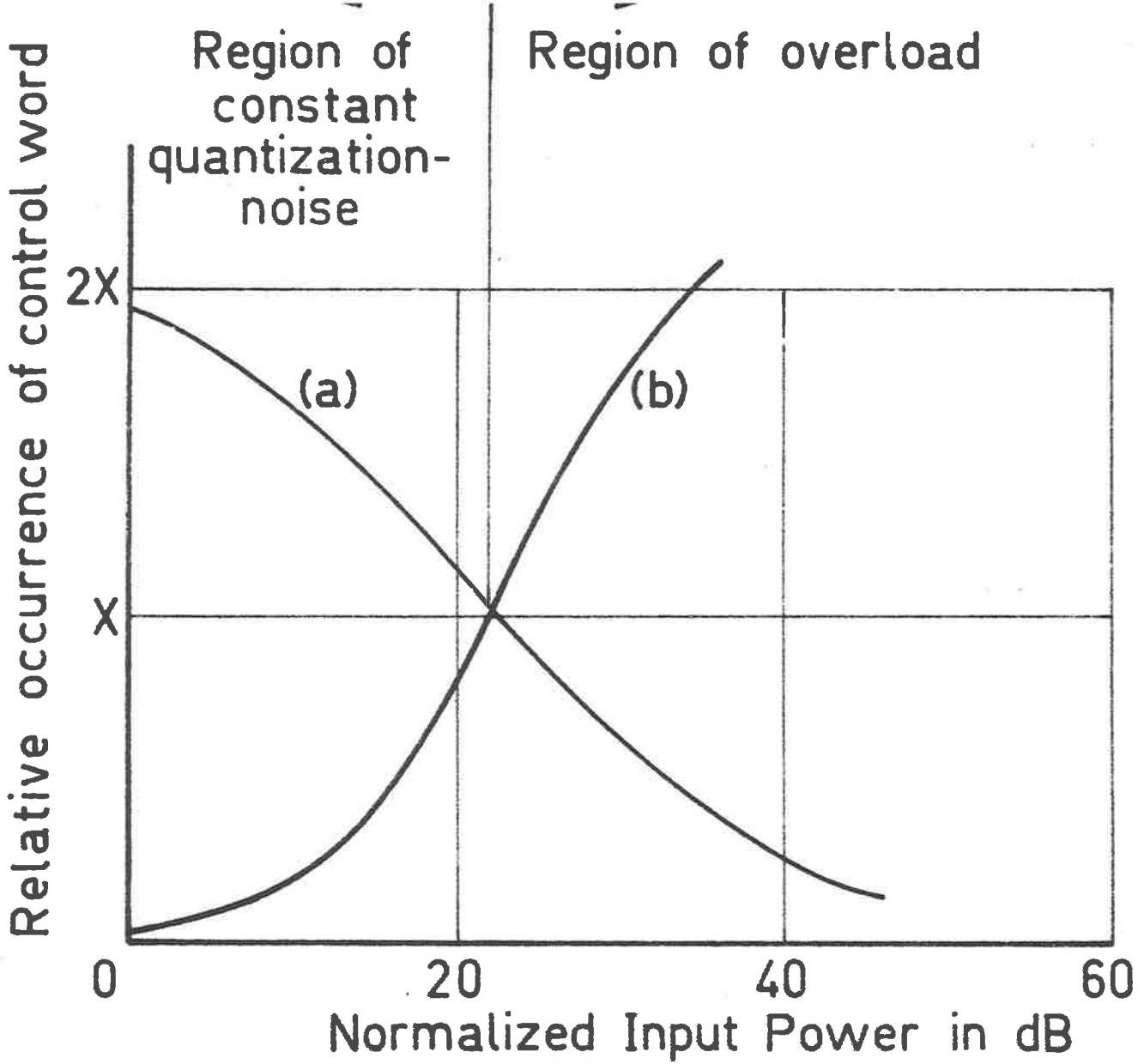

Region of constant quantization-noise
Region of overload
Relative occurrence of control word
2X
X
(a)
(b)
0
20
40
60
Normalized Input Power in dB

Fig.4.6

decrease need not be equal. Consider again a control word whose relative occurrence decreases with normalised input power as indicated above. If the occurrence of a control is word is used to decrease the step size by K(1-X) units and the step size is increased by KX units if no control word occurs, the average step size will remain constant when the system is operating at the normalised input power corresponding to the optimum performance. K is a positive constant.

Consider the delta modulator to be operating under conditions such that the relative occurrence of the control word is Y. The average increase of step size can be seen to be equal to the increase in step size due to the control word not occurring multiplied by the relative occurrence of the control word not occurring, minus the decrease in gain due to the control word occurring multiplied by the relative occurrence of the control word, i.e. the average increase in step size per sampling interval = KX (1-Y) - K (1-X) Y = K (X-Y).

When the relative occurrence of the control word, Y, is equal to X, then X - Y = 0, so that the average step size remains constant.

When the relative occurrence of the control word, Y, is less than or greater than X, then the average step size is increased or decreased as required.

The step size will thus automatically adjust itself to yield the normalised input power corresponding to the optimum

performance.

Because the step size is increased by KX units or decreased by K(1-X) units during each sampling interval. The ratio of the attack to decay time constants will be

$$R = \frac{K.X}{K(1-X)} = \frac{X}{1-X}$$

This ratio can thus be chosen by finding suitable control words.

A similar argument applies if the relative occurrence of the control word increases with normalised input power, except that the occurrence of a control word is used to increase the step size by K(1-X) units and the step size is decreased by KX units if no control word occurs.

The ratio of the attack to decay time constants will now be

$$R = \frac{1-X}{X}$$

The attack time constant, which for linear companding is step size dependant, can be altered without altering the ratio of the attack to decay time constants, by changing the value of K, or by altering the sampling frequency.

4.3.3 Logarithmic Companding

Since the ear has a logarithmic amplitude characteristic,

it is an advantage to use logarithmic companding. The step size is thus changed by a fixed percentage. The average step size should still remain constant, when the relative occurrence of the control word is X. The change of step size must now be selected according to

$$(B+1)^{1-X} \cdot (A+1)^{X} = 1$$

A is the percentage change of step size if a control word occurs, B is the percentage change of step size if no control word occurs. Either A or B will be negative, indicating a decrease in gain, depending on whether the relative occurrence of the control word decreases or increases with normalised input power.

The ratio of attack to decay times is again B to A or A to B, for a relative occurrence of the control word which is decreasing or increasing with normalised input power respectively.

Since the companding produces an exponential rate of change of step size, one can no longer talk about a time constant associated with the companding, as is usual, but one must refer to a rate of change of step size of "so many dB per second".

The rate of change of gain is directly related to the values of A,B and the sampling frequency.

It appears that Shindler [18] has independently developed a system which will fit the requirements for logarithmic

control. From his extremely short description, it was not possible to determine whether he has developed the theory of operation as explained in this section.

Comparing the performance of his system for sinewave input signals with the results shown in fig 4.5, fig 4.11 and fig 4.12 it appears that complete companding has not been obtained, since the SNR characteristic is not flat as would be expected for complete companding. Finally no mention is made of using speech to optimise the companding, which is essential if the optimum performance is to be obtained as is shown in section 4.5.2 and fig 4.13.

4.3.4 Semilogarithmic Companding

Since the complete control is obtained by increasing or decreasing the step size by a certain amount, the step size must be stored. This can either be done in a capacitor or a digital counter. Using the analogue technique restricts the dynamic range that can be obtained due to the accuracy of the store. Furthermore, leakyness of the analogue store will give rise to incomplete companding and different amounts of leakyness at the transmitter and receiver will create a mismatch between signals at the transmitter and the receiver.

A digital forward and reversible counter has thus obvious advantages as a storage element in this application.

Linear control can easily be obtained by making KX and K(1-X) both integers. Logarithmic control however is more

difficult to obtain. The counter should be increased by A.N or B.N, where A and B are the percentage increments as before, and N is the contents of the counter. A.N and B.N need not be integers but the counter can only count in integers, so that approximations must be made.

It is possible to approximate A.N and B.N to the nearest integer, but this will lead to more complex circuitry than is necessary. Relatively simple circuitry will be obtained if the contents of the counter are incremented by A.M or B.M where M is N truncated to a binary weighted integer.

For example when N is between 8192 and 16383 (i.e. between 2^{13} and $(2^{14}-1)$, M is 8192 (i.e. 2^{13}).

This means that linear counting is used over a nearly 2:1 range in the contents of the counter. For large changes in the contents of the counter, the counting is logarithmic, since M is related to N.

Since one now has semilogarithmic counting, involving conditional nonlinearities, it is difficult to prescribe the required increase or decrease in step size at each sampling interval and computer simulation should be used to optimize the increase and decrease in step size. The above describes semilogarithmic companding applied to a binary base. It is however also possible to use other such as decimal bases.

For a decimal base, N is truncated to an integer power of 10. For example if N is between 100 and 999 M is 100.

4.4 Discussion of Parameters

4.4.1 Selecting the Companding Ratio

The companding ratio is defined as the ratio of the largest to the smallest step size. This ratio governs the dynamic range of the delta modulator. Referring to fig 4.5 it can be seen that the dynamic range, which is the range of input power over which the delta modulator has an acceptable performance, is slightly larger than the companding ratio.

The selection of the dynamic range is governed by three factors:

1) The dynamic range of the input signal
2) The complexity of the hardware and hence the cost
3) The tolerance to transmission errors.

The effect of transmission errors will be discussed in section 4.3.6, where it will be shown that the bigger the companding ratio, the worse the tolerance to transmission errors.

For telephone applications, a dynamic range of 40dB should be adequate, particularly if the delta modulator is to be installed in the telephone handset so that variations of attenuation of telephone lines do not have to be allowed for.

A companding ratio of between 30dB and 40dB will thus be a reasonable compromise for a practical delta modulator employing digital syllabic companding.

It should be noted that the theory sets no limit on the

companding ratio, but that the upper limit of the companding ratio is purely dictated by the dynamic range of the analogue circuitry in the summing amplifier and the comparator of the delta modulator.

At present the dynamic range of analogue circuitry is close to 80dB, so that a companding ratio of 60dB is about the maximum that can be employed.

In order to illustrate the versatility of the companding technique, a digital syllabic companded delta modulation (DSCDM) system with a 60dB companding ratio was optimized, using computer simulation, and built. A detailed description of the optimization is given in section 4.5.2 and the hardware is discussed in section 4.5.3.

4.4.2 The Effect of Transmission Errors

Transmission errors can cause two effects:

1) an error in the waveform of the demodulated signal will result
2) a control word may be destroyed or created, causing an error of step size as shown in fig 4.7.

In order for the system to be useful, the effect of both these errors must diminish with time.

The error in the waveform of the demodulated signal is similar to the effect of a transmission error on SIDM, which was discussed in section 3.2.5 and illustrated in fig 3.7 (b). Provided the integrators in the local and receiver

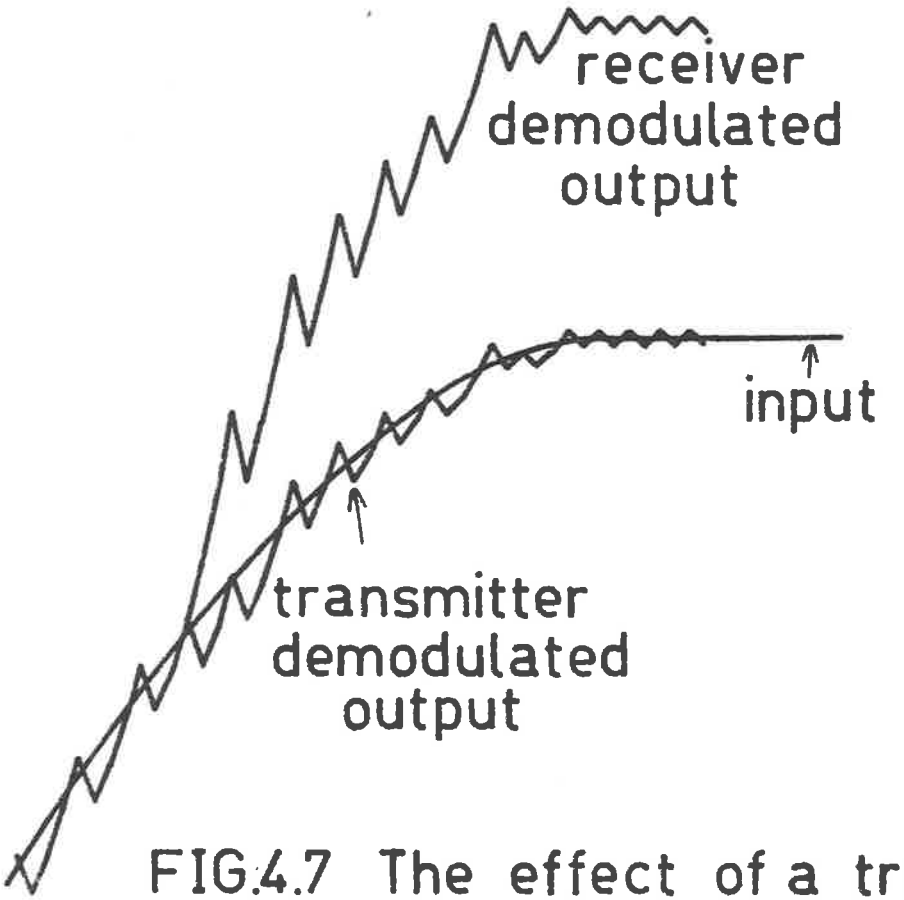


FIG.4.7 The effect of a transmission error on DSCDM

demodulators have some leakyness, the effect of the transmission error will diminish with time.

An error in the step size can, under certain conditions create a much more audible effect. The tolerance to transmission errors will depend on the control words used a and the likelyhood that a transmission error causes an error in the step size.

Since a counter is used to store the step size, the error in the step size will persist until the counters in both the modulator and demodulator reach the upper or lower limit, when the step sizes at the modulator and demodulator will become the same. The step sizes will then remain the same until another transmission error occurs.

If the smallest step size of a digitally syllabic companded delta modulation (DSCDM) system is selected such that the input noise, which includes accoustical background noise, from the room in which the microphone is placed, is small enough to cause a 101010 idling pattern to exist when no words are being spoken, the step sizes at the transmitter and receiver will become the same during the pauses between words. Under these conditions a transmission error will only affect the step size during one word.

An error in the step size will make the demodulated signal louder or softer than the original signal. Provided the difference in the loudness is not too great, the effect will be hardly noticable. When sufficient errors occur

during each word to cause the difference in the step sizes to be of the order of 20dB, the errors become objectionable. The transmission errors will then cause a rapid variation of power which substantially reduces the intelligibility of the demodulated signal.

The companding ratio will thus effect the error performance in two ways, firstly, a smaller companding ratio is normally coupled with the selection of a larger minumum step size, raising the threshold of operation and creating a higher probability of obtaining a 101010 idling pattern in the presence of background noise, thus ensuring the synchronisation of the step sizes in the pauses between the words. Secondly, a smaller companding ratio will decrease the possible difference in the step sizes when many transmission errors occur, thereby making the effect of the transmission errors less significant.

Another interesting feature is that transmission errors tend to increase the step size. As shown in fig 4.10 for delta modulation at a sampling frequency of 40KHz, with speech input and operating at the optimum SNR, the probability of a transition occurring in the binary transmitted signal is about 66%. A transmission error is thus more likely to create a string of ones or zero's than a 1010 pattern. Transmission errors will thus on the average create an impression of slope overload, for which the receiver tries to compensate by increasing the step size. If sufficient transmission errors

occur, the step size at the receiver will increase until the maximum step size is obtained.

If the step size at the transmitter is 20dB above the minumum step size and the modem has a companding ratio of 60dB, a 40dB difference in step size can result, giving rise to a very large increase in level.

The companding ratio should thus be chosen such that:

1) the threshold is normally larger than the background noise and

2) the resulting dynamic range is compatible with the dynamic range of the ear, allowing for accoustical backgroung noise in the listening environment.

4.4.3 Stability Considerations

As described previously, the step size is changed if a control word occurs. This however lead to problems. For example, consider a system where linear companding takes place and the step is increased by 2Δ if a control word occurs and is decreased by Δ if no control word occurs.

Section 4.5.1 shows that the control words 11 and 00 are suitable but fig 4.8 shows that for these control words oscillations can take place which will increase the step size until the largest step size is obtained. This undesirable feature must be overcome if the system is to give a good performance. There are two methods which can be used to overcome this problem:

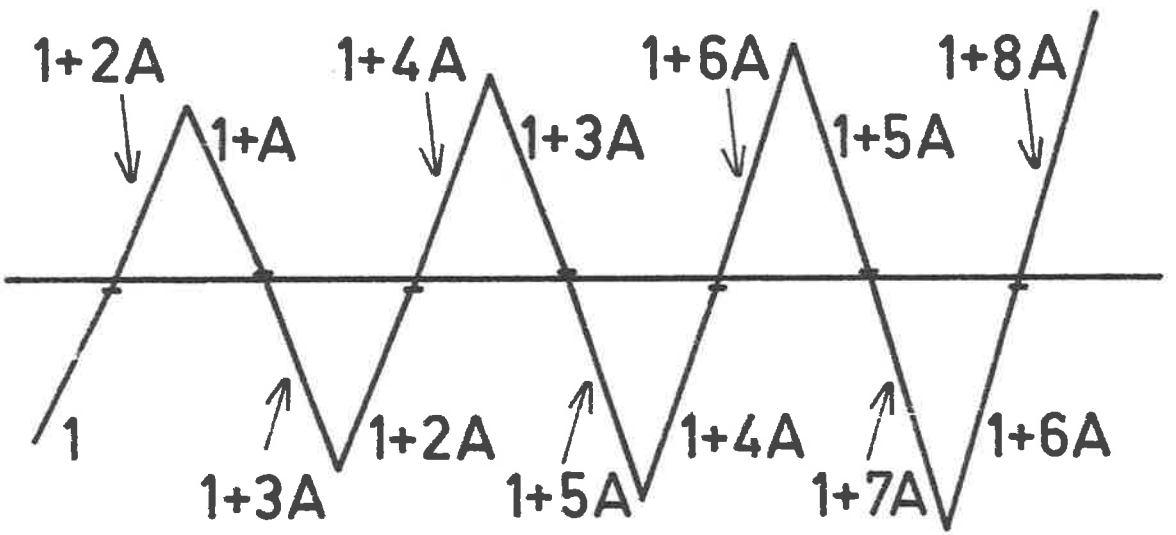


FIG.4.8 Instability due to syllabic companding

1) delay the increase of the step size by one sampling period, so that the step size is increased at the sampling period after the control word has occurred. Fig 4.9 (a) shows the resulting demodulated waveforms

2) make the analogue integrator sufficiently leaky to prevent the oscillations occurring. As shown in fig 4.9 (b), stable operation will result if the integrator decays by more than A% of the value stored during one clockpulse.

The second approach was chosen for the DSCDM hardware, since it is easy to implement and as explained in chapter 3, leakyness in the analogue integrator improves the tolerance to transmission errors.

4.5 The Design of a Digital Syllabic Companded Delta Modulation System

4.5.1 Selection of Parameters

The principle described in the previous section are now applied to the design of DSCDM. Five parameters must be chosen, each one of these can be chosen independently. Their choice will affect the resultant performance of the delta modulator. The five parameters are:

1) The type of companding, i.e. linear, logarithmic or semilogarithmic companding. Linear companding results in the simplest hardware while logarithmic companding is more suited

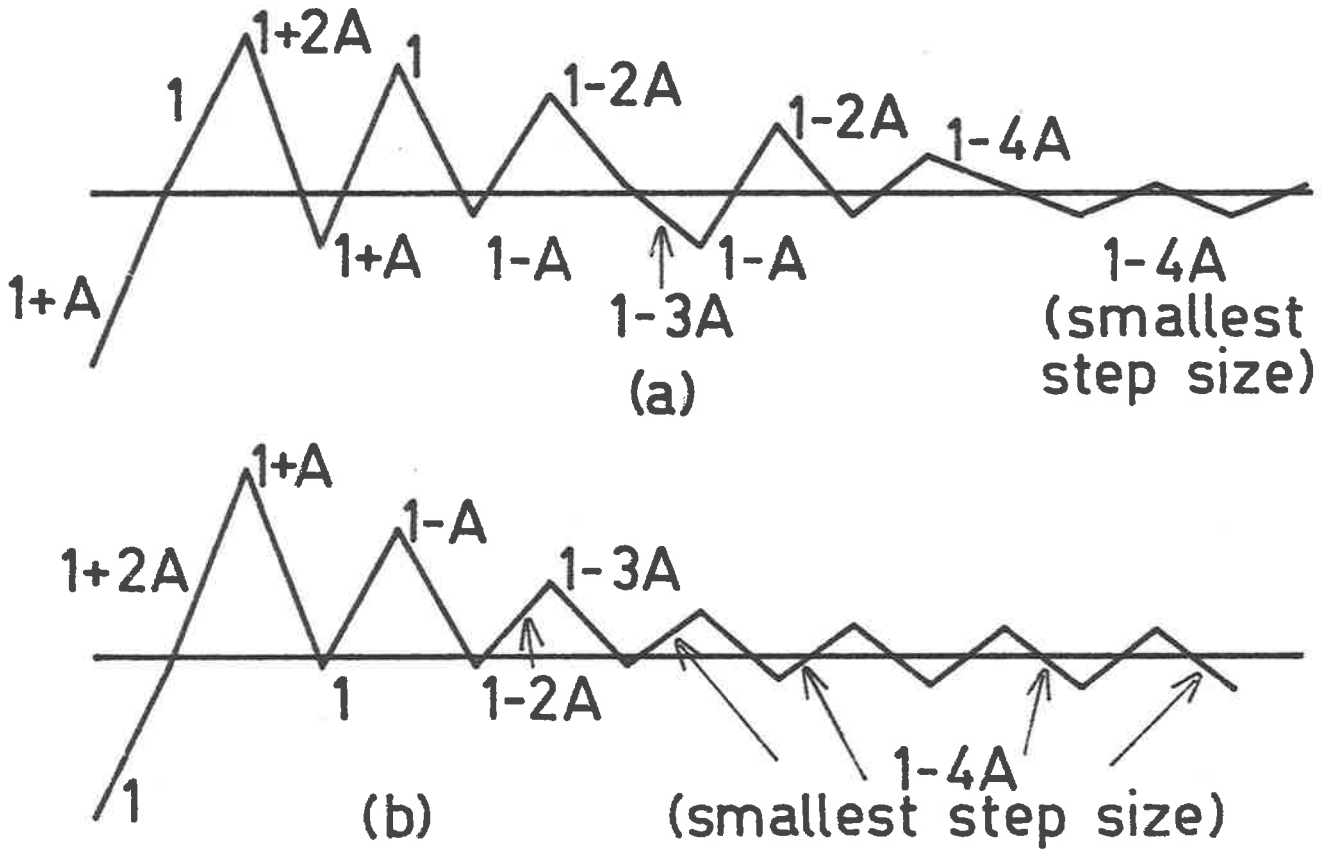


FIG.4.9 Methods of obtaining stability with syllabic companding

to the characteristics of the ear. Semilogarithmic companding however is a good compromise between complexity and performance so that semilogarithmic companding was chosen for the hardware realisation.

2) The sampling frequency.

The sampling frequency was chosen to be 40KHz, since this gives an adequate performance for speech transmission over telephone lines.

3) The companding ratio.

The companding ratio can be chosen at will, which has not been possible with sytems proposed by other workers (6-18). For speech transmission, a companding ratio of 40dB will be satisfactory. However in order to demonstrate the versatility of the digital syllabic companding, a companding ratio of 60dB was chosen. This is about 25dB more than has been achieved previously.

4) The ratio of attack to decay times.

This parameter affects the choice of the control word. Since for SIDM there are only a limited number of control words, the choice of ratio of attack to decay times is limited.

Fig 4.10 shows the relative occurrence of several control words that can be used.

It can be seen that the control words 11 and 00 have a relative occurrence of about 33% at the optimum SNR. This will make the attack time faster than the decay time, a property

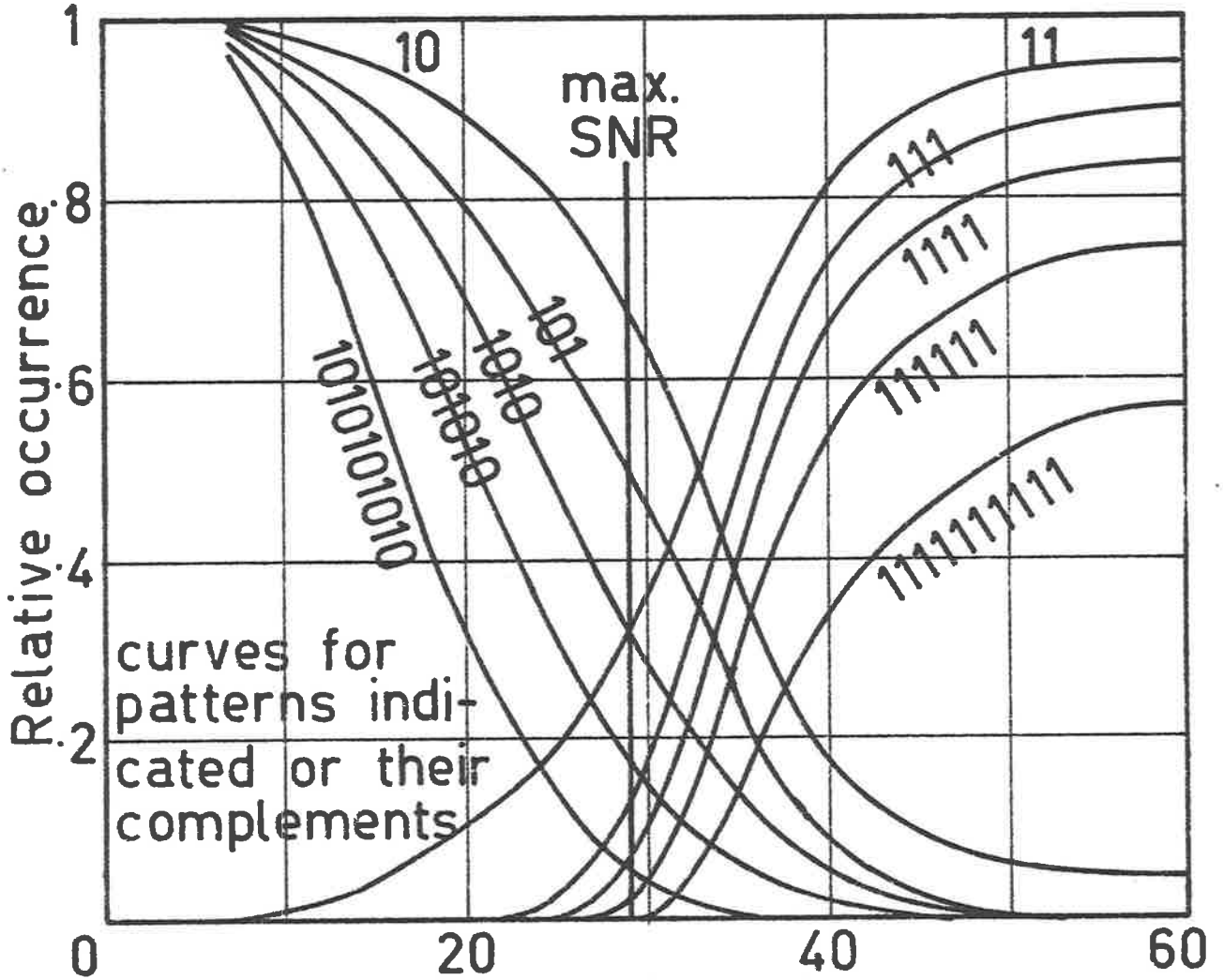


FIG.4.10 Possible control words

which is generally found desirable.

5) The Attack Time

The attack time must be chosen such that the companding can follow the syllabic power variations of speech.

If the attack time is too slow, the normalised input power will still vary and the optimum performance will not be obtained. If the attack time is too fast, the variations in step size at each successive sampling interval will be too large, giving rise to a coarse quantization of step size and hence a degradation of performance.

From (4) and (5) it is possible but difficult to directly nominate the percentage increase in step size when a control word has occurred and the percentage decrease in step size when no control occurs. In practice, the optimization of these parameters using computer simulation is desirable.

4.5.2 Computer Simulation

The computer simulation was carried out in order to:

1) Find and select suitable control words for the companded delta modulation system. Fig 4.10 shows the results of this investigation, and as a consequence the control words 00 and 11 were selected.

2) Optimize the increase in step size when a control word occurs and the decrease in step size when no control word occurs.

3) Determine the performance of the proposed delta modulator due to different input signals, such as simulated speech and sinewaves, before the system was built and to compare the performance with that of the uncompanded delta modulation system.

Since the delta modulator was designed for speech applications, the computer simulation used simulated speech as described in section 5.2.2, to optimize the increase and the decrease of the step size.

The optimization was a trial and error process, whereby the performance of the delta modulator was evaluated for different increases and decreases of step size on the occurrence of a control word.

Fig 4.11 shows the performance of the resulting digital syllabic companded delta modulation (DSCDM) system and compares this with the performance of an uncompanded delta modulator. It can be seen that the dynamic range has been increased by about 60dB.

The best performance was found to occur when the step size is increased by 2×2^n units if a control word occurs and is decreased by 2^n units if no control word occurs, when the contents of the counter, containing the step sizes, is between $2^{(n+5)}$ and $2^{(n+6)} - 1$ units. For this change in step size, there is little difference in the performance of DSCDM when it is subject to simulated speech with or without syllabic variations of power, indicating that the companding

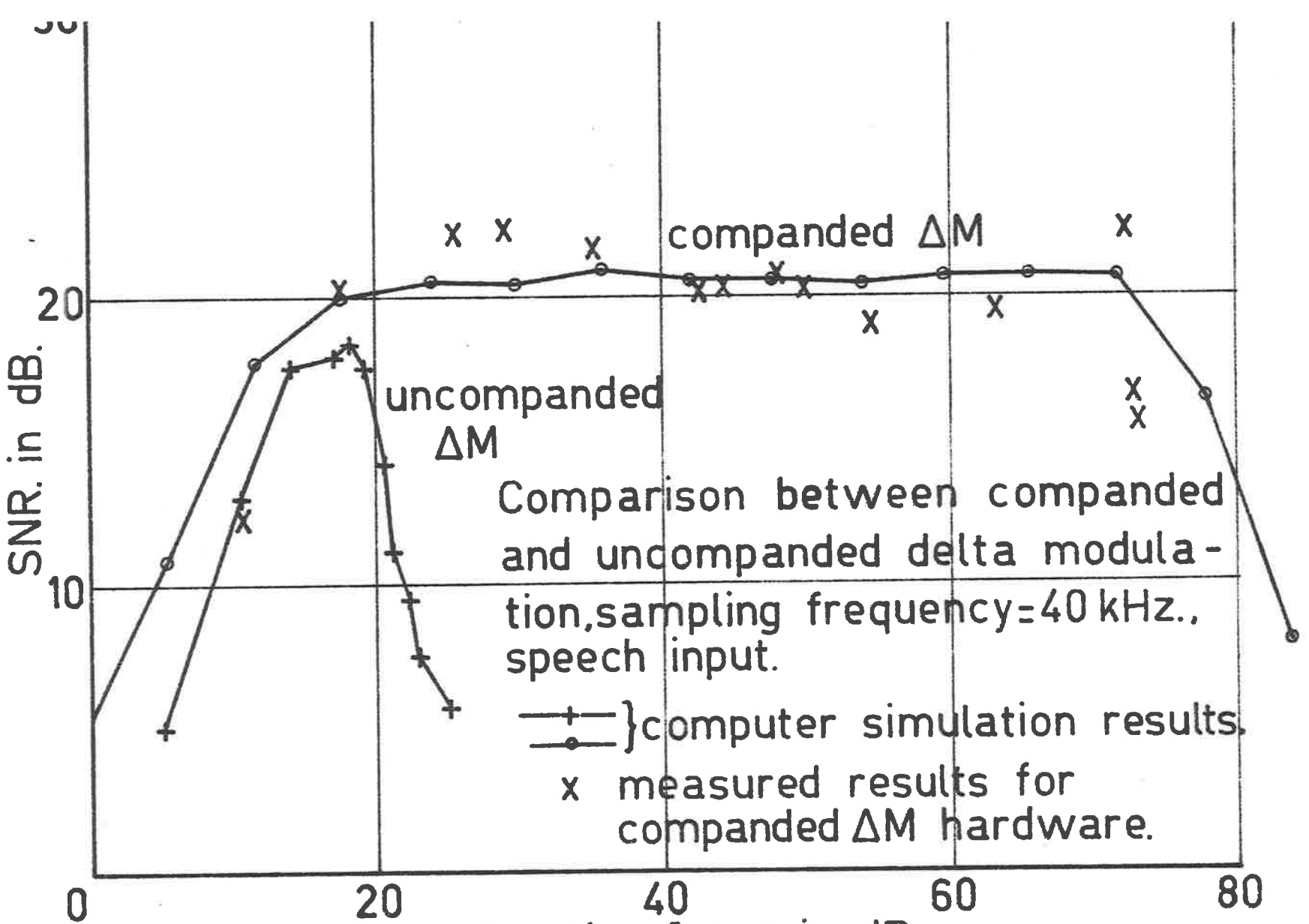

companded ΔM
uncompanded ΔM
Comparison between companded and uncompanded delta modulation, sampling frequency=40 kHz., speech input.
computer simulation results.
x measured results for companded ΔM hardware.
SNR. in dB.
20
10
0
20
40
60
80
Relative Input in dB.

FIG.4.11

is fast enough to track the syllabic variations of power. This change of step size gives an average attack time of 16dB/mSec (0.4dB/sampling interval) and an average decay time of 8dB/mSec (0.2dB/sampling interval).

Because the companding can follow the syllabic variations, the maximum SNR will be higher for DSCDM than for the uncompanded delta modulator.

Fig 4.12 shows the performance of DSCDM when subject to a sinewave input. The peak performance occurs for input signals where the companding no longer operates.

Fig 4.13 shows the performance with a simulated speech input of a DSCDM system which was optimized for (a) speech operation and (b) operation with an 800Hz sinewave.

One can clearly see that if a delta modulator is to be used with speech, the optimization should be carried out using speech or simulated speech, otherwise the optimum performance will not be obtained. Figs 4.12 and 4.13 also clearly show that the performance obtained using 800Hz sinewaves is not necessarily an indication of the performance of the delta modulator when subject to speech.

4.5.3 Hardware

The DSCDM system described in the previous sections was constructed. IC's were used for both the analogue circuitry and the digital circuitry. The block diagram of the circuitry is shown in figs 4.14, 4.15 and 4.16, and further details of

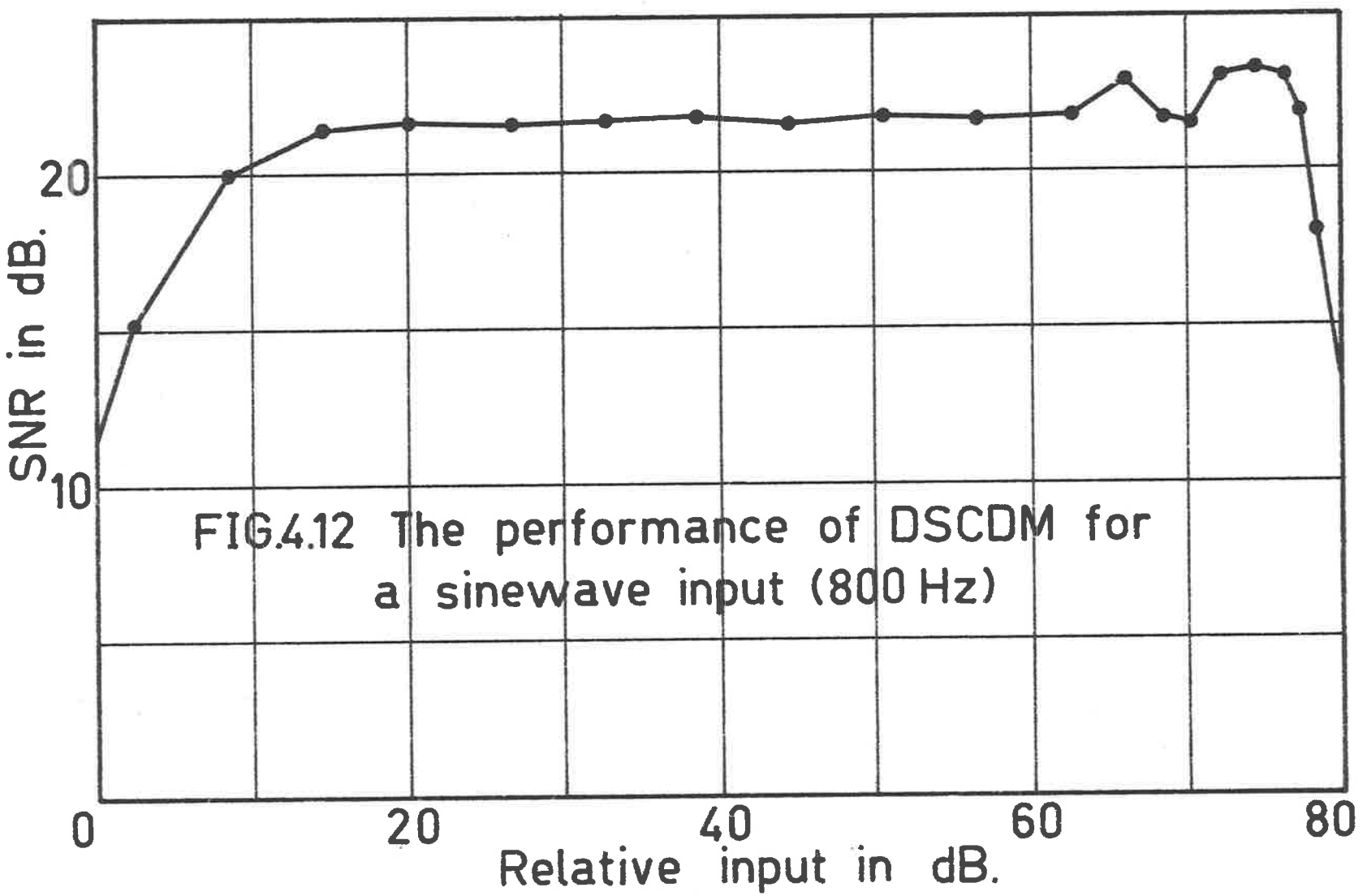


FIG.4.12 The performance of DSCDM for a sinewave input (800 Hz)

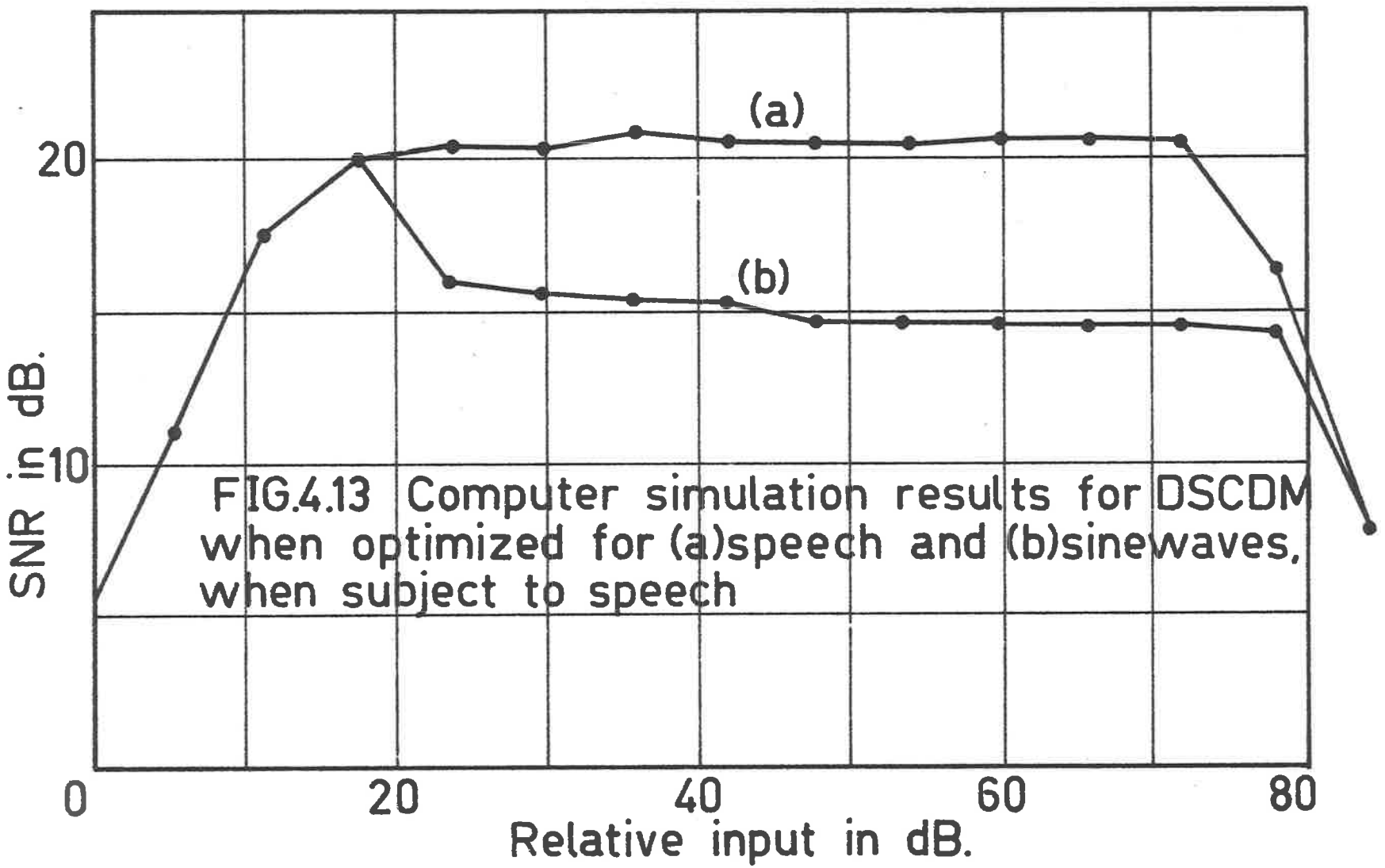


FIG.4.13 Computer simulation results for DSCDM when optimized for (a)speech and (b)sinewaves, when subject to speech

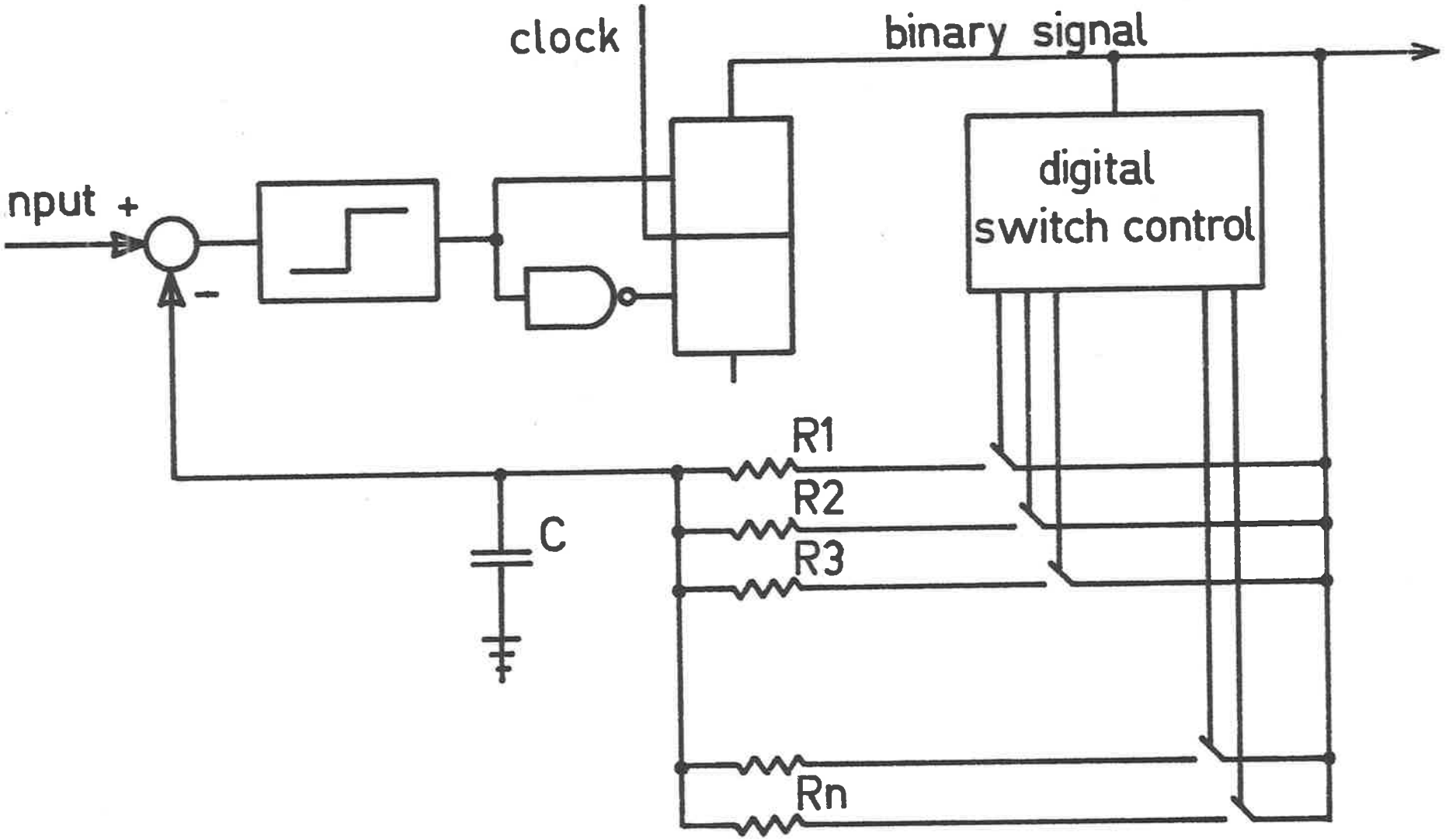
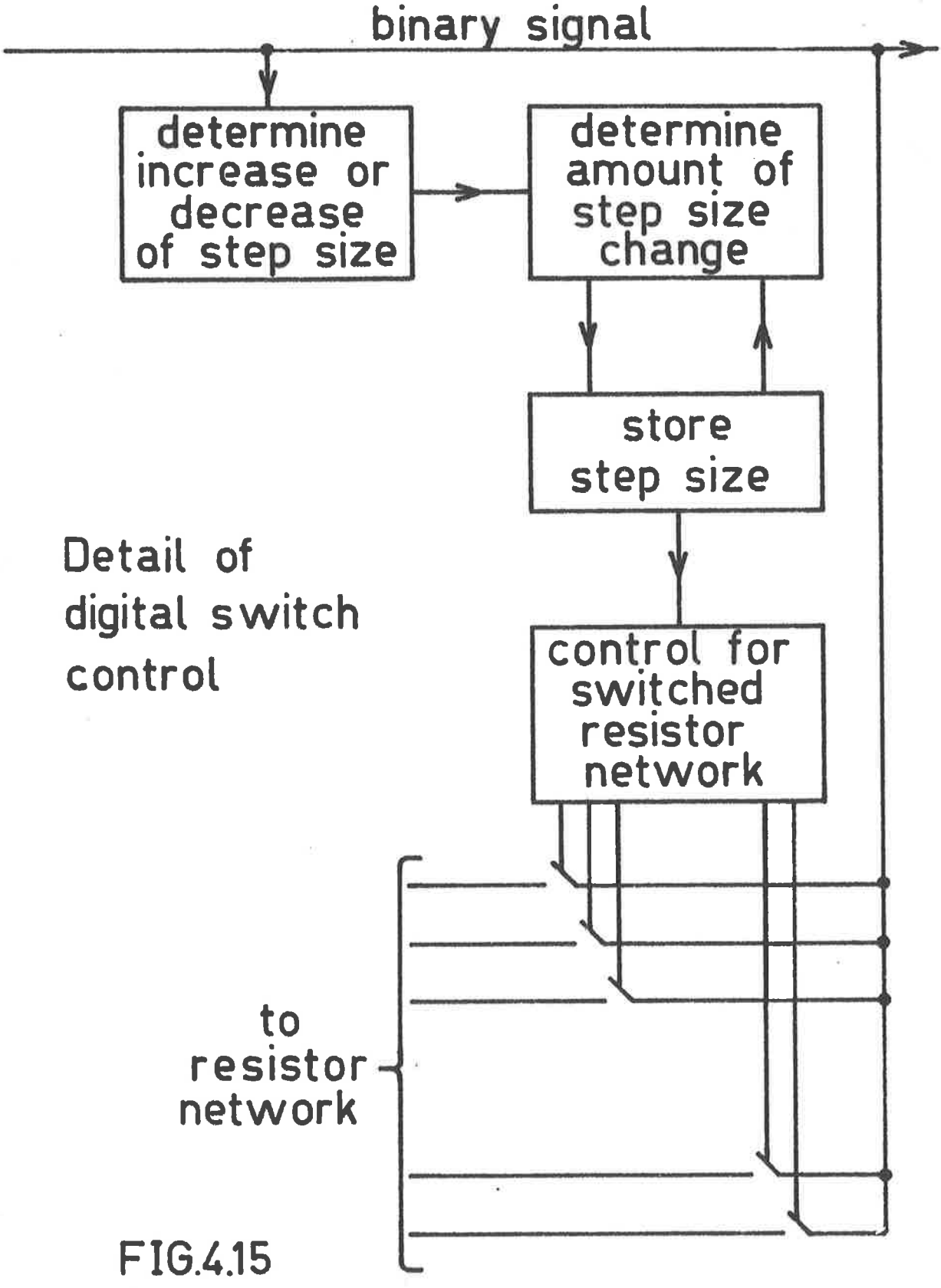


FIG.4.14 Digital syllabic
companded delta modulator block diagram.



Detail of digital switch control

FIG.4.15

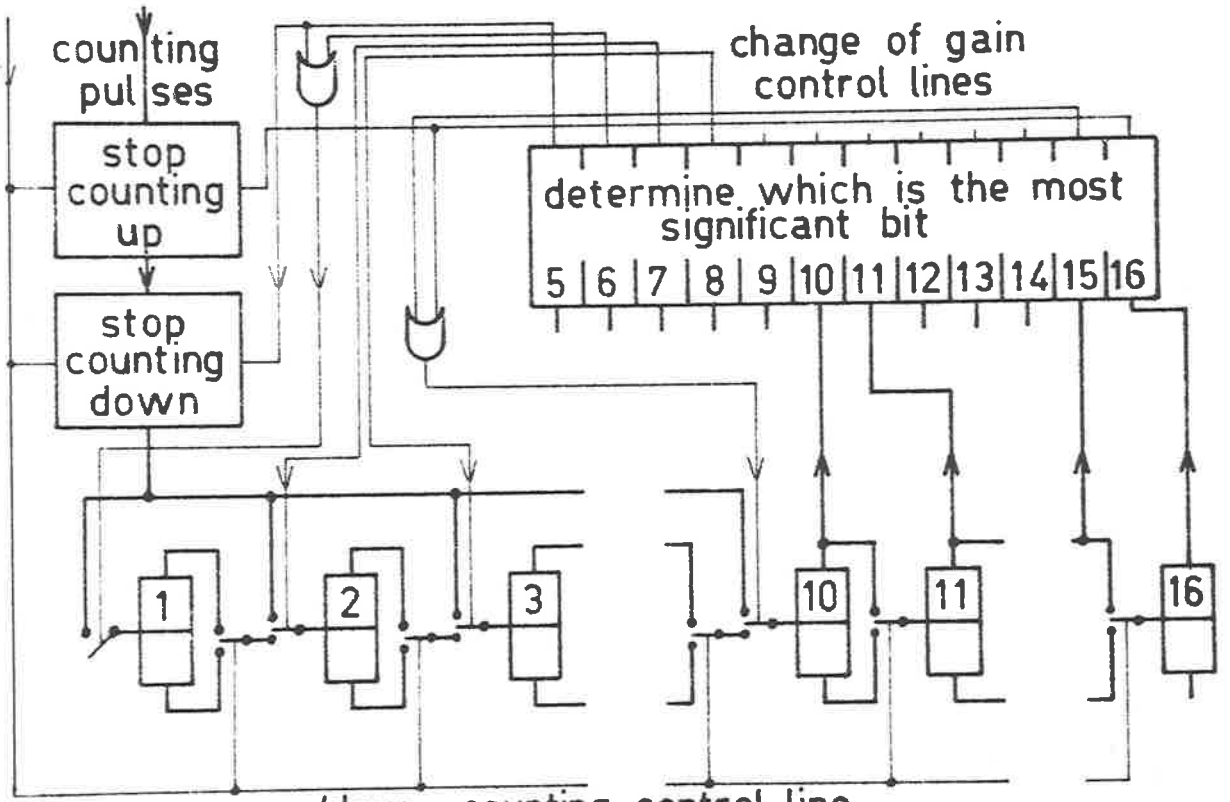


FIG.4.16 Circuit to store the gain and to calculate the change in gain

the hardware shown in Appendix 2.4.

To give some idea of the circuit complexity, 131 RTL digital IC's, 4 analogue IC's and 17 transistor switches, incorporating 4 transistors each, were used in the modulator alone. The demodulator was of similar complexity except that one analogue IC is used.

The number of digital IC's will of course depend on the types of IC that are used. It is however feasible to manufacture the entire digital circuitry in one chip, using large scale integration.

The complexity is proportional to the companding ratio in dB, since each 6dB increase requires an extra bit to be added to the forward and reverse counter containing the step size.

A companding ratio of 60dB was required, which according to section 4.3.4 and 4.5.2 made the largest step size $2^{15}-1$ and the smallest step size 2^5. The values 2^{15} and 2^5-1, simplify the logic connections and were thus used, making the companding ratio $\frac{2^{15}}{31}$ i.e. 60.5dB.

In order to obtain all the required step sizes, the integrator shown in fig 3.4 (b) was used. Each resistor is switched to the positive rail, the negative rail or to ground. The ratio of the smallest to the largest resistor was 2^{15} to 1 i.e. 32768:1. The largest resistance was chosen to be 6.5MΩ which made the smallest 200Ω . The 200Ω resistor, supplies

a current of 75mA which is more than the output current capability of normal operational amplifiers, so that a power integrator had to be used.

The comparator must provide reliable switching on the smallest step size and yet be able to handle the largest input signals as well, so that a dynamic range of 80dB was required.

Fig 14.17 shows a photograph of the hardware for the modulator.

The hardware operated as predicted by the theory as can be seen from the photographs in fig 14.18, which show oscilloscope traces of the input and the demodulated output when the DSCDM system was subject to a 625Hz sinewave of various amplitudes. The sinewave was synchronised to the sampling frequency in order to obtain stationary traces on the oscilloscope.

Fig 4.11 also shows a comparison between the measured performance obtained with the test equipment described in chapter 2, and the results obtained by computer simulation. It can be seen that there is good agreement between the two results. The difference for large signals are due to the integrator limiting, while the differences for small input signals are due to switching spikes and other noise being measured with the demodulated signal.

Actual speech, a tape recording of a newscast, was used for the measurements in fig 4.11.

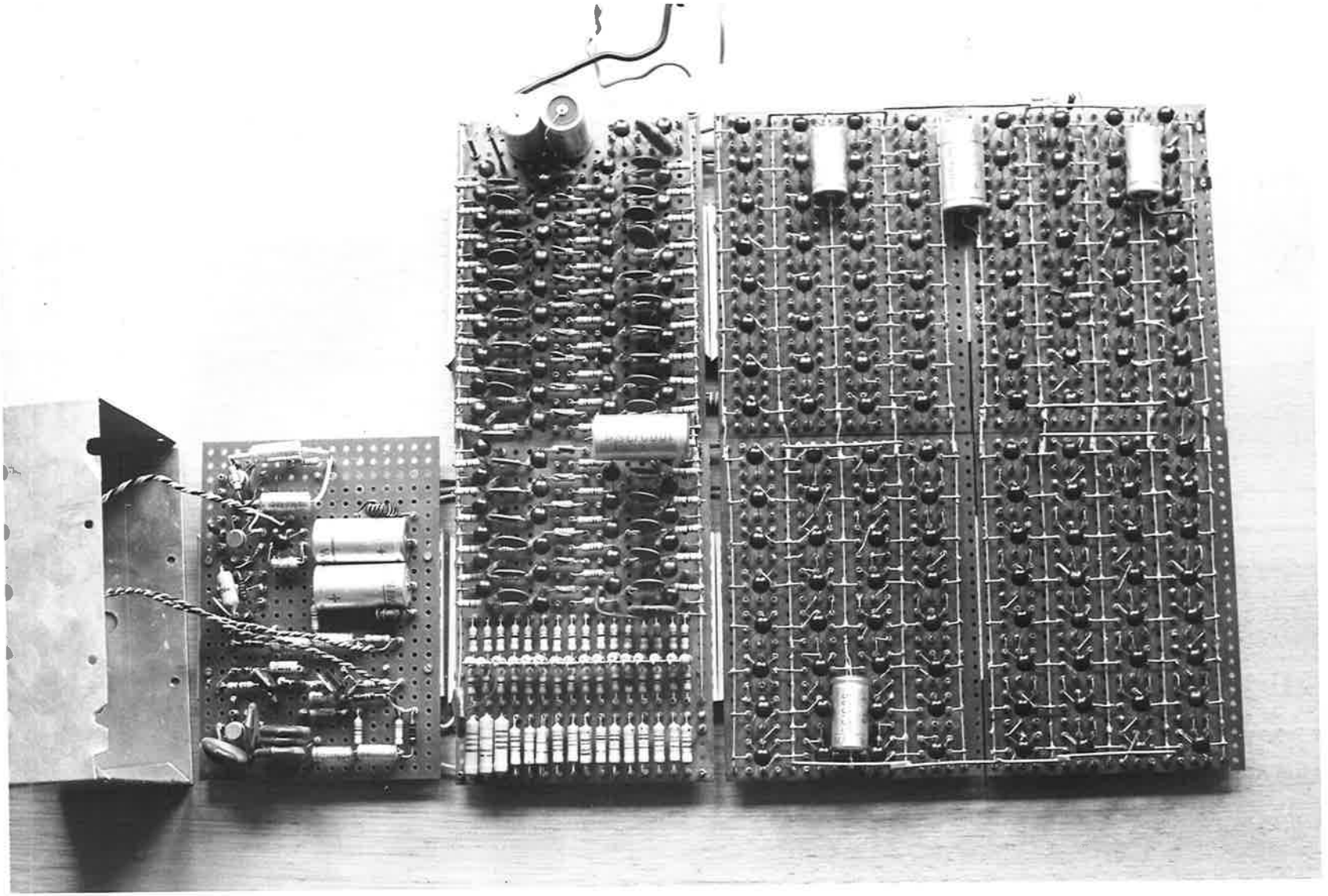
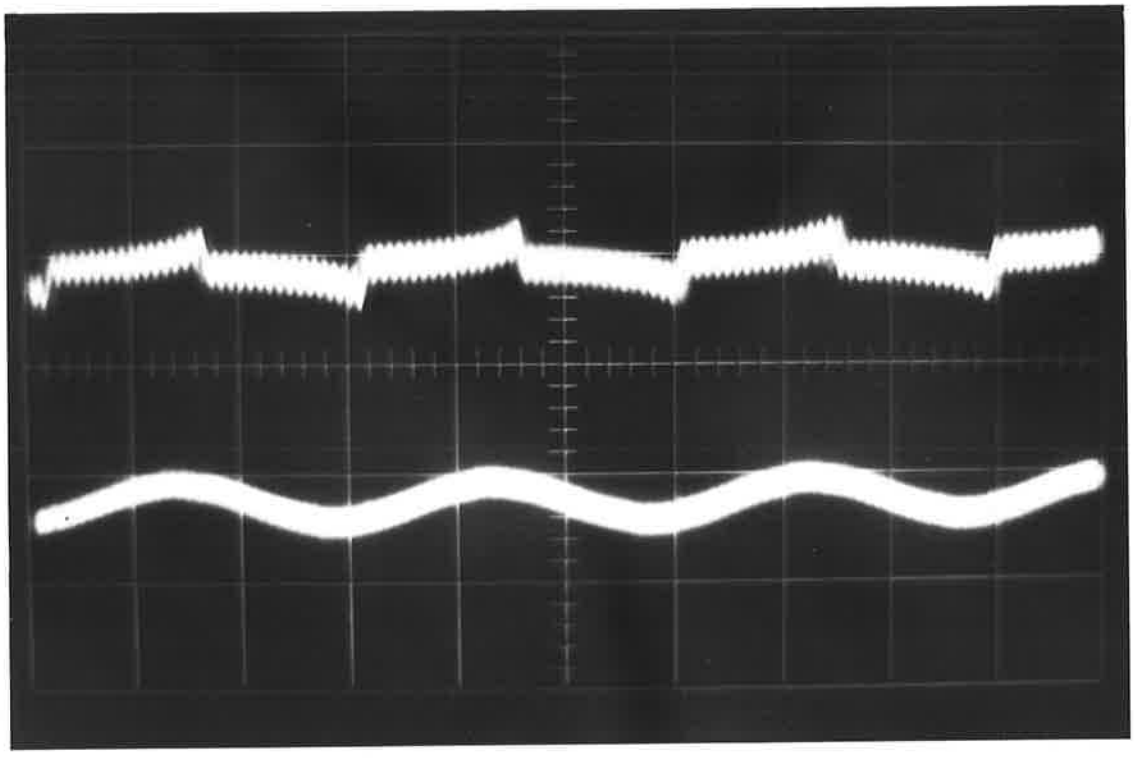


FIG.4.17 DSCDM Hardware



5mV/cm

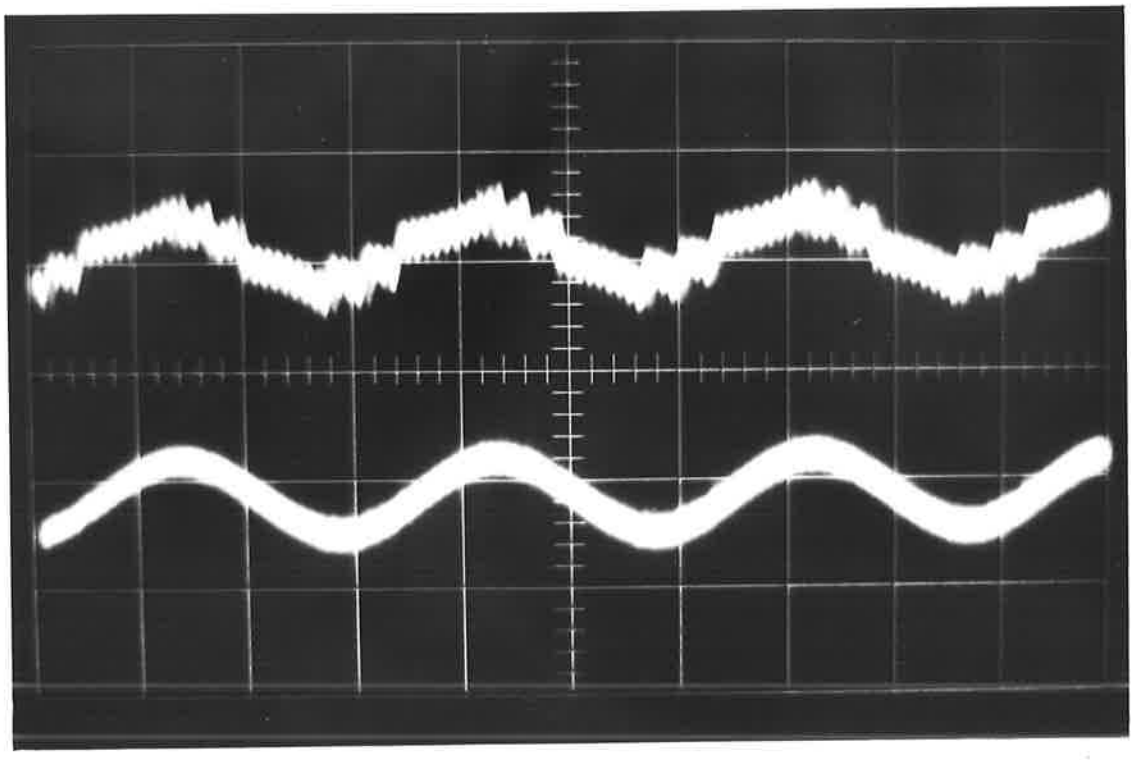
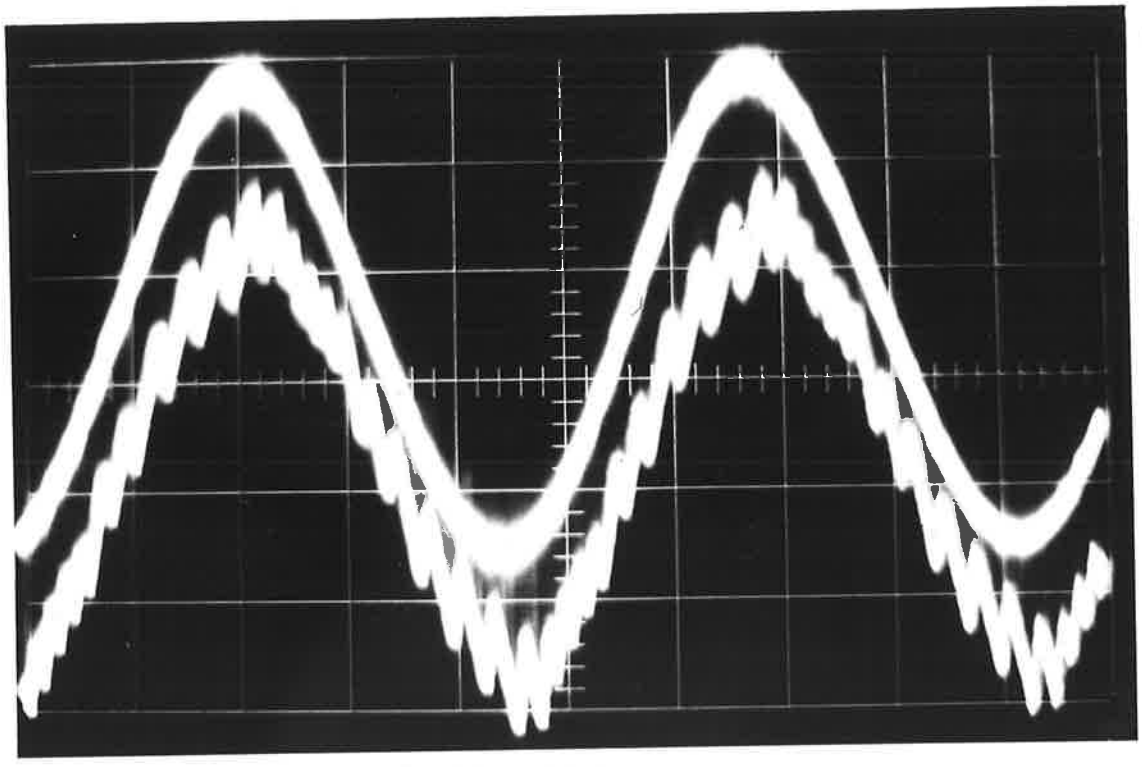


FIG.4.18(a) 5mV/cm



5mV/cm

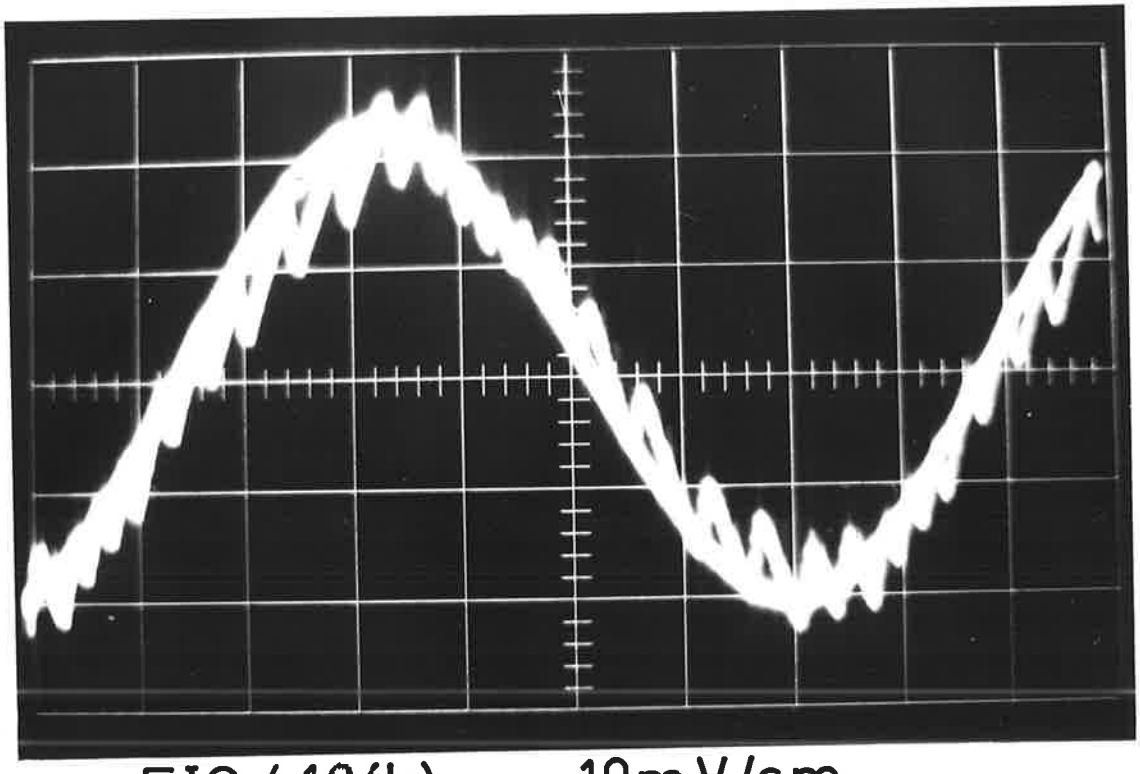
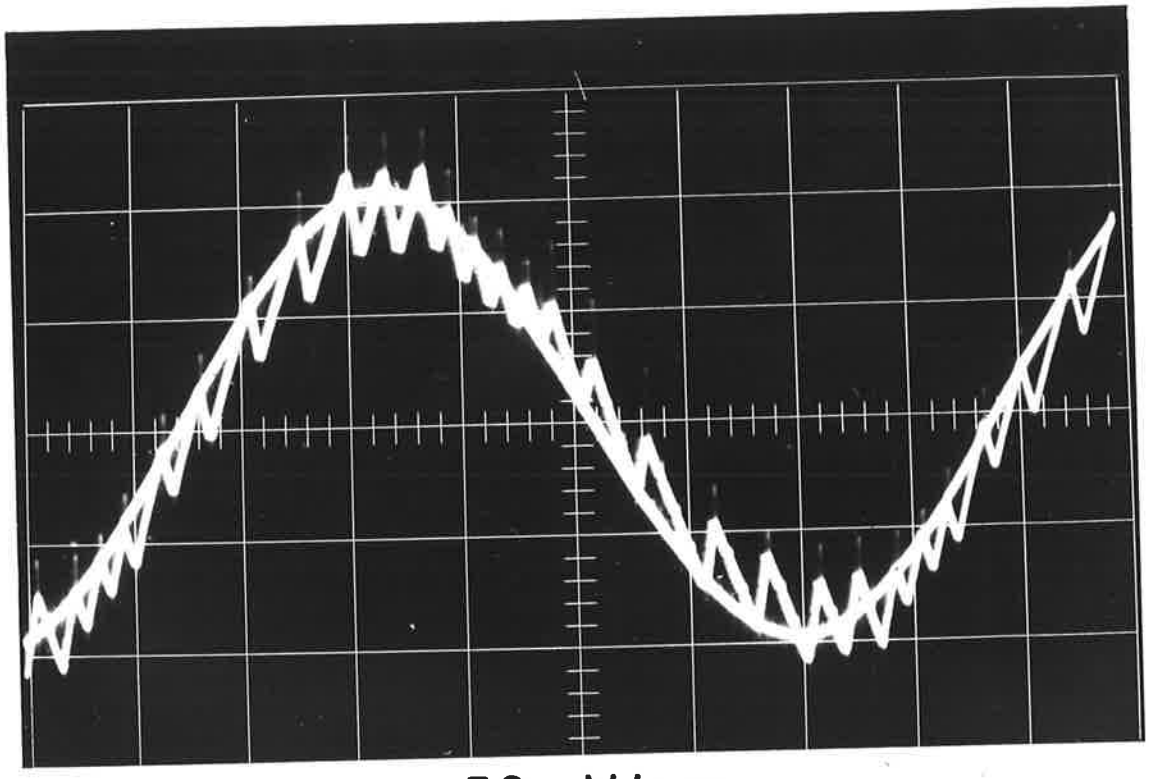


FIG.4.18(b) 10mV/cm



50mV/cm

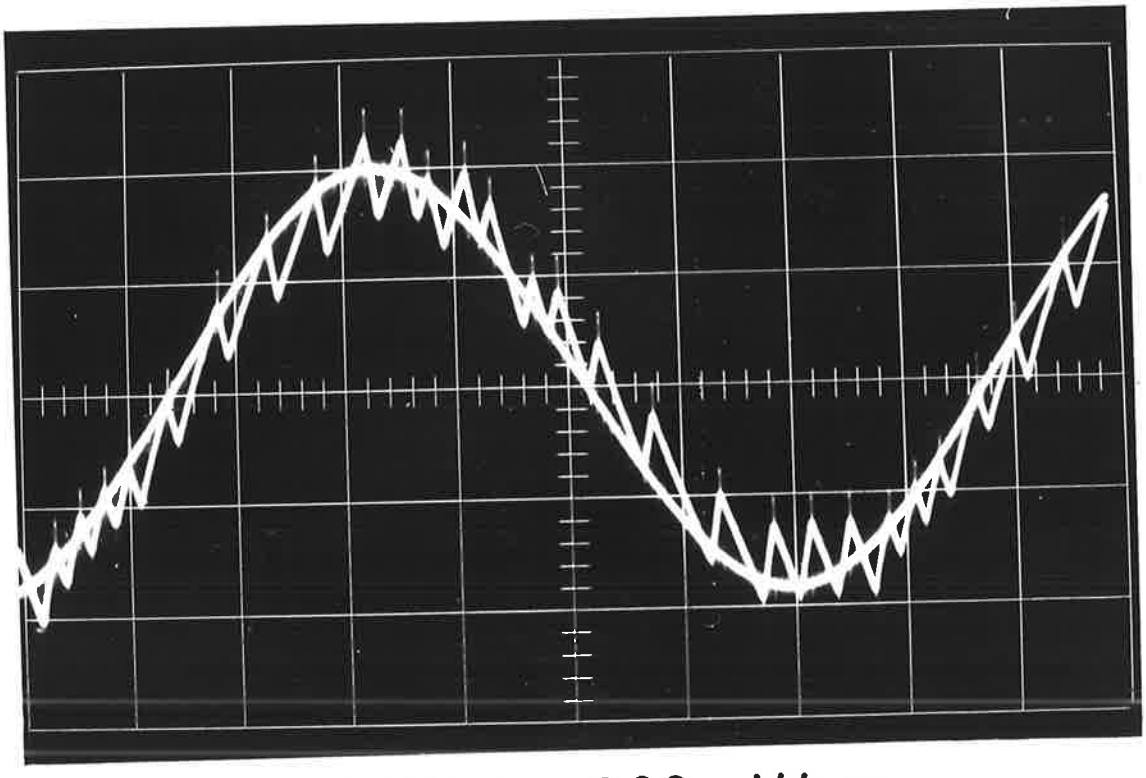
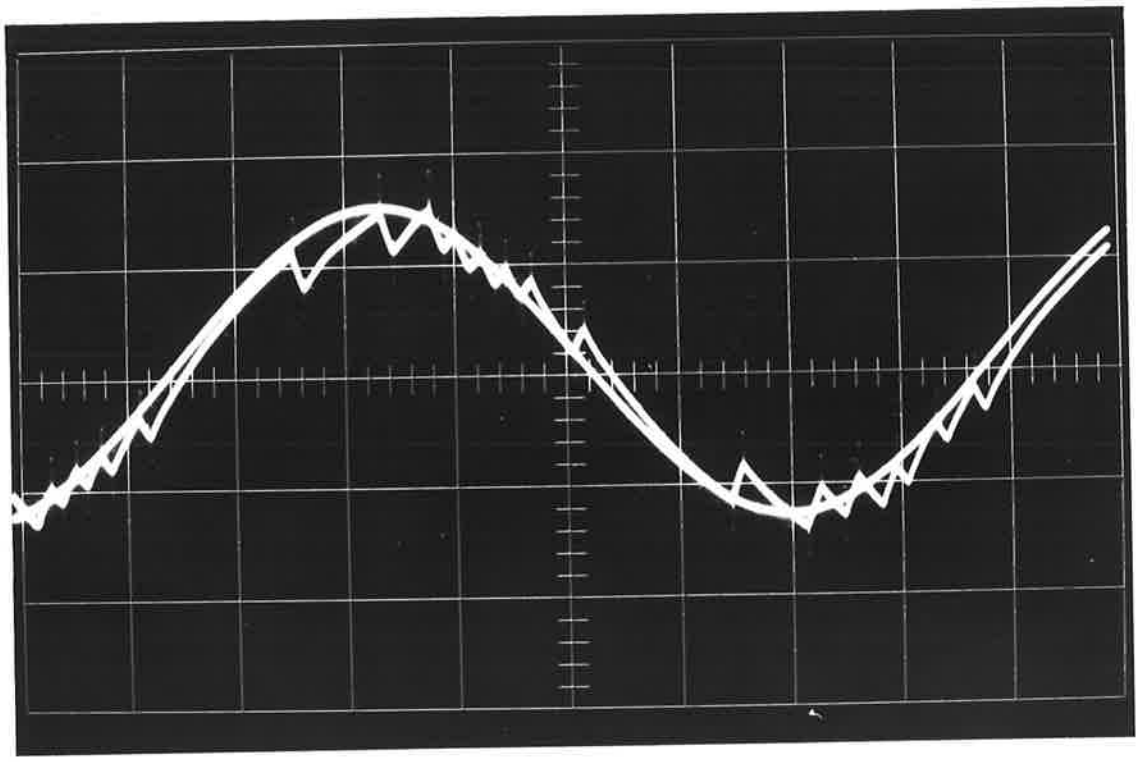


FIG. 4.18(c) 200mV/cm



5V/cm

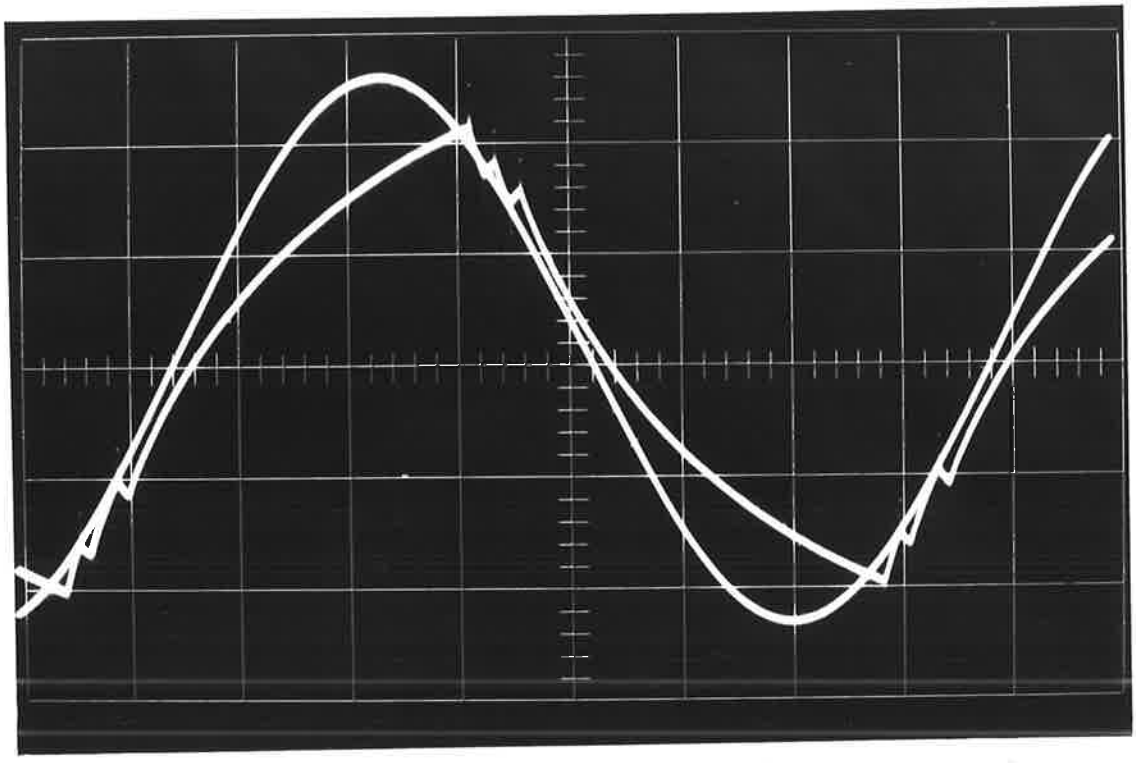


FIG.4.18(e) 5V/cm

4.6 Extension to other Modulators

The principles discussed in section 4.3 can be applied to PCM and ΔPCM as well. One must find control words, the relative occurrence of which vary with signal power. These control words are easy to obtain since for PCM the transmitted signal is made up of binary words, which directly represent the amplitude of the signal. From this binary signal one can easily detect whether the input is greater than a certain level. For instance detecting the most significant bit will give a signal whenever the input is greater than half the maximum amplitude.

Computer simulation was carried out in order to apply the digital syllabic companding to PCM. 7 bit PCM was chosen with a sampling frequency of 8KHz, giving a transmission rate of 56K bits/sec. The control word chosen was the two most significant bits not being zero, giving an output if the amplitude is greater than a quarter of the maximum amplitude. The best performance in keeping with hardware simplicity was found to occur when the step size is increased by 5×2^{n} and decreased by 2×2^{n} when the contents of the counter are between $2^{(n+4)}$ and $2^{(n+5)}-1$. The performance cannot be improved much by using a finer step size graduation, such as 9 or 11 $\times 2^{n-1}$ and $3 \times 2^{n-1}$ respectively, but this will lead to more complex circuitry. The companding ratio was again chosen to be 60dB and the resulting performance is shown in fig 4.19.

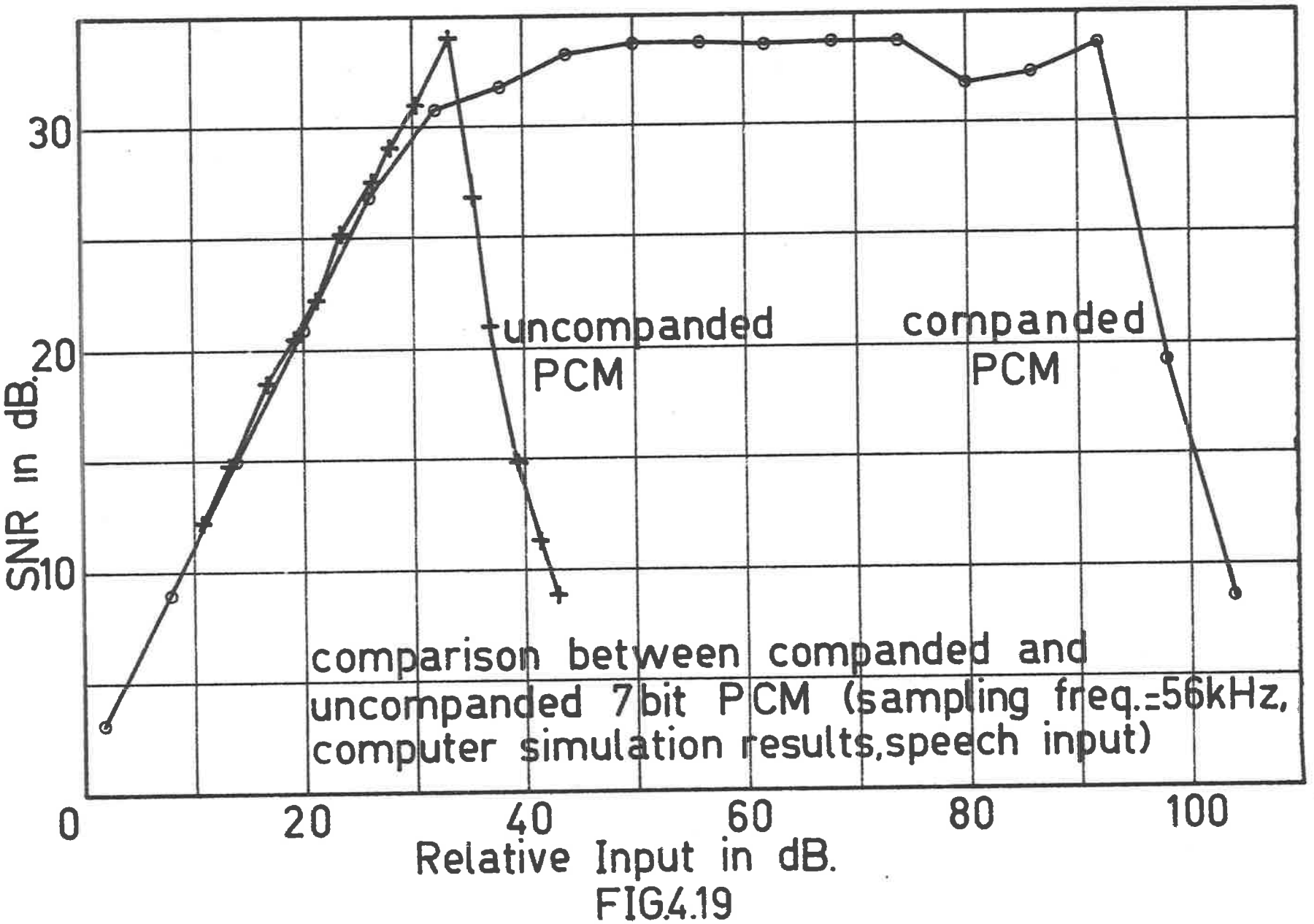

30
20
10
SNR in dB.
uncompanded
PCM
companded
PCM
comparison between companded and
uncompanded 7 bit PCM (sampling freq.=56kHz,
computer simulation results,speech input)
0
20
40
60
80
100
Relative Input in dB.

FIG.4.19

The digital syllabic companding principles can also be applied to PCM, Δ PCM and Δ M systems using instantaneous companding as well, so that double companding can be obtained.

4.7 Conclusions

The application of digital syllabic companding to delta modulation has been shown to extend the dynamic range to any required limit without causing a degradation in the maximum SNR obtainable. By proper design of the companding this maximum SNR can be obtained over a very wide dynamic range.

Transmission errors have the same effect as for the uncompanded modulators, except that they cause an error in the step size. Under normal circumstances however, the step sizes become the same during the pauses between words. Provided the differences between the step sizes is only a few dB, the errors are not objectionable.

The digital syllabic companding has been shown to be applicable to other modulation systems, such as PCM or ΔPCM as well.

CHAPTER 5

COMPUTER SIMULATION

5.1 Introduction

It is extremely difficult if not impossible to construct and analyse a mathematical model for a nonlinear system such as delta modulation with the required accuracy, particularly if the delta modulator has conditional nonlinearities and is subject to a random input, as is the case in this thesis.

It is however possible to simulate the input, the delta modulator and the test equipment on a digital computer thus obtaining an indication of the performance of the delta modulator.

The computer simulation involves using the input and possibly previous values of the input and output, to calculate the output that would be obtained from the equipment to be simulated. These calculations are repeated many times, enabling the performance of the equipment to be obtained. The process can best be illustrated by the use of a simple example. If one is to simulate an integrator, this can be done by the statement Y = Y + X where X is the input and Y is the output. The new values of the output is equal to the input added to the old value of the output. By generating a series of inputs, one can obtain the output of the integrator due to those inputs. At discrete instants of time the input and output values can be used to draw the time waveforms of the input and output.

5.2 Particular Examples of Simulation

5.2.1 Simulation of Delta Modulation

If the delta modulator and the associated test equipment are to be simulated, each of the units in the hardware must be simulated by a few programming statements and the program must co-ordinate the signal flow to be the same as in the hardware. The block diagram of the system to be simulated is shown in fig 5.1.

The description of the resulting program called RANDEL is shown in Appendix 3.

At each sampling interval the input and output of each of the blocks in the block diagram was determined and the signal and quantization noise energy contributions during this interval were added to the respective previous energy totals to give the total signal and quantization noise energy generated.

After sufficient iterations the process was terminated and the average signal and noise powers were calculated. The number of iterations was chosen by a compromise between the computer time and the accuracy of the result. For most of the programs 3000 iterations were used, in addition to 100 iterations which allowed the system to attain the steady state response. This process was repeated for different input levels, enabling a plot of SNR versus input power to be made.

The listings of the programs used to simulate the delta

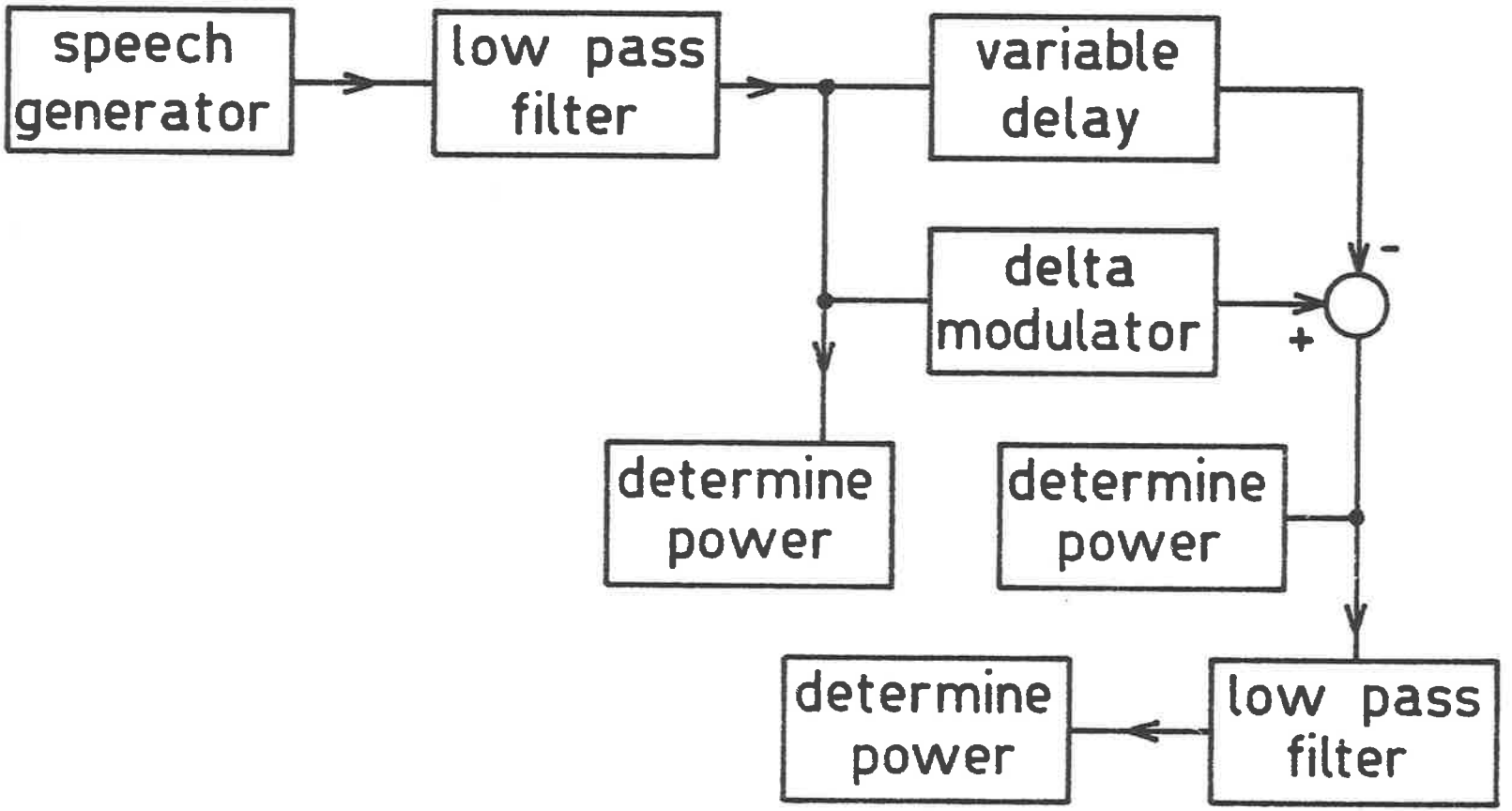


FIG.5.1 Block diagram of the equipment to be simulated

modulators and the relevant subroutines are inserted in Appendix 3. Since about three hundred different computer programs were run, it should be realized that the listings supplied are only a sample. Most of the programs run, however are a slight variation of the ones presented in the Appendix since by altering a few statements an entirely new delta modulator can be investigated.

5.2.2 Simulation of Speech

Since the delta modulators were to be designed for use with speech, the optimization of the modulator required signals that were as close as possible to speech.

There are two properties of speech that must be considered, namely: (1) the frequency spectrum and (?) the variations of power during different syllables.

The required frequency spectrum can be obtained by using a pseudo random sequence as input to a digital filter which has the frequency response of the speech spectrum. Fig 5.2 shows the speech spectrum of a male voice at sea level according to Beranek [23] and compares this with the frequency response of the digital speech filter.

The variation of power during different syllables was obtained by multiplying the output of the speech filter by a random waveform, containing frequency components below 20Hz only. The resulting block diagram for the generation of simulated speech is shown in fig 5.3.

Many workers in this field have ignored the syllabic

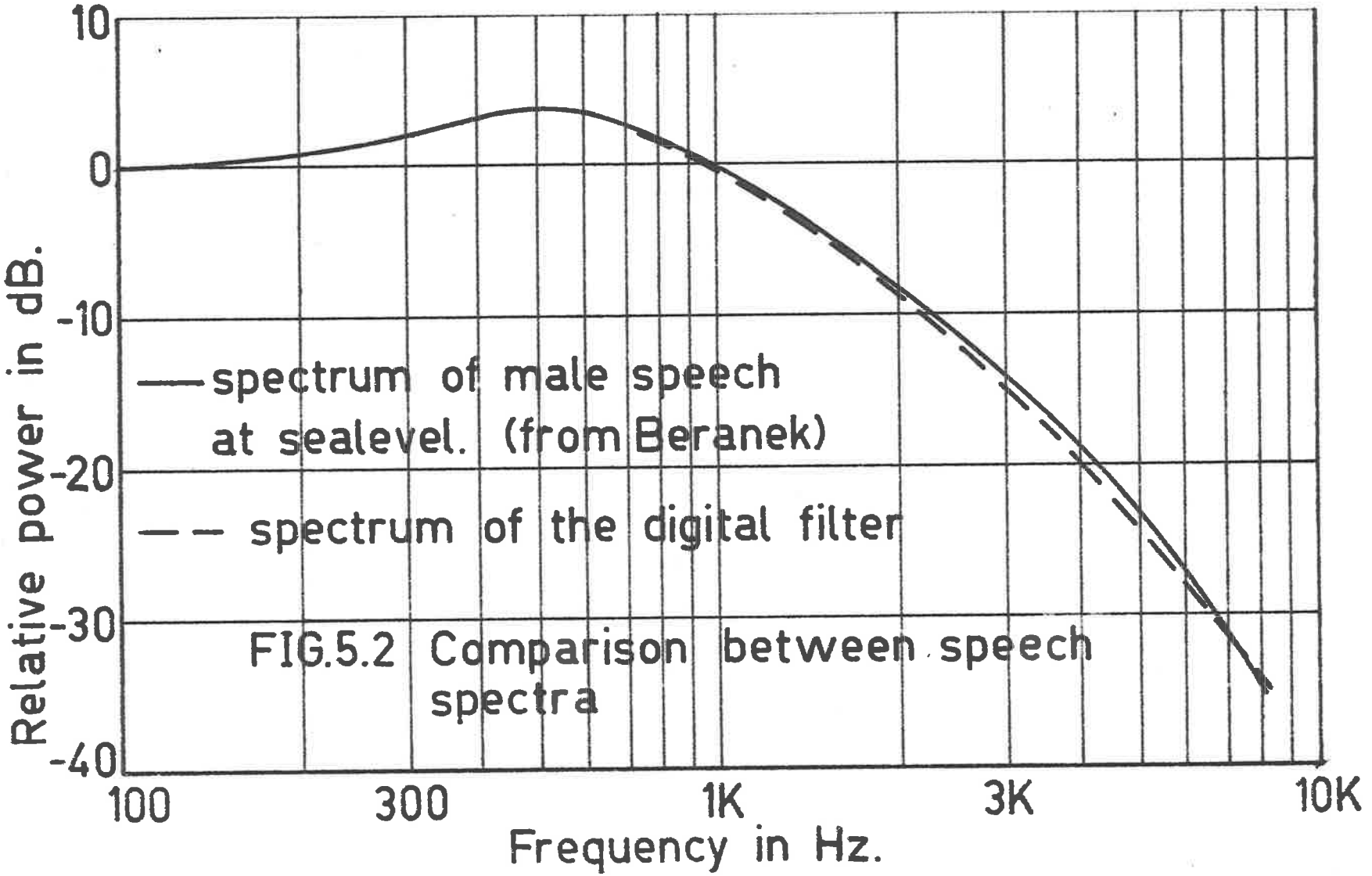


FIG.5.2 Comparison between speech spectra

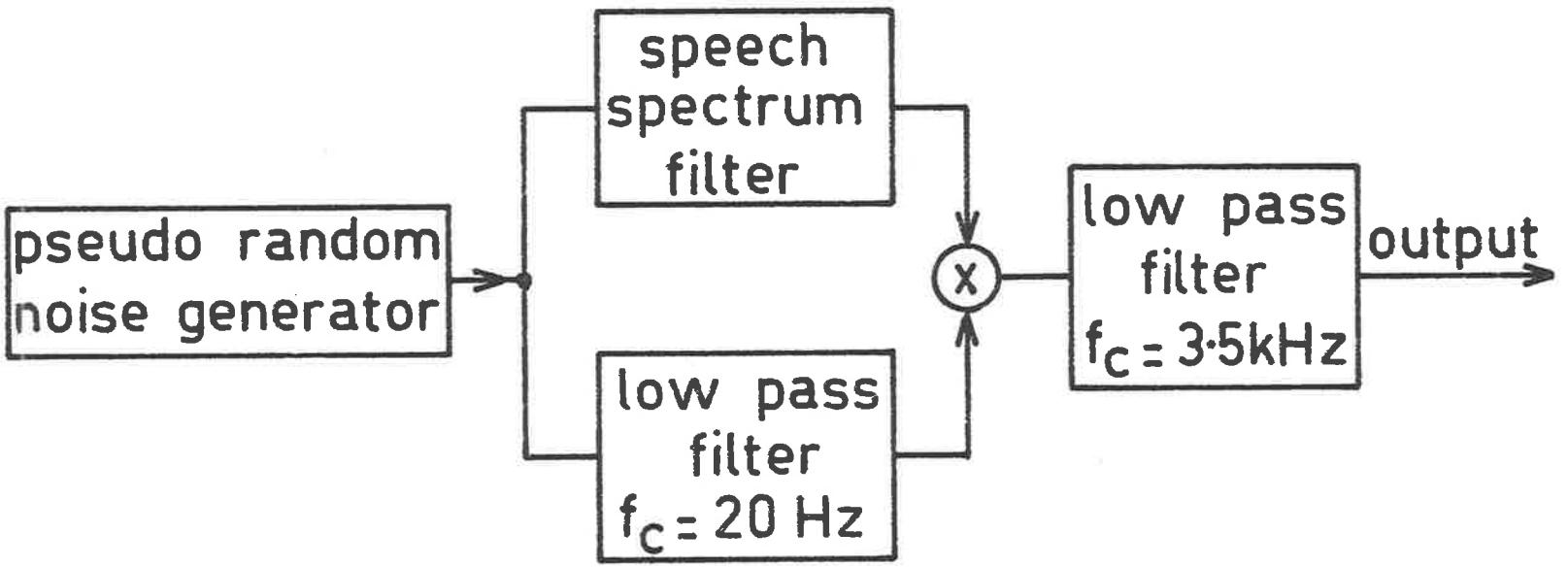


FIG.5.3 Block diagram for generating simulated speech

variation of power in their measurements, particularly if they have used 800Hz sinewaves for testing the delta modulators.

Shindler [18] points out that the controlled-slope delta modulation, used in the telephone network in France has a companding response time that is too long, so that transient distortion occurs. It is thus obvious that if a delta modulator is to be designed for use with speech, syllabic variations of signal power should be considered, so that if companding is used, it can follow the variations of power without the delta modulator deviating from its optimum performance.

The simulated speech obtained above is filtered by a low pass filter with a cut off frequency of 3.5KHz to obtain the required simulated speech.

5.3 Results

The results of the computer simulation of NDDM and DSCDM have been discussed in Chapters 3 and 4 respectively.

The results of the computer simulation for SIDM and PCM are presented here, together with a comparison of the results obtained by other workers.

Fig 5.4 shows the performance of SIDM for different sampling frequencies and with simulated speech as input. An ideal integrator was used in the feedback loop.

Fig 5.5 shows the maximum SNR obtained from de Jager's

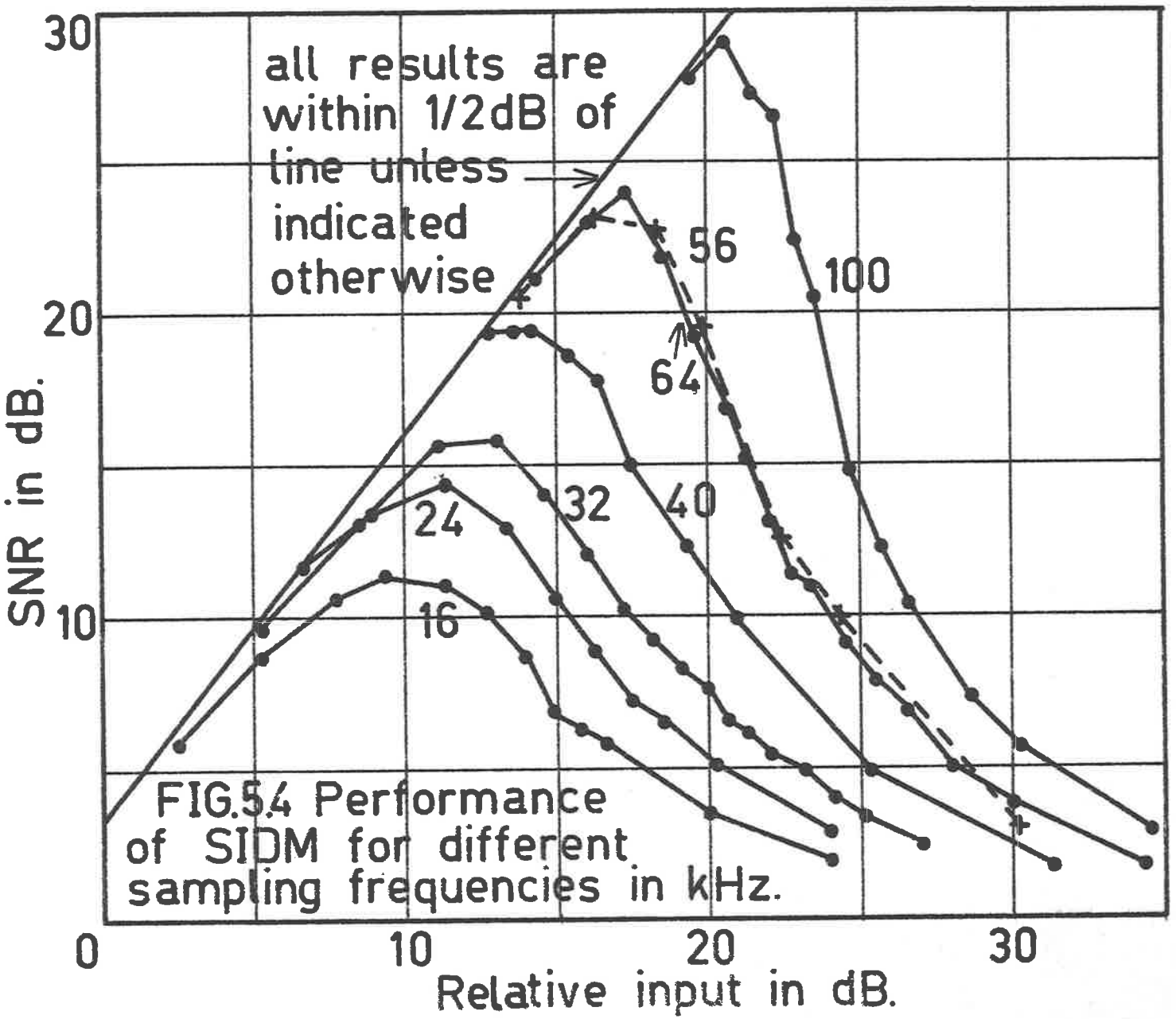


FIG.5.4 Performance of SIDM for different sampling frequencies in kHz.

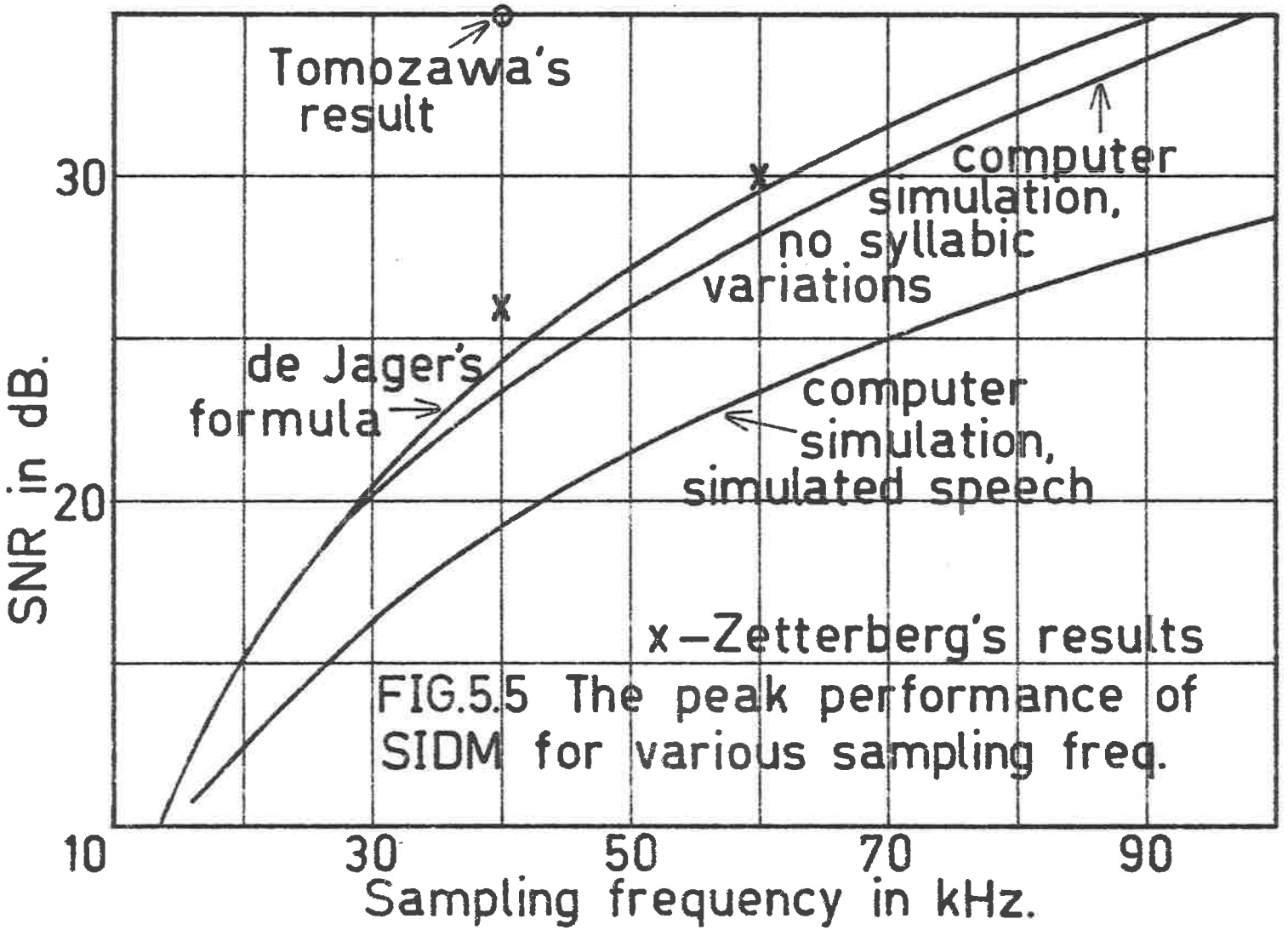


FIG.5.5 The peak performance of SIDM for various sampling freq.

formula [2], the results of other workers and from computer simulation by the author.

De Jager's formula and the results obtained by Tomozawa [10,11] assume speech can be represented by an 800Hz sinewave. It can be seen that optimistic results are obtained. Zetterberg [3] developed a mathematical model for speech, using Markov chains, but did not take syllabic variations of power into consideration.

Fig 5.6 shows the performance of PCM obtained by computer simulation for an 8KHz sampling frequency, a 3.5KHz audio bandwidth and for different word lengths.

Fig 5.7 shows a comparison between the peak performance of PCM, obtained by computer simulation and results obtained by Zetterberg [3]. It can be seen that the computer simulation results, obtained using speech without syllabic variations, agree remarkably well with those obtained by Zetterberg.

Fig 5.8 is a comparison between the maximum SNR's for PCM and SIDM as obtained from computer simulation. It can be seen that SIDM has a superior performance to PCM for transmission rates below 28 K bits/sec.

At transmission rate of 40 K bits/sec, the SNR of PCM exceeds that of SIDM by 4dB and that of DSCDM by 2dB.

Delta modulation does however have the following advantages:

1) The sampling frequency is higher so that the low pass

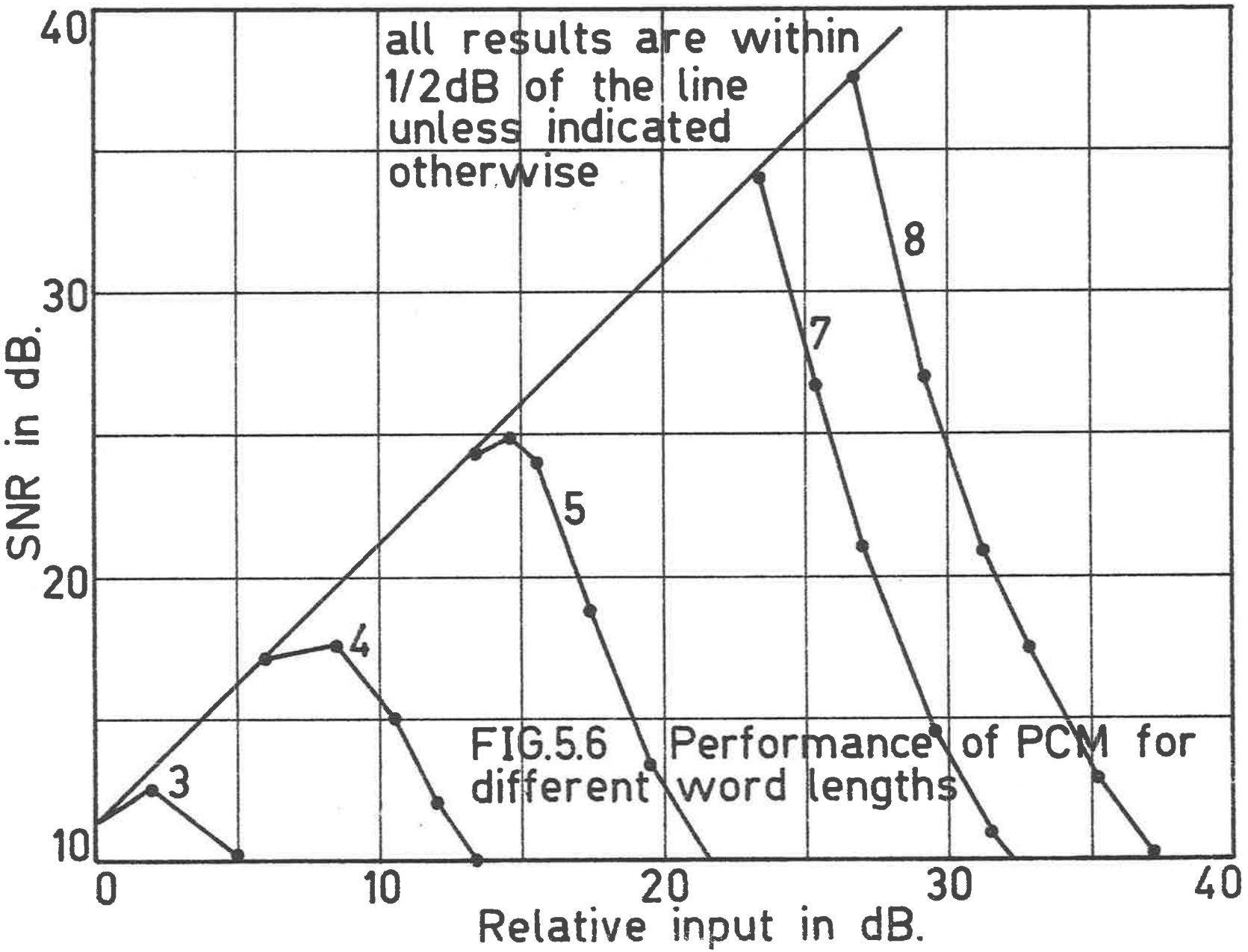


FIG.5.6 Performance of PCM for different word lengths

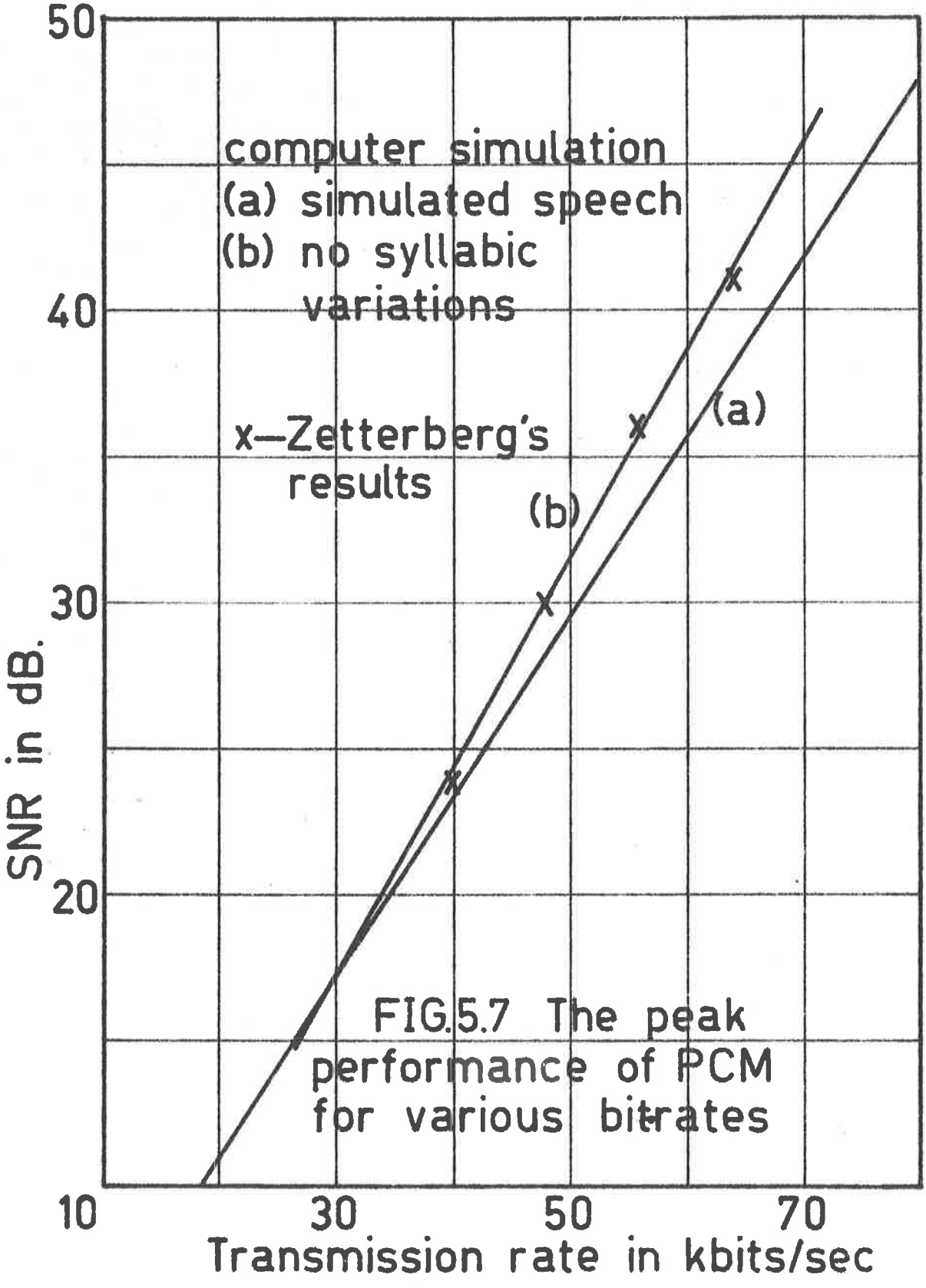


FIG.5.7 The peak performance of PCM for various bitrates

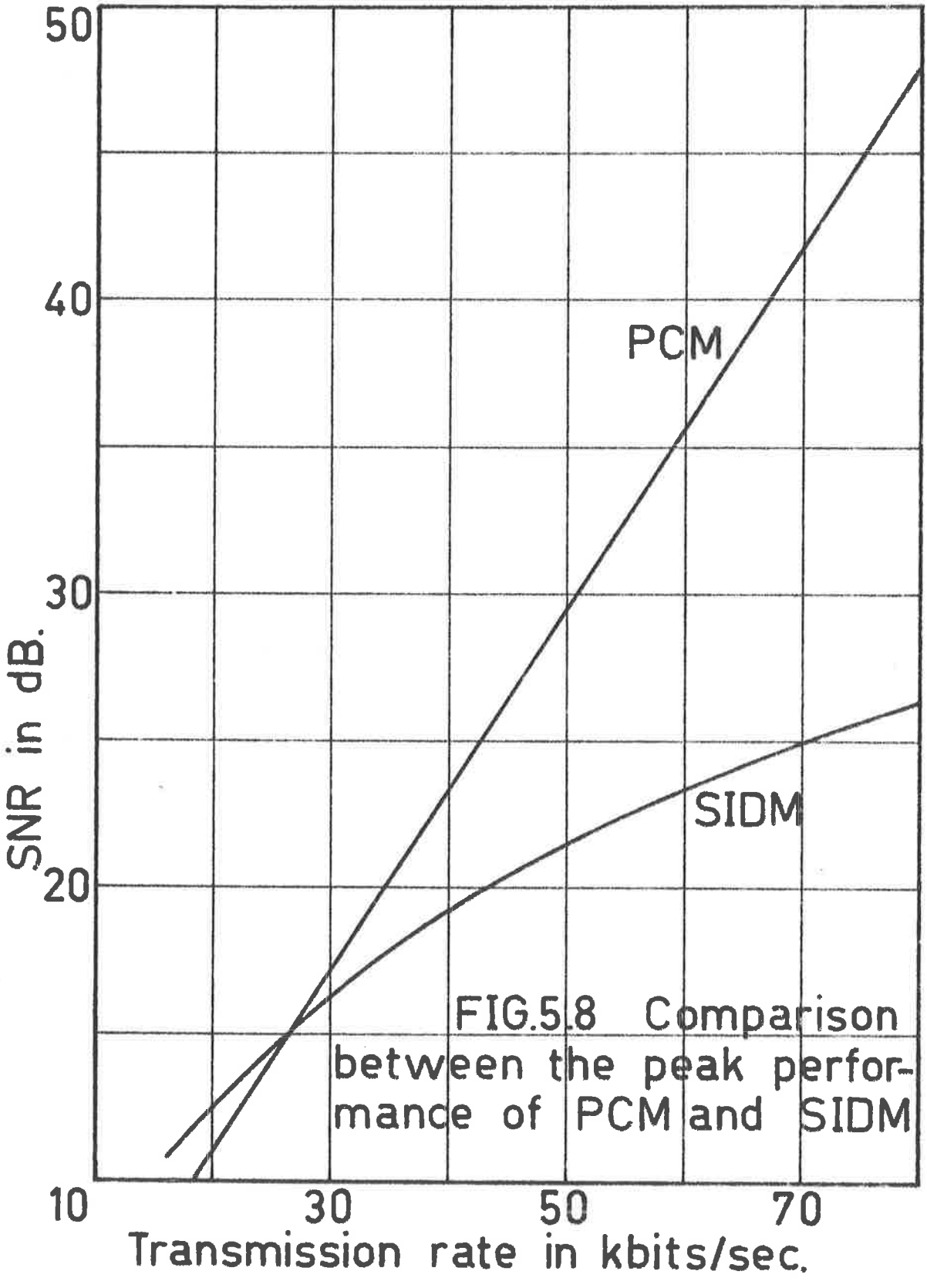


FIG.5.8 Comparison between the peak performance of PCM and SIDM

filters required need not have such a sharp cut-off. Fig 5.9 shows a comparison between the frequency response for the filters used in PCM and SIDM.

For PCM a 6th order Cauer-Chebychev (CC065046) filter [24] was used and for SIDM a 4th order Butterworth filter was sufficient. The filters used for a delta modulator will thus be cheaper than those for a PCM system.

2) For delta modulation there is one bit transmitted per sampling interval, so that no synchronisation bits are required, reducing the complexity of timing circuits compared with PCM.

3) Delta modulation is more tolerant to transmission errors than PCM.

The above points show that for a transmission rate of 40 K bits/sec and speech application, delta modulation will be a more economic system than PCM.

The performance of delta modulation with a sampling frequency of 40KHz is quite acceptable for speech transmission, particularly if the delta modulator uses syllabic companding.

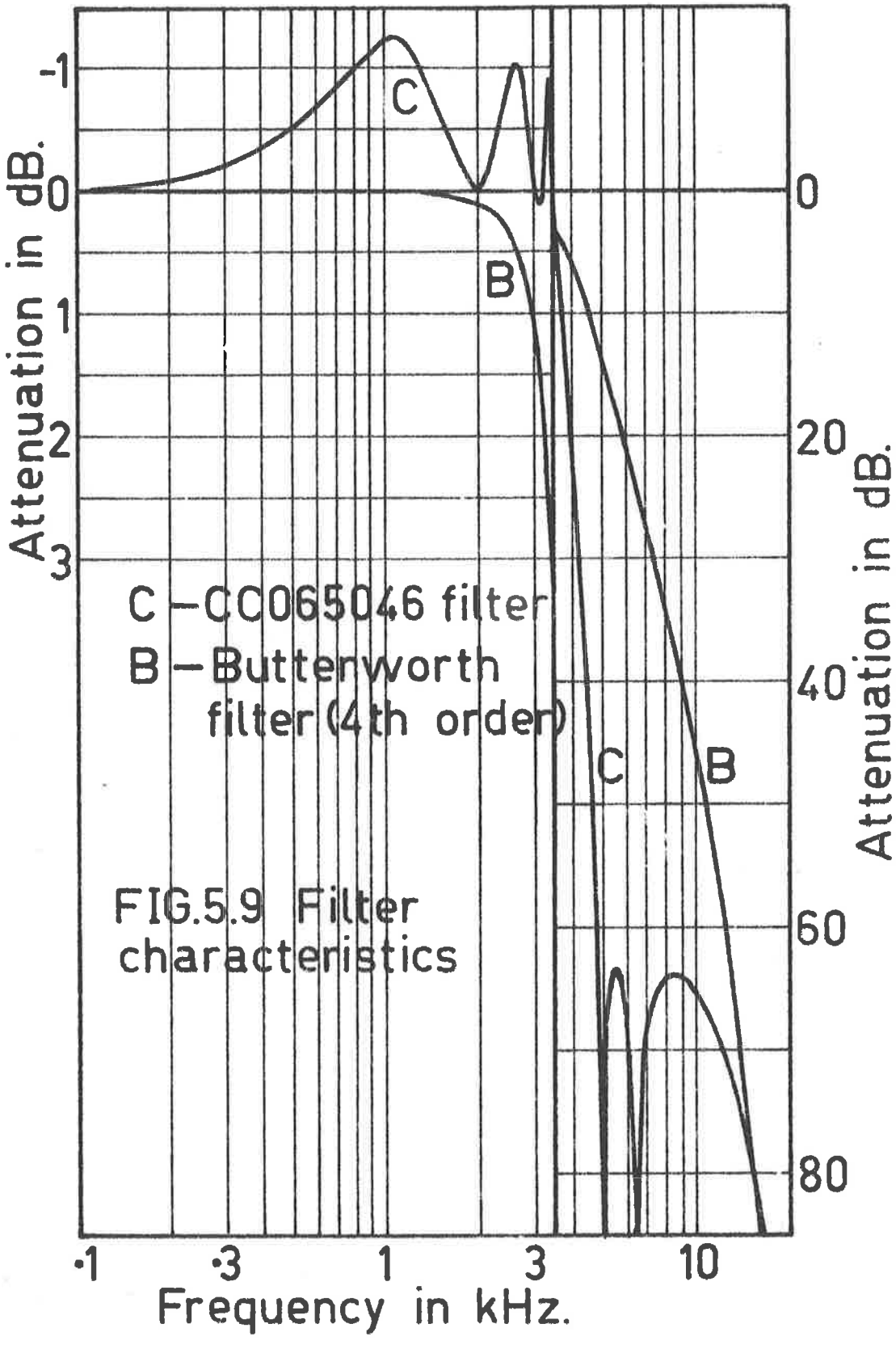


FIG.5.9 Filter characteristics

CHAPTER 6

CONCLUSIONS

Because delta modulation is a form of analogue to digital conversion and the binary transmitted signal contains information from which the modulation depth can be determined, digital circuitry is ideally suited to the control of companding for delta modulation. Furthermore, provided no transmission errors occur, the amount of companding at the modulator and demodulator will be exactly the same if digital companding is used, while for analogue companding there will normally be differences in the companding at the modulator and demodulator. Finally, digital companding enables precisely controlled conditional nonlinearities to be used in the companding to improve the performance of the delta modulator.

The work presented in this thesis shows that if a delta modulator is to be used with speech, the companding must be designed specifically for speech if the best performance is to be obtained. For DSCDM at a 40KHz sampling frequency and speech input, a system optimized for speech was shown to give a SNR of 5dB more than one optimized for sinewaves over the entire companding range.

In order to evaluate the performance of the delta modulators with speech input, equipment was constructed which allowed any signal to be used to test the performance of the

delta modulator. For both the delta modulators presented in this thesis, there is an excellent agreement between the performance obtained using actual speech and the results obtained from computer simulation. It should be realised that since the delta modulators use conditional nonlinearities in the companding and speech is a nonstationary signal, no simplified mathematical model was developed to represent the delta modulators, since a sufficiently accurate model could not be obtained. Computer simulation however, enabled the performance of the delta modulator to be evaluated with sufficient accuracy.

Two methods of digital companding have been developed by the author and are presented in this thesis, namely: nonlinear digital companding and digital syllabic companding.

Nonlinear digital companding is a form of instantaneous companding which adapts the step size to the instantaneous input signal. It was shown that conditional nonlinearities improve the stability of the delta modulator, enabling a large dynamic range to be obtained.

For speech application and 56KHz sampling frequency NDDM was shown to have a good performance over a 30dB dynamic range. Because NDDM uses instantaneous companding, it was shown to have an excellent transient response and this type of companding will thus be suitable to applications where rapid changes in signal level are encountered such as is the case for T.V. signals.

It was shown that the conditional nonlinearities in the companding can be designed such that the system becomes more tolerant to transmission errors, since the companding is designed to reset itself to the smallest step size if a 10101010 binary transmitted pattern occurs.

Digital syllabic companding adapts the step size to the average input signal power, by determining a measure of the modulation depth from the binary transmitted signal and using this to control the step size. The step size is stored in a forward and reverse counter, and by using different circuitry for the control of this counter, linear and semilogarithmic companding can be obtained. Logarithmic companding can be obtained but the circuitry controlling the counter would be unnecessarily complex. Since the companding ratio is determined by the number of bits in the forward and reverse counter, the dynamic range can be chosen at will, provided the analogue circuitry is capable of handling the required dynamic range.

Hardware for a DSCDM system with a companding ratio of 60dB was constructed. This companding ratio is about 25dB more than has previously been possible [14-18].

If the digital syllabic companding is designed as indicated in this thesis, the maximum SNR can be obtained over the entire range for which companding takes place. Furthermore as shown in fig 4.11, the maximum SNR will be

higher than for the uncompanded system.

The DSCM system proposed in this thesis would be extremely suitable for the transmission of speech in a future digital telephone network.

APPENDIX 1

METHODS FOR THE EVALUATION OF THE PERFORMANCE OF DELTA MODULATION

A1.1 Intelligibility Tests

These tests are usually conducted by recording a large number of words or syllables and replaying these through the delta modulator under test. A team of listeners then record what they think the word is. The correctness or incorrectness of the estimates of the words are used to obtain an in intelligibility score. The results are usually normalised to make the intelligibility 100% if no delta modulator is used.

There are many different types of tests a few of which are described in the report on project Mallard [7]. According to this report Egan [25] showed that the intelligibility scores were not affected by SNR's greater than 30dB, indicating that these tests are only useful if a low sampling frequency is used for the delta modulator. The delta modulators described in this thesis are of sufficiently high quality that a nearly 100% intelligibility score would be obtained.

A second type of test exists where the intelligibility of two different delta modulators is compared, so that one can decide which is better. This enables one to arrange different delta modulators in order of performance but an

absolute standard of performance cannot be obtained.

A1.2 Equivalent White Noise Methods

Recorded speech is played through either a delta modulator or a summing amplifier, where white noise is added to the speech signal. The block diagram of the system is shown in fig A1.1. The listener can listen to either signal. The amount of white noise is varied until both systems have the same fidelity. The signal and noise powers can be measured, so that an equivalent SNR can be obtained.

There are two types of methods: firstly, where the noise is independant of the input signal and secondly, where the noise is proportional to the input signal.

In a normal communication system the noise is generally due to transmission over noisy channels and the noise is thus independant of the input signal.

In delta modulation system, the quantization noise is dependant on the input signal. If no input signal is present, the binary transmitted signal will consist of 101010 etc. pattern and there will be no audio components in the quantization noise, while an audible quantization noise will normally exist if an input signal is present.

For delta modulation it is thus more reasonable to assume that the quantization noise is proportional to the input amplitude than to assume that the quantization noise is constant. So that the second method is preferable for delta

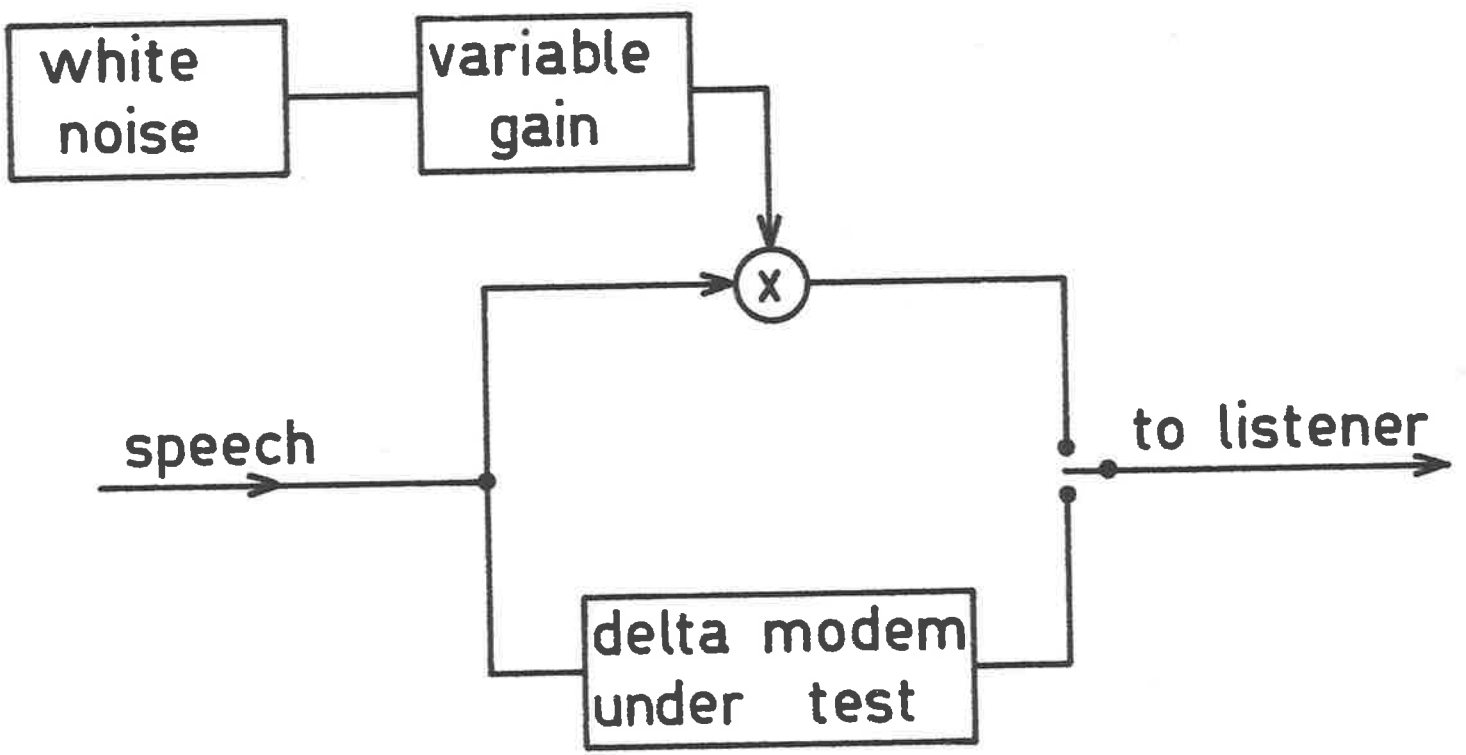


FIG.A1.1 Method for measuring equivalent SNR

modulation.

The British Post Office developed a modulated noise reference unit, which varied the noise proportional to the input signal. The Telephone Standards Group at the Research Laboratories of the Australian Post Office built this system and used it for evaluating the performance of DCDM [17]. By means of some of their unpublished results, a comparison between different methods is available for DCDM at a sampling frequency of 40KHz.

The peak SNR that was obtained using the modulated noise reference unit was 20dB while using noise independant of the input signal gave 30dB. Using an 800Hz sinewave Hauser and Zarda [17] obtained a SNR of 37dB.

It can be seen that widely different results can be obtained, depending on the method used.

A1.3 Notch Filter Method

In the notch filter method a pure sinewave is used as input to the equipment under test and a notch filter is used to remove the input frequency from the output. The remaining signal is then the distortion introduced by the equipment.

A disadvantage of this method for delta modulation is that variations of SNR occur over a narrow range of input signals, giving rise to the SNR characteristic shown in fig 2.3. These variations in SNR have not been reported by other workers.

It is however usual to randomize the input signal by adding band limited white noise to it. The notch filter must then be replaced by a bandstop filter.

Other disadvantages are discussed in Chapter 2.

A1.4 Frequency Analysis Method

This method again uses a pure sinewave as input signal. A spectrum analyser is used to determine the frequencies present in the output. By summing the powers of the harmonics of the input frequency in the output signal, the distortion can be calculated. The disadvantages of using this method for measuring the performance of delta modulation are the same as for the notch filter method.

A1.5 Cancellation Method

With this method the sinewave input is suitably delayed and the gain of the input or output is changed so that the difference signal, shown in fig 2.4 contains no fundamental of the input frequency. This method is similar to the one used for the measuring equipment discussed in Chapter 2, except for the following differences:

1) The network providing the delay does not have to give a frequency independant time delay. A simple RC network can thus be used instead of the delta modem and the tapped digital delay line used in the measuring equipment.

2) For every measurement the gain and delay are adjusted,

while with the measuring equipment the gain and delay are adjusted when no limiting occurs in the delta modulator and the gain and delay are kept at this setting for all measurements.

3) Sinewaves are the only input signals that can be used.

A1.6 Intermodulation Distortion Method

With this method, white noise is passed through a narrow band rejection filter, which removes a narrow region of the noise spectrum. This signal is then used as input to the equipment under test. The output is passed through a band pass filter which removes all frequencies, except for a narrow band corresponding to the gap in the input spectrum. The output from this filter thus only contains signals which are due to distortion.

By shifting the freauency of the band pass and band stop filters over the whole spectrum and adding the distortion contributions due to each section, the distortion can be calculated. This method is however time consuming, particularly if the performance is to be determined for different input powers.

APPENDIX 2

HARDWARE

A2.1 Introduction

The hardware used during the research is presented here. The entire design and construction was carried out by the author. A list of abbreviations and some graphic symbols used in the circuit diagrams are shown in fig A2.1.

A2.2 Measuring equipment hardware

The block diagram of the measuring equipment is shown in fig 2.9. The circuit diagram of the measuring equipment is shown in fig A2.2. The details of the delta modulator are shown in fig A2.3 and those of the multiplier and filter in fig A2.4.

The circuit is self explanatory but a few features can be mentioned.

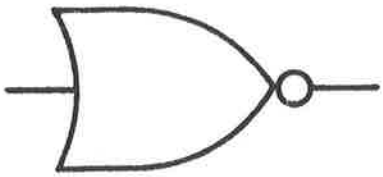
The trimming capacitor in one of the demodulators is to match both demodulators, so that the mismatch of the demodulated signals can be at least 55dB smaller than the demodulated signal.

The lowpass filter shown in fig A2.2 is a 4th order Butterworth lowpass filter.

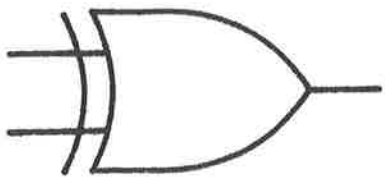
Fig A2.5 shows a photograph of the hardware.

A2.3 Nonlinear digital delta modulation hardware

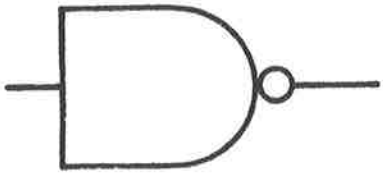
B	Binary transmitted signal
C	Clockpulse for counter
C_{in}	Clockpulse input
C_p	Clockpulse from the timing circuit
D_c	Delay store clockpulse
F	Forward counting
I	Inhibit counting
I_r	Reset inhibit
I_s	Set inhibit
R	Reverse counting



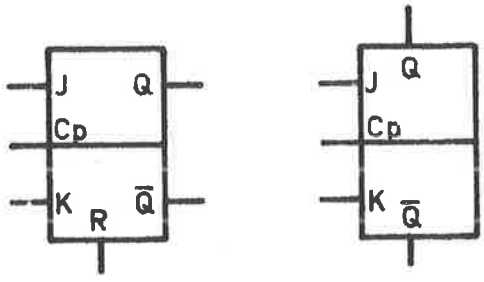
Nor gate



Exclusive or gate



Nand gate



Flip flop

FIG.A2.1 Nomenclature

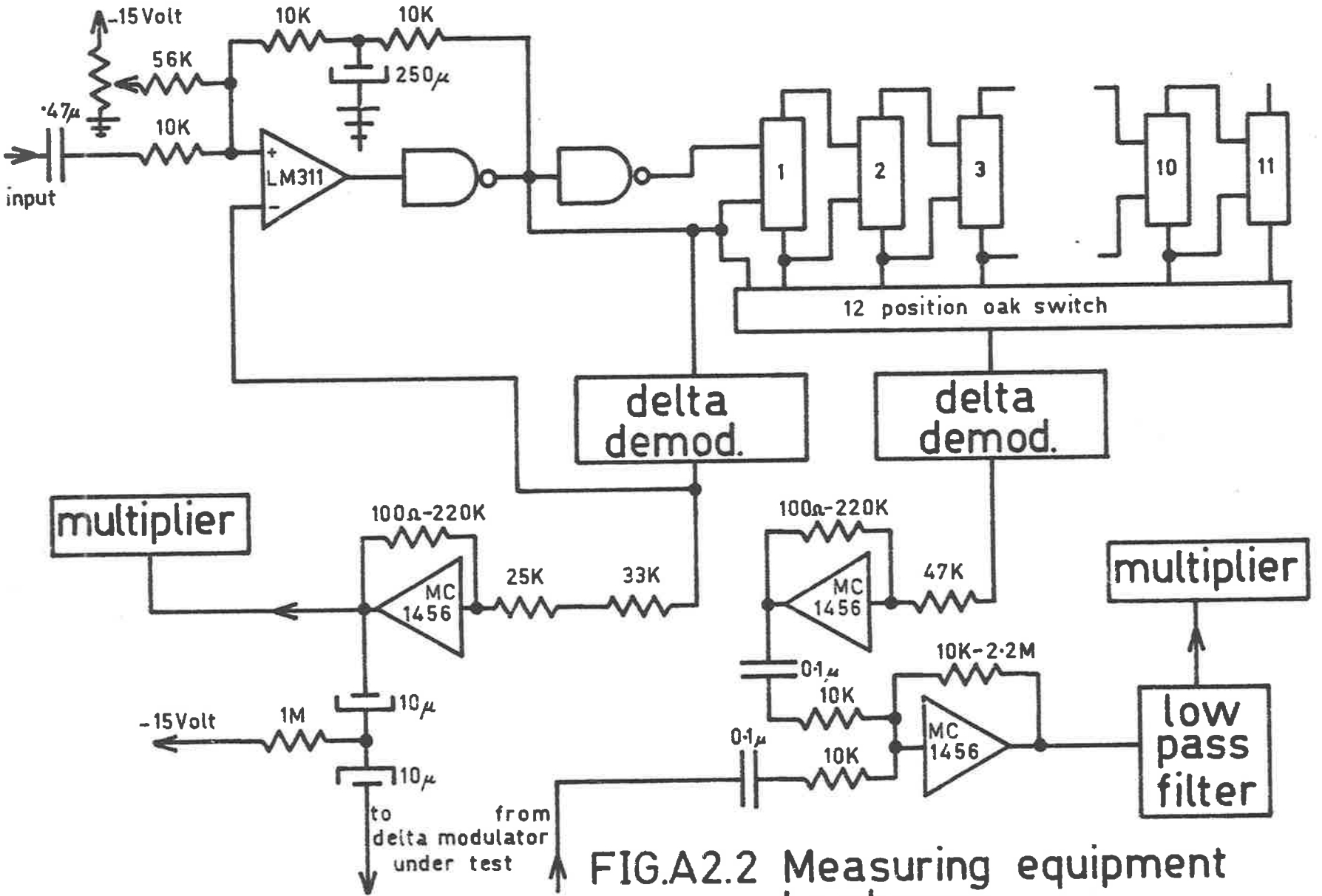
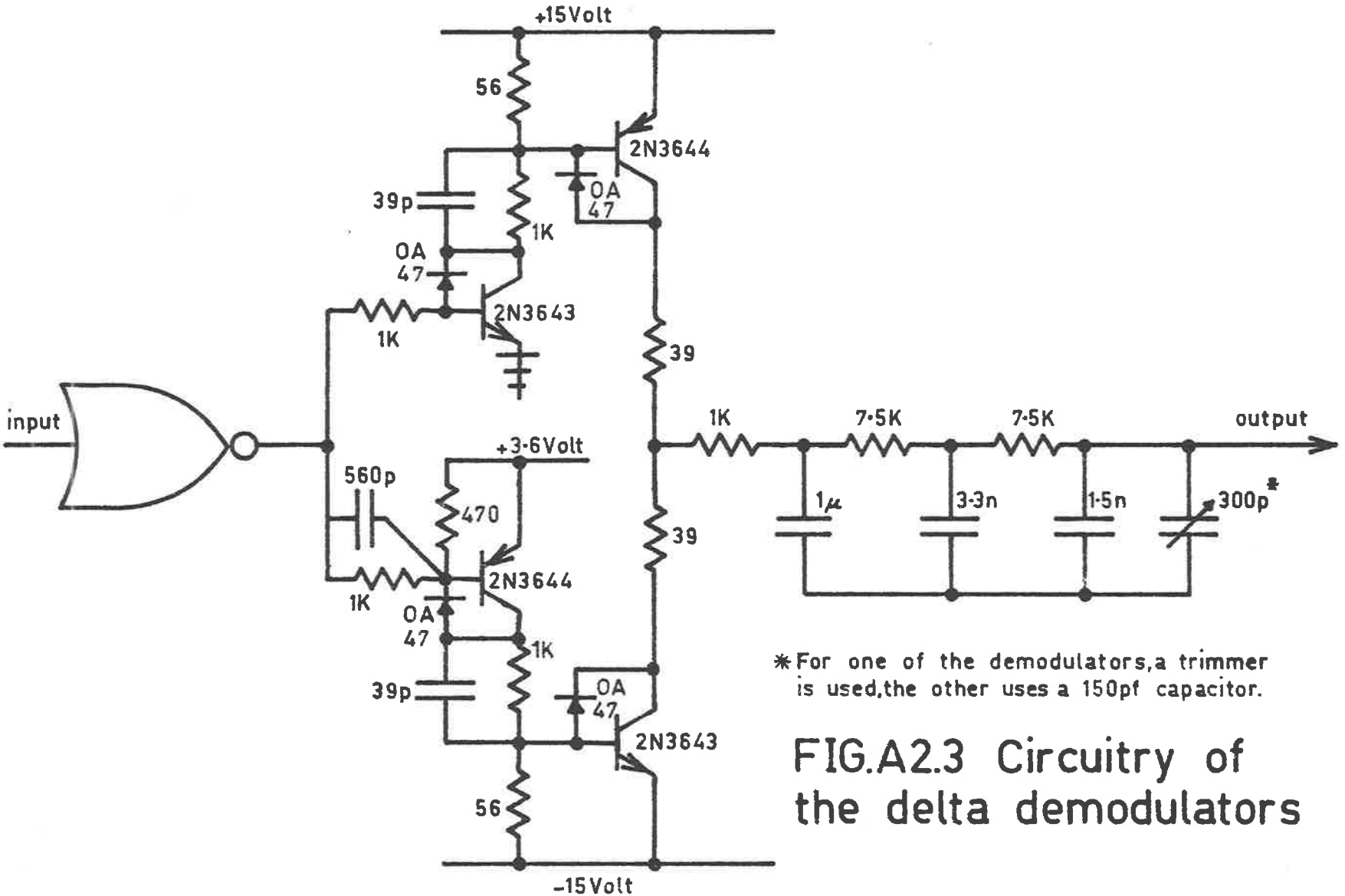


FIG.A2.2 Measuring equipment hardware



*For one of the demodulators, a trimmer is used, the other uses a 150pf capacitor.

FIG.A2.3 Circuitry of the delta demodulators

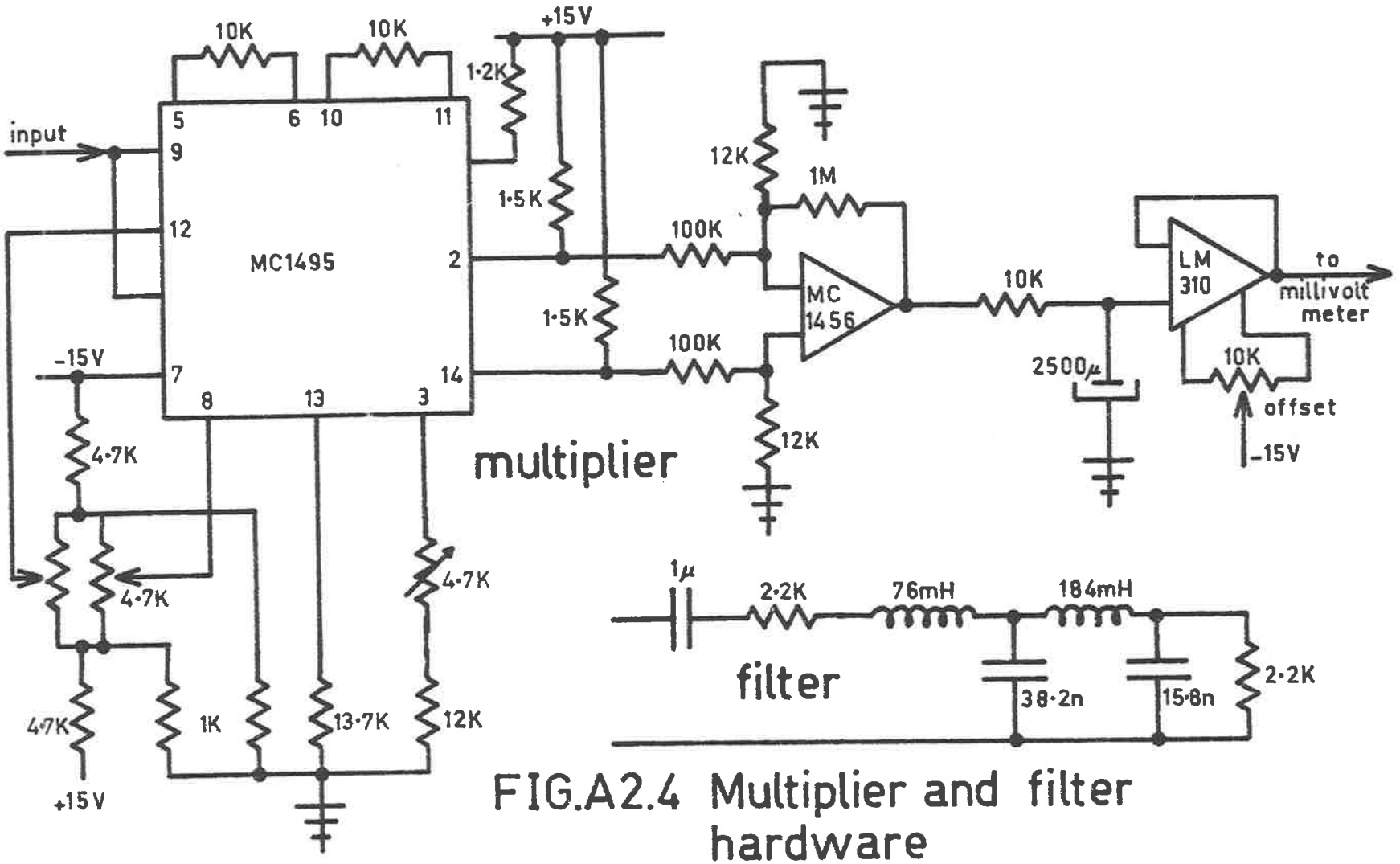


FIG.A2.4 Multiplier and filter hardware

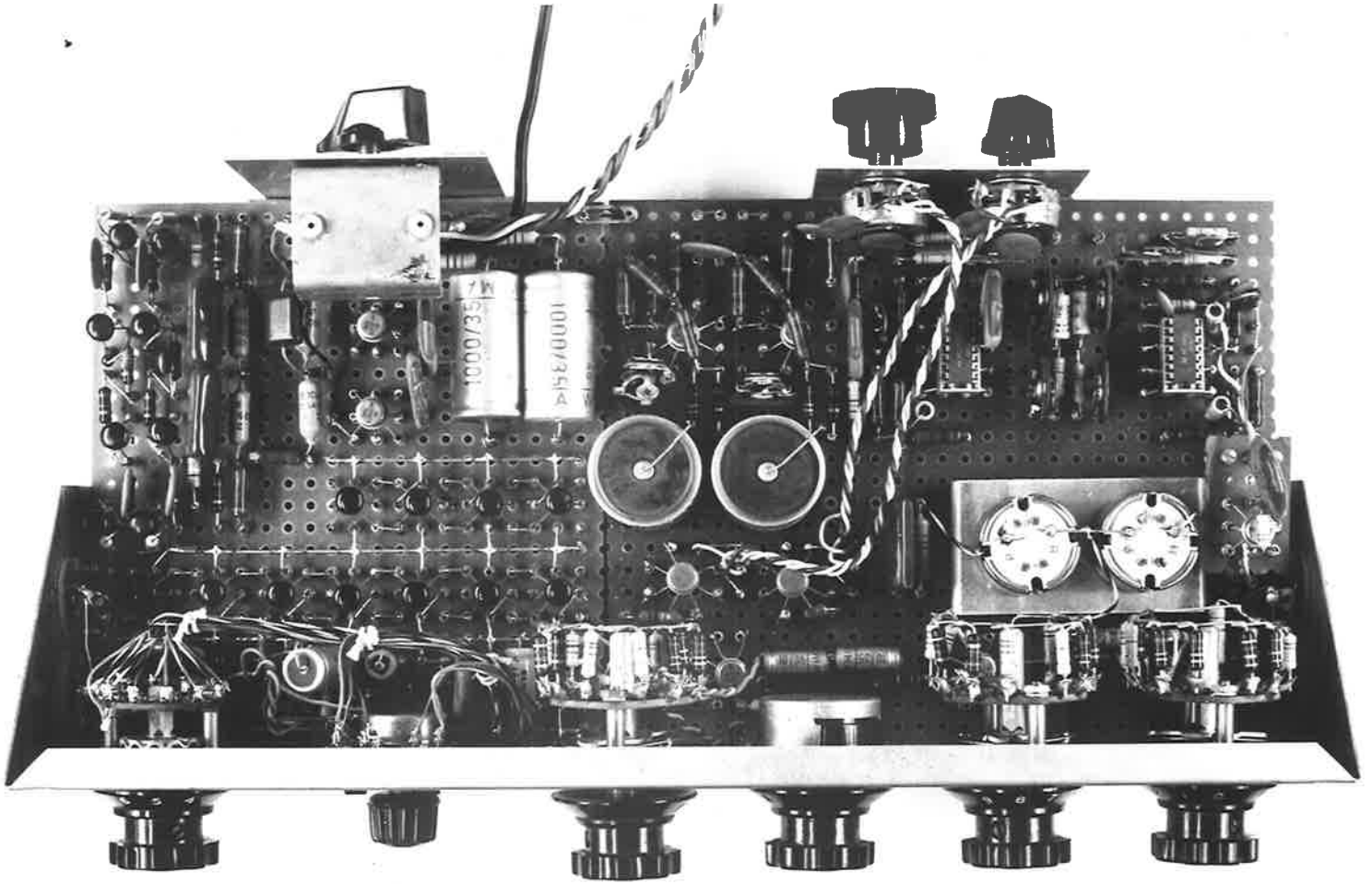


FIG.A2.5 Test equipment

A2.3.1. Hardware of the modulator

The block diagram of the hardware is shown in fig 1.4, the demodulator circuitry in fig 3.4 (c) and the block diagram of the digital circuitry is presented in fig 3.13.

The analogue circuitry consists of the demodulator, adder and comparator of fig 1.4. The circuit diagram of the analogue circuitry is presented in fig A2.6.

The circuit determining the number of clockpulses and controlling the timing is shown in fig A2.7.

The forward and reverse counter consists of a 4 bit counter, one bit of which is shown in fig A2.8. The AC coupling of the gates enables a change to be made from forward to reverse counting without upsetting the counter. 10 decoders are connected to the forward and reverse counter, each representing a step size. The output of this decoder controls the transistor switches as shown in fig A2.9. Since 4 bit forward and reverse counters and BCD decoders were not available in one package at the time the hardware was built, the counter and decoder were constructed from individual gates and flipflops. RTL circuitry was used for the digital section of the hardware.

A2.3.2 Demodulator hardware

The demodulator hardware is identical to the hardware for the modulator, with the following exceptions:

a) the summer and comparator can be deleted from the

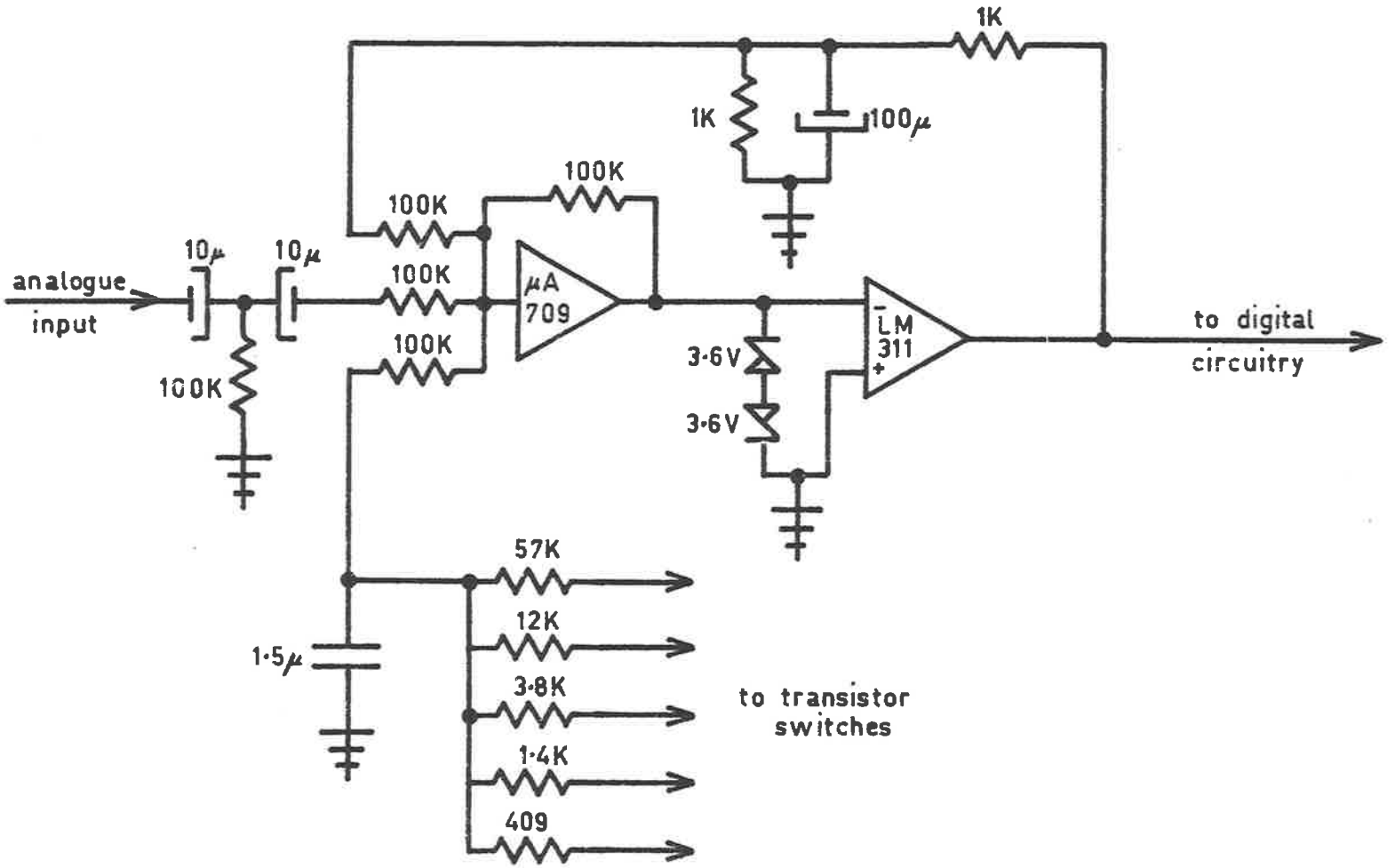


FIG.A2.6 The analogue circuitry of NDDM.

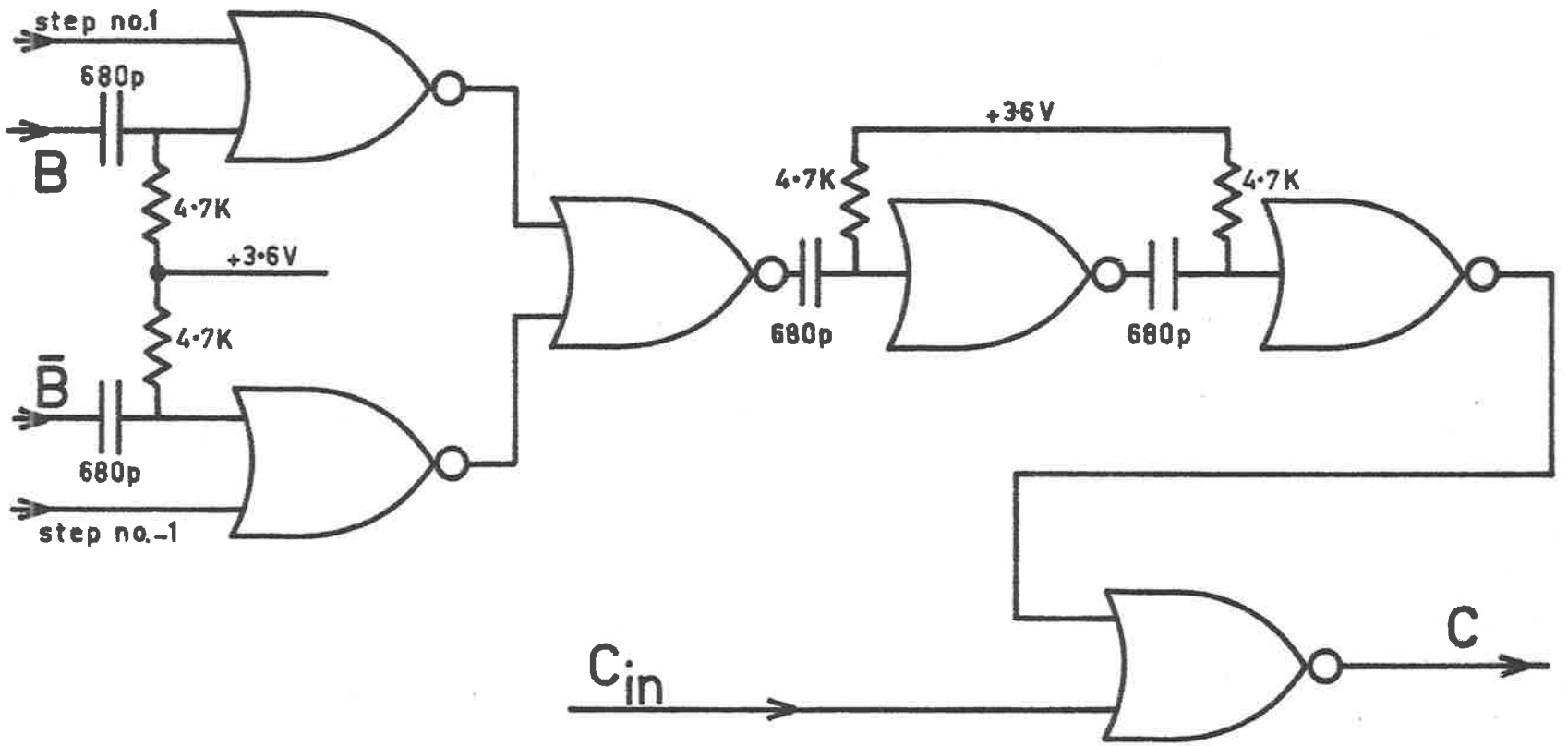


FIG.A2.7 The circuitry generating the clockpulses for NDDM.

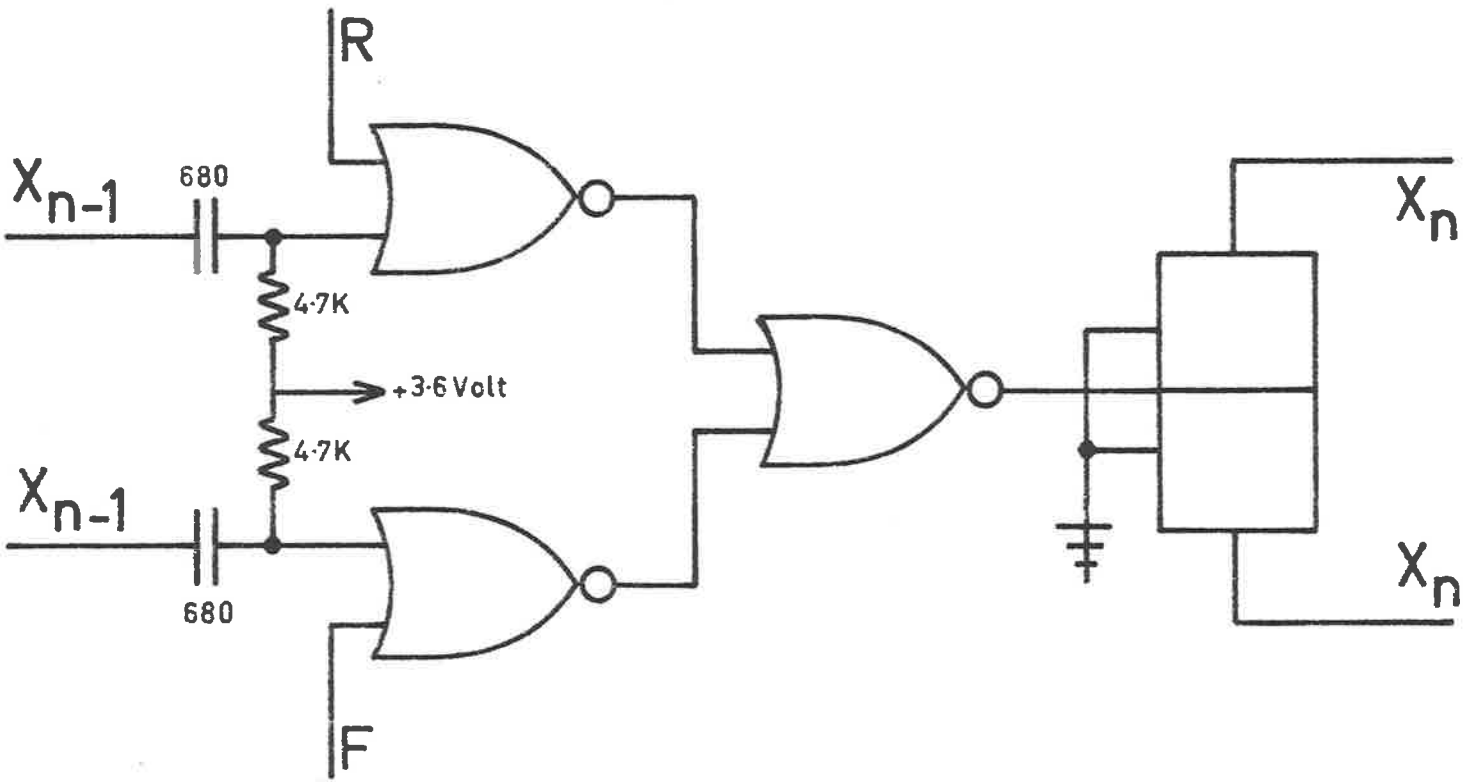


FIG.A2.8 Logic diagram of a bit of the forward and reverse counter

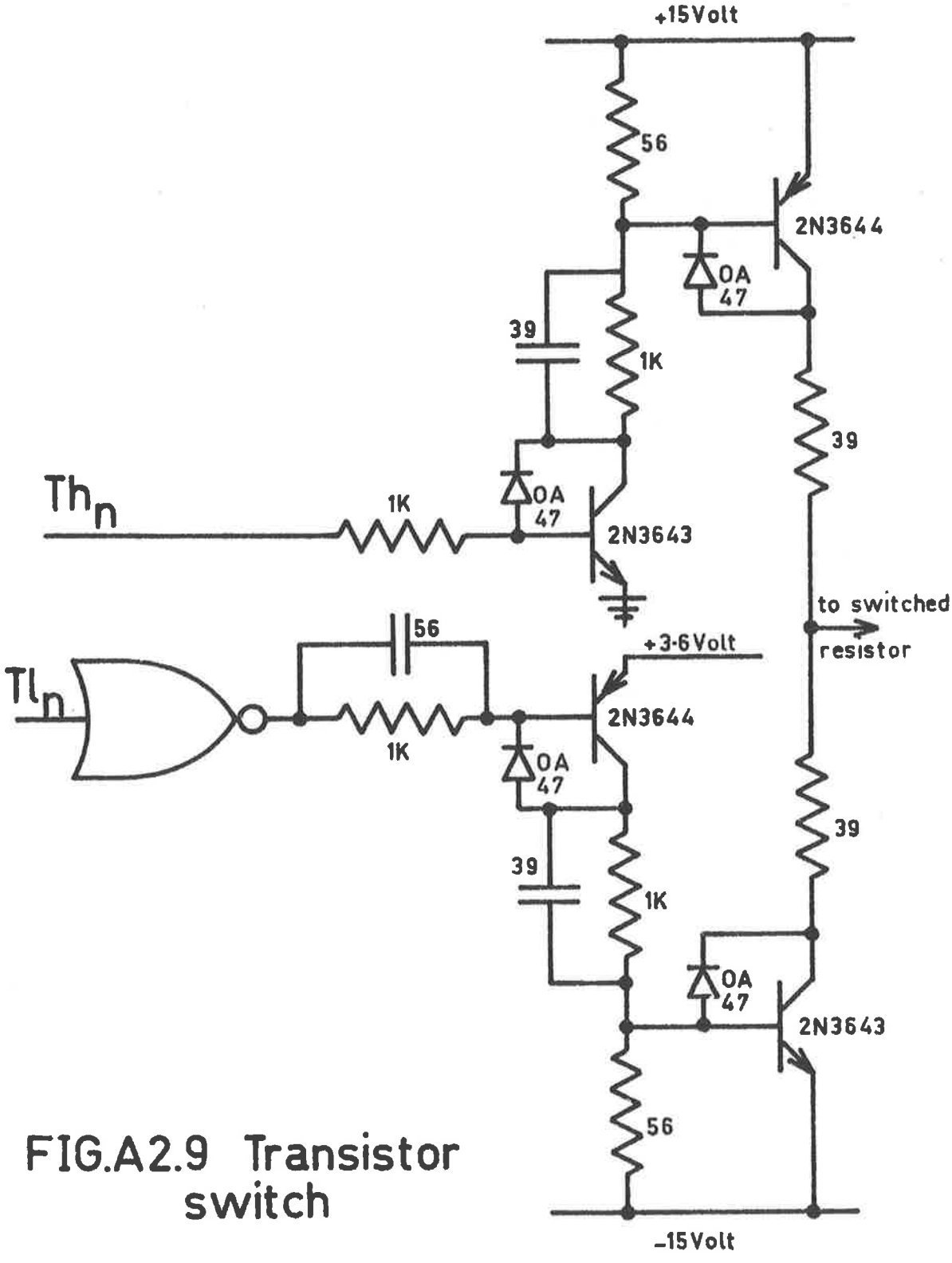


FIG.A2.9 Transistor switch

analogue circuitry

b) the flipflop shown in fig 1.4 can be deleted from the digital circuitry.

A2.4 Digital syllabic companded delta modulation hardware

A brief description of the hardware requirements are given in section 4.5.3, the block diagram of the hardware is presented in fig 4.14 and some of the details of this block diagram are presented in the figs 4.15 and 4.16.

The details of the circuitry are discussed below.

A2.4.1 Circuitry of the modulator

a) Analogue circuitry

The RC integrator, summer and comparator shown in fig 4.14 are the analogue elements of the modulator and their complete circuitry is shown in fig A2.10. The circuitry is self explanatory but a few details are worth mentioning. Operational amplifier 1 together with the external transistors forms a power operational amplifier. The network formed by the operational amplifiers 2 and 3, gives negative feedback to the DC conditions of the comparator, ensuring a 101010 idling pattern when no input signal is applied.

The logic gates are used to give the comparator a higher gain.

b) Digital circuitry

RTL integrated circuits are used for the hardware

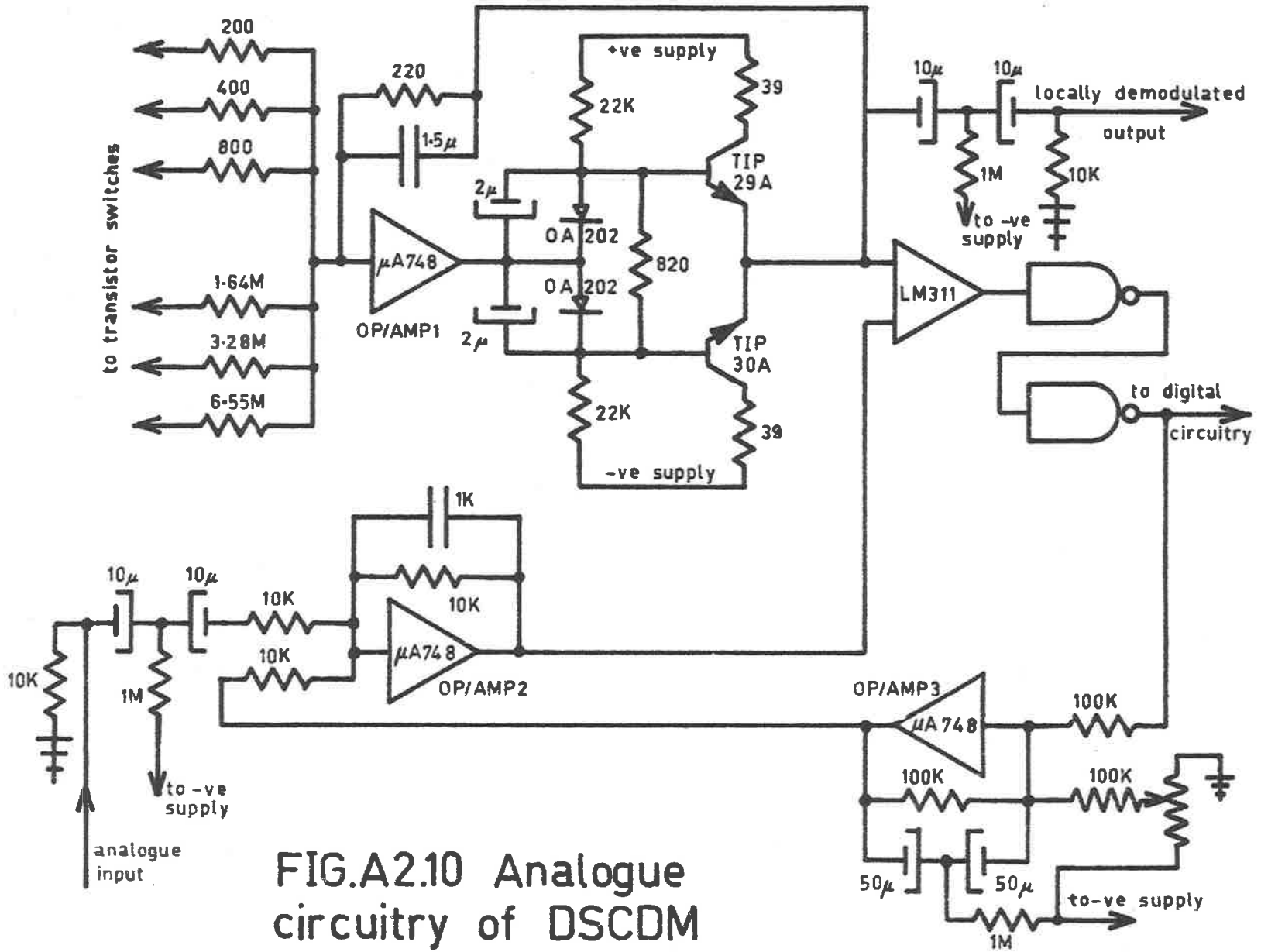


FIG.A2.10 Analogue circuitry of DSCDM

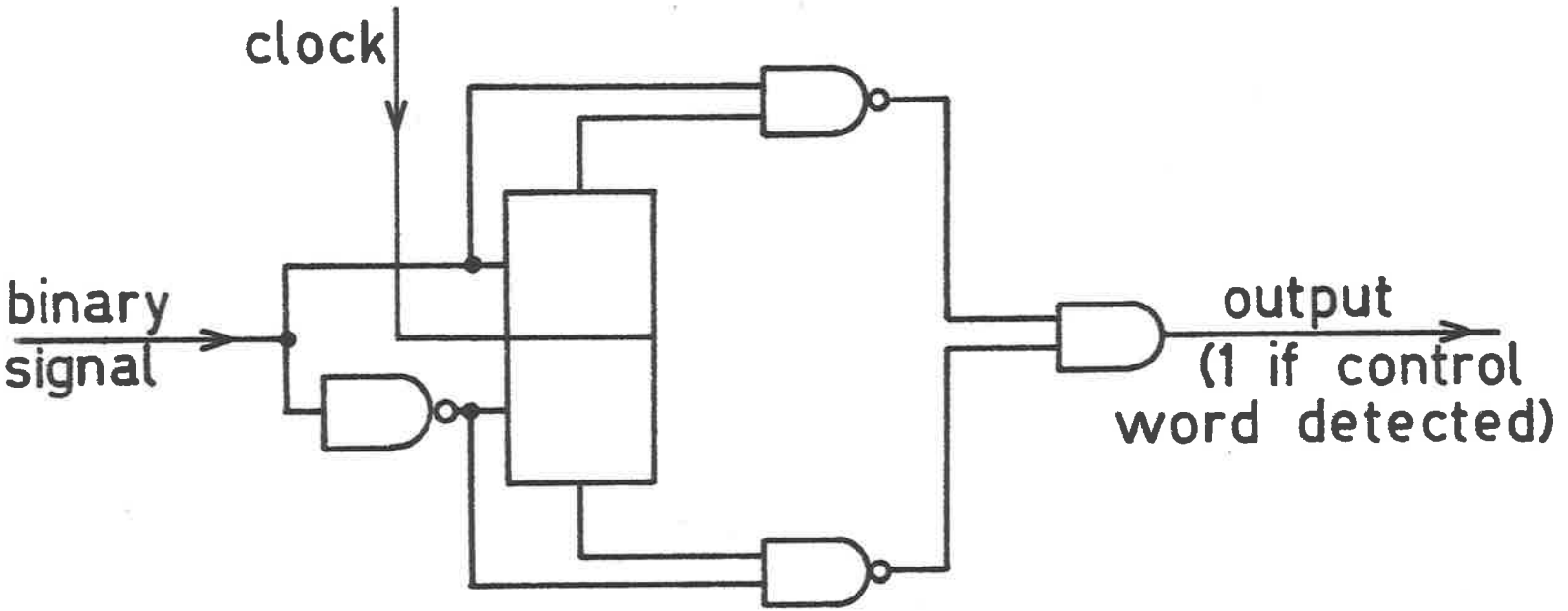
realisation.

The digital circuitry consists of the flipflop and the digital switch control shown in fig 4.14. The details of the digital switch control are shown in fig 4.15. The circuitry detecting the control words and thus determining whether the step size should be increased is shown in fig A2.11. The output of this network is connected to the up/down counting control line shown in fig 4.16, which shows the circuitry for calculating and storing the step size. The details of the second stage of the step size store are shown in fig A2.12. The other stages are similar.

The circuitry for the detection of the most significant bit is shown in fig A2.13, which consists of two parts namely a delay store and logic gates for detecting the most significant bit of the delay store. The delay store is required so that any changes in the control switches of the step size store occur when the counting of the step size store is inhibited, to prevent false counting.

The circuitry preventing forward counting when the 16th bit is the most significant bit and preventing reverse counting when the 5th bit is the most significant bit is shown in fig A2.14.

The circuitry controlling the transistor switches and the transistor switches are shown in fig A2.15 and A2.9 respectively. There are 16 of these stages, each controlling one resistor.



Circuit to determine whether the gain should be increased or decreased

FIG.A2.11

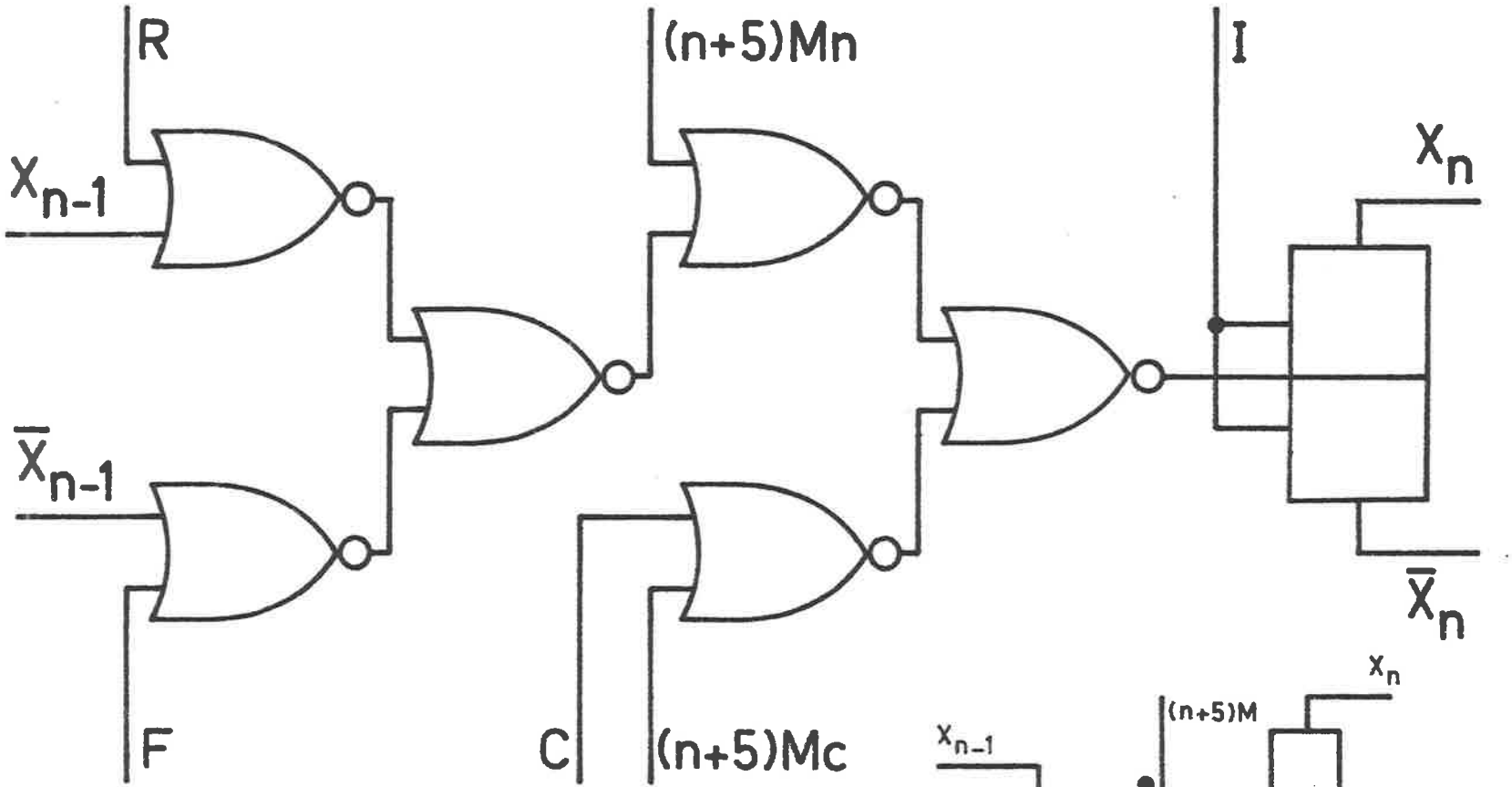
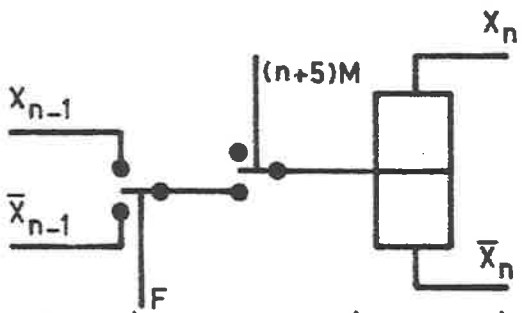


FIG.A2.12 Logic diagram of the 2nd(n=2)stage of the forward and reverse counter



schematic representation used in fig4.16

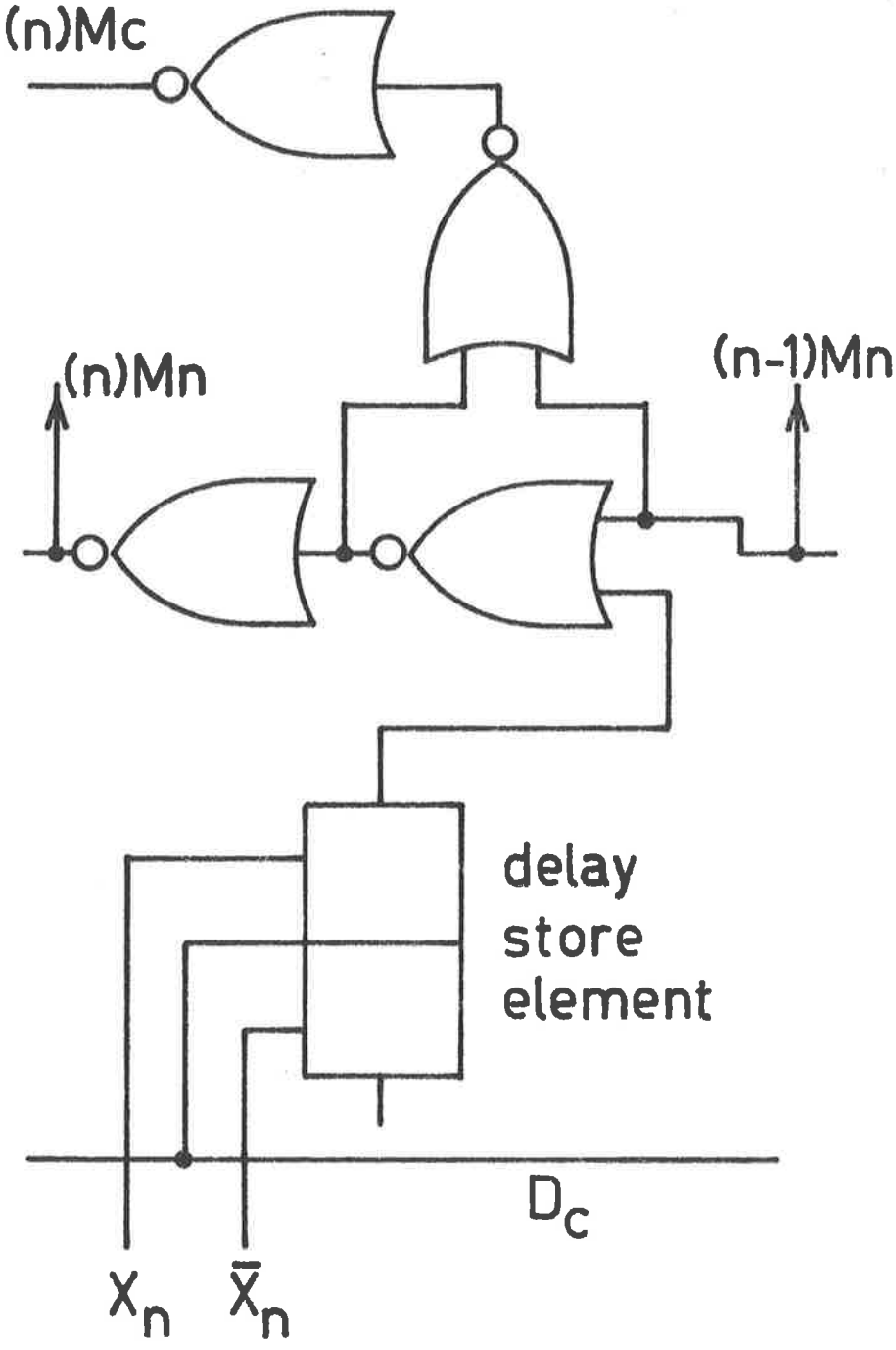


FIG.A2.13 One of the 11 stages of the circuitry detecting the most significant bit

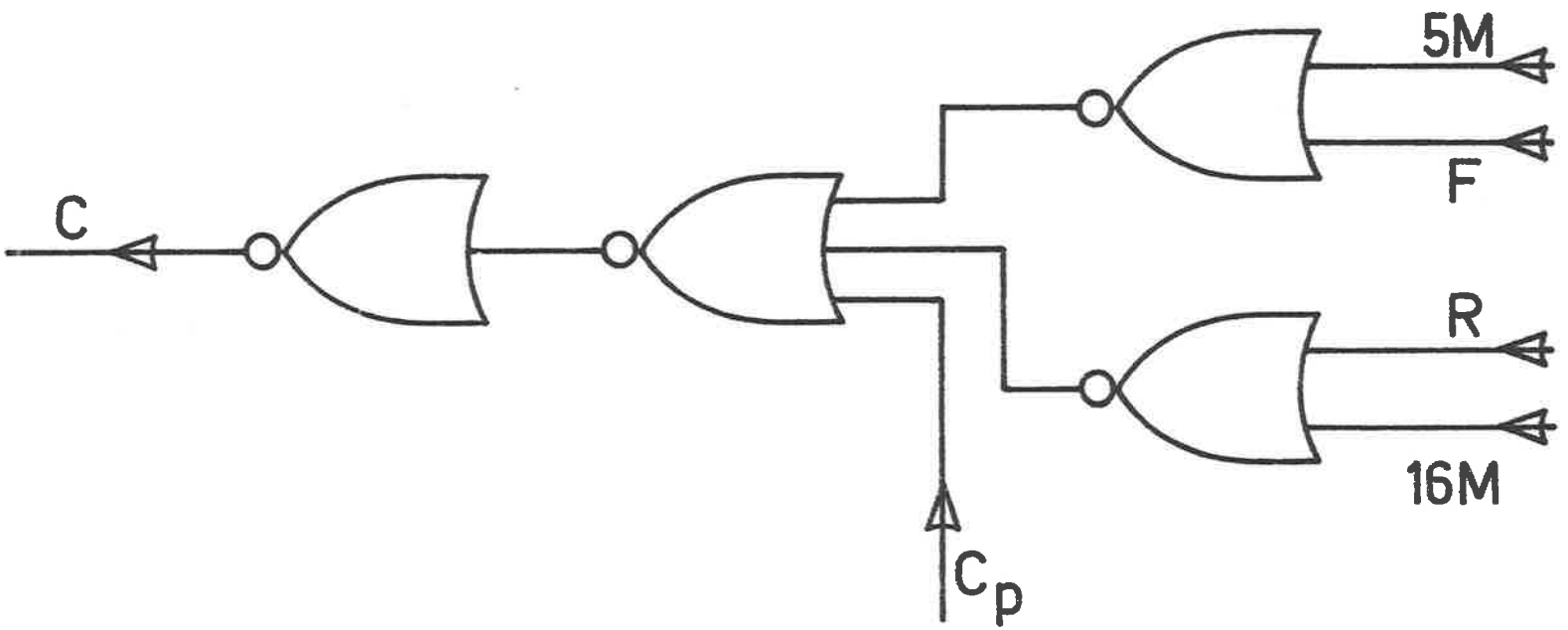


FIG.A2.14 Logic diagram of the upper and lower stops of the step size store

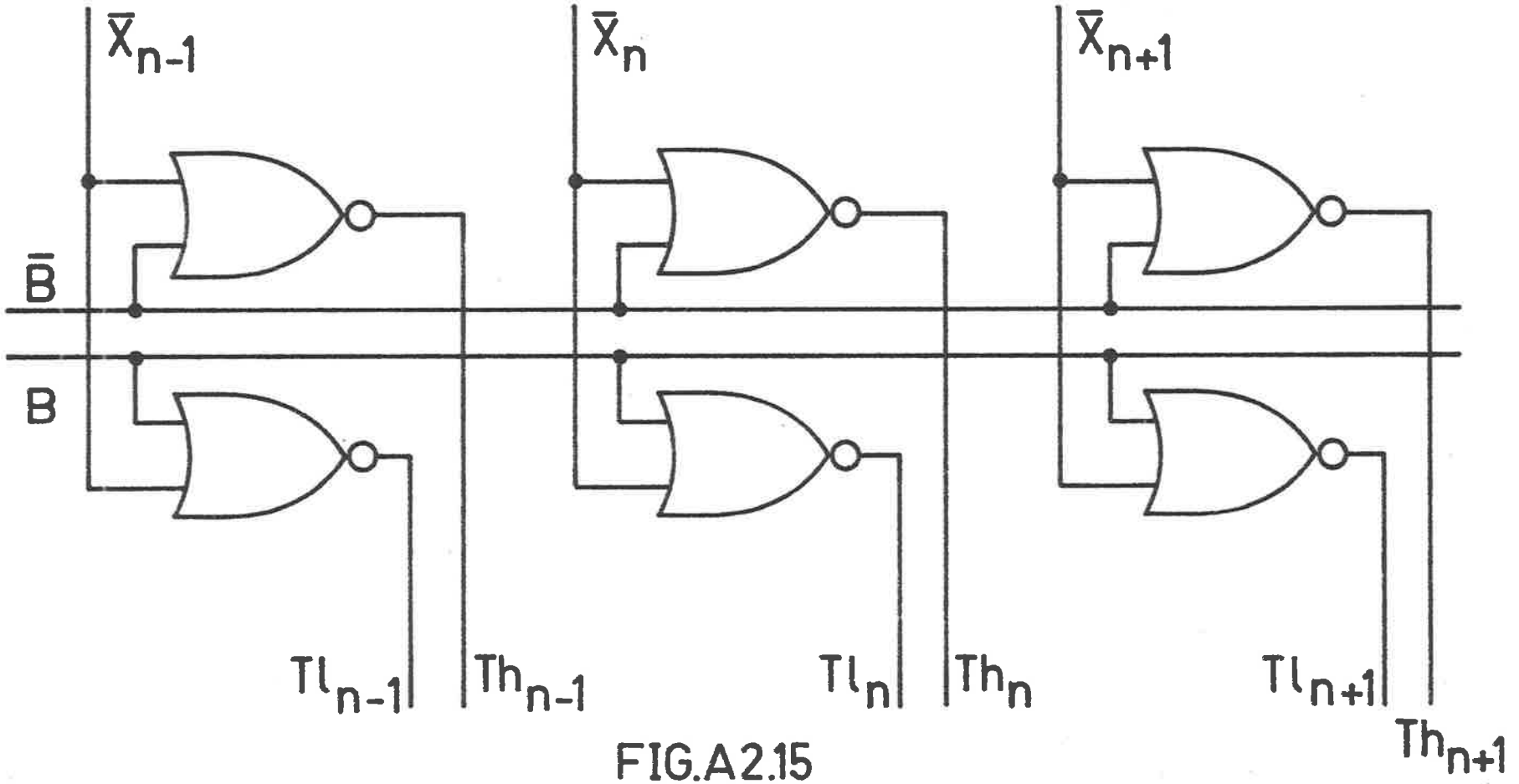


FIG.A2.15

The logic diagram for the circuitry controlling the transistor switches

Timing circuitry must be included to ensure that:

1) one or two clockpulses are generated as explained in section 4

2) counting of the step size store is inhibited when changes of the control switches of the step size store occur.

The timing circuitry is shown in fig A2.16 and the waveforms obtained are shown in fig A2.17 (a).

A2.4.2 Circuitry of the demodulator

a) Analogue circuitry

The analogue circuitry consists of the power integrator shown in fig A2.10.

b) Digital circuitry

The digital circuitry embodies the digital switch control shown in fig 4.14. This can be made the same as the corresponding circuitry of the modulator but for the hardware constructed, the following differences exist.

The inputs to the circuitry controlling the transistor switches are taken from the delay store instead of the step size store. The advantage is that when forward counting takes place, the transistor switches are changed once per sampling period instead of twice, thereby reducing the dissipation in the transistors. Furthermore the loading on the flipflops in the step size store is reduced. Finally the circuitry can be easily converted to the alternate method of stabilisation discussed in section 4.4.3. The delay store

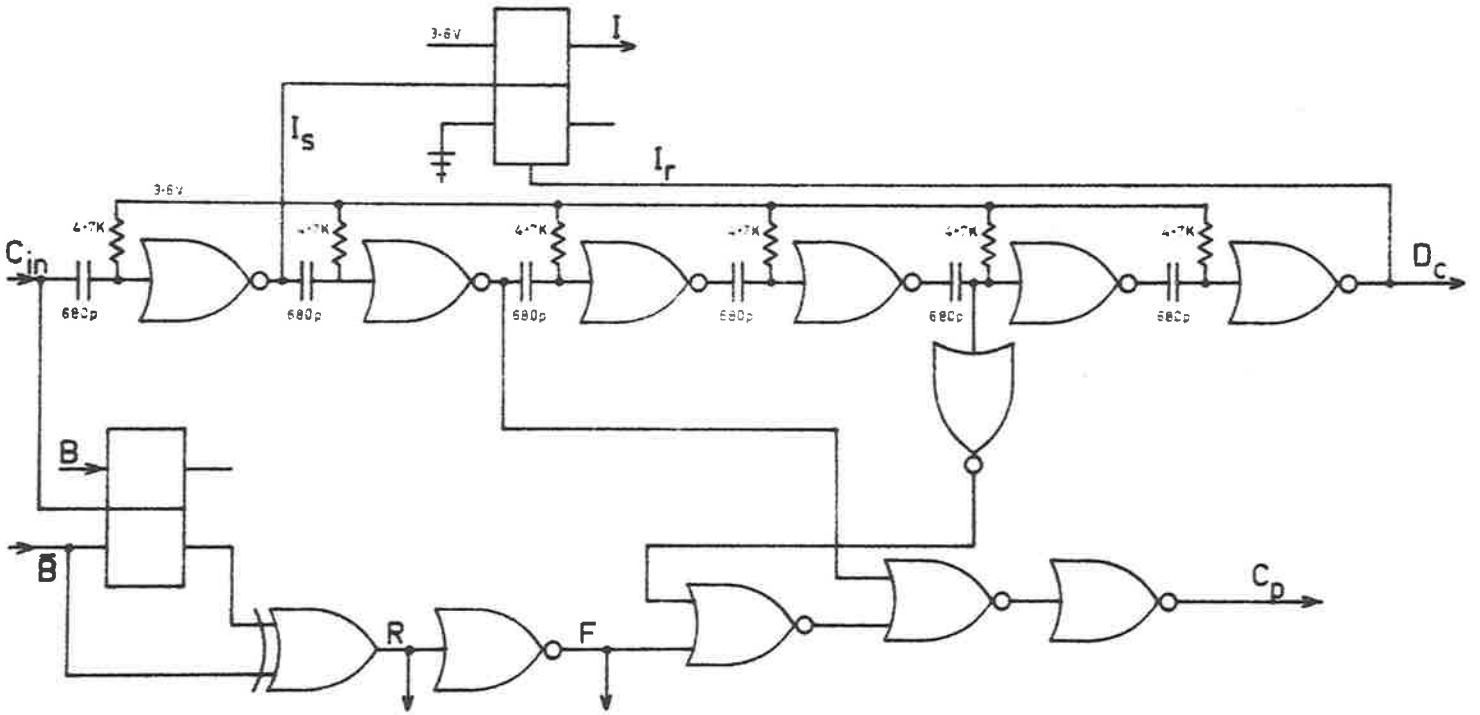


FIG.A2.16 Block diagram of the timing circuitry for DSCDM

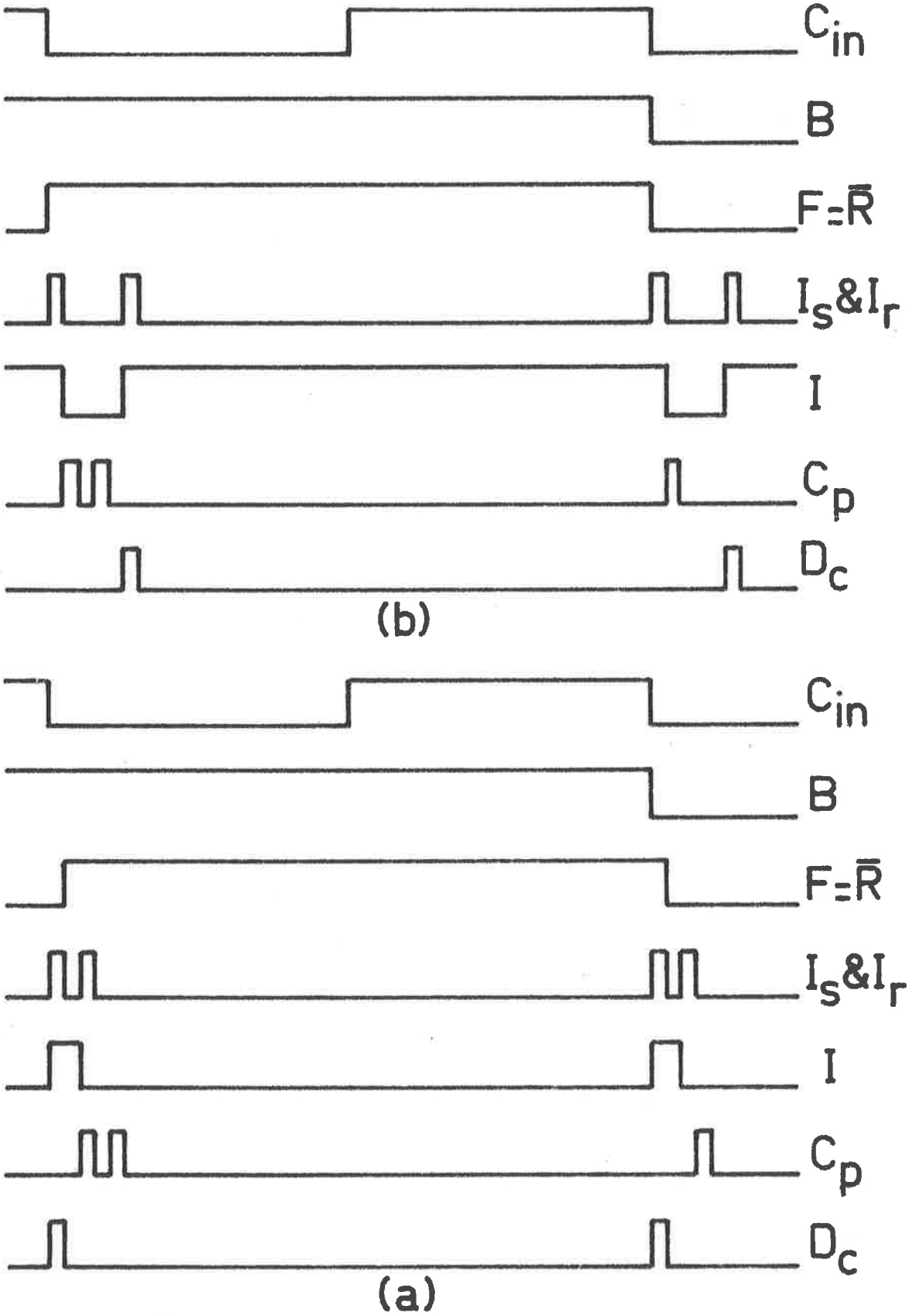


FIG.A2.17 Timing circuitry waveforms

must now have 16 bits instead of 12 bits.

The timing circuitry must be modified in order for the delay of the delay store to be as small as possible. The timing circuitry is thus different for the modulator and demodulator. Since the differences are trivial, no separate circuitry will be shown but the time waveforms are shown in fig A2.17 (b).

APPENDIX 3
COMPUTER PROGRAMS

ALL THE PROGRAMS PRESENTED HERE ARE WRITTEN BY THE AUTHOR EXCEPT THE SUBROUTINE NOISE WHICH WAS WRITTEN BY DR. B.R.DAVIS

A3.1 MAIN PROGRAM

```
      PROGRAM RANDEL(INPUT,OUTPUT)
      DIMENSION B(6),BN(14),CON(6)
      DIMENSION C(10,7)
      DIMENSION IT(19),T(19)
      INTEGER BIT
C  INITIALISE CONSTANTS
      PI=3.141592653589793
      FS=40000.
      FC=3500.
      FCC=20
C  PRINT HEADINGS
      PRINT 20
20    FORMAT (1H1,* DELTA MODULATION SIMULATION *)
      PRINT 21,FS
21    FORMAT (*  SAMPLING FREQUENCY=*,F12.1)
      PRINT 22
22    FORMAT (*      INPUT IN DB    OUTPUT IN DB    UNFILT *
     C,*SNR      FILT SNR *)
C  DESIGN DIGITAL FILTERS
      CALL LPDES(FCC,FS,CON)
      CALL LPDES(FC,FS,B)
      CALL SPDES(FS,BN)
C  READ INPUT SIGNAL AMPLITUDE,V
23    READ 24,V
24    FORMAT (F8.2)
      IF(V) 60,60,25
25    V=V*FS/30
      V=V*FS/100000.
      V=V/1500
      IV=V
C  INITIALISE NOISE GENERATOR
      I=NOISET(I)
C  START OF MAIN LOOP
      DO 29 K=1,3000
      ID=K-200
C  GENERATE A SPEECH SAMPLE
26    IY=NOISE(I)
      Y=V*IY
```

```
2       CALL SPK1(Y,K,BN)
        CALL LPF1(Y,K,B)
        X=Y
C   CALCULATE THE DELTA MODULATOR OUTPUT SAMPLE
        CALL DELTA (X,FB,K,IC)
        CALL WORD(IC,IT,K,ID)
        ER=X-FB
C   INCREMENT THE SIGNAL AND NOISE POWERS
        CALL POWER3(X,PIN,ID)
        CALL LPF3(FB,K,B)
        CALL POWER4(FB,POUT,ID)
        CALL POWER1(ER,UMSN,ID)
        CALL LPF4(ER,K,B)
29      CALL POWER2(ER,FMSN,ID)
C   END OF MAIN LOOP
C   CALCULATE THE AVERAGE SIGNAL AND NOISE POWERS
        IF (PIN.LE.0) GO TO 27
        IF (POUT.LE.0) GO TO 27
        V=ALOG10(PIN/ID)
        POUT=ALOG10(POUT/ID)
        USNR=ALOG10(PIN/UMSN)
        FSNR=ALOG10(PIN/FMSN)
        V=10*V
        POUT=10*POUT
        USNR=10*USNR
        FSNR=10*FSNR
C   PRINT THE RESULTS
        PRINT 30,V,POUT,USNR,FSNR
30      FORMAT (4(5X,F10.3))
C   PRINT THE RELATIVE OCCURRENCE OF THE CONTROL WORDS
        DO 31 N=1,19
        T(N)=IT(N)
31      T(N)=T(N)/ID
        PRINT 32,(T(I),I=1,18)
32      FORMAT (19(X,F6.4))
        GO TO 23
27      PRINT 28
28      FORMAT (*  ZERO POWER *)
        GO TO 23
60      STOP
        END
```

```
C  THE DATA FOR THE MAIN PROGRAM ARE AS FOLLOWS
C  1) DATA FOR THE DIGITAL FILTER SUBROUTINES,IF REQUIRED
C     AN EXAMPLE OF SUCH DATA IS GIVEN IN SECTION A3.3.5
C  2) DATA FOR THE INPUT SIGNAL AMPLITUDE.

C  THE PROGRAM IS TERMINATED BY READING A NEGATIVE OR
C  ZERO INPUT SIGNAL AMPLITUDE,V

C  TYPICAL DATA FOR V ARE AS FOLLOWS
2.0
4.0
8.0
16.0
32.0
64.0
128.0
256.0
512.0
1024.0
2048.0
4096.0
8192.0
16384.
32768.
65536.
131072.
262144.
-100
```

A3.2 DELTA AND PULSE CODE MODULATION SUBROUTINES

A3.2.1 SIDM

```
      SUBROUTINE DELTA (Y,FBEX,K,IC)
C  INITIALISE THE DELTA MODULATOR
      IF (K.GT.1) GO TO 2
      FBM=0
C  CALCULATE THE BINARY TRANSMITTED SIGNAL
2     ER=Y-FBM
      IC=-1
      IF (ER.GT.0) IC=1
C  CALCULATE THE DEMODULATED OUTPUT
      FBEX=FBM=0.937*FBM+IC
      RETURN
      END
```

A3.2.2 DSCDM

```
      SUBROUTINE DELTA (Y,FBEX,K,IC)
      DIMENSION IS(15)
C  INITIALISE THE DELTA MODULATOR
      IF (K.GT.1) GO TO 2
      FB=FBM=0
      IA=100
      DO 3 N=1,15
3     IS(N)=2**N
C  CALCULATE THE BINARY TRANSMITTED SIGNAL
2     ER=Y-FBM
      IC=-1
      IF (ER.GT.0) IC=1
C  DETERMINE THE CHANGE OF STEP SIZE AS M*IG
      M=1
      DO 4 N=6,14
4     IF (IA.GE.IS(N) ) M=IS(N-5)
      IG=2
      IF (IC+ICD.EQ.0) IG=-1
C  INCREMENT THE STEP SIZE STORE AND CHECK FOR OVERFLOW
      IA=IA+M*IG
      IF (IA.LT.31) IA=IA-M*IG
      IF (IA.GT.IS(15)) IA=IA-M*IG
C  CALCULATE THE DEMODULATED OUTPUT
      FBEX=FBM=0.937*FBM+IA*IC
      ICD=IC
      RETURN
      END
```

A3.2.3 NDDM

```
      SUBROUTINE MOD(Y,IC,K,PRED,A)
      DIMENSION A(20)
      IF (K-1) 81,81,82
C  INITIALISE THE DELTA MODULATOR
81    FB=FBM=0
      I=10
C  CALCULATE THE BINARY TRANSMITTED SIGNAL
82    ER=Y-FBM
      IC=-1
      IF(ER.GT.0) IC=1
C  DETERMINE THE CHANGE OF STEP NUMBER
      IF (IC-IC1) 83,84,85
83    IF (I.LT.12) GO TO 84
      GO TO 86
85    IF (I.GT.9) GO TO 84
86    I=I+IC
84    I=I+IC
      IF (A(I).EQ.0) I=I-IC
C  CALCULATE THE DEMODULATED OUTPUT
      FB=0.97*FB+A(I)*(1-FB/1667.)
      FBM=FB+A(I)*PRED
      IC1=IC
      RETURN
      END
```

TYPICAL DATA FOR THE ARRAY A(I)

```
0.
0.
0.
0.
0
-65.
-22.0
-7.5
-2.5
-0.50
0.50
2.5
7.5
22.0
65.
0
0.
0.
0.
0.
```

A3.2.4 DIGITALLY SYLLABIC COMPANDED PCM

```
      SUBROUTINE PCM(Y,FB,K,BIT,IG)
      INTEGER BIT
      DIMENSION IST(20)
C  INITIALISATION OF PARAMETERS (UP TO STATEMENT NO 2)
      IF (K.GT.1) GO TO 2
      LIM=2**(BIT-3)
      IL=4
      IL1=IL+1
      IU=10+IL
      DO 4 IM=1,IU
4     IST(IM)=2**IM
      IYM=0
      IS=0
      IA=128
      UL=2**(BIT-1)-1
      LL=-UL-1
2     FB=0
C  DETERMINE THE SAMPLING INTERVAL. THE SUBROUTINE IS
C  CALLED FOR EVERY TRANSMISSION BIT BUT CALCULATIONS
C  ONLY TAKE PLACE AT THE SAMPLING INSTANT.
      IF (IS.LE.BIT-2) GO TO 3
C  DETERMINE THE CHANGE OF STEP SIZE AS M*IG
      M=1
      DO 5 IM=IL1,IU
      IF (IA.GE.IST(IM)) M=IST(IM-IL)
5     CONTINUE
      IG=-2
      IF (IYM.GE.LIM) IG=5
C  INCREMENT THE STEP SIZE STORE AND CHECK FOR OVERFLOW
      IA=IA+M*IG
      IF (IA.GT.IST(IU)) IA=IST(IU)
      IF (IA.LE.IST(IL)) IA=IST(IL)
C  RESET THE SAMPLING INTERVAL COUNTER
      IS=-1
C  NORMALISE THE INPUT
      A=IA
      YN=Y/A
C  DETERMINE THE INPUT ROUNDED TO THE NEAREST INTEGER
      YP=YN+0.5
      IF (YP.LT.0) YP=YP-1.0
      IYN=YP
C  CHECK THE UPPER AND LOWER LIMITS
      IF (IYN.GT.UL) IYN=UL
      IF (IYN.LT.LL) IYN=LL
      IYM=IABS(IYN)
C  DENORMALISE THE DEMODULATED OUTPUT
      IFB=IYN*IA*BIT
```

```
      FB=IFB
3     IS=IS+1
      RETURN
      END
```

A3.3 DIGITAL FILTERING SUBROUTINES

A3.3.1 FILTER TESTING PROGRAM

```
      PROGRAM SRTEST(INPUT,OUTPUT)
C  DIGITAL FILTER DESIGN TEST PROGRAM.
C  THIS PROGRAM CALCULATES THE FREQUENCY VERSUS GAIN AND
C  PHASE RESPONSE OF A DIGITAL FILTER.
C  SPECIFY THE SAMPLING FREQUENCY,FS,IN HERTZ AND THE CUT
C  OFF FREQUENCY,ALSO IN HERTZ.
C  THE RESPONSE IS CALCULATED AT THE FREQUENCIES,FA,WHICH
C  ARE READ IN AS DATA.THE PROGRAM WILL STOP IF A NEGATIVE
C  FREQUENCY IS READ.THIS CAN BE USED TO TERMINATE THE
C  PROGRAM.
      DIMENSION DEL(4),B(10,7)
      PRINT 14
14    FORMAT (1H1,*   DIGITAL FILTER FREQUENCY RESPONSE*
     C,* PROGRAM *)
C  SET SAMPLING AND CUT OFF FREQUENCY
      PI=3.141592653589793
      FS=40000.
      FC=3500.
C  DESIGN FILTER
      CALL FILDES(FS,FC,B,IMAX)
      PRINT 15
15    FORMAT (*  FREQUENCY        GAIN IN DB        PHASE(1)
     C     PHASE(2)        PHASE(3)       NO OF CYCLES
     C  NO OF SAMPLES  *)
1     READ 2,FA
2     FORMAT (F16.8)
      IF (FA) 60,60,3
C  CALCULATE NORMALIZED FREQUENCY
3     W=FS/(2*PI*FA)
      ID=RUN=-1
      DO 11 K=1,20000
C  GENERATE SINEWAVE
      RK=K
      Z=RK/W
      Y=X1=X2=COS(Z)
C  COMPUTE FILTER OUTPUT SAMPLE DUE TO SINEWAVE INPUT SAMPLE
      CALL FILTER(X1,K,B,IMAX)
C  CALCULATE DELAY
      CALL GRDEL(Y,X1,DEL,K,ID)
      IF(RUN) 4,5,5
C  TEST FOR THE RIGHT STARTING CONDITIONS
4     IF (K.LT.800.OR.Y.LT.0.997) GO TO 10
      RUN=1
      G=K-1
5     ID=K-G
```

```
C  TEST FOR THE RIGHT TERMINATING CONDITIONS
      IF (ID.GT.1000.AND.Y.GT.0.997) K=20000
C  CALCULATE POWER
10    CALL POWER1(X1,PLF,ID)
11    CONTINUE
C  CALCULATE AVERAGE POWER
      PLF=2*PLF
      PLF=ALOG10(PLF/ID)
      PLF=10*PLF
C  CALCULATE AVERAGE PHASE
      DO 20 I=1,3
      DEL(I)=DEL(I)/W
20    DEL(I)=DEL(I)/DEL(4)
      PRINT 16 ,FA,PLF,DEL(1),DEL(2),DEL(3),DEL(4),ID
16    FORMAT (X,6(E11.4,5X),I6)
      GO TO 1
60    STOP
      END
```

A3.3.2 SUBROUTINE TO DESIGN THE SPEECH FILTER

```
      SUBROUTINE SPDES(FS,BN)
C  THIS PROGRAM DESIGNS A DIGITAL FILTER WITH A SPECTRUM
C  SIMILAR TO MALE SPEECH AT SEALEVEL
      DIMENSION BN(14),FC(5),WC(5)
C  INITIALISE THE CONSTANTS
      PI=3.141592653589793
      FC(1)=600
      FC(2)=400
      FC(3)=3000
      FC(4)=10000
      FC(5)=4000
C  CALCULATE THE DIGITAL CUTOFF FREQUENCIES.
      DO 61 I=1,5
      WC(I)=PI*FC(I)/FS
61    WC(I)=TAN(WC(I))
C  CALCULATE THE FILTERCOEFFICIENTS AS THE ARRAY BN
      A0=WC(1)*WC(1)
      A1=WC(1)*1.2
      BN(1)=1+A1+A0
      BN(2)=2*(A0-1)
      BN(3)=1-A1+A0
      BN(4)=A0
      BN(5)=WC(2)+1
      BN(6)=WC(2)-1
      BN(7)=WC(3)+1
      BN(8)=WC(3)-1
      BN(9)=WC(3)/WC(2)
      BN(10)=WC(4)+1
      BN(11)=WC(4)-1
      BN(12)=WC(5)+1
      BN(13)=WC(5)-1
      BN(14)=WC(5)/WC(4)
      RETURN
      END
```

A3.3.3 SPEECH FILTER SUBROUTINE

```
      SUBROUTINE SPK1(X,K,BN)
      DIMENSION BN(14)
C  THIS PROGRAM SIMULATES A FILTER WITH A SPECTRUM
C  SIMILAR TO MALE SPEECH AT SEALEVEL, USING THE FILTER
C  COEFFICIENTS BN.
      U=X
C  INITIALISE THE FILTER
      IF (K.LE.1) U1=U2=V1=V2=W1=X1=0
C  DIGITAL FILTER EQUATIONS
      V=(BN(4)*(U+2*U1+U2)-BN(2)*V1-BN(3)*V2)/BN(1)
      W=(BN(9)*(BN(5)*V+BN(6)*V1)-BN(8)*W1)/BN(7)
      X=(BN(14)*(BN(10)*W+BN(11)*W1)-BN(13)*X1)/BN(12)
C  PROGRESSIVE SHIFT
      U2=U1
      U1=U
      V2=V1
      V1=V
      W1=W
      X1=X
      RETURN
      END
```

A3.3.4 SUBROUTINE TO DESIGN A 4TH ORDER LOW PASS BUTTERWORTH FILTER

```
      SUBROUTINE LPDES(FC,FS,B)
      DIMENSION B(6)
C  INITIALISE THE CONSTANTS
      PI=3.141592653589793
C  CALCULATE THE DIGITAL CUT OFF FREQUENCY
      Z=PI*FC/FS
      WC=TAN(Z)
      X=WC*SIN(PI/8)
      Y=WC*COS(PI/8)
      Z=X+Y
      Z1=WC*WC
C  CALCULATE THE FILTER COEFFICIENTS AS THE ARRAY B
      A=2*Z
      C=A*Z
      D=A*Z1
      E=B(6)=Z1*Z1
      B(5)=-A+C-D+E+1
      B(4)=2*A-2*D+4*E-4
      B(3)=-2*C+6*E+6
      B(2)=-2*A+2*D+4*E-4
      B(1)=A+C+D+E+1
      RETURN
      END
```

A3.3.5 4TH ORDER LOW PASS BUTTERWORTH FILTER SUBROUTINE

```
      SUBROUTINE LPF1(X,K,B)
      DIMENSION B(6)
      Y=X
C  INITIALISE THE FILTER
      IF(K.LE.1) Y1=Y2=Y3=Y4=X1=X2=X3=X4=0
C  DIGITAL FILTER EQUATION
      X=(B(6)*(Y+4*Y1+6*Y2+4*Y3+Y4)-B(2)*X1-B(3)*X2-B(4)*X3
     C-B(5)*X4)/B(1)
C  PROGRESSIVE SHIFT
      Y4=Y3
      Y3=Y2
      Y2=Y1
      Y1=Y
      X4=X3
      X3=X2
      X2=X1
      X1=X
      RETURN
      END
```

A3.3.6 GENERAL FILTER DESIGN SUBROUTINE

```
      SUBROUTINE FILDES (FS,FC,C,IMAX)
C  DIGITAL FILTER DESIGN PROGRAM
C  THIS SUBROUTINE CALCULATES THE FILTER COEFFICIENTS,C,
C  WHICH SPECIFY THE DIGITAL FILTER.
C  THE MAXIMUM ORDER OF THE FILTER IS 20 BUT THIS CAN BE
C  INCREASED BY ALTERING THE DIMENSION  STATEMENT.
C  SPECIFY THE NUMBER OF POLE PAIRS,IP, AND THE NUMBER OF
C  ZERO PAIRS,IZ. THE REAL AND IMAGINARY PARTS OF THE
C  NORMALIZED POLE OR ZERO PAIRS ARE READ IN AS DATA.
C  THE PROGRAM ONLY ALLOWS FOR COMLEX CONJUGATE POLE OR
C  ZERO PAIRS,THE IMAGINARY PART OF WHICH CAN BE ZERO.
      DIMENSION C(10,7),PZ(40),A(20),B(20),R(20)
      REAL N2(20),N1(20),N0(20)
      COMPLEX S,CX,W
      PI=3.141592653589793
C  SET THE NUMBER OF POLE AND ZERO-PAIRS
      IP=3
      IZ=2
      IDIF=IP-IZ
      IORD=IP+IZ
      I2P=2*IP
      I2Z=2*IZ
      IZL=I2P+1
      I2ORD=I2P+I2Z
      IF (IP.EQ.0) GO TO 28
C  READ THE POLE POSITIONS
12    FORMAT (* POLES     REAL PART         IMAG. PART*)
      PRINT 12
      READ 13,(PZ(I),I=1,I2P)
      PRINT 14,(PZ(I),I=1,I2P)
28    CONTINUE
      IF (IZ.EQ.0) GO TO 27
C  READ THE ZERO POSITIONS
      PRINT 15
15    FORMAT (* ZEROS     REAL PART         IMAG. PART*)
      READ 13,(PZ(I),I=IZL,I2ORD)
      PRINT 14,(PZ(I),I=IZL,I2ORD)
27    CONTINUE
13    FORMAT (F16.8)
14    FORMAT (6X,2(E15.5,2X))
C  CALCULATE THE DIGITAL CUT OFF FREQUENCIES
      FN=PI*FC/FS
      FN=TAN(FN)
      DO 10 I=1,I2ORD
10    PZ(I)=PZ(I)*FN
C  ALLOW FOR UNEQUAL NUMBER OF POLES AND ZEROS
      IF (IDIF) 20,22,21
```

```
20      IMAX=IZ
        INDIF=-IDIF
        IPDIF=I2MAX=2*IMAX
        IU=INDIF
        IL=1
        GO TO 23
21      IMAX=IP
        IU=I2MAX=2*IMAX
        IPDIF=I2MAX-IDIF
        INDIF=0
        IL=IPDIF
23      DO 24 I=IL,IU
        N2(I)=1.0
        N1(I)=2.0
        N0(I)=1.0
24      R(I)=1.0
C  FILTER COEFFICIENT CALCULATION
22      DO 25 J=1,IORD
        I=J+INDIF
        L=2*J
        M=L-1
        A(I)=PZ(M)
        B(I)=PZ(L)
        R(I)=A(I)*A(I)+B(I)*B(I)
        N2(I)=1-2*A(I)+R(I)
        N1(I)=2*(R(I)-1)
25      N0(I)=1+2*A(I)+R(I)
        DO 26 J=1,IMAX
        C(J,1)=N2(J)
        C(J,2)=N1(J)
        C(J,3)=N0(J)
        C(J,4)=N2(J+IMAX)
        C(J,5)=N1(J+IMAX)
        C(J,6)=N0(J+IMAX)
26      C(J,7)=R(J)/R(J+IMAX)
        RETURN
        END

C  TYPICAL DATA.THESE DATA ARE FOR A CC065046 FILTER(REF 24)
-0.0415270
0.9934230
-0.1417271
0.7836824
-0.2416728
0.3109199
0.0
1.922972
0.0
1.462178
```

A3.3.9 GENERAL FILTER SUBROUTINE

```
      SUBROUTINE FILTER(SIG,K,C,IMAX)
C  DIGITAL FILTER SUBROUTINE.
C  THE ORDER OF THE FILTER IS AUTOMATICALLY ADJUSTED BY
C  FILDES AS IMAX AND NO SPECIFICATIONS HAVE TO BE
C  INSERTED.
C  THE MAXIMUM ORDER OF THE FILTER IS 20 BUT THIS CAN BE
C  INCREASED BY ALTERING THE DIMENSION STATEMENT.
      DIMENSION C(10,7),Y(21,3)
C  SET Y=0 ON FIRST CALCULATION
      IF (K.GT.1) GO TO 26
      IDIMY=IMAX+1
      DO 25 N=1,IDIMY
      DO 25 M=1,3
25    Y(N,M)=0
26    Y(1,1)=SIG
      DO 27 I=1,IMAX
      L=I+1
C  DIGITAL FILTER EQUATION
27    Y(L,1)=(C(I,7)*(Y(I,1)*C(I,4)+Y(I,2)*C(I,5)+Y(I,3)
     C*C(I,6))-Y(L,2)*C(I,2)-Y(L,3)*C(I,3))/C(I,1
C  Y SHIFT
      DO 28 I=1,IDIMY
      Y(I,3)=Y(I,2)
28    Y(I,2)=Y(I,1)
      SIG=Y(IDIMY,1)
      RETURN
      END
```

A3.4 OTHER SUBROUTINES

A3.4.1 SUBROUTINE TO GENERATE A PSEUDO RANDOM SEQUENCE (WRITTEN BY DR. B.R. DAVIS)

```
      FUNCTION NOISE(X)
      K=N/2
      L=N-2*K
      M=K/16-2*(K/32)
      N=K
      IF (L.NE.M) N=N+34359738368
      NOISE=2*L-1
      RETURN
      ENTRY NOISET
      N=32835725128
      NOISE=0
      RETURN
      END
```

A3.4.2 SUBROUTINE TO CALCULATE THE RMS POWER

```
      SUBROUTINE POWER1(Y0,SP,ID)
C  THIS SUBROUTINE CALCULATES THE POWER OF Y0,STARTING WHEN
C     ID IS POSITIVE.THE ACCUMULATED POWER IS STORED AS SP
      IF(ID)21,21,22
 21   Y1=Y0
      SP=0
      RETURN
C  CALCULATE POWER OF Y IN THE SAMPLING INTERVAL
 22   P=(2*Y0*Y0+Y0*Y1)/3
      Y1=Y0
      SP=SP+P
      RETURN
      END
```

A3.4.3 SUBROUTINE TO CALCULATE THE AVERAGE SIGNAL

```
      SUBROUTINE RECT1(X,ROUT,ID)
C  THIS SUBROUTINE CALCULATES THE ACCUMULATED FULL WAVE
C  RECTIFIED SIGNAL, WHICH IS STORED AS ROUT.
C  TEST FOR STARTING CONDITIONS
      IF (ID) 2,3,3
2     ROUT=0
      XD=X
      RETURN
C   CALCULATE THE AVERAGE OF X DURING THE SAMPLING INTERVAL
3     ISGNX=1
      IF (X.LT.0) ISGNX=-1
      IF (ISGNX+ISGNXD) 4,5,4
4     AV=(X+XD)/2
      GO TO 6
5     AV=(X*X+XD*XD)/(2*(X-XD))
6     XD=X
      ISGNXD=ISGNX
      AV=ABS(AV)
C  INCREMENT THE AVERAGE TO THE PREVIOUS STORED TOTAL
      ROUT=ROUT+AV
      RETURN
      END
```

A3.4.4 SUBROUTINE TO CALCULATE THE RELATIVE OCCURRENCE OF CONTROL WORDS

```
      SUBROUTINE WORD(IC,IT,K,ID)
C  THIS SUBROUTINE STORES THE LAST TEN BITS OF THE
C  BINARY TRANSMITTED SIGNAL AS THE ARRAY IA AND IT
C  PROGRESSIVELY CHECKS THE PRESENCE OF A SEQUENCE OF
C  SIMILAR OR ALTERNATING BITS,INCREMENTING THE COUNTERS
C  IN THE ARRAY IT AS A SEQUENCE IS DETECTED.
      DIMENSION IA(10),IT(19)
C  CLEAR THE STORES
      IF (K.GT.1) GO TO 4
      DO 2 N=1,10
2     IA(N)=0
      DO 3 N=1,19
3     IT(N)=0
C  SHIFT THE BINARY TRANSMITTED SIGNAL STORE AND ADD A
C  NEW BIT.
4     DO 5 N=1,9
5     IA(11-N)=IA(10-N)
      IA(1)=IC
C  TEST FOR THE STARTING CONDITIONS
      IF (ID) 6,6,7
6     RETURN
C  CHECK WHETHER THE LAST TWO BITS ARE THE SAME OR DIFFERENT
7     IF (IA(1)+IA(2).NE.0) GO TO 10
C  INCREMENT THE STORE,CONTAINING THE NUMBER OF TIMES THE
C  CONTROL WORDS 10 OR 01 HAVE OCCURRED
      IT(1)=IT(1)+1
C  DETERMINE THE LENGTH OF THE SEQUENCE OF BITS OF ALTERNATE
C  SIGN
      DO 8 N=2,9
      IF (IA(N)+IA(N+1).NE.0) GO TO 9
C  INCREMENT THE STORE,CONTAINING THE NUMBER OF TIMES A
C  SEQUENCE OF ALTERNATE BITS AND LENGTH N HAS OCCURRED
      IT(N)=IT(N)+1
      GO TO 8
9     N=10
8     CONTINUE
      RETURN
C  INCREMENT THE STORE,CONTAINING THE NUMBER OF TIMES THE
C  CONTROL WORDS 11 OR 00 HAVE OCCURRED
10    IT(10)=IT(10)+1
C  DETERMINE THE LENGTH OF THE SEQUENCE OF SIMILAR BITS
      DO 11 N=2,9
      IF (IA(N)-IA(N+1).NE.0) GO TO 12
C  INCREMENT THE STORE,CONTAINING THE NUMBER OF TIMES A
C  SEQUENCE OF BITS WITH THE SAME SIGN AND LENGTH N
C  HAS OCCURRED
```

```
      IT(9+N)=IT(9+N)+1
      GO TO 11
12    N=10
11    CONTINUE
      RETURN
      END
```

A3.4.5 SUBROUTINE TO CALCULATE THE GROUP DELAY

```
      SUBROUTINE GRDEL(Y,X,DEL,K,ID)
C   THIS SUBROUTINE CALCULATES THE NUMBER OF SAMPLES BETWEEN
C   A ZERO CROSSING OF Y (FILTER INPUT) AND X (FILTER OUTPUT)
C   ,FROM WHICH THE PHASE AND HENCE THE GROUP DELAY CAN BE
C   CALCULATED
      DIMENSION DEL(4)
      IF (K.LE.1) SIGNXD=SIGNYD=N=1
      IF (ID.LE.0) DEL(1)=DEL(2)=DEL(3)=DEL(4)=0
C   FIND SIGN OF Y
      SIGNY=-1
      IF (Y.GT.0) SIGNY=1
C   DETECT ZERO CROSSING OF Y
      IF (SIGNY+SIGNYD.NE.0 ) GO TO 1
      N2=N1
      N1=N
      N=0
1     SIGNX=-1
C   FIND SIGN OF X
      IF (X.GT.0) SIGNX=1
C   DETECT ZERO CROSSING OF X
      IF (SIGNX+SIGNXD.NE.0) GO TO 2
      DEL(1)=N+DEL(1)
      DEL(2)=N+N1+DEL(2)
      DEL(3)=N+N1+N2+DEL(3)
      DEL(4)=DEL(4)+1
2     SIGNYD=SIGNY
      SIGNXD=SIGNX
      N=N+1
      RETURN
      END
```

APPENDIX 4

ASSOCIATED MATHEMATICS

A4.1 Digital Filtering Theory

The mathematics for designing the digital filters used in the computer simulation is presented below.

For conventional filters the S plane is most useful to design the filter, but for digital filters the Z plane must be used. The Z plane is used in sampled data control systems and most automatic control texts [21] will treat this matter.

The theory presented here is self contained but additional details can be found in digital filtering books [26].

The standard Z transform, used in sampled data systems and converting a transfer function in the S plane G(s) into one in the Z plane G(z) is in many cases cumbersome to derive and can present problems due to aliasing. These disadvantages can be overcome by the use of the bilinear Z transform

$$W = \frac{z - 1}{z + 1} = a + jb \qquad (1)$$

This transformation can be shown to have the following properties:

1) The imaginary axis of the W plane is mapped into the unit circle in the Z plane. (The standard Z transform maps

the imaginary axis of the S plane into a unit circle in the Z plane).

2) The relationship between the W plane and the S plane is approximately linear over the useful frequency range.

By definition $Z = e^{sT}$ where T is the sampling period. Substituting this equation into (1) we obtain

$$W = a + jb = \frac{e^{sT} - 1}{e^{sT} + 1} = \tanh\left(\frac{sT}{2}\right) \qquad (2)$$

along the imaginary axis in the s plane we have:

$$a + jb = \tanh \frac{j\omega T}{2} = j \tan \frac{\omega T}{2}$$

$$\therefore \quad a = 0$$

$$b = \tan \frac{\omega T}{2} \simeq \frac{\omega T}{2} \quad \text{if} \quad \text{is small} \qquad (3)$$

The imaginary axis of the S plane will thus map into the imaginary axis of the W plane. Furthermore equation (3) is linear when ω is small compared with the sampling frequency, as is normally the case.

The bilinear Z transform can thus be used to obtain digital filters by the following procedure:

1) Normalise the S plane transfer function G(s) with respect to a required frequency, normally the cut off frequency, ω_c. It should be noted that often the normalised transfer

function is used as a starting point, since this ontained from filter tables [24].

2) Transform the transfer function from the S plane into the W plane by direct substitution of w for s.

3) Denormalise the transfer function with respect to the digital cut off frequency $b_c = \tan\left(\frac{\omega_c T}{2}\right)$.

4) Use the bilinear Z transform to obtain the transfer function in the Z plane G(z).

5) Use G(z) to obtain a digital filter.

The above steps are illustrated for a general second order transfer function.

$$G(s) = \frac{\omega_n^2}{(s^2 + 2 \quad s + \omega_n^2)} \tag{4}$$

1) this transfer function is normalised with respect to some cutoff frequency ω_c.

$$G_n(s) = \frac{\left(\frac{\omega_n}{\omega_c}\right)^2}{s^2 + \frac{2\xi}{\omega_c} s + \left(\frac{\omega_n}{\omega_c}\right)^2} \tag{5}$$

to simplify the mathematics put:

$$d = \frac{2\xi}{\omega_n} \qquad \text{and} \qquad c = \left(\frac{\omega_n}{\omega_c}\right)^2$$

so that

$$G_n(s) = \frac{c}{s^2 + ds + c} \qquad (6)$$

2) Substitute w for s giving:

$$G_n(w) = \frac{c}{w^2 + dw + c}$$

3) Denormalise with respect to the digital cutoff frequency b_c, giving:

$$G(w) = \frac{c(b_c)^2}{w^2 + b_c dw + c(b_c)^2} \qquad (7)$$

It should be noted that the transfer functions G(s) and G(w) are exactly the same at DC and at the frequency $b_c = \tan\left(\frac{\omega_c T}{2}\right)$. At other frequencies however differences will occur.

4) Use the bilinear Z transform giving:

$$G(z) = \frac{c(b_c)^2}{\left(\frac{z-1}{z+1}\right)^2 + b_c d\left(\frac{z-1}{z+1}\right) + c(b_c)^2} \qquad (8)$$

$$= \frac{c(b_c)^2 (z+1)^2}{(z-1)^2 + b_c d(z^2-1) + c(b_c)^2 (z+1)^2} \qquad (9)$$

$$= \frac{c(b_c)^2 (z+1)^2}{(1+b_c d + c(b_c)^2) z^2 + (1-c(b_c)^2) z + (1-b_c d+c(b_c)^2)} \quad (10)$$

5) Equation (10) can be converted into a digital filter as follows:

write G(z) in terms of z^{-1} so that

$$G(z) = \frac{c(b_c)^2 (1+z^{-1})^2}{(1+b_c d + c(b_c)^2) + (1-c(b_c)^2)z^{-1} + (1-b_c d+c(b_c)^2)z^{-2}} \quad (11)$$

if X(z) is the input to the filter and Y(z) is the output we can write

$$Y(z) = G(z)\, X(z) \quad (12)$$

But both X(z) and Y(z) can be expressed as:

$$X(z) = \sum_{n=0}^{\infty} X_n z^{-n} \quad (13)$$

$$Y(z) = \sum_{n=0}^{\infty} Y_n z^{-n} \quad (14)$$

substituting this in equation (12) gives:

$$\left((1+b_c d+c(b_c)^2) + (1-c(b_c)^2)z^{-1} + (1-b_c d+c(b_c)^2 z^{-2}\right) \sum_{n=0}^{\infty} Y_n z^{-n} = c(b_c)^2 (1+2^{-1})^2 \sum_{n=0}^{\infty} X_n z^{-n} \quad (15)$$

If we want to know the output at the nth sampling interval, we collect the coefficients of the terms containing z^{-n} in the above equation, giving:

$$(1 + b_c d + c(b_c)^2)\, Y_n + (1 - c(b_c)^2)\, Y_{n-1}$$

$$+ \; (1 - b_c d + c(b_c)^2)\, Y_{n-2} = c(b_c)^2\, X_n +$$

$$2\, c(b_c)^2\, X_{n-1} + c(b_c)^2\, X_{n-2} \qquad (16)$$

Now Y_n is the output of the filter at the nth sampling interval and Y_{n-1} is the output at the sampling interval before.

The output from the filter can thus be calculated from both the input at the present and previous sampling intervals and the output at previous sampling intervals.

The digital filtering equation is thus:

$$Y_n = \frac{1}{1 + b_c d + c(b_c)^2} \; (\; c(b_c)^2\, (X_n + 2X_{n-1} + X_{n-2})$$

$$- (1 - c(b_c)^2)\, Y_{n-1} - (1 - b_c d + c(b_c)^2)\, Y_{n-2} \;) \qquad (17)$$

For the general filter design program presented in Appendix 3, the transfer function to be simulated is split up into a series of second order transfer functions

$$T(s) = \frac{(a_0 s^2 + a_1 s + 1)}{(b_0 s^2 + b_1 s + 1)} \qquad (18)$$

where the constants a_0, a_1, b_0 and b_1 are calculated from the data read in. (These constants can be zero). The computer program then uses this transfer function to calculate the corresponding digital filter as outlined above. By cascading the resulting digital filters, most transfer functions can be realised.

A4.2 Leaky Integrator Simulation

The transfer function

$$G(s) = \frac{b}{s+a} \qquad (19)$$

corresponds to an RC type integrator with a time constant $\frac{1}{a}$ and a dc gain of $\frac{b}{a}$. Using Z transform tables [21], the above transfer function in the Z plane can be found as

$$G(z) = \frac{bz}{z - e^{-aT}} = \frac{b}{1 - e^{-aT} z^{-1}} \qquad (20)$$

where T is the sampling period.

Using the same technique used to obtain eqn(17) from eqn(10) in section A4.1, the integrator output can be expressed in the form

$$Y_n - e^{-aT} Y_{n-1} = bX_n$$

$$\text{i.e. } Y_n = bX_n + e^{-aT} Y_{n-1} \qquad (21)$$

which can be used in thecomputer simulation.

For the integrator used in the delta modulators bX_n is

the step size and e^{-aT} corresponds to the leakyness of the integrator.

It should be pointed out that since the integrator to be simulated has a finite gain at half the sampling frequency, the bilinear Z transform described in section A4.1 cannot be used, since it would result in an integrator with an infinite attenuation at half the sampling frequency.

A4.3 Delay of an RC Network

Consider an RC network, connected to give a first order low pass Bessel filter. The transfer function of this network is as follows:

$$T(s) = \frac{a}{s+a} \qquad (22)$$

Along the frequency axis this becomes:

$$T(j\omega) = \frac{a}{j\omega+a} = \frac{a}{\sqrt{\omega^2+a^2}} \angle \arctan \frac{\omega}{a} \qquad (23)$$

The group delay can be found as:

$$t_g(\omega) = \frac{d}{d\omega} \arctan \frac{\omega}{a} = \frac{a}{\omega^2+a^2}$$

The average time delay can be found by substituting $\omega = 0$, giving

$$t_g(0) = \frac{1}{a} \qquad (24)$$

(the same result can be obtained by consulting group delay characteristics for Bessel filters as presented in filter

handbooks [24]).

An RC network can thus be used to obtain a delay of one sampling period (T), as required for the measuring equipment of Chapter 2, by making

$$a = f_s = \frac{1}{T} \qquad (25)$$

where f_s is the sampling frequency.

In order to use an RC network as a delay line in the measuring equipment described uin Chapter 2, the difference between the output of the RC network and an ideal delay must be less than 0.3% for all input signal frequencies, if SNR's of up to 40 dB are to be measured.

This difference can be found as

$$D(\omega) = e^{-j\omega T} - \frac{1}{1+j\omega T} \qquad (26)$$

By evaluating the above expression at different frequencies and calculating $|D|$, one finds that $|D| \leqslant 0.003$ if $\omega T \leqslant 0.08$.

An RC network can thus act as a delay line, introducing less than a 0.3% change in waveform, if the input frequency f satisfies the condition that:

$$\frac{\omega}{2\pi} = f \leqslant \frac{0.08a}{2} = 0.08 f_c \qquad (27)$$

where f_c is the cut off frequency of the RC network.

For delta modulation with a sampling frequency of 40KHz, the maximum frequency which enables a SNR of 40dB to be

measured can be obtained from the eqns(25) and (27) as:

$$f \leqslant \frac{0.08 \times 40 \times 10^3}{2\pi} = 204\text{Hz} \qquad (28)$$

From this it can be seen that a single RC network is not suitable for the delay line in the measuring equipment described in Chapter 2.

A4.4 The SNR Obtained from the Notch Filter Method when Slope Limiting Occurs.

When slope limiting occurs the demodulated output becomes a triangular waveform, as can be seen in Fig 2.1.

If the height of this waveform is A, the demodulated output can be expressed by the Fourier series:

$$Y(t) = A \left(\sum_{n=1}^{\infty} \frac{8}{\pi^2 n^2} \times \frac{1}{2} \left(1 - \cos n\pi \right) \times \cos (nt) \right)$$

$$= A \left(\frac{8}{\pi^2} \cos(t) + \frac{8}{9\pi^2} \cos (3t) + \frac{8}{25\pi^2} \cos 5t \right.$$

$$\left. + \ldots\ldots\ldots \right) \qquad (29)$$

The demodulated output power can be found by evaluating the mean square of a triangular wave and is equal to $\frac{1}{3} A^2$.

The quantization noise as measured by the notch filter method is the sum of the power of all the harmonics except the fundamental. This is also the total power minus the power of the fundamental since all harmonics are orthogonal.

Thus

$$\text{Distortion} = \frac{1}{3} A^2 - \frac{1}{2} \left(A \times \frac{8}{\pi^2}\right)^2$$

$$= 0.004822\ A^2 \qquad (30)$$

and the SNR is thus

$$\text{SNR} = \frac{\frac{1}{3} A^2}{0.004822 A^2} = 18.4 \text{ dB} \qquad (31)$$

The above is the SNR obtained when the quantization noise is not filtered.

Normally one is only interested in the noise components below 3.5KHz. If an 800Hz sinewave is used, only the third harmonic component in equation (29) will remain giving:

$$\text{SNR} = \frac{\frac{1}{3} A^2}{\frac{1}{2} \left(\frac{8A}{9\pi^2}\right)^2} = 19.1 \text{ dB} \qquad (32)$$

BACKGROUND OF INVENTION

Pulse code modulators are known which convert an analogue waveform into a binary waveform, such as pulse code modulators or delta modulators. It is known that for small inputs the quantization noise is large compared with the signal, for large inputs the system is limiting. It will be realised that increasing the gain of the local demodulator will increase the input power for which the optimum SNR (signal to quantization noise ratio) occurs. The normalized input power, which is defined as the ratio of the input power to the gain of the demodulator, at which this optimum SNR occurs remains constant. It has been found that the dynamic range of the modulator can be extended by altering the gain of the demodulator in such a way that the normalized input power remains constant.

A measure of the normalized input power can be derived from the binary signal and since the same binary signal is present at both the local demodulator and the distant demodulator, the same measure of the normalized input power can be obtained at both the modulator and demodulator.

In order to derive a measure of the normalized input power, one must select one or more binary patterns, or control words, the relative occurrence of which varies with the input power.

The best control can be achieved if the function of relative occurrence of the binary pattern versus normalized

input power is a monotonic increasing or decreasing function.

Despite the fact that some of the above general principles are known, they have not been applied as in this invention to obtain complete companding, mainly because previously it was not known how to keep the normalized input power at the value corresponding to the optimum performance of the modulator, over a sufficient range of input powers.

SUMMARY OF INVENTION

Consider the case where the relative occurrence of the control word decreases with normalized input power and where the relative occurrence at the normalized input power corresponding to the peak SNR is X .

If the relative occurrence of the control word is less than X% , the normalized input power is too high and the gain of the demodulator must thus be increased, to decrease the normalized input power. If the relative occurrence of the control word is more than X , the normalized input power is too low and the gain of the demodulator must thus be decreased, to increase the normalized input power.

For linear control, the gain is changed linearly, the rate of increase or decrease of gain is thus fixed. Consider again a relative occurrence of the control word which decreases with normalized input power.

If the occurrence of a control word is used to decrease the gain of the demodulator by K (1-X) units of gain

and the gain is increased by KX units if the control word does not occur, the average gain will remain constant when the system operates at the desired optimum normalized input power. K is any positive constant.

Increase in average gain) (increase in gain due to the control word not occurring) x (the relative occurrence of the control word not occurring) - (decrease in gain due to the control word occurring) x (the relative occurrence of the control word) = $KX(1 - X) - (1 - X)X = 0$.

When the relative occurrence is less than X% (say $Y < X$), the gain of the demodulator is increased, since the increase in gain = $KX(1 - Y) - K(1 - X)Y = K(X - Y) > 0$.

This decreases the normalized input power (and increases the relative occurrence of the control word) until the correct normalized input power is reached, when the average gain remains constant (Y has now become equal to X).

Similarly, if the relative occurrence of the control word is greater than X the gain of the demodulator is decreased, which increases the normalized input power, until the optimum normalized input power is reached.

It should be noted that the attack and decay time constants are dependent on the relative occurrence of the control words, the amount by which the gain is changed and the sampling time (i.e. how often the gain can be changed.)

The ratio of attack to decay time constants is X to 1-X. The ratio can thus be selected by selecting control

words which have the relative occurrence of

$$X = \frac{R}{1 + R}$$

at the optimum normalized input power. R is the ratio of attack to decay time constant.

Similar reasoning applies if the relative occurrence of the control word increases with normalized input power. The occurrence of a control word is then used to increase the gain of the demodulator and the gain is decreased if no control word occurs.

Logarithmic control can be achieved by using a percentage change of gain instead of an absolute change in gain. Since the gain of the demodulator varies, the absolute change in gain will also vary. We still want the average gain to remain constant, when the relative occurrence of the control word is X . The percentage change in gain must now be selected according to

$$(B + 1)^{1-X} \cdot (A + 1)^{X} = 1.$$

A is the relative change of gain if a control word occurs, B is the relative change of gain if no control word occurs. Either A or B will be negative, indicating a decrease in gain depending on whether the control word increases or decreases with normalized input power.

The ratio of attack to decay times is again B to A or A to B, for a relative occurrence which is decreasing or increasing with normalized input respectively. Since the companding can produce an exponential rate of change of gain, one can no longer talk about time constants, but one must refer to a rate of change of gain of "so many

dB per second." The rate of change of gain is again directly related to the values of A, B and the sampling time.

This rate can thus be adjusted by altering the percentage change of A and B, but keeping their ratio constant.

Since digital circuitry has several advantages over analogue circuitry, it is desirable to apply this companding technique to digital circuitry as well.

Linear counting can be obtained very easily, using a forward and reversible counter, which is incremented by one or more steps, depending on whether a control word occurs or not. The contents of the counter controls the gain of the demodulator by means of say a switched resistor network.

For true logarithmic control the contents of the counter is increased by A. N. or B. N. where A and B are the percentage increments, as before, and N is the contents of the counter. A. N. and B.N. however need not necessarily be an integers, so that the approximations must be made.

It is possible to approximate A. N. or B. N. to the nearest integer, but this will lead to complex circuitry. Relatively simple circuitry will be obtained if the contents of the counter are incremented by A. M. or B. M. where M is N, truncated to a binary weighted interger.

For example, when N is between 8192 and 16383 (i.e. between 2^{13} and $(2^{14} - 1)$, M is 8192 (i.e. 2^{13}).

This means that linear counting is used over a nearly 2:1 range in the contents of the counter. However for large changes in the contents of the counter the counting is logarithmic, since M is directly related to N.

The increase in dynamic range of the pulse modulator is directly related to the number of bits of the forward and reversible counter, since it is directly related to the change in gain of the demodulator.

ADVANTAGES OF INVENTION

1) Companding with complete control is obtained, enabling the best possible performance to be achieved.

2) The dynamic range over which this optimum performance is obtained, can be chosen at will.

3) The attack and decay times can be chosen separately and at will.

4) Although generally described herein as applied to delta modulation, the principles can be applied equally to pulse code modulation, delta pulse code modulation and their variants.

5) The principles can be applied to systems incorporating an m-ary transmitted signal.

6) The principles can be applied to forms of delta modulation, pulse code modulation, delta pulse code modulation and their variants, incorporating some other form of companding as well, so that double companding can be obtained.

7) The companding can be designed to result in the

optimum performance for any specific input signal.

BRIEF DESCRIPTION OF DRAWINGS

Fig. 1A is a block diagram showing prior art Delta modulator principles, in which an analogue waveform is converted to a binary waveform, 1A, 1B and 1C showing various input levels,

Fig. 2 demonstrates the invention showing how use of control words enables an up and a down count to be used to obtain companding,

Figs. 3A, 3B and 3C show how control can be achieved if the function of relative occurrence of the binary pattern versus normalized input power is a monotoric increasing or decreasing function,

Fig. 4 shows a block diagram of a pulse code modulator with companding according to this invention,

Fig. 5 shows a graph of the performance of the companding system of Fig. 4,

Fig. 6 is a block diagram showing how the gain of a delta modulator can be varied,

Figs. 7, 8 and 9 are an expanded detail of the system shown in Fig. 6, Fig. 7 showing the R.C. integrator, Fig. 8 the control word detector and Fig. 9 a digital control switch and memory, and

Figs. 10 and 11 indicate in graphical form the comparison between companded and uncompanded delta modulation and PCM, as well as the measured performance for the ΔM embodiment.

PREFERRED EMBODIMENT

Two preferred embodiments are given, one for a delta modulation system and one for a pulse code modulation system.

It should be realized however that these embodiments are specific examples only and that different designs must be obtained in order to suit the companding to the type of modulator, the clock frequency and the input signal required.

In Fig. 1 as stated the present state of the art is shown, the modulator 1 of Fig. 1 converting an analogue waveform input at 2 to a binary output at 3. In the demodulator the binary input at 5 is passed to a demodulator and a low pass filter 7 to produce the analogue output at 8.

Figs. 1A and 1B shows respectively the binary signal at low modulation and at high modulation. Fig. 1C shows normal level modulation.

In Fig. 2 is shown the system of companding according to this invention. The input signal and the demodulated output being shown at 'A' and the binary transmitted signal at 'B'.

The control signal at C is derived from B by detecting the binary patterns 01 or 10 being the control words in the binary transmitted signal. If a control word occurs, the gain of the demodulator, as shown in 'D', is decreased and if no control word occurs, the gain is increased.

Fig. 3A shows a graph of relative SNR in decibels plotted against relative input in decibels the region of constant quantization being designated 10 and the region of overload 11.

In Figs. 3B and 3C are shown relative percentage occurrence of control word against normalized input power in decibels to show the region of overload, the region of constant quantization noise being again designated by 10 and the region of overload in each case by 11.

In Fig. 4 is shown how the modulator analogue input at 20 is fed to a gain control 21 but the binary transmitted signal is fed to the control word detector 22 which feeds the NO - YES count to the counter 23 which feeds the converter 24 which in turn feeds back to the gain control multiplier 25.

In Fig. 5 is plotted the relative SNR against relative input in decibels, showing the region of companding at 33 with the region of constant quantization noise at 34 and the region of overload at 35.

One method by which the gain of the modulator can be varied is shown in Fig. 6, which applies specifically to Delta Modulation, however many methods can be used in controlling the gain of the demodulator from the counter contents.

THEORY

By means of computer simulation the relative occurrence of the words 10 and 01 in the binary transmitted signal was found to vary with the shape similar to Fig. 3C. The delta modulator designed is of the single integration delta modulation type, and is intended for operation with speech at a sampling frequency of 40KHz. Under these conditions the peak SNR was found to occur when the control words 10 and 01 have an occurrence in the binary transmitted signal of 66%.

Digital circuitry is used to control the companding of the proposed delta modulator and for practical reasons, semi-logarithmic companding is used.

The relative changes of gain, A and B, must now be selected. It is advisable to optimise these constants by means of computer simulation. From the computer simulation, the best performance was found to occur when $A = \frac{-1}{32}$ and $B = \frac{1}{16}$. From the description of semi-logarithmic companding it is thus clear that the contents of the counter is increased by two or decreased by one if the contents of the counter are between 32 and 63.

The companding ratio, being the ratio of the largest to the smallest gain, must now be selected. In practice the companding ratio will be a compromise between performance and circuit complexity. A companding ratio of 40dB will in practice be more than adequate, but in order to illustrate the versatility of the companding technique, a 60dB companding ratio was chosen.

Referring now again specifically to Fig. 6 which will be expanded into Figs. 7, 8 and 9 it will be seen to have three sections namely: and R.C. integrator 40 a clocked comparator 41 and a digital switch control 42.

The digital switch control 42 controls the charge on the condenser C by bringing in the resistors R1, R2 to Rn as required for companding, and this controls the gain by selecting the correct feedback. 43 represents a comparator.

The digital switch control serves four purposes as indicated in Fig. 7, namely:

1) It determines whether the gain should be increased or decreased.

2) It determines the amount the gain is changed.

3) It stores the gain.

4) It controls the switch resistor network, thereby controlling the gain.

Each of these sections will now be dealt with.

In Fig. 7, 51 is the circuit which determines increase or decrease of gain. The signal from this is fed to 52 which determines the amount of change of gain. 53 is the gain store, while 54 is the switch control for the resistor network. All of this is incorporated in the digital switch control 42.

Determination of increase or decrease of gain.

This section is very simple. The output becomes a one, denoting a decrease in gain when a control word has been detected. Fig. 8 shows the required circuitry which comprises feeding the binary signal into the clock control 60, the binary signal passing to the NAND Gates 61, 62 and 63 and via the AND

gate 64 to the output.

Determination of the amount of the change of gain.

As mentioned previously semilogarithmic companding is used with $A = \frac{-1}{32}$ and $B = \frac{2}{32}$ so that two clockpulses must be generated if the gain is increased and one clock pulse must be generated if the gain is decreased.

In order to obtain the correct fractional increase, the counting must take place 6 bits from the most significant bit of the counter, as is indicated in Fig. 9.

This simply comprises a discriminator 70 which determines the most significant bit. The units 71 and 72 are the stop-count devices, 71 stopping the up count and 72 the down count when the counter has reached the upper and lower limits. The signal is fed in at 73 and goes to the up-down counting assembly 74. Gates ensuring proper counting when the count has reached the upper or lower limit are designated 75.

During the counting, as an example, as soon as the 16th bit becomes a 1, forward counting is prevented. When the 5th bit becomes the most significant bit, downward counting is prevented.
The companding ratio is thus $20 \log \frac{2^{15}}{2^5-1} = 60.5\text{dB}$.

The gain is stored in a counter. This counter 74 must be capable of counting forward and reverse as well as having terminals for counting in binary integers up to 1024.

The bits of the counter control the switches in the resistor network.

Transistor switches were used in the hardware.

The R.C. integrator and the clocked comparator are commonly used circuits and their design will be omitted from this discussion. Since their companding ratio is 60dB, these circuits should however be capable of handling signals with a dynamic range of at least 80dB.

The performance of the companded delta modulator is shown in Fig. 10, together with computer simulation results of the companded and uncompanded delta modulators.

In this the SNR in decibels is plotted against relative input in decibels (base) and the companded delta modulation is indicated by the line 80 while the uncompanded signal is designated 81. Measured points are indicated by X.

PULSE CODE MODULATION

THEORY

For the pulse code modulation embodiment, a 7 bit PCM system was chosen. The sampling frequency used was 8KHz. The control word chosen was the two most significant digits in the PCM code, excluding the sign bit, being zero. In other words a control word is detected if the amplitude of the analogue signal at the sampling instant is less than a quarter of the maximum amplitude. The relative occurrence of the control word again varies with a shape similar to Fig. 4. Similarly to the delta modulation design, the constants A and B

were obtained by computer simulation as $A = \frac{-1}{8}$ and $B = \frac{5}{16}$. Again a 60 dB companding ratio was selected. The resulting performance, obtained by computer simulation is compared with the performance of uncompanded PCM in Fig. 11.

In this again SNR in decibels is plotted against relative input in decibels and the companded PCM is indicated by the line 82 while the uncompanded PCM is indicated by 83.

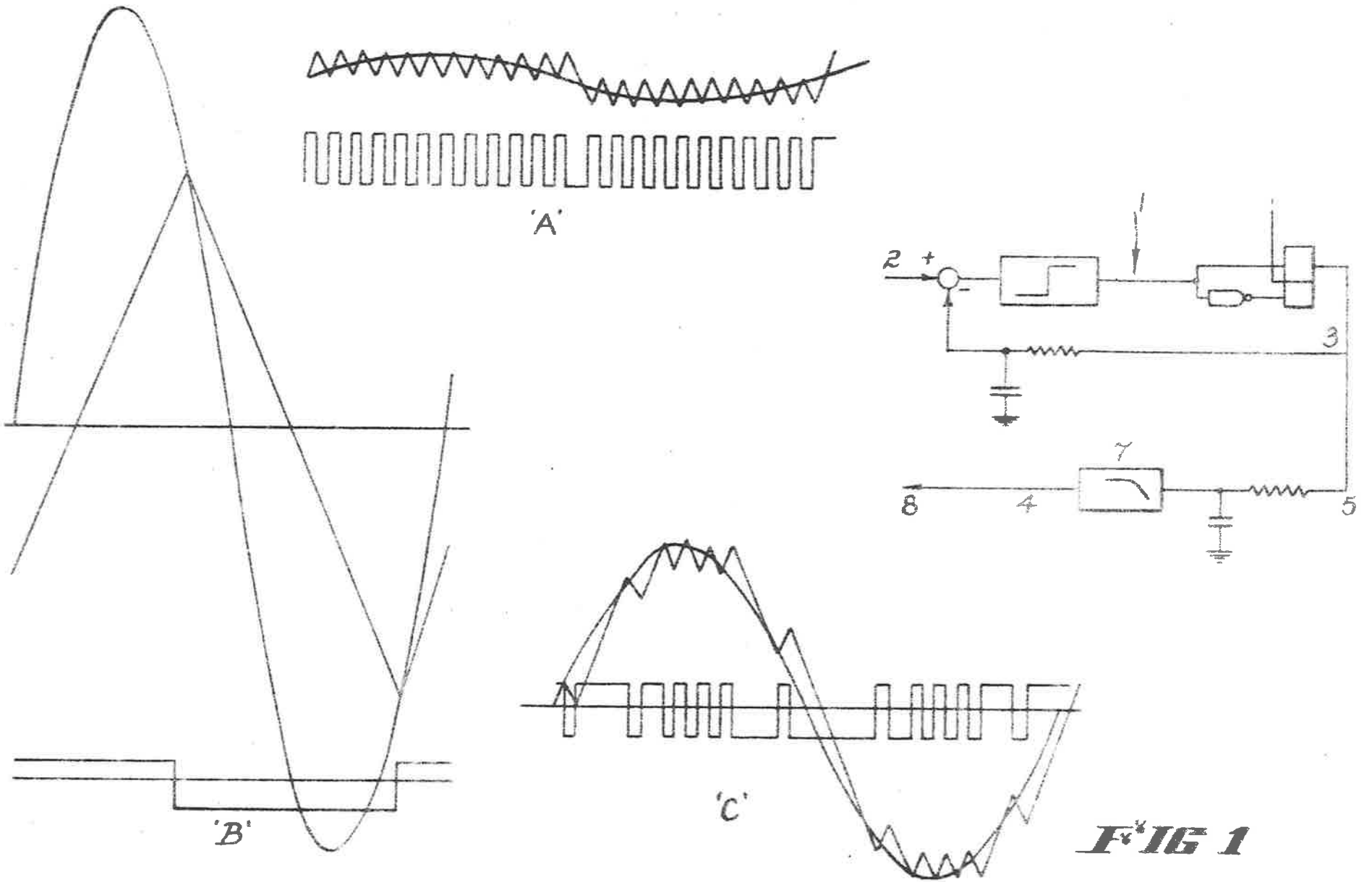


FIG 1

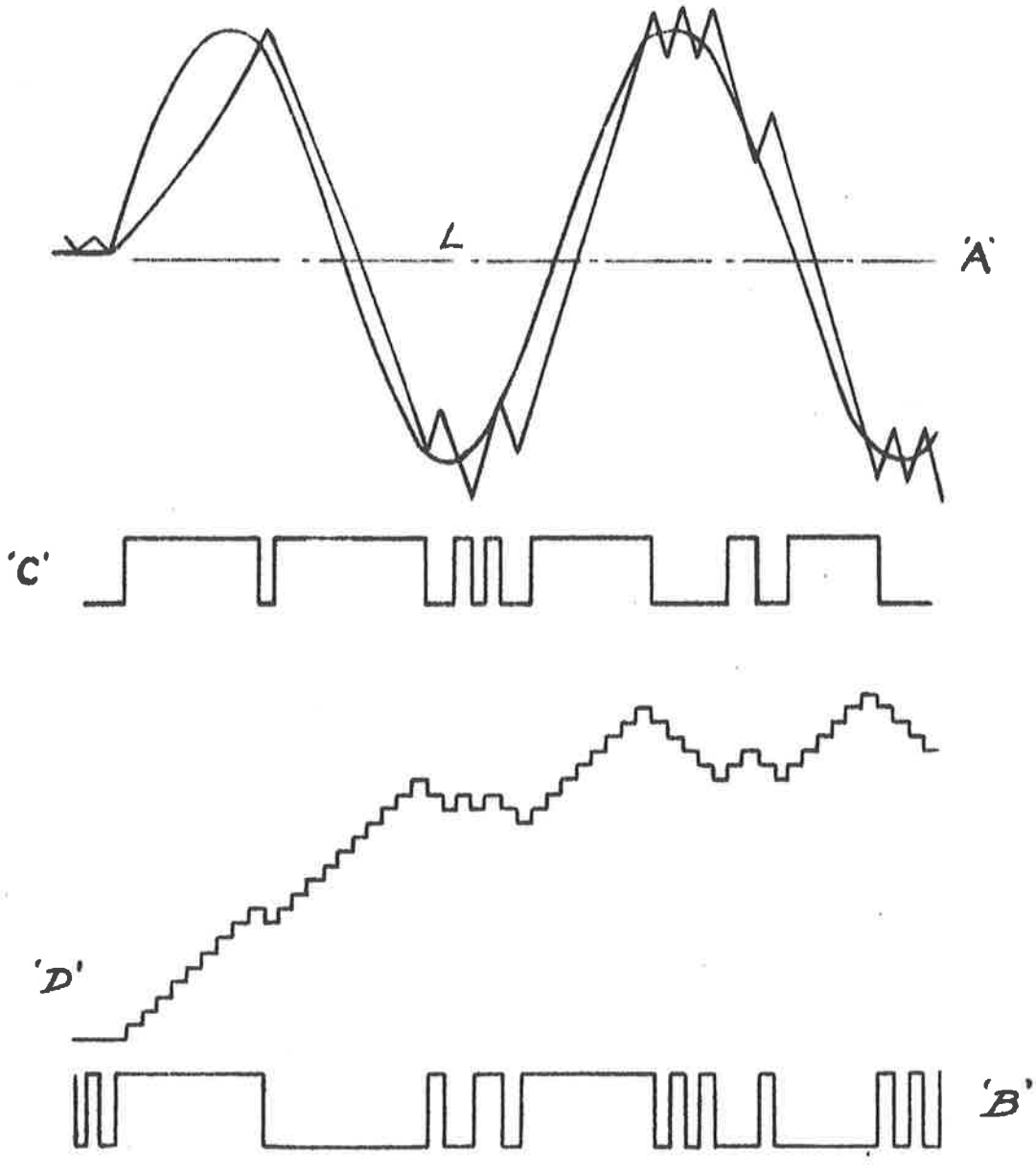
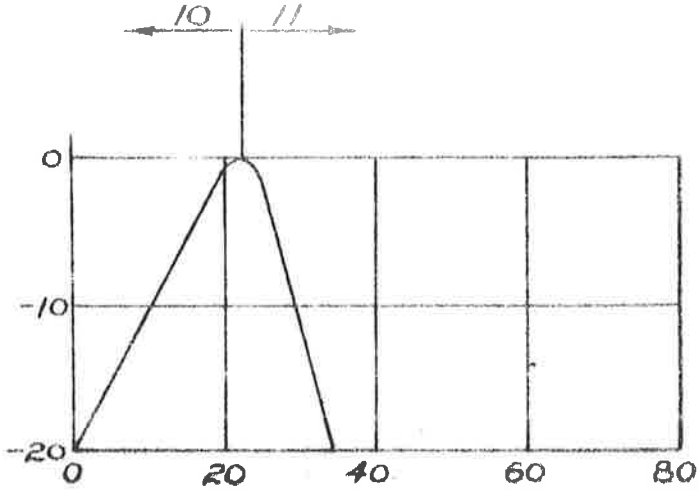
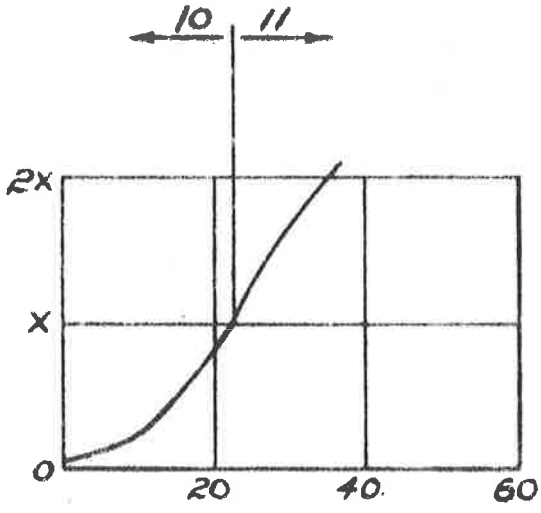


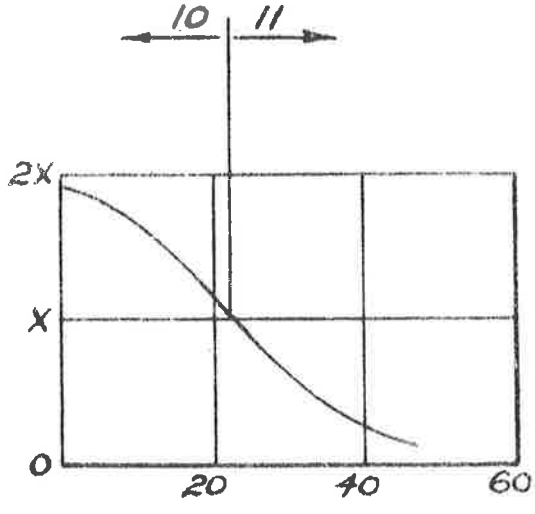
FIG 2



'A'



'B'



'C'

FIG 3

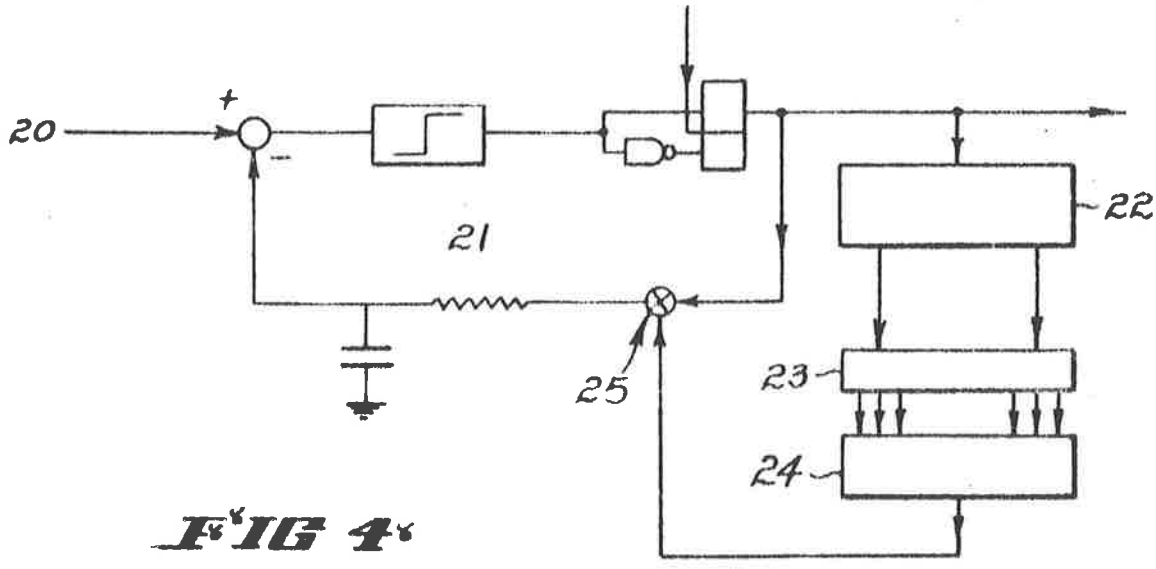


FIG 4

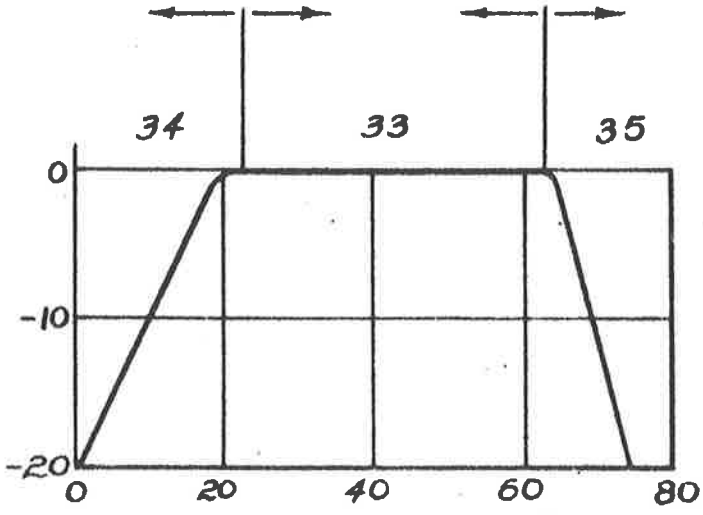


FIG 5

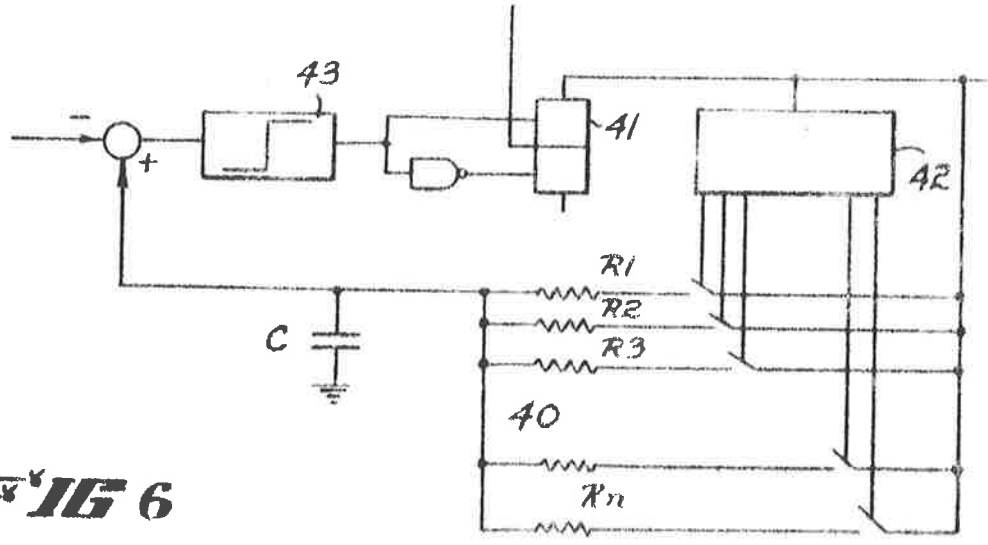


FIG 6

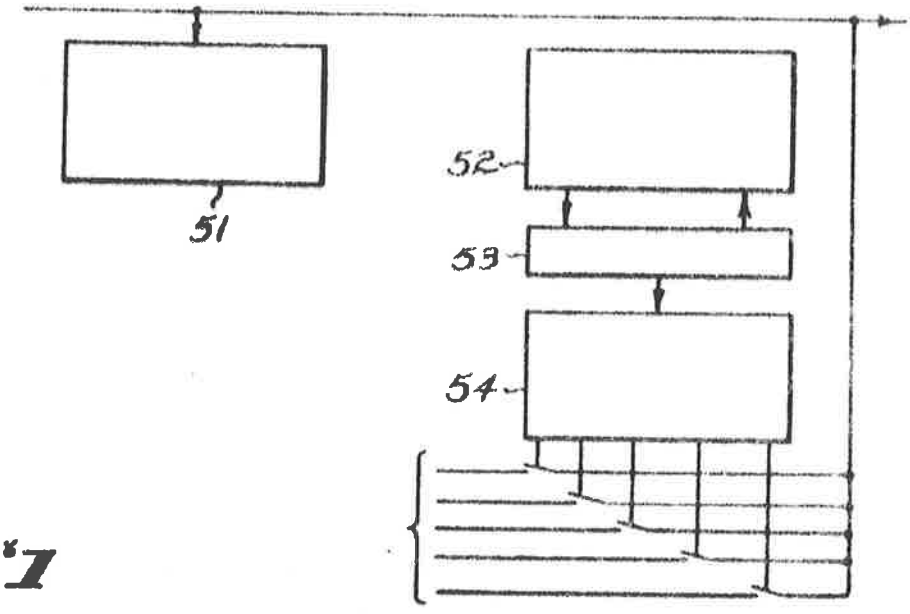


FIG 7

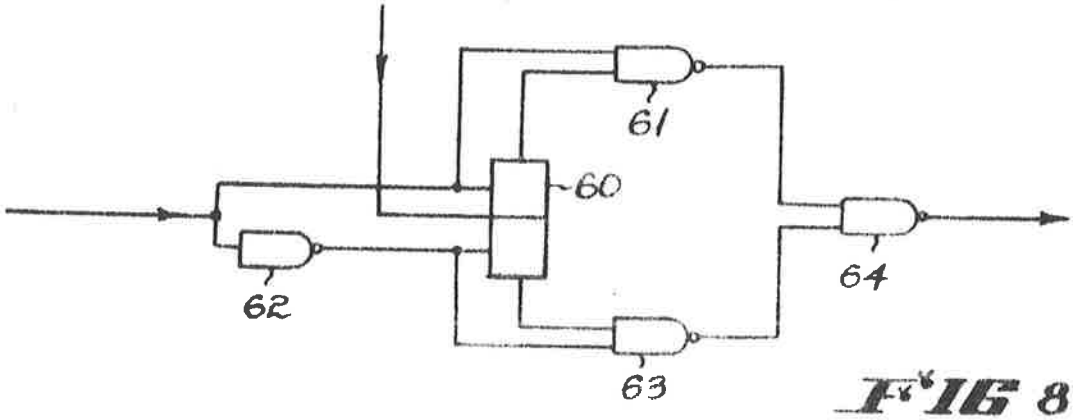


FIG 8

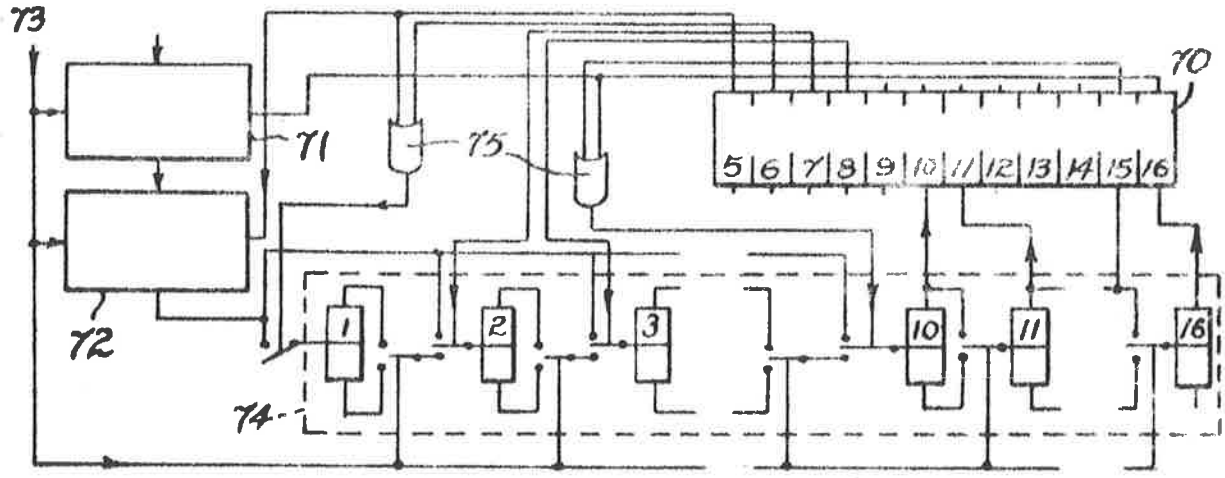


FIG 9

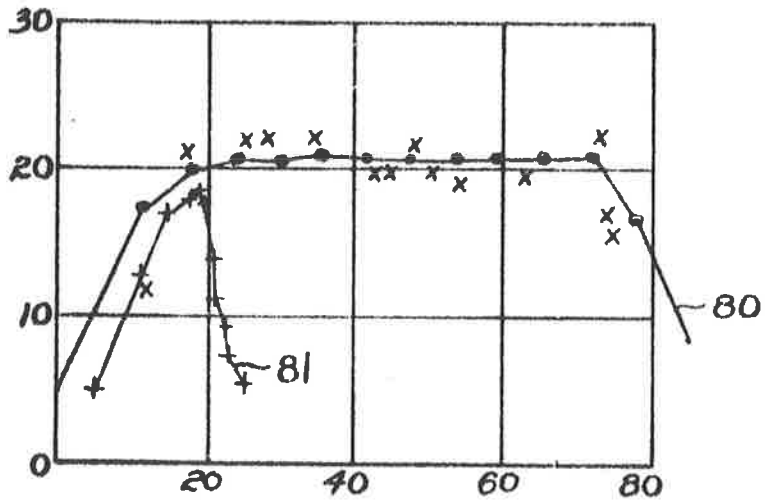


FIG 10

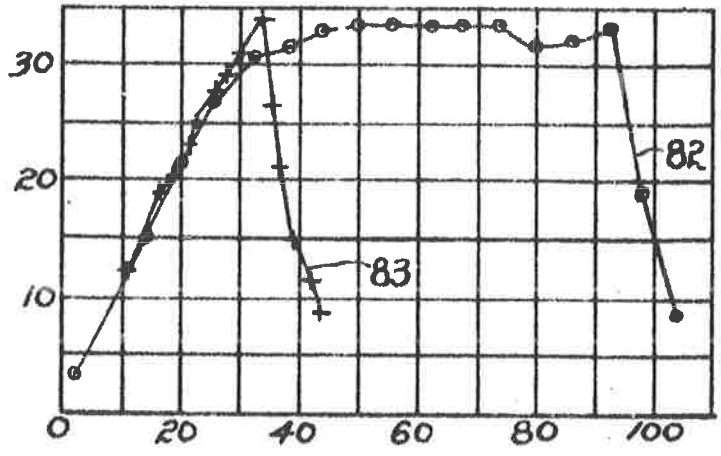


FIG 11

Kikkert, C. (1971). Digital techniques in delta modulation. *IEEE Transactions on Communication Technology*, *19*(4), 570-574.

Kikkert, C. J. (1971). Measurement of quantisation distortion for random inputs. *Proceedings of the I.R.E.E. Australia, Dec*., 459-464.

REFERENCES

(1) Deloraine E.M., van Mierlo S. and Derjavitch B.
"Methode et système de transmission par impulsions"
French patent No. 932140, August 1946

(2) De Jager F.
"Delta modulation: A method of pulse code modulation transmission using a 1 unit code"
Philips research report, Vol.7, No. 6, December 1952
pages 442 - 446

(3) Zetterberg L.H.
"A comparison between delta and pulse code modulation"
Ericsson technics, Vol. 11, No. 1, 1955
pages 95 - 154

(4) Inosi H., Yasuda Y. and Murakami J.
"A telemetring system by code modulation $\Delta\Sigma$ modulation"
I.R.E. transactions on space electronics and telemetry
September 1962
pages 204 - 209

(5) Winkler M.R.
"High information delta modulation"
I.R.E. convention record, part 8, 1963
pages 260 - 265

(6) Montgomery C.T.
"A study of variable slope delta modulation"
M.Sc. thesis submitted to George Washington University
June 1967

REFERENCES (Continued)

(7) Bennier D.J., McKibbin J. and Wollaston T.C.
"Multiplexing of delta modulated signals"
W.R.E. technical report project mallard W.B.S.
No. H A010405 - 04, October 1068

(8) Abate J.E.
"Linear and adaptive delta modulation"
Proceedings I.E.E.E., Vol. 55, No. 3, March 1067
pages 298 - 308

(9) Bosworth R.H. and Candy J.C.
"A companded one bit coder for television transmission"
Bell. Sys. Tech. J., Vol. 48, No. 5, May - June 1969
pages 1459 - 1480

(10) Tomozawa A. and Kaneko H.
"Modulation characteristics of companded delta modulation"
Electron. Commun. Japan, Vol. 49, No. 11, November 1966
pages 277 - 286

(11) Tomozawa A. and Kaneko H.
"Companded delta modulation for telephone transmission"
I.E.E.E. Transactions Communication Technology,
Vol. Com. 16, No. 1, February 1968
pages 149 - 157

(12) Hosokawa S., Tazaky S. and Yamashita K.
"A type of companded delta coder"
Electron. Commun. Japan, Vol. 50, No. 8, August 1967
pages 99 - 108

REFERENCES (Continued)

(13) Wright S.S.
"Amplitude range control"
Bell. Sys. Tech. J., Vol. 17, No. 4, October 1938
page 520

(14) Brolin S.J. and Brown J.M.
"Companded delta modulation for telephony"
I.E.E.E. Transactions Communication Technology,
Vol. Com. 16, No. 1, February 1968
pages 157 - 162

(15) Greefkes J.A. and De Jager F.
"Continuous delta modulation"
Philips Research Report 23, No. 2, April 1968
pages 233 - 246

(16) Hosckawa S. and Yamashita K.
"Companded delta modulation coders of the $\frac{1}{2}$ power and
2/3 power types"
Electron. Comm. Japan, Vol. 51A, No. 11, November 1968
pages 18 - 26

(17) Hauser K. and Zarda S.
"The design of digitally controlled delta modulation
CODECS"
Proceedings I.R.E.E., Vol. 32, No. 7, July 1971
pages 286 - 295

REFERENCES (Continued)

(18) Shindler H.R.
"Delta modulation"
I.E.E.E. Spectrum, October 1970
pages 69 - 78

(19) Kikkert C.J.
"Measurements of quantization distortion for random inputs"
Proceedings I.R.E.E. (Aust.)
Vol. 32, No. 12, December 1971
pages 459 - 464

(20) Kikkert C.J.
"Digital techniques in delta modulation"
I.E. (Aust.) Data Transmission Conference, Brisbane,
June 1970
and
I.E.E.E. Transaction Communication Technology,
Vol. Com. 19, No. 4, August 1971
pages 570 - 574

(21) Raven F.H.
"Automatic Control Engineering"
Book McGraw Hill, International Student Edition, 1961

(22) Kikkert C.J. and The University of Adelaide
"A method for improving modulation efficiency"
Aust. Patent No. C34963/71 and
U.S. Patent No. 193,410

REFERENCES (Continued)

(23) Beranek L.L.

"Acoustic Measurements"

Book J. Wiley and Sons, 1949

(24) Zverev A.I.

"Handbook of filter synthesis"

Book J. Wiley and Sons, 1967

(25) Egan J.P.

"Articulation testing methods"

Laryngoscope Vol. 58 1948

pages 955 - 991

(26) Kuo F.F.and Kaiser J.F.

"System Analysis by Digital Computer"

Book J. Wiley and Sons, 1969

BIBLIOGRAPHY

Delta modulation

(1) Aaron M.R., Fleisman J.S., McDonald R.A. and Protonotarios E.N.
"Response of delta modulation to Gaussian Signals"
Bell. Sys. Tech. J., Vol. 48, No. 5, May - June 1969
pages 1167 - 1196

(2) Arter F.W.
"Simple delta modulation system"
Proceedings I.R.E. (Aust.) September 1962

(3) Bello P.A., Lincoln R.A. and Gish H.
"Statistical delta modulation"
Proceedings I.E.E.E., Vol. 55, No. 3, March 1967
pages 308 - 319

(4) Bergeron J.R.
"Controlled slope delta modulation"
Telecommunications Vol. 3, No. 12, December 1969
pages 31 - 33

(5) Bolder J.C. and Dramer C.
"Video transmission by delta modulation using tunnel diodes"
Proceedings I.R.E. Vol. 50, No. 4, April 1962
pages 428 - 431

BIBLIOGRAPHY (Continued)

(6) Bowers F.K.

"What use is delta modulation to the transmission Engineer"

A.I.E.E. transactions on communication and electronics, Vol. 76, May 1957

pages 142 - 147

(7) Deschenes P.A. and Villeret

"A continuous delta modulator and a numerical converter for an integrated telecommunications network"

I.E.E.E. International Conference Communications Record, Part 7, 1970

pages 27 - 32

(8) Donaldsen R.W. and Douville R.J.

"Analysis, subjective evaluation, optimization and comparison of the performance capabilities of PCM, DPCM, DM, AM, and PM voice communication systems"

I.E.E.E. Transactions on communication technology, Vol. Com. No. 4, August 1969

(9) Emoto O., Tomozawa A., Katayama H., Kaneko H. and Dekimoto T.

"An experimental high speed electronic switching system using delta modulation".

I.E.E.E. International Convention Record, Part 1, 1965

pages 41 - 52

BIBLIOGRAPHY (Continued)

(10) Gatland H.B.
"Transport lag simulator using delta type modulation"
I.F.A.C. Symposium, Sydney 1968

(11) Goodman D.J.
"Delta modulation grannular quantization noise"
Bell. Sys. Tech. J., Vol. 48, No. 5, May - June 1969
pages 1197 - 1218

(12) Greefkes J.A.
"A digitally companded delta modem for speech transmission"
I.E.E.E. International Conference Communications Record,
Part 7, 1970
pages 73 - 48

(13) Haliyak C.A. and Tripp J.S.
"A deterministic study of delta modulation"
I.E.E.E. International Conference Record, Part 8, 1963
pages 247 - 259

(14) Inosi H. and Yasuda Y.
"A unity bit coding method by negative feedback"
I.E.E.E. Proceedings, November 1963
pages 1524 - 1535

(15) Jayant N.S.
"Adaptive delta modulation with 1 bit memory"
Bell. Sys. Tech. J., Vol. 49, March 1970
pages 321 - 342

BIBLIOGRAPHY(Continued)

(16) Johnson F.B.
"Calculating delta modulation performance"
I.E.E.E. Transactions Audio and Electronic, Vol. AU 16,
No. 1, March 1968

(17) Lender A. and Kozuch M.
"Single bit delta modulation system"
Electronics, Vol. 34, November 1961
pages 125 - 129

(18) McKibbin J. and Stradling J.B.M.
"The use of delta modulation in pulse transmission"
Electrical Engineering Transaction I.E. (Aust.)
March 1970

(20) Miyakawa H. and Matuaka T.
"Predictive transformation of binary sequences obtained
by delta modulation"
Electronics and Communication in Japan, Vol. 49, No. 11,
November 1966
pages 183 - 190

(21) Petford B. and Clarke C.M.
"A companded delta speech digitizer"
I.E.E. Conference Publication, No. 64, May 1970
pages 59 - 63

BIBLIOGRAPHY (Continued)

(22) Protonotarios E.N.

"Slope overload noise in delta pulse code modulation systems"

Bell. Sys. Tech. J., Vol. 46, November 1967

pages 2119 - 2161

(23) Schouten J.F., De Jager F. and Greefkes J.A.

"Delta modulation, a new modulation system for telecommunications"

Philips Technical Review, Vol. 13, 1952

pages 237 - 245

(24) Hosakawa S.

"Ternary delta modulation"

Electronics and Communications in Japan, Vol. 49, No. 11

November 1966

page 174

(25) Van de Weg H.

"Quantizing noise of a single integration delta modulation system with an N digit code"

Philips Research Report, No. 8 1953

pages 367 - 385

(26) Wang P.P.

"Idle channel noise of delta modulation"

I.E.E.E. Transaction Communication Technology,

Vol. Com. 18, October 1968

pages 737 - 742

BIBLIOGRAPHY (Continued)

(27) Wolf J.K.

"Effects of channel errors on delta modulation"

I.E.E.E. Transactions Communications Te hnology,

Vol. Com. 14, No. 1, February 1966

pages 2 - 7

COMPANDING

(1) Norwine A.C.

"Devices for controlling amplitude characteristics of telephone signals"

Bell. Sys. Tech. J., Vol. 17, 1938

page 539