NHS3100W8/A1

Product Qualification Information Package

Rev. 1.0 — Jan 3, 2017 Report

Document information

Info	Content
Keywords	NHS3100W8/A1, RDL with Au-bumps, Temperature monitoring and logging
Abstract	This document summarizes the product qualification information
Report Nr.	Technical database #160853

Revision history

Rev	Date	Author	Description
0.1	Aug 30, 2016	K. Rongen	Draft version
0.2	Sept 13, 2016	K. Rongen	Draft version, POD included, bump and package information added.
0.3	Sept 27, 2016	K. Rongen	Draft, added product orientation on foil and updated industrial flow
1.0	Jan 03, 2017	K. Rongen	Final. Updated wafer orientation on FFC and emap-label.

Contact information

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2015. All rights reserved.

Contents

1.	**Introduction**	**4**
1.1	Device description	4
1.2	Order Numbers	4
1.3	Features and Benefits	4
1.3.1	System	4
1.3.2	Memory	4
1.3.3	Digital peripherals	4
1.3.4	Analog peripherals	5
1.3.5	Communication interfaces	5
1.3.6	Clock generation	5
1.3.7	Power control	5
1.3.8	Unique device serial number for identification	5
1.3.9	Target Applications	5
1.3.10	Package	5
1.4	Data Sheet	5
2.	**Manufacturing Locations**	**6**
2.1	Industrial flow	7
3.	**Product Data**	**7**
3.1	Die	7
3.2	Package description	8
3.3	Product Application	8
4.	**Reliability Qualification**	**8**
4.1	Qualification results	8
4.2	Reliability figures (ELFR & IFR)	9
4.2.1	Early Failure rate	9
4.2.2	Intrinsic Failure rate	10
4.2.3	Results of reliability figures	10
5.	**Marking Information**	**11**
6.	**Package**	**12**
6.1	Package Outline	12
6.2	Bump layout	13
7.	**Outline Packing**	**14**
7.1	Packing method for products in tape and reel	14
7.2	Barcode labeling	15
7.3	Wafer on foil	16
8.	**Chemical Content**	**16**
9.	**Legal information**	**17**
9.1	Definitions	17
9.2	Disclaimers	17
9.3	Licenses	17
9.4	Patents	17
9.5	Trademarks	17

All information provided in this document is subject to legal disclaimers.
© NXP B.V. 2015. All rights reserved.

1. Introduction

1.1 Device description

<Quoted from datasheet rev.5; January 2017>

The NXP NHS3100W8/A1 is an IC optimized for temperature monitoring and logging. With its embedded NFC interface, internal temperature sensor and direct battery connection, it supports an effective system solution with a minimal number of external components.

The embedded ARM Cortex-M0+ offers flexibility to the users of this IC to implement their own dedicated solution. The NHS3100W8/A1 contains multiple features, including multiple power-down modes and a selectable CPU frequency of up to 8 MHz, for ultra-low power consumption.

Users can program this NHS3100W8/A1 with the industry-wide standard solutions for ARM.

1.2 Order Numbers

12 NC Number	Orderable part # Cats type	Package type: Reel/ Tube/ Tray/ Quantity
9353 089 67005 SOT1870_1	NHS3100W8/A1	PM SAWN 8 INCH WAFER ON FFC. **Minimum wafers sent: 1**

1.3 Features and Benefits

<Quoted from datasheet>

1.3.1 System

- ARM Cortex-M0+ processor running at frequencies of up to 8 MHz
- ARM Cortex-M0+ built-in Nested Vectored Interrupt Controller (NVIC)
- ARM Serial Wire Debug
- System tick timer
- IC reset input

1.3.2 Memory

- 32 kB on-chip flash programming memory
- 4 kB on-chip EEPROM of which 256 bytes can be write protected
- 8 kB SRAM

1.3.3 Digital peripherals

- Up to 4 General-purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors
- GPIO pins which can be used as edge and level sensitive interrupt sources
- High-current drivers/sinks (20 mA) on two pins
- Programmable watchdog timer (WDT)

All information provided in this document is subject to legal disclaimers.
© NXP B.V. 2015. All rights reserved.

1.3.4 Analog peripherals

- Temperature sensor with +/-0.3 °C absolute temperature accuracy between 0 °C and 40 °C and +/-0.5 °C in the range between -40 and +85 °C

1.3.5 Communication interfaces

- NFC/RFID ISO 14443 type A interface

1.3.6 Clock generation

- 8 MHz internal RC oscillator, trimmed to 2 %, accuracy, which is used for the system clock
- Timer oscillator operating at 32 kHz linked to the RTC Timer unit

1.3.7 Power control

- Support for 1.72 V – 3.6 V external voltages
- The NHS3100 can also be powered from the NFC field
- Activation via NFC possible
- Integrated Power Management Unit (PMU) for versatile control of power consumption
- Four reduced power modes for ARM Cortex-M0+: Sleep, Deep-sleep, and Deep power-down, Battery-off
- Power gating for each analog peripheral for ultra-low power operation
- < 50 nA IC current consumption in Battery-off mode at 3.0 V
- Power-On Reset (POR)

1.3.8 Unique device serial number for identification

1.3.9 Target Applications

- Temperature measurement
- Temperature logging
- Cold chain validation

1.3.10 Package

- Sawn wafer on foil.

1.4 Data Sheet

Datasheets are available at: http://www.nxp.com/

Version	Date	Document Status
Rev. 5	January, 2017	Data sheet

© NXP B.V. 2015. All rights reserved.

2. Manufacturing Locations

Table 1. Manufacturing Locations

Plant/ Contact	Company and Location
Water diffusion plant	**SSMC**, Taiwan Semiconductor Manufacturing Co.Ltd, Taiwan
Wafer test plant	**NXP Manufacturing**, Kaohsiung, Taiwan
Assembly plant	**Chipbond**, Hsinchu Taiwan
Final test plant/location	**NXP Manufacturing**, Kaohsiung, Taiwan
Quality Responsibility	**NXP Semiconductors** Nijmegen, The Netherlands
Quality Contact	**Jan Wijers** NXP Semiconductors Halfgeleiderweg 6, 6534 AV Nijmegen, The Netherlands Building BZ Email: jan.wijers@nxp.com

All information provided in this document is subject to legal disclaimers.
© NXP B.V. 2015. All rights reserved.

2.1 Industrial flow

The following industrial flow is used for NHS3100W8 product:

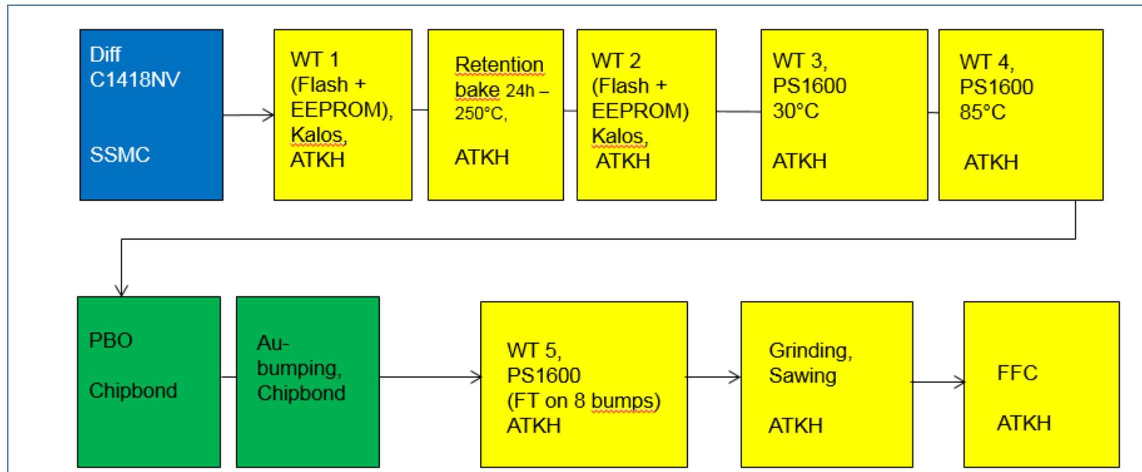

Figure 1: Industrial flow diagram

3. Product Data

3.1 Die

Process	**CMOS14NV, 6LM flash memory, 3VT (Std, LL, Ultra High VT), thicker IMD5, planarized passivation**
Minimum dimension	0.16um (gate length)
Wafer size	8 inch
Die thickness	150 µm
Epi (y/n):	Yes, 4 µm epi, 10 ohm*cm
Gate material	poly
Inter-poly isolation material	SiO_2
Gate to metal isolation material	SiO_2 – PSG – TEOS
Metallization	AlCu
Via plug	W
Inter metal isolation material	FSG (E_r =3.9)
Passivation	HDP / SiN
Backside metallization	None

All information provided in this document is subject to legal disclaimers.
© NXP B.V. 2015. All rights reserved.

3.2 Package description

An overview of the package information of the used WLCSP package is given in table below.

Package type	Bumped die with 8 functional bumps. See POD.
Number of bumps / array size	8 / not applicable, see picture
Nominal package dimensions (W*L*t, mm)	2.51 x 2.51 x 0.16 (+/-0.015)
Scribe line (mm)	0.08
Terminal pitch (mm)	See POD
Die size (mm)	2.51 x 2.51 x 0.15 (Including saw lane)
Bump Technology	Au
Interconnect structure (UBM)	TiW / Au
Redistribution Layer	n.a.
Solder ball	n.a.
Bump Height / Bump Diameter [µm]	10 (+/-2) / see POD.
Shelf life of sawn dies on FFC	6 months after sawing process end
Moisture Sensitivity Level (MSL)	n.a.
Dry pack	n.a.

3.3 Product Application

There is a specific Application Note on the NXP-website for this product, AN11657.

4. Reliability Qualification

4.1 Qualification results

Table 2. Qualification Results

Test description	Test conditions / requirements	# Lots	# Samples / Lot	Result
Electrical robustness tests				
ESD-HBM	2000V (required) 2500V (target)	1 1	9 9	PASS on structural PASS similar type
ESD-CDM	500V (required) 650V (target)	1 1	3 3	PASS on structural PASS similar type
Latch up	Vdd_{max} ±100mA @85°C	1	18	PASS on structural similar type
Characterization	(-40/85°C)	1	1	PASS

 © NXP B.V. 2015. All rights reserved.

Product Reliability tests					
THNB	*Ta = 85°C / 85% RH, no bias*	***300 h***	3	80	PASS on structural similar type
UHST on wafer	*Ta = 130°C / 85% RH*	***96 h***	1	80	PASS
		192 h	1	80	PASS
TMCL on wafer	*Ta = -65°C to 150°C*	***20 c (required)***	1	77	PASS
		50 c (target)	1	77	PASS
		500 c (extended)	1	77	PASS (Extended read point)
TMCL	*Ta = -40°C to 70°C*	***500 c***	3	80	PASS on structural similar type
HTSL	*Ta = 85 °C*	***500 h***	3	80	PASS on structural similar type
HTOL	*Ta = 150°C*	***1000 h***	1	45	PASS on structural similar type, ceramic pack.
		1000 h	3	45	PASS on structural similar type in WLCSP
Constr. Analysis	Dimensions, visual inspection, ball shear test 0 c		1	45	PASS
	Ball shear test after TMCL 20 c		1	5	PASS
	Ball shear test after TMCL 500 c		1	5	Not pass (Extended read point)
	Cross section after TMCL 20 c		1	1	PASS
	Cross section after TMCL 500 c		1	1	Not pass (Extended read point)
Flash Qualification tests (CMOS14NV-release)					
HTOL SILC (ERPR)	Tj = 150 °C, VDD = 1.2V, 1000h, 10k P/E cls		3	77	PASS on structural similar type
Unbiased Data Retention after Cycling (DRET)	Wafer level, Tj = 150 °C, 1000h 10k P/E cls (10 years)		3	77	PASS on structural similar type
EEPROM Qualification tests (CMOS14NV ee)					
Endurance	Vdd=1.5V, 500k, Vdd=2.0V		3	77	PASS on structural similar type
DRET	500k E/P cyc, 250°C, 168h		3	77	PASS on structural similar type
DIST	Vdd=2.0V, 16M E/P cyc		1	10	PASS on structural similar type

4.2 Reliability figures (ELFR & IFR)

The following reliability figures for ELFR (early failure rate) and IFR (intrinsic failure rates) can be given based on HTOL data of product and wafer level reliability (data generated in waferfab based on test vehicle).

4.2.1 Early Failure rate

The onset of the failure rate curve is manifested by an initially high - but rapidly decreasing - failure rate. The Early Failure Rate (EFR), sometimes referred to as Infant Mortality Failures (IMF) or Early

© NXP B.V. 2015. All rights reserved.

Life Failures (ELF), represents a small fraction of the population of components which contain defects that are not immediately fatal, but will cause failure in a relatively short time interval.
Failures can originate from weak products with macroscopic defects.
The early failure rate level can be assessed based on reliability qualification and reliability monitoring data. The early failure rate is expressed in FPM (Fails per Million). The formula used to calculate Early Failure Rate, is as follows:

$$EFR = \frac{n_c(n) * 10^6}{N} \quad [FPM]$$

Where:
- EFR = Early Failure Rate [FPM]
- n = Observed total number of failures during the test
- $n_c(n)$ = Corrected number of failures (Using a 60 % confidence level using Poisson statistics)
- N = Number of units tested

The High Temperature Operating Life test data is used to assess the EFR.
The calculations of failure rate are in line with JEDEC standard JESD85.

4.2.2 Intrinsic Failure rate

The flat portion of the failure rate curve consists of random failures and the failure rate is relatively constant. This is the behavior observed in large populations of mature components and is commonly referred to as the useful life of the product. It consists of random failures due to external circumstances and is significantly impacted by the product robustness (for example ESD rating).
The intrinsic failure rate (IFR) is usually expressed by the Failure-In-Time (1 FIT: 1 failure in 1 billion device hours of operation). The formula used to calculate Intrinsic Failure Rate, expressed in FITs, is as follows:

$$IFR = \frac{n_c(n) * 10^9}{N * t * A} \quad [FIT]$$

Where:
- IFR = Intrinsic Failure Rate [FIT]
- n = Observed total number of failures (excluding early failures)
- $n_c(n)$ = Corrected number of failures (Using a 60% confidence level using Poisson statistics)
- N = Number of units tested
- t = Duration of test at elevated temperature in hours
- A = Arrhenius acceleration factor (E_a = 0.7eV, T_{ref} = 55°C).

The mean time to failure (MTTF) is given by:

$$MTTF = \frac{10^9}{\text{Intrinsic Failure Rate}} \quad [Hrs]$$

Calculation is based on the High Temperature Operating Life test data.
The calculations of failure rate are in line with JEDEC standard JESD85.

4.2.3 Results of reliability figures

Following results have been generated in 2015 which are valid for NHS3100W8/A1.

Failure rate	**Value**
PPM	<300
FIT	*<5*

 © NXP B.V. 2015. All rights reserved.

5. Marking Information

The devices are not marked.

For each wafer on foil, an eMAP-label can be downloaded to identify good and bad devices in a wafer map.

© NXP B.V. 2015. All rights reserved.

6. Package

6.1 Package Outline

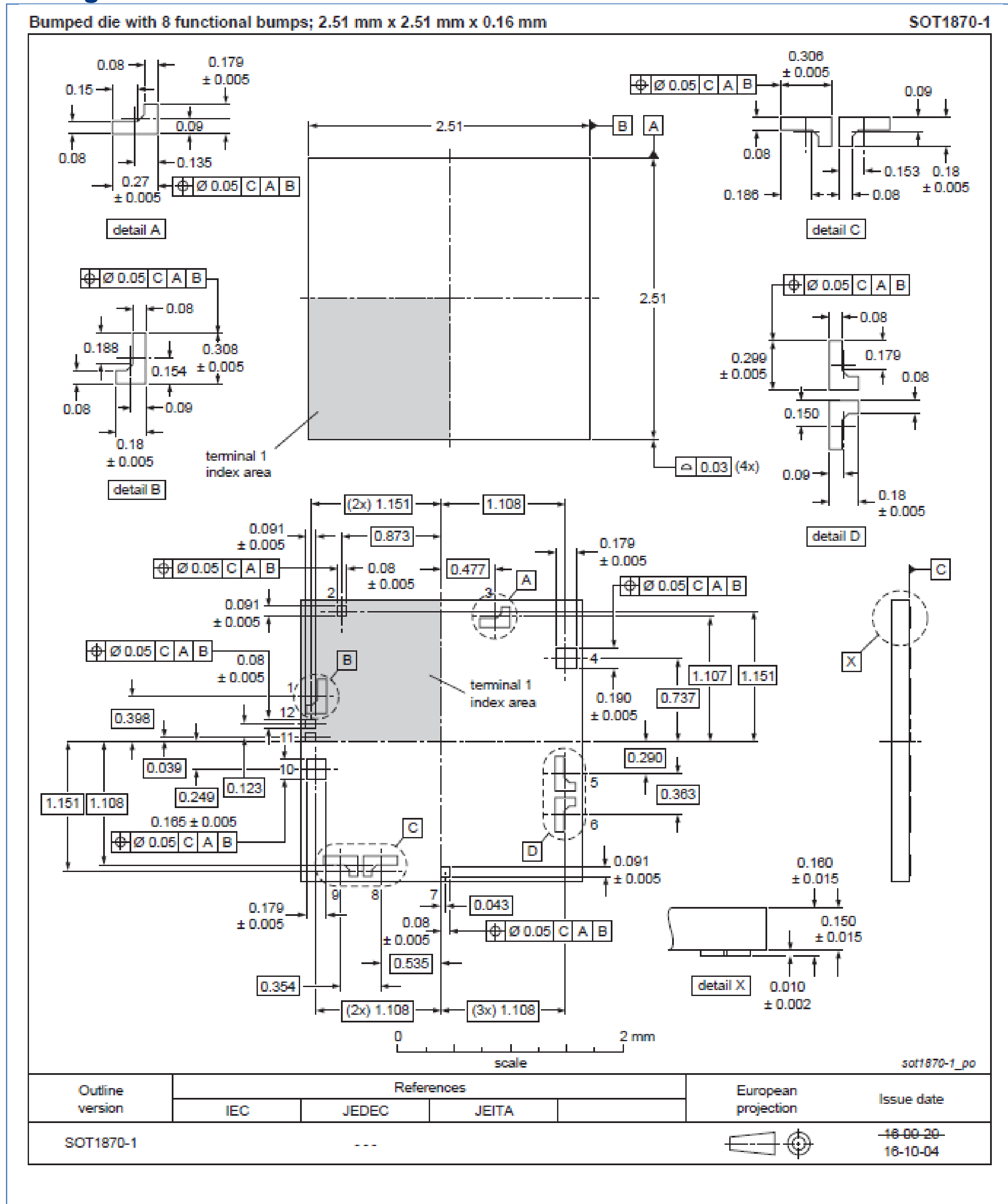

Figure 2: Package Outline NHS3100W8

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2015. All rights reserved.

6.2 Bump layout

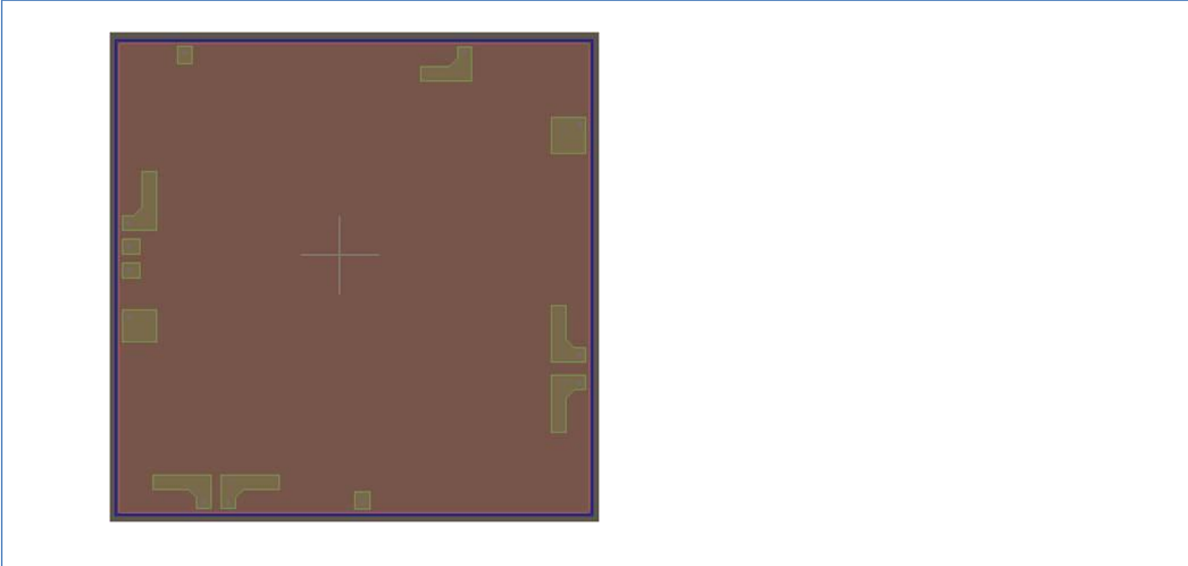

Figure 3: Bump Layout NHS3100W8

© NXP B.V. 2015. All rights reserved.

7. Outline Packing

7.1 Packing method for products in tape and reel

Package version	12NC	PQ (pcs)	Inner Box dimensions l x w x h (mm)	Outer Box dimensions l x w x h (mm)
8"-FFC-A	3322 845 08351 SOT1870_1	net printed dies per wafer: 4409	3422 135 21407 290 x 290 x 25	3422 135 21411 290 x 290 x 125

Smallest Packing Quantity: 1 wafer (sales item NC ending 005)

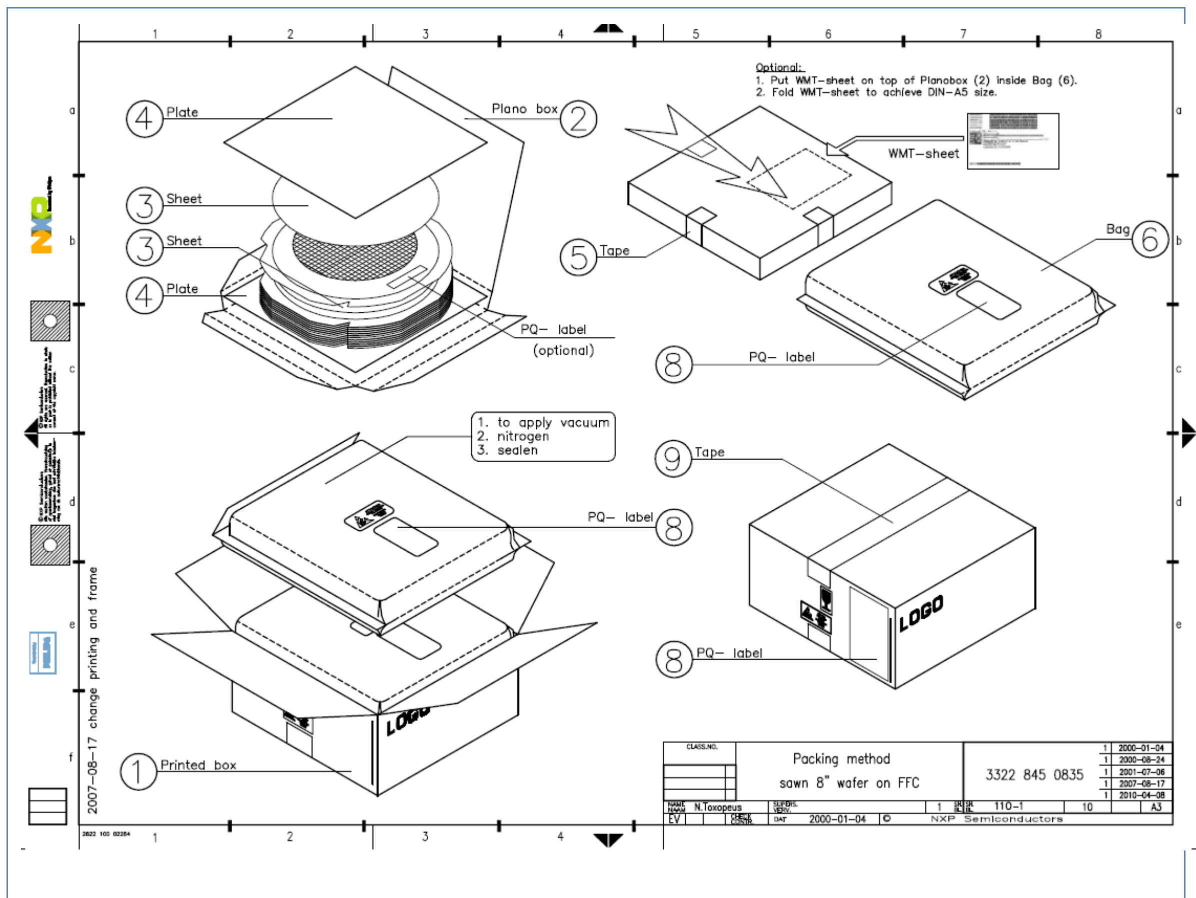

Figure 4: Schematic view of wafer on foil in a box

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2015. All rights reserved.

7.2 Barcode labeling

Below, the PQ label is shown that will be fixed on the FFC bag, the inner and the outer box.

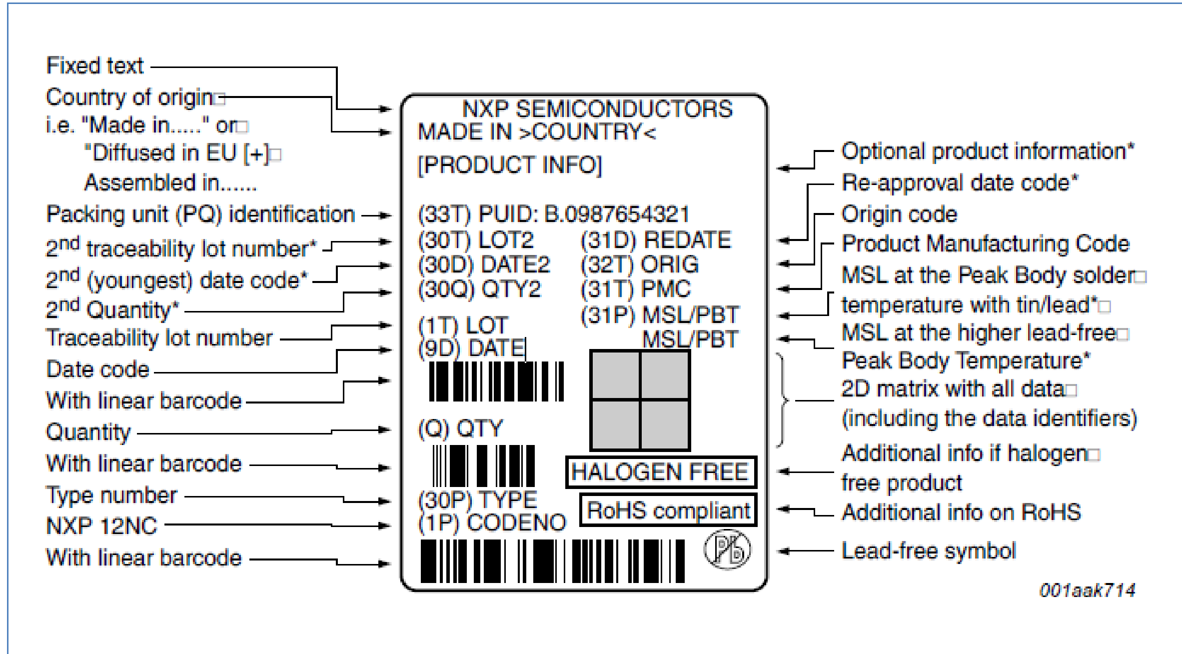

Figure 5: Example PQ label

Besides the PQ label, an additional sticker for emap-notification of each wafer is placed on the relevant inner box. Here, the WMT-webservice link for login and the required authorization key can be found.

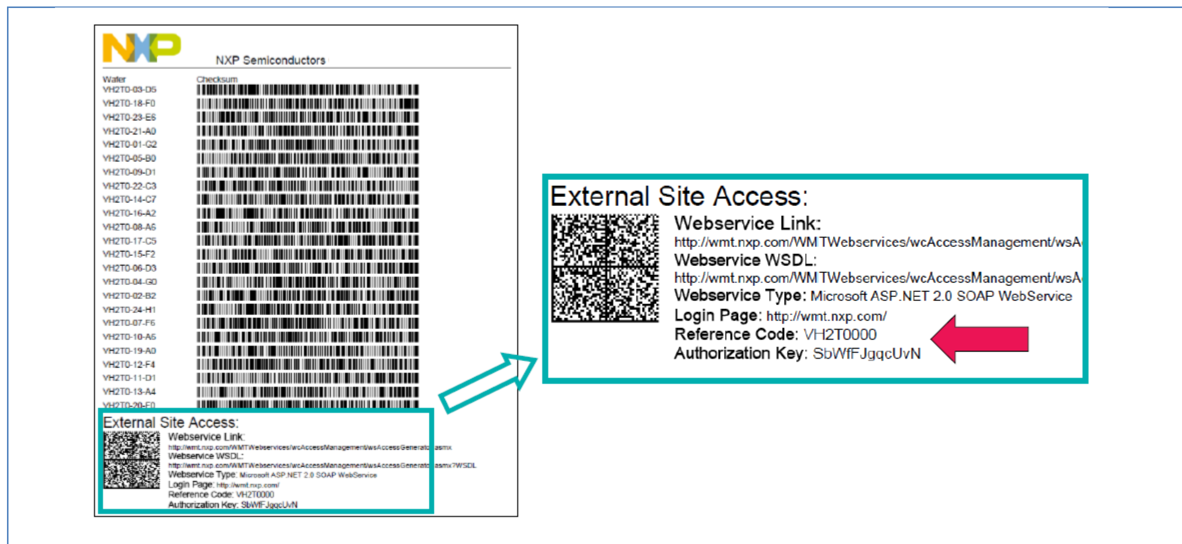

Figure 6: Example WMT label on inner box

 © NXP B.V. 2015. All rights reserved.

7.3 Wafer on foil

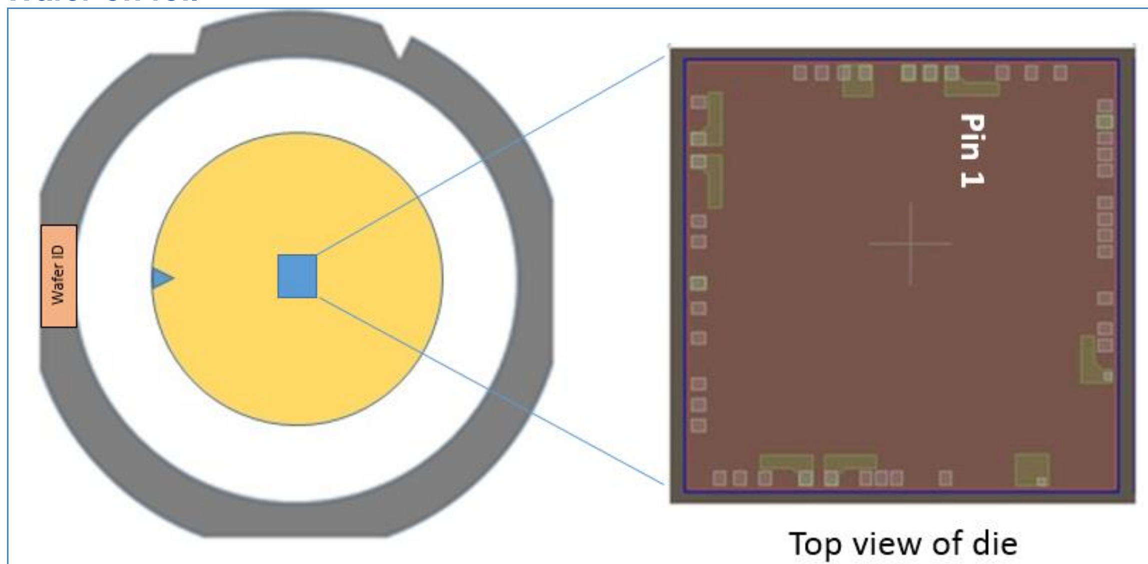

Figure 7: Product orientation on foil

The wafer has a 90 degree rotation with respect to the FFC, as shown in Fig.7. The FFC-ring is plastic.

8. Chemical Content

The product meets ROHS compliance. NXP's ROHS declaration and chemical content information can be found on the NXP website at http://www.nxp.com/chemical-content/search:

Table 3. Chemical content

Name of Component	Material group	Substances (Element)	CAS Number	Material Mass (mg)	Material Mass (%)
Die	Doped silicon	Silicon wafer (Si)	7440-21-3	2.22568	97.93
Repassivation	PBO (HD8820)	Polymer	Proprietary	0.04099	1.80
UBM	metallization	TiW (titanium, wolfram)	7440-326: Ti 7440-337: W	0.00018	0.01
		Au (gold)	7440-57-5	0.00005	0.02
Bump	Plated Au	Au (gold)	7440-57-5	0.00572	0.25
NHS3100W8/A1				2.27 mg	100%

 © NXP B.V. 2015. All rights reserved.

9. Legal information

9.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

9.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

9.3 Licenses

Purchase of NXP <xxx> components
<License statement text>

9.4 Patents

Notice is herewith given that the subject device uses one or more of the following patents and that each of these patents may have corresponding patents in other jurisdictions.

<Patent ID> — owned by <Company name>

9.5 Trademarks

Notice: All referenced brands, product names, service names and trademarks are property of their respective owners.

<Name> — is a trademark of NXP B.V.

© NXP B.V. 2015. All rights reserved.