



Description

JMT N-channel Enhancement Mode Power MOSFET

Features

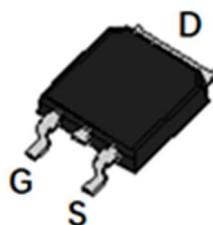
- 40V, 160A
- $R_{DS(ON)} < 4.5\text{m}\Omega$ @ $V_{GS} = 10\text{V}$
- Lead free and Green Device Available
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead free product is acquired

Application

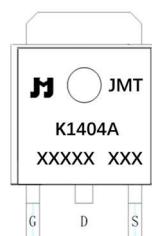
- Load Switch
- PWM Application
- Power management



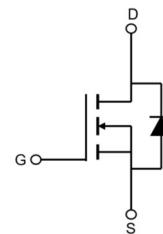
100% UIS TESTED!
100% ΔV_{ds} TESTED!



TO-252(DPAK) top view



Marking and pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
JMTK1404A	JMTK1404A	TAPING	TO-252	13inch	2500	25000

Absolute Maximum Ratings ($T_c=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter		Max.	Units
V_{DSS}	Drain-Source Voltage		40	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current	$T_c = 25^\circ\text{C}$	160	A
		$T_c = 100^\circ\text{C}$	104	A
I_{DM}	Pulsed Drain Current ^{note1}		640	A
E_{AS}	Single Pulsed Avalanche Energy ^{note2}		225	mJ
P_D	Power Dissipation	$T_c = 25^\circ\text{C}$	174	W
R_{eJC}	Thermal Resistance, Junction to Case		0.86	$^\circ\text{C}/\text{W}$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +175	$^\circ\text{C}$

**Electrical Characteristics** ($T_J=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=40\text{V}$, $V_{GS}=0\text{V}$,	-	-	1.0	μA
I_{GSS}	Gate to Body Leakage Current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2.0	2.7	4.0	V
$R_{DS(\text{on})}$	Static Drain-Source on-Resistance note3	$V_{GS}=10\text{V}$, $I_D=30\text{A}$	-	3.4	4.5	$\text{m}\Omega$
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS}=20\text{V}$, $V_{GS}=0\text{V}$, $f=1.0\text{MHz}$	-	5530	-	pF
C_{oss}	Output Capacitance		-	590	-	pF
C_{rss}	Reverse Transfer Capacitance		-	460	-	pF
Q_g	Total Gate Charge	$V_{DS}=20\text{V}$, $I_D=30\text{A}$, $V_{GS}=10\text{V}$	-	117	-	nC
Q_{gs}	Gate-Source Charge		-	32	-	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	40	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=20\text{V}$, $I_D=30\text{A}$, $R_L=1\Omega$, $R_{\text{GEN}}=3\Omega$, $V_{GS}=10\text{V}$	-	35	-	ns
t_r	Turn-on Rise Time		-	88	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	115	-	ns
t_f	Turn-off Fall Time		-	112	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	160	-	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	640	-	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS}=0\text{V}$, $I_S=30\text{A}$	-	-	1.2	V
t_{rr}	Body Diode Reverse Recovery Time	$T_J=25^\circ\text{C}$, $I_F=20\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$	-	20	-	ns
Q_{rr}	Body Diode Reverse Recovery Charge		-	10	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: $T_J=25^\circ\text{C}$, $V_{DD}=20\text{V}$, $R_G=25\Omega$, $L=0.5\text{mH}$, $I_{AS}=30\text{A}$ 3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$

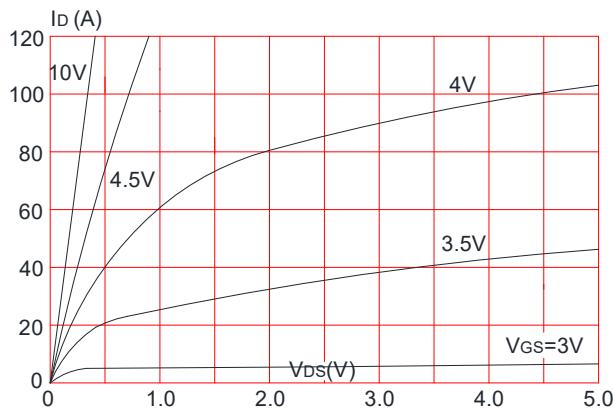
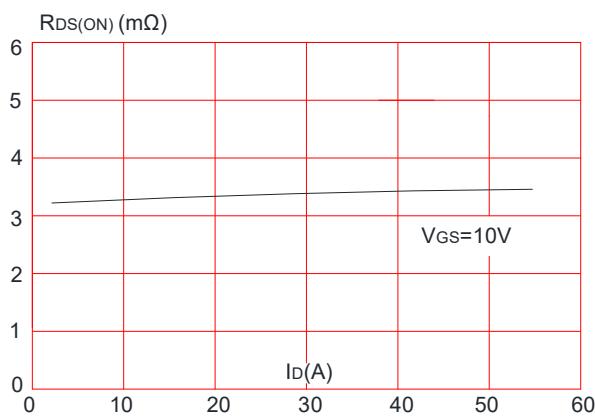
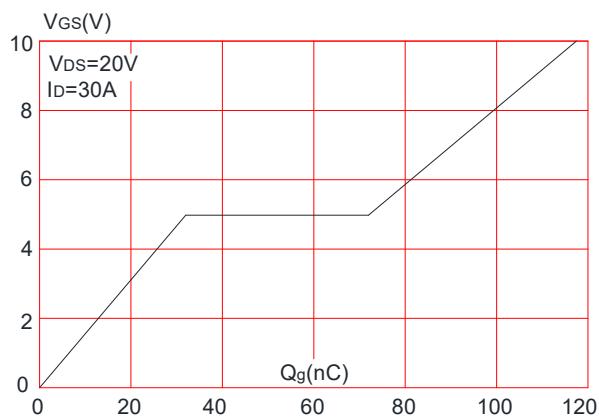
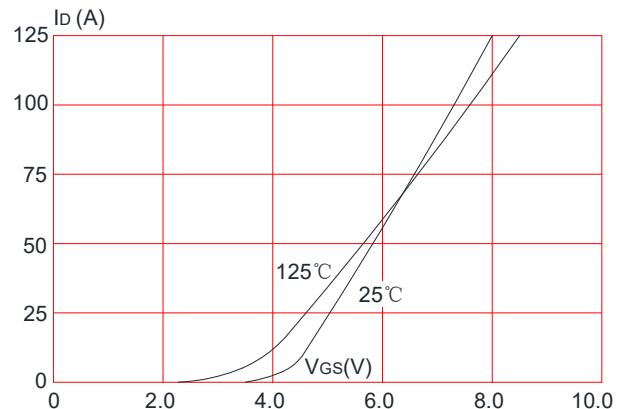
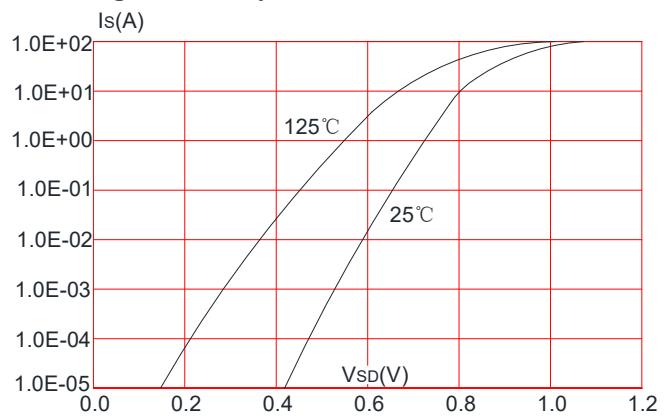
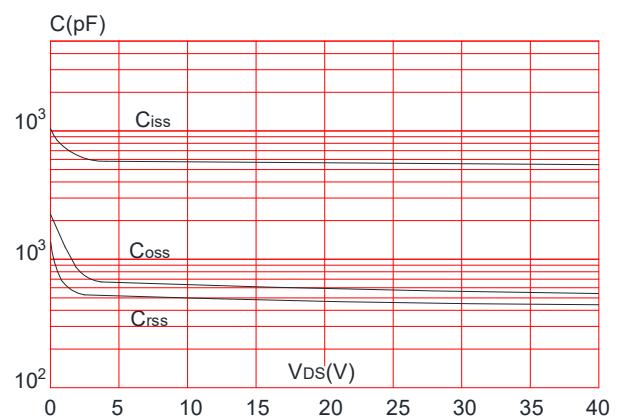
Figure1: Output Characteristics

Figure 3: On-resistance vs. Drain Current

Figure 5: Gate Charge Characteristics

Figure 2: Typical Transfer Characteristics

Figure 4: Body Diode Characteristics

Figure 6: Capacitance Characteristics


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

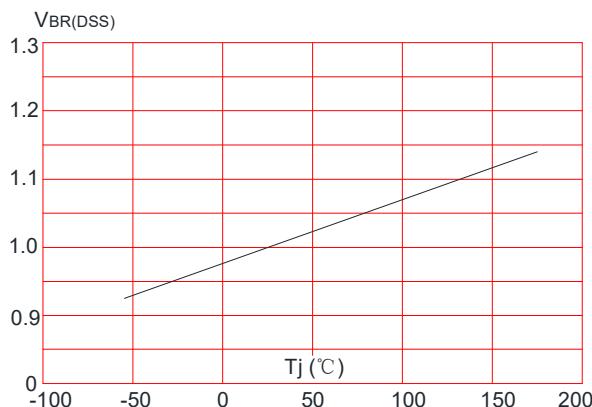


Figure 8: Normalized on Resistance vs. Junction Temperature

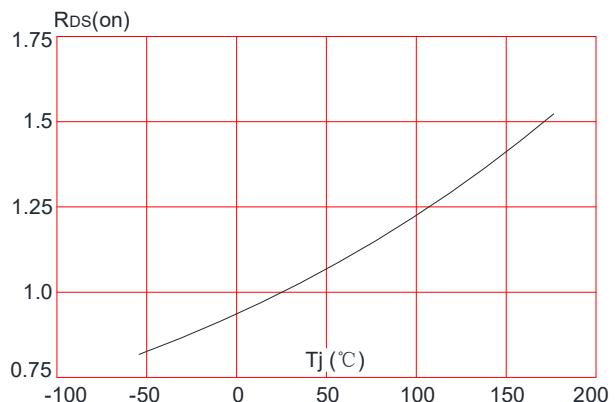


Figure 9: Maximum Safe Operating Area

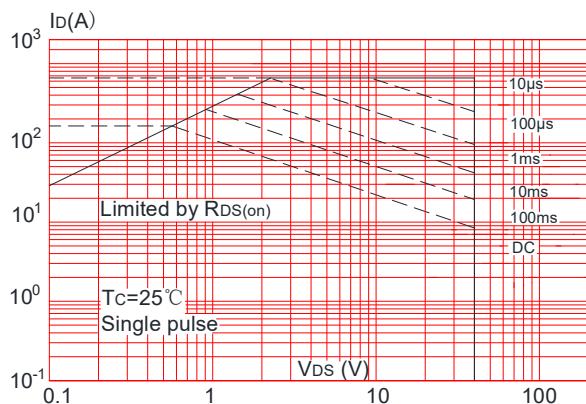


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

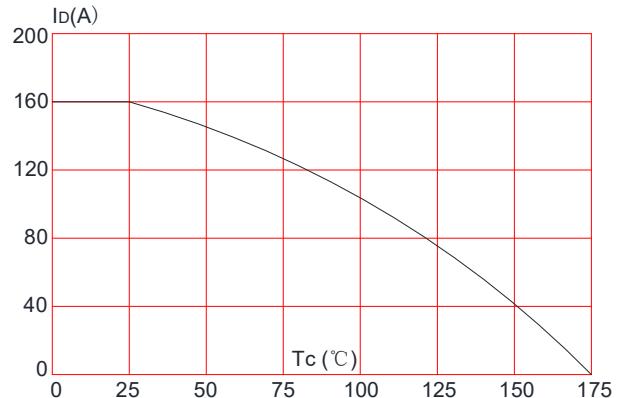
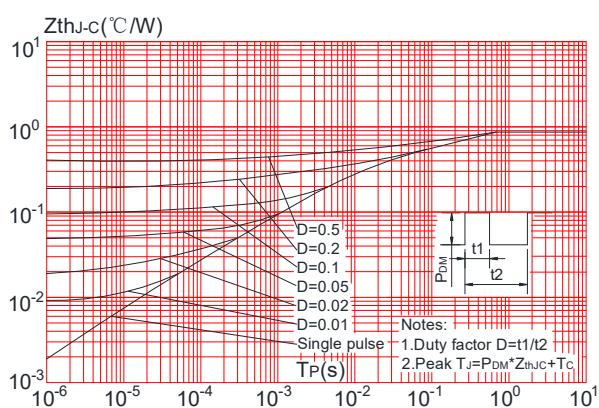


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Case



Test Circuit



Figure1:Gate Charge Test Circuit & Waveform

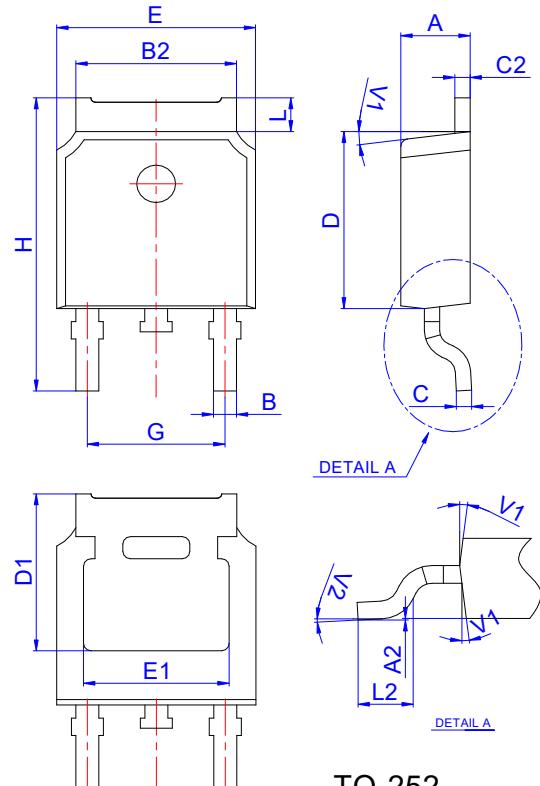


Figure 2: Resistive Switching Test Circuit & Waveforms



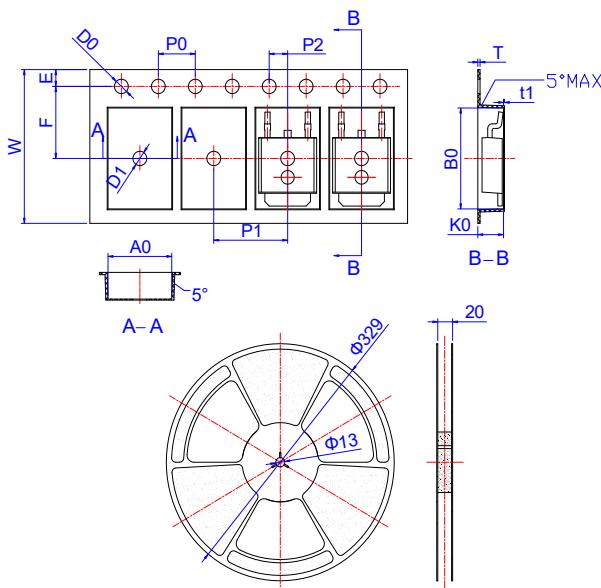
Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms

Package Mechanical Data-TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10			2.50	0.083	
A2	0			0.10	0	
B	0.66			0.86	0.026	
B2	5.18			5.48	0.202	
C	0.40			0.60	0.016	
C2	0.44			0.58	0.017	
D	5.90			6.30	0.232	
D1	5.30REF			0.209REF		
E	6.40			6.80	0.252	
E1	4.63				0.182	
G	4.47			4.67	0.176	
H	9.50			10.70	0.374	
L	1.09			1.21	0.043	
L2	1.35			1.65	0.053	
V1		7°				7°
V2	0°			6°	0°	
						6°

Reel Specification-TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24			0.27	0.009	
t1	0.10				0.004	
10P0	39.80	40.00	40.20	1.567	1.575	1.583



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