# PCI Express® 5.0 EDSFF Interposer CrossSync Capable User Manual and *Quick Start Guide*

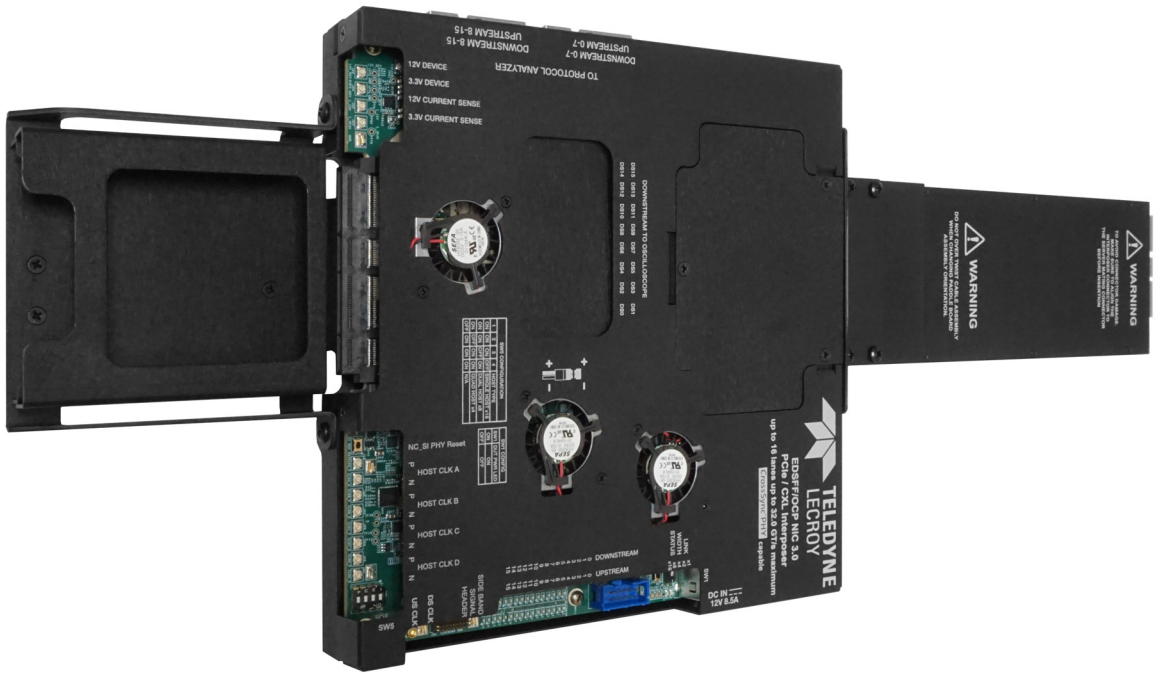
Use this document for quick installation and setup.

## 1 Introduction

Teledyne LeCroy's PCI Express 5.0 EDSFF Interposer provides a quick and simple means for protocol analysis of EDSFF form factor Solid State Drives (SSDs) based on PCI Express protocols. The PCI Express 5.0 EDSFF Interposer Card, used with a Summit T5 Protocol Analyzer, enables PCIe bus traffic between a host backplane and EDSFF form factor SSD device to be monitored, captured, and recorded for protocol analysis. The interposer supports data rates of 2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s and 32 GT/s side band signals such as PERST#, CLKREQ# and SMBus (SMBCLK, SMBDAT). The interposer supports link widths up to x16.

This interposer can be upgraded to support the CrossSync PHY feature allowing cross-triggering with a Teledyne LeCroy scope and sample high speed serial signals while simultaneously being recorded by the protocol analyzer.

The interposer is shipped with a mounting bracket that supports installation of different brackets to hold "thin" and "thick" devices with different form factors (E1.S x4, E1.S x8, E1.L, and E3).




**PCI Express 5.0 E3 EDSFF Interposer (PE240UIA-X)**

## 2 Components

The interposer package includes the following components:

- PCI Express 5.0 EDSFF Interposer
- DC Power Adapter (+12V @ 8.5A)
- Vertical Support Brackets and Screws
- User Manual and Quick Start Guide (this document)

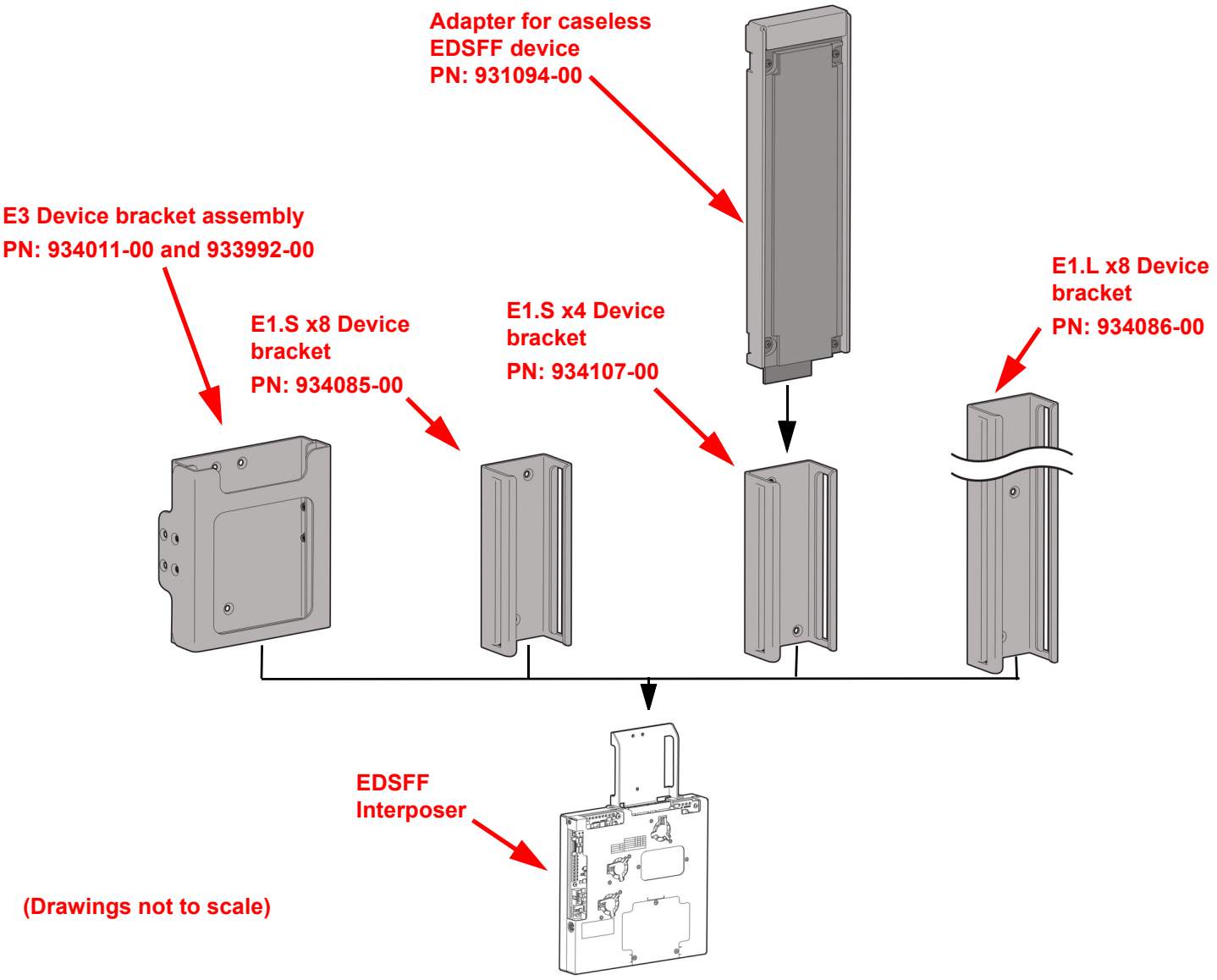
Depending on Configuration (PE240UIA-X, PE241UIA-X, PE243UIA-X):

- E3 Device Bracket Assembly
- E1.S x8 Device Bracket
- E1.L Device Bracket
- E1.S x4 Device Bracket
- Adapter for Caseless EDSFF device and 4 screws
- 4 flat head screws for mounting bracket
- 3 flat head screws for device adapter bracket

Inspect the received shipping container for any damage. Unpack the container and account for each of the system components listed on the accompanying packing list. Visually inspect each component for absence of damage. In the event of damage, notify the shipper and Teledyne LeCroy. Retain all shipping materials for shipper's inspection.

## 3 Brackets and Adapters

Select the appropriate brackets for your application and install in the DUT side of interposer following the steps in section 4.

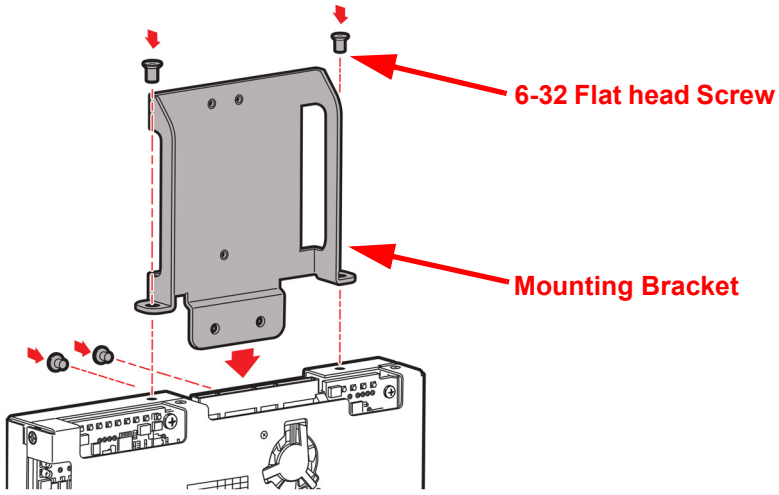



## 4 Bracket Installation

If not installed already, follow the steps below to attach the appropriate bracket on to the DUT side of the interposer:

1. Locate the mounting bracket and 4 screws.
2. If there is already another device bracket installed in the mounting bracket, remove it using a Phillips head screw driver.
3. The mounting bracket must be inserted into the Interposer very carefully with the four holes in the bracket aligned with the four holes in the Interposer.
4. Attach the mounting bracket to the EDSFF Interposer using the supplied four flat head screws from the sides and the bottom. See figures below.

**Top Side of Interposer**



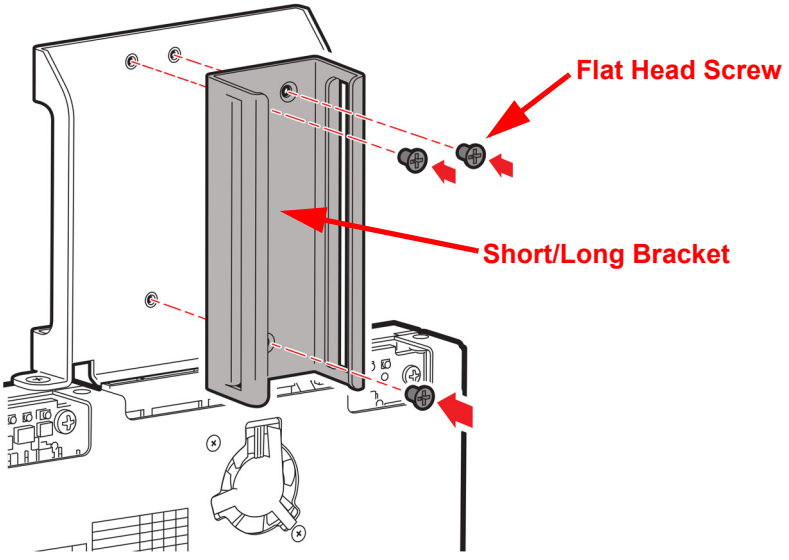

**Carefully align the bracket properly and use the four screws.**

**Slide outside feet underneath PCB and secure with the four screws.**

5. Place short or long bracket against mounting bracket and secure with three flat head screws.

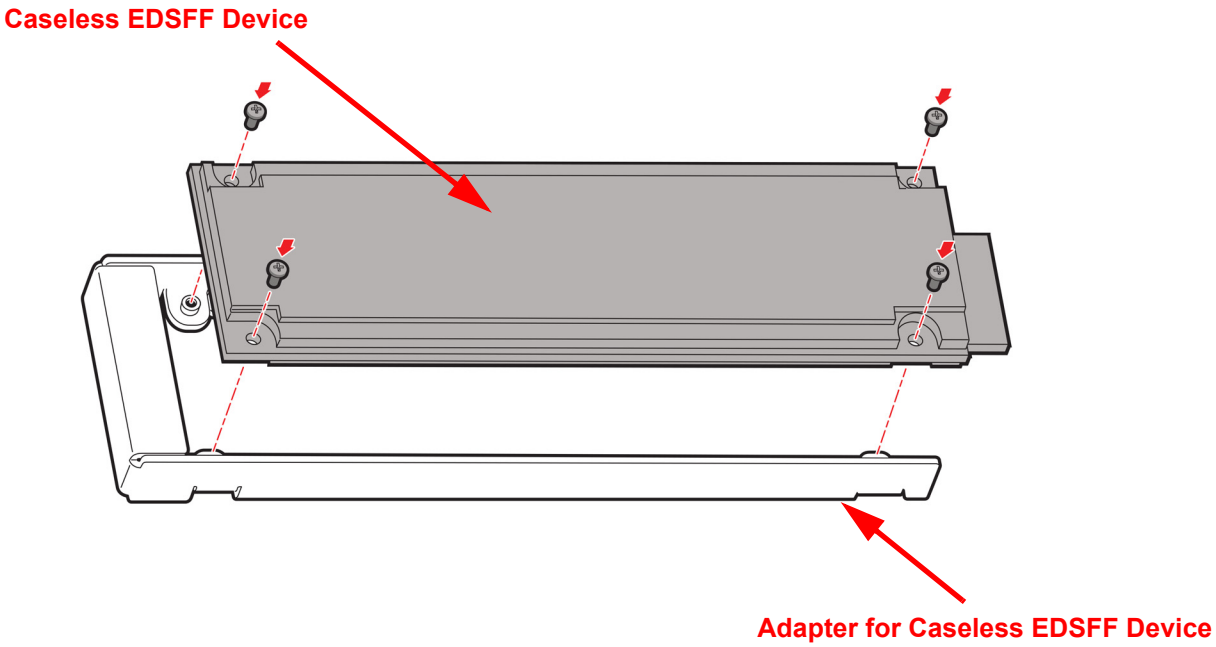
.

**Top Side of Interposer**

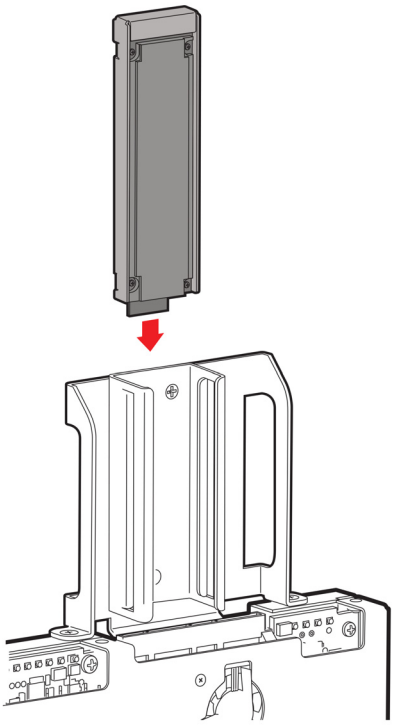



**Align the bracket properly and use the three screws**

An optional adapter is provided for a caseless EDSFF device. The caseless device needs to be secured to the adapter before it can slide in to the device bracket on the interposer. Attach the caseless EDSFF Device to the adapter using a Phillips-head screwdriver and the four (4) supplied screws.




Slide the assembled adapter and device in to the device bracket side of the interposer.



# 5 Connections

Perform the following steps to connect the Interposer (see the image below):

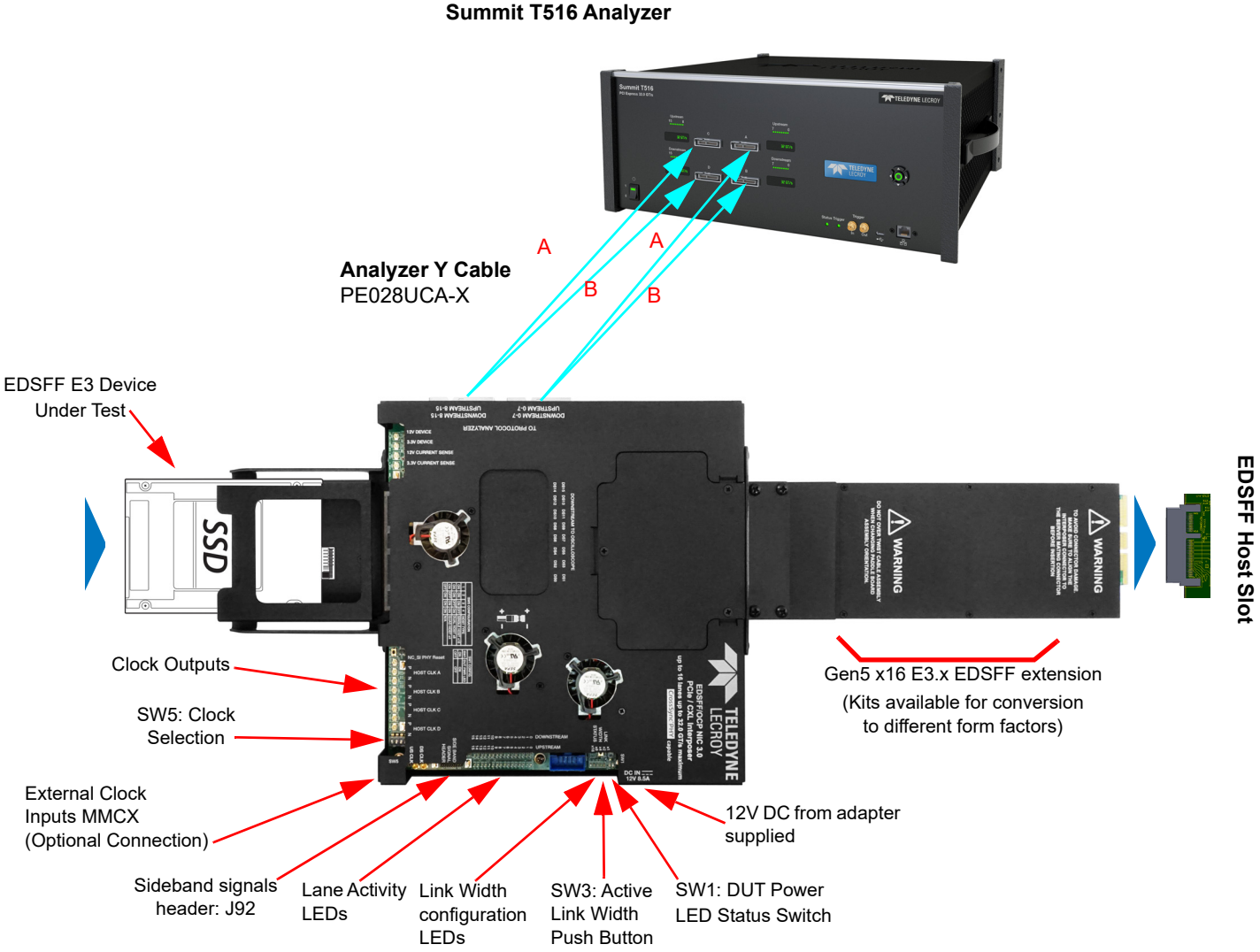
1. Set the SW5 DIP switch to the desired positions to set the clock selection for SINGLE HOST x16,DUAL HOST x8,QUAD HOST x4 Configuration according to the table above (see Section “6” on page viii).
   2.Slide the EDSFF memory device into the device bracket and carefully push it into its mating connector on the EDSFF Interposer. If the device under test is a caseless device make sure to have installed the caseless adapter.
3. Connect the first Gen5 to Gen5 x8 Y cable (PE028UCA-X) to the DS,US [0:7] Connector.
   a.Connect the cable connector labeled B to the connector B on the Summit T516.
   b.Connect the cable connector labeled A to the connector A on the Summit T516.
4. Connect the second Gen5 to Gen5 x8 Y cable (PE028UCA-X) to the DS,US[8:15] connector on the interposer.
   a. Connect the cable connector labeled B to the connector D on the Summit T516.
   b. Connect the cable connector labeled A to the connector C on the Summit T516.
5. Connect the analyzer to a host computer system using the USB port on the front panel of the Summit analyzer.
6. If not already done, install the PCIe Protocol Analysis software on the host machine.
7. Connect 12V DC using the AC adapter supplied with the interposer. Make sure that the AC adapter is powered on.
8. Power on the analyzer.
9. Launch the PCIe Protocol Analysis application, setup the appropriate recording options and start a recording. For more information see the Summit T5 PCI Express Multi-Lane Protocol Analyzer User Manual, 5.0 EDSFF Interposer Configurations.
10. Install the Interposer into the host system connector.
11. Power on the host machine.
12. Use the PCIe Protocol Analysis application to monitor, record and view PCI Express traffic passing through the 5.0 EDSFF Interposer.

**Notes:**

- For step 9, if testing for hot plug, run recording first from the PCIe Protocol Analysis software then install the interposer into the host system connector. For more connection examples see the *Summit T5 PCI Express Gen5 User Manual*.

We are continuously improving and releasing new products. For new interposers to operate optimally always check the Teledyne LeCroy website for the latest version of the PCIe Protocol Analysis Software.

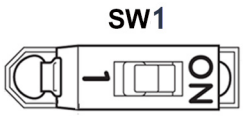
## Connecting the PCI Express 5.0 EDSFF Interposer to a Summit T516 Analyzer



# 6 Clock Selection and other Switch Settings

## SW1: DUT Power LED Status Switch

This switch connects the DUT power Indication LED to the bus power. It is located near the DC In connector.

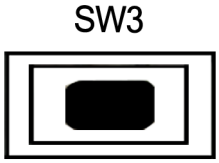



**SW1: DUT Power LED Status Switch**

| | |
|---|---|
| ON | LED Connected (Default) |
| OFF | LED Disconnected |

**Note:** This switch connects the DUT power indication LEDs to the bus power. In some systems with Hot-Plug management the Power Indication LEDs on the interposer may prevent the host system from turning ON bus power to the device, if this happens disconnect the LEDs using SW1 to allow proper bus power operation.

## SW3: Active Width Control Pushbutton

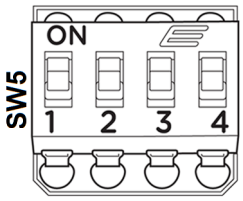



Pushbutton SW3 is used to turn off the terminations and remove all loads on the unused interposer receivers depending on the maximum number of lanes to be analyzed. Press the pushbutton switch (SW3) to move to the next active width as indicated by the LEDs (next to the switch) on the interposer. This is useful for devices that require terminations not to be present in order to train to a lower link width. The Active Width can be also controlled from the PCIe Protocol Analysis.

**Note:** Even though the Active Width may be lower than x16, it may be possible that the Signal Detect LEDs for higher lanes are ON if those lanes are transmitting signal.

## SW5: Clock Selection Configuration Switch

The source for the reference clock used by the analyzer to record PCI Express traffic is configurable according to below table. The Default setting for SW5 is ON-ON-ON-OFF positions for Single Host x16 Configuration (Default).




| SW5.1 | SW5.2 | SW5.3 | SW5.4 | Clock Selection Switch | Description |
|---|---|---|---|---|---|
| ON | ON | ON | OFF | SINGLE HOST x16 [Default] | Lanes [15:0] for Upstream and Downstream in the analyzer will use CLK_A from EDSFF connector. |
| ON | ON | OFF | ON | DUAL HOST x8 | Lanes [7:0] for Upstream and Downstream in the analyzer will use CLK_A from EDSFF connector.<br><br>Lanes [15:8] for Upstream and Downstream will use CLK_B from the EDSFF connector |
| ON | OFF | ON | ON | RESERVED | |
| OFF | ON | ON | ON | N/A | |

**Note:** Other clocking configurations are controlled by the PCIe Protocol Analysis software. See the *Summit T5 PCI Express Gen5 User Manual* for more information.

# 7 Test Points

**Table 1: J92 Sideband Signal Header**

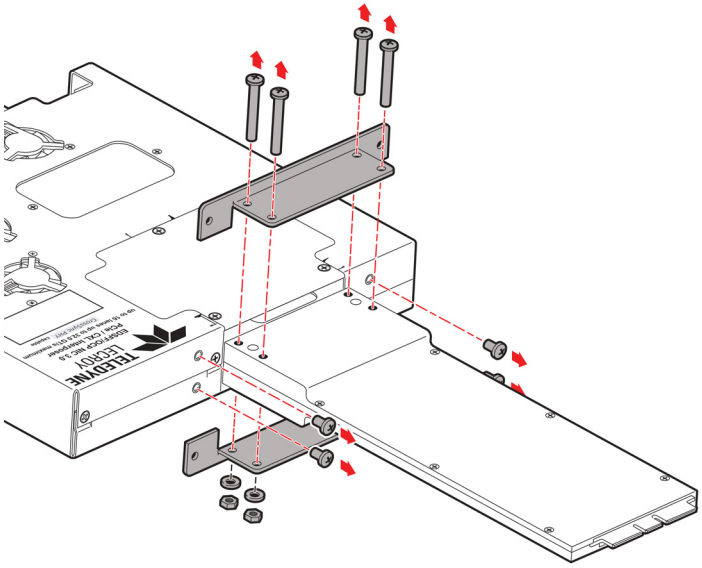
| Header Pin Number | Sideband Signal Name | Header Pin Number | Sideband Signal Name |
|---|---|---|---|
| J92-1 | BIF0# | J92-2 | SMCLK |
| J92-3 | BIF1# | J92-4 | SMDAT |
| J92-5 | BIF2# | J92-6 | PRSNT0# |
| J92-7 | PRSNTB0# | J92-8 | PRSNT1# |
| J92-9 | PRSNTB1# | J92-10 | PRSNT2# |
| J92-11 | PRSNTB2# | J92-12 | PRSNT3# |
| J92-13 | MAIN_PWR_EN | J92-14 | PWRBRK#IN |
| J92-15 | NIC_PWR_GOOD | J92-16 | AUX_PWR_EN |
| J92-17 | PRSNTB2# | J92-18 | SMBRST# |
| J92-19 | PRSNTB3# | J92-20 | WAKE#IN |

**Table 2: Test Points**

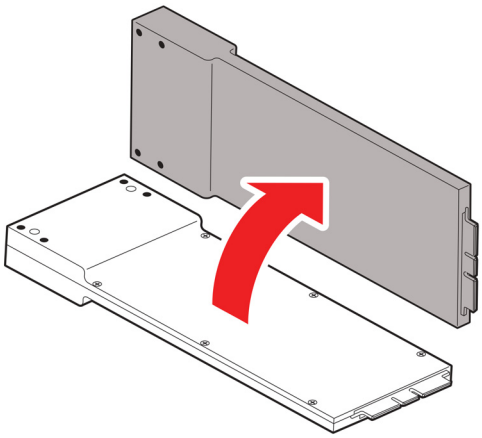
| Test Point Number | Test Point Name | Description |
|---|---|---|
| TP72/J42 | 12V_DEV | 12V DEVICE |
| TP76//J44 | P3P3_DEV | 3.3V DEVICE |
| TP82/J22 | I_12V | 12V CURRENT SENSE |
| TP78/J23 | I_3P3V | 3.3V CURRENT SENSE |
| J19 | CLKA_P | REFCLKA_HOST_P |
| J20 | CLKA_N | REFCLKA_HOST_N |
| J84 | CLKB_P | REFCLKB_HOST_P |
| J85 | CLKB_N | REFCLKB_HOST_N |
| J88 | CLKC_P | RESERVED |
| J89 | CLKC_N | RESERVED |
| J90 | CLKD_P | RESERVED |
| J91 | CLKD_P | RESERVED |
| J4 | DS_CLK | DS_REF_CLKIN |
| J3 | US CLK | US_REF_CLKIN |
| TP83,TP6,TP124,TP126, TP127,TP54,TP55,TP67, TP129,TP125 | GND | GROUND |

# 8 Vertical Support Bracket Installation

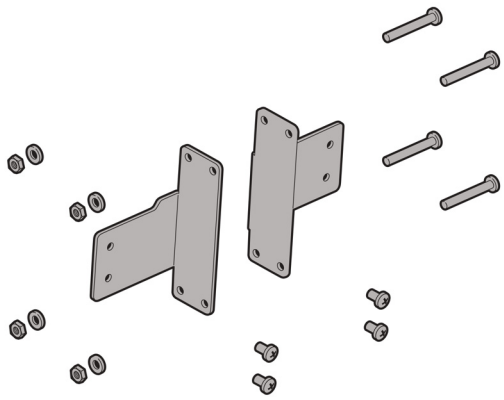
1. Remove the screws and support brackets from the interposer.

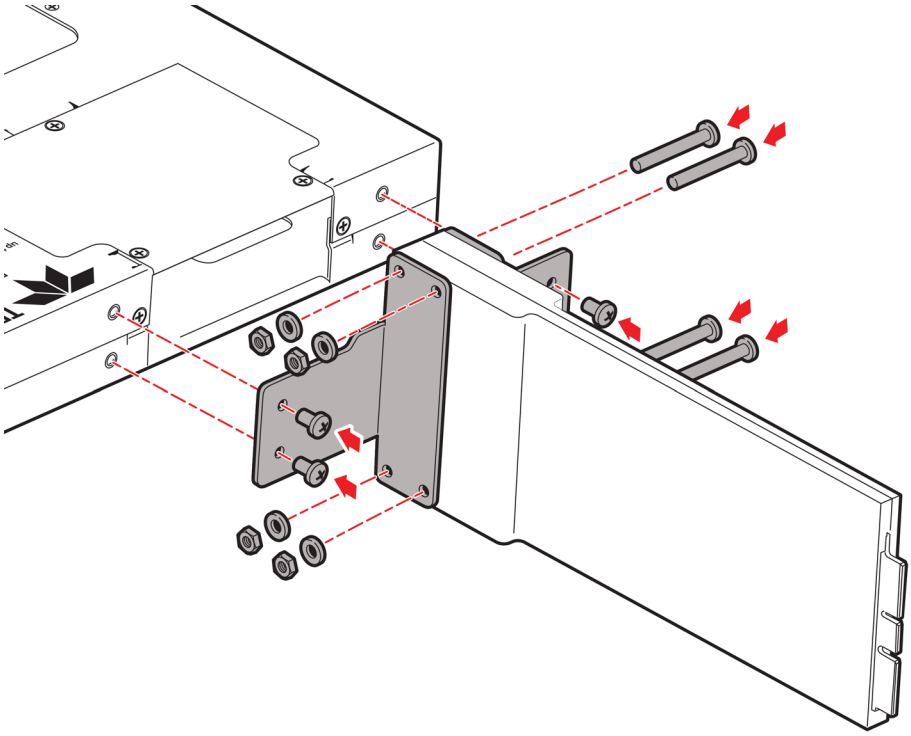


2. With the EDSFF extension in place, flip 90 degrees in relation to the interposer. Cable should twist and allow for this operation.

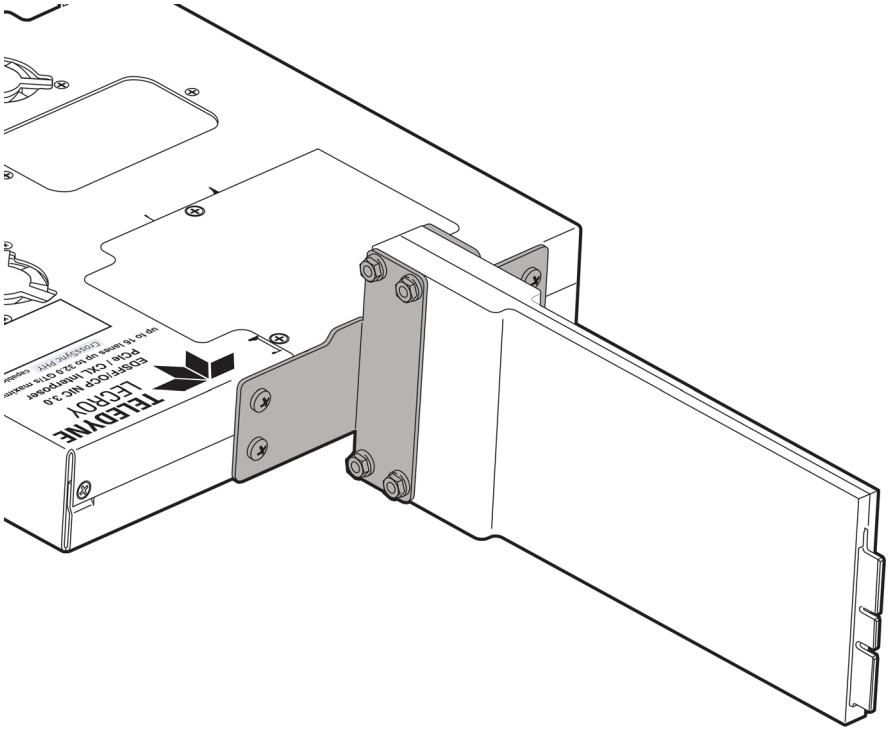


3. Locate the vertical support brackets and install as shown (cable piece from the interposer has been removed from the drawing for clarity). Reuse the screws, nuts and washers from the horizontal brackets that you removed in step one.





4. Replace the screws, washers and nuts and tighten them securely.

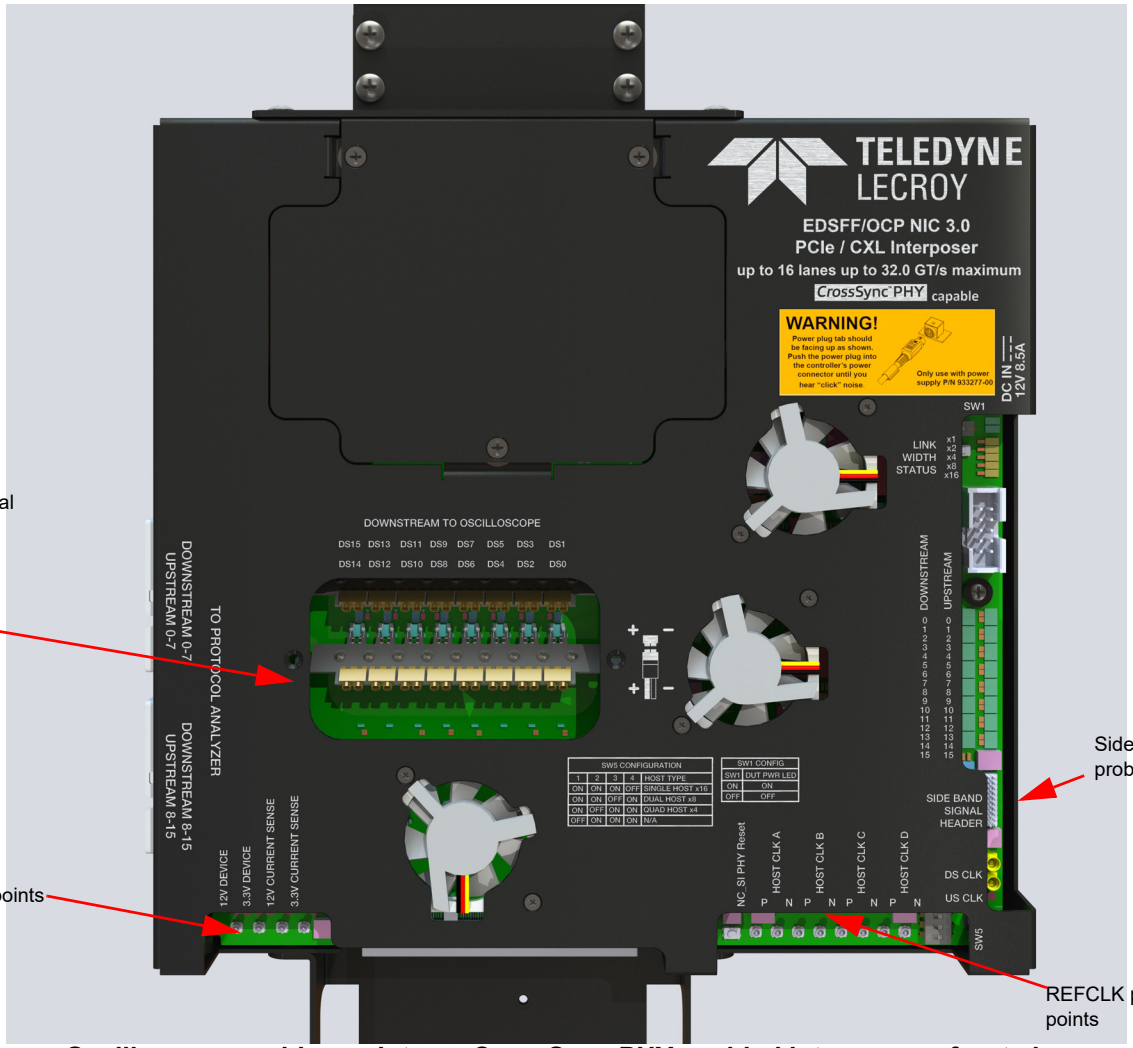


# 9 CrossSync PHY Capability

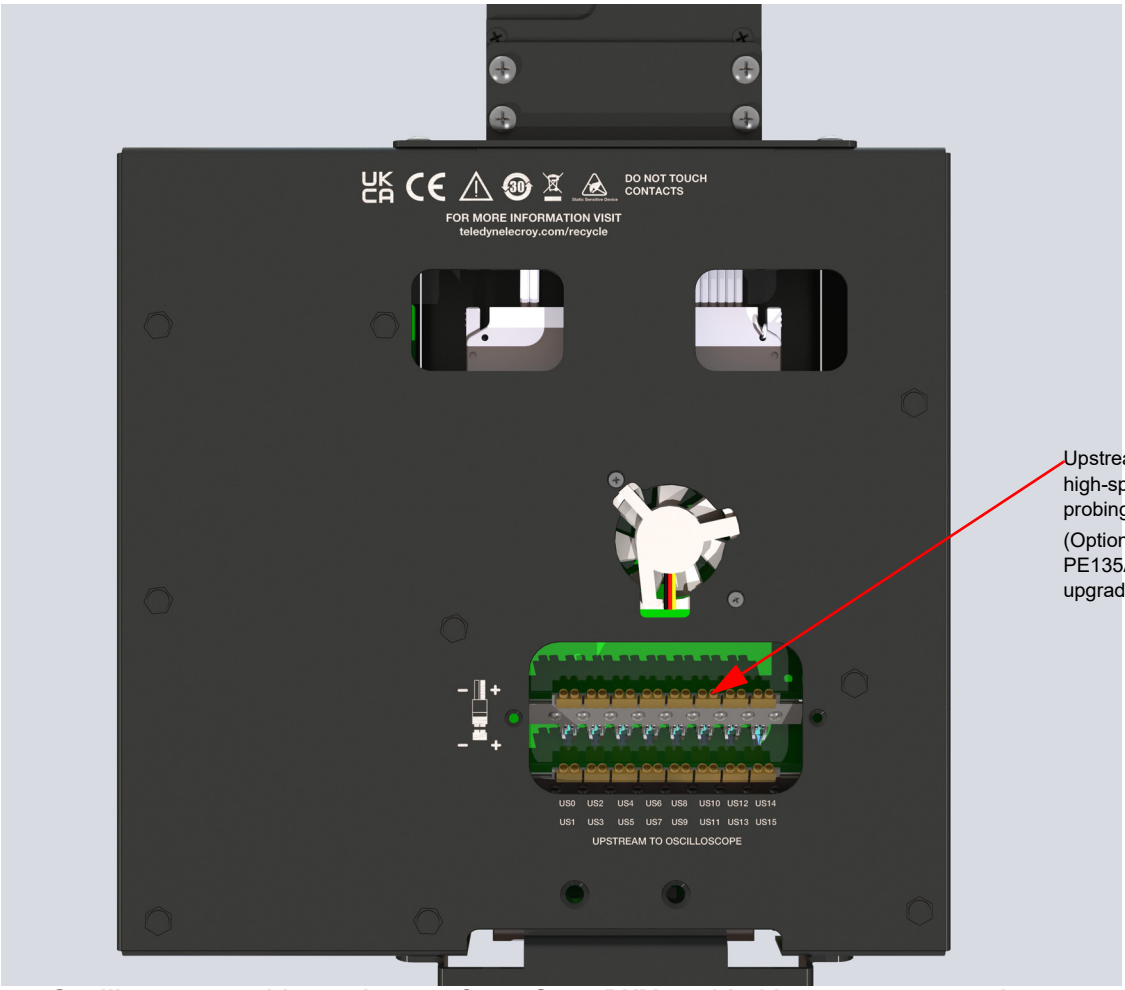
The PE243UIA-X G5x4 EDSFF E1.S, PE241UIA-X G5x8 EDSFF E1.L, and PE240UIA-X G5x16 EDSFF E3.x interposers all include CrossSync PHY capability, enabling:

- Easy signal access to sideband signals, power rail and refclk probing points
- Optional PE135ACA-X upgrade adds preinstalled connections on data lanes for Teledyne LeCroy DH Series high-bandwidth differential oscilloscope probes
- Optional CrossSync PHY oscilloscope software adds time-synchronization and integrated cross-analysis between PETracer protocol analysis software and MAUI oscilloscope software

The figures below show the location of the CrossSync PHY oscilloscope probing points on the interposer (version with PE135ACA-X upgrade pictured).




**Oscilloscope probing points on CrossSync PHY enabled interposer – front view**




**Oscilloscope probing points on CrossSync PHY enabled interposer - rear view**

## Connecting Probes to Sideband Signals

Sideband signals are available on standard square header pins in the location shown in first figure above, with pinout detailed in “J92 Sideband Signal Header” on page 9. These may be probed with a standard passive or active high-impedance oscilloscope probe.

Available sideband signals include: SMCLK, SMDAT, PRSNT0#, PRSNT1#, PRSNT2#, PRSNT3#, PWRBRK#IN, AUX_PWR_EN, SMBRST#, WAKE#IN. Specific pins are labeled directly on the circuit board for reference.

## Connecting to Rail Voltage and Current Monitoring Points

Rail voltage and current points are available on UMC connectors in the location shown in the front view. These are best probed with an RP4030 voltage rail probe, but connection directly to a coaxial oscilloscope input is also possible.

Voltage and current can be monitored for the 3.3V and 12V rails. The voltage points are connected directly to the voltage being supplied from the host to the endpoint. The current monitoring point for 3.3V operates at a conversion factor of 1A → 1V, and the current point for 12V operates at a conversion factor of 4A → 1V.

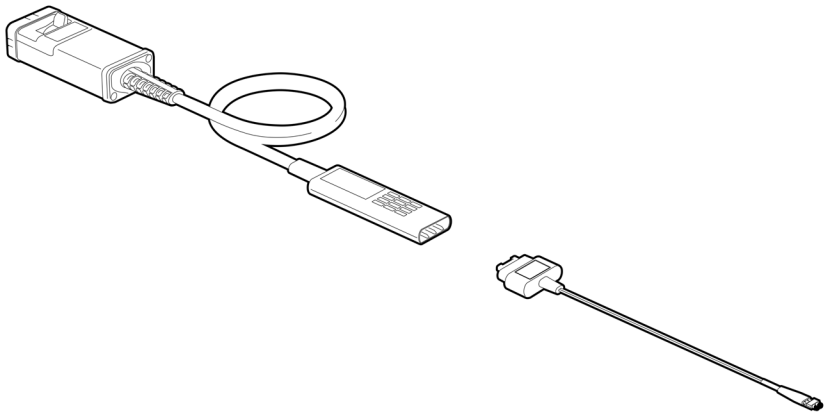
## Connecting to Reference Clock Probing Points

Reference clock activity can be monitored on UMC connectors in the location shown in the first figure above. Reference clock probing points can be connected directly to a 50Ω oscilloscope input. This reference clock signal has been buffered so that it does not connect directly to the host's reference clock.

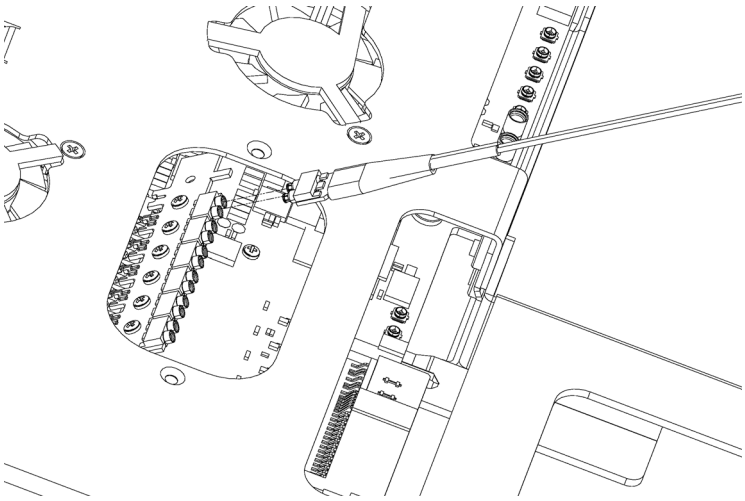
## Connecting Probes to High-speed Signals

With the PE135ACA-X CrossSync PHY upgrade, the interposer exposes 32 connections for high-speed probes, allowing any of the upstream or downstream lanes to be probed as desired.

High-speed signal probing points are designed exclusively for Teledyne LeCroy DH series high-bandwidth differential probes. A special probe lead, the DH-CSPHY-PCIE5-EDSFF, is used to create the connection between amplifier and interposer. See the figures below.

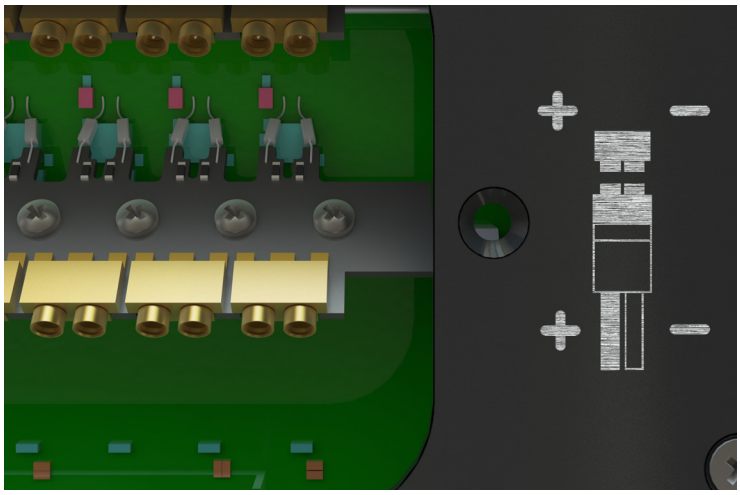


**Connect DH-CSPHY-PCIE5-EDSFF lead to Teledyne LeCroy DH series high-bandwidth differential oscilloscope probe**



**Connect DH-CSPHY-PCIE5-EDSFF lead to desired lane on interposer**

A polarity indication is printed directly on the interposer next to the probing points (see figure below)- this indicates the side of the connector that should align with the side of the DH-CSPHY-PCIE5-EDSFF denoted by a white indicator. Note that since devices in a PCIe link may invert polarity of any given lane, this indication on the interposer and probe is provided for consistency, and not as an absolute indication of signal polarity.



**Polarity indication for high-speed probing points**

# 10 Recommended Oscilloscope Options

**Oscilloscope Probes**

| Product Description | Product Code |
|---|---|
| *High-speed Data Signals* | |
| 8 GHz differential probe with ProLink interface | DH08-PL |
| 13 GHz differential probe with ProLink interface | DH13-PL |
| 16 GHz differential probe with ProLink interface | DH16-PL |
| 20 GHz differential probe with ProLink interface | DH20-PL |
| 25 GHz differential probe with 2.92 mm interface | DH25-2.92MM |
| 30 GHz differential probe with 2.92 mm interface | DH30-2.92MM |
| *Rail voltage/current points* | |
| Voltage Rail Probe - 4 GHz bandwidth, 1.2x attenuation, ±30V offset | RP4030 |

## Oscilloscope Software Options

The Oscilloscope Software options allow you to enable CrossSync PHY functionality on installed CrossSync software.

| Product Description | Product Code |
|---|---|
| CrossSync PHY option for LabMaster 10 Zi - sync oscilloscope with PCIe Protocol Analyzer hardware | LM10Zi-CrossSyncPHY |
| CrossSync PHY option for WaveMaster 8 Zi - sync oscilloscope with PCIe Protocol Analyzer hardware | WM8Zi-CrossSyncPHY |

## Recommended Oscilloscopes

CrossSync PHY is compatible with all LabMaster 10 Zi and WaveMaster 8 Zi series oscilloscopes. Below are some recommendations for example test configurations.

**PCI Express 3.0 - CrossSync PHY and Compliance Test Capable**

| Product Description | Product Code |
|---|---|
| 13 GHz (or higher), 40 GS/s, 4ch, 64 Mpts/Ch Serial Data Analyzer with 6.5 Gb/s Serial Trigger, 8b/10b and 64b/66b decode. | SDA 813Zi-B |
| QualiPHY PCIe 3.0 Compliance Software Option | QPHY-PCIE3-TX-RX |

**PCI Express 4.0 - CrossSync PHY and Compliance Test Capable**

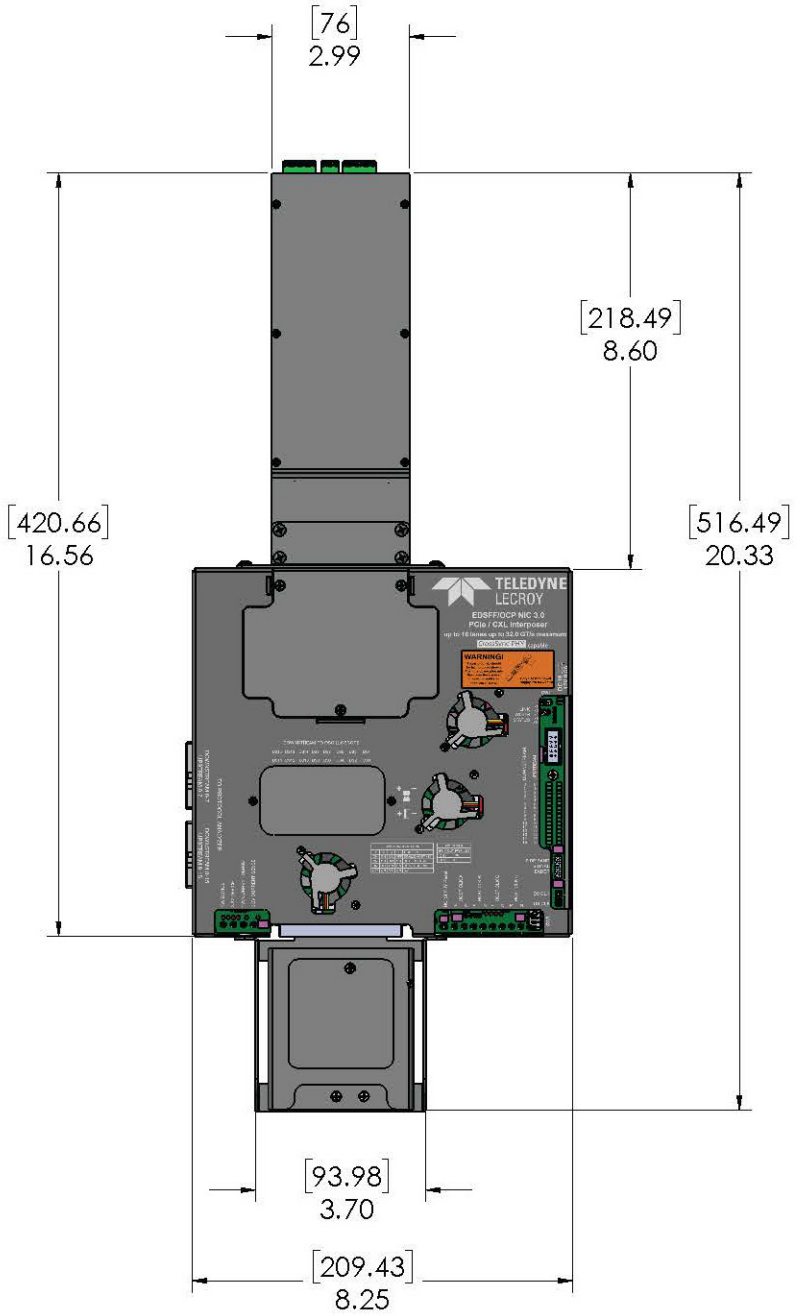
| Product Description | Product Code |
|---|---|
| 25 GHz (or higher) 80 GS/s LabMaster 10 Zi Acquisition Module | LabMaster 10-25Zi-A |
| LabMaster Master Control Module | LabMaster MCM-Zi-A |
| QualiPHY PCIe 4.0 Compliance Software Option (Also includes PCIe 3.0 compliance) | QPHY-PCIE4-TX-RX |
| 2.92mm to ProBus Adapter for connecting RP4030 and passive probes to LabMaster acquisition module | L2.92A-PBUS |
| 1 MΩ adapter – used with L2.92A-PBUS for connecting passive probes to LabMaster acquisition module | AP-1M |

**PCI Express 5.0 - CrossSync PHY and Compliance Test Capable**

| Product Description | Product Code |
|---|---|
| 50 GHz (or higher) 160 GS/s LabMaster 10 Zi Acquisition Module | LabMaster 10-50Zi-A |
| LabMaster Master Control Module | LabMaster MCM-Zi-A |
| QualiPHY PCIe 5.0 Compliance Software Option (Also includes PCIe 3.0 and 4.0 compliance) | QPHY-PCIE5-TX-RX |
| 2.92mm to ProBus Adapter for connecting RP4030 and passive probes to LabMaster acquisition module | L2.92A-PBUS |
| 1 MΩ adapter – used with L2.92A-PBUS for connecting passive probes to LabMaster acquisition module | AP-1M |

# 11 Dimensions

Interposer with E3 DUT bracket and E3 EDSFF Extension assembly installed horizontally. Dimension units in inches [mm].



## 12 Environmental Conditions

- Temperature: Operating 32° F to 122° F (0° C to 50° C)
- Temperature: Non-Operating 14° F to 176° F (-10° C to 80° C)
- Humidity: Operating 10% to 90% RH (non-condensing)

## Teledyne LeCroy Customer Support

Online Download

Periodically check the Teledyne LeCroy Protocol Solutions Group web site for software updates and other support related to this product. Software updates are available to users with a current Maintenance Agreement.


Web: teledynelecroy.com/tm/software/PCIe
E-mail: psgsupport@teledyne.com
Support: teledynelecroy.com/support/contact


## Trademarks and Servicemarks



## Changes

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