Characterization of Chip-to-Package Interconnects for Glass Panel Embedding (GPE) for Sub-THz Wireless Communications

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***Abstract*—This work presents characterization of microvia interconnects in D-band frequencies for use as chip-to-package interconnects in Glass Panel Embedded (GPE) packages. Antenna-in-Package based on wafer-level fanout technology have demonstrated superior performance along its small form factor by eliminating wire-bond, assembly, underfill and package substrates. However, epoxy mold compounds, which limit the use of fanout packages at sub-Thz frequencies, do not support the electrical performance, thermal and thermo-mechanical needs of such applications. Embedding chips in glass panels, on the other hand, leverages all benefits of glass substrates and low-loss polymer buildup dielectrics while also mitigating the effects of wire-bond and microbumps for chip-to-package interconnects. In this paper, the design, fabrication, and characterization of these all-copper microvia-like chip-to-package interconnects is presented. These interconnects achieve an average chip-to-package loss of 0.146 dB in D-band and 0.177 dB maximum loss at 170 GHz which is lower than current flip-chip approaches, and our objective is to incorporate such interconnects in the proposed GPE package.**

***Index Terms*—microvia, D-band, chip-to-package interconnect, Glass Panel Embedding, sub-THz**

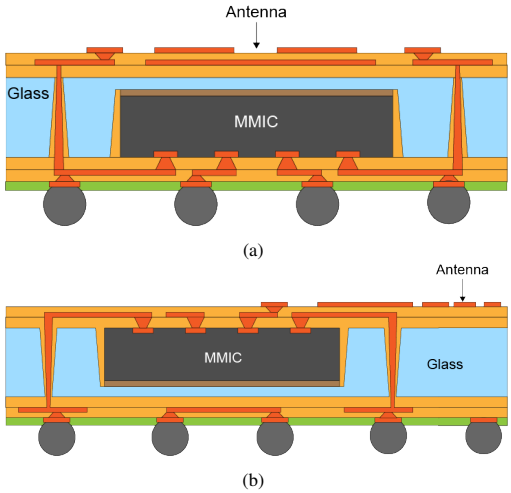


Fig. 1. Antenna-in-Package (AiP) options using Glass Panel Embedding

I. Introduction

Wireless technologies have developed significantly in recent years with the launching of 5G [1]. Use of higher carrier frequencies is essential to be able to achieve the bandwidth and data rates that emerging wireless technologies require. Besides the rapid development of on-chip wireless circuitry, high performance packages play an increasingly important role for wireless systems. Design at high frequencies is more challenging due to factors such as increasing material losses and parasitics. In addition, smaller form factor is also required by new technologies as devices become smaller. Therefore, highly integrated packaging approaches are an attractive solution for achieving lower interconnect loss and smaller size requirements imposed by these new technologies. Fanout packages have disrupted the entire semiconductor industry due to its benefits in size, cost, electrical performance, reliability, and potential for heterogeneous integration when compared to traditional flip-chip and wire bond packages [2]. Fanout eliminates the use of wire bonding and assembly, and therefore, mitigates major signal losses, while also reducing the footprint of the die by reducing the bump-pitches. The significantly lower parasitics present a strong case for using fanout packages in sub-THz applications over standard BGA-wirebond and BGA flip-chip packages [3]. However, today most fanout packages use epoxy mold compounds (EMC) that are not suitable for 6G applications due to their higher dk/df, high moisture absorption & surface roughness, higher warpage especially for larger packages. Glass Panel Embedding (GPE) has been studied as an inorganic fanout approach to address the challenges with EMCs [4], [5]. Glass substrates with low-loss polymeric build-up films perform well at sub-THz frequencies [6]. The high dimensional stability and surface smoothness enable precision RDL, while the CTE tailorability of Glass enables large-body reliability. The embedded mm-wave ICs (MMIC) may dissipate 0.75 W/mm^2 thermal fluxes [7], and GPE allows direct heat spreader integration with the embedded die to extract this heat from the package [8].

Some options for antenna-in-package applications using GPE is shown in Fig. 1. As opposed to traditional bond wires or microbumps, the chip-to-package interconnect in

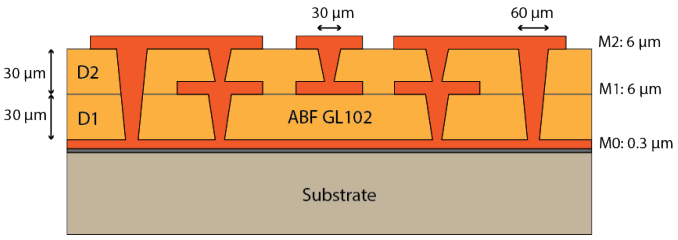


Fig. 2. Schematic showing the stackup of characterization test vehicle

fanout/embedding is through an all-copper microvia landing from the package RDL onto the die pads. Bonding wires are widely used at lower frequencies. However, there are several challenges to realize bond wire transitions such as chip placement, alignment, and the control of the wire loop shape, etc [9]. Besides fabrication challenges, wire-bonded interfaces also suffer from parasitics and narrow bandwidth. Recent work using wire-bond in chip-to-antenna interface shows 1.8 dB loss at 140 GHz for the transition [10]. Flip-chip is another popular approach used in mmWave modules. Formed by solder bumps or Cu pillar, flip-chip interface has lower transition loss (<1 dB) and higher bandwidth [11]. A similar extraction of the losses of microvia transitions to be used in fanout/embedded packages has not been studied previously for sub-THz frequencies. In this paper, the electrical performance of chip-to-package microvia transitions through polymer buildup films on silicon wafer are characterized and demonstrated. The paper presents the challenges in characterization of the vertical interconnects and the design of a test vehicle for the same in Section II. The fabrication of the test vehicle and measurement results are shown in Section III followed by conclusions in Section IV.

II. Test Vehicle Design

Characterization of microvia losses needs to be performed using structures containing more than one via transition since only the top layer of the panel can be probed. In this study, loss per microvia has been extracted from measurements of conductor-backed CPW structures of various lengths with multiple via transitions. The stack-up is shown in Fig. 2. Microvias drilled on dielectric build-up layer on silicon substrate with a blanket copper layer will be characterized. The build-up film used in this study is GL-102 from Ajinomoto. Reported properties of the material at 5.8 GHz is ϵ_r = 3.3, $\tan\delta$= 0.0044. This build-up film is not individually characterized in D-band, but studies on a stack-up using the same build-up film on glass substrate show that the loss tangent of the whole stack-up goes from 0.005 at 50 GHz to 0.015 at 170 GHz [12], which shows a three times increase. Therefore, we have used 0.012 as the loss tangent for the material in D-band while designing the structures.

The intended application for the microvias characterized in this study is to achieve electrical connection to chips embedded in a package. However, reliable characterization of said structures using multiple microvia transitions directly on

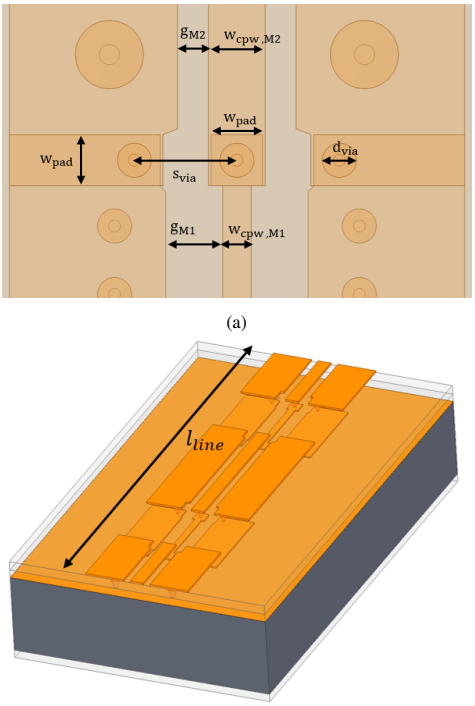


Fig. 3. (a) Top view of a via transition (b) 3mm CBCPW line with 4 via transitions

TABLE I
Design Dimensions

Structure		Parameter	Value
CBCPW on M1		$w_{cpw,M1}$	30 μm
		g_{M1}	50 μm
CBCPW on M2		$w_{cpw,M2}$	50μm
		g_{M2}	27 μm
Microvia		d_{via}	30 μm
		s_{via}	90 μm
		w_{pad}	45 μm
Set 1	Line 1	l_{line}, n_{via}	3 mm, 4 vias
	Line 2	l_{line}, n_{via}	6 mm, 8 vias
Set 2	Line 1	l_{line}, n_{via}	1.5 mm, 4 vias
	Line 2	l_{line}, n_{via}	3 mm, 8 vias
	Line 3	l_{line}, n_{via}	6 mm, 16 vias

silicon substrate embedded in a package is challenging. The reason for that is related to the high dielectric constant of the silicon substrate compared to that of the build-up film used. The difference between dielectric constants between silicon (11.9) and dielectric buildup film used in this study (3.3) leads to difficulties in matching impedances of transmission lines built on these materials using lines on a similar size scale. Making a 50 Ω CPW line on the build-up layer requires line widths exceeding the probe pitch (75 μm), whereas making a 70 Ω line on silicon substrate requires CPW lines with high spacing/width ratio, therefore increasing radiation loss of the line. Good matching of the line impedances is particularly im-

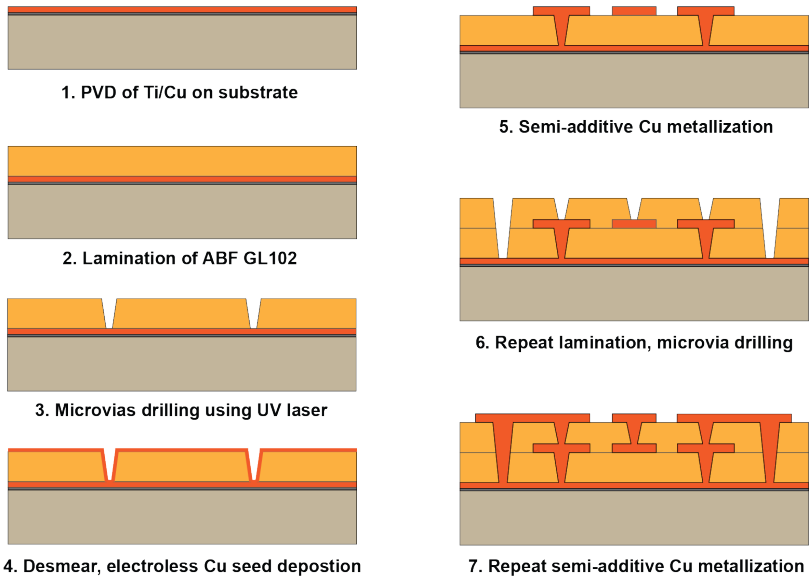


Fig. 4. Process flow for fabrication of test vehicle for via characterization

portant in structures containing multiple cascaded transitions like the ones used in this study. When multiple transmission lines of equal length are cascaded, reflections at each transition between the lines add up constructively when electrical length of the line sections is 90 degrees. In such a structure, even a small impedance mismatch between transmission line sections causes a resonance in scattering parameters at frequencies where lengths of the line sections are near integer multiples of quarter wavelength. One way to avoid this is to keep all line sections smaller than $\lambda/4$ in the frequency band of operation. Wavelength of a CPW line on silicon is on the order of 700 μm at 170 GHz. This would require line sections on chip to be smaller than 175 μm, which brings other problems such as unwanted parasitic coupling between consecutive microvias. Therefore the stack-up given in Fig 2 is used in this study to be able to characterize microvia losses more reliably in D-band. This stack-up characterizes microvias from conductor-backed CPW lines from top layer (M2) to the ones on bottom metal layer (M1) over a silicon substrate with a blanket copper layer (M0) serving as the ground. In order to be able to probe the structures directly without requiring a separate probing pad, distance between the signal conductor of CBCPW to the ground conductors should be kept smaller than the probe pitch. Using 75 μm-pitch GSG probes excludes the possibility of using 50 Ω CBCPW lines, since that would require a line width greater than 80 μm. Therefore, lines are designed with a characteristic impedance of 65 Ω for ease of fabrication and measurement. Designed dimensions of the lines in M1 and M2 layers are given in Table I. Two sets of daisy chain structures have been designed to be able to cover the lower (110-150 GHz) and upper (125-170 GHz) parts of D-band for the characterization of microvia loss. Details of the structures are provided in Table I. The reason for requiring two different sets is to be able to relax the fabrication requirements and to tolerate impedance mismatches between the lines that may occur due to process variations.

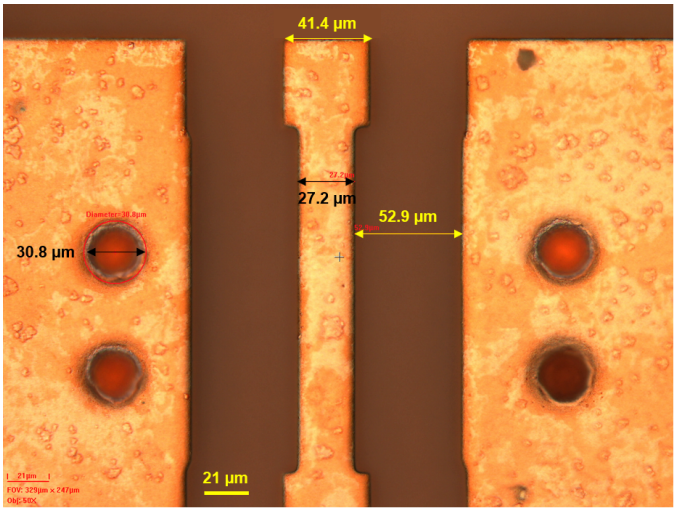
III. Fabrication

The process flow for fabrication of the test vehicle is shown in Fig. 4. A blanket Ti/Cu layer of 100 nm and 300 nm was deposited onto the substrate core using physical vapor deposition (PVD). 30 μm of ABF GL102 was then molded before drilling the vias using a picosecond UV laser. The dimensions of this via was measured to be 30 μm. The dielectric is then chemically desmeared to remove any debris from via drilling [13]. To metallize both M1 and M2, a standard semi-additive process (SAP) with a electro-less Cu seed is used. A 7 μm negative photoresist was laminated upon a 180 nm Cu seed prior to photolithography. 6-7 μm of Cu was then electroplated and photoresist was stripped before differentially etching the Cu seed. In order to improve the adhesion of M1 to the D2 ABF layer, NovaBond® process was used [14]. Another 30 μm ABF GL102 was laminated to form D2 following which, vias from M2-M1 and M2-M0 were drilled simultaneously before using SAP to metallize M2 as well. Fig. 5 shows the dimensions of structures in M1 and M2 and these vias were measured to be 30 μm and 60 μm in diameter.

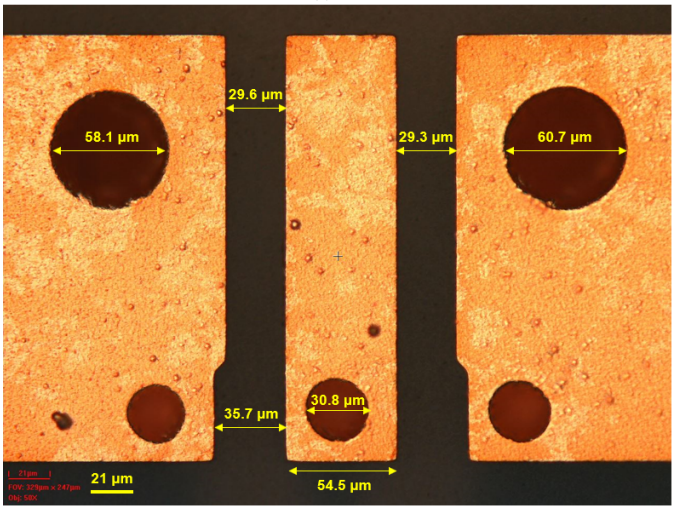
IV. Measurements & Results

Measurements have been performed with Agilent E8361C vector network analyzer, millimeter wave controller and V06VNA2 D-band frequency extenders. Cascade i170-S-GSG-75-BT Infinity probes have been used for probing the structures. LRRM calibration has been performed to move the measurement reference plane to probe tip. Measured scattering parameters have been re-normalized to 65 Ω.

Measurement results for the two sets of daisy chains are given in Fig. 7. Measurements are taken from four different



(a) M1



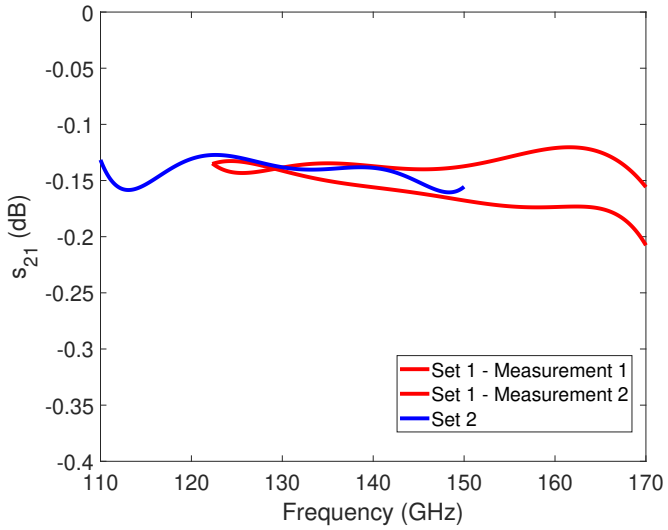
(b) M2

Fig. 5. Dimensions of fabricated structures on (a) M1, and (b) M2

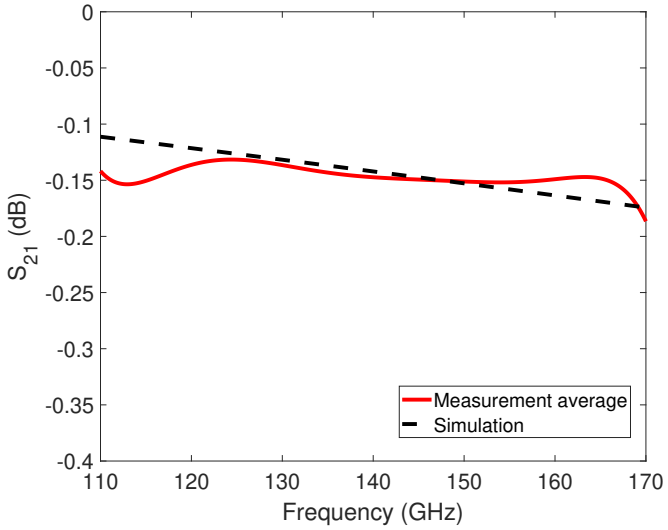
TABLE II
COMPARISON WITH EXISTING LITERATURE

	Material	Interconnect type	Loss per interconnect
This work	ABF GL-102	Microvia	0.145 dB @ 140 GHz 0.177 dB @ 170 GHz
[15]	LTCC	Flip-chip	0.3 dB @ 165 GHz
[16]	Astra MT77	Flip-chip	0.3 dB
[10]	Astra MT77	Wirebonding	1.8 dB @ 140 GHz

coupons. In order to further eliminate the losses introduced by the discontinuity at the probe tip and the measured structures, 1.5mm line + 4 via measurement in set 1 and 3mm + 4 via measurement in set 2 have been used as the baseline measurement and are subtracted from insertion loss measurements of other structures. CBCPW loss has been subtracted from the measurements and then results are normalized by the number of vias to obtain loss per via.



(a)



(b)

Fig. 6. (a) Extracted via loss from each set of measurement, (b) Extracted via loss vs simulation.

As can be seen in Fig. 7, insertion loss of set 1 is matched well for 110-150 GHz, whereas set 2 is matched well in 125-170 GHz range. As explained in the test vehicle design section, insertion loss of daisy chain structures can be used for extracting loss per microvia only when return loss shows good matching. Therefore non-matched parts of the responses from each set are discarded. Fig. 6 shows the extracted via loss obtained by each set of measurements. Results from the two sets match well in the overlapping frequency band 125-150 GHz. The difference between the simulated and measured microvia losses can mostly be attributed to material properties not being exactly known in these frequencies. Other causes of discrepancy can be related to topology of the microvias, or copper surface roughness. In simulations microvias were assumed to be fully-filled, whereas fabricated microvias were conformal. This can introduce higher parasitics [17]. Extracted

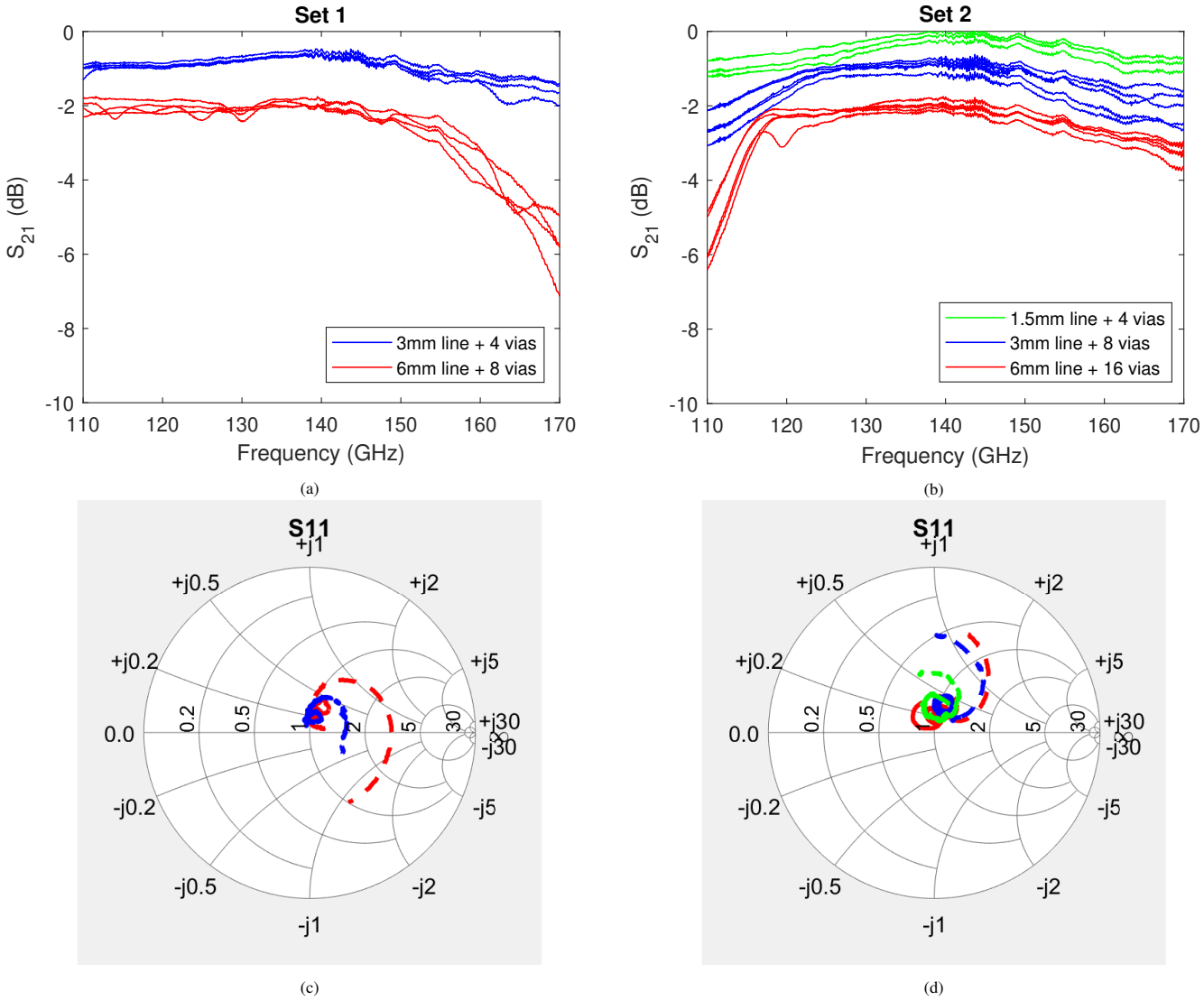


Fig. 7. (a) S_{21} of Set 1 structures (b) S_{21} of Set 2 structures (c) S_{11} of Set 1 structures (d) S_{11} of Set 2 structures where data points corresponding to mismatched frequencies are shown with dashed lines on Smith chart.

via loss from measurements show that microvias with 30 μm diameter have 0.146 dB average loss in D-band with 0.177 dB maximum loss at 170 GHz.

Comparison with existing literature is given in Table II. A matching network is used in [15] to compensate for parasitics. As can be seen in the table, microvia transitions offer lower insertion loss compared to flip-chip and does not require a matching network to account for parasitics.

V. Conclusion

This paper demonstrated characterization of insertion loss of microvia transitions through polymer build-up film in D-band. Microvia transitions showed an average loss of 0.146 dB in D-band with 0.177 dB maximum loss at 170 GHz. Having $<$ 0.2 dB loss in D-band makes microvia transitions a promising alternative to flip-chip and wirebonding. These microvia interconnects can be implemented as chip-to-package interconnects in glass panel embedding as shown in Fig 1, making GPE a promising alternative to flip-chip packages to achieve low-loss chip-to-package interconnections in D-band.

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