



**Semiconductor Discretes for RF-Microwave Applications**



## Skyworks Solutions

Skyworks Solutions, Inc. is an innovator of high-performance analog and mixed-signal semiconductors enabling mobile connectivity. The company's power amplifiers, front-end modules and direct conversion transceivers are at the heart of many of today's leading-edge multimedia handsets. Leveraging core technologies, Skyworks also offers a diverse portfolio of linear products that support automotive, broadband, cellular infrastructure, industrial and medical applications.



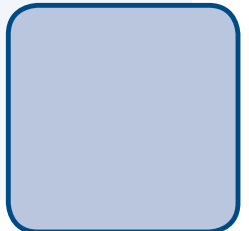
Headquartered in Woburn, Massachusetts, USA, Skyworks is worldwide with engineering, manufacturing, sales and service facilities throughout Asia, Europe and North America.



New products are continually being introduced at Skyworks. For the latest information, visit our Web site at [www.skyworksinc.com](http://www.skyworksinc.com). For additional information, please contact your local sales office or email us at [sales@skyworksinc.com](mailto:sales@skyworksinc.com).

## The Skyworks Advantage

- Broad multimode radio and precision analog product portfolio
- Market leadership in key product segments
- Solutions for all air interface standards, including CDMA2000, GSM/GPRS/EDGE, LTE, WCDMA, WLAN and WiMAX
- Engagements with a diverse set of top-tier customers
- Analog, RF and mixed-signal design capabilities
- Access to all key process technologies: GaAs HBT, PHEMT, BiCMOS, SiGe, CMOS and RF CMOS
- World-class manufacturing capabilities and scale
- Unparalleled level of customer service and technical support
- Commitment to technology innovation





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# Introduction

## Proven Performance and Leadership

As a world-class supplier of RF microwave components for today's wireless communication systems, Skyworks continues to deliver the highest performance Silicon and GaAs discrete products. Building on a proven legacy (which includes products developed at Alpha Industries prior to its merger with Skyworks), these innovative solutions are manufactured using the most advanced processes, driven by decades of experience and industry leadership.

With market demands constantly changing, Skyworks is committed to expanding its microwave portfolio to meet a wider range of applications including radar, point-to-point, point-to-multipoint, cellular, military, space-based communications, and other wireless microwave functions. As always, all of our solutions are backed by world-class customer service, advanced manufacturing capabilities and leadership technology.

## The Right Design Choice Starts Here

We invite you to review our complete catalog of packaged and unpackaged semiconductor diodes, passive elements, and switches for specific RF and microwave applications. Products include silicon varactors, PIN diodes, Schottky diodes, GaAs Schottky diodes, passive elements, and PHEMT-based switches. Design engineers will find this catalog especially useful in finding the key specifications for Skyworks' semiconductor products to easily select appropriate part numbers.

For more information—including how we can help you design the perfect solution for your application—contact our dedicated team of engineers at [sales@skyworksinc.com](mailto:sales@skyworksinc.com). They have the experience and technical expertise to answer any of your questions.

Visit [www.skyworksinc.com](http://www.skyworksinc.com) for regularly updated technical data, application notes, and new product information.

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## PIN DIODES

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**DATA SHEET**

# **APD Series: Silicon PIN Diodes Packaged and Bondable Chips**

**Applications**

- Switches
- Attenuators

**Features**

- Established Skyworks PIN diode process
- Low capacitance designs to 0.05 pF
- Voltage ratings to 200 V
- Chip size smaller than 15 mils square
- Lead (Pb)-free, RoHS-compliant, and Green™

**Description**

Skyworks APD Series of silicon PIN diodes are designed for use as switch and attenuator devices in high-performance RF and microwave circuits. These PIN diode designs are useful over a wide range of frequencies from below 100 MHz to beyond 30 GHz. These devices utilize Skyworks well-established silicon technology resulting in high resistivity and tightly controlled I region width PIN diodes. APD0505-000 through APD0810-000 are designed for fast speed through moderate speed switch applications. They have low resistance and capacitance at zero bias and reverse bias. The thick I region APD2220-000 is designed for low-distortion attenuator applications.



Skyworks Green™ products are RoHS (Restriction of Hazardous Substances)-compliant, conform to the EIA/EICTA/JEITA Joint Industry Guide (JIG) Level A guidelines, are halogen free according to IEC-61249-2-21, and contain <1,000 ppm antimony trioxide in polymeric materials.


**Absolute Maximum Ratings**

Characteristic	Value
Power dissipation	$P_{diss} = \frac{175 - T_{amb}}{\theta} \text{ W}$
Operating temperature	-65 °C to +175 °C
Storage temperature	-65 °C to +200 °C
Reverse voltage	Voltage rating

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum Ratings. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

**CAUTION:** Although these devices are designed to be robust, ESD (Electrostatic Discharge) can cause permanent damage. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.

**Electrical Specifications at 25 °C**

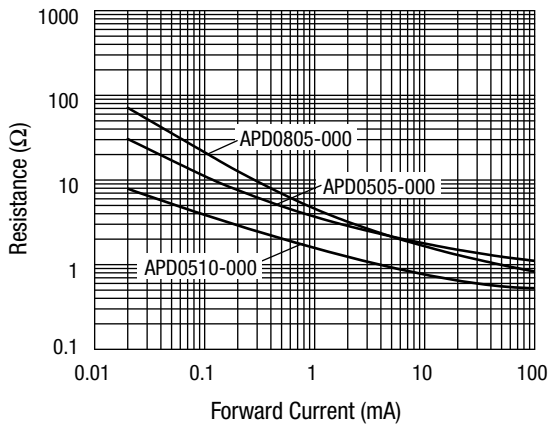
Part Number	Capacitance V <sub>R</sub> = 50 V, 1 MHz (pF)	Capacitance V <sub>R</sub> = 0 V, 1 MHz (pF)	R <sub>S</sub> I = 10 mA, 500 MHz (Ω)	TL I = 10 mA (ns)	Voltage Rating <sup>(1)</sup> (V)	I Region Thickness (μm)	Thermal Resistance (°C/W)	Contact Diameter (Mils)	Outline Drawing
	Max.	Typ.	Max.	Typ.		Nom.	Max.	Nom.	
Switching Applications									
APD0505-000	0.05	0.1	2	20	50	5	100	1.5	150-806
APD0510-000	0.1	0.2	1.5	40	50	5	80	2.5	150-801
APD0520-000	0.2	0.25	1	50	50	5	80	3.5	150-801
APD0805-000	0.05	0.1	2	100	100	8	80	2	150-801
APD0810-000	0.1	0.15	1.5	160	100	8	60	3	150-801
APD1510-000	0.1	0.2	2	300	200	15	60	3	150-813
APD1520-000	0.2	0.25	1.2	900	200	15	30	4	150-802
Attenuator Applications									
APD2220-000	0.2	0.35	4	700	100	50	80	7.5	149-815

1. Reverse current is specified at 10  $\mu\text{A}$  maximum at the voltage rating. This voltage should not be exceeded.

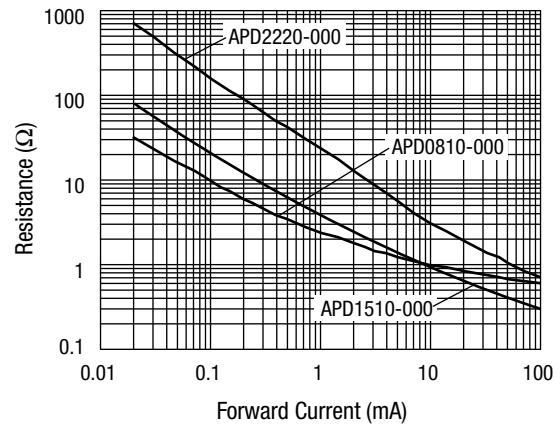
**Hermetic Packages**

Hermetic Stripline 240	Typical $\theta_{JC}$ (°C/W)	Hermetic Pill 203	Typical $\theta_{JC}$ (°C/W)	Hermetic Pill 210	Typical $\theta_{JC}$ (°C/W)	Hermetic Pill 219	Typical $\theta_{JC}$ (°C/W)
APD0505-240	190	APD0505-203	130	APD0505-210	120	APD0505-219	190
APD0510-240	180	APD0510-203	110	APD0510-210	100	APD0510-219	180
APD0520-240	180	APD0520-203	110	APD0520-210	100	APD0520-219	180
APD0805-240	180	APD0805-203	110	APD0805-210	100	APD0805-219	180
APD0810-240	160	APD0810-203	90	APD0810-210	80	APD0810-219	160
APD1510-240	160	APD1510-203	90	APD1510-210	80	APD1510-219	160
APD1520-240	130	APD1520-203	60	APD1520-210	50	APD1520-219	130
APD2220-240	110	APD2220-203	100	APD2220-210	100	APD2220-219	110

## Typical Performance Data

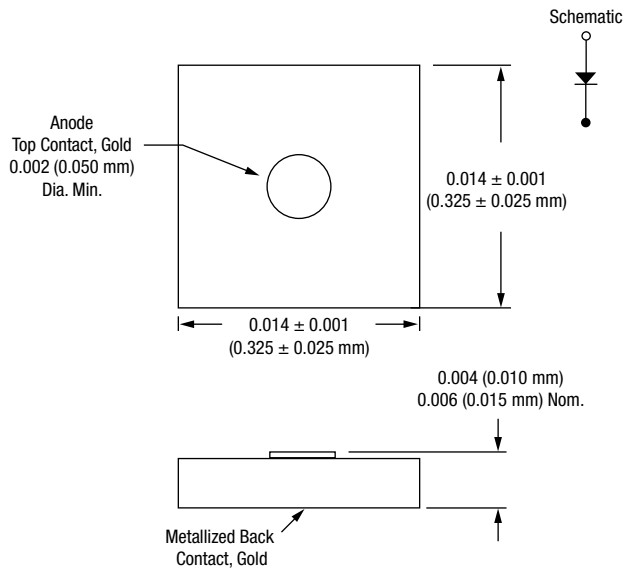


Resistance vs. Forward Current @ 1 GHz

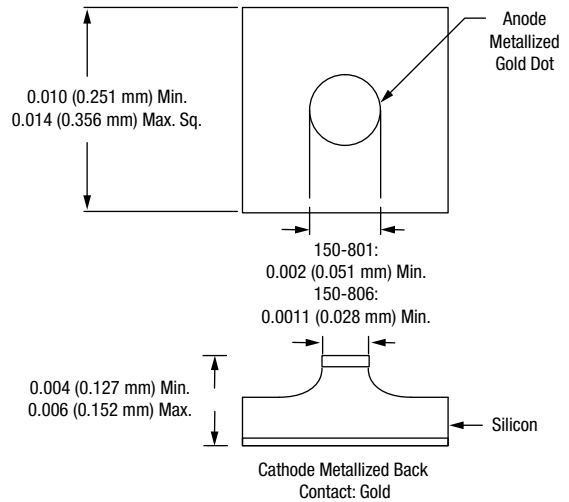


Resistance vs. Forward Current @ 1 GHz

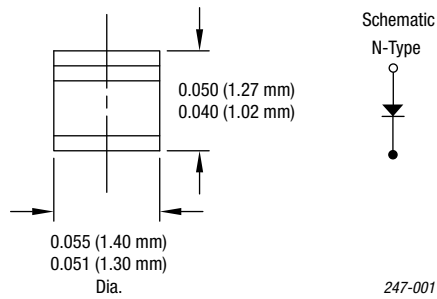
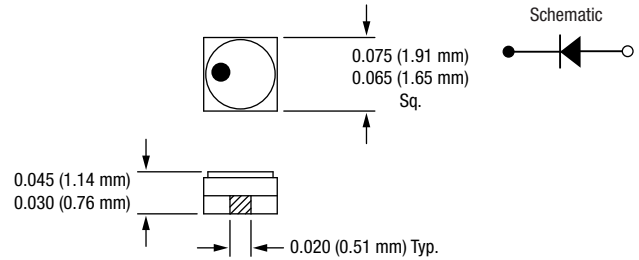
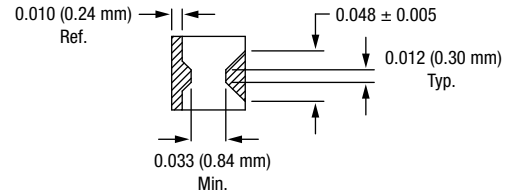
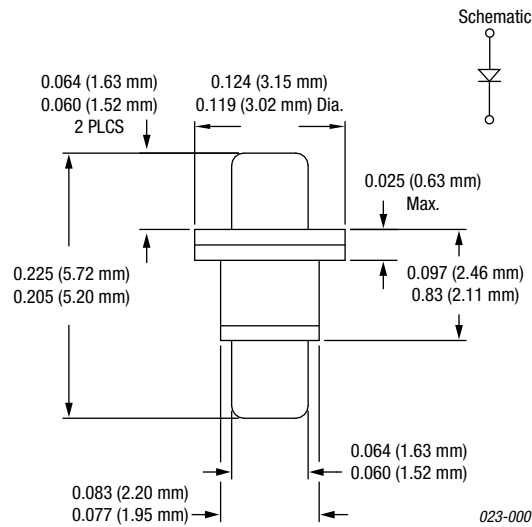
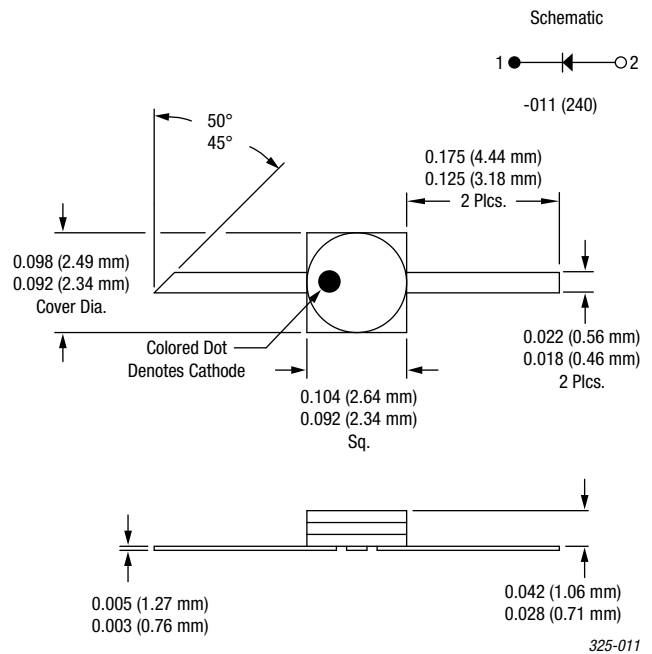
## 149-815



## 150 Series





**-203****-219****-210****-240**

**DATA SHEET**

# Silicon PIN Diodes in Hermetic Surface Mount Package

## Applications

- Switches
- Attenuators
- Limiters

## Features

- Hermetic ceramic package, 1.83 x 1.43 x 1.0 mm
- Very low parasitic impedance
- Low thermal impedance
- Usable to 10 GHz
- Operating temperature range -55 °C to 150 °C
- ESD Class 1B, human body model
- Low inductance 0.48 nH typ.
- Lead (Pb)-free, RoHS-compliant, and Green™, MSL-1 @ 260 °C per JEDEC J-STD-020

## Description

The family of proven silicon PIN diodes is packaged in a hermetic, ceramic package. This package offers excellent, very low parasitic inductance and capacitance for wide bandwidth, high-frequency operation. It has low thermal impedance and meets fine and gross leak requirements for excellent reliability. Its small form factor, 1.83 x 1.43 x 1.0 mm, compares favorably to that of the smallest plastic packages.

This package meets Skyworks definition of Green: it is lead (Pb)-free, fully complies with current RoHS requirements and contains no halogens and no antimony (Sb).

SMP1340-108, SMP1345-108 and SMP1352-108 are optimized for use in switching circuits. The SMP1352-108 can also be used in attenuator circuits.

SMP1302-108 and SMP1304-108 offer thicker I layers, making them ideal for low-distortion attenuator circuits.

The CLA4605-108 and CLA4607-108 are well suited for limiter applications.

The diodes available in this package can operate over the temperature range of -55 °C to 150 °C.


**NEW**


Skyworks Green™ products are RoHS (Restriction of Hazardous Substances)-compliant, conform to the EIA/EICTA/JEITA Joint Industry Guide (JIG) Level A guidelines, are halogen free according to IEC-61249-2-21, and contain <1,000 ppm antimony trioxide in polymeric materials.

## Electrical Specifications

**T = 25 °C, unless otherwise noted**

Part Number	Voltage Rating <sup>(1)</sup> (V)	Nom. I Region Thickness (μm)	Typ. Total Capacitance $V_R = 0\text{ V}$ & $f = 1\text{ MHz}$ (pF)	Max. Total Capacitance $V_R = 10\text{ V}$ 1 MHz (pF)	Typ. Forward Voltage $I_F = 10\text{ mA}$ (mV)	Max. Series Resistance $I_F = 1\text{ mA}$ & $f = 100\text{ MHz}$ (Ω)	Max. Series Resistance $I_F = 10\text{ mA}$ & $f = 100\text{ MHz}$ (Ω)	Typ. $T_L$ $I_F = 10\text{ mA}$ (ns)
<b>Switching Applications</b>								
SMP1340-108	50	7	0.26	0.325	880	1.7 typ.	1.2	100
SMP1345-108	50	10	–	0.285	850	3.5 typ.	2	100
SMP1352-108	200	50	–	0.425 @ 20 V	825	8 typ.	2.8	1000
<b>Attenuator Applications</b>								
SMP1302-108	200	50	–	0.36 @ 30 V	800	20	3	700
SMP1304-108	200	100	–	0.36 @ 30 V	800	50	7	1000
<b>Limiter Applications</b>								
CLA4605-108	30	2	–	0.28	–	4 typ.	2.7	–
CLA4607-108	120	7	0.27	–	–	–	2.5	50
CLA4608-108	120	7	–	0.69 @ 38 V	–	–	1.2	100

1. Reverse current is specified at 10 μA maximum at the voltage rating. This voltage should not be exceeded.

## Absolute Maximum Ratings

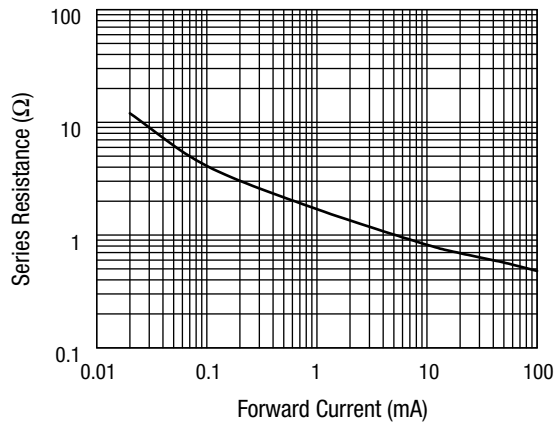
Characteristic	Value
Reverse voltage	Voltage rating
Forward current	150 mA
Dissipated power at 25 °C	250 mW
Operating temperature	-55 °C to +150 °C
Storage temperature	-65 °C to +200 °C

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum Ratings. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

**CAUTION:** Although these devices are designed to be robust, ESD (Electrostatic Discharge) can cause permanent damage. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.

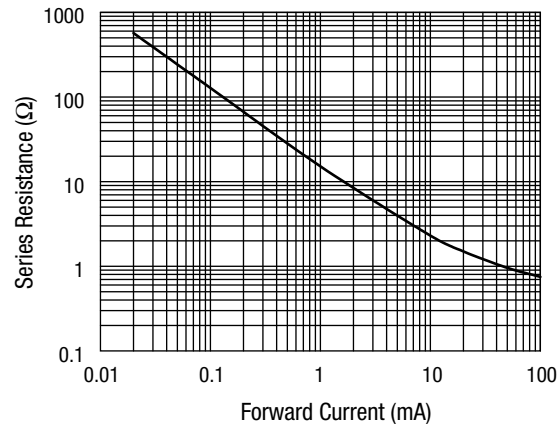
Typical Performance Data (0, +3 V)

SMP1340



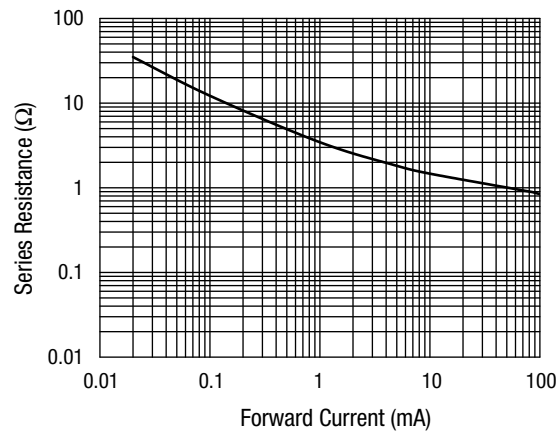
Series Resistance vs. Current @ 100 MHz

SMP1302



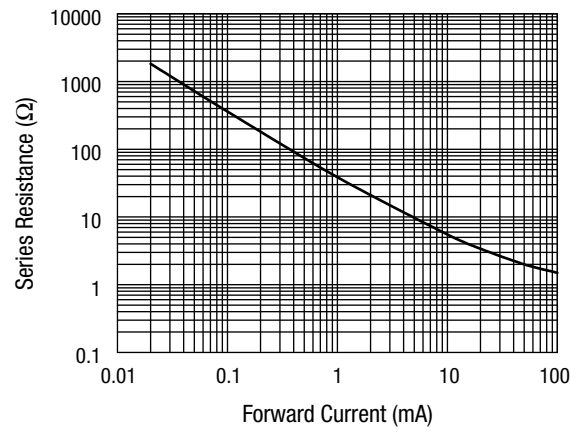
Series Resistance vs. Current @ 100 MHz

SMP1345



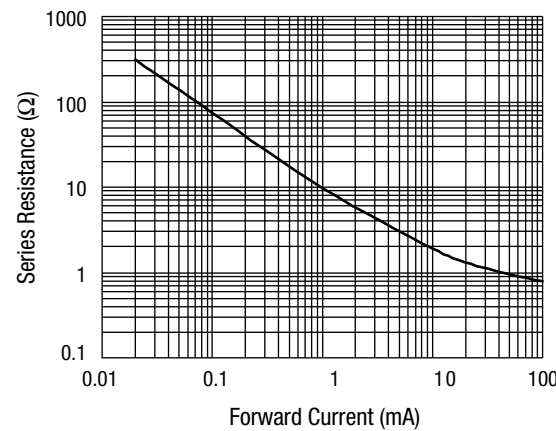
Series Resistance vs. Current @ 100 MHz

SMP1304

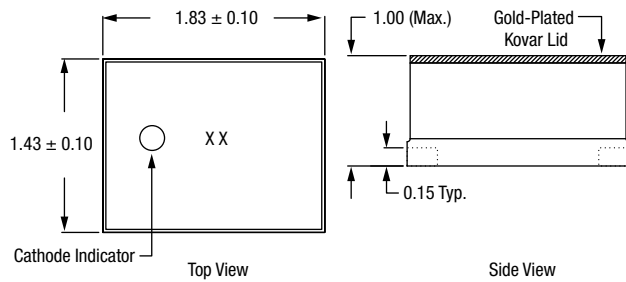
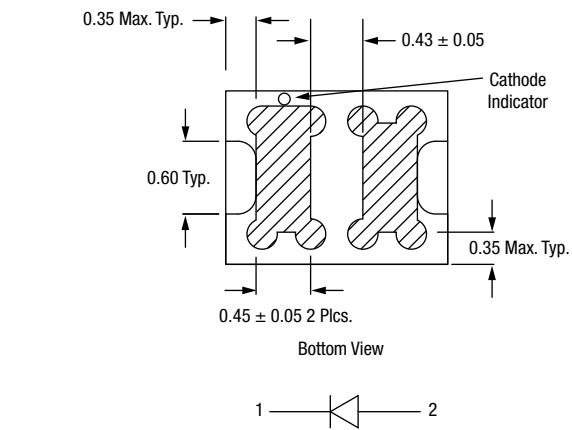


Series Resistance vs. Current @ 100 MHz

SMP1352

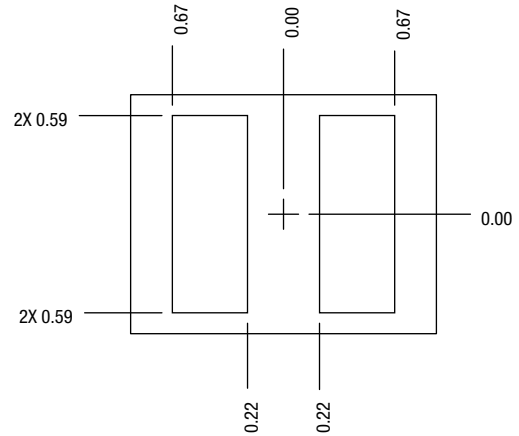


Series Resistance vs. Current @ 100 MHz

**-108 Package Outline**

All dimensions in mm

586-011

**-108 Land Pattern**

**DATA SHEET**

# PIN Diode Chips Supplied on Film Frame

**Applications**

- Switches
- Attenuators

**Features**

- Preferred device for module applications
- PIN diodes supplied 100% tested, saw cut, mounted on film frame
- Low cost
- Lead (Pb)-free, RoHS-compliant, and Green™

**Description**

The SMP series of PIN diodes is designed for high-volume switch applications from 10 MHz to beyond 2 GHz. The low-current, low-capacitance performance of these diodes makes the SMP series particularly suited for battery-operated circuits, power amplifier modules, VCO, T/R switches and other applications. The SMP1302-099 and SMP1304-099 parts are designed as low-distortion attenuators used in TV distribution and cellular base station applications.

**NEW** Skyworks Green™ products are RoHS (Restriction of Hazardous Substances)-compliant, conform to the EIA/EICTA/JEITA Joint Industry Guide (JIG) Level A guidelines, are halogen free according to IEC-61249-2-21, and contain <1,000 ppm antimony trioxide in polymeric materials.


**Absolute Maximum Ratings**

Characteristic	Value
Reverse voltage	Voltage rating
Power dissipation @ 25 °C at the base of the chip	250 mW
Storage temperature	-65 °C to +150 °C
Operating temperature	-65 °C to +150 °C
ESD human body model	Class 1 B

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum Ratings. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

**CAUTION:** Although these devices are designed to be robust, ESD (Electrostatic Discharge) can cause permanent damage. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.



**Electrical Specifications at 25 °C**

Part Number	Voltage Rating (V)	Typ. $C_J$ $V_R = 0$ V F = 1 MHz (pF)	Max. $C_J$ $V_R = 30$ V F = 1 MHz (pF)	Typ. $V_F$ @ $I_F = 10$ mA (mV)	Max. $R_S$ $I_F = 1$ mA F = 100 MHz ( $\Omega$ )	Max. $R_S$ $I_F = 10$ mA F = 100 MHz ( $\Omega$ )	Typ. $T_L$ $I_F = 10$ mA (nsec)
<b>Switching Applications</b>							
SMP1320-099	50	0.23	0.175	850	2 Typ.	0.9	400
SMP1321-099	100	0.18	0.15	860	3 Typ.	2	400
SMP1322-099	50	1.1	0.85	825	1.5	0.45 Typ.	400
SMP1340-099	50	0.2	0.15 @ 10 V	880	1.7 Typ.	1.2	100
SMP1353-099	100	0.35	0.15 @ 10 V	825	15	2.8	1000
<b>Attenuator Applications</b>							
SMP1302-099	200	0.27	0.15	800	20	3	700
SMP1304-099	200	0.18	0.15	800	50	7	1000

Reverse current is specified at 10  $\mu$ A maximum at the voltage rating. This voltage should not be exceeded.

The above PIN switch diode chips are processed on 100 mm silicon wafers, 100% DC tested, saw cut and shipped on 6" film frame hoops.

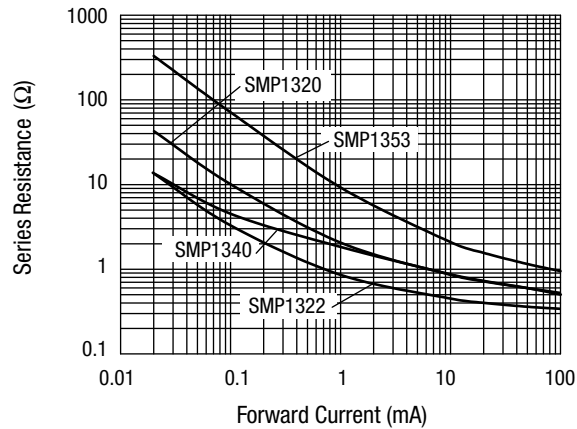
Electrical rejects are identified with black ink.

Attenuators 100%  $R_S$  tested @ 1 mA/100 MHz.

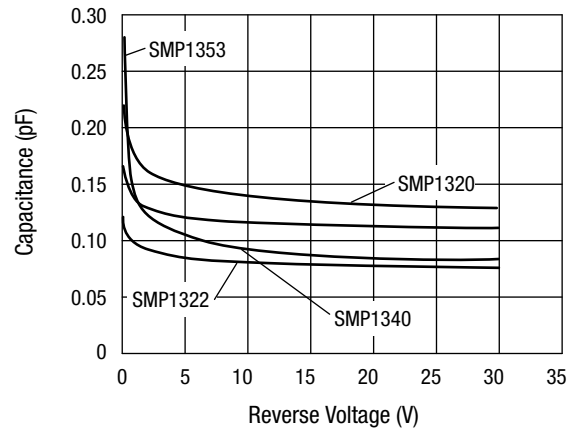
**Chip Dimensions**

Part Number	Quantity of Good Diodes Per Wafer		Chip Size (Inches)	Chip Height (Inches)	Anode Contact (Inches)
	Min.	Nom.			
SMP1320-099	40,000	46,000	0.0135 $\pm$ 0.001	0.0055 $\pm$ 0.0005	0.003 $\pm$ 0.0003
SMP1321-099	40,000	46,000	0.0135 $\pm$ 0.001	0.0055 $\pm$ 0.0005	0.003 $\pm$ 0.0003
SMP1322-099	40,000	46,000	0.0135 $\pm$ 0.001	0.0055 $\pm$ 0.0005	0.0075 $\pm$ 0.0003
SMP1340-099	65,000	72,000	0.011 $\pm$ 0.001	0.0055 $\pm$ 0.0005	0.003 $\pm$ 0.0003
SMP1353-099	65,000	72,000	0.011 $\pm$ 0.001	0.0055 $\pm$ 0.0005	0.008 $\pm$ 0.0005
SMP1302-099	40,000	46,000	0.0135 $\pm$ 0.001	0.0055 $\pm$ 0.0005	0.0085 $\pm$ 0.0005
SMP1304-099	40,000	46,000	0.0135 $\pm$ 0.001	0.01 $\pm$ 0.001	0.0085 $\pm$ 0.0005

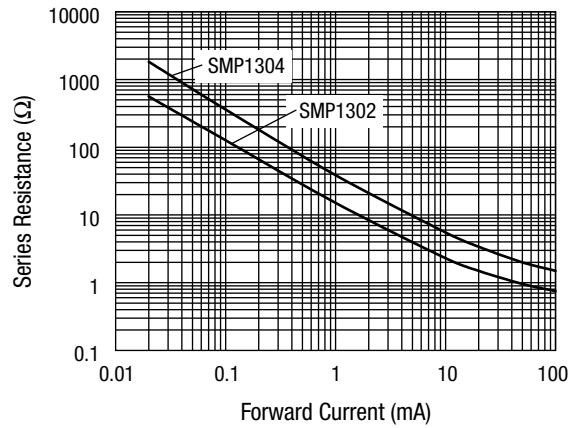
Typical Performance Data at 25 °C



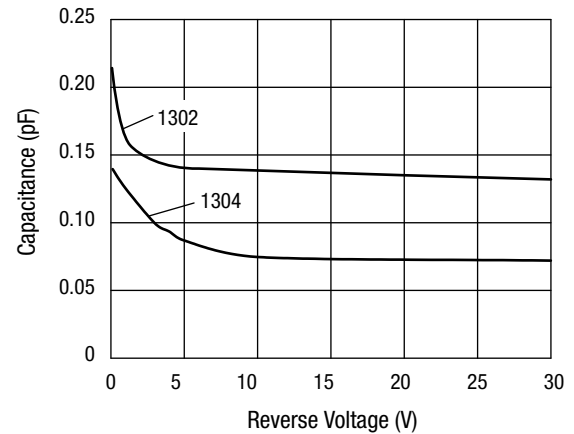
Series Resistance vs.  
Forward Current @ 100 MHz



Capacitance vs. Reverse Voltage

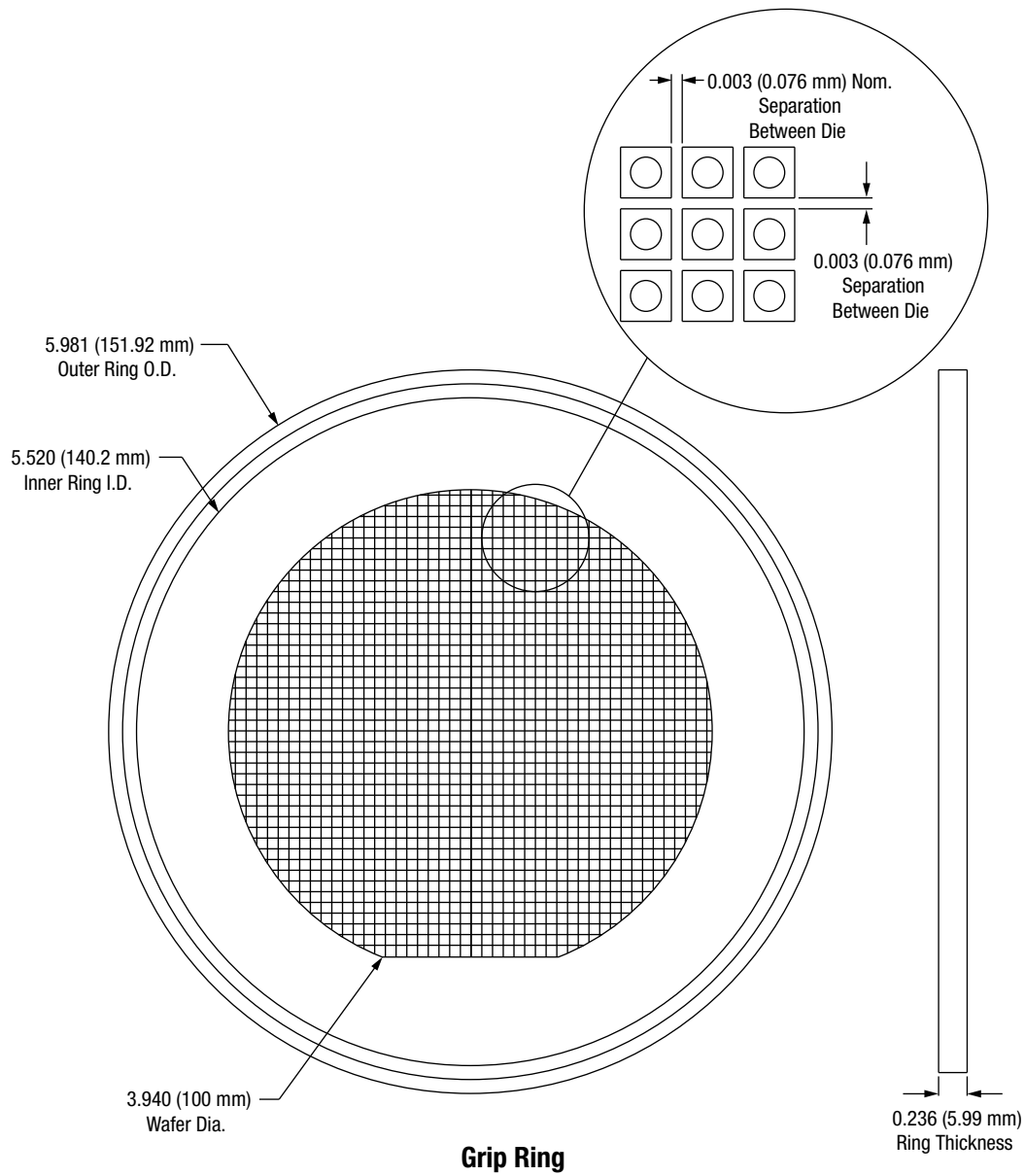


Series Resistance vs. Current @ 100 MHz



Capacitance vs. Reverse Voltage

## Wafer On Film



### Wafer Film Frame Description

- Wafer on nitto tape
- Color: light blue
- Thickness: 2.2–3 mils
- Tensile strength: 6.6 (lbs. in width)
- Ring material: plastic

**DATA SHEET**

# DSM8100-000: Mesa Beam-Lead PIN Diode

**Applications:**

- Designed for switching applications

**Features**

- Low capacitance
- Low resistance
- Fast switching
- Oxide-nitride passivated
- Durable construction
- Lead (Pb)-free, RoHS-compliant, and Green™


**Description**

Skyworks Silicon Mesa Beam-Lead PIN diode is surrounded by a glass frame for superior strength and electrical performance that surpasses the standard beam-lead PINs. The DSM8100-000 is designed for low resistance, low capacitance and fast switching time. The oxide-nitride passivation layers provide reliable operation and stable junction parameters that provide complete sealing of the junction permitting use in assemblies with some degree of moisture sealing. A layer of glass provides increased mechanical strength.

The DSM8100 is designed for microstrip or stripline circuits and for circuits requiring high isolation from a series-mounted diode such as broadband multithrow switches, phase shifters, limiters, attenuators and modulators.

**NEW**


Skyworks Green™ products are RoHS (Restriction of Hazardous Substances)-compliant, conform to the EIA/EICTA/JEITA Joint Industry Guide (JIG) Level A guidelines, are halogen free according to IEC-61249-2-21, and contain <1,000 ppm antimony trioxide in polymeric materials.

**Absolute Maximum Ratings**

Characteristic	Value
Operating temperature	-65 °C to +150 °C
Storage temperature	-65 °C to +200 °C
Power dissipation (derate linearly to zero @ 175 °C)	250 mW
Typical lead strength	8 grams pull
Reverse voltage	60 V

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum Ratings. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

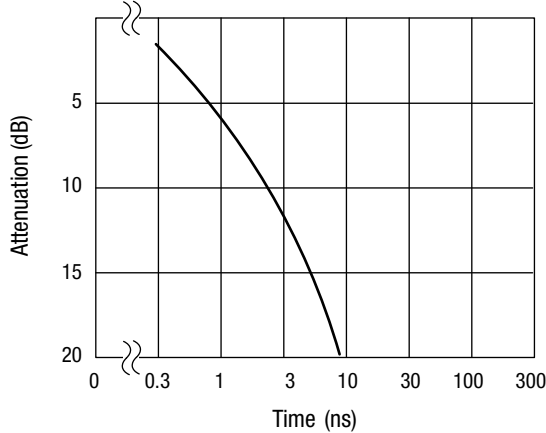
**CAUTION:** Although these devices are designed to be robust, ESD (Electrostatic Discharge) can cause permanent damage. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.

# Mesa Beam-Lead Diode Specifications

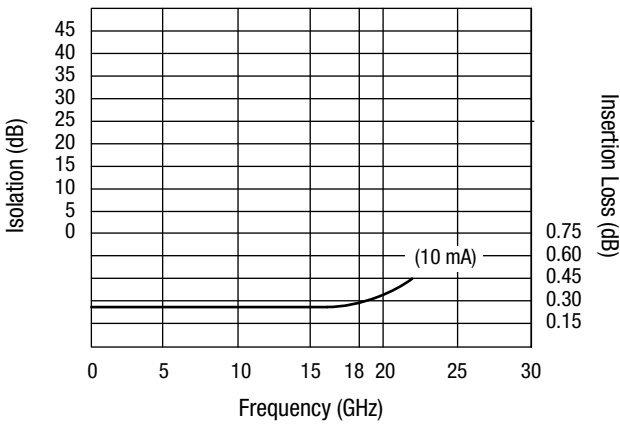
Part Number	Min. Voltage Rating <sup>(1)</sup> (V)	Max. Total Capacitance 10 V, 1 MHz (pF)	Max. Series Resistance 10 mA, 100 MHz ( $\Omega$ )	Typ. $T_L$ $I_F = 10$ mA (ns)	Outline Drawing
DSM8100-000	60	0.025	3.5	25	389-003

1. Reverse current is specified at 10  $\mu$ A maximum at the voltage rating. This voltage should not be exceeded.

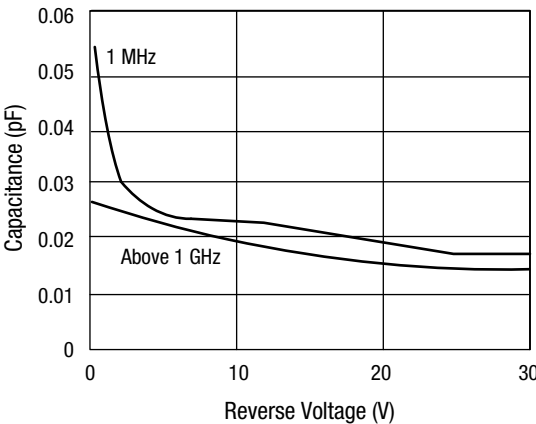
## Typical Performance Data



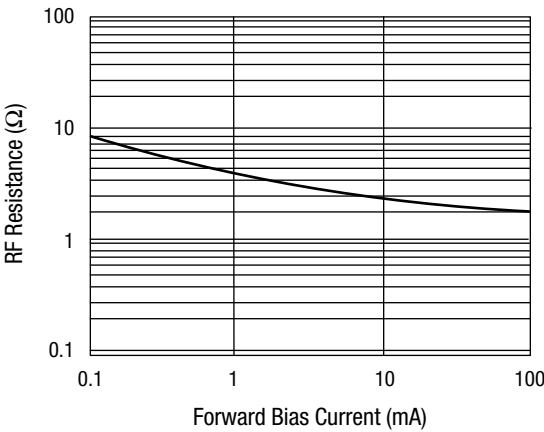
Switching Time Data



Typical Isolation and Insertion Loss Characteristics

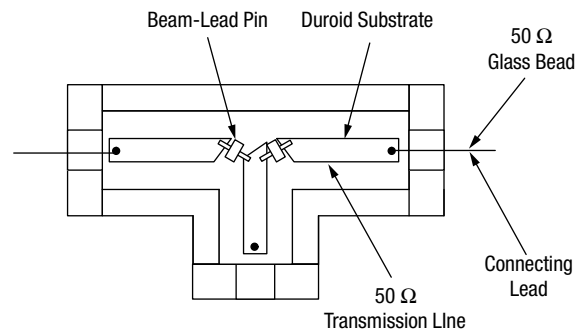


Typical Capacitance vs. Reverse Voltage

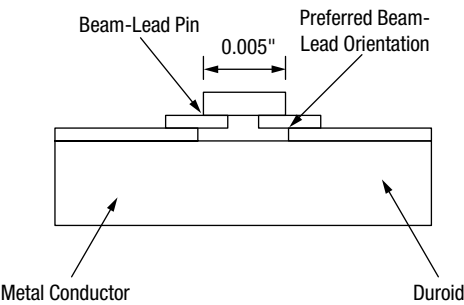


Typical RF Resistance vs. Forward Bias Current

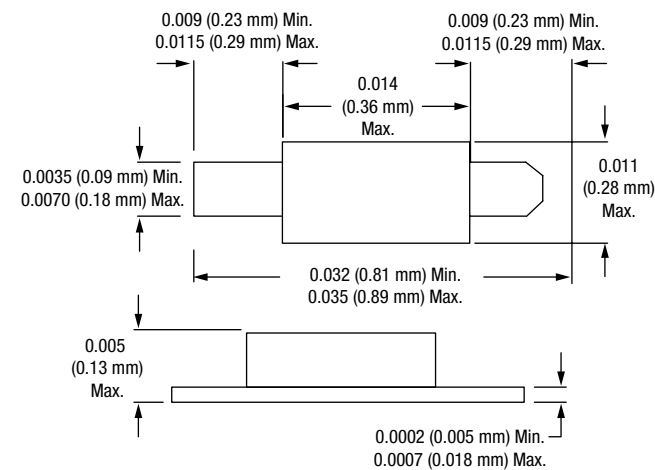
Typical SPDT Circuit Arrangement



Typical Beam-Lead Mounting



389-003





## Beam-Lead Diodes

### Handling

Due to their small size, beam-lead devices are fragile and should be handled with extreme care. The individual plastic packages should be handled and opened carefully, so that no undue mechanical strain is applied to the packaged device. It is recommended that the beam-lead devices be handled through use of a vacuum pencil using an appropriate size vacuum needle or a pointed wooden stick such as a sharpened Q-tip or match stick. The device will adhere to the point and can easily be removed from the container and positioned accurately for bonding without damage. Such handling should be done under a binocular microscope with magnification in the range of 20X to 30X.

Special handling precautions are also required to avoid electrical damage, such as static discharge.

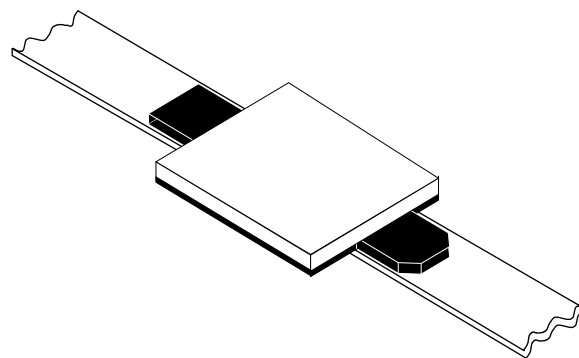
### Bonding

The DSM8100-000 can best be bonded to substrates by means of thermocompression bonding. Essentially this type of bonding involves pressing the gold beam of the device against the gold-plated metalized substrate under proper conditions of heat and pressure so that a metallurgical bond joint between the two occurs.

### Procedure

The beam-lead devices to be bonded should be placed on a clean, hard surface such as a microscope slide. It is recommended that the beam side of the device be down so that this side will be toward the substrate when bonded. The device can be picked up by pressing lightly against one beam with the heated tip. The substrate can then be appropriately positioned under the tip and the device brought down against the substrate, with proper pressure applied by means of the weld head.

A bonding tip temperature in the 350 °C to 450 °C range is recommended along with a bonding force of 50 to 70 grams. The bonding time is in the range of 2 to 3 seconds. Optimum bonding conditions should be determined by trial and error to compensate for slight variations in the condition of the substrate, bonding tip, and the type of device being bonded.



### Equipment

The heat and pressure are obtained through use of a silicon carbide bonding tip with a radius of two to three mils. Such an item is available from several commercial sources. In order to supply the required tip-travel and apply proper pressure, a standard miniature weld head can be used. Also available is a heated wedge shank which is held by the weld head and in turn holds the tip and supplies heat to it. The wedge shank is heated by means of a simple AC power supply or a pulse-type heated tool.

### Substrate

For optimum bonding, a gold-plated surface at least 100-micro-inches thick is necessary. Although it is possible to bond to relatively soft metalized substrate material such as epoxy-fiber-glass, etc., optimum bonding occurs when a hard material such as ceramic can be used.

### Quality

If a good bond has been obtained, it is impossible to separate the beam-lead device from the metalized substrate without damage. If the device is destructively removed, the beam will tear away, leaving the bonded portion attached to the substrate.

### Beam-Lead Packaging

The DSM8100-000 is shipped in 2" x 2" black gel packs. The beam-leads are mounted on the gel, and the devices are covered with a piece of lint-free release paper, on top of which is placed a piece of conductive foam.

**DATA SHEET**

# DSG9500-000: Planar Beam-Lead PIN Diode

**Applications**

- Designed for switching applications

**Features**

- Low capacitance
- Low resistance
- Fast switching
- Oxide-nitride passivated
- Durable construction
- High voltage
- Lead (Pb)-free, RoHS-compliant, and Green™

**Description**

The DSG9500-000 silicon planar beam-lead PIN diode is designed for low resistance, low capacitance and fast switching time.

The oxide-nitride passivation layers protect the diode junction to provide excellent reliability and stable electrical performance, especially when the diode is housed in a hermetically sealed assembly to further protect the junction from moisture.

The DSG9500-000 is designed for microstrip or stripline circuits and for circuits requiring high isolation from a series-mounted diode such as broadband multithrow switches, phase shifters, limiters, attenuators and modulators.

**NEW**


Skyworks Green™ products are RoHS (Restriction of Hazardous Substances)-compliant, conform to the EIA/EICTA/JEITA Joint Industry Guide (JIG) Level A guidelines, are halogen free according to IEC-61249-2-21, and contain <1,000 ppm antimony trioxide in polymeric materials.


**Absolute Maximum Ratings**

Characteristic	Value
Operating temperature	-65 °C to +150 °C
Storage temperature	-65 °C to +200 °C
Power dissipation (derate linearly to zero @ 175 °C)	250 mW
Typical lead strength	8 grams pull
Reverse voltage	100 V

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum Ratings. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

**CAUTION:** Although these devices are designed to be robust, ESD (Electrostatic Discharge) can cause permanent damage. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.

# Electrical Specifications

Part Number	Voltage Rating <sup>(1)</sup> (V)	$C_T$ 50 V, 1 MHz (pF)	$R_S$ 50 mA, 100 MHz ( $\Omega$ )	$T_L$ $I_F = 10$ mA (ns)	RF Switching Time $T_S$ (ns) <sup>(2)</sup>	Outline Drawing
		Max.	Max.	Typ.	Typ.	
DSG9500-000	100	0.025	4	250	25	169-001

1. Reverse current is specified at 10  $\mu$ A maximum at the voltage rating. This voltage should not be exceeded.  
 2.  $T_S$  measured from RF transition, 90% to 10%, in series configuration.

# Performance Data for DSG9500-000

Figures 1 and 2 show a single pole double throw 1–18 GHz switch. These diodes are mounted on Alumina, Duroid, or Teflon fiberglass 50  $\Omega$  microstrip circuits. Typical bonding methods include thermal compression bonding, parallel gap welding, and soldering.

SPDT isolation curves are shown in Figure 3, and insertion loss in Figures 4 and 5. With proper transitions and bias circuits, VSWR is better than 2.0 to 1 through 18 GHz.

# Switching Considerations

The typical minority carrier lifetime of the DSG9500 diodes is 250 ns. With suitable drivers, the individual diodes can be switched from high impedance (off) to low  $R_S$  (on) in about 10 ns.

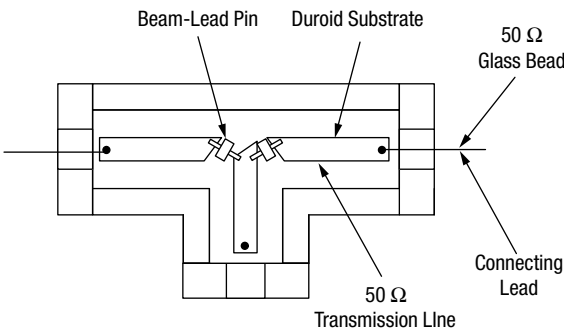


Figure 1. Typical SPDT Circuit Arrangement

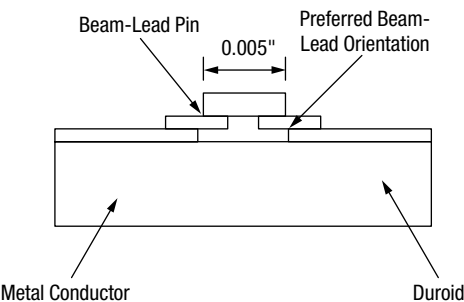


Figure 2. Typical Beam-Lead Mounting

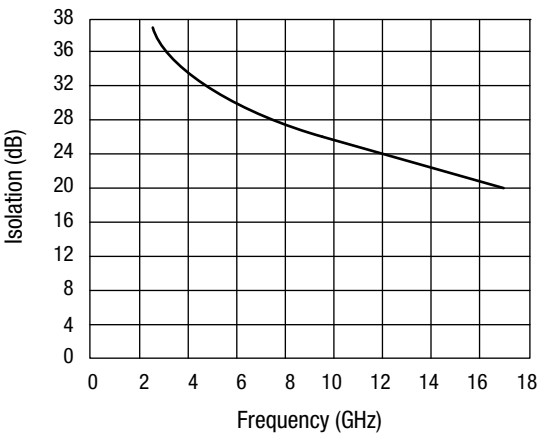


Figure 3. Isolation vs. Frequency, SPDT

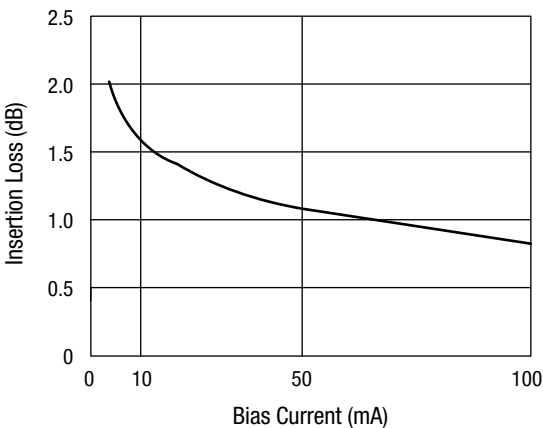


Figure 4. Diode Insertion Loss vs. Bias, SPST 18 GHz

Power Handling for DSG9500-000

Beam-lead diodes are not suitable for high-power operation because of high internal thermal impedance of about 600 °C/W.

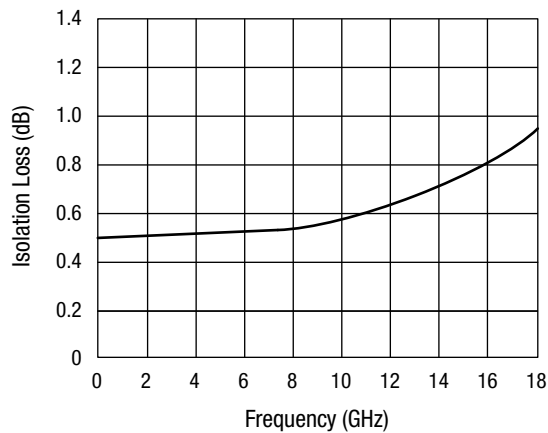


Figure 5. Diode Insertion Loss vs. Frequency, SPST,  $I_F = 50\text{ mA}$

With maximum CW power dissipation of 250 mW, the DSG9500-000 diodes are normally rated at 2 W incident CW with linear derating between 25 °C and 150 °C.

For pulsed operation, the total RF plus bias voltage must not exceed the rated breakdown. Skyworks has made high-power tests at 1 GHz with 1  $\mu\text{s}$  pulses, 0.001 duty, with 100 V diodes. With 50 mA forward bias, there is no increase in insertion loss over the 0 dBm level with a peak power input of 50 W. In the open state, reverse bias voltage is required to minimize distortion, which may decrease isolation and cause possible failure. Figure 6 shows allowed peak power versus reverse bias at 1 GHz.

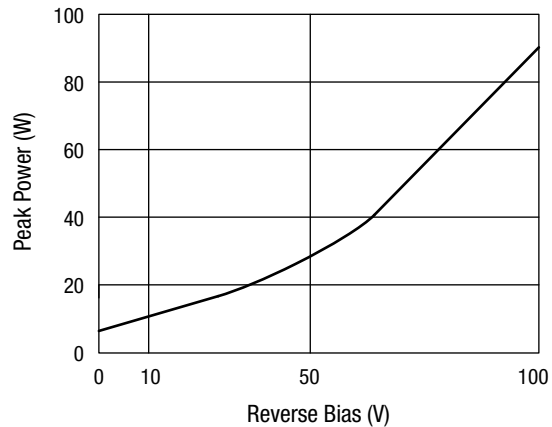
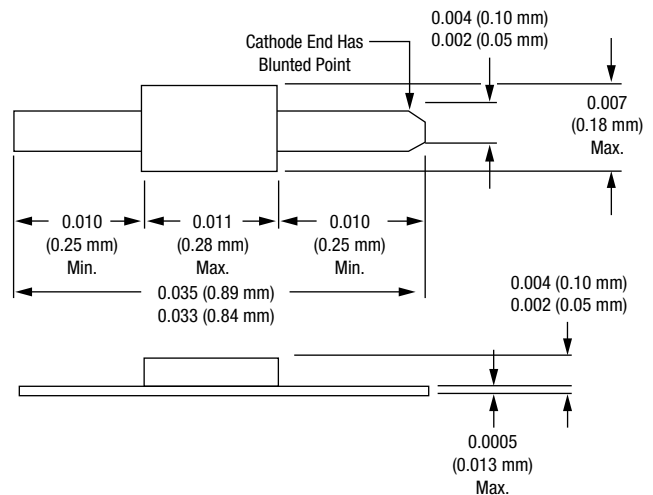


Figure 6. Peak Power Handling, SPST 1 GHz

169-001



## Beam-Lead Diodes

### Handling

Due to their small size, beam-lead devices are fragile and should be handled with extreme care. The individual plastic packages should be handled and opened carefully, so that no undue mechanical strain is applied to the packaged device. It is recommended that the beam-lead devices be handled through use of a vacuum pencil using an appropriate size vacuum needle or a pointed wooden stick such as a sharpened Q-tip or match stick. The device will adhere to the point and can easily be removed from the container and positioned accurately for bonding without damage. Such handling should be done under a binocular microscope with magnification in the range of 20X to 30X.

Special handling precautions are also required to avoid electrical damage, such as static discharge.

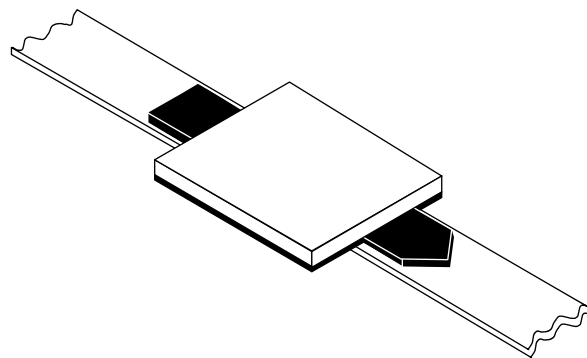
### Bonding

The DSG9500-000 can best be bonded to substrates by means of thermocompression bonding. Essentially this type of bonding involves pressing the gold beam of the device against the gold-plated metalized substrate under proper conditions of heat and pressure so that a metallurgical bond joint between the two occurs.

### Procedure

The beam-lead devices to be bonded should be placed on a clean, hard surface such as a microscope slide. It is recommended that the beam side of the device be down so that this side will be toward the substrate when bonded. The device can be picked up by pressing lightly against one beam with the heated tip. The substrate can then be appropriately positioned under the tip and the device brought down against the substrate, with proper pressure applied by means of the weld head.

A bonding tip temperature in the 350 °C to 450 °C range is recommended along with a bonding force of 50 to 70 grams. The bonding time is in the range of 2 to 3 seconds. Optimum bonding conditions should be determined by trial and error to compensate for slight variations in the condition of the substrate, bonding tip, and the type of device being bonded.



### Equipment

The heat and pressure are obtained through use of a silicon carbide bonding tip with a radius of two to three mils. Such an item is available from several commercial sources. In order to supply the required tip-travel and apply proper pressure, a standard miniature weld head can be used. Also available is a heated wedge shank which is held by the weld head and in turn holds the tip and supplies heat to it. The wedge shank is heated by means of a simple AC power supply or a pulse-type heated tool.

### Substrate

For optimum bonding, a gold-plated surface at least 100-micro-inches thick is necessary. Although it is possible to bond to relatively soft metalized substrate material such as epoxy-fiber-glass, etc., optimum bonding occurs when a hard material such as ceramic can be used.

### Quality

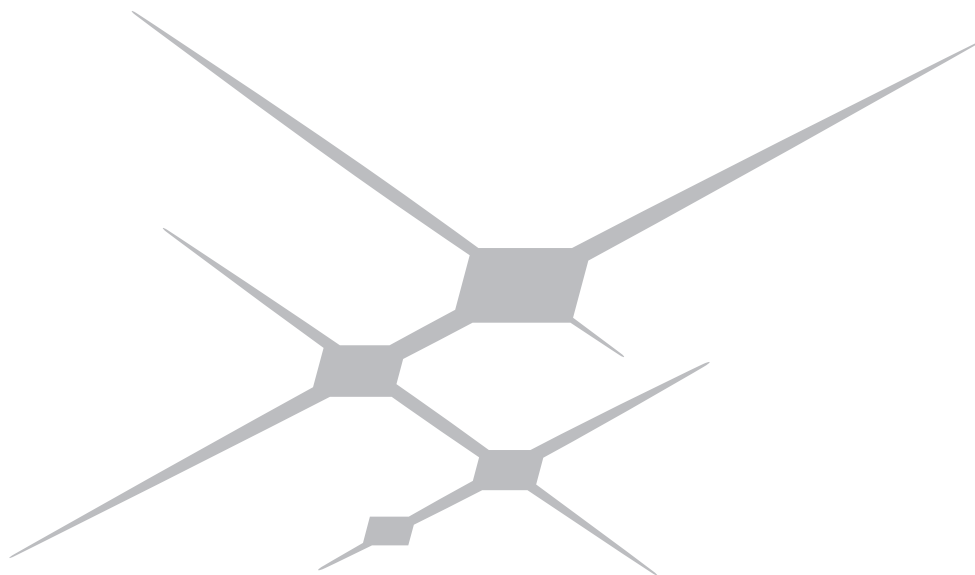
If a good bond has been obtained, it is impossible to separate the beam-lead device from the metalized substrate without damage. If the device is destructively removed, the beam will tear away, leaving the bonded portion attached to the substrate.

### Beam-Lead Packaging

The DSG9500-000 is shipped in 2" x 2" black gel packs. The beam-leads are mounted on the gel, and the devices are covered with a piece of lint-free release paper, on top of which is placed a piece of conductive foam.







**LIMITER DIODES**

Silicon Limiter Diodes, Packaged and Bondable Chips ..... 30

**DATA SHEET**

# CLA Series: Silicon Limiter Diodes Packaged and Bondable Chips

## Applications

- Limiters

## Features

- Established Skyworks limiter diode process
- High-power, mid-range and cleanup designs
- Low insertion loss (0.1 dB at 10 GHz)
- Power handling to 66 dBm
- Tight control of basewidth
- Mesa and planar chip designs
- Lead (Pb)-free, RoHS-compliant, and Green™

## Description

Skyworks CLA series of silicon limiter diodes provides passive receiver protection over a wide range of frequencies from 100 MHz to beyond 30 GHz. These devices utilize Skyworks well-established silicon technology for high resistivity and tightly controlled thin base width PIN limiter diodes. Limiter circuits employing these devices will perform with strong limiting action and low loss.

The CLA series consists of eight individual chip designs of different intrinsic region basewidths and capacitances designed to accommodate multistage limiter applications. The mesa constructed, thin basewidth, low capacitance CLA4601-000, CLA4602-000, CLA4604-000 and CLA4605-000 are designed for low-level and cleanup applications. The CLA4603-000, and CLA4606-000 through CLA4608-000 are planar designs designed for high-power and mid-range applications.

**NEW** Skyworks Green™ products are RoHS (Restriction of Hazardous Substances)-compliant, conform to the EIA/EICTA/JEITA Joint Industry Guide (JIG) Level A guidelines, are halogen free according to IEC-61249-2-21, and contain <1,000 ppm antimony trioxide in polymeric materials.



## Absolute Maximum Ratings

Characteristic	Value
Power dissipation	$P_{diss} = \frac{175 - T_{amb}}{\theta} W$
For CW signals	$\theta = \theta_{ave}$
For pulsed signals	$\theta = DF \times \theta_{ave} + \theta_{pulse}$ ( $\theta_p$ @ 1 $\mu s$ x normalized $\theta_p$ from figure 2)
Operating temperature	-65 °C to +175 °C
Storage temperature	-65 °C to +200 °C

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum Ratings. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

**CAUTION:** Although these devices are designed to be robust, ESD (Electrostatic Discharge) can cause permanent damage. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.

## Electrical Specifications at 25 °C

Part Number	Breakdown Voltage (V)	I Region (μm)	C <sub>J</sub> @ 0 V (pF)	C <sub>J</sub> @ 6 V (pF)	R <sub>S</sub> @ 10 mA (Ω)	T <sub>L</sub> @ 10 mA (ns)	Thermal Impedance (θ)		Top Contact Diam. (mils/mm)	Outline Drawing
	Min. – Max.	Nominal	Typ.	Max.	Max.	Typ.	Average (°C/W)	1 μs Pulse (°C/W)	Typ.	
CLA4601-000	15–30	1	0.12	0.1	2.5	5	120	15	1.2/0.03	150-806
CLA4602-000	15–30	1	0.2	0.15	2	5	80	10	1.5/0.038	150-806
CLA4603-000	20–45	1.5	0.2	0.15	2	5	100	10	1.5/0.038	149-815
CLA4604-000	30–60	2	0.12	0.1	2.5	7	100	10	1.5/0.038	150-806
CLA4605-000	30–60	2	0.2	0.15	2	7	70	7	2.5/0.064	150-813
CLA4606-000	45–75	2.5	0.2	0.15	2	10	80	7	2.5/0.064	149-815
CLA4607-000	120–180	7	0.2	0.15 @ 50 V	2	50	40	1.2	3/0.076	149-815
CLA4608-000	120–180	7	0.8	0.5 @ 50 V	1.2	100	15	0.3	5/0.127	149-815

Capacitance, C<sub>J</sub>, specified at 1 MHz.Resistance, R<sub>S</sub>, measured at 500 MHz.

CW thermal resistance for infinite heat sink.

Pulse thermal resistance for single 1 μs pulse.

## Typical Performance at 25 °C

Part Number	Insertion Loss @ -10 dBm (dB)	Input Power for 1 dB Loss (dBm)	Maximum Pulsed Input Power (dBm)	Output at Max. Pulsed Input (dBm)	Maximum CW Input Power (W)	Recovery Time (ns)
CLA4601-000	0.1	7	47	21	2	5
CLA4602-000	0.1	7	50	24	3	5
CLA4603-000	0.1	10	50	22	2	10
CLA4604-000	0.1	12	47	24	3	10
CLA4605-000	0.1	12	50	27	4	10
CLA4606-000	0.1	15	53	27	3	20
CLA4607-000	0.1	20	60	39	6	50
CLA4608-000	0.2	20	66	44	15	100

Insertion loss for CLA4601-000 through CLA4607-000 at 10 GHz; insertion loss for CLA4608-000 at 5 GHz.

Limiter power results at 1 GHz for shunt connected, single limiter diode and DC return in 50 Ω line.

Maximum pulsed power for 1 μs pulse and 0.1% duty factor with chip at 25 °C heat sink. Derate linearly to 0 W at 175 °C.

Maximum CW input power at 25 °C heat sink. Derate linearly to 0 W at 175 °C.

Recovery time to insertion loss from limiting state.

Hermetic Packages

Hermetic Stripline 240	Typical $\theta_{JC}$ (°C/W)	Hermetic Pill 203	Typical $\theta_{JC}$ (°C/W)	Hermetic Pill 219	Typical $\theta_{JC}$ (°C/W)	Hermetic Pill 210	Typical $\theta_{JC}$ (°C/W)
CLA4601-240	200	CLA4601-203	150	CLA4601-219	200	CLA4601-210	140
CLA4602-240	160	CLA4602-203	110	CLA4602-219	160	CLA4602-210	100
CLA4603-240	180	CLA4603-203	130	CLA4603-219	180	CLA4603-210	120
CLA4604-240	160	CLA4604-203	130	CLA4604-219	180	CLA4604-210	120
CLA4605-240	150	CLA4605-203	100	CLA4605-219	150	CLA4605-210	90
CLA4606-240	160	CLA4606-203	110	CLA4606-219	160	CLA4606-210	100
CLA4607-240	120	CLA4607-203	70	CLA4607-219	120	CLA4607-210	60
CLA4608-240	100	CLA4608-203	45	CLA4608-219	100	CLA4608-210	35

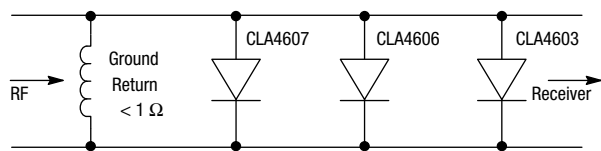


Figure 1. Cascaded Limiter Design

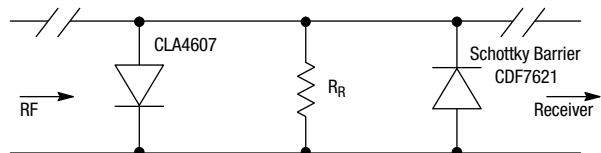


Figure 2. Quasi-Active Limiter

The CLA4603 and CLA4606 limiter diodes are constructed in a passivated flat-chip configuration and are available in a basic chip form or encapsulated in Skyworks -210 ceramic package.

Limiter diodes with lower capacitance values, to 0.08 pF, constructed with a passivated mesa configuration, are available in the CLA4601 and 4605 series. The mesa devices offer low  $C_J$ , and therefore broader bandwidth, lower loss, and faster response, at reduced power. These diodes are also available in chip package form, and represent the ultimate in limiter performance, not approached by other manufacturers. The CLA4607 diodes (highest power) are available in both planar and mesa construction.

Figures 3 and 4 illustrate the fundamental structures of diodes mounted in a 50  $\Omega$  microstrip circuit. The diode characteristics listed in the table refer to chips mounted in such a circuit. The designer can use these parameters in modeling the chip in any package, provided overall package parasitics are considered.

Additional bonding and handling methods are contained in Skyworks application notes.

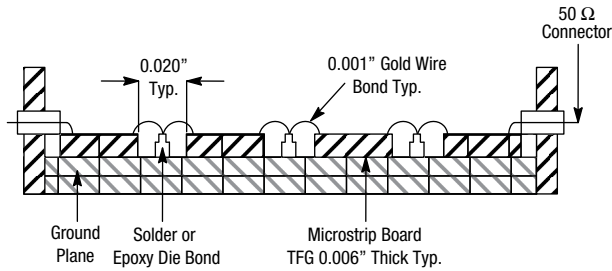


Figure 3. Side View

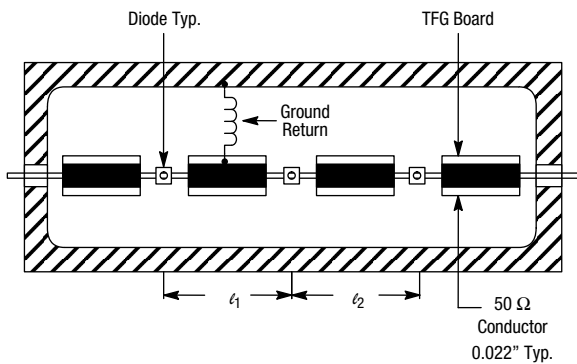


Figure 4. Top View

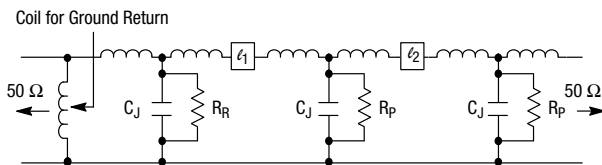


Figure 5. Low-Level Equivalent Circuit

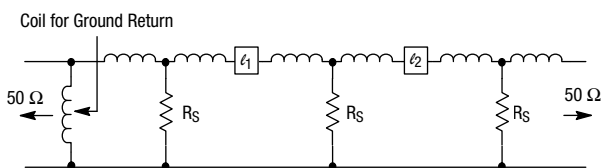


Figure 6. High-Power Equivalent Circuit

## Basic Application

When designing microstrip limiters, the bonding wire length and diameter, in conjunction with the chip capacitance, form a low pass filter (see Figure 5). Line lengths ( $L_1$  and  $L_2$ ) are varied to provide broadband matching and flat leakage characteristics. Typically,  $L_1$  and  $L_2$  are on the order of 0.1 wavelength. In Figure 1, the CLA4607 chip provides about 20 dB attenuation, reducing a 1 kW input to 10 W. The CLA4606 reduces this to 100 mW and the CLA4603 to about 20 mW.

During the rise time of the incident pulse, the diodes behave in the following manner. The CLA4603, due to its thin I region, is the first to change to a low impedance. Experiments indicate that the CLA4603 reaches the 10 dB isolation point in about 1 ns and 20 dB in 1.5 ns with an incident power of 10 W. The CLA4606 takes about 4 ns and the CLA4607 about 50 ns. Consequently, the CLA4603 provides protection during the initial stages of pulse rise time, with the thicker diodes progressively “turning on” as the power increases. With proper spacing ( $L_1$  and  $L_2$ ), the “on” diodes reflect high impedances to the upstream diodes, reducing the turn-on time for those diodes and ensuring that essentially all of the incident power is reflected by the input diode, preventing burnout of the thinner diodes. At the end of the pulse the process reverses, and the diodes “recover” to the high impedance state; the free charge which was injected in the I region by the incident power leaks off through the ground return and additionally is reduced by internal combination. With a ground return, recovery time is on the order of 50 ns. With a high impedance return, for example the circuit of Figure 2, the Schottky diodes recover or one “opens” in practically zero time, and internal recombination, on the order of several diode lifetimes, is the only available mechanism for recovery. This recovery time can be long—on the order of 1 ms for the CLA4607 series. The shunt resistor  $R_R$  minimizes the problem. One hundred ohms will approximately double the recovery time, compared to a short circuit.

When the Schottky diode is directly coupled to the transmission line, in cascade after the coarse limiter, the leakage power will be less than if a 0  $\Omega$  ground return were used. If the Schottky is decoupled too much, the leakage power increases, owing to the high DC impedance of a Schottky. Similarly, a 3.0  $\Omega$  ground return causes an increase of about 3 dB in leakage power compared to a 0  $\Omega$  return.

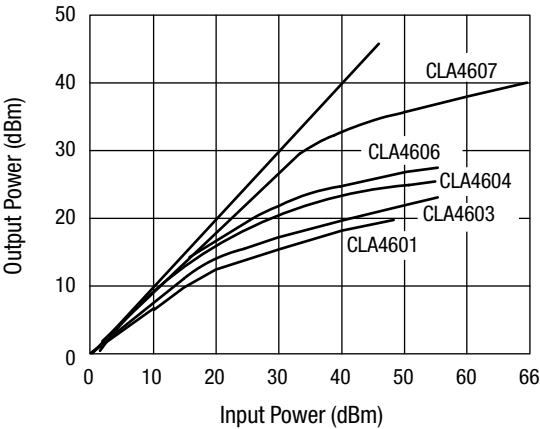


Figure 7. Typical Peak Leakage Power at 1 GHz

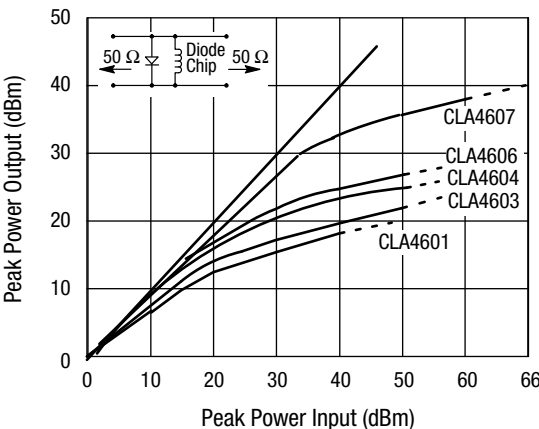


Figure 10. Typical Peak Leakage Power at 1 GHz

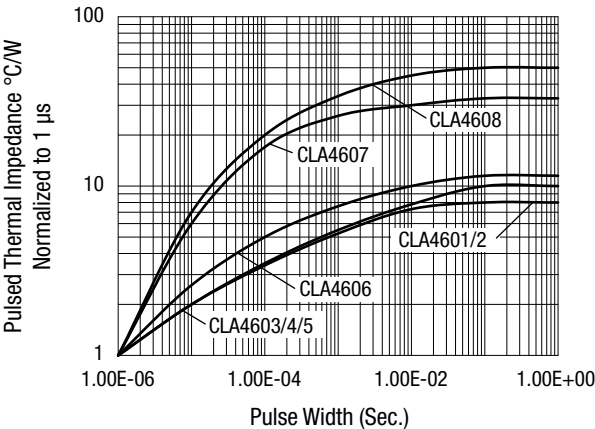


Figure 8. Normalized Pulsed Thermal Impedance

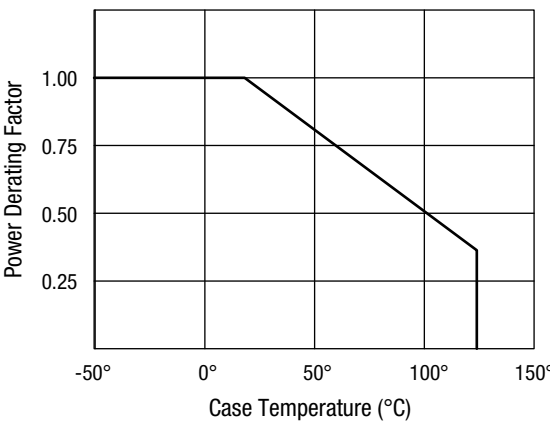


Figure 11. Power Handling Capability vs. Temperature

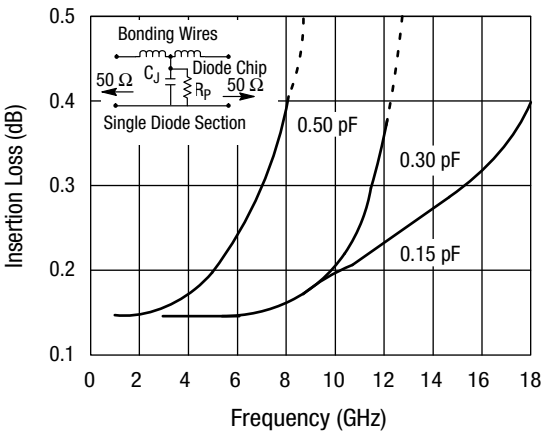
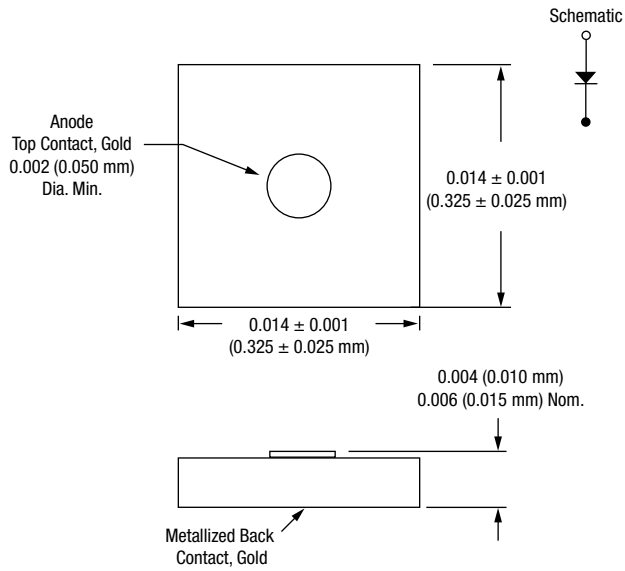
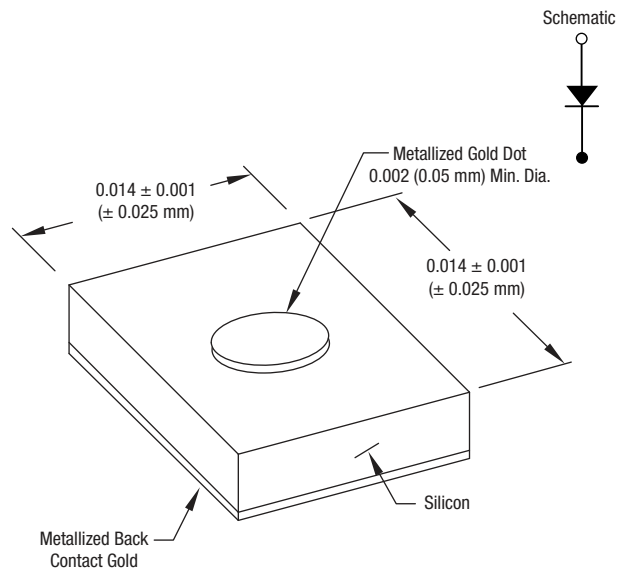
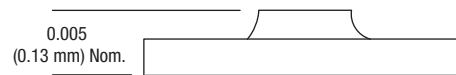
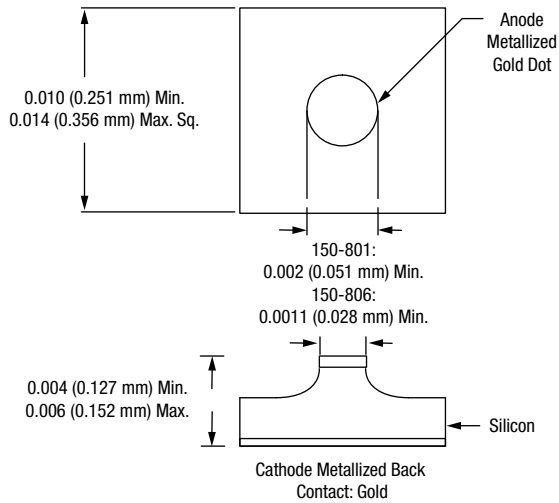
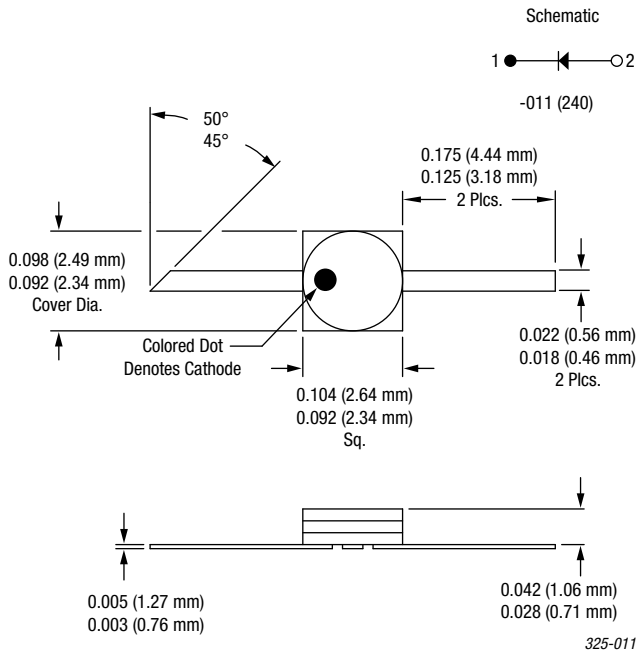


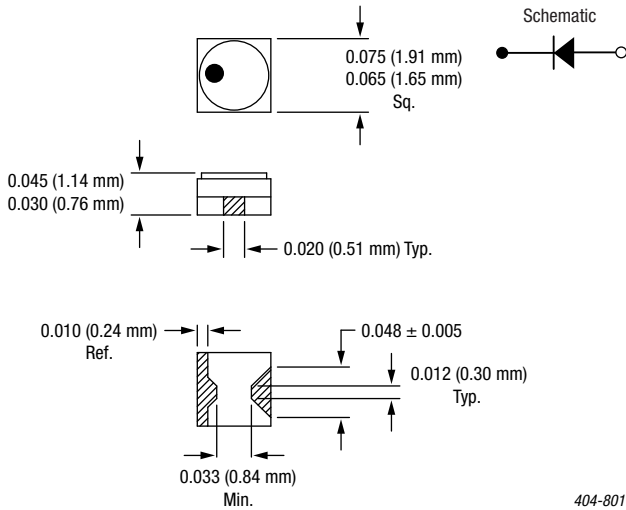
Figure 9. Typical Diode Insertion Loss vs. Frequency

**149-815****150-813****150 Series**

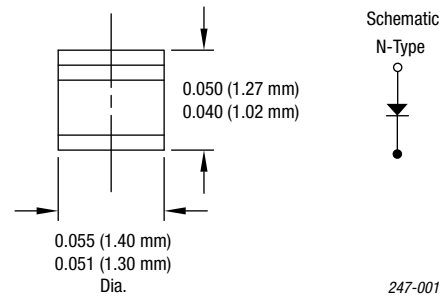
## -240



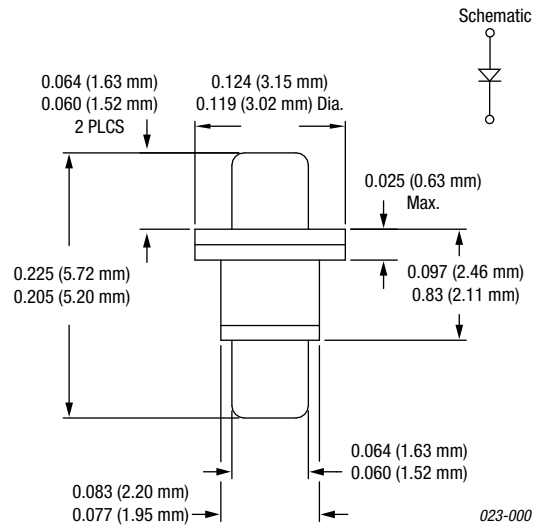
## -219



## -203



## -210







## VARACTOR DIODES

Silicon Abrupt Junction Varactors, Packaged and Bondable Chips .....	38
Silicon Abrupt Junction Tuning Varactors, Packaged and Bondable Mesa Chips .....	43
Silicon Hyperabrupt Junction Varactors, Packaged and Bondable Planar Chips.....	47
Silicon Tuning Varactors in Hermetic Surface Mount Package .....	51

**DATA SHEET**

# SMV1405–SMV1413: Silicon Abrupt Junction Varactors Packaged and Bondable Chips

## Applications

- For VCO applications 2.5 GHz and higher
- Voltage tuned filters
- Voltage variable phase shifters

## Features

- High Q
- Low series resistance for low phase noise
- Multiple chip and hermetic packages
- Lead (Pb)-free and RoHS-compliant MSL-1 @ 260 °C per JEDEC J-STD-020
- SPICE models are provided



## Description

The SMV1405–SMV1413 series of bare die, epoxy and hermetic packaged silicon abrupt junction varactor diodes is designed for use in VCOs requiring tight capacitance tolerances. The low resistance of these varactors makes them appropriate for high Q resonators in wireless system VCOs to frequencies beyond 2.5 GHz. The devices are characterized for capacitance over temperature. SPICE models are provided.

**NEW**

Skyworks offers lead (Pb)-free, RoHS (Restriction of Hazardous Substances)-compliant packaging.

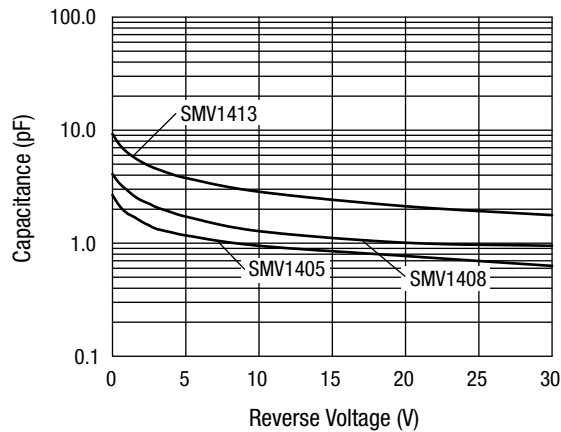
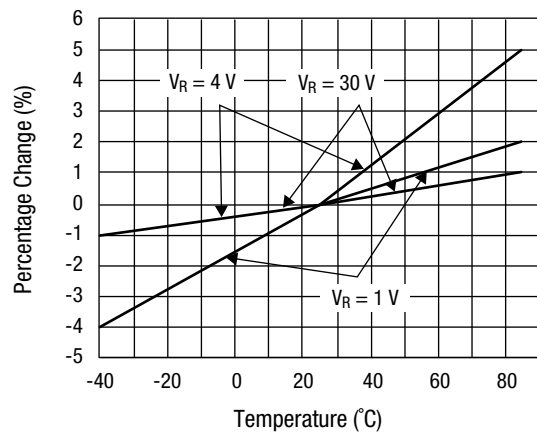


**Electrical Specifications at 25 °C Abrupt Junction Tuning Varactor Chips**

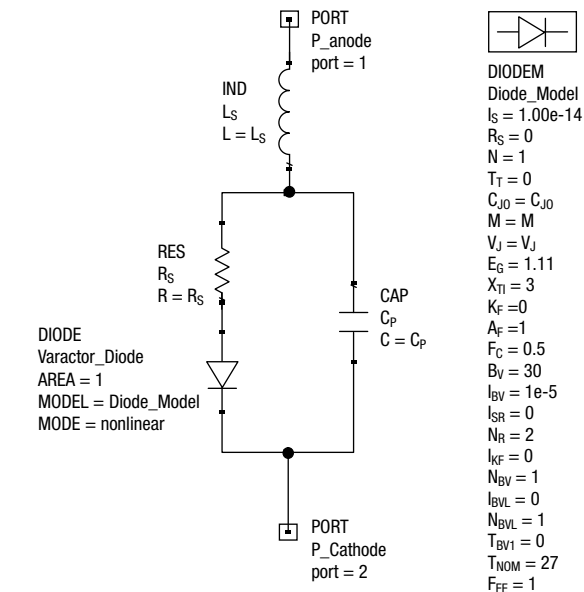
Part Number	Min. $V_B$ $I_R$ @ 10 $\mu A$ (V)	$C_T$ @ 4 V (pF)	Min. $C_T$ @ 0 V / $C_T$ @ 30 V (Ratio)	Max. $R_S$ @ 4 V 500 MHz ( $\Omega$ )	Typ. Q @ 4 V 50 MHz	Outline Drawing
SMV1405-000	30	1.08–1.32	4.1	0.80	3200	150-813
SMV1408-000	30	1.62–1.98	4.1	0.60	2900	150-813
SMV1413-000	30	3.59–4.29	4.2	0.35	2400	150-813

**Hermetic Packaged Abrupt Junction Tuning Varactor Chips**

Hermetic Stripline 240	Hermetic Pill 203	Stripline 219	Coaxial 210	Hermetic Surface Mount 108
SMV1405-240	SMV1405-203	SMV1405-219	SMV1405-210	SMV1405-108
SMV1408-240	SMV1408-203	SMV1408-219	SMV1408-210	
SMV1413-240	SMV1413-203	SMV1413-219	SMV1413-210	

**Typical Performance Data****Capacitance vs. Reverse Voltage****Relative Capacitance Change vs. Temperature**

SPICE Model



Part Number	$C_{J0}$ (pF)	$V_J$ (V)	M	$C_P$ (pF)	$R_S$ ( $\Omega$ )
SMV1405	2.7	0.68	0.41	0.05	0.8
SMV1408	3.7	0.8	0.48	0.13	0.6
SMV1413	9.2	0.79	0.45	0.13	0.35

Values extracted from measured performance.  
For package inductance ( $L_S$ ) refer to package type.  
For more details refer to the “Varactor SPICE Models for RF VCO Applications” Application Note.

Typical Capacitance Values

$V_R$ (V)	SMV1405 $C_T$ (pF)	SMV1408 $C_T$ (pF)	SMV1413 $C_T$ (pF)
0	2.67	4.08	9.24
0.5	2.12	3.36	7.39
1	1.84	2.94	6.37
1.5	1.7	2.6	5.71
2	1.55	2.38	5.22
2.5	1.44	2.24	4.85
3	1.34	2.08	4.55
4	1.25	1.88	4.1
5	1.17	1.72	3.77
10	0.95	1.28	2.85
20	0.77	1.01	2.12
30	0.63	0.95	1.77

Recommended Solder Reflow Profiles

Refer to the “*Recommended Solder Reflow Profile*” Application Note.

Tape and Reel Information

Refer to the “*Discrete Devices and IC Switch/Attenuators Tape and Reel Package Orientation*” Application Note.

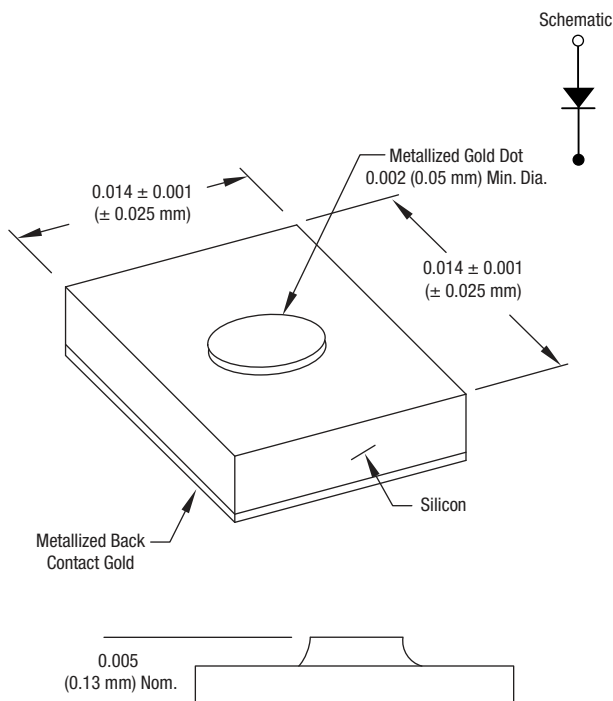
## Absolute Maximum Ratings

Characteristic	Value
Reverse voltage ( $V_R$ )	30 V
Forward current ( $I_F$ )	20 mA
Power dissipation ( $P_D$ )	250 mW
Storage temperature ( $T_{ST}$ )	-55 °C to +150 °C
Operating temperature ( $T_{OP}$ )	-55 °C to +125 °C
ESD human body model	Class 0

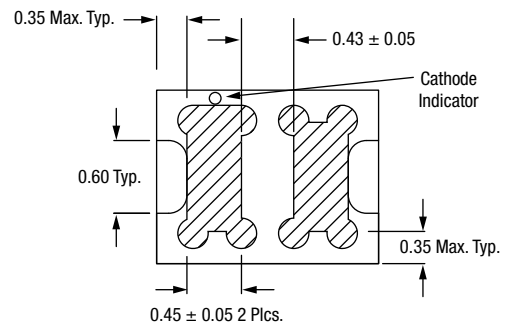
Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum Ratings. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

**CAUTION:** Although these devices are designed to be robust, ESD (Electrostatic Discharge) can cause permanent damage. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.

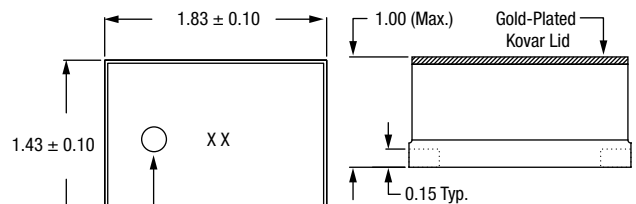
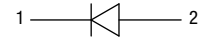
## 150-813



## -108



Bottom View



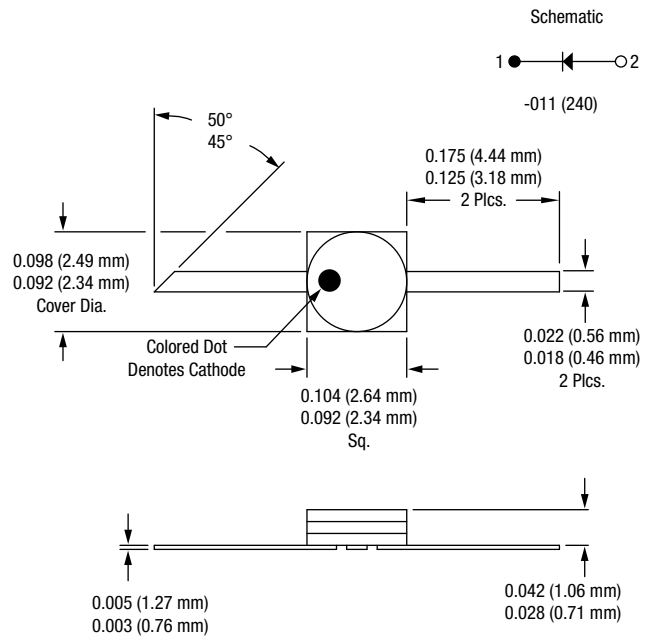
Top View

Side View

All dimensions in mm

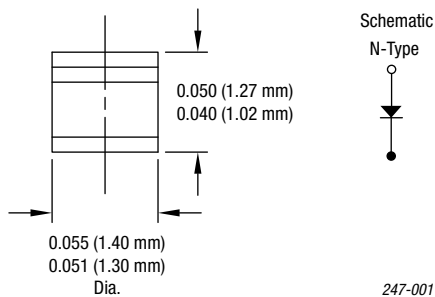
586-011

## -240

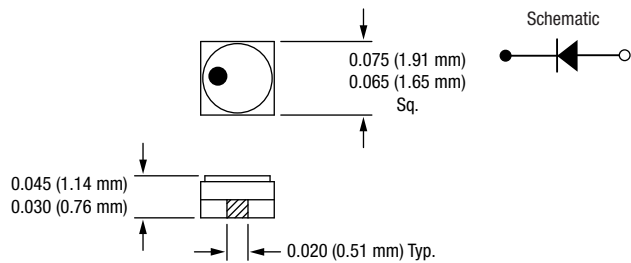


325-011

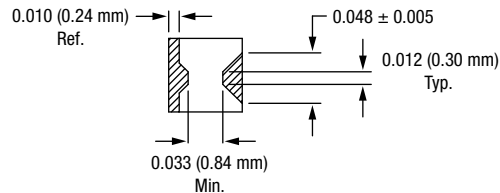
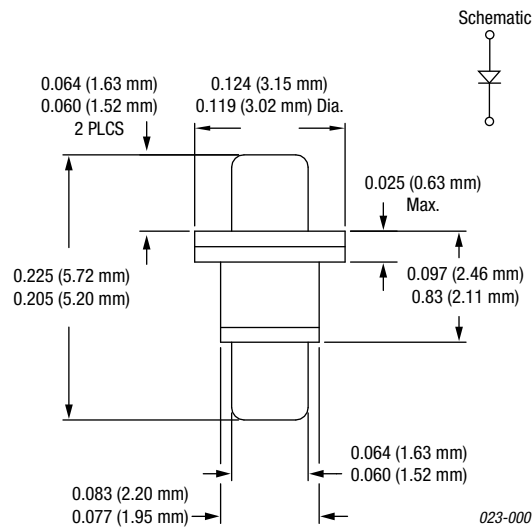
-203



-219



-210



404-801

**DATA SHEET**

# **SMV1493, SMV1494: Silicon Abrupt Junction Tuning Varactors Packaged and Bondable Mesa Chips**

**Applications**

- For RF and UHF VCO applications
- Voltage tuned filters
- Voltage variable phase shifters

**Features**

- High frequency to beyond 56 GHz
- Low series resistance for low phase noise
- Lead (Pb)-free and RoHS-compliant MSL-1 @ 260 °C per JEDEC J-STD-020
- SPICE models are provided


**Description**

The SMV1493 and SMV1494 bare die and hermetic packaged silicon abrupt junction varactor diodes are designed for use in VCOs requiring tight capacitance tolerances. The low resistance of these varactors makes them appropriate for high Q resonators in wireless system VCOs from RF to beyond 56 GHz.

**NEW** Skyworks offers lead (Pb)-free, RoHS (Restriction of Hazardous Substances)-compliant packaging.

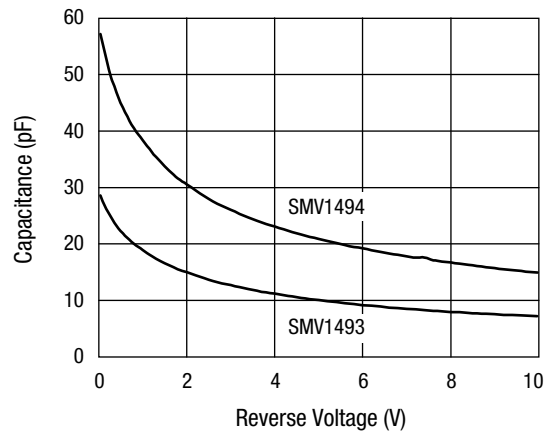

**Electrical Specifications at 25 °C**

Part Number	Min. $V_B$ $I_R$ @ 10 $\mu A$ (V)	$C_J$ @ 1 V (pF)	$C_J$ @ 4 V (pF)	Max. $R_S$ @ 1 V 500 MHz ( $\Omega$ )	Outline Drawing
SMV1493-000	12	17.4–20.0	9.87–11.97	0.50	150-802
SMV1494-000	12	36.3–41.7	20.57–25.07	0.45	150-802

**Hermetic Packages**

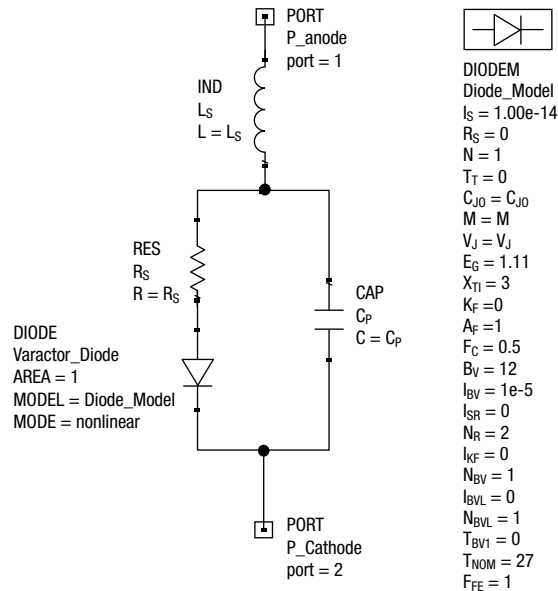
Hermetic Stripline 240	Hermetic Pill 203	Stripline 219	Coaxial 210
SMV1493-240	SMV1493-203	SMV1493-219	SMV1493-210
SMV1494-240	SMV1494-203	SMV1494-219	SMV1494-210

Typical Performance Data



Capacitance vs. Reverse Voltage

SPICE Model



Part Number	Cj0 (pF)	Vj (V)	M	Cp (pF)	Rs (Ω)
SMV1493	29	0.63	0.47	0	0.5
SMV1494	58	0.63	0.47	0	0.45

Values extracted from measured performance.  
For package inductance (Ls) refer to package type.  
For more details refer to the “Varactor SPICE Models for RF VCO Applications” Application Note.

Capacitance vs. Reverse Voltage

VR (V)	SMV1493	SMV1494
	CT (pF)	CT (pF)
0	28.7	57.8
0.2	25.6	51.5
0.4	23.3	46.9
0.6	21.5	43.4
0.8	20.1	40.5
1	19	38.4
1.2	17.9	36.3
1.4	17	34.6
1.6	16.2	33
1.8	15.5	31.6
2	15	30.6
2.2	14.4	29.5
2.4	13.9	28.5
2.6	13.5	27.6
2.8	13.1	26.7
3	12.7	26.1
3.2	12.4	25.3
3.4	12	24.7
3.6	11.7	24.1
3.8	11.4	23.5
4	11.2	23.1
4.2	10.9	22.6
4.4	10.7	22.1
4.6	10.5	21.7
4.8	10.3	21.3
5	10.1	20.9
6	9.2	19.2
7	8.5	17.9
8	8	16.7
9	7.6	15.7
10	7.1	14.7

Recommended Solder Reflow Profiles

Refer to the “Recommended Solder Reflow Profile” Application Note.

Tape and Reel Information

Refer to the “Discrete Devices and IC Switch/Attenuators Tape and Reel Package Orientation” Application Note.



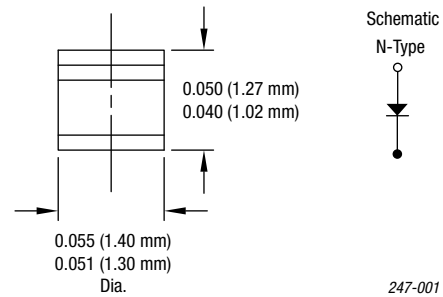
## Absolute Maximum Ratings

Characteristic	Value
Forward current ( $I_F$ )	20 mA
Power dissipation ( $P_D$ )	250 mW
Storage temperature ( $T_{ST}$ )	-55 °C to +150 °C
Operating temperature ( $T_{OP}$ )	-55 °C to +125 °C
ESD human body model	Class 0

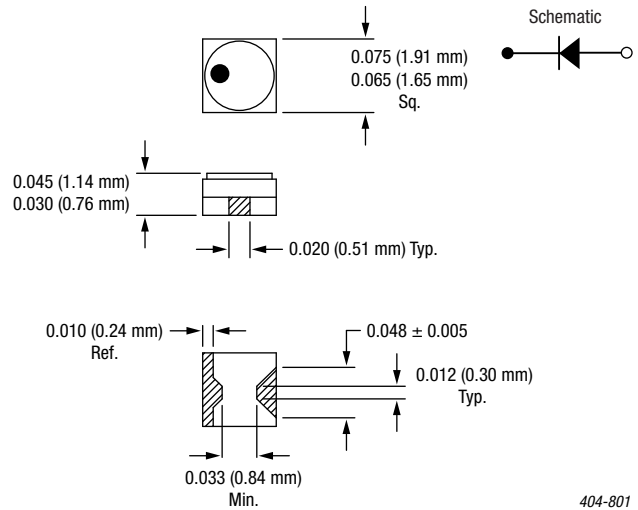
Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum Ratings. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

**CAUTION:** Although these devices are designed to be robust, ESD (Electrostatic Discharge) can cause permanent damage. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.

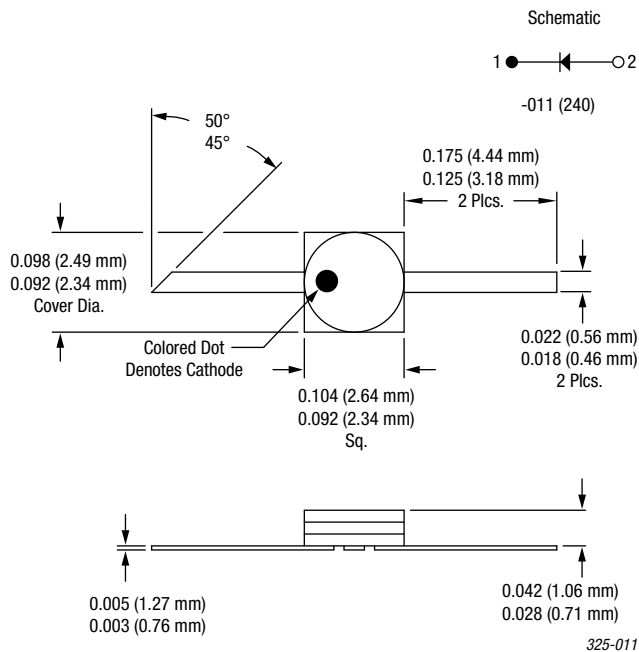
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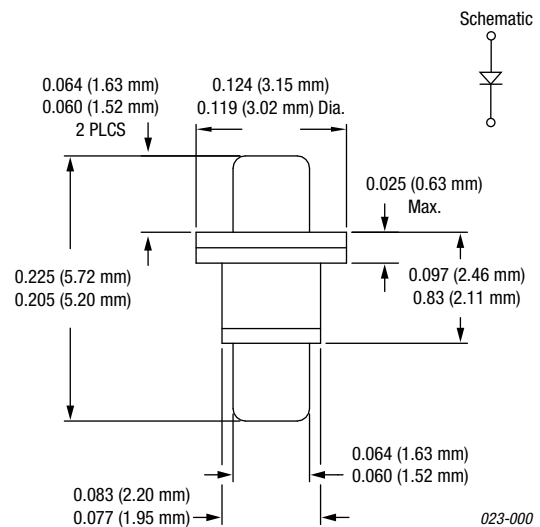
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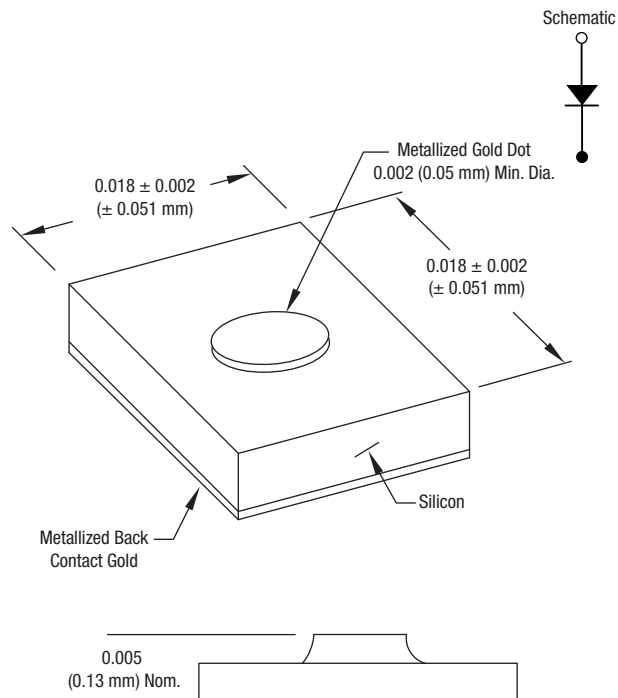
## -240



## -210



150-802



**DATA SHEET**

# SMV2019 to SMV2023: Silicon Hyperabrupt Junction Varactors, Packaged and Bondable Planar Chips

**Applications**

- Voltage controlled oscillators

**Features**

- High Q for low loss resonators
- Low leakage current
- High tuning ratio for wideband VCOs
- SPICE model parameters
- Small footprint chip design
- Lead (Pb)-free, RoHS-compliant, and Green™

**Description**

Skyworks silicon hyperabrupt junction varactor diodes are processed using established ion-implantation technology resulting in low  $R_S$  wide tuning ratio devices with high Q values. These diodes are available as chips or in ceramic packages. These planar chips have a small outline size (12 x 12 mils nominal) and are fully passivated, resulting in low leakage current and high reliability. These varactor chips are intended for assembly in hybrid integrated circuit resonators used in VCOs and analog tuned filters.

**NEW** Skyworks Green™ products are RoHS (Restriction of Hazardous Substances)-compliant, conform to the EIA/EICTA/JEITA Joint Industry Guide (JIG) Level A guidelines, are halogen free according to IEC-61249-2-21, and contain <1,000 ppm antimony trioxide in polymeric materials.


**Absolute Maximum Ratings**

Characteristic	Value
Reverse Voltage ( $V_R$ )	22 V
Forward Current ( $I_F$ )	100 mA
Power Dissipation at 25 °C ( $P_D$ )	250 mW
Operating Temperature ( $T_{OP}$ )	-55 °C to +150 °C
Storage Temperature ( $T_{ST}$ )	-65 °C to +200 °C

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum Ratings. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

**CAUTION:** Although these devices are designed to be robust, ESD (Electrostatic Discharge) can cause permanent damage. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.

Electrical Specifications at 25 °C

Part Number	C <sub>J</sub> @ 0 V (pF) <sup>(1)</sup>	C <sub>J</sub> @ 4 V (pF)		C <sub>J</sub> @ 20 V (pF)		Q @ 4 V 50 MHz <sup>(2)</sup>	1 GHz R <sub>S</sub> @ 4 V (Ω)	I <sub>R</sub> @17.6 V (nA) <sup>(3)</sup>	Contact Diam. (mils) <sup>(4)</sup>
	Typ.	Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Nom.
SMV2019-000	2.3	0.68	0.88	0.13	0.23	500	4.8	50	2
SMV2020-000	3.1	1.13	1.43	0.23	0.33	500	4.1	50	2.5
SMV2021-000	4.5	1.58	1.98	0.32	0.44	500	2.8	50	3
SMV2022-000	7.1	2.48	3.08	0.48	0.68	400	2.2	50	3.75
SMV2023-000	10.8	4.28	5.28	0.78	1.08	400	1.4	50	5

1. All capacitance values specified at 1 MHz.

2. 50 MHz Q calculated from 1 GHz R<sub>S</sub> and 1 MHz C<sub>J</sub>.

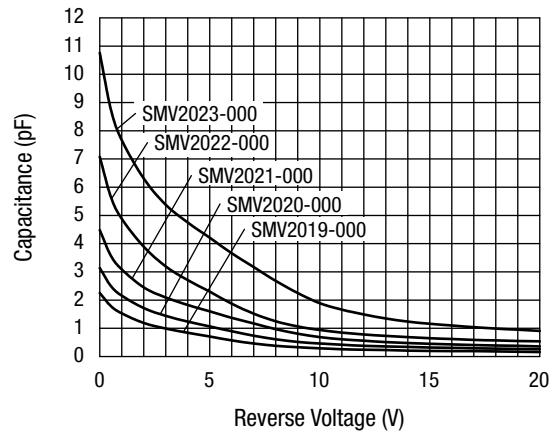
3. V<sub>B</sub> at 10 μA specified at 22 V Min.

4. Outline drawing 149-801.

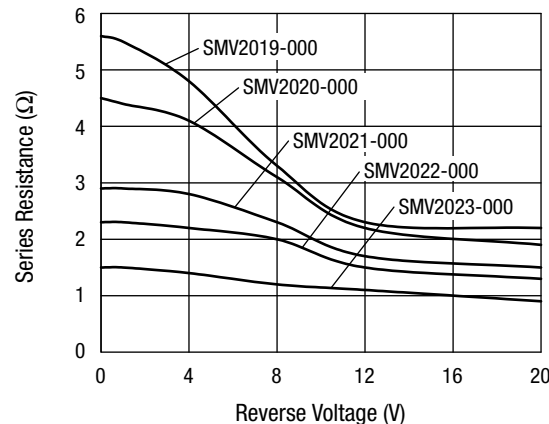
Hermetic Packaged Varactor Diodes

Stripline 240	Hermetic Pill 203	Stripline 219	Coaxial 210
SMV2019-240	SMV2019-203	SMV2019-219	SMV2019-210
SMV2020-240	SMV2020-203	SMV2020-219	SMV2020-210
SMV2021-240	SMV2021-203	SMV2021-219	SMV2021-210
SMV2022-240	SMV2022-203	SMV2022-219	SMV2022-210
SMV2023-240	SMV2023-203	SMV2023-219	SMV2023-210

Typical Performance Data



Capacitance vs. Reverse Voltage

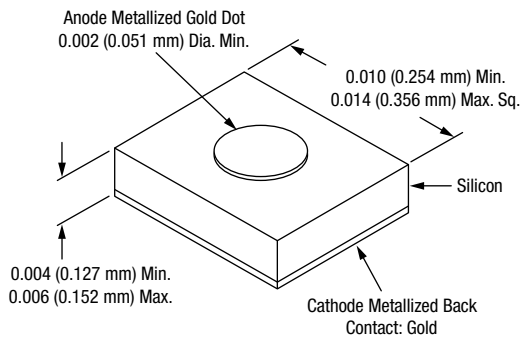


Series Resistance vs. Voltage @ 1 GHz

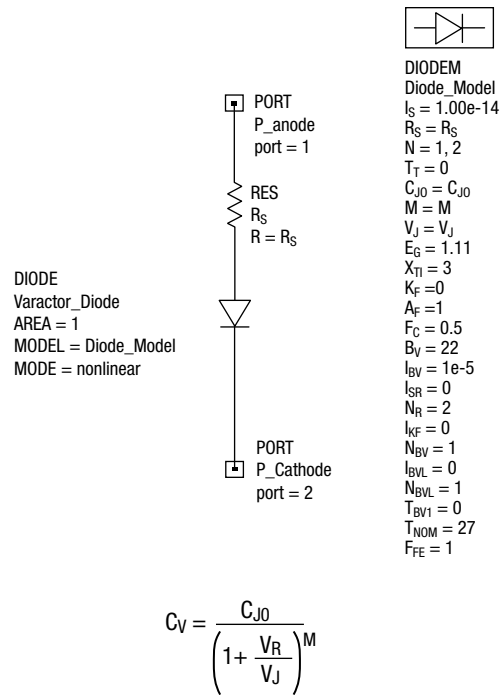
## Typical Capacitance Values

$V_R$ (V)	SMV2019 $C_J$ (pF)	SMV2020 $C_J$ (pF)	SMV2021 $C_J$ (pF)	SMV2022 $C_J$ (pF)	SMV2023 $C_J$ (pF)
0	2.25	3.14	4.48	7.08	10.76
0.5	1.79	2.5	3.57	5.66	8.76
1	1.53	2.16	3.09	4.88	7.67
2	1.19	1.72	2.45	3.89	6.31
3	0.99	1.44	2.09	3.19	5.38
4	0.84	1.24	1.83	2.71	4.75
5	0.71	1.07	1.6	2.3	4.21
6	0.57	0.9	1.37	1.87	3.66
7	0.46	0.74	1.17	1.52	3.17
8	0.38	0.61	0.97	1.25	2.68
9	0.33	0.52	0.81	1.07	2.25
10	0.29	0.46	0.69	0.94	1.89
11	0.26	0.42	0.61	0.85	1.66
12	0.24	0.38	0.56	0.78	1.49
13	0.23	0.36	0.51	0.73	1.35
14	0.21	0.34	0.48	0.69	1.24
15	0.2	0.32	0.45	0.65	1.16
16	0.19	0.31	0.43	0.62	1.1
17	0.19	0.29	0.41	0.59	1.04
18	0.18	0.28	0.39	0.57	0.99
19	0.17	0.27	0.38	0.55	0.95
20	0.16	0.26	0.36	0.54	0.91

## 149-801



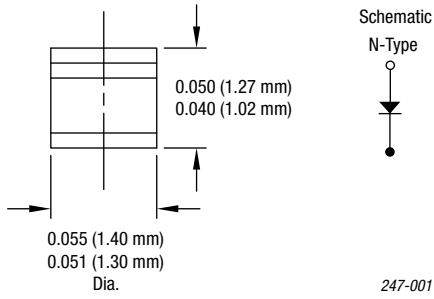
## SPICE Model



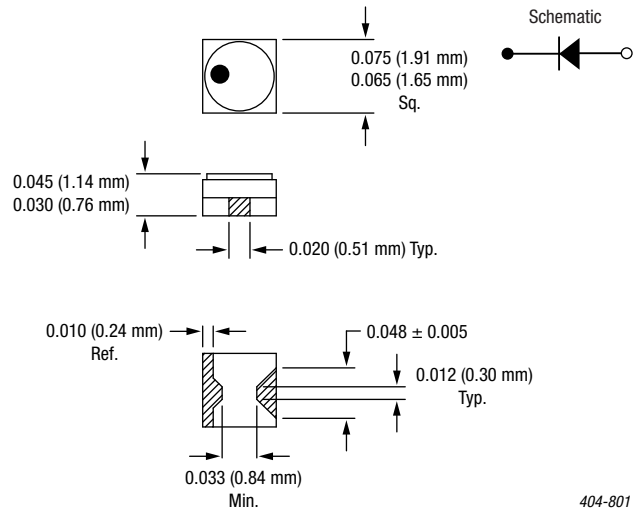
Part Number	$C_{J0}$ (pF)	$V_J$ (V)	M	$R_S$ ( $\Omega$ )
SMV2019	2.3	3.5	1.4	4.8
SMV2020	3.3	3.6	1.3	4.1
SMV2021	4.5	3.9	1.34	2.8
SMV2022	7.1	4	1.4	2.2
SMV2023	10.8	4.6	1.45	1.4

SPICE model parameters extracted from measured characteristics may not reflect exact physical or electronic properties. See application note APN1004.

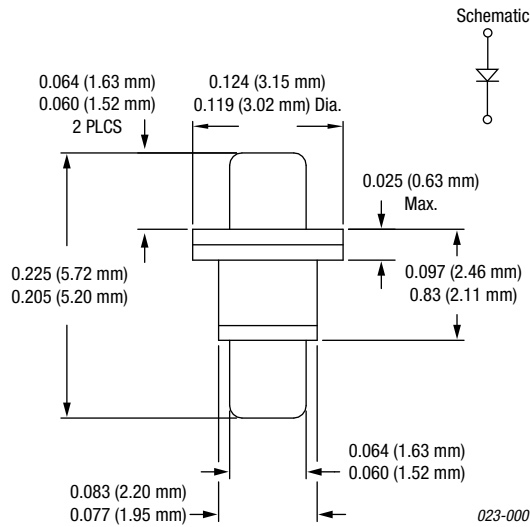
## -203



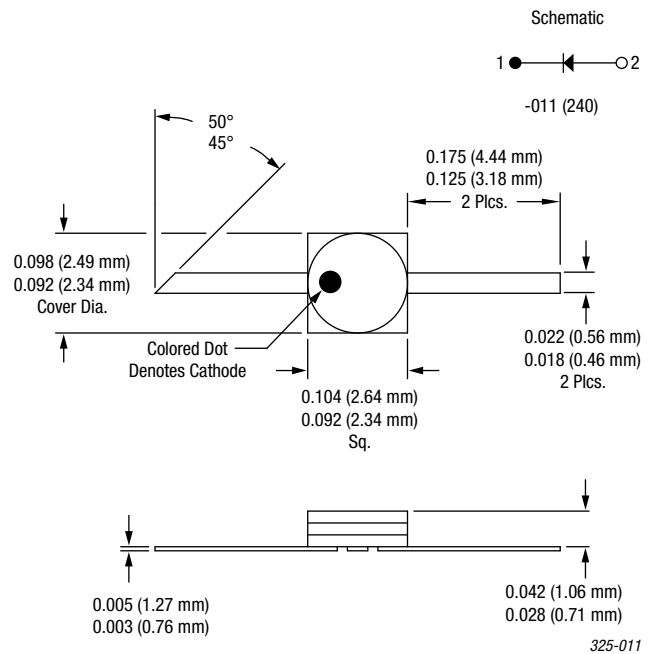
## -219



## -210



## -240



## DATA SHEET

# Silicon Tuning Varactors in Hermetic Surface Mount Package

## Applications

- VCOs
- Voltage tuned filters

## Features

- Silicon abrupt and hyperabrupt devices available
- Hermetic ceramic package, 1.83 x 1.43 x 1.0 mm
- Usable to 10 GHz
- Operating temperature range -55 °C to 150 °C
- ESD Class 1A, human body model
- Low inductance 0.48 nH
- Lead (Pb)-free, RoHS-compliant, and Green™, MSL-1 @ 260 °C per JEDEC J-STD-020

## Description

The family of proven silicon tuning varactor diodes is packaged in a hermetic, ceramic package. This package offers excellent, very low parasitic inductance and capacitance for wide bandwidth, high-frequency operation. It has low thermal impedance and meets fine and gross leak requirements for excellent reliability. Its small form factor, 1.83 x 1.43 x 1.0 mm, compares favorably to that of the smallest plastic packages.

This package meets Skyworks definition of Green: it is lead (Pb)-free, fully complies with current RoHS requirements and contains no halogens and no antimony (Sb).

SMV1405-108 is an abrupt junction device, with high Q and moderately large tuning bandwidth.

SMV1206-108 and SMV2019-108 are hyperabrupt junction varactors, which offer large tuning bandwidths by virtue of their high ratio capacitance voltage characteristic.

The diodes available in this package can operate over the temperature range of -55 °C to 150 °C.



**NEW**



Skyworks Green™ products are RoHS (Restriction of Hazardous Substances)-compliant, conform to the EIA/EICTA/JEITA Joint Industry Guide (JIG) Level A guidelines, are halogen free according to IEC-61249-2-21, and contain <1,000 ppm antimony trioxide in polymeric materials.

## Electrical Specifications

T = 25 °C, unless otherwise noted

Part Number	Min. Reverse Breakdown Voltage $I_R = 10 \mu A$ (V)	Max. Reverse Current @ $V_R = 24 V$ (nA)	Total Capacitance @ $V_R = 4 V$ $f = 1 MHz$ (pF)		Min. Capacitance Ratio $C_{T0}/C_{T30}$	Max. Series Resistance @ $V_R = 4 V$ $f = 500 MHz$ ( $\Omega$ )	Typ. Quality Factor @ $V_R = 4 V$ $f = 50 MHz$	ESD Rating, Human Body Model
			Min.	Max.				
SMV1405-108	30	20	1.25	1.56	3.8	0.8	3200	1A

Part Number	Min. Reverse Breakdown Voltage $I_R = 10 \mu A$ (V)	Max. Reverse Current @ $V_R = 16 V$ (nA)	Total Capacitance @ $V_R = 3 V$ $f = 1 MHz$ (pF)		Total Capacitance @ $V_R = 20 V$ $f = 1 MHz$ (pF)		Min. Capacitance Ratio $C_{T3}/C_{T20}$	Min. Quality Factor @ $V_R = 3 V$ $f = 50 MHz$	ESD Rating, Human Body Model
			Min.	Max.	Min.	Max.			
SMV1206-108	20	50	10.6	12.6	2.15	2.6	4.45	400	1A

Part Number	Min. Reverse Breakdown Voltage $I_R = 10 \mu A$ (V)	Max. Reverse Current @ $V_R = 17.6 V$ (nA)	Total Capacitance @ $V_R = 4 V$ $f = 1 MHz$ (pF)		Total Capacitance @ $V_R = 20 V$ $f = 1 MHz$ (pF)		Min. Quality Factor @ $V_R = 4 V$ $f = 50 MHz$	ESD Rating, Human Body Model
			Min.	Max.	Min.	Max.		
SMV2019-108	22	50	0.86	1.10	0.28	0.42	500	1A

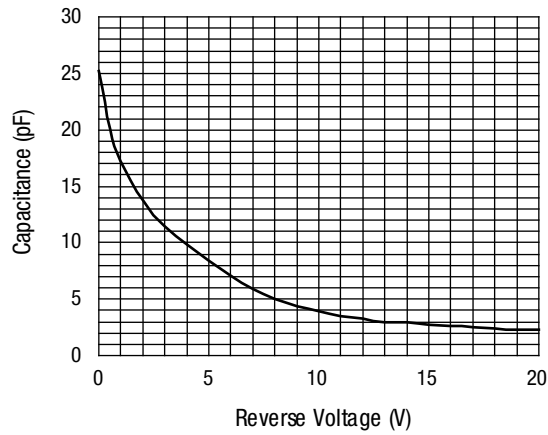
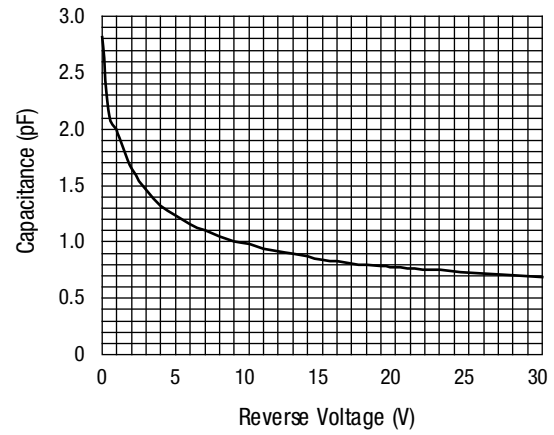
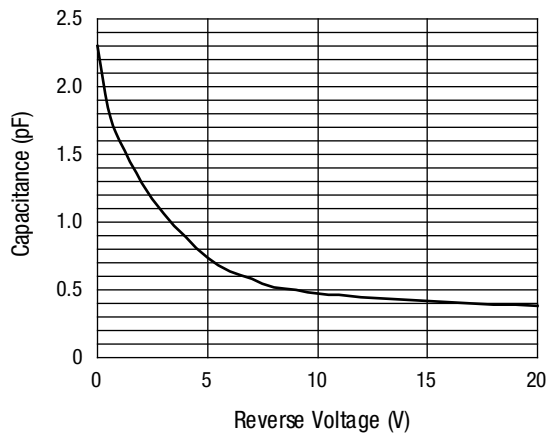
## Absolute Maximum Ratings

Characteristic	Value
Reverse voltage	Minimum Reverse Breakdown Voltage
Forward current	150 mA
Dissipated power at 25 °C	250 mW
Operating temperature	-55 °C to +150 °C
Storage temperature	-65 °C to +200 °C

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum Ratings. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

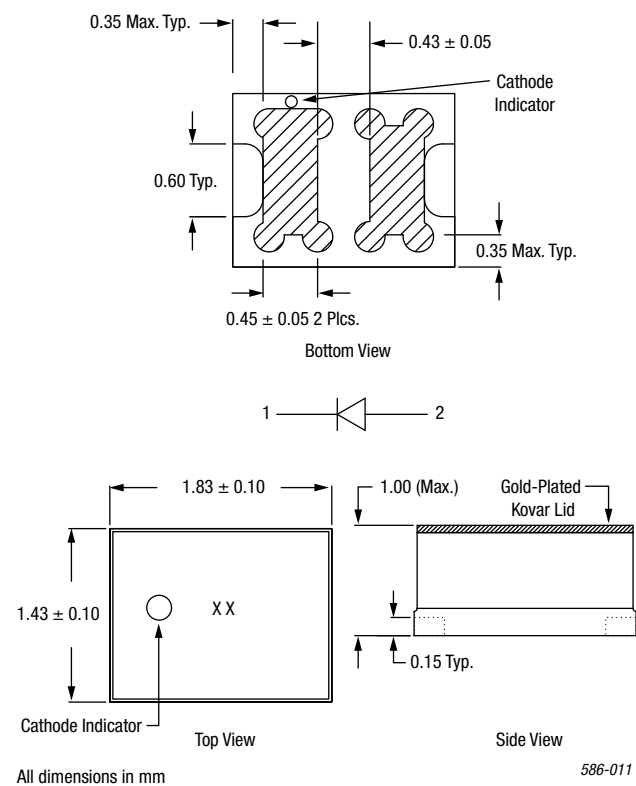
**CAUTION:** Although these devices are designed to be robust, ESD (Electrostatic Discharge) can cause permanent damage. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.



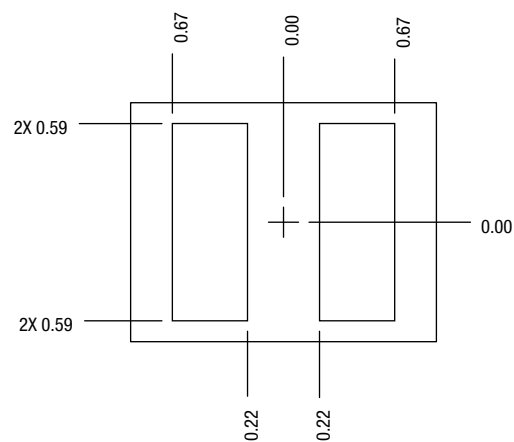
**Typical Performance Data (0, +3 V)****SMV1206****Capacitance vs. Voltage****SMV1405****Capacitance vs. Voltage****SMV2019****Capacitance vs. Voltage****Typical Capacitance Values**

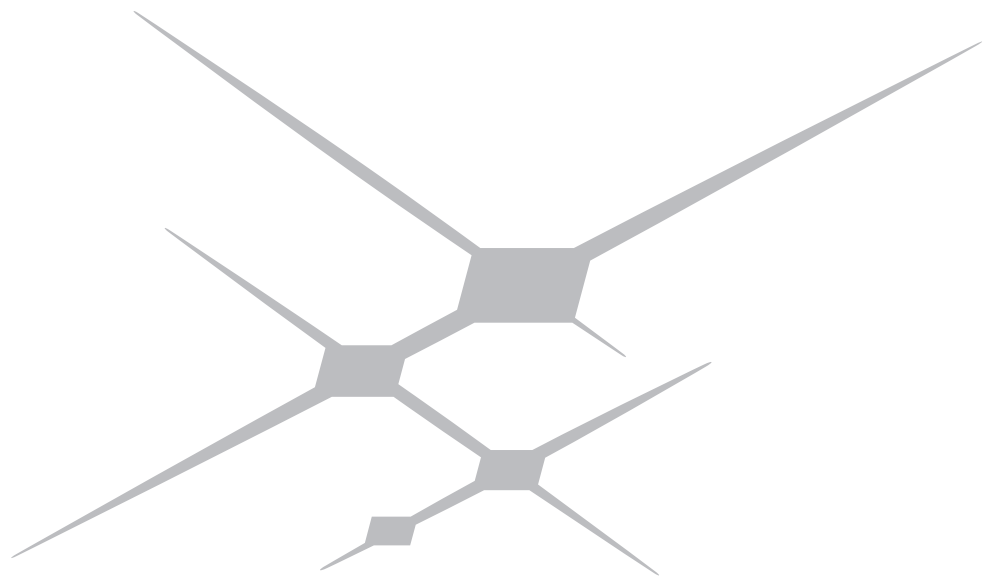
$V_R$ (V)	SMV1206 $C_T$ (pF)	SMV1405 $C_T$ (pF)	SMV2019 $C_T$ (pF)
0	25.2	2.81	2.3
0.5	20.1	2.12	1.85
1	17.2	2	1.6
2	13.7	1.65	1.29
3	11.5	1.46	1.06
4	9.8	1.32	0.89
5	8.4	1.23	0.74
6	7.1	1.16	0.64
7	5.9	1.1	0.58
8	5	1.05	0.52
9	4.4	1	0.5
10	3.9	0.98	0.47
11	3.5	0.94	0.46
12	3.3	0.92	0.45
13	3	0.89	0.44
14	2.9	0.87	0.43
15	2.7	0.84	0.42
16	2.6	0.83	0.41
17	2.5	0.81	0.4
18	2.4	0.8	0.39
19	2.3	0.79	0.39
20	2.3	0.77	0.38
30		0.69	

-108 Package Outline



-108 Land Pattern





## SCHOTTKY DIODES

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**PRELIMINARY DATA SHEET**

# SMS7621-096: 0201 Surface Mount Low Barrier Silicon Schottky Diode

## Applications

- Sensitive detector circuits
- Sampling circuits
- Mixer circuits

## Features

- Low profile, ultraminiature 0201 surface mount package
- Low barrier height
- Suitable for use beyond 26 GHz
- Low parasitic impedance ( $C_p < 0.05$  pF,  $L_s < 0.2$  nH)
- Lead (Pb)-free and RoHS-compliant

## Description

The SMS7621-096 is a silicon low barrier N-type Schottky diode in the ultraminiature 0201 footprint. This diode may be used in detector circuits, sampling circuits and in mixer circuits.

The low series resistance ( $R_s$ ) of this low-barrier diode enables good performance as a low-level mixer at frequencies as high as 26 GHz and higher.

SPICE model parameters are provided.

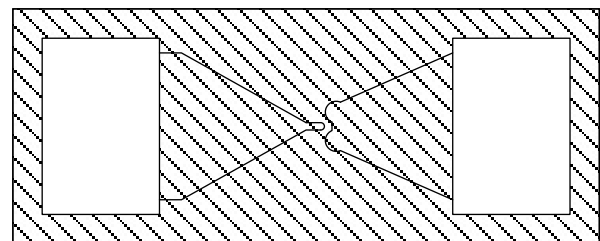
This package is lead (Pb)-free and fully complies with current RoHS requirements.

This device can operate over the temperature range of -65 °C to 150 °C.

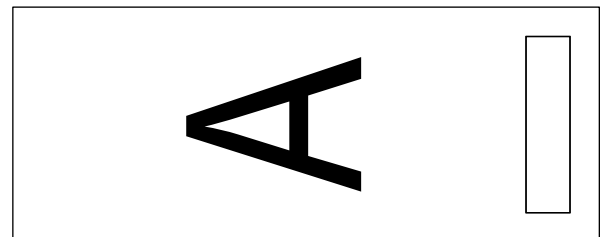
**NEW** Skyworks offers lead (Pb)-free, RoHS (Restriction of Hazardous Substances)-compliant packaging.



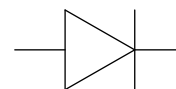
## Pin Out



Bottom View



Top View



**Preliminary Data Sheet:** Based on engineering results. Sampling quantities available. Pin out and package have been determined.

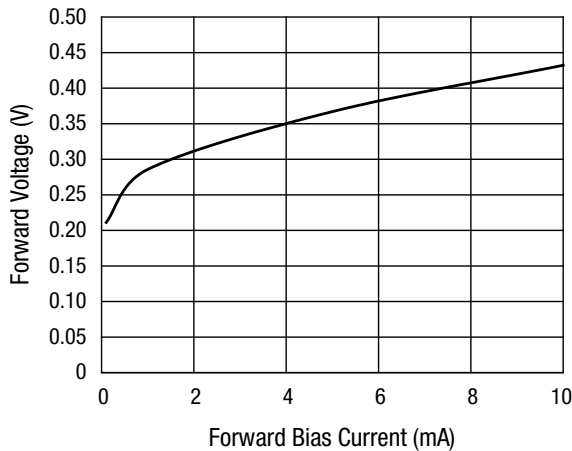
## Electrical Specifications

$T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted

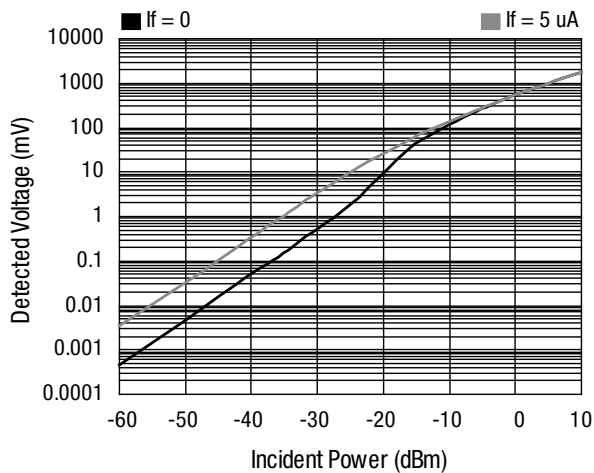
Minimum Breakdown Voltage @ $I_R = 10\text{ }\mu\text{A}$ (V)	Maximum Total Capacitance $C_T$ @ $V_R = 0\text{ V}$ , $f = 1\text{ MHz}$ (pF)	Forward Voltage @ $I_F = 1\text{ mA}$ (mV)	Maximum Series Resistance $R_S$ @ $I_F = 5\text{ mA}$ ( $\Omega$ )
2	0.18	260–320	12

## Typical Performance Data

$T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted



Forward Voltage vs. Forward Current



Detector Voltage at 2.45 GHz ( $T_A = 25\text{ }^{\circ}\text{C}$ )

## SPICE Model Parameters

Parameter	Unit	Value
$I_S$	A	9e-8
$R_S$	$\Omega$	8
N		1.1
TT	s	1e-11
$C_{JO}$	pF	0.1
M		0.35
$E_G$	eV	0.69
XTI		2
$F_C$		0.5
$B_V$	V	3
$I_{BV}$	A	1e-5
$V_J$	V	0.51

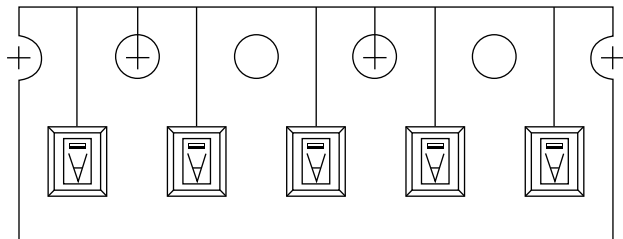
## Absolute Maximum Ratings

Characteristic	Value
Reverse voltage	2 V
Forward current	50 mA
Dissipated power at $25\text{ }^{\circ}\text{C}$	75 mW
Operating temperature	$-65\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$
Storage temperature	$-65\text{ }^{\circ}\text{C}$ to $+200\text{ }^{\circ}\text{C}$
Electrostatic Discharge (ESD) Human Body Model (HBM)	Class 0

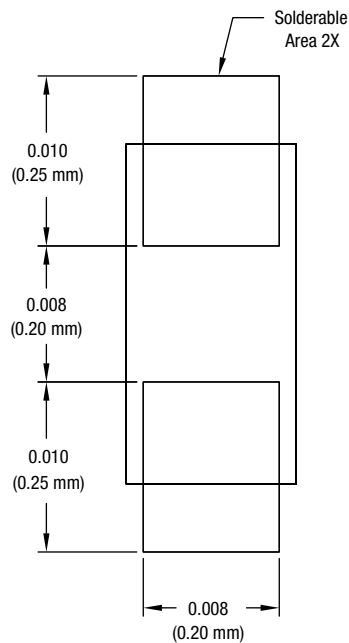
Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum specifications. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

**CAUTION:** Although this device is designed to be as robust as possible, ESD (Electrostatic Discharge) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.

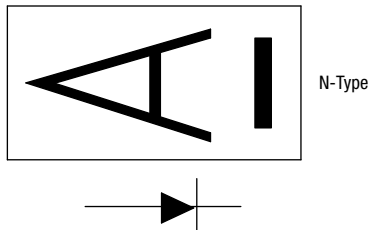
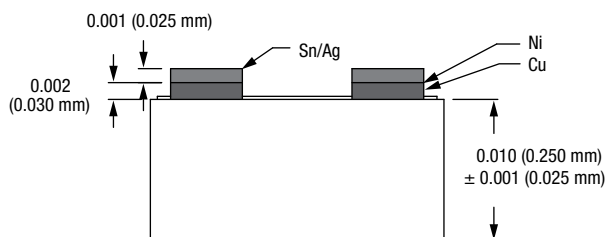
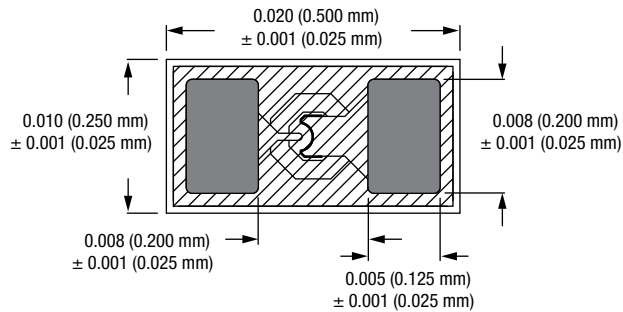
Tape and Reel Orientation



Land Pattern



-096



589-011

**PRELIMINARY DATA SHEET**

# SMS7630-093: 0201 Surface Mount Silicon Schottky Zero Bias Detector Diode

## Applications

- Sensitive detector circuits
- Sampling circuits

## Features

- Low profile, ultraminiature 0201 surface mount package
- Extremely low barrier
- Suitable for use beyond 26 GHz
- Low parasitic impedance ( $C_P < 0.05$  pF,  $L_S < 0.2$  nH)
- Lead (Pb)-free and RoHS-compliant

## Description

The SMS7630-093 is a silicon zero bias detector diode with very low barrier height, in the ultraminiature 0201 footprint. This P-type diode can be used for sensitive video detector circuits and sampling circuits.

The low barrier height results in good detector sensitivity without the need for external bias current. This diode's low junction capacitance make it an excellent detector at frequencies beyond 26 GHz.

SPICE parameters are provided.

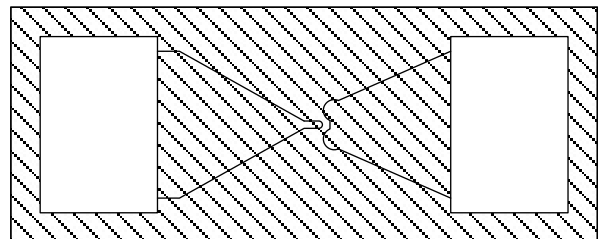
This package is lead (Pb)-free and fully complies with current RoHS requirements.

This device can operate over the temperature range of -65 °C to 150 °C.

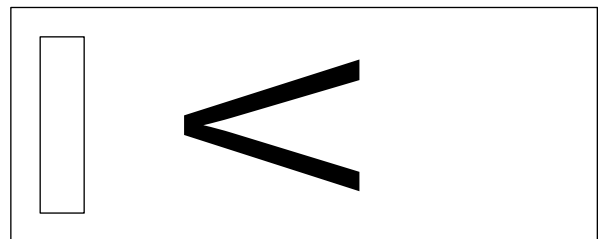
**NEW** Skyworks offers lead (Pb)-free, RoHS (Restriction of Hazardous Substances)-compliant packaging.



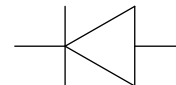
## Pin Out



Bottom View



Top View



**Preliminary Data Sheet:** Based on engineering results. Sampling quantities available. Pin out and package have been determined.

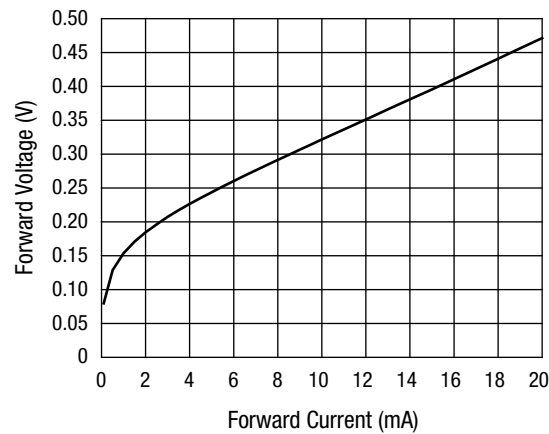
Electrical Specifications

T<sub>A</sub> = 25 °C, unless otherwise noted

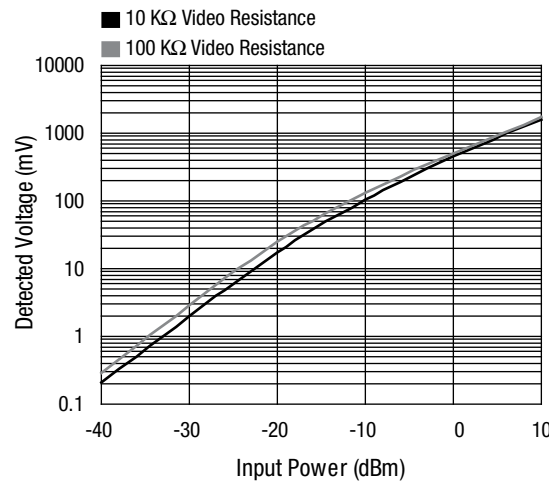
Minimum Breakdown Voltage @ I <sub>R</sub> = 10 μA (V)	Typical Total Capacitance @ V <sub>R</sub> = 0.15 V (pF)	Forward Voltage @ I <sub>F</sub> = 0.1 mA (mV)	Forward Voltage @ I <sub>F</sub> = 1.0 mA (mV)	Video Resistance @ V <sub>R</sub> = 0 V (Ω)
1	0.3	60–120	135–240	3000–7000

Typical Performance Data

T<sub>A</sub> = 25 °C, unless otherwise noted



Forward Voltage vs. Forward Current



Detector Voltage vs. Input Power (25 °C)

SPICE Model Parameters

Parameter	Unit	Value
I <sub>S</sub>	A	5e-6
R <sub>S</sub>	Ω	20
N		1.05
TT	s	1e-11
C <sub>JO</sub>	pF	0.14
M		0.4
E <sub>G</sub>	eV	0.69
XTI		2
F <sub>C</sub>		0.5
B <sub>V</sub>	V	2
I <sub>BV</sub>	A	1e-4
V <sub>J</sub>	V	0.34

Absolute Maximum Ratings

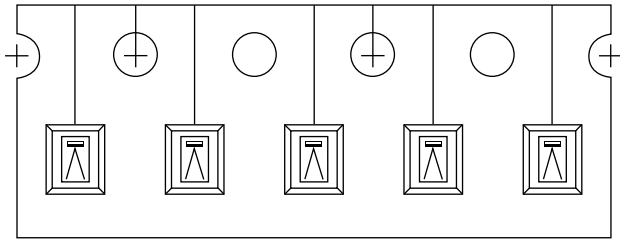
Characteristic	Value
Reverse voltage	Minimum Reverse Breakdown Voltage
Forward current	50 mA
Dissipated power at 25 °C	75 mW
Operating temperature	-65 °C to +150 °C
Storage temperature	-65 °C to +200 °C
Electrostatic Discharge (ESD) Human Body Model (HBM)	Class 0

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum Ratings. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

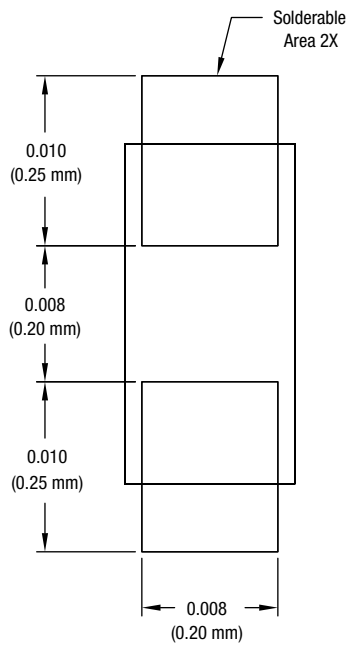
**CAUTION:** Although these devices are designed to be robust, ESD (Electrostatic Discharge) can cause permanent damage. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.



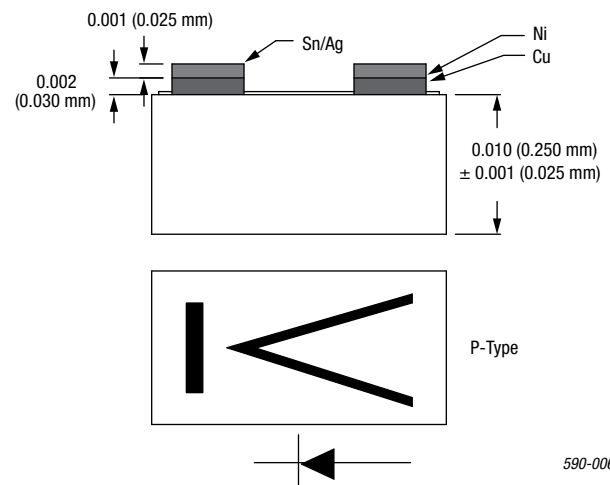
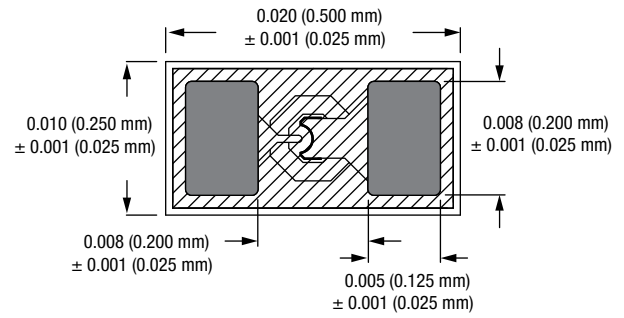
## Tape and Reel Orientation



## Land Pattern



## -093



590-006

## DATA SHEET

# Silicon Schottky Diode Chips

## Applications

- Detectors
- Mixers

## Features

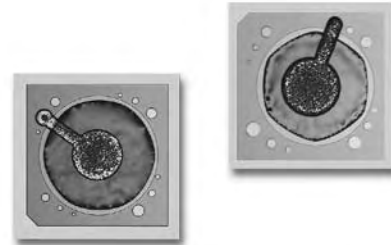
- Low capacitance for usage beyond 40 GHz
- ZBD and low-barrier designs
- P-type and n-type junctions
- Large bond pad chip design
- Lead (Pb)-free, RoHS-compliant, and Green™

## Description

Skyworks silicon Schottky diode chips are intended for use as detector and mixer devices in hybrid integrated circuits at frequencies from below 100 MHz to higher than 40 GHz. Skyworks “Universal Chip” design features a 4-mil-diameter bond pad that is offset from the semiconductor junction preventing damage to the active junction as a result of wire bonding.

As detectors, these Schottky diode chips have the same voltage sensitivity so long as the output video impedance is much higher than the video resistance of the diode. Figure 1 shows the expected detected voltage sensitivity as a function of RF source impedance in an untuned circuit. Note that sensitivity is substantially increased by transforming the source impedance from 50  $\Omega$  to higher values. Maximum sensitivity occurs when the source impedance equals the video resistance.

In a detector circuit operating at zero bias, depending on the video load impedance, a ZBD device with  $R_V$  less than 10 k $\Omega$  may be more sensitive than a low-barrier diode with  $R_V$  greater than 100 k $\Omega$ . Applying forward bias reduces the diode video resistance as shown in Figure 2. Lower video resistance also increases the video bandwidth but does not increase voltage sensitivity, as shown in Figure 3. Forward biased diodes have better temperature stability and also may be used in temperature compensated detector circuits.



P-type Schottky diodes generate lower 1/F noise and are preferred for Doppler mixers and biased detector applications. The bond pad for the P-type Schottky diode is the cathode. N-type Schottky diodes have lower parasitic resistance,  $R_S$ , and will perform with lower conversion loss in mixer circuits. The bond pad for the N-type Schottky diode is the anode.

**NEW** Skyworks Green™ products are RoHS (Restriction of Hazardous Substances)-compliant, conform to the EIA/EICTA/JEITA Joint Industry Guide (JIG) Level A guidelines, are halogen free according to IEC-61249-2-21, and contain <1,000 ppm antimony trioxide in polymeric materials.



Electrical Specifications at 25 °C

Part Number	Barrier	Junction Type	$C_J^{(1)}$ (pF)	$R_T^{(2)}$ ( $\Omega$ )	$V_F$ @ 1 mA (mV)	$V_B^{(3)}$ (V)	$R_V$ @ Zero Bias (k $\Omega$ )	Outline Drawing
			Max.	Max.	Min.-Max.	Min.	Typ.	
CDC7630-000	ZBD	P	0.25	30	135–240	1	5.5	571-006
CDC7631-000	ZBD	P	0.15	80	150–300	2	7.2	571-006
CDB7619-000	Low	P	0.1	40	275–375	2	735	571-006
CDB7620-000	Low	P	0.15	30	250–350	2	537	571-006
CDF7621-000	Low	N	0.1	20	270–350	2	680	571-011
CDF7623-000	Low	N	0.3	10	240–300	2	245	571-011

1.  $C_J$  for low barrier diodes specified at 0 V.  $C_J$  for ZBDs specified at 0.15 V reverse bias.  
2.  $R_T$  is the slope resistance at 10 mA.  $R_S$  Max. may be calculated from:  $R_S = R_T - 2.6 \times N$ .  
3.  $V_B$  for low barrier diodes is specified at 10  $\mu$ A.  $V_B$  for ZBDs is specified at 100  $\mu$ A.

Typical Performance Data

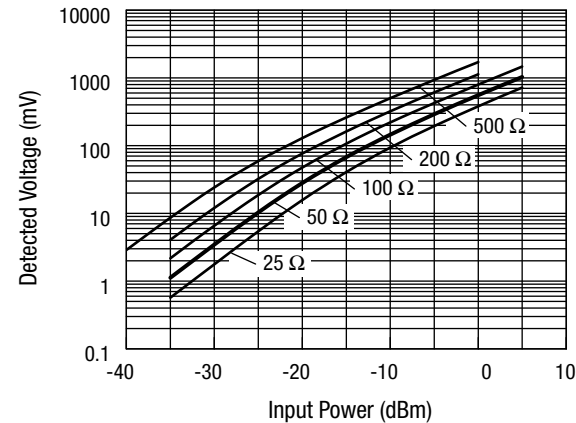
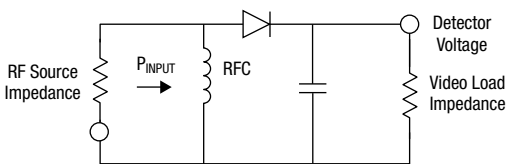
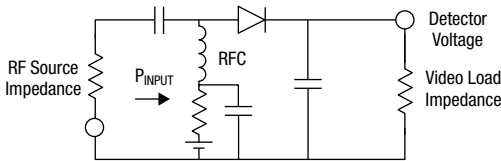


Figure 1. Detected Voltage vs. Input Power and RF Source Impedance



Zero Biased Detector



Biased Detector

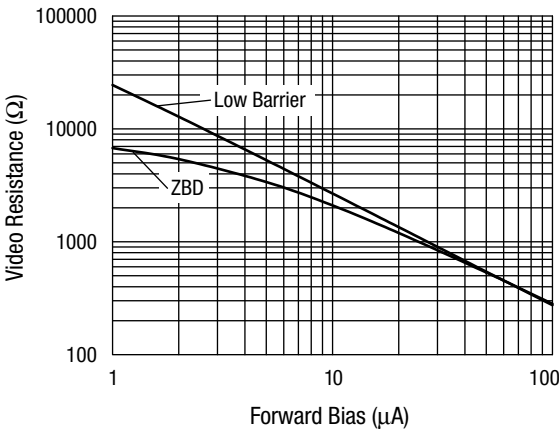


Figure 2. Video Resistance vs. Forward Bias Current

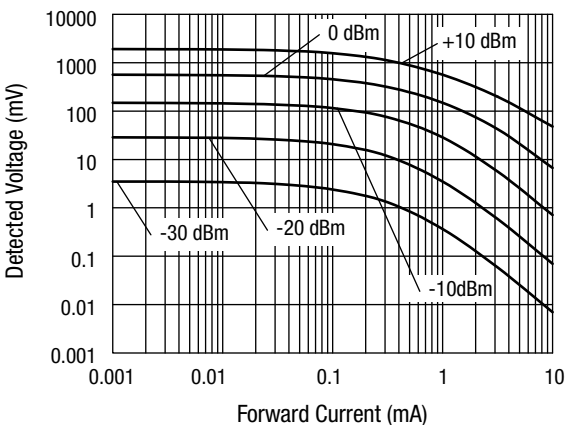


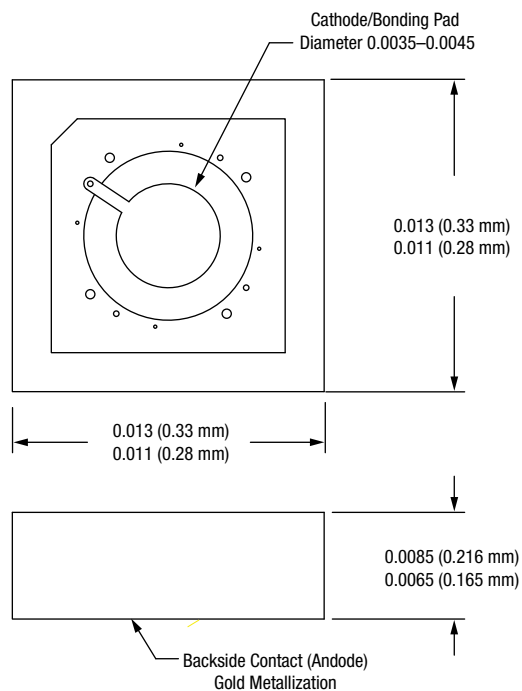
Figure 3. Detected Voltage vs. Forward Current

SPICE Model Parameters

Parameter	CDB7619	CDB7620	CDF7621	CDF7623	CDC7630	CDC7631	Units
I <sub>S</sub>	3.70E-08	5.40E-08	9.0E-08	1.1E-07	5.0E-06	3.8E-06	A
R <sub>S</sub>	3	14	6	6	20	51	Ω
N	1.05	1.12	1.1	1.04	1.05	1.05	
TT	1E-11	1E-11	1E-11	1E-11	1E-11	1E-11	s
C <sub>J0</sub>	0.08	0.15	0.1	0.22	0.14	0.08	pF
M	0.35	0.35	0.35	0.32	0.4	0.4	
E <sub>G</sub>	0.69	0.69	0.69	0.69	0.69	0.69	eV
XTI	2	2	2	2	2	2	
F <sub>C</sub>	0.5	0.5	0.5	0.5	0.5	0.5	
B <sub>V</sub>	2	4	3	2	2	2	V
I <sub>BV</sub>	1E-05	1E-05	1E-05	1E-05	1E-04	1E-04	A
V <sub>J</sub>	0.495	0.495	0.495	0.495	0.34	0.34	V

Outline Drawing

571-006 (Cathode Bond Pad), 571-011 (Anode Bond Pad)



Absolute Maximum Ratings

Characteristic	Value
Reverse voltage (V <sub>R</sub> )	Voltage rating
Forward current (I <sub>F</sub> )	50 mA
Power dissipation (P <sub>D</sub> )	75 mW
Storage temperature (T <sub>ST</sub> )	-65 °C to +150 °C
Operating temperature (T <sub>OP</sub> )	-65 °C to +150 °C
Electrostatic Discharge (ESD) Human Body Mode (HBM)	Class 0
Electrostatic Discharge (ESD) Charged Device Model (CDM)	Class C4

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum Ratings. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

**CAUTION:** Although these devices are designed to be robust, ESD (Electrostatic Discharge) can cause permanent damage. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.

## DATA SHEET

# Silicon Schottky Barrier Diodes: Packaged, Bondable Chips and Beam-Leads

## Applications

- Detectors

## Features

- Both P-type and N-type low barrier silicon available
- Low  $1/f$  noise
- Bonded junctions for reliability
- Planar passivated beam-lead and chip construction
- See also zero bias silicon schottky barrier detector diodes

## Description

Skyworks packaged, beam-lead and chip Schottky barrier detector diodes are designed for applications through 40 GHz in Ka band. They are made by the deposition of a suitable barrier metal on an epitaxial silicon substrate to form the junction. The process and choice of materials result in low series resistance along with a narrow spread of capacitance values for close impedance control. p-type silicon is used to obtain superior  $1/f$  noise characteristics. n-type silicon is also available.

Packaged diodes are suitable for use in waveguide, coaxial, and stripline applications.

Beam-lead and chip diodes can also be mounted in a variety of packages or on special customer substrates.

Unmounted beam-lead diodes are especially well suited for use in MIC applications. Mounted beam-lead diodes can be easily used in MIC, stripline or other such circuitry.

The "Universal Chips" are designed for a high degree of device reliability in both commercial and industrial uses. The offset bond pad assures that no mechanical damage will occur at the junction during the wire bonding. Additionally the 4 mil bond pad eliminates performance variation due to bonding and is ideal for automated assembly, and improves efficiency during manual operations as well.

The choice on n- and p-type silicon allows for the designer to optimize the silicon material for the intended application.

- Doppler mixers, high-sensitivity detectors will benefit from using the low noise characteristics of the p-type silicon.
- Low conversion loss mixers and biased detectors can be designed using standard n-type material.



## Applications

These diodes are categorized by TSS (Tangential Signal Sensitivity) for detector applications in four frequency ranges: S, X, Ku, and Ka band. However, they can also be used as modulators, high-speed switches and low-power limiters.

TSS is a parameter that describes a diode's detector sensitivity. It is defined as the amount of signal power, below a one-milliwatt reference level, to produce an output pulse whose amplitude is sufficient to raise the noise fluctuations by an amount equal to the average noise level. TSS is approximately 4 dB above the Minimum Detectable Signal.

The p-type Schottky diodes in this data sheet are optimized for low noise, in the  $1/f$  region. They require a small forward bias (to reduce video resistance) if efficient operation is required. Bias not only increases sensitivity but also reduces parameter variation due to temperature change. Video impedance is a direct function of bias and follows the  $26/I$  (mA) relationship. This is important to pulse fidelity, since the video impedance in conjunction with the detector output capacitance affects the effective amplifier bandwidth.

Bias does, however, increase typical noise, particularly in the  $1/f$  region. Therefore, it should be kept at as low a level as possible (typically 5–50 microamps). Typical voltage output versus power input as a function of load resistance and bias is shown in Figures 1a and 1b.

## Assembly and Handling Procedure

### Die Attach Methods

Universal chips are compatible with both eutectic and conductive epoxy die attach methods.

Eutectic composition performs of Au/Sn or Au/Ge are useful when soldering devices in circuit. Gold/silicon eutectic die attach can be accomplished by scrubbing the chip directly to the gold plated bonding area.

Epoxy die attach with silver or gold filled conductive epoxies can also be used where thermal heat sinking is not a requirement.

### Wire Bonding

Two methods can be used to connect wire, ribbon, and wire mesh to the chips:

- Thermocompression
- Ballbonding

Skyworks recommends use of pure gold wire (0.7–1.25 mil diameter).

## Beam-Lead P-Type Detector Schottky Diodes

Frequency Band	Part Number	Electrical Characteristics						Test Conditions	Outline Drawing
		TSS – dBm <sup>1,2</sup>	R <sub>V</sub> (Ω)		C <sub>J</sub> @ 0V (pF)	V <sub>F</sub> @ 1 mA (mv)	V <sub>B</sub> @ 10 mA (V)	Frequency (GHz)	
		Typ.	Min.	Max.	Max.				
X	DDB2503-000	50	500	700	0.15	200–350	2	10	491–006
Ku	DDB2504-000	48	500	700	0.10	200–350	2	16	491–006
K	DDB2265-000	50 <sup>3</sup>	800 <sup>3</sup>	1200 <sup>3</sup>	0.10	300–450	3	24.15	491–006

1. Bias = 50 μA.

2. Video bandwidth = 10 MHz.

3. Bias = 30 μA.

## Epoxy and Hermetic Packaged Beam-Lead P-Type Detector Schottky Diodes

Epoxy Stripline 250	Epoxy Stripline 230	Hermetic Stripline 220
DDB2503-250	DDB2503-230	DDB2503-220
DDB2504-250	DDB2504-230	DDB2504-220
DDB2265-250	DDB2265-230	DDB2265-220

## P-Type Detector Schottky Diode Universal Chips

Frequency Band	Part Number	Electrical Characteristics					Outline Drawing
		TSS – dBm <sup>1,2,4</sup>	C <sub>J</sub> @ 0V (pF)	V <sub>F</sub> @ 1 mA (mv)	R <sub>T</sub> @ 10 mA (Ω)	V <sub>B</sub> @ 10 mA (V)	
		Min.	Max.		Max.	Min.	
Ku	CDB7620-000	40	0.15	250–350	30	2	571–006
K	CDB7619-000	50 <sup>3</sup>	0.10	300–450	40	3	571–006

1. Bias = 50 μA.

2. Video bandwidth = 10 MHz.

3. Bias = 30 μA.

4. R<sub>V</sub> = 2800 Ω.

**Hermetic Packaged P-Type Detector Schottky Diode Chips**

Hermetic Pill 207	Hermetic Pill 203	Hermetic 109
CDB7620-207	CDB7620-203	SMS7620-109
CDB7619-207	CDB7619-203	SMS7619-109

**N-Type Detector Schottky Diode Chips**

Frequency Band	Part Number	Electrical Characteristics					
		Barrier	$V_F$ @ 1 mA (mV)	Max. $C_J$ @ 0V (pF)	Max. $R_T$ @ 10 mA ( $\Omega$ )	Min. $V_B$ @ 10 $\mu$ A (V)	Outline Drawing Number
X	CDF7623-000	Low	240–300	0.30	10	2	571-011
K	CDF7621-000	Low	270–350	0.10	20	2	571-011
Ku	CME7660-000	Med	350–450	0.15	10	3	571-011
K	CDE7618-000	Med	375–500	0.10	20	3	571-011
Ku	CDP7624-000	Med/High	450–575	0.15	15	3	571-011

**Hermetic Packaged Beam-Lead N-Type Detector Schottky Diode Chips**

Hermetic Ceramic Pill 207	Hermetic Ceramic Pill 203	Hermetic Surface Mount 108
CDF7623-207	CDF7623-203	SMS7623-108
CDF7621-207	CDF7621-203	SMS7621-108
CME7660-207	CME7660-203	SMS7660-108
CDE7618-207	CDE7618-203	SMS7618-108
CDP7624-207	CDP7624-203	SMS7624-108

**SPICE Model Parameters**

Parameter	Unit	Part Number			
		CDF7620-000	CDF7621-000	CDC7623-000	CDB7619-000
$I_S$	A	4e-08	9e-08	1.1e-7	3e-08
$R_S$	$\Omega$	4	6	5	30
n	–	1.2	1.1	1.1	1.04
$T_D$	s	1e-11	1e-11	1e-11	1e-11
$C_{J0}$	pF	0.15	0.11	0.2	0.11
m	–	0.35	0.3	0.3	0.32
$E_G$	eV	0.69	0.69	0.69	0.69
$V_J$	V	0.495	0.51	0.51	0.54
$X_{T1}$	–	2	2	2	2
FC	–	0.5	0.5	0.5	0.5
$B_V$	V	10	2.5	2.5	3
$I_{BV}$	A	1e-05	1e-05	1e-05	1e-05

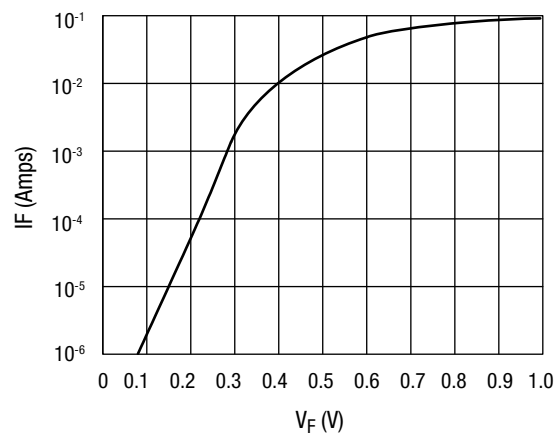
**Shipping Information****Individual Chips**

Standard packaging procedures at Skyworks are for “waffle pack” delivery. Devices can also be packaged on “Gel Pack” carriers.

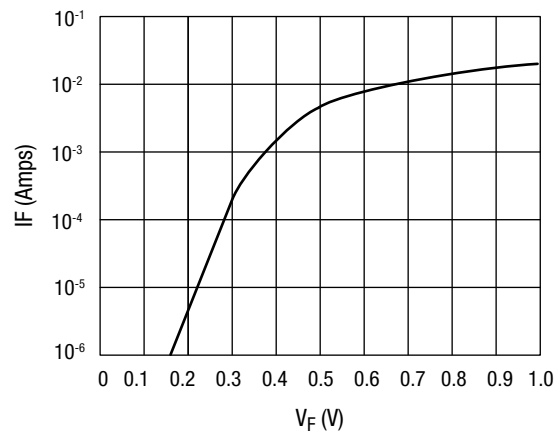
**Wafer Shipment for Whole Wafer**

Packaging options include delivery for devices on film frame where wafer is sawn on wafer gel pack for uncut, unsawn wafer.

Typical I-V Characteristics



CDF7621-000



CDB7619-000

Typical Performance Data

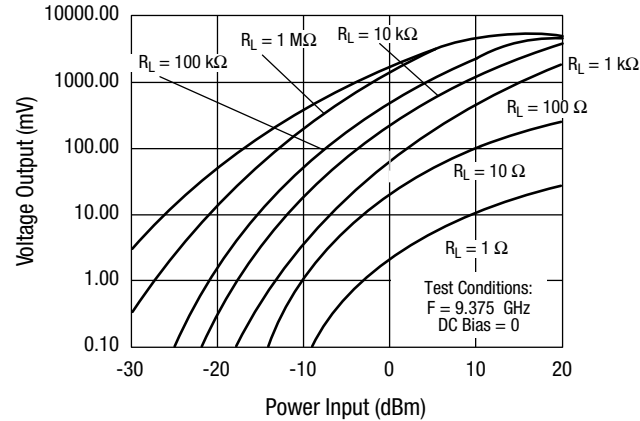


Figure 1a. Voltage Output vs. Power Input  
As a Function of Load Resistance

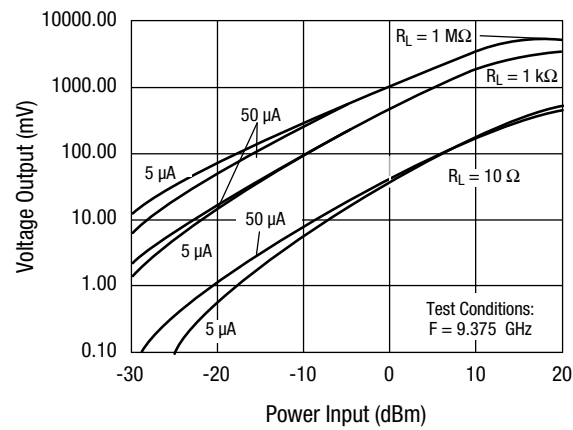
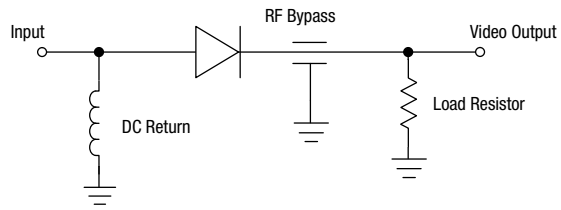


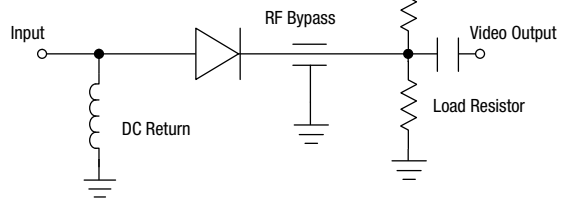
Figure 1b. Voltage Output vs. Power Input  
As a Function of Load Resistance and Bias



a) Unbiased

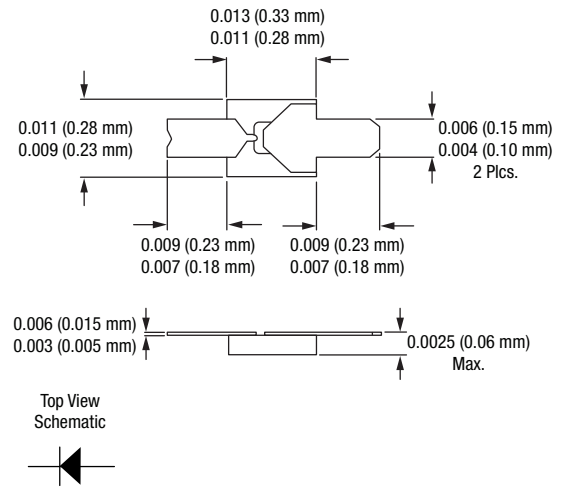


a) Biased

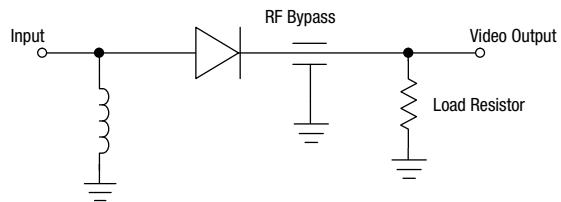


Multi-Octave-High Sensitivity

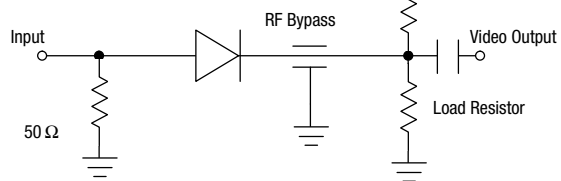
491-006



a) Unbiased



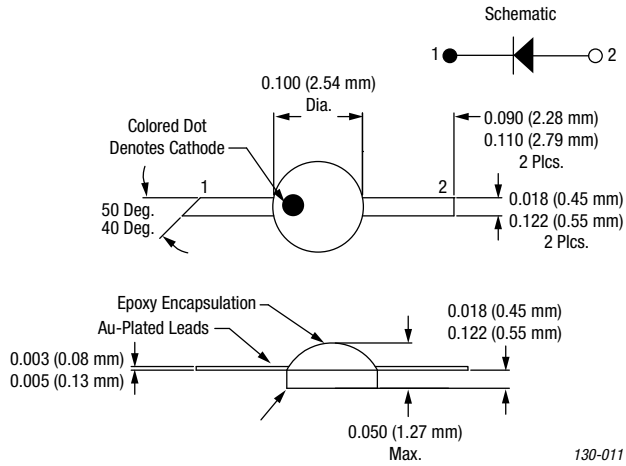
a) Biased



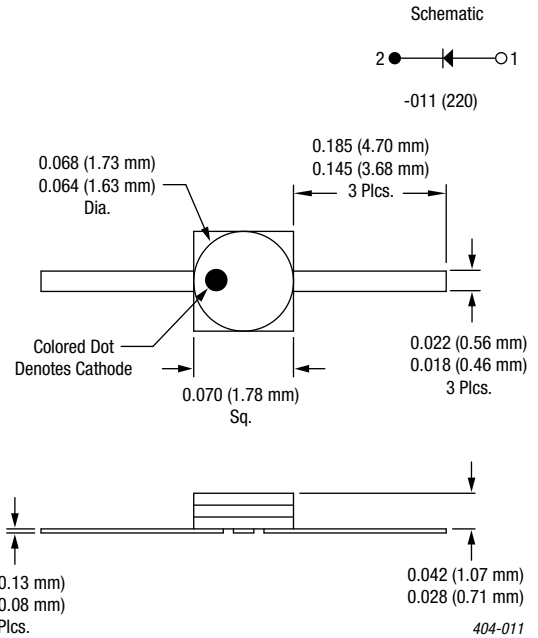
Broadband-Low Sensitivity

Figure 2. Typical Video Detector Circuits

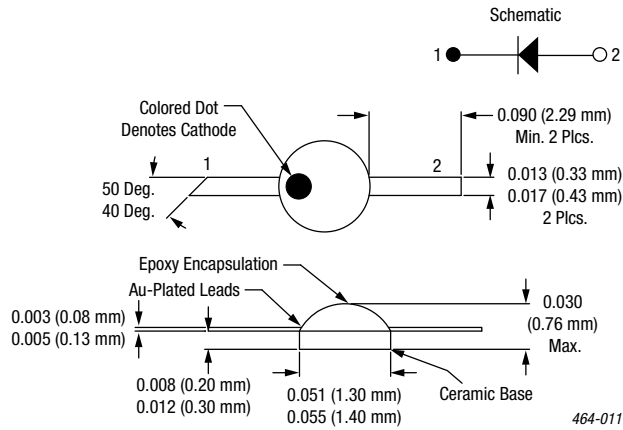
**-250**



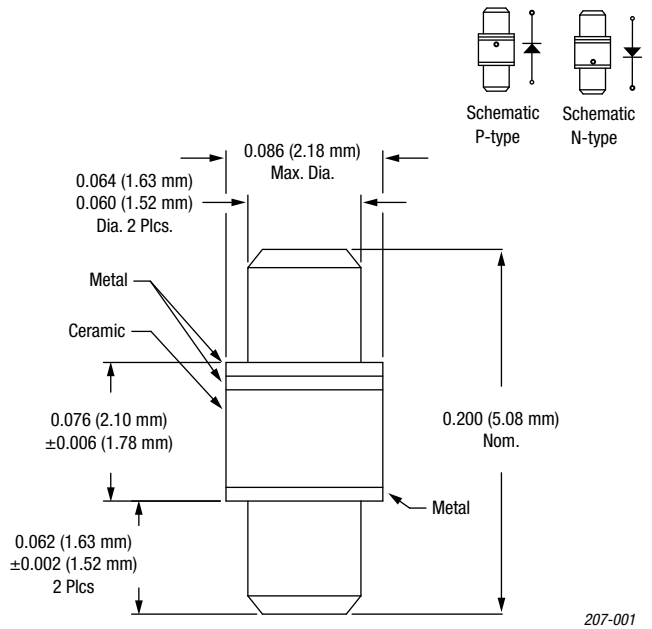
**-220**



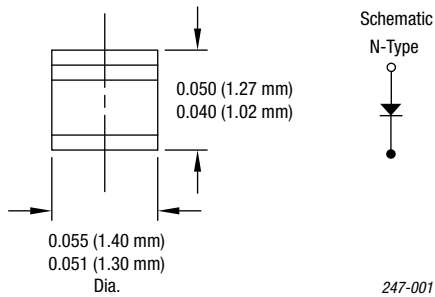
**-230**

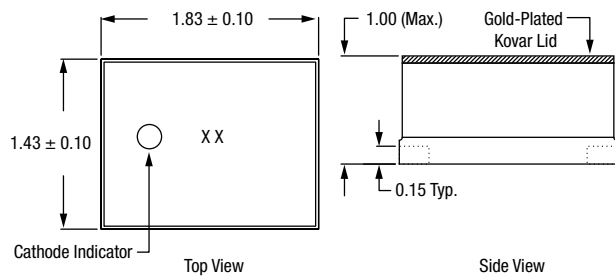
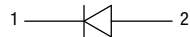
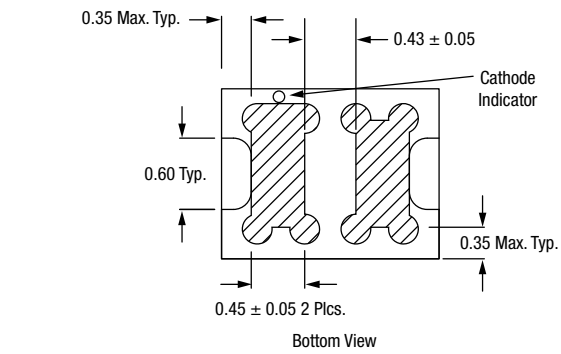


**-207**



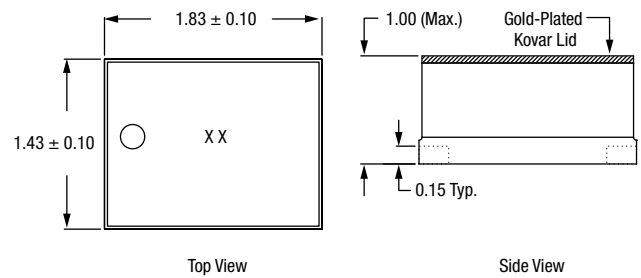
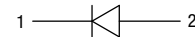
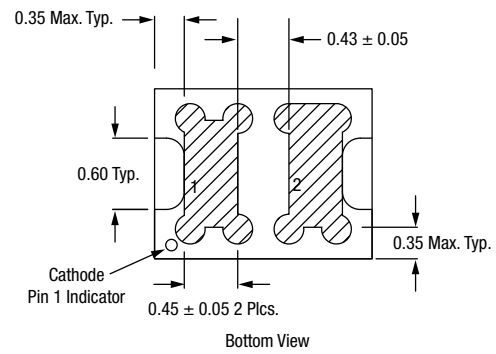
**-203**



**-108**

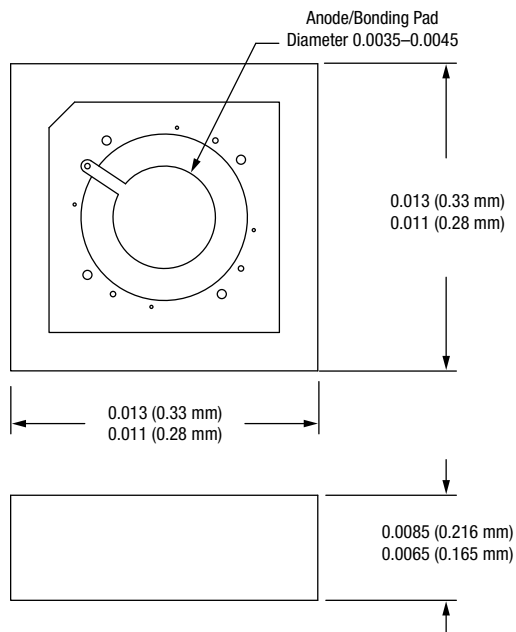
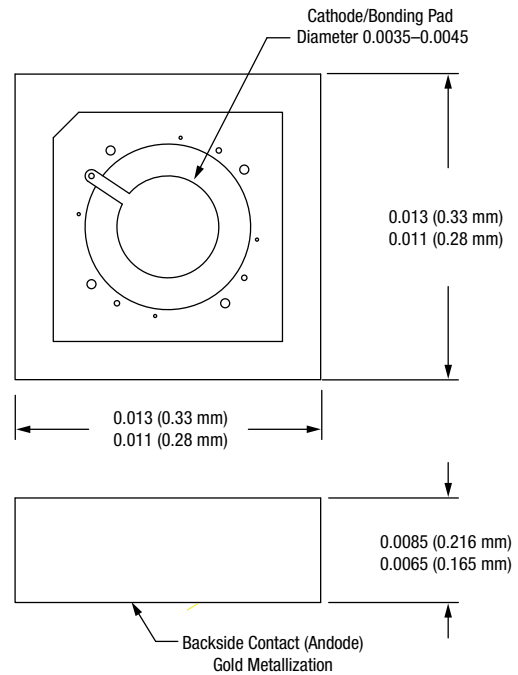
All dimensions in mm

586-011

**-109**

All dimensions in mm

585-006

**571-011****571-006**

## DATA SHEET

# Zero Bias Silicon Schottky Barrier Detector Diodes

## Features

- High sensitivity
- Low video impedance

## Description

Skyworks series of packaged, beam-lead and chip zero bias Schottky barrier detector diodes are designed for applications through K band. The choice of barrier metal and process techniques results in a diode with a wide selection of video impedance ranges.

The packaged diodes are suitable for use in waveguide, coaxial and stripline applications. The beam-lead and chip diodes can also be mounted in a variety of packages.

Unmounted beam-lead diodes are especially well suited for use in MIC applications. Mounted beam-lead diodes can be easily used in MIC, stripline and other such circuitry.

A complete line of chips is shown for those MIC applications where the chip and wire approach is more desirable.

## Applications

The zero bias Schottky detector diodes are designed for detector applications through 26 GHz and are useful to 40 GHz. They require no bias and operate efficiently even at tangential signal power levels. Since they require no bias, noise is at a minimum. Their low video impedance means a short R-C time constant and hence wide video bandwidth and excellent pulse fidelity. As power monitors, these diodes may also be used to drive metering circuits directly even at low power input levels. These diodes are categorized by TSS (Tangential Signal Sensitivity), voltage output and video impedance for detector applications.

TSS is the parameter that best describes a diode's use as a video detector. It is defined as the amount of signal power, below a one-milliwatt reference level, required to produce an output pulse whose amplitude is sufficient to raise the noise fluctuations by an amount equal to the average noise level. TSS is approximately 4 dB above the Minimum Detectable Signal.



Voltage output is another useful parameter, since it can be used in the design of threshold detectors and power monitor circuits. Since voltage output is a function of the diode's video impedance, a different minimum value is specified for each video impedance range.

Figure 1 is a plot of the forward DC characteristics. In Figure 2 voltage output is plotted as a function of power input for diodes of various video impedances. Tangential Signal Sensitivity as a function of video impedance is shown in Figure 3. Figure 4 shows two typical detector circuits. The multi-octave-high-sensitivity circuit would be used in ECM and similar applications. An RF matching structure that will present the maximum power at the diode junction must be incorporated to insure maximum sensitivity. The broadband-low-sensitivity circuit would be used where low input VSWR is required. In this circuit the low VSWR is accomplished by the use of the 50  $\Omega$  terminating resistor. Sensitivity, however, is degraded by typically 10 dB from the multi-octave-high-sensitivity circuit. The most common use for this circuit is in the broadband, flat detector used primarily in the laboratory.

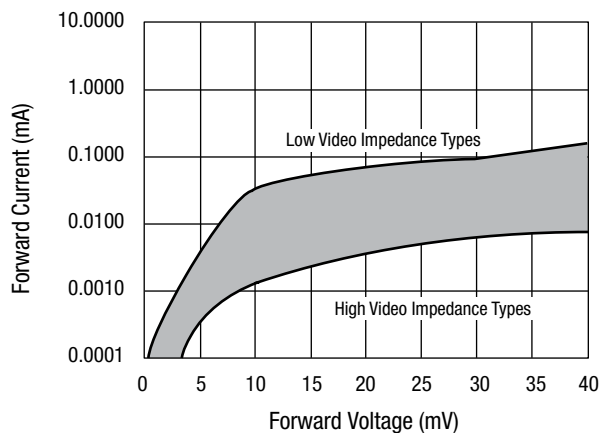
## Electrical Specifications at 25 °C

Part Number	Min. E0 (mV)	$Z_V$ ( $\Omega$ )	Min. $T_{SS}$ (dBm)	Outline Drawing
DDC2353-000	8	2000–5000	-52	491-006
DDC2354-000	15	5000–15000	-56	491-006
CDC7630-000	8	2000–5000	-52	571-006
CDC7631-000	15	5000–15000	-56	571-006

## Epoxy and Hermetic Packages

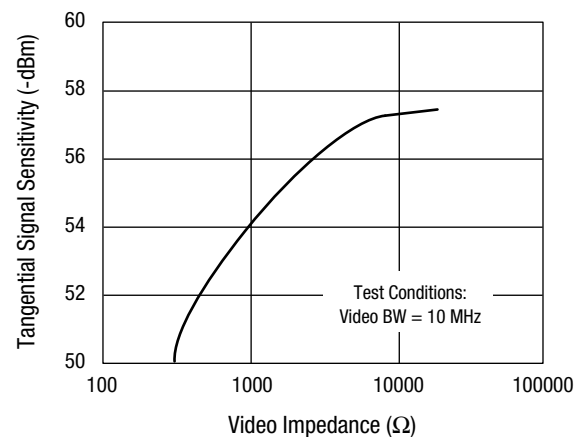
Epoxy Stripline 250	Hermetic Pill 207	Hermetic Pill 203	Hermetic 109	Hermetic 220
DDC2353-250	CDC7630-207	CDC7630-203	SMS7630-109	DDC2353-220
DDC2354-250	CDC7631-207	CDC7631-203	SMS7619-109	DDC2354-220

## Typical Performance Data



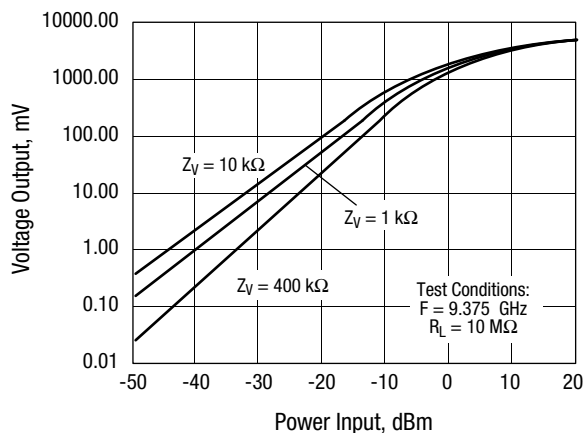
## Zero Bias Schottky Detector Diodes

Figure 1. Typical Forward DC Characteristics



## Typical Zero Bias X-Band Detector Diodes

Figure 3. Tangential Signal Sensitivity vs. Video Impedance



## Typical Zero Bias X-Band Detector Diodes

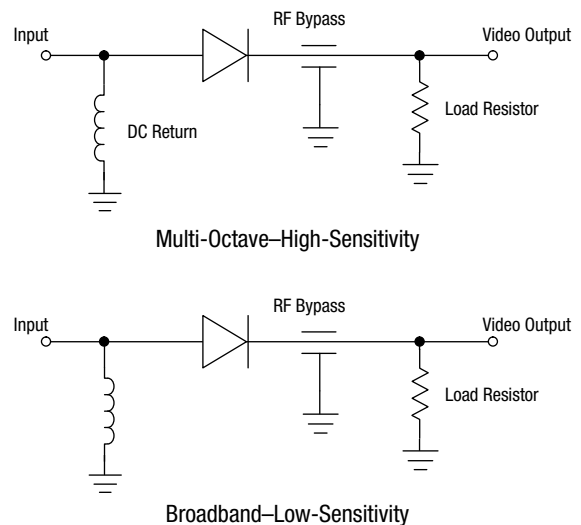
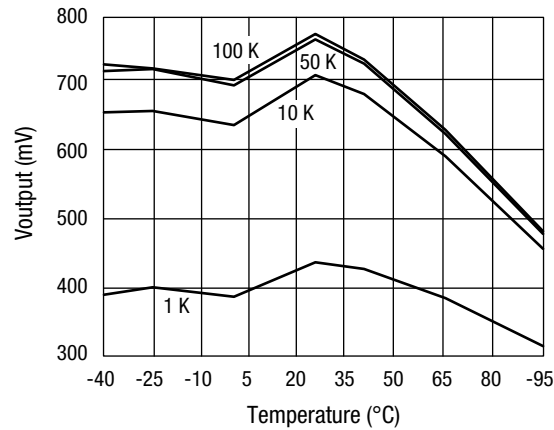
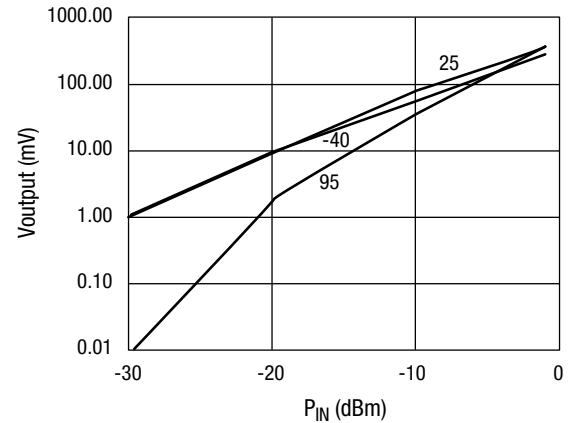
Figure 2. Voltage Output vs. Power Input  
As a Function of Video Impedance

Figure 4. Typical Video Detector Circuits

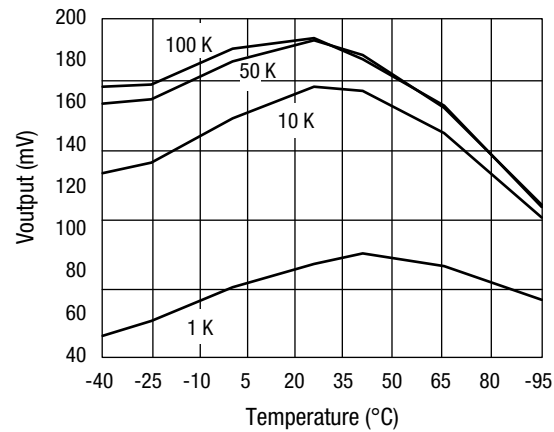
### Typical I-V Characteristics



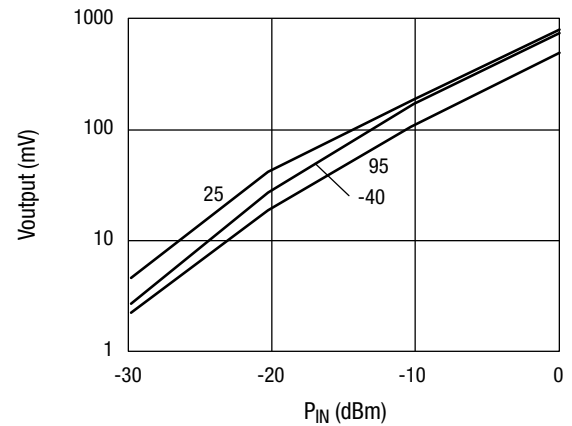
**Voltage Output vs. Resistance  
at 0 dBm vs. Temperature °C**



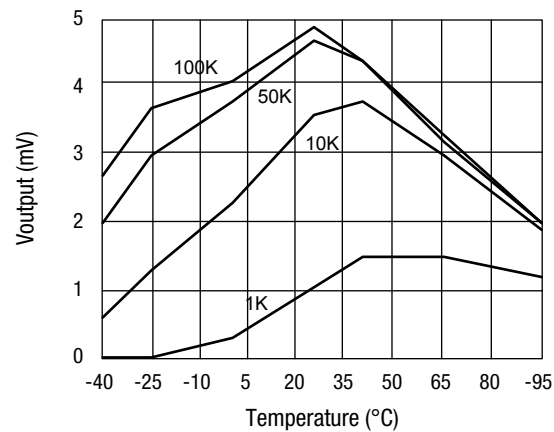
**Transfer at -40, 25, 90 °C  
 $R_L = 1\text{ k}\Omega$**



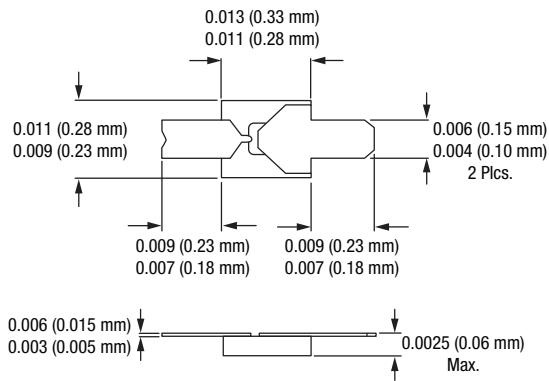
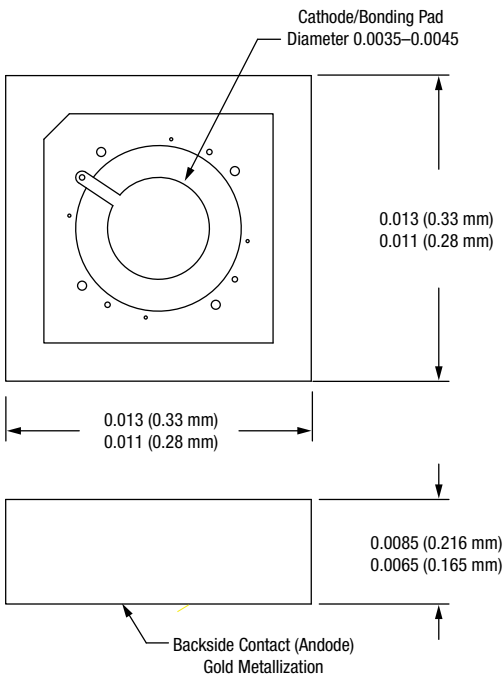
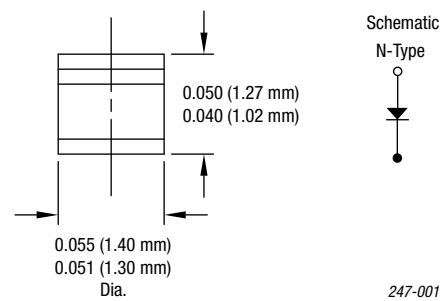
**Voltage Output vs. Resistance  
at -10 dBm vs. Temperature °C**



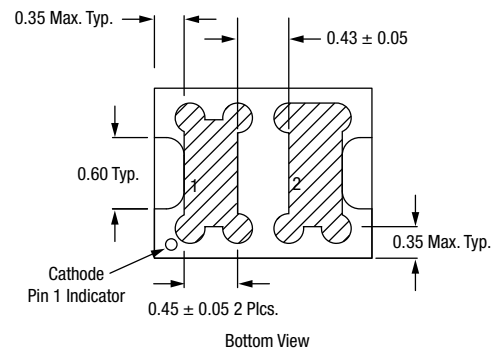
**Transfer at -40, 25, 90 °C  
 $R_L = 100\text{ k}\Omega$**



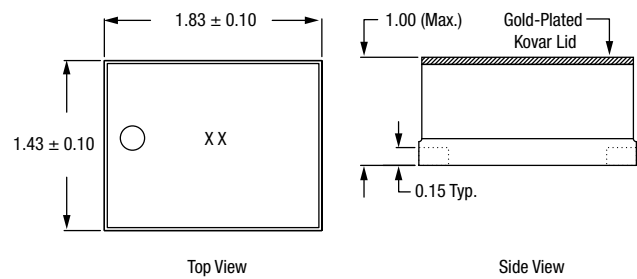
**Voltage Output vs. Resistance  
at -30 dBm vs. Temperature °C**

**491-006**Top View  
Schematic**571-006****-203**

247-001

**-109**

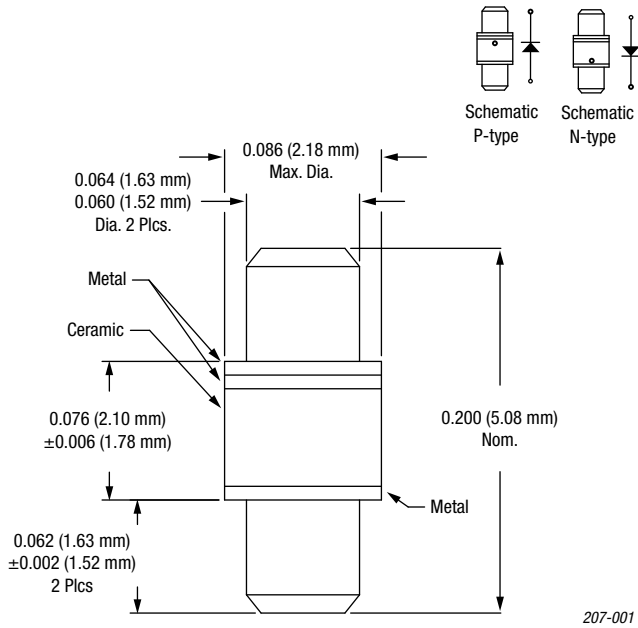
1 ——— 2



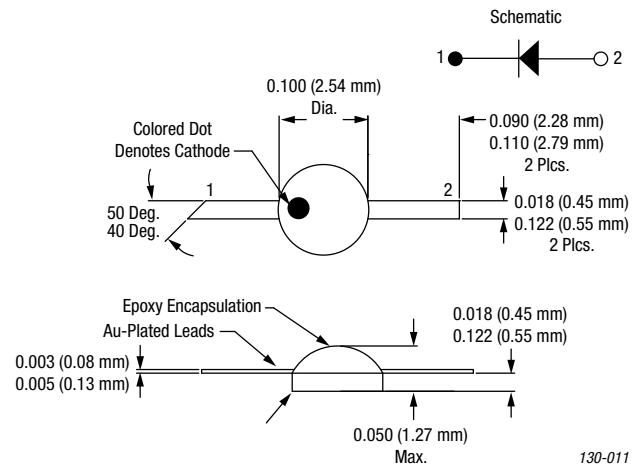
All dimensions in mm

585-006

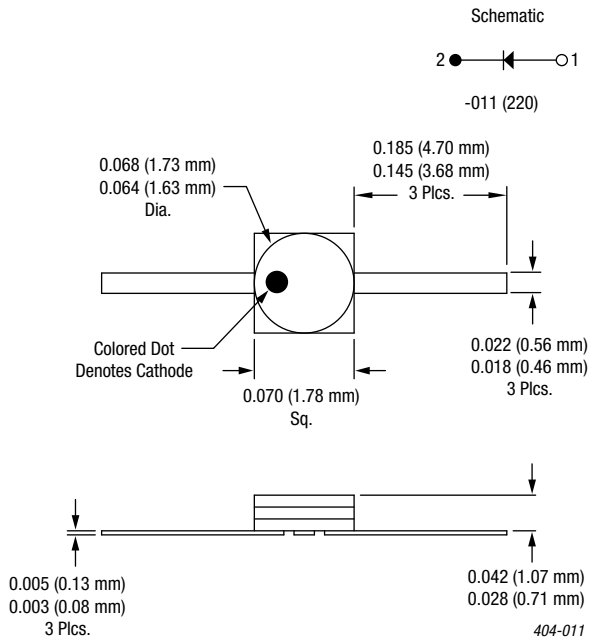
**-207**



**-250**



**-220**





**DATA SHEET**

# **DME, DMF, DMJ Series: Silicon Beam-Lead Schottky Mixer Diodes—Singles, Pairs and Quads Bondable and Packaged Chips**

**Applications**

- Designed for MIC applications
- Mixers
- Detectors

**Features**

- Low 1/f noise
- Low intermodulation distortion
- Epoxy and hermetically sealed packages
- SPC controlled wafer fabrication

**Description**

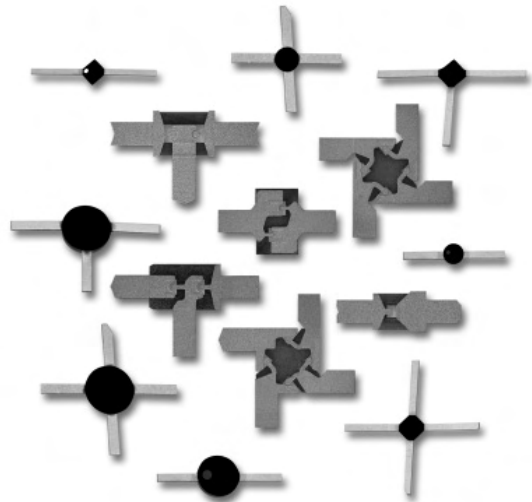
Skyworks beam-lead silicon Schottky barrier mixer diodes are designed for applications through 40 GHz. The beam-lead design reduces the problem of bonding to the very small area characteristic of the low capacitance junctions.

Beam-lead Schottky barrier mixer diodes are made by the deposition of a suitable barrier metal on an epitaxial silicon substrate to form the junction. The process and choice of materials result in low series resistance with a narrow spread of capacitance values for close impedance control.

A variety of forward voltages are available, ranging from low values for low, or starved, local oscillator drive levels to high values for high drive, low distortion mixer applications. Beam-lead diodes are available in a wide range of packages. Capacitance ranges and series resistances are comparable with the packaged devices that are available through K-band. Unpackaged diodes are well suited for use in microwave integrated circuits. The packaged devices are designed to be inserted as hybrid elements in strip, transmission line applications.

Beam-lead Schottky barrier diodes are categorized by universal mixer applications in four frequency ranges: S, X, Ku and Ka bands. They may also be used as modulators and high-speed switches.

Beam-lead diodes are suited for balanced mixers, due to their low parasitics and uniformity. A typical  $V_F$  vs.  $I_F$  curve is shown in Figure 1. Typical noise figures vs. LO drive is shown in Figure 2 for single N-type, low drive diode types.


**Frequency Table**

Band	Frequency
S	2–4
C	4–8
X	8.2–12.4
Ku	12.4–18

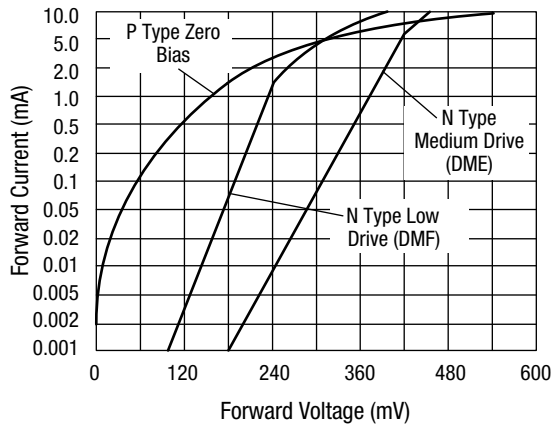


Figure 1. Typical Forward DC Characteristics Curves Voltage vs. Current

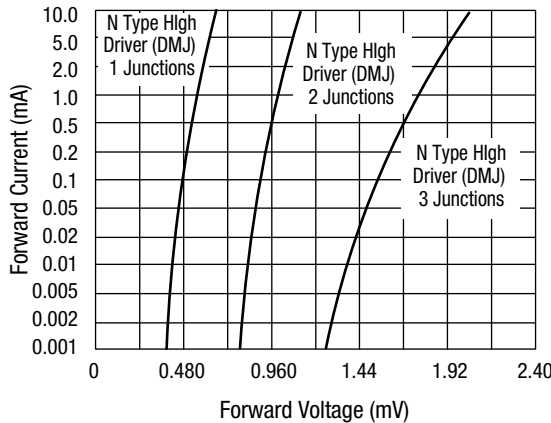


Figure 2. Typical Forward DC Characteristics Curves Voltage vs. Current

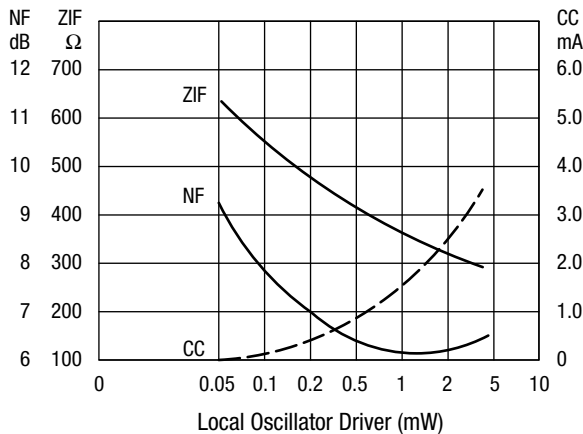


Figure 3. Typical X Band Low Drive Mixer Diode RF Parameters vs. Local Oscillator Drive

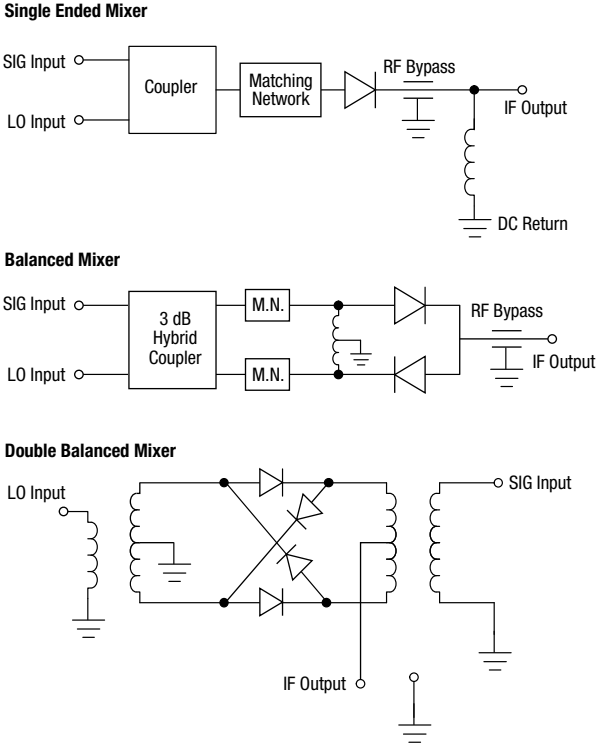


Figure 4. Typical Mixer Circuits

Ordering Information

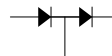
To order a packaged diode, simply append the part number to the package outline number. For example, a Medium Drive Ring Quad, Ku band (part number DME2859-000) in a 234 package would be ordered as DME2859-234.

**Beam-Lead Single, N-Type, Low, Medium, High Drive Schottky Diodes** —▶—

Beam-Lead	Frequency Band	$C_J$ 0 V @1 MHz (pF)	Max. $R_S$ @ 5 mA ( $\Omega$ )	Min. $V_B$ @ 10 $\mu$ A (V)	$V_F$ @ 1 mA (mV)	Drive Level	Outline Drawing
DMF2820-000	S	0.30–0.50	5	2	200–260	Low	491-011
DME2127-000	S	0.30–0.50	5	3	300–400	Med	491-011
DMJ2823-000	S	0.30–0.50	5	4	500–600	High	491-011
DMF2821-000	X	0.15–0.30	8	2	250–310	Low	491-011
DME2957-000	X	0.15–0.30	8	3	325–425	Med	491-011
DMJ2777-000	X	0.15–0.30	8	4	550–650	High	491-011
DMF2344-000	Ku	0.05–0.15	13	2	260–330	Low	491-011
DME2333-000	Ku	0.05–0.15	13	3	350–450	Med	491-011
DMJ2824-000	Ku	0.05–0.15	13	4	500–680	High	491-011
DMF2822-000	K	0.1 Max.	18	2	270–350	Low	491-011
DME2458-000	K	0.1 Max.	18	3	375–550	Med	491-011
DMJ2825-000	K	0.1 Max.	18	4	600–700	High	491-011

**Epoxy and Hermetic Packaged Beam-Lead Single, N-Type, Low, Medium, High Drive Schottky Diodes**

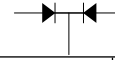
Epoxy Stripline 250	Epoxy Stripline 230	Hermetic Stripline 220
DMF2820-250		DMF2820-220
DME2127-250		DME2127-220
DMJ2823-250		DMJ2823-220
DMF2821-250		DMF2821-220
DME2957-250		DME2957-220
DMJ2777-250		DMJ2777-220
DMF2344-250	DMF2344-230	DMF2344-220
DME2333-250	DME2333-230	DME2333-220
DMJ2824-250	DMJ2824-230	DMJ2824-220
	DMF2822-230	DMF2822-220
	DME2458-230	DME2458-220
	DMJ2825-230	DMJ2825-220

**Beam-Lead Series Pair, N-Type, Low, Medium, High Drive Schottky Diodes**

Beam-Lead	Frequency Band	$C_J$ 0 V, 1 MHz (pF)	Max. $R_S$ @ 5 mA ( $\Omega$ )	Min. $V_B$ @ 10 $\mu$ A (V)	$V_F$ @ 1 mA (mV)	Drive Level	Outline Drawing
DMF2835-000	S	0.30–0.50	5	2	200–260	Low	504-012
DME2050-000	S	0.30–0.50	5	3	300–400	Med	504-012
DMJ2092-000	S	0.30–0.50	5	4	500–600	High	504-012
DMF2826-000	X	0.15–0.30	8	2	250–310	Low	504-012
DME2829-000	X	0.15–0.30	8	3	325–425	Med	504-012
DMJ2093-000	X	0.15–0.30	8	4	550–650	High	504-012
DMF2827-000	Ku	0.05–0.15	13	2	260–330	Low	504-012
DME2830-000	Ku	0.05–0.15	13	3	350–450	Med	504-012
DMJ2832-000	Ku	0.05–0.15	13	4	500–680	High	504-012
DMF2828-000	K	0.1 Max.	18	2	270–350	Low	504-012
DME2831-000	K	0.1 Max.	18	3	375–550	Med	504-012
DMJ2833-000	K	0.1 Max.	18	4	600–700	High	504-012

**Epoxy and Hermetic Packaged Beam-Lead Series Pair, N-Type, Low, Medium, High Drive Schottky Diodes**

Epoxy Stripline 252	Epoxy Stripline 232	Hermetic 222
DMF2835-252		DMF2835-222
DME2050-252		DME2050-222
DMJ2092-252		DMJ2092-222
DMF2826-252		DMF2826-222
DME2829-252		DME2829-222
DMJ2093-252		DMJ2093-222
DMF2827-252	DMF2827-232	DMF2827-222
DME2830-252	DME2830-232	DME2830-222
DMJ2832-252	DMJ2832-232	DMJ2832-222
	DMF2828-232	DMF2828-222
	DME2831-232	DME2831-222
	DMJ2833-232	DMJ2833-222

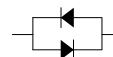
**Beam-Lead Common Cathode, N-Type, Low, Medium, High Drive Schottky Diodes**

Beam-Lead	Frequency Band	$C_J$ 0 V, 1 MHz (pF)	Max. $R_S$ @ 5 mA ( $\Omega$ )	Min. $V_B$ @ 10 $\mu$ A (V)	$V_F$ @ 1 mA (mV)	Drive Level	Outline Drawing
DMF2182-000	S	0.30–0.50	5	2	200–260	Low	504-013
DME2205-000	S	0.30–0.50	5	3	300–400	Med	504-013
DMJ2208-000	S	0.30–0.50	5	4	500–600	High	504-013
DMF2183-000	X	0.15–0.30	8	2	250–310	Low	504-013
DME2206-000	X	0.15–0.30	8	3	325–425	Med	504-013
DMJ2209-000	X	0.15–0.30	8	4	550–650	High	504-013
DMF2184-000	Ku	0.05–0.15	13	2	260–330	Low	504-013
DME2207-000	Ku	0.05–0.15	13	3	350–450	Med	504-013
DMJ2210-000	Ku	0.05–0.15	13	4	500–680	High	504-013
DMF2834-000	K	0.1 Max.	18	2	270–350	Low	504-013
DME2864-000	K	0.1 Max.	18	3	375–550	Med	504-013
DMJ2836-000	K	0.1 Max.	18	4	600–700	High	504-013

**Epoxy and Hermetic Packaged Beam-Lead Common Cathode, N-Type, Low, Medium, High Drive Schottky Diodes**

Epoxy Stripline 253	Hermetic Stripline 223
DMF2182-253	DMF2182-223
DME2205-253	DME2205-223
DMJ2208-253	DMJ2208-223
DMF2183-253	DMF2183-223
DME2206-253	DME2206-223
DMJ2209-253	DMJ2209-223
DMF2184-253	DMF2184-223
DME2207-253	DME2207-223
DMJ2210-253	DMJ2210-223
	DMF2834-223
	DME2864-223
	DMJ2836-223

## Beam-Lead Antiparallel, N-Type, Low, Medium, High Drive Schottky Diodes



Beam-Lead	Frequency Band	$C_J$ 0 V, 1 MHz (pF)	Max. $R_S$ @ 5 mA ( $\Omega$ )	Min. $V_B$ @ 10 $\mu$ A (V)	$V_F$ @ 1 mA (mV)	Drive Level	Outline Drawing
DMF2185-000	S	0.30–0.50	5	2	200–260	Low	522-025
DME2282-000	S	0.30–0.50	5	3	300–400	Med	522-025
DMJ2303-000	S	0.30–0.50	5	4	500–600	High	522-025
DMF2186-000	X	0.15–0.30	8	2	250–310	Low	522-025
DME2283-000	X	0.15–0.30	8	3	325–425	Med	522-025
DMJ2304-000	X	0.15–0.30	8	4	550–650	High	522-025
DMF2187-000	Ku	0.05–0.15	13	2	260–330	Low	522-025
DME2284-000	Ku	0.05–0.15	13	3	350–450	Med	522-025
DMJ2246-000	Ku	0.05–0.15	13	4	500–680	High	522-025
DMF2837-000	K	0.1 Max.	18	2	270–350	Low	522-025
DME2838-000	K	0.1 Max.	18	3	375–550	Med	522-025
DMJ2839-000	K	0.1 Max.	18	4	600–700	High	522-025

## Epoxy and Hermetic Packaged Beam-Lead Antiparallel, N-Type, Low, Medium, High Drive Schottky Diodes

Epoxy Stripline 251	Hermetic Stripline 221
DMF2185-251	DMF2185-221
DME2282-251	DME2282-221
DMJ2303-251	DMJ2303-221
DMF2186-251	DMF2186-221
DME2283-251	DME2283-221
DMJ2304-251	DMJ2304-221
DMF2187-251	DMF2187-221
DME2284-251	DME2284-221
DMJ2246-251	DMJ2246-221
	DMF2837-221
	DME2838-221
	DMJ2839-221

**Beam-Lead Ring Quad, N-Type, Low, Medium, High Drive Schottky Diodes**

Beam-Lead	Frequency Band	$C_J$ 0 V, 1 MHz (pF)	Max. $R_S$ @ 5 mA ( $\Omega$ )	Min. $V_B$ @ 10 $\mu$ A (V)	$V_F$ @ 1 mA (mV)	Drive Level	Outline Drawing
DMF2865-000	S	0.30–0.50	5	2	200–260	Low	488-002
DME2857-000	S	0.30–0.50	5	3	300–400	Med	488-002
DMJ2502-000	S	0.30–0.50	5	4	500–600	High	488-002
DMF2011-000	X	0.15–0.30	8	2	250–310	Low	488-002
DME2858-000	X	0.15–0.30	8	3	325–425	Med	488-002
DMJ2990-000	X	0.15–0.30	8	4	550–650	High	488-002
DMF2012-000	Ku	0.05–0.15	13	2	260–330	Low	488-002
DME2859-000	Ku	0.05–0.15	13	3	350–450	Med	488-002
DMJ2667-000	Ku	0.05–0.15	13	4	500–680	High	488-002
DMF2454-000	K	0.1 Max.	18	2	270–350	Low	488-002
DME2459-000	K	0.1 Max.	18	3	375–550	Med	488-002
DMJ2455-000	K	0.1 Max.	18	4	600–700	High	488-002

**Epoxy and Hermetic Packaged Beam-Lead Ring Quad, N-Type, Low, Medium, High Drive Schottky Diodes**

Epoxy Stripline 254	Epoxy Stripline 234	Hermetic Stripline 224
DMF2865-254		DMF2865-224
DME2857-254		DME2857-224
DMJ2502-254		DMJ2502-224
DMF2011-254		DMF2011-224
DME2858-254		DME2858-224
DMJ2990-254		DMJ2990-224
DMF2012-254	DMF2012-234	DMF2012-224
DME2859-254	DME2859-234	DME2859-224
DMJ2667-254	DMJ2667-234	DMJ2667-224
	DMF2454-234	DMF2454-224
	DME2459-234	DME2459-224
	DMJ2455-234	DMJ2455-224



### Beam-Lead Bridge Quad, N-Type, Low, Medium, High Drive Schottky Diodes

Beam-Lead	Frequency Band	$C_J$ 0 V, 1 MHz (pF)	Max. $R_S$ @ 5 mA ( $\Omega$ )	Min. $V_B$ @ 10 $\mu$ A (V)	$V_F$ @ 1 mA (mV)	Drive Level	Outline Drawing
DMF2076-000	S	0.30–0.50	5	2	200–260	Low	488-004
DME2029-000	S	0.30–0.50	5	3	300–400	Med	488-004
DMJ2312-000	S	0.30–0.50	5	4	500–600	High	488-004
DMF2077-000	X	0.15–0.30	8	2	250–310	Low	488-004
DME2850-000	X	0.15–0.30	8	3	325–425	Med	488-004
DMJ2088-000	X	0.15–0.30	8	4	550–650	High	488-004
DMF2078-000	Ku	0.05–0.15	13	2	260–330	Low	488-004
DME2031-000	Ku	0.05–0.15	13	3	350–450	Med	488-004
DMJ2768-000	Ku	0.05–0.15	13	4	500–680	High	488-004
DMF2848-000	K	0.1 Max.	18	2	270–350	Low	488-004
DME2851-000	K	0.1 Max.	18	3	375–550	Med	488-004
DMJ2852-000	K	0.1 Max.	18	4	600–700	High	488-004

### Epoxy and Hermetic Packaged Beam-Lead Bridge Quad, N-Type, Low, Medium, High Drive Schottky Diodes

Stripline 255	Stripline 235	Hermetic Stripline 225
DMF2076-255		DMF2076-225
DME2029-255		DME2029-225
DMJ2312-255		DMJ2312-225
DMF2077-255		DMF2077-225
DME2850-255		DME2850-225
DMJ2088-255		DMJ2088-225
DMF2078-255	DMF2078-235	DMF2078-225
DME2031-255	DME2031-235	DME2031-225
DMJ2768-255	DMJ2768-235	DMJ2768-225
	DMF2848-235	DMF2848-225
	DME2851-235	DME2851-225
	DMJ2852-235	DMJ2852-225





## Epoxy Packaged Octo Quad Ring, N-Type, Low, Medium, High Drive Schottky Diodes

Part Number	Frequency Band	$C_J$ 0 V, 1 MHz (pF)	Max. $R_S$ @ 5 mA ( $\Omega$ )	Min. $V_B$ @ 10 $\mu$ A (V)	$V_F$ @ 1 mA (mV)	Drive Level
DME3938-257	S-X	0.15–0.30	16	4	400–520	Low
DMF3939-257	S-X	0.15–0.30	16	6	600–800	Medium
DMJ3940-257	S-X	0.15–0.30	16	8	1000–1200	High

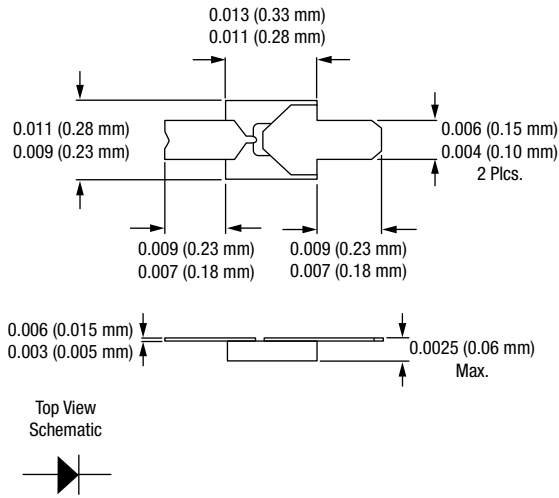
## Absolute Maximum Ratings

Characteristic	Value
Maximum current ( $I_{MAX}$ )	100 mA
Power dissipation ( $P_D$ ) CW	75 mW/junction
Storage temperature ( $T_{ST}$ )	–65 °C to +175 °C
Operating temperature ( $T_{OP}$ )	–65 °C to +175 °C

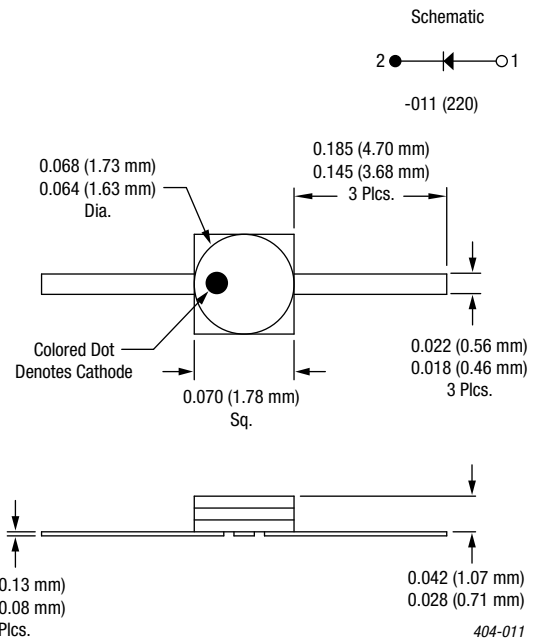
Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum Ratings. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

**CAUTION:** Although these devices are designed to be robust, ESD (Electrostatic Discharge) can cause permanent damage. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.

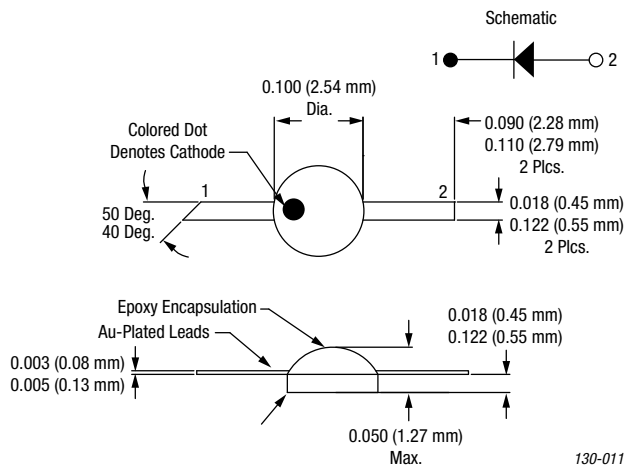
## 491-011



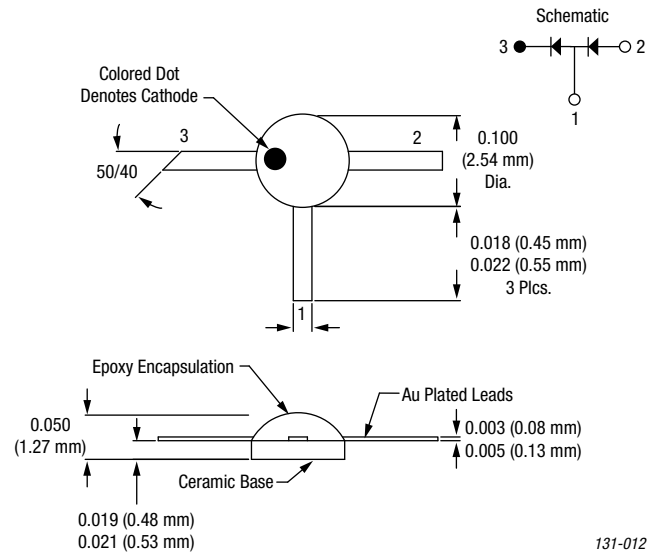
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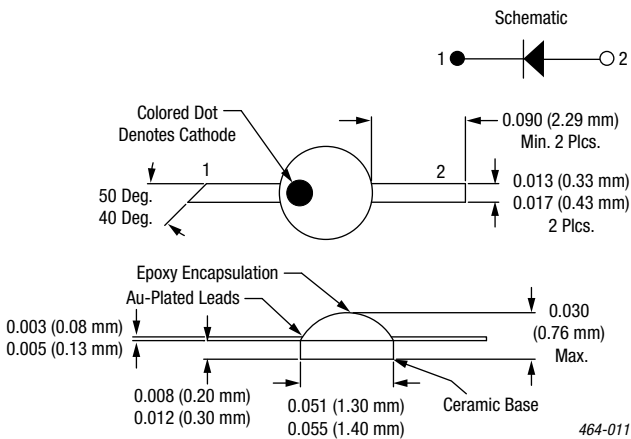
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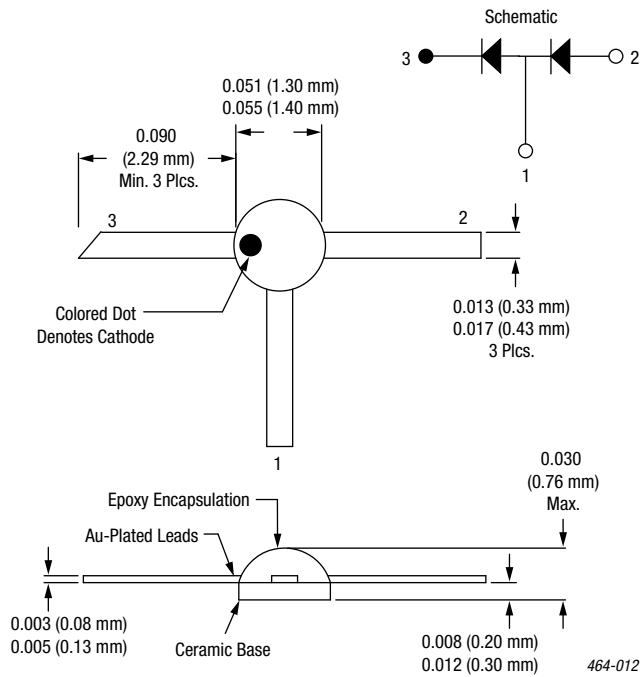
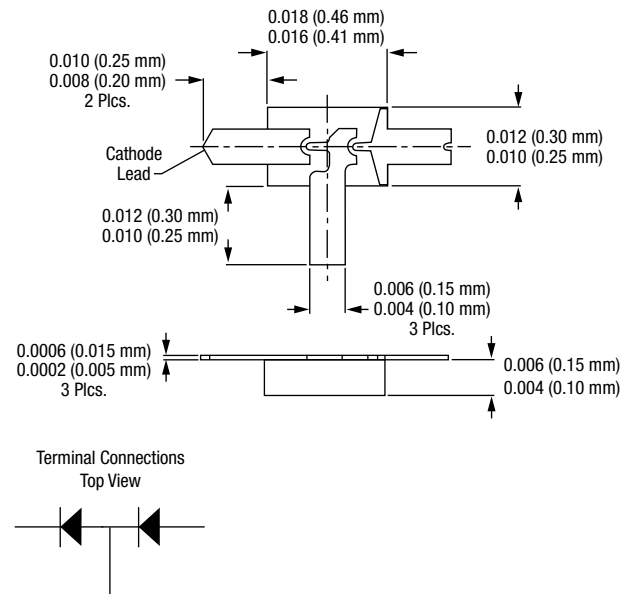
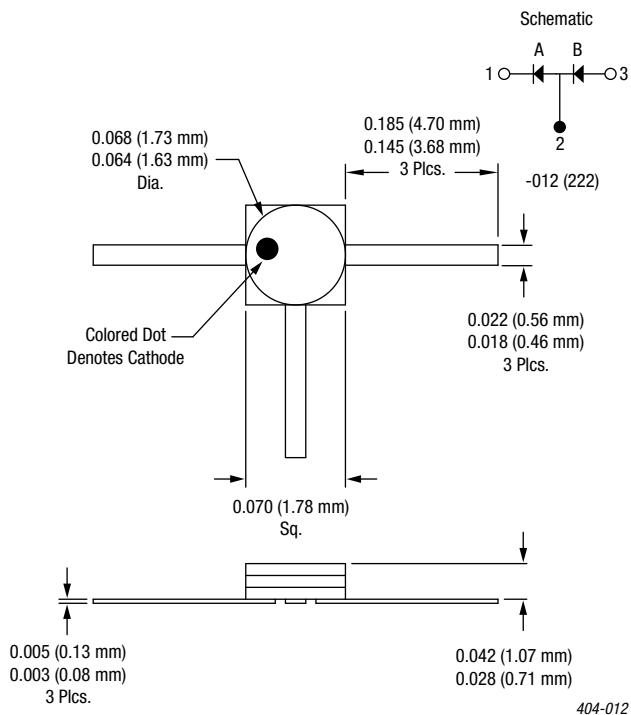
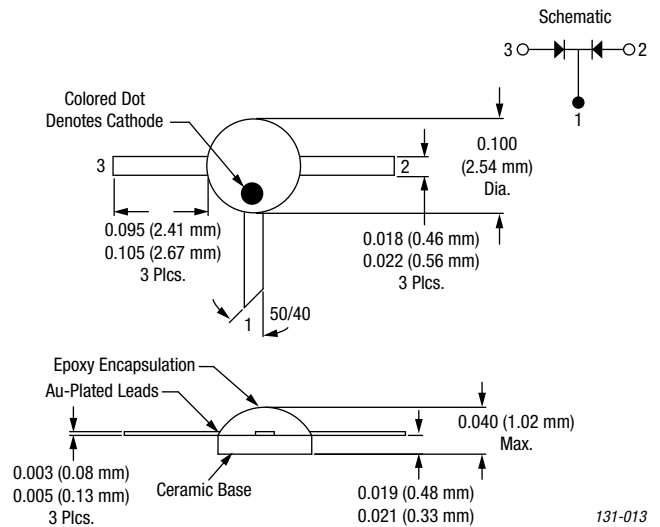


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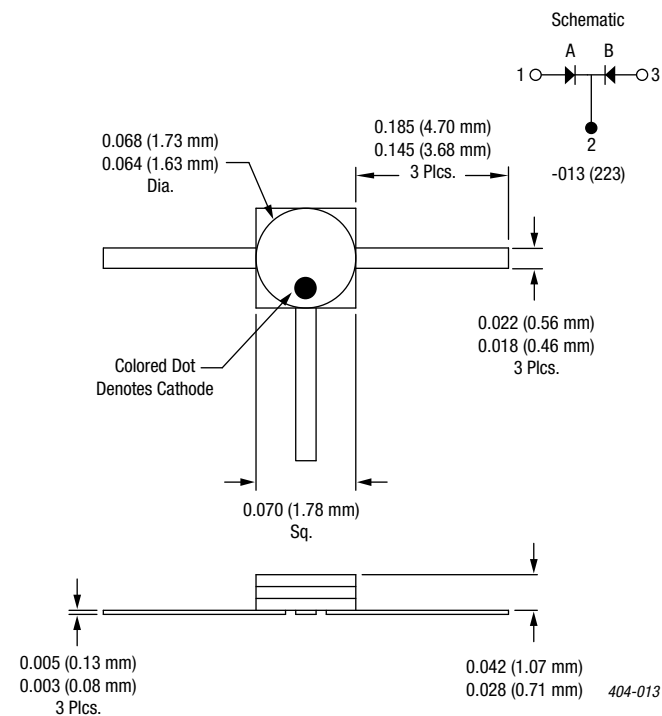


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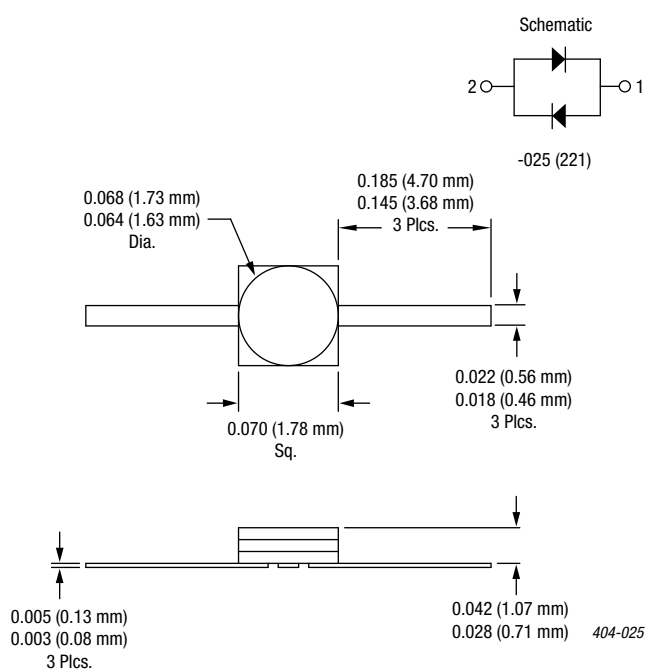


**-232****504-012****-222****-253**

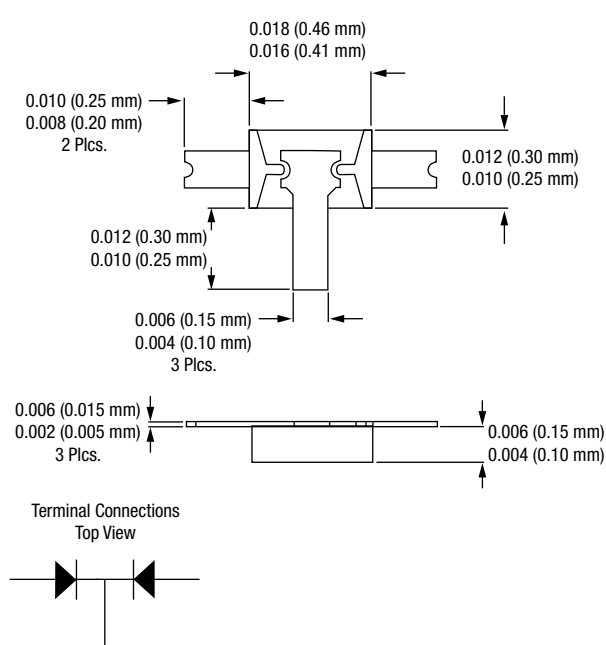
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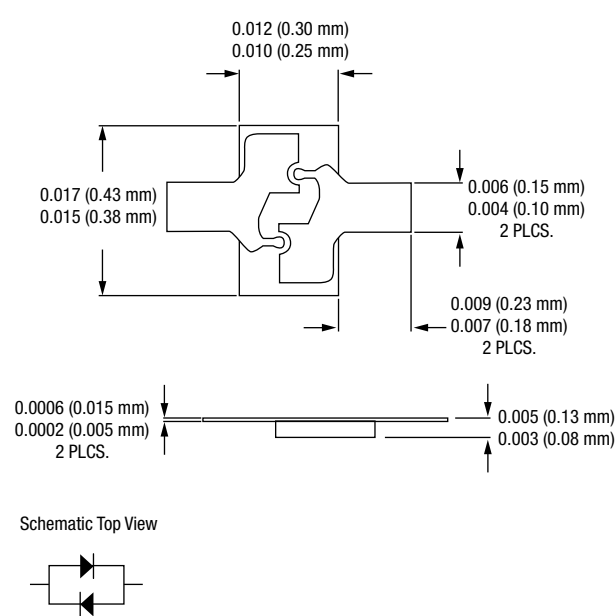
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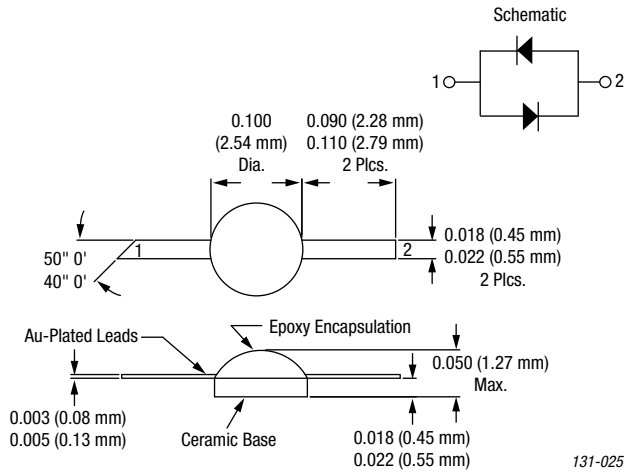
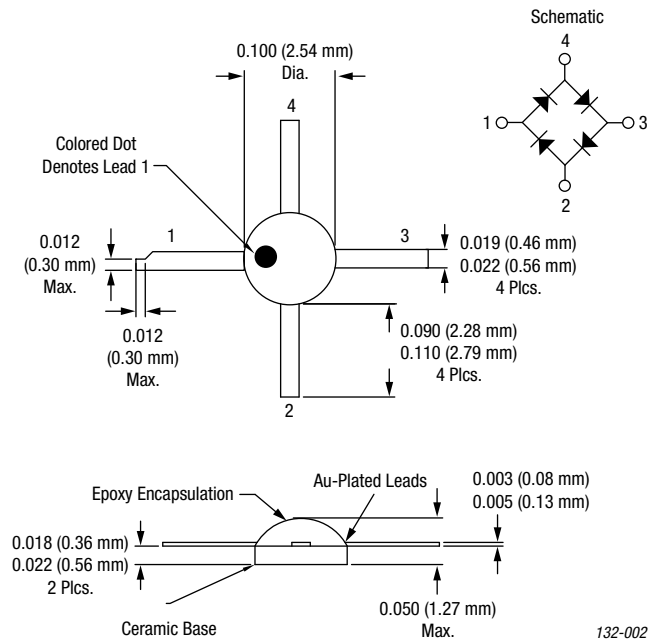
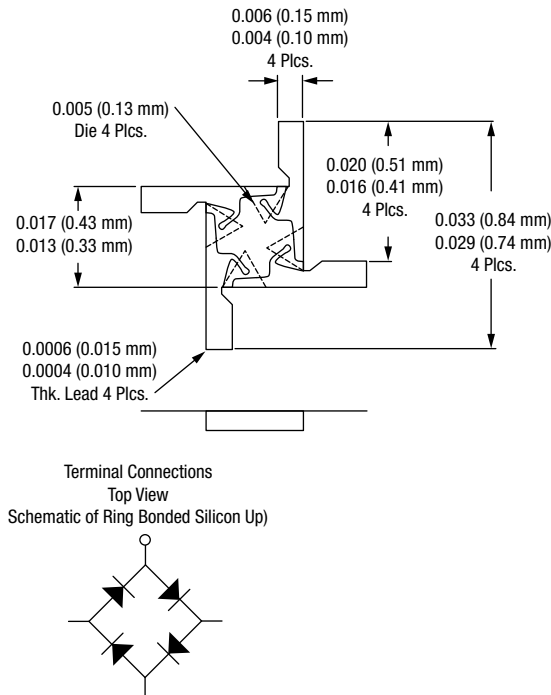
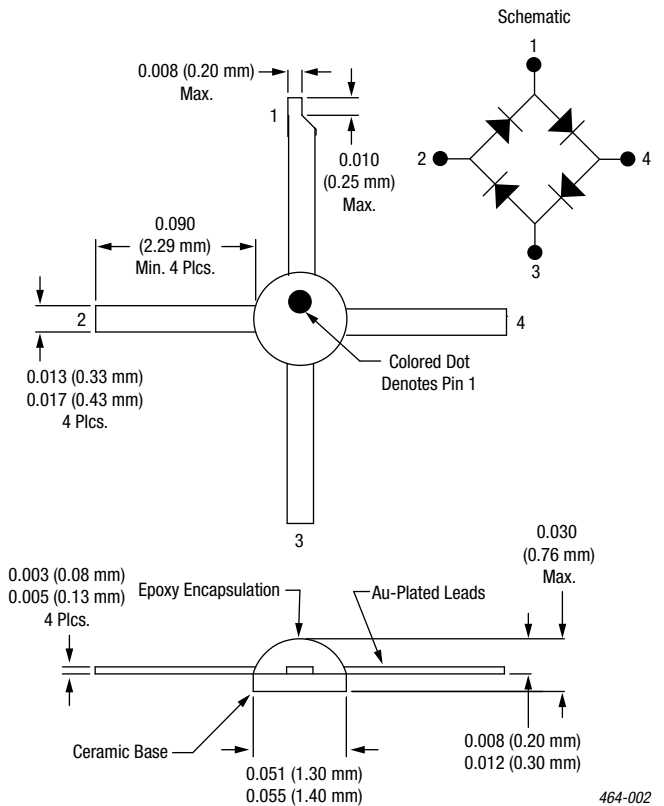


504-013

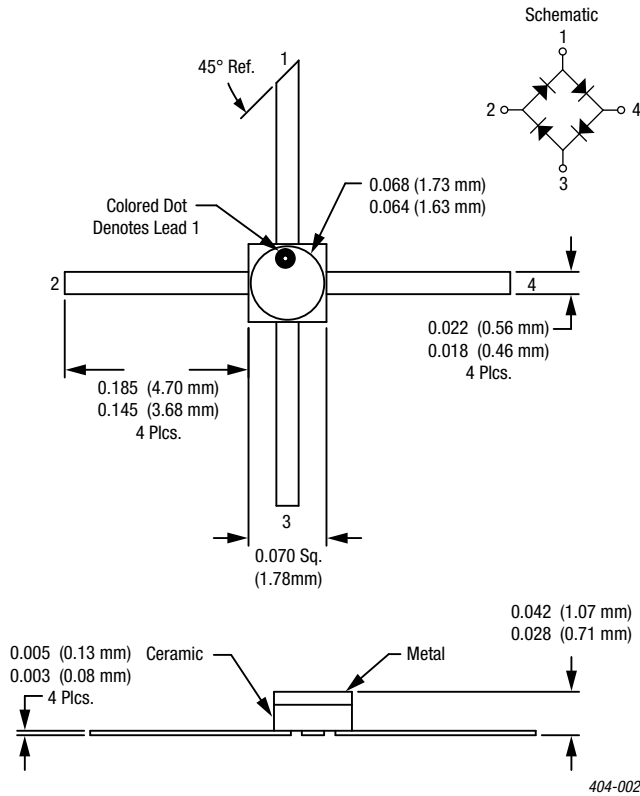


522-025

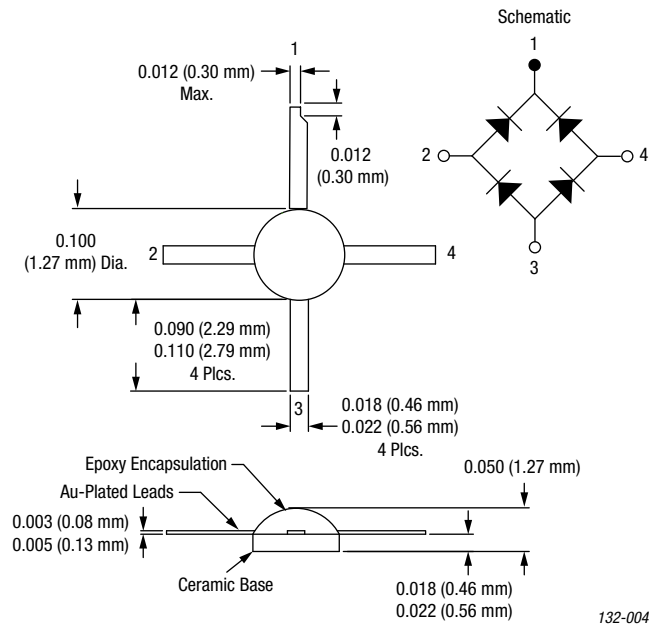


**-251****-254****488-002****-234**

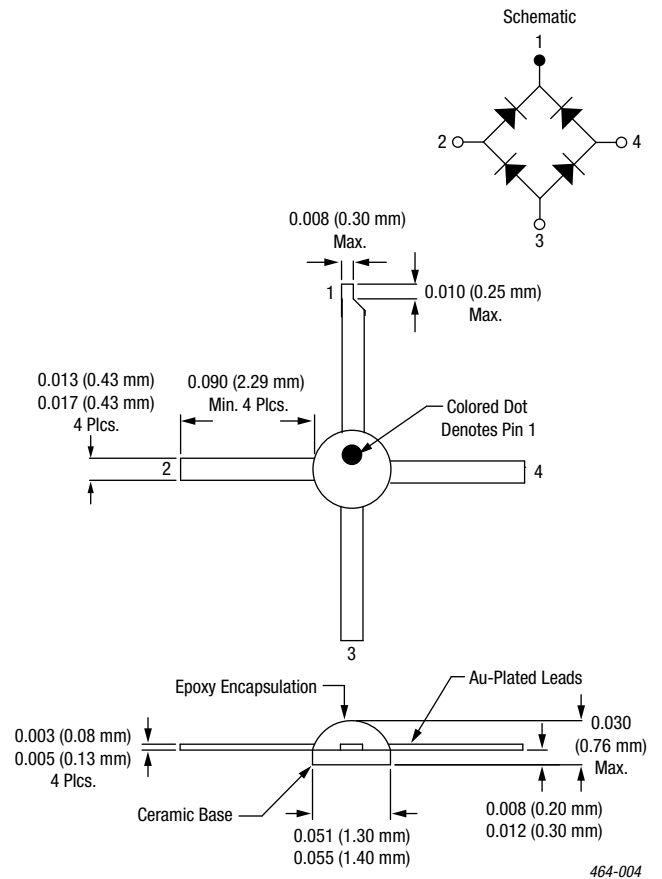
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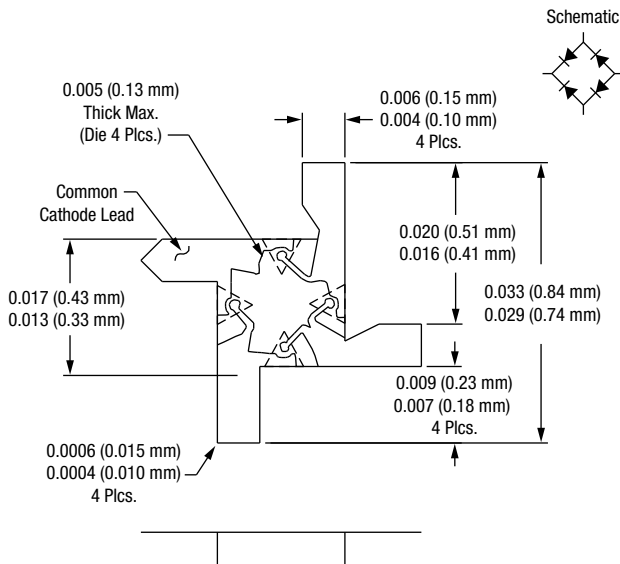
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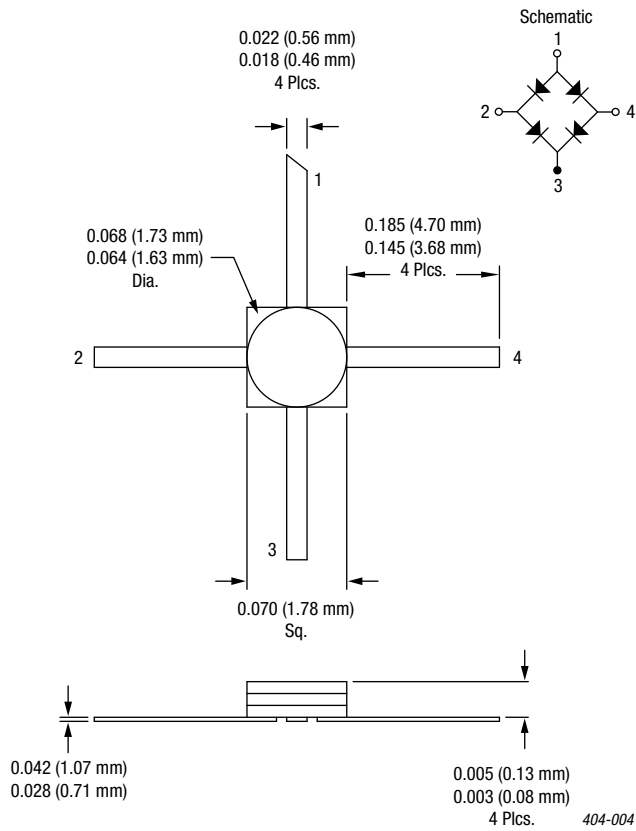
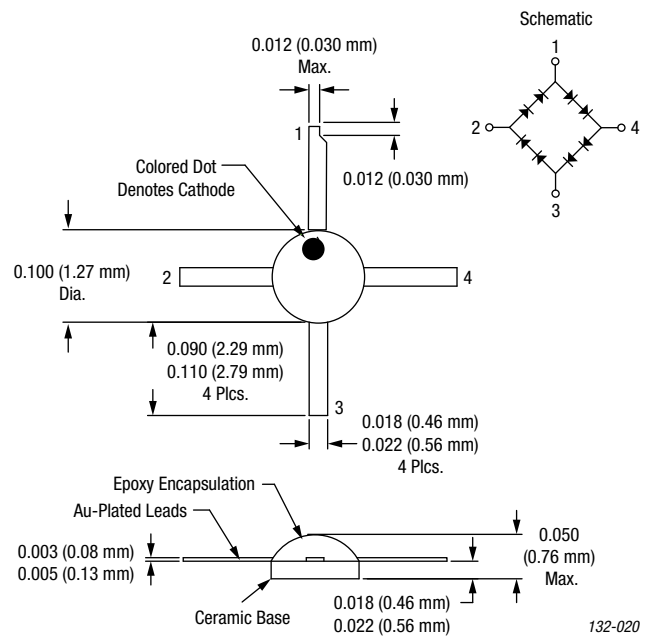


-235



488-004



**-225****-257**

**DATA SHEET**

# Silicon Schottky Diodes in Hermetic Surface Mount Package

**Applications**

- Mixers
- Detectors

**Features**

- Medium, low and ZBD barrier diodes
- Hermetic ceramic package, 1.83 x 1.43 x 1.0 mm
- Usable to 10 GHz
- Low inductance 0.48 nH typ.
- Operating temperature range -55 °C to 150 °C
- ESD Class 0, human body model
- Lead (Pb)-free, RoHS-compliant, and Green™, MSL-1 @ 260 °C per JEDEC J-STD-020

**Description**

The family of proven silicon Schottky diodes is packaged in a hermetic, ceramic package. This package offers excellent, very low parasitic inductance and capacitance for wide bandwidth, high-frequency operation. It has low thermal impedance and meets fine and gross leak requirements for excellent reliability. Its small form factor, 1.83 x 1.43 x 1.0 mm, compares favorably to that of the smallest plastic packages.

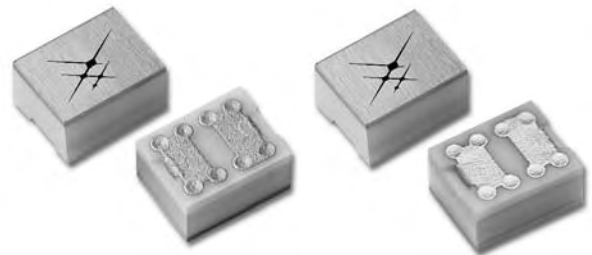
This package meets Skyworks definition of Green: it is lead (Pb)-free, fully complies with current RoHS requirements and contains no halogens and no antimony (Sb).

The SMS3922-108 and SMS3923-108 are silicon medium barrier Schottky diodes suitable for use in mixers and high level detector circuits.

The SMS7621-108 is a silicon low barrier Schottky diode, suitable for use in small signal, sensitive detector circuits.

The SMS7630-109 is a silicon Schottky zero bias detector diode (ZBD) diode, suitable for use in the most sensitive detector circuits.

The diodes available in this package can operate over the temperature range of -55 °C to 150 °C.



**NEW** Skyworks Green™ products are RoHS (Restriction of Hazardous Substances)-compliant, conform to the EIA/EICTA/JEITA Joint Industry Guide (JIG) Level A guidelines, are halogen free according to IEC-61249-2-21, and contain <1,000 ppm antimony trioxide in polymeric materials.



## Electrical Specifications

**T = 25 °C, unless otherwise noted**

Part Number	Barrier Height	Reverse Breakdown Voltage $I_R = 10 \mu A$ (V)	Reverse Current (nA)	Total Capacitance $V_R = 0 V$ $f = 1 MHz$ (pF)		Forward Voltage $I_F = 1 mA$ (mV)		ESD Rating, Human Body Model
		Min.	Max.	Min.	Max.	Min.	Max.	
SMS3922-108	Med./Low	8	100 @ 1.0 V		1.5	280	340	Class 0
SMS3923-108	Medium	20	500 @ 15 V	0.875	1.275	310	370	Class 0

Part Number	Barrier Height	Reverse Breakdown Voltage $I_R = 10 \mu A$ (V)	Total Capacitance $V_R = 0 V$ & $f = 1 MHz$ (pF)	Forward Voltage $I_F = 1 mA$ (mV)		Slope Resistance $I_F = 5 mA$ ( $\Omega$ )	ESD Rating, Human Body Model
		Min.	Max.	Min.	Max.	Max.	
SMS7621-108	Low	2	0.325	260	320	18	Class 0

Part Number	Barrier Height	Reverse Breakdown Voltage $I_R = 100 \mu A$ (V)	Total Capacitance $V_R = 0.15 V$ & $f = 1 MHz$ (pF)	Forward Voltage $I_F = 100 \mu A$ (mV)		Forward Voltage $I_F = 1 mA$ (mV)		Video Resistance ( $\Omega$ )	ESD Rating, Human Body Model
		Min.	Typ.	Min.	Max.	Min.	Max.	Typ.	
SMS7630-109	ZBD	1	0.50	65	100	135	240	5000	Class 0

## Absolute Maximum Ratings

Characteristic	Value
Reverse voltage	Minimum Reverse Breakdown Voltage
Forward current	100 mA
Dissipated power at 25 °C	250 mW
Operating temperature	-55 °C to +150 °C
Storage temperature	-65 °C to +200 °C
Electrostatic Discharge (ESD) Human Body Mode (HBM)	Class 0
Electrostatic Discharge (ESD) Charged Device Model (CDM)	Class C4

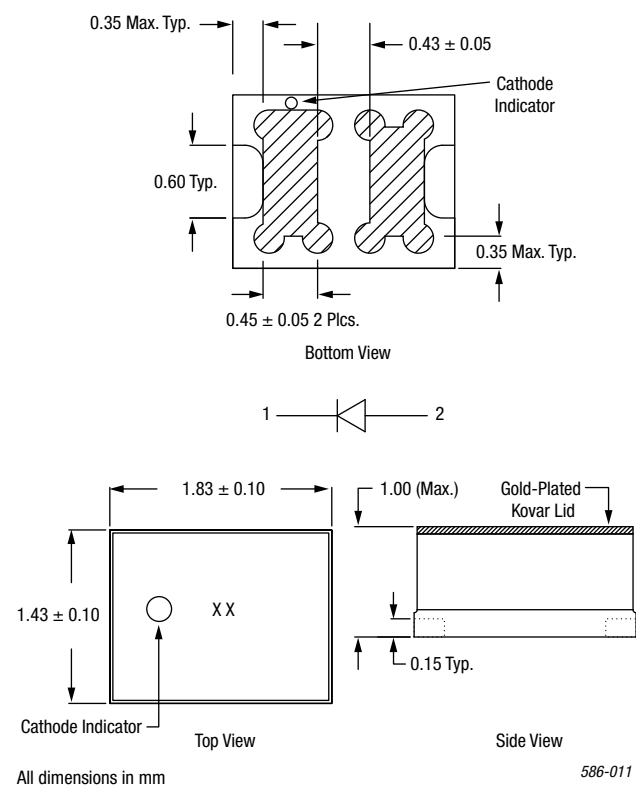
Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum Ratings. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

**CAUTION:** Although these devices are designed to be robust, ESD (Electrostatic Discharge) can cause permanent damage. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.

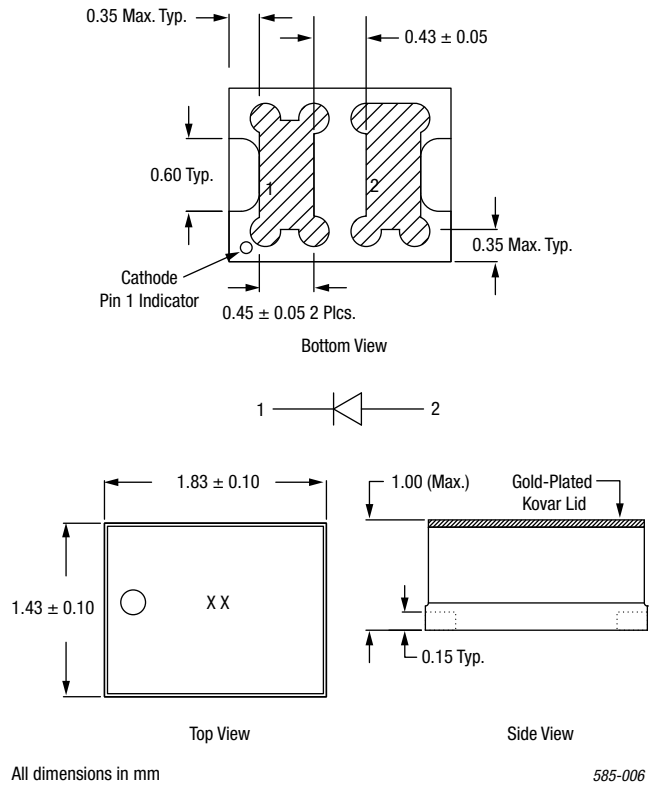
## SPICE Model Parameters

Parameter	Unit	SMS7621	SMS3922	SMS3923	SMS7630
$I_S$	A	9e-8	1e-8	5e-9	5e-6
$R_S$	$\Omega$	6	5	11	20
N		1.1	1.04	1.05	1.05
TT	s	1e-11	8e-11	8e-11	1e-11
$C_{J0}$	pF	0.10	0.9	0.9	0.14
M		0.35	0.26	0.24	0.40
$E_G$	eV	0.69	0.69	0.69	0.69
XTI		2	2	2	2
$F_C$		0.5	0.5	0.5	0.5
$B_V$	V	3	20	46	2
$I_{BV}$	A	1e-5	1e-5	1e-5	1e-4
$V_J$	V	0.51	0.595	0.64	0.34
$L_S$	nH	0.48			
$C_P$	pF	0.07			

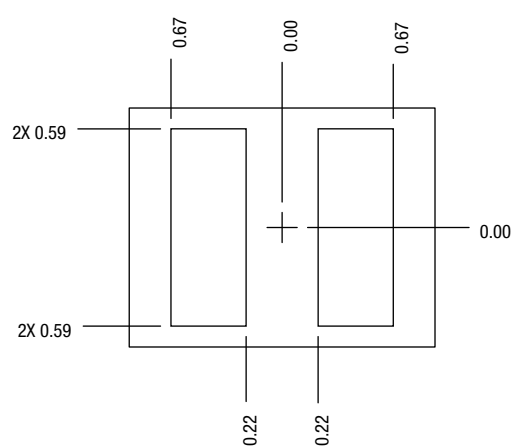
-108



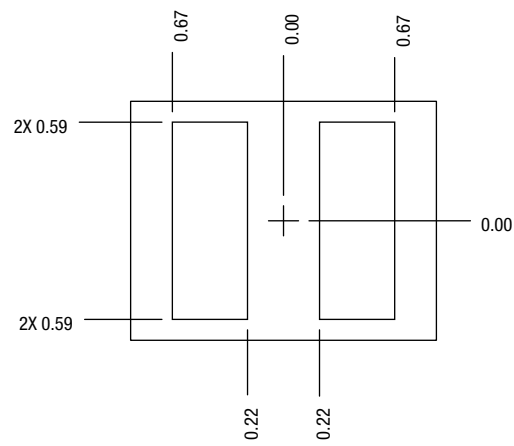
-109



-108 Land Pattern



-109 Land Pattern



**DATA SHEET**

# Chip On Board Mixer Quads

## Applications

- Double balanced mixers
- Sampling circuits

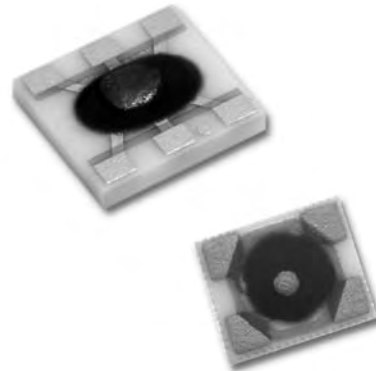
## Features

- High-volume automatic assembly
- For microwave MIC assembly and automated high-volume manufacturing
- Mechanically rugged design
- 100% DC tested
- Three barrier heights for customized mixer performance
- Lead (Pb)-free, RoHS-compliant, and Green™

## Description

Skyworks ceramic Chip on Board (COB) mixer quads are designed for high-performance RF and microwave receiver applications. These devices utilize Skyworks advanced silicon beamless Schottky technology, combined with precision ceramic COB assembly techniques, to achieve a high degree of device reliability in commercial applications.

**NEW** Skyworks Green™ products are RoHS (Restriction of Hazardous Substances)-compliant, conform to the EIA/EICTA/JEITA Joint Industry Guide (JIG) Level A guidelines, are halogen free according to IEC-61249-2-21, and contain <1,000 ppm antimony trioxide in polymeric materials.



## Absolute Maximum Ratings

Characteristic	Value
Maximum current ( $I_{MAX}$ )	50 mA
Power dissipation ( $P_D$ ) CW	75 mW/junction
Storage temperature ( $T_{ST}$ )	-65 °C to +175 °C
Operating temperature ( $T_{OP}$ )	-65 °C to +150 °C
Electrostatic Discharge (ESD) Human Body Model (HBM)	Class 0

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum Ratings. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

**CAUTION:** Although these devices are designed to be robust, ESD (Electrostatic Discharge) can cause permanent damage. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.

## Electrical Specifications at 25 °C

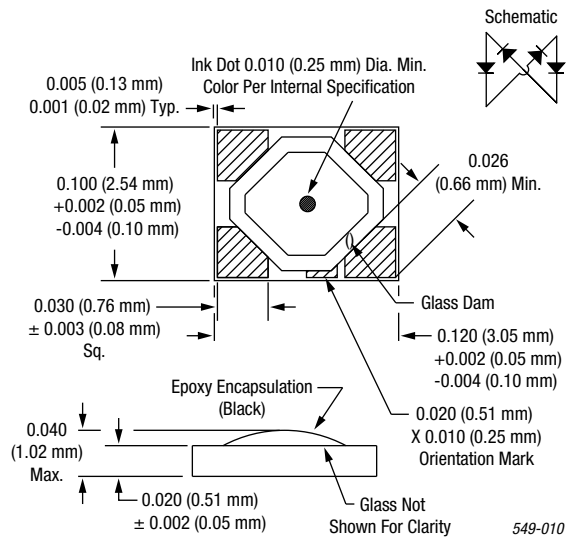
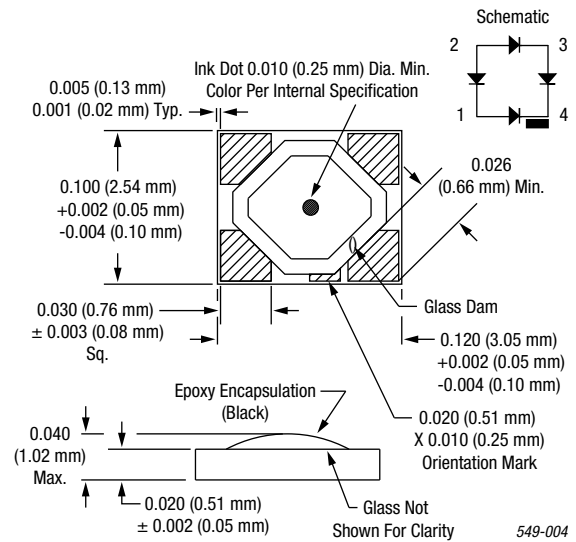
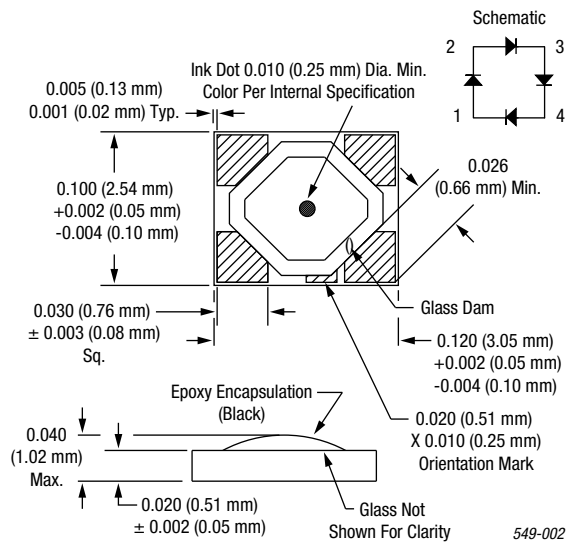
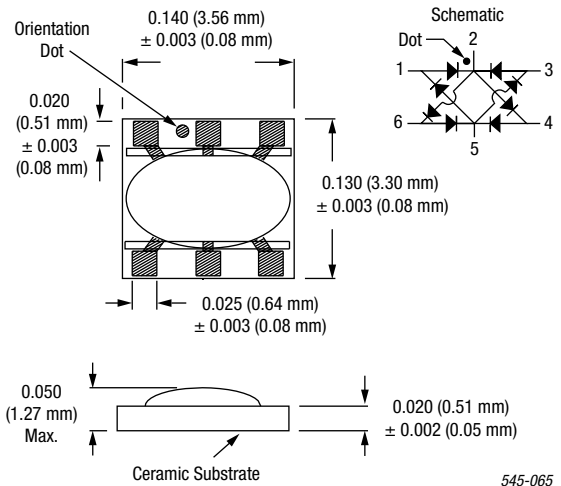
Part Number	Barrier	$V_F$ $I_F = 1 \text{ mA}$ (mV)	Max. $\Delta V_F$ $I_F = 1 \text{ mA}^{(1)}$ (mV)	$C_J$ $V_R = 0 \text{ V}$ , $F = 1 \text{ MHz}$ (pF)	Max. $\Delta C_T @ 0 \text{ V}$ (pF)	Max. $R_T$ $I_F = 10 \text{ mA}$ ( $\Omega$ )	Min. $V_B @ 10 \mu\text{A}$ (Min.)	Outline Drawing
<b>Ring Quads (To 6 GHz)</b>								
DMF3926-101	Low	200–260	15	0.3–0.5	0.07	8	–	549-002
DME3927-101	Medium	300–400	15	0.3–0.5	0.07	8	–	549-002
DMJ3928-101	High	525–625	15	0.3–0.5	0.07	8	–	549-002
<b>Crossover Ring Quads (To 6 GHz)</b>								
DMF3926-100	Low	200–260	15	0.3–0.5	0.07	8	–	549-010
DME3927-100	Medium	300–400	15	0.3–0.5	0.07	8	–	549-010
DMJ3928-100	High	525–625	15	0.3–0.5	0.07	8	–	549-010
<b>Back-to-Back Crossover Ring Quads (To 6 GHz)</b>								
DMF3945-103	Low	200–260	15	0.3–0.5	0.07	8	–	545-065
DME3946-103	Medium	300–400	15	0.3–0.5	0.07	8	–	545-065
DMJ3947-103	High	525–625	15	0.3–0.5	0.07	8	–	545-065
<b>Bridge Quads (To 6 GHz)</b>								
DMF3929-102	Low	200–260	15	0.3–0.5	0.07	8	2	545-065
DME3930-102	Medium	300–400	15	0.3–0.5	0.07	8	3	545-065
DMJ3931-102	High	525–625	15	0.3–0.5	0.07	8	4	545-065

1. Forward voltage difference between package electrodes.

2. Capacitance difference between package electrodes.

## SPICE Model Parameters (Per Junction)

Parameter	Unit	DMF3926 DMF3929 DMF3945	DME3927 DME3930 DME3946	DMJ3928 DMJ3931 DMJ3947
$I_S$	A	2.5E–07	1.3E–09	9.0E–13
$R_S$	$\Omega$	4	4	4
N		1.04	1.04	1.04
TT	s	1E–11	1E–11	1E–11
$C_{J0}$	pF	0.42	0.39	0.39
M		0.32	0.37	0.42
$E_G$	eV	0.69	0.69	0.69
XTI		2	2	2
$F_C$		0.5	0.5	0.5
$B_V$	V	2	3	4
$I_{BV}$	A	1E–05	1E–05	1E–05
$V_J$	V	0.495	0.595	0.8

**-100****-102****-101****-103**

Bottom side is free of metallization.

The minimum specified area of the contact pads (0.017 x 0.022) shall be free of epoxy.

**DATA SHEET**

# DMF3926-116, DME3927-116, DMJ3928-116: Surface Mount Hermetic Silicon Schottky Crossover Ring Quads

**Applications**

- Double-balanced mixers

**Features**

- Surface mount crossover ring quads
- Low, medium and high barrier devices
- Suitable for use up to 4 GHz
- Low parasitic impedance
- Miniature hermetic ceramic package
- Lead (Pb)-free, RoHS-compliant, and Green™, MSL-1 @ 260 °C per JEDEC J-STD-020
- ESD Class 0, Human Body Model

**Description**

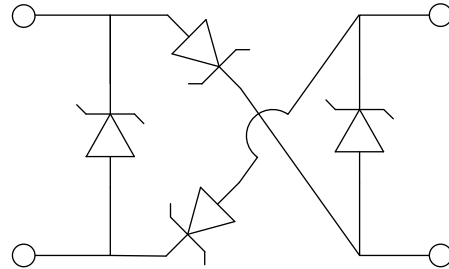
This family of crossover ring quads comprised of silicon Schottky diodes is offered with one of three barrier heights. DMF3926-116 contains low barrier diodes, DME3927-116 contains medium barrier diodes and DMJ3928-116 contains high barrier diodes. Each of these parts is packaged in a surface mount, 1.7 x 2 x 1.1 mm hermetic ceramic package.

These ring quads are fabricated as single dice that contain all four junctions and the crossover connection, thereby inherently matching electrical characteristics including capacitance, forward voltage and series resistance.

This package meets fine and gross leak test requirements per MIL-STD-750. It is lead (Pb)-free and fully complies with current RoHS requirements. It also meets Skyworks definition of Green: it contains no halogens or antimony (Sb).

SPICE parameters are provided.

These ring quads can operate over the temperature range of -40 °C to +85 °C.

**Functional Diagram**


**NEW** Skyworks Green™ products are RoHS (Restriction of Hazardous Substances)-compliant, conform to the EIA/EICTA/JEITA Joint Industry Guide (JIG) Level A guidelines, are halogen free according to IEC-61249-2-21, and contain <1,000 ppm antimony trioxide in polymeric materials.

## Electrical Specifications

**T = 25 °C, per junction, unless otherwise noted**

Part Number	Breakdown Voltage @ $I_R = 10 \mu A^{(1)}$ (V)	Total Capacitance @ $V_R = 0 V^{(2)}$ (pF)	Forward Voltage @ $I_F = 5 mA$ (mV)		Forward Voltage @ $I_F = 10 mA$ (mV)		Forward Voltage Difference per Pair @ $I_F = 5 mA$ (mV)	Forward Voltage Difference per Pair @ $I_F = 10 mA$ (mV)	Total Resistance @ $I_F = 5 mA$ ( $\Omega$ )
	Min.	Max.	Min.	Max.	Min.	Max.	Max.	Max.	Max.
DMF3926-116	2	0.55	260	330			10	10	10
DME3927-116	3	0.55			435	520		10	12
DMJ3928-116	5	0.55			610	700		10	10

1. It is not possible to measure breakdown voltage on any junction in a ring quad.

2. In a ring quad the capacitance at 0 V bias measured across any single diode is 4/3 the actual diode capacitance.

## Absolute Maximum Ratings

Characteristic	Value
Forward current—steady state	50 mA
Forward current—1 ms pulse	1 A
Dissipated power at 25 °C	250 mW
Operating temperature range	-40 °C to +150 °C
Storage temperature range	-65 °C to +200 °C
Junction temperature	150 °C

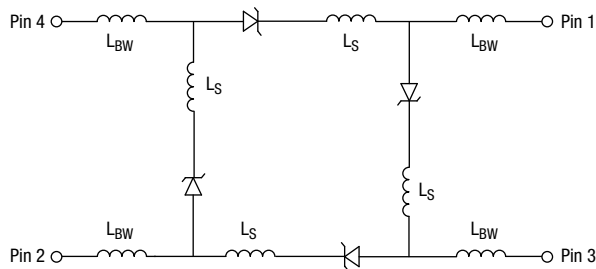
Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum Ratings. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

**CAUTION:** Although these devices are designed to be robust, ESD (Electrostatic Discharge) can cause permanent damage. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.

## SPICE Model Parameters (Per Junction)

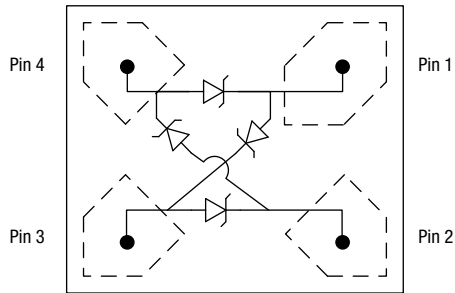
Parameter	Unit	DMF3926	DME3927	DMJ3928
$I_S$	A	2.5e-7	1.5e-9	9e-13
$R_S$	$\Omega$	9	10	9
N		1.05	1.05	1.05
TT	s	1e-11	1e-11	1e-11
$C_{J0}$	pF	0.375	0.375	0.375
M		0.3	0.36	0.41
$E_G$	eV	0.69	0.69	0.69
XTI		2	2	2
$F_C$		0.5	0.5	0.5
$B_V$	V	2.5	4	6
$I_{BV}$	A	1e-5	1e-6	1e-6
$V_J$	V	0.495	0.595	0.75

Equivalent Circuit



Parameter	Value	Unit
L <sub>BW</sub>	0.3	nH
L <sub>S</sub>	0.15	nH

Pin Out



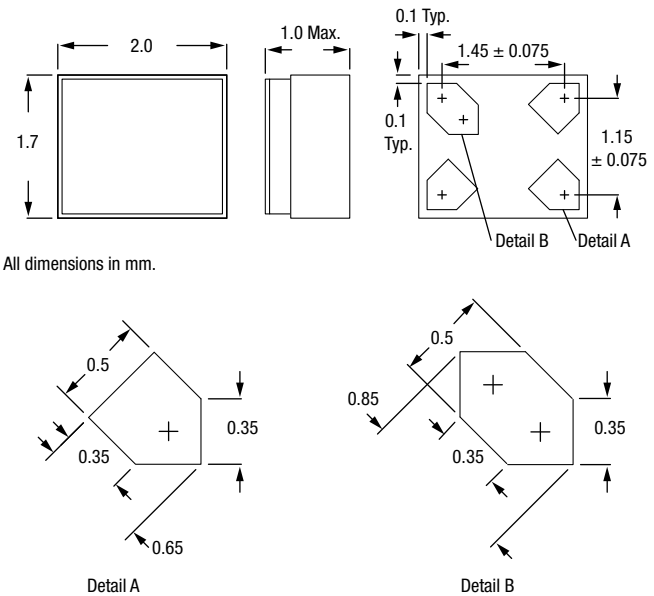
Recommended Solder Reflow Profiles

Refer to the *“Recommended Solder Reflow Profile”* Application Note.

Tape and Reel Information

Refer to the *“Discrete Devices and IC Switch/Attenuators Tape and Reel Package Orientation”* Application Note.

Outline Drawing



All dimensions in mm ± 0.075.



**DATA SHEET**

# DMF3929-117, DME3930-117, DMJ3931-117: Surface Mount Hermetic Silicon Schottky Bridge Quads

**Applications**

- Double-balanced mixers

**Features**

- Surface mount bridge quads
- Low, medium and high barrier heights
- Suitable for use up to 4 GHz
- Very low parasitic impedance
- Miniature hermetic ceramic package
- Lead (Pb)-free, RoHS-compliant, and Green™, MSL-1 @ 260 °C per JEDEC J-STD-020
- ESD Class 0, human body model

**Description**

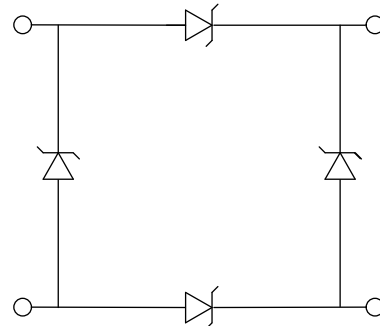
This family of bridge quads comprised of silicon Schottky diodes is offered with one of three barrier heights. DMF3929-117 contains low barrier diodes, DME3930-117 contains medium barrier diodes and DMJ3931-117 contains high barrier diodes. Each of these parts is packaged in a surface mount, 1.7 x 2 x 1.1 mm hermetic ceramic package.

These bridge quads are fabricated as single dice that contain all four junctions and the connection, thereby inherently matching electrical characteristics including capacitance, forward voltage and series resistance.

This package meets fine and gross leak test requirements per MIL-STD-750. It is lead(Pb)-free and fully complies with current RoHS requirements. It also meets Skyworks definition of Green: it contains no halogens or antimony (Sb).

SPICE parameters are provided.

These ring quads can operate over the temperature range of -40 °C to 85 °C.


**NEW**


Skyworks Green™ products are RoHS (Restriction of Hazardous Substances)-compliant, conform to the EIA/EICTA/JEITA Joint Industry Guide (JIG) Level A guidelines, are halogen free according to IEC-61249-2-21, and contain <1,000 ppm antimony trioxide in polymeric materials.

## Electrical Specifications

**T = 25 °C, per junction, unless otherwise noted**

Part Number	Breakdown Voltage @ $I_R = 10 \mu A$ (V) <sup>(1)</sup>	Total Capacitance @ $V_R = 0 V$ (pF) <sup>(2)</sup>	Forward Voltage $I_F = 1 mA$ (mV)		Forward Voltage Difference per Pair @ $I_F = 1 mA$ (mV)	Total Resistance @ $I_F = 10 mA$ ( $\Omega$ )
			Min.	Max.		
DMF3929-117	2	0.30–0.50	260	260	15	8
DME3930-117	3	0.30–0.50	300	400	15	8
DMJ3931-117	4	0.30–0.50	525	625	15	8

1. It is not possible to measure breakdown voltage on any junction in a ring quad.

2. In a ring quad the capacitance at 0 V bias measured across any single diode is 4/3 the actual diode capacitance.

## Absolute Maximum Ratings

Characteristic	Value
Forward current—steady state	50 mA
Forward current—1 ms pulse	1 A
Dissipated power at 25 °C	250 mW
Storage temperature range	-65 °C to +200 °C
Operating temperature range	-40 °C to +150 °C
Junction temperature	150 °C

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum Ratings. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

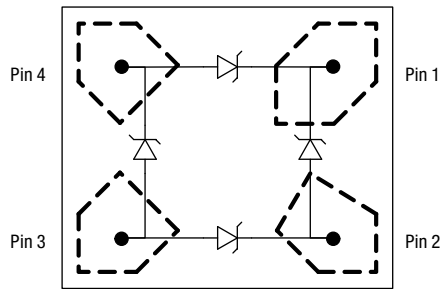
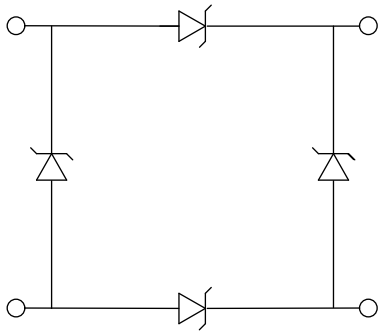
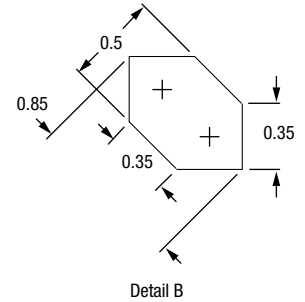
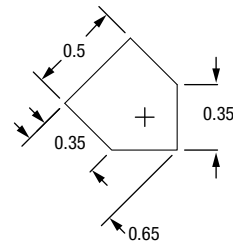
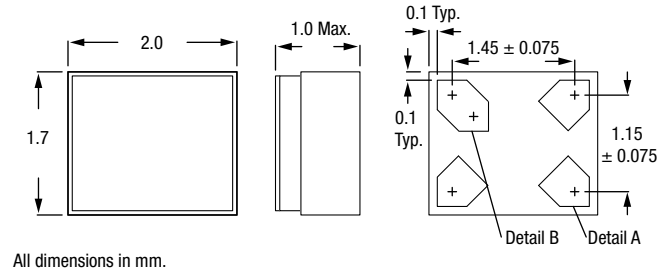
**CAUTION:** Although these devices are designed to be robust, ESD (Electrostatic Discharge) can cause permanent damage. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.

## SPICE Model Parameters (Per Junction)

Parameter	Unit	DMF3929	DME3930	DMJ3931
$I_S$	A	2.5e-07	1.3e-9	9e-13
$R_S$	$\Omega$	4	4	4
N		1.04	1.04	1.04
TT	s	1e-11	1e-11	1e-11
$C_{J0}$	pF	0.42	0.39	0.39
M		0.32	0.37	0.42
$E_G$	eV	0.69	0.69	0.69
XTI		2	2	2
$F_C$		0.5	0.5	0.5
$B_V$	V	2	3	4
$I_{BV}$	A	1e-5	1e-5	1e-5
$V_J$	V	0.495	0.595	0.80

## Tape and Reel Information

Refer to the “*Discrete Devices and IC Switch/Attenuators Tape and Reel Package Orientation*” Application Note.

**Pin Out (Top View)****Functional Diagram****Outline Drawing**

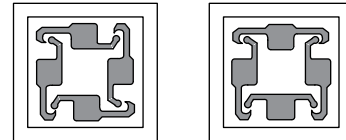
All dimensions in mm  $\pm 0.075$ .

DATA SHEET

# Silicon Beamless Schottky Diodes—Pairs and Quads

## Applications

- For microwave MIC assembly & automated high-volume manufacturing lines
- Mixers



## Features

- Mechanically rugged design
- Three barrier heights for optimized mixer performance
- Wide product range: series pair, ring, bridge, and 8-diode rings
- Use in ring or crossover designs in double balanced mixer designs
- Virtually any LO requirement can be met with choice of barrier height
- 100% DC tested on wafer
- Available in film frame or waffle pack
- Lead (Pb)-free, RoHS-compliant, and Green™

## Description

The Beamless Diode family is designed for a high degree of device reliability in both commercial and industrial uses. They are designed to offer the utmost in performance as well as achieving price sensitive cost targets for commercial systems.

**NEW** Skyworks Green™ products are RoHS (Restriction of Hazardous Substances)-compliant, conform to the EIA/EICTA/JEITA Joint Industry Guide (JIG) Level A guidelines, are halogen free according to IEC-61249-2-21, and contain <1,000 ppm antimony trioxide in polymeric materials.



## Electrical Specifications (Per Junction)

Part Number	Band	Barrier	$V_F$ $I_F = 1.0 \text{ mA (mV)}$		$\Delta V_F$ $I_F = 1.0 \text{ mA (mV)}$	$C_J^{(1,2)}$ $V_R = 0 \text{ V,}$ $f = 1 \text{ MHz (pF)}$		$R_S$ $I_F = 5 \text{ mA}$ $(\Omega)$	$V_B \text{ (V)}$ $@ 10 \mu\text{A}$	Outline Drawing Number
			Min.	Max.	Max.	Min.	Max.	Min.		
Ring Quad <sup>(3)</sup>										
DMF3926–000	S	Low	200	260	10	0.3	0.5	5	–	551–002
DME3927–000	S	Medium	300	400	10	0.3	0.5	5	–	551–002
DMJ3928–000	S	High	500	600	10	0.3	0.5	5	–	551–002
DMF3942–000	X	Low	250	310	10	0.15	0.3	8	–	551–002
DME3943–000	X	Medium	325	425	10	0.15	0.3	8	–	551–002
DMJ3944–000	X	High	550	650	10	0.15	0.3	8	–	551–002
Bridge Quad <sup>(3)</sup>										
DMF3929–000	S	Low	200	260	10	0.3	0.5	5	2	551–004
DME3930–000	S	Medium	300	400	10	0.3	0.5	5	3	551–004
DMJ3931–000	S	High	500	600	10	0.3	0.5	5	4	551–004
Series Pair <sup>(3)</sup>										
DMF3932–000	S	Low	200	260	10	0.3	0.5	5	2	551–012
DME3933–000	S	Medium	300	400	10	0.3	0.5	5	3	551–012
DMJ3934–000	S	High	500	600	10	0.3	0.5	5	4	551–012
Back-to-Back Ring Series Pair <sup>(3)</sup>										
DMF3935–000	S	Low	200	260	10	0.3	0.5	5	–	551–056
DME3936–000	S	Medium	300	400	10	0.3	0.5	5	–	551–056
DMJ3937–000	S	High	500	600	10	0.3	0.5	5	–	551–056
Octoquad Ring <sup>(4)</sup>										
DMF3938–000	S–X	Low	400	520	15	0.15	0.3	16	–	556–020
DME3939–000	S–X	Medium	600	800	15	0.15	0.3	16	–	556–020
DMJ3940–000	S–X	High	1000	1200	15	0.15	0.3	16	–	556–020
Back-to-Back Crossover Quad (To 6 GHz)										
DMF3945–000	S	Low	200	260	15	0.3	0.5	5	–	588-065
DME3946–000	S	Medium	300	400	15	0.3	0.5	5	–	588-065
DMJ3947–000	S	High	525	625	15	0.3	0.5	5	–	588-065

1.  $C_J$  represents total capacitance.2. Maximum  $C_J$  unbalance @ 0 V, 1 MHz = 0.025 pF.3. Matching criteria  $V_F$  @ 1 mA  $\leq$  15 mV available for matched sets.4. Matching criteria  $V_F$  @ 1 mA  $\leq$  20 mV available for matched sets.

## Spice Parameters (Per Junction)

Part Number Prefix	$I_S$ (A)	$R_S$ ( $\Omega$ )	N	$T_T$ (s)	$C_{J0}$ (pF)	M	$E_G$ (eV)	$V_J$ (V)	XTI	$F_C$	$B_V$ (V)	$I_{BV}$ (A)
DMF3920	2.5E-7	4	1.04	1.E-11	0.42	0.32	0.69	0.51	2	0.5	2	1E-5
DME3927	1.3E-9	4	1.04	1.E-11	0.39	0.34	0.69	0.65	2	0.5	3	1E-5
DMJ3928	9E-13	4	1.04	1.E-11	0.39	0.42	0.69	0.84	2	0.5	3	1E-5

## Absolute Maximum Ratings

Characteristic	Value
T <sub>STG</sub>	-65 °C to +175 °C
T <sub>OP</sub>	-65 °C to +150 °C
P <sub>DISS</sub> CW	75 mW/junction
I <sub>MAX</sub>	50 mA V
PIV	V <sub>B</sub> rating

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum Ratings. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

**CAUTION:** Although these devices are designed to be robust, ESD (Electrostatic Discharge) can cause permanent damage. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.

## Assembly and Handling Procedure

The process flow for assembly is:

1. Die attach using nonconductive epoxy
2. Wire bond
3. Encapsulation—nonconductive epoxy

## Die Attach Methods

All leadless chips are compatible with both eutectic and conductive epoxy die attach methods. Eutectic processes use Sn/Au or Sn/Pb solder. Nonconductive die attach is recommended.

## Packing Methods

1. Vacuum release gel pack.
2. Wafer on film frame (rejects are marked with ink).
  - Diced, ready for pick and place
  - Unsawn whole wafer, 7 mil thick, max.

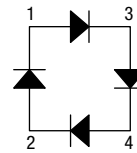
## Wire Bonding

Two methods can be used to connect wire, ribbon, or wire mesh to the chips:

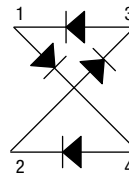
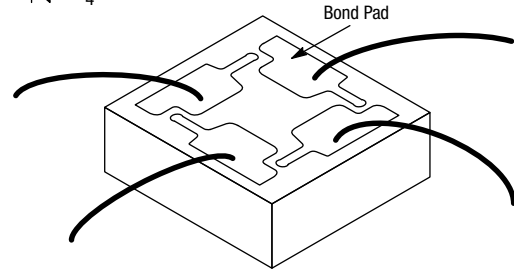
- Thermocompression
- Ballbonding

Skyworks recommends use of pure gold wire

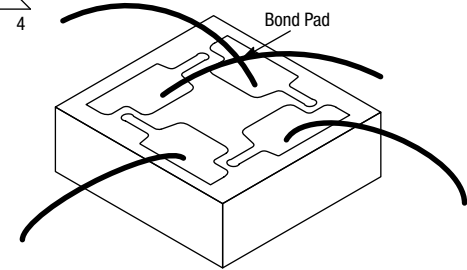
## Typical Bonding Configuration



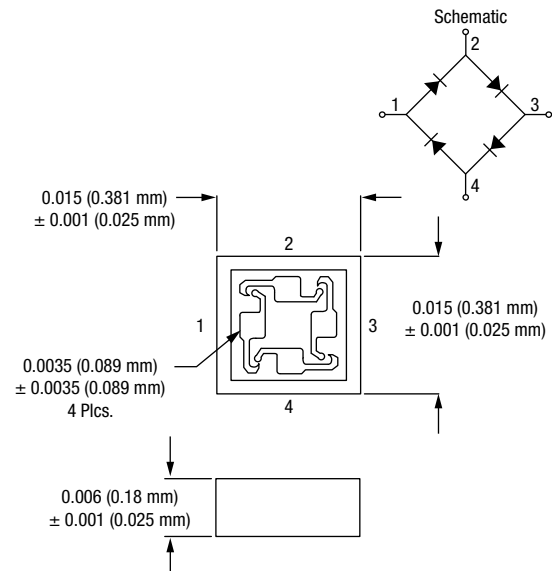
Ring Quad

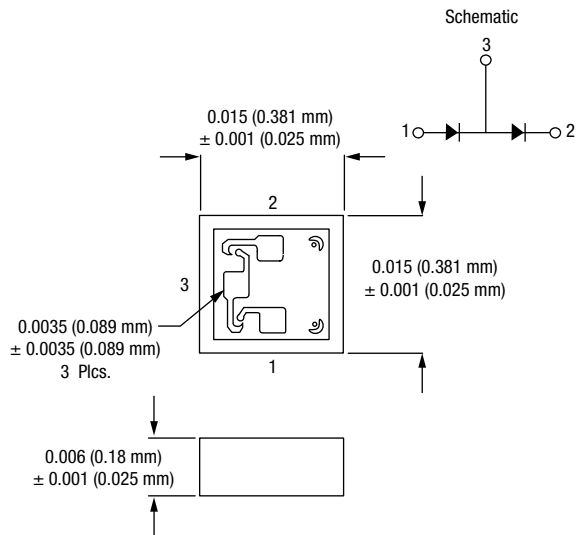
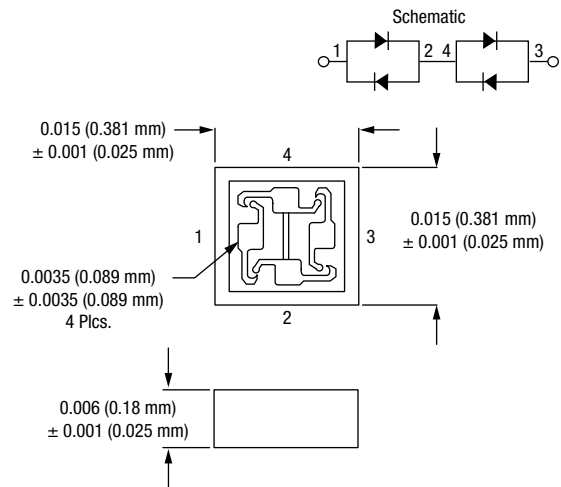
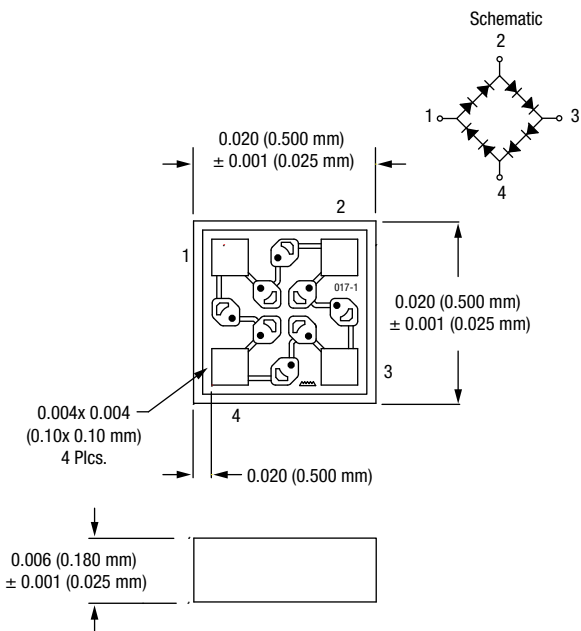
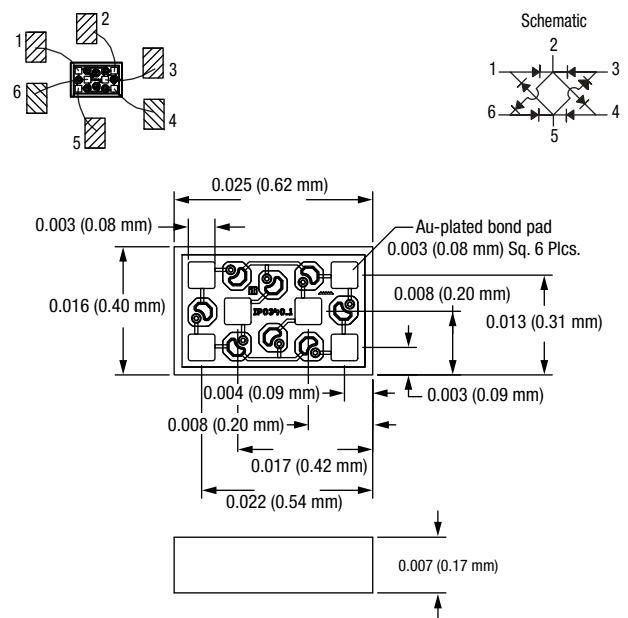


Crossover Quad



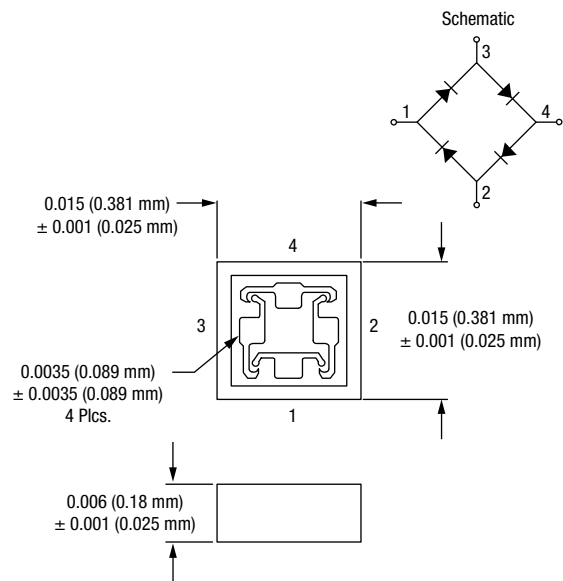
551-002



**551-012****551-056****556-020****588-065**

All dimensions in inches (mm) ± 0.001 (± 0.025)

551-004





## DATA SHEET

# Schottky Diode Quad Mixer Chips Supplied on Film Frame

## Applications

- Double-balanced mixers

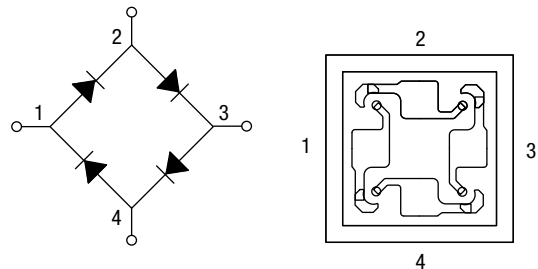
## Features

- Three barrier heights available
- Schottky diodes supplied 100% tested, sawn, mounted on film frame
- Low cost
- Lead (Pb)-free, RoHS-compliant, and Green™

## Description

The Skyworks SMS392x-099 family of Si Schottky diodes are configured as ring quads intended for use in double-balanced mixers. Each ring quad die is comprised of four Schottky junctions, connected anode to cathode. There are three barrier heights available: SMS3926 is composed of low-barrier diodes, which can be driven with low-power local oscillator signals; SMS3927 is composed of medium-barrier diodes, for applications in which moderate-power local oscillator signals are available; and SMS3928 is composed of high-barrier diodes for applications that require very low distortion performance and have higher local oscillator power available. These ring quads are 100% tested, sawn and supplied on film frame in wafer quantities.

**NEW** Skyworks Green™ products are RoHS (Restriction of Hazardous Substances)-compliant, conform to the EIA/EICTA/JEITA Joint Industry Guide (JIG) Level A guidelines, are halogen free according to IEC-61249-2-21, and contain <1,000 ppm antimony trioxide in polymeric materials.



## Absolute Maximum Ratings

Characteristic	Value
Forward current ( $I_F$ )	75 mA
Power dissipation @ 25 °C at the base of the chip	75 mW per junction
Storage temperature	-65 °C to +200 °C
Operating temperature	-65 °C to +150 °C
ESD human body model	Class 0

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum Ratings. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

**CAUTION:** Although these devices are designed to be robust, ESD (Electrostatic Discharge) can cause permanent damage. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.

Electrical Specifications at 25 °C

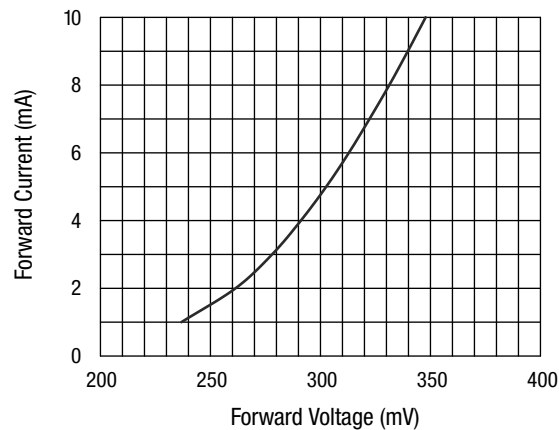
Part Number	Min. $V_B^{(1)}$ $I_R = 10 \mu A$ (V)	$C_J V_R = 0 V$ $F = 1 MHz$ (pF)	$V_F @ I_F = 1 mA$ (mV)	Max. Delta $V_F @ 1 mA$ (mV)	Max. $R_T$ $I_F = 10 mA$ ( $\Omega$ )
SMS3926-099	2	0.3–0.5 pF	200–260	10	8
SMS3927-099	3	0.3–0.5 pF	300–400	10	8
SMS3928-099	4	0.3–0.5 pF	500–600	10	8

The above Schottky diode chips are processed on 100 mm silicon wafers, 100% DC tested, sawn and shipped on 6" film frame hoops. Electrical rejects are identified with black ink.  
 $R_T$  is the slope resistance.  
All parameters are based upon a single junction.  
1. Guaranteed by design. It is not possible to measure breakdown voltage in a ring quad.

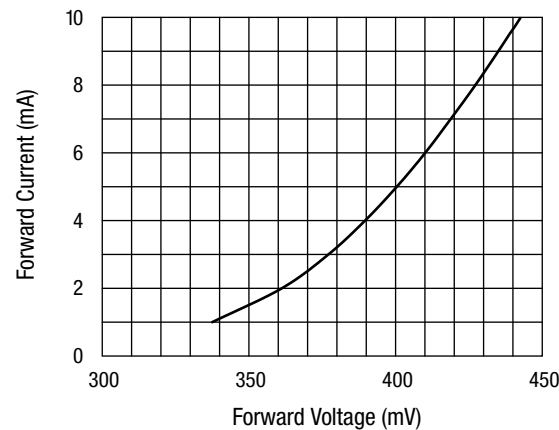
Chip Dimensions

Part Number	Quantity of Good Diodes Per Wafer		Bonding Pad Nominal (In.)	Chip Size Nominal (In.)	Chip Height Nominal (In.)
	Min.	Nom.			
SMS3926-099	20,000	23,000	0.0035 ± 0.0005	0.0150 ± 0.001	0.006 ± 0.001
SMS3927-099	20,000	23,000	0.0035 ± 0.0005	0.0150 ± 0.001	0.006 ± 0.001
SMS3928-099	20,000	23,000	0.0035 ± 0.0005	0.0150 ± 0.001	0.006 ± 0.001

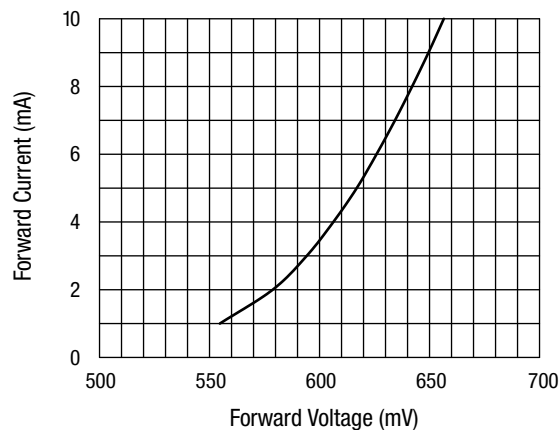
Typical Performance Data at 25 °C



SMS3926 DC Characteristic



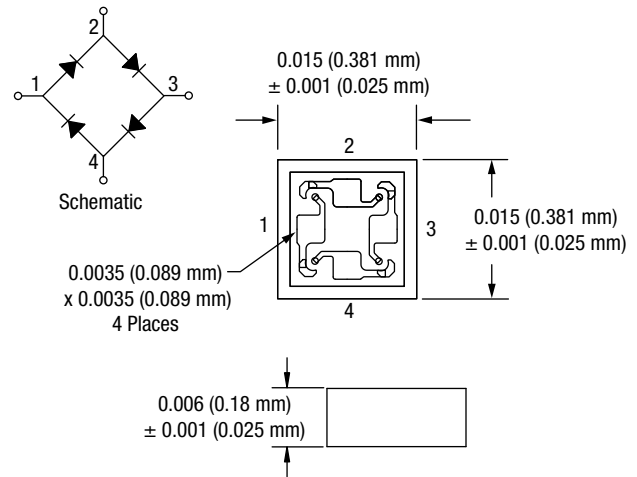
SMS3927 DC Characteristic



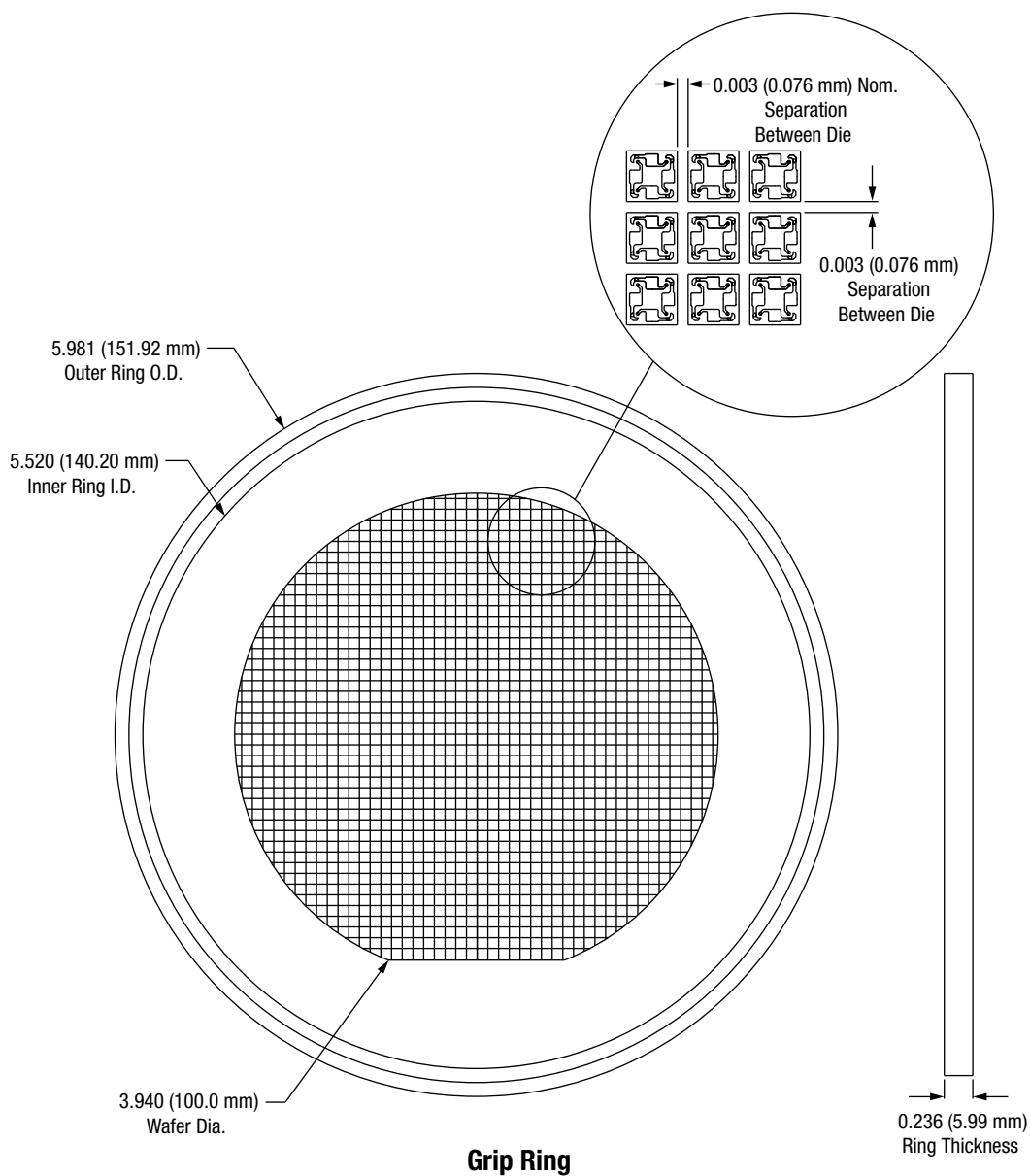
SMS3928 DC Characteristic

**SPICE Model Parameters (Per Junction)**

Parameter	Units	SMS3926	SMS3927	SMS3928
$I_S$	A	2.5E-07	1.3E-09	9.0E-13
$R_S$	$\Omega$	4.00	4.00	4.00
N	-	1.04	1.04	1.04
TT	s	1E-11	1E-11	1E-11
$C_{JO}$	pF	0.42	0.39	0.39
M	-	0.32	0.37	0.42
$E_G$	eV	0.69	0.69	0.69
XTI	-	2.00	2.00	2.00
$F_C$	-	0.50	0.50	0.50
$B_V$	V	2.00	3.00	4.00
$I_{BV}$	A	1.0E-05	1.0E-05	1.0E-05
$V_J$	V	0.495	0.595	0.800

**Outline Drawing**

## Wafer On Film



### Wafer Film Frame Description

- Wafer on nitto tape
- Color: light blue
- Thickness: 2.2–3.0 mils
- Tensile strength: 6.6 (lbs. in width)
- Ring material: plastic

**DATA SHEET**

# GaAs Flip Chip Schottky Diodes— Singles and Antiparallel Pairs

**Applications**

- Mixers
- Detectors

**Features**

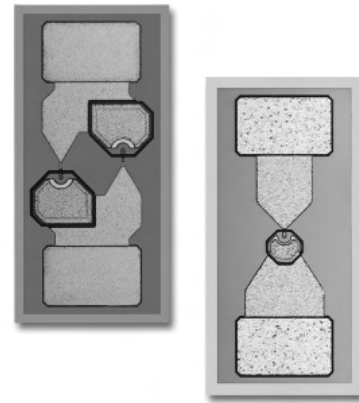
- Designed for high-volume designs
- High frequency (20–100 GHz)
- Exceeds environmental requirements for MIC & hybrid applications
- Designed for low junction capacitance and low series resistance
- Applications include PCN mixers and circuits, as well as low power, fast switching
- Low parasitic flip chip configuration
- Lead (Pb)-free, RoHS-compliant, and Green™

**Description**

This series of Skyworks GaAs Schottky barrier flip chip diodes produces excellent high-frequency performance up to millimeter wave range in a mechanically robust, small form factor. The series is comprised of a single junction device, DMK2790-000, and an antiparallel pair, DMK2308-000. These products offer very low series resistance and capacitance typically available only in beam-lead devices, but without the fragility of beam leads. The DMK2308-000 antiparallel pair is suited for use in subharmonically pumped mixers or in limiting circuits.

These diodes are designed to be mounted on hard or soft substrate printed circuit boards with conductive epoxy or solder.

Typical applications include mixers or detectors in point-to-point millimeterwave radios, collision avoidance automotive radars, adaptive cruise control radar systems, etc.



**NEW** Skyworks Green™ products are RoHS (Restriction of Hazardous Substances)-compliant, conform to the EIA/EICTA/JEITA Joint Industry Guide (JIG) Level A guidelines, are halogen free according to IEC-61249-2-21, and contain <1,000 ppm antimony trioxide in polymeric materials.

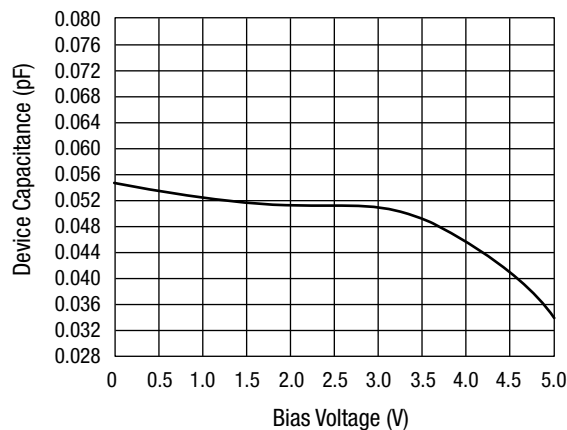
## Electrical Specifications at 25 °C (Per Junction)

Recommended Frequency (GHz)	$V_B^{(1)}$ @ 10 $\mu$ A (V)	$C_T^{(2)}$ 0 V, 1 MHz (pF)		$R_S$ @ 10 mA ( $\Omega$ )	$V_F$ @ 1 mA (mV)		Single	Antiparallel
		Min.	Max.		Min.	Max.		
20–100	3.0	0.04	0.07	7	650	750	DMK2790-000	DMK2308-000

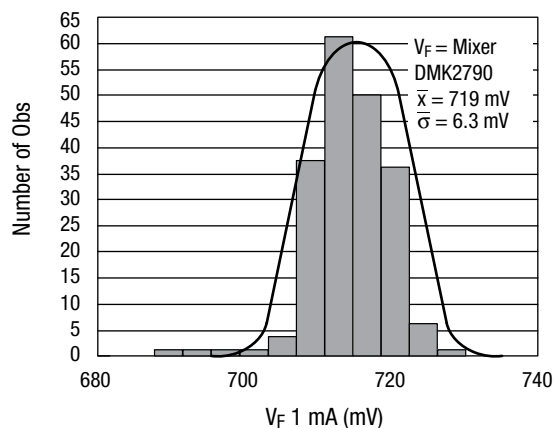
1.  $V_B$  cannot be measured nondestructively in antiparallel configuration.

2.  $C_T$  = junction capacitance plus 0.02 pF (overlay).

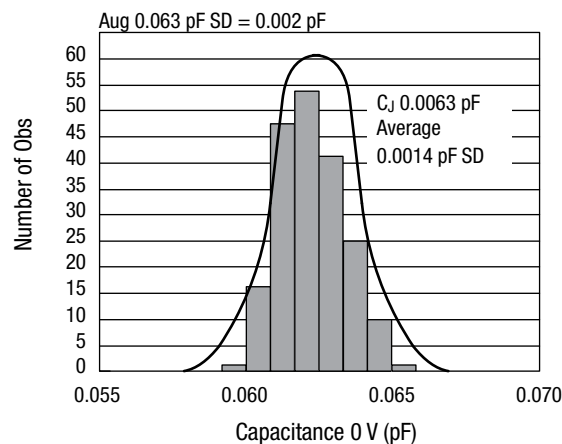
## Typical Parameter Distribution on Wafer



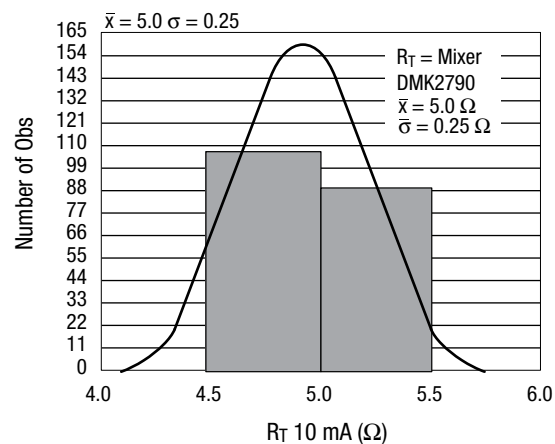
Capacitance/Voltage Variation



Histogram



Histogram



Histogram

## Spice Parameters (Per Junction)

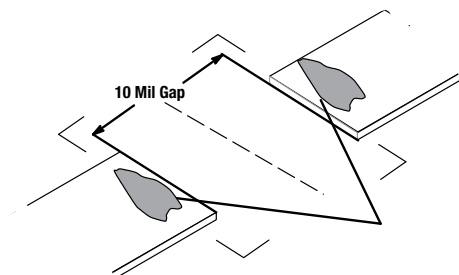
$I_S$ (Amp)	$R_S$ ( $\Omega$ )	$n$	$T_D$ (s)	$C_{j0}$ (pF)	$m$	$E_G$ (eV)	$V_J$ (V)	XTI	FC	$B_V$ (V)	$I_{BV}$ (A)
0.5 E-12	4	1.05	1E-11	0.05	0.26	1.43	0.82	2	0.5	4.0	1E-05

## The Epoxy Die Attach Process For GaAs Flip Chip Devices

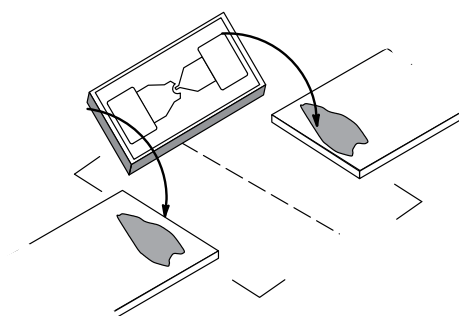
**Epoxy Material**—Microelectronic grade conductive epoxy. For attachment to soft boards, a stress absorbent conductive epoxy must be used to produce a consistent process and reliable bond.

**Cleanness**—Flexible or hard substrate must be clean and free of contaminants before epoxy die attachment takes place.

**Epoxy Dispensing**—Dispense epoxy dot size, approximately 0.008", and a bondlike thickness of approximately 0.001", between die and substrate.



**Die Attachment**—Flip device, aligning bond pads of device to dispensed dots, using even force of approximately 15–30 grams of bond force.



**Epoxy Curing**—Cure per manufacturer's recommendations.

**Attachment Quality**—The strength of the die attachment can be verified by stressing the attachment joint to failure, by performing die shear test on a sample base. The force of the shear test equipment on the die is increased until the component pops from the surface of the circuit, recording a gram force value at the time of fracture from substrate. This value for pass or fail criteria is based on the contact bond pad size of the die and compared against MIL requirements.

## Absolute Maximum Ratings

Characteristic	Value
Forward current	50 mA
Storage temperature ( $T_{ST}$ )	-65 °C to +150 °C
Operating temperature ( $T_{OP}$ )	-65 °C to +125 °C
Junction temperature ( $T_J$ )	175 °C
Electrostatic Discharge (ESD) Human Body Mode (HBM)	Class 0

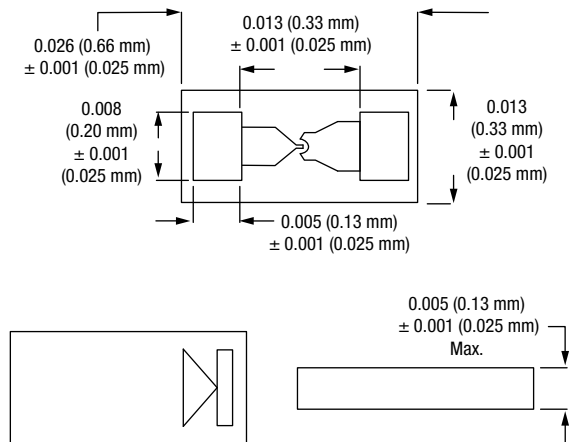
Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum Ratings. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

**CAUTION:** Although these devices are designed to be robust, ESD (Electrostatic Discharge) can cause permanent damage. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.

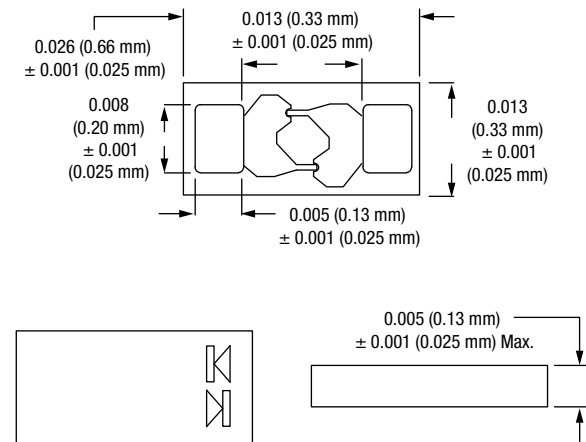
## Tape and Reel Information

Refer to the *"Discrete Devices and IC Switch/Attenuators Tape and Reel Package Orientation"* Application Note.

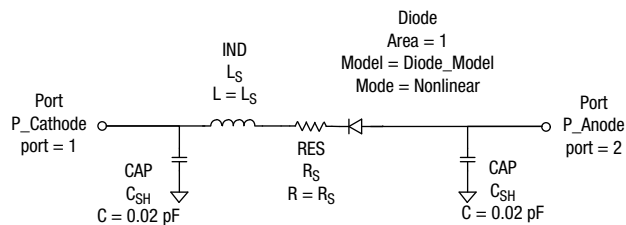
540-011



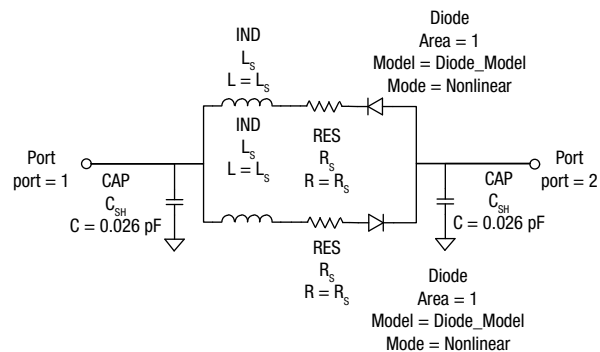
540-025



DMK2790 SPICE



DMK2308 SPICE







## PASSIVE ELEMENTS

Fixed Attenuator Pads .....	118
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Sampling Phase Detectors .....	123

**DATA SHEET**

# **ATN3580 Series: Fixed Attenuator Pads**

**Applications**

- Attenuators

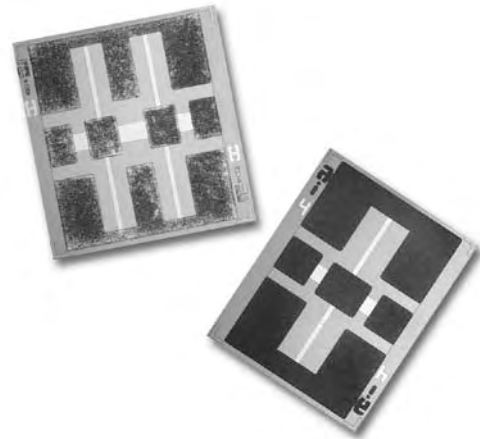
**Features**

- Specified flat response to 40 GHz
- Return loss > 16 dB to 40 GHz
- Available at 1–10, 12, 15, 20, 30 and 40 dB
- Power handling to 1 W CW
- Rugged thin-film silicon chips
- Lead (Pb)-free, RoHS-compliant, and Green™

**Description**

The ATN3580 series of attenuator chips incorporates thin-film resistors on high-resistivity silicon to achieve precision attenuation, tight flatness and excellent return loss to 40 GHz. The design uses a balanced TEE resistive structure to assure broad bandwidth performance. The thin-film technology offers improved power-handling capability in comparison to the traditional thick-film printed attenuator. All ATN3580 attenuator chips are specified for their attenuation at DC. A wafer probe sample test is performed to 40 GHz to assure the flatness specification.

**NEW** Skyworks Green™ products are RoHS (Restriction of Hazardous Substances)-compliant, conform to the EIA/EICTA/JEITA Joint Industry Guide (JIG) Level A guidelines, are halogen free according to IEC-61249-2-21, and contain <1,000 ppm antimony trioxide in polymeric materials.


**Absolute Maximum Ratings**

Characteristic	Value
Incident power @ 25 °C	1 W
Operating temperature	-55 °C to +150 °C
Storage temperature	-65 °C to +150 °C

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum Ratings. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

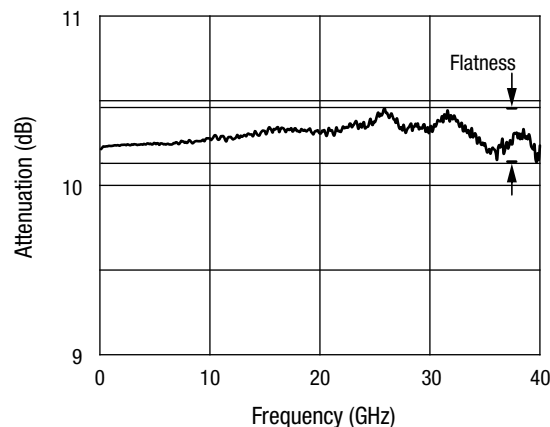
**CAUTION:** Although these devices are designed to be robust, ESD (Electrostatic Discharge) can cause permanent damage. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.

**Electrical Specifications at 25 °C**

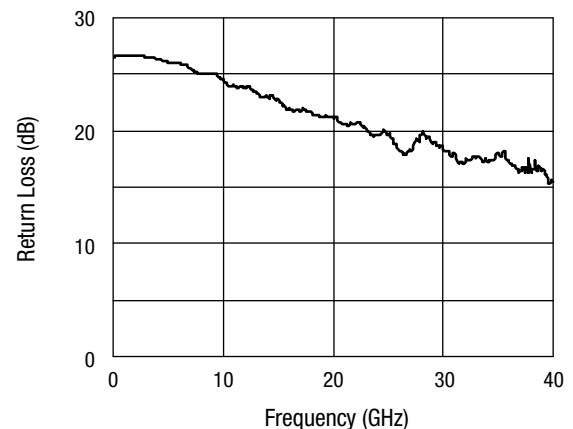
Nominal Attenuation (dB)	DC Tolerance (dB)	Attenuator Flatness			Outline Drawing	Part Number
		0.1–12 GHz (dB)	0.1–26.5 GHz (dB)	0.1–40 GHz (dB)		
1	±0.15	0.2	0.4	0.6	516-060	ATN3580-01
2	±0.15	0.2	0.4	0.6	516-060	ATN3580-02
3	±0.25	0.2	0.4	0.6	516-060	ATN3580-03
4	±0.25	0.2	0.4	0.6	516-060	ATN3580-04
5	±0.25	0.3	0.5	0.8	516-060	ATN3580-05
6	±0.25	0.3	0.5	0.8	518-060	ATN3580-06
7	±0.25	0.3	0.5	0.8	518-060	ATN3580-07
8	±0.35	0.3	0.5	0.8	518-060	ATN3580-08
9	±0.35	0.3	0.5	0.8	518-060	ATN3580-09
10	±0.35	0.4	0.6	1	518-060	ATN3580-10
12	±0.50	0.4	0.6	1	518-060	ATN3580-12
15	±0.50	0.4	0.6	1	518-060	ATN3580-15
20	±1.10	0.4	0.6	1	518-060	ATN3580-20
30	±1.60	0.6	1	2	518-060	ATN3580-30
40	±1.60	1	2	4	518-060	ATN3580-40

**Minimum Return Loss  $S_{11}$** 

	0.1–7 GHz (dB)	0.1–12 GHz (dB)	0.1–26.5 GHz (dB)	0.1–40 GHz (dB)
ATN3580 Series	25	23	18	15

**Typical Performance Data**

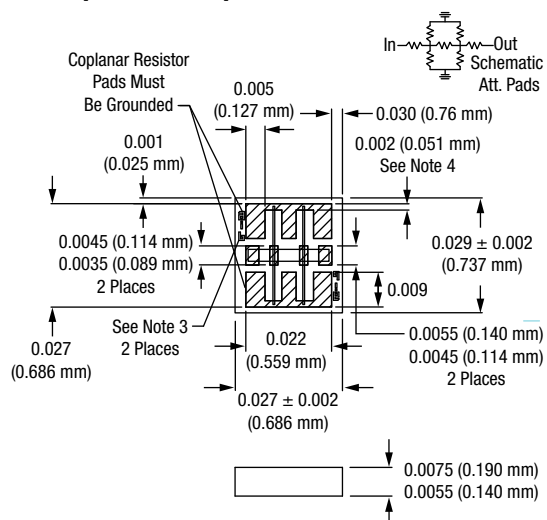
**Figure 1. ATN3580-10**  
Typical Attenuation vs. Frequency



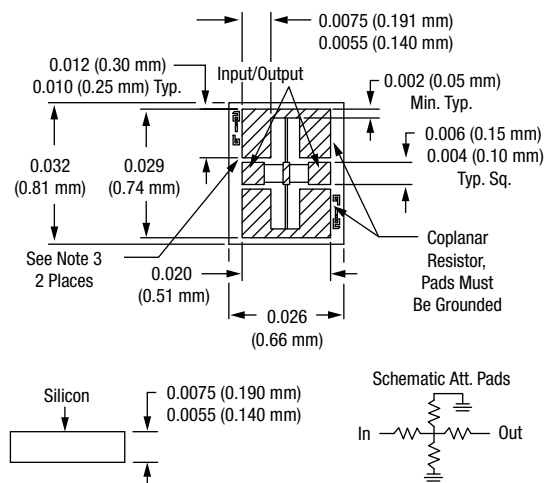
**Figure 2. ATN3580-10**  
Typical Input Return Loss vs. Frequency

## Outline Drawings

## 518-060 (ATN3580-04)



## 516-060 (ATN3580-04)





## DATA SHEET

# SC Series: MIS Chip Capacitors

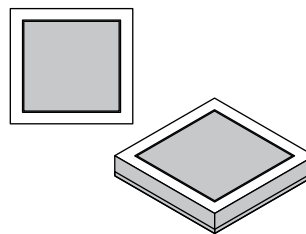
## Features

- Readily available from stock
- High reliability silicon oxide–nitride dielectric
- Low loss—typically 0.04 dB in a 50  $\Omega$  system
- Operation through 26 GHz
- Wide temperature operation
- Lead (Pb)-free, RoHS-compliant, and Green™

## Description

Skyworks MIS Chip Capacitors are available in a wide range of sizes and capacitance values. They are frequently used in applications requiring DC blocking, RF bypassing, or as a fixed capacitance tuning element in filters, oscillators, and matching networks. The devices have a dielectric composed of thermally grown silicon dioxide over which a layer of silicon nitride is deposited. This dielectric possesses a low temperature coefficient of capacitance and very high insulation resistance. The devices also exhibit excellent long-term stability making them suitable for high-reliability applications. The capacitors have a high dielectric breakdown which permits the use of thin dielectrics resulting in large capacitance per unit area. The temperature coefficient is less than 50 ppm/°C, and operation is suitable from -65 °C to 200 °C. Compared to ceramic capacitors, Skyworks MIS chip capacitors offer higher Q, and insertion loss of 0.04 dB, in a 50  $\Omega$  system. Insulation resistance is greater than 10<sup>5</sup> M  $\Omega$ . To accommodate high-volume automated assembly methods, wafers can be supplied on expanded film frame. To reduce cost, chips can be supplied packaged in vials with sample testing only. Packaging in waffle packs with 100% electrical test and visual inspection is available.

**NEW** Skyworks Green™ products are RoHS (Restriction of Hazardous Substances)-compliant, conform to the EIA/EICTA/JEITA Joint Industry Guide (JIG) Level A guidelines, are halogen free according to IEC-61249-2-21, and contain <1,000 ppm antimony trioxide in polymeric materials.



## Electrical Specifications

Capacitance range: 0.8 to 1000 pF

Temperature coefficient: 50 ppm/°C typical

Capacitance tolerance:  $\pm 20\%$

Operating temperature: -65 °C to +200 °C

Dielectric withstanding voltage: 100 V

Insulation resistance: 10<sup>5</sup> megohms typical

Leakage current: typ. < 1 nA

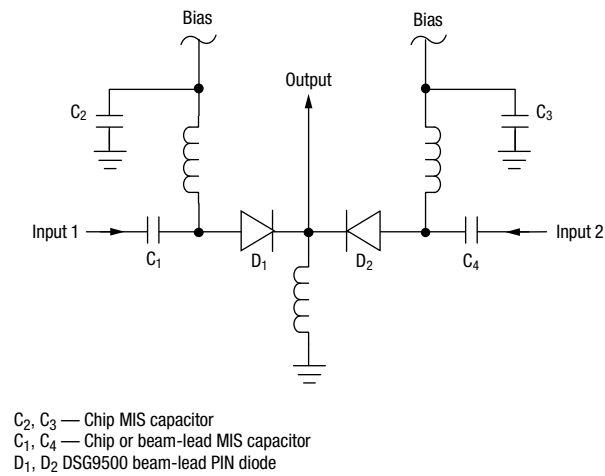
## Absolute Maximum Ratings

Characteristic	Value
Operating temperature range ( $T_{OP}$ )	-65 °C to +200 °C
Storage temperature range ( $T_{STG}$ )	-65 °C to +200 °C
Dielectric withstanding voltage	100 V

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum Ratings. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

**CAUTION:** Although these devices are designed to be robust, ESD (Electrostatic Discharge) can cause permanent damage. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.

Typical SPDT Switch



C<sub>2</sub>, C<sub>3</sub> — Chip MIS capacitor  
C<sub>1</sub>, C<sub>4</sub> — Chip or beam-lead MIS capacitor  
D<sub>1</sub>, D<sub>2</sub> DSG9500 beam-lead PIN diode

Example

Part Number Structure — SCXXXXYYZZ

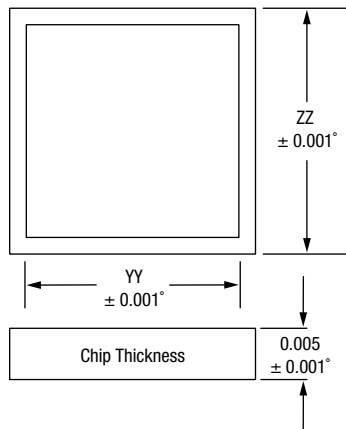
where:

SC = Silicon Capacitor

XXXX = Capacitance (pF)

YY = Square Contact Size (mils)

ZZ = Square Chip Size (mils)



Performance Data

Tests on typical MIS capacitors at L and S band show insertion loss to be 1/2 to 1/3 that of equivalent ceramic-type capacitors, without any of the associated resonance problems. Power tests indicate that the only limitation is the actual breakdown voltage of the device (see data section). A typical insertion loss versus frequency graph is shown in Figure 1. This data is taken from an actual test circuit with series mounted beam-lead or chip capacitors on a 50 Ω microstrip transmission line. The apparent higher loss at lower frequencies on the lower capacitance units is strictly due to the capacitive reactance of the capacitor.

Electrical Specifications

Part Number	Capacitance (±20%) pF	Chip Dimensions (±1 mil)
SC00080912	0.8	9 mil pad/12 mil chip
SC00120912	1.2	9 mil pad/12 mil chip
SC00180912	1.8	9 mil pad/12 mil chip
SC00260912	2.6	9 mil pad/12 mil chip
SC00380912	3.8	9 mil pad/12 mil chip
SC00560912	5.6	9 mil pad/12 mil chip
SC00680912	6.8	9 mil pad/12 mil chip
SC00820710	8.2	7 mil pad/10 mil chip
SC00821518	8.2	15 mil pad/18 mil chip
SC01000710	10	7 mil pad/10 mil chip
SC01000912	10	9 mil pad/12 mil chip
SC01001518	10	15 mil pad/18 mil chip
SC01501518	15	15 mil pad/18 mil chip
SC02201518	22	15 mil pad/18 mil chip
SC03301518	33	15 mil pad/18 mil chip
SC04701518	47	15 mil pad/18 mil chip
SC06801518	68	15 mil pad/18 mil chip
SC10002430	100	24 mil pad/30 mil chip
SC33303440	333	34 mil pad/40 mil chip
SC50004450	500	44 mil pad/50 mil chip
SC99906068	1000	60 mil pad/68 mil chip

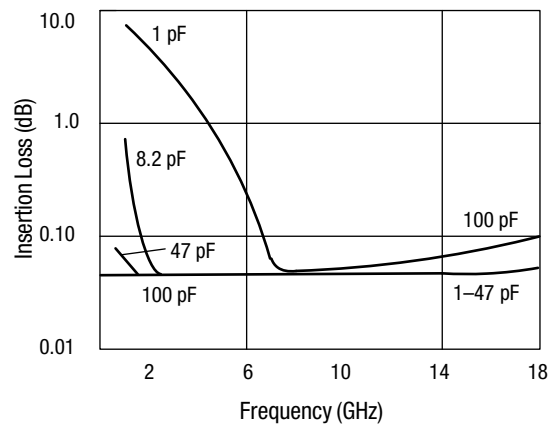


Figure 1. Typical Insertion Loss vs. Frequency (50 Ω System)



## DATA SHEET

# SPD1101-111, SPD1102-111, SPD1103-111: Sampling Phase Detectors

## Applications

- Phase-locked loops

## Features

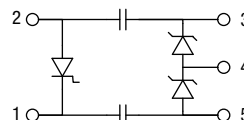
- For phase-locked VCOs to 22 GHz
- Reference frequencies below 50 MHz
- New surface mount package design
- Small footprint (90 x 110 mils)
- Automated chip on board construction
- Available on tape and reel
- Lead (Pb)-free, RoHS-compliant, and Green™

## Description

Each member of Skyworks family of sampling phase detectors, SPD1101-111, SPD1102-111 and SPD1103-111, consists of a step recovery diode (SRD), a series pair of Schottky mixer diodes and a pair of coupling capacitors. These chip on board components are manufactured using automated pick-and-place techniques to provide uniformly performing, surface mountable, small footprint devices with excellent high-frequency performance.

Sampling phase detectors are typically used in systems which lock the output signal of a high-frequency voltage controlled oscillator (VCO) to a lower frequency, stable reference oscillator output signal. The reference oscillator signal is applied to the SRD, which produces outputs at the harmonics of the reference oscillator frequency. This comb of harmonics is coupled to the Schottky series pair, which comprises a singly balanced mixer, via the on-board coupling capacitors. The high-frequency signal from the VCO is applied to the center node of the Schottky diode pair. The high-frequency VCO signal is mixed with the harmonics of the low-frequency, stable reference oscillator signal in the Schottky diode pair. The desired output signal, which is typically the difference frequency signal that is produced by the VCO signal and the harmonic of the reference oscillator signal nearest to it in frequency, is present at pin 4 of the sampling phase detector, along with the other mixer products produced by the other harmonics of the reference oscillator signal and the VCO signal, all of which are higher in frequency than the desired output signal. The desired output signal is selected by an external low pass filter, and can be utilized to lock the frequency and the phase of the VCO signal to the stable reference oscillator signal.

## Schematic Diagram



## Absolute Maximum Ratings

Characteristic	Value
Incident power	27 dBm
Operating temperature	-65 °C to +150 °C
Storage temperature	-65 °C to +175 °C
ESD human body model	Class 1B

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum Ratings. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

**CAUTION:** Although these devices are designed to be robust, ESD (Electrostatic Discharge) can cause permanent damage. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.

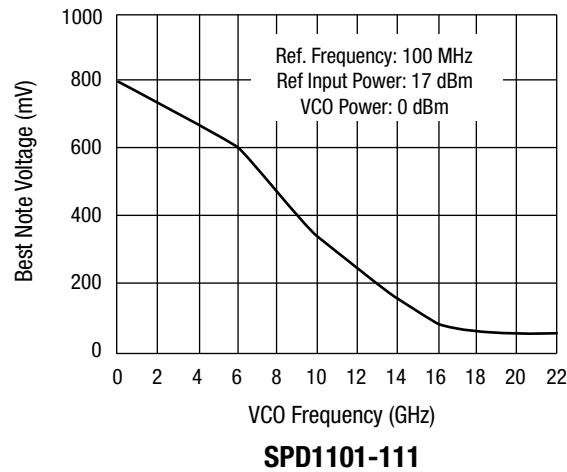
**NEW** Skyworks Green™ products are RoHS (Restriction of Hazardous Substances)-compliant, conform to the EIA/EICTA/JEITA Joint Industry Guide (JIG) Level A guidelines, are halogen free according to IEC-61249-2-21, and contain <1,000 ppm antimony trioxide in polymeric materials.



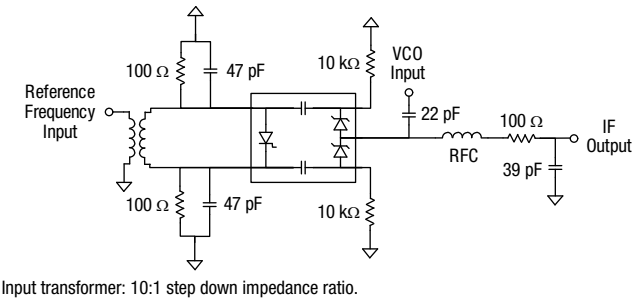
Electrical Characteristics at 25 °C

Part Number	Microwave Signal Drive Level (dBm)	Schottky Diode				Capacitor	Step Recovery Diode		
		Barrier	V <sub>F</sub> @ 1 mA (mV)	C <sub>J</sub> @ 0 V (pF)	R <sub>T</sub> @ 5 mA (Ω)	C <sub>C</sub> (pF)	C <sub>J</sub> @ 6 V (pF)	T <sub>L</sub> (ns)	TT (ps)
		Typ.		Max.	Max.	Typ.	Max.	Typ.	Typ.
SPD1101-111	-3 to 0	Low	270–350	0.1	24	0.5	0.25	10	70
SPD1102-111	0 to 3	Medium	370–550	0.1	24	0.5	0.25	10	70
SPD1103-111	0 to 13	High	600–700	0.1	24	0.5	0.25	10	70

Typical Performance



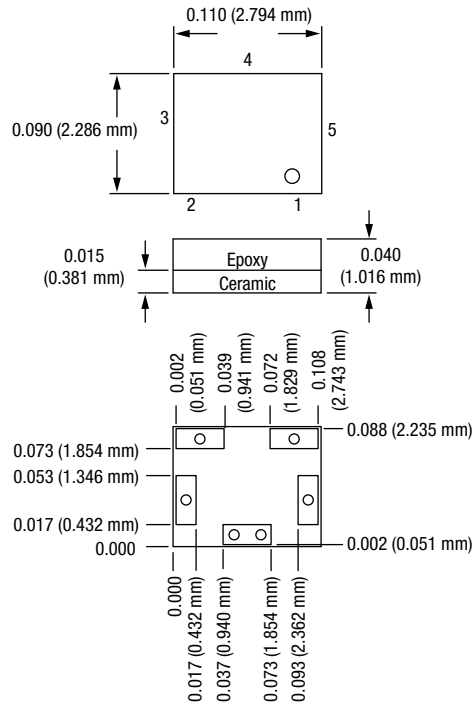
Suggested Circuit



Input transformer: 10:1 step down impedance ratio.

**Recommended Solder Reflow Profiles**  
Refer to the *“Recommended Solder Reflow Profile”* Application Note.

-111 Package Outline



Tape and Reel Information

Refer to the *“Discrete Devices and IC Switch/Attenuators Tape and Reel Package Orientation”* Application Note.





## SWITCHES

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## PRELIMINARY DATA SHEET

# AS179-000: GaAs SPDT Switch 300 kHz–3 GHz Medium Power

## Applications

- General-purpose medium-power switch in telecommunication applications
- Transceiver transmit-receive switch in 802.11b/g WLAN, etc., systems

## Features

- Broadband: 300 kHz–3 GHz
- Low insertion loss: 0.3 dB @ 900 MHz
- High isolation: 25 dB @ 900 MHz
- $P_{1\text{ dB}}$ : 30 dBm @ 3 V control voltage
- IP3: 43 dBm @ 3 V control voltage
- Low DC power consumption
- 100% RF tested in die form
- Lead (Pb)-free, RoHS-compliant, and Green™
- ESD Class 1A

## Description

The AS179-000 is a monolithic SPDT switch, fabricated using Skyworks proprietary GaAs PHEMTs as the switching elements. This wideband switch operates with RF signals from 300 kHz–3 GHz. The RF signal paths within the AS179-000 are bilateral. The  $J_1$  and  $J_2$  RF input/output terminals are reflective.

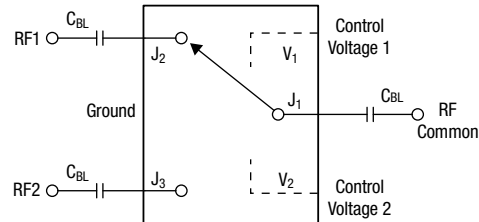
Switching is controlled via a pair of high impedance control voltage inputs. Depending upon the logic voltage level applied to the control voltage pins, the common RF pin ( $J_1$ ) is connected to one of two switched RF pins ( $J_2$  or  $J_3$ ) via a low insertion loss path, while the path between the RF common and the other RF pin is in its high-isolation state.

DC power consumption is very low, 100  $\mu$ A nominal with control voltage of 3 V. The switch can operate over the temperature range of -40° C to +85° C.

**NEW** Skyworks Green™ products are RoHS (Restriction of Hazardous Substances)-compliant, conform to the EIA/EICTA/JEITA Joint Industry Guide (JIG) Level A guidelines, are halogen free according to IEC-61249-2-21, and contain <1,000 ppm antimony trioxide in polymeric materials.

**Preliminary Data Sheet:** Based on engineering results. Sampling quantities available. Pin out and package have been determined.

## Functional Block Diagram



DC blocks required on all RF ports for positive control voltage operation.

## Absolute Maximum Ratings

Characteristic	Value
RF input power ( $V_{CTL}$ 0 V/7 V)	6 W, $f > 500$ MHz 2 W, $100 > f > 500$ MHz 315 mW, $f = 300$ kHz <sup>(1)</sup>
Control voltage range	-0.2 V $V_C$ +8 V
Operating temperature range	-40 °C to +85 °C
Storage temperature range	-40 °C to +150 °C

1. Derate linearly for 300 kHz <  $f$  < 100 MHz.

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum specifications. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

**CAUTION:** Although this device is designed to be as robust as possible, ESD (Electrostatic Discharge) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.

## Electrical Specifications at 25 °C

$V_{CTL} = 0 \text{ V/3 V}$ ,  $T = 25 \text{ °C}$ ,  $P_{INPUT} = 0 \text{ dBm}$ ,  $Z_0 = 50 \text{ } \Omega$ , unless otherwise noted

Parameter	Frequency	Min.	Typ.	Max.	Unit
Insertion loss	300 kHz–1 GHz		0.30	0.4	dB
	1–2 GHz		0.30	0.4	dB
	2–3 GHz		0.35	0.5	dB
Isolation	300 kHz–1 GHz	22	25		dB
	1–2 GHz	20	22		dB
	2–3 GHz	20	22		dB
VSWR <sup>(1)</sup>	300 kHz–3 GHz		1.1:1	1.3:1	

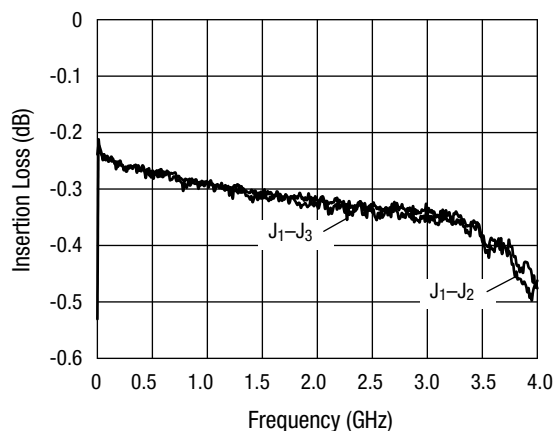
1. Insertion loss state.

## Operating Characteristics at 25 °C

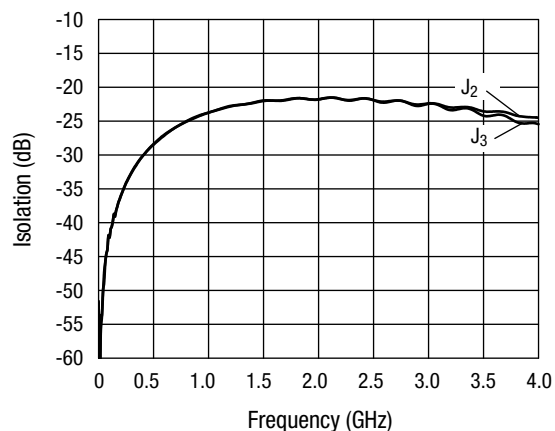
$V_{CTL} = 0 \text{ V/3 V}$ ,  $T = 25 \text{ °C}$ ,  $P_{INPUT} = 0 \text{ dBm}$ ,  $Z_0 = 50 \text{ } \Omega$ , unless otherwise noted

Parameter	Condition	Frequency	Min.	Typ.	Max.	Unit
Switching characteristics						
Rise, fall	10/90% or 90/10% RF			10		ns
On, off	50% CTL to 90/10% RF			20		ns
Video feedthru	$T_{RISE} = 1 \text{ ns}$ , $BW = 500 \text{ MHz}$			25		mV
Input power for 1 dB compression ( $IP_{1 \text{ dB}}$ )	$V_{CTL} = 0/3 \text{ V}$	0.5–3 GHz		30		dBm
	$V_{CTL} = 0/5 \text{ V}$	0.5–3 GHz		34		dBm
Input Intermodulation intercept point (IIP3)	For two-tone input power 5 dBm					
	$V_{CTL} = 0/3 \text{ V}$	0.5–3 GHz		43		dBm
	$V_{CTL} = 0/5 \text{ V}$	0.5–3 GHz		50		dBm
Thermal resistance				15		°C/W
Control voltage	$V_{HIGH}$		3		5	V
	$V_{LOW}$		0		0.2	V
Control port current	$V_{CTL} = 5 \text{ V}$				100	μA
	$V_{CTL} = 0 \text{ V}$				20	μA

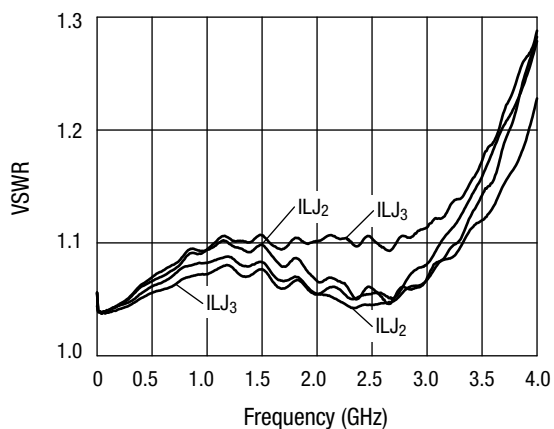
## Typical Performance Data



Insertion Loss vs. Frequency

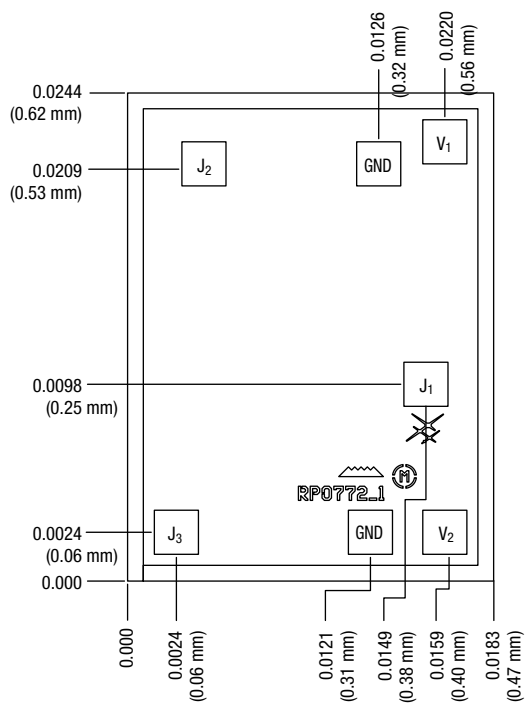


Isolation vs. Frequency



VSWR vs. Frequency

## Die Outline



Bond-pad dimensions: 0.0022 (0.06 mm) square.  
 Bond-pad metallization: Gold.  
 Backside metallization: None.  
 Die thickness  $0.008 \pm 0.001$  (0.203  $\pm$  0.025).  
 Dimensions in inches (mm).

## Port Descriptions

Parameter	Description
$J_1$	<b>RF Common</b> — RF input/output port that is connected via low impedance path to either RF1 or RF2, depending upon the voltage applied to control voltage pin. External DC block required for positive control voltages.
$J_2, J_3$	<b>RF Input/Output</b> — RF input/output port that is connected via low impedance path to either RF common ( $J_1$ ) or to ground, depending upon the voltage levels applied to control voltage pins. External DC block required for positive control voltages.
$V_1, V_2$	<b>Control Voltage Inputs</b> — Combination of voltage logic levels applied to these pins determines the state of the RF paths between $J_1$ and $J_2/J_3$ .
GND	<b>Ground</b> — Should be down-bonded to circuit ground

## Truth Table

$V_{CTL1}$	$V_{CTL2}$	$J_1-J_2$	$J_1-J_3$
$V_{HIGH}$	0	Isolation	Insertion loss
0	$V_{HIGH}$	Insertion loss	Isolation
0	0	Not allowed	Not allowed
$V_{HIGH}$	$V_{HIGH}$	Not allowed	Not allowed

## Theory of Operation

The AS179-000 Single Pole Double Throw (SPDT) switch comprises two RF signal paths, one of which connects the RF common pin ( $J_1$ ) to RF1 ( $J_2$ ) and the other connects RF common to RF2 ( $J_3$ ). Depending upon the logic voltage levels applied to the control voltage pins ( $V_1$  and  $V_2$ ), one of these paths is in its minimum insertion loss state while the other is in its high-isolation state. When these logic levels are toggled, the state of each of the paths toggles accordingly.

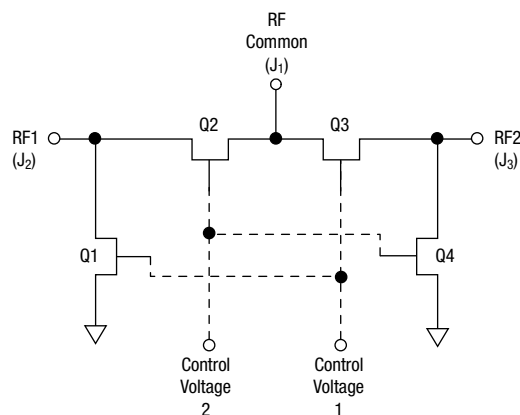
Starting at the RF common pin, each signal path is comprised of a depletion mode PHEMT, Q2 or Q3, in series with the signal path, followed by another depletion mode PHEMT, Q1 or Q4, in shunt with the signal path. A HI logic level applied to the control voltage pin  $V_1$  and a low logic level applied to the control voltage pin  $V_2$  forces the path between RF common and RF1 into its high-isolation state and the other path, from RF common to RF2, into its low insertion loss state.

The shunt PHEMT to common, Q1 or Q4, is biased to produce minimum impedance when the signal path of which it is part is placed into its isolation state. Consequently, the magnitude of the reflection coefficient looking into this pin is close to 1, that is, the VSWR looking into that port approaches infinity.

The AS179-000 can operate with control voltage from 3 V up to 5 V.

The logic threshold voltage for the control voltage pin is one half of the minimum high control voltage. The impedance looking into each of the control voltage pins is several tens of kilohms. For positive control voltage, DC blocks are required on each RF port.

## Simplified Block Diagram

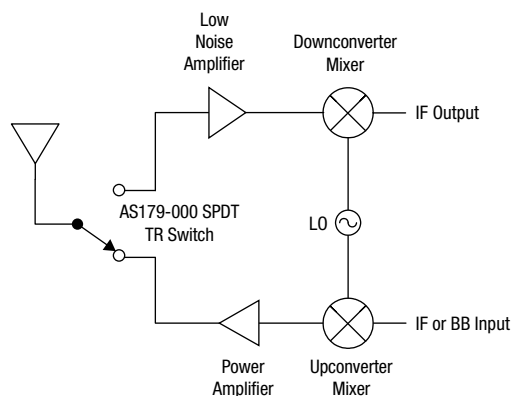


## Applications

The AS179-000 SPDT switch can be used in a number of ways: it can be used to select one of two loads; it can also be used to alternately connect an antenna to a radio transmitter and receiver, etc.

## Transmit-Receive Switch

A SPDT switch can be used as a transmit-receive (TR) switch, to alternately connect a transmitter and a receiver to a single antenna in a single duplex system.



**DATA SHEET**

# **AS192-000: PHEMT GaAs IC High-Power SP4T Switch 0.1–2.5 GHz**

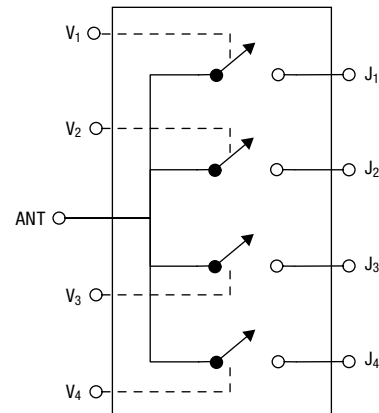
**Features**

- 4 symmetric RF paths
- Positive voltage control
- High IP3
- Excellent harmonic performance
- Handles GSM power levels
- Available in 100% RF tested chip form
- Available lead (Pb)-free, RoHS-compliant, and Green™

**Description**

The AS192-000 is a reflective SP4T switch. It is an ideal switch for higher power applications. It can be used for GSM dual-band handset applications where low loss, low current and small size are critical parameters.

**NEW** Skyworks Green™ products are RoHS (Restriction of Hazardous Substances)-compliant, conform to the EIA/EICTA/JEITA Joint Industry Guide (JIG) Level A guidelines, are halogen free according to IEC-61249-2-21, and contain <1,000 ppm antimony trioxide in polymeric materials.

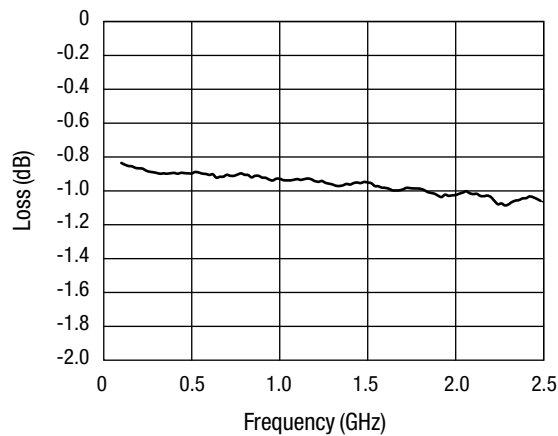
**Simplified Schematic**

**Electrical Specifications at 25 °C (0, +4.5 V)**

Parameter		Frequency	Min.	Typ.	Max.	Unit
Insertion loss	Ant-J <sub>1</sub> , J <sub>2</sub> , J <sub>3</sub> , J <sub>4</sub>	0.1–0.5 GHz		0.90	1.1	dB
		0.5–1.0 GHz		0.95	1.1	dB
		1.0–2.0 GHz		1.00	1.2	dB
		2.0–2.5 GHz		1.10	1.3	dB
Isolation	Ant-J <sub>1</sub> , J <sub>2</sub> , J <sub>3</sub> , J <sub>4</sub>	0.1–0.5 GHz	30	34		dB
		0.5–1.0 GHz	25	29		dB
		1.0–2.0 GHz	19	23		dB
		2.0–2.5 GHz	18	21		dB
VSWR		0.1–1.0 GHz		1.3:1		
		1.0–2.5 GHz		1.4:1		

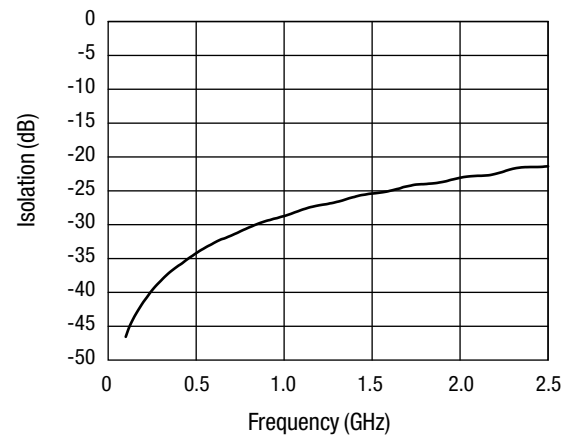
## Operating Characteristics at 25 °C (0, +4.5 V)

Parameter	Condition	Frequency	Min.	Typ.	Max.	Unit
Switching characteristics	Rise, fall (10/90% or 90/10% RF)			50		ns
	On, off (50% CTL to 90/10% RF)			100		ns
	Video feedthru			50		mV
IP3	13 dBm/tone			+55		dBm
2nd and 3rd harmonics	34 dBm input 900 MHz			-65		dBc
Control voltage	$V_{HIGH}V_{LOW}$		3		5	V
			0		0.2	V
Control port current	$V_{CTL} = 5\text{ V}$				200	$\mu\text{A}$
	$V_{CTL} = 3\text{ V}$				200	$\mu\text{A}$
	$V_{CTL} = 2.7\text{ V}$				200	$\mu\text{A}$
	$V_{CTL} = 0\text{ V}$				20	$\mu\text{A}$

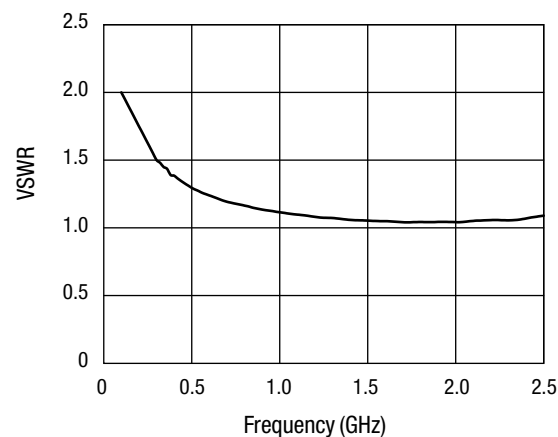
## Typical Performance Data



Typical Insertion Loss vs. Frequency



Typical Isolation vs. Frequency



Typical VSWR

## Absolute Maximum Ratings

Characteristic	Value
RF input power	4 W > 0.5 GHz 0/+6 V control
Control voltage	+6 V
Operating temperature	-40 °C to +85 °C
Storage temperature	-65 °C to +150 °C

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum specifications. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

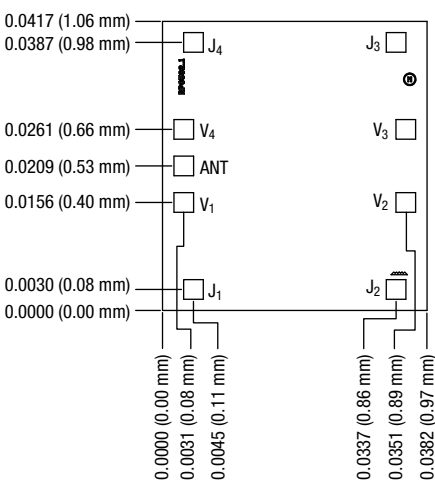
**CAUTION:** Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.

Truth Table

V <sub>1</sub>	V <sub>2</sub>	V <sub>3</sub>	V <sub>4</sub>	Ant-J <sub>1</sub>	Ant-J <sub>2</sub>	Ant-J <sub>3</sub>	Ant-J <sub>4</sub>
V <sub>HIGH</sub>	V <sub>LOW</sub>	V <sub>LOW</sub>	V <sub>LOW</sub>	Ins. loss	Isolation	Isolation	Isolation
V <sub>LOW</sub>	V <sub>HIGH</sub>	V <sub>LOW</sub>	V <sub>LOW</sub>	Isolation	Ins. loss	Isolation	Isolation
V <sub>LOW</sub>	V <sub>LOW</sub>	V <sub>HIGH</sub>	V <sub>LOW</sub>	Isolation	Isolation	Ins. loss	Isolation
V <sub>LOW</sub>	V <sub>LOW</sub>	V <sub>LOW</sub>	V <sub>HIGH</sub>	Isolation	Isolation	Isolation	Ins. loss

V<sub>LOW</sub> = 0.  
V<sub>HIGH</sub> = 4.5 to 5.0 V for RF power > 30 dBm.  
V<sub>HIGH</sub> = 3.0 to 5.0 V for RF power 20–30 dBm.  
V<sub>HIGH</sub> = 2.7 to 5.0 V for RF power < 20 dBm.  
All other conditions not recommended.

Outline and Pin Out Drawing



Chip thickness 0.008 ± 0.001 (0.203 ± 0.025).  
Bond pad dimensions: 0.028 (0.07 mm square).  
Bond pad metallization: gold.  
Backside metallization: none.  
Dimensions in inches (mm).

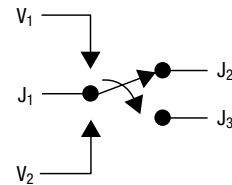


**DATA SHEET**

# **AS193-000: PHEMT GaAs IC High-Linearity 3 V Control SPDT 0.1–2.5 GHz Switch Chip**

**Features**

- 2.5 to 5 V linear operation
- Harmonics  $H_2, H_3 < -65$  dBc @  $P_{IN} = 34.5$  dBm
- Low insertion loss (0.35 dB @ 0.9 GHz)
- High isolation (24 dB @ 0.9 GHz)
- Lead (Pb)-free, RoHS-compliant, and Green™

**Functional Block Diagram**

**Description**

The AS193-000 is a PHEMT GaAs FET IC high-linearity SPDT switch. This switch has been designed for use where extremely high linearity, low control voltage, high isolation and low insertion loss are needed. Some standard implementations include antenna changeover, T/R and diversity switching over 3 W. The AS193-000 switch is ideal for GaAs based antenna switch front-end modules.

**NEW** Skyworks Green™ products are RoHS (Restriction of Hazardous Substances)-compliant, conform to the EIA/EICTA/JEITA Joint Industry Guide (JIG) Level A guidelines, are halogen free according to IEC-61249-2-21, and contain <1,000 ppm antimony trioxide in polymeric materials.

**Electrical Specifications at 25 °C (0, 3 V)**

Parameter <sup>(1)</sup>	Frequency	Min.	Typ.	Max.	Unit
Insertion loss <sup>(2)</sup>	0.1–0.5 GHz		0.30	0.4	dB
	0.5–1.0 GHz		0.35	0.5	dB
	1.0–2.0 GHz		0.45	0.6	dB
	2.0–2.5 GHz		0.55	0.7	dB
Isolation	0.1–0.5 GHz	28	30		dB
	0.5–1.0 GHz	22	24		dB
	1.0–2.0 GHz	17	19		dB
	2.0–2.5 GHz	15	17		dB
VSWR <sup>(3)</sup>	0.1–1.0 GHz		1.2:1		dB
	1.0–2.5 GHz		1.3:1		dB

1. All measurements made in a 50  $\Omega$  system, unless otherwise specified.

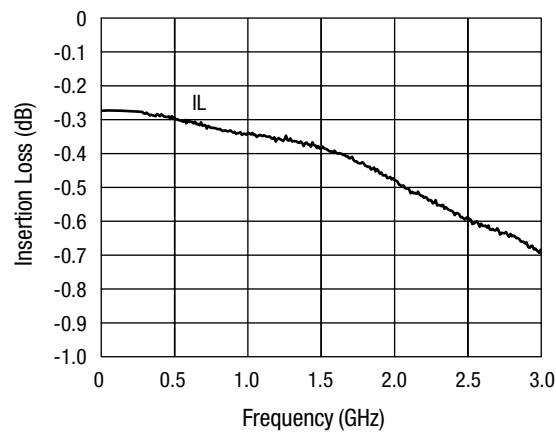
2. Insertion loss changes by 0.003 dB/°C.

3. Insertion loss state.

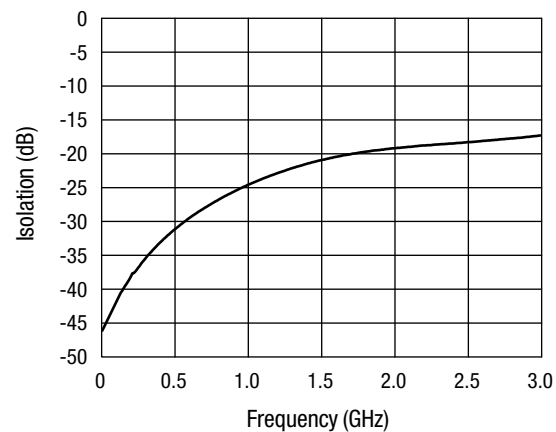
Operating Characteristics at 25 °C (0, 3 V)

Parameter	Condition	Frequency	Min.	Typ.	Max.	Unit
Switching characteristics						
Rise, fall	10/90% or 90/10% RF			60		ns
On, off	50% CTL to 90/10% RF			100		ns
Video feedthru	T <sub>RISE</sub> = 1 ns, BW = 500 MHz			50		mV
Input power for -0.1 dB compression	V <sub>CTL</sub> = 0/3 V	0.9 GHz		37		dBm
Harmonics H <sub>2</sub> , H <sub>3</sub>	P <sub>IN</sub> = 34.5 dBm	0.9 GHz		-65		dBc
Thermal resistance				25		°C/W
Control voltages	V <sub>LOW</sub> = 0 to 0.2 V @ 20 µA max. V <sub>HIGH</sub> = 2.5 V @ 50 µA max. to 5 V @ 100 µA max.					

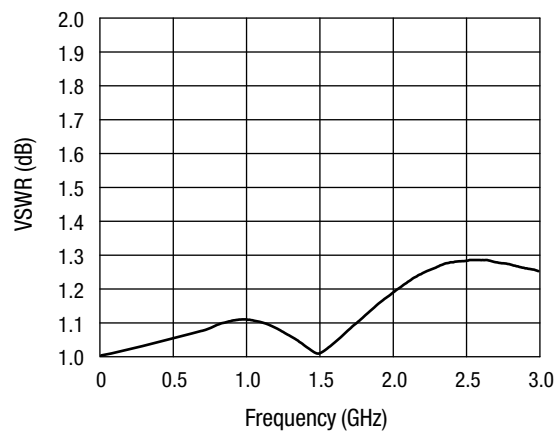
Typical Performance Data



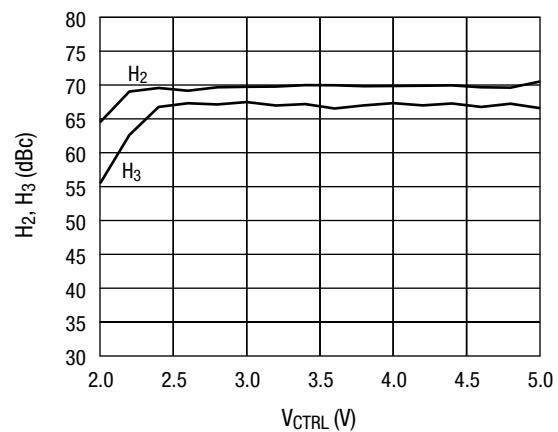
Insertion Loss vs. Frequency



Isolation vs. Frequency



VSWR vs. Frequency



Harmonics vs. Control Voltage  
P<sub>IN</sub> = 34.5 dBm, 900 MHz, GSM Pulsed

Note: Contact factory for S-parameter data.

Absolute Maximum Ratings

Characteristic	Value
RF input power	6 W max. > 900 MHz, 0/5 V control
Control voltage	-0.2 V, +8 V
Operating temperature	-40 °C to +85 °C
Storage temperature	-65 °C to +150 °C

Bond-pad metallization: gold.  
Backside metallization: none.  
See application note, Handling GaAs MMIC Die.  
Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum specifications. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

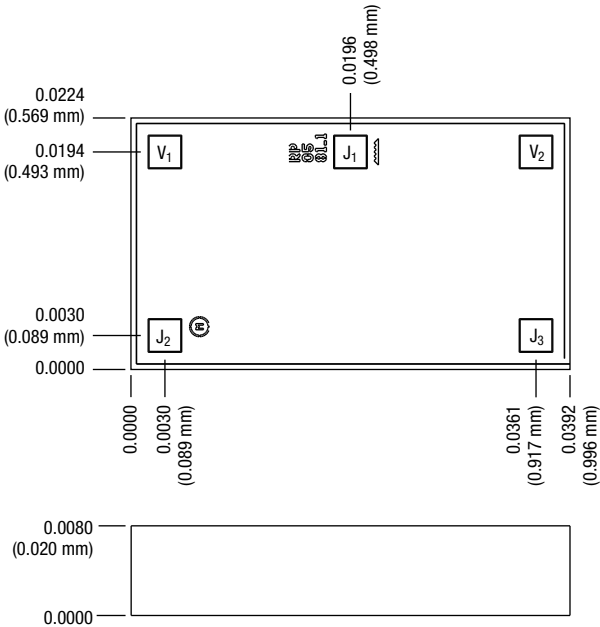
**CAUTION:** Although this device is designed to be as robust as possible, ESD (Electrostatic Discharge) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.

Truth Table

V <sub>1</sub>	V <sub>2</sub>	J <sub>1</sub> -J <sub>2</sub>	J <sub>1</sub> -J <sub>3</sub>
0	V <sub>HIGH</sub>	Isolation	Insertion loss
V <sub>HIGH</sub>	0	Insertion loss	Isolation

All other conditions not recommended.  
V<sub>HIGH</sub> = 2.5 to 5 V.

Outline Drawing



Chip thickness 0.008 ± 0.001 (0.203 ± 0.025).  
Bond pad dimensions: 0.028 (0.07 mm square).  
Bond pad metallization: gold.  
Backside metallization: none.  
Dimensions in inches (mm). Tolerance ± 0.001 (0.025 mm).

**DATA SHEET**

# AS218-000: PHEMT GaAs IC High-Power Transfer Switch

## 0.1–6 GHz

**Applications**

- WLAN 802.11a, b, g diversity

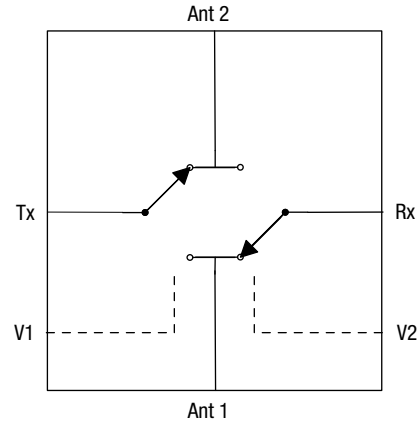
**Features**

- Operating frequency 0.1–6 GHz
- Positive low voltage control (0/3 V operation)
- Low insertion loss
- Lead (Pb)-free, RoHS-compliant, and Green™

**Description**

The AS218-000 is a broadband transfer switch designed to combine T/R and antenna diversity switching functions on a single IC. The device is designed to handle high power and maintain high linearity at low control voltages. This low-cost switch is ideal for Wi-Fi systems and is capable of covering both the 2.4 and 5 GHz bands.

**NEW** Skyworks Green™ products are RoHS (Restriction of Hazardous Substances)-compliant, conform to the EIA/EICTA/JEITA Joint Industry Guide (JIG) Level A guidelines, are halogen free according to IEC-61249-2-21, and contain <1,000 ppm antimony trioxide in polymeric materials.


**Pin Out (Top View)**


DC blocking caps required on RF lines for positive voltage operation.

**Electrical Specifications at 25 °C (0, 3 V)**

**T = 25 °C, Z<sub>0</sub> = 50 Ω, unless otherwise noted**

Parameter <sup>(1)</sup>	Condition	Frequency	Min.	Typ.	Max.	Unit
Insertion loss <sup>(2, 4)</sup>	Ant 1, Ant 2 to Tx, Rx	0.10–6.00 GHz		1.6	1.8	dB
		2.40–2.50 GHz		1.2	1.4	dB
		5.15–5.85 GHz		1.4	1.6	dB
Isolation	Ant 1, Ant 2 to Tx, Rx	0.10–6.00 GHz	17	19		dB
		2.40–2.50 GHz	32	37		dB
		5.15–5.85 GHz	17	19		dB
Return loss <sup>(3)</sup>	Ant 1, Ant 2 to Tx, Rx	0.10–6.00 GHz		10		dB
		2.40–2.50 GHz		15		dB
		5.15–5.85 GHz		20		dB

1. All measurements made in a 50 Ω system.

2. Insertion loss changes by 0.003 dB/°C.

3. Return loss for insertion loss state.

4. Tx and Rx paths can be used interchangeably.

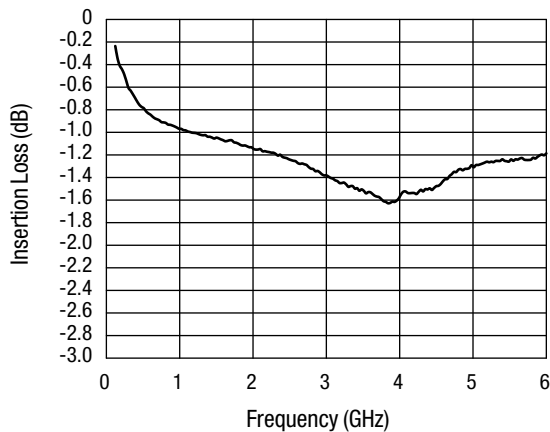
Operating Characteristics at 25 °C (0, 3 V)

T = 25 °C, Z<sub>0</sub> = 50 Ω, unless otherwise noted

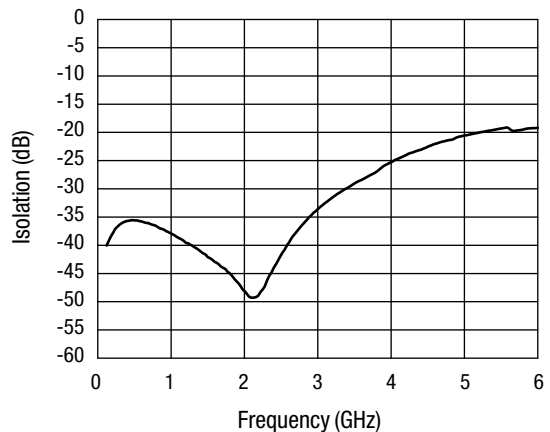
Parameter	Condition	Frequency	Min.	Typ.	Max.	Unit
2nd and 3rd harmonic	23 dBm input @ 0,3 V	2–6 GHz		-63		dBc
P <sub>1</sub> dB		2–6 GHz		33		dBm
IIP3	20 dBm per tone	2–3 GHz		54		dBm
	22 dBm per tone	5–6 GHz		47		dBm
Control voltages	V <sub>LOW</sub> = 0–0.2 V @ 20 μA max. V <sub>HIGH</sub> = 3–5 V @ 200 μA max.					

Typical Performance Data (0, 3 V)

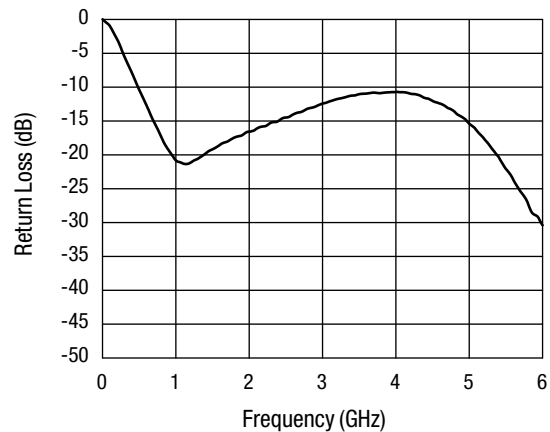
T = 25 °C, Z<sub>0</sub> = 50 Ω, unless otherwise noted



Insertion Loss vs. Frequency



Isolation vs. Frequency



Return Loss vs. Frequency

Absolute Maximum Ratings

Characteristic	Value
RF input power	35 dBm >500 MHz 0/7 V control
Control voltage	-0.2 V, +8 V
Operating temperature	-40 °C to +85 °C
Storage temperature	-65 °C to +150 °C

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum specifications. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

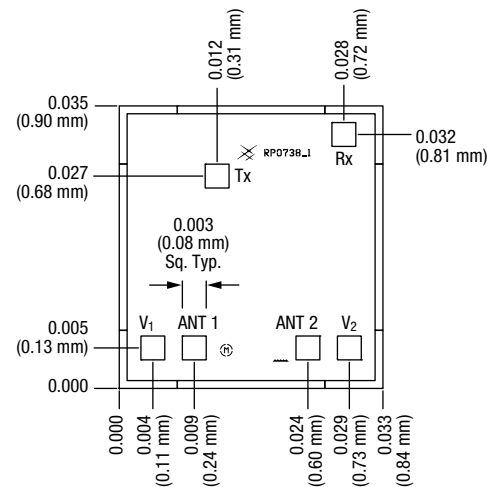
**CAUTION:** Although this device is designed to be as robust as possible, ESD (Electrostatic Discharge) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.

Truth Table

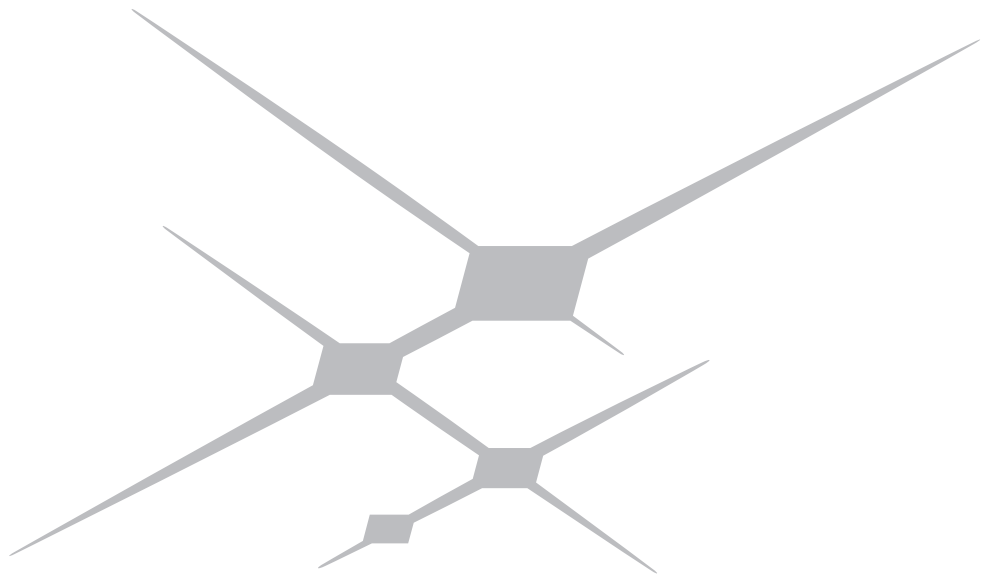
V <sub>1</sub>	V <sub>2</sub>	Insertion Loss Path
0	1	Ant 1 to Tx, Ant 2 to Rx
1	0	Ant 2 to Tx, Ant 1 to Rx

All other conditions not recommended.  
“1” = 3 to 5 V.  
“0” = 0 to 0.2 V.

Outline Drawing



Chip thickness 0.008 ± 0.001 (0.203 ± 0.025).  
Bond pad dimensions: 0.028 (0.07 mm square).  
Bond pad metallization: gold.  
Backside metallization: none.  
Dimensions in inches (mm).



**APPLICATION NOTES**

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## APPLICATION NOTE

# PIN Diode Basics

## Introduction

### Basic Theory—Variable Resistance

A PIN diode is essentially a variable resistor. To determine the value of this resistance, consider a volume comparable to a typical PIN diode chip, say 20 mil diameter and 2 mils thick. This chip has a DC resistance of about 0.75 MΩ. Note: 1 mil = 0.001 inches.

In real diodes there are impurities, typically boron, which cannot be segregated out of the crystal. Such impurities contribute carriers, holes or electrons, which are not very tightly bound to the lattice and therefore lower the resistivity of the silicon.

The resistivity of the I region and thus the diode resistance is determined by the number of free carriers within the I region. The resistivity of any semiconductor material is inversely proportional to the conductivity of the material.

Expressed mathematically the resistivity of the I region is

$$l/\rho_I = q (\mu_N N + \mu_P P)$$

where  $q$  is the electronic charge ( $q = 1.602 \times 10^{-19}$  coul.),  $\mu_N$  and  $\mu_P$  are the mobilities of electrons and holes respectively, and  $N$  and  $P$  are the numbers of electrons and holes, respectively.

Consider electrons and holes travelling in opposite directions within the I region under the impetus of an applied, positive electric field. The I region will fill up and an equilibrium condition will be reached. In non-equilibrium conditions excess minority carriers exist, and recombination between holes and electrons restore equilibrium. Recombination often occurs because of interactions between mobile charge carriers and imperfections in the semiconductor crystalline structure, either structural defects or dopant atoms. The rate of recombination of holes and electrons is proportional to the carrier concentrations and inversely proportional to a property of the semiconductor called the lifetime,  $T_L$ , of the minority carriers. [2]

In the case of applied forward bias, the equation governing mobile charges in the I region is

$$\frac{dQ_S}{dt} = I_F - \frac{Q_S}{T_L}$$

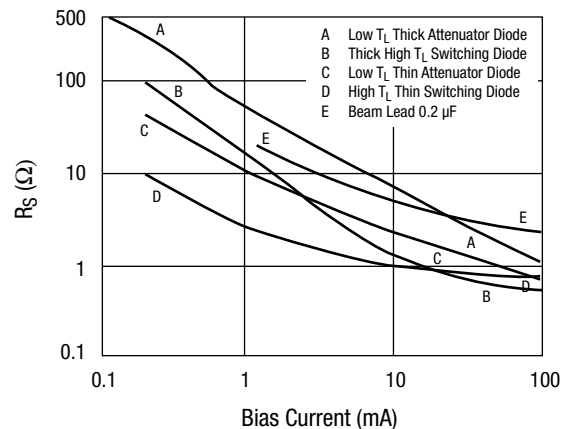
where  $Q_S$  is the stored charge and  $Q_S = q(N+P)$ .

Under steady conditions the mobile charge density in the I region is constant, i. e.,

$$\frac{dQ_S}{dt} = 0, \text{ so that}$$

$$I_F = Idc = \frac{Q_S}{T_L}$$

Typical data for  $R_S$  as a function of bias current are shown in Figure 1. A wide range of design choices is available, as the data indicate. Many combinations of  $W$  and  $T_L$  have been developed to satisfy the full range of applications.



**Figure 1. Typical Series Resistance as a Function of Bias (1 GHz)**

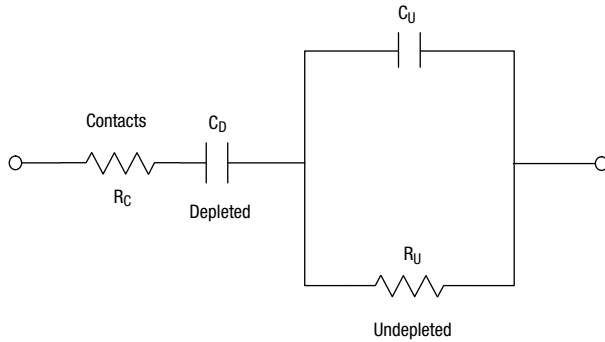
### Breakdown Voltage Capacitance, Q Factor

The previous section on  $R_S$  explained how a PIN can become a low resistance, or a “short.” This section will describe the other state—a high impedance, or an open.



$V_B$  is usually specified at a reverse current of 10 microamps.

In simplest form the capacitance of a PIN is determined by the area and width of the I region and the dielectric constant of silicon. This minimum capacitance is obtained by the application of a reverse bias in excess of  $V_{PT}$ , the voltage at which the depletion region occupies the entire I layer.



**Figure 2. Equivalent Circuit of I Region Before Punch-Through**

Consider the undepleted region: this is a lossy dielectric consisting of a volume (area  $A$ , length  $W$ ) of silicon of relative permittivity 12 and resistivity  $\rho$ . The capacitance is

$$\frac{12\epsilon_0 A}{W}, \text{ and the admittance is } \frac{24\pi 12\epsilon_0 A}{W}$$

The resistance is proportional to  $W/A$  and the conductance to  $A/L$ . At voltages below  $V_{PT}$ ,  $C_J$  will increase and approach  $\infty$  capacitance at a forward bias of 0.7 V in silicon and 0.9 V in GaAs.

Skyworks measures junction capacitance at 1 MHz; this is a measure of the depletion zone capacitance.

For I region thickness of  $W$  and a depletion width  $X_d$ , the undepleted region is  $(W - X_d)$ .

The capacitance of the depleted zone is, proportionally,

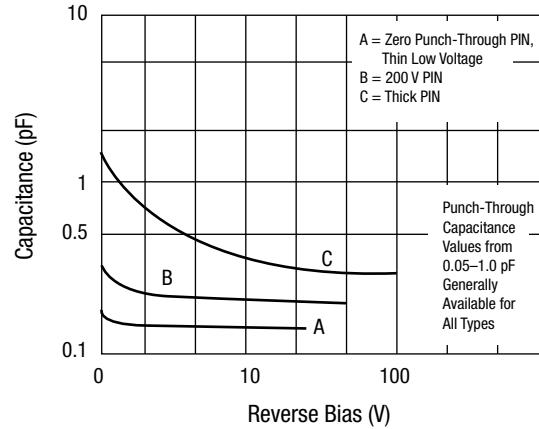
$$\frac{1}{X_d}, \text{ of the undepleted, } \frac{1}{W - X_d}$$

The 1 MHz capacitance decreases with bias until “punch-through” where  $X_d = W$ . At microwave frequencies well above the crossover, the junction looks like two capacitors in series.

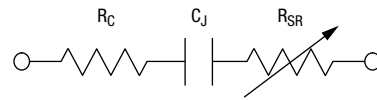
$$C_T = \frac{C_d C_U}{C_d + C_U}, \text{ which is proportional to } 1/W$$

i. e., the microwave capacitance tends to be constant, independent of  $X_d$  and bias voltage.

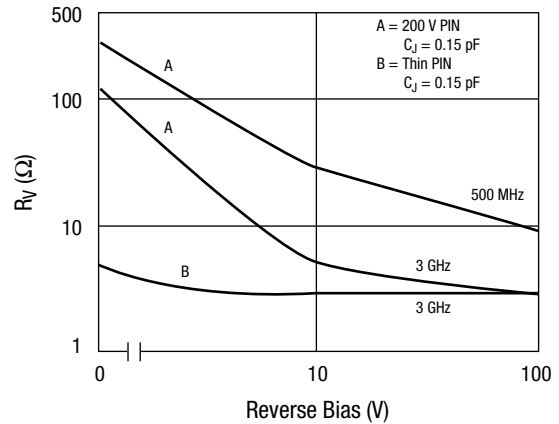
However, since the undepleted zone is lossy, an increase in reverse bias to the punch-through voltage reduces the RF power loss.



**Figure 3. Typical Capacitance**

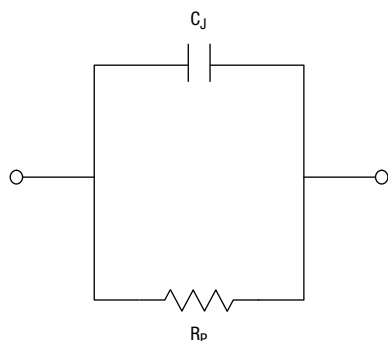


**Figure 4. Simplified Equivalent Circuit, Series**

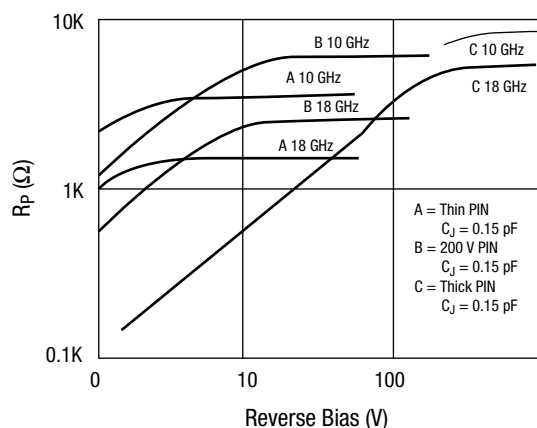


**Figure 5. Reverse Series Resistance**

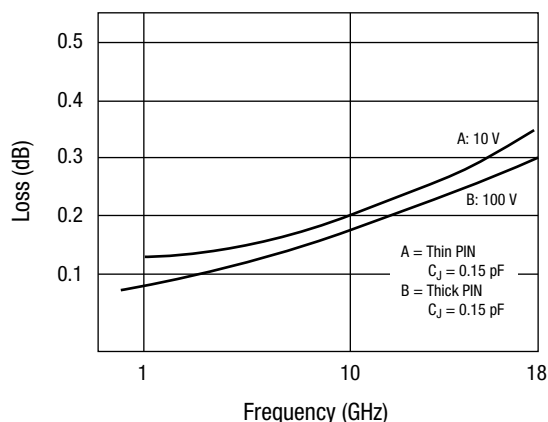
A good way to understand the effects of series resistance is to observe the insertion loss of a PIN chip series mounted in a 50  $\Omega$  line.



**Figure 6. Simplified Equivalent Circuit, Shunt**



### Figure 7. Reverse Shunt Resistance



### Figure 8. Insertion Loss vs. Frequency

An accepted way to include reverse loss in the figure of merit of a PIN is to write the switching cutoff frequency

$$F_{CS} = \frac{1}{2\pi C_T \sqrt{R_S R_V}}$$

where  $R_S$  and  $R_V$  are measured under the expected forward and reverse bias conditions at the frequency of interest.

The punch-through voltage is a function of the resistivity and thickness of the I region. It is advisable to measure loss as a function of bias voltage and RF voltage to determine if the correct diode has been selected for your application.

## Switching Considerations

Consider a PIN diode and a typical drive circuit. When the system calls for a change in state, the logic command is applied to the driver. There is delay time in the driver, in the passive components as well as in the transistors, before the voltage at Point A begins to change. There is a further delay before that voltage has stabilized. Most diode switching measurements are measured with the time reference being the 50% point of the (Point A) command waveform.

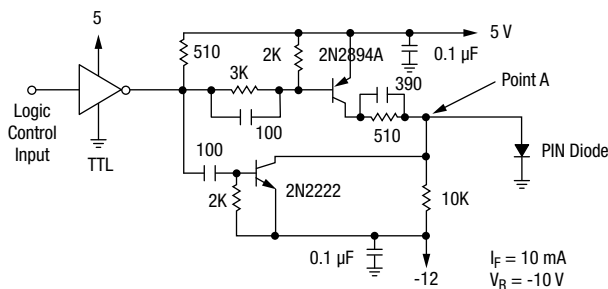
The diode begins to respond immediately, but there is a delay before the RF impedance begins to change. It is the change in impedance that causes the RF output to switch.

The driver waveforms shown are required for the fastest total switching times.

## Reverse to Forward

In the high impedance state, the IV characteristics are inductive. This can be considered a function of the fact that the I region must become flooded with stored charge before the current (and RF impedance) stabilizes. Accordingly, the driver must deliver a current spike with substantial overvoltage. The capacitor paralleling the output dropping resistor is called a “speed-up” capacitor and provides the spike.

Typical total switching time can be on the order of 2% to 10% of the specified diode lifetime and in general is much faster than switching in the other direction, from forward to reverse.



**Figure 9. SPST Switch Driver for 10 ns**

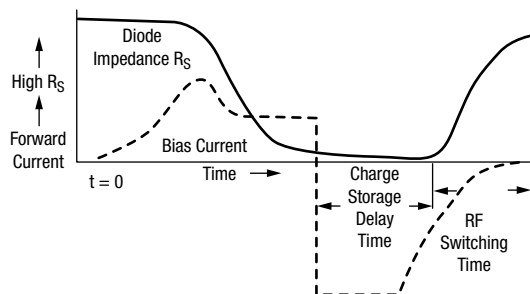


Figure 10. PIN Diode Switch Waveforms

### Forward To Reverse

In this mode the problem is to rapidly extract the stored charge from the I layer. Once again the solution is a reverse current spike coupled with a moderately high reverse bias voltage, with reverse current on the order of 10 to 20 times forward bias,

$$10 I_F \leq I_R \leq 20 I_F$$

The charge storage delay will be 5% to 10% of the lifetime. Additionally the actual RF switching time will be minimized by a large negative bias and/or by a low forward bias.

### Bias Circuitry

It is advisable to design the bias circuit to have the same characteristic impedance as the RF line to minimize reflections and ringing. Extraneous capacitance, in the form of blocking and bypass elements, must not be excessive. A typical 60+ pF bypass in a 50  $\Omega$  RF circuit produces a 3.0 nanosecond rise time. A few of these make it impossible to exploit the fastest PINs.

## Temperature Effects on Forward Resistance

### Series Resistance

Two conflicting mechanisms influence temperature behavior. First, as temperature rises, lifetime increases, allowing a greater carrier concentration and lowering  $R_S$ . Secondly, however, at higher temperature, mobility decreases, raising  $R_S$ . The net result of these competing phenomena is a function of diode design, bias current, RF power level, and frequency.

Figure 11 shows unlabeled curves of  $R_S$  vs. temperature with bias as a parameter. Most diodes show a monotonic increase of series resistance as temperature increases, while reverse losses tend to increase.

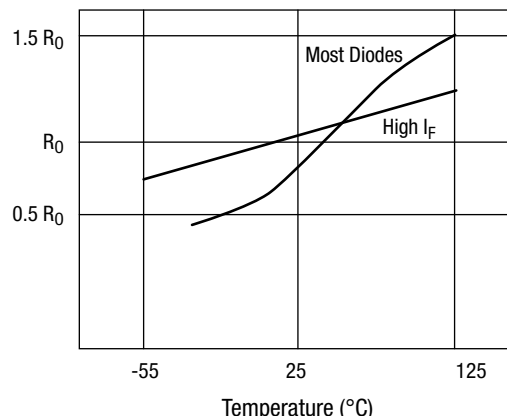


Figure 11. Series Resistance vs. Temperature

A typical fast switching diode will draw 10 mA at 850 mV at 25  $^{\circ}\text{C}$ . At -55  $^{\circ}\text{C}$ , the same  $V_F$  will draw about 500 microamps; at 100  $^{\circ}\text{C}$ ,  $I_F$  will be 200 mA.

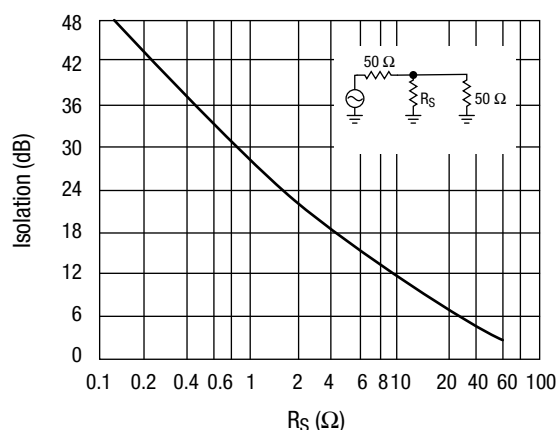


Figure 12. Shunt Diode Isolation vs. Forward Biased Resistance

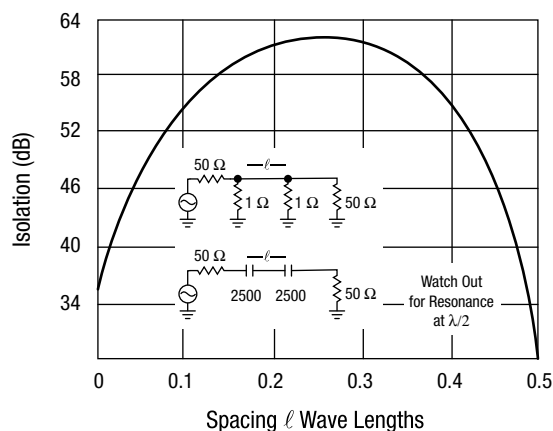


Figure 13. Isolation vs. Diode Spacing

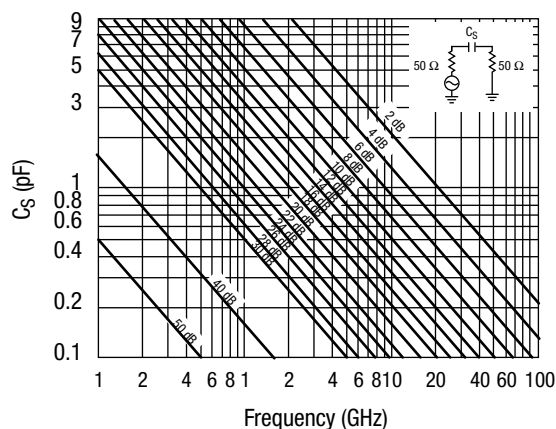


Figure 14. Isolation vs. Series Capacitance

### Simple Circuit Performance Charts

Figures 12 and 13 refer to chips shunt mounted in 50  $\Omega$  microstrip. Figure 14 refers to series-mounted diodes. Figure 12 shows isolation as a function of diode series resistance  $R_S$ . Figure 13 shows isolation as a function of diode spacing for a shunt pair of 1.0  $\Omega$  diodes, and a series pair of diodes with  $X_C = 2500 \Omega$ .

### How to Specify PIN Diodes

The uses for PIN diodes fall into three categories: series element, shunt element, and a limiter diode. The following guidelines should help in specifying a PIN diode for these applications.

#### For Series Diodes

$R_S$ —The forward series resistance will determine the minimum loss in the insertion loss state. Normally the diode will have a resistance slightly higher than  $R_S$  due to the internal junction resistance because of limited forward current. The ideal PIN diode series resistance is low, however. Low series resistances are associated with high idle state capacitance and a trade-off must, therefore, be made between off-state capacitance ( $C_J$ ) and series resistance ( $R_S$ ). Skyworks does this by choosing the proper junction diameter for your application.

$C_J$ —The capacitance (specified at 1 MHz at punch-through) is the off state capacitance, and for a series element determines the broadband isolation or, for narrow-band applications, the bandwidth of the switch.

#### Shunt Elements

$R_S$ —The forward series resistance of the shunt element determines the maximum isolation that can be obtained from this element. The ideal diode has extremely low  $R_S$ ; however, diodes with low  $R_S$  have an associated capacitance ( $C_J$ ) which may be high. The shunt element trade-off is to balance the required isolation with the effective insertion loss of a broadband switch at the band width of a narrow-band switch.

$C_J$ —The capacitance (specified at 1 MHz at punch-through) needs to be a low value to maintain low loss, broadband switching.  $C_J$  will also determine the input VSWR of the switch for broadband applications.

$V_B$ —The breakdown voltage of a PIN diode must be specified to assure the power handling of the switch component. In general the voltage must be high enough to prevent breakdown during the reverse bias condition, including the DC applied bias and the peak RF voltage. Failure to do so will cause a condition that can result in diode limiting and under severe circumstances can cause failure. For a simple shunt switch, a 100 V breakdown diode biased at 50 V can accommodate a peak voltage of ~50 V or power of 25 W average in a 50  $\Omega$  system. For maximum power handling, the reverse bias should be one-half of  $V_B$ .

## Limiters

PIN diodes with low breakdown voltages can serve as power limiters. The onset of limiting is primarily determined by the  $V_B$  of the diode. The limiting function is also affected by the lifetime of the base region. For this reason the frequency range, peak power requirements and threshold must be specified to choose a diode with minimum leakage. The power handling capability of limiter diodes is determined by  $V_B$  for short pulse applications and thermal heat sinking for long pulsed applications. The heat sinking is a composite of the thermal path in the diode and the mounting thermal resistance. Beam-lead diodes provide very low power handling capability due to the extremely high (1200 °C/W) thermal resistance—high powers can be achieved from shunt chips which can have thermal resistances below 5 °C/W. To determine the power handling capability of a limiter circuit one needs to determine the maximum power absorbed by the limiter diode. In hard limiting, the diode will reflect most of the power and only a small portion will be absorbed.

## References

1. Watson, H.A. *"Microwave Semiconductor Devices and their Circuit Applications,"* Chap. 2, McGraw-Hill, 1969.
2. op.cit. Watson, Chap. 9, "p-i-n Diodes" Olson, H.M.
3. *ibid.*
4. Chaffin, R.J. "Permanent Neutron Damage in PIN Microwave Diode Switches" Sandia Laboratories Report, SC-PR-70-853, Dec.1970.
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## APPLICATION NOTE

# Design With PIN Diodes

The PIN diode finds wide usage in RF, UHF and microwave circuits. It is fundamentally a device whose impedance, at these frequencies, is controlled by its DC excitation. A unique feature of the PIN diode is its ability to control large amounts of RF power with much lower levels of DC.

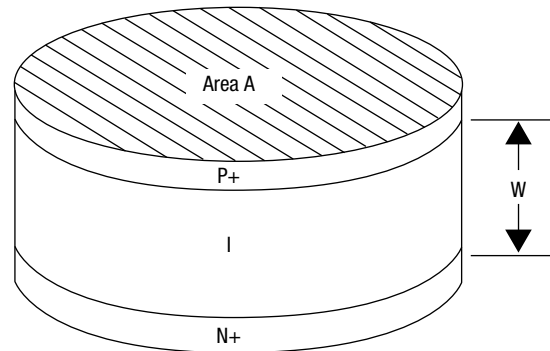
## PIN Diode Fundamentals

The PIN diode is a current controlled resistor at radio and microwave frequencies. It is a silicon semiconductor diode in which a high-resistivity intrinsic I region is sandwiched between a P-type and N-type region. When the PIN diode is forward biased, holes and electrons are injected into the I region. These charges do not immediately annihilate each other; instead they stay alive for an average time, called the carrier lifetime,  $\tau$ . This results in an average stored charge,  $Q$ , which lowers the effective resistance of the I region to a value  $R_S$ .

When the PIN diode is at zero or reverse bias there is no stored charge in the I region and the diode appears as a capacitor,  $C_T$ , shunted by a parallel resistance  $R_P$ .

PIN diodes are specified for the following parameters:

$R_S$	series resistance under forward bias
$C_T$	total capacitance at zero or reverse bias
$R_D$	parallel resistance at zero or reverse bias
$V_R$	maximum allowable DC reverse bias voltage
$\tau$	carrier lifetime
$\theta_{AV}$	average thermal resistance <u>or</u>
$P_D$	maximum average power dissipation
$\theta_{pulse}$	pulse thermal impedance <u>or</u>
$P_P$	maximum peak power dissipation



**Figure 1**

By varying the I region width and diode area, it is possible to construct PIN diodes of different geometrics to result in the same  $R_S$  and  $C_T$  characteristic. These devices may have similar small signal characteristics. However, the thicker I region diode would have a higher bulk, or  $R_F$  breakdown voltage, and better distortion properties. On the other hand, the thinner device would have faster switching speed.

There is a common misconception that carrier lifetime,  $\tau$ , is the only parameter that determines the lowest frequency of operation and the distortion produced. This is indeed a factor, but equally important is the thickness of the I region,  $W$ , which relates to the transit time frequency of the PIN diode.

## Low-Frequency Model

At low frequencies (below the transit time frequency of the I region) and DC, the PIN diode behaves like a silicon PN junction semiconductor diode. Its I-V characteristic determines the DC voltage at the forward bias current level. PIN diodes are often rated for the forward voltage,  $V_F$ , at a fixed DC bias.

The reverse voltage ratings on a PIN diode,  $V_R$ , are a guarantee from the manufacturer that no more than a specified amount, generally 10  $\mu\text{A}$ , of reverse current will flow when  $V_R$  is applied. It is not necessarily the avalanche or bulk breakdown voltage,  $V_B$ , which is determined by the I region width (approximately 10 V/ $\mu\text{m}$ ). PIN diodes of the same bulk breakdown voltage may have different voltage ratings. Generally, the lower the voltage rating, the less expensive the PIN diode.

## Large Signal Model

When the PIN diode is forward biased, the stored charge,  $Q$ , must be much greater than the incremental stored charge added or removed by the RF current,  $I_{RF}$ . To insure this, the following inequality must hold:

$$Q \gg \frac{I_{RF}}{2\pi f}$$

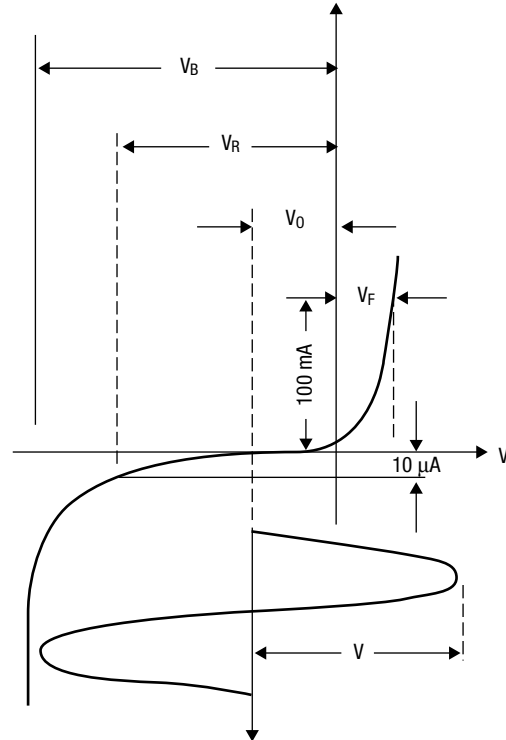


Figure 2

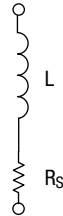
## RF Electrical Modeling of PIN Diode

### Forward Bias Model

$$R_S = \frac{W^2}{(\mu_n + \mu_p) Q} (\Omega)$$

Where:

- $Q = I_F \times \tau$  (coulombs)
- $W$  = I region width
- $I_F$  = forward bias current
- $\tau$  = carrier lifetime
- $\mu_n$  = electron mobility
- $\mu_p$  = hole mobility



Notes:

1. In commercially available diodes the parasitic resistance of the diode package and contact limit the lowest resistance value.
2. The lowest impedance will be affected by the parasitic inductance,  $L$ , which is generally less than 1 nHy.
3. The equation is valid at frequencies higher than the I region transmit time frequency, i.e.,

$$f > \frac{1300}{W^2} \text{ (where frequency is in MHz and } W \text{ in } \mu\text{m).}$$

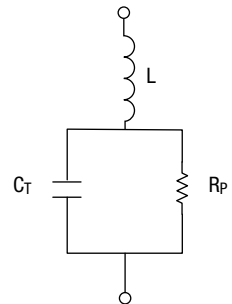
4. The equation assumes that the RF signal does not affect the stored charge.

### Zero or Reverse Bias Model

$$C_T = \frac{\epsilon A}{W}$$

Where:

- $\epsilon$  = dielectric constant of silicon
- $A$  = area of diode junction



Notes:

1. The above equation is valid at frequencies above the dielectric relaxation frequency of the I region, i.e.,

$$f > \frac{1}{2\pi \rho \epsilon} \text{ (where } \rho \text{ is the resistivity of the I region).}$$

At lower frequencies the PIN diode acts like a varactor.

2. The value  $R_P$  is proportional to voltage and inversely proportional to frequency. In most RF applications, its value is higher than the reactance of the capacitance,  $C_T$ , and is less significant.

Under reverse bias, the diode should not be biased beyond its DC voltage rating,  $V_R$ . The avalanche or bulk breakdown voltage,  $V_B$ , of a PIN diode is proportional to the I region wide,  $W$ , and is always higher than  $V_R$ . In a typical application, maximum negative voltage swing should never exceed  $V_B$ . An instantaneous excursion of the RF signal into the positive bias direction generally does not cause the diode to go into conduction because of slow reverse to forward switching speed. The DC reverse bias needed to maintain low PIN diode conductance has been analyzed<sup>6</sup> and is related to the magnitude of the RF signal and I region width.

Switching Speed Model

The switching speed in any application depends on the driver circuit, as well as the PIN diode. The primary PIN properties that influence switching speed may be explained as follows:

A PIN diode has two switching speeds from forward bias to reverse bias,  $T_{FR}$ , and from reverse bias to forward bias,  $T_{RF}$ . The diode characteristic that affects  $T_{FR}$  is  $\tau$ , carrier lifetime. The value of  $T_{FR}$  may be computed from the forward current,  $I_F$ , and the initial reverse current  $I_R$ , as follows:

$T_{RF}$  depends primarily on I region width,  $W$ , as indicated in the following chart which shows typical data:

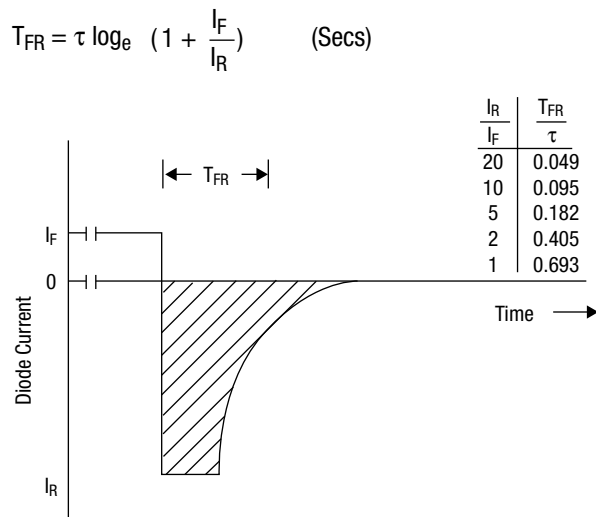


Figure 3

Thermal Model

I-Width μm	To 10 mA from		To 50 mA from		To 100 mA from	
	10 V	100 V	10 V	100 V	10 V	100 V
175	7 μs	5 μs	3 μs	2.5 μs	2 μs	1.5 μs
100	2.5 μs	2 μs	1 μs	0.8 μs	0.6 μs	0.6 μs
50	0.5 μs	0.4 μs	0.3 μs	0.2 μs	0.2 μs	0.1 μs

The maximum allowable power dissipation,  $P_D$ , is determined by the following equation:

$$P_D = \frac{T_J - T_A}{\theta} \quad (W)$$

where  $T_J$  is the maximum allowable junction temperature (usually 175 °C) and  $T_A$  is the ambient or heat sink temperature. Power dissipation may be computed as the product of the RF current squared, multiplied by the diode resistance,  $R_S$ .

For CW applications, the value of thermal resistance,  $\theta$ , used is the average thermal resistance,  $\theta_{AV}$ .

In most pulsed RF and microwave applications where the duty factor, DF, is less than 10 percent and the pulse width,  $T_P$ , is less than the thermal time constant of the diode, good approximation of the effective value of  $\theta$  in the above equation may be computed as follows:

$$\theta = DF \times \theta_{AV} + \theta_{TP} \quad ^\circ\text{C/W}$$

where  $\theta_{TP}$  is the thermal impedance of the diode for the time interval corresponding to  $T_P$ .

The following diagram indicates how junction temperature is affected during a pulsed RF application.

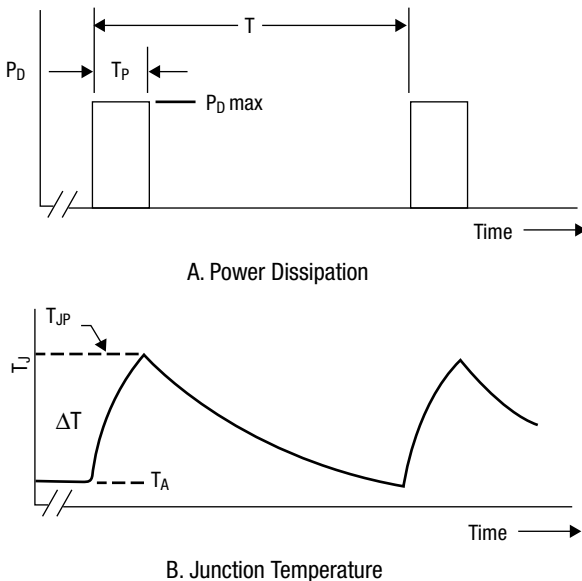


Figure 4



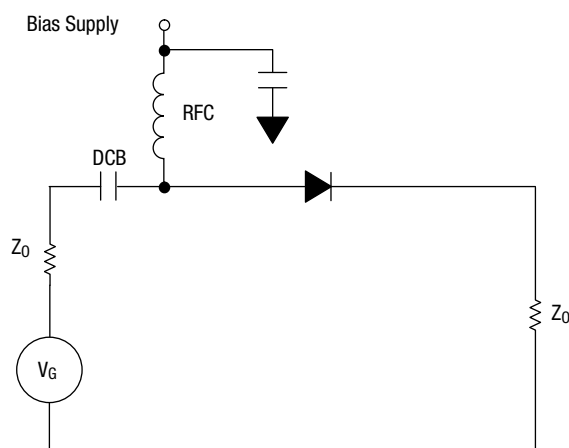
## PIN Diode Applications

### Switches

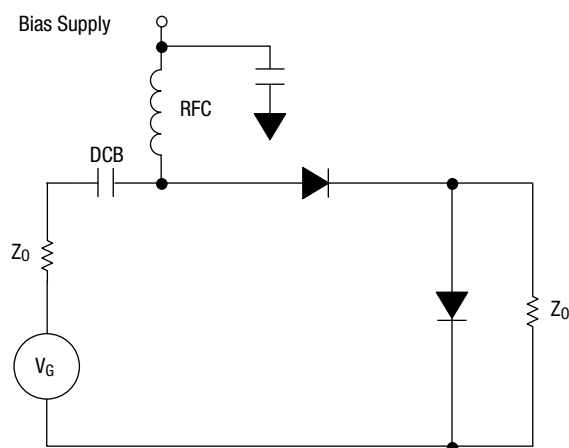
PIN diodes are commonly used as switching elements to control RF signals. In these applications, the PIN diode can be biased to either a high or low impedance device state, depending on the level of stored charge in the I region.

A simple untuned single pole, single throw (SPST) switch may be designed using either a single series or shunt connected PIN diode, as shown in Figure 5. The series connected diode switch is commonly used when minimum insertion loss is required over a broad frequency range. This design is also easier to physically realize using printed circuit techniques, since no through holes are required in the circuit board.

A single shunt mounted diode will, on the other hand, produce higher isolation values across a wider frequency range and will result in a design capable of handling more power since it is easier to heat sink the diode.



A. Series SPST Switch

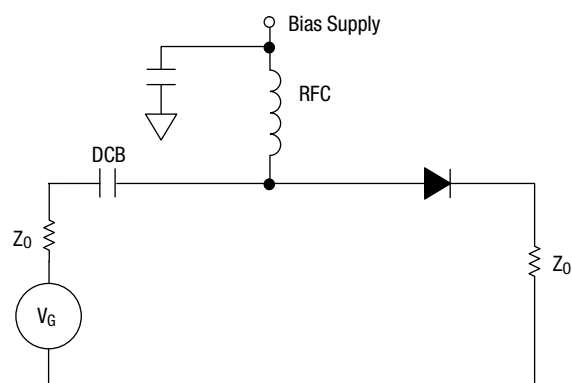


B. Shunt SPST Switch

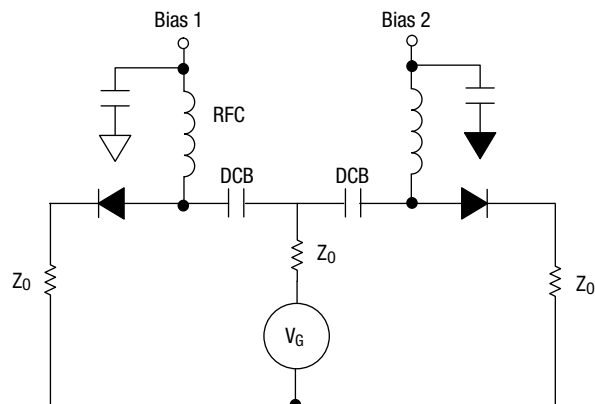
**Figure 5**

Multithrow switches are more frequently used than single-throw switches. A simple multithrow switch may be designed employing a series PIN diode in each arm adjacent to the common port. Improved performance is obtained by using “compound switches,” which are combinations of series and shunt connected PIN diodes, in each arm.

For narrow-band applications, quarter-wave spaced multiple diodes may also be used in various switch designs to obtain improved operation. In the following section, we shall discuss each of these types of switches in detail and present design information for selecting PIN diodes and predicting circuit performance.



A. Single Pole Single Throw (SPST)



B. Single Pole Double Throw (SPDT)

**Figure 6**

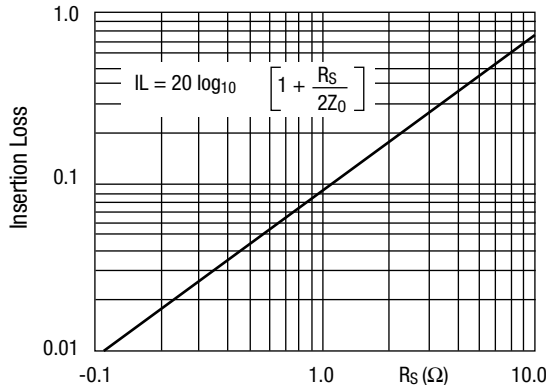
## Series Connected Switch

Figure 6 shows two basic types of PIN diode series switches, (SPST and SPDT), commonly used in broadband designs. In both cases, the diode is in a “pass power” condition when it is forward biased and presents a low forward resistance,  $R_S$ , between the RF generator and load. For the “stop power” condition, the diode is at zero or reverse bias so that it presents a high impedance between the source and load. In series connected switches, the maximum isolation obtainable depends primarily on the capacitance of the PIN diode, while the insertion loss and power dissipation are functions of the diode resistance. The principal operating parameters of a series switch may be obtained using the following equations:

### A. Insertion Loss (Series Switch)

$$IL = 20 \log_{10} [1 + R_S/2Z_0] \quad \text{dB (1)}$$

This equation applies for an SPST switch and is graphically presented in Figure 7 for a 50  $\Omega$  impedance design. For multithrow switches, the insertion loss is slightly higher due to any mismatch caused by the capacitance of the PIN diodes in the “off” arms. This additional insertion loss can be determined from Figure 10, after first computing the total shunt capacitance of all “off” arms of the multithrow switch.

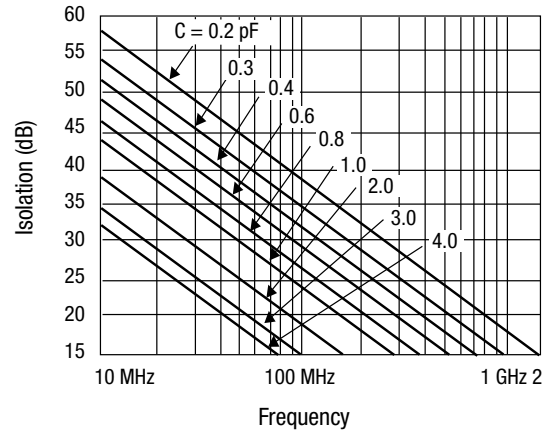


**Figure 7. Insertion Loss for PIN Diode Series Switch in 50  $\Omega$  System**

### B. Isolation (Series Switch)

$$I = 10 \log_{10} [1 + (4\pi f C Z_0)^{-2}] \quad \text{dB (2)}$$

This equation applies for an SPST diode switch. Add 6 dB for an SPNT switch to account for the 50 percent voltage reduction across the “off” diode, due to the termination of the generator in its characteristic impedance. Figure 8 graphically presents isolation as a function of capacitance for simple series switches. These curves are plotted for circuits terminated in 50  $\Omega$  loads.



**Figure 8. Isolation for SPST Diode Series Switch in 50  $\Omega$  System. Add 6 dB to Isolation for Multithrow Switches (SPNT)**

### C. Power Dissipation (Series Switch in Forward Bias)

$$P_D = \frac{4R_S Z_0}{(2Z_0 + R_S)^2} \cdot P_{AV} \quad \text{[W] (3)}$$

For  $Z_0 \gg R_S$ , this becomes:

$$P_D \approx \frac{R_S}{Z_0} \cdot P_{AV} \quad \text{[W] (4)}$$

Where the maximum available power is given by:

$$P_{AV} = \frac{V_G^2}{4Z_0} \quad \text{[W] (5)}$$

It should be noted that Equations 3 and 4 apply only for perfectly matched switches. For SWR ( $\sigma$ ) values other than unity, multiply these equations by  $[2\sigma/(\sigma + 1)]^2$  to obtain the maximum required diode power dissipation rating.

### D. Peak Current (Series Switch)

$$I_P = \sqrt{\frac{2P_{AV}}{Z_0}} \cdot \left( \frac{2\sigma}{\sigma + 1} \right) \quad \text{[amps] (6)}$$

In the case of a 50  $\Omega$  system, this reduces to:

$$I_P = \sqrt{\frac{P_{AV}}{5}} \left( \frac{2\sigma}{\sigma+1} \right) \quad [\text{amps}] \quad (7)$$

### C. Peak RF Voltage (Series Switch)

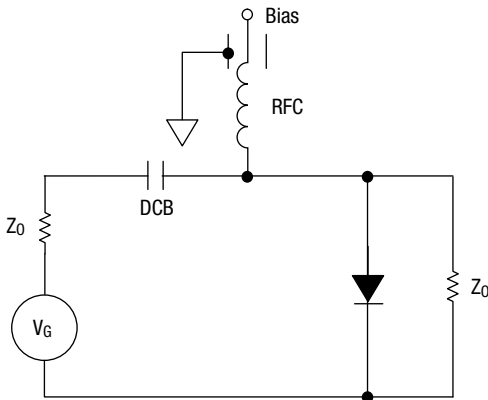
$$V_P = \sqrt{8Z_0 P_{AV}} \quad [\text{V}] \quad (\text{SPST})$$

$$V_P = \sqrt{2Z_0 P_{AV}} \left( \frac{2\sigma}{\sigma+1} \right) \quad [\text{V}] \quad (\text{SPST}) \quad (8)$$

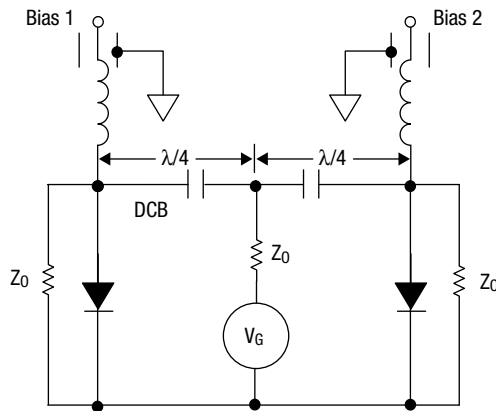
For a 50  $\Omega$  system, this becomes:

$$V_P = 20 \sqrt{P_{AV}} \quad [\text{V}] \quad (\text{SPST})$$

$$V_P = 10 \sqrt{P_{AV}} \left( \frac{2\sigma}{\sigma+1} \right) \quad [\text{V}] \quad (\text{SPST}) \quad (9)$$



A. Single Pole Single Throw Switch (SPST)



B. Single Pole Double Throw Switch (SPDT)

**Figure 9. Shunt Connected Switches 2–5**

## Shunt Connected Switch

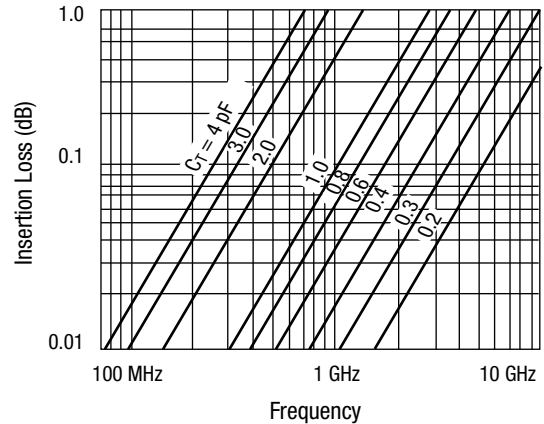
Figure 9 shows two typical shunt connected PIN diode switches. These shunt diode switches offer high isolation for many applications, and since the diode may be heat sunk at one electrode it is capable of handling more RF power than a diode in a series type switch.

In shunt switch designs, the isolation and power dissipation are functions of the diode's forward resistance, whereas the insertion loss is primarily dependent on the capacitance of the PIN diode. The principal equations describing the operating parameters of shunt switches are given by:

### A. Insertion Loss (Shunt Switch)

$$IL = 10 \log_{10} [1 + (\pi f C_T Z_0)^2] \quad [\text{dB}] \quad (10)$$

This equation applies for both SPST and SPNT shunt switches and is graphically presented in Figure 10 for a 50  $\Omega$  load impedance design.

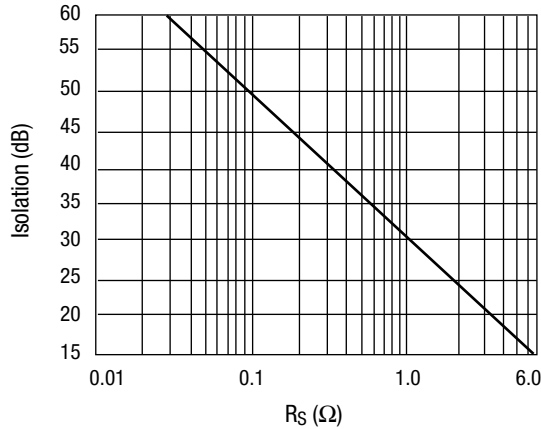


**Figure 10. Insertion Loss for Shunt PIN Switch in 50  $\Omega$  System**

### B. Isolation (Shunt Switch)

$$I = 20 \log_{10} \left[ 1 + \frac{Z_0}{2R_S} \right] \quad [\text{dB}] \quad (11)$$

This equation, which is illustrated in Figure 11, applies for an SPST shunt switch. Add 6 dB to these values to obtain the correct isolation for a multithrow switch.



**Figure 11. Isolation for SPST Shunt PIN Switches in 50 Ω System. Add 6 dB to Isolation for Multithrow Switches (SPNT)**

#### C. Power Dissipation (Shunt Switch in Forward Bias)

$$P_D = \frac{4R_S Z_0}{(Z_0 + 2R_S)^2} \cdot P_{AV} \quad [W] \quad (12)$$

For  $Z_0 \gg R_S$  this becomes:

$$P_D = \frac{4R_S}{Z_0} \cdot P_{AV} \quad [W] \quad (13)$$

where the maximum available power is given by:

$$P_{AV} = \frac{V_G^2}{4Z_0} \quad (14)$$

#### D. Power Dissipation (Shunt Switch in Reverse)

$$P_D = \frac{Z_0}{R_P} \cdot P_{AV} \quad [W] \quad (15)$$

where  $R_P$  is the reverse biased diode's parallel resistance.

#### E. Peak RF Current (Shunt Switch)

$$I_P = \sqrt{\frac{8P_{AV}}{Z_0}} \quad [\text{amps}] \quad (\text{SPST})$$

$$I_P = \sqrt{\frac{2P_{AV}}{Z_0} \left( \frac{2\sigma}{\sigma + 1} \right)} \quad [\text{amps}] \quad \text{SPNT} \quad (16)$$

for a 50 Ω system, this becomes:

$$I_P = 0.4 \sqrt{P_{AV}} \quad [\text{amps}] \quad (\text{SPST})$$

$$I_P = 0.2 \sqrt{P_{AV} \left( \frac{2\sigma}{\sigma + 1} \right)} \quad [\text{amps}] \quad \text{SPNT} \quad (17)$$

#### F. Peak RF Voltage (Shunt Switch)

$$V_P = \sqrt{2Z_0 P_{AV} \left( \frac{2\sigma}{\sigma + 1} \right)} \quad [V] \quad (18)$$

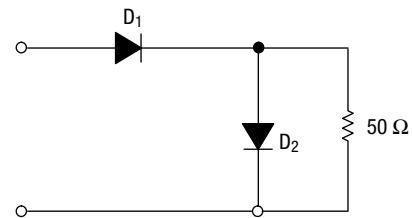
In the case of a 50 Ω system, this reduces to:

$$V_P = 10 \sqrt{P_{AV} \left( \frac{2\sigma}{\sigma + 1} \right)} \quad [V] \quad (19)$$

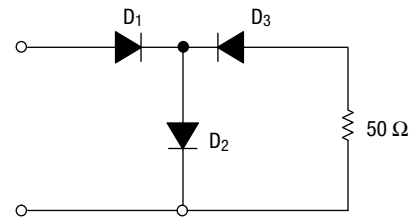
### Compound and Tuned Switches

In practice, it is usually difficult to achieve more than 40 dB isolation using a single PIN diode, either in shunt or series, at RF and higher frequencies. The causes of this limitation are generally radiation effects in the transmission medium and inadequate shielding. To overcome this, there are switch designs that employ combinations of series and shunt diodes (compound switches), and switches that employ resonant structures (tuned switches) affecting improved isolation performance.

The two most common compound switch configurations are PIN diodes mounted in either ELL (series-shunt) or TEE designs, as shown in Figure 12. In the insertion loss state for a compound switch, the series diode is forward biased and the shunt diode is at zero or reverse bias. The reverse is true for the isolation state. This adds some complexity to the bias circuitry in comparison to simple switches. A summary of formulas used for calculating insertion loss and isolation for compound and simple switches is given in Figure 13.



A. ELL (Series-Shunt) SPST Switch

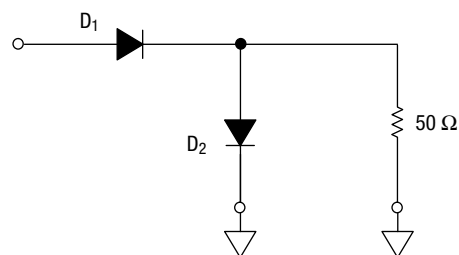


B. TEE SPST Switch

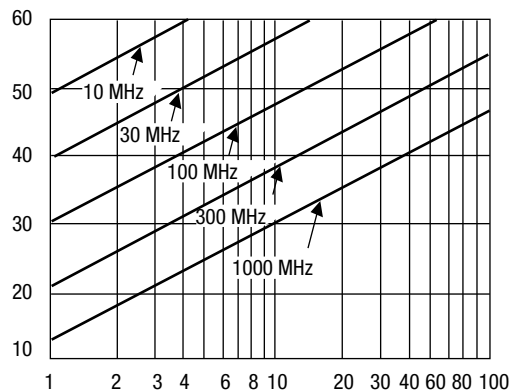
**Figure 12. Compound Switches**

Type	Isolation	Insertion Loss (dB)
Series	$10 \log_{10} \left[ 1 + \left( \frac{X_C}{2Z_0} \right)^2 \right]$	$20 \log_{10} \left[ 1 + \frac{R_S}{2Z_0} \right]$
Shunt	$20 \log_{10} \left[ 1 + \frac{Z_0}{2R_S} \right]$	$10 \log_{10} \left[ 1 + \left( \frac{Z_0}{2X_C} \right)^2 \right]$
Series-Shunt	$10 \log_{10} \left[ \left( 1 + \frac{Z_0}{2R_S} \right)^2 + \left( \frac{X_C}{2Z_0} \right)^2 \left( 1 + \frac{Z_0}{R_S} \right)^2 \right]$	$10 \log_{10} \left[ \left( 1 + \frac{R_S}{2Z_0} \right)^2 + \left( \frac{Z_0 + R_S}{2X_C} \right)^2 \right]$
TEE	$10 \log_{10} \left[ 1 + \left( \frac{X_C}{Z_0} \right)^2 \right] + 10 \log_{10} \left[ \left( 1 + \frac{Z_0}{2R_S} \right)^2 + \left( \frac{X_C}{2R_S} \right)^2 \right]$	$20 \log_{10} \left[ 1 + \frac{R_S}{Z_0} \right] + 10 \log_{10} \left[ 1 + \left( \frac{Z_0 + R_S}{2X_C} \right)^2 \right]$

**Figure 13. Summary of Formulas for SPST Switches.**  
(Add 6 dB to Isolation to Obtain Value for Single Pole Multithrow Switch.)

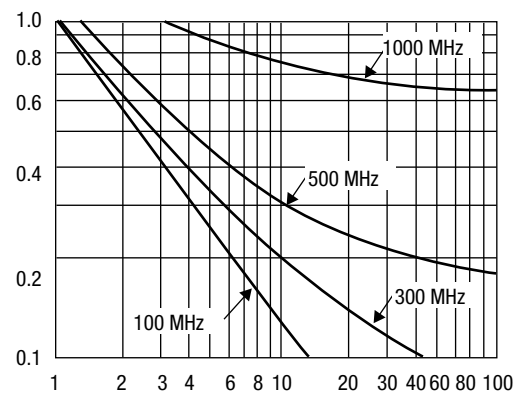


A. Circuit Diagram



B. Isolation

Bias Current in  $D_2$  mA ( $D_1$  Reversed Biased)  
Note: Add 6 dB for SPNT Switch



C. Insertion Loss

Bias Current in  $D_1$  mA ( $D_2$  Reversed Biased)

**Figure 14. Series Shunt Switch**

Figure 14 shows the performance of an ELL type switch, a diode rated at 3.3 pF, maximum capacitance, and 0.25  $\Omega$ ,  $R_S$  maximum at 100 mA. In comparison, a simple series connected using the same diode switch would have similar insertion loss to the 100 MHz contour and the isolation would be 15 dB maximum at 100 MHz, falling off at the rate of 6 dB per octave.

A tuned switch may be constructed by spacing two series diodes or two shunt diodes a wavelength apart, as shown in Figure 15. The resulting value of isolation in the tuned switch is twice that obtainable in a single diode switch. The insertion loss of the tuned series switch is higher than that of the simple series switch and may be computed using the sum of the diode

resistance as the  $R_S$  value in equation 1. In the tuned shunt switch the insertion loss may even be lower than in a simple shunt switch because of a resonant effect of the spaced diode capacitances.

Quarter-wave spacing need not be limited to frequencies where the wavelength is short enough to install a discrete length of line. There is a lumped circuit equivalent which simulates the quarter-wave section and may be used in RF band. This is shown in Figure 16. These tuned circuit techniques are effective in applications having bandwidths on the order of 10 percent of the center frequency.

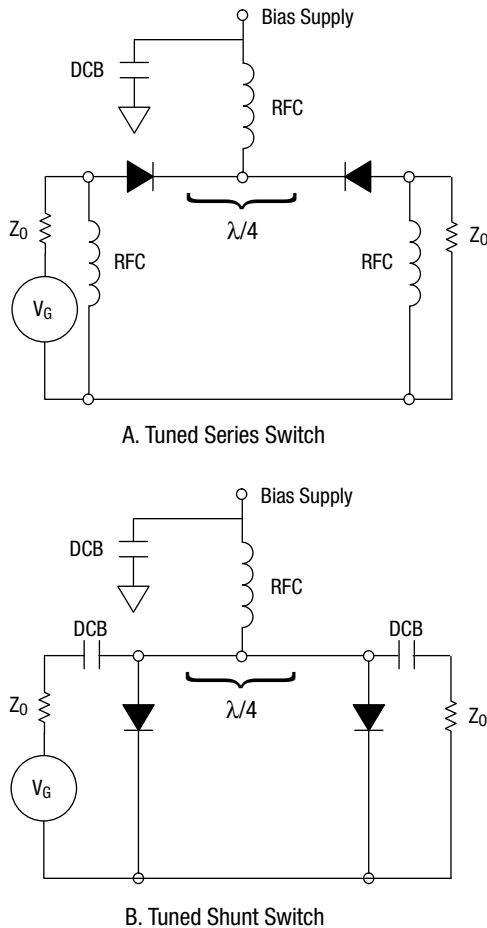


Figure 15

## Transmit-Receive Switches

There is a class of switches used in transceiver applications whose function is to connect the antenna to the transmitter (exciter) in the transmit state and to the receiver during the receiver state. When PIN diodes are used as elements in these switches, they offer higher reliability, better mechanical ruggedness and faster switching speed than electro-mechanical designs.

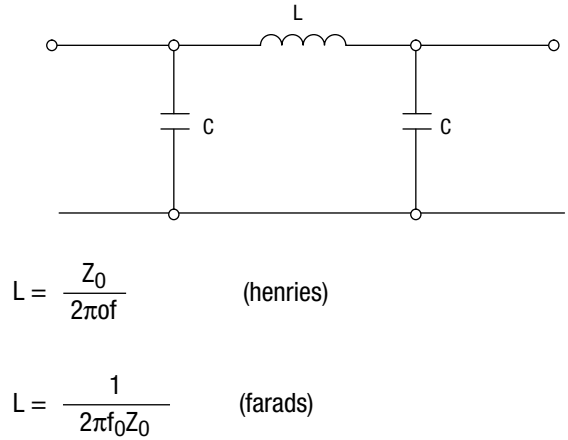


Figure 16. Quarter-Wave Line Equivalent

The basic circuit for an electronic switch consists of a PIN diode connected in series with the transmitter, and a shunt diode connected a quarter wavelength away from the antenna node. A lumped-component equivalent of a quarter wave transmission line is shown in Figure 16.

When switched into the transmit state, each diode becomes forward biased. The series diode appears as a low impedance to the signal heading toward the antenna, and the shunt diode effectively shorts the receiver's antenna terminals to prevent overloading. Transmitter insertion loss and receiver isolation depend on the diode resistance. If  $R_S$  is 1  $\Omega$  greater than 30 dB isolation and less than 0.2 dB insertion, loss can be expected. This performance is achievable over a 10 percent bandwidth.

In the receive condition, the diodes are at zero or reverse bias and present essentially a low capacitance,  $C_T$ , which creates a direct low insertion loss path between the antenna and receiver. The off transmitter is isolated from this path by the high impedance series diode.

The amount of power,  $P_A$ , this switch can handle depends on the power rating of the PIN diode,  $P_D$ , and the diode resistance. The equation showing this relationship is as follows for an antenna maximum SWR of  $\sigma$ :

$$P_A = \frac{P_D Z_0}{R_S} \left( \frac{\sigma + 1}{2\sigma} \right)^2 \quad [W]$$

In a 50  $\Omega$  system where the condition of a totally mismatched antenna must be considered this equation reduces to:

$$P_A = \frac{12.5 \times P_D}{R_S} \quad [W]$$

The SMP1322-011 is a surface mount PIN diode rated at 0.25 W dissipation to a 25 °C contact. The resistance of this diode is a 0.50  $\Omega$  (max) at 10 mA. A quarter-wave switch using SMP1322-011 may then be computed to handle 6.25 W with a totally mismatched antenna.

It should be pointed out that the shunt diode of the quarter-wave antenna switch dissipates about as much power as the series diode. This may not be apparent from Figure 17; however, it may be shown that the RF current in both the series and shunt diode is practically identical.

Broadband antenna switches using PIN diodes may be designed using the series connected diode circuit shown in Figure 18. The frequency limitation of this switch results primarily from the capacitance of  $D_2$ .

In this case, forward bias is applied either to  $D_1$  during the transmit or  $D_2$  during receive. In high power application (> 5 W) it is often necessary to apply reverse voltage on  $D_2$

during transmit. This may be accomplished either by a negative polarity power supply at Bias 2, or by having the forward bias current of  $D_1$  flow through resistor R to apply the required negative voltage.

The selection of diode  $D_1$  is based primarily on its power handling capability. It need not have a high voltage rating since it is always forward biased in its low resistance state when high RF power is applied. Diode  $D_2$  does not pass high RF current but must be able to hold off the RF voltage generated by the transmitter. It is primarily selected on the basis of its capacitance, which determines the upper frequency limit and its ability to operate at low distortion.

Using the SMP1322-011 as  $D_1$ , and an SMP1302-001 or SOT-23 PIN diode which are rated at 0.3 pF max as  $D_2$ , greater than 25 dB receiver isolation may be achieved up to 400 MHz. The expected transmit and receive insertion loss with the PIN diodes biased at 10 mA are 0.1 dB and 0.3 dB, respectively. This switch can handle RF power levels up to 6.25 W.

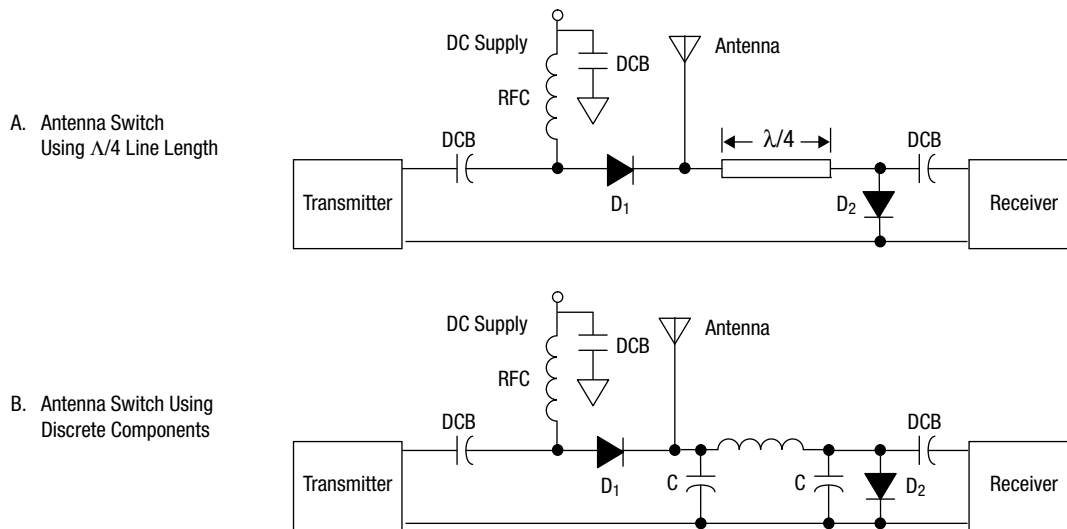


Figure 17. Quarter-Wave Antenna Switches

## Practical Design Hints

PIN diode circuit performance at RF frequencies is predictable and should conform closely to the design equations. When a switch is not performing satisfactorily, the fault is often not due to the PIN diode but to other circuit limitations, such as circuit loss, bias circuit interaction or lead length problems (primarily when shunt PIN diodes are employed).

It is good practice in a new design to first evaluate the circuit loss by substituting alternatively a wire short or open in place of the PIN diode. This will simulate the circuit performance with "ideal PIN diodes." Any deficiency in the external circuit may then be corrected before inserting the PIN diodes.

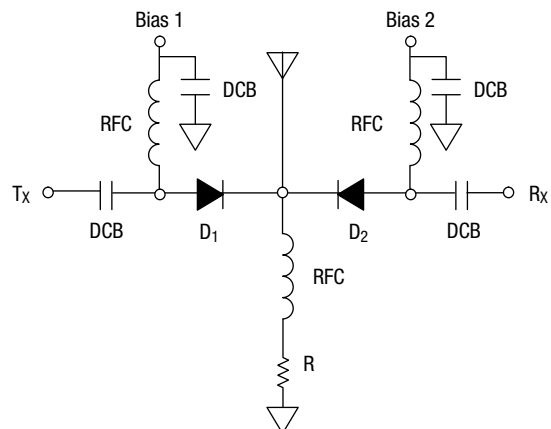


Figure 18. Broadband Antenna Switch



## PIN Diode Attenuators

In an attenuator application, the resistance characteristic of the PIN diode is exploited not only at its extreme high and low values, as in switches, but at the finite values in between.

The resistance characteristic of a PIN diode when forward biased to IF1 depends on the I region width ( $W$ ) carrier lifetime ( $\tau$ ), and the hole and electron mobilities  $\mu_p$   $\mu_n$  as follows:

$$R_S = W^2 / (\mu_p + \mu_n) I_F \tau \quad \Omega \quad (1)$$

For a PIN diode with an I region width of typically 250  $\mu\text{m}$ , carrier lifetime of 4  $\mu\text{s}$ , and  $\mu_n$  of 0.13,  $\mu_p$  of 0.05  $\text{m}^2/\text{V}\cdot\text{s}$ , Figure 19 shows the  $R_S$  versus current characteristic.

In the selection of a PIN diode for an attenuator application, the designer must often be concerned about the range of diode resistance, which will define the dynamic range of the attenuator. PIN diode attenuators tend to be more distortion sensitive than switches since their operating bias point often occurs at a low value of quiescent stored charge. A thin I region PIN will operate at lower forward bias currents than thick PIN diodes, but the thicker one will generate less distortion.

PIN diode attenuator circuits are used extensively in Automatic Gain Control (AGC) and RF leveling applications, as well as in electronically controlled attenuators and modulators. A typical configuration of an AGC application is shown in Figure 20. The PIN diode attenuator may take many forms ranging from a simple series or shunt mounted diode acting as a lossy reflective switch, or a more complex structure that maintains a constant matched input impedance across the full dynamic range of the attenuator.

Although there are other methods for providing AGC functions, such as varying the gain of the RF transistor amplifier, the PIN diode approach generally results in lower power drain, less frequency pulling, and lower RF signal distortion. The latter results are especially true when diodes with thick I regions and long carrier lifetimes are used in the attenuator circuits. Using these PIN diodes, one can achieve wide dynamic range attenuation with low signal distortion at frequencies ranging from below 1 MHz up to well over 1 GHz.

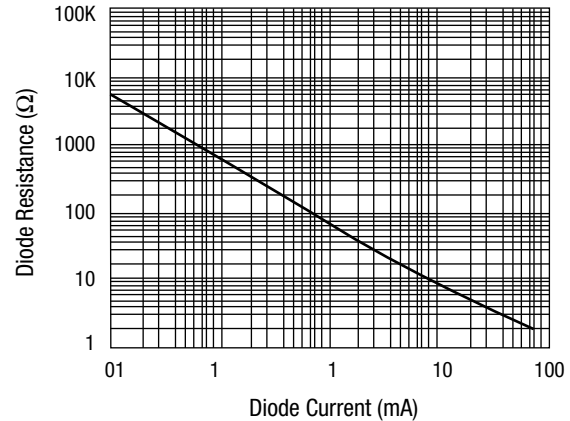


Figure 19. Typical Diode Resistance vs. Forward Current

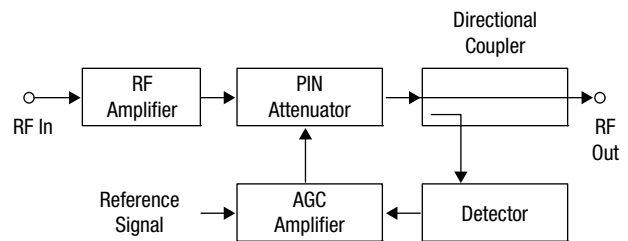


Figure 20. RF AGC/Leveler Circuit

## Reflective Attenuators

An attenuator may be designed using single series or shunt connected PIN diode switch configurations, as shown in Figure 21. These attenuator circuits utilize the current controlled resistance characteristic of the PIN diode, not only in its low loss states (very high or low resistance), but also at in-between, finite resistance values.

The attenuation value obtained using these circuits may be computed from the following equations:

Attenuation of Series Connected  
PIN Diode Attenuator

$$A = 20 \log \left( 1 + \frac{R_S}{2Z_0} \right) \quad \text{dB} \quad (2)$$

Attenuation of Shunt Connected  
PIN Diode Attenuator

$$A = 20 \log \left( 1 + \frac{Z_0}{2R_S} \right) \quad \text{dB} \quad (3)$$

These equations assume the PIN diode to be purely resistive. The reactance of the PIN diode capacitance, however, must also be taken into account at frequencies where its value begins to approach the PIN diode resistance value.



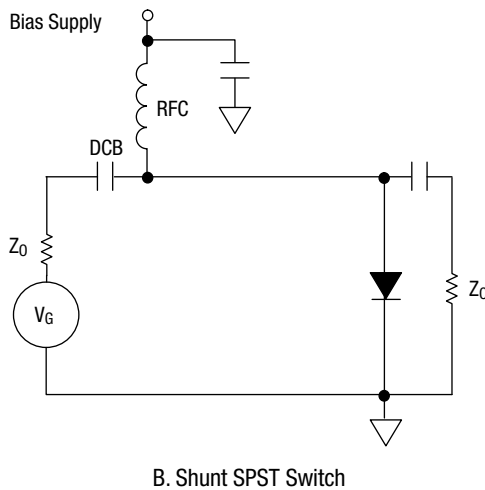
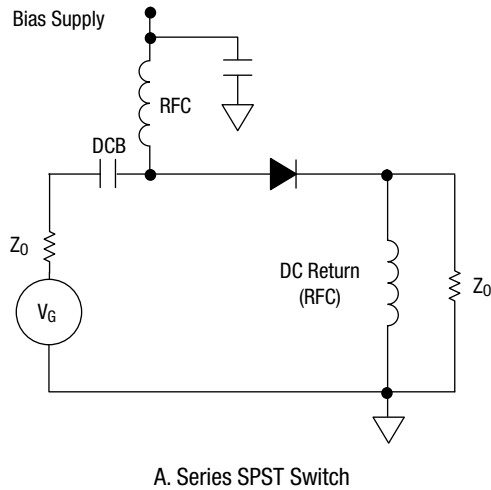


Figure 21. SPST PIN Diode Switches

### Matched Attenuators

Attenuators built from switch design are basically reflective devices which attenuate the signal by producing a mismatch between the source and the load. Matched PIN diode attenuator designs, which exhibit constant input impedance across the entire attenuation range, are also available. They use either multiple PIN diodes biased at different resistance points or bandwidth limited circuits utilizing tuned elements. They are described as follows:

### Quadrature Hybrid Attenuators

Although a matched PIN attenuator may be achieved by combining a ferrite circulator with one of the previous simple reflective devices, the more common approach makes use of quadrature hybrid circuits. Quadrature hybrids are commonly available at frequencies from below 10 MHz to above 1 GHz, with bandwidth coverage often exceeding a decade. Figures 22

and 23 show typical quadrature hybrid circuits employing series and shunt connected PIN diodes. The following equations summarize this performance:

Quadrature Hybrid  
(Series Connected PIN Diodes)

$$A = 20 \log \left( 1 + \frac{2Z_0}{R_S} \right) \text{ dB (4)}$$

Quadrature Hybrid  
(Shunt Connected PIN Diodes)

$$A = 20 \log \left( 1 + \frac{2R_S}{Z_0} \right) \text{ dB (5)}$$

The quadrature hybrid design approach is superior to the circulator coupled attenuator from the standpoint of lower cost and the achievement of lower frequency operation. Because the incident power is divided into two paths, the quadrature hybrid configuration is also capable of handling twice the power, and this occurs at the 6 dB attenuation point. Each load resistor, however, must be capable of dissipating one-half the total input power at the time of maximum attenuation.

Both the above types of hybrid attenuators offer good dynamic range. The series connected diode configuration is, however, recommended for attenuators used primarily at high attenuation levels (greater than 6 dB), while the shunt mounted diode configuration is better suited for low attenuation ranges.

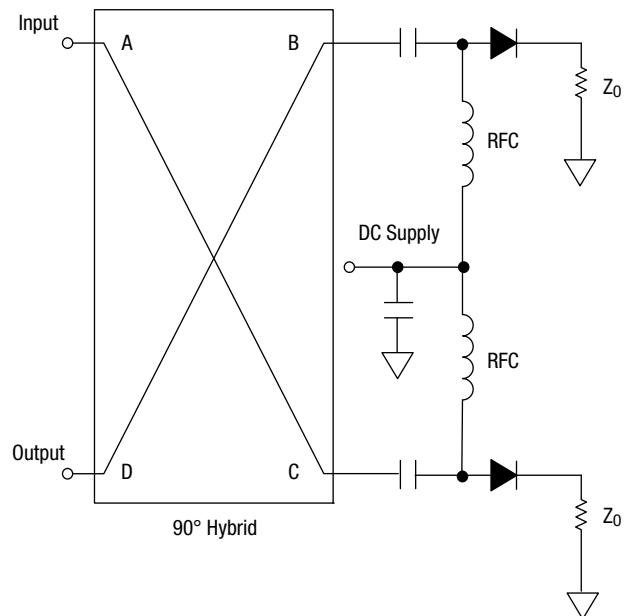
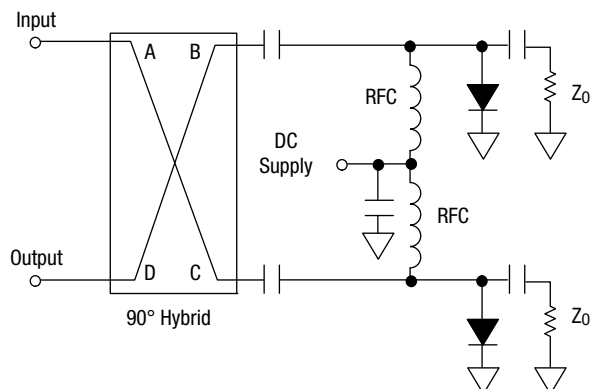


Figure 22. Quadrature Matched Hybrid Attenuator (Series Connected Diodes)



**Figure 23. Quadrature Hybrid Matched Attenuator (Shunt Connected PIN Diodes)**

Constant impedance attenuator circuit. The power incident on port A divides equally between ports B and C, port D is isolated. The mismatch produced by the PIN diode resistance in parallel with the load resistance at ports B and C reflects part of the power. The reflected power exits port D, isolating port A. Therefore, A appears matched to the input signal.

Quadrature hybrid attenuators may also be constructed without the load resistor attached in series or parallel to the PIN diode as shown. In these circuits the forward current is increased from the 50  $\Omega$ , maximum attenuation/ $R_S$  value to lower resistance values. This results in increased stored charge as the attenuation is lowered, which is desirable for lower distortion. The purpose of the load resistor is both to make the attenuator less sensitive to individual diode differences and to increase the power-handling capacity by a factor of two.

## Quarter-Wave Attenuators

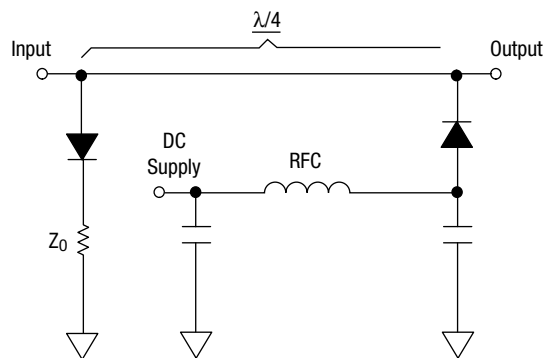
An attenuator matched at the input may also be built using quarter-wave techniques. Figures 24 and 25 show examples of these circuits. For the quarter-wave section a lumped equivalent may be employed at frequencies too low for practical use of line lengths. This equivalent is shown in Figure 26.

The performance equations for these circuits are given below:

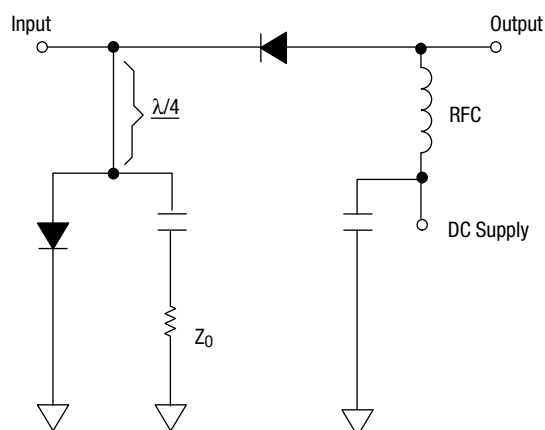
Quarter-Wave Attenuator  
(Series Connected Diode)

$$A = 20 \log \left( 1 + \frac{Z_0}{R_S} \right) \quad \text{dB (6)}$$

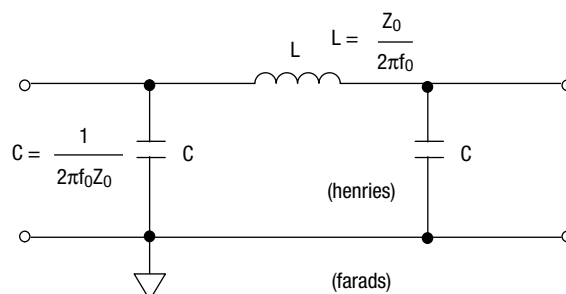
$$A = 20 \log \left( 1 + \frac{R_S}{Z_0} \right) \quad \text{dB (7)}$$



**Figure 24. Quarter-Wave Matched Attenuator (Series Connected Diodes)**



**Figure 25. Quarter-Wave Matched Attenuator (Shunt Connected Diodes)**



**Figure 26. Lumped Circuit Equivalent of Quarter-Wave Line**

A matched condition is achieved in these circuits when both diodes are at the same resistance. This condition should normally occur when using similar diodes, since they are DC series connected, with the same forward bias current flowing through each diode. The series circuit of Figure 24 is recommended for use at high attenuation levels, while the shunt diode circuit of Figure 25 is better suited for low attenuation circuits.

### Bridged TEE and PI Attenuators

For matched broadband applications, especially those covering the low RF (1 MHz) through UHF, attenuator designs using multiple PIN diodes are employed. Commonly used for this application are the bridged TEE and PI circuits shown in Figures 27 and 28.

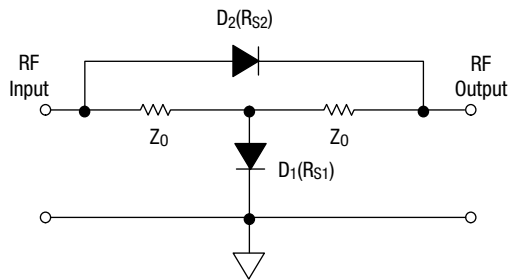


Figure 27. Bridged TEE Attenuator

The attenuation obtained using abridged TEE circuit may be calculated from the following:

$$A = 20 \log \left( 1 + \frac{Z_0}{R_{S1}} \right) \quad \text{dB (8)}$$

where:

$$Z_0^2 = R_{S1} \times R_{S2} \quad \Omega^2 \text{ (9)}$$

The relationship between the forward resistance of the two diodes insures maintenance of a matched circuit at all attenuation values.

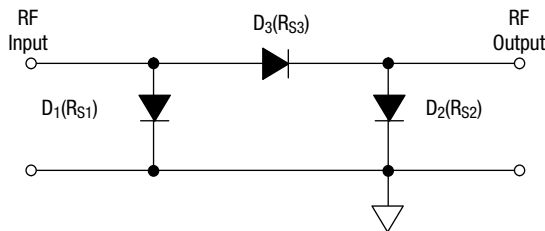


Figure 28. PI Attenuator (the  $\pi$  and TEE are Broadband Matched Attenuator Circuits)

The expressions for attenuation and matching conditions for the PI attenuator are given as follows:

$$A = 20 \log \left( \frac{R_{S1} + Z_0}{R_{S1} - Z_0} \right) \quad \text{dB (10)}$$

where:

$$R_{S3} = \frac{2R_{S1}Z_0^2}{R_{S1}^2 - Z_0^2} \quad \Omega \text{ (11)}$$

$$R_{S1} = R_{S2} \quad \Omega \text{ (12)}$$

Using these expressions, Figure 29 gives a graphical display of diode resistance values for a 50  $\Omega$  PI attenuator. Note that the minimum value for  $R_{S1}$  and  $R_S$  is 50  $\Omega$ . In both the bridged TEE and PI attenuators, the PIN diodes are biased at two different resistance points simultaneously, which must track in order to achieve proper attenuator performance.

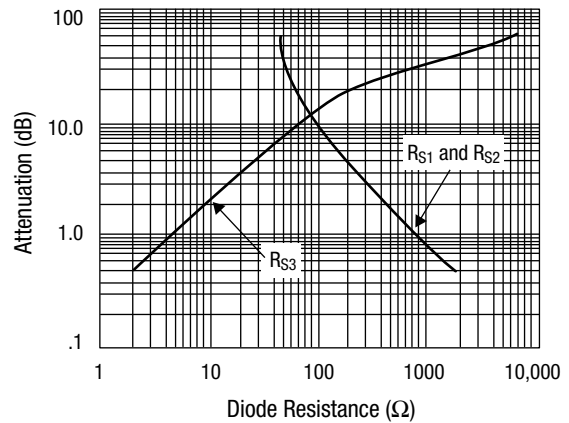


Figure 29. Attenuation of PI Attenuators

### PIN Diode Modulators

PIN diode switches and attenuators may be used as RF amplitude modulators. Square wave or pulse modulation use PIN diode switch designs, whereas linear modulators use attenuator designs.

The design of high-power or distortion-sensitive modulator applications follows the same guidelines as their switch and attenuator counterparts. The PIN diodes they employ should have thick I regions. Series connected, or, preferably, back-to-back configurations always reduce distortion. The sacrifice in using these devices will be lower maximum frequencies and higher modulation current requirements.

The quadrature hybrid design is recommended as a building block for PIN diode modulators. Its inherent built-in isolation minimizes pulling and undesired phase modulation on the driving source.

## PIN Diode Phase Shifters

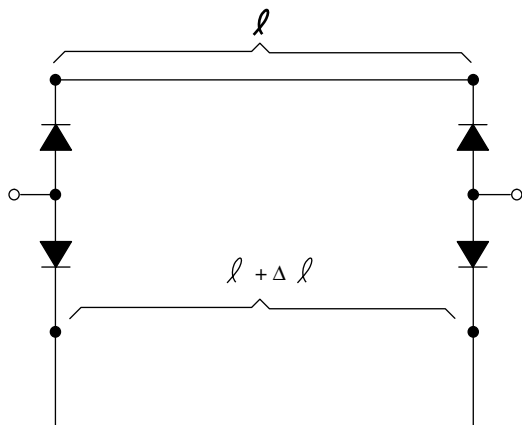
PIN diodes are utilized as series or shunt connected switches in phase shifter circuit designs. In such cases, the elements switched are either lengths of transmission line or reactive elements. The criteria for choosing PIN diodes for use in phase shifters are similar to those used in selecting diodes for other switching applications. One additional factor, however, that must often be considered is the possibility of introducing phase distortion, particularly at high RF power levels or low reverse bias voltages. Of significant note is the fact that the properties inherent in PIN diodes which yield low distortion, i.e., a long carrier lifetime and thick I regions, also result in low phase distortion of the RF signal. Three of the most common types of semiconductor phase shifter circuits, namely the switched line, loaded line and hybrid coupled designs, are described as follows:

### A. Switched Line Phase Shifter

A basic example of a switched line phase shifter circuit is shown in Figure 30. In this design, two SPDT switches employing PIN diodes are used to change the electrical length of transmission line by some length  $\Delta \ell$ . The phase shift obtained from this circuit varies with frequency and is a direct function of this differential line length as shown below:

$$\Delta\theta = 2\pi\Delta\ell\lambda \quad \text{radians (13)}$$

The switched line phase shifter is inherently a broadband circuit producing true time delay, with the actual phase shift dependent only on  $\Delta \ell$ . Because of PIN diode capacitance limitations, this design is most frequently used at frequencies below 1 GHz.



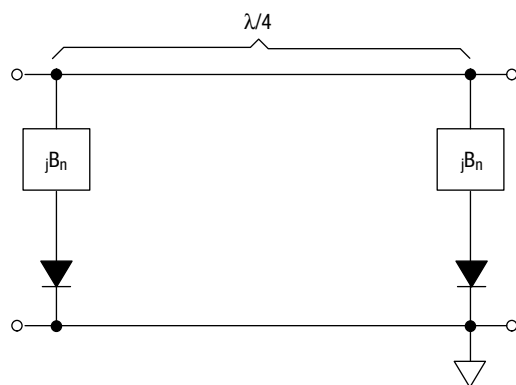
**Figure 30. Switched Line Phase Shifter**

The power capabilities and loss characteristics of the switched line phase shifter are the same as those of a series connected SPDT switch. A unique characteristic of this circuit is that the

power and voltage stress on each diode is independent of the amount of differential phase shift produced by each phase shifter. Thus, four diodes are required for each bit, with all diodes having the same power and voltage ratings.

### B. Loaded Line Phase Shifter

The loaded line shifter design shown in Figure 31 operates on a different principle than the switched line phase shifter. In this design the desired maximum phase skirt is divided into several smaller phase shift sections, each containing a pair of PIN diodes, which do not completely perturbate the main transmission line. A major advantage of this phase shifter is its extremely high power capability, due partly to the use of shunt mounted diodes, plus the PIN diodes are never in the direct path of the full RF power.



**Figure 31. Loaded Line Phase Shifter**

In loaded line phase shifters, a normalized susceptance,  $B_n$ , is switched in and out of the transmission path by the PIN diodes. Typical circuits use values of  $B_n$  much less than unity, resulting in considerable decoupling of the transmitted RF power from the PIN diode. The phase shift for a single section is given as follows:

$$\theta = 2 \tan^{-1} \left( \frac{B_n}{1 - B_n^2/8} \right) \quad \text{radians (14)}$$

The maximum phase shift obtainable from a loaded line section is limited by both bandwidth and diode power handling considerations. The power constraint on obtainable phase shift is shown as follows:

$$\theta_{\max} = 2 \tan^{-1} \left( \frac{V_{BR} I_F}{4P_L} \right) \quad \text{radians (15)}$$

where:

$\theta_{\max}$  = maximum phase angle

$P_L$  = power transmitted

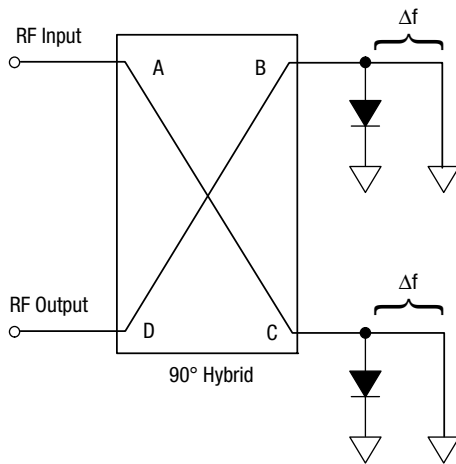
$V_{BR}$  = diode breakdown voltage

$I_F$  = diode current rating

The above factors limit the maximum phase shift angle in practical circuits to about 45°. Thus, a 180° phase shift would require the use of four 45° phase shift sections in its design.

### C. Reflective Phase Shifter

A circuit design which handles both high RF power and large incremental phase shifts with the fewest number of diodes is the hybrid coupled phase shifter shown in Figure 32. The phase shift for this circuit is given below:



**Figure 32. Hybrid Coupler Reflective Phase Shifter**

The voltage stress on the shunt PIN diode in this circuit also depends on the amount of desired phase shift, or “bit” size. The greatest voltage stress is associated with the 180° bit and is reduced by the factor  $(\sin\theta/2)^{1/2}$  for other bit sizes. The relationship between maximum phase shift, transmitted power, and PIN diode ratings is as follows:

$$\theta_{\max} = 2\sin^{-1} \left( \frac{V_{BRF}}{8P_L} \right) \quad \text{radians (17)}$$

In comparison to the loaded line phase shifter, the hybrid design can handle up to twice the peak power when using the same diodes. In both hybrid and loaded line designs, the power dependency of the maximum bit size relates to the product of the maximum RF current and peak RF voltage the PIN diodes can handle. By judicious choice of the nominal impedance in the plane of the PIN diode, the current and voltage stress can usually be adjusted to be within the device ratings. In general, this implies lowering the nominal impedance to reduce the voltage stress in favor of higher RF currents. For PIN diodes, the maximum current rating should be specified or is dependent upon the diode power dissipation rating, while the maximum voltage stress at RF frequencies is dependent on I region thickness.

### PIN Diode Distortion Model

The beginning sections of this article were concerned with large signal operation and thermal considerations allowing the circuit designer to avoid conditions that would lead to significant changes in PIN diode performance or excessive power dissipation. A subtle, but often significant, operating characteristic is the distortion or change in signal shape, which is always produced by a PIN diode in the signal it controls.

The primary cause of distortion is any variation or nonlinearity of the PIN diode impedance during the period of the applied RF signal. These variations could be in the diode’s forward bias resistance,  $R_S$ , parallel resistance,  $R_P$ , capacitance,  $C_T$ , or the effect of the low frequency I-V characteristic. The level of distortion can range from better than 100 dB below, to levels approaching the desired signal. The distortion could be analyzed in a Fourier series and takes the traditional form of harmonic distortion of all orders, when applied to a single input signal, and harmonic intermodulation distortion when applied to multiple input signals.

Nonlinear, distortion-generating behavior is often desired in PIN and other RF oriented semiconductor diodes. Self-biasing limiter diodes are often designed as thin I region PIN diodes operating near or below their transit time frequency. In a detector or mixer diode, the distortion that results from the ability of the diode to follow its I-V characteristic at high frequencies is exploited. In this regard, the term “square law detector” applied to a detector diode implies a second order distortion generator. In the PIN switch circuits discussed at the beginning of this article, and the attenuator and other applications discussed here, methods of selecting and operating PIN diodes to obtain low distortion are described.

There is a common misconception that minority carrier lifetime is the only significant PIN diode parameter that affects distortion. This is indeed a major factor but another important parameter is the width of the I region, which determines the transit time of the PIN diode. A diode with a long transit time will have more of a tendency to retain its quiescent level of stored charge. The longer transit time of a thick PIN diode reflects its ability to follow the stored charge model for PIN diode resistance according to:

$$Q = I_F \tau \quad \text{coulombs (18)}$$

$$R_S = \frac{W^2}{(\mu_p + \mu_n)Q} \quad \Omega \quad (19)$$

where:

$I_F$  = forward bias current

$\tau$  = carrier lifetime

$W$  = I region width

$\mu_n$  = electron mobility

$\mu_p$  = hole mobility

The effect of carrier lifetime on distortion relates to the quiescent level of stored charge induced by the DC forward bias current and the ratio of this stored charge to the incremental stored charge added or removed by the RF signal.

The distortion generated by a forward biased PIN diode switch has been analyzed and has been shown to be related to the ratio of stored charge to diode resistance and the operating frequency. Prediction equations for the second order intermodulation intercept point (IP2) and the third order intermodulation intercept point (IP3) have been developed from PIN semiconductor analysis and are presented as follows:

$$IP2 = 34 + 20 \log \frac{FQ}{R_S} \quad \text{dBm (20)}$$

$$IP3 = 21 + 15 \log \frac{FQ}{R_S} \quad \text{dBm (21)}$$

where:

$F$  = Frequency in MHz

$R_S$  = PIN diode resistance in  $\Omega$

$Q$  = Stored charge in nC

In most applications, the distortion generated by a reversed biased diode is smaller than forward biased generated distortion for small or moderate signal size. This is particularly the case when the reverse bias applied to the PIN diode is larger than the peak RF voltage, preventing any instantaneous swing into the forward bias direction.

Distortion produced in a PIN diode circuit may be reduced by connecting an additional diode in a back-to-back orientation (cathode to cathode or anode to anode). This results in a cancellation of distortion currents. The cancellation should be total, but the distortion produced by each PIN diode is not exactly equal in magnitude and opposite in phase. Approximately 20 dB distortion improvement may be expected by this back-to-back configuration.

### Distortion in Attenuator Circuits

In attenuator applications, distortion is directly relatable to the ratio of RF to DC stored charge. In such applications, PIN diodes operate only in the forward bias state, and often at high resistance values where the stored charge may be very low. Under these operating conditions, distortion will vary with charges in the attenuation level. Thus, PIN diodes selected for use in attenuator circuits need be chosen only for their thick I region width, since the stored charge at any fixed diode resistance,  $R_S$ , is dependent only on this dimension.

Consider an SMP1304-001 PIN diode used in an application where a resistance of 50  $\Omega$  is desired. The data sheet indicated that 1 mA is the typical diode current at which this occurs. Since the typical carrier lifetime for this diode is 1  $\mu$ s, the stored charge for the diode at 50  $\Omega$  is 1.0 nC. If two PIN diodes, however, are inserted in series to achieve the same 50  $\Omega$  resistance level, each diode must be biased at 2 mA. This results in a stored charge of 2 nC per diode, or a net stored charge of 4 nC. Thus, adding a second diode in series multiplies the effective stored charge by a factor of 4. This would have a significant positive impact on reducing the distortion produced by attenuator circuits.

## Measuring Distortion

Because distortion levels are often 50 dB or more below the desired signal, special precautions are required in order to make accurate second and third order distortion measurements. One must first ensure that the signal sources used are free of distortion and that the dynamic range of the spectrum analyzer employed is adequate to measure the specified level of distortion. These requirements often lead to the use of fundamental frequency bandstop filters at the device output, as well as preselectors to clean up the signal sources employed. In order to establish the adequacy of the test equipment and signal sources for making the desired distortion measurements, the test circuit should be initially evaluated by removing the diodes and replacing them with passive elements. This approach permits one to optimize the test setup and establish basic measurement limitations.

Since harmonic distortion appears only at multiples of the signal frequency, these signals may be filtered out in narrow band systems. Second order distortion, caused by the mixing of two input signals, will appear at the sum and difference of these frequencies and may also be filtered. As an aid to identifying the various distortion signals seen on a spectrum analyzer, it should be noted that the level of a second distortion signal will vary directly at the same rate as any change of input signal level. Thus, a 10 dB signal increase will cause a corresponding 10 dB increase in second order distortion.

Third order intermodulation distortion of two input signals at frequencies  $F_A$  and  $F_B$  often produce in-band, nonfilterable distortion components at frequencies of  $2F_A - F_B$  and  $2F_B - F_A$ . This type of distortion is particularly troublesome in receivers located near transmitters operating on equally spaced channels. In identifying and measuring such signals, it should be noted that third order distortion signal levels vary at twice the rate of change of the fundamental signal frequency. Thus, a 10 dB change in input signal will result in a 20 dB change of the third order signal distortion power observed on a spectrum analyzer.

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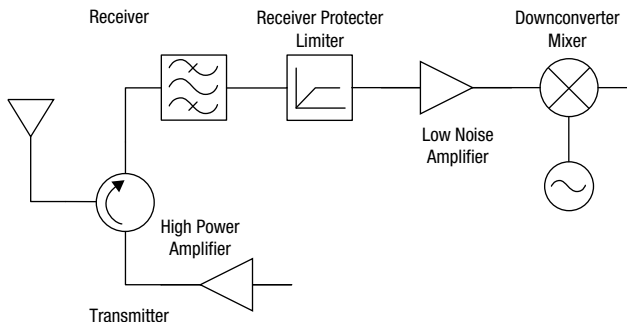
## APPLICATION NOTE

# PIN Limiter Diodes in Receiver Protectors

## Introduction

Radio and radar receivers must be capable of processing very small signals, necessitating the use of very sensitive circuit blocks that can contain fragile semiconductors. Many of these systems must also be capable of surviving very large incident signals, without damage to the sensitive components they contain. The receiver protection limiter, most often referred to simply as a limiter, can protect the receiver from large input signals and also allow the receiver to function normally when these large signals are not present.

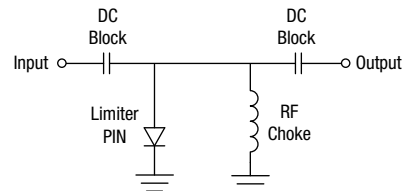
Limiters are most often employed in radar transceivers, whose transmitters and receivers are tuned to the same frequency. The transmitter produces a signal, the peak level of which is in most systems in the kilowatts or megawatts order of magnitude, which is applied to an antenna that is typically also utilized by the receiver. The receiver must be capable of reliably detecting and processing very weak reflected signals, so it has a sensitive, low noise amplifier (LNA) at its input, although some receivers apply the received signal directly to the input of a downconverter mixer. Both of these circuit blocks employ sensitive semiconductor components that will very likely be damaged by even a small portion of the transmitter signal that might be coupled to the receiver input, either by reflection from the antenna or by other means. A limiter can protect these components.



**Figure 1. Simplified Radar Transceiver with a Receiver Protector Limiter**

## A Simple Limiter Circuit

A simple, passive receiver protection limiter is shown in Figure 2. In its most fundamental form, this circuit consists of a PIN diode and an RF choke inductor, both of which are in shunt with the main signal path. In most limiter circuits, DC blocking capacitors are included at the input and the output of the circuit. A single-stage limiter can typically reduce the amplitude of a large input signal by 20–30 dB.

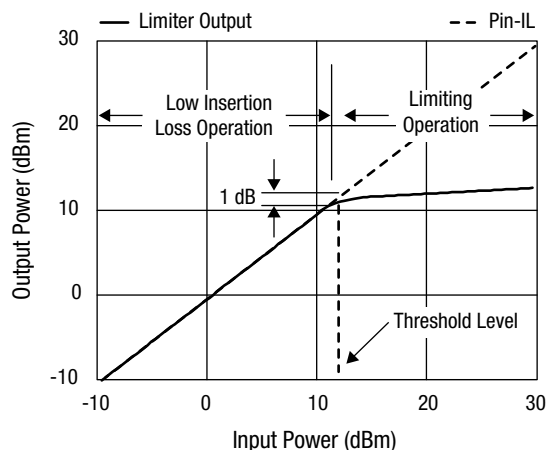


**Figure 2. A Single-Stage Limiter**

The PIN limiter diode can be described as an incident power-controlled, variable resistor. In the case when no large input signal is present, the impedance of the limiter diode is at its maximum, thereby producing minimum insertion loss, typically less than 0.5 dB. The presence of a large input signal temporarily forces the impedance of the diode to a much lower value, producing an impedance mismatch which reflects the majority of the input signal power back towards its source. A nominal transfer curve for a limiter stage is shown in Figure 3.

When the large input signal is no longer present, the impedance of the diode reverts from a very low value to its maximum value after a brief delay elapses. The limiter diode and its environment determine the duration of this delay.



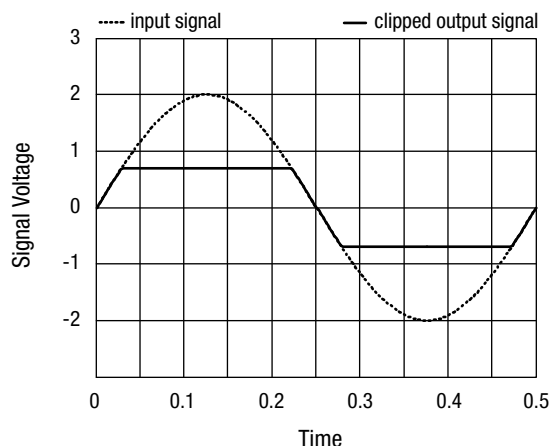


**Figure 3. Output Power vs. Input Power for a Single-Stage Limiter**

It is important to note that when a large input signal is present, the limiter diode reflects rather than dissipates the majority of the input signal power. In a properly designed circuit, a limiter diode that is capable of safely dissipating only a few hundred milliwatts is also capable of protecting a receiver from signals many orders of magnitude larger, without damage to the limiter diode. Of course, this is based upon the assumption that the reflected signal is either re-radiated from the system antenna, or is directed by a non-reciprocal device, such as a circulator or an isolator, to a resistive load that can dissipate the reflected signal power.

### Clipper (Limiter) Circuit

Note that the PIN limiter circuit operates differently from another class of limiter, known as a “clipper,” an example of which is shown in Figure 4. In that type of circuit, two rectifying diodes (which could be Schottky or PN junction diodes) are utilized to limit the peak voltage of the positive and negative signal alternations, either referenced to ground or to some arbitrarily selected DC level. This circuit, in this case with the rectifier diodes connected to ground, allows signals whose amplitudes are less than the cut-in voltage of the rectifier diodes to pass unchanged. Signals whose voltage amplitudes are larger than the cut-in voltage of the rectifying junction will force the diode into conduction. In this case, the voltage drop across the diode is approximately 0.7 V for a Si PN diode, so the peak voltage of the alternation that forward biases the diode is clamped to within a forward voltage drop of the potential to which the diode is connected. Note that the output signal is no longer purely sinusoidal—plentiful harmonics of the input signal can be generated by clipper circuits.



**Figure 4. Clipper Circuit and Large Signal Input/Output Waveforms**

Clipper circuits are typically used for low-frequency applications, nominally at VHF and below, since the stored charge of the rectifier diodes limits rectification efficiency at higher frequencies. This type of limiting circuit is often found in frequency modulation or phase modulation receiver IF amplifier sections.

In the “grey area” where the frequency of a signal is at the higher end of the range where clippers are useful, but at the lower end of the range where a PIN limiter circuit (as shown in Figure 2) is utilized, an antiparallel pair of PIN diodes, such as SMP1330-005<sup>(1)</sup>, can be used in the clipper circuit shown in Figure 4. In the lower UHF band, this circuit will act as a hybrid of the clipper and the incident-power-controlled, variable resistor limiter.

1. Data sheet available at [www.skyworksinc.com](http://www.skyworksinc.com)

Description of the PIN Limiter Diode

The cross-sectional diagram of a typical mesa PIN limiter diode die is shown in Figure 5.

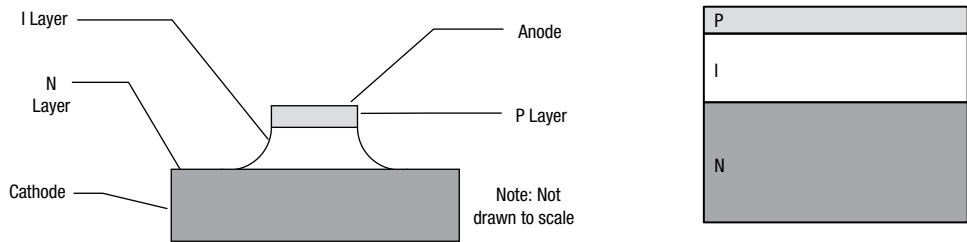


Figure 5. Cross-Sectional Views of a Limiter PIN Diode Die (Left) and Its Cylindrical Section Approximation (Right)

When a large input signal is incident upon the limiter PIN diode, the electric field of the signal temporarily forces positive charge carriers (holes) from the diode P layer and negative charge carriers (electrons) from the diode N layer into the nominally undoped, high impedance I layer, causing the impedance of the diode to be temporarily reduced to a much lower value.

The minimum and maximum impedances of the limiter PIN diode are determined by the geometry of the diode as well as the resistivity of the diode’s I layer. In the simplest approximation, the PIN diode can be modeled as a right cylindrical section with three separate layers: the P layer, the I layer and the N layer, where the resistance of each layer is given by

$$R_{\text{LAYER}} = \frac{p_{\text{LAYER}} \times \text{Thickness}_{\text{LAYER}}}{\text{Area}_{\text{LAYER}}}$$

where  $p_{\text{LAYER}}$  is the resistivity of the layer.

P Layer

The P layer is heavily doped with P-type acceptor impurities. It is typically quite thin, so its resistance is sufficiently small (of the order of a few mΩ) that it is ignored in most analyses.

N Layer

The N layer is sometimes called the N<sup>+</sup> layer because it is very heavily doped with N-type donor impurities. Its thickness is generally the largest of the three diode layers, so while its resistivity is small, its resistance is large enough that it should not be ignored. The resistance of this layer is most often of the order of tenths of an ohm. The electrical resistance of this layer is a major constituent of the minimum impedance of the limiter PIN diode. The N layer is also a significant element of the diode thermal impedance.

I Layer

The I layer that is sandwiched between the P and the N layers is “where the action is” for a PIN diode. This layer is nominally undoped (“I” stands for “intrinsic”), but in actual practice it is very lightly doped with N-type donor impurities. In the state when no external forward bias is applied to the diode, the resistivity of this layer is of the order of a few hundred Ω-cm or more, so the resistance it produces can be in the many hundreds to few thousands of ohms.

The resistance of the I layer can be modulated by forcing charge carriers into it from the P and N layers, simply by applying a forward bias voltage or current to the diode. The resistance of the I layer is exponentially indirectly proportional to the current flowing through the diode, that is, it can be described by

$$R_{\text{ILAYER}} = k \times I^{-\alpha} + R_{\text{BULK}}$$

where

- $R_{\text{ILAYER}}$  is the series resistance of the I layer of the diode
- $k$  is a constant, which is equal to the  $R_{\text{ILAYER}}$  of the diode when  $I = 1 \text{ mA}$ , assuming  $I$  is also expressed in mA
- $I$  is the current through the diode, expressed in mA, assuming  $k$  is also expressed in mA
- $\alpha$  is a curve fitting factor which is related to the slope of the  $R_{\text{ILAYER}}$  vs.  $I$  curve for the diode. For a typical PIN diode,  $0.84 \leq \alpha \leq 0.9$
- $R_{\text{BULK}}$  Saturated resistance of the I layer

It is also possible to express the resistance of the I layer in terms of its physical properties and bias current:

$$R_{I-LAYER} = \frac{w^2}{2 * I_F * \mu_A * T_L}$$

where

$R_{I-Layer}$	is the series resistance of the I layer of the diode
$w$	is the thickness of the I layer
$I_F$	is the bias current through the diode
$\mu_A$	is ambipolar carrier mobility, $\mu_A = (\mu_N + \mu_P)/2$ , where $\mu_N$ and $\mu_P$ are the carrier mobilities of electrons and holes, respectively
$T_L$	is the minority carrier lifetime

From this we can see that I layer resistance and minority carrier lifetime are indirectly proportional to each other.

The shape and resistivity of this layer determine the minority carrier lifetime of the diode. The thickness and doping concentration of the I layer determine reverse breakdown voltage and the threshold level of the diode; more about these important parameters later.

### Total PIN Diode Resistance, $R_S$

The total resistance of a PIN diode is equal to the sum of the resistances of the P, I and N layers, since they are electrically in series. The resistances of the P and N layers are constants. For non-zero bias current, the total series resistance of a PIN diode is

$$R_S = R_{I-LAYER} + R_{P-LAYER} + R_{N-LAYER} = K * I^{-\alpha} + R_{SAT}$$

The three constant terms,  $R_{BULK}$ ,  $R_{P-LAYER}$  and  $R_{N-LAYER}$ , are typically lumped together and referred to as  $R_{SAT}$ .

### Power Dissipation

The power dissipated by a PIN diode in conduction is the sum of a DC and an AC term: the product of the DC current and the DC forward voltage; and, the product of the square of the RF current and series resistance of the diode. Since the DC component of the dissipated power is typically quite small (of the order of a few mW), it is often ignored. The RF currents in a limiter PIN diode can be large, so the AC term dominates the total power dissipation.

$$P_{DISS} = I_{DC} * V_{DC} + I_{RF}^2 * R_S \approx I_{RF}^2 * R_S \quad (\text{conducting state})$$

The PIN diode can also dissipate power when it is not conducting. In this state, dissipated power is given by

$$P_{DISS} = \frac{V_{RF}^2}{R_S} \quad (\text{non-conducting state})$$

Since a passive limiter PIN diode is not in conduction when very small RF voltages are present,  $R_S$  remains large while  $V_{RF}$  is small; power dissipation in this state is negligible.

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**NOTE:** This may not be the case for a PIN diode used as a switch for high power signals.

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### Threshold Level

The threshold level for a limiter PIN diode is defined as the input signal level at which the diode is 1 dB into compression. That is, the input signal level at which the insertion loss, due to the reduction of the diode's impedance resulting from the presence of a large RF signal, is 1 dB greater than that when a very small signal is incident upon the diode. The threshold level is primarily determined by the thickness of the I layer of the diode: they are directly proportional to each other. The thinnest practical limiter PIN diode has a nominal I layer thickness of 1  $\mu\text{m}$ . Such a diode has a threshold level of approximately 7–10 dBm in a 50  $\Omega$  system. The thickest commercially available PIN limiter diodes have I layer thickness around 7 to 10  $\mu\text{m}$ , with threshold levels of around 20–23 dBm. Limiter PIN diodes with I layer thicknesses between these values are available, with corresponding threshold levels.

### Minority Carrier Lifetime

Minority carrier lifetime,  $T_L$ , is defined as the mean time that a free charge carrier exists before recombination occurs. It is also determined by characteristics of the I layer of a PIN diode: it is directly proportional to the volume of the I layer, but is slightly reduced by larger ratios of the I layer outer surface to I layer volume, and is directly proportional to the resistivity of the I layer. Small minority carrier lifetime of a limiter PIN diode is generally desirable because it is proportional to the brief delay between the cessation of a large RF signal across the diode and the reversion of the diode's impedance to its maximum value. The I layer of a limiter PIN diode is doped with gold atoms to establish charge trapping sites, thereby substantially reducing minority carrier lifetime, which is desirable for radar receiver protectors and other applications such as EW receivers. But, we have already seen that the minority carrier lifetime and series resistance of a PIN diode are indirectly proportional to each other; these two characteristics must be balanced against each other for optimal limiter performance.

Minority carrier lifetime is related to limiter recovery time, which is a very important characteristic of a limiter that will be discussed in more detail later.

## Junction Capacitance

The capacitance of the PIN limiter diode affects the small signal insertion loss of the diode. Capacitance is given by the familiar equation

$$C_J = \frac{\epsilon \times A}{d}$$

where

- $C_J$  is the junction capacitance of the diode
- $\epsilon$  is the dielectric constant of the I layer, where  $\epsilon = \epsilon_0 \epsilon_R$ , the product of the dielectric constant of free space and the relative dielectric constant of the material comprising the I layer
- $A$  is the area of the junction of the diode
- $d$  is the thickness of the depletion layer

So, it is clear from the discussions of threshold level, resistance, capacitance and minority carrier lifetime that the design of a PIN limiter diode is an exercise in tradeoffs: adjusting I layer thickness and junction area to determine junction capacitance and series resistance, while maintaining I layer thickness to meet requirements for a given threshold level; and looking at I layer volume, shape and doping to minimize minority carrier lifetime without deleteriously affecting series resistance and junction capacitance.

## Avalanche Breakdown Voltage

Avalanche breakdown voltage is the reverse bias voltage at which “a breakdown is caused by the cumulative multiplication of charge carriers through field-induced impact ionization”<sup>(2)</sup>. For RF and microwave diodes, reverse breakdown voltage is most often defined to be the voltage required to force 10  $\mu$ A of current to flow in the reverse-bias direction. The minimum rated breakdown voltage can be considered to be the absolute maximum reverse voltage that should be applied to the diode, unless otherwise noted in the manufacturer’s specifications.

Direct measurement of the avalanche breakdown voltage of a PIN diode is not recommended. The avalanche breakdown condition can very easily cause catastrophic damage to a PIN diode. Under reverse bias, the resistivity of the I layer is maximum, so driving

a charge carrier through this region requires a very large electric field, typically of the order of 10 to 20 V per  $\mu$ m of thickness. Since the crystal structure of this region inevitably has discontinuities (remember the Au doping and the fact that during wafer processing the Si has been subjected to many processing steps, many of which can induce strain in the semiconductor crystal), when avalanche breakdown starts to occur, the current density through the I layer is not distributed equally but is concentrated in some regions, which are referred to as “filaments.” The current densities in these filaments can be so large that the localized heating raises the temperature in these volumes to the point that diffusion of the P-type and N-type dopants from the P and N layers, respectively, into the I layer occurs. These filaments of dopants can extend through the entire thickness of the I layer, forming permanent short circuits. This process happens slowly enough, on a tenths-of-a-second scale, that it can be observed on a curve tracer. The diode will briefly produce the well-known diode I-V curve until filamentary diffusion shorts the I layer so that the curve shown on the curve tracer snaps to one that looks very much like that of a small-value resistor.

## Thermal Impedance

The thermal impedance of a limiter diode is quite important, since it is well known that the serviceable life of a semiconductor is reduced exponentially as operating junction temperature increases. Even though in normal operation a limiter diode will dissipate only a small portion of the RF power incident upon it, that small portion can be appreciable. This power is converted from electrical energy to heat in the diode by Joule heating, primarily in the diode’s I and N layers, since that is where the majority of the resistance of the diode resides.

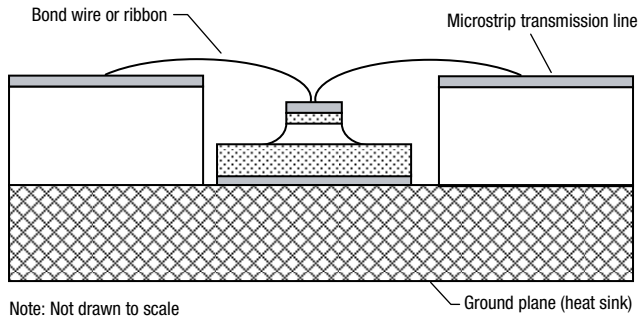
## Thermal Resistance

It is well known that there are three means by which heat can flow from a region of high temperature to regions of lower temperature: convection, radiation and conduction. Convection and radiation of heat from a diode die are negligible and are typically assumed to not contribute to the removal of heat from the diode.

Conduction of the heat generated in the I layer and at the pn junction (the interface between the heavily doped, P-type P layer and the lightly doped, N-type I layer) is through the cathode layer, which is typically the thickest layer of the diode. The electrical connection to the anode of the diode is made using a circular-cross-section wire (typically 0.0007 inches [17.8  $\mu$ m] diameter) or a rectangular-cross-section ribbon (typically 0.00025 x 0.003 inches [6.35  $\mu$ m x 76.2  $\mu$ m]). The cross-sectional area of each of these conductors is sufficiently small that conduction of heat through this path is also considered to be negligible<sup>(3)</sup>.

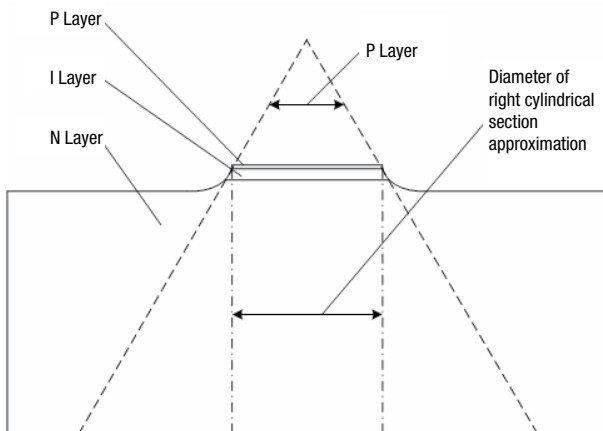
2. “IEEE Standard Dictionary of Electrical and Electronics Terms,” IEEE, Second Edition, 1977, p. 45.

3. A. W. Davis, “Microwave Semiconductor Circuit Design,” Van Nostrand Reinhold Co., 1984, p. 160.



**Figure 6. Cross Section of a Shunt PIN Limiter Diode in a Microstrip System**

Rigorous calculation of thermal impedance for a diode can be quite involved. However, if we make some simplifying assumptions, we can reduce this calculation to a more manageable problem. Heat flows from a point source in conical section whose major angle is roughly  $60^\circ$ . If we assume nominal dimensions for a limiter PIN diode with a mesa, and that the heat is generated at the interface between the P and I layers, as long as a  $60^\circ$  conical section whose minor diameter is the circumference of the P-I interface is completely contained within the diode, then we simplify the analysis to assume that all heat flows from the diode through a right cylindrical section whose diameter is also equal to the diameter of the P-I interface as shown in Figure 6. This assumption is valid for virtually all commercially available limiter diodes. This analysis will predict a thermal resistance somewhat larger than that which is actually produced by the entire volume of the conic section, but this over-estimation of thermal resistance is often offset by overly optimistic assumptions about other thermal impedances within the system.



**Figure 7. Cross Section of a Shunt PIN Limiter Diode in a Microstrip System**

The thermal resistance from junction to heat sink,  $\theta_{JC}$ , is given by

$$\theta_{JC} = \frac{L}{G_{THERMAL} \times A}$$

where

- $\theta_{JC}$  = Thermal resistance from junction to heat sink
- $L$  = Length of thermal conduction path (approximately the combined thickness of the I and N layers of a limiter PIN diode)
- $G_{THERMAL}$  = Thermal conductivity of the material in the thermal path (for Si,  $0.84 \text{ W/(cm}^\circ\text{C)}$ )<sup>(4)</sup>
- $A$  = Cross-sectional area of the right cylindrical section assumed to be path for heat flow

## Thermal Capacitance

A finite period of time is required for heat to flow out of the diode. During this time, the temperature of the diode increases as the heat propagates from the junction to the die attach interface to the heatsink. Thermal capacitance,  $C_{THERMAL}$ , also known as heat capacity, is defined as the amount of energy required to raise the temperature of the diode I layer by  $1^\circ\text{C}$ , in the absence of heat flow from the diode<sup>(5)</sup>. Thermal capacitance is given by

$$C_{THERMAL} = \frac{(\text{Specific\_Heat} \times \text{Density})}{\text{Volume}}$$

where

- $C_{THERMAL}$  = Thermal capacitance
- Specific Heat = Specific heat of Si =  $0.176 \text{ cal/(g }^\circ\text{C)}$
- Density = Density of Si =  $2.43 \text{ g/cm}^3$
- Volume = I & N layer volumes =  $(\pi \times \text{radius}_{I\text{ LAYER}}^2) / (\text{thickness}_{I\text{ LAYER}} + \text{thickness}_{N\text{ LAYER}})$

## Thermal Time Constant

The thermal time constant of a limiter diode can be used to understand how the junction temperature of a limiter diode changes over time. It is important since the diode will not reach its final, steady state temperature until approximately 6 thermal time constants,  $\tau_{THERMAL}$ , have elapsed, assuming a constant amplitude input signal. For signal bursts of briefer duration, junction temperature may reach a peak value less than that it would reach for much longer bursts.

4. "Reference Data for Radio Engineers," Howard W. Sams & Co., Sixth Edition, 1975, p. 4-13.  
5. J. F. White, "Microwave Semiconductor Engineering," J. F. White Publications, 1995, p. 106.

Thermal time constant is the analog of electrical time constant. It is the product of thermal resistance and thermal capacitance.

$$\tau_{\text{THERMAL}} = \theta_{\text{JC}} \times C_{\text{THERMAL}}$$

The junction temperature of a limiter diode versus time is given by

$$T_J = T_{\text{HEATSINK}} + \Delta T_J$$

where

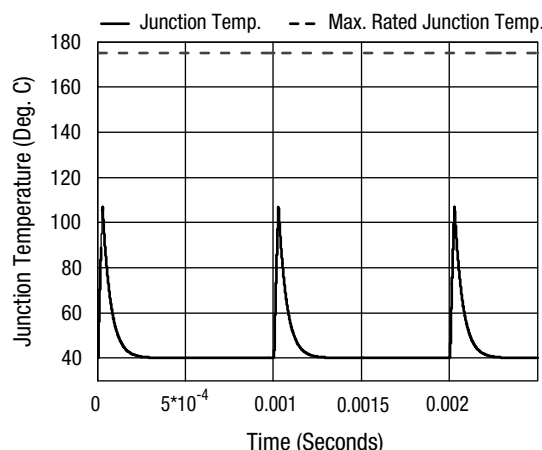
$$\Delta T_J = P_{\text{DISSIPATED}} \times \theta_{\text{JC}} \left( 1 - e^{\frac{-t}{\tau_{\text{THERMAL}}}} \right)$$

Since the heat sink in a typical system is not infinite, rigorous analysis should include the thermal resistances and capacitances of the remainder of the system, such as that of the die attach medium, system ground plane, system housing, etc.

### $T_J$ vs. Time

Consider a series of RF bursts incident upon a typical limiter diode, such as CLA4606-000. The thermal resistance of the diode is 80 °C/W, the diode's P layer diameter is 63.5 µm, its I layer is 2.5 µm thick and its N layer is 100 µm thick. Also assume that the peak dissipated power in the diode is 2 W, the duration of each RF burst (sometimes called the "pulse width") is 25 µs at 2.5% duty cycle and the die attach surface is maintained at 40 °C.

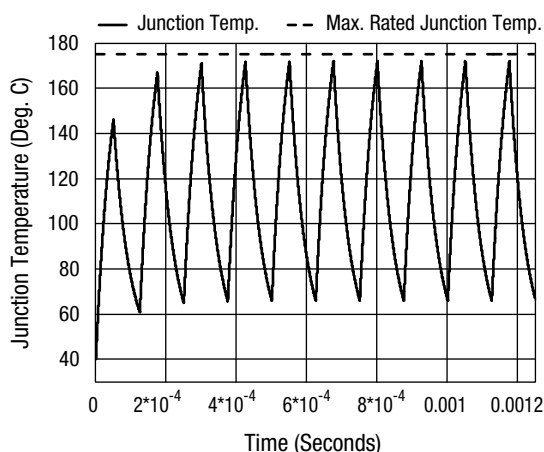
If the input signal were continuous wave (CW), the junction temperature would seriously exceed the maximum rated temperature, and the diode would consequently be destroyed. The thermal capacitance of this diode is 57.6 µJ/°C, so the thermal time constant is  $\tau_{\text{THERMAL}} = 46 \mu\text{s}$ . Since  $6 \times \tau_{\text{THERMAL}}$  is substantially longer than the burst duration, we can expect that the junction temperature of diode will not reach the maximum possible temperature. The simulated junction temperature versus time for this set of conditions is shown in Figure 8.



**Figure 8. Diode Junction Temperature vs. Time, Duty Cycle = 10%**

We can see in Figure 8 that the peak diode temperature is approximately 107 °C, which is well under the rated maximum junction temperature of 175 °C. Notice that after each RF burst there is ample time for the  $T_J$  to recover to the die attach surface temperature before the next burst occurs. Under these signal conditions, the diode is not subjected to overstress.

Assume the duty cycle increases to 40% and the burst duration increases to 50 µs. In this case, the diode is capable of handling peak power dissipation of only 2 W, in which case the peak  $T_J$  climbs alarmingly close to that maximum rated temperature. We can see in Figure 9 that the junction temperature does not recover to the temperature of the die attach surface before the start of the next burst, so the  $T_J$  for the diode follows a stair-step-like curve, until the peak  $T_J$  finally reaches its steady state value of approximately 172 °C at the end of the third RF burst. At that point, the average  $T_J$  is approximately 120 °C.

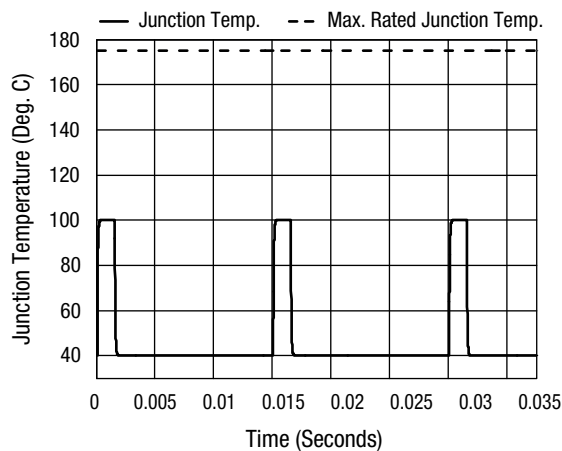


**Figure 9. Diode Junction Temperature vs. Time, Duty Cycle = 50%**



Finally, consider the case where the RF burst duration is longer than  $6\tau_{\text{THERMAL}}$ . The plot in Figure 10 shows the junction temperature versus time for an input RF burst duration of 1.5 ms and 10% duty cycle, but with the diode dissipating 750 mW peak. Notice that the diode reaches its peak junction temperature and remains there for a substantial interval, so the fact that the signal is bursted rather than CW is not significant. The analysis of the thermal conditions for this case must be performed as if the input signal were CW, rather than a sequence of bursts.

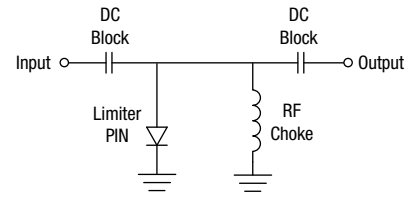
In summary, the physical properties of the diode determine its thermal time constant (product of thermal resistance and thermal capacitance), which must be compared against the duration of the pulse which heats the diode in order to determine how much power the diode can safely dissipate without overheating.



**Figure 10. Diode Junction Temperature vs. Time,  
Burst Width = 1.5 ms, Duty Cycle = 10%**

## The Limiter Circuit

A typical, single-stage limiter circuit is shown in Figure 11. When a small signal, such as the input signal to a receiver, is incident upon the diode, the electric field of this signal is not large enough to force carriers into the I layer of the diode so its resistance remains high. The insertion loss of the diode in this state is primarily the mismatch loss produced by the capacitive reactance of the diode's junction capacitance. The inductor, which is present to complete the required DC circuit path, is chosen to have a sufficiently large reactance and out-of-band series resonance so that it also produces negligible in-band reflection loss.



**Figure 11. A Single-Stage Limiter**

## The Leading Edge of an RF Signal Burst

Consider what happens at the leading edge of a large signal RF burst incident upon the diode. The electric fields produced by this signal will force charge carriers into the I layer of the diode, reducing its series resistance. The series resistance of the I layer changes from its maximum value to its minimum value, assuming the amplitude of the input RF signal is sufficiently large. The low impedance of the limiter diode causes a large impedance mismatch to the transmission line, thereby reflecting almost all of the input signal power back towards the source.

Initially, when the diode is still in its high impedance state, virtually all of the input signal power passes by the diode limiter, only attenuated by the small mismatch loss from the diode's capacitance. After sufficient time has passed for the impedance of the diode to reduce to its minimum, which is approximately the carrier transit time across the I layer, the input power is attenuated by the isolation produced by the diode's low impedance. The isolation produced by

$$\text{Isolation} = 20 \log \left( \frac{Z_0}{2 \times R} \right)$$

The maximum output power from the diode is called "spike leakage." The power level out of the diode after it has changed to its low impedance is called "flat leakage." It is important to select a limiter diode such that the energy that propagates past the limiter during the output spike is sufficiently small that no damage to the following receiver stages will occur.

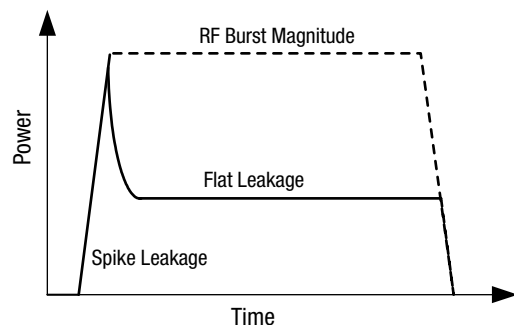


Figure 12. Limiter Input and Output Power vs. Time

As implied above, even after the limiter diode has reached its low impedance state a small portion of the input signal is not reflected back to its source. Some of this energy propagates past the limiter stage to the limiter circuit's load. The balance of the input energy is dissipated by the diode, due to the Joule heating produced by the RF signal voltage across the diode's resistance. The amount of power that propagates to the load is typically 2–4 dB larger than the threshold level of the diode, again assuming the incident signal is much larger than the input threshold level. This is the case for increasing RF signal levels, until the series resistance of the limiter PIN reaches its minimum value.

If the input signal amplitude increases further, then the output power from the limiter will also increase on a dB-for-dB basis, since the finite, non-zero minimum impedance of the diode remains fixed at approximately  $R_{SAT}$ . Consequently, the reflection loss caused by the impedance mismatch also remains constant. The transfer function for a single-stage limiter is shown in Figure 13. For a practical limiter, the RF currents in the limiter diode when it is operating in its saturated mode can approach or exceed the value which will cause damage to the diode, so care should be taken to avoid operating with input signal levels that force the diode to operate well into its saturated mode region.

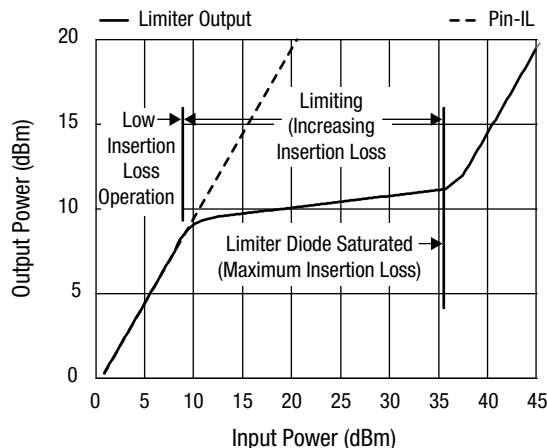


Figure 13. The Transfer Function for a Single-Stage Limiter

### After the RF Signal Burst—Recovery Time

At the end of the RF input signal burst and for a brief period thereafter, there are still free charge carriers present in the diode I layer, so its resistance remains low. During this interval, the limiter is still operating in its isolation state. In a radar transceiver this means that the receiver is essentially “blind” during this interval, even though the transmitter is no longer producing its high power RF burst. The sensitivity of the receiver is temporarily degraded during this interval, since reflected signals that might arrive from a target during this interval would be attenuated by the mismatch loss of the diode's very low impedance. Clearly, the operators of radar systems would like to see the duration of this condition to be as short as possible.

After completion of the RF burst there is no externally applied electric field to force these charge carriers to be conducted out of the I layer, so the primary mechanism to eliminate them and thereby allow the diode to revert to its high impedance, low insertion loss state is recombination of the negatively charged electrons with the positively charged holes. The time that this process takes is proportional to the minority carrier lifetime of the diode, so limiter PIN diodes are treated during wafer fabrication to reduce minority carrier lifetime, without adjusting I layer thickness or junction area. In most cases, this treatment consists of the addition of gold (Au) doping to the I layer by thermal diffusion<sup>(6)</sup>. The minority carrier lifetime of an Au-doped limiter diode with a 2  $\mu\text{m}$  thick I layer and a junction capacitance of 0.1 pF is approximately 5 ns. The same diode without Au doping would have minority carrier lifetime of 20 to 40 ns.

6. Platinum (Pt) has also been used as the I layer dopant, rather than gold, but this is generally not done in modern RF/microwave limiter diode fabrication.



## Multistage Limiters

We have seen how the electrical characteristics of a limiter PIN diode are determined by the diode's geometry and by the composition of its layers. The single-stage limiter can typically produce 20–30 dB of isolation, depending on the input signal frequency and the characteristics of the diode. In most cases, much more isolation is required to protect sensitive receiver components. Multistage limiters are used for such applications.

A two-stage limiter circuit is shown in Figure 14. The limiter PIN diode at the output, commonly referred to as the “clean-up stage,” is the diode with thinner I layer, selected so that the threshold level of the circuit is low enough to protect the remainder of the receiver components.

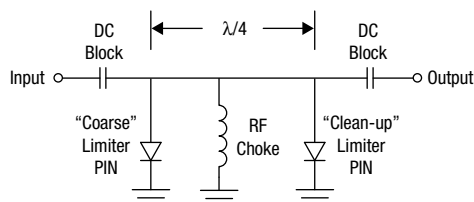


Figure 14. Two-stage limiter

The limiter diode at the input, often called the “coarse limiter,” has a thicker I layer for several reasons. The P layer diameter can be larger for a diode with a thicker I layer while maintaining a capacitance value that produces low insertion loss under small input signal conditions. This produces a diode series resistance that is often smaller than that of the clean-up diode, so the isolation of the coarse limiter can be larger than that of the clean-up stage. Thermal resistance of diodes typically used as coarse limiters can also be lower than that of clean-up-type diodes.

The placement of these stages with respect to each other is important. The coarse limiter is normally placed one-quarter wavelength ( $\lambda/4$ ), or an odd multiple of one-quarter wavelength, from the clean-up stage towards the signal source.

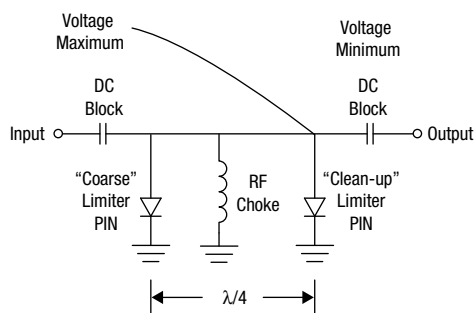


Figure 15. The Standing Wave in a Two-Stage Limiter

Under small signal conditions, both diodes are in their high impedance states, so the total insertion loss produced is a result of each diode's capacitance and the small mismatch loss they create.

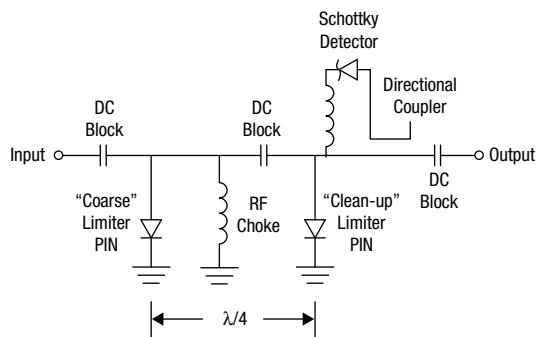
At the leading edge of a large RF signal burst, both diodes are initially in their high impedance state. Consequently, for a very brief period, the entire input signal amplitude, less the small insertion loss, propagates past the limiter. The impedance of clean-up stage changes first, since the carrier transit time across its thinner I layer is less than that of the coarse diode. This establishes a standing wave on the transmission line, with a voltage minimum at the low-impedance clean-up stage. Since the coarse limiter stage is spaced  $\lambda/4$  away, a voltage maximum occurs across it. This large voltage forces charge carriers into the coarse limiter I layer, thereby reducing its impedance. Consequently, the lower impedance of the coarse diode ultimately produces the majority of the overall limiting that takes place, while the clean-up stage determines the threshold level and spike leakage of the circuit.

For example, this circuit could be implemented with a 1.5  $\mu\text{m}$  clean-up diode, such as CLA4603-000, and a 7  $\mu\text{m}$  coarse limiter, such as CLA4607-000. The capacitance for each of these diodes is 0.2 pF maximum, and the maximum resistance specified with 10 mA forward bias current is 2  $\Omega$ . Since the coarse diode has a substantially thicker I layer, it can have a junction diameter twice that of the clean-up stage and still maintain low capacitance. This results in a much lower thermal resistance for the coarse stage (40  $^{\circ}\text{C/W}$ ) than for the clean-up stage (100  $^{\circ}\text{C/W}$ ), allowing it to handle larger input signals.

If the limiter is required to handle very large input signals, a third stage may be added at the limiter input, spaced another  $\lambda/4$  from the second diode, which now becomes known as the “intermediate limiter.” The new coarse limiter diode has an even thicker I layer diode than the intermediate stage limiter. The spike and flat leakage remain functions of the clean-up limiter I layer thickness, and the power handling and overall isolation a function of the characteristics of the three-diode cascade. More stages with increasingly thick I layers, spaced at  $\lambda/4$ , can be added at the input of the limiter as is required to handle extremely large signals, but most practical limiters are designed with 3 stages or less.

## Detector Limiters

The threshold level for the thinnest I layer diode available is approximately 7 dBm. Some extremely sensitive receiver components may be damaged by the spike leakage energy even at this level. The threshold level of the limiter circuit can be lowered arbitrarily by adding a Schottky detector diode and some passive components to the circuit, as shown in Figure 16.



**Figure 16. A Two-Stage Detector Limiter**

The Schottky diode is used as a peak (envelope) detector. It is coupled to the output of the limiter circuit, often via a directional coupler. The current produced by the Schottky detector is applied as a bias current to the clean-up stage, via an RF choke. The combination of the coupling factor of the directional coupler and the barrier height of the Schottky diode determines the threshold level of this circuit, which is typically in the 0 dBm range for most practical implementations.

## Conclusion

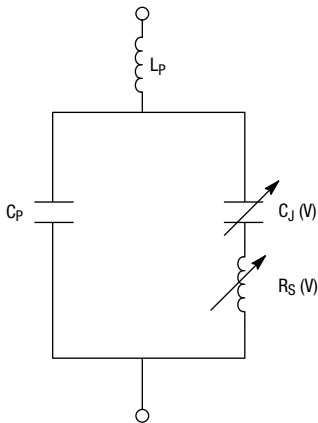
A limiter PIN diode is a three-layer device whose middle I layer is doped with Au to reduce minority carrier lifetime. The design of the diode, specifically I layer thickness, I layer resistivity and P-to-I-layer junction area is an exercise in trade-offs to produce the desired resistance, capacitance, recovery time and threshold level. The diode can be used as an input-power-controlled RF variable resistance to produce attenuation that is a function of the diode characteristics as well as the incident signal amplitude. The limiter circuit can consist of a single diode or multiple cascaded diodes separated by  $\lambda/4$ . Adding a directional coupler and Schottky detector diode to the system can lower threshold level.

## APPLICATION NOTE

# Varactor Diodes

### Introduction

A varactor diode is a P-N junction diode that changes its capacitance and the series resistance as the bias applied to the diode is varied. The property of capacitance change is utilized to achieve a change in the frequency and/or the phase of an electrical circuit. A simple model of a packaged varactor diode is shown below:



In the above figure,  $C_J(V)$  is the variable junction capacitance of the diode die and  $R_S(V)$  is the variable series resistance of the diode die.  $C_P$  is the fixed parasitic capacitance arising from the installation of the die in a package. Contributors to the parasitic capacitance are the package material, geometry and the bonding wires or ribbons. These factors also contribute to the parasitic inductance  $L_P$ . The contribution to the series resistance from the packaging is very small and may be ignored. Similarly, the inductance associated with the die itself is very small and may be ignored.

Variation of the junction capacitance and the junction series resistance as a function of applied reverse voltage is reported in the individual varactor data sheets of this catalog.

A common package configuration is to assemble two junctions in one package in a common cathode or common anode configuration. An empirical model for this dual configuration assumes the same value of parasitic capacitance in parallel with each junction die as for a single junction assembly. On the other hand, the parasitic inductance  $L_P$  may be assumed to be common for the assembly. For example, suppose two junctions

each with a junction capacitance of 0.5 pF ( $C_J = 0.5$  pF) are assembled together in one package which has a parasitic capacitance of 0.15 pF ( $C_P = 0.15$  pF) and a parasitic inductance of 0.5 nH ( $L_P = 0.5$  nH). The model for this case may be represented by two diodes with total capacitance of 0.65 pF each ( $C_J + C_P = 0.5 + 0.15$ ) in parallel or in series depending on the configuration. The inductance of 0.5 nH would appear in series with the entire assembly.

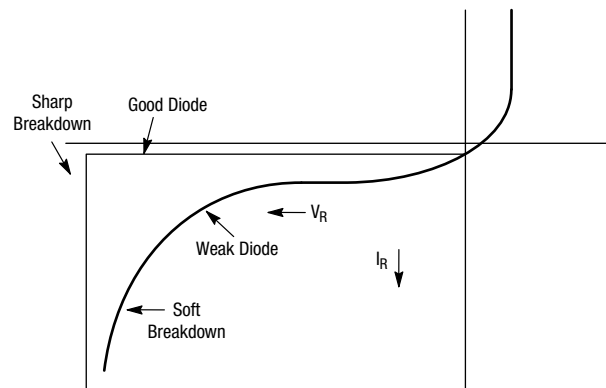
### Key Electrical Parameters

The key electrical parameters guiding the selection and usage of a varactor diode are

- Reverse breakdown voltage and reverse leakage current.
- Capacitance value and the capacitance-voltage change behavior.
- Quality factor (also known as figure of merit),  $Q$ .

### Reverse Breakdown Voltage and Reverse Leakage Current

The reverse breakdown voltage ( $V_B$ ) and the reverse leakage current ( $I_R$ ) are typically measures of the intrinsic quality of the semiconductor diode. Their effect on the frequency or phase tuning behavior is only indirect and of secondary importance. The IV characteristics of a good-quality diode and a weak diode are depicted in the following figure.



The reverse breakdown voltage is normally measured at 10  $\mu\text{A}$  of reverse leakage current. In a well-constructed diode, the breakdown occurs when the electric field across the diode reaches the limit that causes an avalanche of conductors through the diode. The breakdown voltage, therefore, defines the operating limit for the reverse bias across the diode. A rule of thumb is to specify the reverse breakdown voltage a minimum of 5 V above the maximum operating reverse DC voltage.

The breakdown voltage of the diode is determined by the density of dopants in the semiconductor. Higher dopant density translates into a lower breakdown voltage. An equally important factor determining the breakdown is the defect density (mostly an outcome of wafer fabrication processes). Hence, when a diode breakdown voltage is low, it could be either intentional in an effort to lower the resistance and increase the diode Q, or unintentional—simply an outcome of poor wafer processing. Because of this latter factor, a low breakdown voltage is not necessarily an indicator of a high diode Q. Therefore, it is not a good idea to specify an upper limit on breakdown voltage as a means of specifying high diode Q. It is better to specify directly a minimum acceptable limit on diode Q.

The reverse leakage current drawn by the diode is a direct measure of the diode quality as opposed to the reverse breakdown voltage. In a well-constructed varactor diode, depending on the geometry and the junction size, the leakage current can be less than a nanoampere to a couple of hundreds of nanoamperes. A larger leakage current is usually the result of excessive defects in the semiconductor that present shortcut passage for movement of electrons and holes.

As shown in Figure 1, a good quality diode draws a very small leakage current up to the avalanche breakdown point. A soft diode, on the other hand, draws a greater and greater leakage current as the bias applied to the diode is increased. The reverse leakage current is typically specified at 80 percent of the rated breakdown voltage.

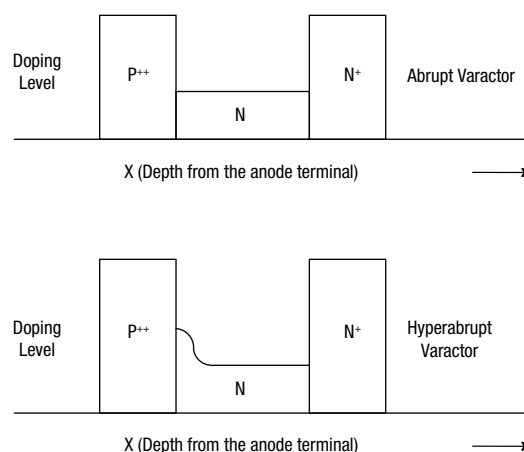
The reverse leakage current is also the best indicator of the diode stability through a stress cycle such as burn-in. Of all the measurable parameters, a shift in leakage current at a given bias voltage is the most sensitive measure of the diode's ability to withstand the burn-in stress.

The reverse leakage current of a varactor diode increases rapidly with temperature as the motion of carriers is enhanced by the thermal energy. A rule of thumb is that a fiftyfold increase in leakage current is obtained by an increase in temperature from 25 °C to 125 °C, or double the current for every 10 °C.

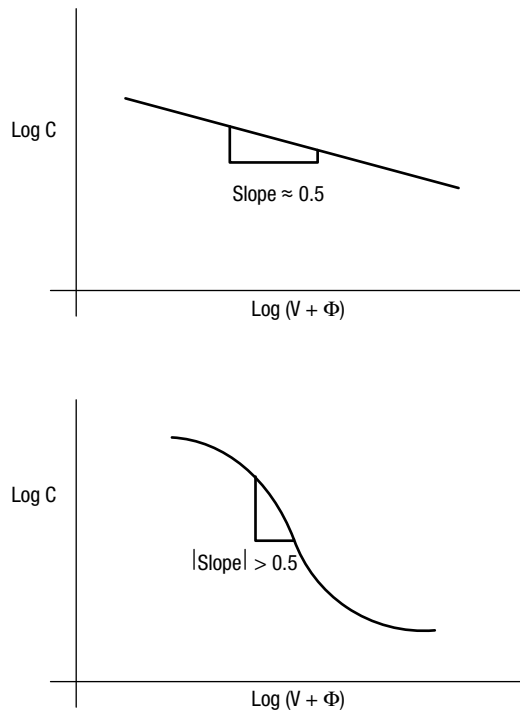
## Capacitance

The absolute capacitance of the varactor diode contributes to the total capacitance of the LC circuit in which it operates, and thus determines the frequency of operation. Additionally, the change of capacitance of a varactor diode with the change of applied reverse bias voltage is what governs the change of the frequency or the phase of the signal. Therefore, both parameters—the absolute capacitance value as well as the capacitance variation property—are extremely important for a user to understand.

The capacitance and the capacitance change characteristic are both functions of the doping structure introduced within the semiconductor during the wafer fabrication process. For example, note the difference in the doping characteristic of an abrupt and a typical hyperabrupt diode.



The difference translates into the following capacitance-voltage variation characteristic.



The slope of the log C vs. log V curve is typically denoted by gamma ( $\gamma$ ). For an ideal abrupt varactor diode, gamma is 0.5. However, a gamma of 0.47 is more representative of a practical abrupt varactor diode.

$$C = \frac{C_0}{(V/\Phi + 1)^{0.47}}$$

The value of built-in potential  $\Phi$  is 0.7 V for silicon and 1.3 V for gallium arsenide.

The modeling of the capacitance change of a hyperabrupt varactor is more complex. The slope of the log C vs. log  $(v + \Phi)$  curve typically varies with the applied reverse bias. Hence, a description of capacitance change with voltage in terms of gamma is an approximation at best. If the range of applied bias used is sufficiently narrow, then one may use an equation with an average value of gamma over that range. If the range of applied bias used is wide, then the common practice is to use a curve-fitting technique to generate a model. The user may refer to capacitance-voltage curves presented for each part type. These curves are based on actual data from a typical diode in each group. Please contact the factory should you need more detailed data on capacitance-voltage change for a specific diode type.

The capacitance of a varactor diode changes with temperature. Capacitance increases as the temperature increases and decreases as the temperature drops. The following empirical relationship may be used to predict the temperature coefficient of capacitance (ppm change in capacitance per degree C change in temperature).

$$T_{cc}(V) = \frac{1}{C(V)} \cdot \frac{dC(V)}{dT} \times 10^6$$

$$= \frac{K \cdot \gamma(V)}{(V + \Phi)}$$

The value of parameter K may be assumed to be 2,300 for an abrupt varactor and 1,700 for a hyperabrupt varactor.

It follows from the above equation that the higher the gamma, the higher the  $T_{CC}$ ; i.e., the higher the sensitivity of capacitance to voltage, the higher the sensitivity of capacitance to temperature. The capacitance of hyperabrupt diode is more sensitive to temperature in comparison to the abrupt diode. Additionally, hyperabrupt diodes with higher gamma (i.e., higher capacitance ratio) are more sensitive to temperature than the ones with relatively smaller gamma.

Capacitance values reported in this catalog are measured at 1 MHz. Numerous experiments have shown that the junction capacitance is constant with frequency. A 1 MHz capacitance bridge or meter must operate with a low signal voltage to avoid errors due to the nonlinear properties of the varactor. Typically, about 15 millivolts RMS is recommended. A balanced measuring circuit must be used so that stray capacitance to ground of the measurement setup will be negligible.

In any real, physical environment the electric fields across any capacitor fringe away from the active or dielectric material into the surrounding space and are terminated on nearby or remote conductors. This contributes to the fringe capacitance and is inherent to any capacitor. Some of this fringing is properly associated with the dielectric chip, as Figure 1 indicates. Clearly, the fringing fields shown here, because they exist (and cannot be reduced in any practical way) for all environments, are properly considered as part of the junction capacitance.

Let's now take the chip and mount it in one of the many metal-ceramic packages available.

We have added the following items:

1. A metal pedestal upon which the chip rests.
2. Bonding wires, or straps, to contact the top of the chip.
3. A ceramic envelope (almost always Alumina,  $\epsilon = 10$ ).
4. Various pieces of metal, copper or Kovar, to hermetically seal the package and provide mounting prongs.

We have also added capacitance:

1.  $C_S$ , from the straps to the pedestal and the base.
2.  $C_C$ , the ceramic capacitance.
3. More fringing  $C_F$  from the top of the package to the bottom and to the surrounding environment.

The strap and ceramic contributions are inherent to the package and are generally lumped together as  $C_P$ . The fringe capacitance, because it is dependent upon the exact method of mounting the package and the mechanical (conductive or dielectric) environment, is not inherent to the package and accordingly cannot be included in the diode specification. This capacitance is subject to control by the user, not the manufacturer.

Therefore, when the capacitance of the packaged tuning varactors is measured, a so-called fringe-free holder is used.

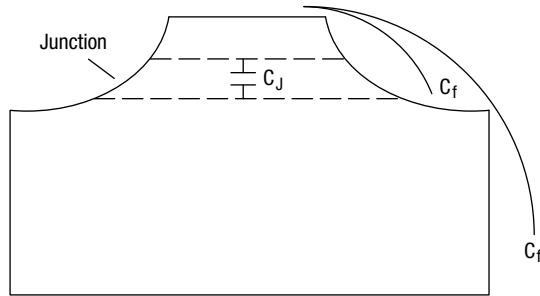


Figure 1. Inherent Chip Fringe Capacitance

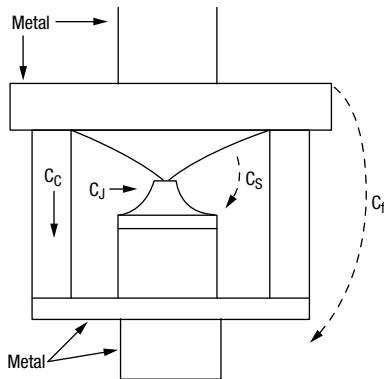


Figure 2. Stray Capacitance for Packaged Diodes

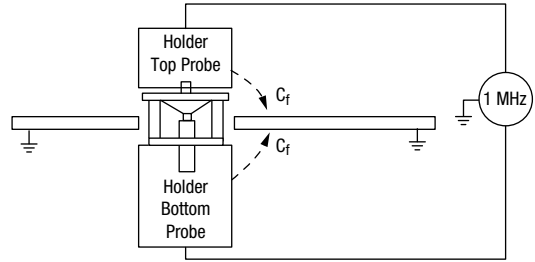


Figure 3. Fringe-Free Capacitance

We belabor this point because it is quite often a serious point of contention between customer and manufacturer, especially for low  $C_J$  varactors where theoretical capacitance ratios are often hard to obtain.

### Quality Factor (Q)

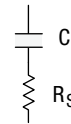
The Q factor, also known as the figure of merit and the quality factor, is an important parameter for a varactor diode since it determines the frequency limit applicability for the diode.

The classical definition of the Q of any device or circuit is

$$Q = \frac{\text{Energy Stored}}{\text{Energy Dissipated}}$$

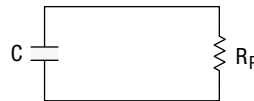
For a capacitor, two equivalent circuits are possible.

Series



$$Q = \frac{1}{(2\pi) f R_S C}$$

Parallel



$$Q = (2\pi) f R_P C$$

Clearly, the two definitions must be equal at any frequency, which establishes

$$R_P = \frac{1}{(2\pi f)^2 C^2 R_S}$$

In the case of a high Q tuning diode, the better physical model is the series configuration, for the depleted region is an almost perfectly pure capacitance; and the undepleted region, due to its relatively low resistivity, is almost a pure resistor in series with the capacitance. Furthermore, the contact resistances are also clearly in series.

Q, then, for a tuning varactor is given by

$$Q_{(-V)} = \frac{1}{2 \pi f R_{(-V)} C_{(-V)}}$$

where  $f$  is the operating frequency,  $C_V$  is the junction capacitance, and  $R_V = R(\text{epi}) + R_C$ , the sum of the resistance of the undepleted epi and the fixed contact resistance.

From the above equation it follows that  $Q$  is a sensitive function of the applied reverse bias. As this bias is increased, epi depletion expands, reducing the junction capacitance as well as the undepleted epi resistance. Both of these changes translate into an increase in  $Q$ .

Also important to note is the dependence of  $Q$  on the operating frequency. Historically, the tuning varactor business developed the habit of specifying  $Q$  at 50 MHz, in spite of the fact that  $Q$  values of microwave diodes are so high that it is impossible to measure them accurately at 50 MHz. However, one may extrapolate  $Q$  to a different frequency simply by using the reciprocal relationship.

$$Q(f_1) = Q(f_2) \frac{f_2}{f_1}$$

The higher the  $Q$  factor of the varactor diode, the lower the energy dissipation and higher the operating frequency limit of the LC circuit in which it is used. There are two empirical rules developed by circuit designers that determine the frequency limits in two applications.

In voltage controlled oscillators, the maximum frequency of operation is approximately the one at which the varactor  $Q$  drops to 10

$$f_{\text{max limit}} = \frac{Q_{\text{ref}} f_{\text{ref}}}{10}$$

where  $Q_{\text{ref}}$  is the varactor  $Q$  measured at the reference frequency  $f_{\text{ref}}$ .

In tunable filters, the maximum frequency of operation is approximately the one at which the varactor  $Q$  drops to 100.

$$f_{\text{max limit}} = \frac{Q_{\text{ref}} f_{\text{ref}}}{100}$$

$Q_{\text{ref}}$  and  $f_{\text{ref}}$  have the same meaning as above.

The varactor  $Q$  is also a sensitive function of the temperature. In a well-constructed varactor diode

$$Q = T^{-\frac{3}{2}}$$

where  $T$  is the absolute temperature in degrees K. It follows from this equation that as temperature increases, the circuit losses increase and the frequency limitation becomes more severe. This relationship is particularly important to note when the operating temperature range extends well above the ambient temperature at which the  $Q$  values are measured and specified. A varactor selection based on its reported  $Q$  at ambient temperature may prove incorrect if its  $Q$  falls below the acceptable limit at the operating temperature.

## APPLICATION NOTE

# Mixer and Detector Diodes

## Surface Barrier Diodes

Surface barrier diodes, the most common of which is known as the Schottky diode, are commonly used in mixer and detector circuits. In a surface barrier diode the rectifying junction is formed between a metal and a semiconductor, which may be either n-type or p-type, rather than between two differently doped semiconductor layers (n-type and p-type) as would be the case for a p-n diode. The Schottky barrier diode is made by sputtering or evaporating the metal onto the surface of the semiconductor (silicon or gallium arsenide). The type of metal and the doping of the semiconductor material determine many of the electrical characteristics of the Schottky barrier diode. The physics, construction and applications of Schottky diodes are discussed in this application note.

## Types of Construction

Schottky diodes that are made from either silicon or gallium arsenide are available from Skyworks. Silicon diodes made with either n-type or p-type material are available while GaAs diodes are available in n-type only. Skyworks Schottky diodes can be classified based on packaging and chip construction.

### Mounted Beam-Lead Package

In this type, one or more beam-lead Schottky diodes with coplanar leads are bonded onto a ceramic, fiberglass, or plastic substrate. This construction is mechanically rugged, has very low inductance, and is particularly convenient for double-balanced mixers.

### Unmounted Chip

Schottky diodes are available as dice. They are offered with several different die sizes and bonding pad configurations.

### Unmounted Beam-Lead Diodes

Beam-lead diodes are used in microwave integrated circuits (MIC) or other special constructions, in which minimum inductance and/or minimum size are important. They are available as single diodes, pairs, quads, and other monolithic arrangements.

## Electrical Characteristics and Physics of Schottky Barriers

Schottky barrier diodes differ from junction diodes in that current flow involves only one type of carrier instead of both types. That is, in N-type Schottkys, forward current results from electrons flowing from the N-type semiconductor into the metal; whereas in P-type Schottkys, the forward current consists of holes flowing from the P-type semiconductor into the metal.

Diode action results from a contact potential set up between the metal and the semiconductor, similar to the voltage between the two metals in a thermocouple. When metal is brought into contact with an N-type semiconductor (during fabrication of the chip), electrons diffuse out of the semiconductor into the metal, leaving a region under the contact that has no free electrons ("depletion layer"). This region contains donor atoms that are positively charged (because each lost its excess electron), and this charge makes the semiconductor positive with respect to the metal. Diffusion continues until the semiconductor is so positive with respect to the metal that no more electrons can go into the metal. The internal voltage difference between the metal and the semiconductor is called the contact potential and is usually in the range 0.3–0.8 V for typical Schottky diodes.

When a positive voltage is applied to the metal, the internal voltage is reduced, and electrons can flow into the metal. Only those electrons whose thermal energy happens to be many times the average can escape, and these "hot electrons" account for all the forward current from the semiconductor into the metal.

One important thing to note is that there is no flow of minority carriers from the metal into the semiconductor and thus no neutral plasma of holes and electrons is formed. Therefore, if the forward voltage is removed, current stops "instantly," and reverse voltage can be established in a few picoseconds. There is no delay effect due to charge storage as in junction diodes. This accounts for the exclusive use of surface barrier diodes in microwave mixers, where the diode must switch conductance states at microwave local oscillator rates.



The voltage-current relationship for a barrier diode is described by the Richardson equation (which also applies to thermionic emission from a cathode). The derivation is given in many textbooks (for example, Sze).

$$I = AA^{**} \exp\left(-\frac{q\phi_B}{kT}\right) \left[\exp\left(\frac{qV}{NkT}\right) - 1\right]$$

where

A = area (cm<sup>2</sup>)

A\*\* = modified Richardson constant (amp/oK)<sup>2</sup>/cm<sup>2</sup>)

k = Boltzman's Constant

T = absolute temperature (°K)

φB = barrier heights in volts

V = external voltage across the depletion layer (positive for forward voltage) - V - IR<sub>S</sub>

R<sub>S</sub> = series resistance

I = diode current in amps (positive forward current)

n = ideality factor

The barrier height φB is primarily determined by choice of barrier metal and the type (n or p) of semiconductor used. A secondary consideration is the crystal orientation of the substrate. The barrier height is important as it determines the amount of local oscillator power required to drive the diode into its nonlinear region. If there is limited local oscillator power available a low barrier diode would be used. If more local oscillator power is available a higher barrier diode could be used to improve intermodulation distortion.

Richardson's equation describes the behavior of the diode but it is hard to use for circuit design. A better equation for circuit designers to use is one in which all parameters are independent of voltage and current. The simplest one that agrees fairly well with Richardson's equation is

$$I = A^*J_0^*(\exp(q^*V/nkT) - 1) = I_S \exp\left(\frac{qV}{nkT} - 1\right)$$

where

I = current in amps

A = area of Schottky barrier in cm<sup>2</sup>\*

J<sub>0</sub> = saturation current density in amps/cm<sup>2</sup>\*

V = applied voltage in volts

n = ideality factor

T = temperature in Kelvin

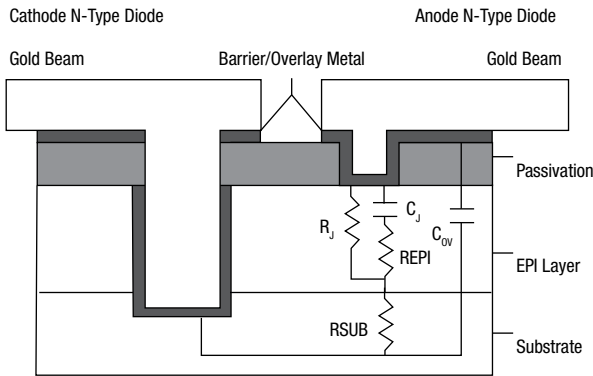
\* typical values for these variables and others necessary for computer modelling are included in the following table.

### Matrix for mW Spice Diode Model

Frequency	Drive	V <sub>B</sub> (V)	C <sub>J0</sub> Min. (pF)	C <sub>J0</sub> Max. (pF)	R <sub>S</sub> (Ω)	V <sub>F</sub> (V)	I <sub>S</sub> (A)
KU	DMF	2	0.05	0.15	12	0.5	3.17E-08
	DME	3	0.05	0.15	12	0.6	6.33E-10
	DMJ	4	0.05	0.15	12	0.8	6.33E-13
X	DMF	2	0.15	0.30	7	0.5	1.27E-07
	DME	3	0.15	0.30	7	0.6	2.53E-09
	DMJ	4	0.15	0.30	7	0.8	2.53E-12
S	DMF	2	0.30	0.50	4	0.5	2.48E-07
	DME	3	0.30	0.50	4	0.6	4.97E-09
	DMJ	4	0.30	0.50	4	0.8	4.97E-12

## Diode Cross-Section

The following picture shows a cross-section of a typical beam-lead Schottky diode.



where

$R_J$  = junction resistance

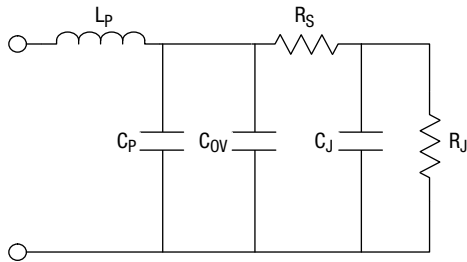
$C_J$  = junction capacitance

$R_{EPI}$  = resistance of epi layer

$R_{SUB}$  = resistance of substrate (spreading resistance)

$C_{OV}$  = overlay capacitance

The equivalent circuit of these structures is shown below.



where

$R_S = R_{EPI} + R_{SUB}$

$C_P$  = package capacitance (where applicable)

$L_P$  = package inductance (where applicable)

The following table lists  $C_P$  and  $L_P$  for some standard single diode packages.

Package	CP (pF)	LP (nH)
130-011	0.10	0.6
207-011	0.13	0.6
247-001	0.15	0.3
325-011	0.14	0.6
404-011	0.09	0.5
464-011	0.03	0.5

## Schottky Barrier Diode Capacitance

The total capacitance of a Schottky diode is

$$C_T = C_J + C_{OV} + C_P$$

where

$C_J$  = junction capacitance

$C_{OV}$  = overlay capacitance

$C_P$  = package capacitance

The junction capacitance is generally measured without bias and is governed by the following equation:

$$C_J(0) = \frac{A \cdot q \cdot E_S \cdot N_d^{1/2}}{(2 \cdot (V_i - kT/q))^{1/2}}$$

At an applied voltage  $C_J(V)$  can be computed by the following equation:

$$C_J(V) = \frac{C_J(0)}{(1 - (V/V_i - kT/q))^{1/2}}$$

where

$A$  = area of Schottky barrier in  $\text{cm}^2$

$N_d$  = doping density of epi layer in  $\text{cm}^3$

$E_S$  = dielectric constant of material  $\cdot E_0$

$V$  = applied voltage in volts

$V_i$  = built in voltage =  $\phi_B - 0.15$  for N-type silicon

with  $N_d = 10^{17}$

## Series Resistance

The series resistance of a Schottky diode is the sum of the resistance due to the epi layer and the resistance due to the substrate. The resistance of the epi is given by the following equation:

$$R_{EPI} = \frac{t}{q \cdot \mu_n \cdot N_d \cdot A}$$

$$= \frac{L}{q \cdot \mu_n \cdot N_d \cdot A}$$

where

$L$  = thickness of epi in cm

$\mu_n$  = mobility of electrons for N-type Si (for P-type silicon the mobility of holes would be used)

$N_d$  = doping density of the epi layer in  $\text{cm}^3$

$A$  = area of Schottky contact in  $\text{cm}^2$

The resistance of the substrate is given by the following equation:

$$R_{SUB} = 2 \cdot \rho_S \cdot (A/\pi)^{1/2}$$

where

$A$  = area of Schottky contact in  $\text{cm}^2$

$\rho_S$  = substrate resistivity in  $\Omega\text{-cm}$

## Mixer Diodes Compared To Detector Diodes

Mixer diodes are designed to convert radio frequency (RF) energy to an intermediate frequency (IF) as efficiently as possible. (In practice, the conversion efficiency should be at least 20%.) The reason for doing this is that selective amplifiers at the RF frequency are expensive, so the signal is converted to a lower frequency where high gain and good selectivity can be more easily achieved.

The frequency conversion is obtained by operating a diode with fast response and high cutoff frequency as a switch, turning it on and off at a rate determined by a local oscillator (LO). The output frequency ( $f_F$ ) is then the difference between the LO frequency and the RF frequency.

A good mixer diode with a high cutoff frequency will be capable of low conversion loss ( $L_C$ ). This, combined with a low noise figure in the IF amplifier, will result in a low overall noise figure, unless the diode itself generates noise (other than normal thermal noise). Ideally, the mixer diode should accomplish this with a minimum of LO power and no DC bias.

Detector diodes are designed to rectify very low levels of RF power to produce a DC output voltage proportional to the RF power. The diode may be operated at a small DC bias (typically 50  $\mu\text{A}$ ) which results in a relatively high RF impedance (typically 600  $\Omega$ ). As a result, very low capacitance is required to achieve high sensitivity. Since the output is at a very low level, the low frequency, audio frequency excess noise (“1/f noise”) is an important consideration.

## Mixer Parameters

The quality of a mixer diode is generally controlled by either low frequency parameters or RF operating parameters.

Low frequency parameters customarily specified are (in order of importance):

Junction Capacitance ( $C_{J0}$ ) at zero bias

Series Resistance ( $R_S$ ) or cutoff frequency ( $f_{CO}$ )

Reverse Voltage ( $V_B$ ) at 10 mA or 100 mA

Forward Voltage ( $V_F$ ) at 1 mA

Excess Noise Voltage (1/f noise)

Leakage Current ( $I_R$ ) at IV

Series resistance is sometimes controlled by specifying dynamic resistance,  $R_T$ , at some particular forward current. Series resistance can then be calculated by subtracting  $R_B$  ( $R_B = 28/I(\text{mA})$ ) from  $R_T$ . The excess noise voltage need not be specified unless the IF frequency is less than 1.0 MHz (such as for Doppler radars or autodyne mixers).

Some people prefer to specify RF parameters instead of the above low frequency parameters. In order of importance, the customary parameters are:

### Noise Figure (NF in dB)

would be specified in a particular mixer circuit at a particular RF frequency and LO power level.

### Conversion Loss ( $L_C$ in dB)

would be specified in a particular mixer circuit at a particular RF frequency and LO power level.

### RF Impedance (VSWR)

expresses how well the diode and circuit are matched to the LO source at a particular LO power.

### IF Impedance ( $Z_{IF}$ )

expresses the low frequency impedance of the driven diode, considered as a source of IF voltage. The IF amplifier should be designed to have its optimum noise figure for this source impedance. This parameter is dependent on LO power, as well as RF and harmonic impedance presented to the diode.

## Detector Parameters

As with mixers, a detector diode can be specified by its low frequency parameters, the same ones that apply to the mixer diodes, with the exception that 1/f noise is now second in importance instead of fifth.

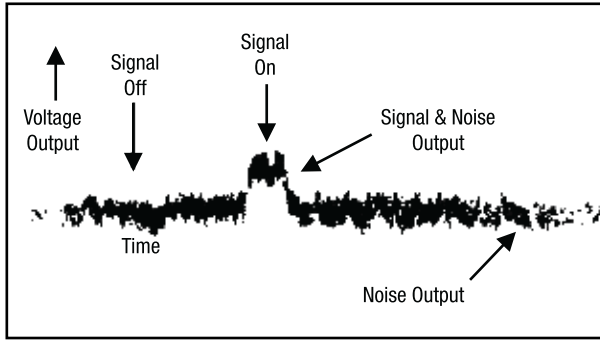
Alternatively, a detector diode can be specified by RF parameters, the customary ones being:

### Voltage Sensitivity (V/mW)

is the ratio of DC voltage output to RF power input at a particular frequency and power level. Voltage sensitivity depends on bias current and  $C_{J0}$ .

### Tangential Signal Sensitivity (TSS, in dBm)

is the minimum RF signal level, in dB below 1 mW, that produces a tangential indication on a low frequency oscilloscope. See Figure 1:



**Figure 1. Measurement of Tangential Signal Sensitivity**

(Tangential sensitivity depends on voltage sensitivity, diode excess noise voltage, and both RF and video bandwidth).

#### Video impedance ( $Z_V$ , in $\Omega$ )

is the low frequency impedance of the diode, considered as a source of video voltage. It is the same as  $R_T$  at the bias current used (about 600 W for any diode with 50  $\mu$ A bias).

#### Figure of Merit (FM)

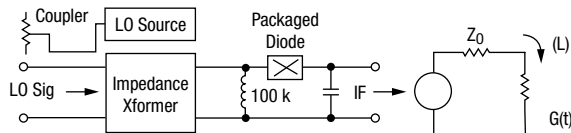
This parameter combines voltage output and  $Z_V$  to give a convenient bandwidth-independent measure of TSS.

### Mixer Diodes

#### Theory of Mixers

The simplest way to think about the action of a mixer diode is to consider a single-ended mixer consisting of a single diode at the end of a transmission line. The RF signal and the local oscillator drive power are coupled into the same line by filters or hybrids. The local oscillator drives the diode into heavy forward conduction for nearly half a cycle and into reverse bias for the other half cycle. The reflection coefficient of the diode,  $\Gamma$ , then varies periodically as a function of time.

In this model the only effect of the junction capacitance and package parasitics is to transform the source impedance from its actual value to some other number,  $Z_0$ , at the semiconductor junction. If the instantaneous junction conductance is  $G(t)$ , then you have the situation indicated in Figure 2:



**Figure 2. Mixer and Equivalent Circuit**

For available LO power,  $P_L$ , the generator voltage is

$$2V_L(t) = 2V_L \cos \omega_L t$$

where

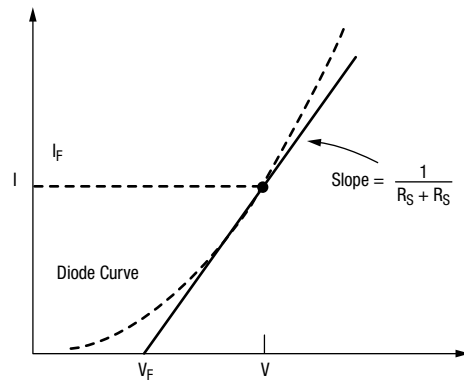
$$V_L = (2Z_0^2 P_L)^{-0.5}$$

#### Diode I–V Approximation

The forward diode characteristic is given by the equation

$$L(t) = I_S \exp[(Vt) - IR_S / 0.028]$$

This equation can be approximated by a two-piece linear approximation, which has the diode conducting only if the voltage exceeds a forward voltage,  $V_F$ :



**Figure 3. Diode Forward Characteristics**

The barrier resistance,  $R_B$ , should be evaluated at the peak current using  $R_B = 0.028/I_P$ . The equation for  $I_P$  is

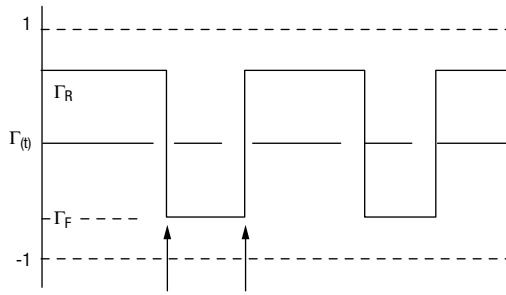
$$I_P = \frac{2V_L - V_F}{Z_0^2 + R_S + R_B}$$

The approximation can be justified by graphing the equation or by looking at an actual diode on a curve tracer (1 mA/cm). In practice,  $V_{F1}$ , the forward voltage at 1 mA, can be used for  $V_F$ .

Therefore, the low frequency diode conductance,  $G$  is

$$G(t) = \begin{cases} \frac{1}{R_S + R_B}, & \text{if } 2V_L(t) > V_F \\ \omega^2 C_J^2 R_S, & \text{otherwise} \end{cases}$$

If you use this reasoning to compute the time-dependent reflection coefficient, the result is a rectangular waveform (Figure 4).



**Figure 4. Time Dependent Reflection Coefficient**

$$\Gamma_F = \frac{R_S + R_B - Z_0^1}{R_S + R_B + Z_0^1} \approx 1 + \frac{2(R_B + R_S)}{Z_0^1}$$

$$\Gamma_R = \frac{1 - Z_0^1 \omega^2 C_J^2 R_S}{1 + Z_0^1 \omega^2 C_J^2 R_S} \approx 1 - 2Z_0^1 \omega^2 C_J^2 R_S$$

The angle,  $\Theta$ , is the conduction angle, i.e. the number of electrical degrees of the LO waveform during which the diode is conducting.

$$\begin{aligned} \Theta &= 2 \arccos \left( \frac{V_F}{V_T} \right) \\ &= 2 \arccos \left( \frac{V_F}{(8Z_0^1 P_L)^{0.5}} \right) \end{aligned}$$

Typically the conduction angle is between  $120^\circ$  and  $170^\circ$ .

## Conversion Loss

In order to handle the mathematics of the mixer, the  $\Gamma$  waveform must be expressed as a Fourier series

$$\Gamma(t) = \Gamma_0 = \Gamma_1 \cos \omega_L t + \Gamma_2 \cos \omega_L t + \dots$$

where

$$\begin{aligned} \Gamma_1 &= 2/\pi(\Gamma_F - \Gamma_R) \sin \Theta/2 \\ &- 2/\pi(2 - 2Z_0^1 \omega^2 C_J^2 R_S - 2R_S + R_B/Z_0^1) \sin \Theta/2 \end{aligned}$$

When there is an incident of RF signal voltage  $V_S \cos \omega_S t$ , in addition to the LO voltage, the voltage of the reflected wave is

$$\begin{aligned} V_R(t) &= \Gamma(t) V_S \cos \omega_S t \\ &= \Gamma_0 V_S \cos \omega_S t + \Gamma_1 \cos \omega_L t \cos \omega_S t + \dots \\ &= \Gamma_0 V_S \cos \omega_S t + 1/2 \Gamma_1 V_S [\cos(\omega_L - \omega_S)t \\ &\quad \cos(\omega_L + \omega_S)t] \dots \end{aligned}$$

The important term is the one involving  $\omega_L - \omega_S$ , because this is the difference frequency (IF). The ratio of reflected power at this frequency to the incident power at  $\omega_S$  is the conversion efficiency,  $\eta$ .

$$\begin{aligned} \eta &= \frac{P_{IF}}{P_S} = \frac{(0.5 \Gamma_1 V_S)^2}{V_S^2} = \frac{\Gamma_1^2}{4} \\ &= \frac{4}{\pi^2} \left[ 1 - Z_0^1 \omega^2 C_J^2 R_S \frac{(R_S + R_B)}{Z_0^1} \right]^2 \sin^2 \frac{\Theta}{2} \end{aligned}$$

To optimize the conversion efficiency, you clearly want  $R_S$  to be zero; however, nature won't allow you to do this. In practice low  $R_S$  means large junction diameter and thus high  $C_J$  (and vice versa), so diode manufacturers introduce a parameter, the "cutoff frequency," which is essentially independent of junction diameter:

$$f_c = \frac{1}{2\pi R_S C_J}$$

where  $f_c$  = cutoff frequency

It is useful to express conversion loss in terms of  $f_c$  instead of  $R_S$ , leaving  $C_J$  as the free parameter, since the range of variation of  $f_c$  in actual products is limited by material properties, whereas  $C_J$  can be designed for almost any value.

$$\begin{aligned} R_S &= \frac{1}{\omega_L^2 C_J} \\ \eta &= \frac{4}{\pi^2} \sin^2 \frac{\Theta}{2} \left[ 1 - \left( \frac{Z_0^1}{X_C} + \frac{X_C}{Z_0^1} \right) \frac{f}{f_c} - \frac{R_B}{Z_0^1} \right]^2 \end{aligned}$$

The quantity in parenthesis is close to 2, if the reactance of  $C_J$  is between  $Z_0^1/2$  and  $2Z_0^1$ . So, for a large range of  $C_J$ , the conversion efficiency is determined almost entirely by the ratio of LO frequency to the cutoff frequency of the junction, by the peak current which determines  $R_B$ , and by the conduction angle.

For this reason, the capacitive reactance should be chosen to be  $Z_0^1$  or typically  $100 \Omega$ . The exact value is not critical for conversion loss unless very wide bandwidth is desired. Cutoff frequency should clearly be as high as possible. Conduction angle and  $R_B$  are determined by LO power and forward voltage. Therefore, LO power should be high and forward voltage should be low.

For high drive levels,  $\Theta$  is close to  $180^\circ$ ,  $\sin t/2$  is nearly one and  $R_S = 0$  so the best conversion efficiency is

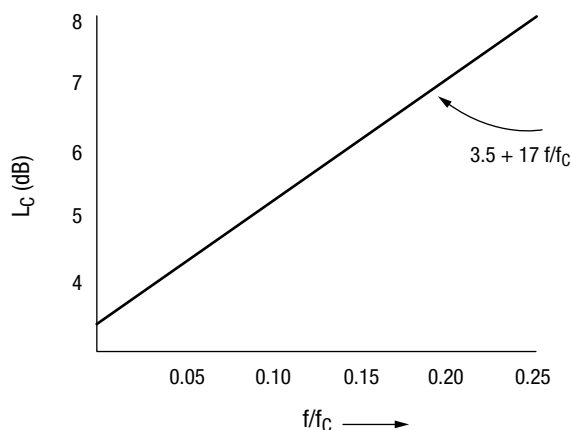
$$\eta = \frac{4}{\pi^2} \left( 1 - 2 \frac{f}{f_c} - \frac{R_B}{Z_{I_0}^2} \right)^2$$

and the conversion loss, in dB, is

$$L_C \approx 3.9 \text{ dB} + 17 \frac{f}{f_c} + 9 \frac{R_B}{Z_{I_0}^2}$$

Actual single-ended mixers give results similar to this equation, or slightly better. Theoretically, an actual mixer can be 0.9 dB better than this because of harmonic suppression. That is, instead of the sum frequency and other harmonics being absorbed in the source resistance, they are reflected back into the diode to be remixed with harmonics of the  $-\Gamma$  waveform to produce more IF output. In actual diodes this happens automatically if the package is designed to have a low pass characteristic that cuts off frequencies between the operating frequency and the harmonics. In any case, the circuit can be designed to reflect all harmonics back into the diode, and if these reflections are phased properly, the full 0.9 dB improvement can be attained.

The conversion loss actually measured on production diodes is in general agreement with the previous equations, as indicated in the following figure. The conversion loss points are from a large number of production lots measured at Skyworks over the last several years. As can be seen in Figure 5, the results follow equation (4–15) if 0.9 dB is subtracted for harmonic suppression, and the last term contributes about 0.5 dB.



**Figure 5. Conversion Loss as a Function of Normalized Frequency**

## Noise Figure

### Definitions and Formulas

In practice, not only the wanted signal comes into the diode to be converted to the IF frequency, but also random signals of various sorts. This noise is also converted to the IF frequency with the same conversion efficiency as the signal. In addition to this, the mixer adds other sources of noise:

1. Image noise—If the signal frequency is  $f_L + f_{IF}$ , then noise at the frequency  $f_L - f_{IF}$  is also converted to the IF frequency with the same efficiency. This doubles the noise at the IF port.
2. Diode thermal noise—The parasitic resistance  $R_S$  generates thermal noise. The higher the  $R_S$  the more the conversion loss and the higher this contribution is, in direct proportion. This noise source will increase if the diode is run at elevated temperatures.
3. Shot noise—Electron flow across the diode depletion layer generates shot noise. This noise turns out to be half what the thermal noise would be in an ordinary resistor equal to  $R_B$ , and will be directly proportional to the absolute temperature of the diode.
4. Excess noise—At low frequencies, the junction noise increases due to trapping of electrons. This noise often has  $1/f$  spectrum and is therefore called  $1/f$  noise. At high current levels there is additional noise due to velocity saturation of the carriers and carrier trapping. This noise has a minor effect on mixers and is discussed in a later section.
5. IF noise—The input stage of the IF amplifier adds some noise of its own. Most mixer specifications assume that the IF amplifier has a noise figure of 1.5 dB.
6. LO noise—The sidebands of the noise from the local oscillator may overlap the signal and image frequencies, thus acting like an excess noise source. (This effect can be eliminated by filtering the LO or by using a balanced mixer.)
7. Harmonic noise—In the wide-open, single-ended mixer design we are talking about, noise at frequencies near harmonics of the LO frequency can also be converted to the IF frequency. This can be eliminated by using a harmonic enhanced design, or by making sure that the package parasitics isolate the junction from the circuit at the harmonic frequencies.

Noise factor is defined as the ratio of the signal-to-noise (S/N) ration at room temperature at the signal input to the mixer to the S/N ration at the output of the IF amplifier. Noise figure is the noise factor expressed in dB. For a moderately heavily driven mixer ( $R_B \approx 0$ ), the noise added from the image and the diode thermal noise (from  $R_S$ ) exactly makes up for the noise lost in the conversion process, if the diode is at room temperature. Therefore, the noise power going into the IF amplifier is exactly equal to the noise coming in with the signal; but the signal is reduced, so the signal-to-noise ratio is reduced by exactly the amount of the conversion loss.



After adding in the IF noise figure, the result is

$$NF = \text{noise figure (dB)} \\ = L_C \text{ (dB)} + N_{IF} \text{ (dB)}$$

However, the shot noise and the excess junction noise should be considered. The shot noise added by the junction is only half what would be expected from a resistor equal to  $R_B$ . For low drive the increase in noise figure is not as great as the increase in conversion loss. If enough LO power is absorbed to heat the diode significantly, one should take into account the temperature of the diode. Also, excess noise ( $1/f$  noise) should be taken into account if the IF frequency is low. This is usually accounted for by assigning an effective temperature to the diode, which may be either less or more than room temperature,  $T_0$ .

$$NF = L_C \text{ (dB)} + NTR \text{ (dB)} + N_{IF} \text{ (dB)}$$

where the NTR, in this model, is

$$NTR = \frac{T_{eff}}{T_0} = 1 - 4 \frac{f}{f_c} \left( \frac{T}{T_0} - 1 \right) \\ + \frac{R_B}{Z_0^2} \left( 2 - \frac{T}{T_0} \right)$$

### NTR = Noise Temperature Ratio

In most specifications, the IF amplifier noise figure is assumed to be 1.5 dB (if the actual amplifier has a different noise figure, the data are corrected to the nominal 1.5 dB). In addition, the diode is assumed to be operated at a junction temperature equal to room temperature.

Therefore, if the IF frequency is not too low the expected noise figure for the single-ended mixer, driven with a quiet local oscillator, is

$$NF \approx 5.4 \text{ dB} + 17 f/f_c + 10 \log_{10} (NTR) + 9 R_B/Z_0^2$$

For IF frequencies below 1.0 MHz the  $1/f$  noise becomes important and the noise figure could be higher than this unless the diodes are selected for low  $1/f$  noise. At high local oscillator drive levels,  $R_B$  decreases, but the high forward current activates additional noise due to traps and velocity saturation, as well as higher temperature. Thus the noise figure increases instead of approaching a constant. In addition, as the reverse swing from the LO approaches diode breakdown, the back resistance,  $R_R$ , decreases, and conversion loss will be degraded further.

### Double Sideband (DSB) Noise Figure

When noise figure is actually measured, a hot source or broadband noise tube (or noise diode) is used as a "signal" source. Unless filtering is used, this kind of source provides "signal" both at the signal frequency and image frequency. Therefore, when the noise source is switched on and off to determine the signal-to-noise ratio at the output of the IF amplifier, twice as much output is obtained with the noise source on than if a single frequency signal were used. The measured noise figure (the so-called "double sideband" noise figure) will be 3 dB lower than the specified ("single sideband") noise figure. Nevertheless, this kind of measurement is more convenient to do, and usually the measurement consists of measuring the DSB noise figure and adding 3 dB to obtain the SSB noise figure.

There are many other factors, such as line losses, coupler losses, the loss in signal -LO combiner or filter, and the deviation of the IF noise figure from 1.5 dB which must be taken into account as part of the calibration in order to get the correct noise figure for the single diode mixer alone.

### Crystal Current

The diode produces DC current as a result of rectifying the local oscillator current. The total current is

$$I(t) = \begin{cases} \frac{2V_L \cos \omega_L t - V_T}{Z_0^2} & \text{if } 2V_L(t) > V_T \\ \omega^2 C_J^2 R_S V_L \cos \omega_L t, & \text{(otherwise)} \end{cases}$$

The average DC current, or crystal current: ( $\omega = t$ ) is

$$\text{crystal current } I_{DC} = \frac{2V_L \left[ \sin \frac{\theta}{2} - \frac{\theta}{2} \cos \frac{\theta}{2} \right]}{kT\pi (Z_0^2 + R_S + R_B)}$$

If the DC voltage is computed by similar reasoning, there is an apparent reverse DC voltage equal to

$$V_{DC} = -Z_0 I_{DC}$$

This is caused by the DC current through the DC circuit assumed to be equal to  $Z_0$ . (Actual single ended mixers typically use a 100  $\Omega$  resistor.)

## VSWR

The VSWR expresses how well the RF diode impedance is matched to the LO source impedance. In terms of the LO current and voltage it is defined as:

$$VSWR = \frac{Z_{LO}}{Z_0} \text{ or } \frac{Z_0}{Z_{LO}}, \text{ whichever is larger}$$

The large signal impedance,  $Z_{LO}$ , is the ratio of  $V_{LO}$  and  $I_{LO}$  which are the first order Fourier coefficients of the voltage and current waveforms:

$$V(t) = V_{DC} + V_{LO}\cos\omega_L t + V_2\cos 2\omega_L t + \dots$$

$$I(t) = I_{DC} + I_{LO}\cos\omega_L t + I_2\cos 2\omega_L t + \dots$$

$$I_{LO} = \frac{2V_L(\theta - \sin\theta)}{2\pi(Z_1' + R_S + R_B)} + 2\omega^2 C_J^2 R_S V_L$$

$$V_{LO} = 2V_L - Z_1' I_{LO}$$

$$\frac{Z_{LO}}{Z_1'} = \frac{V_L}{Z_1' I_{LO}} = \frac{2\pi \left( \frac{R_S + R_B}{Z_1'} + 1 \right)}{\theta - \sin\theta + \pi\omega^2 C_J^2 R_S Z_1'} - 1$$

$$VSWR = \left[ \frac{Z_{LO}}{Z_1'} \right]^{\pm 1}$$

In order to reduce radiation of the LO from the antenna, the VSWR should be less than 1.6. This corresponds to a reflection of less than 5% of the LO power.

## IF Impedance

When the diode is considered as a source of IF voltage, it is important to know what its low frequency (IF) impedance is. The IF amplifier has to be designed to work optimally when driven from a source of this impedance, or diodes and circuit conditions should be chosen to prove an optimum impedance for the input of the IF amplifier.

If an external DC bias is applied to the diode, the crystal current will change, due to a change in the conduction range. Applying a small reverse DC (or IF frequency) voltage is the same as increasing  $V_T$  by the same amount. The IF impedance is the ratio of the applied DC or IF voltage to the change in crystal current.

$$Z_{IF} = \frac{\Delta V_F}{\Delta I_{DC}} = \frac{1}{(dI_{DC}/dV_f)}$$

$$= \frac{2\pi}{\Theta} (Z_1' + R_S + R_B)$$

This is always greater than  $2Z_0$  and typically ranges from 200 to 500  $\Omega$ .

As an example of the behavior of these parameters as LO power is varied, the following graph shows the noise figure, VSWR, crystal current and IF impedance of an X-band diode. The fixed parameters are  $V_F = 0.28$  V,  $R_S = 7\omega$ ,  $C_J = 0.20$  pF, and  $Z_0 = 150$   $\Omega$ , values appropriate for low barrier diodes in a waveguide test holder.

Performance is better at low LO power levels than these formulas indicate because actual diodes have a soft knee in the forward I-V characteristic. Also, the noise figure for actual diodes can be about 1 dB better due to harmonic suppression, but the noise figure goes up at high LO power due to heating and other effects. Nevertheless, these formulas can give some insight into the meaning of the various RF parameters and their relationship to the capacitance and I-V characteristics of an actual diode.

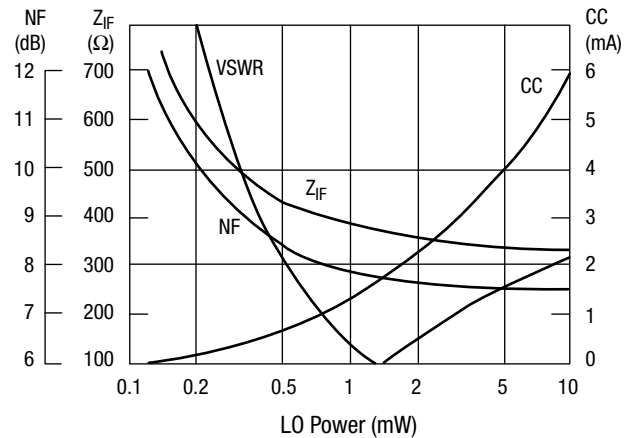


Figure 6. Mixer Parameters as a Function of LO Power

## Practical Mixer Configurations

### Single-Ended Mixer

The single-ended mixer used in the above analysis has some disadvantages which limit its usefulness.

1. Even with a low VSWR, too much LO power is reflected into the signal port.
2. To couple the LO and signal onto the same line with broad bandwidth requires a coupler which increases the conversion loss, noise figure and multiplies required LO power. (For example, a 6 dB coupler adds 1.2 dB to the conversion loss and noise figure and requires four times the LO power.)



3. If the coupler is unacceptable, a set of filters can be used, but if the IF and LO frequencies are close, the bandwidth will be restricted severely. However, no extra LO power is needed.
4. The mixer is very sensitive to amplitude variations (AM noise) in the LO power, which will increase the noise figure, if the AM noise spectrum overlaps the signal frequency.

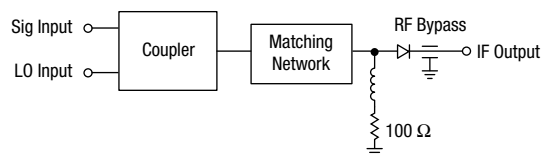
### Balanced Mixer

For many years, the solution to these problems was to use a balanced mixer containing two diodes driven in opposite phase. In this case, the reflected LO power cancels, but the IF output adds if the diodes are reversed. Conversion loss is the same as for the single-ended mixer.

Twice the LO power is required as for a single diode mixer. The VSWR can be much lower, and the ZIF depends on how the signals are combined (for the transformer circuits it will be half that of a single diode). The noise figure will be reduced dramatically compared to the single-ended mixer because the AM noise from the local oscillator at the signal frequency is cancelled at the IF output, provided the diodes are well matched.

Figure 7 shows some of the common balanced mixer configurations, as well as a practical single-ended mixer:

#### A. Single-Ended Mixer



#### B. Balanced Mixers

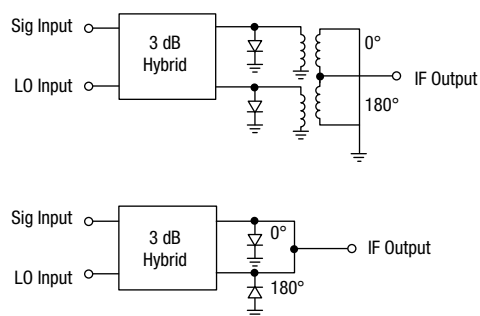


Figure 7. Single-Ended and Balanced Mixers

### Double-Balanced Mixers

The use of four diodes in a ring, bridge, or star configuration makes it possible to cancel the LO reflections and noise at both the signal and IF ports, so no filtering is needed at the IF port. This requires the use of very broadband baluns or transformers. In recent years, several manufacturers have developed these double-balanced mixers to the point where bandwidths over 25 GHz are possible. To do this requires that the diodes

be physically very close together to avoid inductive parasitics, and exhibit good electrical matching between all four diodes.

The best solution is to make all four diodes simultaneously in a ring configuration using beam-lead technology. (These are available mounted on various carriers, or as unmounted beam-lead quads.) Figure 8 shows one of the most common circuit configurations.

#### C. Double-Balanced Mixer

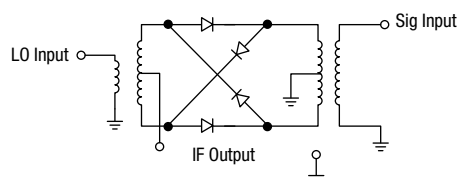


Figure 8. Ring Quad Configuration

In circuits with bandwidth over one octave, harmonic enhancement cannot be used, so there is a penalty in conversion loss.

The easiest way to understand the conversion action is to consider Figure 9:

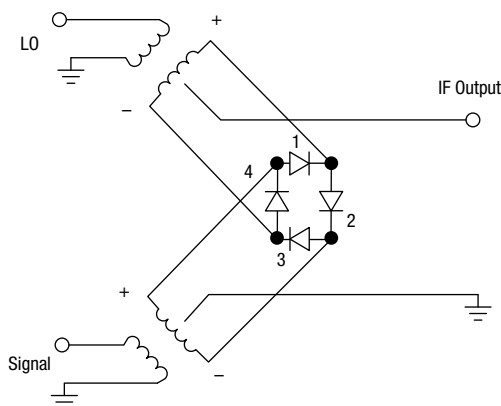


Figure 9. Ring Quad for Analysis

When LO is in "positive" phase, diodes (2) and (3) conduct, and the negative arm of the signal transformer is connected to IF. When the LO is negative, diodes (1) and (4) conduct and connect the positive arm of the signal transformer to the IF output. The two pairs of diodes therefore act like a high-speed SPDT switch. When one goes through the mathematics for the conversion loss (involving the transmission coefficient instead of the reflection coefficient) formulas for conversion loss and noise figure similar to the ones for the single-ended mixer can be derived.

Parameter Tradeoffs

Barrier Height

The barrier height of a Schottky diode is important because it directly determines the forward voltage. In order to get good noise figure the LO drive voltage,  $V_L$ , must be large compared to  $V_T$ , which is essentially  $V_{F1}$ . Normally, it is best to have a low forward voltage (low  $V_{F1}$ , or low drive) diode, to reduce the amount of LO power needed. However, if high dynamic range is important, high LO power is needed, and the diode can have a higher  $V_F$  and should also have a high  $V_B$  (see table below).

Type	Typical $V_{F1}$	LO Power	Application
Zero Bias	0.10–0.25	<0.1 mW	Mainly for Detectors
Low Barrier	0.25–0.35	0.2–2 mW	Low–Drive Mixers
Medium Barrier	0.35–0.50	0.5–10 mW	General Purpose
High Barrier	0.50–0.80	>10 mW	High Dynamic Range

Noise Figure vs. LO Power

At low LO drive levels, noise figure is poor because of poor conversion loss, due to too low a conduction angle. At high LO drive levels noise figure again increases due to diode heating, excess noise, and reverse conduction.

If high LO drive level is needed, for example, to get higher dynamic range, then  $V_B$  should be specified (>5 V). However, nature requires that the price for this with higher  $R_S$  (lower  $f_c$ ), so the noise figure will be degraded compared to what could be obtained with diodes designed for lower LO drive. Forward voltage and breakdown are basically independent parameters, but high breakdown is not needed or desirable unless high LO power is used.

Such a high breakdown diode will have low reverse current (which is important only if the diode has to run hot).

Silicon vs. GaAs

Typical silicon Schottky diodes have cutoff frequencies in the 80–200 GHz range, which is good for use through Ku-band.

At Ku–band and above or for image enhanced mixers, higher  $f_c$  may be needed, which calls for the use of GaAs diodes. These have lower  $R_S$  due to higher mobility, which translates to cutoff frequencies in the 500–1000 GHz range.

However, if the IF frequency is low, be careful; GaAs diodes have high 1/f noise. They also have high  $V_{F1}$ , so more LO power is required.

C vs. Frequency

There is quite a lot of latitude in choosing  $C_J$ . However, in general, the capacitive reactance should be a little lower than the transformed line impedance ( $Z_0$ ). If  $Z_0$  is not known, a good way to start is to use  $X_C = 100 \Omega$ . Experience has shown that most practical mixers use an  $X_C$  near this value (a little higher in waveguide, and lower in 50 W systems). This translates to the following “rule of thumb” for choosing the junction capacitance of a diode for operation at frequency  $f$  (in GHz):

$$C_{J0} \approx \frac{100}{\omega}$$
$$\approx \frac{1.6}{f} \text{ (in pF)}$$

Detectors

General

Detectors are typically used to convert low levels of amplitude modulated RF power to modulated DC. The output can be used for retrieval of modulated information, or as a level sensor to determine or regulate the RF level.

Detector diodes act as square law detectors for low-level signals. That is, the output voltage is proportional to the square of the RF voltage at the junction (i.e., proportional to the RF power). At higher signal levels, the detector will become linear, and at still higher levels, the voltage output will saturate, and not increase at all with increasing signal.

Detector Circuits

In general, a diode detector will require a single diode together with an RF impedance transformation circuit and some low-frequency components. The configuration looks like:

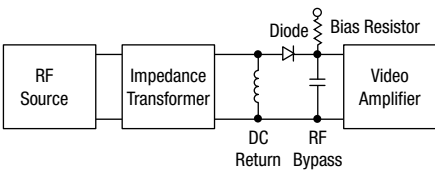


Figure 10. Typical Detector Circuit

The bias resistor generally has a very high impedance compared to the diode a constant current will bias the diode to a favorable impedance level.

## Theory of Detection

### Low Level (Square-Law)

Detection occurs because of the nonlinear I-V characteristics of the diode junction. The I-V curve of the junction is the same at microwave frequencies as at DC.

If the junction capacitance is left out of consideration for the moment, the forward I-V curve of the diode (at room temperature) is

$$I = I_S \left[ \exp \left( \frac{V_J}{0.028} \right) - 1 \right]$$

Where  $V_J = V - IR_S$  = junction voltage

If the DC current is held constant by a current regulator or a large resistor, then the total junction current, including RF, is

$$I = I_0 + i \cos \omega t$$

and the I-V relationship can be written

$$\begin{aligned} V_J &= 0.028 \ln \left( \frac{I_S + I_0 + i \cos \omega t}{I_S} \right) \\ &= 0.028 \ln \left( \frac{I_0 + I_S}{I_S} \right) + 0.028 \ln \left( \frac{i \cos \omega t}{I_0 + I_S} \right) \end{aligned}$$

If the RF current,  $i$ , is small enough, the LN-term can be approximated in a Taylor series:

$$\begin{aligned} V_J &\approx 0.028 \ln \left( \frac{I_0 + I_S}{I_S} \right) + 0.028 \left[ \frac{i \cos \omega t}{I_0 + I_S} - \frac{i^2 \cos^2 \omega t}{2(I_0 + I_S)^2} + \dots \right] \\ &= V_{DC} + V_J \cos \omega t + \text{higher frequency terms} \end{aligned}$$

If one assumes the average value of  $\cos^2$  is 0.50, then the RF and DC voltages are given by the following equations:

$$V_J = \frac{0.028}{I_0 + I_S} \quad i = R_S i$$

$$V_{DC} = 0.028/n \left( 1 + \frac{I_0}{I_S} \right) - \frac{0.028^2}{4(I_0 + I_S)^2} = V_0 - \frac{V_J^2}{0.112}$$

Therefore, the DC voltage decrease from the bias voltage,  $R_0$ , depends on the square of the RF junction voltage only. (Note, however, that the number "0.112" is really  $4nkT/q$  and is temperature dependent.)

To get the maximum voltage sensitivity, it is clearly necessary to arrange the circuit to get the maximum possible RF voltage at the junction. That is, the impedance transformer should be designed to have the highest possible impedance at the diode, and the diode should be biased to a high enough impedance (low  $I_0$ ) so the open circuit RF voltage will not be loaded down too much. In addition,  $C_J$  should be low for the same reason.

### Voltage Output (Square-Law Region)

The output voltage of a detector will depend on the parasitics and circuit impedances. Suppose the impedance transformer is designed to boost the source impedance to an impedance,  $o$ , at the diode. Then the relation between  $V_J$  and the available power of the source PRF can be seen in Figure 11.

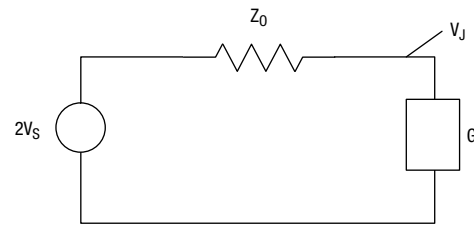


Figure 11.

$$V_S = \sqrt{2Z'_0 P}$$

$$G = \frac{1}{R_s} + \frac{R_s}{X_c^2}$$

As before, the  $C_J$  is absorbed into the impedance transformation and the impedance,  $Z'$ , is assumed real at the junction (i.e.,  $C_J$  has been "parallel-tuned" to get the highest possible  $V_J$ ):

$$\begin{aligned} V_J^2 &= \frac{(2V_S)^2}{(1 + Z'_0 G)^2} \\ &= \frac{8Z'_0 P_{RF}}{(1 + Z'_0 G)^2} \end{aligned}$$

The output voltage of the detector will be

$$V_{DC} - V_0 = \frac{-8Z'_0 P_{RF}}{0.112 (1 + Z'_0 G)^2} = \frac{-71.4Z'_0 P_{RF}}{(1 + Z'_0 G)^2}$$

The impedance  $Z'_0$  is usually limited by bandwidth considerations or by the practical design of the impedance transformer. For a fixed  $Z'_0$ ,  $R_J$  should be as high as possible (which results in a high VSWR). Most manufacturers specify the output voltage for one microwatt RF input power.

An important special case is  $Z'_0 = 50 \Omega$ , because many of the voltage sensitivity specifications are measured by placing the diode in the end of a  $50 \Omega$  line. If the  $C_J$  is small enough, the voltage output per unit power input for  $Z'_0 = 50 \Omega$  is

$$E_0 = \frac{V_0 - V_{DC}}{P_{RF}} = \frac{V_J^2}{0.112} = \frac{3570}{1 + \left(\frac{100}{R_B}\right)} \mu V/\mu W$$

Remember

$$R_S = \frac{28}{I_0 + I_S}, \text{ (for } I_0 \text{ in mA)}$$

So for  $I_0 = 50 \mu A$ ;  $R_B = 560 \Omega$ , and therefore:

$$E_0 = 3000 \mu V/\mu W$$

It should be pointed out that the VSWR will be very high for this kind of detector. In this case the VSWR is equal to  $R_B/50$ , which is over 11 if  $I_0 = 50 \mu A$ , a typical bias current.

Another important special case is when  $Z'_0$  is matched to the shunt conductance,  $Z'_0 = 1/G$ . In this case the voltage output is

$$\begin{aligned} E_0 &= \frac{18}{\frac{1}{R_S} + \left(\frac{R_S}{X_C^2}\right)} \mu V/\mu W \\ &= \frac{18 R_S}{1 + \frac{R_S + R_B}{X_C^2}} \mu V/\mu W \end{aligned}$$

If the detector diodes are specified at a bias current of 50 mA ( $R_B = 560 \Omega$ ) and  $X_C$  is designed to be large, then the matched output voltage is from the previous equation, the larger  $X_C$ , the higher the output voltage, but remember that practical diodes are limited by a finite cutoff frequency so a large  $X_C$  automatically means a larger  $R_S$ .

$$E_0 = 18 R_S = 10,000 \mu V/\mu W$$

In practice, it is usually sufficient to have  $X_C > 20 \Omega$  and  $R_X < 40 \Omega$  which results in no more than 2 dB degradation of the output voltage compared to the above equation.

## Sensitivity

### Tangential Signal Sensitivity (TSS)

At low power levels, sensitivity is specified by the “tangential signal sensitivity” (TSS). This is the power level that raises the DC voltage by an amount so the noise fluctuations do not drop below the level of the noise peaks with no signal. This is about 4 dB above the minimum detectable signal (MDS). Detection is so inefficient that even for wideband systems, the incoming noise (antenna noise) need not be considered. All the noise is produced in the diode and the video amplifier.

$$V_N^2 = 4kTBR_S + 2kTBR_B \left(1 + \frac{I_S}{I_0 + I_S}\right)$$

To this should be added the noise voltage due to the video amplifier, which can be expressed in terms of fictitious noise resistance,  $R_a$ , of the amplifier:

$$V_{NA}^2 = 4kTBR_a$$

The standard value of  $R_a$  is  $1200 \Omega$ .

The total noise voltage is

$$V_N^2 = 2kTB \left[ R_B \left(1 + \frac{I_S}{I_0 + I_S}\right) + 2R_a + 2R_S \right]$$

Since the peak noise voltage is 1.4 times the rms noise voltage, ( $V_N$ ), the condition for tangential voltage output is

$$V_{DC} + 1.4 V_N = V_0 - 1.4 V_N$$

$$\text{or } V_0 - V_{DC} = 2.8 V_N$$

For the biased diode measured in a  $50 \Omega$  circuit,

$$\begin{aligned} \text{Tangential Power} &= \frac{2.8 V_N}{V_{OUT}} = \frac{\left(1 + \frac{50}{R_S}\right)^2 (2.8 V_N)}{3750} \\ &= 0.78 \left(1 + \frac{50}{R_J}\right) \sqrt{2kTB[R_B + 2R_a + 2R_S]mW} \end{aligned}$$

The tangential sensitivity is the tangential power expressed in –dBm. For a diode with 50  $\mu A$  bias ( $R_J = 560 \Omega$ ) measured with a video bandwidth of 10 MHz, this is

$$\begin{aligned} TSS &= 10 \log_{10}(2828 V_N/V_0) \\ &= 10 \log_{10} \left[ 0.92 \sqrt{2kTB[560 + 2R_a + 2R_S]} \right] \\ &= 48.8 \text{ dBm for } R_a \sim 1200 \Omega \end{aligned}$$

Note that if the diode has high  $1/f$  noise, the tangential sensitivity will be reduced considerably.

If the circuit is matched to the diode, the tangential sensitivity will be significantly increased. In this case the TSS is

$$\begin{aligned} \text{Tangential Power} &= \left( \frac{1 + \frac{R_S R_B}{X_C^2}}{18 R_B} \right) 2.8 V_N \\ &= 0.157 \left( 1 + \frac{R_S R_B}{X_C^2} \right) \sqrt{\frac{2kTB}{R_B} \left[ 1 + \frac{I_S}{I_0 + I_S} + 2 \frac{R_S + R_B}{R_B} \right]} \end{aligned}$$

For a zero bias detector diode,  $I_0 = 0$  and

$R_S = R_0 - R_B = Z_V - R_B$  so the tangential sensitivity is:

$$\text{TSS} = 10 \log_{10} \left[ 0.157 \left( 1 + \frac{R_S Z_V}{X_C^2} \right) \sqrt{\frac{4kTB}{Z_V} \left( 1 + \frac{R_a}{Z_V} \right)} \right]$$

If you assume typical values as  $X_C = 200 \Omega$ ,  $B = 10 \text{ MHz}$

$R_a = 1200 \Omega$ , and  $R_S = 20 \Omega$ , then the result is:

$$\begin{aligned} \text{TSS} &= 10 \log_{10} \left[ 4.6 \times 10^{-5} (1 + 0.0005) \sqrt{\frac{1}{Z_V} \left( 1 + \frac{1200}{Z_V} \right)} \right] \\ &= -55 \text{ dBm for } Z_V = 2000 - 5000 \Omega \end{aligned}$$

### Figure of Merit (FM)

The measurement of TSS is complicated by the fact that the apparent peak noise voltage may not be exactly  $1.4 V_N$ . Depending on the intensity setting of the oscilloscope, the apparent peak noise can be much larger than this, resulting in an error of several dB in the apparent TSS.

To take the operator dependence out of the TSS measurement, FM is introduced, which is defined by

$$\text{FM} = \frac{E_0}{\sqrt{Z_V + R_N}}$$

For diodes with zero bias the TSS is calculated from the FM by the formula

$$\text{TSS} = 10 \log_{10} \frac{\sqrt{4kTB}}{\text{FM}}$$

For biased diodes, the situation is slightly more complicated

$$S = 10 \log_{10} \left( \frac{\sqrt{4kTB}}{\text{FM}} \right) + 5 \log_{10} \left( \frac{2Z_V + 2R_a}{Z_V + 2R_a} \right)$$

The relationship is even more complicated if 1/f noise is considered which may be necessary if the diode is biased.

### High Voltage Output

At high signal levels, the detector will begin to deviate from square-law behavior. This begins to happen when  $V_J = 0.028 \text{ V}$ . For these signal levels, the sensitivity can be calculated from the same formulas as for the crystal current of a mixer if  $V_T$  is replaced by  $V_{F1} - V_{DC}$ . At high signal levels, the diode will develop enough reverse bias to keep the crystal current at the value  $I_0$  and the output voltage will approach twice the signal voltage,  $V_S$ . Therefore:

$$V_{DC} - V_F \cong 2V_S = -\sqrt{8Z_0^2 P_{RF}}$$

This behavior is called linear detection because of the linear relationship between  $V_{DC}$  and  $V_S$ .

At higher power levels, the reverse bias behavior of the I-V curve becomes important; as the reverse voltage approaches  $V_B$ , the slope of the reverse characteristic becomes comparable to  $Z_0$ , and begins to lead down the circuit. At a little higher power, the diode starts rectifying in the reverse direction as well as in the forward direction, and this results in a limitation of the output voltage.

The whole input/output characteristic of a detector is illustrated in Figure 12.

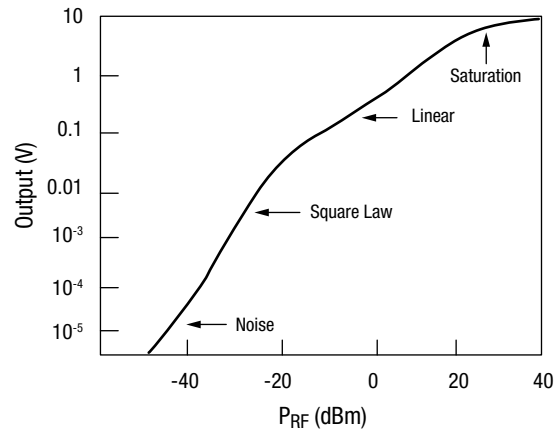


Figure 12. Detector Output Characteristics

### 1/f Noise

Excess noise due to surface static and traps often has 1/f frequency spectrum instead of the uniform spectrum characteristic of thermal noise and shot noise. That is, the noise power per unit bandwidth has a behavior:

$$\Delta(V^2_{N1}) \sim \frac{A}{f} \Delta f$$

To find the total noise voltage, the actual lower frequency limit,  $f_L$ , of the video amplifier must be known.

$$V_{N1}^2 = \int_{f_L}^{f_L + \frac{B_A}{f}} df = A/n \left( \frac{f_L + B}{f_L} \right)$$

Combining this with the thermal and shot noise expressions gives

$$V_{N1}^2 = A \ln \left( 1 + \frac{B}{f_L} \right) + 2kTB \left[ R_S \left( 1 + \frac{I_S}{I_0 + I_S} \right) + 2R_a + R_S \right]$$

It is convenient to eliminate the constant A by defining a noise corner frequency  $f_N$ , the frequency at which the  $1/f$  noise is equal to the shot noise.

$$f_N = \frac{A}{2KTR_J}$$

In terms of noise corner,

$$V_{N1}^2 = 2kTB \left\{ R_B \left[ 1 + \frac{I_S}{I_0 + I_S} + \frac{f_N}{B} / n \left( 1 + \frac{B}{f_L} \right) \right] + 2R_a + R_S \right\}$$

The noise corner can be specified for a diode, but this is complicated by the fact that for typical diodes the excess noise does not have an exact  $1/f$  spectrum, and also because the noise corner can depend on bias conditions. At Skyworks, the  $1/f$  noise output is measured in a bandwidth of 60 kHz (with  $f_L = 8$  Hz) as a measure of  $1/f$  noise. This is sufficient as a qualitative measurement of noise corner frequency, since  $V_{N1}^2$  is proportional to  $f_N$ . It is interesting to note that for a 50  $\mu$ A biased diode with a noise corner of less than 3 kHz, the noise output will be less than a 560  $\Omega$  resistor.

## Detector Configuration

### High Sensitivity

In this type, an impedance transformer is used to raise the impedance to as high a value as practical. Ideally, this should be the zero bias resistance of the diode, but this approach is limited by the  $R_S$  and  $C_J$ . It is also limited by bandwidth considerations and losses in the impedance transformer. Narrow-band detectors with voltage outputs of 10–30 mV/ $\mu$ W can be achieved this way. Tangential sensitivity approaching -70 dBm (in a  $\ll 1$  MHz video bandwidth) is achievable with good diodes, high  $Z_0$  (over 10 K), and low noise video amplifiers. Even higher sensitivity can be obtained by reducing the video bandwidth. A schematic is shown in Figure 13.

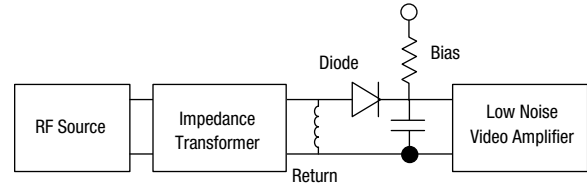


Figure 13. Typical Detector Circuit—High Sensitivity

### Wideband

A detector circuit uses a wider band impedance transformer or balun and is limited to a much smaller impedance at the diode, usually 50–200  $\Omega$ . For the 50  $\Omega$  type the best voltage sensitivity is 3600  $\mu$ V/ $\mu$ W, (unless the diode package increases the impedance at the chip above 50  $\Omega$ ), and tangential sensitivities are limited to about -54 dBm (in a 50 MHz band). The configuration is shown in Figure 14.

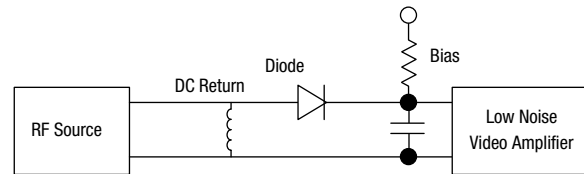


Figure 14. Typical Detector Circuit—Wideband

### Flat Detector

The above configuration has a reasonable flat response if the RF source is well matched, but has a high VSWR. Therefore, it is sensitive to any mismatch in the source which will then reflect back some of the reflected signal. To avoid this, a 50  $\Omega$  resistor can be included to eliminate the reflections, but this halves the signal voltage available at the diode, and reduces the output to less than 1 mV/ $\mu$ W, and the TSS will not be more than -48 dBm. However, the extremely wide bandwidth and low VSWR of this type of detector make it very useful. The circuit is shown in Figure 15.

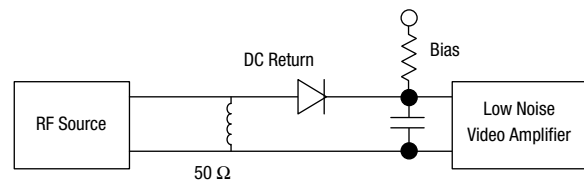


Figure 15. Typical Detector Circuit—Flat Response



### Matched Pairs

Detectors that must operate over a temperature range, or must be insensitive to variations of bias supply voltage, must have the reference voltage,  $V_0$ , built into the detector. This can be done by using an identical diode as a reference. For this reason, detectors are often sold in matched pairs. A typical circuit is shown in Figure 16.

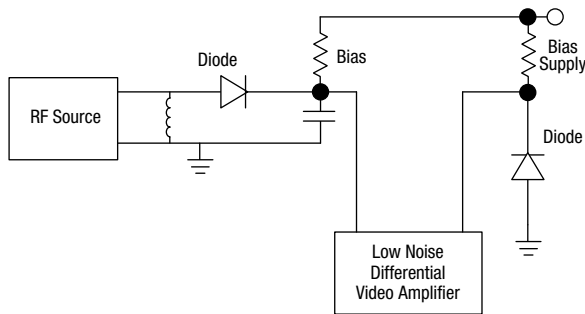


Figure 16. Temperature Compensated Detector

### Parameter Tradeoffs

#### Bias vs. No Bias

Although the zero-bias detector diode looks like a good way to reduce circuit complexity, applying bias to a diode reduces the noise temperature of the resistance  $R_B$  at video frequencies. In addition, the bias resistor can be chosen to compensate for the natural temperature variation of  $R_J$  (which is proportional to absolute temperature in K for constant current). That is, if the resistance is inversely proportional to  $T$ , then  $R_B$  will be constant over temperature. The video impedance of a zero-bias diode is very temperature dependent. However, a diode operated at zero bias has no  $1/f$  noise. Therefore, this type of diode is the choice for audio frequency output, such as motion detectors. The lack of bias resistor also simplifies the design of impedance matching networks for narrowband, high sensitivity detectors.

Caution should be used in selecting diodes for use in unbiased detector circuits because deviation from square-law behavior can occur at low levels. If a mixer diode or a detector diode not designed for zero-bias operation is used without bias, the small

signal resistance,  $R_B$ , (video impedance) will be too high. In this case, it will be impossible to get a good match to the diode, even over a narrow bandwidth, and the RF power will be dissipated in lossy circuit elements. Thus the RF voltage at the junction will be much less than it should be, resulting in lower TSS and voltage sensitivity at very low signal levels. When the signal level is increased, the diode self-biases to a lower resistance,  $R_B$ , and more of the power reaches the diode. Therefore, the voltage sensitivity increases. The net result is that the detected response is faster than square law at very low signal levels, approaching fourth law or fifth law in many cases. This results in substantial error if a square-law characteristic is assumed, as in many power level measurement applications. This effect does not happen if a zero-bias Schottky diode is used, properly matched, in a low loss detector mount.

#### $C_J$ vs. Frequency

For most purposes, it is sufficient to have  $X_C > 150 \Omega$  in a detector diode. This leads to the following “rule of thumb” (for  $C_{J0}$  in pF):

$$C_{J0} < 1.1/f \quad (f = \text{signal frequency in GHz})$$

which is good for “typical” detectors. However, this is usually too stringent for  $50 \Omega$  detectors, especially flat detectors. Conversely, in the case of high output detectors, the  $C_J$  may not allow enough bandwidth. In this case, lower  $C_J$  should be traded for more  $R_S$ , since  $R_S$  matters less in detectors than in mixer diodes. Some detector designers use diodes with  $R_S$  as high as  $100 \Omega$ .

#### $1/f$ Noise

Detector diodes are usually used in systems whose video bandwidth extends below 10 kHz. In this case  $1/f$  noise voltage becomes much more important than for typical mixer diodes. It can be specified by a noise corner frequency, or by an upper limit or the noise output in a particular audio band. Skyworks diodes are screened using an audio amplifier with a response from 8 Hz to 60 kHz (at 50  $\mu\text{A}$  bias) when low  $1/f$  noise is specified.

## **Burnout**

### **General**

Schottky barrier diodes are more subject to burnout due to incident RF pulses than are typical junction diodes, even the very small junction diodes used in microwave systems. Basically, there are three reasons for this:

1. The barrier diameters are very small (less than 0.5 mil diameter), resulting in high dissipated power density.
2. The metal semiconductor contact is not as stable chemically as a junction between two regions deep within a semiconductor, and can be damaged by temperatures on the order of 400 °C.
3. Because of lack of charge storage (conductivity modulation) the resistance of the diode at high currents will not be very low (typically around 10  $\Omega$ ). Therefore, the diode does not protect itself as well as junction diodes, whose dynamic resistance may drop to a few tenths of an  $\Omega$  at high forward currents or high incident RF power.

### **Dependence of Burnout Power on Pulse Length**

A diode will begin to degrade when some part of the junction reaches a certain high temperature. The exact temperature depends on the metallurgy used, and on the degree of perfection of the junction, especially at the edges. All of the metallurgies used in Skyworks Schottky diodes are good for at least 350 °C.

For RF pulses less than 5 ns long, the temperature rise is directly proportional to the total pulse energy dissipated in the epitaxial layer just under the barrier metal. This would appear to lead to the conclusion that the energy content of the RF pulse determines whether the diode will burn out, but the situation is not that simple. For example, if the incoming RF pulse has a peak-to-peak voltage (at the diode) less than the diode breakdown, there will be relatively little dissipation in the junction. At higher pulse voltages, the percentage of the incoming energy that is dissipated will increase. The amount of dissipation in the diode will also depend on the circuit, which determines what happens to the energy reflected by the diode. All that can be said without exact knowledge of both the diode and the circuit is that the susceptibility of the diode to burnout is related to both the power (or voltage) in the incoming RF pulse and pulse duration.

For longer pulse lengths (5 ns to 100 ns) the temperature of the diode junction is dominated by thermal diffusion, and the temperature rise will be proportional to the square root of time for a given power dissipation. Therefore, the burnout is not expected to depend on the total dissipated energy for pulse lengths over 5 ns, but is more related to the incident power (if the peak-to-peak voltage is high enough).

If the pulse length is longer than about 100 ns, the maximum junction temperature is controlled by the thermal resistance of the chip and package. In this case, the burnout rating will depend to some extent on the quality of the heat sink used for the diode.

### **Burnout vs. Frequency**

Because the capacitance of mixer diodes must be smaller at higher frequencies, smaller diameter junctions are used. This, of course, makes higher frequency diodes more susceptible to burnout than low-frequency diodes. For short pulses, the burnout power is approximately inverse with frequency, whereas for long pulses, or CW, the effect is more gradual.

Detector diodes typically have lower capacitance and thus smaller junctions than mixer diodes. This is often not an issue, because detector diodes are not usually exposed to high power RF pulses. However, if the system requires that they be exposed, then the burnout rating should be given serious consideration in selecting the diode.

### **Transients and Electrostatic Discharges**

For the same reasons outlined above, Schottky diodes are subject to burnout due to circuit transients and electrostatic discharges. (The majority of diode burnout problems encountered are due to these two causes.)

Electrostatic discharge is becoming even more of a problem than it used to be, since most people wear plastic clothes and shoes. A person's hand can easily acquire a charge of over 5000 V on a dry winter day, and when it touches the diode, it can release as much as 10 amperes of short circuit current in less than a nanosecond. The solution is to always ground your hand, tweezers, pliers, or any other tool before touching the diode. (Also, both terminals of the circuit it goes into should be grounded—someone may have touched one of the conductors and charged it.)

Another way of damaging diodes is to check the front-to-back ratio with a conventional multimeter to see if it is still a diode. (It won't be.) The ohmmeter batteries in a typical multimeter range from 1.5–9 V, and the leads will be charged to this voltage until they touch the diode. The discharge is usually sufficient to burn out the diode within about 2 nanoseconds (the longer the leads, the worse the effect). This effect can be avoided by using a push-to-test switch across the diode when testing it in this way, or by using a curve tracer instead of a multimeter. Some DVMs are just as bad as multimeters, because they produce digital pulses which hit the diode.

Switching transients in actual circuits can cause the same effect, if there is sufficient inductance between the source and the diode. This can be eliminated by using a small capacitor between the source of the transient and the diodes.



## APPLICATION NOTE

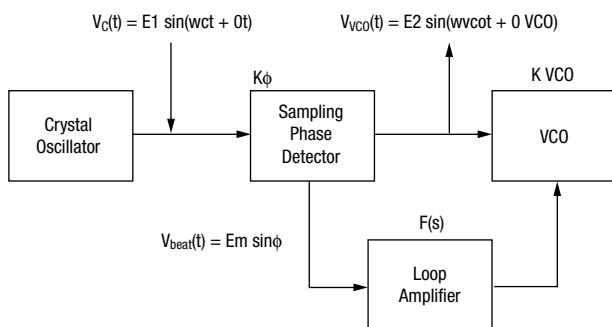
# Theory and Application of Sampling Phase Detector

The phase lock of a Voltage Controlled Oscillator (VCO) for VHF, UHF and microwave frequencies is very important in communications and radar application. It combines the far-out phase noise of fundamental oscillators, especially in the microwave frequency range (100 kHz away from carrier frequency and beyond), the excellent long-term stability, and the close-in phase noise of a crystal oscillator (from carrier frequency to 100 kHz away).

A voltage-controlled oscillator can be phase locked by two methods:

1. Digital phase lock: This is usually achieved by using a frequency divider to divide the higher frequency of the VCO to the same frequency of the crystal reference. A digital phase detector is then used to acquire the phase lock. The advantage of this method is that it is self-acquiring and can operate at very low frequencies. It is widely used at low frequencies from 1 MHz up to 3 GHz. However, this method also has two disadvantages. First, the noise floor of the divider will limit its phase noise; and second, at microwave frequencies it will not be economical.
2. Analog phase lock: This is achieved by using an SRD as a comb generator to create a comb of reference frequencies to the frequency of the VCO. The phase detecting is accomplished by using a mixer to detect the phase differences between the reference and the VCO. The Skyworks sampling phase detector is designed to perform the analog phase lock in a simple and more economical way.

The sampling phase detector used in phase lock of a VCO operating by the theory of principles of feedback control systems is shown in Figure 1.



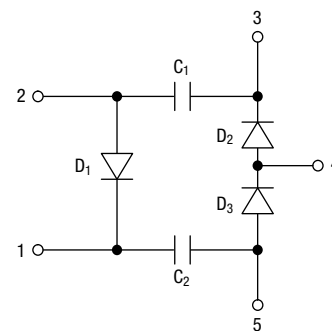
**Figure 1.**

The error signal output of the sampling phase detector  $V_{beat} = E_m \sin\phi$  is the differential phase error between the VCO and the crystal oscillator. The loop amplifier amplifies the error signal to the VCO and corrects the VCO to be in phase with the crystal oscillator. At the same time, the loop amplifier acts as a low pass filter and filters away the crystal frequency.

This method of phase lock will achieve the lowest phase noise possible beside the theoretical degradation of  $20 \log N$ , where  $N$  is the multiplication factor between the crystal oscillator and the VCO. The other circuits that will generate additional noise are the driver amplifier, sampling phase detector, and the loop amplifier. They may all contribute to further degradation in phase noise (typically 1 dB if the crystal oscillator has a noise floor of -155 dBc/Hz or 3 dB if the crystal oscillator noise floor is -160 dBc/Hz).

## Circuit Description and Operation of the Sampling Phase Detector

The sampling phase detector is shown in figure 2.



**Figure 2.**

The sampling phase detector consists of three main parts integrated to form a module. The integrated part has the advantage of minimized size and improved performance, as it eliminates the circuit self-resonance, especially at higher frequencies (13 GHz and above). The following is the description and function of the three parts:

1. SRD: The SRD takes an input crystal frequency and generates a sharp narrow pulse (in the time domain) or combs (in the frequency domain). The period of the pulse is the same as that of the input crystal frequency. The operating range of the sampling phase detector is heavily dependent on the narrow pulse generated by the SRD or the transition time of the SRD. The SRD also needs to recover before the next cycle of the crystal frequency. This is defined by the carrier lifetime of the SRD. Thus, for a selected input crystal frequency and output phase locked VCO frequency, a special SRD is selected in the particular sampling phase detector. There are two ways to optimize the SRD:
  - a) For narrow-band operation, the SRD is selected to optimize at the first peak of  $\sin X/X$  wave form, which generates the maximum beat note at a specific frequency.
  - b) For broadband operation, the SRD is selected to 70% of the first null of the  $\sin X/X$  wave form, which generates a broad band of combs of virtually equal amplitude. This is more suitable for wide bandwidth operation, as it generates equal beat note over a wide frequency range.
2. Capacitors: The capacitors in the sampling phase detector act as a switch. The switch turns on/off by the pulse generated by the SRD. Therefore, these capacitors should be a single layer microwave capacitor that has very low ESR and high self-resonating frequency well above the operating frequency of the sampling phase detector. The value of the capacitor is typically inversely proportional to the operating frequency. Thus, the higher the operating frequency, the smaller the value of the capacitor. The capacitor controls the efficiency of the transfer of energy or signal from VHF (crystal or multiple frequency) to microwave frequency (VCO). As the capacitor turned "ON," it quickly charged up to its peak RF level, and when turned "OFF," it quickly fully discharged its energy. A more efficient transfer of energy results in lower phase noise.

3. Series pair Schottky diodes: The series pair Schottky diodes in the sampling phase detector are used to detect the errors between the microwave VCO frequency and the crystal reference. The Schottky diodes are turned on and off by the gated capacitor. When turned on, a sample of microwave frequency is compared with the switch frequency. An error frequency proportional to the differences will be generated as an error signal output or beat note. This error signal will be processed through the loop amplifier for phase lock (refer to figure 1). The crucial parameter on the Schottky diodes is the balance between the series pair, especially over temperature. Also, the drive level of the microwave signal sometimes requires medium or high-level Schottky diodes instead of the normal low-level diodes. The drive level should be proportional to the diodes used. Any underdrive results in temperature and unit-to-unit variation. Excessive overdrive will result in increased noise floor. Therefore, the diodes should be selected based on the operation parameter design for them. Skyworks has a variety of sampling phase detectors for all applications.

### Characterization and Evaluation of Sampling Phase Detector

There are two circuits widely used to evaluate and characterize the performance of the sampling phase detector. Figure 3a and 3b show the single-end and double-end configuration of the test circuit. These circuits can also be used in real application for phase locked VCO.

To evaluate the sampling phase detector, certain precautions have to be taken to ensure that the data are varied and repeatable. The following is the sequence of setup and test equipment required for the test.

### Test Equipment

1. Stable signal source: Crystal oscillators or signal generators. If a signal generator is selected, a synthesized signal generator is preferred.
2. Power amplifier: Frequency range of 10–500 MHz. Capable of 15 dB min. gain and a linear power output of 25 dBm min.
3. Sweep microwave signal generator: Should cover the microwave frequency range to be tested. Power output up to 5 dBm min.
4. Oscilloscope: A dual channel 400 MHz oscilloscope will be adequate for this test.

10 TO 1 TURN RATIO  
STEP DOWN TRANSFORMER

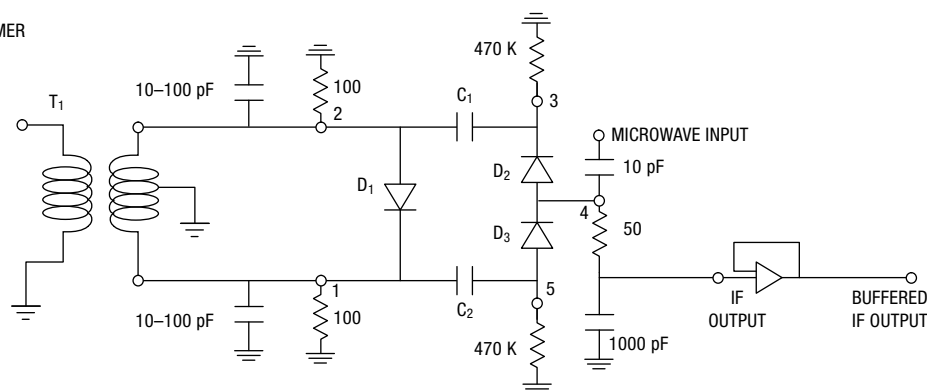


Figure 3a. Test Circuit for Sampling Phase Detector

3 TO 1 TURN RATIO  
STEP DOWN TRANSFORMER

REFERENCE INPUT  
100 MHz SINE WAVE  
+17 to +20 dBm

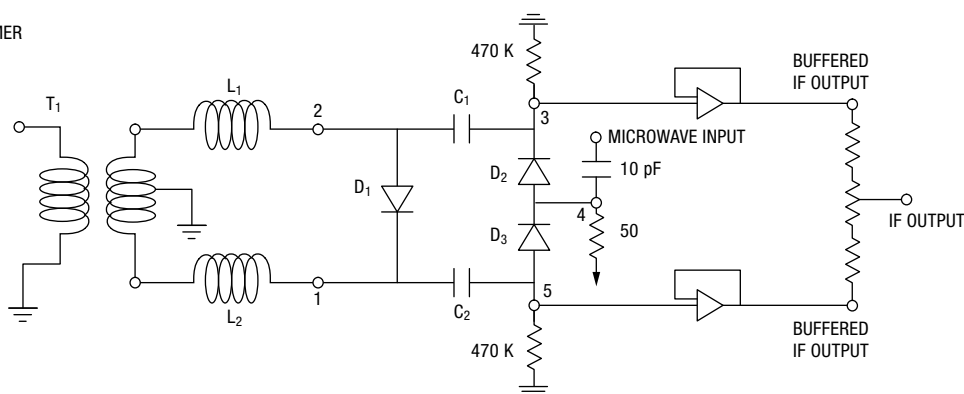


Figure 3b. Test Circuit for Sampling Phase Detector

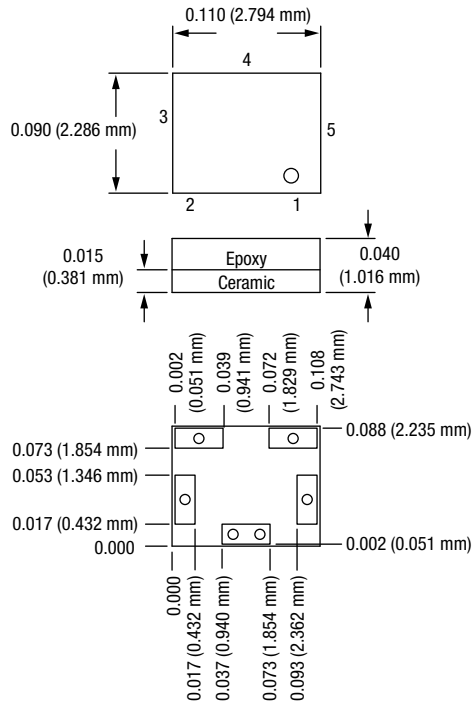
### Test Setup

1. Set up the reference signal, typically 100 MHz @ 17 dBm or 16 V<sub>pp</sub>, across the primary of the transformer. The reference signal should have minimum harmonic contents.
2. Between the secondary of the transformer and the sampling phase detector is a matching network, which isolates the transformer from the sampling phase detector. The matching network also acts as a termination and tune circuit (Figure 3a) or as a short at reference frequency and an open circuit at microwave frequency. The transformer should have an amplitude balance of 0.5 dB and a phase balance of 2 degrees at the operating frequency of 100 MHz.
3. The microwave signal input is terminated by a thin-film, high-frequency, 50  $\Omega$  terminating resistor. The coupling input capacitor acts as a high pass filter, which allows the microwave frequency to pass through, but blocks the lower reference frequency. The beat note output is connecting to the operational amplifier, which is wired as a unity gain buffer.

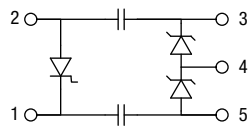
The operational amplifier is used as a low pass filter and it also lowers the impedance of the Sampling Phase Detector output. As a result, the measured beat note will be consistent and will not be loaded down by the capacitance of the scope probe. The frequency set for the microwave source is the frequency we set to test. The power level of the microwave signal is typically set to 0 dBm.

Once all the test conditions are set, the beat note can be measured at the output using the oscilloscope. The input reference signal level and the microwave signal levels are adjusted to measure the 1 dB compression point of the sampling phase detector. The data can be taken across the entire operating bandwidth. Temperature data can be taken in the same manner. From these data, one can select the proper reference frequency and drive level, as well as the proper microwave frequency and power level, which will ensure that their system requirements are met.





### -111 Package Outline



**Schematic Diagram**

## Application of the Sampling Phase Detector

The most widely used application of the sampling phase detector is for phase locking a Dielectric Resonator Oscillator (DRO). The phase-locked DRO is mainly used in the wireless industry, communication systems and RADAR as a stable LO. In all these systems, low cost simplicity, reliability, and good performance are required. Here, we discuss the application of the sampling phase detector used in the function of a phase-locked DRO.

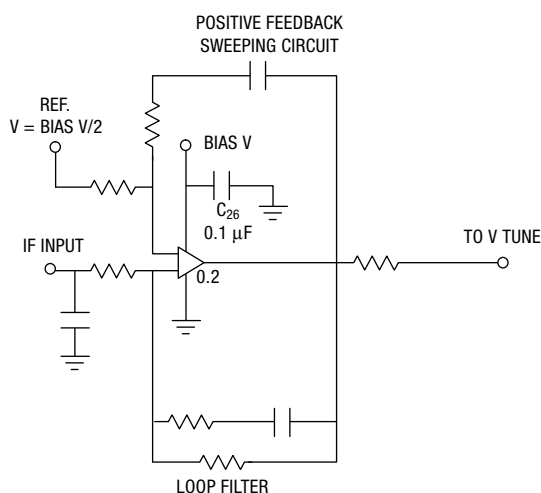
To design a good phase-locked DRO the first requirement is to define the performance of all the components as follows:

1. **Crystal oscillator:** To ensure the best performance, a 100 MHz 3rd overtone SC-cut crystal is selected to design a crystal oscillator, which can achieve a noise floor of -0.170 dBc/Hz. The cost of the crystal is high, approximately \$20.00 each in 50K quantities. The alternative is to use an AT-cut crystal, which costs approximately \$4.00 each in 50K quantities. However, the trade-off is 3 dB degrading in phase noise and some increase in the long-term aging rate.
2. **DRO:** The DRO performance is very important. The DRO should have a buffer amplifier to isolate the load pulling and also to achieve an output power of 19 dBm, which is adequate for most applications as LO. The free running phase noise of the DRO at 100 KHz away from carrier should be -116 dBc/Hz minimum over temperature in the operating range (9–13 GHz). The operating range is defined as the linear tuning range of the DRO, which should be twice the temperature drift of the DRO over its operating temperature range. The linear tuning range is defined as the tuning range over which the tuning sensitivity of the DRO varies less than 10%.
3. **Sampling phase detector:** The sampling phase detector SPD1102-111 will suit for this design.
4. **Loop amplifier:** For low cost, an Analog Device OP113 will be adequate for the design.
5. **Low noise power supply:** A low noise power supply is very important for the performance of the phase-locked DRO. In the system, it is preferable to have local, on-board, low noise regulators to supply the voltage source to the individual circuits. This will also isolate the interference from outside and minimize the voltage variation created by current variation and power wire length variation.

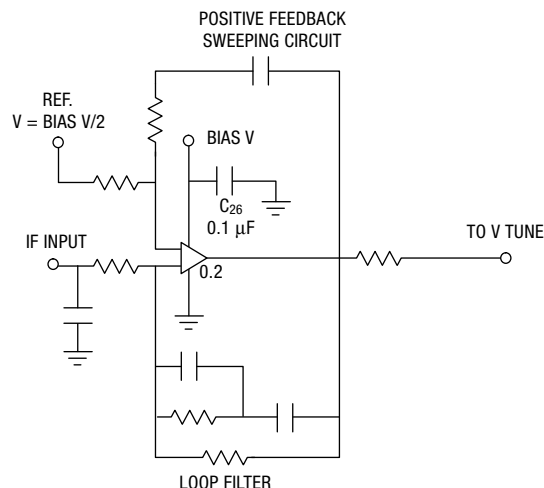
In this design, the sampling phase detector circuit we selected is shown in Figure 3b. This was selected because most systems do not have negative voltage available. This allows us to use a single supply and make everything simple and universally adaptable to most systems. The crystal oscillator will be amplified and drive the primary of the transformer with a power level of 16 V peak-to-peak. The DRO/Amp. output is passed through a 16 dB directional coupler. This results in a 2 dBm microwave signal to the sampling phase detector. This will generate a beat note of 400 mV peak-to-peak output. The loop amplifier used is a second-order loop (Figure 4a), and the phase noise loop bandwidth was set at 300 kHz.

A wide loop bandwidth will be less susceptible to microphonics. This is very important in the wireless industry, as the unit is normally mounted outside and is subject to such environmental effects as wind, rain and hail. In this configuration, we can achieve a system phase noise of -80 dBc/Hz at 100 Hz; -104 dBc/Hz at 1 kHz; -114 dBc/Hz at 10 kHz; -124 dBc/Hz at 100 kHz; -136 dBc/Hz at 1 MHz; -155 dBc/Hz at 5 MHz. The system noise floor limits the phase noise measurement at 5 MHz on the HP Phase Noise Measurement System. If further suppression of noise is required, a higher order of loop amplifier design can be selected as shown in Figures 4b through 4d.

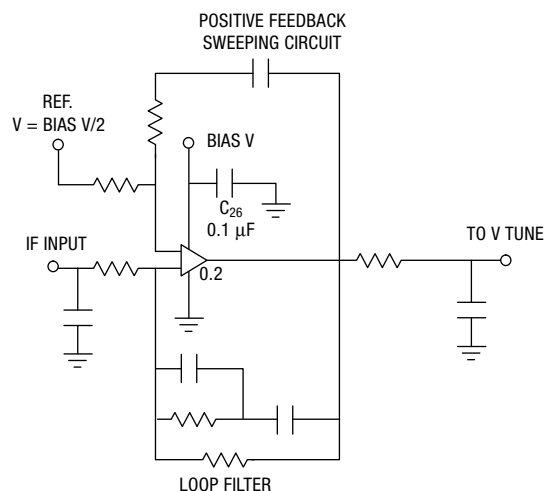
The simplicity of the sampling phase detector used in the phase-locked DRO allows us to fabricate the complete circuit including the reference crystal oscillator all on one small PC board. The integration of the high-frequency components into one single package allows us to eliminate wire-bonding, and as a result, create a complete system which can be automated using surface mount technology.



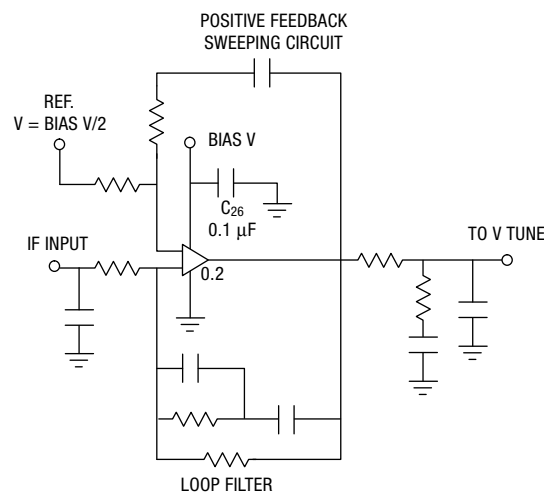
**Figure 4a. Second-Order Loop**



**Figure 4b. Third-Order Loop**



**Figure 4c. Fourth-Order Loop**



**Figure 4d. Fifth-Order Loop**



## REFERENCE MATERIAL

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## Quality/Reliability

### Certifications

As an industry leader, Skyworks has demonstrated its quality leadership and strengthened its commitment to customer satisfaction through formal, third-party registration to ISO 9001, ISO/TS 16949 and ANSI/ESD S.20.20.



### ISO 9001

ISO 9001 is an internationally recognized Quality Management System standard that promotes customer satisfaction through continual improvement of the system's effectiveness. ISO 9001 provides a model for a Quality Management System which focuses on the effectiveness of the processes in a business to achieve desired results. The standard promotes the adoption of a process approach emphasizing the requirements, added value, process performance and effectiveness, and continual improvement through objective measurements.

### ANSI/ESD S.20.20

ANSI/ESD S20.20 is a standard for the Development of an Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies and Equipment. The standard covers the requirements necessary to design, establish, implement, and maintain an Electrostatic Discharge (ESD) Control Program.

### ISO/TS 16949

One of the major challenges facing today's manufacturers is that, even though there is a low failure probability for each individual component, the total failure probability for all parts combined may reach unacceptable levels. The ISO/TS 16949 standard answers this challenge by defining requirements focused on continual improvement, and the understanding of process interaction. It also creates an implementation framework for customer specific requirements, and includes clear requirements for development processes and techniques to prevent problems in the earliest possible stage of product development.

Jointly developed by International Automotive Task Force (IATF), ISO/TS 16949 is the automotive industry's international quality management system standard intended to answer the need for global consistency, continual improvement, and increased customer satisfaction. It is approved and released by the International Organization for Standardization (ISO).



## What Certification Means to You

- Partnering with a company that has made a commitment to quality
- Doing business with an organization with a recognized management system model
- Assurance that necessary resources have been dedicated
- Consistent processes and products
- A management team that has established clear quality objectives and targets that are constantly monitored and analyzed
- Quality systems and procedures that are continuously audited and improved



## Quality Policy

Skyworks has adopted a simple yet powerful quality policy that guides business decisions day-in and day-out.

Skyworks is committed to the never-ending quest for perfect quality.

Our ultimate goals:

- No Field Failures
- No Customer Returns
- No Reliability Failures
- No Yield Loss

## ISO 14001:2004

As an industry leader, Skyworks is committed to the protection and preservation of the environment in all its business operations. We understand that our actions today can have environmental impacts tomorrow. Improvements at our facility will affect our customers and ultimately consumers. To this end, we have an established ISO 14001 certified Environment Management System by which we operate. We build products in consideration of regulatory and industry requirements, such as Restriction of Hazardous Substances Derivative (RoHS), and offer lead (Pb)-free, RoHS-compliant, and Green™ solutions to meet the needs of our customers in today's environmentally-conscious market.

## Quality Testing Programs

Environmental and electrical tests are used to verify and improve the reliability of commercial semiconductor components.

### Six Sigma

As we strive for continuous improvement, Skyworks has adopted the Six Sigma approach, a practical methodology that applies statistical tools and methods to aid in continuous process improvement.

### Quality Conformance Testing

Quality conformance testing (also called lot acceptance testing), is testing performed on a sample of the lot to determine that the devices meet specified electrical and mechanical requirements.

### Qualification Test

Qualification testing is used to determine that the manufacturer of a device can supply devices that meet the full electrical and environmental capability requirements of the customer's specification. Skyworks qualification testing is conducted according to JEDEC standards.

### Ongoing Reliability Monitoring Program

The reliability monitor program is administered and executed by the Quality Assurance Department. The intent of this program is to:

- Provide an ongoing evaluation of our product reliability.
- Maintain a pulse on the fabrication and assembly processes.
- Samples are selected quarterly from representative qualified products from the production line that have passed functional electrical test. The product selection lists will include considerations for forecasted product volume and customer requests.

## Product Qualification Testing

Test <sup>(1)</sup>	Qty. (SS x lot)	Conditions	Standard	Endpoints	Accept Criteria
Dynamic operating life (HTOL)	77 x 1	T <sub>CASE</sub> = 125 °C or T <sub>J</sub> or T <sub>CH</sub> = 150 °C; Depends on accel factor and life expectancy. Typically 1000 hours	JESD22-A108	Electrical test, pre and post stress with additional readpoints per qual plan	0 fail/77
ESD – HBM	3 per level per partition <sup>(2)</sup>	Post-zap 1 positive discharge and 1 negative discharge per pin for each pin combination	JESD22-A114	Electrical test, pre and post stress	Pass/fail criterion is ATE functional test w/production limits
ESD – MM	3 per level per partition	Post-zap 1 positive discharge and 1 negative discharge per pin for each pin combination	JESD22-A115	Electrical test, pre and post stress	Pass/fail criterion is ATE functional test w/production limits
ESD – CDM	3 per level	Post-zap 5 discharges per pin; field-induced, charge-discharge method	JESD22-C101	Electrical test, pre and post stress	Pass/fail criterion is ATE functional test w/production limits
Preconditioning	231 x 1	Sequence: visual inspection min. 25X, 24 hr bake at 125 °C, moisture soak per MSL, reflow 3x	JESD22-A113	Electrical test, pre and post stress	0 fail/231
HAST or THB or unbiased HAST or autoclave	77 x 1	96 hrs, 130 °C, 85% RH, 18.6 psig or 1000 hrs, 85 °C, 85% RH, or 96 hrs, 121 °C, 100% RH, 15 PSIG; preconditioned samples	JESD22 -A110 (HAST) -A101 (THB) -A102 (AC), -A118 (unbiased HAST)	Electrical test, pre and post stress	3% LTPD (0 fail/77)
Temperature cycling	77 x 1	-65 °C to +150 °C 500 cycles, or -55 °C to +125 °C 1000 cy. Preconditioned samples	JESD22-A104	Electrical test, pre and post stress	3% LTPD (0 fail/77)
High temp storage	77 x 1	150 °C 500 hours (preproduction) 1000 hours (production) Preconditioned samples	JESD22-A103	Electrical test, pre and post stress	3% LTPD (0 fail/77)

## Ongoing Reliability Monitor Program

Test	Qty.	Standard	Endpoints	Accept Criteria
Dynamic operating life (HTOL)	77/lot	JESD22-A108	48 or 168 hours, and 1000 hours	0 fail/77
Preconditioning (PC)	154/lot	JESD22-A113	3X reflow	0 fail/154
HAST or unbiased HAST or autoclave	77/lot (from PC)	JESD22 -A110 (HAST) -A102 (AC), -A118 (unbiased HAST)	96 hours	3% LTPD (0 fail/77)
Temperature cycling	77/lot (from PC)	JESD22-A104	500 cycles	3% LTPD (0 fail/77)

\*Temp. cycle and THB/autoclave will be redone if the moisture sensitivity classification changes, otherwise these tests are repeated each year.

## ESD Awareness

Skyworks deploys state-of-the-art ESD controls from wafer fabrication through to assembly, test, and pack. In order to maintain device integrity, Skyworks has outlined critical ESD guidelines that should be followed as a minimum. Skyworks adheres to the requirements outlined in MIL-HDBK-263, MIL-STD-1686 and ESD Association 2.0 Handbook. GaAs products can be damaged at ESD voltages in the 250 V range. In this case, strict adherence to ESD Class 0 guidelines is recommended.

### Device Handling

Remove ESD-sensitive devices from protective containers at approved ESD work stations only.

ESD wrist straps are required when handling devices outside their ESD-protective packaging.

All personnel shall be properly grounded (footstraps/wrist straps) prior to opening static shielding bags.

ESD-sensitive devices should always be handled by the part body. Avoid touching the leads. When hand tools are required to accomplish an operation, use only tools that are dissipative, conductive, or treated with topical antistat.

### ESD Workstation

Your ESD-safe work area should follow the requirements outlined in MIL-HDBK-263 and ESD Association Handbook 2.0. The following requirements are strongly recommended:

#### Personnel

The use of constant wrist strap monitors is highly recommended. This monitor guarantees that the connection to ground is continuously made. An alarm will sound when that connection is broken.

### Clothing

An ESD-protective garment (smock, etc.) shall be used at the workstation. While a person may be grounded using a wrist strap or foot strap, that does not ensure that certain clothing fabrics can dissipate a charge to ground. The use of a conductive smock is required.

### Floors

Conductive or dissipative ESD flooring shall be utilized whenever possible. This flooring shall be checked for ESD properties on a regular basis.

### Work Surfaces

Your ESD work surface shall be covered with soft dissipative material. This surface shall be tied to earth ground and shall be configured in a common point ground. In addition, the work surface shall be free of any static generating material, such as nonessential plastics, or cellophane tape.

### Equipment

All equipment used to process ESD-sensitive devices shall be checked for the generation of static charging. Whether soldering irons, wave solder machines, device insertion machines or test equipment, the generation of static electricity is of concern.

## ESD Component Classifications

ESD-sensitive components are classified according to their ESD withstand voltage using the test procedure described in this standard. The HBM ESDS components classification levels are shown below.

**ESD Component Classification**

JEDEC Standard	Test	Class	Voltage Range
JESD22-C101	Charged-Device Model CDM	1	<200 V
JESD22-C101	Charged-Device Model CDM	2	200–500V
JESD22-C101	Charged-Device Model CDM	3	500–1000 V
JESD22-C101	Charged-Device Model CDM	4	>1000 V
JESD22-A114	Human Body Model HBM	0	<250 V
JESD22-A114	Human Body Model HBM	1A	250–500 V
JESD22-A114	Human Body Model HBM	1B	500–1000 V
JESD22-A114	Human Body Model HBM	1C	1000–2000 V
JESD22-A114	Human Body Model HBM	2	2000–4000 V
JESD22-A114	Human Body Model HBM	3A	4000–8000 V
JESD22-A114	Human Body Model HBM	3B	>8000 V
JESD22-A115	Machine Model (MM)	A	< 200 V
JESD22-A115	Machine Model (MM)	B	200–400 V
JESD22-A115	Machine Model (MM)	C	>400 V

**JANTX Screening Requirement in Accordance with Table E-IV-MIL-PRF-19500**

Step	Process	Conditions	Comments	JANTX
1	Visual inspection	MIL-STD-750 - Method 2073		X
2	High temperature bake	MIL-STD-750 - Method 1032		X
3	Temperature cycling	MIL-STD-750 - Method 1051	Condition C	X
4	Constant acceleration	MIL-STD-750 - Method 2006	20,000G's min., Y1 axis only	X
5	Initial electrical test		Serialize, read & record	X
6	High temperature reverse bias	MIL-STD-750 - Method 1038	Condition A, t = 48 hrs	X
7	Interim electricals		Read and record	X
8	Burn-in	MIL-STD-750 - Method 1038	Condition B, t = 96 hrs	X
9	Final electrical test		Read and record	X
10	Delta calculation		Compare interim test to final test	X
11	PDA		Percent defective allowable = 10% max.	X
12	Fine leak	MIL-STD-750 - Method 1071	Condition H	X
13	Gross leak	MIL-STD-750 - Method 1071	Condition C	X
14	External visual inspection	MIL-STD-750 - Method 2071		X

**Group A Inspection in Accordance with Table E-V-MIL-PRF-19500**

Subgroup 1				
1	Visual and mechanical inspection	MIL-STD-750 - Method 2071	Sample size = 45 (0)	X
Subgroup 2				
1	Electrical testing		DC (static) @ T <sub>A</sub> = 25 °C, sample size = 116 (0)	X
Subgroup 3				
1	Electrical testing		DC (static) @ min. & max. operating temp., sample size = 116 (0)	X
Subgroup 4				
1	Electrical testing		Dynamic @ T <sub>A</sub> = 25 °C, sample size = 116 (0)	X
Subgroup 5			Not applicable for diodes	N/A
Subgroup 6			Not applicable for diodes	N/A
Subgroup 7			Not applicable for diodes	N/A

**Group B Inspection in Accordance With Table E-VIB - MIL-PRF-19500**

Step	Process	Conditions	Comments	JANTX
Subgroup 1				
1	Solderability	MIL-STD-750 - Method 2026	Sample size = 15 (0)	X
2	Resistance to solvents	MIL-STD-750 - Method 1022	Sample size = 15 (0)	X
Subgroup 2				
1	Temperature cycling	MIL-STD-750 - Method 1051	Condition C, sample size = 22 (0)	X
3	Fine leak	MIL-STD-750 - Method 1071	Condition H, sample size = 22 (0)	X
4	Gross leak	MIL-STD-750 - Method 1071	Condition C, sample size = 22 (0)	X
5	Electrical testing		DC @ T <sub>A</sub> = 25 °C, sample size = 22 (0)	X
Subgroup 3				
1	Steady-state operation life	MIL-STD-750 - Method 1027	Sample size = 45 (0)	X
2	Electrical testing		DC @ T <sub>A</sub> = 25 °C, sample size = 45 (0)	X
3	Bond strength	MIL-STD-750 - Method 2037	Sample size = 11 wires (0)	X
Subgroup 4				
1	Decap internal visual	MIL-STD-750 - Method 2075	Sample size = 1 (0)	X
Subgroup 5				
1	Thermal resistance	MIL-STD-750 - Method 4081	Sample size = 15 (0)	X
Subgroup 6				
1	High temperature life	MIL-STD-750 - Method 1032	t = 340 hrs @ max. rated storage temp., sample size = 32 (0)	X
2	Electrical testing		DC @ T <sub>A</sub> = 25 °C, sample size = 32 (0)	X

**Group C Inspection in Accordance with Table E-VII-MIL-PRF-19500**

Subgroup 1				
1	Physical dimensions	MIL-STD-750 - Method 2066	Sample size = 15 (0)	X
Subgroup 2				
1	Thermal shock	MIL-STD-750 - Method 1056	Sample size = 22 (0)	X
2	Temperature cycling	MIL-STD-750 - Method 1051	Condition C, sample size = 22 (0)	X
3	Fine leak	MIL-STD-750 - Method 1071	Condition H, sample size = 22 (0)	X
4	Gross leak	MIL-STD-750 - Method 1071	Condition C, sample size = 22 (0)	X
5	Moisture resistance	MIL-STD-750 - Method 1021	Sample size = 22 (0) (hermetic packages only)	X
6	Electrical testing		DC @ T <sub>A</sub> = 25 °C, sample size = 22 (0)	X
Subgroup 3				
1	Shock	MIL-STD-750 - Method 2016	Sample size = 22 (0)	X
2	Vibration, variable frequency	MIL-STD-750 - Method 2056	Sample size = 22 (0)	X
3	Constant acceleration	MIL-STD-750 - Method 2006	Sample size = 22 (0)	X
4	Electrical testing		DC @ T <sub>A</sub> = 25 °C, sample size = 22 (0)	X
Subgroup 4				
1	Salt atmosphere	MIL-STD-750 - Method 1041	Sample size = 15 (0)	X
Subgroup 5				
1	Thermal resistance	MIL-STD-750 - Method 4081	Sample size = 15 (0)	X
Subgroup 6				
1	Steady-state operation life	MIL-STD-750 - Method 1026	Sample size = 22 (0)	X
2	Electrical testing		DC @ T <sub>A</sub> = 25 °C, sample size = 22 (0)	X
Subgroup 7				
1	Internal water vapor	MIL-STD-750 - Method 1018	Sample size = 3 (0) (hermetic packages only)	X

## High Reliability Product Flow for Element Evaluation

Product	MIL-PRF-38534	Application
Bare Die	Class H Class K	Military Space

Skyworks provides Discrete “bare die” and beam-lead products with Class H and Class K element evaluation in accordance with MIL-PRF-38534 Table C-II for Microcircuit and semiconductor die and Table C-III for Passive devices.

IE: CLA4601-000 = Commercial Product Flow  
 CLA4601H000 = Class H  
 CLA4601K000 = Class K

## Chip Element Evaluation for Microcircuits and Semiconductors

Test Inspection	MIL-STD-883		Requirement	
	Method	Condition	Class H	Class K
Element electrical	Per product specification	On-wafer	100%	100%
Element visual	2010	A = Class K B = Class H	100%	100%
Internal visual	2010		10/0	10/0
Stabilization bake	1008	C	N/A	10/0
Temperature cycling	1010	C	N/A	10/0
Mechanical shock or Constant acceleration	2002 2001	B, Y1 direction A, Y1 direction	N/A	10/0 10/0
Interim electrical	Per product specification	25 °C, Min. and Max. operating temps.	N/A	
Burn-in	1015	240 hrs. min. @ 125 °C	N/A	10/0
Post burn-In electrical	Per product specification	25 °C, Min. and Max. operating temps.	N/A	10/0
Steady–state life	1005	1,000 hrs min. @ 125 °C	N/A	10/0
Final electrical	Per product specification	25 °C, Min. and Max. operating temps.	10/0	10/0
Wire bond evaluation	2011	C	10/0	10/0
SEM	2018		N/A	4/0

## Chip Element Evaluation for Passive Devices

Subgroup	Class		Test	MIL-STD-883		Quantity (accept number)	Reference Paragraph
	K	H		Method			
1	X	X	Element electrical			100%	C.3.4.1
2	X	X	Visual inspection	2032		100% 22 (0)	C.3.4.2
3	X		Temperature cycling	1010	C	10 (0)	C.3.4.3
	X		Mechanical shock or	2002	B, V1 direction	10 (0)	
	X		Constant acceleration	2001	3,000Gs Y1 direction	10 (0)	
	X		Voltage conditioning or			10 (0)	C.3.4.7
	X		Aging (capacitors)			10 (0)	
	X		Visual inspection	2032		10 (0)	C.3.4.5
4	X	X	Electrical			10 (0)	C.3.4.4
	X	X	Wire bond evaluation	2011		10 (0) wires or 20 (1) wires	C.3.4.3 C.3.4.6

## APPLICATION NOTE

# ESD Compliance Testing and Recommended Protection Circuits for GaAs Devices

## Introduction

Skyworks conducts ESD testing at both the device and system levels. These tests are based on the requirements outlined in:

- ESD Association 2.0 Handbook
  - Human Body Model (HBM)
  - Charged Device Model (CDM)
- IEC 61000-4-2 International Standard: Testing and Measurement Techniques
  - Electrostatic Discharge Immunity Test
- MIL-STD-1686
- MIL-HDBK-263
- Skyworks designed and tested several circuits that provide adequate ESD protection for Skyworks GaAs switches

## Device Level ESD Testing

Device level ESD classification is conducted as part of Skyworks standard qualification process, with the intent to fully characterize a component's electrostatic discharge susceptibility.

The Failure Analysis Laboratory at Skyworks utilizes an Oryx Instrument's Bench Top ESD tester. This instrument allows Human Body Model (HBM) and Machine Model (MM) ESD events to be applied to devices. In addition, Skyworks performs ESD testing to Charged Device Model (CDM). These tests are conducted on the packaged device.

Class	Voltage Range
Class 0	0– ≤ 249 V
Class 1A	250– ≤ 449 V
Class 1B	500– ≤ 999 V
Class 1C	1000– ≤ 1999 V
Class 2	2000– ≤ 3999 V
Class 3A	4000– ≤ 7999 V
Class 3B	> 8000 V

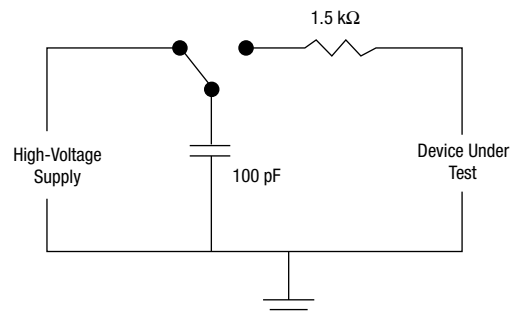
**Table 1. ESD Component Sensitivity Classifications for HBM ESD Testing.**

## Human Body Model (HBM)

This testing model simulates the ESD discharge delivered from the fingertip of an individual to a device. The model uses an RC circuit, such as the one shown in Figure 1, to deliver an exponentially decaying current pulse. Component ESD sensitivity levels for HBM are defined in Table 1.

The testing conducted consists of applying one positive and one negative pulse to the component, allowing a 0.3 second interval between pulses. A set of devices is exposed to these pulses at a given voltage level and pin grounding combinations; the device is tested for full static and dynamic parameters.

A typical test run consists of 20 devices. A set of five (5) devices is exposed to each level in 50 V increments. Most device level testing ranges from 150–500 V.



**Figure 1. HBM Circuit for Delivering a Current Pulse to a Device.**

Charged Device Model (CDM)

This testing model simulates the ESD discharge event that occurs as a charged component discharges to another object at a different electrostatic potential. Component ESD sensitivity levels for CDM are defined in Table 2.

Class	Voltage Range
Class C1	< 125 V
Class C2	125– < 250 V
Class C3	250– < 500 V
Class C4	500– < 1000 V
Class C5	1000– < 1500 V
Class C6	1500– < 2000 V
Class C7	> 2000 V

Table 2. ESD Component Sensitivity Classifications for CDM ESD Testing.

Three samples are submitted to CDM test for each voltage level. The device’s potential is raised by applying a test voltage to the field charge electrode, see Figure 2 (Field Induced CDM Simulator). Five positive and negative discharges are applied to each pin, allowing enough time between discharges for the device to reach the full test voltage. Test voltages applied start at the 100 V level and are increased by 50 V increments. The device passes a voltage level when all three (3) samples stressed at this level pass. The device is tested for full static and dynamic parameters.

A typical test run consists of 20 devices. A set of five (5) devices is exposed to each level in 50 V increments.

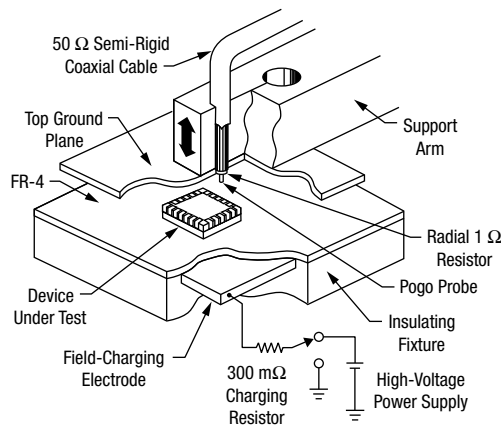


Figure 2. Field Induced CDM Simulator.

System Level ESD Tests

To better understand device performance within an application, Skyworks conducts ESD testing at the system level utilizing the guidelines specified in IEC 61000-4-2. The IEC standard defines typical discharge current waveforms, range of test levels, test equipment, test configuration, and test procedure. System-level testing simulates the device in an application, such as a switch in a cellular handset. Test environment must emulate actual end-use environment.

Test Configuration

The test configuration used at Skyworks (Figure 3) corresponds to that outlined in the IEC Standard for tabletop equipment. The configuration consists of a 6 mm thick, 122 cm x 122 cm square aluminum plate on the laboratory floor. This plate is connected to earth ground. The discharge return cable of the ESD generator is connected to this ground reference plane.

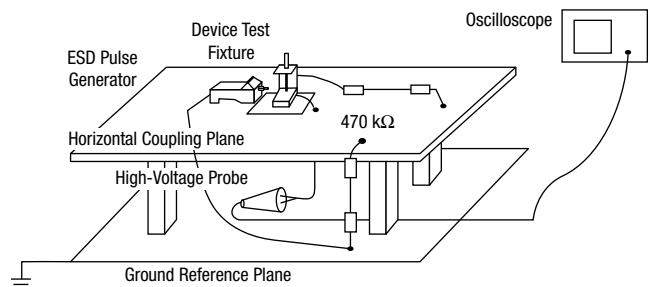


Figure 3. Sketch of the ESD Immunity Test Configuration.

A wooden table 0.8 m high sits on top of the ground reference plate. A horizontal coupling plane of the same dimensions as the ground reference plane is bolted on the wooden table. The device is centrally located on this top surface. The fixture that holds the device is insulated from the horizontal coupling plane by a 0.5 mm thick, 30 cm x 46 cm insulating sheet.

An SMA cable is fed through a hole in the horizontal coupling plane in order to connect to the DUT fixture. This cable is connected to the high-voltage probe that, in turn, connects to the oscilloscope. This allows the voltage at the outputs of the device to be recorded.

ESD Protection Circuit

GaAs devices are used in different system architectures and are applied as power amplifiers, switches, attenuators, detector/couplers, etc. In general, devices that are well embedded within the circuit are better protected, however some applications may require an ESD protection circuit. A possible ESD protection mode utilizes a band pass filter, as shown in Figure 4.

The figure is of a Band Pass Filter (BPF) Protection Circuit for SP4T Switch IC. The BPF shown was mounted in front of an SP4T Switch IC in series.



Skyworks recommends the use of spark gap, band pass filters, and Chebyshev filters as ESD protection circuitry.

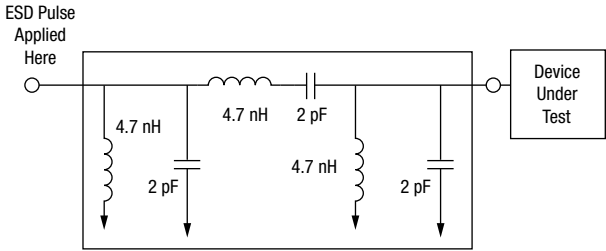
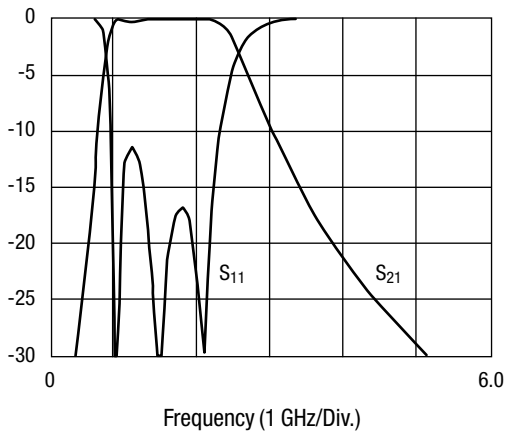


Figure 4. Band Pass Filter—ESD Protection Circuit.



Band Pass Filter Performance

Test Procedure

Skyworks conducts tests on devices mounted on RF test fixture boards to the electrostatic discharge as outlined in the IEC Standard. The fixture is a printed circuit board with SMA connectors to the stripline leading to the device. The device is held in place on the fixture by a spring-loaded plunger (Figure 5).

Considering the recommendation by IEC (International Electrotechnical Commission) and various individual application requirements, both contact and air discharge modes are applied to all system-level tests. The test levels used by Skyworks are outlined in Table 3.

Contact Discharge		Air Discharge	
Level	Test Voltage (kV)	Level	Test Voltage (kV)
1	2	1	2
2	4	2	4
3	6	3	8
4	8	4	16

Table 3. IEC Standard Defined Test Levels for Contact and Air Discharge Modes.

The device is exposed to only one level of ESD energy during the test. The device is RF tested prior to the ESD test, then tested again after the test. The unbiased device is first exposed to ESD air discharge of 16 kV. Upon passing this level of test, a device is biased in a functional state (for example, R<sub>x</sub> mode for a switch) and exposed to incrementally larger contact mode ESD pulses of each polarity.

ESD Protection Circuit Recommendations for Portable, Handheld Devices

Portable electronic devices, like cellular handsets, contain numerous RF and DC components, such as amplifiers, attenuators, switches and filters. Some of them may require ESD protection, some may not. However, to protect even one ESD sensitive chip, like a GaAs switch, it is necessary to consider the whole handset as an ESD-sensitive system, since the ESD pulse can leak into the switch through either one of the RF inputs, outputs, or even through the DC bias paths. Here are points to consider:

- Proper shielding of the whole handset is crucial.
- Bias source should not be located in the poorly shielded section of the board. Bias paths should not be running close to the poorly shielded sections, for example: volume buttons on the side of the case can be a physical opening in the casing of the handset through which the ESD pulse can jump onto the bias path.
- Layout of the circuit board is very important, especially the location of the ESD-sensitive part. There should be no other closely located components that can serve as a path for the ESD pulse into the sensitive part.
- The ESD protective circuit placed in front of the ESD-sensitive part should not significantly degrade the RF performance.

Skyworks has tested several circuits that provide adequate ESD protection with various degrees of shielding. Protection circuits insertion loss varied from 0.06–0.15 dB at 0.88 GHz and from 0.05–0.1 dB at 1.9 GHz, depending on the circuit topology.

Since portable handset designs differ from manufacturer to manufacturer, the ESD protection issue has to be approached on a specific manufacturer’s design basis.

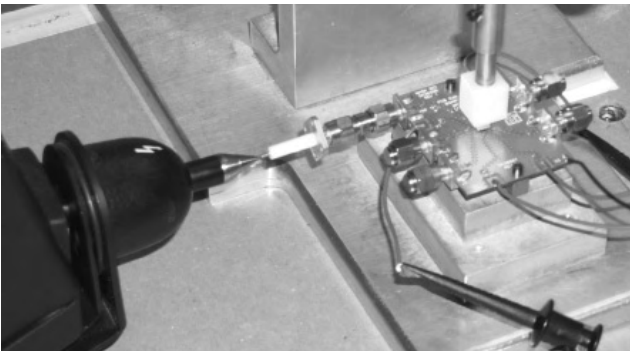


Figure 5. Photograph of the ESD Pulse Application to the Test Fixture.

## APPLICATION NOTE

# Handling Precautions for Schottky Barrier Mixer and Detector Diodes

### Damage by Burnout from Static Electricity

Source of Static Electricity	Precautions
Operator discharging charge on self through diode	Use metal or conductive plastic bench tops and chair seats. Ground operator with strap or use static eliminators, radioactive or ionized air type. Instruct operator in handling precautions.
Use of snow (expanded polystyrene) to hold diodes	Don't use.
Use of plastic bags	Only use dissipative bags or containers. Do not use non-dissipative plastic bags

Cold dry weather (resulting in low humidity) will increase the likelihood of static burnout.

### Damage by Burnout on Test Kits

Source of Transient	Precautions
Bias circuit voltage transient	Have low voltage supply—not high voltage with dropping resistor. Do not use high value capacitance in voltage network. Bring bias voltage to zero before inserting diode.
Bias voltage wrong polarity	Use polarized plugs and supplies.
Transients in power supplies	Use regulated power supply shunting diodes.
Coupled voltage from other circuits	Use shielded leads to diodes. Avoid common wire harness for diode leads and high voltage circuits.
Charge in cables while connecting to circuit	Design checkout procedure and circuits to avoid this.
Ground loops	Have all connecting cables touch outside connections first.
High resistance scale ohmmeter	Maximum open circuit voltage should be 1.5 V. Use appropriate circuit or ohmmeter.

It is extremely important in all diode testing that the test equipment, test jig, and test fixtures be all connected and at the same electrical potential before the diode is inserted.

### Damage by Burnout by Microwave Energy

Source of Microwave Power	Precautions
Pulse energy from same system	Use TR tubes in good condition. Use solid state limiters as well as TR tubes.
Pulse energy from other systems	Use shutter tubes when system not working.
High rectified voltage	Restrict dynamic range of signal or limit load resistor size.

**Damage by Burnout During Electronic Assembly and Test**

Source of Burnout Energy	Precautions
Leakage current from welding equipment and soldering irons	Ground equipment if possible. Test for leakage current and ground loops.
Pulse voltages from controllers and relays on ovens, environmental test equipment, etc.	Put capacitors across relays. Shield equipment. Shield diodes.
Pickup of RF energy from sources such as induction heaters, high power transmitters.	Shield and ground transmitters. Keep diodes in shielded containers. Keep diode and plumbing subassemblies shielded.
Accumulated charge on handling or assembly equipment	Use adequate grounding on all assembly and handlers

**Damage by Mechanical Shock**

Source of Shock	Precautions
Handling	Don't drop diodes or packages on bench or floor. Don't shake in packages.
Insertion in equipment	Diodes should not seat with a jerk or snap. Adjust mechanical tolerances for smooth insertion.
Cutting and forming leads	Support diode during operation. Have cutting and forming tools work smoothly.

**Damage by Excessive Heat**

Source of Heat	Precautions
Soldering	Use heat sink between diode body and point of soldering heat application. Keep exposure to heat at a minimum.

**Detection of Damage**

Test	Precautions
DC reverse test—3 V reverse	Low resistance indicates burnout of some type.
DC forward test	High resistance indicates mechanical or thermal damages.

**General Precautions**

Mark packages containing diodes with cautionary notices.  
(Upon request, Skyworks will supply diode packaging with such notation.)

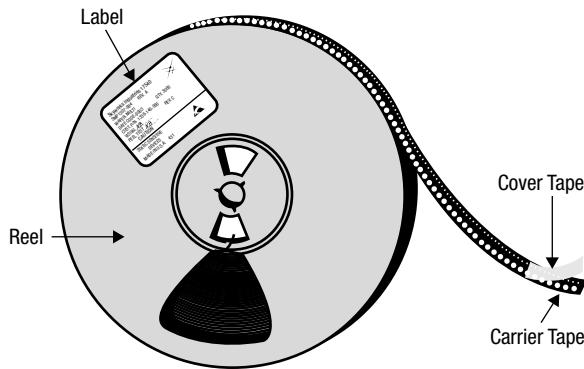
Post instructions at locations where diodes are handled (such as incoming inspection, test stations, etc.).

Instruct inspectors and test operators as to precautions required.

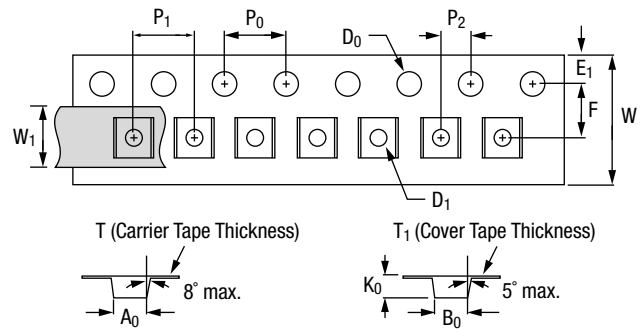
It is extremely important in all microwave diode testing that the test equipment, test fixtures, diode holders, etc., all be connected together and at the same potential before the diode is inserted into the diode holder.

## APPLICATION NOTE

# Discrete Devices and IC Switch/Attenuators Tape and Reel Package Orientation



## Tape Dimensions



Description	Sym.	SC-79	SOD-323	SC-70	SC-88	SOT-23	SOT-143	SOT- 5
<b>Cavity</b>								
Length	A <sub>0</sub>	0.90±0.05	1.45±0.10	2.25±0.10	2.25±0.10	3.15±0.10	3.099±0.10	3.15±0.10
Width	B <sub>0</sub>	1.40±0.05	3.20±0.10	2.70±0.10	2.70±0.10	3.20±0.10	2.692±0.10	3.20±0.10
Depth	K <sub>0</sub>	0.80±0.05	1.35±0.10	0.53±0.05	1.19±0.10	1.40±0.10	1.295±0.10	1.40±0.10
Pitch	P <sub>1</sub>	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10	4.00± 0.10
Bottom hole diameter	D <sub>1</sub>	0.50±0.05	1.00±0.10	0.50±0.05	1.00±0.10	1.00±0.10	1.00±0.10	1.00±0.10
<b>Perforation</b>								
Diameter	D <sub>0</sub>	1.50±0.1	1.50±0.10	1.50±0.10	1.50±0.10	1.55±0.05	1.50±0.10	1.50±0.10
Pitch	P <sub>0</sub>	4.00±0.1	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10
Position	E <sub>1</sub>	1.75±0.1	1.75±0.10	1.75±0.10	1.75±0.10	1.75±0.10	1.75±0.10	1.75±0.10
<b>Carrier Tape</b>								
Width	W	8.00±0.20	8.00±0.20	8.00±0.10	8.00±0.30	8.00±0.30	8.00±0.10	8.00±0.30
Thickness	T	0.229±0.02	0.254±0.013	0.30±0.05	0.254±0.013	0.254±0.013	0.254±0.013	0.20±0.03
<b>Cover Tape</b>								
Width	W <sub>1</sub>	5.40±0.10	5.40±0.10	5.40±0.10	5.40±0.10	5.40±0.10	5.40±0.10	5.40±0.10
Tape thickness	T <sub>1</sub>	0.062±0.01	0.062±0.01	0.062±0.01	0.062±0.01	0.062±0.01	0.062±0.01	0.062±0.01
<b>Distance</b>								
Cavity to perforation (width direction)	F	3.5±0.05	3.50±0.05	3.50±0.05	3.50±0.05	3.50±0.05	3.50±0.05	3.50±0.05
Cavity to perforation (length direction)	P <sub>2</sub>	2.0±0.05	2.00±0.05	2.00±0.05	2.00±0.05	2.00±0.05	2.00±0.05	2.00±0.05

Note: All dimensions are in mm.

Description	Sym.	SOT-6	SOIC-8	MSOP-8	PLCC-28	MCM-20 6 x 6	MCM-24 8 x 7	QFN 2 X 3	QFN 3 x 3	QFN 4 x 4
<b>Cavity</b>										
Length	A <sub>0</sub>	3.15±0.10	6.70±0.10	5.20±0.10	13.0±0.10	6.30±0.10	7.35±0.10	2.20±0.10	3.30±0.10	4.35±0.10
Width	B <sub>0</sub>	3.20±0.10	5.40±0.10	3.30±0.10	13.0±0.10	6.30±0.10	8.35±0.10	3.20±0.10	3.30±0.10	4.35±0.10
Depth	K <sub>0</sub>	1.40±0.10	2.00±0.10	1.60±0.10	4.90±0.10	1.85±0.10	2.00±0.10	1.10±0.10	1.10±0.10	1.10±0.10
Pitch	P <sub>1</sub>	4.00±0.10	8.15±0.02	8.00±0.10	12.0±0.10	8.00±0.10	12.00±0.10	4.00±0.10	8.00±0.10	8.00±0.10
Bottom hole diameter	D <sub>1</sub>	1.00±0.10	1.60±0.02	1.00±0.10	1.60±0.02	1.00±0.10	1.50±0.10	1.50±0.10	1.00±0.10	1.00±0.10
<b>Perforation</b>										
Diameter	D <sub>0</sub>	1.50±0.10	1.60±0.03	1.50±0.10	1.60±0.03	1.50±0.10	1.55±0.10	1.50±0.10	1.50±0.10	1.50±0.10
Pitch	P <sub>0</sub>	4.00±0.10	3.75±0.02	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10
Position	E <sub>1</sub>	1.75±0.10	1.75±0.10	1.75±0.10	1.75±0.10	1.75±0.10	1.75±0.10	1.75±0.10	1.75±0.10	1.75±0.10
<b>Carrier Tape</b>										
Width	W	8.00±0.30	12.00±0.30	12.00±0.30	24.00±0.30	12.00±0.30	16.00±0.30	12.00±0.30	12.00±0.30	12.00±0.30
Thickness	T	0.20±0.03	0.30±0.05	0.30±0.013	0.30±0.005	0.30±0.05	0.30±0.05	0.30±0.05	0.30±0.05	0.30±0.05
<b>Cover Tape</b>										
Width	W <sub>1</sub>	5.40±0.10	9.20±0.10	9.20±0.10	18.50±0.10	9.20±0.10	13.30±0.10	9.20±0.10	9.20±0.10	9.20±0.10
Tape thickness	T <sub>1</sub>	0.062±0.01	0.062±0.01	0.062±0.01	0.062±0.01	0.051±0.01	0.045±0.01	0.051±0.01	0.051±0.01	0.051±0.01
<b>Distance</b>										
Cavity to perforation (width direction)	F	3.50±0.05	3.50±0.05	5.60±0.05	11.50±0.10	5.50±0.10	7.50±0.05	5.50±0.05	5.50±0.10	5.50±0.10
Cavity to perforation (length direction)	P <sub>2</sub>	2.00±0.05	2.00±0.05	4.00±0.05	2.00±0.05	2.00±0.05	2.00±0.05	2.00±0.05	2.00±0.05	2.00±0.05

Note: All dimensions are in mm.

Description	Sym.	QFN 5 x 5	TSSOP-16	SOIC-14	SOIC-16	SSOP-16	SSOP-20	LGA-4	LGA-6	LGA-8	LGA-16
<b>Cavity</b>											
Length	A <sub>0</sub>	5.25±0.10	6.80±0.10	6.50±0.10	6.50±0.10	6.70±0.10	8.20±0.10	1.57±0.10	1.40±0.10	3.25±0.10	8.40±0.10
Width	B <sub>0</sub>	5.25±0.10	5.40±0.10	9.00±0.10	10.30±0.10	5.40±0.10	7.60±0.10	1.38±0.10	1.70±0.10	5.75±0.10	10.70±0.10
Depth	K <sub>0</sub>	1.10±0.10	1.60±0.10	2.10±0.10	2.10±0.10	2.10±0.10	3.00±0.10	1.00±0.10	1.00±0.10	2.70±0.10	2.40±0.10
Pitch	P <sub>1</sub>	8.00±0.10	8.00±0.10	8.00±0.10	8.00±0.10	8.15±0.02	12.00±0.10	4.00±0.10	4.00±0.10	8.00±0.10	16.00±0.10
Bottom hole diameter	D <sub>1</sub>	1.00±0.10	1.60±0.10	1.60±0.10	1.60±0.10	1.60±0.02	1.60±0.10	0.60±0.10	1.00±0.10	1.00±0.10	1.60±0.20
<b>Perforation</b>											
Diameter	D <sub>0</sub>	1.50±0.10	1.50±0.10	1.55±0.10	1.55±0.10	1.60±0.03	1.50±0.10	1.50±0.10	1.50±0.10	1.50±0.10	1.60±0.03
Pitch	P <sub>0</sub>	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10
Position	E <sub>1</sub>	1.75±0.10	1.75±0.10	1.75±0.10	1.75±0.10	1.75±0.10	1.75±0.10	1.75±0.10	1.75±0.10	1.75±0.10	1.75±0.10
<b>Carrier Tape</b>											
Width	W	12.00±0.30	12.0±0.30	16.00±0.30	16.00±0.30	12.0±0.30	16.00±0.30	8.00±0.30	8.00±0.30	12.00±0.30	16.00±0.30
Thickness	T	0.30±0.05	0.30±0.05	0.30±0.05	0.30±0.05	0.30±0.05	0.30±0.05	0.30±0.05	0.30±0.05	0.35±0.05	0.30±0.005
<b>Cover Tape</b>											
Width	W <sub>1</sub>	9.20±0.10	9.20±0.10	13.30±0.10	13.30±0.10	9.20±0.10	13.30±0.10	5.40±0.10	5.40±0.10	9.20±0.10	13.30±0.10
Tape thickness	T <sub>1</sub>	0.051±0.01	0.062±0.01	0.062±0.01	0.062±0.01	0.062±0.01	0.062±0.01	0.062±0.10	0.062±0.10	0.062±0.10	0.062±0.01
<b>Distance</b>											
Cavity to perforation (width direction)	F	5.50±0.10	7.50±0.10	7.50±0.10	7.50±0.05	3.50±0.05	7.50±0.05	3.50±0.05	3.50±0.05	3.50±0.05	7.50±0.10
Cavity to perforation (length direction)	P <sub>2</sub>	2.00±0.05	2.00±0.1	2.00±0.10	2.00±0.10	2.00±0.05	2.00±0.10	2.00±0.10	2.00±0.05	2.00±0.05	2.00±0.10

Note: All dimensions are in mm.

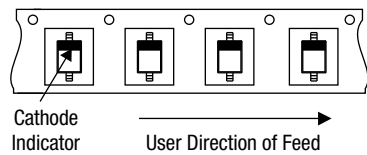
Description	Sym.	SOT-89	SOT-666	3 x 3	2 x 2	1.5 x 1.5	MSOP-10	Micro-X	4 x 4	LQFP-32	LTCC (-108, 109)
<b>Cavity</b>											
Length	A <sub>0</sub>	4.60±0.10	1.78±0.05	3.30±0.10	2.40±0.10	1.78±0.05	5.20±0.10	2.198±0.10	4.35±0.10	9.6±0.10	1.55±0.10
Width	B <sub>0</sub>	4.90±0.10	1.78±0.05	3.30±0.10	2.40±0.10	1.78±0.05	3.30±0.10	5.769±0.10	4.35±0.10	9.6±0.10	1.96±0.10
Depth	K <sub>0</sub>	1.96±0.10	0.69±0.05	1.10±0.10	1.20±0.10	0.69±0.05	1.60±0.10	1.648±0.10	1.10±0.20	2.2±0.10	1.13±1.10
Pitch	P <sub>1</sub>	4.00±0.20	4.00±0.10	8.00±0.10	4.00±0.10	4.00±0.10	8.00±0.10	8.00±0.10	8.00±0.10	12.0±0.10	4.00±0.10
Bottom hole diameter	D <sub>1</sub>	1.50±0.10	0.50±0.05	1.00±0.10	1.00±0.10	0.50±0.05	1.00±0.10	1.50±0.25	1.00±0.10	1.50±0.10	0.80±0.05
<b>Perforation</b>											
Diameter	D <sub>0</sub>	1.50±0.10	1.50±0.10	1.50±0.10	1.50±0.10	1.50±0.10	1.50±0.10	1.50±0.10	1.5±0.10	1.50±0.10	1.50±0.10
Pitch	P <sub>0</sub>	4.00±0.20	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10
Position	E <sub>1</sub>	1.75±0.10	1.75±0.10	1.75±0.10	1.75±0.10	1.75±0.10	1.75±0.10	1.75±0.10	1.75±0.10	1.75±0.10	1.75±0.10
<b>Carrier Tape</b>											
Width	W	12.0±0.30	8 mm	12.0±0.30	8.0+ .3, -0.10	8.0+ .3, -0.10	12.00±0.30	12 mm	12.0±0.30	16.0±0.30	8.00 +0.30/-0.10
Thickness	T	0.30±0.05	0.20±0.02	0.30±0.05	0.30±0.05	0.30±0.05	0.30±0.013	0.293±0.13	0.30±0.05	0.30±0.05	0.254±0.02
<b>Cover Tape</b>											
Width	W <sub>1</sub>	9.2±0.10	5.40±0.10	9.20±0.10	5.40±0.10	5.40±0.10	9.2±0.10	9.3±0.10	9.2±0.10	13.3±0.10	5.40±0.10
Tape thickness	T <sub>1</sub>	0.062±0.01	0.61	0.062±0.01	0.062±0.01	0.062±0.01	0.062±0.01	0.61	0.062±0.01	0.062±0.01	0.062±0.01
<b>Distance</b>											
Cavity to perforation (width direction)	F	5.5±0.05	3.50±0.05	5.50±0.05	3.50±0.05	3.50±0.05	5.6±0.05	5.5±0.05	5.50±0.05	7.50±0.10	3.50±0.05
Cavity to perforation (length direction)	P <sub>2</sub>	2.0±0.05	2.00±0.025	2.00±0.05	2.00±0.05	2.00±0.05	4.00±0.05	2.0±0.05	2.00±0.05	2.00±0.10	2.00±0.05

Note: All dimensions are in mm.

Description	Sym.	LTCC (-116, -117)	Flip Chip 540-011	Flip Chip 540-025	0201 (-093)	0201 (-096)
<b>Cavity</b>						
Length	A <sub>0</sub>	1.93±0.10	0.45±0.05	0.45±0.05	0.32±0.05	0.32±0.05
Width	B <sub>0</sub>	2.24±1.10	0.78±0.05	0.78±0.05	0.57±0.05	0.57±0.05
Depth	K <sub>0</sub>	1.13±0.10	0.25±0.05	0.25±0.05	0.32 ± 0.05	0.32 ± 0.05
Pitch	P <sub>1</sub>	4.00±0.10	2.00±0.05	2.00±0.05	2.00±0.05	2.00±0.05
Bottom hole diameter	D <sub>1</sub>	1.00±0.25	0.15±0.05	0.15±0.05	0.20±0.05	0.20±0.05
<b>Perforation</b>						
Diameter	D <sub>0</sub>	1.50±0.10	1.50±0.10	1.50±0.10	1.50±0.10	1.50±0.10
Pitch	P <sub>0</sub>	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10
Position	E <sub>1</sub>	1.75±0.10	1.75±0.10	1.75±0.10	1.75±0.10	1.75±0.10
<b>Carrier Tape</b>						
Width	W	8.00	8.00±0.10	8.00±0.10	8.00±0.10	8.00±0.10
Thickness	T	0.254±0.02	0.25±0.05	0.25±0.05	0.25±0.05	0.25±0.05
<b>Cover Tape</b>						
Width	W <sub>1</sub>	5.40±0.10	0.495±0.05	0.495±0.05	0.495±0.05	0.495±0.05
Tape thickness	T <sub>1</sub>	0.062±0.01	0.045±0.01	0.045±0.01	0.045±0.01	0.045±0.01
<b>Distance</b>						
Cavity to perforation (width direction)	F	3.50±0.05	3.50±0.05	3.50±0.05	3.50±0.05	3.50±0.05
Cavity to perforation (length direction)	P <sub>2</sub>	2.00±0.05	2.00±0.05	2.00±0.05	2.00±0.05	2.00±0.05

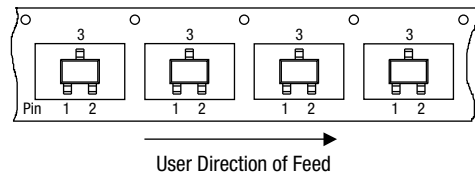
Note: All dimensions are in mm.

SOD-323



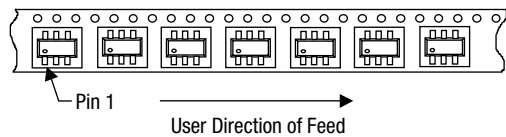
Standard Reel Size	7"	13"
Standard Reel Quantity	3,000	12,000

SC-70



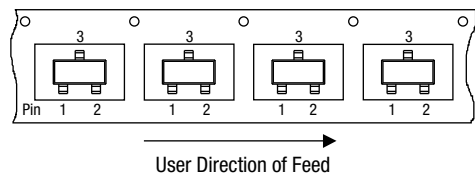
Standard Reel Size	7"	13"
Standard Reel Quantity	3,000	12,000

SOT-6 and SC-88



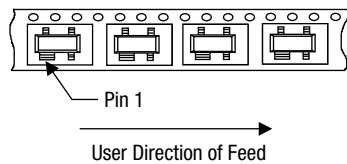
Standard Reel Size	7"	13"
Standard Reel Quantity	3,000	12,000

SOT-23



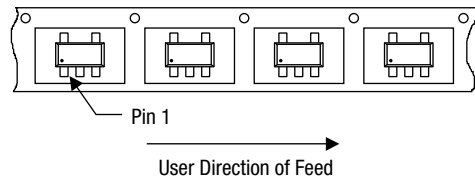
Standard Reel Size	7"	13"
Standard Reel Quantity	3,000	12,000

SOT-143



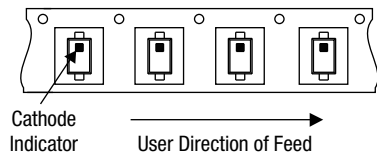
Standard Reel Size	7"	13"
Standard Reel Quantity	3,000	12,000

SOT-5



Standard Reel Size	7"	13"
Standard Reel Quantity	3,000	12,000

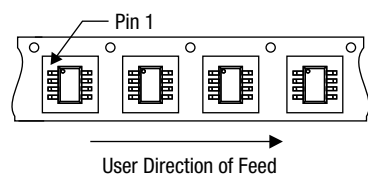
SC-79



Standard Reel Size	7"	13"
Standard Reel Quantity*	3,000	12,000

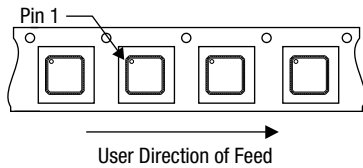
\*Available through distribution.

MSOP-8, MSOP-10 and SOIC-8

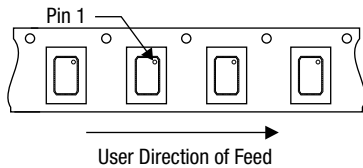


Standard Reel Size	7"	13"
Standard Reel Quantity	1,000	3,000

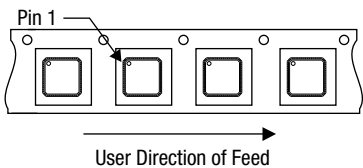


**MCM-20 (6 x 6)**

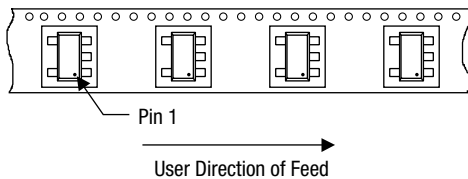
Standard Reel Size	7"	13"
Standard Reel Quantity	1,000	3,000

**MCM-24 (8 x 7)**

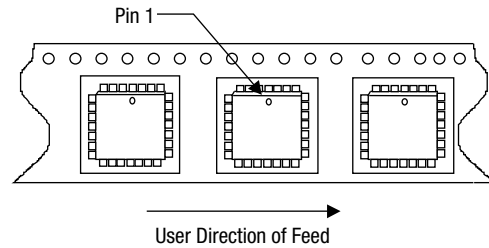
Standard Reel Size	7"	13"
Standard Reel Quantity	N/A	2,000

**QFN (3 x 3), (4 x 4), (5 x 5)**

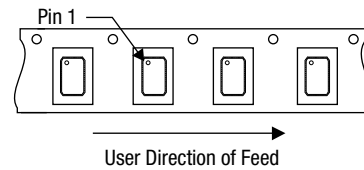
Standard Reel Size	7"	13"
Standard Reel Quantity	1,000	3,000

**SOT-89**

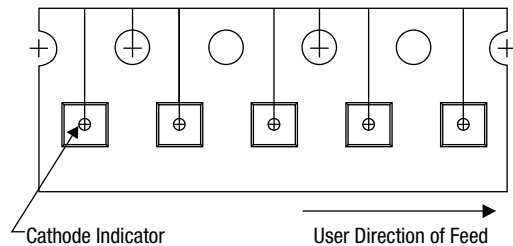
Standard Reel Size	7"	13"
Standard Reel Quantity	N/A	2,500

**28-Lead PLCC**

Standard Reel Size	7"	13"
Standard Reel Quantity	N/A	1,500

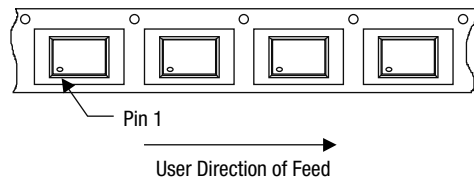
**QFN (2 x 3)**

Standard Reel Size	7"	13"
Standard Reel Quantity	1,000	3,000

**QFN (1.5 x 1.5), (2 x 2)**

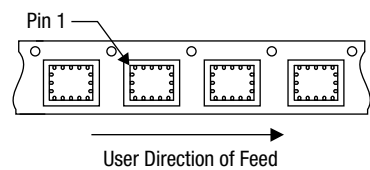
Standard Reel Size	7"	13"
Standard Reel Quantity	1,000	3,000

LGA-4, LGA-6 and SOT-666



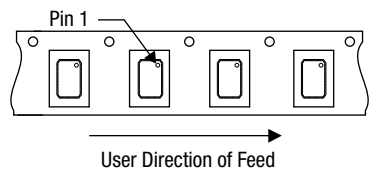
Standard Reel Size	7"	13"
Standard Reel Quantity	3,000	12,000

LGA-16 (-501)



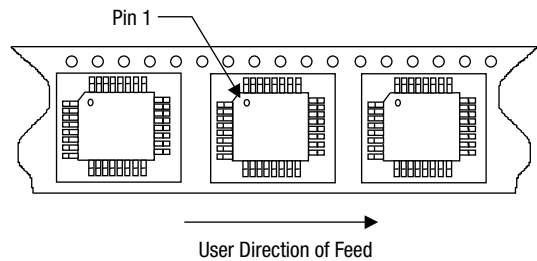
Standard Reel Size	7"	13"
Standard Reel Quantity	1,000	3,000

LGA-8 (-315)



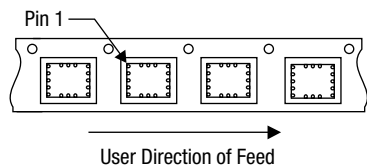
Standard Reel Size	7"	13"
Standard Reel Quantity	1,000	3,000

32-Lead TQFP and LQFP



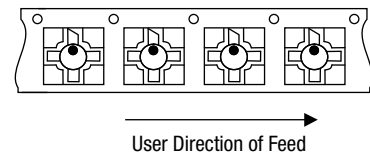
Standard Reel Size	7"	13"
Standard Reel Quantity	N/A	2,000

LGA-16 (-500)



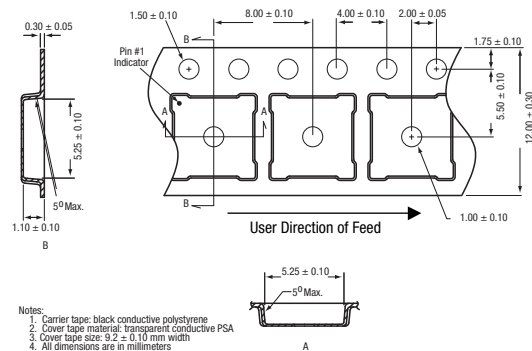
Standard Reel Size	7"	13"
Standard Reel Quantity	1,000	3,000

Micro X



Standard Reel Size	7"	13"
Standard Reel Quantity	1,000	3,000

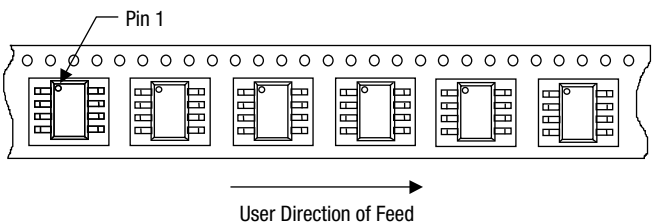
QFN 32L 5 x 5 x 0.9 mm (-364)



Standard Reel Size	7"	13"
Standard Reel Quantity	500	3,000

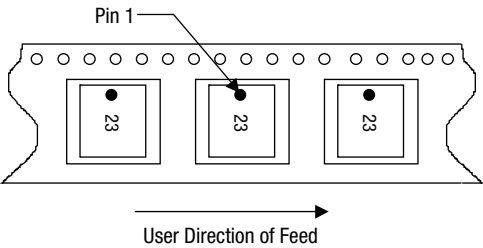
SOIC, MSOP, QSOP, SSOP and TSSOP Devices

8, 10, 14, 16, 20, 28 Leads



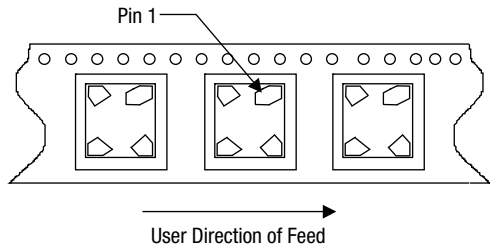
Standard Reel Size	7"	13"
Standard Reel Quantity	1,000	3,000

**Ceramic LTCC (-108, -109)**



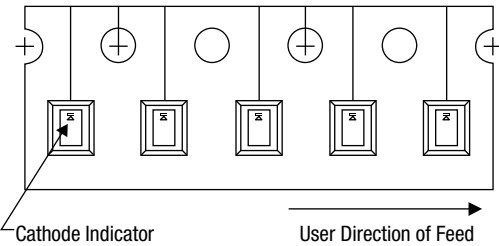
Standard Reel Size	7"	13"
Standard Reel Quantity	3,000	12,000

**Ceramic LTCC (-116, -117)**

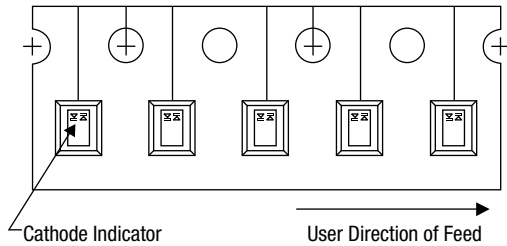


Standard Reel Size	7"	13"
Standard Reel Quantity	3,000	12,000

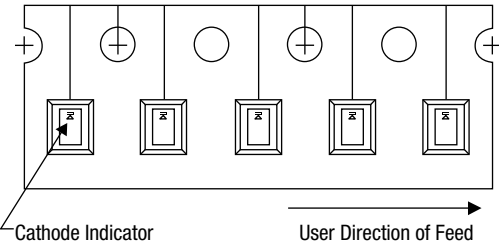
**Flip Chip 540-011**



**Flip Chip 540-025**



**0201 (-093, -096)**



## APPLICATION NOTE

# Diode Chips, Beam-Lead Diodes, Capacitors: Bonding Methods and Packaging

## Diode Chips

### Handling

Skyworks chips are shipped in plastic chip trays containing up to 400 individual devices. The chips may be removed from the tray and positioned for inspection or bonding using tweezers or a vacuum pickup. Particular care must be exercised to avoid any mechanical damage to the active junction area when handling chips. In addition, if tweezers are used, care must be taken to avoid excessive force which might result in nicks or cracks.

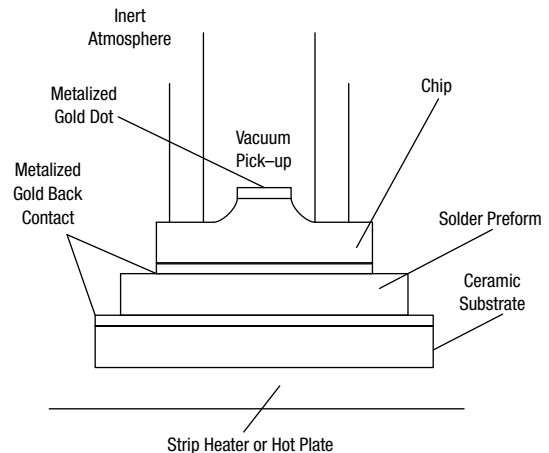
Special handling precautions are also required to avoid electrical damage by static discharge. For package opening instructions see Figure 4.

### Die Attach

The recommended method for attaching Skyworks semiconductor chips to substrates is by means of a solder preform or silver epoxy. Basically this method involves the use of the preform or epoxy to form a joint between the gold metalized base of the chip and the metalized area of the substrate. Recommended preform materials are: Gold (80%)—Tin (20%); Gold (89.5%)—Gallium (0.5%)—Germanium (10%); or Gold (90%)—Germanium (10%). These are available from Alpha Metals, Jersey City, New Jersey. Recommended silver epoxy is Epo-Tek H31D Single Component from Epoxy Technology, Inc.

### Procedure

The substrate may be heated directly by placement on a heater strip or hot plate. Resistance heating may also be used, in which case the localized heat is supplied by passing current through the appropriate metalized portion of the substrate by use of two contact electrodes. Hot gas heating may also be used, in which case the localized heat is supplied by a jet flow of heated forming gas or nitrogen.



**Figure 1. Die Attach Procedure**

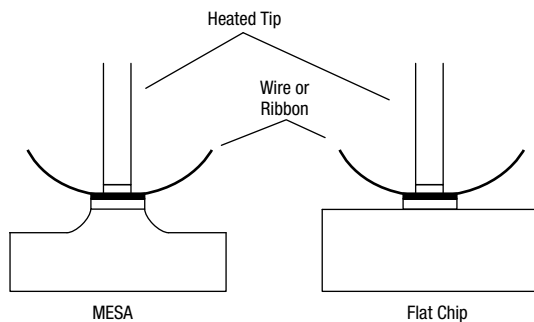
Temperatures of approximately 280 °C for gold-tin, 350 °C for gold-gallium-germanium and 380 °C for gold-germanium are recommended. A 100 °C bake for 1 hour is recommended for silver epoxy. Exact temperatures should be determined empirically for the particular conditions at hand. The bonding should be done in an atmosphere of nitrogen or forming gas. Both solder preform and chip may best be handled by means of a vacuum pickup. A preform is placed on the desired location of the substrate followed by the chip. Appropriate force is maintained between substrate and chip while the preform melts and wets both substrate metallization and chip. The force, approximately 50 grams, is maintained until the preform solidifies. Cooling may be accelerated through use of a blast of inert gas.

### Lead Bonding

Wire or ribbon leads should be attached to the chip and the substrate by use of thermocompression bonding. As with the beam-lead devices, this method involves pressing the gold lead against the gold metalized area on the chip or substrate under proper conditions of heat pressure and scrub to effect a bond.

**Procedure (See Figure 2)**

Gold should be used for the lead wire or ribbon. Though either ball bonding or wedge bonding may be used, the latter is generally preferred since smaller bond areas are possible with consequent less parasitic capacitance. The bonding tool is tungsten carbide, and the detail tip design is dependent upon the dimensions of the lead material to be bonded. A tip temperature of 350 °C to 400 °C with approximately 50 grams pressure is recommended. This temperature may be reduced by heating the substrate to 325 °C or using ultrasonics for a scrub. Generally, a satisfactory bond is attained with a bonding time of 2–3 seconds. Optimum conditions should be determined by trial and error to adjust for differences in chip configurations, substrate condition and other variables.



**Figure 2. Lead Bonding Procedure**

**Equipment**

Equipment for die attachment and lead bonding is commercially available from several manufacturers and varies in sophistication from laboratory setups to automated machines.

**Beam-Lead Diodes and Capacitors**

Due to their small size, beam-lead devices are fragile and should be handled with extreme care. The individual plastic packages should be handled and opened carefully, so that no undue mechanical strain is applied to the packaged device. It is recommended that the beam-lead devices be handled through use of a vacuum pencil using an appropriate size vacuum needle or a pointed wooden stick such as a sharpened Q-tip or match stick. The device will adhere to the point and can easily be removed from the container and positioned accurately for bonding without damage. Such handling should be done under a binocular microscope with magnification in the range of 20X to 30X.

Special handling precautions are also required to avoid electrical damage, such as static discharge. For waffle pack package opening instructions see Figure 4.

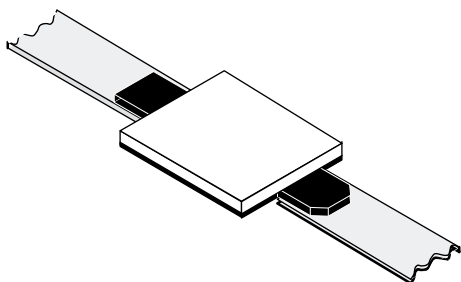
**Bonding**

Skyworks beam-lead devices can best be bonded to substrates by means of thermocompression bonding. Essentially this type of bonding involves pressing the gold beam of the device against the gold plated metalized substrate under proper conditions of heat and pressure so that a metallurgical bond joint between the two occurs.

**Procedure**

The beam-lead devices to be bonded should be placed on a clean, hard surface such as a microscope slide. It is recommended that the beam side of the device be down so that this side will be toward the substrate when bonded. The device can be picked up by pressing lightly against one beam with the heated tip. The substrate can then be appropriately positioned under the tip and the device brought down against the substrate, with proper pressure applied by means of the weld head.

A bonding tip temperature in the 350 °C to 450 °C range is recommended along with a bonding force of 50 to 70 grams. The bonding time is in the range of 2–3 seconds. Optimum bonding conditions should be determined by trial and error to compensate for slight variations in the condition of the substrate, bonding tip, and the type of device being bonded.



**Figure 3. Beam-Lead Cap Mounted**

### Equipment

The heat and pressure are obtained through use of a silicon carbide bonding tip with a radius of two to three mils. Such an item is available from several commercial sources. In order to supply the required tip-travel and apply proper pressure, a standard miniature weld head can be used. Also available is a heated wedge shank which is held by the weld head and in turn holds the tip and supplies heat to it. The wedge shank is heated by means of a simple AC power supply or a pulse-type heated tool.

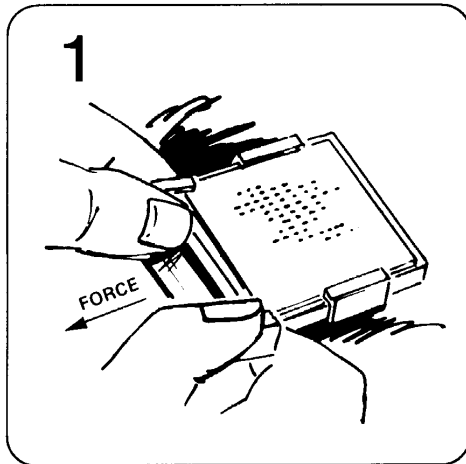
### Substrate

For optimum bonding, a gold-plated surface at least 100 micro-inches thick is necessary. Although it is possible to bond to relatively soft metalized substrate material such as epoxy-fiberglass, etc., optimum bonding occurs when a hard material such as ceramic can be used.

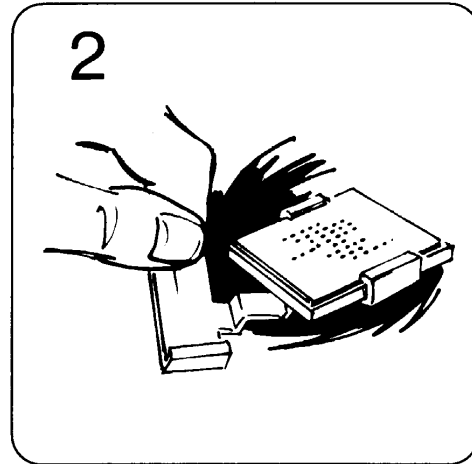
### Quality

If a good bond has been obtained, it is impossible to separate the beam-lead device from the metalized substrate without damage. If the device is destructively removed, the beam will tear away, leaving the bonded portion attached to the substrate. In bonding the high value capacitors, it is important that the bond be made at the ends of the beams.

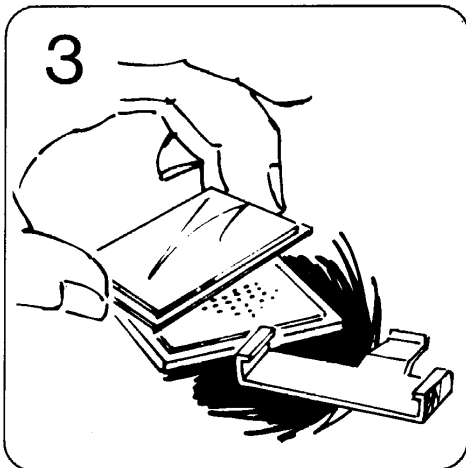
## Chip Packaging



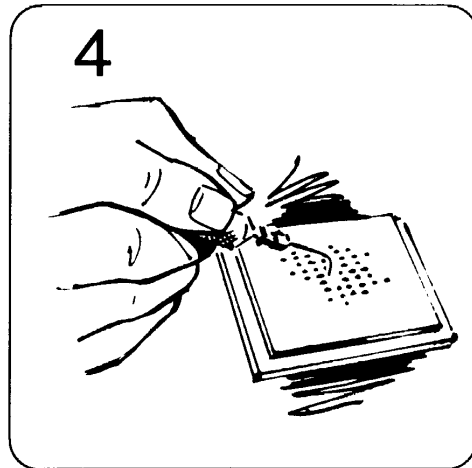
1. Place package on table top. There are two interlocking fasteners. Turn package so that interlocking side is facing down.
2. Grip one section of the plastic fasteners with thumbs; hold package when applying force.
3. Pull one plastic fastener from package.



Remove both plastic fasteners.



Remove lid from waffle.



Remove chip from waffle at work station with vacuum pickup.

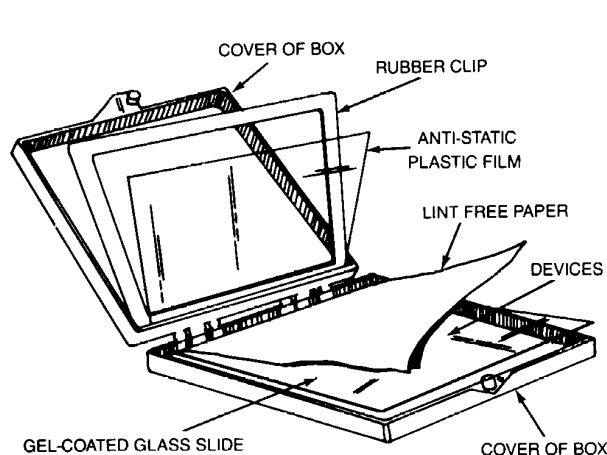
**Figure 4. Diode Chip Waffle Package Opening Instructions**

## Beam-Lead Packaging

Skyworks beam-lead diodes and capacitors are shipped in various package styles depending upon the customer's preference. See Beam-Lead Diodes and Capacitors Bonding Procedure for proper device handling.

### Type 1 (Gel Pak)

This is a 2" x 2" black plastic conductive box. The beam-leads are mounted on a gel-coated glass slide. The devices are covered with a piece of lint-free release paper, on top of which is placed a piece of anti-static plastic film. The glass slide and paper are held down by a rubber clip which runs along the perimeter of the box. The cover of the box is snapped shut and taped to prevent opening during shipment.



**Drawing #1**

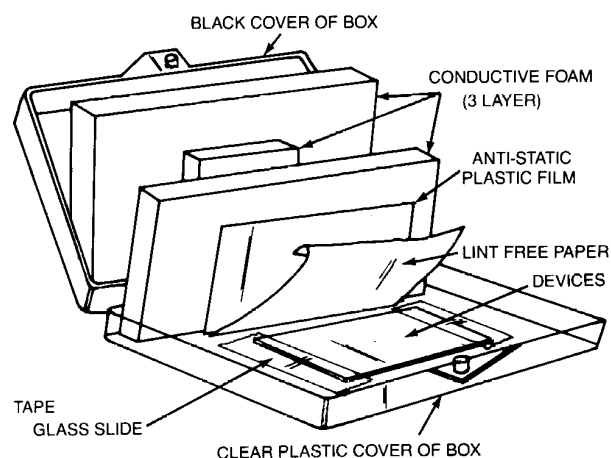
**Caution:** Care must be taken in removing foam, film, and lint-free release paper, because if units fall off the glass slide, they may get stuck to tape. One advantage of this packaging is that the devices can be transferred directly from the glass slide to the circuit.

### Type 2 (Gel Pak)

For larger beam-leads, a piece of foam is substituted for the rubber clips to ensure that devices will not be released from the gel during shipment.

### Type 3

Some customers prefer shipment of beam-leads on glass slides without gel. In this case, a glass slide is taped to the bottom of a 2" x 3" plastic box, and the units are placed on the glass slide. Pieces of lint-free release paper and antistatic plastic film are placed on top of the glass slides. Three pieces of antistatic foam are placed within the box as a filler to prevent the devices from moving. The box is snapped shut and taped to prevent movement during shipment. The lower part of the box is clear to allow the incoming inspection groups to count the units without opening the box. The upper part of the box is black conductive plastic material.



**Drawing #2**

The sequence is as follows:

1. Open the box.
2. Carefully remove the foam, plastic and release paper.
3. Use an X-acto knife to cut the tape holding the glass slide and beam-lead devices.
4. A hot bonding tool may then be used to pick up the beam-lead from the glass slide and place it directly across the gap in the circuit.



## WARRANTY/ORDER INFORMATION

### How to Order

To order products from this brochure or for additional information, please contact your local representative, distributor, or contact us directly.

A worldwide list of Sales Offices/Representatives and Distributors appears at the back of this brochure. Please provide part numbers, quantities, and any additional information that will help us expedite your order.

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### Notice

The information contained in this brochure is subject to change without notice. Skyworks reserves the right to change specifications, designs, and any other information in this brochure at any time, without notice, and assumes no responsibility for errors and/or omissions.

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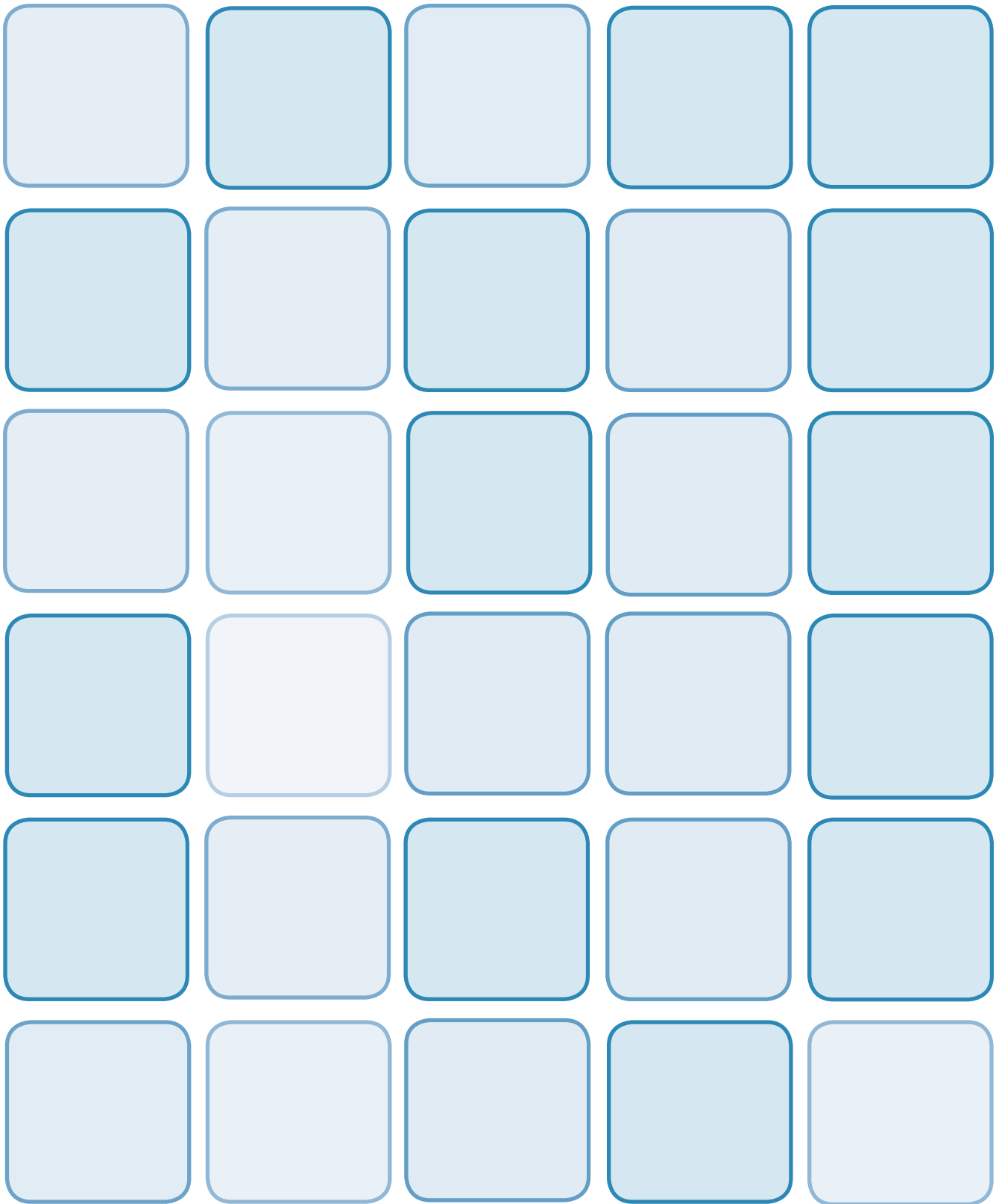
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CAT501-09A 1/09

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