COGNITIVE SYSTEMS RESEARCH PROGRAM

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REPORT NO. 5

SYSTEM AND CIRCUIT DESIGNS FOR THE TOBERMORY PERCEPTRON

(Preliminary Report on Phase I)

By

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SUMMARY

Dwg. No. 1.2 Detailed System Design*
Dwg. No. 1.1 Tobermory Floor Plan

Tobermory, named after Saki's eavesdropping talking cat, is a general purpose pattern recognition machine roughly modelled on biological prototypes.† Phase I, described in this report, consists of a four-layer audio-perceptron organized as shown in figure 0.0.1.

The sensory analyzer breaks up the signal into a 1600 bit time-frequency-amplitude pattern. The outputs of the sensory units are connected in many-to-many fashion to 1000 association units, which, in turn, are linked by 12,000 variable weights to 12 decision elements (response units). A given signal may thus be represented by one of 2^{12} code words. This scheme is implemented as follows.

A microphone and a tapehead serve as alternative inputs to 45 resonant band pass filters. The bandwidth of the filters is manually variable in five steps, corresponding to Q's in the range of one to twelve, while the center frequencies may be changed in a two to one range. The center frequencies are distributed uniformly on a pitch (mel) scale. The logarithms of the outputs of the filters are pairwise compared in variable-threshold difference amplifiers. This operation serves to localize peaks, valleys, and sharp transitions in the instantaneous frequency profile. Provision is also made to monitor the overall amplitude level.

The outputs of the difference amplifiers constitute the input to eighty delay lines consisting of twenty monostable multivibrators each. The time delay associated with each multivibrator may be set independently in the range of 10 to 100 milliseconds, yielding asynchronous sampling of words up to two seconds long. The 1600 bit pattern represented by the multivibrators is

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* Drawings listed after section headings refer to CSRP file numbers.

† References are listed at the end of the report.

available on a plugboard, which permits selection of arbitrary subsets as 'receptive fields' for each A-unit.

The A-units are simply difference amplifiers with a threshold setting. When the threshold is exceeded, a carrier signal is gated to each of the twelve analog memory elements associated with an A-unit, and a signal proportional to the setting of the tapewound cores is contributed to the appropriate R-unit, where all such signals are summed. The R-units are also threshold elements, with built-in hysteresis to increase stability.

In automatic operation, digital signals from one channel of the tape (representing the desired output) regulate reinforcement (incrementing or decrementing the flux levels in the cores). During training, the reinforcement history of each R-unit is printed out on an electric typewriter, which also serves to code the training tapes. A number of other convenient features facilitate experimentation on word and music recognition, continuous speech processing, language, regional accent, and individual speaker identification, phoneme structure analysis, and related problems.

Figure 0.0.2 depicts the physical location of the various units described above, while figure 0.0.3 is an isometric sketch of the structure. Following presentation, the introductory sections cover the material in each chapter in block diagram form. The remaining sections contain detailed descriptions of the mode of operation and calibration of the circuits necessary to implement the block diagrams. The author hopes to relieve the repetitious, pedestrian style of these descriptions by the use of numerous apposite illustrations.

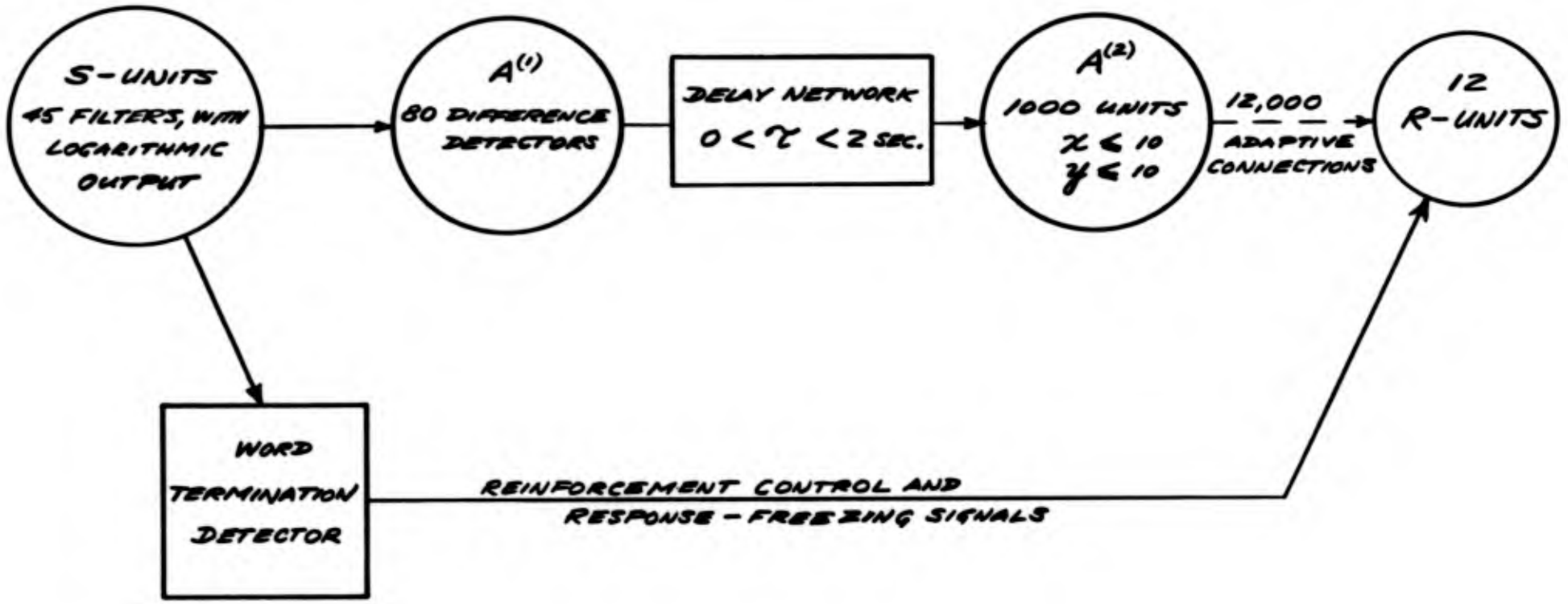


FIG. 0.0.1: TOBERMORY, PHASE I (FOUR-LAYER PERCEPTRON)

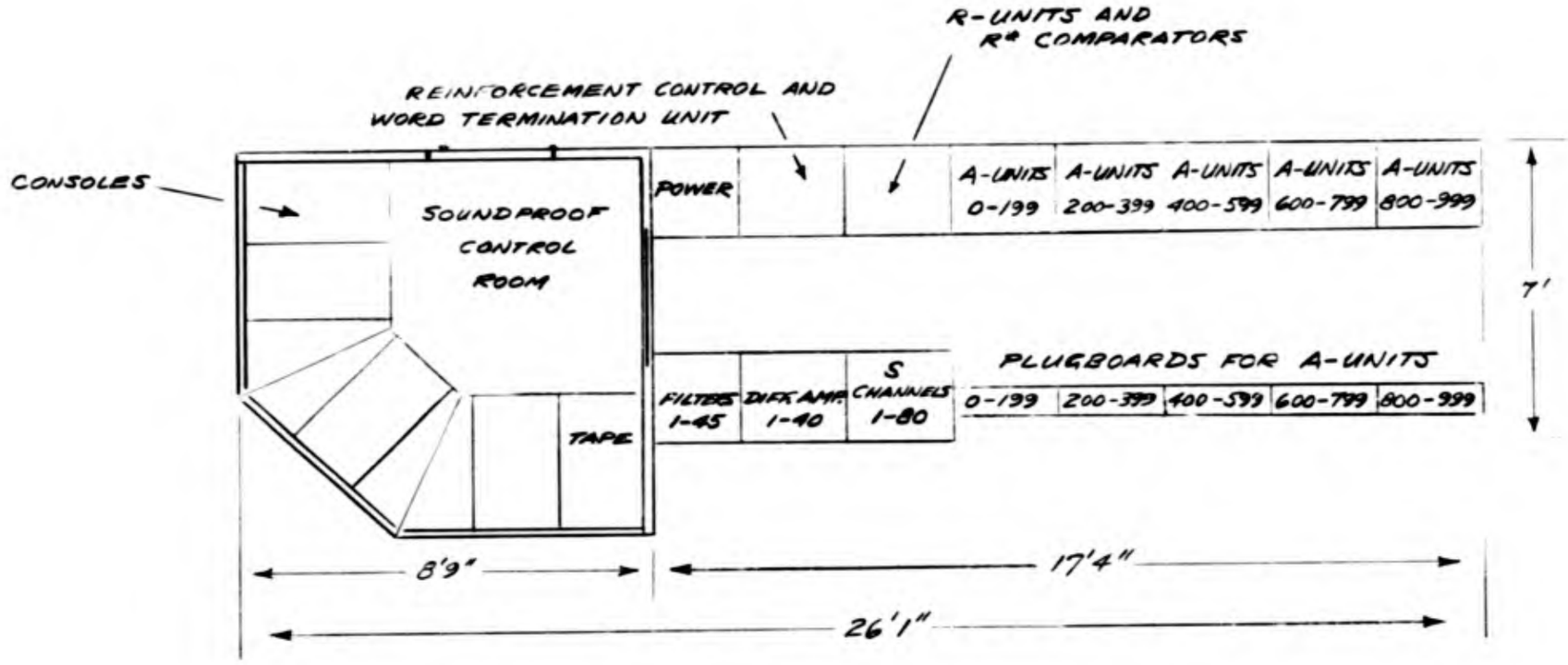


FIG. 0.0.2 : TOBERMORY PHASE I FLOOR PLAN (SCALE 1:48)

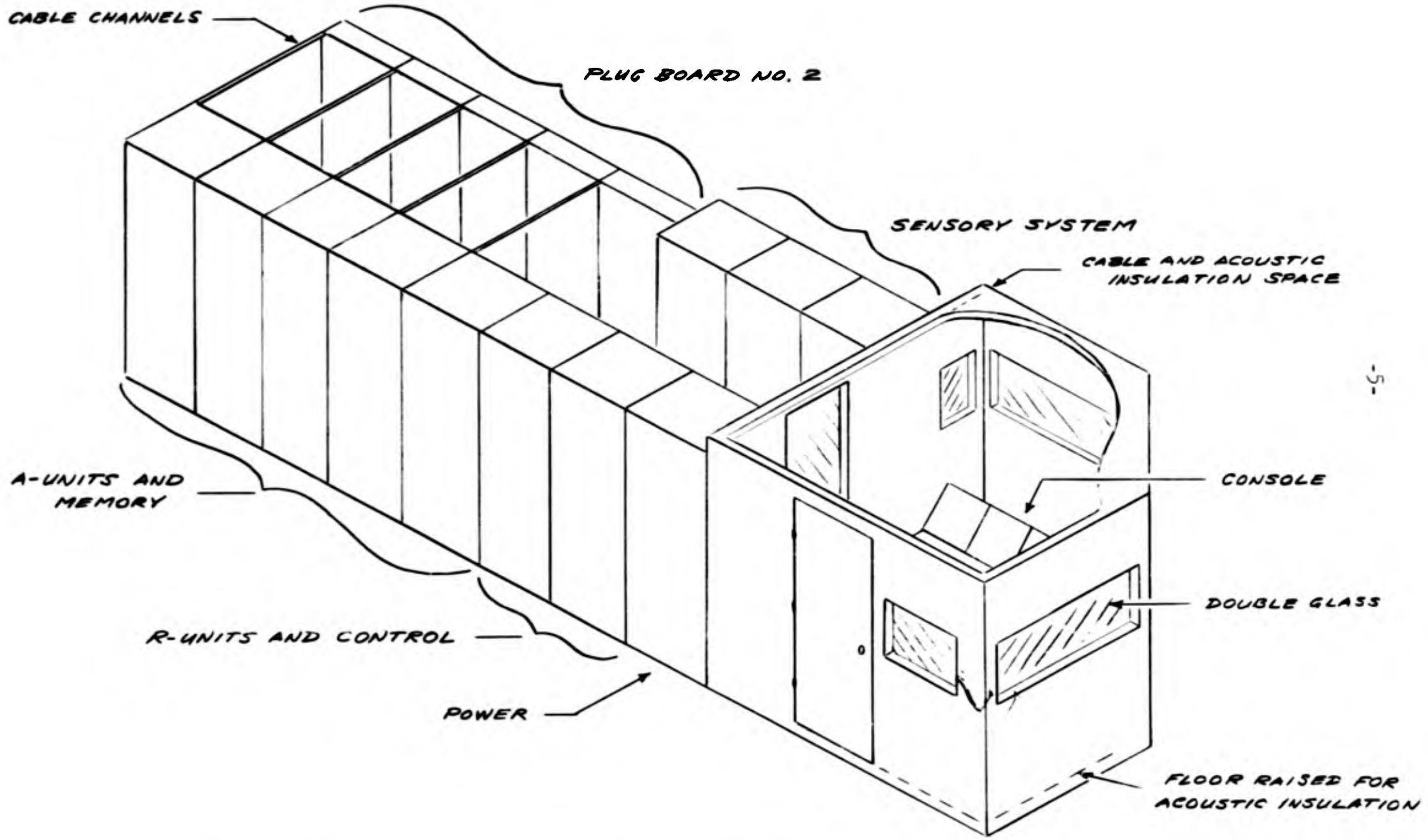


FIG. 0.0.3 : ISOMETRIC VIEW OF TOBERMORY, PHASE I

CHAPTER I - THE SENSORY ANALYZER

1.0 - Introduction

A detailed block diagram of the sensory analyzer, consisting of the audio input system, the $A^{(1)}$ units, and the delay connections to the $A^{(2)}$ units, is shown in figure 1.0.1.

The sensory input, dialed on the input selector in the control booth, can be any mixture of signals from a tape recorder, a microphone, a pair of audio oscillators, and a noise generator. An AGC amplifier with 25db. compression can be switched into the system at the operator's discretion. From here the signals are amplified for input to the filter network. The signal coming from the main amplifier is available for display on an oscilloscope in the control room, as are the outputs of the filters. The audio signal also goes to the monitoring speakers, a volume meter, and an amplitude measurement circuit which emits a voltage proportional to the average amplitude of the signal. This measurement is used to trigger the word termination (or pause) detector which is activitated by a period of silence following an audio input signal. It is also averaged over a longer time period, to provide information to the perceptron on the amplitude profile of the input pattern, which would otherwise be lost in the frequency analyzing network. Both the "momentary amplitude" and the "average amplitude" are available, along with the logarithms of the 45 filter outputs, at Plug Board no. 1.

The 45 audio filters can be set to cover one of three ranges: 30 to 4700 cps, 47 to 7000 cps, or 60 to 9400 cps. The bandwidths are variable from 8.4% to 100% of the center frequencies.

Each of the 40 differential amplifiers (representing the $A^{(1)}$ units of figure 0.0.1) can be connected to any pair of signals from filters or amplitude measuring devices by means of plug board no. 1. Since all of these signals are represented in logarithmic form, the signal from the differential amplifier represents the ratio of two amplitudes, rather than the absolute difference. This eliminates the need for a very high compression AGC amplifier, and

effectively normalizes the speech input for variability due to changes in volume, distance from the microphone, etc. Each differential amplifier has two output channels, one of which carries a signal if the difference is positive, and the other, if the difference is negative. Each difference signal is fed to a threshold gate with adjustable threshold. This system, then, extracts from the profile of the instantaneous frequency spectrum the ratios of the amplitudes at selected pairs of points throughout the spectrum. It is this set of ratios, now represented in digital form by the outputs of the 80 threshold gates, which characterizes the audio pattern for the subsequent parts of the system.

In order to represent the time dimension of the input pattern, the sets of eighty signals representing the momentary frequency spectrum are fed into eighty channels of twenty delay multivibrators each. Whenever a threshold gate is activated (indicating that some ratio of frequency amplitudes has exceeded its threshold) it permits a pulse from a trigger generator to touch off the first delay unit in the corresponding chain. This signal travels down the delay chain; the state of each multivibrator represents the output of the threshold gate at some previous instant of time. The 1600 individual multivibrator outputs are available at plugboard number 2, so that they may be connected to any combination of the 1000 $A^{(2)}$ units.

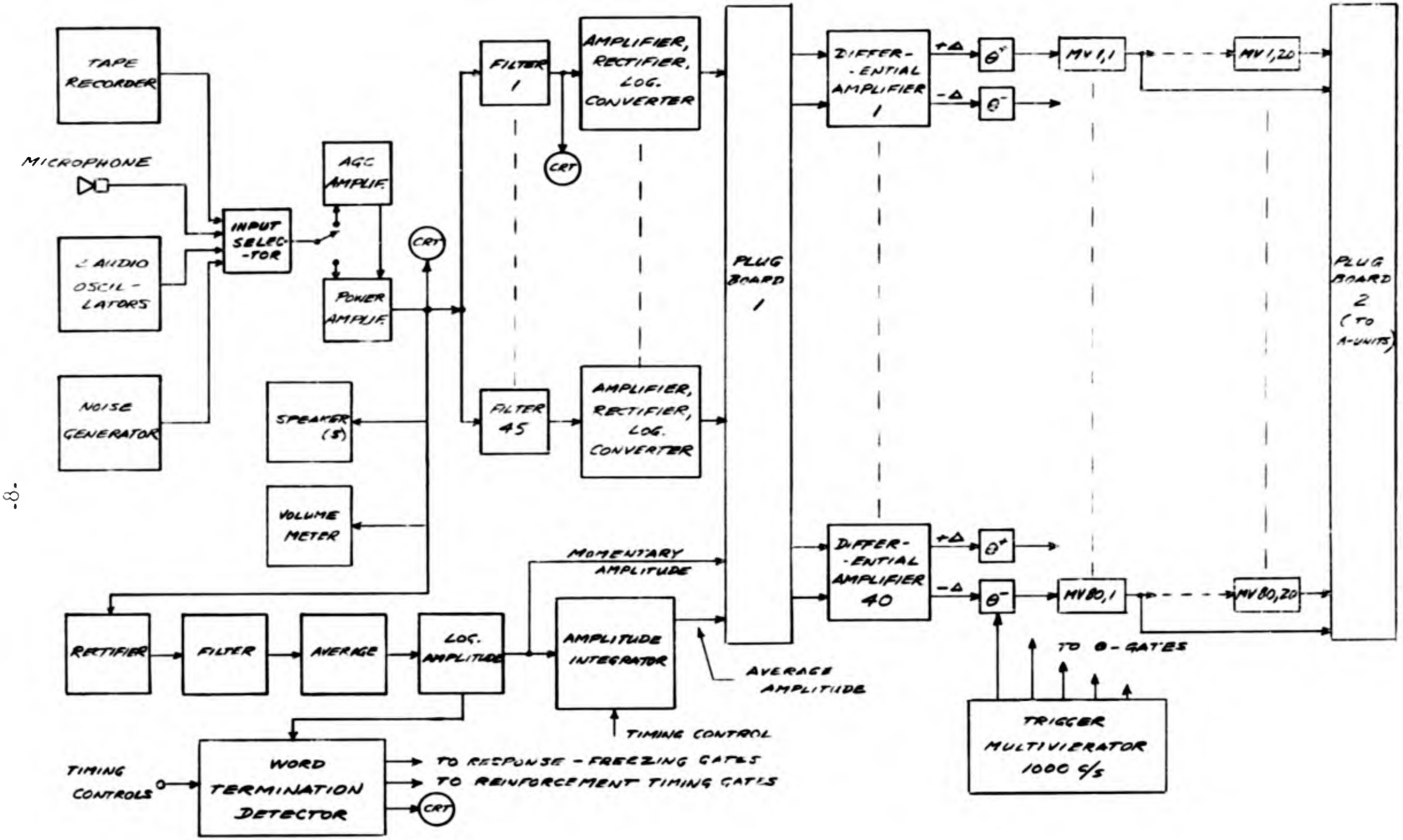


FIG. 1.0.1 : THE SENSORY ANALYSER

1.1 The Input Selector

Dwg. No. 3.2 The Input Selector

The input selector (Figure 1.1.1) is a resistive network designed to equalize the signal levels from the various input devices (microphone, tape recorder, two audio signal generators, and a noise generator) and render them accessible to the audio amplifier. The logarithmic potentiometers are chosen in such a way that at their maximum setting the output of the input selector is about 1 mv. p-t-p. The pots also have an "off" position. These potentiometers, mounted on the audio control panels, are normally used to adjust the amplitude according to the level shown on the amplitude level meter. The tape recorder, main audio amplifier, and AGC controls should be used for calibration purposes only.

Any mixture of signals, as well as any "pure" signal, may be obtained from the input selector. The noise generator is to be used mainly for simulating the effect of various levels of noise added to "clean" recordings. The audio oscillators are handy for adjusting threshold levels in the difference amplifiers; for this purpose, the control room oscilloscope may be used to monitor the two filter or amplitude channels, while the pilot lamp at the end of the sensory delay line to which the differential amplifier is connected indicates when the threshold has been exceeded.

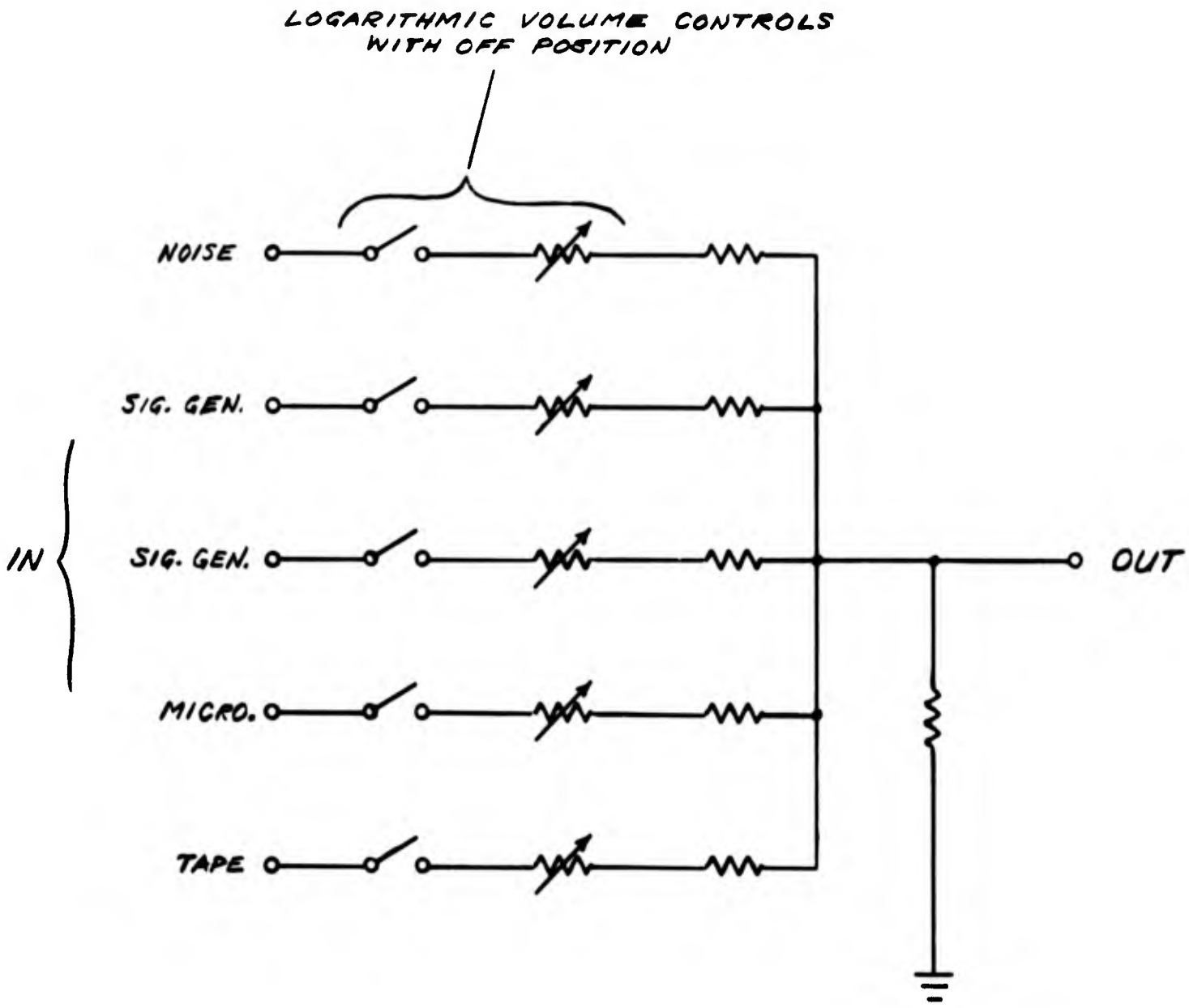


FIG. 1.1.1: INPUT SELECTOR

1.2 Main Audio Amplifier

Elco Manual

The main audio amplifier is an Electronic Instrument Co. Inc. (EICO) model HF-30 30 watt high fidelity integrated unit. Trouble shooting instructions are given in EICO Manual No. HF: 32-1.

Since all the inputs originate from the input selector, the microphone input and preamplifier are used under all conditions. The bass and treble compensation are set to the neutral (center) position, and the loudness control is turned fully clockwise to avoid low and high frequency emphasis. The rumble and scratch filters are left in the "off" position. The level control is adjusted to provide 100 mv. p-t-p signal at the input to the audio filters with maximum input from any of the signal generating devices connected to the input selector. With proper adjustment this should correspond to 5 on the level-setting dial.

A step-down audio transformer and a variable ratio voltage divider reduces the output of the amplifier (4 Ω tap) to a level suitable for feeding into the filters. The aggregate input impedance of the filter bank is at least 5 ohms, so any arrangement which reduces the impedance level of the signal to below 1 ohm is satisfactory.

Note that it is imperative to use high quality shielded wire for all connections to and from the amplifier.

1.3 Automatic Gain Control Amplifier

Dwg. No. 3.1 Automatic Gain Control Amplifier

The purpose of the automatic gain control amplifier (AGC) is to reduce the dynamic range requirements of subsequent stages. Without exceedingly cumbersome precautions, it is unreasonable to expect transistor circuits to handle analog quantities susceptible to a greater than 40 decibels (a factor of 100) variation. The AGC reduces the normal 65 db. range of the human voice (as picked up by a microphone) to an acceptable 40 dbs.

This amplifier is connected between the input selector (section 1.1) and the Eico power amplifier (section 1.2). A remote control relay permits bypassing the AGC altogether, at the operator's discretion. The relay also cuts off the high voltage and filament supply to the tubes.

The control action of the AGC is shown on Fig 1.3.1, and the frequency response on Fig. 1.3.2. The output is free of noticeable distortion except below 100 cps. The minimum attack time (measured to 90 per cent of the final response) is about 15 msecs, while the release time is of the order of 1 second. Both of these time constants are adjustable by means of front panel potentiometers.

The AGC (circuit schematic on Fig. 1.3.3) has a low noise, high impedance input, suitable for direct connection to any (except carbon button) common microphone. Provision is made on the front panel to adjust the gain of the input section to different microphones. The single ended output is designed to feed into a load impedance of at least 50,000 ohms.

The heart of the control action lies in the circuitry associated with the double triode V4. This will be recognized to constitute an unbalanced bridge. Since the plate resistance of the V4 is strongly dependent upon its grid-to-cathode voltage, the signal voltage developed between the output nodes of the bridge is also a function of this grid-to-cathode voltage. This voltage, in turn, is proportional to the amplitude of the input signal, due to the action of A.C. amplifier V6, bridge rectifiers V7 and V8, and D.C. amplifier V9. Note that the amount of control is directly dependent upon the input signal. There is no feedback loop of any kind in the amplifier, hence phase shift and

oscillation problems do not arise.

For initial adjustment (after tube or compcnent changes), it is necessary to warm up the amplifier for at least an hour. Connect a 1000 cps signal generator to the input, and set the level to about 250 mv. Adjust the two level controls, on the panel and on the chassis, to their half way points, and monitor the output with an oscilloscope. Then alternately advance the two settings until distortion in the output is noticed. At this point, the signal voltage across the load resistors of V3 will be about 80 volts peak to peak. Now connect the oscilloscope to the plates of V8 (white wire marked with blue), and adjust the chassis balance control until alternate peaks of the waveform are of equal height. This is necessary to limit distortion at low frequencies, since the output of the bridge rectifier is only capacitively filtered in order to avoid time lags.

Now replace the signal generator with the microphone to be used, and measure the maximum input generated by talking loudly into the microphone at close range. Set the signal generator at the measured level, and substitute it for the microphone. Then adjust the panel level control for maximum output without distortion. The AGC is now ready for action.

Some low frequency distortion will occur before the amplifier is fully warmed up, but this will usually affect only a deep male voice. Distortion may also occur if the supply voltage is not kept at exactly 210 volts.

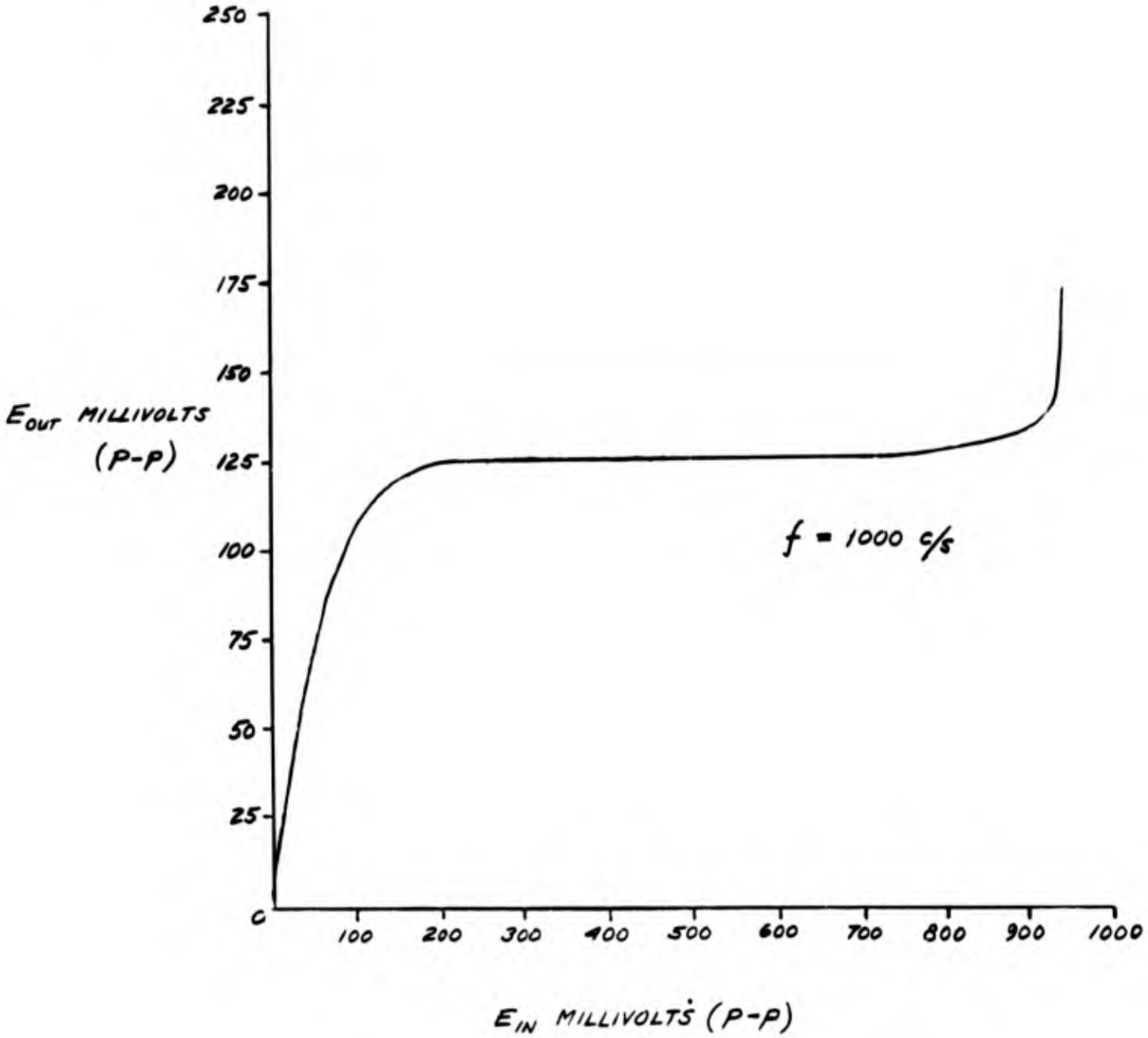


FIG. 1.3.1: AMPLITUDE RESPONSE OF AGC AMPLIFIER

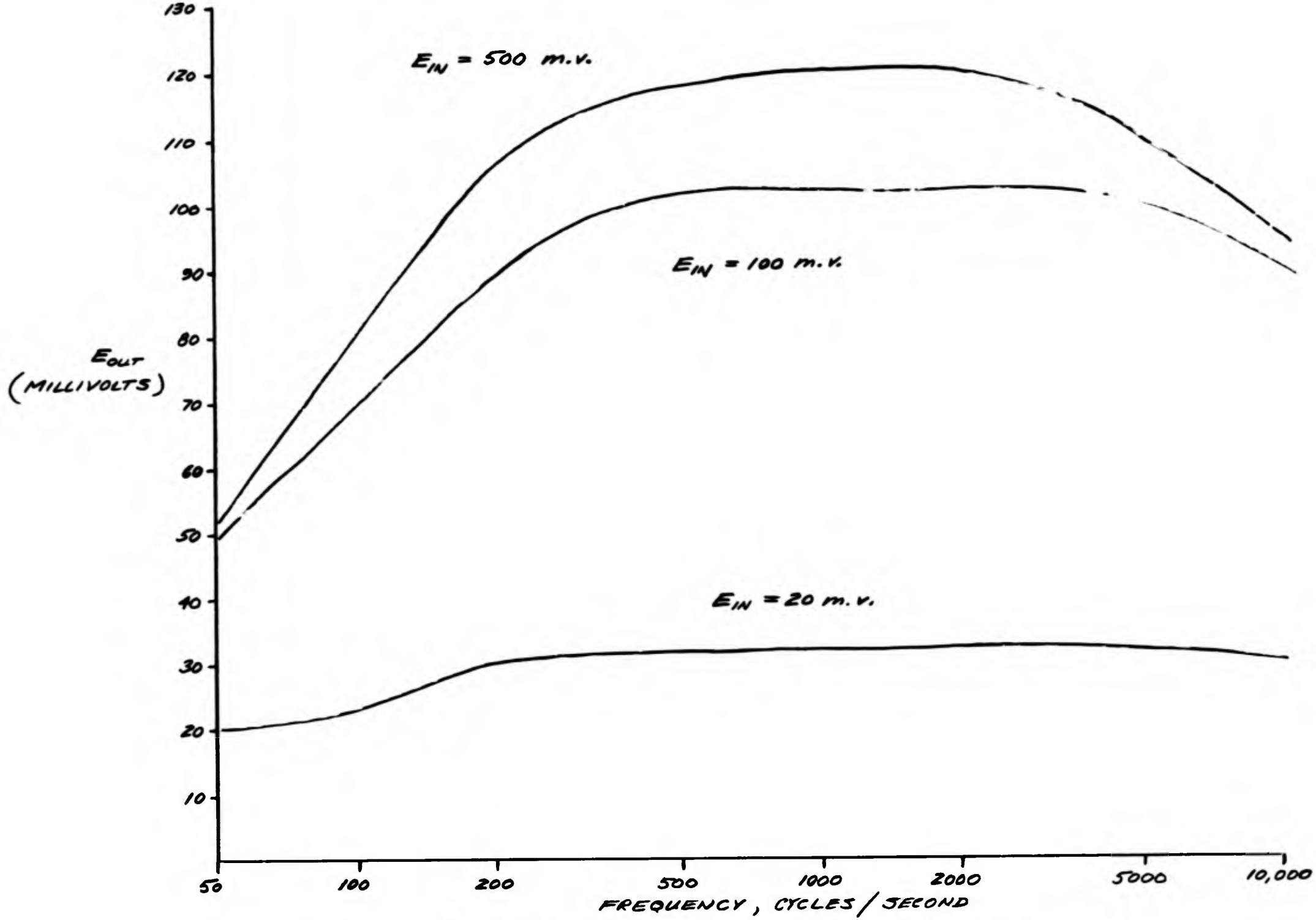


FIG. 1.3.2: FREQUENCY RESPONSE OF AGC AMPLIFIER

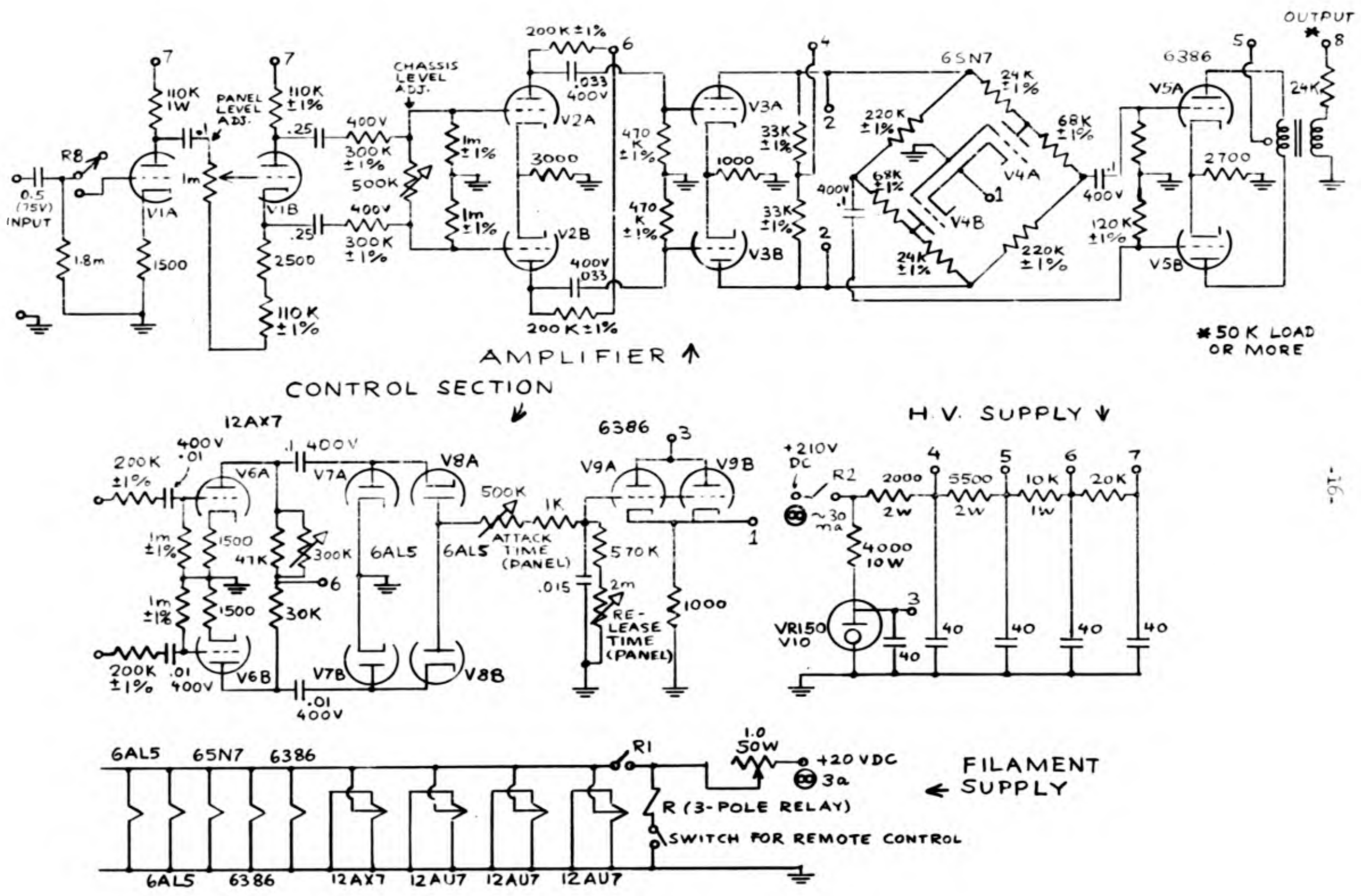


FIG. 1.3.3 : AGC CIRCUIT DIAGRAM

1.4 Volume Monitors

Dwg. No. 3.3 Loudspeaker Controls
4.2.4 Volume Detector Amplifier
4.2.5 Average Amplitude Detector

The volume monitoring system, shown on figure 1.4.1, is quite straightforward. The signal from the input selector (section 1.1) is fed to two loudspeakers through a matching transformer and volume control pads. The output of the input selector is also displayed on the logarithmic volume meter (100 mv full scale deflection) and serves as input to the volume detector amplifier. This amplifier (figure 1.4.2) is similar to the forty-five audio amplifiers described in section 1.6. The smoothing circuit is borrowed from Gunnar Fant's "Acoustic Analysis and Synthesis of Speech with Applications to Swedish"; it is an optimum phase designed LRC whole section low pass filter with a cut off frequency of 300 radians per second (about 50cps). The nominal impedance of 8000 ohms satisfies both the amplifier and the parallel combination of the inputs of the word termination detector (section 3.8) and the standard log converter without any impedance matching other than a 60 KΩ bleeder.

The average amplitude indicator (fig. 1.4.3) is an R-C integrator isolated by two inverting amplifiers. The net gain of this circuit is unity. The time constant of the integrator may be varied from 0.1 second to 1.0 second by means of potentiometer R1.

Provisions are made to monitor on the screen of the control room oscilloscope the total speech waveform injected into the perceptron, the momentary amplitude, and the average amplitude.

Note that either the momentary amplitude or the average amplitude signal may be used with any frequency channel for comparison in a difference amplifier. The signals, as found on plug board number one, are compatible.

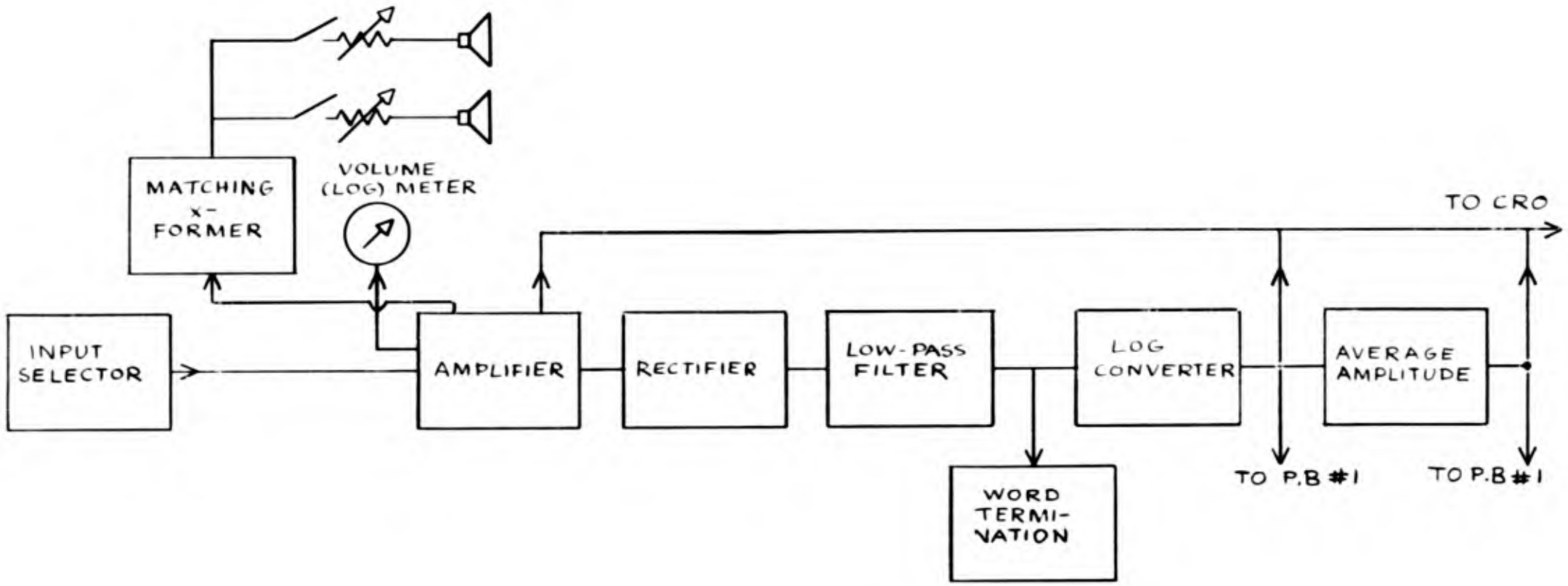
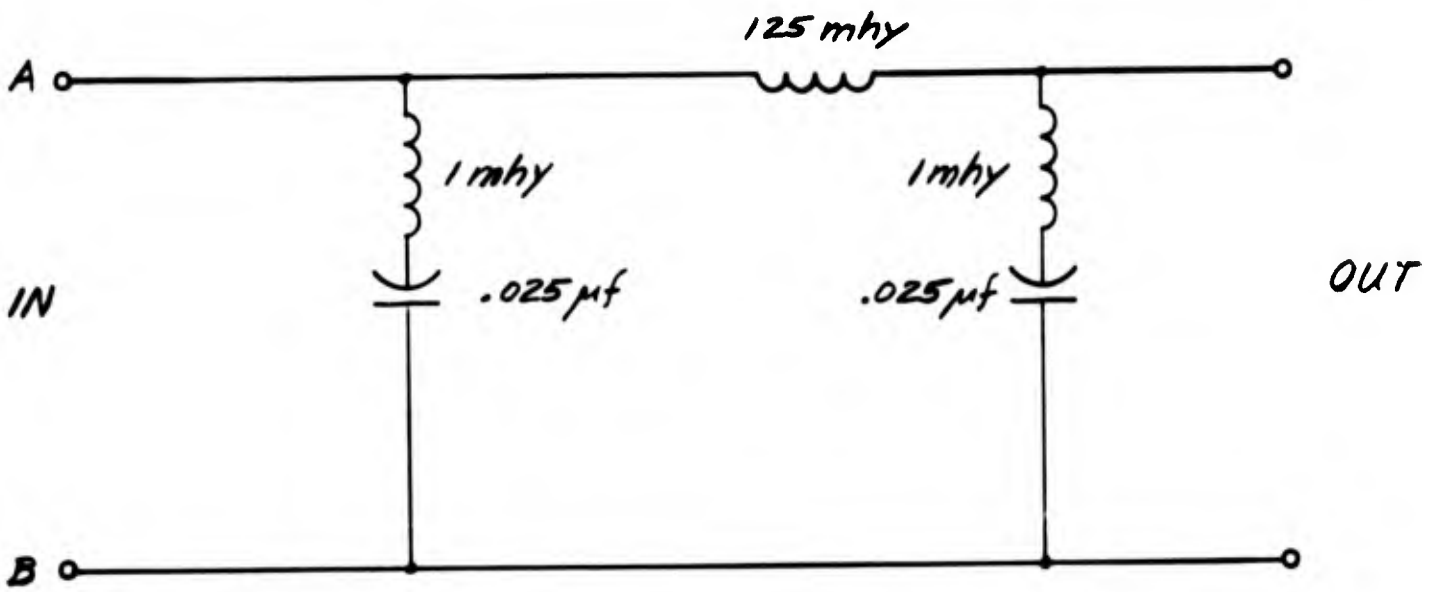


FIG. 1.4.1 : VOLUME MONITOR BLOCK DIAGRAM



ATTACHED TO AMPLIFIER IDENTICAL WITH FIG. 1.6.1, AT POINTS "A" AND "B", SUBSTITUTING FOR CIRCUIT TO RIGHT OF A-B IN FIG. 1.6.1

FIG. 1.4.2: FILTER FOR AUDIO MONITOR AMPLIFIER

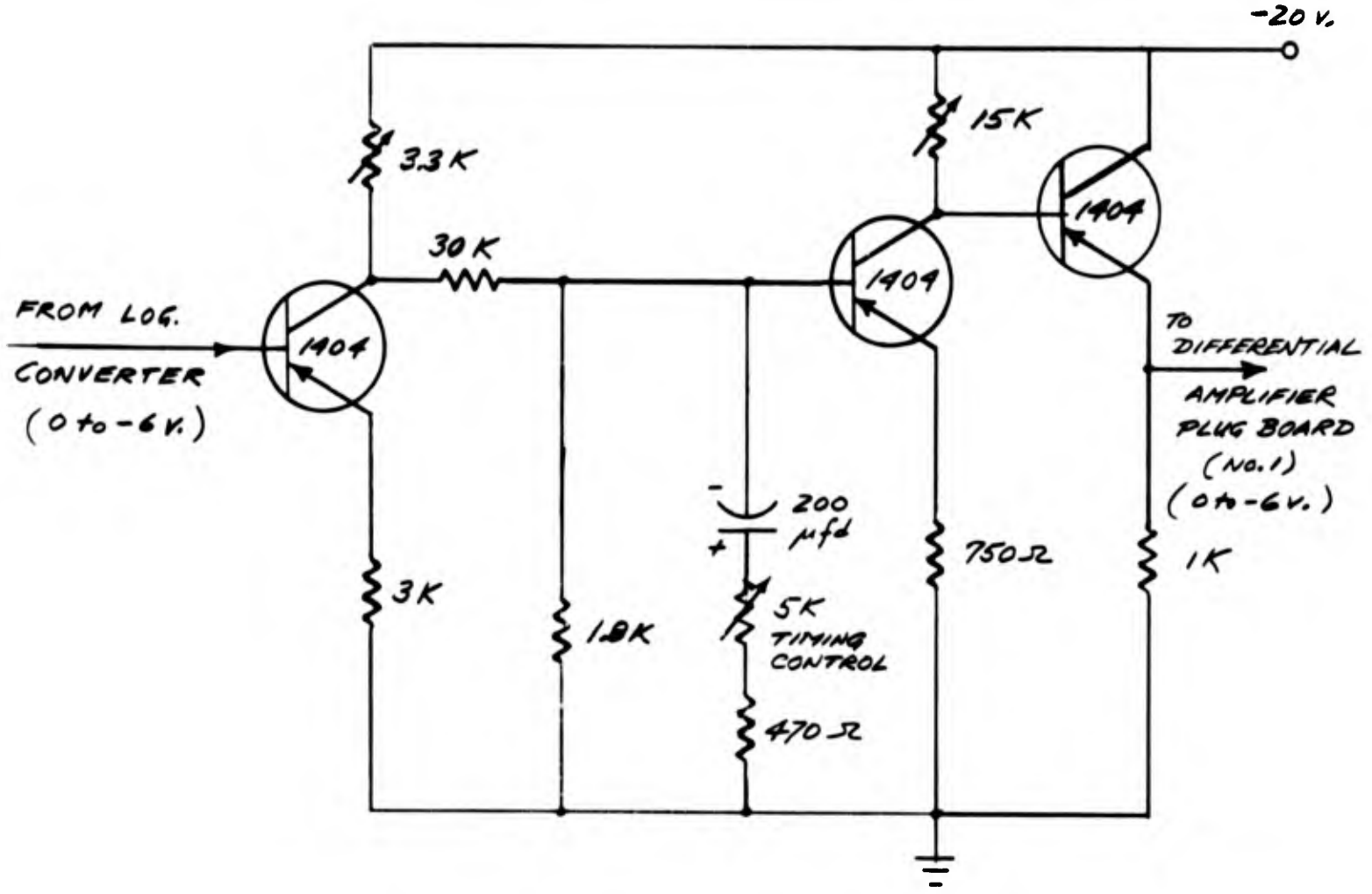


FIG. 1.4.3: AVERAGE AMPLITUDE INDICATOR

1.5 Audio Filters

Dwg. No. 4.2.1 Filter Amplifier and Log Converter
2.6 Rack No. 1, Front View

The 45 audio filters (fig. 1.5.1) are series resonant L-C circuits using high-Q inductors. The center frequencies are uniformly distributed on the pitch (mel) scale, which roughly approximates human audio response. The equivalence between pitch and frequency may be expressed by

$$P = \frac{1000}{\log 2} \log \left(1 + \frac{f}{1000}\right)$$

where P is in mels
and f is in cycles per second

This equation is plotted in fig. 1.5.2. In addition to its center frequency f_2, each filter may be tuned to f_1 and to f_3 by switching capacitors. f_1 has been chosen equal to $\frac{2}{3} f_2$, and f_3 equal to $\frac{3}{2} f_2$. The ranges attainable by the different settings are plotted on both pitch and frequency scales in fig. 1.5.3.

The output is the voltage developed across a series resistor. The five values of resistance which may be switched in here yield bandwidths corresponding to factors of merit (Q) of 1, 3, 5, 8, and 12. The Q and the bandwidth are related by $BW = \frac{f_c}{Q}$. The resistance values here have been chosen to be large compared to the internal equivalent resistance of the inductors (that of the capacitors is negligible) so that at resonance most of the input voltage is developed across the output resistor.

Since only the relative amplitudes of the filter outputs are taken into account by the difference amplifiers, the change of about 20% in amplitude as the Q is changed from 1 to 12 is immaterial as long as the two filters connected to a single difference amplifier are both set to the same Q. In a further effort to minimize output amplitude variation with frequency, each inductor was padded with a series resistance to present an unloaded Q of 40 at the center frequency.

The 1962-63 United Transformer Corporation Catalogue on Electric Wave

Filters and High Q Coils covers the overall characteristics of inductors used in the audio filters, while fig. 1.5.4 shows the representative Q vs. frequency plots of the different units. It is to be noted that for best performance, the inductors should be used at low (mv) voltage levels.

The capacitors are +0%, -5% tolerance components padded with small mica capacitors to resonate with the coils at the design frequencies. To keep the bandwidth and the resonant gain as constant as possible, precision resistors were used throughout.

The design values of the various components appear in Figure 1.5.5. R_L refers to the internal equivalent resistance of the inductor measured at the center frequency, R_p is the value of the padding resistor required to bring the Q down to 40, the r_i's are the resistance values, which, in combination with R_L and R_p would yield the appropriate filter bandwidths, and the R_i's are the actual resistors on the filter panels. R_i in parallel with the input resistance of the next stage is equal to r_i.

Figure 1.5.6 shows the measured resonant frequencies and bandwidth of the 45 filters with all possible settings.*

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* Before deciding on the simple passive filter described above, several other approaches were explored. Odarchenko (see Filter and Multivibrator by A. Odarchenko) worked on a continuously variable center frequency filter based on the well known parallel-T null network. The chief difficulty here was interaction between frequency and bandwidth adjustments, and insufficient frequency variability. Liskov tried shifting the poles of a two-stage R-C filter with an active feedback network, but could not obtain a sufficiently narrow bandwidth without oscillations. Commercial variable parameter bandpass filters begin at about $250 a piece. A firm of consulting engineers submitted a bid for the whole filter network at $8000. In view of these impasses, the several requirements for the filters were somewhat relaxed, resulting in the adoption of the resonant L-C circuit. Components for the latter averaged about $20 a filter.

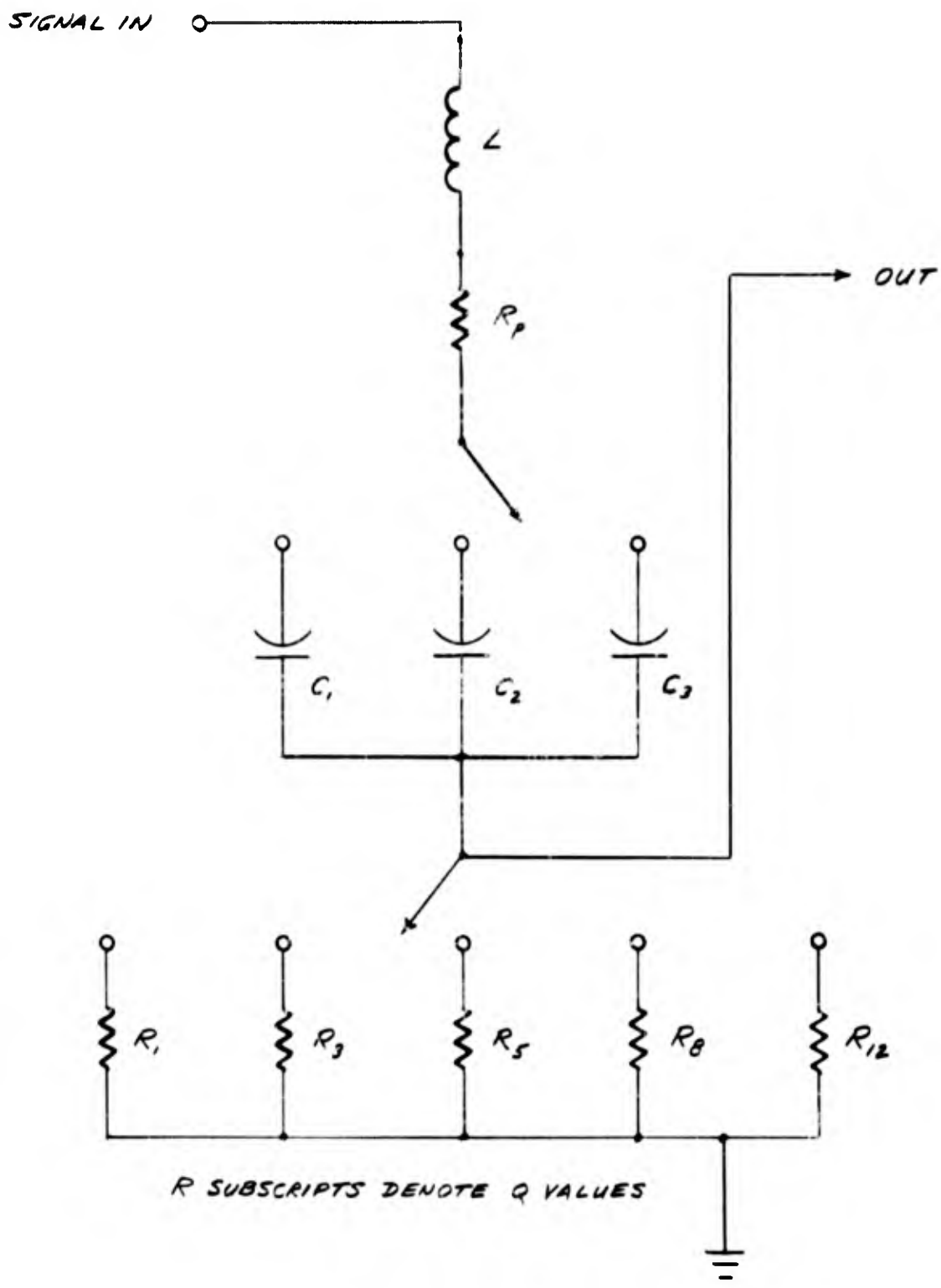


FIG. 1.5.1: AUDIO FILTER CIRCUIT DIAGRAM

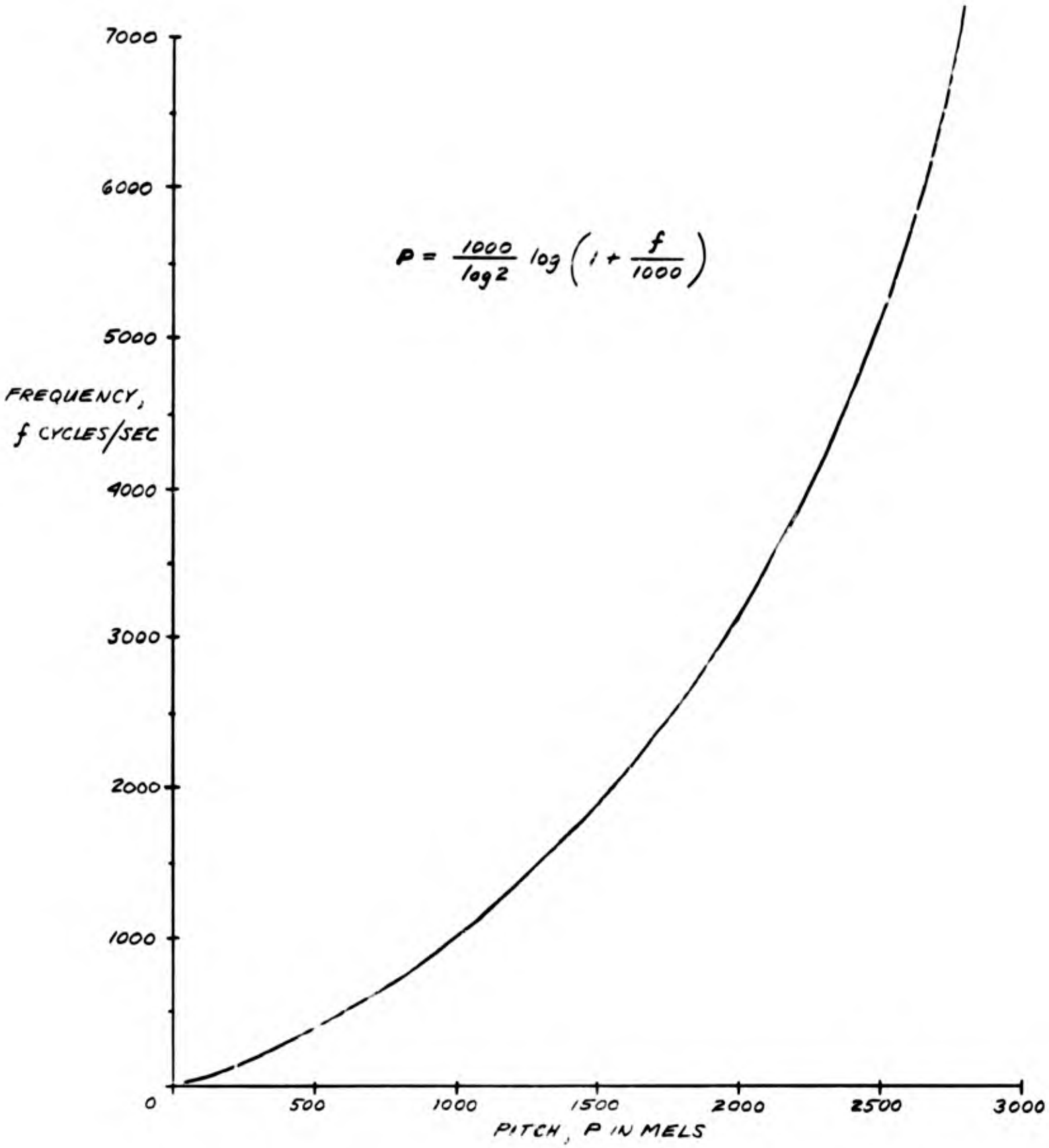
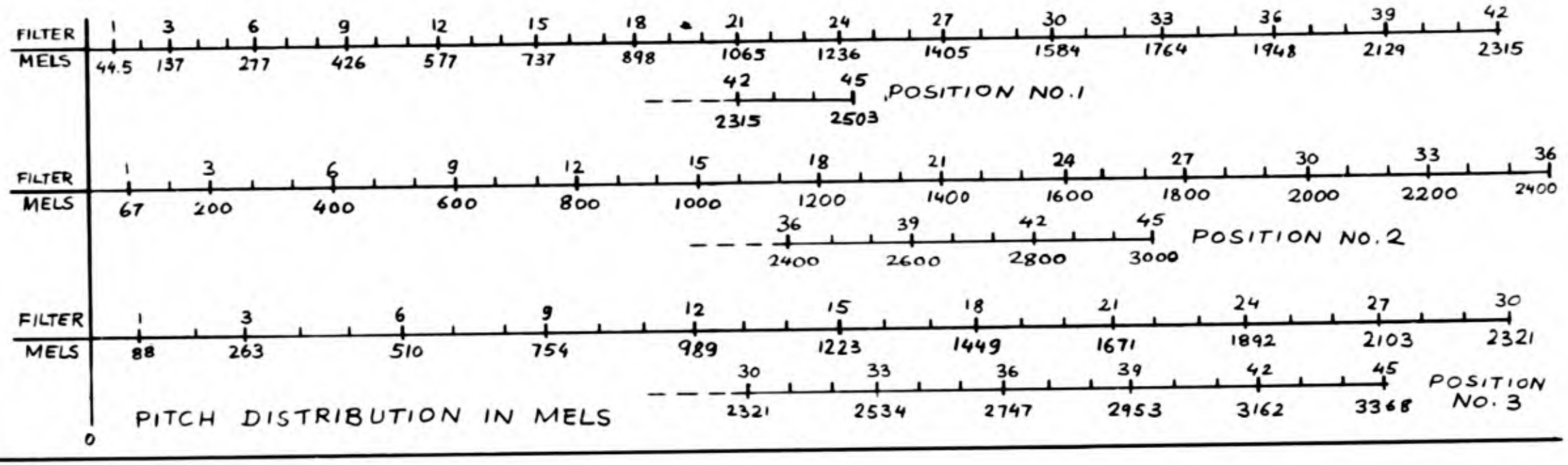


FIG. 1.5.2: PITCH-FREQUENCY EQUIVALENCE



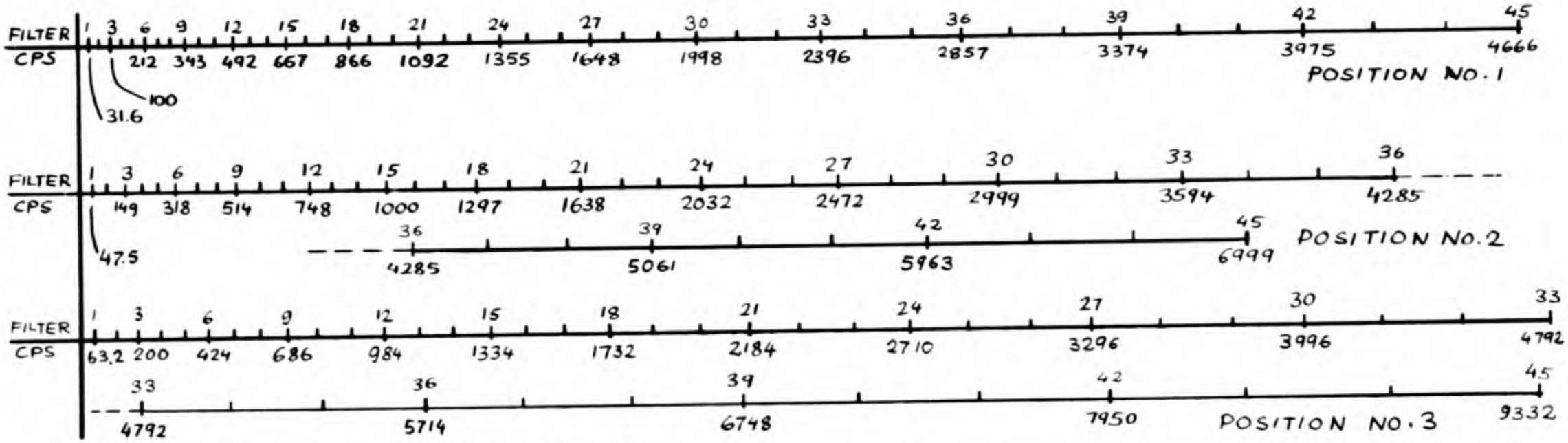


FIG. 1.5.3 : AUDIO FILTER CENTER FREQUENCY DISTRIBUTION

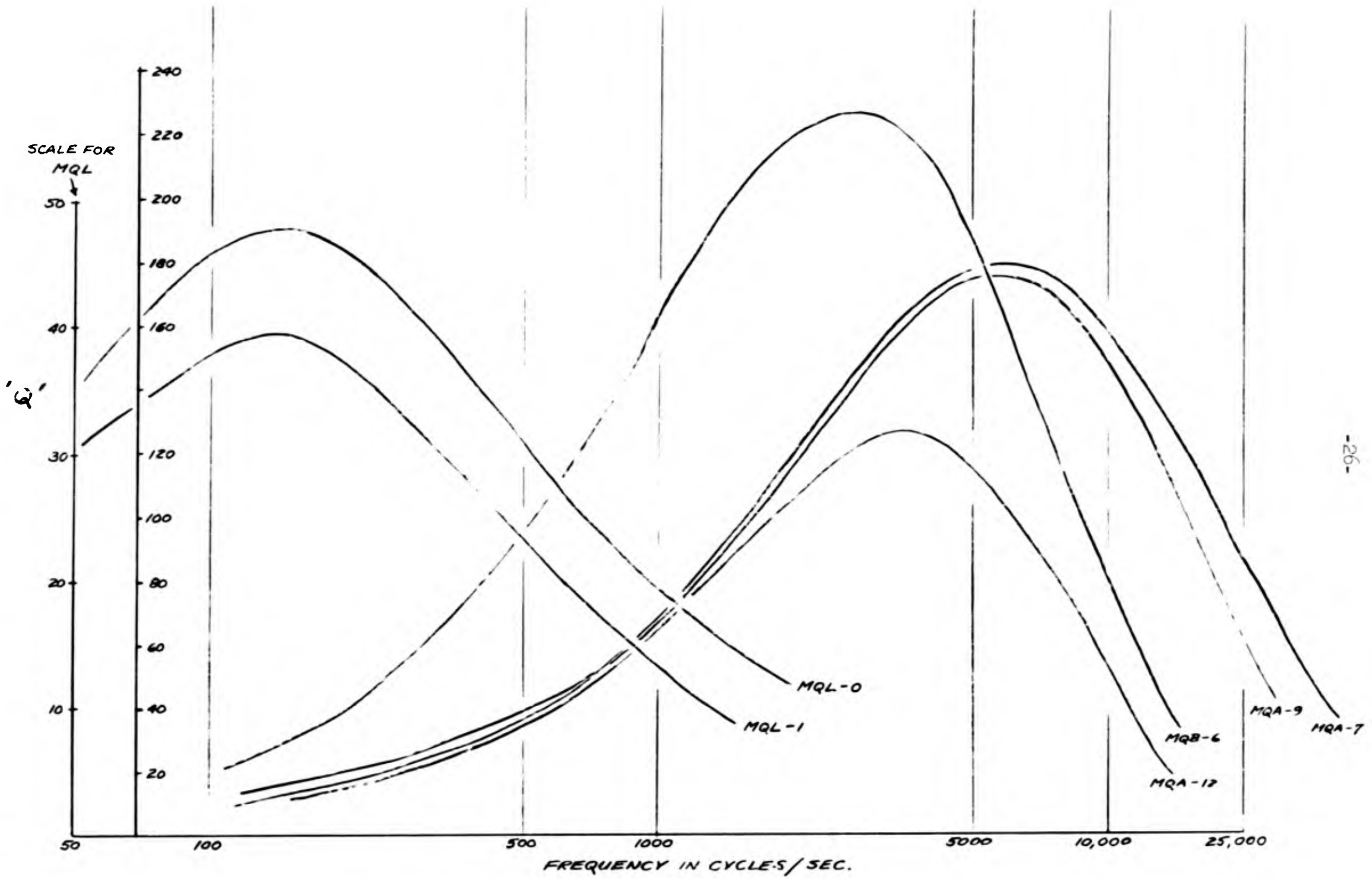


FIG. 1.5.4: Q VARIATION IN AUDIO INDUCTORS

Figure 1.5.5 Component Values for Audio Filters

F	fc	BW_1	BW_2	BW_3	BW_4	BW_5	Q_1	Q_2	Q_3	Q_4	Q_5
	31.6	51	17.1	10.4	7	5.1	.62	1.8	3	4.5	6.2
1	47.5	53.4	17.6	10.8	7	5.5	.89	2.7	4.4	6.8	8.7
	63.2	49	17.2	11	7.2	5.5	1.3	3.7	5.7	8.8	11.5
	66	109.3	36.2	21.8	13.7	9.5	.6	1.8	3.	4.8	7.
2	96	90.7	33.	23.8	13.2	10	1.1	2.9	4.	7.3	9.1
	128	100.4	34.8	22	14	10.5	1.3	3.8	5.8	9.2	12.2
	100	129.8	46.6	28.6	17.5	12.4	.78	2.1	3.5	5.7	8.1
3	149	120	48	31	20.5	14.5	1.2	3.1	4.8	7.3	10.3
	200	170	60	35	33	18	1.2	3.3	5.7	6.1	11.1
	135	177.5	65.5	42.7	25	16	.76	2.1	3.2	5.4	8.5
4	202	209.5	80	49	30	21.5	.97	2.5	4.1	6.7	9.4
	270	142	73	45	30	20	1.9	3.7	6	9	13.5
	173	277	77	55	38	33	.63	2.3	3.2	4.6	5.3
5	259	286	92	61	46	36	.91	2.8	4.3	5.6	7.2
	346	265	100	65	47	42	1.2	3.5	5.3	7.4	8.2
	212	330	105	67	46	34	.64	2	3.2	4.6	6.2
6	318	310	118	61	43	36	1.	2.7	5.2	7.4	8.9
	424	294	112	78	55	48	1.4	3.8	5.5	7.7	8.8
	254	388	128	81	51	37	.66	2.	3.1	5.	6.9
7	381	362	140	69	50	41	1.	2.7	5.5	7.6	9.3
	508	356	139	94	64	54	1.4	3.6	5.4	8.	9.4
	297	463	121	82	56	44	.64	2.5	3.6	5.3	6.8
8	450	483	152	95	63	42	.93	3.	4.7	7.2	10.7
	594	402	137	79	62	47	1.5	4.3	7.5	9.6	12.6
	343	703	230	135	104	83	.49	1.5	2.5	3.3	4.1
9	514	619	185	126	90	70	.83	2.8	4.1	5.8	7.4
	686	472	146	107	71	52	1.4	4.7	6.4	9.7	13.2
	390	617	189	112	66	52	.63	2.1	3.5	5.9	7.5
10	585	702	205	131	89	60	.83	2.9	4.5	6.6	9.8
	780	464	197	126	84	60	1.7	4.	6.2	9.3	13.
	439	665	225	145	85	69	.66	2.	3.	5.2	6.4
11	664	593	217	136	89	65	1.1	3.1	4.9	7.5	10.2
	875	600	203	142	96	90	1.5	4.3	6.2	9.1	9.7

F	fc	BW_1	BW_2	BW_3	BW_4	BW_5	Q_1	Q_2	Q_3	Q_4	Q_5
	492	739	246	163	104	74	.67	2	3	4.7	5.2
12	747	703	251	158	104	70	1.1	3	4.7	7.2	10.7
	980	705	213	154	103	75	1.4	4.6	6.4	9.5	13
	547	830	285	174	109	82	.66	1.9	3.1	5.	6.7
13	820	836	270	167	102	79	.98	3.	4.9	8.	10.4
	1100	813	254	164	112	86	1.4	4.3	6.7	9.8	12.8
	603	905	310	183	114	82	.67	2.	3.3	5.3	7.4
14	908	977	318	192	123	80	.93	2.9	4.7	7.4	11.4
	1215	862	290	175	120	90	1.4	4.2	7.	10.1	13.5
	667	987	303	196	128	88	.68	2.2	3.4	5.2	7.6
15	1008	1006	354	196	128	87	1.	3.1	5.5	8.4	12.4
	1334	930	320	200	130	100	1.4	4.2	6.7	10.3	13.3
	731	1022	332	210	142	101	.71	2.2	3.5	5.2	7.2
16	1150	1285	385	250	157	117	.9	3.	4.6	7.3	9.8
	1462	1161	350	205	150	100	1.3	4.2	7.1	9.8	12.2
	796	1275	359	224	125	105	.62	2.2	3.6	6.4	7.6
17	1194	1390	415	240	160	122	.86	2.9	5.	7.5	9.8
	1592	1140	295	240	150	120	1.4	5.4	6.6	10.6	13.3
	866	1263	440	296	183	148	.67	2.	2.9	4.7	5.9
18	1298	1417	415	257	155	120	.92	3.1	5.1	8.4	10.8
	1720	1290	320	260	170	120	1.3	5.4	6.6	10.1	14.4
	938	1360	474	282	180	110	.68	2.	3.3	5.2	8.5
19	1406	1512	445	280	175	120	.93	3.2	5.	8.	11.7
	1876	1350	465	305	180	120	1.4	4.	6.2	10.4	15.6
	1014	1654	520	292	182	137	.61	2.	3.5	5.6	7.4
20	1520	1565	490	315	205	140	.97	3.1	4.8	7.4	10.9
	2040	1440	490	310	210	160	1.4	4.2	6.6	9.7	12.7
	1092	1855	932	613	415	310	.59	1.2	1.8	2.6	3.5
21	1638	1680	565	335	215	150	.98	2.9	4.9	7.6	10.9
	2184	1630	525	340	215	150	13.4	4.2	6.4	10.2	14.5
	1164	1030	470	320	210	150	1.1	2.5	3.6	5.6	7.8
22	1760	1010	490	305	215	160	1.7	3.6	5.8	8.2	11.0
	2350	1140	520	300	220	170	2.1	5.6	7.8	10.7	13.9
	1264	1778	620	370	240	180	.71	2.	3.4	5.3	7.
23	1893	1500	580	285	230	190	1.3	3.3	6.6	8.2	10.
	2524	1710	540	340	240	180	1.5	4.7	7.4	10.5	14.

F	fc	BW_1	BW_2	BW_3	BW_4	BW_5	Q_1	Q_2	Q_3	Q_4	Q_5
	1355	2060	660	435	290	210	.66	2.1	3.1	4.7	6.5
24	2032	2090	550	440	280	215	.97	3.7	4.6	7.3	9.5
	2710	2090	650	440	300	230	1.3	4.2	6.2	9.	11.8
	1450	1920	725	460	300	220	.76	2.	3.2	4.8	6.6
25	2200	2420	770	500	310	220	.91	2.9	4.4	7.4	10.
	2900	2280	740	420	290	200	1.3	3.9	6.9	10.	14.5
	1570	2070	780	480	305	200	.76	2.	3.3	5.2	7.8
26	2324	2510	750	490	340	240	.93	3.1	4.8	6.9	9.7
	3098	2370	650	460	300	230	1.3	4.8	7.	10.3	13.4
	1660	2040	780	500	330	240	.81	2.1	3.3	5.	6.9
27	2500	2710	740	470	300	230	.92	3.4	5.3	8.3	10.2
	3296	2560	810	490	320	240	1.3	4.1	6.7	10.3	13.7
	1763	2200	845	560	340	250	.8	2.1	3.1	5.2	7.1
28	2645	3160	870	560	390	280	.84	3.	4.7	6.8	9.4
	3526	3210	870	520	360	260	1.1	4.	6.8	9.8	13.5
	1879	2460	895	535	360	260	.76	2.1	3.5	5.2	7.2
29	2818	3350	980	590	390	250	.84	2.9	4.8	7.2	11.3
	3758	2650	870	580	360	260	1.4	4.3	6.5	10.4	14.4
	1998	2610	1060	600	380	280	.77	1.9	3.3	5.3	7.2
30	2999	3530	1080	590	400	270	.85	2.8	5.1	7.5	11.1
	3996	2790	850	580	380	290	1.4	4.7	6.9	10.5	13.8
	2125	3040	1080	645	430	300	.7	2.	3.3	5.	7.1
31	3187	3290	1070	630	440	320	.97	3.	5.1	7.2	10.
	4250	3340	1040	670	420	300	1.3	4.1	6.3	10.1	14.1
	2257	3140	1160	690	450	300	.72	1.9	3.3	5.	7.5
32	3385	3360	1110	690	450	310	1.	3.	4.9	7.5	10.9
	4515	3410	1170	670	440	330	1.3	3.8	6.7	10.2	13.7
	2396	3240	1170	740	470	330	.74	2.	3.2	5.1	7.3
33	3594	3690	1160	700	470	340	.98	3.1	5.1	7.7	10.6
	4792	3690	1130	700	450	340	1.3	4.2	6.9	10.6	14.1
	2540	4030	1350	760	490	330	.63	1.9	3.3	5.2	7.7
34	3810	3710	1170	740	490	360	1.	3.2	5.2	7.8	10.6
	4960	3770	1100	730	480	340	1.3	4.5	6.8	10.3	14.6
	2691	4220	1220	790	510	340	.64	2.2	3.3	5.3	7.9
35	4037	4440	1290	790	520	360	.91	3.1	5.1	7.8	11.2
	5382	4100	1270	790	530	340	1.3	4.2	6.8	10.1	15.8

F	fc	BW_1	BW_2	BW_3	BW_4	BW_5	Q_1	Q_2	Q_3	Q_4	Q_5
	2857	4235	1430	850	560	380	.68	2.	3.4	5.1	7.5
36	4285	5020	1550	930	610	450	.85	2.8	4.6	7.	9.5
	5730	3820	1340	820	520	380	1.5	4.3	7.	11.	15.
	3017	4560	1425	980	570	390	.66	2.1	3.1	5.3	7.7
37	4525	5370	1570	950	600	430	.84	2.9	4.8	7.5	10.5
	6090	4370	1385	820	560	390	1.4	4.4	7.4	10.8	15.5
	3191	5160	1500	930	580	420	.7	2.1	3.4	5.5	7.6
38	4787	5470	1540	890	580	400	.88	3.1	5.4	8.3	12.
	6382	4570	1490	870	590	430	1.4	4.3	7.3	10.8	14.8
	3374	4625	1570	1040	690	500	.73	2.1	3.2	4.9	6.8
39	5061	5920	1600	1000	700	490	.86	3.2	5.1	7.2	10.3
	6748	4800	1620	1000	690	500	1.4	4.2	6.7	9.8	13.5
	3564	5130	1550	1060	700	505	.7	2.3	3.4	5.1	7.1
40	5346	6290	1760	1060	760	540	.85	3.	5.	7.	9.9
	7128	5510	1800	1070	710	530	1.3	4.	6.7	10.	13.4
	3764	6040	1860	1150	800	540	.62	2.	3.3	4.7	7.
41	5646	4670	1840	1110	760	450	1.2	3.1	5.1	7.4	12.5
	7450	5200	1850	1190	750	580	1.4	4.	6.3	9.9	12.8
	4000	5280	2060	1270	800	570	.76	1.9	3.2	5.	7.
42	5963	4950	1900	1230	790	580	1.2	3.1	4.8	7.6	10.3
	8100	6700	1400	740	580	420	1.2	5.8	11.	14.	19.3
	4220	6260	2150	1290	840	590	.67	2.	3.3	5.	7.2
43	6290	6330	1950	1260	840	600	.94	3.2	5.	7.5	10.4
	8386	6300	2070	1300	840	600	1.3	4.1	6.4	10.	14.
	4424	7070	2160	1360	890	610	.63	2.1	3.3	5.	7.3
44	6636	6875	2000	1250	850	640	.96	3.3	5.3	7.8	10.2
	8848	6380	2000	1300	820	680	1.3	4.2	6.5	10.2	12.5
	4660	6450	2310	1430	920	670	.72	2.	3.3	5.1	7.
45	7090	7440	2110	1350	880	630	.95	3.4	5.2	8.1	11.2
	9220	6970	2120	1330	900	650	1.3	4.3	6.9	10.1	14.2

Figure 1.5.6 Audio Filter Performance Chart

Type	Filter	L (hys)	Fc (cps)	C (μF)	R_p (Ω)	R_1 (Ω)	R_3 (Ω)	R_5 (Ω)	R_8 (Ω)	R_{12} (Ω)
MQL-1	1	10	31.6	2.53						
			47.5	1.12	29.4	2980	910	500	275	148
			63.2	.640						
	2	10	65	.620						
			96	.275	81	6550	1870	1020	560	303
			128	.155						
	3	10	100	.252						
			149	.112	103	10800	2970	1610	870	470
			200	.063						
	4	10	135	.140						
			202	.063	164	15000	4150	2320	1190	640
			270	.035						
MQL-0	5	1	173	.840						
			259	.376	14.4	1620	500	275	150	80
			346	.212						
	6	1	212	.560						
			318	.248	16.7	2010	607	335	183	100
			424	.140						
	7	1	254	.392						
			381	.176	11	2420	730	403	221	120
			508	.100						
MQB-6	8	1	297	.288						
			445	.128	62.5	2850	845	466	256	137
			594	.072						
	9	1	343	.216						
			514	.096	74	3330	935	540	293	162
			686	.054						
	10	1	390	.168						
			585	.074	87	3800	1130	613	337	183
			780	.042						
	11	1	439	.131						
			659	.0584	101	4305	1265	705	381	210
			878	.0328						

Type	Filter	L (hys)	Fc (cps)	C	R_p	R_1	R_3	R_5	R_8	R_{12}
MQL-12	12	1	492 745 984	.105 .0456 .0261	64	4930	1440	795	430	234
	13	1	547 820 1094	.0847 .0376 .0211	75	5480	1592	875	475	258
	14	1	603 905 1206	.0695 .0309 .0174	86	6120	1770	963	525	284
	15	1	667 1000 1334	.058 .0253 .0142	91	6350	1945	1065	573	314
	16	1	731 1096 1462	.0475 .0211 .0119	117	7585	2140	1170	638	345
	17	1	796 1194 1592	.0400 .0178 .0100	140	8380	2350	1280	698	378
	18	1	866 1298 1732	.0339 .0150 .0085	160	9235	2570	1396	759	411
	19	1	938 1406 1876	.0288 .0128 .0072	184	10140	2785	1513	823	446
	20	1	1014 1520 2028	.0247 .0109 .0062	208	11130	3022	1640	891	483
	21	1	1092 1638 2184	.0212 .00942 .00531	232	12200	3290	1770	960	520
	22	1	1164 1746 2328	.0187 .0083 .00457	254	13100	3508	1890	1020	555
	23	1	1264 1893 2524	.0158 .00687 .00397		14600	3830	2050	1100	650

Type	Filter	L (hys)	Fc (cps)	C	R_p	R_1	R_3	R_5	R_8	R_{12}
MQA-9	24	.3	1355 2032 2710	.0461 .0204 .0115	93	3970	1130	650	360	200
	25	.3	1450 2175 2900	.0401 .0178 .0100	100	4270	1250	690	375	200
	26	.3	1549 2324 3098	.0352 .0156 .0088	111	4580	1340	740	400	215
	27	.3	1648 2472 3296	.0310 .0137 .00775	119	4900	1420	785	425	230
	28	.3	1763 2645 3526	.0271 .0121 .00687	130	5300	1520	850	460	250
	29	.3	1879 2818 3758	.0239 .0106 .00598	138	5670	1630	900	490	260
	30	.3	1998 2999 3996	.0211 .0094 .0053	149	6100	1730	960	525	280
	31	.3	2125 3187 4250	.0187 .0083 .00467	165	6640	1910	1020	560	300
	32	.3	2257 3385 4515	.0166 .00735 .00414	170	6980	1990	1080	600	320
	33	.3	2396 3594 4792	.0147 .00652 .00369	182	7450	2110	1150	625	340
	34	.3	2540 3810 5080	.0131 .00581 .00339	192	7970	2240	1220	675	365
	35	.3	2691 4037 5382	.0117 .00519 .00292	205	8600	2340	1300	720	390

Type Film		L (hys)	Fc (cps)	C	R_p	R_1	R_3	R_5	R_8	R_{12}
	36	.3	2857 4285 5714	.0103 .0046 .00259	220	8950	2550	1380	760	410
	37	.3	3017 4525 6034	.0093 .0042 .00232	235	9750	2700	1460	810	440
	38	.3	3191 4787 6382	.00828 .00369 .00207	235	10400	2850	1540	850	460
MQA-7	39	.12	3374 5061 6748	.0185 .00826 .00463	98	3950	1160	650	350	190
	40	.12	3564 5346 7128	.0165 .00739 .00415	111	4200	1230	690	380	206
	41	.12	3764 5646 7528	.0149 .00661 .00372	118	4460	1310	695	380	203
	42	.12	3975 5963 7950	.0133 .00594 .00333	117	4720	1390	760	414	225
	43	.12	4193 6290 8386	.012 .00534 .003	128	5000	1460	800	440	238
	44	.12	4424 6636 8848	.0108 .0047 .00269	135	5325	1530	850	460	251
	45	.12	4666 6999 9332	.00971 .00431 .00242	146	5630	1633	893	488	265

1.6 Audio Filter Amplifier

Dwg. No. 4.2.1 Filter Amplifier and Log Converter

The filter amplifier (fig. 1.6.1) consists of five transistors numbered Q1 through Q5. Q1 and Q2 are cascaded emitter followers providing a high impedance (54KΩ) input to the signal from the audio filters (section 1.5). Q3 is a high gain (20 db) class A amplifier feeding into emitter follower Q4, which in turn drives the power output stage Q5. Q5 is also operating under class A conditions, but in order to obtain a flat frequency response (3 dbs down from 30 cps to 15 Kcps) with a low price transformer, it incorporates a feedback loop from the secondary of T1 to the base of Q4.

The output of T1 is rectified by a full wave bridge rectifier, and filtered through CH1, C11, and C12. In order to keep the signal frequency ripple below 5% (5V. at 100V.) choke CH1 and filter capacitor C12 are required in the twelve low frequency amplifiers. More smoothing would interfere with the speed of response.

A tap between R21 and R22 is available in order to monitor the output of the filters at the control room oscilloscope. At this point the impedance level is fairly low (about 1000Ω), so the loading effect of the shielded cable (240KΩ per foot at 10,000 cps) is negligible.

Gain set R21 should be adjusted to obtain 100 V.D.C. at the input to the log converters (amplifier side of R33) for 100 mv. p.t.p. input to the amplifier.

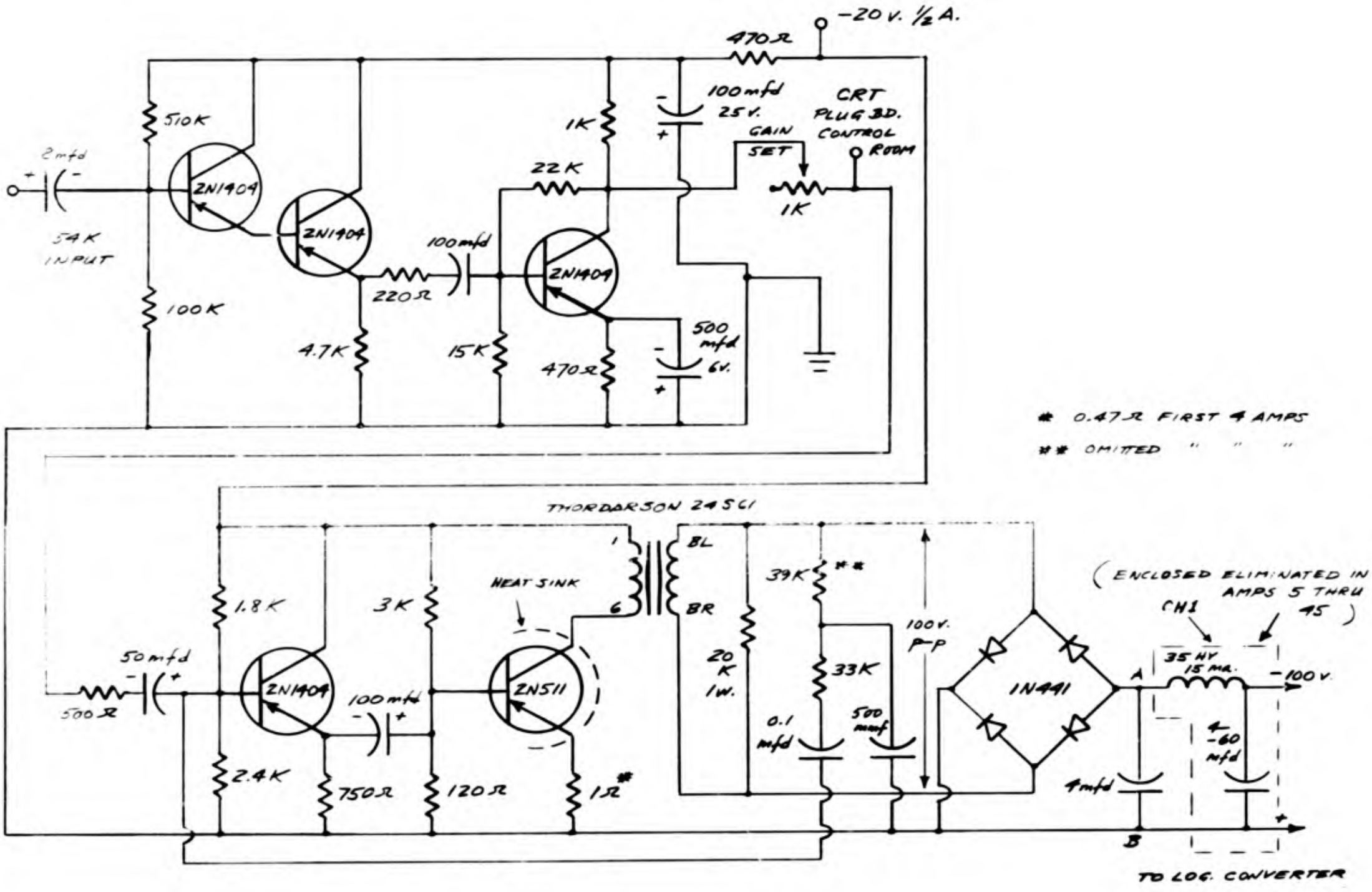


FIG. 1.6.1: AUDIO FILTER AMPLIFIER

1.7 Logarithmic Converters and Reference Supplies

Dwg. No. 4.2.1 Filter Amplifier and Log Converter
4.2.3 Voltage Regulator Assembly

The log converter (fig. 1.7.1) is a resistor-diode network whose transfer function approximates a logarithmic curve by means of straight line segments. The logarithmic conversion allows the association units to pay attention only to the ratios of the amplitudes of the various frequency components - a very useful form of amplitude normalization.

The particular function to be approximated, $y = 3 \log_{10} x$, was chosen because its realization yields practicable voltage and impedance levels. The ideal curve, and the input-output curve of a typical log conversion unit, are shown on figure 1.7.2.

The reference supply voltages represent the y-intercepts of the straight line segments. These voltages are accurately maintained by the log converter voltage regulators at the following values:

V.R. no. 1 at 1.2 Volts
V.R. no. 2 at 2.3 Volts
V.R. no. 3 at 3.3 Volts
V.R. no. 4 at 4.3 Volts

Each of the four log converter regulators is a three transistor circuit, as shown on figure 1.7.3. Q3 is part of the primary feedback loop through R39 and diodes CR8; it acts as a comparison amplifier feeding the cascaded emitter followers Q1 and Q2. R30, R31, and the Zener diode CR7 form the secondary feedback network (the preregulator), and also serve to reduce the ripple current.

Voltage set R39 should not be adjusted to obtain an output more than 20% larger than the nominal value.

A quick check on the frequency channels may be performed as follows: set the input voltage to the audio amplifier at 100 mv p.t.p. Then the input to the log converters should be exactly 100 V, and the output 6 V.D.C.

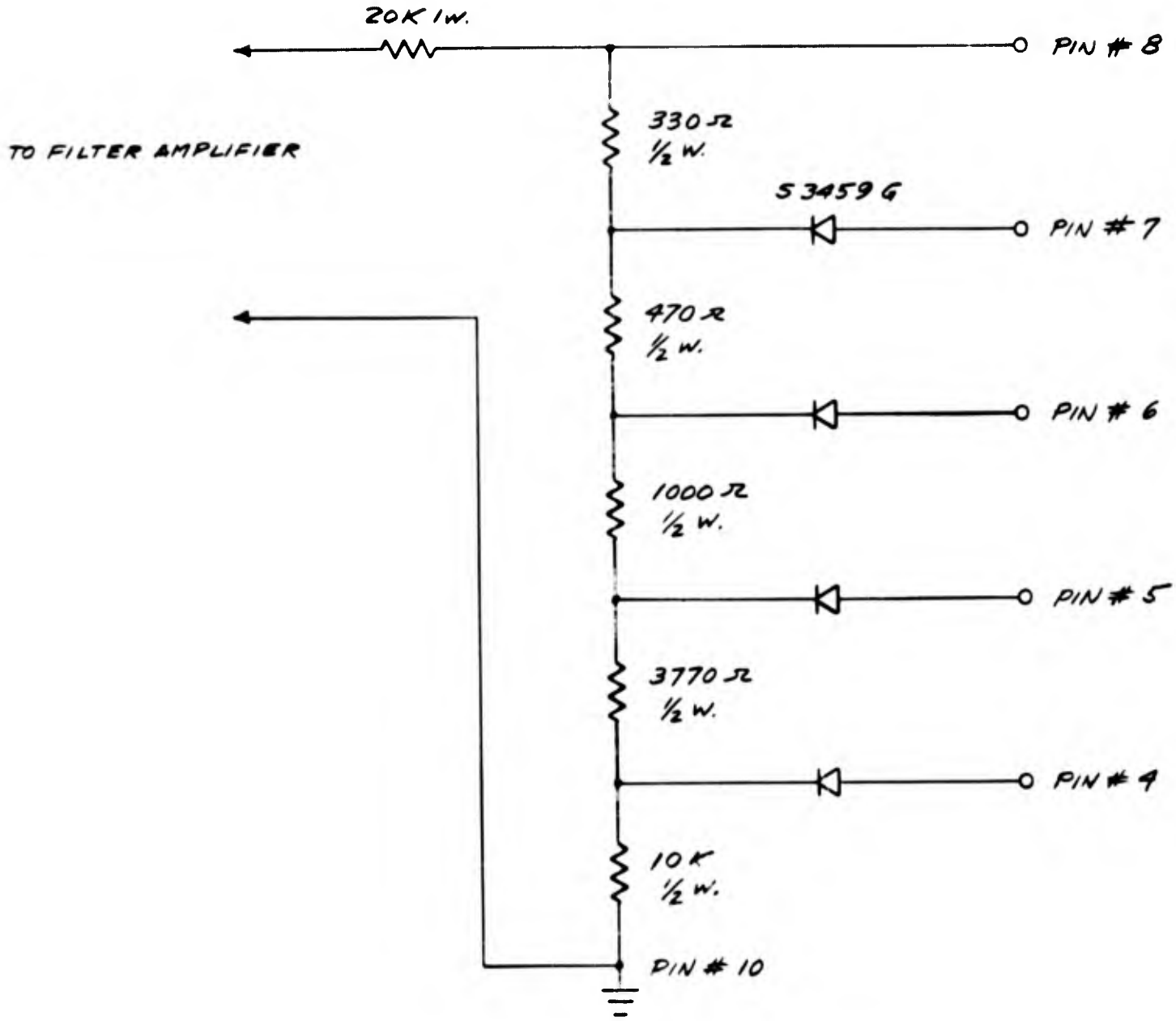


FIG. 1.7.1: LOGARITHMIC CONVERTER

FIG. 1.7.2: AMPLITUDE RESPONSE

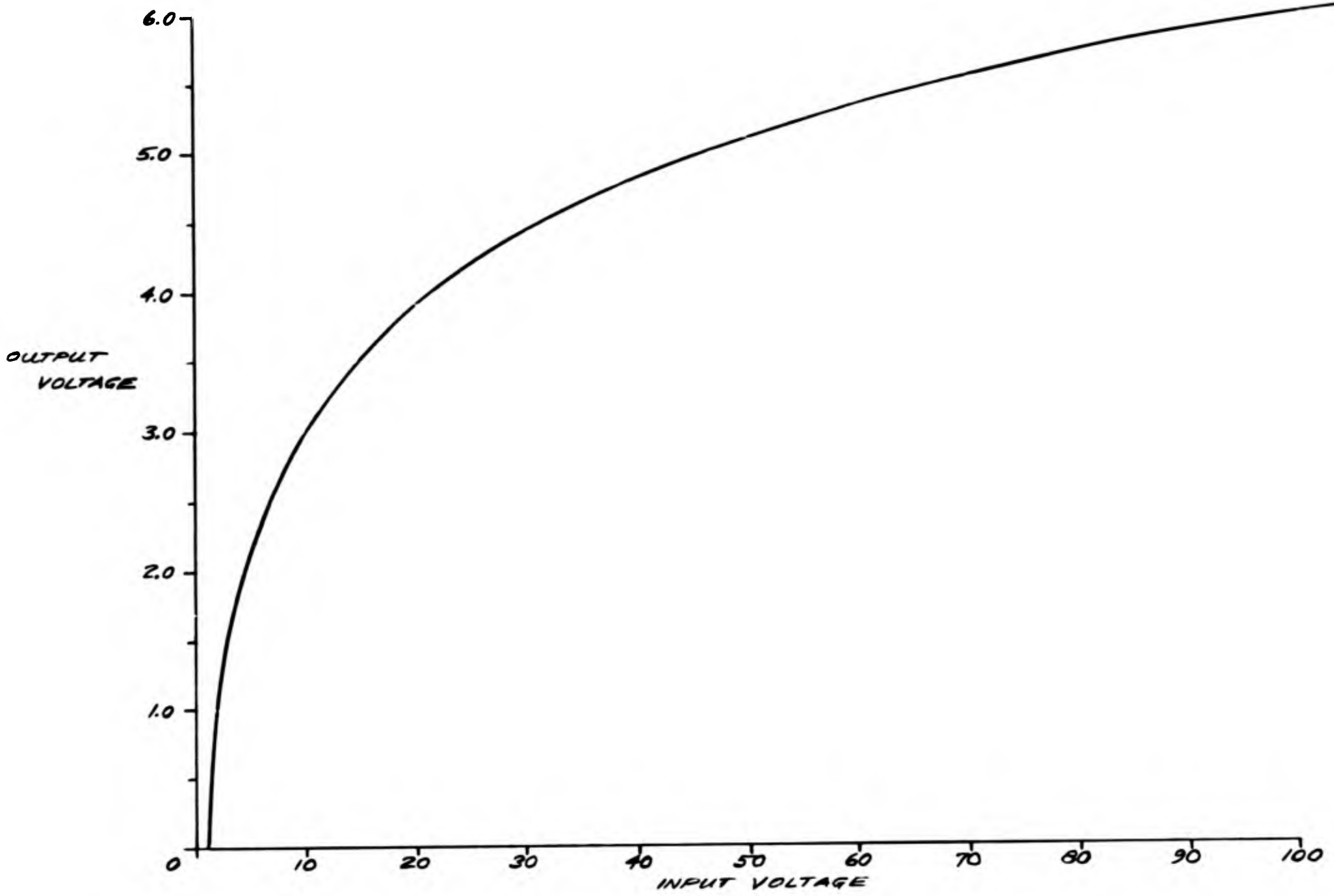


FIG. 1.7.2: AMPLITUDE RESPONSE OF LOGARITHMIC CONVERTER

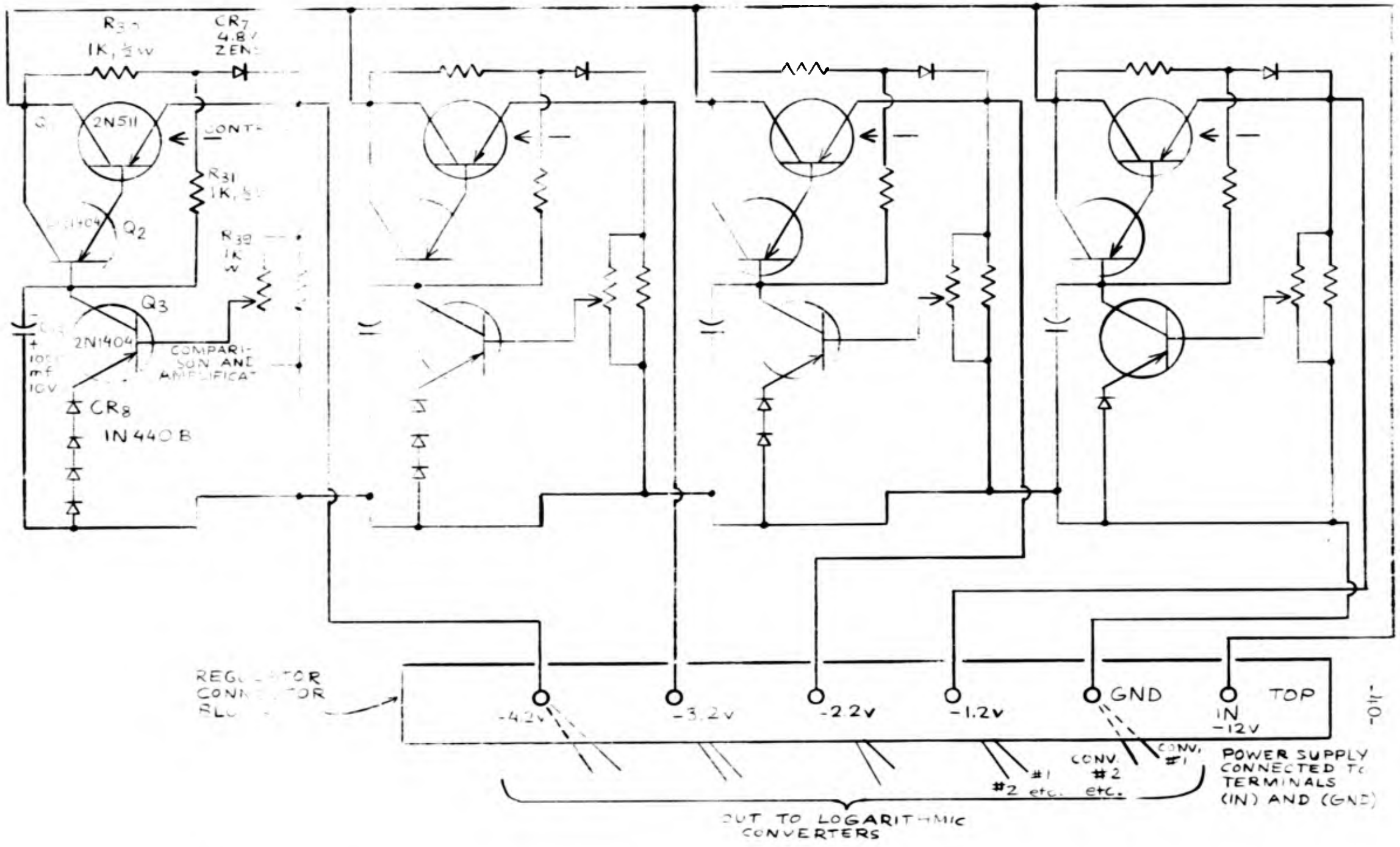


FIG. 1.7.3: LOGARITHMIC CONVERTER VOLTAGE REGULATOR

1.8 Plugboard No. 1

Plugboard No. 1 links the outputs of the logarithmic converters to the inputs of the differential amplifiers. Different arrangements on the plugboard correspond to the extraction of different "local" and "global" properties of the frequency-amplitude profile. In general, comparison of the outputs of narrow band filters will yield information about the local features, while the broad-band filters and the amplitude monitoring channels will project tonal quality, inflexion pattern, and other global features.

Although the output of each frequency channel is available on eight hubs, no more than four differential amplifiers should be connected to a single one of these channels. The input impedance of the differential amplifier (section 4.5) is of the order of 150 Kohms, and to avoid distortion, the parallel combination of these input impedances should remain small compared to the 15K output impedance of the logarithmic converters.

The logarithmic converters associated with the two amplitude channels have a lower output impedance, and these may be loaded by up to ten differential amplifiers.

The upper row of hubs on the red section of the panel represents the "A" inputs of the differential amplifiers, and the lower row represents the "B" inputs.

1.9 Differential Amplifier

Dwg. No. 4.3 Differential Amplifier and Sensory Threshold
10.1 Differential Amplifier (Printed Cct. Layout)

The differential amplifier amplifying the algebraic difference between the outputs of two logarithmic converters, the A_1- unit threshold settings, and the gates channelling trigger pulses to the delay chains, are all combined on one card. The circuit is displayed in fig. 1.9.1.

In order to minimize loading on the log units (section 1.7), the input is accepted on either side through a 50 K resistor feeding two transistor cascaded direct current emitter followers. The difference amplitude, available between the two emitters, provides the emitter-base bias of two gate transistors used in the ungrounded common base configuration. * The gate transistors are capacitor coupled through the collector to the Trigger Generator (section 1.11), and through the emitter to the base of the output transistors.

The gates are operated under class A conditions, so that the 1000 cps square wave current through them is proportional to the bias, and hence to the voltage difference between the A input and the B input. Note that one of these transistors is always cut off, depending on whether A is bigger than B, or B bigger than A.

The output transistors are operated in the Class C mode, so that either there is a square wave output big enough to trigger the first multivibrator in the delay chain, or there is no output. The threshold at which each output transistor will fire is independently adjustable on a front panel potentiometer. Thus a certain threshold may be set at which A-B will fire a delay chain, and a different threshold at which B-A will fire another delay chain. The thresholds may be varied to correspond to a filter output amplitude difference of 20% to infinity. The collectors of the output transistors are available on plugboard number 1 (section 1.8).

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* This unusual transistor configuration is necessitated by the fact that the output of the double ended difference amplifier is not referenced to ground.

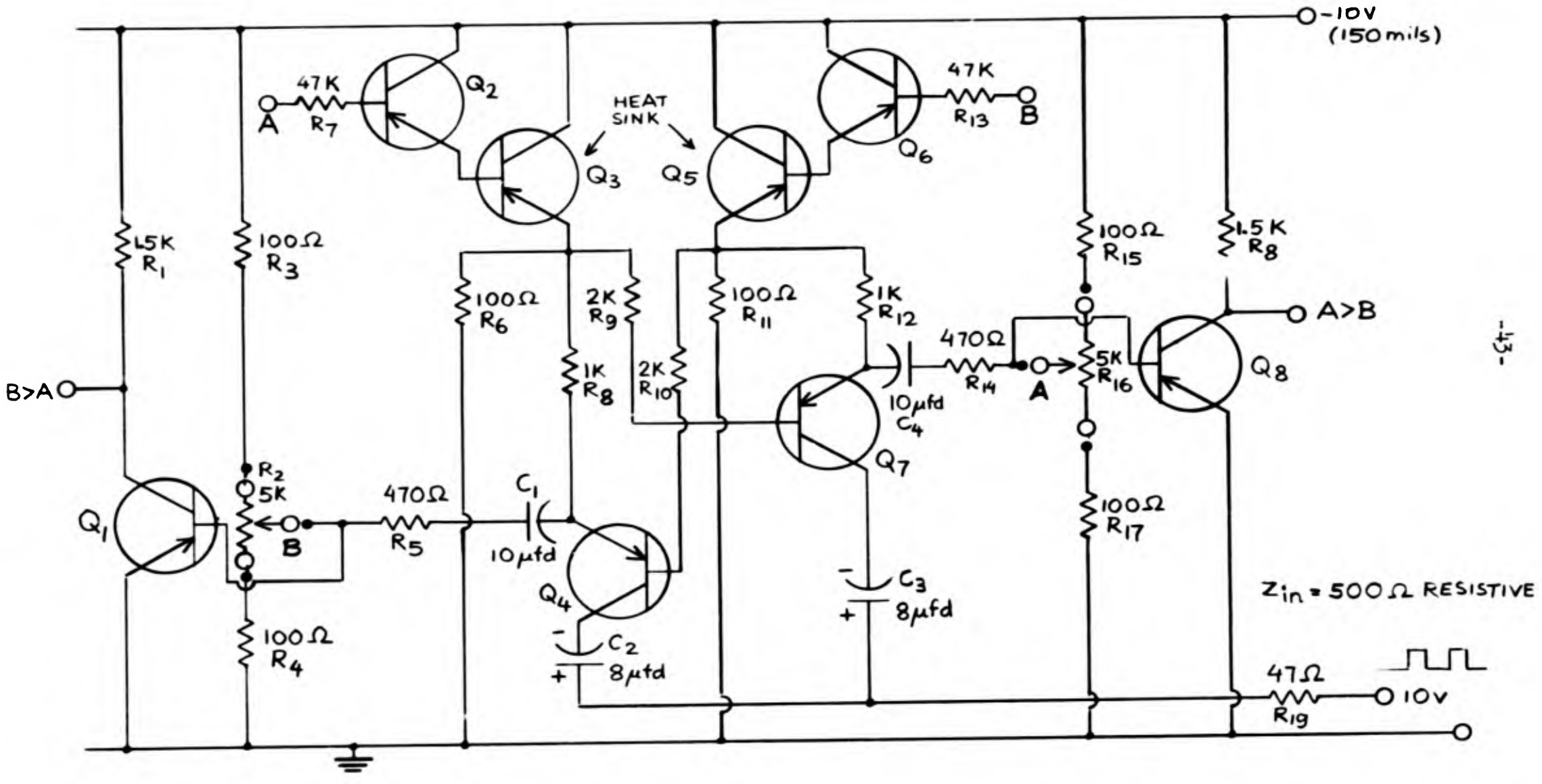


FIG. 1.9.1: DIFFERENTIAL AMPLIFIER

1.10 Sensory Delays

Dwg. No. 4.4 Delay Multivibrators and Drivers
10.2 Multivibrator Driver Connections (Printed Cct. Layout)
4.8 Delay Wiring Diagram - Rack No. 3

The delay system contains eighty chains of twenty multivibrators each. Each multivibrator consists of a three transistor 'single shot' and a driver (fig. 1.10.1). Whenever the threshold of the differential amplifier (section 1.9) to which a particular delay chain is connected is exceeded, the first 'monoflop' is triggered by the falling edge of the first of the 1000 pps pulses which is passed through the gate. Thus firing is guaranteed within no more than 1 msec. of the time the threshold is exceeded.

The single shots may be set by means of front panel potentiometers to yield delays of about 8 msec to 150 msec each. The recovery time varies between 1 msec and 3 msec depending on the delay settings. The outputs of the drivers (+10V in the quiescent state, -10V in the triggered state) are available at Plugboard No. 2. In addition, the last multivibrator in each chain triggers a lamp driver in the control booth (section 4.5).

Transistors Q_1 and Q_2 in the delay multivibrator are normally off, transistor Q_3 is normally on. Q_2 is just an emitter follower; it is needed to lower the output impedance of Q_1, for faster recovery time, and to decrease the fall time of the output (this falling edge triggers the next delay in the chain). The delay is approximately equal to $0.7\,(R_7 + R_8)\cdot C_3$. In order that the activity of the delays in a chain may be truly representative of the time dependence of the input, it is necessary to set the delay of the first single shot a little longer than that of the others in the chain. To this end, the first single shot is provided with a 10 fd instead of an 8 fd capacitor.

The delay multivibrators are very sensitive to noise spikes in the power buses, especially in the -20V. line. In order to avoid parasitic triggering, two 500 fd capacitors are hung on each delay board, about half way through the chain.

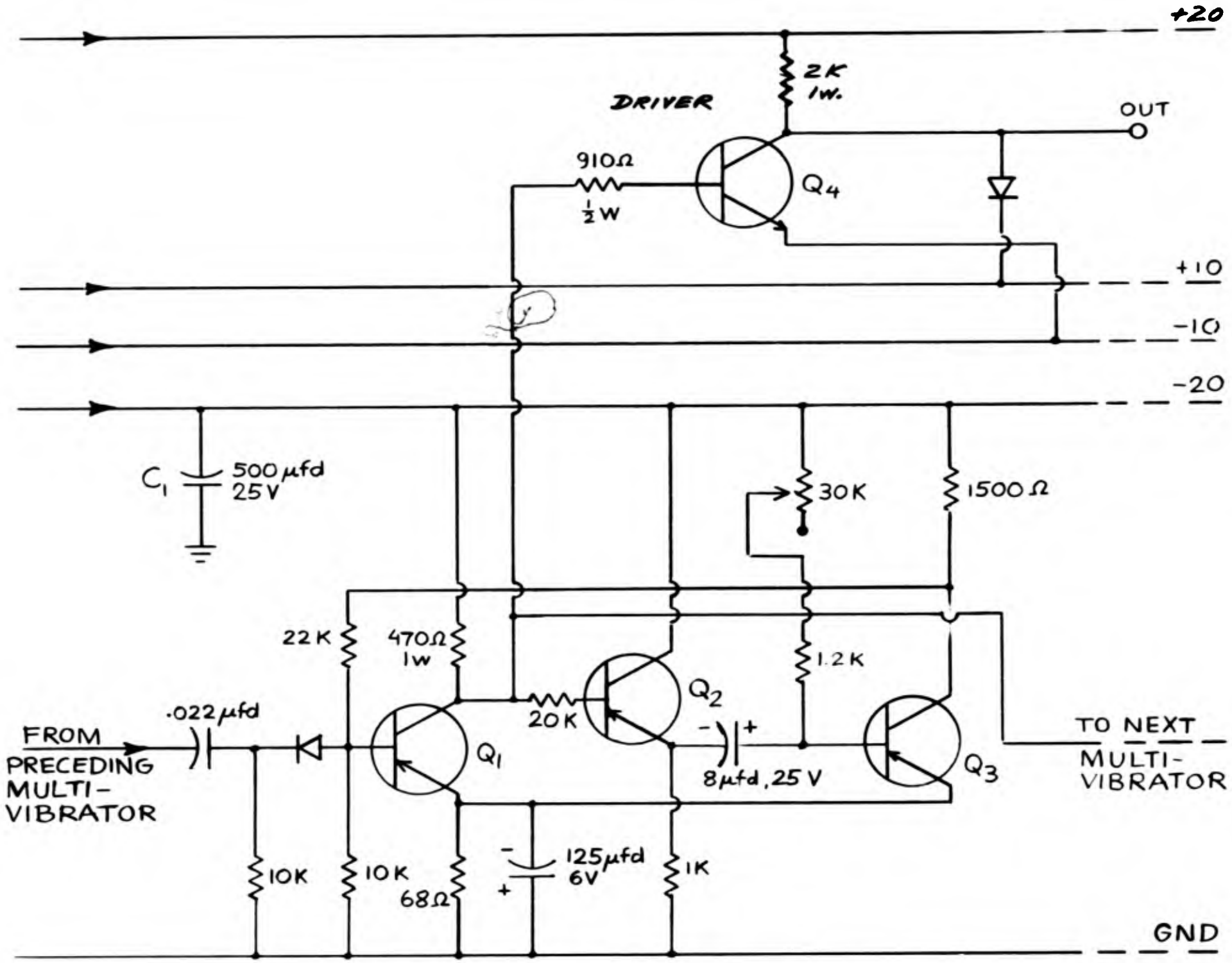


FIG. 1.10.1: SENSORY DELAY CIRCUIT DIAGRAM

1.11 Trigger Generator

Dwg. No. 8.3 Trigger Generator

The trigger generator (fig. 1.11.1) provides the sensory delay chains (section 4.6) with negative trigger pulses through the differential amplifiers (section 4.5). Thus the output of the trigger generator is fed simultaneously to all the differential amplifiers, but trigger pulses will be allowed through only to selected multivibrator channels, depending on the direct current input to the differential amplifiers.

The trigger generator, which shares a chassis with the reinforcement pulse generator (section 3.7), consists of six transistors, numbered Q1 through Q6. Q1 and Q2 form a 1 Kcs free running multivibrator feeding into emitter follower Q3 and saturated amplifier Q4. Q4 drives emitter follower Q5, whose output amplitude may be varied by R14. Q5, in turn, drives emitter follower power output Q6, which is capable of delivering 1.5 A p.t.p. square wave into a 10 ohm load continuously.

The amplitude adjustment should be set in such a way that, with all the differential pulse gates connected, if the inputs to a test amplifier are balanced, and both thresholds are set to the minimum value, both outputs should be just on the point of triggering the connected multivibrator chains.

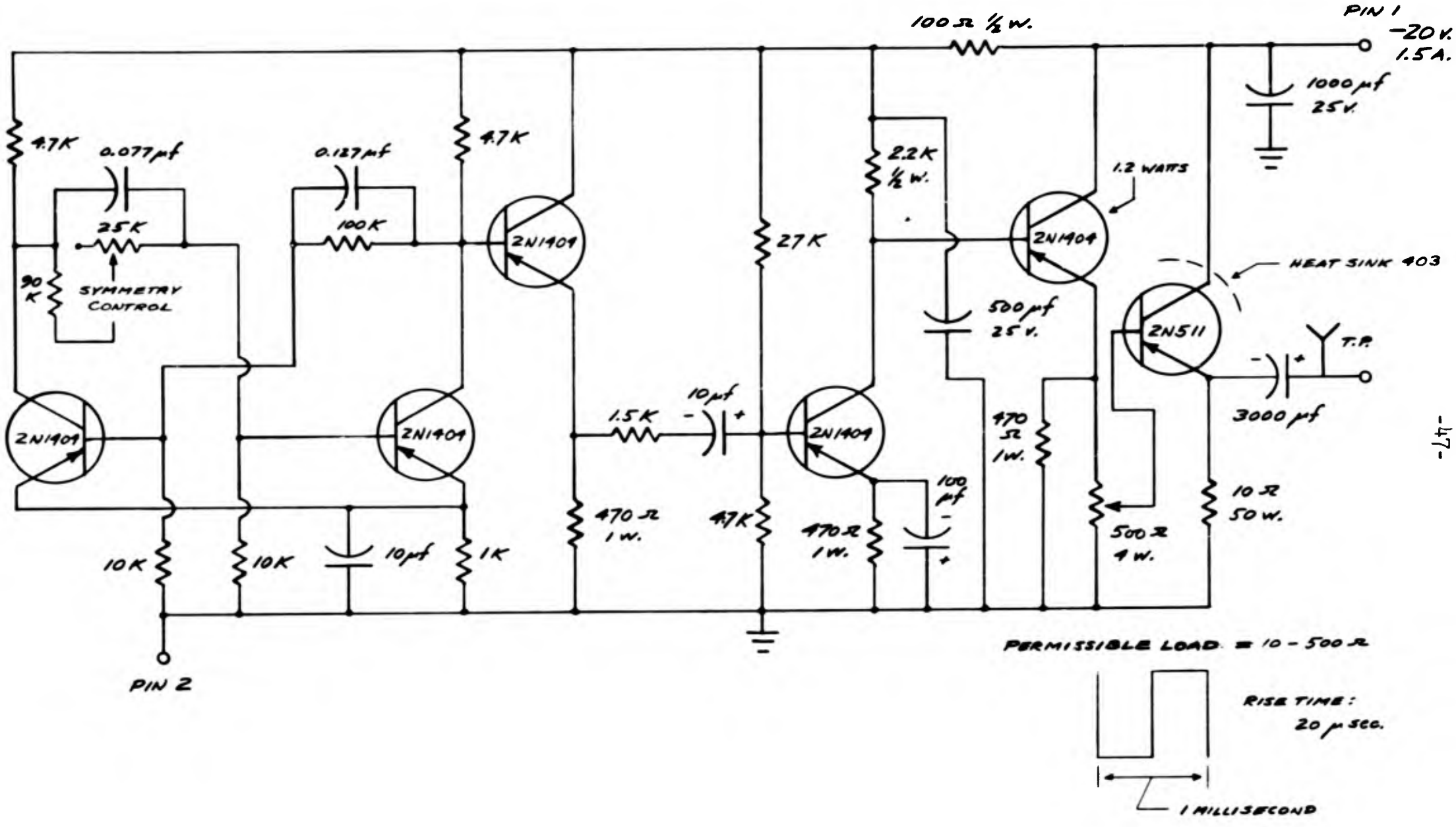


FIG. 1.11.1 : TRIGGER GENERATOR (1 K.C.)

CHAPTER 2 - THE ADAPTIVE SYSTEM

2.0 Introduction

The input to each $A^{(2)}$ unit (referred to henceforward as the A-unit) may consist of up to twenty delay multivibrator signals. Plugboard no. 1 permits the arbitrary assignment of positive or negative signs to these signals.

The A-unit itself comprises a differential amplifier, an adjustable threshold, a variable pulse stretcher, and a carrier gate (see below). The role of the pulse stretcher is to smooth the sum of input signals to the R-units. The A-unit outputs are accumulated by an activity indicator, which displays the level of A-unit activity throughout a word on the CRT in the control room.

The memory consists of 12,000 tape wound cores, arranged in a 12 by 1000 matrix, as shown in figure 2.0.1. When the threshold of an A-unit is exceeded by the algebraic sum of the signals from the delay multivibrators to which it is connected, it opens a carrier gate, permitting a 100 Kc signal to pass through the drive winding of the twelve cores to which it is connected. The active cores generate a 200 Kc signal (second harmonic) proportional to the stored setting (remanent flux). The algebraic sum (phase reversal denotes sign reversal) of the signal generated in the sense winding (which corresponds to one column of the matrix) is extracted from the carrier fundamental at the R-unit, where it now determines the state of the output flip-flop. The sense winding also serves to increment and decrement the stored flux (by means of pulses), and for erasure.

The R-unit amplifier can be cut off by the response freezing signal from a word termination detector to prevent further changes in the state of the R-unit after an input message has been completed. Precautions are also taken to minimize the effect of noise by ensuring that the R-unit will change its state only if the change in the input is greater than a preset amount. Both the input and output of the R-unit may be monitored in the control room, and the latter is also printed by the automatic typewriter after each word.

FIG. 2.0.1: THE ADAPTIVE SYSTEM

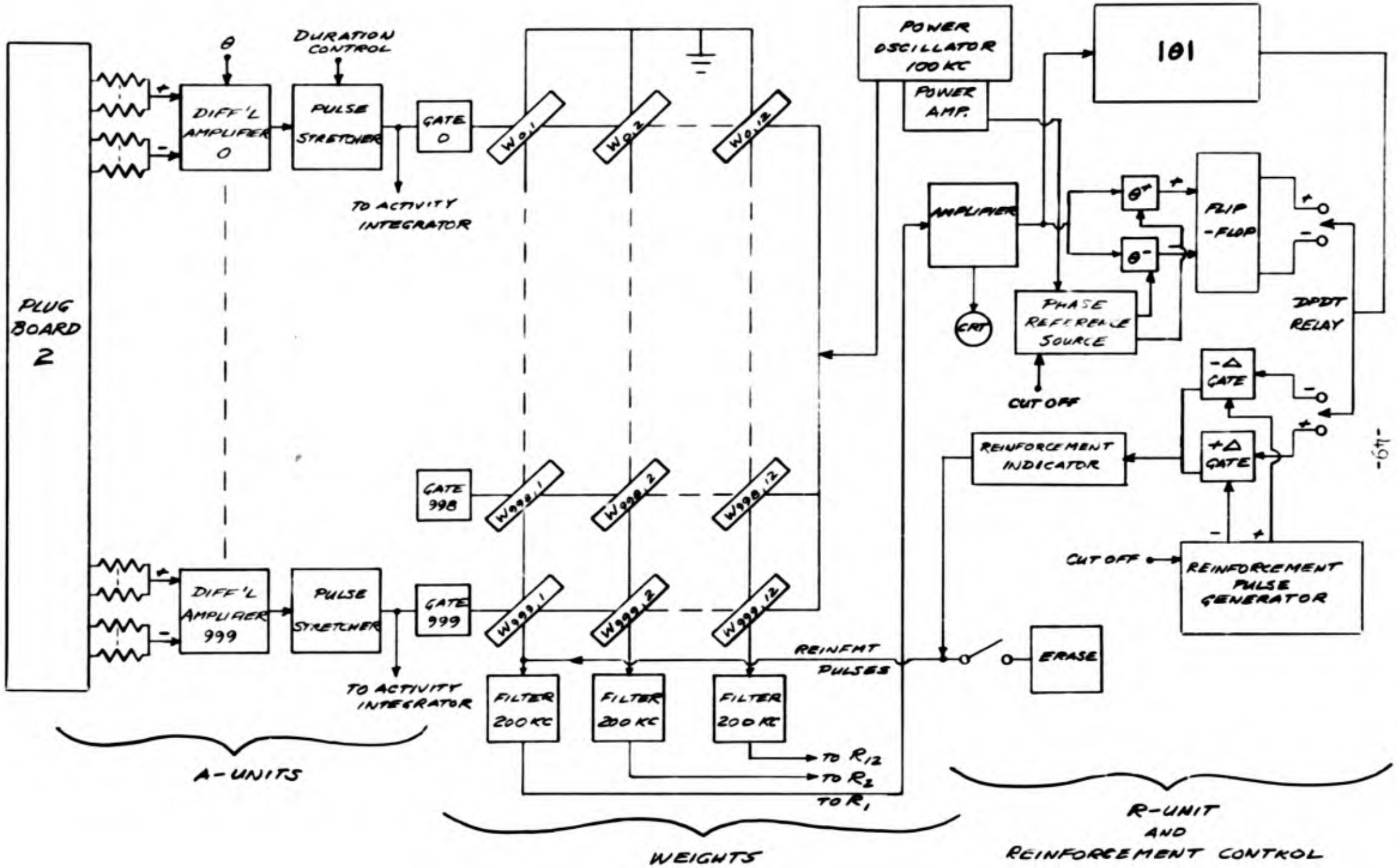


FIG. 2.0.1: THE ADAPTIVE SYSTEM

Reinforcement is generally performed by an error correction procedure, which requires that the desired response be available in the machine before a word is presented. Depending on the setting of the relay storing the desired response, a "wrong" R-unit will open a positive pulse gate or a negative pulse gate, channelling the appropriate write pulses to the cores associated with it. The reinforcement pulse generator, which provides the necessary write pulses, is turned on only during the period for which reinforcement is permitted, as scheduled by the word termination detector. This period will generally be set for a few milliseconds during which the entire word is "in register", and overlapping the instant at which the response state is frozen. Provision is also made (through the reinforcement overshoot control) to briefly continue reinforcement after the R-unit has reached the correct state, in order to stabilize the correct response.

In summary, the incrementing or decrementing of the flux level of a single core is determined by: 1) the activity state of the A-unit to which its drive winding is connected; 2) the algebraic sum of the inputs to the R-unit to which its sense-write winding is connected; 3) the absolute amplitude of the input to this same R-unit; and 4) the time elapsed since the word has fully entered the delay chains.

2.1 Plugboard No. 2

Dwg. No. 5.1 (S-P wiring diagram) Rack and Connector Layout
8.6.5 (P-A wiring diagram) Rack and Connector Layout

The main plugboard (P.B. no. 2 on Dwg. No. 1.2) is mounted on five racks bolted side by side. On the front of each rack there are six 1600 hub panels (black) and five 800 hub panels (black and yellow).

The 1600 hub panels are wired in parallel with each other and with a similar panel at the base of the rear of each rack. Parallel wiring here denotes that corresponding points are wired together. The rear panels are in turn wired in parallel with each other and with a 1600 hub (really two panels totalling 1600 hubs) clip-on terminal block set on the back of rack no. 4. Each of the 1600 terminal block points is connected to the output of one of the sensory delay drivers. Thus the thirty black panels on the plug board represent the same 1600 driver outputs repeated over and over.

The smaller panels represent excitatory (yellow) and inhibitory (black) inputs to the 1000 A-units. Each column of 10 hubs is either the excitatory or the inhibitory input to an A-unit. Isolating resistors (adding resistors in lab parlance) are mounted on the backs of the A-panels. About 1000 of the 20,000 resistors in the plugboard were tested; the resistances were found to average 19.4KΩ , with a standard deviation of 0.4KΩ. The connections to the A-unit racks are wired through multiple plugs and sockets (one set per panel) through overhead cables from the common terminals of the isolating resistor sets.

To establish an S-A connection, one simply selects a free hub in the appropriate black or yellow column, and runs a double male connector to the correct sensory point of the nearest S-panel. The parallel panel organization was devised after consideration of the possibility of extending the chain-wiring method of establishing connections (used in Mark I) to a 1600 x 2000 matrix with up to twenty connections per A-unit and thirty per S-unit. It is expected that the normal connection density will be only a fraction of the permissible density.

Since there are 48,000 S-point terminations, the probability of wiring errors in the construction of the plug-board is by no means megligible. It is

therefore necessary to test each hub for proper connection to its S-line, i.e. to check whether the corresponding thirty points, and only the corresponding thirty points are connected together.

In general, the most time consuming portion of the testing procedure is the continuity check. An arbitrary panel is chosen, and a continuity check is performed between each hub on that panel, and the corresponding hubs on every other panel. The size of the plug board justified the construction of equipment designed to test several connections simultaneously. A schematic diagram of the S-unit continuity tester is shown on figure 2.1.1.

When the moving contacts of the stepping relay (wiper contacts) "find" a continuous circuit, i.e. there is continuity between the pair of hubs under test, the relay coil is actuated and the wiper moves to the next contact pair. When the relay encounters an open circuit, its coil is not supplied with power and thus it cannot advance beyond the open circuit without depression of the manual "override" button. An auxiliary set of relay contacts lights a set of numbered pilot lamps to indicate the position of the wiper contacts and localize possible wiring errors.

Connections are tested for continuity in groups of twenty-five. The procedure is as follows. Insert the multi-pin plugs into corresponding blocks of hubs and press the white push button on either plug. The button is only effective in starting a test, it will have no effect at any other time. The stepping switch now proceeds to test each pair of terminals, advancing until it either finds an open circuit or reaches the last circuit to be tested. In the latter case, a tone is heard signaling the end of the test (an audio oscillator and a speaker are connected through the last circuit). The operator will undoubtedly encounter some difficulty in inserting the multi-pin plug. An open circuit indication is, in fact, most often caused by poor contact at the plug, which in no way reflects on the panel wiring. Working the plug up and down usually completes the circuit; if the panel wiring is truly faulty, nothing short of the manual override, effected through the "single step" switch on top of the chassis, will continue the test. The single step switch should be used only to skip over a connection which has been recorded as faulty. The "full reset" switch connects the pulse circuit to the stepper, and advances the

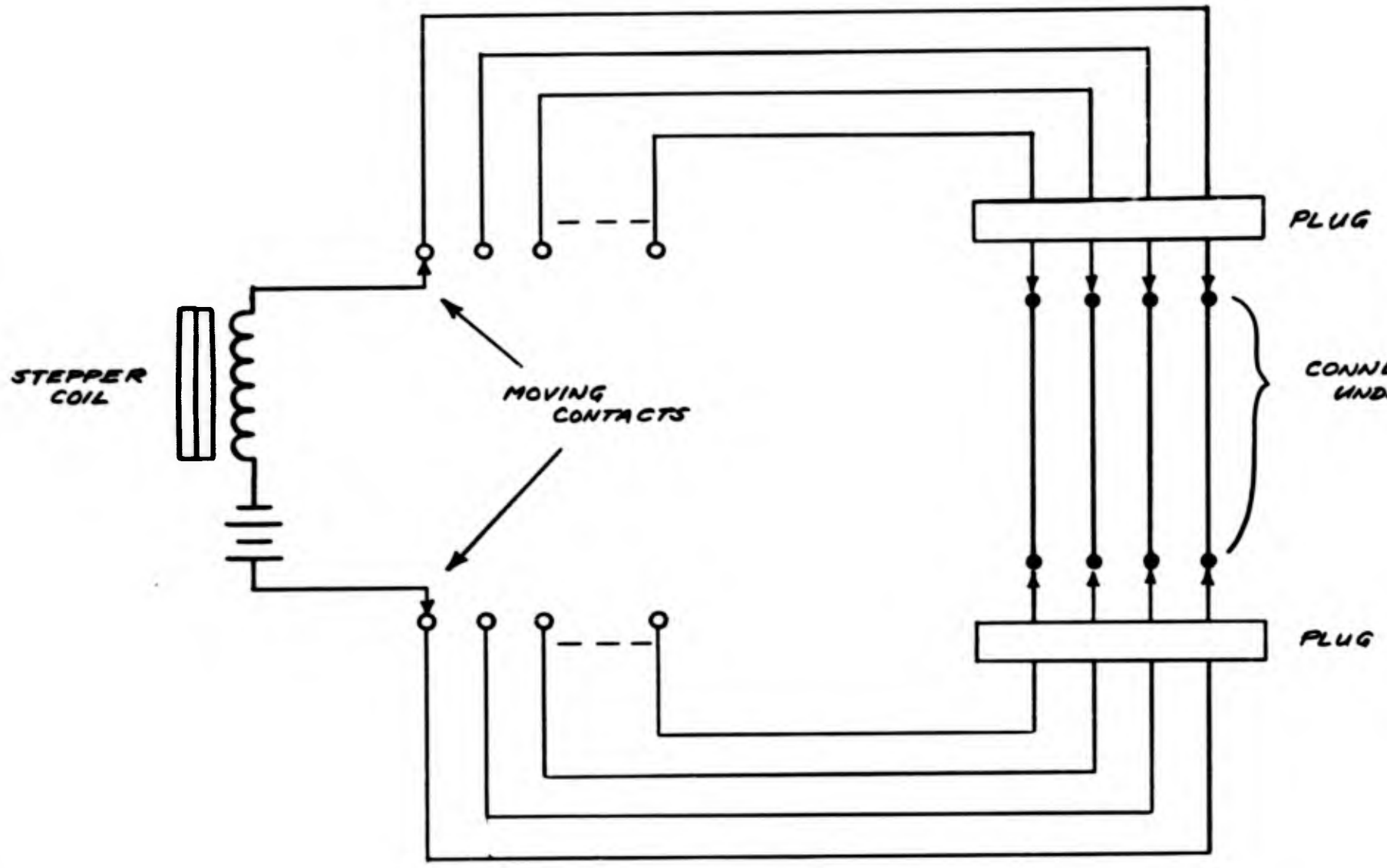


FIG. 2.1.1: SCHEMATIC DIAGRAM OF S-UNIT CONTINUITY TESTER

contacts to the last position, ready for a new start.

The circuit diagram of the continuity tester is shown in detail on figure 2.1.2. Note that since the stepper has only twenty positions, five pairs of circuits must be tested simultaneously (i.e., in series). The probability that a wiring error will be overlooked by this scheme is slight, since the five pairs so tested are not adjacent to one another.

Caution should be exercised in connecting the 22 1/2 V. and the 6 V. batteries with the correct polarities.

The resistor-diode combination in parallel with the relay coil prevents inductive spikes from destroying the transistor. The frequency of stepping is determined by the resistor; the higher the resistance, the quicker the action.

To test the S-panels for shorts, all 1600 S-points are shorted through standard front panel patch cords. To test any S-line, the appropriate patch cord is removed, and the S-line is tested for a short to ground; this test will of course also reveal a short to any of the other S-lines. If the line is found to be shorted, the patch cord is reconnected, so that one of the subsequent tests may reveal to which S-line it is shorted. If the line is "clear", it is not re-grounded, and plays no further role in the testing procedure, which continues until all patchcords have been removed.

A piece of equipment was also constructed to check the A-board to plug board connections. Its principal element is a set of eighty leaf-spring single pole single throw switches which may be operated in the single throw double pole mode by pressing a conducting probe against the spring leaf to hold it away from one one of the contacts.

The eighty switch blades are connected, for testing purposes, to all eighty conductors of an A-cable through a plug matching the terminal blocks in the A-unit cabinets. The moveable end of each switch leaf normally rests against a ground bus. The tester itself consists of an audio oscillator (and amplifier) and a speaker connected in series between two probes. One of the probes is clipped on the plugboard end of the wire being tested, while the other probe is inserted into the appropriate hole in the switch board. If the wire is open, no

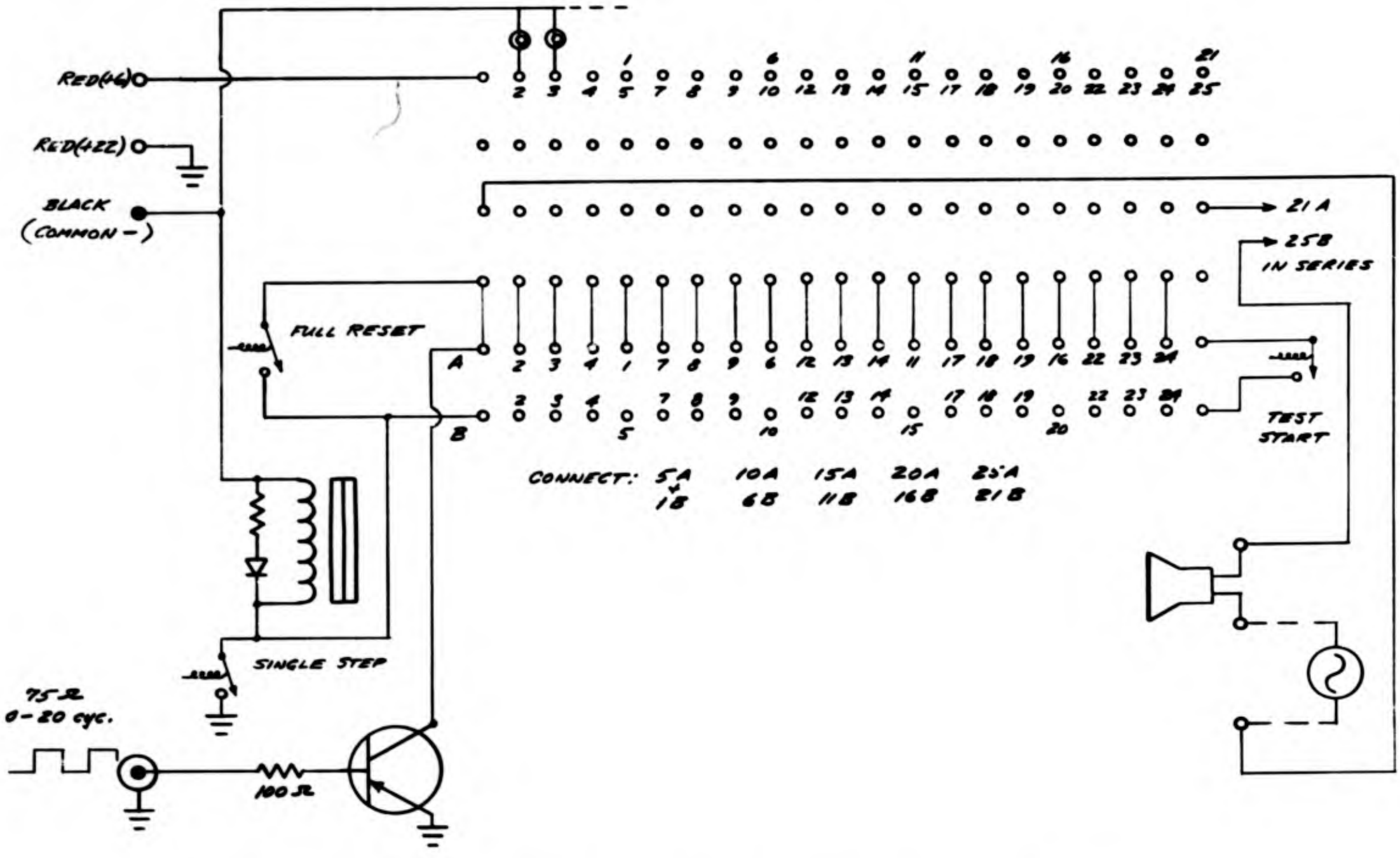


FIG. Z.1.2: CIRCUIT DIAGRAM OF S-UNIT CONTINUITY TESTER

sound will be heard because the connection is not completed, while if the wire is shorted to ground (either directly, or through one of the other wires) then no sound will be heard because the oscillator is shorted out. If the connections to the resistors need also be tested, then the first probe should be inserted into each of the A-unit hubs on the front panel instead of being clipped to the common point of the isolating resistors. A schematic diagram of the test jig is shown on figure 2.1.3.

The construction of the plugboard, with the attendant wiring, is easily the most expensive single item in the machine. The reader who is offended by the high price, lack of reliability, extensive set-up time, and general clumsiness of the arrangement is invited to contribute ideas towards superior implementations of fixed connections.

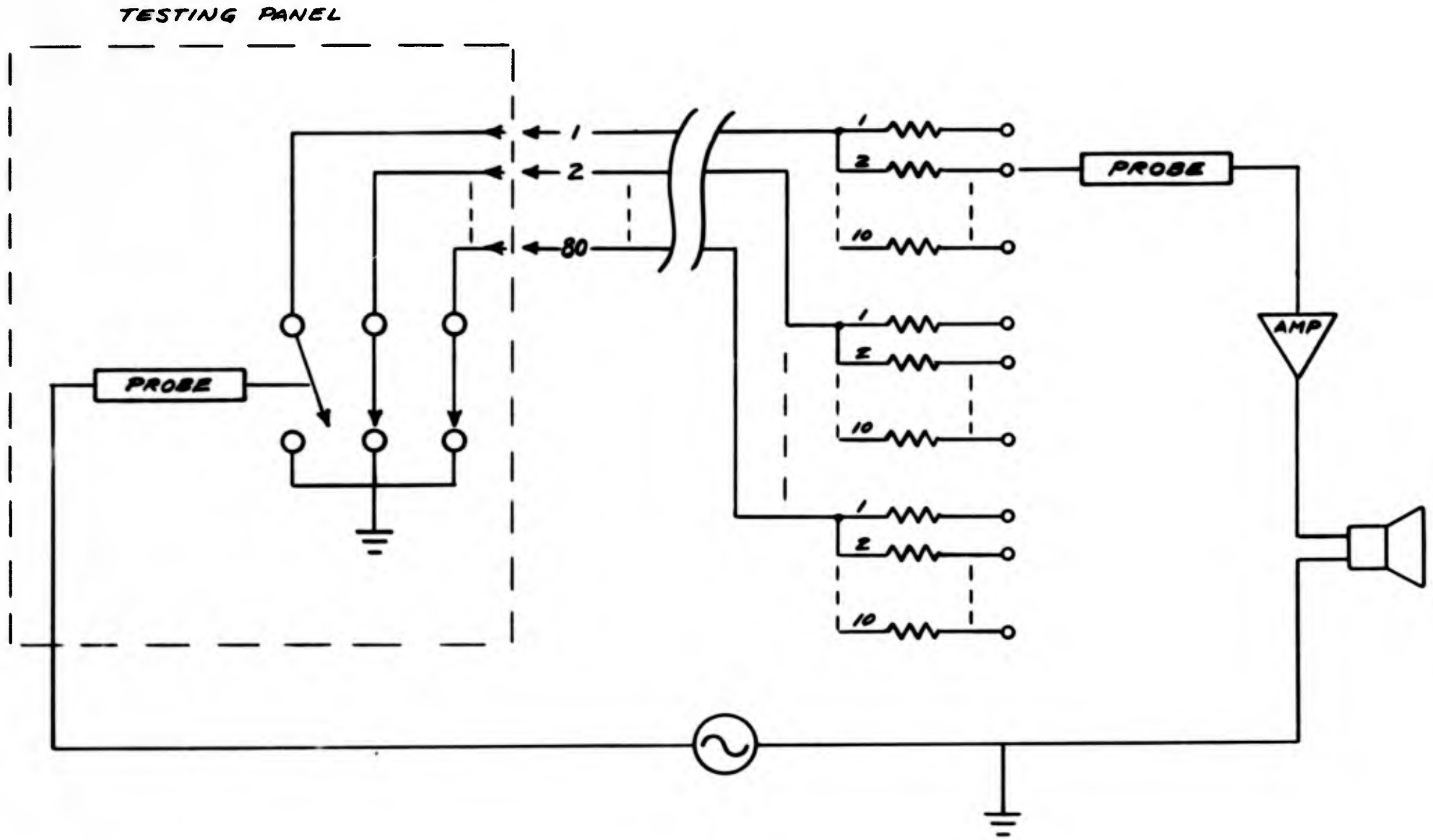


FIG. 2.1.3: SCHEMATIC DIAGRAM OF A-UNIT CONTINUITY TESTER

2.2 The A-unit

Dwg. No. 6.1.1 A-unit and Gate

The inputs to the A-unit consist of the +10V to -10V pulse outputs of the sensory delay drivers (section 1.10) which are conveniently available on plugboard no. 2. The 20 KΩ resistors imbedded in this plugboard are part of the summing network: they permit the algebraic addition of up to twenty identical signals, some of which are arbitrarily considered positive, and some negative.

The purpose of the circuit is to turn on a carrier gate when the number of excitatory inputs (signals assigned positive sign) exceeds the number of inhibitory signals (signals assigned negative sign) by a preset threshold, and to keep the gate turned on for an additional, manually set interval beyond the period during which the threshold is exceeded.

Ten A-units are mounted on each printed circuit card. The thresholds are individually adjustable from about 1/2 to 10 by means of edge mounted potentiometers, and the stretch times may be varied from 5 msec to 125 msec in the same manner. The front row of pots controls the thresholds, and the back row, the stretch times.

The A-unit operates as follows. Q1 and Q2 (figure 2.2.1) constitute the actual decision circuit. While the configuration resembles that of a difference amplifier, Q1 really operates as an emitter follower whose output determines at what base voltage Q2 will switch. Inhibitory inputs tend to drive the emitter of Q1, and therefore that of Q2, negative, resulting in Q2 being cut off unless the excitatory inputs generate a corresponding negative voltage at the base of Q2. The threshold pot, linking the base of Q1 to a negative supply, is equivalent to a variable amplitude negative input. Note that for maximum accuracy, the current summing resistors R_2 and R_7 must be matched to within 1%.

Due to the 5% tolerance on the isolation resistors (the cost of 20,000 precision resistors would have been prohibitive), switching at precisely the correct number of excess excitatory inputs cannot be guaranteed when the number of competing excitatory and inhibitory signals (including the threshold) exceeds about 10. This is not, however, likely to be detrimental to the operation of

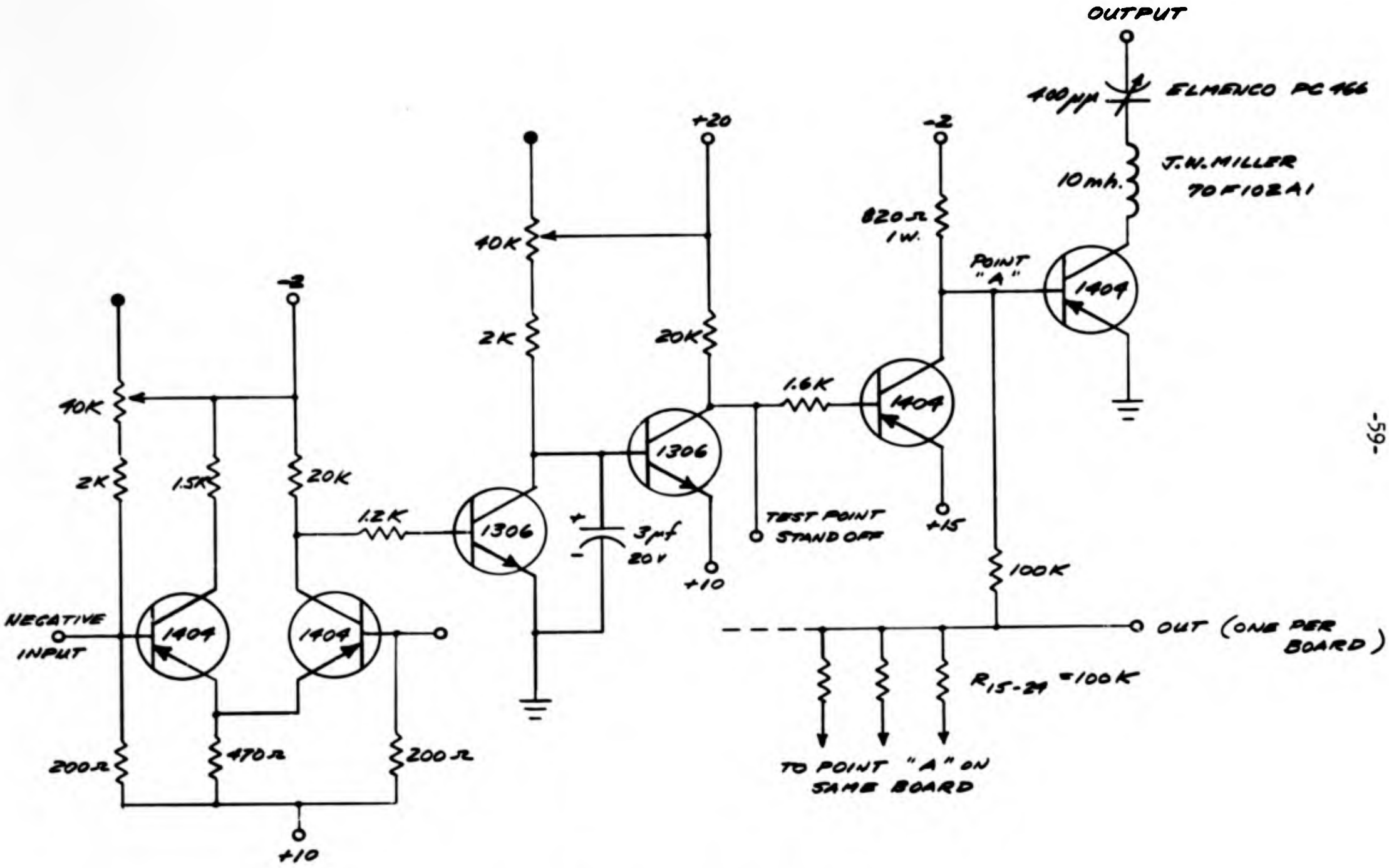


FIG. 2.2.1: THE A-UNIT

the machine, since the R-units are sensitive only to root mean square fluctuations.

Q3 serves mainly as a buffer for Q2, which cannot be heavily loaded without affecting the clean switching action. Q4 turns off when Q2 and Q3 turn on, but time constant circuit R_9C_1 prevents it from turning on again until some time after Q2 and Q3 have turned off.

Q5 is a power amplifier for gate Q6. In order to ensure that Q6 will operate as a bidirectional gate, passing both halves of a sine wave current, it must be generously overdriven; hence the need for a separate driver. The cost of the extra 2N1404 is still considerably lower than that of a genuine bidirectional transistor. Q6 operates at a gain of about 2.5, in both forward and reverse directions.

The variable air gap capacitors must be tuned before the A-unit board is inserted into its frame. Grounding the excitatory input, with the threshold pot set for a minimum, suffices to turn the A-unit on. For tuning, proceed as follows. Connect the 100 Kc/s carrier at 20 or 25 p-t-p amplitude, and 10 "typical" 12 core assemblies, to the appropriate pins. Monitor the current with a current probe at the wires connecting the A-boards and the core boards. Then adjust each capacitor in turn until the current is a maximum in all ten wires. These adjustments are independent.

The core assemblies are sufficiently alike so that each A-unit does not have to be tuned with its own set of cores. The inductance of the 12 core assemblies is roughly the same as that of the filter inductor. Careful tuning is necessary both to prevent second harmonic current from circulating in the drive windings of the cores, and to ensure that all of the drive currents are in phase with one another. Note that in tuning allowance should be made for the effect of the release of pressure when the tuning tool is removed.

A separate test point is provided for each A-unit (at the collector of Q4) in order to monitor the pulse stretching while adjusting R_9. The easiest way to adjust both threshold and stretch time is to feed in at an unoccupied excitatory hub of plugboard no. 2 a repetitive signal of amplitude corresponding to the aggregate of the minimum number of signals which should turn the A-unit on, and then adjusting the pots until a signal sufficiently longer than the triggering signal may be observed at the test point with an oscilloscope.

The sensory delays should of course be quiescent during this adjustment. The A-unit input simulator (section 2.7) may also be used to advantage here.

The collector of Q5 provides the signal for the A-unit activity indicator described in section 2.3.

The finer points taken into consideration in the design of the A-unit circuitry are treated in some detail in a report by Charles Kiessling.

2.3 A-unit Activity Indicator

Dwg. No. 8.8 A-unit Activity Indicator
6.1.1 A-unit

The A-unit activity indicator (fig. 2.3.1) serves to monitor the number of 'on' A-units by means of an oscilloscope display. The range switch in the control booth selects one of three ranges (1%, 10%, and 100%), depending on the maximum percentage of A units expected to be active. There is also a Calibrate position, which gives a zero reference. The full scale output to the oscilloscope is 1 Volt on all ranges. Note that the inverted (B) input on the 'scope should be used for positive deflection.

The integration time constant switch in the control booth selects the capacitors paralleled with the current sampling resistors. Time constants of 0 msec (no integration), 25 msec, 50 msec, 100 msec, and 200 msec are available.

The accuracy of the current summing network is within 4% at full scale, and proportionally better for smaller deflections. There is no sudden loss of accuracy above full scale: if, for example, a 2 volt output is measured on the 10% range, this means that twenty percent of the total number of A-units (i.e. 200) are on, with a maximum possible error of 16 units. The indicator will always err on the low side. The time constant capacitors are 20% components.

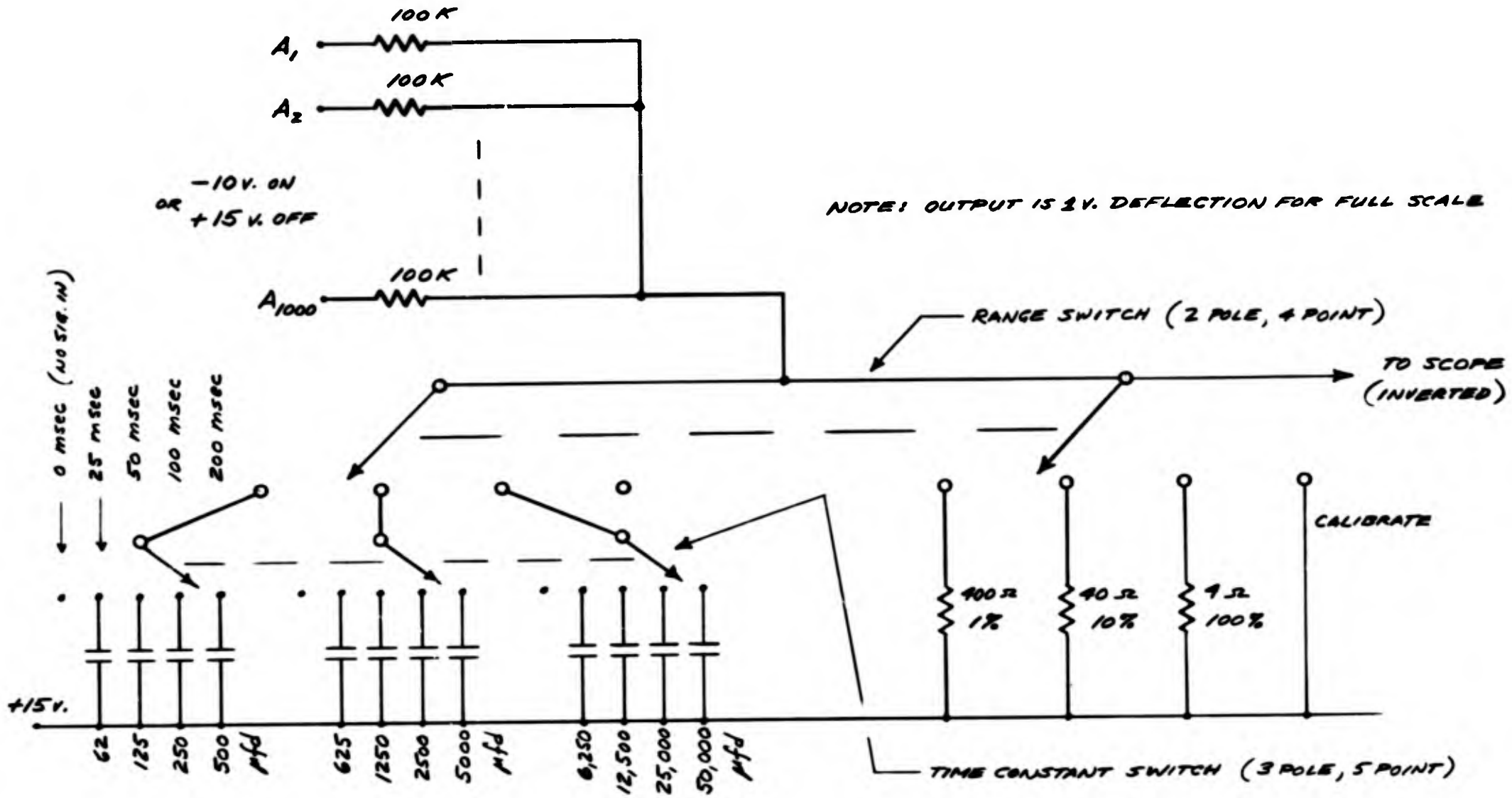


FIG. 2.3.1: A-UNIT ACTIVITY INDICATOR

2.4 Weight Cores

Dwg. No. 6.2 Tobermory Memory Matrix
6.3 Memory Matrix Wiring Diagram
6.4 Rack and Connector Layout for A-unit Cabinets

The magnetic integrator used in Tobermory's memory matrix is derived from the second harmonic weight proposed by Harold Crafts. The original work is described in A Magnetic Variable Gain Component for Adaptive Networks by H.S. Crafts, Technical Report No. 1851-2, Solid State Electronics Laboratory, Stanford Electronics Laboratories, Stanford University, Stanford, Cal., December 1962.

The function of the integrator is simply to furnish an indication of the algebraic sum of the equal sized reinforcement increments it has received in a certain time interval. The two properties necessary to fulfill this function are a passive memory mechanism, and a non-destructive readout. In the present design, the memory feature is a consequence of remanent magnetism in square loop cores, while the basis of the non-destructive readout is the even harmonic distortion introduced by an iron core transformer when the core is approaching saturation.

A detailed analysis of the harmonic generating process cannot be undertaken without a thorough understanding of the energy levels involved in the various kinds of elemental switching processes (domain rotation, wall movement, and wall building). Further complications are introduced by the presence of eddy currents in the high conductivity alloy tape cores, and by non-homogeneous boundary conditions.

Very roughly, what happens is as follows. When the majority of the domains in the core are already lined up in one direction, further magnetomotive force in the same direction will not be as effective in inducing domain movement, hence flux change, as magnetomotive force in the opposite direction. With a sinusoidal current drive, this means that the counter e.m.f. (or the e.m.f. in another winding) induced by Lenz's law will have a considerable second harmonic component. The behavior of the core in terms of the hysteresis loop

is depicted in figure 2.4.1. Note that the domain movement in question is elastic domain movement; the sinusoidal drive must remain small enough so that no permanent change in the level of magnetization occurs.

The highest tolerable drive is a function both of the frequency and of the maximum remanent setting desired. The demagnetization due to eddy current damping offsets the effectiveness of the drive at high frequencies, while the remanent flux level is most easily changed when it is close to the saturation level. In practice, the core is set with the drive on, so that one does not have to worry about the second consideration.

The flux level is incremented and decremented with constant current pulses. The current switching threshold of a square loop core is a function of its coercive force Hc. When the pulse amplitude is below this level, no switching occurs, while when the threshold is exceeded, the amount of flux switched is proportional to the volt-second integral of the excess. If the switching pulse exceeds the threshold by an amount sufficient to render the tilt of the sides of the hysteresis loop negligible, approximately constant flux increments may be attained. The negative feedback provided by the eddy currents greatly improves the linearity of the incrementation.

One feature of particular interest in the second harmonic weight is the possibility of coincidence mode operation. In this mode, the reinforcement pulses are normally kept under threshold, so that when the pulses occur by themselves, no permanent flux switching occurs. The drive, while in itself also insufficient to cause any permanent flux change, "shakes up the domain" (lowers threshold) enough to allow the reinforcement pulses to effect a flux change, provided they occur while the drive is on.

The significant second harmonic component is separated from the carrier fundamental by means of a filter. Other systems use for each weight a pair of cores wound in such a way that the fundamental cancels out while the second harmonic components add. While this scheme greatly reduces the precautions necessary to prevent coupling between the cores and also simplifies the sensing circuitry, it adds 100% to the cost of the cores and the winding, and increases the drive power requirements by about 50%.

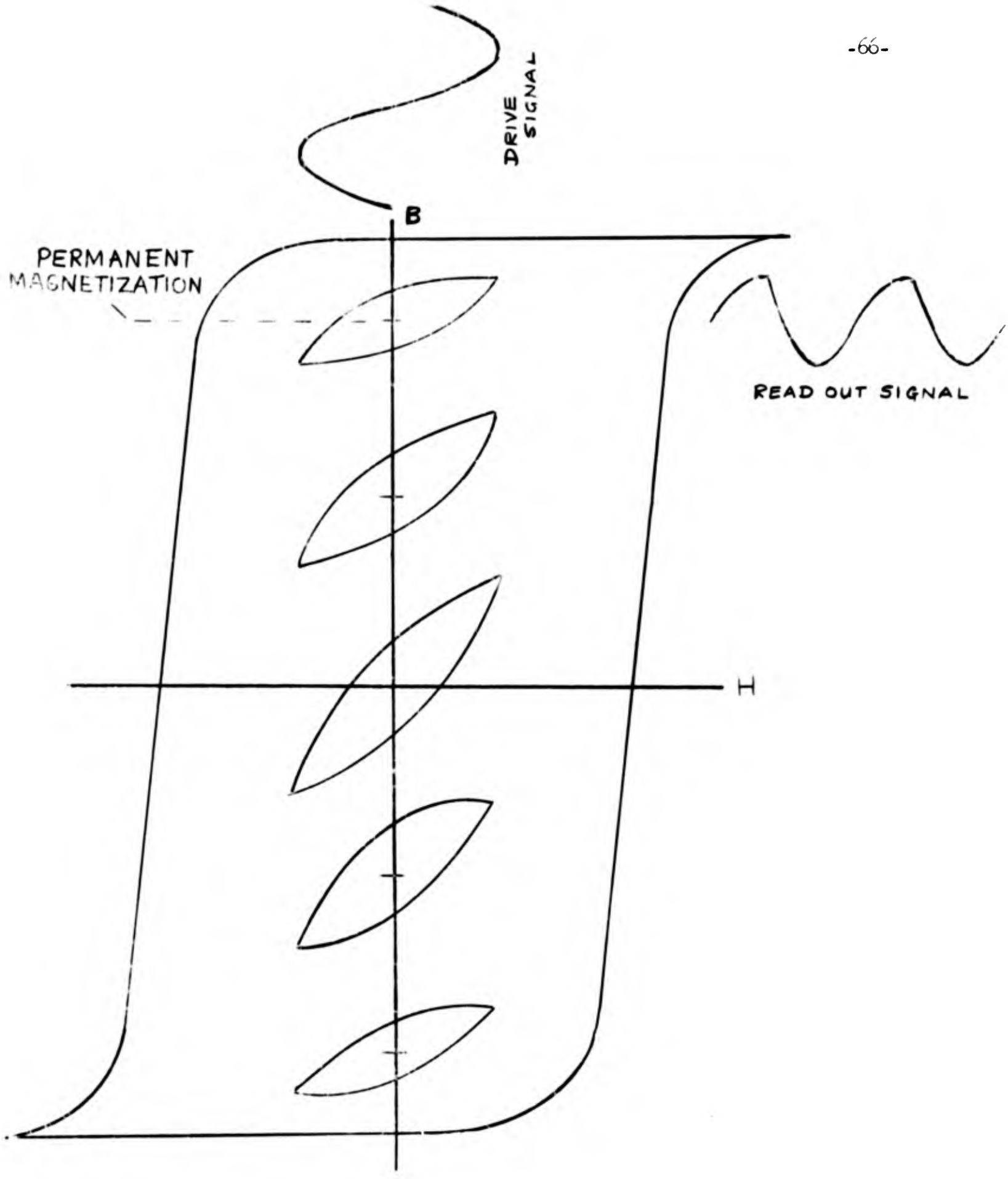


FIG. 2.4.1: HYSTERESIS LOOP IN INTEGRATOR CORE

The cores used in Tobermory are 200 maxwell, orthanol wrapped, .313" I.D. x 1/16" wide bobbins purchased from Magnetics Inc. of Butler, Pennsylvania. The manufacturer's part number is 02806231A00. Larger cores are advantageous for the linearity of integration (less variation in the length of the flux path); the core selected is a compromise between linearity and cost. One mil tape is suitable for 100 Kcs operation; for higher frequencies thinner tape should be used.

Each core card carries 50 groups of 12 cores. The drive (or carrier) winding consists of 30 turns of no. 24 magnet wire in series through the 12 cores belonging to a single A-unit. The sense, reinforcement, and erase signals share a single turn of no. 24 magnet wire in series through the thousand cores belonging to a single R-unit. The relation between the two windings is shown in fig. 2.4.2.

The ultra-low distortion (less than 0.1% second harmonic content) 100 Kcs generator described in section 2.5 is connected to the 'high' end of all 1000 carrier windings. The 'low' end leads to the A-unit switch (section 2.2) through a tuned circuit consisting of a 10 millihenry inductor in series with a variable 150-400 mmfd air capacitor. When the capacitor is tuned for maximum current (note that it is necessary to tune out the inductance of the carrier winding, as well as that of the 10 mhy. inductor), a carrier generator setting of 20 v. peak-to-peak forces a 48 ma. current to flow. Although the tuning must be done accurately in order to avoid misleading phase shift in the output, the carrier windings are sufficiently alike so that it is not necessary to match up the capacitors individually before tuning. If a higher output signal is desired, the carrier voltage may be increased up to 25 V. without degradation of the performance. This increases the signal level by better than 50%, since the second harmonic content in the output is approximately proportional to the square of the drive current.

The tuned circuit in the carrier winding prevents the circulation of second harmonic currents, thus eliminating interference between cores belonging to the same A-unit. It is also necessary to prevent current from circulating in the secondary (single turn) winding in order to preserve the summing action. This is accomplished by the relatively high (500 ohms) input impedance of the

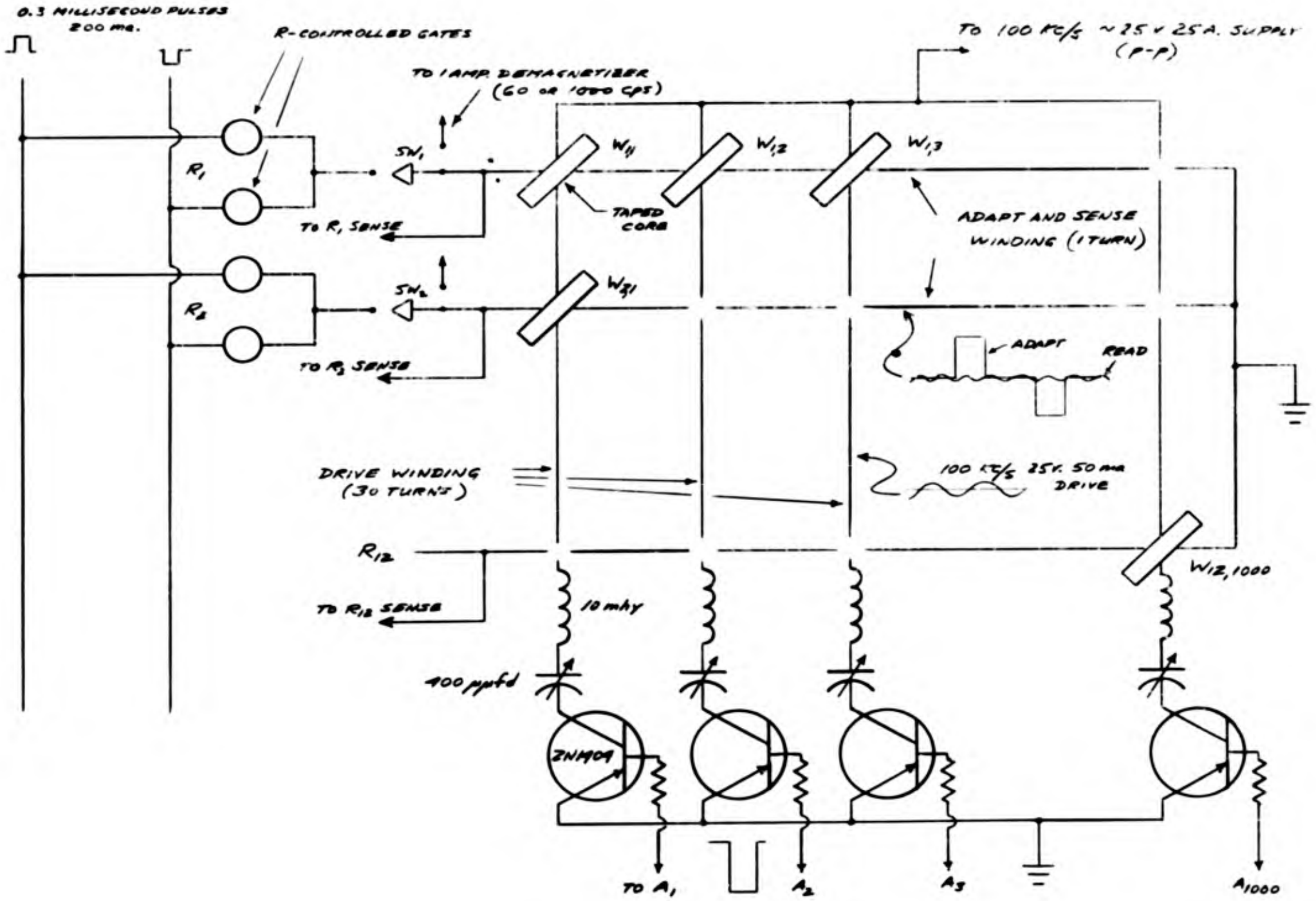


FIG. 2.4.2 : 2nd HARMONIC MEMORY MATRIX

filter (section 3.1) at both the fundamental and the second harmonic frequencies. The impedance of the secondary winding is of the order of 10 ohms at the frequency range of interest.

140 ma, 0.2 millisecond duration reinforcement pulses yield more than 100 steps at both 20 V. and 25 V. carrier settings. It is desirable to monitor the performance of a single core on the oscilloscope when adjusting the reinforcement current amplitude in order to ensure that incrementing and decrementing will proceed at the same speed. The R-unit controlled gates which provide the reinforcement pulses are described in section 3.6.

The carrier frequency output at 25 V. drive is 70 m v ptp., with about 10% second harmonic content when the core is saturated in either direction.

Erasure takes place when a low frequency current of smoothly decreasing amplitude flows through the single turn winding. A 100 cps current with an initial amplitude of 1.2 amperes leaves the cores with the remanent flux within 20% of zero. Section 2.6 describes the erase current generator. Erasure may also be accomplished manually with a variac connected to the single turn winding through a 115 V. - 6.3 V. filament transformer and a 10 ohm series resistor. The 60 cps impedance of the single turn winding is of the order of 0.2 ohms.

2.5 100 Kcs Carrier Generator

Dwg. No. 8.9 Crystal Oscillator
8.10 100 Kcs Power Amplifier

The 100 Kcs carrier generator (fig. 2.5.1) consists of a crystal oscillator, a narrow band filter, and a commercially manufactured ultra low distortion power amplifier.

Figure 2.5.2 shows the oscillator circuit followed by a buffer stage. C_1 provides a regenerative feedback path from the tank circuit to the base of the oscillator transistor. The frequency stability of the oscillator is within 50 parts per million (5cps). The measured frequency, under load, is five cycles short of 100 Kc.

The output impedance of the buffer stage is 500 ohms resistive. A high beta ($\beta > 70$) transistor should be used in this emitter follower.

The narrow band filter is a United Transformer Corporation Type BPH-100,000 unit. Source and load impedance are specified at 500 ohms. The attenuation is less than 3 db. within 5% of the 100,000 cps center frequency, and 40 db per octave elsewhere. Thus the filter guarantees that the input to the power amplifier will be free from harmonics.

The power amplifier is Communication Measurements Laboratory, Inc. Model N120M, which is a modified version of a standard CML unit. An instruction manual for the amplifier is available in the CSRP files, but some of the more salient features will be reviewed here for ease of reference.

The amplifier contains its own high voltage power supply, and operates from standard A.C. line voltage. Its maximum output is 100 VA, which corresponds to half the A-units in Tobermory (i.e. 500) being "on" at any one time. The output voltage, with a 1 Ω load, is variable from 0V to 28V p-t-p; the regulation is 0.5 from no load to full load. A 5% change in line voltage causes a 0.5% change in output voltage. The harmonic distortion due to the amplifier is less than 1%, with the second harmonic down 60 db. Hum and noise are also down 60 db below maximum output voltage. The response time of the amplifier (time needed to adjust to new load conditions) is of the order of 50 microseconds, or 5 cycles

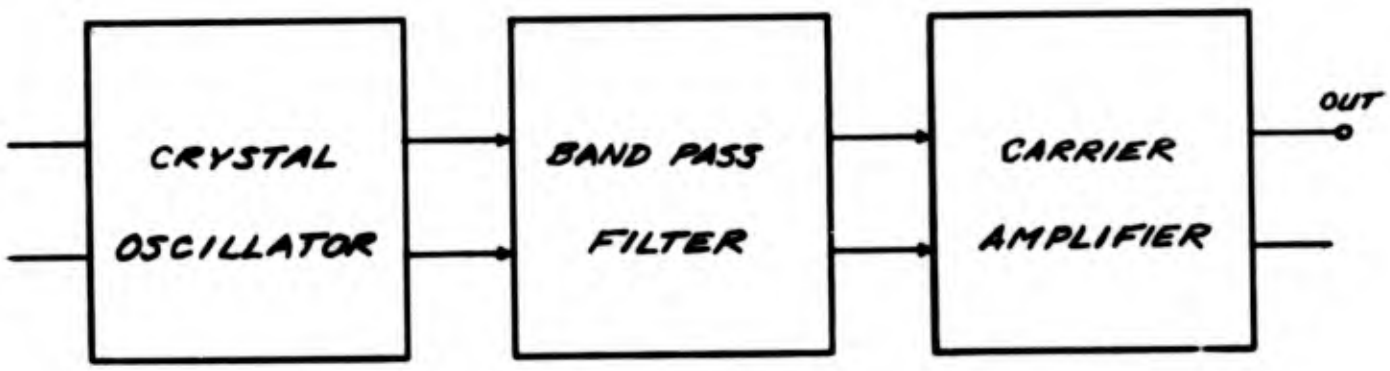


FIG. 2.5.1: 100 K.C./SEC. CARRIER GENERATOR

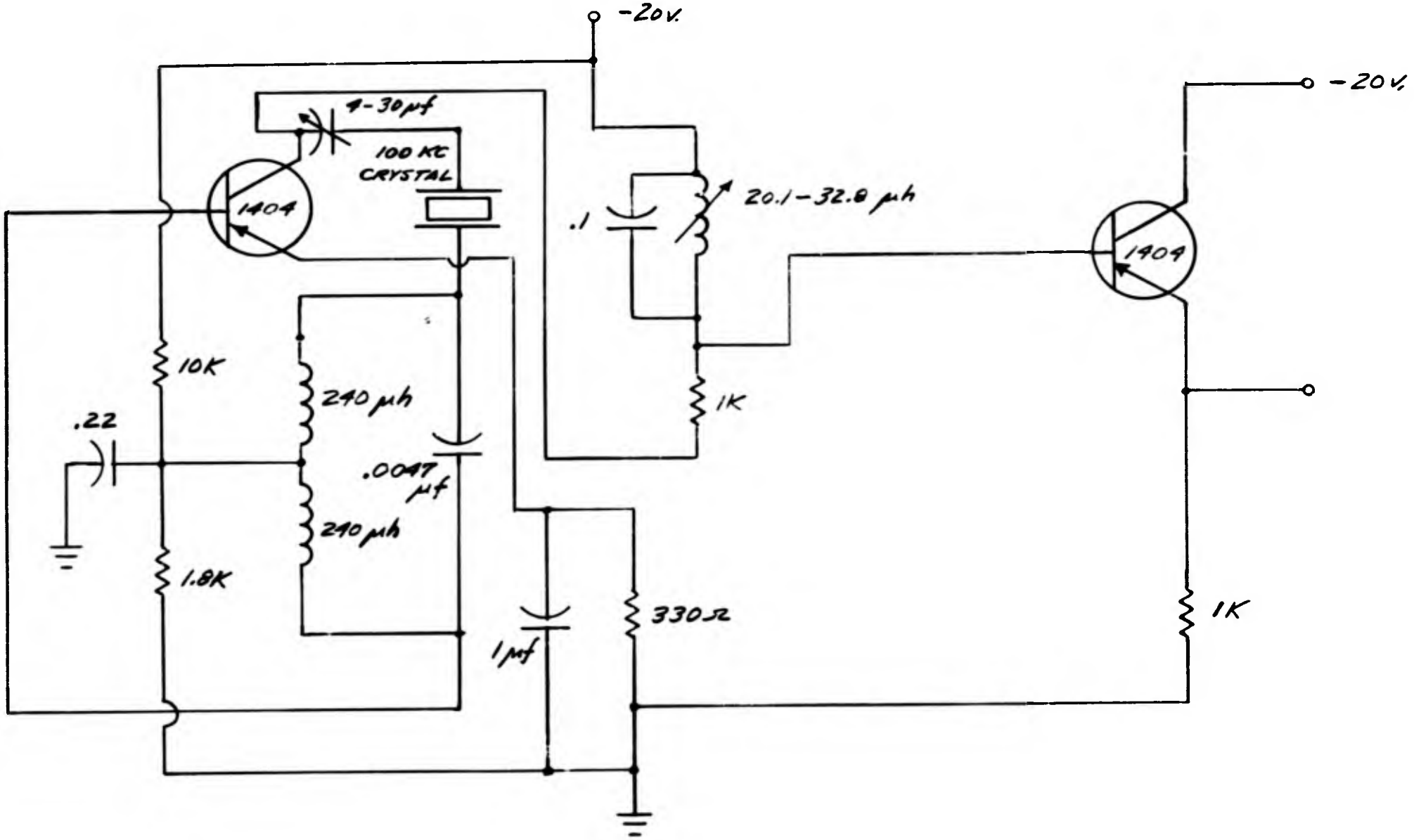


FIG. 2.5.2 : 100 K.C./SEC. CRYSTAL OSCILLATOR

at 100 Kcs. This time is negligible compared to the reinforcement rate.

Since the amplifier contains a number of vacuum tubes, a 30 second delay relay is built into the circuit to allow the filaments to heat up prior to application of the plate voltages. An additional fifteen minute warm up time is required for optimum operation.

The feedback amplifier in the input section (figure 2.5.3) consists of a 6AN8 tube whose pentode section is used as a voltage amplifier (10,000 Ω input impedance) and is directly coupled to the triode section. The triode section is the phase inverter and driver for the power amplifier tubes (6550's). These tubes have a fixed bias of -33V and operate push-pull parallel in class AB1. Negative feedback of approximately 18 db is supplied from the output to the cathode of the 6AN8 pentode section. Positive feedback is also taken advantage of to control the full load to no load regulation. The regulation is adjustable with the "Positive feedback" control on the chassis rear apron (R-33).

In the event of a component change, the following adjustments should be checked:

1. Regulated low voltage power supply, R-48

This control on the rear of the panel is used to set the supply to the recommended 300 V. The adjacent test jack is used to monitor the supply output voltage.

2. Bias adjustment, R-41

The Bias Adj. control is located adjacent to the regulated supply control on the chassis rear apron. The control is adjusted to develop -33V at the test jacks located on the chassis close to the 6550 tubes.

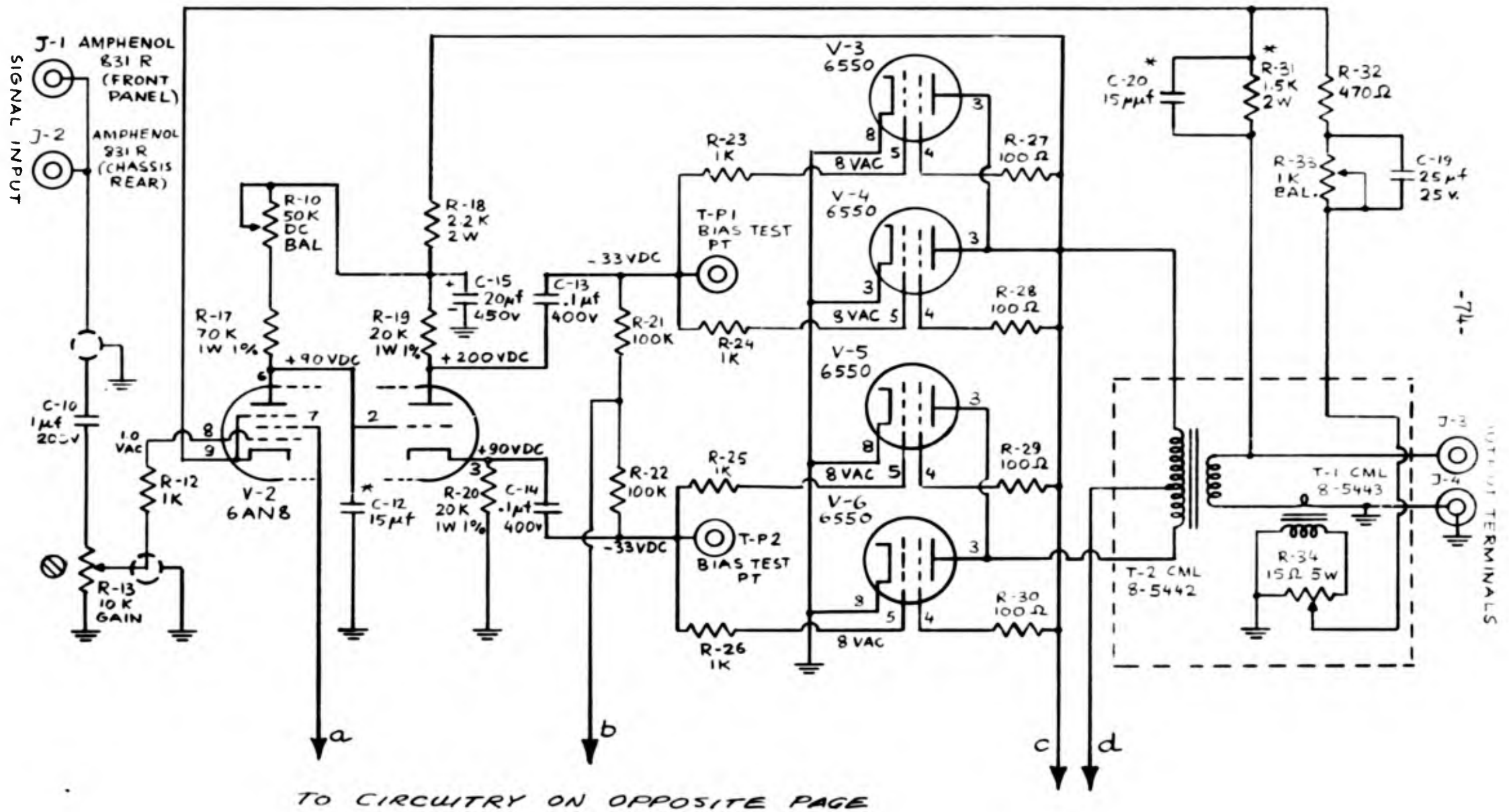
3. A.C. Balance Control, R-33

This control is located on the top of the chassis and marked "A.C. Balance". The extra R-unit filter (or a harmonic distortion analyzer) should be used to set this control for minimum second harmonic content in the output. This adjustment should be made with a dummy load, otherwise a false indication may result from the weight cores.

4. D.C. Balance Control, R-10

This control establishes the operating point of the tube. It should be set in the same manner as the A.C. Balance Control. Proper adjustment of both of these controls is critical to the satisfactory operation of the memory, since

(CML MODEL NO. N120M)



TO CIRCUITRY ON OPPOSITE PAGE

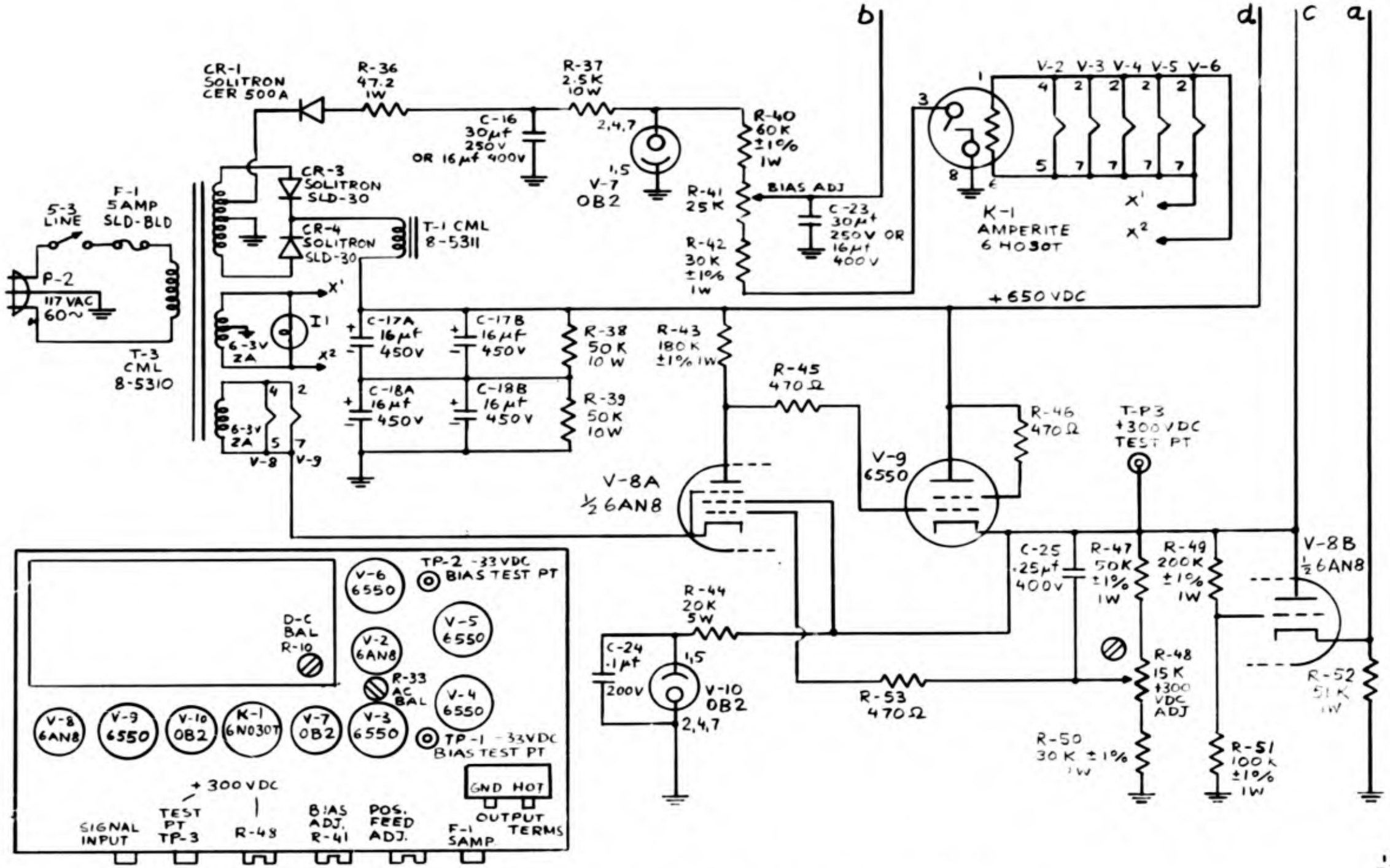


FIG. 2.5.3: 100 K.C./SEC. CARRIER AMPLIFIER
(CML MODEL NO. N120M)

even with only 10% of the A-units active, 0.1 second harmonic in the carrier corresponds to the maximum output of an A-unit.

In actual operation, the output of the carrier generator should be set to 25V p-t-p with the front panel control. A change in the setting of this adjustment necessitates a corresponding change in the reinforcement signal, as shown in section 4.4.

2.6 Erase Circuit

Dwg. No. 8.11 Erase Circuit
6.2 Memory Matrix Detail

The erase circuit, shown on fig. 2.6.1, generates a hundred cycle quassi-sinusoidal waveform of decreasing amplitude. This current, applied through the read-write winding of the memory cores, takes the material through in-spiraling hysteresis loops, eventually leaving the domains oriented at random. The cores are then in the demagnetized state.

The input to the erase circuit is one of the Hewlett-Packard signal generators. The frequency should be set about 100 cps, and the amplitude should be sufficient to give an initial erase current of 1.2 amperes peak-to-peak.

The circuit consists of a single stage emitter follower with a Clairex CL-4 crystal photocell in series with the input signal. The photoresistor's resistance changes from above 10 Megohms to below 3 Kil ohms when the sensitive surface is illuminated. The light source is a G.E. W1820 28 volt bulb, which takes about 250 milliseconds to extinguish. A 150 mfd capacitor in parallel with the lamp prolongs the erase period to about 400 milliseconds.

The R-unit erase selectors on the main control panel are double throw double pole switches which simultaneously connect the D.C. power to the amplifier and switch the single turn core winding from the R-unit to the erase circuit. A momentary contact pushbutton then turns on the light, which goes out at its own rate once the button is released.

The erase circuit reduces the remanent magnetization in the cores to less than 20% of the maximum value, and leaves them in a state independent of their previous magnetization.

Erasure may also be accomplished manually by attaching a 6.3 V filament step down transformer with 10 ohms in series with the low voltage winding to the output of a variac. Very good results may be attained by evenly decreasing the setting from about 50 volts to 0 volts.

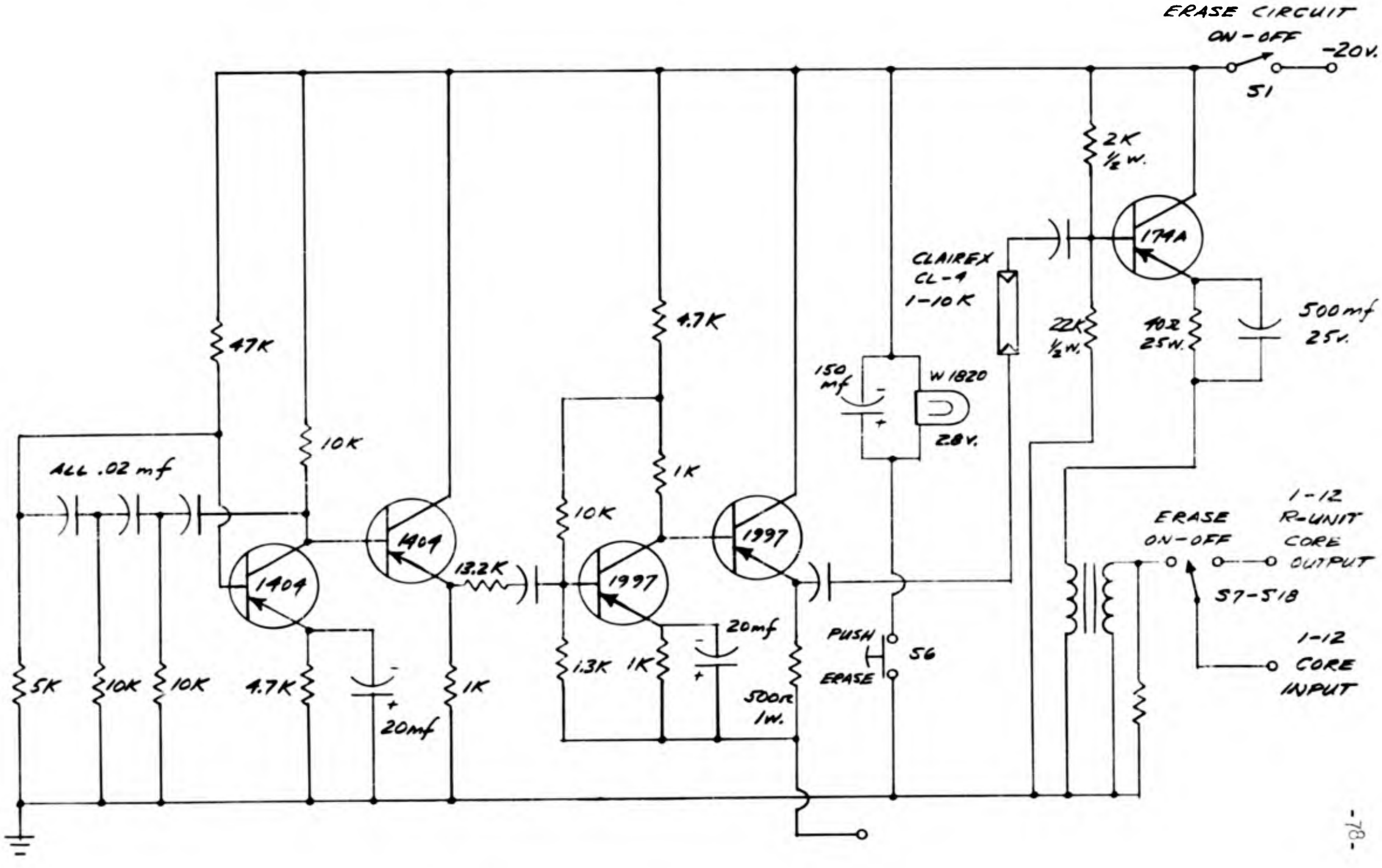


FIG. 2.6.1: ERASE CIRCUIT

2.7 A-unit Input Simulator

Dwg. No. 8.12 A-unit Input Simulator

The A-unit input simulator, shown in block diagram form in figure 2.7.1, is intended to facilitate setting the threshold and pulse stretch time controls of the A-unit.

The simulator is portable and may be plugged in to any A-unit by means of the main plugboard. The output of the unit, triggered by a pushbutton, consists of two simultaneous 10ms pulses, the magnitudes of which may be independently adjusted to the equivalent of one to six S-unit outputs. Whether the pulses represent excitatory or inhibitory inputs depends of course on which hubs they are connected to (yellow or black columns).

The input to the simulator is the signal at the A-unit test point (stand-off). A red light on the simulator chassis indicates whether the pulse has been transmitted to this point, i.e. whether the A-unit threshold has been exceeded. The length of time this signal persists after the input has vanished, i.e. the stretch time, is measured by counting clock pulses at the output of an AND gate which is open only during the "stretch" period. The counter is a four bit binary chain, capable of counting up to 15. In order to maintain an accuracy of at least 10 regardless of how long the stretch time is, the clock rate may be set to 100, 200, or 1000 pps, corresponding to stretch times of 1 to 15, 5 to 75, and 10 to 150 ms.

The counter is reset each time the pushbutton is actuated by the leading edge of the pulse. To ensure that only one pulse is produced, the pushbutton is followed by an integrating circuit. Figure 2.7.2 is a circuit diagram of the whole simulator.

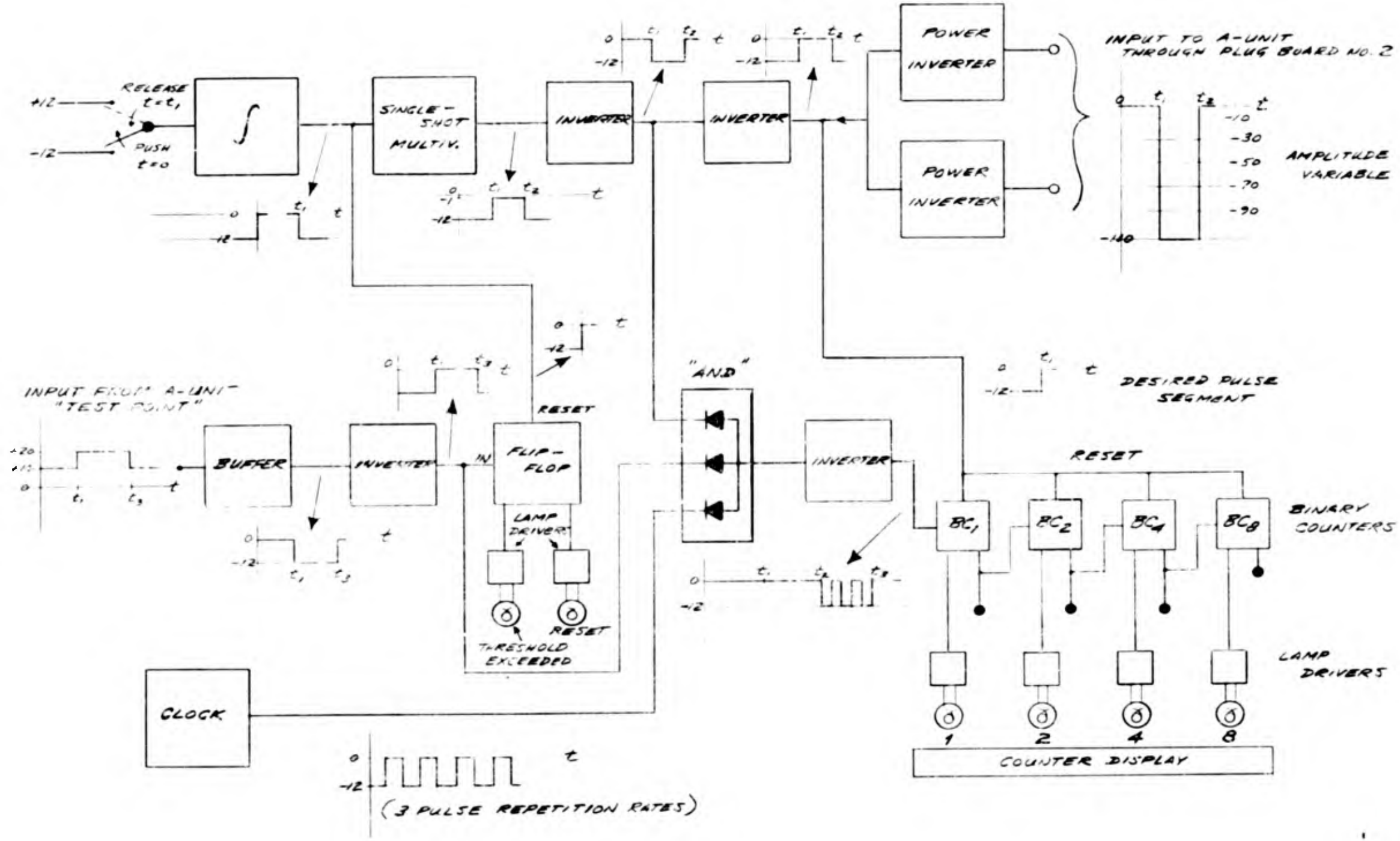
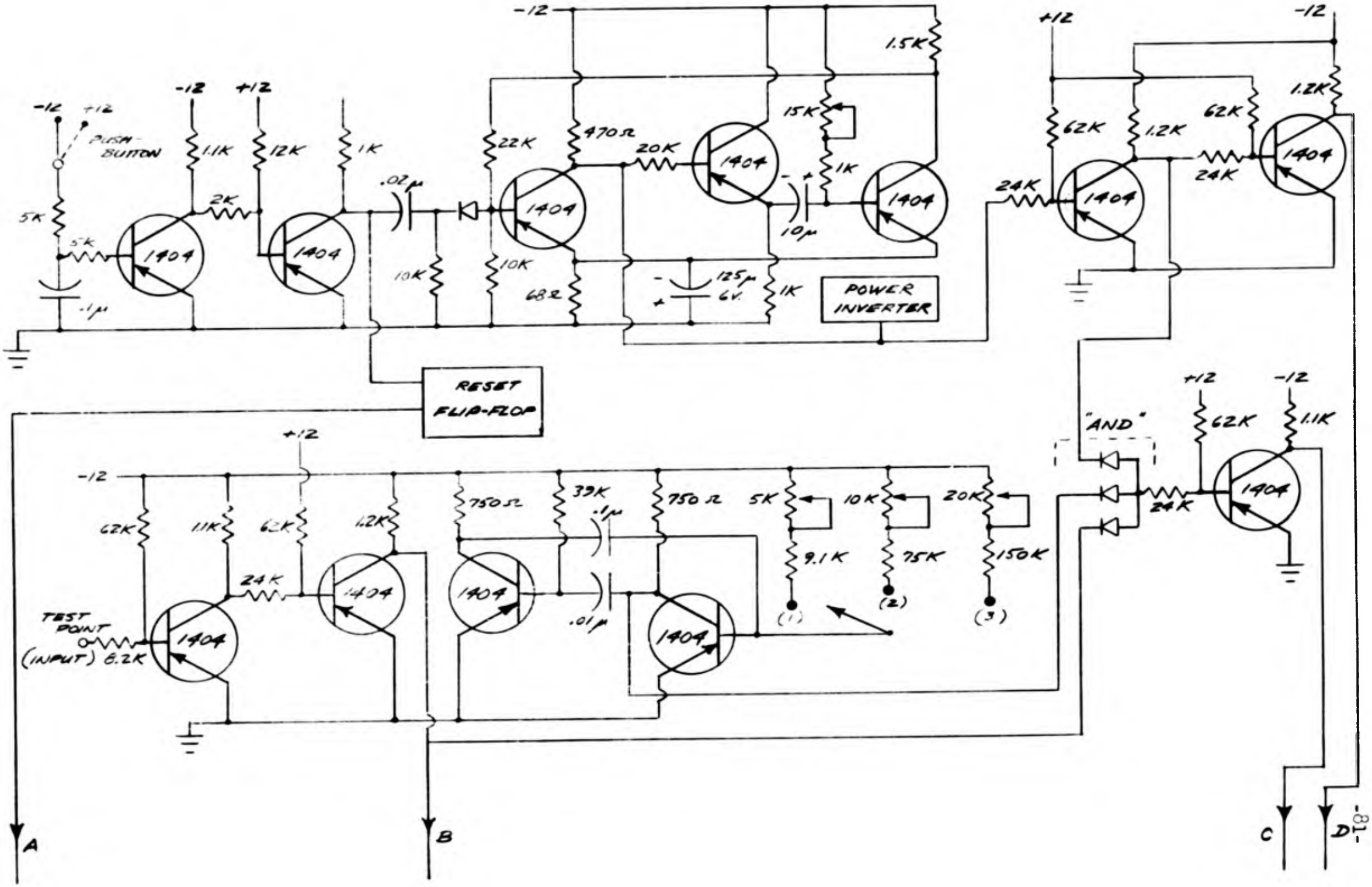


FIG. 2.7.1: A-UNIT INPUT SIMULATOR - BLOCK DIAGRAM

FIG. 2.7.2: A-UNIT INPUT SIMULATOR; PART I (SEE PAGES 82 AND 83)



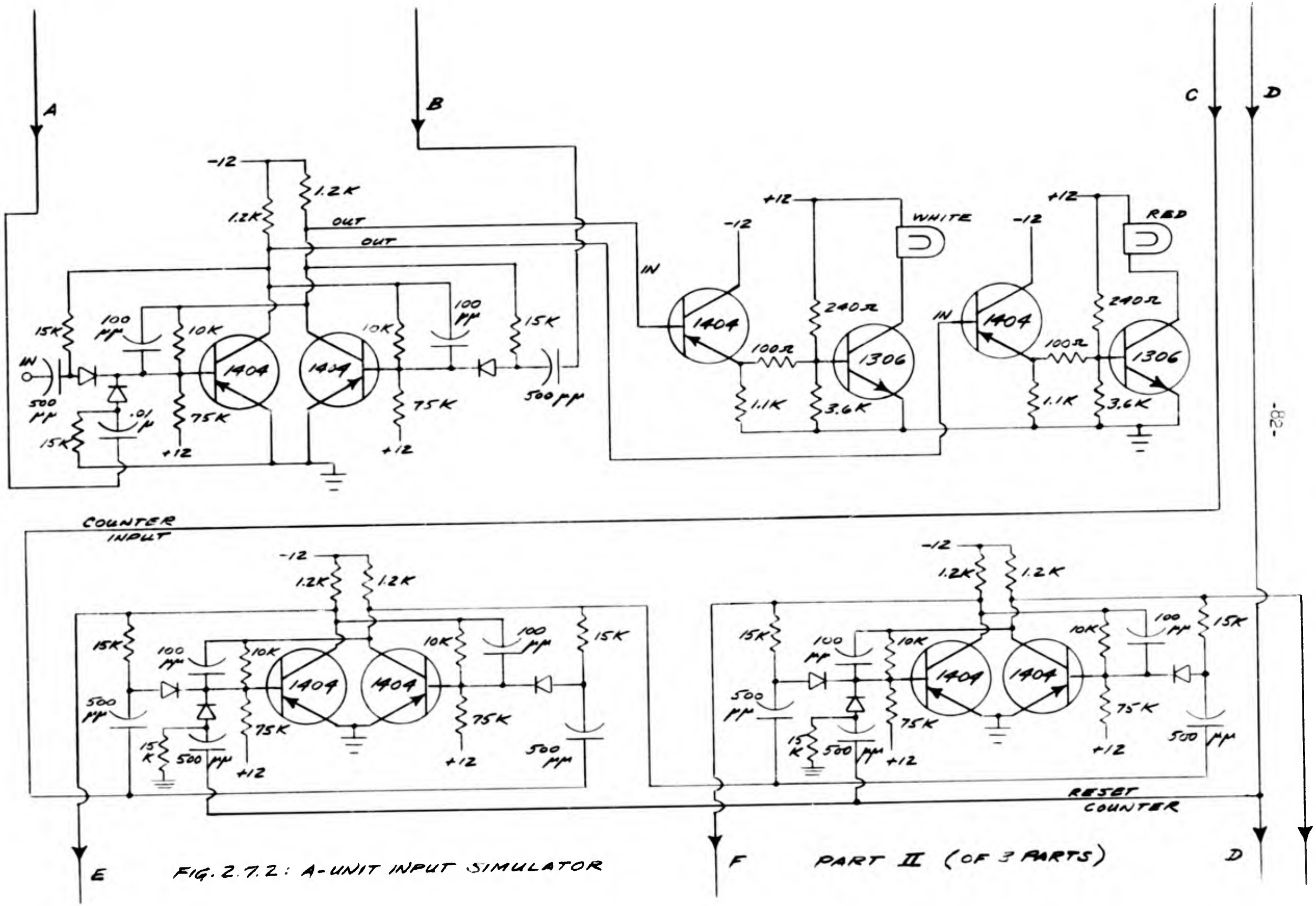


FIG. 2.7.2: A-UNIT INPUT SIMULATOR

PART II (OF 3 PARTS)

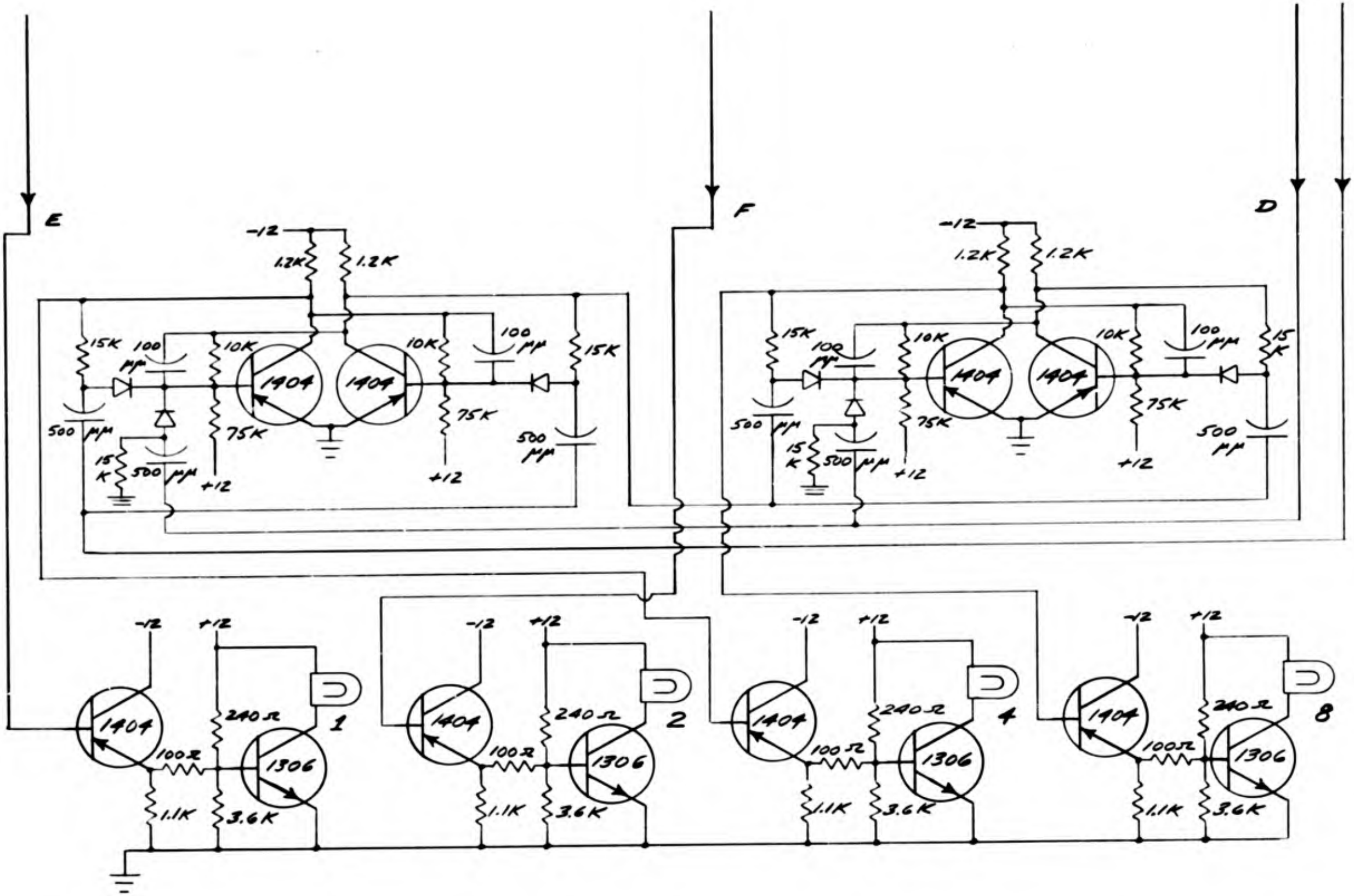


FIG. 2.7.2: A-UNIT INPUT SIMULATOR - CIRCUIT DIAGRAM
PART III ; CONCLUDED FROM PAGES 81 AND 82 .

CHAPTER 3 THE R-UNIT

3.0 Introduction

Dwg. No. 7.1 R-unit Assembly

Each of the 12 R-units receives the weighted outputs of up to 1000 A-units. The function of the R-unit is to determine whether (1) the algebraic sum of its input signals is greater than a preset positive threshold; (2) the algebraic sum of its input signals is less than a preset negative threshold; and (3) the absolute value of the algebraic sum of its inputs is less than a preset absolute threshold.

The information derived from the input is represented in two devices: a bistable multivibrator (flip-flop), and a d.c. gate. The flip-flop is considered to be in the positive state when the signal exceeds the positive threshold, and in the negative state when it exceeds the negative threshold. When the signal falls in between the two thresholds, the flip-flop remains in its previous state. The output of the d.c. gate is at ground level when the absolute threshold is exceeded, and at -10 V. when it is not. The three thresholds are independently adjustable.

The outputs of the R-units are used to control reinforcement, i.e. gate the write pulses to the memory cores.

Since the signals from the weight cores are in the form of 200 Kcs sinewaves, polarity is denoted by phase, and amplitude by peak to peak amplitude. The signed thresholds operate by measuring the peak amplitude of the half wave in-phase or out-of-phase with a reference pulse derived from the 100 Kcs signal generator, while the absolute threshold operates on the peak value of the signal, regardless of phase.

A block diagram of the R-unit is shown on figure 3.0.1. The 200 Kcs signal component is separated from the 100 Kcs carrier by a highly selective band rejection filter, and amplified by a three stage RC amplifier. From this point, the signal is processed along three parallel paths. When the positive threshold detector is triggered, the flip-flop is switched into the

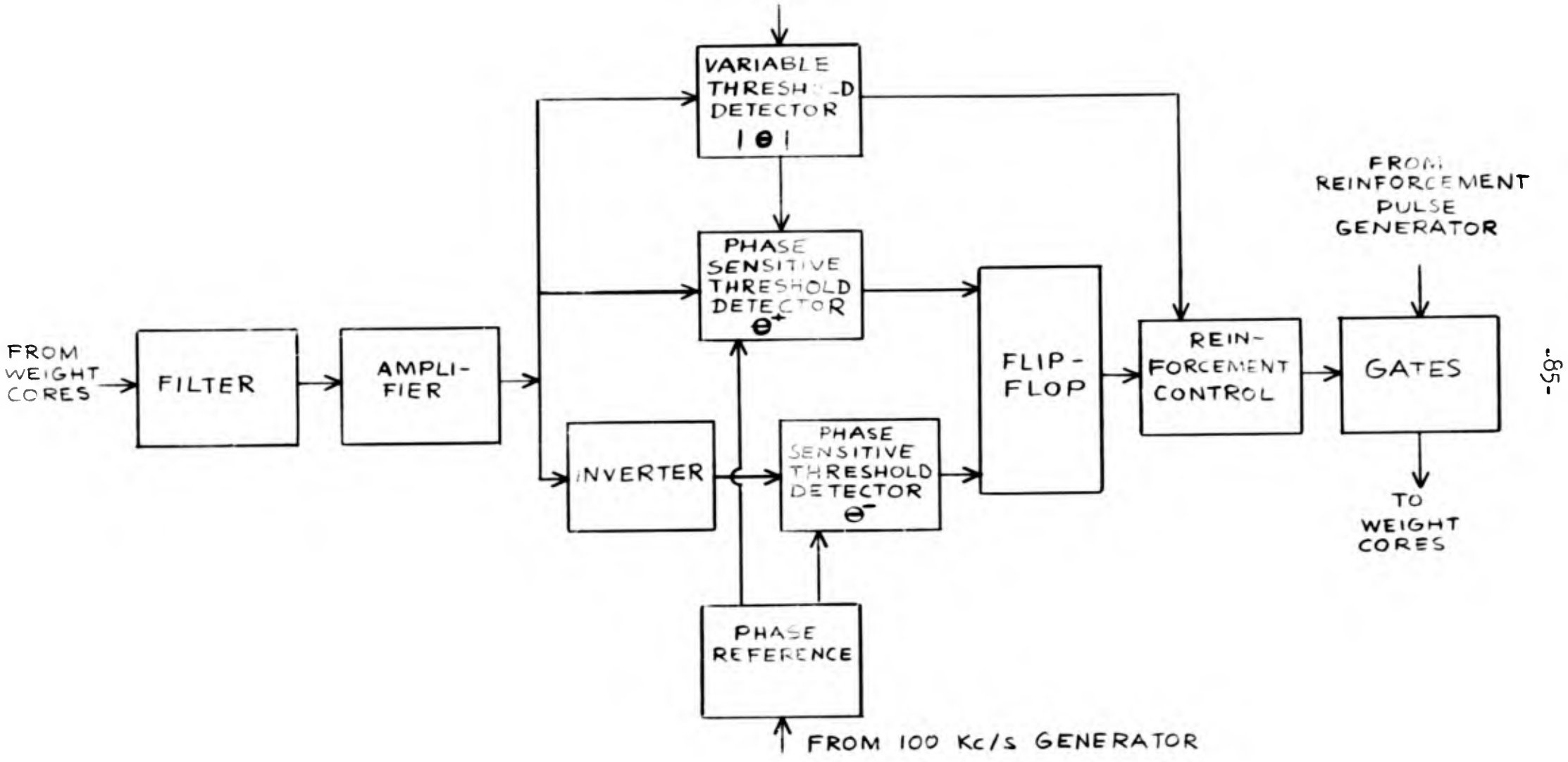


FIG. 3.0.1 : BLOCK DIAGRAM OF R-UNIT

positive state unless it is already in that state; similarly for the negative path. The third path leads to the absolute threshold detector, which activates the d.c. gate.

The outputs of both the flip-flop and the d.c. gate are connected to a double pole double throw relay whose position, set from the main control panel or from the tape, marks the desired response for the R-unit in question. If the control panel switch is in addition in the "error correction" position, then the R-unit signals also determine which of the two pulse gates leading to the write windings of the weight cores are open.

An auxiliary flip-flop, actuating a signal light in the control room, keeps a record of whether the cores belonging to a given R-unit have been reinforced during the course of the last word.*

The various circuits making up the R-unit will now be described in some detail, but for the complete story, the reader is referred to Jules Walder's report.

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* Provision is also made to freeze the response of the R-units by cutting off the reference pulse. This precludes state changes prompted only by the tail end of a word in the delay registers.

3.1 The R-unit Filter

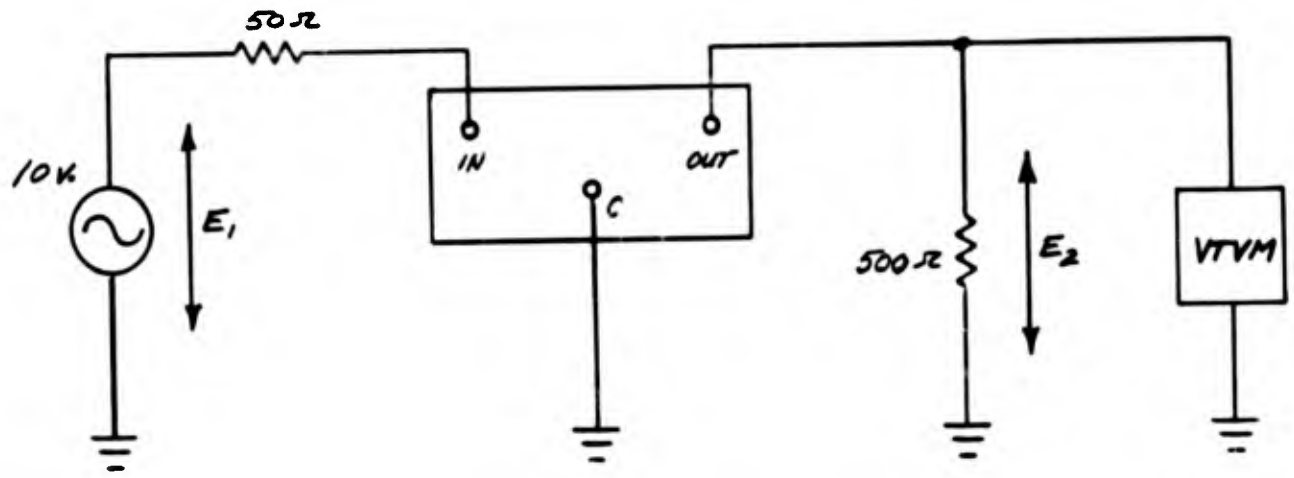
The function of the R-unit filter is to separate the 200 Kcs signal component of the sum of the A-unit outputs from the 100 Kcs carrier. The signal to carrier ratio may be exceedingly small. Suppose, for example, that 201 A-units are on. 100 are reinforced to saturation in the positive direction, and 101 in the negative direction. We are thus trying to detect a difference corresponding to the full output of a single core (assuming that all the cores are identical). The second harmonic component at saturation is about 10 percent of the fundamental. Then the signal to carrier ratio is 1:2000 (63db). This does not even represent the worst possible case, since the cores will not, in general, be set to their maximum level.

It was shown in the preceding paragraph that a very sharp bandpass filter is required for adequate signal detection. In addition to maximal attenuation at the carrier frequency, it is desirable to have rejection peaks at harmonic frequencies other than the second. The pass band should not be too narrow, lest phase distortion result. The characteristic impedance should be high compared to the output impedance of the cores, otherwise circulating second harmonic currents will invalidate the summing scheme. The filter should be capable of handling signalsup to 10 V in magnitude without significant distortion.

A filter was designed to these specifications by Miss Mary Fuchs of United Transformer Corp, New York, New York. The appropriate filter data sheet is reproduced in figure 3.1.1.

Should it be noticed during the operation of Tobermory that the A-unit activity is fairly steady at some level, the task of the filters could be greatly facilitated by adding to the R-unit input a 100 Kcs signal (derived from the carrier generator) of appropriate magnitude and phase to approximately cancel out the carrier component of the original input.

TEST SETUP



TEST RESULTS

DATE: _____ OBSERVED BY: _____

FREQ.	SPECS.	RESULTS
↑	>20	>50
100KC	>80	82
165KC	<3	+2.1
200KC	0 REF. I_L < 2	1.0
220KC	<3	.5
300KC	>40	46.5
400KC	>40	57
↓	>20	>46

U.T.C. NO. EL-309A SOURCE IMPEDANCE 50Ω

CUSTOMER'S NO. _____ LOAD IMPEDANCE 500Ω

DESCRIPTION BAND PASS LEVEL = E1 10V.

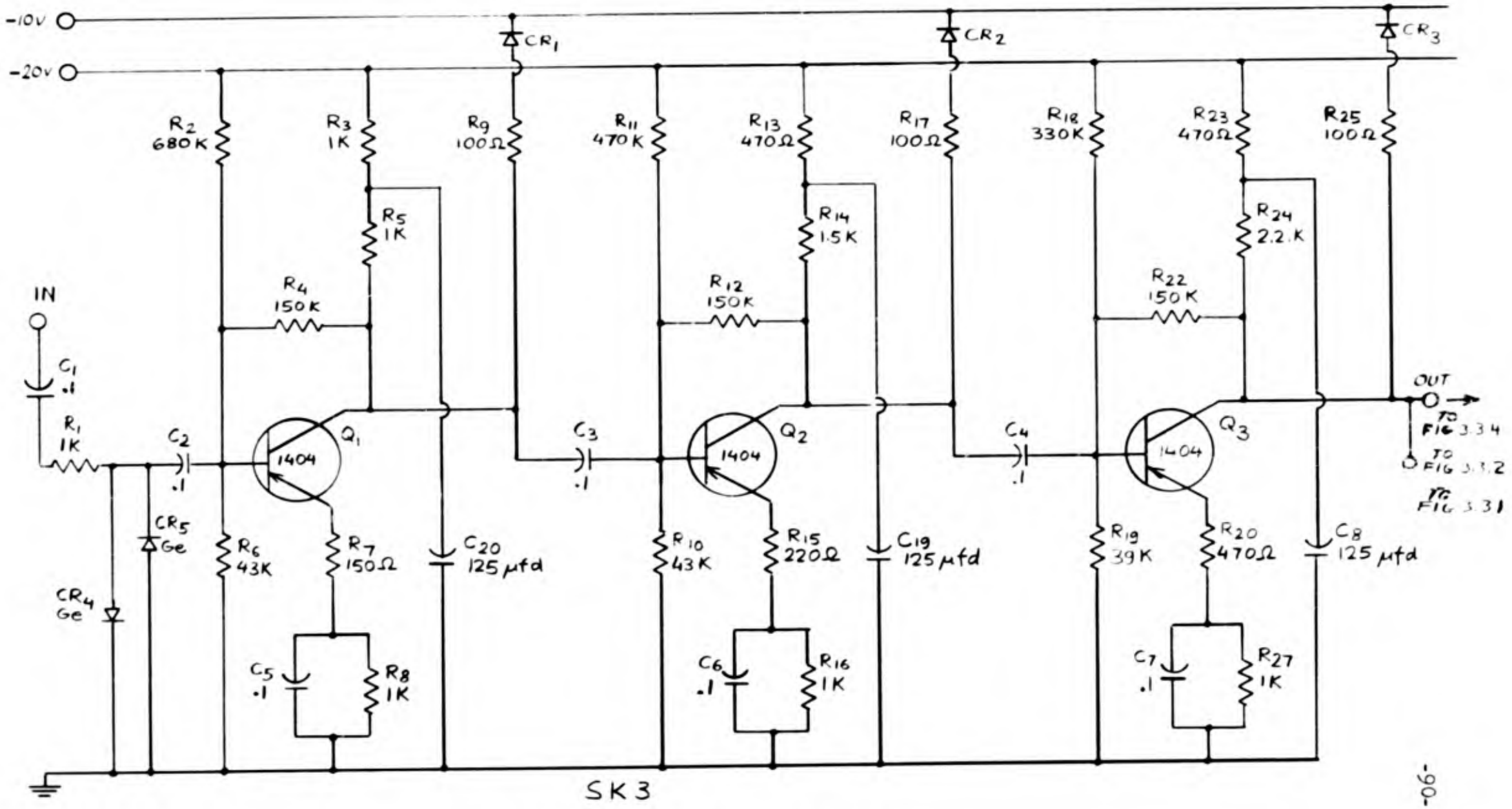
FIG. 3.1.1: FILTER DATA SHEET

3.2 R-unit Amplifier

The maximum 200 Kcs output of each core is about 3 mv. It is desirable to have the R-unit thresholds sensitive to inputs ranging from the equivalent of a single core to the equivalent of fifty. This requires an amplifier with a linear dynamic range of about 34 dbs (50 to 1), from say 3 mv up to 150 mv. The sensitivity of the tunnel diode threshold device furthermore dictates that the amplification be of the order of 70. In order to prevent spurious response at very large inputs, the phase fidelity must be satisfactory over a dynamic range of about 60 dbs.

An amplifier fulfilling these requirements is shown on figure 3.2.1. Two germanium diodes at the input serve to limit the signal input to the amplifier in order to prevent injurious phase shift due to transistor saturation in the last stage. The limiting action begins at about 200 mv. peak to peak (the knee of the diode curve).

Collector to base, and emitter feedback resistors in the amplifier itself increase stability at the expense of gain, and allow for considerable variation in transistor parameters. The biasing resistors were selected to insure symmetrical outputs at each stage even near saturation. Clamping at -10 volts contributes to keeping the outputs symmetrical at high levels. 125 microfarad capacitors are used to decouple each stage.



-90-

FIG. 3.2.1: R-UNIT AMPLIFIER

3.3 R-unit Threshold Circuits

The three threshold circuits (figures 3.3.1 and 3.3.2) are based on the tunnel diode whose generalized current-voltage characteristics are shown on figure 3.3.3. Whenever the current through the tunnel diode is between I_v and I_p (in tunnel diode lore, the subscripts v and p are use to denote valley and peak), the diode may be in one of two states, depending on its previous history; the voltage across it will either be less than V_p or greater than V_v. If the current falls below I_v, the diode will fall back into its low voltage state, while if it rises above I_p, the diode will go into its high voltage state. The switching action is clean and fast.

In the phase sensitive threshold detectors, the phase reference pulse from the reference source (section 3.4) biases the tunnel diode between I_v and I_p. If a signal peak of sufficient amplitude occurs simultaneously with the reference pulse, the tunnel diode will switch into the high voltage state for long enough to trigger the transistor following it. As soon as the reference pulse disappears, the diode returns into its low impedance state, since the signal input to it is limited in order to prevent the signal from triggering the diode by itself (i.e. out of phase). In the off-phase, the tunnel diode is actually back biased by the reference signal for further insurance against out-of-phase triggering.

In the absolute threshold detector, the reference pulse is replaced by a d.c. level, allowing a signal of sufficient amplitude to trigger the diode regardless of its phase.

The impedance level of the signal from the amplifier is decreased to about 50 ohms by means of cascaded emitter followers in order to provide sufficient current for the tunnel diodes. To provide a variable threshold, the fraction of the read-out signal from the cores which is allowed to reach the tunnel diode is adjusted by means of 5KΩ potentiometers mounted in the control room. The diode CR6 limits the positive peaks of the signal to about 200 mv. for the reasons described above. The worst possible condition occurs when the threshold is set to a minimum, but the input signal to the R-unit is

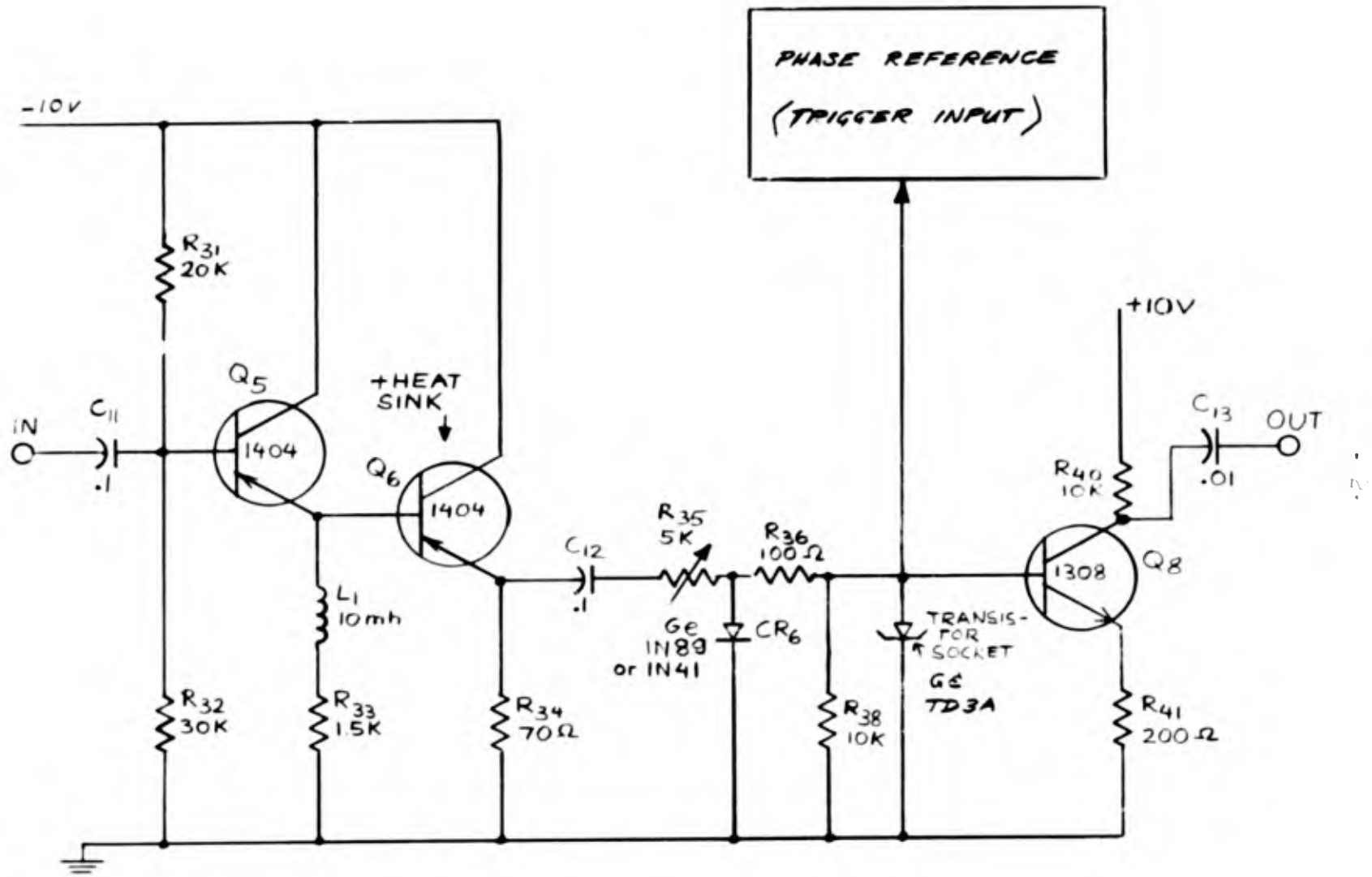


FIG. 3.3.1: PHASE-SENSITIVE THRESHOLD CIRCUIT

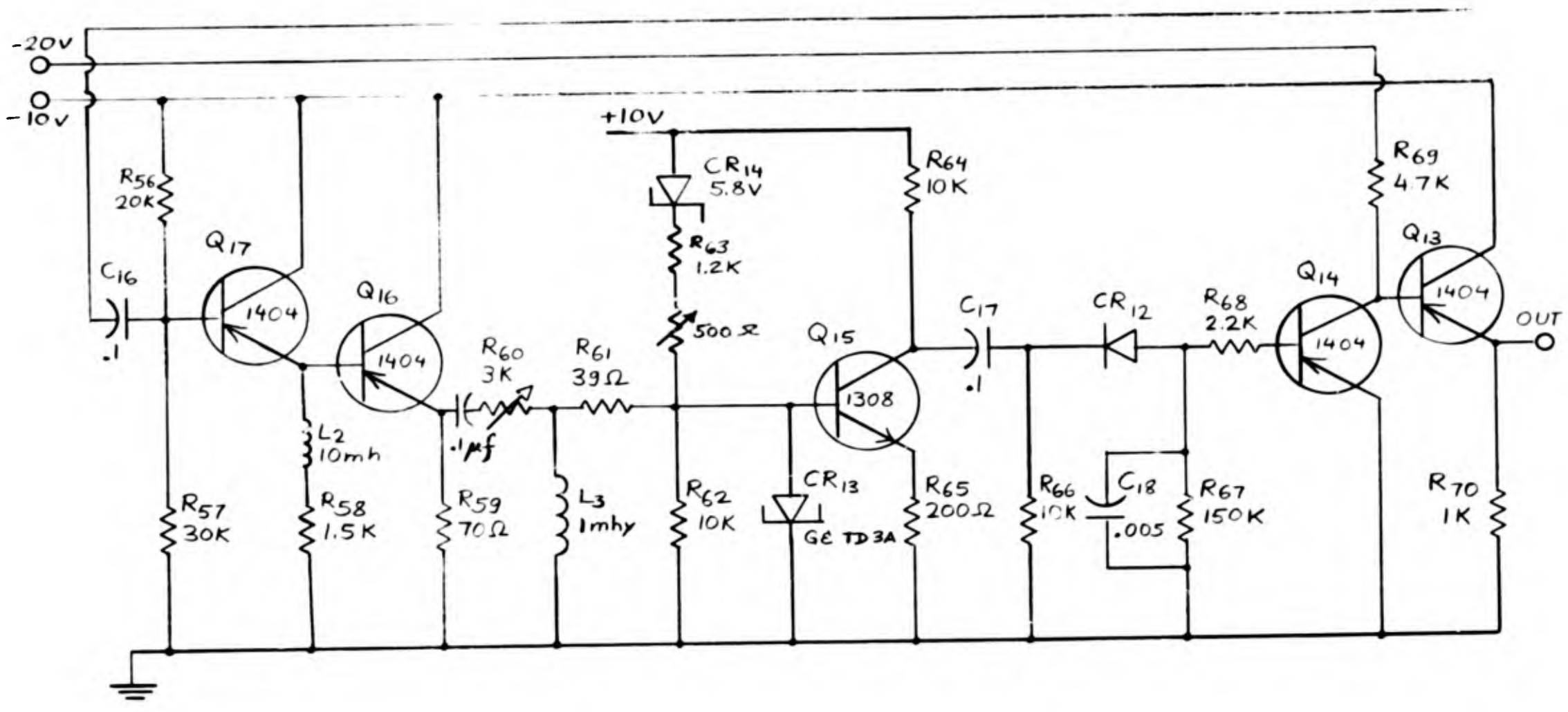


FIG. 3.3.2 : ABSOLUTE THRESHOLD CIRCUIT (4)

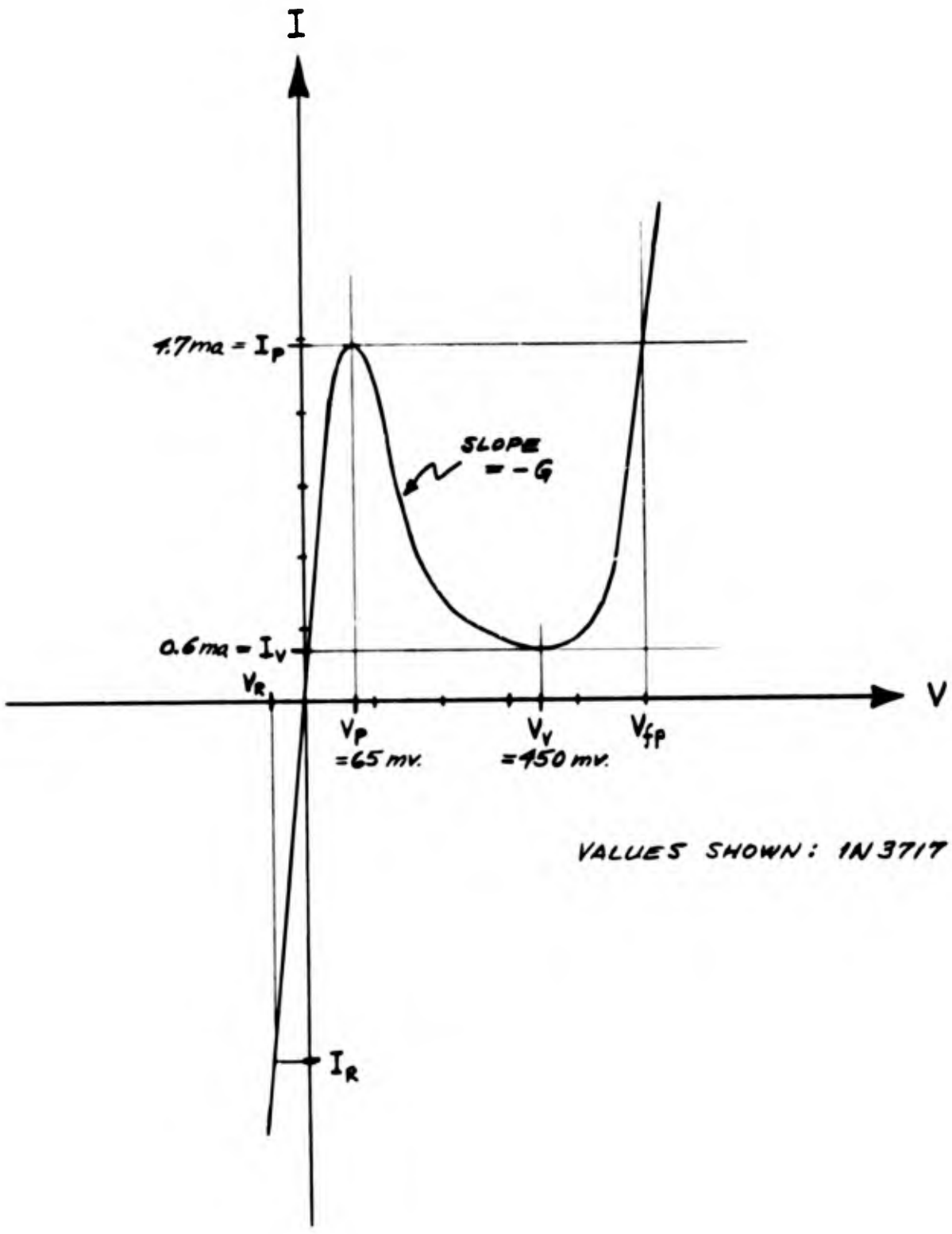


FIG. 3.3.3 : TYPICAL STATIC CHARACTERISTIC - TUNNEL DIODE CURVE

very large. The negative peaks do not, of course, affect the tunnel diode. Note that before reaching the negative threshold detector, the signal goes through a unity gain inverter, (fig. 3.3.4) so that the signal at the tunnel diode of the negative threshold is always 180° out of phase with the signal at the positive threshold. Hence the two tunnel diodes can never be on simultaneously although it is possible for neither to be on.

The threshold detection takes place at the 100 Kcs rate dictated by the reference pulse repetition frequency, but the rest of the system does not respond to cycle-by-cycle variations. The flip-flop which represents the state of the phase sensitive detectors is described in section 3.5. The output of the absolute threshold tunnel diode is amplified, rectified, filtered, (i.e. integrated), inverted, and amplified some more, with the final result that when the absolute threshold is exceeded, the emitter of emitter follower Q13 (figure 3.3.2) sits at 0 V, and at -10 V otherwise.

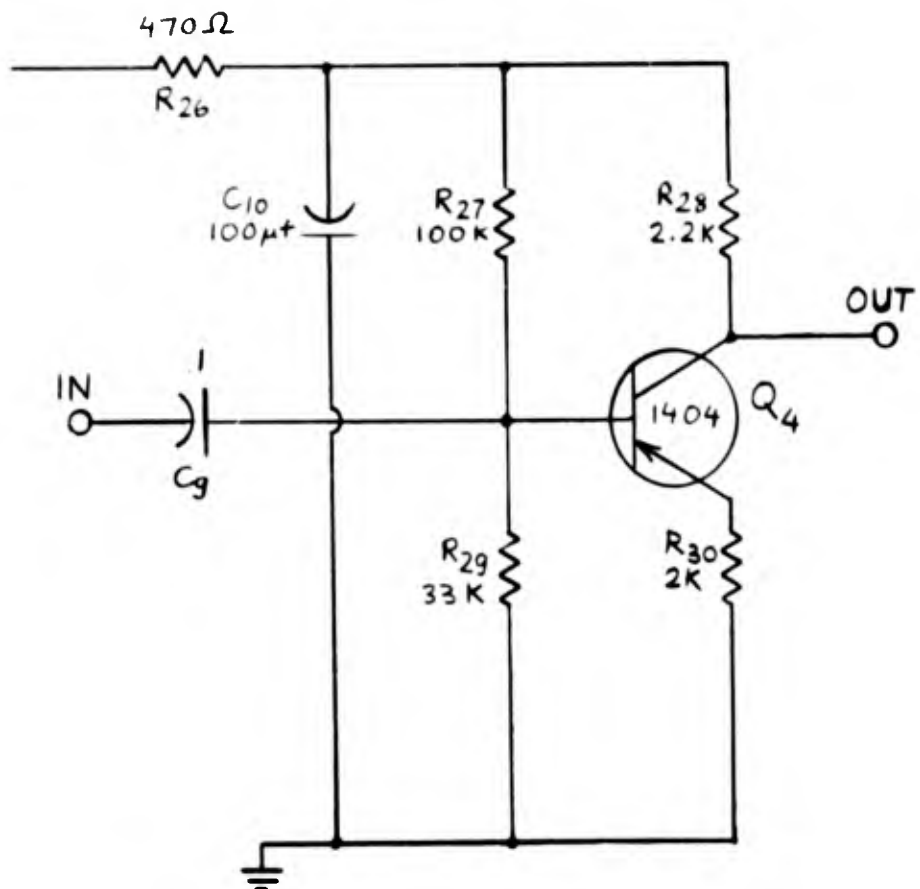


FIG. 3.3.4 : UNITY GAIN INVERTER (2)

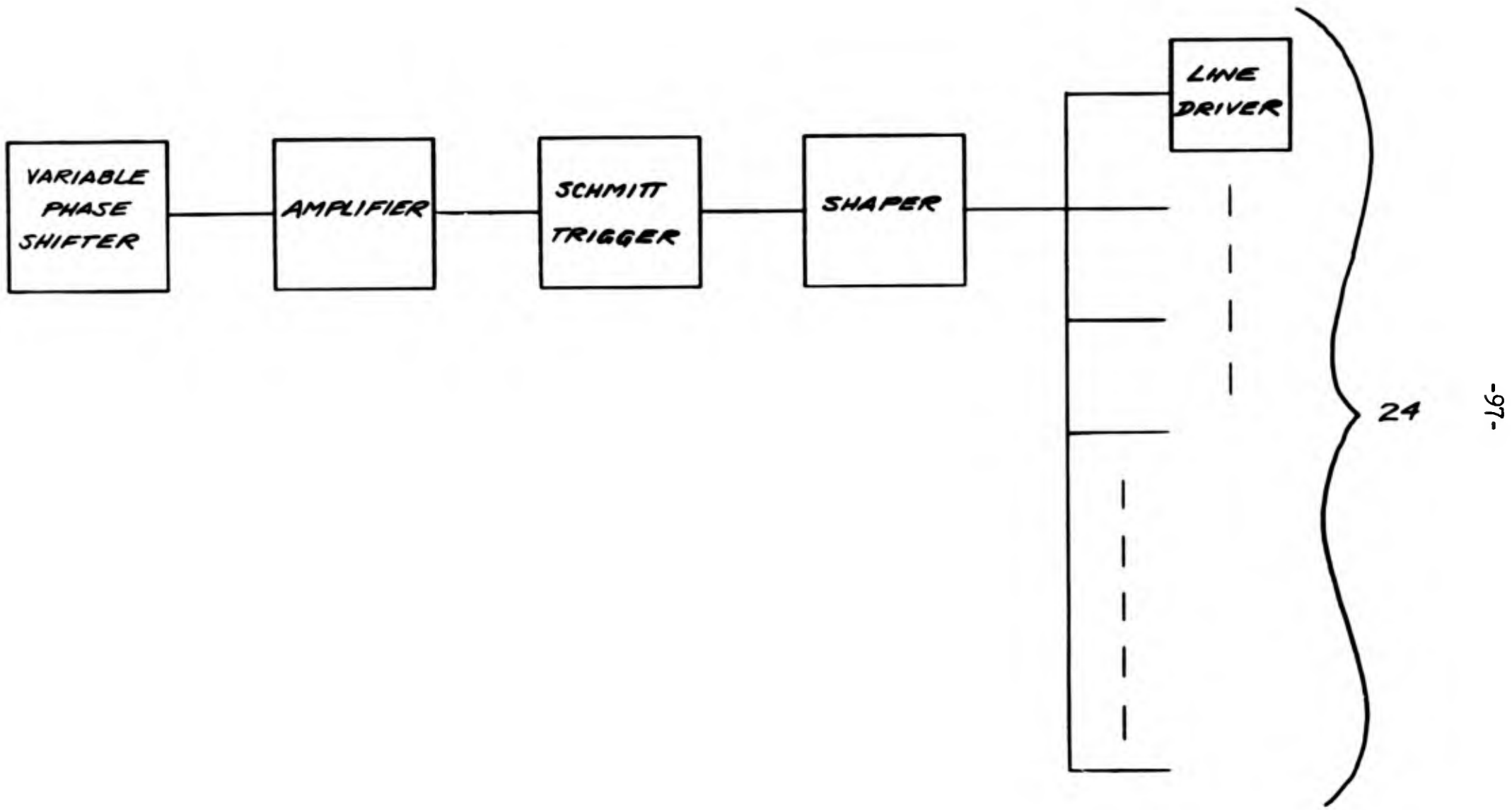
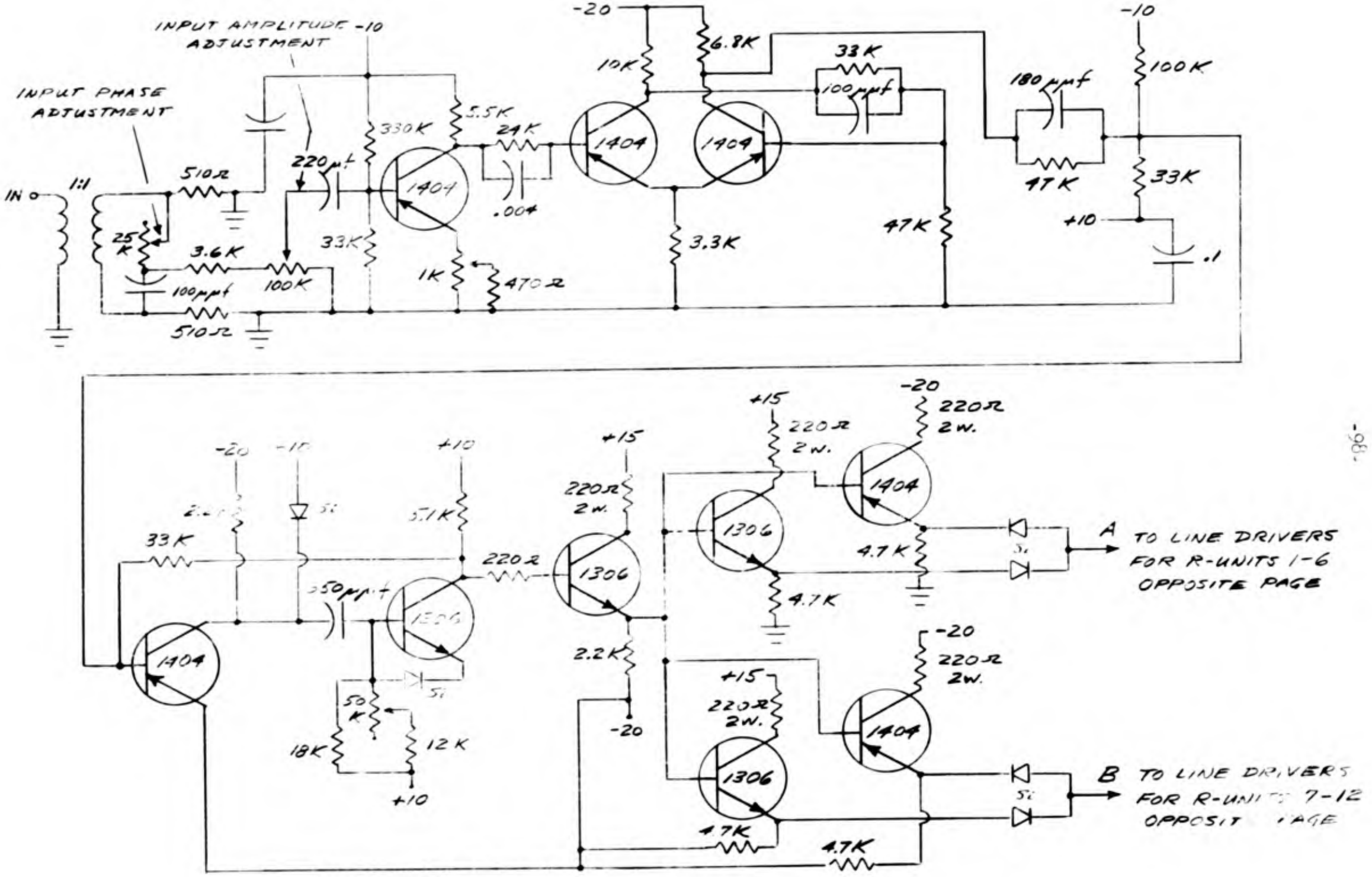


FIG. 3.4.1 : PHASE REFERENCE BLOCK DIAGRAM

FIG. 3.4.2 : CIRCUIT DIAGRAM FOR PHASE REFERENCE SOURCE



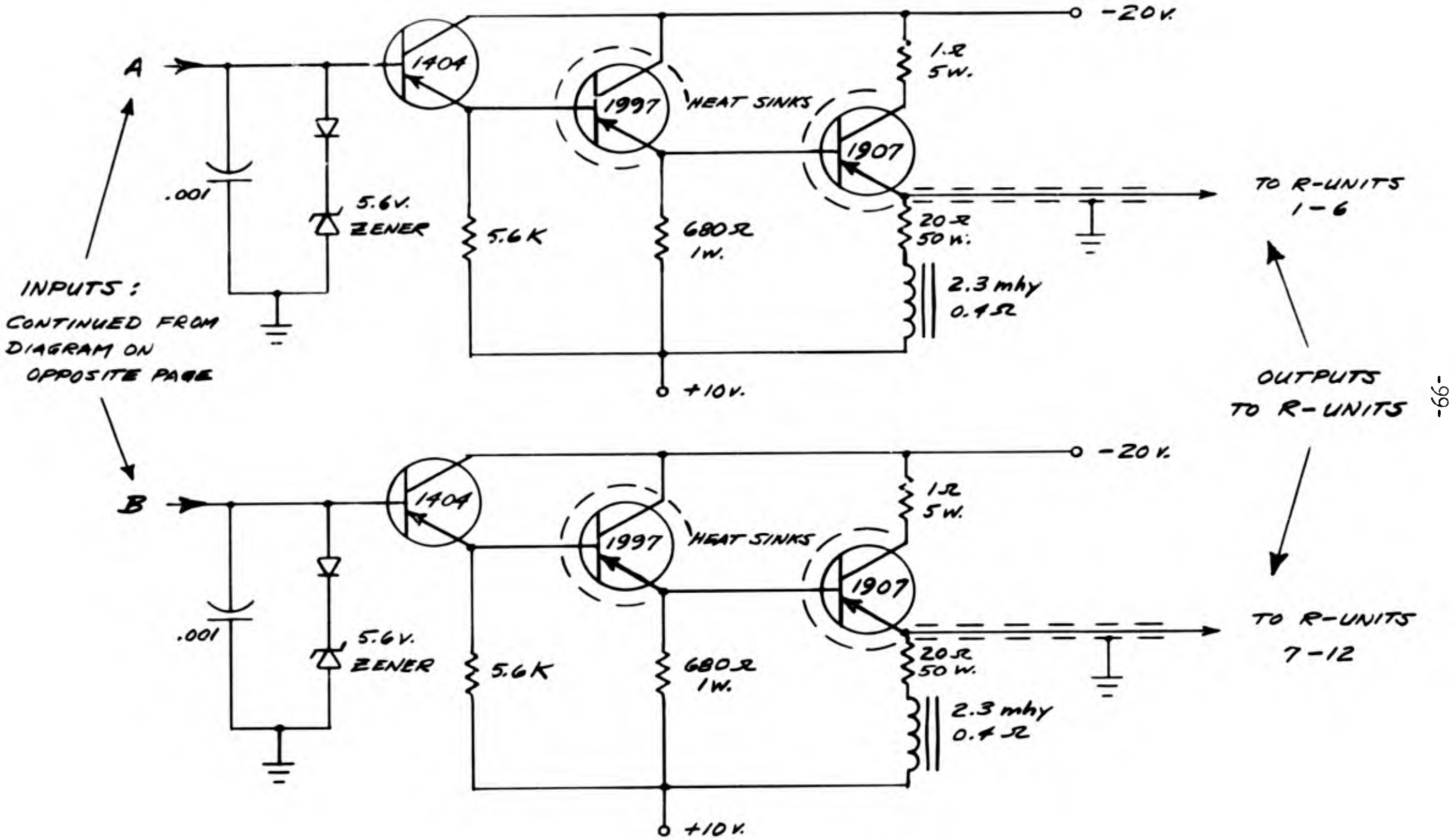


FIG. 3.4.2 : CIRCUIT DIAGRAM FOR PHASE REFERENCE SOURCE

3.4 Phase Reference Source

Dwg. No. 8.13 Phase Reference Source

The purpose of the phase reference source is to supply the R-unit phase comparators with a short pulse at the peak of the (arbitrarily designated) positive waveform. A narrow pulse is necessary in order to ensure that a sloppy waveform (neither in-phase nor out-of-phase) will not attempt to trigger both sides of the terminal flip-flop. The phase detection takes place at a 100 Kcs rate rather than at 200 Kcs since it is convenient to derive the phase reference pulse directly from the carrier generator.

A block diagram of the phase reference source is shown on figure 3.4.1. The phase shifter is an R-C bridge network which can provide up to 180° phase delay in order to compensate for the phase shift through the R-unit amplifier. It also attenuates the signal from the carrier generator to a level suitable for input to the amplifier. The gain adjustment of the amplifier varies the level at which the Schmitt trigger fires; this provides a fine phase adjustment. The leading edge of the Schmitt trigger output pulse is differentiated (the time constant here provides the pulse width adjustment), clipped, and current amplified. The output stage consists of complementary emitter followers to provide a low enough output impedance to drive the twenty four emitter followers at the R-units. These emitter followers are mounted on the same chassis as the phase reference source in order to minimize pick-up by the sensitive R-unit amplifier.

Figure 3.4.2 is a circuit diagram of the phase reference source. Q1 is the input amplifier. Q2 and Q3 make up the Schmitt trigger; Q2 is normally off and Q3 normally on. Q4 is a buffer amplifier, while the differentiation takes place at Q5. Q6 is an emitter follower to drive the output stage. Q7 to Q10 are the parallel push pull (class B) output transistors.

The state of the R-unit may be frozen by cutting off the reference pulse. This is accomplished by cutting off the input amplifier (Q1).

A single manuscript of the original description of the operation of this unit, by Sherman Chow, is conserved in the archives of the Program.

3.5 R-unit Output Flip-Flop

The output flip-flop attached to each R-unit (figure 3.5.1) is aconventional a.c. triggered bistable multivibrator followed by two simple inverters to provide greater fan-out. The output levels are 0 V. and -10 V.

When a tunnel diode is triggered, the inverting amplifier following it emits short pulses at a 100 Kcs rate. The first of these pulses, channeled to the base of one of the transistors of the multivibrator, causes that transistor to conduct, and switches the multivibrator. Subsequent pulses from the same phase detector have no effect. The output of the diode amplifier is buffered by an emitter follower in order to allow a higher load resistor, with increased sensitivity, in the amplifier.

The chief function of the flip-flop is to open and close the reinforcement gates, in accordance with the setting of the desired response relay, when the reinforcement mode switch is in the "error correction" position. The output of the flip-flop also goes to the logic circuits, for display on the control panel and print output.

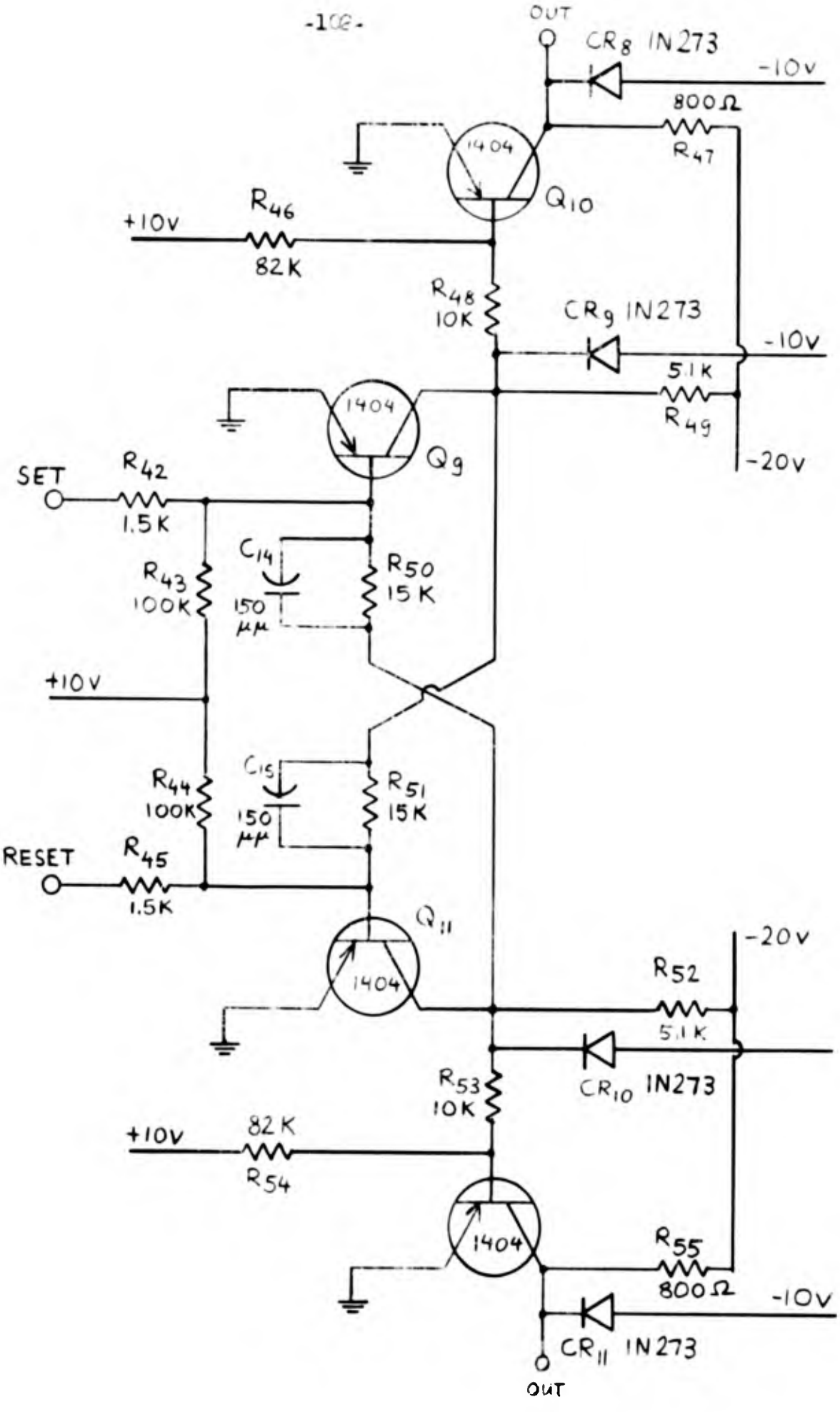


FIG. 3.5.1: R-UNIT FLIP-FLOP (3)

3.6 Reinforcement Gates

Dwg. No. 7.2 Pulse Reinforcement Gates

The purpose of the reinforcement gates is to channel reinforcement pulses of the appropriate polarity to the weight cores when the perceptron is operating the error correction reinforcement mode. The desired response relay connections implement the truth table of figure 3.6.1. Here a 1 indicates that threshold has been exceeded, and a 0 that it has not. The effect of the absolute threshold is to switch the perceptron to the forced response reinforcement mode when the input to the R-unit is not sufficiently decisive.

The three transistor gates (one gate for positive pulses, one for negative pulses) are shown in figure 3.6.2. The drive transistor is turned on only if a pulse from the reinforcement pulse generator coincides with a -10V. signal from the desired response relay. The design load is 50Ω, most of which is made up by a current regulating potentiometer in series with the write winding of the cores. The gates can tolerate considerable drift in the power supplies and in the trigger pulse amplitudes.

Whenever a word has been reinforced, a signal light in the control room, actuated by a flip-flop, is lit. The flip-flop is sensitive to a negative-going edge, so it is triggered by the trailing edge of a positive pulse and the leading edge of a negative pulse. A reset signal from the auxiliary logic resets the flip-flop at the completion of each word cycle.

The operation of the gate is explained on a transistor-by-transistor basis in a report by Jules Walder (manuscript in Program files).

Desired Response	Absolute threshold 0 if exceeded	Actual Response	Signal to Sense Winding
0	0	0	0
		1	-10 v.
	1	0	-10 v.
		1	-10 v.
1	0	0	+10 v.
		1	0
	1	0	+10 v.
		1	+10 v.

Truth Table for Reinforcement Gates

Figure 3.6.1

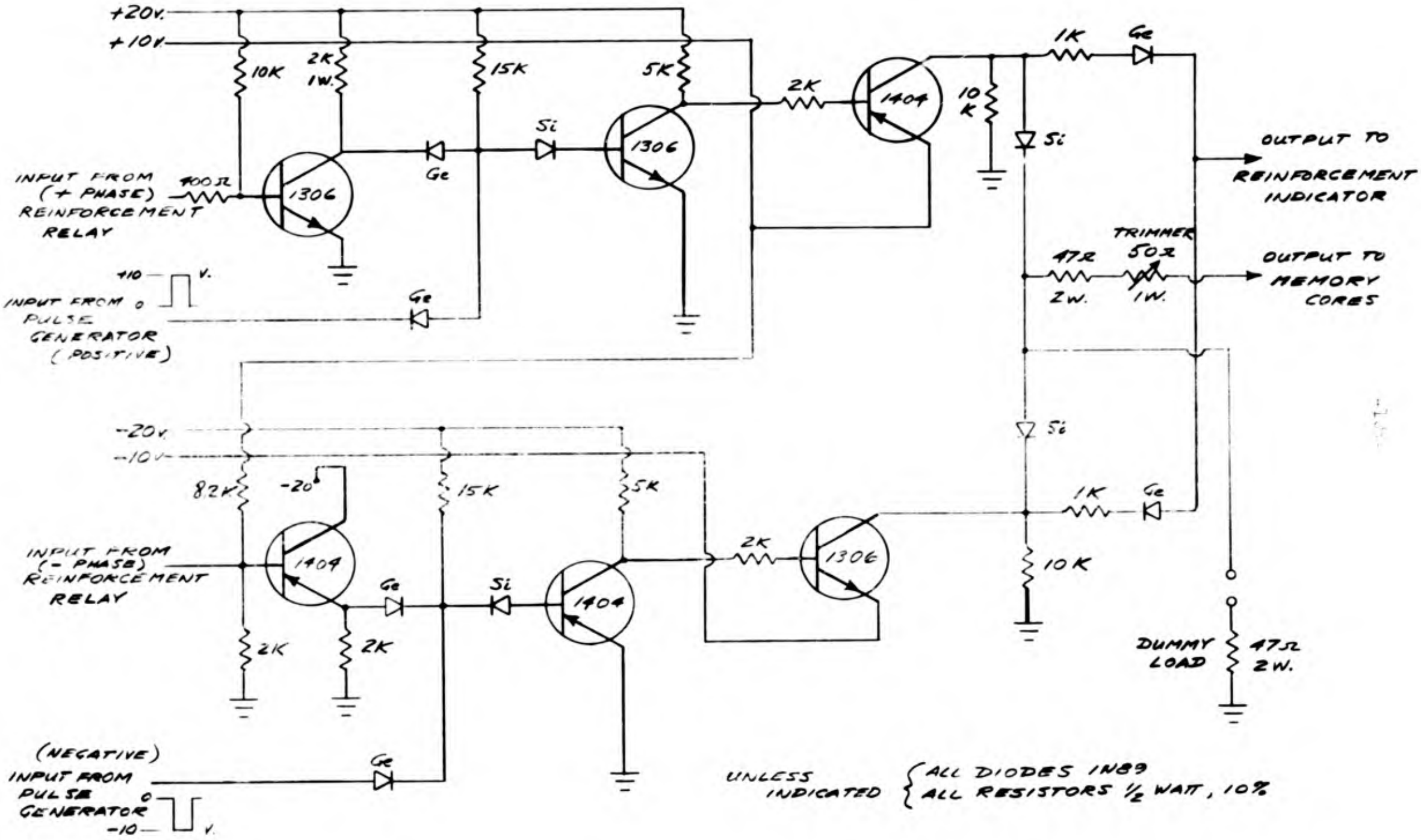


FIG 3.6.2 : PULSE REINFORCEMENT GATES

3.7 Reinforcement Pulse Generator

Dwg. No. 8.4 Reinforcement Pulse Generator

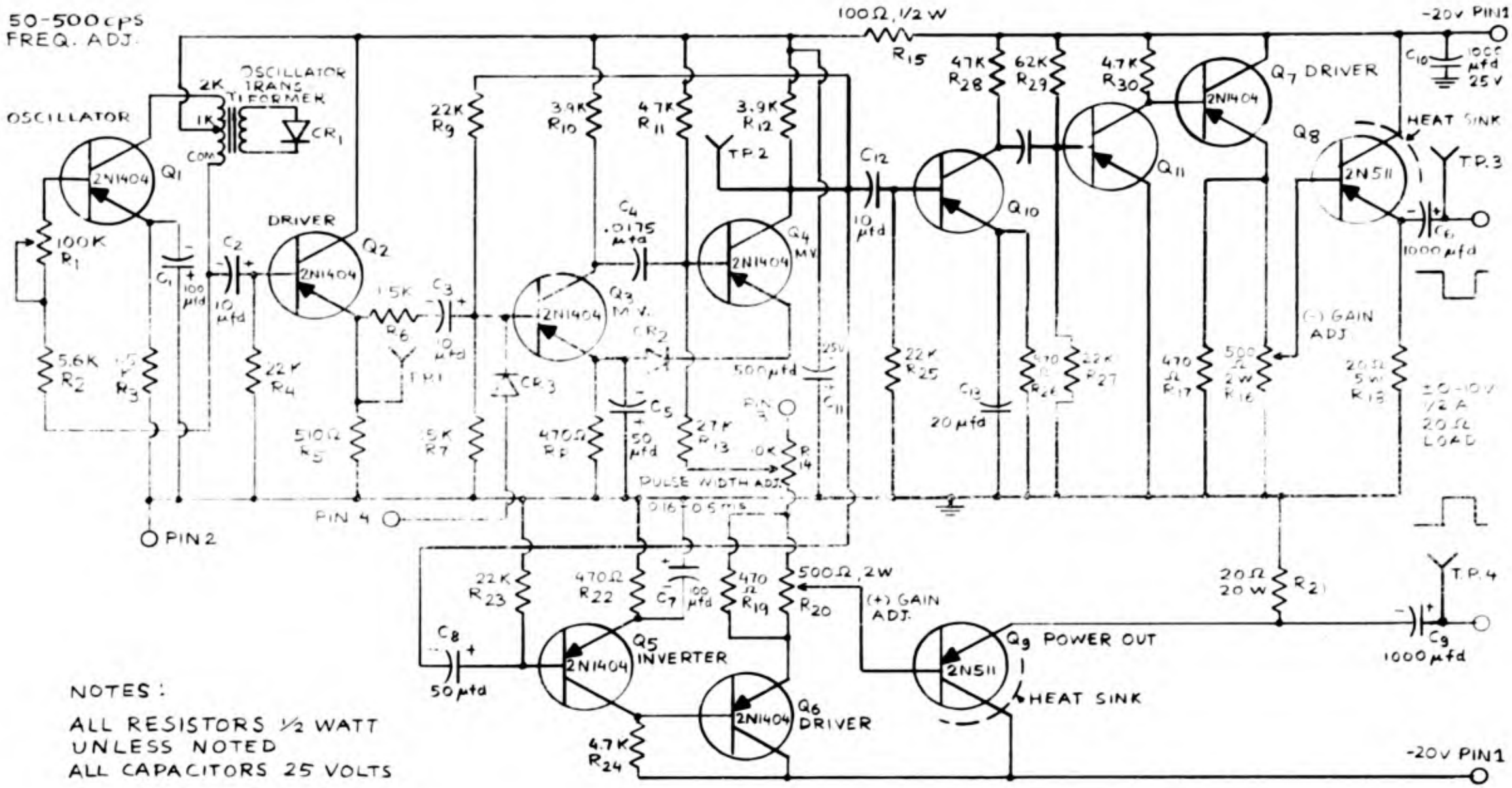
The reinforcement pulse generator provides the R-unit pulse gates (section 3.6) with positive and negative pulses of up to 500 ma amplitude, .16 to .50 ms. pulse width, and 50 to 500 pps pulse repetition frequency.

The pulse generator, which shares a chassis with the trigger generator described in section 1.11, consists of eleven transistors numbered Q1 tc Q11 (fig. 3.7.1). Q1 and T1 (oscillator transformer) produce a square wave whose frequency may be varied in the 50 cps to 500 cps range by feedback frequency control R1. Q2 is an emitter follower buffer stage which keeps the oscillator from being loaded. Q3 and Q4 form a 'one shot' multivibrator triggered by the positive portion of the oscillator output. The output of the multivibrator (at Q4) is a negative pulse whose width may be varied from .16 msec. to .50 msec. with pulse width control R14. This negative pulse is fed into saturated amplifier Q10 in order to keep the frequency variation from affecting the pulse amplitude. Q11 is a saturated inverter providing emitter follower Q7 with the necessary drive. The output of Q7 is controlled by the negative gain adjustment R16, and in turn serves as drive for the power output stage, emitter follower Q8.

The positive pulses are obtained in a similar manner through saturated inverter Q5, emitter follower Q6, positive gain adjustment R20, and power emitter follower Q9.

The amplitude adjustments should be set at 6 V. with all the pulse gates connected, and 0 volt signals on the R-unit lines.

Grounding the base of Q3 through a diode turns the pulse generator off.



NOTES:

ALL RESISTORS ½ WATT
UNLESS NOTED
ALL CAPACITORS 25 VOLTS

FIG. 3.7.1: REINFORCEMENT PULSE GENERATOR

3.8 Word Termination Detector

Dwg. No. 8.5 Word Termination Detector

The word termination detector serves to distinguish the period of silence ensuing immediately after the termination of a word from the normal absence of input. The chain of switching transistors and the two flip-flops forming this unit are shown in fig. 3.8.1. Functionally, the detector consists of an amplitude threshold, a time lag setting which allows ignoring the very brief periods of silence which occur normally in the course of a word, a Start flip-flop which remembers that a word has begun since the last reset signal, and an End flip-flop which indicates that the word has actually ended.

The sequence of events is as follows. 0 V. reset signal from the control logic (Chapter 4) turns Q_8 and Q_9 on. The unit is now ready for an input from the average amplitude indicator (section 1.4). If a negative voltage of sufficient amplitude ('sufficient' depends on the setting of the 100K threshold potentiometer) is sensed, Q_1, and hence Q_2 and Q_3 are turned on. Q_2 turns Q_7 on, reminding Start that a word is in progress.

If the input now falls below threshold amplitude for long enough to allow the 20 µfd capacitor in the collector circuit of Q_3 to discharge through the time lag potentiometer, then Q_3 is turned off, turning Q_4 on. This permits Q_5 to cut off, turning on Q_6. Note that Q_5 can be off only if both Q_4 and Q_7 are on, i.e. a word must begin before it can end. Q_6 turns Q_9 off, and a 0 V. output at the emitter follower Q_{11} signals the end of the word. This signal persists until the next reset signal, regardless of the input.

The amplitude threshold may be set at .5% to 20% of full scale, and the time lag setting will ignore pauses up to 50 msec. long.

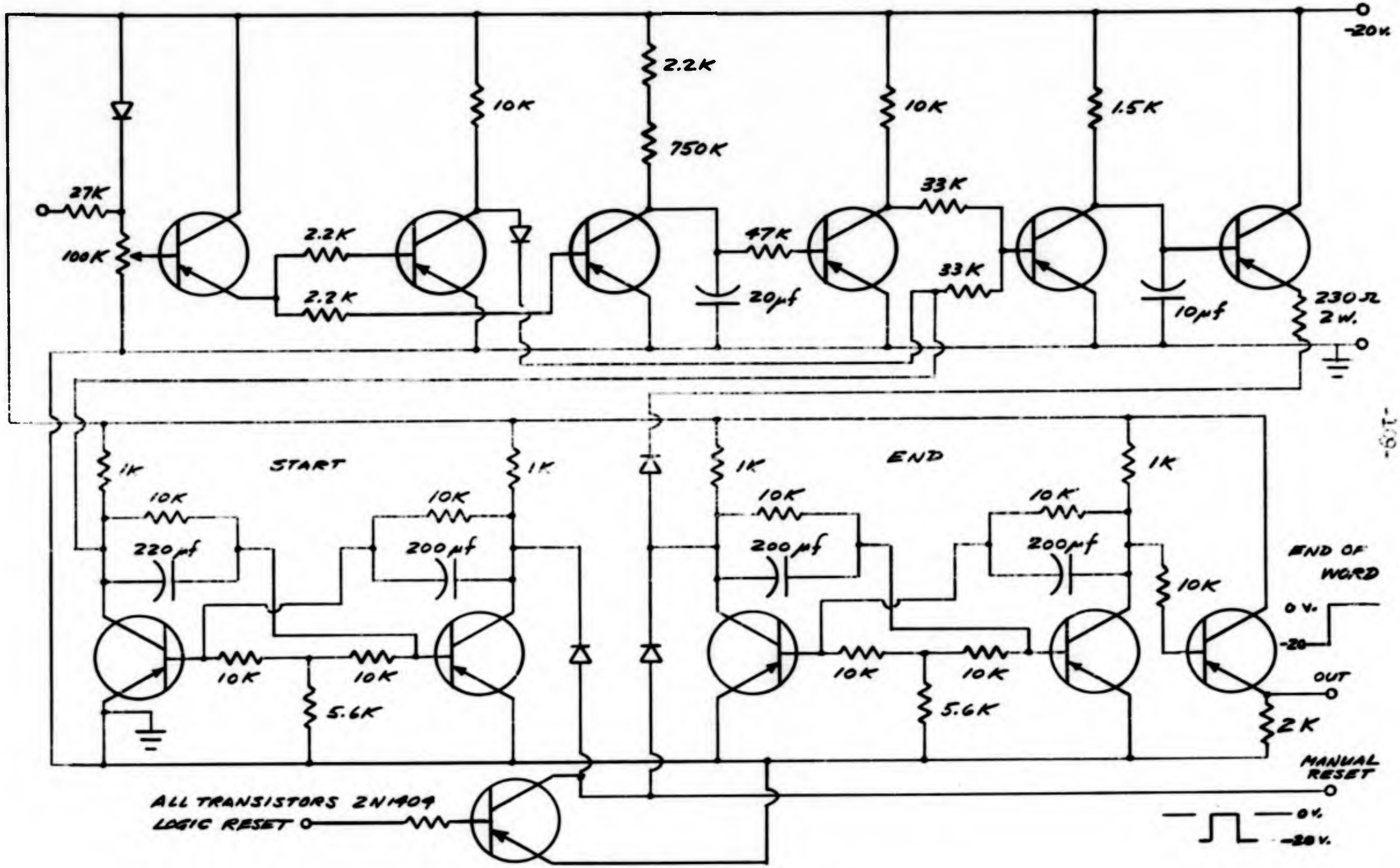
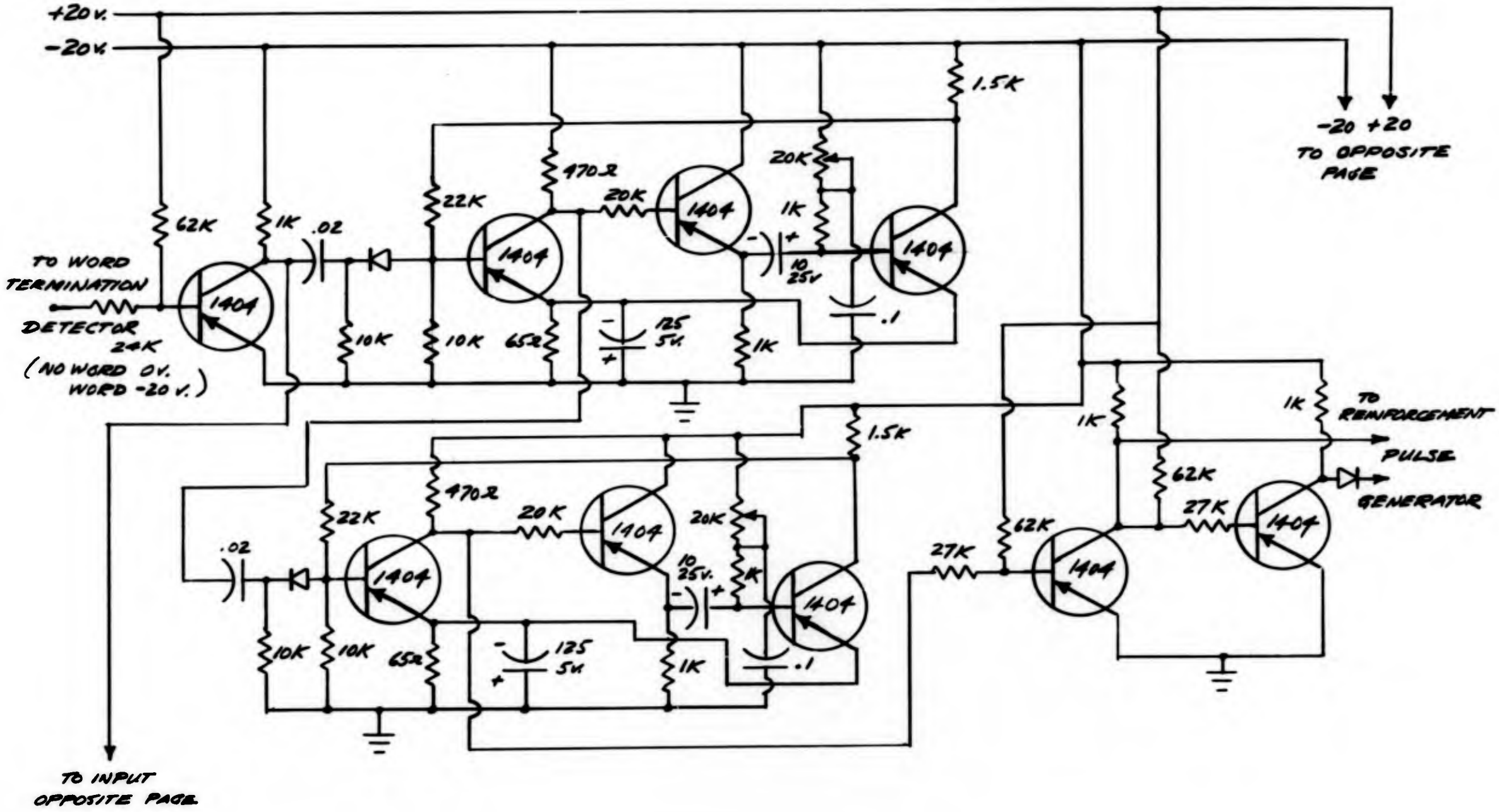


FIG. 3.8.1: WORD TERMINATION DETECTOR


+20 v.
-20 v.
1.5K
-20 +20
TO OPPOSITE
PAGE
470Ω
20K
22K
20K
1404
1K
62K
1K .02
1404
1404
TO WORD
TERMINATION
DETECTOR
24K
(NO WORD 0V.
WORD -20 V.)
10K
10K
652
125
5M
1K
.1
10
25V
1K
TO
REINFORCEMENT
PULSE
GENERATOR
62K
27K
1404
1.5K
470Ω
22K
20K
1404
20K
.02
1404
10
25V.
1K
10K
10K
652
125
5M
1K
.1
27K
62K
1404
TO INPUT
OPPOSITE PAGE

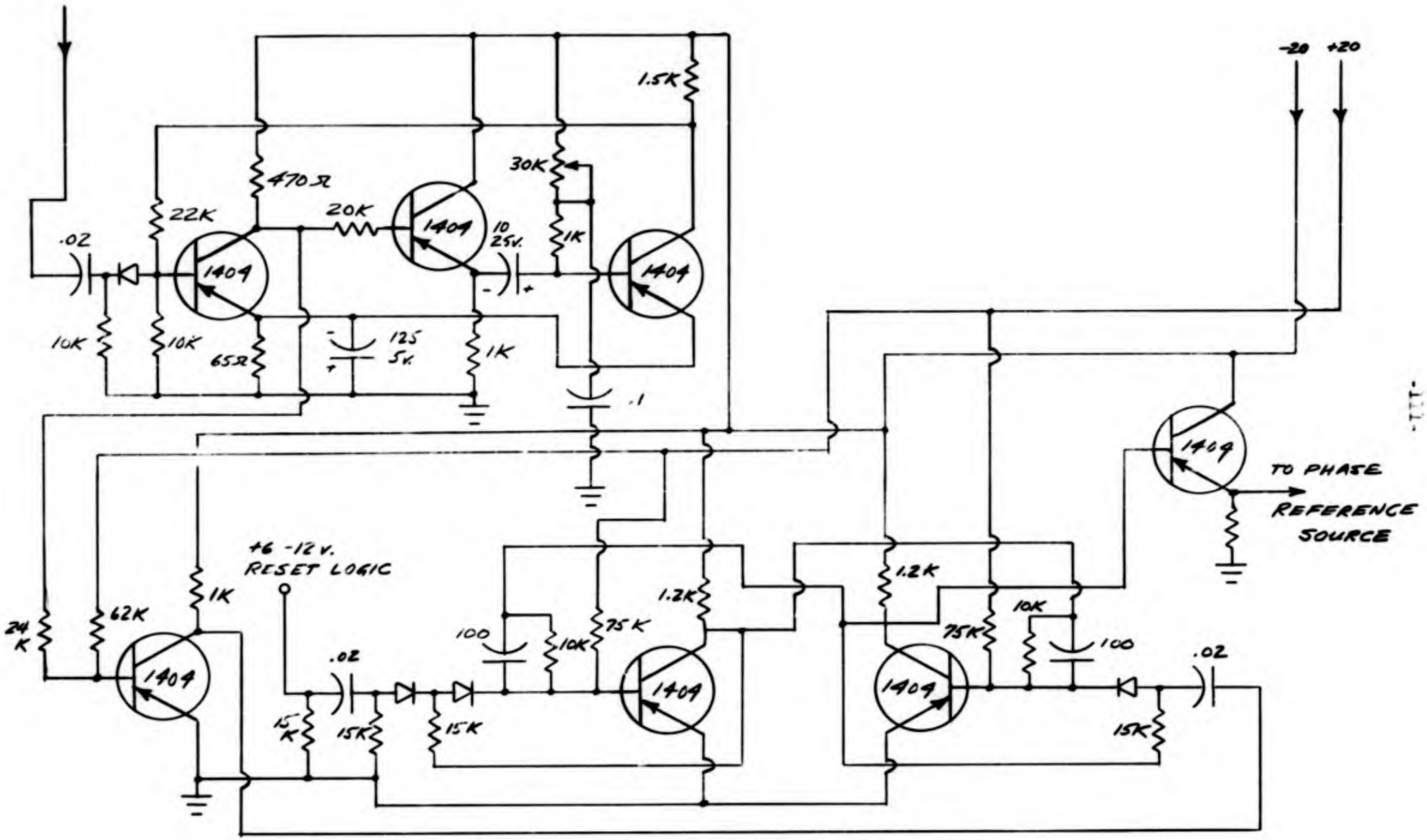


FIG. 3.9.1 : REINFORCEMENT TIMING CONTROL (PAGES 110 AND 111)

3.9 Reinforcement Timing Control

Dwg. No. 8.14 Reinforcement Timing Control

The reinforcement timing control triggers a burst of reinforcement pulses from the reinforcement pulse generator on a delayed signal from the word termination detector. This ensures that the word is reinforced only while it is in registration in the sensory delay channels. In addition, provision is made to freeze the response by cutting off the phase reference pulse to the R-units at some arbitrary time near the end of the reinforcement cycle.

The time at which reinforcement begins after the end of the word has been signalled, t_1, may be adjusted in the 10 to 100 ms range. The duration of the reinforcement burst, t_2, is variable from 10 to 200 ms. The freezing of the response occurs t_3 ms after the end of the word; t_3 is adjustable from 10 to 300 ms.

The circuit, shown on fig. 3.9.1, consists of three monostable multivibrators, and the response freezing flip-flop. The flip-flop acts on an early stage of the phase reference pulse generator; it may be reset by the overall clear-reset button on the control panel or its equivalent in the AUTOMATIC mode. Single shot t_2 turns on the first pulse stage of the reinforcement pulse generator through a buffer stage.

Controls for the three time settings are available in the control room; they may be adjusted with the aid of an oscilloscope display which shows the relative lengths of the time intervals on a pushbutton command.

CHAPTER 4 AUXILIARY LOGIC

4.0 Introduction

Dwg. No. 11.0 Auxiliary Logic

The digital logic in Tobermory serves to control and display the information flow into and out of the perceptron itself. While none of the logic is really indispensable to the operation of the machine, its absence would render all sustained experimentation exceedingly cumbersome.

The block diagram of figure 4.0.1 describes the major paths of information flow. In the MANUAL mode of operation, the microphone is used as input, and the output, as well as certain auxiliary functions relating to internal conditions in the perceptron, are read off the various display panels in the control room, or responses may be printed by pushbutton command. In the AUTOMATIC mode, a magnetic tape provides the input, and an electric typewriter prints out the obtained response and a few additional items. The tape contains a recording of the word (or other audio pattern) to be identified on one channel, and the desired response, and typed comments, or a heading, on the other. The heading, and information pertaining to which R-units have been reinforced, are printed along with the desired and the actual response. In the SEMIAUTOMATIC mode, one word at a time will be processed from the tape, on pushbutton command.

The format of the messages on tape is shown on figure 4.0.2. The first item in the message is the desired response code. The second item is the heading; this may be arbitrarily long. In general it will include an identification number, a transcription of the word to be presented, and perhaps instructions to the operator. These two items are recorded directly from the typewriter, without going through a buffer storage. The digital data is followed, on the other channel, by the word itself, spoken on prompting by a signal light. The end of the message is marked by a three second silent period, designed to facilitate backspacing, and to allow the machine sufficient time to process even the longest word without requiring the tape to stop.

The print-out format is shown on figure 4.0.3. This figure is self explanatory.

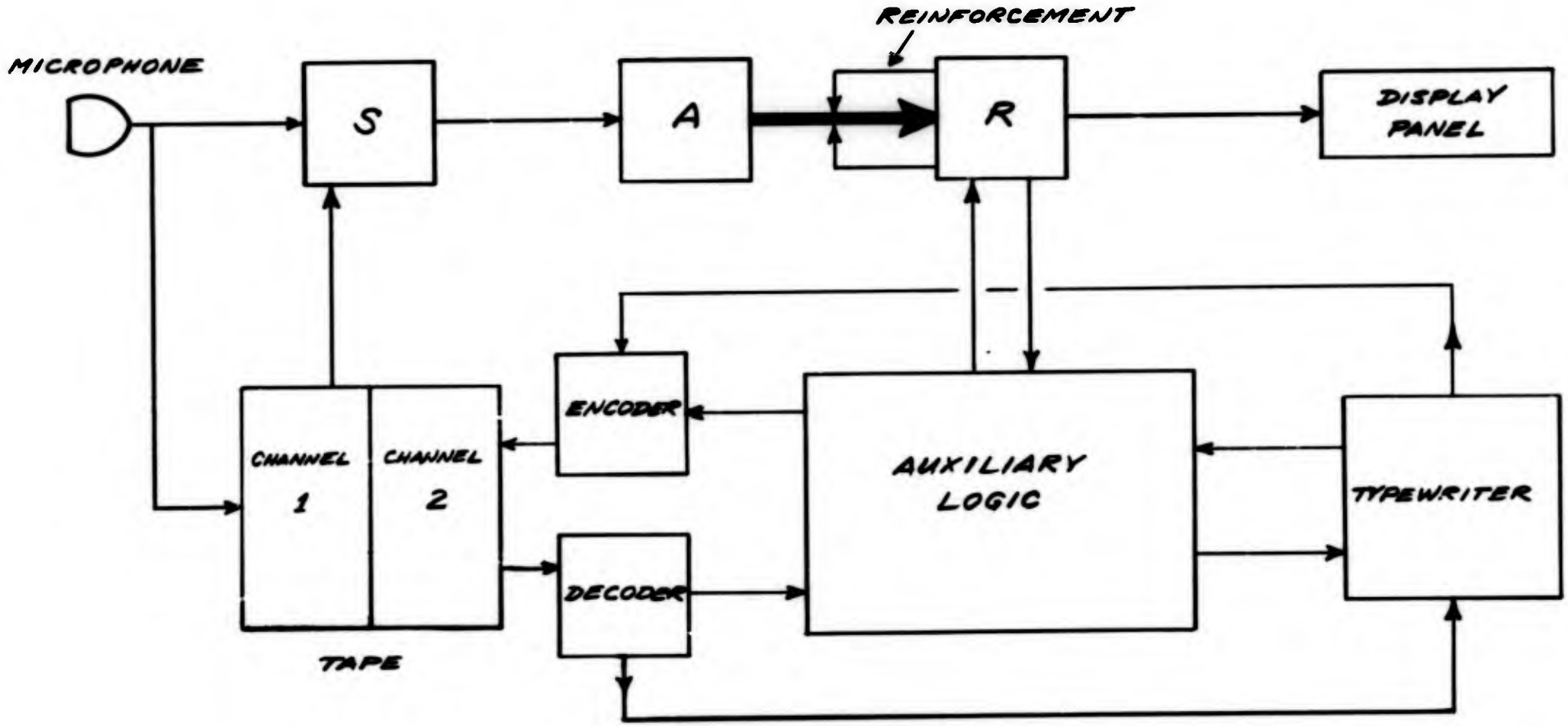


FIG. 4.0.1: FLOW OF INFORMATION IN TOBERMORY SYSTEM

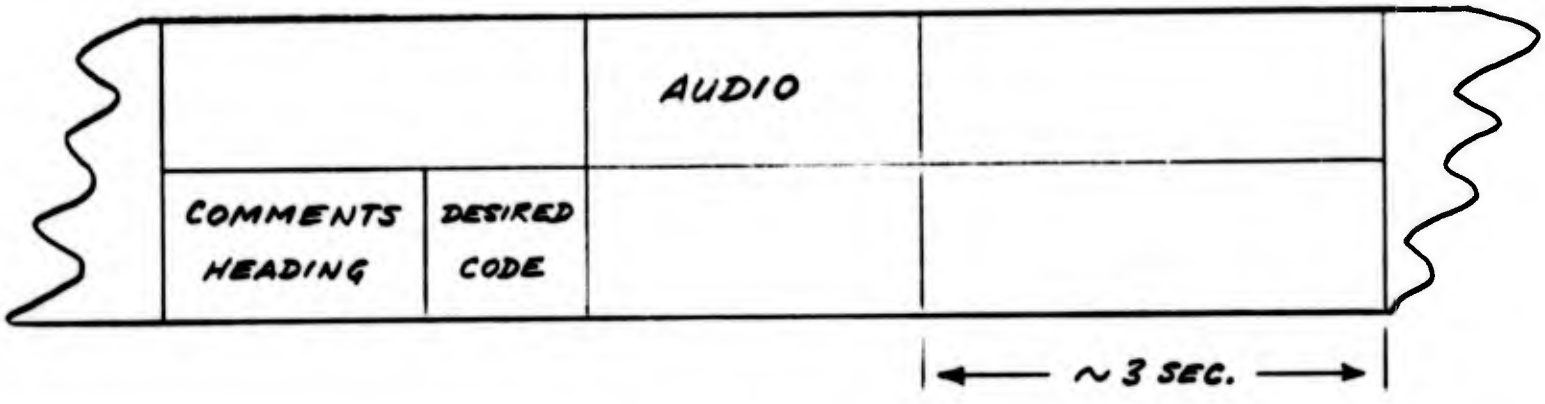


FIG. 4.0.2 : MESSAGE FORMAT ON TAPE

```
101  000  110  010          <- DESIRED RESPONSE
101  100  101  010          <- ACTUAL RESPONSE
     X    X         X       <- REINFORCEMENT OCCURRED
                               (X'S TO BE PRINTED IN
                               ERROR POSITION)
COMMENTS
110  110  001  101
110  110  001  101

MORE COMMENTS
001  101  000  100
000  111  010  011
  X   X    X   XXX  X
THE END
```

FIG. 4.0.3: PRINTOUT FORMAT

4.1 Summary of Logic Circuits for Automatic Control

by

Charles Kiessling

Purpose:

1. To prepare the tape recording to be used by Tobermory. This tape contains:
   - A. Track 1 audio information
   - B. Track 2 digital information
     1. desired R unit code
     2. heading and any other information about that word
2. To recover the digital information from the tape and load the D register.
3. Print out the contents of the D register, print out the response of Tobermory indicating errors between response and desired response. Print out which R units had been re-enforced for that word.

Functions, their operation, inputs and outputs:

Function A

Operation:

1. Converts the 7 bit parallel code into a 7 bit serial code.
2. Encodes typewriter functions into a 7 bit even parity code and then serializes the code.

Inputs :

1. Typewriter
2. Clock pulses from Function D to time serialization.

Outputs:

1. Serialized line to tape modulator
2. Parallel output from register to Function B for decoding "1" and "0".

*The serialized code is separated into a "1" line and "0" line which go to the tape modulator.

Function A acts as an input buffer from the typewriter. It takes the 7 bit typewriter code and stores it in 7 flip-flops. From here the signal is serialized and sent to the tape modulator. It also goes to Function B. The tape modulator which is actually contained within Function A receives the "1" on one line and the "0" on another line. These then produce two pulses of different frequencies.

The logic used to set the flip-flops is actually negative logic. The serialization timing pulses are derived from Function D.

Function B

Operation :

1. decodes carriage return, "1", "0".
2. the "1" and "0" are used to load function J (D register).
3. start and stop tape recorder.
4. Count number of words learned or tested.

Inputs:

1. Typewriter
2. Function A supplies the 7 lines for the "1", "0" signals
3. Timing control comes from Function E.

Outputs:

1. Tape recorder motor control
2. to Function J loading D register
3. Advance line to Function C.

Function B is used to decode the "1" and "0's" from the typewriter, then load them into the D register. The cycle is started by a carriage return which then allows the next 12 "1's" and "0's" to enter the D register. Any other character from the typewriter is ignored.

A second carriage return shuts off the line to the D register and starts the tape recorder. The timing for this comes from Function E and the D register loading location is timed by Function C.

Function C

Operation:

16 position counter and decoding circuits determine which position of D register is to be loaded next.

Input:

Advance line from Function B

Output:

14 lines to D register (Function J).

Function C consists of a counter that can count to 16 although it is only used to 12. These determine which of the 12 positions is to be entered in the D register during the loading of the D register by Function B. The 4 position counter is decoded and one of the lines is known as AAF which originated in Function B.

Function D

Operation:

Ring that is started by typewriter, develops timing pulses for Function A.

Input:

1. Typewriter
2. Master clock

Output:

Timing pulses for Function A.

Function D is a ring circuit which is started by the typewriter operation pulse which is synchronized with the master clock (C_8). The output of this ring is used to serialize the data stored in Function A.

Function E

Operation:

Ring that is started by typewriter, develops timing pulses for loading D register

Input:

1. Typewriter
2. Master clock

Output:

Timing pulses to Function B and C.

The timing control for Functions B and C are obtained from this ring. This ring is started by the character operation pulse which is synchronized with the master clock (C_6).

Function F

Operation :

System Reset.

1. Provides timing for quiet tape after each word when making tape recording.
2. Provides waiting time after each word.
3. Generates reset pulse to:
   A. Initialize logic circuits at turn-on time
   B. Reset logic circuits after each word

Inputs:

1. Manual push button
2. End of word detector

Outputs:

To any and all flip-flops that have to be reset in all functions.

This is the system reset circuit. When an end of word pulse occurs or the system reset button is pushed, a reset pulse is generated. This is also a 1/2 to 3-1/2 second delay circuit which is used to space extra tape when preparing the tape at the end of each record.

Function H

Operation :

Back space from typewriter starts 16 count counter and moves the contents of the D register serially to the tape modulator.

Inputs:

1. Typewriter
2. Master clock

Outputs:

1. D register contents
2. Indicator lights, time to say word to be recorded.
3. Microphone control (on/off).

When a back space is detected the contents of the D register are sent to the tape modulator. The purpose of Function H is to count 16 pulses to shift out the contents of the D register. After that it turns on the microphone and lights an indicator light telling the operator it is time to say the word.

Function J

Operation:

1. In making a tape recording the D register is loaded in a parallel/serial manner from the typewriter. Later it is sent to the tape modulator.
2. It is loaded serially from the tape in normal automatic operation.
3. In manual operation the contents of the D register will agree with the console push buttons. This is to allow the typewriter to print the D register even in manual operation if desired.

Inputs:

1. Function C during tape-making
2. Function P from tape recorder
3. Manual push buttons.

Outputs

1. To Tobermory R units
2. To indicator lights

This is the D register. It has 16 positions numbered from D_0 through

D_{15}. D_1 through D_{12} contains the information related to the R unit coding. $D_{13,14}$ are not used this time. D_0 and D_{15} are always set to a "1". This is so that when loading the D register from the tape a check of D_0 and D_{15} will indicate the register is full when they both have a "1". This register may be loaded in several ways: (1) From the 12 position buttons on the console, (2) From the typewriter and (3) Serially from the tape recorder. Each position of the register has the following connected to it: an indicator on both the "1" and "0" side of the flip-flop to the typewriter desk, an indicator on the "1" side to the main console and a relay on the "1" side which is also driven by an indicator circuit. This relay is the Tobermory D register component.

Function K

Operation:

6 bit buffer between typewriter and tape recorder with power drivers to drive the typewriter.

Inputs:

1. Function R from tape recorder
2. Function S
3. Reset from typewriter

Outputs:

6 lines to typewriter

Function K is a 6 position register that drives the typewriter in printing. The only code that will not activitate the typewriter is all "0's". Whenever information is in this register the typewriter will immediately type it. The operation pulse from the typewriter is then used to reset the register to "0". The register has only 6 positions since the parity bit check is not used during printing.

Function L

Operation:

Master clock, generates primary source of all timing pulses.

Input:

100 Kc sine wave

Output:

Pulses with cycle time $(10x10^{-6})\cdot(2^{n})$ where $0 \leq n \leq 13$

The master clock uses a 100 Kc oscillator which will probably come from the oscillator in Tobermory. This is passed through an And/Or circuit and fed into a 13 position binary counter. At each position, if required, there is a driver which provides the rest of the system with clock pulses at the correct timing.

Function M

Operation:

Controls the timing for the printing by the typewriter by supplying 16 pulses during printing cycle.

Input:

Phase control lines from Function N

Output:

1. 16 lines to Function S
2. Pulse to cause carriage return.

In printing out the R, A, and D registers timing for the typewriters must be provided. The pulse for carriage return and the printing of the 12 characters is controlled by this function. The lines T_1 through T_{15} originate here. They are advanced at a rate of C_{13} from the master clock. When each of these registers is printed out a carriage return is required to reset the typewriter, followed by 12 pulses for the 12 characters and 4 pulses for spacing after every 3 characters. This makes it easier to read.

Function N

Operation:

Seven flip-flops which indicate which of seven phases the logic is currently in.

Input:

1. System reset
2. Carriage return
3. Back space
4. Function J indicating D register is loaded
5. Printing control indicating
   a. D register has been printed
   b. A register has been printed
   c. R register has been printed
6. Tobermory has reached steady state
7. Cycle is over.

Outputs

1. To Function M
2. To Function S
3. To Function P

In order to separate the different states that the logic may be in, there is a phase control circuit. It can be in any one of 8 states. When the conditions arise to enter a new state a single shot is turned on, which sets all the 8 flip-flops to "0" and following this another single shot is combined with incoming conditions to set one flip-flop into the "1" state. A few of the inputs require knowing what state you are in and since this is lost when all the flip-flops are reset, these lines have single shots to momentarily store the state of the input. There is a rotary switch and push button which will allow manually putting the machine into any desired phase.

Function P

Operation:

"1" and "0" come from the tape demodulator. A bit count check

clears the register (Function F) if the number of pulses is in error. In phase 2 the output of the tape demodulator is sent to the D register.

Input:

1. From tape demodulator
2. Phase control (Function N).

Output:

1. To D register
2. To shift register (Function R).

The output of the tape demodulator enters the logic at this point and for the type-written information a parity bit check is made and a pair of single shots are used to determine whether or not stray noise has entered the system. If an error is detected with the parity check or the single shot timing, Function R is automatically reset. This may cause some trouble for one or two characters, but the system will eventually reach a corrected condition and operate properly afterwards. The parity check and single shot check are disconnected when the D register data are arriving.

Function R

Operation:

Receives the tape output from Function P and holds it for short time ($\sim$ 1 ms) before being reset. The contents are decoded for backspace, carriage return, space and tab. The characters are sent in parallel to Function K.

Input:

1. Data pulses from Function P.
2. Resets from
   a. system
   b. typewriter
   c. parity check

Outputs:

1. To Function K
2. To carriage return, tab, space, back space

Function R is a 9 position shift register. When a pulse arrives from the tape demodulator and Function P it enters one end of the register. This position is considered the high order position of the register. In the reset condition of the register the next to the highest order position is set to a "1" and everything else to "0". When the register fills, the lowest order position should have a "1" in it. If it does not, some bits were lost. The output of the lowest order position is fed into a single shot check in Function P. Of the possible single errors it is impossible to detect an extra "0" added to the character where the lowest order bit of the character was a "1". In that case the parity check will be correct and a "1" will exist in the lowest order position of this register. Other errors of lost bits or extra bits will be detected. The output of this register when there is an odd parity check is sent directly to Function K. If it has an even parity check it is decoded into one of the typewriter functions.

Function S

Operation:

Serialize the contents of the D, R, and A registers for print-out. If a "1", print a "1". A "0" is detected logically by comparing the phase, timing and register location. The R register is compared to the D register bit by bit, if they agree a "1" or "0" is printed, if not, an X is printed at that position and at the end of the line. The print out format is 3 characters, space, 3 characters, space, etc.

Input:

1. From the D, R, and A registers
2. Timing from Function M
3. Phase control from Function N

Output:

Coded lines to Function K.

This function involves sensing D, A, and R registers and printing

their contents with the typewriter. If a "1" or "0" is found in the D or A registers, it is printed as such. The R register is compared bit by bit to the D register. If they agree, a "1" or "0" is printed. If they do not agree, an X is printed and at the end of the line there are two spaces and an extra X printed indicating an error in that line.

In order to sense just the "1" side of each position in these registers it is necessary to evaluate logically each bit as to whether it is a "1" or "0". If at one of the times T_1 through T_{15} a "1" is encountered in a position of a register it is printed as a "1". If at that time there is not a "1" but the printing clock Function M is running and it is not time T_4, T_8, or T_{12} then it is considered a "0" and a "0" is printed. Times T_4, T_8, and T_{12} are the times when a space is printed.

In printing the R register the comparison is made to the D register and the same analysis as to whether it whould be a "1" or "0". If an error occurs a flip-flop records this and at the end of the line the extra X is printed. The "1", "0" and X are sent to Function K where they are encoded into the typewriter code.

Function T

Operation:

Detects that D register has been loaded from tape and unshorts the audio input to Tobermory.

Input:

1. Phase control
2. D register

Output:

To shorting relay in Tobermory

Function T senses that the D register has been loaded from tape and unshorts the audio input into Tobermory.

Summary of Tape Preparation:

The procedure is as follows:

1. At start of operation, press system reset.
2. Press carriage return. This is a control operation and important.
3. The next 12 "1's" and "0's" typed will enter the D register; typing anything else will just be ignored. After the 12 bits for the D register have been typed, or if you are not using all 12, push button carriage return again.
4. This shuts down the input to the D register and starts the tape recorder moving.
5. A message of any length may now be typed, such as headings, the date, etc., and the carriage return may now be used as a normal typing operation when the heading is finished.
6. Press the back space key. This will transfer the contents of the D register to the tape. When this is done (it takes a fraction of a second) a light will light and
7. the operator will now say the word to go on the tape.
8. Following the end-of-word detection the tape recorder will continue for 1/2 to 3-1/2 seconds depending on how it has been set by the operator.
9. The tape will now stop and the operator may go back to step 2 and repeat the process for the next record.

If an error has been made while loading the D register before the tape is running, it may be corrected by hitting system reset and starting at step 2 again. If an error is made while the tape is running, just keep going since this will only affect print-out and result in a misspelled word.

CHAPTER 5 POWER SUPPLIES

Dwg. No. 2.5 General Power Distribution Schematic

The heterogeneous nature of the electronic circuitry required to implement the Tobermory perceptron necessitates the existence of a large number of separate power supplies within the machine. The function of each power supply, and the procedure for turning the machine "on" will now be briefly described. Subsequent sections of this chapter contain detailed descriptions of the various power supplies.

The primary source of power is the three phase four wire 208 V. 60 cps line from the Hollister Hall transformer room. In event of an emergency, all power to the machine may be cut off by pulling the lever on the central Square-D box on the North wall of the Laboratory. Under normal conditions, the machine is turned "on" and "off" by means of the master power switch in the control room. In addition, each separate power supply, and the 115 V. a.c. outlet, may be turned off by means of individual switches located in the control room.

The main power supply is a 5 Kilowatt low voltage d.c. unit with taps at -20V., -10V., +10V., +15V., and +20V. It provides power for all the transistors in Tobermory, except for special systems such as the logic blocks, and the reinforcement pulse generator.

The logic supply is the source of -12V., -6V., +6V., and +12V. bias for the auxiliary logic. These voltages were selected because of the availability of a complete logic system designed for these levels. The conversion of the logic system to 10-20V. operation was rejected in order to save engineering time. A -45V. supply for the IBM Selectric typewriter is also associated with the logic supply.

The log reference supply is an adjustable regulated supply providing the breakpoint voltages for the diode-resistor approximations to the logarithmic curve.

The trigger and reinforcement pulse generators have their own -25V.

Sola power supply. They have, in addition, a tap to the -6V. line. In the event of the machine being turned on for manual operation before the installation of the logic supply, a battery may be substituted here. The power drain off the 6V. source is negligible.

High voltage supplies are required only by the A.G.C. amplifier and by the A-unit test jig. Other pieces of equipment using tubes have their own internal power supplies.

All the above supplies, with the exception of the main power supply, operate directly off an unregulated 115 V.a.c. line. 115 V. is required also for the fans, the noise generator, the Eico amplifier, the signal generators, and the tape recorder.

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