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FOR

COMPLEMENTARY METAL OXIDE SEMICONDUCTOR

VERY LARGE SCALE INTEGRATION

THESIS

AFIT/GE/ENG/84D-41   Brian T. Kelley
                           Captain   USAF

DTIC
ELECTE
APR 9 1985

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DEPARTMENT OF THE AIR FORCE
AIR UNIVERSITY
AIR FORCE INSTITUTE OF TECHNOLOGY

Wright-Patterson Air Force Base, Ohio

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AFIT/GE/ENG/84D-41

SPEED-UP TECHNIQUES

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Presented to the Faculty of the school of Engineering

of the Air Force Institute of Technology

Air University

in Partial Fulfillment of the

Requirements for the Degree of

Master of Science

by

Brian T. Kelley, B.S.

Captain   USAF

Graduate Electrical Engineering

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Preface

Documentation of techniques for increasing the speed of MOS circuits, evaluation of a specific technique and application of the technique to existing and newly designed CMOS/SOS circuits were performed. A 4x4 bit RAM, 2x4 decoder, two registers and read/write control logic were designed and the precharge speed-up technique was evaluated and simulated using SPICE2, to determine if it actually increased the operating speed of circuits to which it was applied. A methodology was determined for applying precharging to existing circuits through application to a previously designed portion of a CMOS/SOS ALU and to the newly designed circuit elements mentioned above. Extensive SPICE2 simulation indicated that precharging does increase circuit operating speed, but must be selectively applied.

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List of Symbols

V_{T_N} threshold voltage for n-type transistor

V_{T_P} threshold voltage for p-type transistor

C_{be} base-emitter bipolar transistor capacitance

C_{bc} base-collector bipolar transistor capacitance

R_b bipolar transistor base resistance

     bipolar transistor barrier voltage

τ_d time delay of bipolar transistor

β_o large signal current gain of bipolar transistor

     corner frequency of bipolar transistor frequency response

C_D bipolar transistor diffusion capacitance

r_{bc} bipolar base-collector resistance

D D factor

I_{B2} initial base current

I_{B3} final base current

τ_s recombination time associated with excess charged stored on the base of a bipolar transistor

C_L load capacitance

T_L depletion mode transistor

T_D pull-down transistor

τ_L time delay of depletion mode transistor

τ_D time delay of pull-down transistor

β_D gain of pull-down transistor

β_L gain of pull-up transistor

μ_n electron mobility of n-type material

μ_p hole mobility of p-type material

C_i insulator capacitance

V_{ds_N} drain-source voltage of n-type transistor

I_{ds_N} drain-source current of n-type transistor

$V_{threshold_N}$ threshold voltage of n-type transistor

V_{gs} gate-source voltage of n-type material

K_N n-type transistor constant

ϵ_{ox} permitivity of oxide layer

W channel width

L channel length

T_{ox} thickness of insulating oxide

C_{eff} effective gate capacitance

I_P current through the P-type transistor

K_P p-type transistor constant

$V_{threshold_N}$ threshold voltage of p-type transistor

α_N normalized threshold voltage for n-type transistor

α_P normalized threshold voltage for p-type transistor

T_F signal falltime

T_R signal risetime

ch   total driver delay

dr   elementary driver delay

C_L load capacitance

C_G gate capacitance of basic NMOS transistor

$\mathcal{T}_L$ load line delay

$\mathcal{T}_i$ input circuit delay

$\mathcal{T}_D$ total delay for large capacitance line drive circuits

V_{ss} substrate bias voltage

W_{opt} optimum width of crossunder

C_t capacitance of crossunder

R_{xo} sheet resistance of crossunder

R_o output impedance of line driver

C_{xo} capacitance per unit area of crossunder

Abstract

   ─Methods of increasing the operating speed of integrated circuits were investigated and a reference to speed-up techniques was generated. Precharging, a specific method, was applied to existing and newly designed CMOS/SOS circuit elements and evaluated. The SPICE was used for transient signal timing analysis.

   Precharging was applied to a test circuit, the first bitslice of a previously designed ALU circuit and three newly designed chip circuit elements, to determine its effect on the operating speed of each circuit. Precharge configurations of each circuit were then simulated with SPICE.

   The results of this thesis research indicate that precharging can be applied to both existing and newly designed circuits, that it significantly reduces low-to-high signal transition delays, if applied correctly, and, in general, it has a detremental effect on high-to-low signal transitions, and increases the associated delays. In addition, the effectiveness of precharging is dependent on the amount of current applied to the precharged nodes.

I. Introduction

A. Background

1. CMOS Technology

Complementary Metal Oxide Semiconductor (CMOS) technology is characterized by low power consumption and excellent noise immunity, while offering high integration density and rapid circuit switching speeds when compared to other technologies. CMOS originated due to requirements for portable/low power systems for avionics and aerospace applications. Although CMOS has a lower switching speed than some technologies, specifically NMOS and bipolar, and thus a lower maximum frequency of operation, its advantages have made it the emerging technology for both military and civilian applications for Very Large Scale Integration (VLSI).

CMOS circuit performance can be improved as smaller geometries are used. Circuit speed will be improved and power dissipation reduced. However two basic limitations exist; optical printing capabilities, since the wavelength of light provides a lower bound on the dimension sizes used, and the fabrication processes themselves which will call not only for reduced lateral dimensions, but for oxide thicknesses less than 20 nanometers. For these thinner oxides, more "pure" manufacturing elements will be required to maintain a minimum acceptable yield during the fabrication process.

When comparing integrated circuit parameters, layout

density, speed-power product and gate delay are the primary characteristics of concern to the circuit designer. A small speed-power product can result in low power dissipation and rapid circuit operation (associated with gate delay) and higher circuit densities become increasingly important as VLSI applications and requirements become more advanced.

2. Silicon-On-Sapphire (SOS)

SOS technology uses sapphire as a substrate in place of silicon in the basic MOS fabrication process. SOS has increased in popularity since it offers the highest speed power product of any silicon technology and can compete with any other silicon technology in packing density. However, the cost of the sapphire substrate has limited its use primarily to military systems where its additional advantage of low susceptability to radiation effects is of critical importance. Optimum performance is obtained when SOS is used with CMOS devices, where power consumption is minimal and noise immunity is excellent. Speed can thus be increased since the parasitic capacitance that exists when a silicon substrate is used doesn't exist when sapphire is used. SOS processing requires only a third of the steps required for silicon substrate (bulk CMOS) and is less susceptible to mask and oxide defects.

3. Factors Influencing Circuit Operating Speed
The two factors contributing to the speed of a circuit

are: capacitance and resistance. Capacitance measures the amount of charge that must be provided to a unit of area before the voltage changes and resistance is a measure of the ease with which current can be supplied to this given area. The values of the resistance and capacitance of certain materials and circuits is dependent on both the size (length and width) of the materials used for a specific application and on the process that is used for fabrication of the circuit or chip. To increase the speed of the circuit, the resistance or capacitance (or both) must be reduced to minimize the resultant RC time constant delay. The following data reviews some of the various approaches used to affect speed changes in integrated circuits.

a. Fabrication Materials

Lower loading capacitances have been achieved using insulators such as sapphire and gallium arsenide in place of silicon for IC substrates. Use of sapphire has resulted in higher clock frequency operation in large scale integrated circuits and is believed to be based on the reduction of long interconnect capacitances in data buses and control lines. Medium scale integrated circuits using gallium arsenide substrates have shown to have overall higher switching speeds. Yuan et al [1], provided test results upon comparison of silicon to both sapphire and gallium arsenide substrates. Their studies indicated that for line widths greater than 2.5 microns, substantial

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capacitance reduction could be achieved by use of sapphire and gallium arsenide substrates. Propagation over inter-connect lines with greater than 2.5 micron widths have shown these positive results but little data is available on line widths below this 2.5 level.

b. Fabrication and Processing

Dennard et al [2], have accumulated data on the optimization of silicon gate MOSFETs for high performance logic applications for both room temperature and liquid nitrogen temperature operating environments. The principal factor affecting their success has been the optimization of ion-implant techniques that have been able to achieve lightly doped substrates, resulting in shallower junctions for minimizing lateral diffusion under the edge of the gate and the field oxide. Strict control of doping has permitted fine adjustment of device and field region thresholds.

New developments in lithographic and etching techniques have resulted in reduced feature size. An expected increase in speed is associated with any reduction in feature size, however this has been found to hold true for only small (low density) circuits. As the size of a circuit increases due to its complexity, the density of the chip per given unit area increases. Since feature size reduction results in less cross sectional area for line widths, hence reduced drive current capability, the effect of reducing the feature size with an increase in the density of the chip, is

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expected to increase time delays. Device performance is no longer expected to be the primary source of delay since the individual transistors are expected to switch more quickly, however interconnection delays are expected to dominate the delay times. The distances that a signal will need to travel will be greatly increased relative to the feature sizes of the circuits themselves.

c. Circuit Design and Layout

From the previous information, it appears that improvements in the manufacturing processes are going to continue to have a significant effect on the performance of integrated circuits. However, circuit design methods can be a more flexible approach to increase the speed of circuits. The circuit designer can modify an existing design or incorporate specfic techniques into an original design as part of a routine design procedure, to attempt to overcome or at least reduce the RC time delay within the circuit.

"Bootstrapping", "charge pumping" and "precharging" are terms used among circuit designers and rarely refered to within available design literature, to refer to circuit modifications and "hybrid" type circuits used to increase a circuit's operating speed. The distinct lack of data concerning these topics in technical publications and other literature implies a reluctance by circuit designers to disclose their personal "tricks" of the trade due to profes-

sional (competitive) as well as other reasons.

In some cases, however, even though a particular method may be frequently used and refered to by both individuals and literature, no quantitative performance data in support of this particular speed-up approach is presented or is otherwise made available. As a result, the reader is left with only the author's interpretation of the success of the method and must speculate on its applicability to other circuits.

B. Problem Statement

The purpose of this thesis is to investigate and collect data on various techniques developed and implemented to increase the operating speed of electronic circuits, and to select a specific technique and demonstrate its applicability to CMOS technology for VLSI applications by determining the extent to which the circuit speed is actually affected by the speed-up technique.

At this time, the only CMOS research performed at AFIT was performed by Capt. W. Sommars, GE-83D, in his thesis [3] which developed a CMOS/SOS cell library. Since AFIT interest is primarily in SOS technology, this thesis will involve only CMOS/SOS and will make use of the existing SOS library.

Since time will not permit fabrication of the actual chip and subsequent testing, a simulation will be performed to determine the performance of the circuitry. However, the

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data package required for fabrication will be completed and sent to MOSIS. Additional thesis work can then be generated to test the chip.

This thesis is intended to provide the VLSI circuit designer with a consolidated source of information on the analysis of circuit signal delays and a reference to specific methods that may be used to increase the operating speed of ciruits under design. Much of the available literature refers to and uses specific speed-up techniques, but the impact of the technique on the circuit's performance is often assumed rather than specifically evaluated. This project will also provide an evaluation of a specific technique to prove or disprove its inherent worth for application.

A secondary objective of this thesis is to actively use the CMOS/SOS library previously designed by Sommars [3] and extend the AFIT knowledge base in the CMOS/SOS area.

C. Assumptions

The following asssumptions were made to limit the scope of this project:

    1. The reader has an extensive understanding of the VLSI CAD tools at AFIT

    2. The reader has a basic understanding of circuit theory and transient signal analysis

    3. The reader is familiar with Metal Oxide

Semiconductor devices

D. Approach

The following approach was used for this thesis:

1. Evaluate transient switching as it pertains to bipolar, MOS and CMOS circuits.

2. Evaluate the existing CMOS/SOS library and become familiar with SPICE2, a circuit simulator

3. Perform a literature search for "speed-up" circuits and techniques

4. Apply precharging to the first bitslice of Sommars' CMOS/SOS ALU

5. Run a SPICE simulation on the modified bitslice and the original ALU bitslice and compare the timing results

6. Design a Memory/ALU Bitslice circuit modified ALU and apply precharging to it where possible

7. Design additional library cells as required to support the Memory/ALU Bitslice circuit design

8. Run a SPICE simulation on the Memory/ALU Bitslice circuit with and without precharging applied and compare results

9. Design chip layout

E. Sequence of Presentation

Chapter II provides a review of basic CMOS circuits.

Chapter III continues with a review of transient timing analysis for bipolar, MOS and CMOS circuits. A review of bipolar transistor timing is included to facilitate the timing review, since most practicing engineers are more familiar with timing analysis as it applies to the bipolar transistor than to the MOS transistor. Chapter IV provides data on speed-up techniques and circuits that can be applied during the design process and presents the criteria for selection of precharging as the technique evaluated during this thesis. Chapter V presents the system designs for the modified CMOS/SOS ALU Bitslice and for a Memory/ALU Bitslice circuit that demonstrates an application of the modified ALU bitslice and the use of precharging in a larger circuit. Chapter VI presents the detailed design of the circuits described in Chapter V. Chapter VII presents a comparison of the results of a SPICE2 circuit simulation on a test circuit, and the modified and unmodified ALU bitslice circuits. Chapter VIII provides this authors conclusions and recommendations for future projects.

II. CMOS Review

The following sections provide a review of basic CMOS circuits.

A. The basic CMOS element is a series combination of an N-type and a P-type metal oxide semiconductor transistor as shown below in Figure II-1.
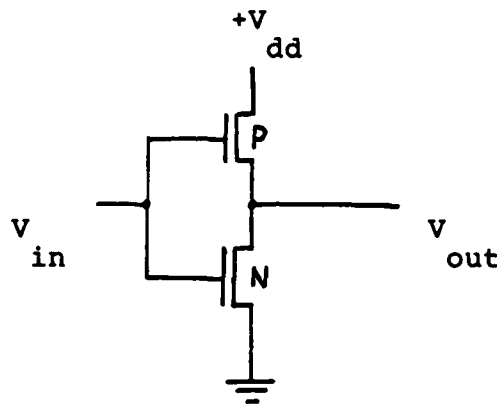
Figure II-1. CMOS inverter.

This circuit performs a logical inversion function. A metal oxide semiconductor transistor is a device in which the current in a channel between two electrodes, referred to as the source and drain respectively, is modulated by the voltage applied to a third electrode, referred to as the gate, which is physically separated from the source and drain by an insulating material. In the N-type transistor, the majority carriers are electrons so that positive voltage on the gate will increase the conductivity of the channel. For gate voltages less than an established minimum positive threshold voltage, the channel is cut-off and no appreciable drain current flows. The operation of the P-

type transistor is similar to the N-type however, the majority carriers are holes and the operating voltages of the P-type device are negative. The threshold voltages for either type transistor can be controlled by the impurity doping level of the channel during fabrication and is therefore a design parameter of the transistor itself.

The basic operation of the circuit of Figure II-1 is as follows: if V_{in} is at 0 volts, the P-type transistor is biased on by a negative gate-to-drain voltage and the N-type transistor is cut-off by a zero gate-to-drain voltage. The output of the inverter then approaches $+V_{dd}$ (the supply voltage), since the N-type transistor causes an "open circuit" to exist between the output and ground when it is cut-off. If the input voltage is increased, the current in the N-type transistor rises and the current in the P-type transistor falls. The input voltage at which the two transistors are in the constant current region at the same time marks the active operating region of the inverter circuit. As the input voltage increases beyond this point, the output voltage falls to zero. Therefore for an input voltage at or near the value of the supply voltage, the N-type transistor will be turned on, bringing the output of the inverter to ground potential and the P-type transistor will be cut-off.

For either output state, the total current flow results from the equivalent of a cut-off transistor since either the N-type or the P-type transistor will be in cut-off

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permitting near zero current flow. This is the principal advantage of using CMOS technology, since low current flow results in low power dissipation. Current flows in the CMOS circuit only during high to low or low to high transitions as the circuit passes through the active operating region of the transistors.

In order for one or the other of these transistors to be turned off when the input is either high or zero, the threshold voltages for the N-type and P-type transistors must be positive and negative respectively so both transistors must be enhancement mode types for correct circuit operation. A transfer characteristic for the basic CMOS inverter is provided in Figure II-2. Where V_{T_P} and V_{T_N} are the respective threshold voltages of the p-type and n-type materials.
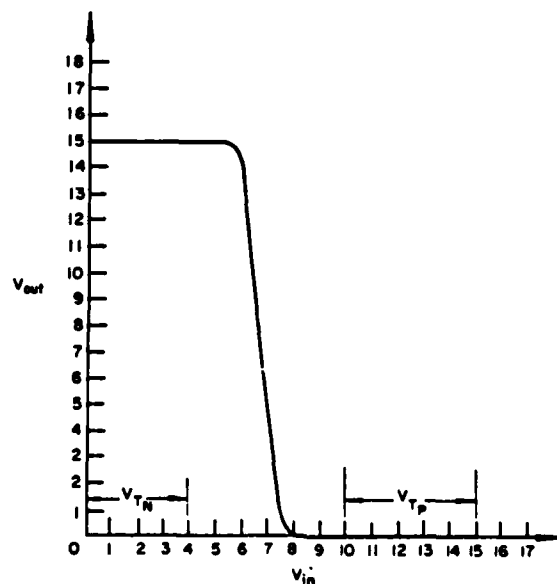
Figure II-2. Transfer characteristic for
CMOS transistor inverter [4].

The single CMOS inverter may be extended to provide NAND and NOR applications as illustrated in Figure II-3 and Figure II-4.
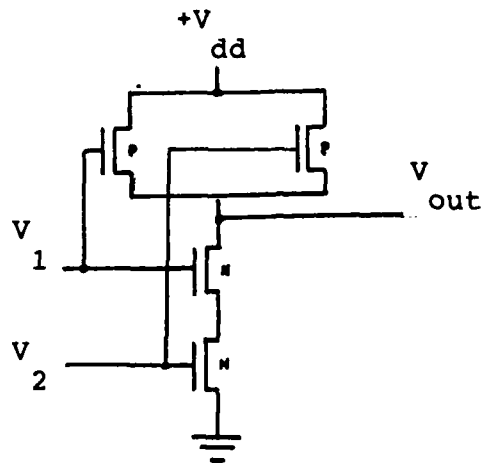
Figure II-3.   CMOS NAND circuit.
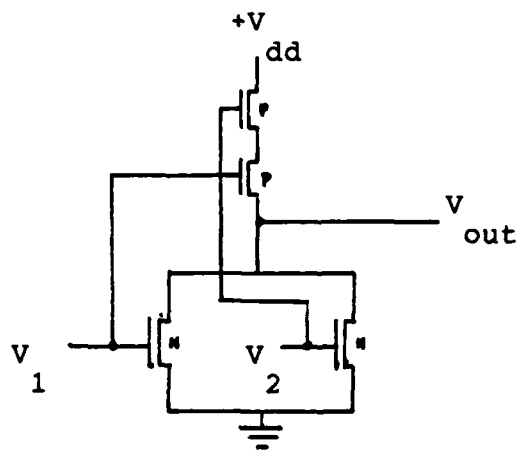
Figure II-4.   CMOS NOR circuit.

In the NAND configuration, when all inputs are high, all N-type transistors in series are in a conducting mode while all P-type transistors are in cut-off. The line to ground is closed and the output is low. In the NOR configuration,

if any one of the inputs is high, the output will be shorted
to ground.

B.   Four characteristics must be considered if a
specific transistor technology is to be used for design:

        1.   Speed of operation

        2.   Power dissipation/consumption

        3.   Ease of designability

        4.   Ease of integration

CMOS dissipates very little power as already stated, but is
not the fastest transistor technology. However, measures
can be taken to speed up its operation. This is the primary
effort of this thesis.

Ease of designability and integration then become
primary driving factors in the choice of a specific
technology. Conflicting opinions exist over the integration
capability of CMOS circuits since proponents of other tech-
nologies contend that twice as much area is required for
CMOS applications since both a P-type and N-type transistor
is required to implement even the most simple inversion
function, as compared to NMOS technology for instance, where
a smaller transistor/load transistor pair can be used for
the same function. However, Krambeck et al [5] have
developed a new approach in CMOS requiring the use of only a
single P-type device with mulitple N-type devices in their
domino logic cirucit. This approach has considerably reduced

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the requirement for chip area and threatens the design

community's universal acceptance of the factor of two

increase in chip real estate when using CMOS technology.

From the data available, CMOS is on an equal ranking with

other technologies as far as ease and flexibility of design

are concerned. CMOS offers standard cells for design that

leave the problem of compactness and density of design as a

function of the state-of-art as in the case of Very Large

Scale Integration (VLSI) applications, and as a function of

If CMOS is selected as a transistor technology to be used

for design, two basic types exist, CMOS bulk and CMOS

Silicon-On-Sapphire (SOS). Table I-1 provides comparison

data on the advantages and disadvantges of bulk versus SOS

[1].

TABLE I-1

CMOS/SOS versus CMOS Bulk

Advantages of CMOS/SOS	Disadvantages of CMOS/SOS
Lower parasitic junction capacitance	Parasitic edge leakage
Lower power dissipation	Back channel leakage
Lower propagation delay	Floating substrate
Higher packing density	- ChargeStorageeffect
Higher packing density	
Higher punch through voltage	Reduced mobility - N channel
Reduced junction shorts	Sapphire variability
Radiation hardened	Thermal conductivity
Reduced "soft" errors	Wafer Breakage -
Reduced Latch-up	Thermal shock
Good scaling	Commercial viability
Tolerant to Parameter variations	
Simplicity of design	
Mixed technologies	

CMOS/SOS is characterized by better ease of design, better control of threshold and punchthrough voltages, radiation hardness and according to the available data has a factor of two better power dissipation and propagation delay than its bulk counterpart. The fabrication process however causes many of the problems associated with CMOS/SOS. SOS is subject to variable starting material characteristics and planar substrates during processing, floating substrate charging effects and "back-channel" leakage [1].

There is cause for concern among proponents of SOS technology when CMOS is considered for VLSI application. Present predictions and preliminary test results indicate that as feature sizes decrease below the present state-of-the-art (2 micron) that loading capacitances are expected to increase in SOS to the point where bulk and SOS become comparable in performance. Figure II-5 provides preliminary data on loading capacitance as a function of feature size for both SOS and bulk [1].
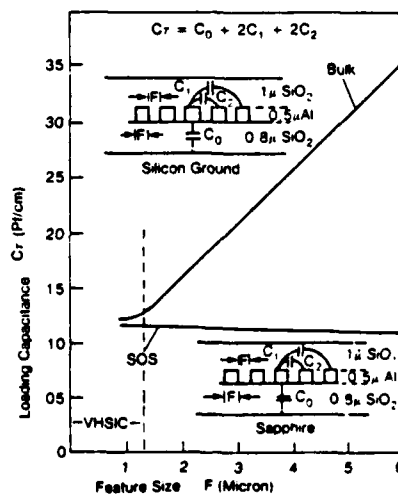
Figure II-5. Loading capacitance vs. feature size [1].

The applications of CMOS in VLSI design is an emerging field, however whether SOS or bulk technology is the most advantageous appears to be a matter of preference at this point in time since present efforts by industry seem to be making bulk and SOS technologies more comparable and the field is a competitive one.

III. Circuit Delay and Timing Analysis

The following sections provide a review of timing analysis with respect to bipolar, MOS and CMOS circuits.

For the reader who is not familiar with timing analysis for basic circuits, this chapter begins with a review of bipolar transistor timing (the most easily understood analysis) and concludes by expanding the basic bipolar concepts to MOS and CMOS devices switching theory and reviews circuit propagation delay.

There are two types of delays that must be evaluated for signals in circuits, switching delays that are characteristic of individual transistors, and propagation delays associated with the transfer of a signal over an interconnection line.

The section on NMOS circuits is intended to introduce the reader to the switching delays associated with MOS devices. A more detailed review is provided in the section on CMOS devices.

1. Bipolar Transistor

The transistor can be used to closely approximate a switch. A simple bipolar transistor is used here for the purpose of simplifying the analysis and is illustrated in Figure III-1.
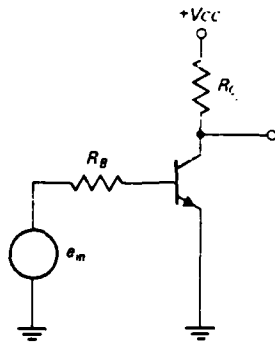
Figure III-1.   Bipolar transistor [6].

Figure III-2 represents the two ideal cases of transistor
operation, as an ideal open switch and as an ideal closed
switch.
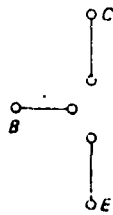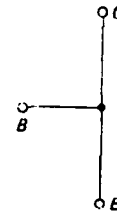
a.   b.

Figure III-2. a.   Bipolar transistor as an open switch
              b.   Bipolar transistor as a closed switch [6].

In Figure III-2a, when the transistor acts as an open
switch, no current flows. When the transistor acts as a
closed switch, shown in Figure III-2b, a high value of
current flows through the transistor to ground. In Figure
III-1, when the voltage on the base of the transistor is

III-2

zero, the transistor is cut-off and no current flows, similar to the ideal open switch case described above, and the output voltage approaches the supply voltage, Vcc. If a large enough voltage supplies enough current to the base to drive the transistor into saturation, then the transistor turns on and approximates the case of the ideal closed switch. Current flows from collector to emitter and the output voltage drops to an effective ground level. During the time that the transistor switches from cut-off to saturation, the transistor passes through its linear operating range. If high speed switching is to take place, reactive effects of the transistor in this region must be taken into consideration. Three transistor equivalent circuits are used when evaluating the switching characteristics of the transistor switch:

    a. Open switch in the cut-off region.

    b. An active region model as illustrated in Figure III-3.

    c. A closed switch in the saturation region

The open and closed switch models have already been refered to.
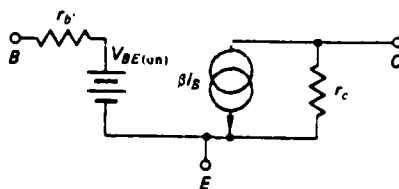
Figure III-3. Active region transistor model [6].

III-3

There are three factors that affect the transition switching times (from high to low or from low to high) of a transistor:

1. Depletion region capacitances causing a delay time

2. Diffusion capacitances and the Miller effect capacitances causing rise and fall times to exist

3. A storage time constant during which time excess base charge is removed before the transistor is permitted to drop from its saturation region into its active operating region

The response of a common-emitter bipolar switch to a rectangular pulse is shown in Figure III-4.
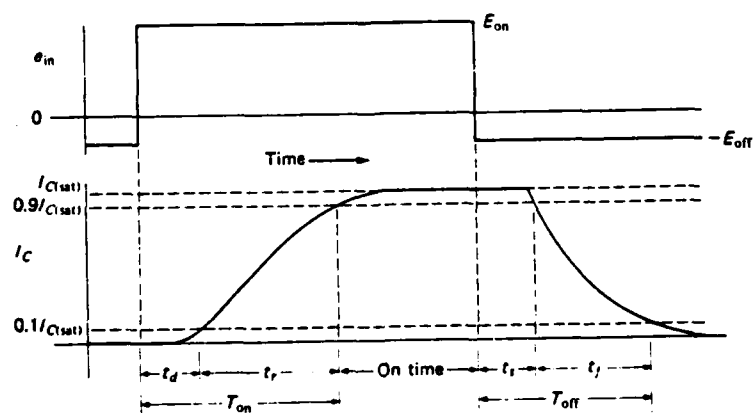
Figure III-4. Input waveform and response [6].

III-4

The waveform is composed of a delay time, a rise time, an on time, a storage time, and a fall time. The delay time is defined as the amount of time required for the waveform to rise to 10% of its peak value after the input changes. The rise time is the time taken for the waveform signal to rise from 10% to 90% of its final value. The turn-on time is the sum of the delay time and rise time. The storage time is defined as the sum of the saturation storage time and the amount of time required for the waveform to drop to 90% of its peak value after the input changes. The fall-time is the time required for the waveform to drop from 90% to 10% of its peak achieved value. The turn-off time is the sum of the storage time and the fall time.

If the input to the base of the transistor is less than the required minimum turn-on voltage of the transistor, then the circuit will be cut-off since no current will flow. If the base terminal is driven with a negative voltage, Voff, for a specified period of time, then it will charge the base-emitter and base-collector depletion region capacitances C_{be} and C_{bc} respectively. If the input voltage is then changed to a positive value, the voltage of the base will not be able to change immediately and will approach the turn-on voltage of the transistor at a rate controlled by the capacitance values C_{be}, C_{bc} and the base resistance R_b. The transistor will not turn on until the minimum turn-on voltage has been achieved on the base. The time lapse between the application of the positive input to

III-5

the base and the time when the transistor actually turns on
is the passive delay time. As the base voltage changes, the
voltage across the depletion-region capacitances changes in
a non-linear manner. For high frequency transistors the
depletion region capacitance is defined as the average
value of capacitance determined from the total change in
charge on the capacitance as the voltage varies from one
value to another, divided by the total voltage change,
and is approximated by the equation [6]:

$$C = \frac{1.5k}{(V'-V)} [(\phi - V')^{2/3} - (\phi - V)^{2/3}] \qquad [1]$$

where ϕ is the barrier voltage, k is a constant, and V and
V' are two different values of voltage. The time constant
of the circuit is:

$$\tau_d = (C_{BE} + C_{BC})R_B \qquad [2]$$

If the initial voltage on the base is $-V_{off}$ and must
increase to V_{on} for the transistor to turn on, then the time
required to reach V_{on} can be determined from a general
charging equation:

$$v(t) = v_i + (v_t - v_i)(1 - e^{t/\tau}) \qquad [3]$$

where v_i is the initial voltage and v_t is the target

III-6

voltage.

The passive delay time can then be solved for:

$$V = -V_{OFF} + (V_{ON} + V_{OFF}(1 - e^{-t_d/\mathcal{T}_d}) \qquad [4]$$

where V_{ON} and $-V_{OFF}$ are the transistor maximum and minimum input voltages respectively as seen by the base then the passive delay is:

$$t'_d = \mathcal{T}_d \ln\left[\frac{(V_{ON} + V_{OFF})}{(V_{ON} - V_{BE(ON)})} \right] \qquad [5]$$

To determine the rise time of the switch, the analysis must include the transition of the waveform through the active region of operation. To accurately perform this analysis the D factor of the transistor must be used. The D factor is given by the equation:

$$D = (1 + \omega_t R_c C_{BC}) \qquad [6]$$

and is a standard form for aiding in representing the total capacitance from base to emitter when a load resistance is applied to a high frequency transistor circuit and is related to the Miller effect capacitance. For more detailed information the reader is referred to Modern Electronic Circuit Design, by Comer [6].

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The minimum base current required to saturate the transistor is:

$$I = \frac{V_{cc}}{\beta_o R_c}$$ [7]

where β_o is the large signal current gain of the transistor. If the transistor enters the active region, the collector current will achieve its final value exponentially with a time constant based on the D factor of:

$$\tau = \frac{D}{\omega_\beta}$$ [8]

where   is the corner frequency of the transistor frequency response and is defined as:

$$\omega_\beta = \frac{1}{r_{bc} C_D}$$ (beta cut-off frequency)   [9]

where C_D is the diffusion capacitance which will vary with the emitter current and r_{bc} is the base to collector resistance.

Turn-off time analysis must consider two cases. The first case is for the fall-time associated with a nonsaturated switch when the base current is greater than or equal to zero and the second case is for a base current less than zero.

III-8

If the base current is lowered the collector current reacts to this decrease with its own exponential decrease with a time constant equal to:

$$t_{OFF} = \frac{D}{\omega_\beta} \tag{10}$$

as given earlier for turn-on delay analysis review.

If the input voltage changes to a negative value, the base-emitter junction will become reverse biased. However, the base voltage will not change instantaneously and a negative base current exists. The negative current will be present until the capacitance is totally discharged, corresponding to the point in time when the collector current reaches zero. The negative base current removes charge much faster and the collector current will reach a zero value much faster than in the previous case. The time required for the collector current to reach zero is the turn-off time of the transistor. The collector current can be represented by the equation:

$$I_C = I_{C2} + (\beta_o I_{B3} - I_{C2})(1 - e^{-t\omega_\beta/D}) \tag{11}$$

and the turn-off time can be determined by setting I_C to zero and solving for t:

$$t = \frac{D}{\omega_\beta} \ln \left[1 - \frac{I_{B2}}{I_{B3}} \right] \qquad [12]$$

where I_{B2} is the initial base current and I_{B3} the final value of base current.

If the base current is greater than the minimum level required to put the transistor into saturation, a decrease in the the base current will not have any noticeable effect on the collector current i.e. no instantaneous changes will try to occur. If the base current is suddenly changed from an overdrive condition to a zero value there will be a time delay associated with the recognition of the change in base current and any noticeable effect on the collector current. The time associated with this "recognition" of a change in base current is the storage delay time and is based on the gradient of minority carriers in the base region. The storage delay is determined by the equation:

$$t = \mathcal{T}_s \ln \frac{(I_{B2} - I_{B3})}{(I_{B(sat)} - I_{B3})} \qquad [13]$$

where $\mathcal{T}_s$ is the recombination time associated with excess charge stored on the base.

Many of these delays can be controlled by the fabrication process, through manipulation of the operating parameters of the transistor.

III-10

2. MOS Transistor Timing

Consider the NMOS transistor circuit shown in Figure III-5.
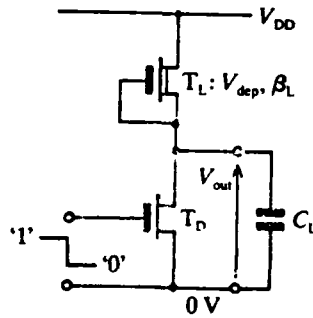
Figure III-5. NMOS transistor with depletion load [7].

The time to discharge the load capacitance C_L from a high output state to a low state is smaller than the time required to charge the capacitance C_L through the depletion transistor resistance of T_L due to the low resistance of the pull-down device T_D when it is in the on state. The time to charge the load capacitance is longer than the time to discharge since the charging takes place via the high resistance pull-up transistor T_L.

The t_{off} and t_{on} times can be approximated by using the equation:

$$I_L = C_L \frac{dV_{out}}{dt} = I_{DS} \quad (+ \text{ or } -) \qquad [14]$$

III-11

Time constants are defined for each of the delay times.

$$T_D \text{ is proportional to } \frac{C_L}{D}$$

and

$$T_L \text{ is proportional to } \frac{C_L}{L}$$

Where T_L is the time required to charge the load capacitance C_L and T_D is the time required to discharge the same load capacitance where β_D and β_L are the respective gains of the pull-down and pull-up devices. The time constant for the pull-down will be much less than the pull-up since β_D is much greater than β_L.

The gain factor (either L or D) is given by:

$$= \mu_n C_i \frac{W}{L} \qquad [15]$$

where C_i is the insulator capacitance, μ_n is the electron mobility (μ_n for n-channel devices) and the hole mobility (μ_p for p-channel devices) and W and L are the dimensions of the transistor. The greater mobility of electrons than holes in silicon is one reason for the higher gain obtained for n-channel devices. The effective mobility can also be affected by temperature, electric field strength and the fabrication process used. However, the major

contributor to the gain of a transistor is the proper design of the "aspect ratio", W/L, where the gains of the transistors can be individually determined.

In Figure III-6, the input and switching waveforms for the NMOS circuit are shown. As indicated an increase in the gain of the load device would correspondingly reduce the charging time but would use more power since power dissipated by the transistor is proportional to the gain factor β.
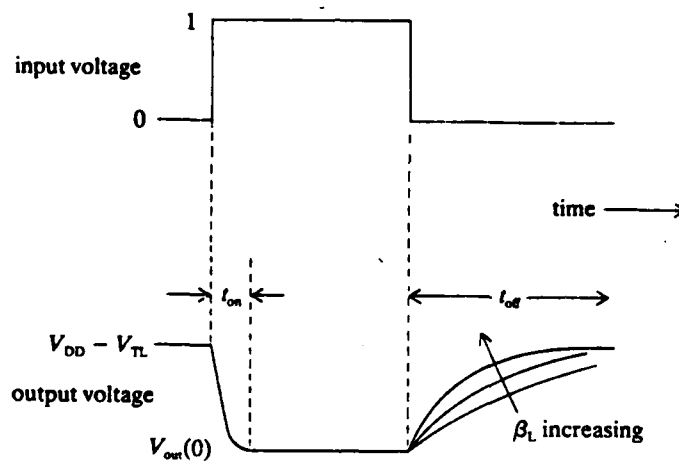
Figure III-6. Turn-on and turn-off waveforms [7].

The transient waveforms are similar to the bipolar waveforms previously presented, however the primary difference is the lack of storage time delay in the MOS transistor. In operation a current path is established from source to drain and a voltage applied to the gate controls the source-to-drain current similar to the operation of a valve. A positive voltage applied to the gate with respect to the source, will tend to attract free electrons from the

substrate into a layer or channel adjacent to the oxide. This effect is large enough to cause the channel to have an excess of electrons. The drain-to-source voltage will then cause a considerable current to flow. The gate characteristics differ with the bipolar base characteristics and result in zero storage time for a transient signal. The other delays associated with the MOS transistor are common to the bipolar transistor. In the next section Complementary MOS (CMOS) circuits will be evaluated for their switching characteristics. This is an abbreviated, qualitative analysis of NMOS switching. A more extensive analysis is provided in the following section concerning both NMOS and PMOS devices since both are used in the complementary structure of CMOS.

3. CMOS Timing Analysis

The drain-current characteristic of an N-type transistor is a function of the drain and gate voltages:

$$I_{ds_N} = K_N [2 V_{ds_N} (V_{gs_N} - V_{threshold_N}) - V_{ds_N}]^2 \qquad [16]$$

$$\text{for } V_{ds_N} < V_{gs_N} - V_{threshold_N}$$

$$I_{ds_N} = K_N [V_{gs_N} - V_{threshold_N}]^2 \qquad [17]$$

$$\text{for } V_{ds_N} \geq V_{gs_N} - V_{threshold_N}$$

III-14

$$I_{d_N} = 0 \text{ for } V_{gs_N} \leq V_{threshold_N} \qquad [18]$$

where K_N is a constant defined by:

$$K_N = \mu_N \, \epsilon_{ox} W / (2LT_{ox}) \qquad [19]$$

where
$$\mu_N = \text{electron mobility}$$
$$\epsilon_{ox} = \text{permitivity of the oxide layer}$$
$$W = \text{channel width}$$
$$L = \text{channel length}$$
$$T_{ox} = \text{thickness of the insulating oxide}$$

The effective capacitance at the gate of the transistor is:

$$C_{eff} = \frac{\epsilon_{ox} \, (L) \, (W)}{T_{ox}} \qquad [20]$$

Similar equations for a P-type device can be derived.

For the inverter shown in Figure II-1, the current in the P-type transistor is determined by:

$$I_P = K_P [2(V_{dd} - V_{out})(V_{dd} - V_{in}$$
$$- |V_{threshold_P}|) - (V_{dd} - V_{out})^2] \qquad [21]$$

$$\text{for } V_{out} > V_{in} + |V_{threshold_P}|$$

$$I_P = K_P[V_{dd} - V_{in} - |V_{threshold_P}|]^2 \qquad [22]$$

$$\text{for } V_{out} \leq V_{in} + |V_{threshold_P}|$$

and

$$I_P = 0 \quad \text{for } V_{in} + |V_{threshold_P}| \geq V_{dd} \qquad [23]$$

The switching response time of the CMOS logic circuit is determined by the amount of current that can be provided by the transistors to charge the load capacitance of the circuit at the input and the output.

If a step input signal is applied to the circuit, the output voltage can be used to solve for an approximate value of switching speed:

$$I_P = I_N + I_C \qquad [24]$$

$$I_C = C_{out} \frac{dV_{out}}{dt} = I_P - I_N \qquad [25]$$

and solving for t:

$$t = C_{out} \int_{V_o}^{V} \frac{dV_{out}}{[I_P - I_N]} = C_{out} \int_{V_o}^{V} \frac{dV_{out}}{I_C} \qquad [26]$$

A minimum value of t is achieved if the current charging the
capacitance, I_C , is made as large as possible.

Based on the inverter circuit, if V_{in} is a positive
voltage equal to V_{dd} , then:

$$C_{out}\frac{dV_{out}}{dt} = -I_N \qquad [27]$$

since the P-type transistor will be an "open" and will not
effect the circuit. The NMOS device will be driven into
saturation and I_N can be represented by:

$$I_N = K_N(V_{in} - V_{threshold_N})^2 \qquad [28]$$

and

$$C_{out}\frac{dV_{out}}{dt} = -K_N(V_{in} - V_{threshold_N})^2 \qquad [29]$$

since $V_{gs} = V_{in} = V_{dd}$

$$C_{out}\frac{dV_{out}}{dt} = -K_N(V_{dd} - V_{threshold_N})^2$$

$$= -K_N V_{dd}^2 (1 - \alpha_N)^2 \qquad [30]$$

where $\alpha_N = \dfrac{V_{threshold_N}}{V_{dd}} = \dfrac{V_{T_N}}{V_{dd}}$ (refer to Figure II-2)

solving for $V_{out}(t)$ gives:

$$V_{out}(t) = V_{dd} \left[1 - \frac{K_N V_{dd}(1 - \alpha_N)^2}{C_{out}} t \right] \qquad [31]$$

The fall time can then be calculated as [4]:

$$T_F = \tau_N \left[\frac{\alpha_N - 0.1}{(1 - \alpha_N)^2} + \frac{\tanh^{-1}\left(1 - \dfrac{0.1}{1 - \alpha_N}\right)}{(1 - \alpha_N)} \right] \qquad [32]$$

where $\tau_N = \dfrac{C_{out}}{(K_N)(V_{dd})}$ and $K_N = \dfrac{\mu_N C_{IN}}{2L^2}$

The rise time response can be determined similarly and results in [4]:

$$T_R = \tau_P \left[\frac{\alpha_P - 0.1}{(1 - \alpha_P)^2} + \frac{\tanh^{-1}\left(1 - \dfrac{0.1}{1 - \alpha_P}\right)}{(1 - \alpha_P)} \right] \qquad [33]$$

III-18

where $\tau_P = \dfrac{C_{out}}{(K_P)(V_{dd})}$ and $K_P = \dfrac{\mu_P\ C_{IN}}{2L^2}$

Any difference in the rise and fall times results from the difference in the mobility factors of the majority carriers in the P-type and N-type materials, the input (gate) capacitance C_{IN}, and the length of the channel of the respective transistors.

The response times of particular interest for the CMOS inverter circuit are the rise and fall times and the associated pair delay. The pair delay (for the P-type and N-type transistor pair) is approximated by [4]:

$$T = 0.9\ \tau \left(\frac{1}{(1 - \alpha_N)^2} + \frac{1}{(1 - \alpha_P)^2} \right) \qquad [34]$$

where $\tau = \dfrac{C_{out}}{K_N\ V_{dd}} = \dfrac{2LT_{ox}C_{out}}{N\ W\ V_{dd}} = \tau_N$

where α_N and α_P are the normalized threshold voltages for the inverter.

The pair delay is the delay that a signal experiences after it has propagated through two cascaded stages of inversion thus representing the effect of one rise-time and

III-19

one fall-time. It is measured at the 50% points of the
signal waveform. This is how signals are standardized for
experimental analysis. This approximation results from
summing T_F and T_R while:

1. Ignoring the tanh term
2. Approximating the α - 0.1 factor with 0.9 in
    the numerator of the first term

Experimental results have shown that this approximation
is within 10% of the measured values [4] and depends on the
response of the two stages since one delay will be
determined by the N-type device and the other delay will be
determined by the P-type device due to the inversion of the
input signal.

B. Propagation Delay Analysis

Propagation delay is the result of transmitting
signals from one part of a circuit to another or from one
chip to another. This brief analysis is based upon the work
of Mohsen and Mead [8].

The propagation path is modeled as a large
capacitance. As such, delays are associated with the
charging and discharging of this capacitive load when
signals are transmitted. A driver stage (composed of a
driver chain and output driver) is used at the transmitting
end of the line and some form of an input (sensing) circuit

stage is used at the receiving end of the line. Figure III-
7 shows the system design model:
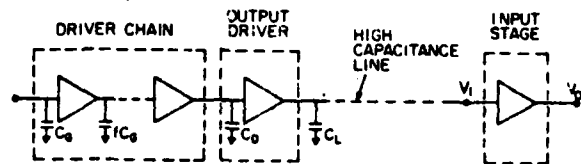
Figure III-7. Large capacitance design model [8].

Delay times exist for the output driver and driver chain,
the time required to charge the line capacitance through the
output driver, and an input circuit delay. A load (line)
capacitance, C_L, is driven with a signal that originates on
the gate of an MOS transistor with gate capacitance C_G.

To drive a large capacitance C_L, an elementary driver
circuit is used to drive increasingly larger drivers in
cascade until the last (output) driver is large enough to
drive the load. If the delay of the elementary driver T_{DR}
is then the delay of a driver f times as large is f T_{DR}. If
N stages are used, then the total driver delay is:

$$T_{ch} = Nf T_{DR} \qquad\qquad [35]$$

The output driver circuit, with input capacitance C_D,
charges the capacitance of the line, C_L, with a voltage.
There is a delay associatd with the output driver which
should be included for in the total driver delay T_{ch} and the

III-21

capacitive load (line) delay T_L. The input circuit detects
the signal at the other end and generates an output voltage
V_o. A delay T_i exists for the input circuit.

Figure III-8 shows the relationship among the three
delays considered here.
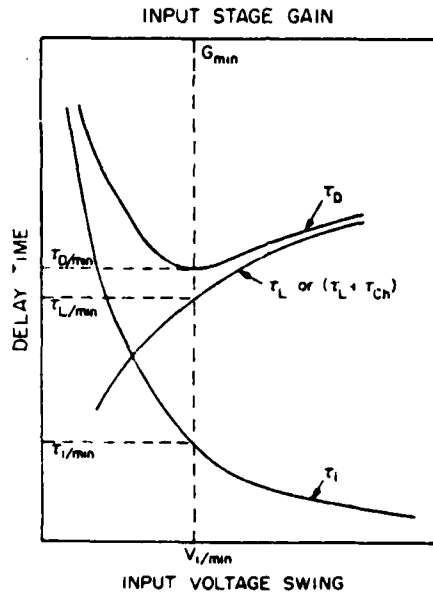
Figure III-8. Delay relationships chart for large
capacitance line [8].

The total delay, T_D, may be calculated as the sum of the
driver   delay, the line delay and the input circuit delay:

$$T_D = T_{ch} + T_L + T_i \qquad [36]$$

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IV.   Speed-up Techniques

This chapter provides information on various speed-up techniques. As previously discussed, these techniques deal with methods of circuit modification that can be implemented by the circuit designer if additional speed is desired within a specific circuit being developed.

This chapter begins with a presentation of capacitor pull-up circuits as they apply to MOS circuits in general and concludes with a review of the "precharge" techniques that have been implemented by various designers.   The section on precharge techniques begins with applications to NMOS circuits and concludes with CMOS based applications. The intent of this chapter is to present speed-up techniques that are presently or have been used in circuit applications, to provide reference data for the potential circuit designer.

A.   MOS Capacitor Pull-Up Circuits

Simple speed-up capacitors may be used to increase the switching speed of bipolar transistors by reducing the storage time during the switching transient.   However, for MOS circuits, there is no storage time delay. Alternative uses have been developed however, for adding capacitors to MOS circuits to try to increase their their operating speed through pull-up circuits.

The data available on this technique dates back to 1969 and addresses only its application to MOS circuits in

general. The circuits are "ratioless" type circuits and are
based on a single phase clock. The RC time constant of the
circuit will limit its operating speed. In normal ratio
type circuits the DC current is limited by the use of high
impedance loads. This method implements a capacitor as a
load element in place of the normal load resistor to
increase the speed of the circuit to the range of 5 - 10
Megahertz.

The pull-up circuit is illustrated in Figure
IV-1 below [9].
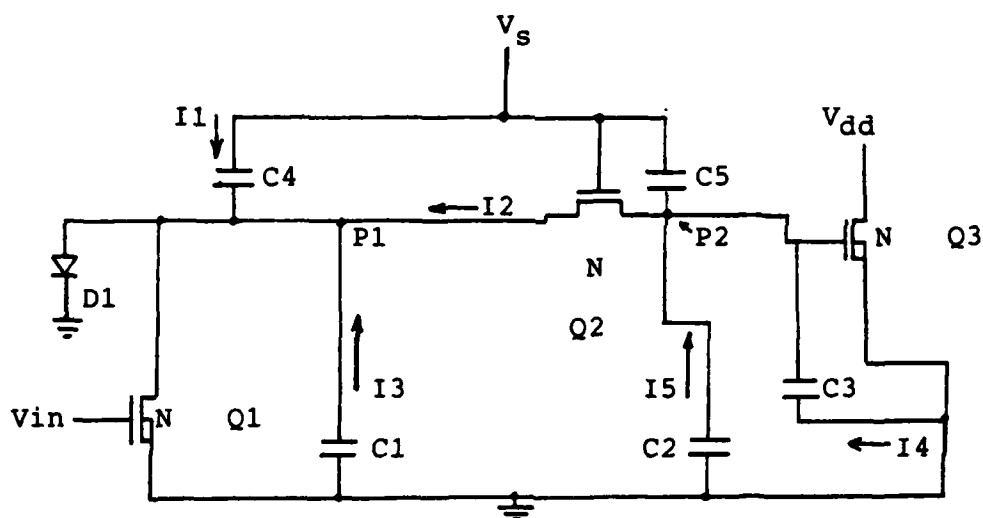
Figure IV-1. Ratioless capacitive pull-up
inverter circuit [9].

The characteristics of the circuit are:

    a.   Operating voltage is obtained from the
        clock pulse

    b.   MOS capacitor C4 blocks all DC current

    c.   The rise time at point P1 is as fast as
        the clock pulserisetime dueto C1-C4

capacitance division

    d. Calculations indicated that the circuit has the capability to perform at 25-30 MHz

Referring to the circuit of Figure IV-1, capacitors C1 and C2 are non-linear p-n junction capacitances associated directly with the MOS devices, C4 is the load element, C3 is the input capacitance to transistor Q3 of the next stage and C5 is the overlap capacitance of the coupling device. Q1 and Q3 are driver devices and Q2 is the coupling device.

When transistor Q1 is off, during the rise time of the clock pulse the voltage at P1 rises rapidly. The coupling device begins to conduct when the clock pulse reaches the Q2 turn-on threshold voltage. The charge stored on C1 and C2 is redistributed such that V1 = V2. During the fall time of the clock signal, V1 falls rapidly due to an appropriate C1:C4 ratio while node P2 discharges slightly through Q2 during turn-off.

If Q1 is on, then during the clock rise time the capacitive divider at P1 is in parallel with the resistance of Q1 giving V1 an exponential form. As the clock passes the threshold voltage of Q2 it turns-on putting C1 in parallel with C2 + C3. This results in a lower maximum value of V1 which decays toward zero as the clock pulse decays toward zero. The purpose of this technique is to force the circuit to operate as closely to the shape of the input clock as possible thereby reducing delays.

Measured circuit time constants were determined to be short enough for 10-20 MHz operation, somewhat less than the computer predicted operating speed.

Use of capacitors alone as load elements has not developed as a widespread technique for speeding up circuits. The primary reason being the impracticality of designing capacitors as the scale technology progressed from small, medium and large to very large scale integration. The most widely used load element at this time is the depletion-mode transistor, which provides a high load impedance. However, the parasitic capacitances internal to the load transistor do have an effect on the operating speed of the switching transistor, as discussed above.

B. Bootstrap Pull-Up Inverter

The inverter circuit shown in Figure IV-2 is useful for fast switching operations when large capacitive loads are to be driven.
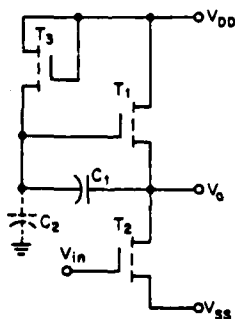
Figure IV-2. Bootstrap Pull-up circuit for increased drive capability [10].

IV-4

An additonal transistor, T3, is coupled to the capacitance C1 to drive the load capacitance C2. During initial operation, T1 was operating in the saturation region, the driver, T2, was in the triode region, the output was at a low voltage level and a voltage of $V_{dd} - V_o$ appears across C1. As V_{in} switches to zero voltage, the output voltage increases as transistor T2 shuts off. The gate bias for T1 is then the voltage across C1.

As T2 begins to shut off due to a zero input voltage, the voltage stored across C1 remains during the switching transient. As the voltage at the output increases, the load transistor is forced into its triode operating region which causes V_o to rapidly reach its maximum. The gate of the load transistor T1, reaches a maximum of $2V_{dd} - V_o - V_{SS}$, where V_{SS} is the substrate bias voltage. Transistor T3 simply acts as an additional pull-up device that enhances the speed of the voltage rising from a low to a high level.

C. Precharging

The concept of precharging is based on the premise that the transition of a low level signal to a high level takes a longer period of time than the transition of a high level signal to a low level. This premise is valid assuming the discharge of the circuit occurs through a small resistance compared with the resistances encountered when the circuit is charged to a high level, creating a smaller RC time delay on discharge of the circuit. This situation

IV-5

exists in the standard MOSFET circuit using a depletion mode load transistor.

The precharge concept can be effective for both switching and propagation applications. The precharging process is easily used when a two phase clock is being implemented within the designed circuit. Temporarily unused lines are precharged to a high level through the relatively low resistance of the wire. The capacitance of the wire holds the line high (similiar to the action of a pull-up transistor). This precharging is accomplished under control of phase 1 of the clock and actual circuit switching occurs during phase 2 of the clock.

In this way if the next signal on the line is high the line will already have the high level available on it and if the next signal is a low level, advantage can be taken of the more rapidly occurring transition fall-time of the line from high to low. The careful design of the circuit to synchronize the two phase clock scheme to accomplish this precharge task is critical to valid operation of the circuit. Coordination of either pulling or setting a point or line high is used to reduce the slow low to high transitions. It has applications in carry-chain circuits for ALUs and is frequently used within RAM memory cells for read operations when increased speed is desired in the slow memory access process. The precharge concept can be used selectively within a circuit to set specific lines high on the first phase of the two phase clock. Due to the

IV-6

discharge times of the individual gates, the precharged line(s) will remain at the high level and trigger subsequent combinational logic to its functionally correct levels (either high or low), until the actual input signals on gates which electrically precede the precharged node propagate to the precharged lines and the gates tha+ follow. As the input signals arrive, they can either be high and take advantage of the already high (precharged) inputs to subsequent gates and not have to suffer a gate by gate delay for each gate, or be low where the more rapid high to low transition time is the only speed-up that can occur. This is similar to the "domino" effect [4] described by Krambeck et al as the precharge is used to initialize the circuit for operation using a two phase clock.In practice, precharged lines to the same gate could, in the optimum case, propagate the correct signal level to the output of the combinational logic, occur independently of the input, and reduce the gate delay for circuits beyond the precharged node to near zero, since all the gates will be set to the correct high or low level before the actual inputs ever reach the combinational logic themselves. If high levels occur on certain lines more frequently during operation in comparison to other lines, and this can be predicted during the design process, then those lines should be precharged. The advantage of thii is that this charging to a high level is automatically applied to combinational logic gates that follow the precharged layer of gates, thereby "presetting" the inputs and outputs

IV-7

of the following gates so that "highs" on the "real" inputs that occur later won't have to do it and the only gate delays that will occur happen while the "real" inputs are propagating to the location of the precharged gates.

For switching applications, fabrication techniques and new materials are progressing to the point where equal rise and fall times will be achievable. Even so, this application of precharge will continue to be valuable. However, the designer should keep in mind the limitations of this application. The maximum frequency of operation of a circuit will be determined by the speed of the slowest part of the circuit. Even though some lines may be precharged, and the delays along these portions of the circuit reduced, if other parts of the circuit operate slower, i.e. a large number of "real" input lows occur, then this slower part of the circuit and its associated delays will determine the maximum frequency of operation. This effectively negates the addition of the precharging, since the remainder of the circuit must wait for the slowest part to complete its function.

A complementary alternative to the precharging concept is the selective grounding of certain lines that are expected to have a high occurrence of low signals on them. This produces the same effect as the precharge since the ground, or low signals are propagated through the combinational logic that follows the "grounding" layer and set the gates that follow to the correct level before the

actual input signals arrive. The delays associated with these following gates are again reduced/eliminated since the real input signals will not have to cause the actual switching of the gates since it will have already occurred by the grounding taking place on phase one of the two phase clock. The effective use of precharging or grounding is clearly dependent upon the individual delays of the gates being used. The precharge/ground must have time to occur (and stabilize) before the actual input signals arrive at the precharged layer of gates. Additionally, phase two of the clock, which controls when the signals are passed out of the "black box" circuit, must not occur until the actual input signals have propagated through the circuit itself. This aspect of delay reduction will continue to be a function of the individual gate delays which are controlled primarily by the fabrication techniques used. However, the use of precharge will remain as a good means for reducing the delays associated with long, high capacitance lines within circuits as well as for the selective method discussed above.

There is very little reference material on the concepts of precharging. Most of the data available deals with specific applications in which precharging was used. No established guidelines seem to exist at this time. The following information refers to specific implementations of precharge or precharge-like techniques. Although the first section below is directed at NMOS circuits, the applications

of precharge can be modified to CMOS design. A review of precharge-based circuits follows.

1. NMOS Applications

    a. Charge Pumping

        This charge pump technique was designed to realize the standard erase-then-write two step write operation of a memory circuit in a single step. The charge pump circuit is shown in Figure IV-3 [11]. The charge pump circuit was applied to the read/write circuit as shown in Figure IV-4. The actual operation of the circuit will not be discussed here. Any reference to actual circuit operation is only intended to aid in evaluating the operation of the precharge circuitry.
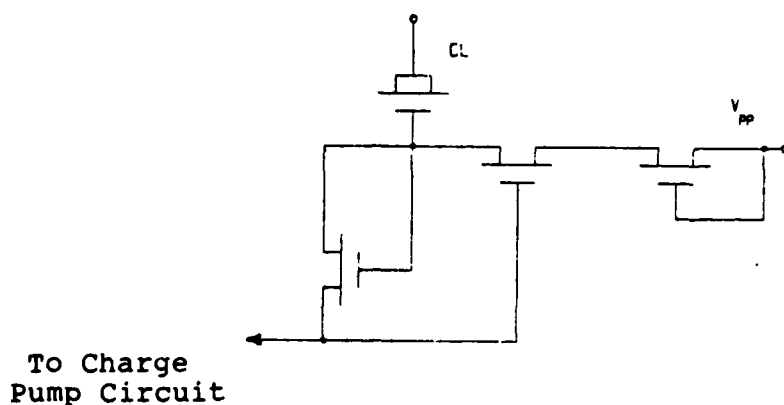
Figure IV-3. Charge pump circuit [11].
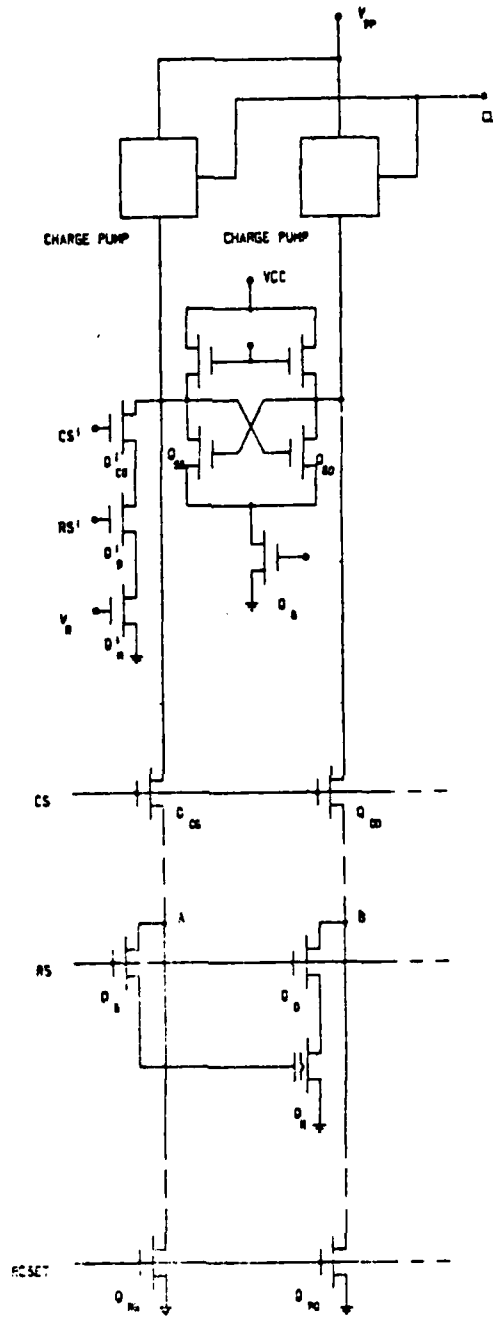
Figure IV-4. Read/Write circuit [11].

When the read operation begins, Q_{CG}, Q_{CD}, Q_E, and Q_D are turned on by the column select (CS) and the row select (RS) respectively. The data is stored on Q_M and is provided at point B for output. If Q_M is ON originally, then node B is low and node A is high after the read operation. The charge pump circuit pulls the level of node A to the value of V_{dd} and since the path to ground through point B is still closed, point B will remain low. After a short time Q_M will invert its state due to tunneling and node B will be pulled high by the charge pump circuit. Therefore by applying CL to the charge pump circuit, the state of Q_M can be inverted. The simultaneous occurrence of Q_M driven to a high or a low, and node B driven to the inverse of the signal stored on the gate of Q_M, turns the normal two step erase-then-write process into a single step.

Although refered to as "charge pumping" this circuit performs a simple precharge function on the memory cell. Whenthe clock pulse occurs, the state of the transistor Q_M will determine if the node A will be charged to a high level and whether or not node B will be high or low.

b. <u>NMOS</u> <u>Dynamic</u> <u>RAM</u> <u>Cell</u>

Newkirk and Matthews [12] implement precharging when their dynamic RAM cell is used in a 3 transistor memory subsystem, with an interface and address cell. The interface cell is precharged during phil,the first clock pulse of a two-phased clock. If sense (read) is high then ExtIO will be high due to the precharge unless a stored

"high" discharges the precharge. If drive (write) is high,
then the input value on ExtIO to be written to the memory
cell will determine if the precharged line is grounded
(value on ExtIO is high) or if it stays at a high level
(ExtIO is low). Figure IV-5 shows a diagram of the memory
subsystem.
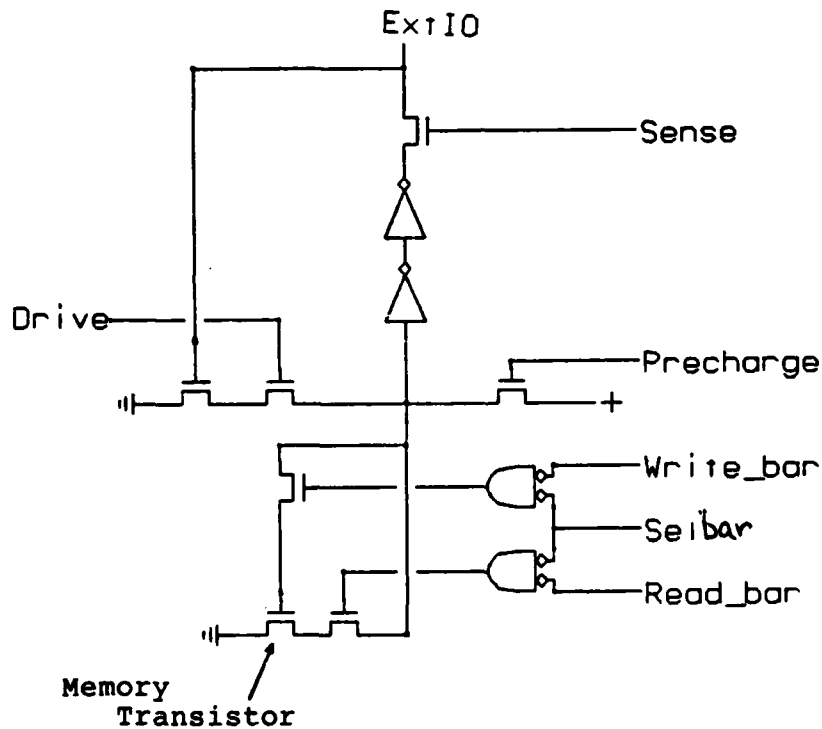
Figure IV-5. 3-transistor Memory Subsystem [12].

In this implementaion, the precharge scheme was used to facilitate the reading and writing of data to the memory cell. An underlying benefit of using the precharge is an increase in the speed of the read and write operations of the cell. Memories are inherently slow in this regard and precharging is an excellent way to shorten the memory access cycle.

c. CalTech OM2 Arithmetic Logic Unit (ALU)

Mead and Conway [13] provide a review of their "Our Machine" (OM) Project at Caltech and emphasize the system requirement for a high performance carry chain within the ALU since they felt the carry chain would have the most limiting effect on the performance of the system. They implemented a Manchester-type carry chain, and since it had a limited capability to propagate high signals, they took advantage of a null period experienced in the processing cycle of the op-code of the computer. They decided to precharge the data paths of the carry chain, to reduce the requirement for high-level signal propagation through relatively slow pass transistors. The carry-out line was precharged and the actual data being supplied to the carry-out line determined if the carry-out line would be shorted to ground or not. Figure IV-6 shows the carry chain circuit for the ALU.
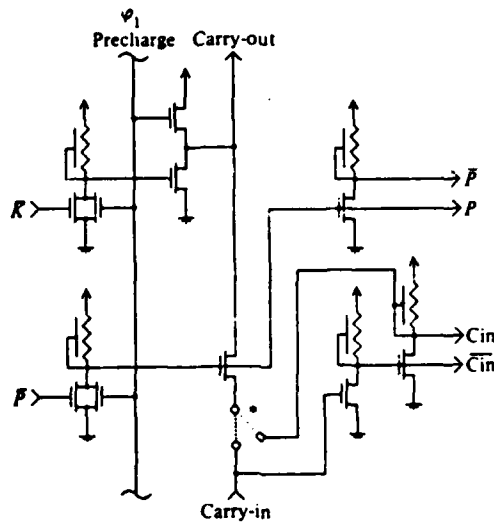
Figure IV-6. Carry chain circuit for OM2 ALU [13].

2. CMOS Applications

a. Domino Logic Circuit

Krambeck et al [5] apply the concept of pre-
charging in their design of a CMOS domino circuit. They
employ a precharge signal that is used to turn on all the
gates in a circuit at one time thereby reducing the
requirement for complex timing schemes and reportedly taking
advantage of the inherent speed of the CMOS gates.
Specific application of their domino circuit to an 8-bit ALU
has indicated through simulation to be one and a half to two
times as fast as traditional circuits performing similar
functions. The domino circuit is shown in Figure IV-7. The
values of the inputs (I1 - I5) to the transistors determine
the output of the domino circuit cell after the precharge.
Individual dynamic cells are isolated from each other by

inverter stages.
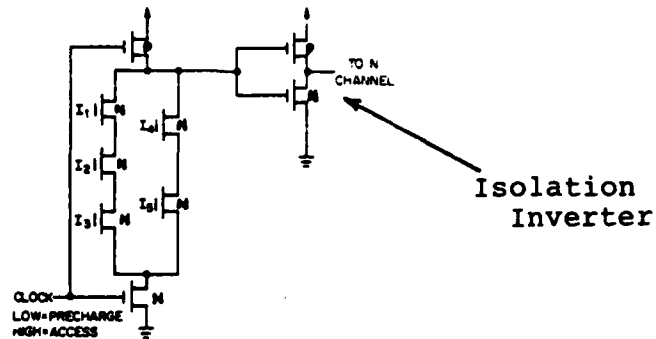
Figure IV-7. Domino logic circuit [5].

In addition to increasing circuit speed, Krambeck's circuit has eliminated the internal clock race condition by placing the inverter after each logic block for isolation. During the precharge phase, the outputs of all the inverters are driven to a low level by the precharged node and therefore all n-type transistors driven by these inputs are turned off. During phase two of the clock, any internal clock delays cannot incorrectly discharge the storage nodes since the path to ground through the n-type transistors is open. All internal nodes can make at most one transition until the next precharge, therefore a stable propagation state exists. Since this process is similar to the falling of dominos as the signal passes from block to block, this name was applied to the design.

b. <u>Domino Logic Modification</u>

Gonsalves and Man [1] describe a dynamic CMOS

technique making use of the domino circuit previously described. The redundancy of information characteristic of CMOS, low power dissipation and lower capacitances, thus higher speeds, can be achieved if the n-type dynamic CMOS logic block shown in Figure IV-8 is used in lieu of standard CMOS circuitry. Silicon area is also reduced since only N n-type devices are used and 2 p-type devices (total N+2 devices) are used instead of N p-type and N n-type devices as in standard CMOS.
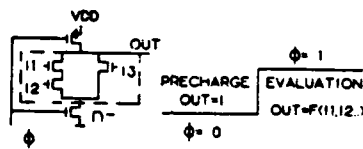
Figure IV-8. n-type dynamic CMOS logic block [14].

The inherent deficiencies of Krambeck's design are determined as:

1. The combination of the dynamic block and inverter results in inverted signals which decreases logic design flexibility

2. The clock race problem is just controlled, it is not overcome

These deficiencies are resolved by a specific "No Race" (NORA) [1] design approach. However, the precharge scheme

is treated in the same manner as implemented by Krambeck. The primary difference between the two approaches is Krambeck's use of inverters for isolation versus Gonsalves use of latch stages to store information in successive stages, his addition of p-type dynamic blocks as well as the n-type domino logic cell used by Krambeck and a subsequent emphasis on pipelining of data within cirucits.

3. High Speed Precharge Circuit

Stewart and Plus have integrated precharging to provide a high performance, high speed EEPROM [15]. The precharge generation circuit is shown in Figure IV-9. The precharge signal generated in the precharge and control circuit is used to switch on the decoders and sense amplifiers following changes in the memory address inputs.

A high speed parallel decoder and sense amplifier circuit which detect small voltage changes on the lines as data is read out of the memory cells. The actual operation of the circuitry will not be discussed. This circuit simply demonstrates another application of precharging used to drive other circuits.

The parallel decoder is shown in Figure IV-10 and the sense amplifier circuit in Figure IV-11.

PC - Precharge

Figure IV-9. Precharge generation and control circuit [15].

Figure IV-10. High-speed word decoder [15].
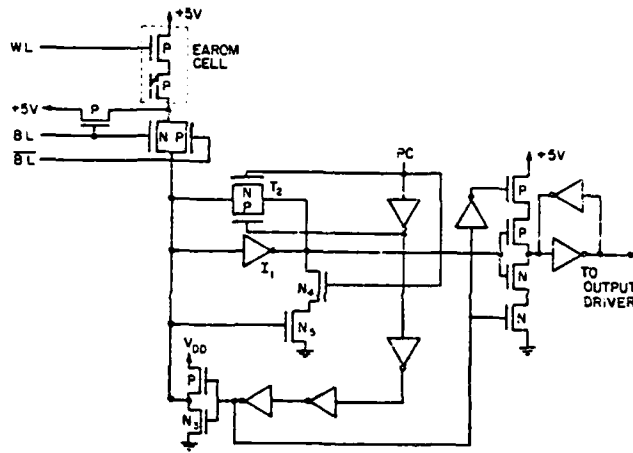
PC - Precharge

Figure IV-11. Sense Amplifier Circuit [15].

When the precharge occurs, the source of P1 remains high and the drain of P3 is set to low and NODE 3 will be precharged high. This sets up the circuit for inputs from A1 through Am which will determine the final value of NODE 3.

4. Bootstrap Circuit

Masuda et al have designed an advanced and accurate 5-V "bootstrap" generator circuit for accessing a MOS structure 64K RAM and achieved 5 nanosecond delays using another form of precharge [16].

The bootstrap circuit is simply a two phase precharge circuit similar to those already mentioned.

D. Propagation Delay Reduction

There is one standard rule to follow when

IV-20

designing for minimum propagation delay: avoid dominating the chip area with wiring interconnections.

a. Cross Under Effect

In addition, Anami et al [17] have recommended an approach for reducing the "crossunder effect" and its associated delay due to the parasitic effect of the resulting resistance. The designer should avoid crossunders in the critical signal paths of the circuit. The aspect ratio can be minimized however to reduce any loss in speed and the optimum width of the crossunder can be expressed by:

$$W_{opt} = [(C_t R_{xo})/(R_o C_{xo})]^{1/2} \qquad [1]$$

where R_o is the output impedance of the line driver driving the crossunder line, C_t is the capacitance following the crossunder, C_{xo} is the capacitance per unit area of the crossunder and R_{xo} is the sheet resistance of the crossunder. They have verified this equation through experimental use of ring oscillators.

b. Large Capacitance Loads

Mohsen and Mead [8] have addressed driving a large capacitive load as referred to in Chapter III.

Mohsen and Mead have evaluated specific cases for minimization. Delay times for push-pull depletion load driver stages with a single-ended depletion load input stage were analyzed. For this case the following analysis was derived [8].

IV-21

Total driver chain delay is minimized when each successive driver stage is larger than the previous one by a factor of e (the base of the natural logarithm). Where:

$$Y = \frac{C_L}{C_G} = f \quad \text{and} \quad \ln(Y) = N[\ln(f)]$$

and

$$= \ln Y \left[\frac{f}{\ln f}\right] \quad = \quad e \ln\left[\frac{C_L}{C_G}\right] \qquad [2]$$

Minimum total delay is achieved with a fan-out factor f equal to the base of the natural logarithm, e.

Depending on the application, the input stage delay can be optimized to different values.

Their overall conclusions suggest that for minimum delay time, the designer should try to keep the delays of the driver circuit, the high capacitive line and the sense circuit comparable, i.e. $T_{ch} = T_L = T_i$. This conclusion follows from the delay relatonships presented in Figure III-8.

c. Repeaters

A repeater is simply a series pair of inverters. Chwang et al [18] have successfully implemented both precharging and line buffers/repeaters in their high density 64K CMOS Dynamic RAM. The repeaters used in series between 8K memory array segments reduced the word-line delay from 30 nanoseconds to 10 nanoseconds.

This application uses both precharging and simple inverters to increase circuit operation. Figure IV-12 shows the dynamic RAM arrays with the repeaters located between arrays and Figure IV-13 shows the use of precharging within the circuit.

ARRAY ARCHITECTURE
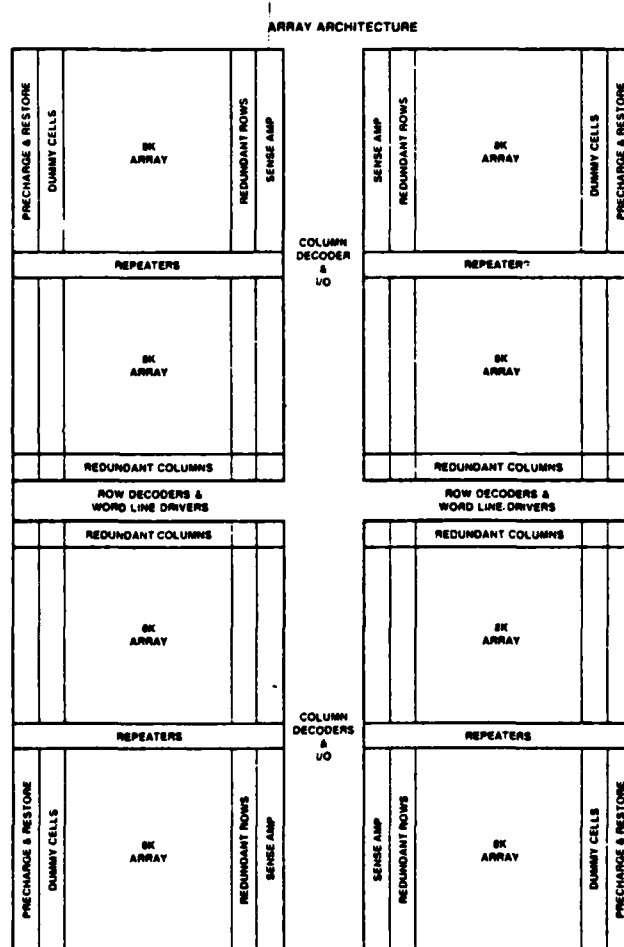
Figure IV-12. 64K Dynamic RAM with repeaters [18].
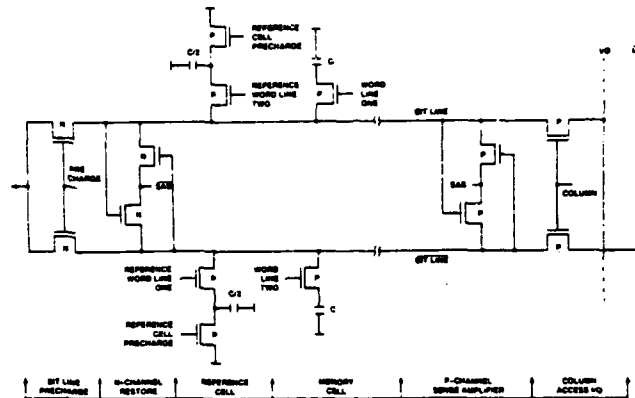
Figure IV-13. Precharge implementation circuit [18].

E. General Remarks

This chapter consists of all the data that was found as a result of a continuing literature search for information. Much data was found referring to fabrication methods and improved selection of fabrication materials. These appear to be the primary areas in which most of the effort is being expended to improve the speed of circuitry.

Different terms have been used i.e. charge pumping and bootstraping, to describe, after analysis, what in actuality is a form of precharging. However, the term, "bootstraping" has also been associated with transistor pull-up circuits. The reader is cautioned to disregard the terms used to describe specific techniques and really

determine exactly what the circuit is doing prior to considering it for use in a design, since different names are sometimes associated with the same method or technique.

F. CMOS VLSI Applications

1. Requirements

The major requirements for a specific speed-up technique to be considered useful are (in order of importance):

        a. Simplicity

        b. Ease of Implementation

        c. Applcability to variety of circuits

        d. Frequency of Use

The designer should be able to implement the method with minimum modification if a circuit exists already, the particular technique should use a minimum of chip area, which becomes critical in VLSI applications, and should be a simple enough approach to permit use by even the most basic of designers.

The frequency of use of a certain technique is a measure of the design community's acceptance of the technique for use. This requirement is included as a justification for selection of a specif c technique for evaluation during this thesis.

2. Selection of Technique

From the information provided in section A of this

chapter, and from a review of available literature, the most commonly used speed-up technique is precharging or some modification thereof; i.e. Krambeck et al [5] and the charge pumping scheme [11].   There are two primary methods of precharge implementation.   The first method, using precharging on output lines with a two-phase clock, permits an implementation of a precharged line as shown in Figure IV-14 below.   The line is charged high in phi1 and the value of the data and the phi2 clock determine if the line will be grounded or not. This circuit is useful for reducing delays over large capacitance lines and will reduce the charging delay time of the lines.   This method was not considered for simulation during this thesis.

```
                         +V
                          | dd

        phi1bar ─────┌──────────────┐
                     │              │
        phi1    ─────┤              │
                     │              │
        databar ─────┤      3       │
                     │              │
        data    ─────┤ Transmission │
                     │              │
        phi2bar ─────┤    Gates     │
                     │              │
        phi2    ─────└──────┬───────┘
                            │
          ──────────────────────────────────
                                      databar line
```
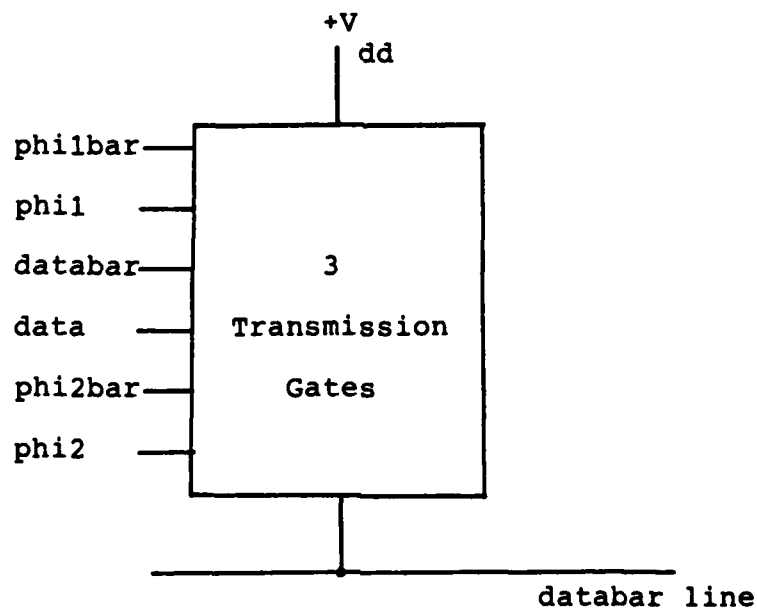
Figure IV-14.   Output precharge circuit scheme.

The second method precharges selected nodes within a circuit using individual transmission gates that pass Vdd to the selected node when a pass signal is applied to the transmission gate. This normally occurs on phase one of a two phase clock. This scheme is shown in Figure IV-15. Any number of transmission gates can be used for this appication, however a single transmission gate is required for each line that is to be precharged to maintain isolation of the individual signals.

```
                          +V
                            dd
                            |
        phil ───────┌───────────────────┐
                    │          N         │
                    │     Transmission   │
        philbar ────│        Gates       │
                    └───┬───────────┬────┘
                        │           │
                        │  . . .    │
                        ▼           ▼
             N lines to N precharge nodes
```
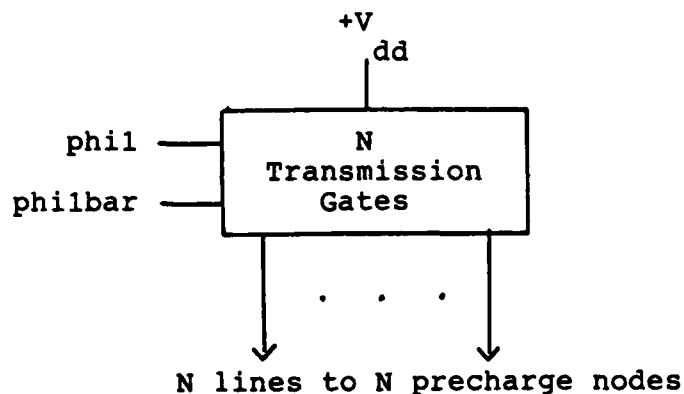
Figure IV-15. Internal transmission gate precharge scheme.

Implementation of transmission gate circuits can be accomplished during the design of the circuit with no additional effort and with minimal use of circuit area. The precharge scheme can be used anywhere within the circuit where additional speed is required and can be applied to any circuit design. Any line that can be charged high and then pulled low or left high, based on circuit data manipulation,

can be subjected to precharging. Transmission gates will be discussed in more detail in chapter V.

These characteristics make the precharging concept a reasonable choice for evaluation.

From review of the literature, precharging was the most popular manual design technique used to speed-up circuit operation. Although it was frequently used, little data was available on exactly how good an approach it really was. Many designers had used it, with reported increases in speed, however, a consolidated source of information was not available. Since precharging had the highest frequency of use, an analysis of its capabilities was performed.

Therefore, the remainder of this thesis was concerned with applying precharging to an existing ALU bitslice and to newly designed circuit elements using CMOS/SOS technology. The circuits were extensively simulated using SPICE transient analysis to determine the success of precharge application.

Chapters V and VI present the precharge design of the ALU bitslice and the design and precharge of additional circuit elements to be used for simulation.

The results of the simulations are presented and evaluated in Chapter VII.

V. System Design

A. Introduction

The design portion of this project was divided into two main areas:

1. CMOS/SOS ALU Bitslice modification using precharge techniques

2. Implementation of a circuit using the modified ALU bitslice as a circuit element built around a 4x4 bit Random Access Memory (RAM) referred to as the Memory/ALU Bitslice circuit

In this chapter, the modified ALU bitslice using precharging, and the Memory/ALU Bitslice circuit design, incorporating the modified ALU bitslice, are presented. The more elaborate circuit was used to demonstrate the applications of precharging techniques to elements within a more complex circuit. The applications presented here demonstrated the flexibility of precharging as a design tool which can be used in new designs as well as being added to existing designs.

B. Requirements

1. The following design requirements applied to the modification of the ALU bitslice and the design of the Memory/ALU Bitslice circuit:

    a. The bitslice precharge circuitry must be:

        1. Capable of speeding up circuit operation

        2. Be easy to implement

3.   Use as little area as possible

4.   Apply to a wide variety of circuits

b.   The Memory/ALU Bitslice circuit must:

1. Demonstrate the precharging concept applied at a chip level, i.e. a large circuit application.

2. Demonstrate uses of precharging applied to elements commonly used by the circuit designer

2.   To meet these requirements, SPICE2 was used for simulation.   To determine the performance of the precharge speed-up technique, the following steps were followed:

a.   Design a test circuit

b.   Simulate the test cirucit with SPICE2

c. Use a variety of precharge configurations and simulate circuit operation for each configuration

d.   Compare test circuit results

e.   Simulate the 2x4 decoder circuit using SPICE2

f.   Apply precharging to the decoder, RAM and registers

g.   Simulate the operation of the circuit using SPICE2

h.   Compare the results of the two simulations

i.   Simulate basic bitslice operation using SPICE2

j.   Select bitslice nodes to apply precharge

k.   Design of the precharge circuit itself

l.   Implement the precharge modifications to the circuit

V-2

m. Simulate operation of modified bitslice with SPICE2

n. Compare the results from each analysis

o. Incorporate the ALU bitslice into a circuit using a 4x4 memory circuit

p. Evaluate results and present conclusions

C. Circuit Selection

For the evaluation, a test circuit was designed for basic precharge and timing evaluation and the first bitslice of the CMOS/SOS ALU designed and developed by Sommars [3], was selected as a more complex circuit to which the precharge technique was applied and evaluated. At the time this thesis took place, the ALU and the CMOS/SOS library were the only existing CMOS/SOS based VLSI components available at AFIT. The precharge technique was applied to only the first bitslice of the ALU to limit the scope of the simulation required and to eliminate redundancy of effort for application/evaluation since the subsequent bitslices of the ALU differed only slightly from the first one and thererfore could be precharged in the same way.

D. Design Rules

This design effort made use of the same design rules used by Sommars [3] in support of his design of the CMOS/SOS library cells based on the unpublished notes of Seitz [18].

E. ALU Bitslice Modifications

The output lines of the ALU were precharged on phase

one of a two phase clock and the data will be read out of the ALU on phase two of the clock. The capacitance of the output lines will be charged on phase one and the value of the data (high or low) will determine if the line is discharged to ground through the low resistance of the pull-down transmission gate or will remain high at the output of the circuit. The CMOS transmission gate is used for the precharge pass element. This gate is shown in Figure V-1.
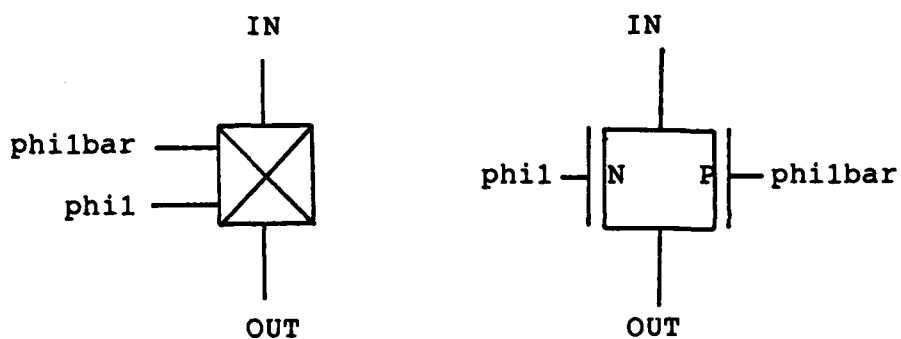
Figure V-1. CMOS transmission gate [7].

This gate ideally has zero resistance when closed and infinite resistance when open. It is formed by joining the sources and drains of a pair of MOS transistors of opposite polarity. Control signals on the gates of each transistor determine whether or not the signal will be transmitted. If each device has a threshold voltage of 2 volts, and the control voltages to the gate of the p and n type devices are

0 and 10 volts respectively, the n type device will remain "on" until the input to the transmission gate reaches 10 - 2 = 8 volts, when it will turn "off". However, the p type device will continue to conduct since the gate to source voltage of 8 volts is greater than the p type device threshold voltage of -2 volts. In this manner the entire supply voltage, Vdd, can be transmitted by the gate and a "good" precharge can take place. Two precharge circuits were used; an internal precharge circuit and an output precharge circuit. The internal precharge circuit was used to selectively precharge nodes within the bitslice circuit and the output precharge circuit precharged only the output lines of the bitslice. The basic block diagrams for the internal and output precharge circuits are shown in Figure V-2 and Figure V-3 respectively. Block diagrams of the unmodified and the modified ALU bitslices are also provided in Figures V-4 and V-5 for comparison.
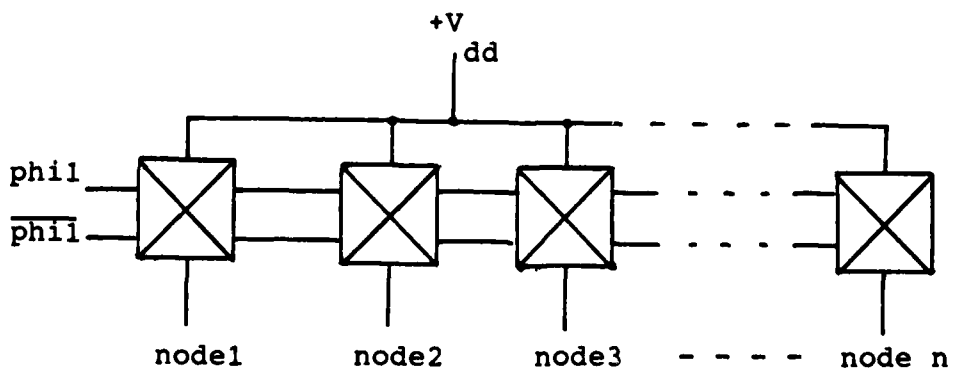
Figure V-2. Internal precharge circuit.
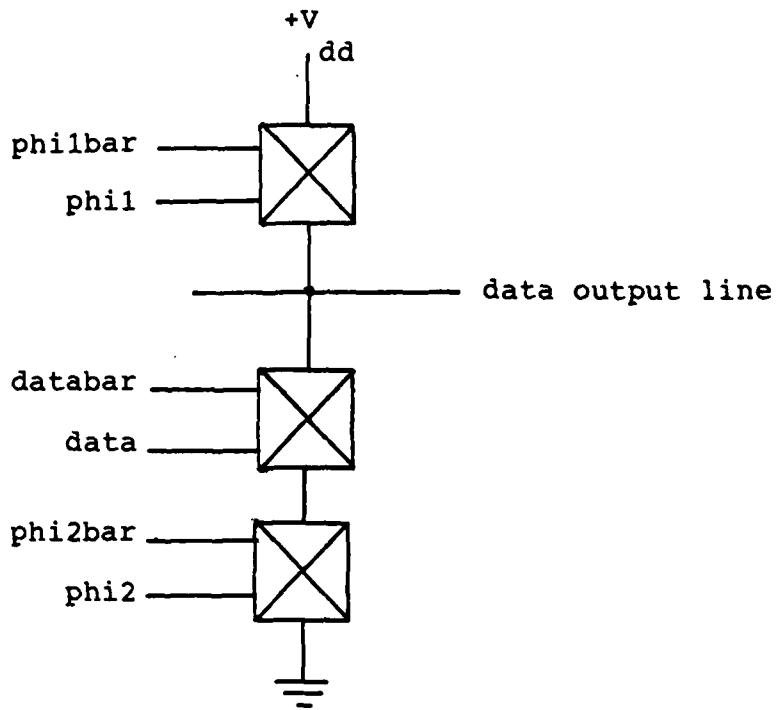
Figure V-3.   Output precharge circuit.
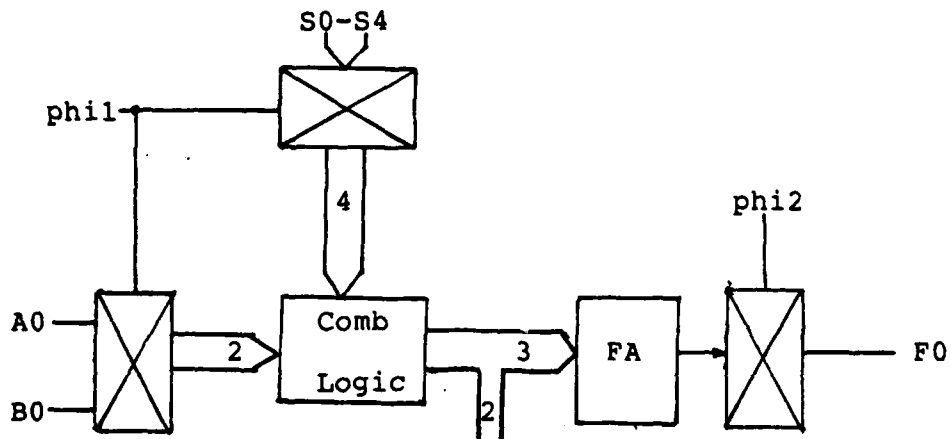
Figure V-4.   Unmodified ALU design [3].
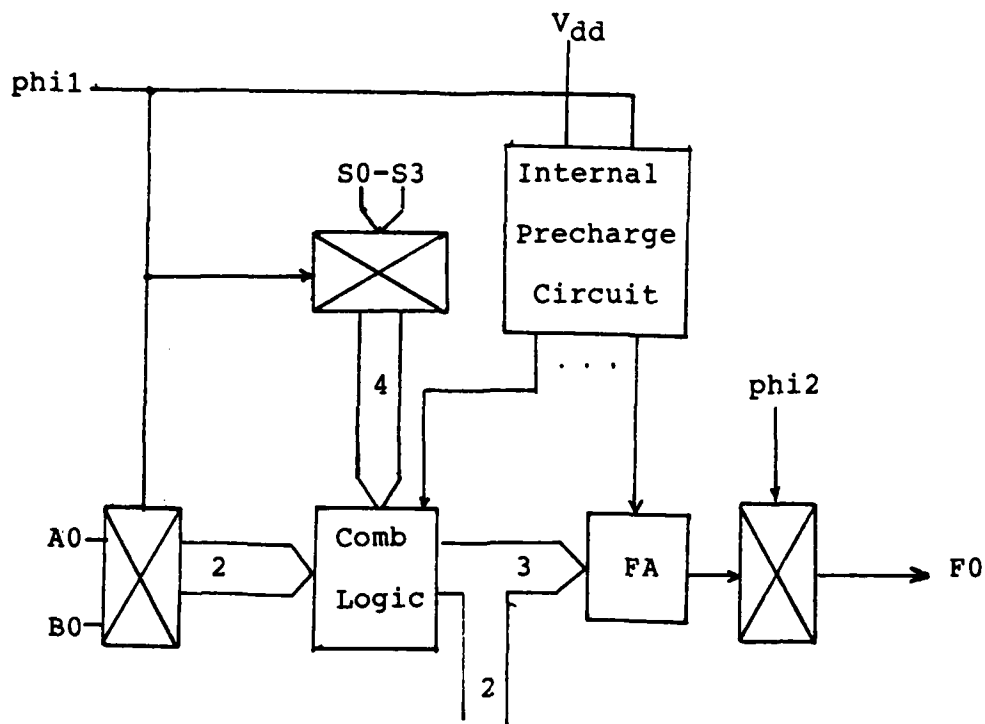
Figure V-5.   Modified (precharged) ALU bitslice circuit.

F.   Memory/ALU Bitslice Circuit Design

To complete the second part of this system design, a circuit was designed that incorporates the modified ALU, makes active use of other CMOS/SOS library cells and requires the development and implementation of additional circuit components. Precharging is applied to this expanded circuit (in addition to the ALU) to further demonstrate the use of precharging techniques in basic design.

In addition, design of the Memory/ALU circuit

demonstrates the utility of the CMOS/SOS library for practical design and sets the stage for future design efforts in the CMOS/SOS area.

The Memory/ALU circuit was designed to perform in conjunction with a microprocessor controller. The circuit is composed of the basic ALU, a 4 bit by 4 bit static Random Access Memory (RAM), a row decoder and the necessary control logic required to manipulate the memory and the ALU.

The transmission gate is used in this design to clock the signals within the circuit, since the use of transmission gates is presently the only effective way to control and isolate clocked signals in CMOS circuits.

1. Circuit Function

The function of the circuit is as follows:

Data will be written into memory in 4-bit words in accordance with a decoded 2-bit row address, with both data and address supplied by the microprocessor. Data processing can be performed for two operator functions and for single operator functions. To perform arithmetic or logical operations between different operators, two registers will be implemented to hold the two respective 4-bit words that have been read from memory. The registers will be selected by a register select line. Data is first read into the A register. As data is subsequently read into the B-register, the register select signal will pass the ALU command on the
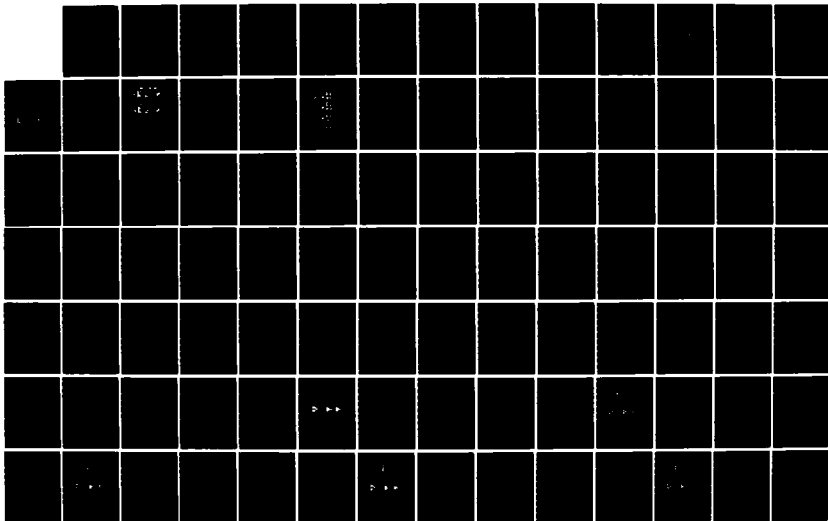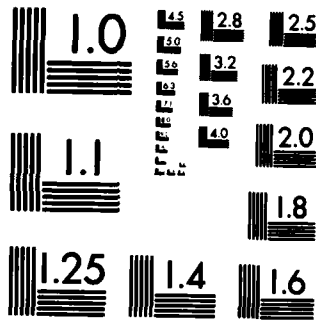
MICROCOPY RESOLUTION TEST CHART

NATIONAL BUREAU OF STANDARDS-1963-A

S0-S3 input lines into the ALU, and the function selected by S0-S3 will be performed. If only a single operator is required, i.e. A + 1 (an increment function), the register select line will still select register B, after data is entered into register A, but the contents of register B will not be used. For either case, the data from memory is applied to the ALU for manipulation based upon the command input to the ALU generated by the microprocessor controller. The output of the ALU can be monitored to determine if the circuit performs the desired functions correctly.

For single chip implementation, the following signal lines will be required:

    a. Two address lines

    b. Four data input lines

    c. One read/write line

    d. Four ALU command lines

    e. Two ALU bitslice output lines

    f. One register select line to the ALU

    g. One external clock line.

    h. One chip ground line

    i. One Vdd line

    j. One substrate connection

        Total: 18 chip pins

The system circuit diagram is shown in Figure V-6.

V-9
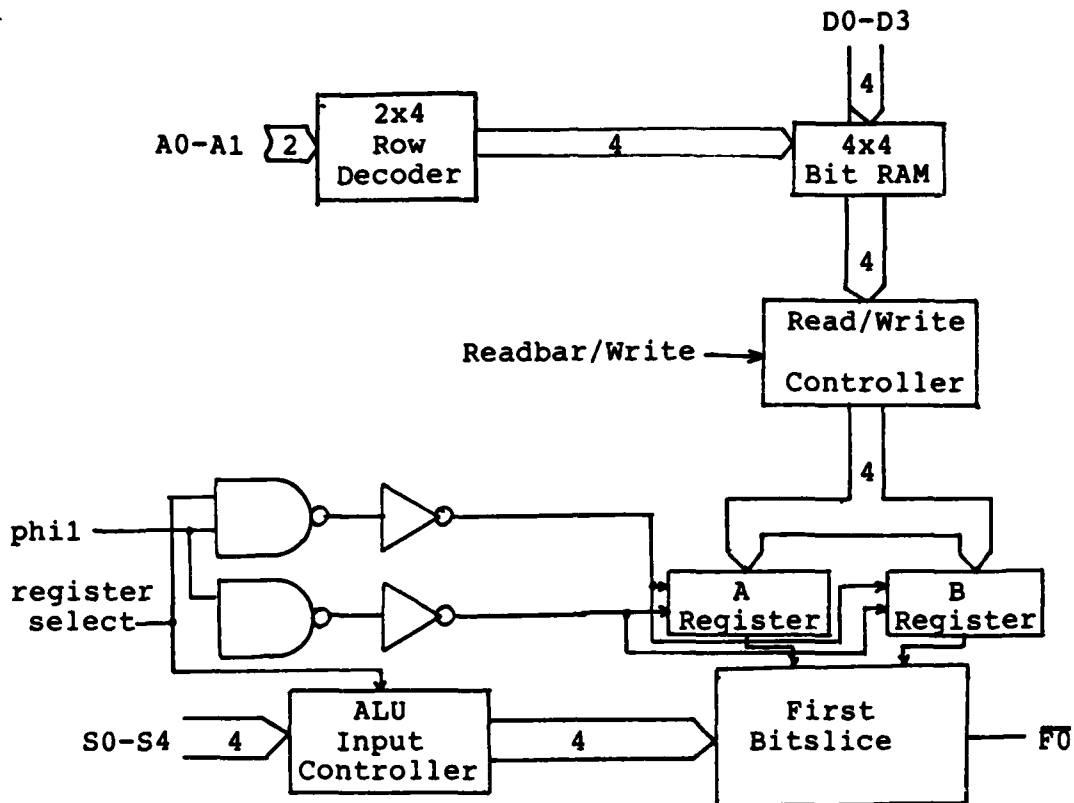
Figure V-6.   System circuit diagram.

2.   Additional Components Required

In addition to the existing ALU, the following
additional circuit components that will be required are:

1. RAM cell - static (no refresh required) from
   which a 4x4 bit RAM was realized

2.   2x4 Decoder

3.   Two four-bit registers

4.   Read/Write Control

5.   ALU input control

The basic decoder, 4x4 bit RAM and the register

circuit elements were initially designed, and then precharged. This was done to demonstrate the flexibility of precharging during the circuit design phase.

F. Memory/ALU Circuit Chip Layout

The pad layout for the expanded circuit chip is provided in Figure V-7. The choice of chip pads is limited for CMOS/SOS applications. Pads will be selected from the following list:

1. padVdd
2. padground
3. padblank
4. padout (composed of paddriver and padamp)
5. padin

At this time no capability exists to generate a two phase clock on chip. Therefore, these circuits were designed with the intention of driving them with an off-chip two phase clock source. Pad types are represented by their respective numbers listed above.

R/W   Reg V_{dd} D0   D1   D2   D3
        Sel

	3	3	5	5	3	1	5	5	5	5	
A0 5											3
A1 5											3
S0 5		2x4 Decoder		4x4 RAM		Read/Write Controller					3
S1 5											3
S2 5							A&B Registers				3 SUB
S3 5		Internal Precharge Circuit									4 FO
CLK 5				Bitslice Circuit							3
3											3
3											3
3											3
	3	3	3	3	2	3	3	3	3	3	

GND
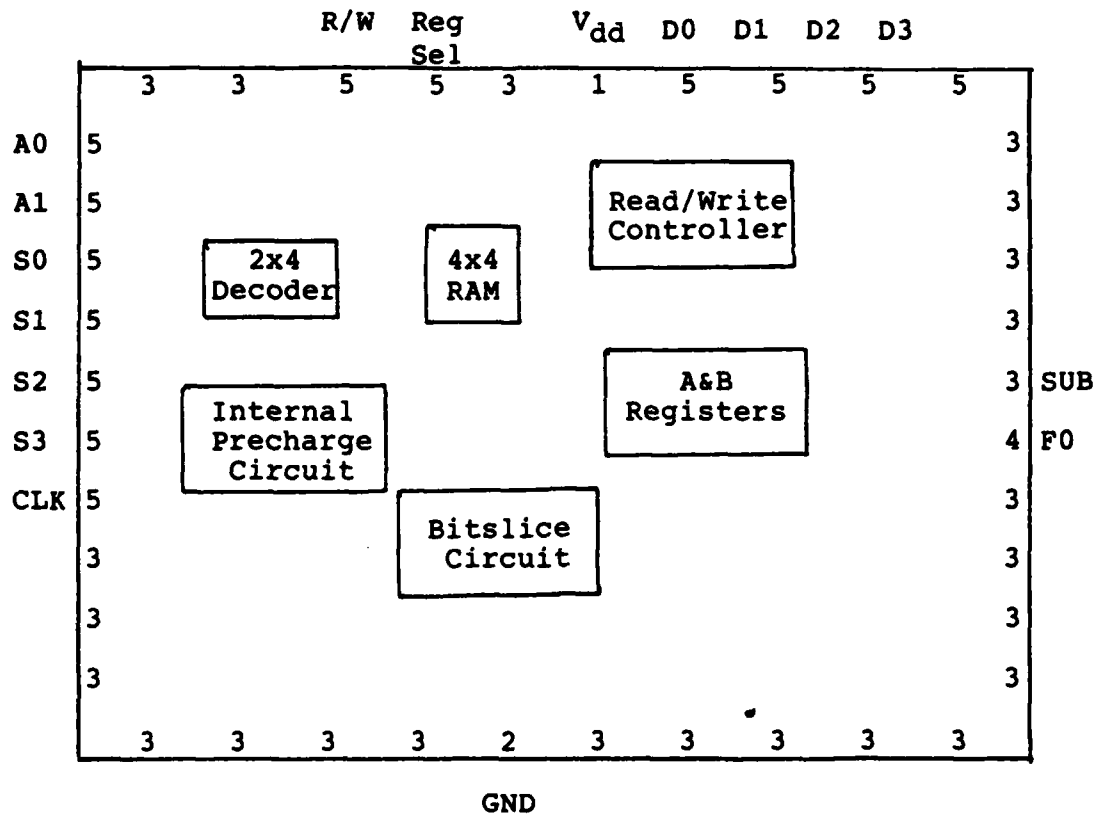
Figure V-7. Pad layout for chip.

VI. Detailed Design and Analysis

This chapter begins with a brief analysis of the predicted advantage of precharge when used with the CMOS/SOS library cells in circuit design.

The chapter concludes with a presentation of the detailed designs of the modified ALU bitslice and the Memory/ALU Bitslice circuit. The precharge circuitry which is applied to the ALU bitslice and the elements of the Memory/ALU Bitslice circuits are shown in their schematic and CLL plot layouts.

A. Test Circuit Delay Analysis

This analysis is intended to provide the reader with a better understanding of the expected advantage of using precharge as a circuit speed-up technique. The timing values presented are those results achieved by Sommars from his SPICE2 simulations of the individual CMOS/SOS library cells that were designed [3]. SPICE2 circuit simulations were performed on this test circuit to determine the validity of this analysis and demonstrate the precharge concept. The results of the simulations are discussed in more detail in Chapter VII.

This is a rough approximation analysis of the delays associated with logic gates to be used for this design and is only intended to provide the reader with some basic reference information to more easily understand the nature of the delays being evaluated. In Figure VI-1, a series logic circuit is presented composed of one nand gate and two

inverters.

Nand   Inv1   Inv2
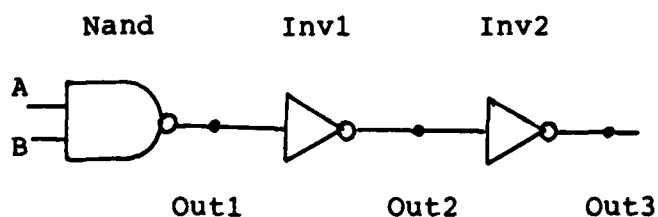
Figure VI-1.   Delay analysis circuit.

The delays referred to here are taken from SPICE2
analyses performed by Sommars [3].

The delays in the nand gate, as the inputs change, are:

    inputs: 0 volts to 5 volts - 1.0 nsec

                (output goes from high to low)

    inputs: 5 volts to 0 volts - 1.0 nsec

                (output goes from low to high)

When inputs A and B are both driven high, OUT1 is
driven low and OUT2 is driven high. OUT1 experiences a 1.0
nsec delay before it reaches its final low value.

The delay times for the inverter are:

    input: 0 volts to 5 volts - 0.15 nsec (at the output)

               (output goes from high to low)

    input: 5 volts to 0 volts - 0.25 nsec (at the output)

               (output goes form low to high)

If A and B are driven low then OUT1 will be driven to a
low value after 1.0 nsec, OUT2 will be driven high after a

0.25 nsec delay and OUT3 is driven low after an additional delay of 0.15 nsec. The total delay time is calculated in equation [1]:

$$1.0 + 0.25 + 0.15 = 1.4 \text{ nsec} \qquad [1]$$

If A and B are driven high the same delay time is achieved due to the equal rise and fall times for the respective gates. Therefore the maximum operating frequency of the test circuit is:

$$1/1.4 \text{ nsec} = 714 \text{ MHz} \qquad [2]$$

If precharge was implemented, and applied to OUT1, then OUT2 and OUT3 would be driven low and high respectively. If nand inputs A and B were subsequently driven low, driving the output of the nand gate high, maximum advantage could be taken of the high precharge at OUT1 and the only contribution to the circuit delay time would be the nand transition delay (which would, theoretically, be reduced since the nand wouldn't necessarily need the entire 1.0 nsec to drive the OUT1 node high when it is already precharged high), since the precharge signal would have already "set up" the circuit. Therefore the overall circuit delay would be reduced by 0.4 nsec and the operating frequency would be:

$$1/1.0 = 1000 \text{ MHz} \qquad [3]$$

Therefore, with the nand output driven high by inputs A and B, a 40% increase in operating speed could be achieved by

precharging the OUT1 node. However, if the nand inputs drive the output low after it has been precharged, then OUT1 will be driven from a high precharged level to a low level, OUT2 will be driven high from a low level and OUT3 will be driven low from a high level. The only delay reduction that occurs for this scenario is the reduction in transition delay in the second inverter, since OUT3 will be driven low from a high level and in an inverter, a high to low transition takes 0.15 nsec and the low-to-high transition takes 0.25 nsec in an inverter. The total delay is reduced by only 0.1 nsec, from 1.4 nsec to 1.3 nsec, and a maximum operating frequency of 769 MHz, a 7% increase in operating frequency.

If each output, OUT1 through OUT3 were precharged on phase one of the clock, even if the output of the nand were driven low, a gain in speed would be achieved since OUT2 would already be high and OUT2 would not have to wait for the inverter delay. The delay would then be reduced by the 0.25 nsec savings incurred by the precharge. The maximum operating frequency would then be:

$$1/1.15 \text{ nsec} = 869 \text{ Mhz} \qquad [4]$$

Therefore, a 21% increase in operating frequency could be achieved with the addition of the precharge. This method is only valid for alternating inversion of signals within the combinational logic. This situation occurs frequently within common combinational circuits and can be taken

advantage of by the circuit designer by applying precharge techniques. This is the method by which the nodes within the bitslice were selectively precharged. If all of the nodes, OUT1, OUT2 and OUT3 are precharged, then no matter what the output of the nand gate (either high or low), there will always be at least a minimum time savings of one transition from low to high across an inverter, either INV1 or INV2.

This delay approximation can be performed for each possible precharge configuration that could be applied to the test circuit.

This analysis provided the baseline from which the results of the SPICE simulations of the test circuit, Memory/ALU bitslice circuit elements and the bitslice were interpreted.

B. Modified ALU Bitslice

The detailed design of the precharge implementation was performed in three steps. First, the lines to be precharged were selected. For simulation, two precharge configurations were used, the bitslice with ten internal nodes precharged and the bitslice with four nodes precharged. The two configurations were chosen to determine the best approach to precharging the bitslice based on the results of the test circuit simulation. The bitslice was divided into three sections and each section was simulated independently. The simulations and results are presented in more detail in

Chapter VII. Secondly, the layout of the circuit was
determined to minimize wasted space, although this is not
critical for this application and simulation, and remain
within the established design rules. The third step was the
active implementation of the circuit using CMOS/SOS library
cells developed by Sommars [3]. The CLL layouts of the
internal precharge circuit for each bitslice precharge
configuration are shown in Figure VI-2. Some redesign of
Sommars' ALU was required to permit SPICE simulation and to
correct deficiencies in design.
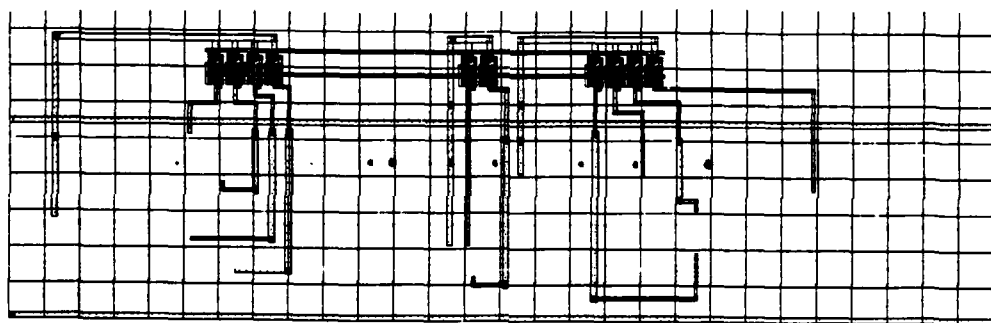
a.
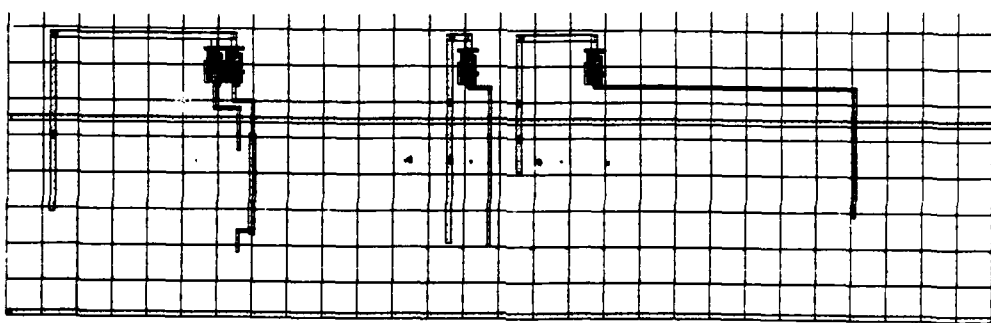
b.

Figure VI-2.   CLL layout of internal precharge circuit.
                a.   Ten node precharge
                b.   Four node precharge

Ten transmission gates are required for the internal precharge circuit of the first approach and four transmission gates are required for the second precharge approach. A single transmission gate is required for each precharge line. Therefore, to precharge more lines the designer need only add more transmission gates.

The output precharge circuit is more complex since it is based on the output line being pulled down to ground or left at a high level depending on the value of the data on the output line. This precharge scheme causes the output of the ALU to be inverted for each line that is precharged. If the output from the ALU is high, the precharged output line will be grounded. If it is low, the output line will remain high. The advantage of the precharge applied here is that, although they are inverted, the outputs from the ALU are realized more quickly, since all the output lines are charged high and only the high data outputs will cause any type of delay when the precharged line is grounded through the low impedance transmission gates to ground. This precharge approach is typically used for high capacitance lines and is recommended by Ullman [24]. A CLL layout of the output precharge circuit is shown in Figure VI-3.

This circuit was not used in the circuit simulations, since analysis of delays in long high capacitance lines was not the primary purpose of this thesis.

                    +V$_{dd}$

phi1

phi1bar
                                        databar
data

databar

phi2

phi2bar

                    GND
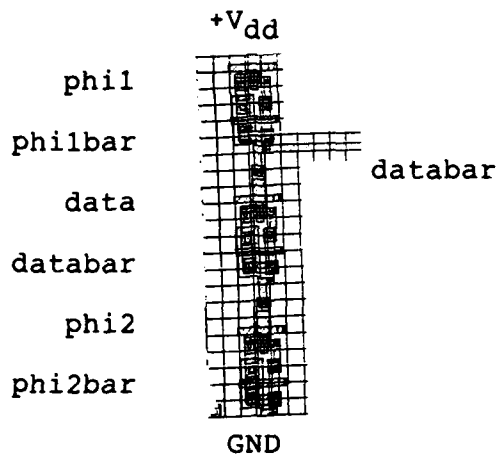
Figure VI-3.   Output precharge circuit CLL layout.

If the output precharge circuit had been used, the first
bitslice of the ALU would have used only one such circuit
since the bitslice has only output.   However, the output
precharge circuit could easily be expanded to handle more
precharge lines by addition of more output precharge
circuits.

The ALU performs the basic functions of the Motorola ALU
after which it was modeled, which are listed in Table VI-1.

Table VI-1.   ALU Functions

Function Select				Logic Functions M is High F	Arithmetic Operation M is Low C$_n$ of LSB must be High F
S3	S2	S1	S0		
L	L	L	L	F = $\bar{A}$	F = A minus 1
L	L	L	H	F = $\overline{A \cdot B}$	F = A plus (A · $\bar{B}$)
L	L	H	L	F = $\bar{A}$ · B	F = A plus (A · B)
L	L	H	H	F = Logical "0"	F = A times 2
L	H	L	L	F = $\overline{A \cdot B}$	F = (A · B) minus 1
L	H	L	H	F = $\bar{B}$	F = (A · B) plus (A · $\bar{B}$)
L	H	H	L	F = A⊕B	F = A plus B
L	H	H	H	F = A · $\bar{B}$	F = A plus (A · B)
H	L	L	L	F = $\bar{A}$ · B	F = (A · $\bar{B}$) minus 1
H	L	L	H	F = A⊕B	F = A minus B minus 1
H	L	H	L	F = B	F = (A · $\bar{B}$) plus (A · B)
H	L	H	H	F = A · B	F = (A · $\bar{B}$) plus A
H	H	L	L	F = Logical "1"	F = minus 1 (two's complement)
H	H	L	H	F = A · $\bar{B}$	F = (A · B) plus 0
H	H	H	L	F = A · B	F = (A · B) plus 0
H	H	H	H	F = A	F = A plus 0

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The first bitslice schematic diagram is shown in Figure VI-4 and the associated CLL layout is shown in Figure VI-5.
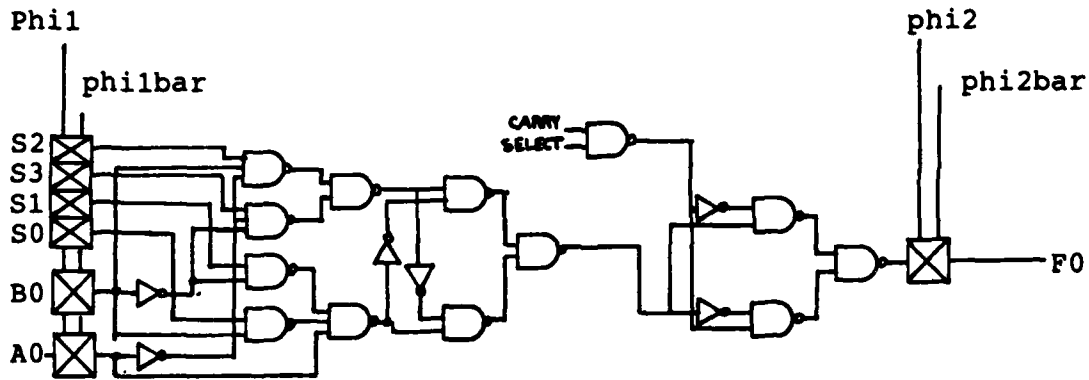
Figure VI-4. ALU Bitslice Schematic Diagram [3].
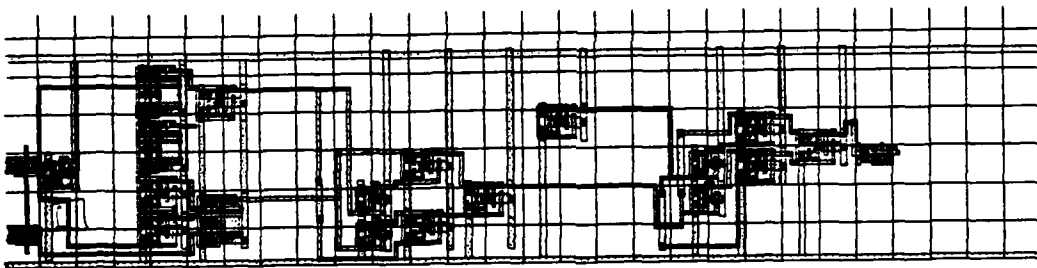
Figure VI-5. ALU Bitslice CLL Layout.

The ALU bitslice schematic diagrams with the precharge circuit implemented for the ten node and four node precharge configurations are presented in Figure VI-6.
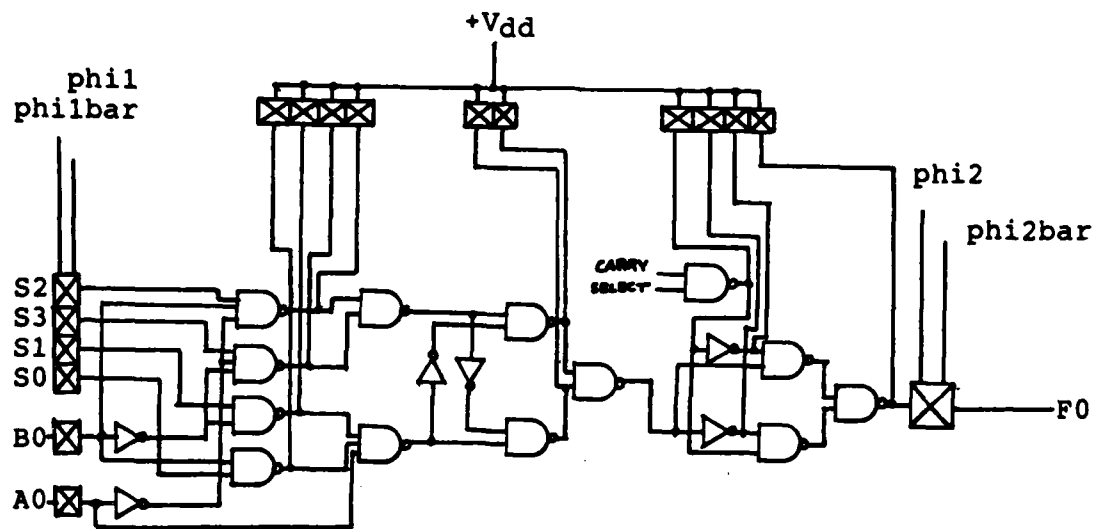
Figure VI-6a.   Detailed Schematic Diagram of Bitslice with
Ten nodes precharged.
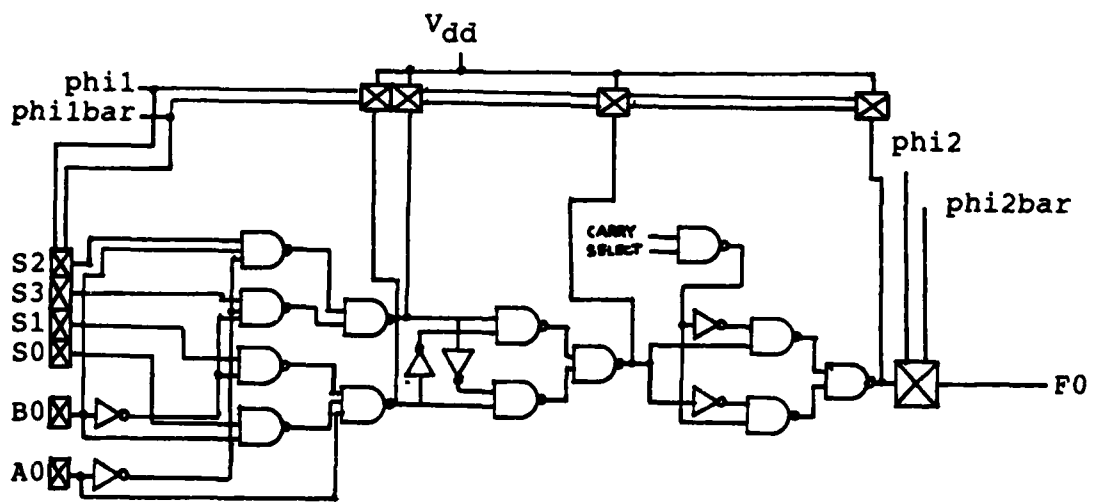
Figure VI-6b.   Detailed Design Schematic of Bitslice with
Four nodes precharged.

A CLL layout of the two precharged bitslice
configurations is provided in Figure VI-7.
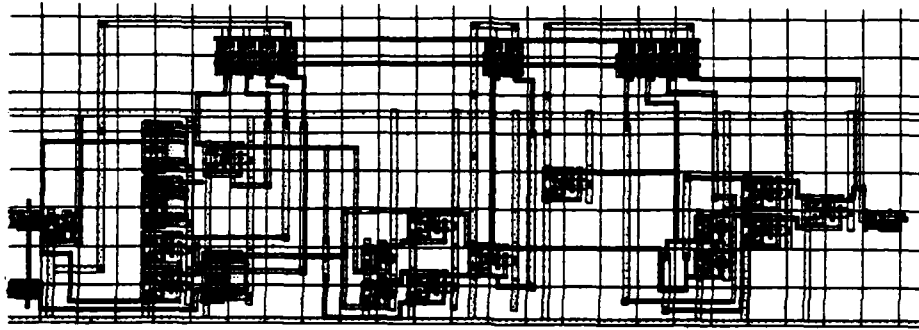
Figure VI-7a. CLL layout of Ten node precharge bitslice.
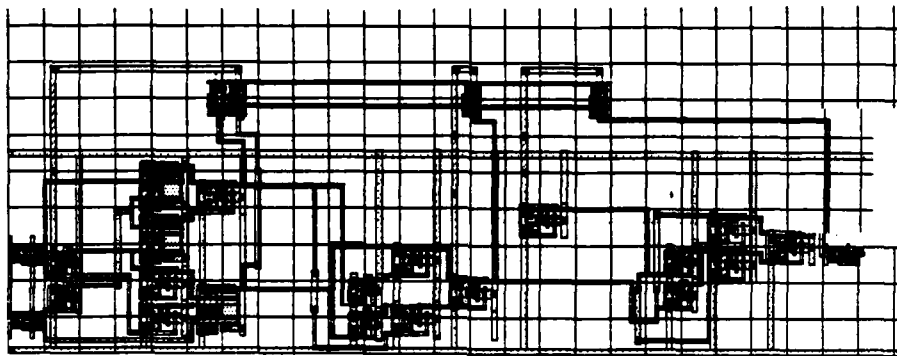
Figure VI-7b. CLL layout of Four node precharge bitslice.

C. Memory/ALU Bitslice Circuit Design

The Memory/ALU circuit design was accomplished in three steps. First, the schematic designs were generated for each circuit element within the limits imposed by the availability of logic circuit cells in the CMOS/SOS library. The following gates were available:

- Inverter Gate (Slow and Fast types)

- 2 Input NAND Gate

- 3 Input NAND Gate

- 4 Input NAND Gate

- Transmission Gate

- 2 Input NOR Gate

- Double Buffer

Second, the elements were layed out to minimize the area used and remain within the imposed design rules. Third, the circuits were implemented using the available NMOS CAD design tools and required CMOS/SOS library cells.

The following circuit elements were designed:

- Two 4 Bit Registers

- Read/Write Controller

- ALU Bitslice Input Controller

- 2x4 Decoder

- 4x4 Bit Static Random Access Memory (RAM)

1. Register Design

Two different size registers were required. The A register received data first when data is read from the memory to be processed. Data is read from memory and stored in the A regsister on phi 1 of a two phase clock. On phi 2 of the same system clock cycle the data is retained in the A register and, on the next phi 1, data is read into the B register. On the next phi 2 pulse the data from both registers is read into the ALU for manipulation. To properly time this process the A register is designed twice as large as the B register so the data it contains may be retained throughout another read cycle as data is read into the B register. Both registers are composed of transmission gates to isolate the signals and inverters on which the

VI-12

signal is stored temporarily as it is passed between register layers. A register select signal controls the direction to where the read data is stored. The schematic diagram for the A register is shown in Figure VI-8 and the associated CLL layout in Figure VI-9. The third and fourth layers of the register reverse the signal connections required to pass the signal between layers since during this time data is being read into the B register and the register select line will be selecting register B. A schematic diagram and CLL layout of the B register are shown in Figures VI-10 and VI-11 respectively.
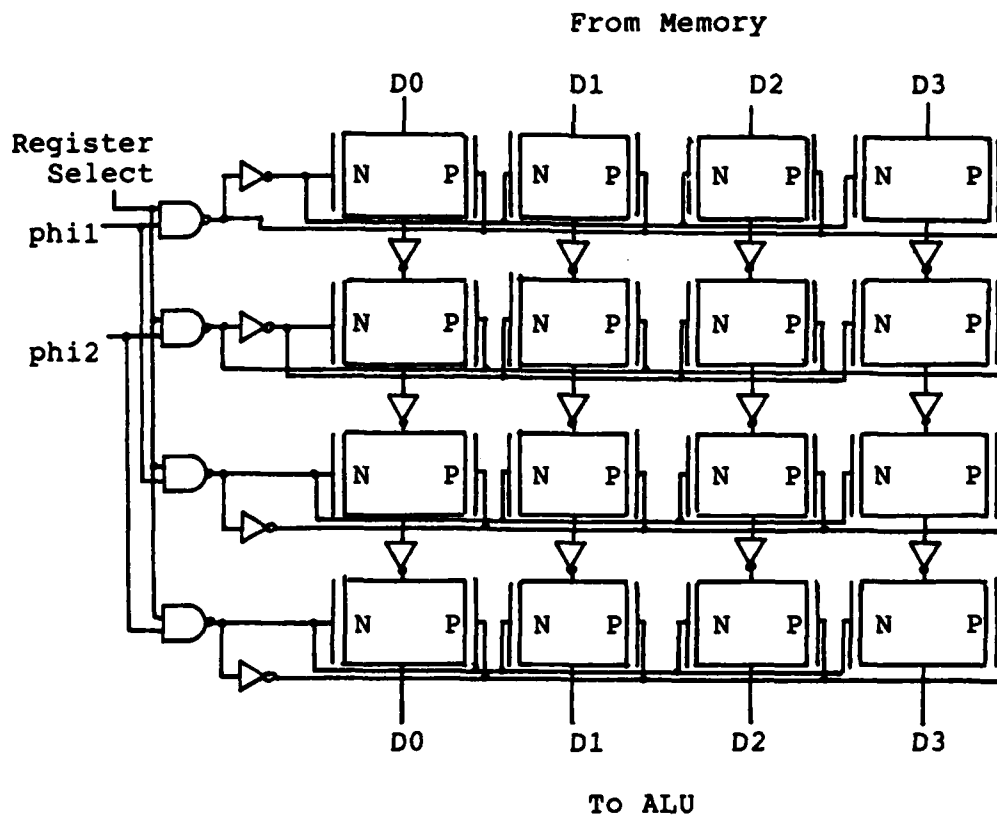
Figure VI-8. A register schematic.
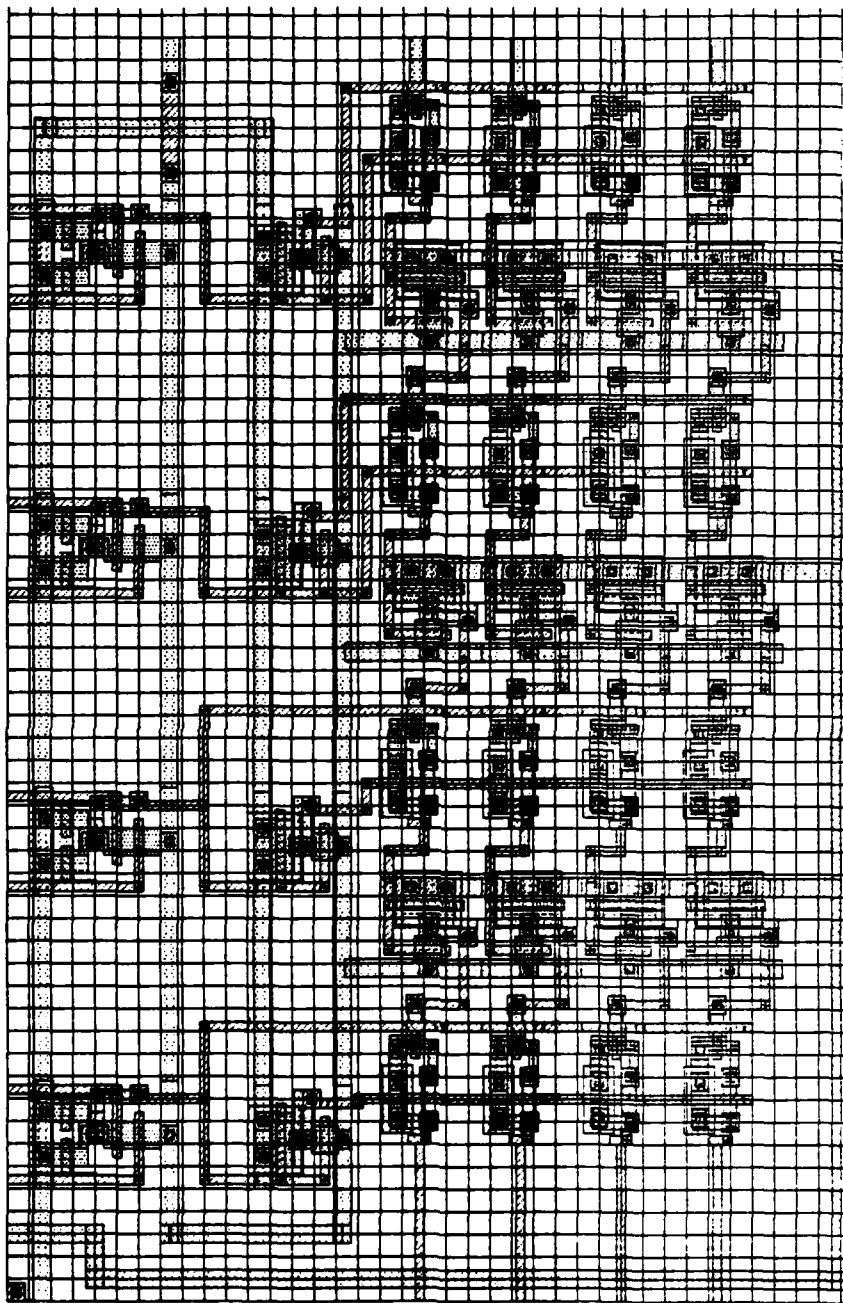
Figure VI-9. CLL layout for A register.

From Memory
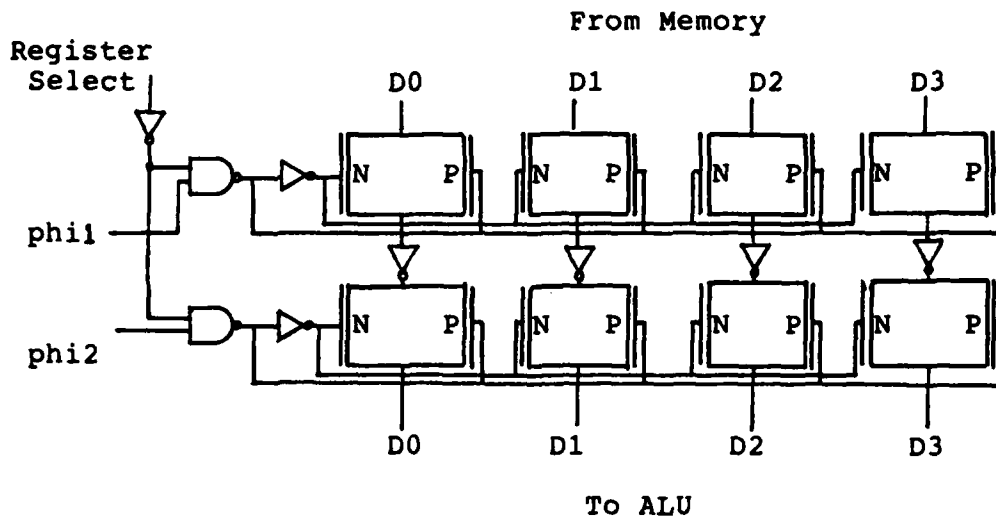
Figure VI-10. B register schematic.
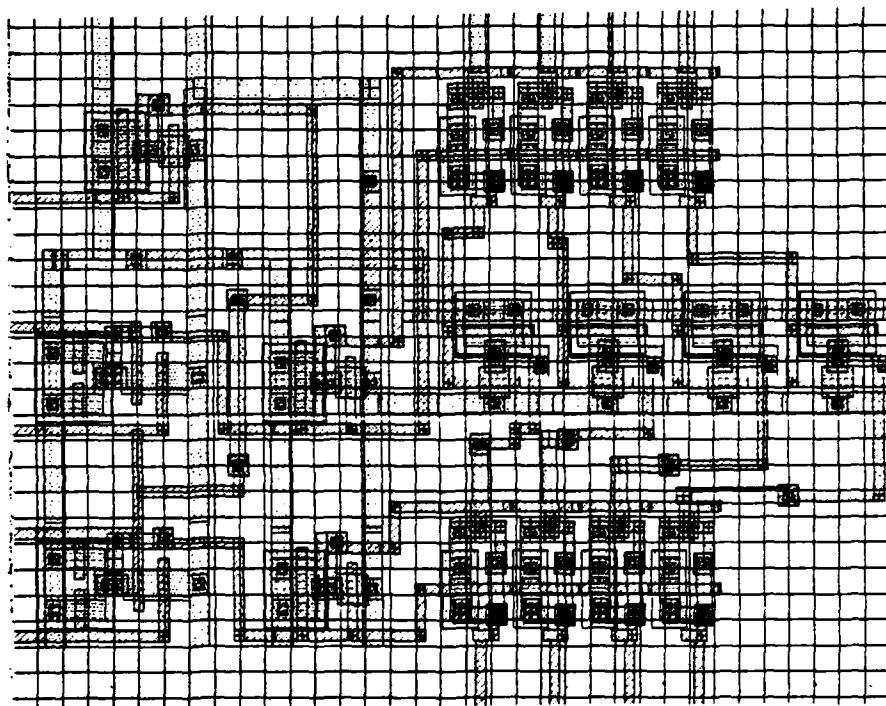
Figure VI-11. CLL Layout of B Register.

2. Read/Write Controller

The Read/Write Controller determines in which direction data is transferred to or from the 4x4 bit RAM.

Data is written to the memory on phi 2 and when the
read/write line is high. Data must be available on the data
input lines D0 - D3. Both the inverted and non-inverted
data values are written into the memory cells. Data is read
from the memory on phi 2 when the read/write line is low.
Data is read only from the non-inverted data line of the
memory cell. The schematic diagram for this circuit is
shown in Figure VI-12.
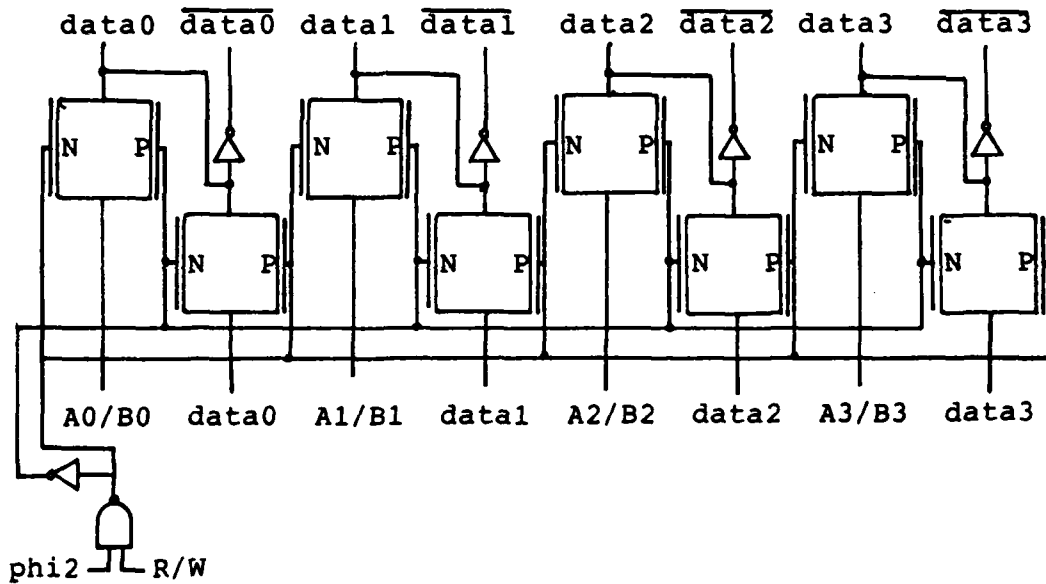
Figure VI-12. Read/Write Controller schematic diagram.

A CLL layout of the Read/Write Controller is shown in Figure
VI-13.
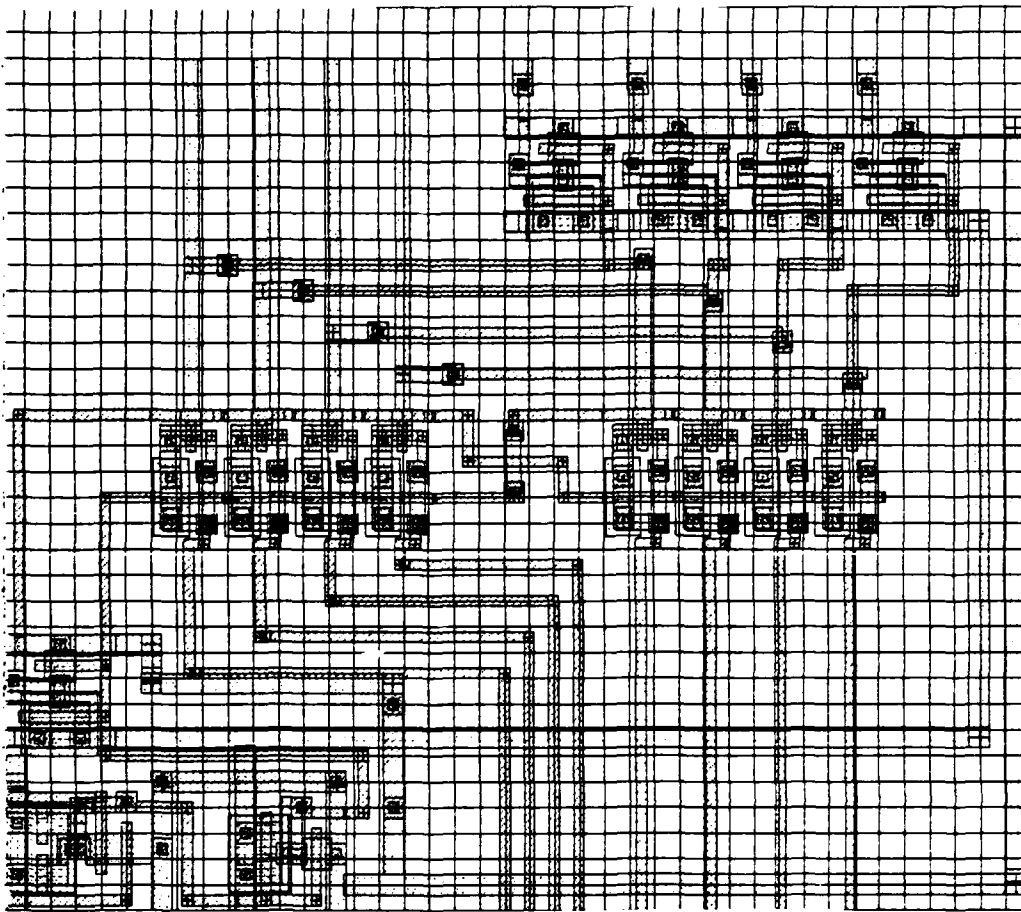
Figure VI-13. CLL layout of Read/Write Controller.

3. ALU Input Controller

The commands to the ALU, S0 - S3 must be applied only after the data has been read from memory into the A and B registers (or just the A register - depending on the function to be performed). The input commands S0 - S3 are passed into this circuit on phi 2 and when register select goes low, indicating that data is being read into the B register, passed along in the A register and eventually out of both registers, the command is passed into the ALU.

The data that was input from the A and B registers (or just the A register - depending upon the command input) is processed. This circuit insures that only valid data is processed. The ALU has a built in level of transmission gates that clock data in on phi 1, therefore this circuit is buffered on its output to insure the charge signal is held until the following phi 1 clock pulse when the S0-S3 inputs are applied to the ALU. A schematic diagram of the ALU Input Controller is shown in Figure VI-14 and a CLL layout is shown in Figure VI-15.
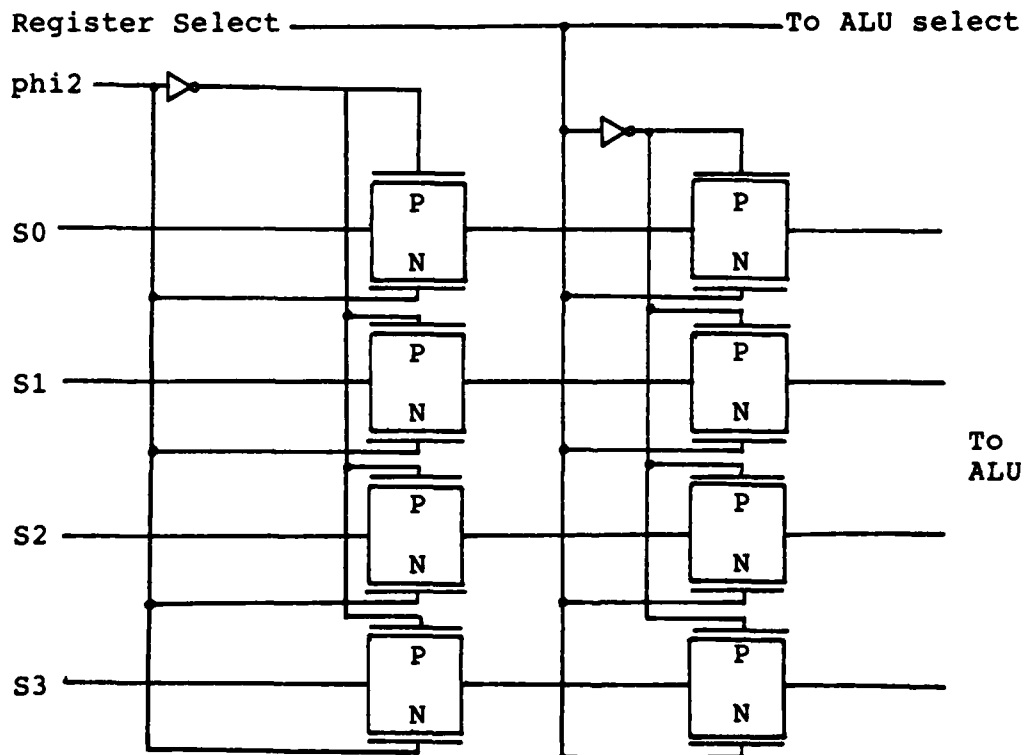
Figure VI-14.   ALU Input Controller schematic.
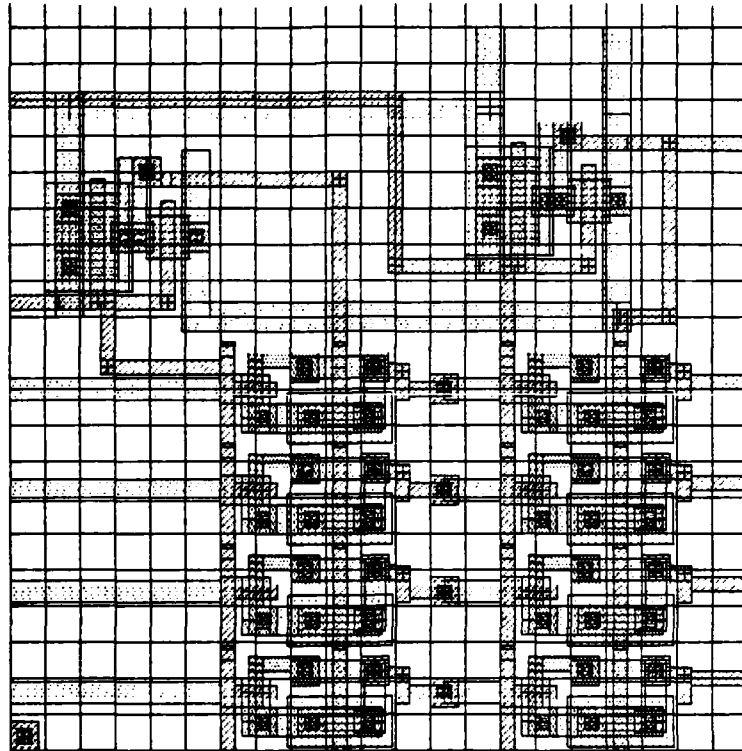
Figure VI-15. ALU Input Controller CLL layout.

4. 4x4 Bit Random Access Memory (RAM)

The memory is composed of the vertical and horizontal iterations of a basic six-transistor static memory cell that is shown in Figure VI-16.
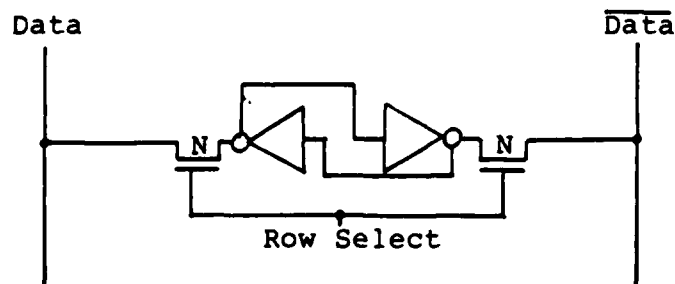
Figure VI-16. Six-transistor memory cell.

The operation of the cell is based on back-to-back inverters connected in a flip-flop configuration. Whenever data is to be written, the row select is set high and the data on the data line and the data bar line is applied to their respective inputs of the flip-flop. This data remains available on the flip-flop indefinitely, may be read at any time and does not require refresh (i.e. a static memory cell).

The CLL layout for the static memory cell is shown in Figure VI-17. This cell is iterated sixteen times to generate the 4x4 bit memory.
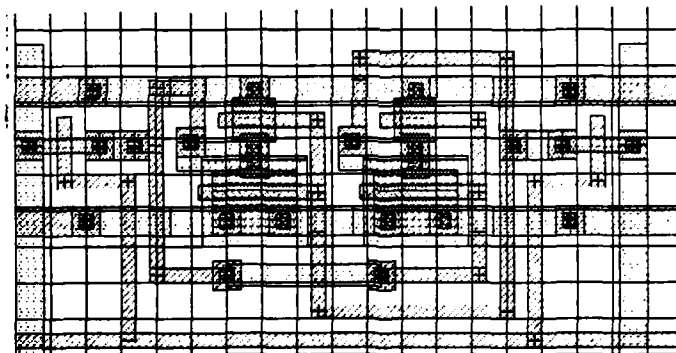
Figure VI-17. Single Bit Memory Cell CLL layout.

5. 2x4 Decoder

The 2x4 memory row decoder provides the row select signal to the row of memory cells that is read from or written to. The schematic diagram of the circuit is shown in Figure VI-18 and a CLL layout in Figure VI-19.
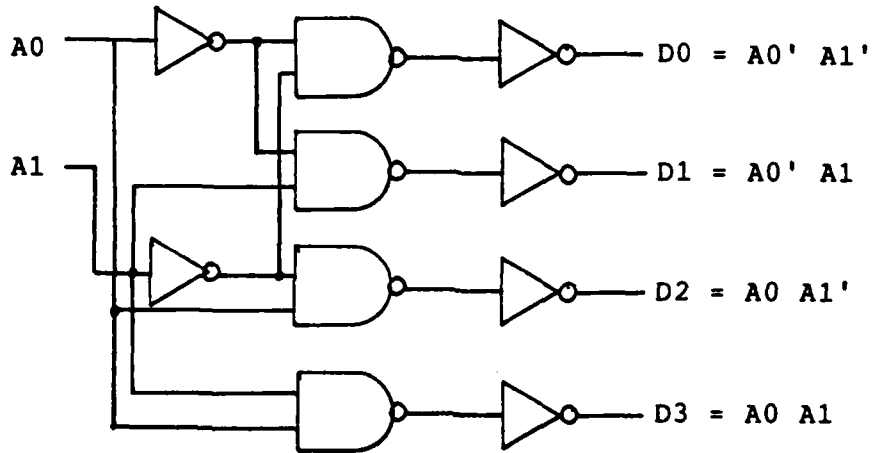
Figure VI-18.   2x4 Decoder schematic diagram.
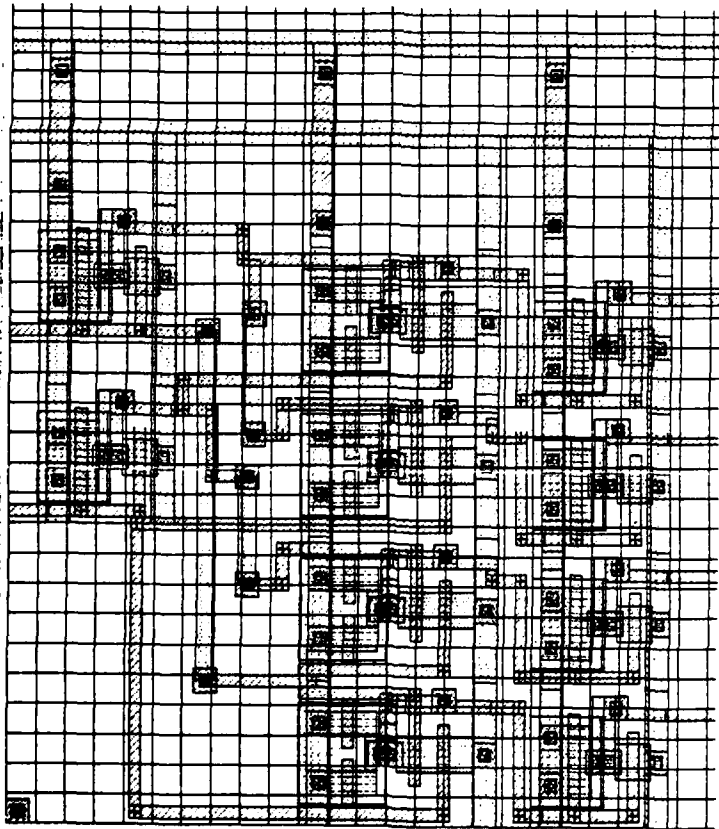
Figure VI-19.   CLL layout of 2x4 Decoder.

C. ALU/Memory Bitslice Precharge

The ALU/Memory was precharged in accordance with the previously presented precharge schemes. For this project, the chip elements that were precharged were the one bitslice of the ALU, the 2x4 row decoder, the A and B registers and the 4x4 bit RAM.

To effectively isolate the interconnections between chip elements and to precharge selected lines efficiently, transmission gates were used on the inputs and outputs of each chip element. Signals are passed on alternating phases of a two phase clock.

The bitslice was precharged as outlined in Secton B and the decoder was precharged as shown in Figure VI-20.
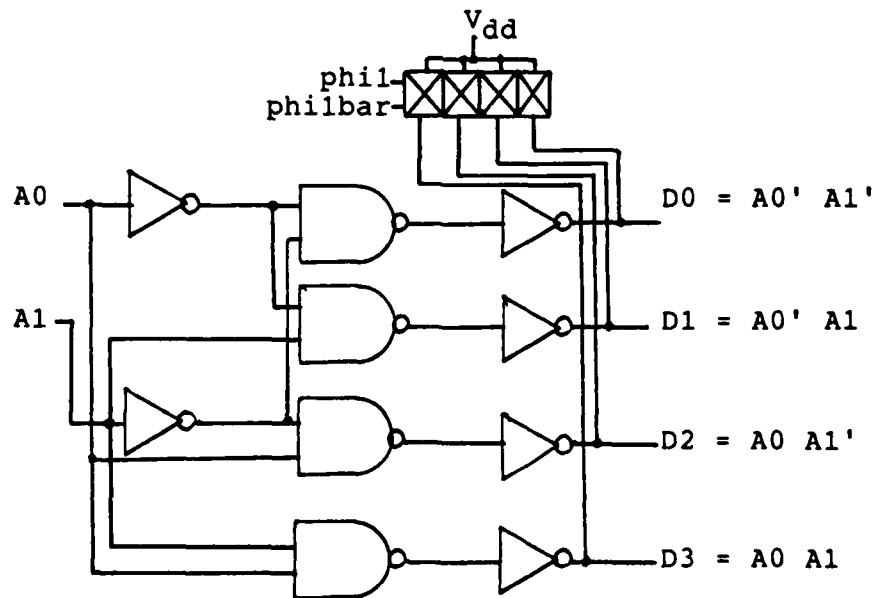
Figure VI-20. Schematic of precharged 2x4 Decoder

Figure VI-21 shows the CLL layout of the decoder circuit.
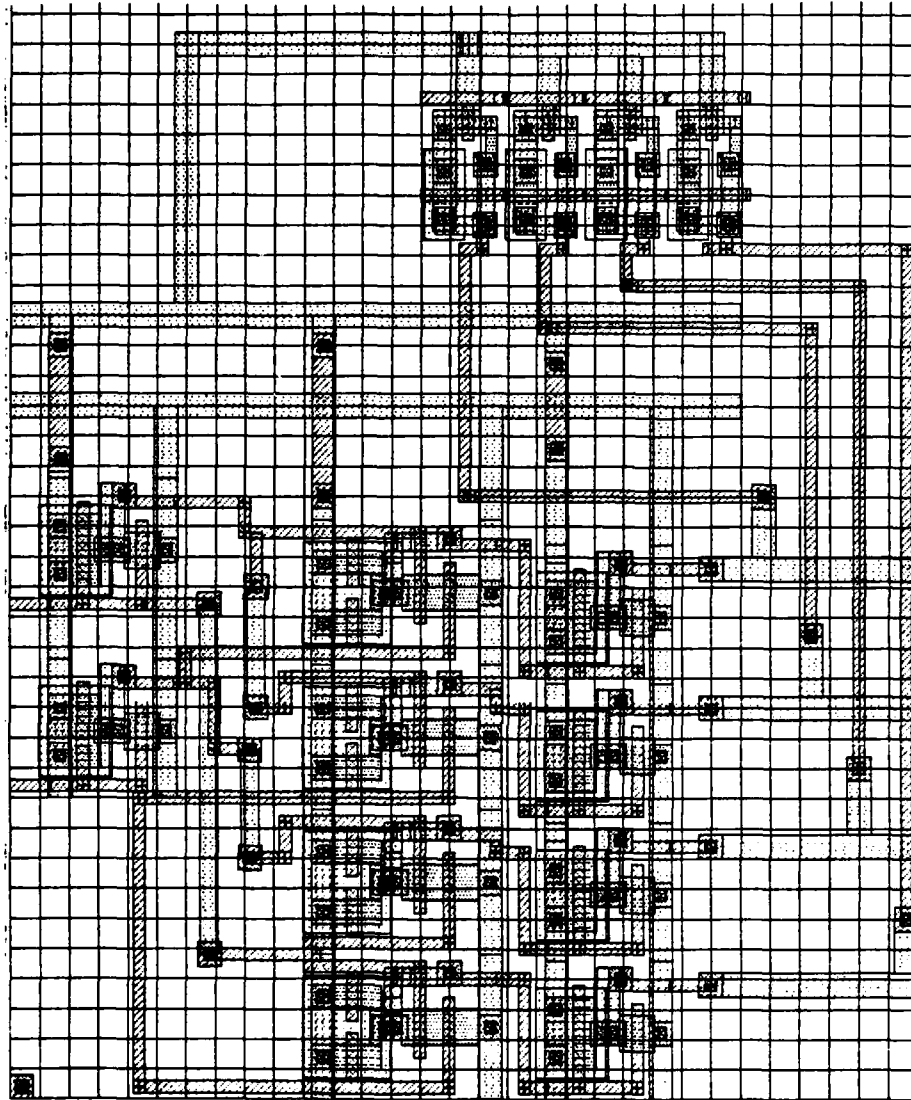
Figure VI-21. 2x4 Precharged Decoder Circuit.

The only change to the basic RAM, in addition to one
transmission gate for each of the four data lines, was the
addition of inverters on the data output lines to the
registers to isolate the precharge on the output lines. If
this isolation did not occur, the data lines, of the

individual flip-flop memory cells, would change to all high states if the data lines were directly precharged. The A and B registers were designed to compensate for the additional inverter on the output lines from the memory.

The corresponding schematic diagram and CLL layout for the precharged memory are provided in Figures VI-22 and VI-23 respectively.
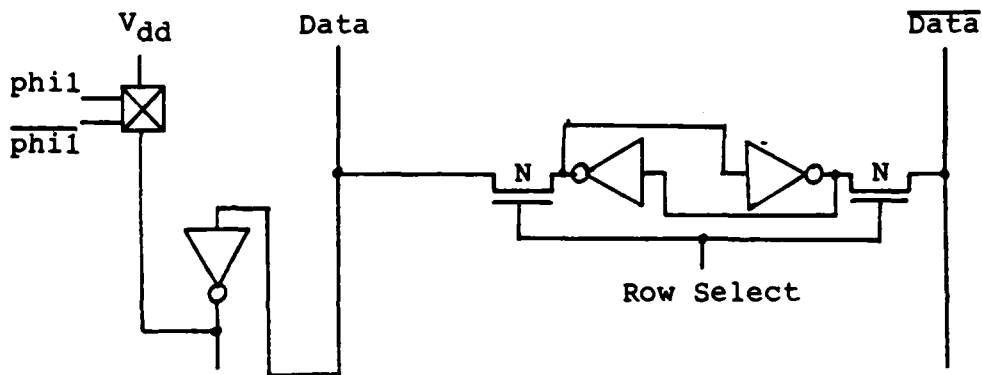
Figure VI-22. Schematic of precharged memory.
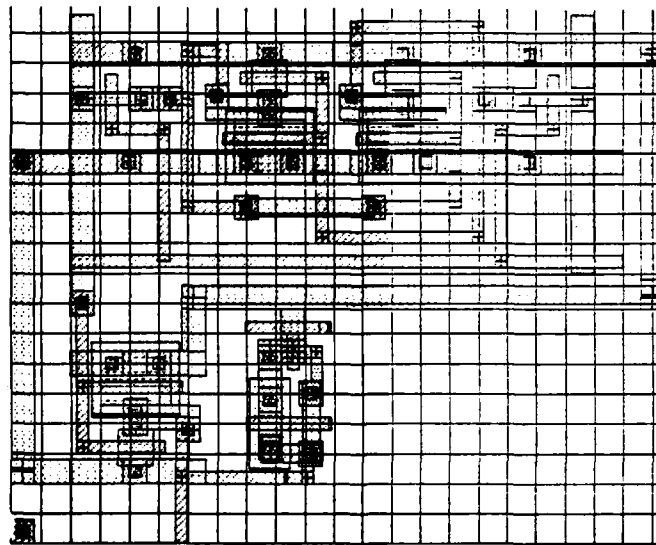
Figure VI-23. CLL layout of precharged memory cell.

The registers were precharged on their outputs only using one transmisiion gate for each output line. The schematic diagrams and CLL layouts for each register are presented in Figures VI-24 through VI-26.
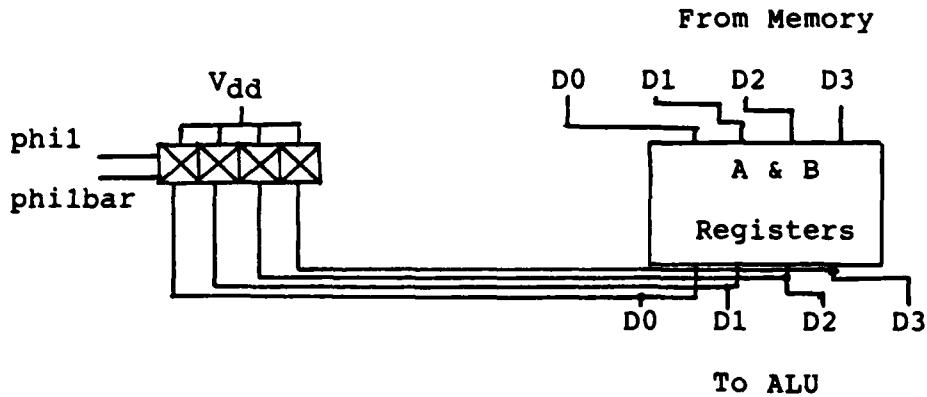
Figure VI-24. Precharged A & B register schematic.
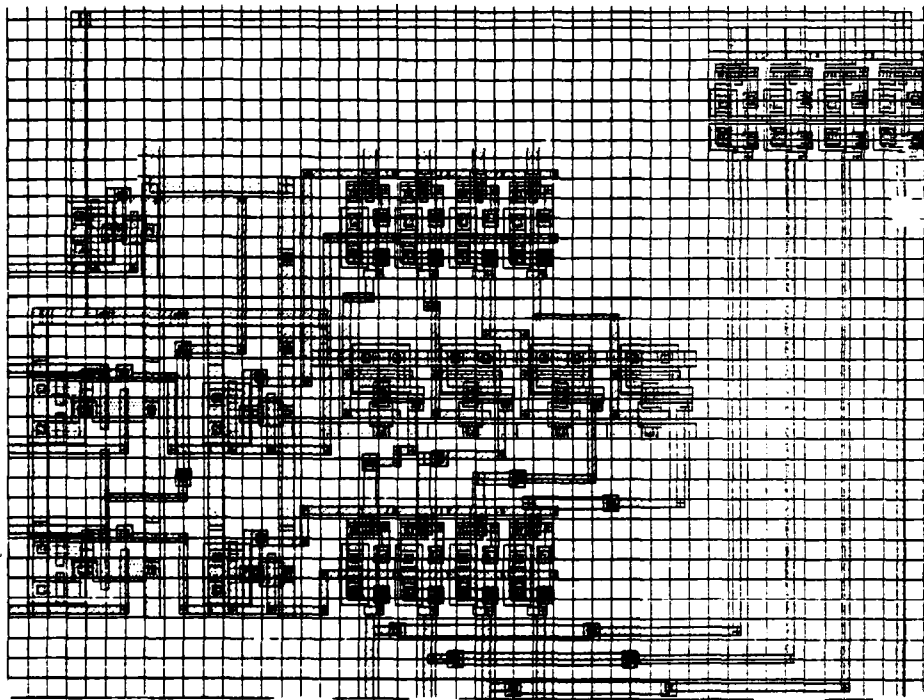
Figure 25.   CLL layout of Precharged B register.
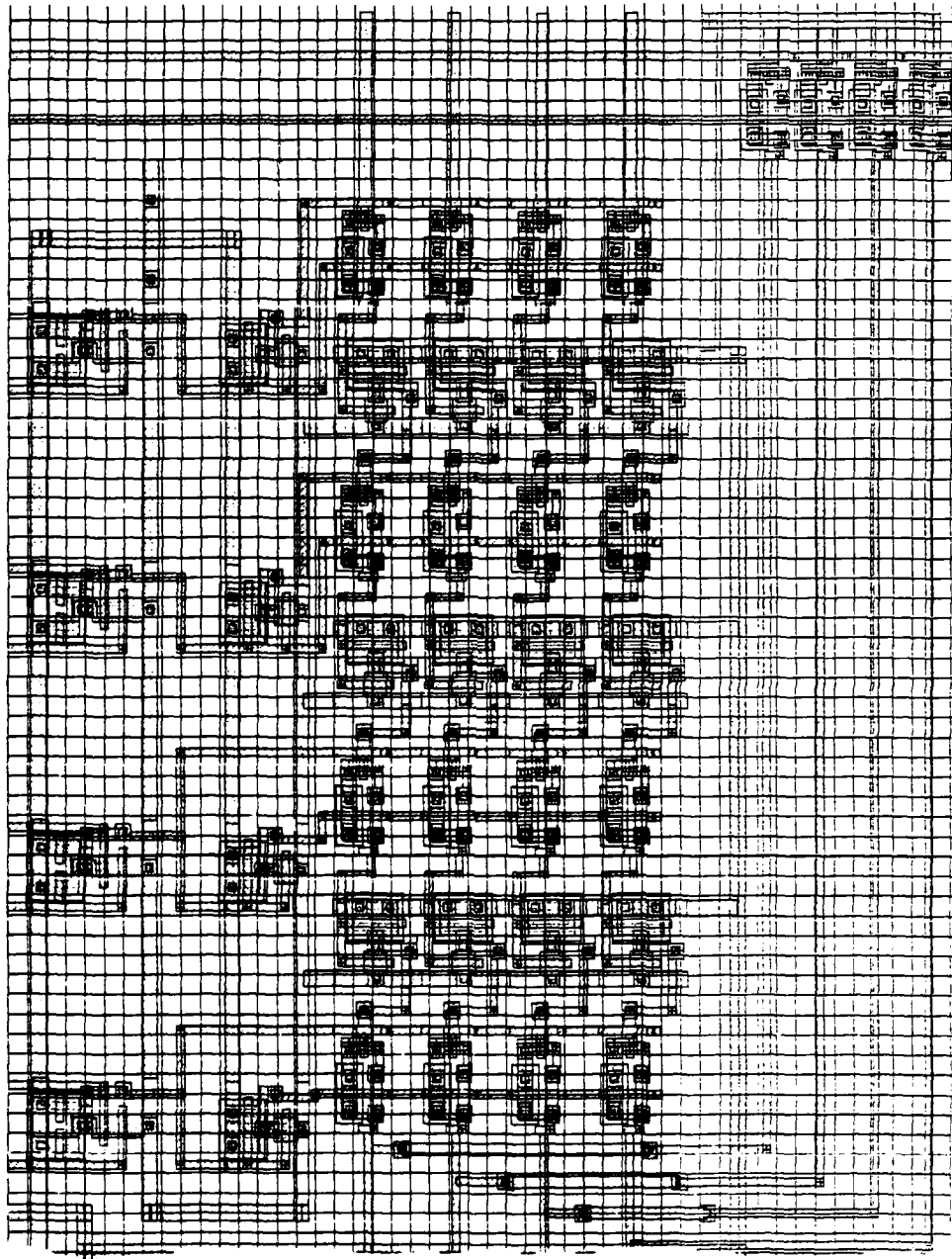
Figure VI-26. CLL layout of precharged A register.

The Memory/ALU Bitslice design presented here demonstrated a practical application to at least a part of Sommars' ALU, offered a larger circuit in which to demonstrate the technique of precharging, and demonstrated the application of precharging to an existing circuit (ALU bitslice) and newly designed circuits (2x4 decoder and RAM). The decoder, RAM and the registers were selected as candidates for precharge since these elements are traditonally slow devices. Memory and other storage elements have slow access times and are in most need of speed-up technique application. The ALU input controller and read/write controller were composed primarily of transmission gates used as pass elements, and were not good candidates for precharge application.

To conclude this chapter a detailed schematic diagram of the Memory/ALU Bitslice chip circuit is shown in Figure VI-27.
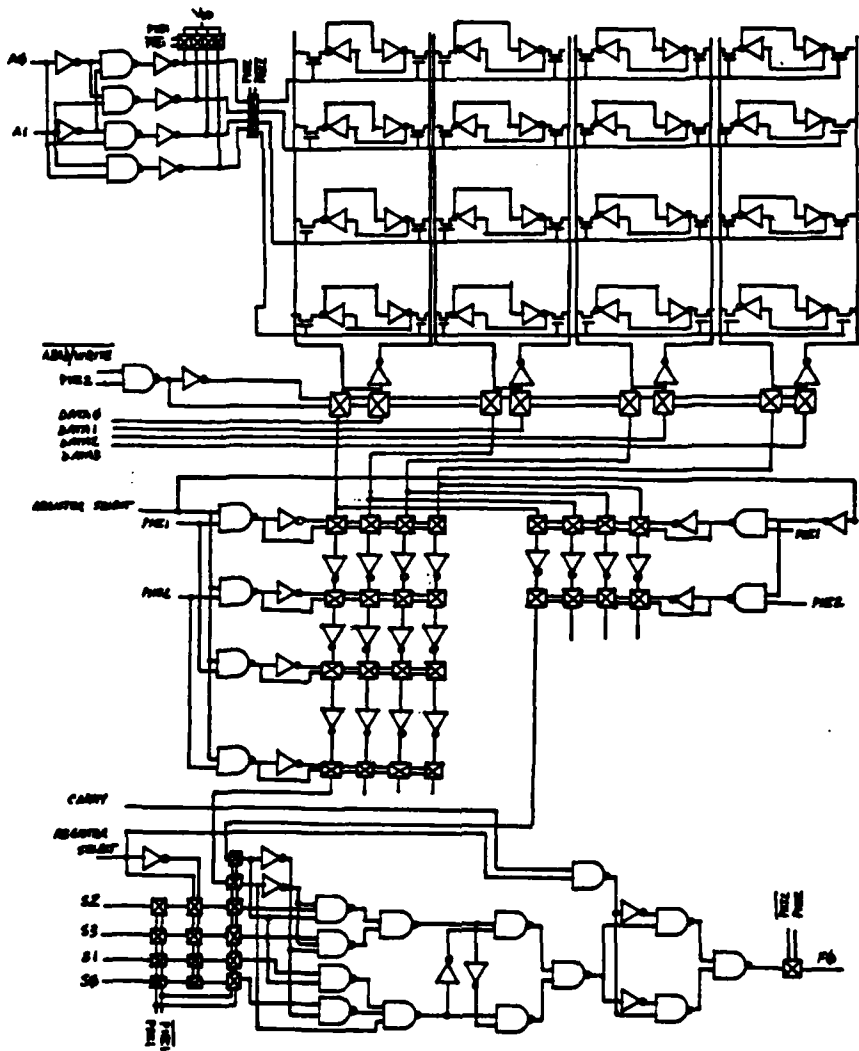
Figure VI-27 Detailed Memory/ALU bitslice circuit
schematic.

VII. Simulation Results Analysis

This chapter reviews the results of the simulations performed on the test circuit presented in Chapter VI, the newly designed circuit elements of the Memory/ALU Bitslice circuit and the first bitslice of the ALU previously designed by Sommars [3].

The intent of this simulation was to determine the validity of the precharging concept as a legitimate method of speeding up circuit operation, to demonstrate the use of precharging in both newly designed and already existing circuit elements, and, given a specific circuit to speed-up, how to most effectively precharge the circuit.

Experience was gained on an incremental basis as more simulations were performed on the different circuits.

Since the design of many of the circuit elements was in process and modifications to the bitslice circuit were being considered in conjunction with the performance of the initial test circuit simulations, the precharged circuit element designs and the precharged bitslice implement precharging in accordance with the results of those initial simulations.

Specific constraints were established for the simulations to evaluate circuit precharge performance and for standardizing the inputs and outputs of the circuits. These criteria are discussed in the following section.

A.   Simulation Scenario Evaluation Criteria

Simulations were performed for each test circuit configuration, each newly designed Memory/ALU bitslice circuit element except the A shift register, and each bitslice section. Each circuit's inputs were selected to generate an output high-to-low transition for one simulation and an output low-to-high transition for the other simulation. This illustrated the effect of precharging on both high and low transitioning signal levels.   Transitioning input waveforms were used to enhance delay analysis.

A 2 nsec precharge pulse width was selected since simulations on the individual gates demonstrated that they switched on the order of 2 nsec, and thus this was considered a valid precharge pulse width based on the expected operating speed of the circuits under simulation. The precharge pulse was applied to selected nodes without isolating the nodes from the rest of the circuit. There is an advantage gained by applying precharge in this fashion to the active circuit. Since the precharge occurs when the circuit becomes active, the requirement to isolate the individual gates/circuit elements when nodes are precharged is reduced. In this way, most transmission gates required for isolation could be eliminated, thus saving space on the chip.

For purposes of simulation, the precharge pulse was delayed (from the start of the input signal sequences) by 4

nsec and "straddled" the 5 nsec transition point of the input waveforms. This insured that the precharge was available when the circuit became active. It was not intended to simulate an actual phase 1 signal of a two-phase clock.

The varying input levels insured a varying output that illustrated the effects of high-to-low and low-to-high transition gate delays for purposes of analysis. The input signals sequences are shown in Figure VII-1. The first signal level (1 or 0) began at 0 nsec and lasted for 5 nsec where it transitioned to either high or low, lasted 10 nsec and then transitioned back to its original value for 25 nsec, for a total signal time of 40 nsec. The same time frames for the precharge and input pulses were used for each simulated circuit configuration to permit direct comparison of results.

```
1st Simulation
  (Identical           ┌────────────────────────┐
   010 nand       0    │           1            │        0
   inputs)      ───────┘                        └──────────

2nd Simulation ────────┐                        ┌──────────
  (Identical           │                        │
   101 nand       1    │           0            │        1
   inputs)             └────────────────────────┘

                       ┌──┐
Precharge        0     │ 1│             0
               ────────┘  └──────────────────────────────

Time(nsec)   0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 -- 40
```
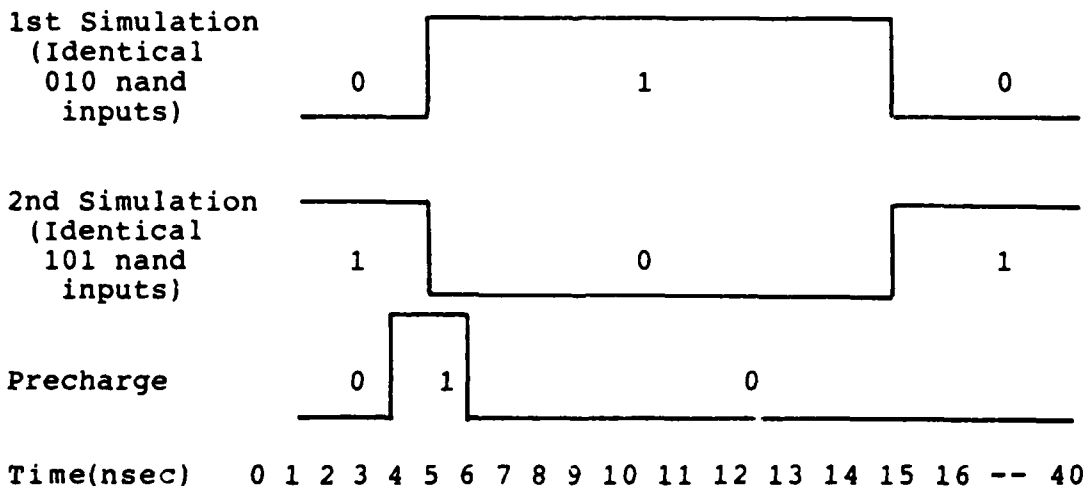
Figure VII-1. Test circuit input waveforms.

VII-3

All input waveforms were "ideal" with no delays
(instanteous level transitions). This simplified the delay
analysis. Circuit delays for each simulated circuit were
determined with respect to the ideal input waveforms as they
transition from high-to-low or low-to-high at the 5 nsec
point. For this analysis, all the circuit delays presented
are measured with respect to the 5 nsec ideal transition
point on the time scale.

For purposes of delay evaluation, "valid" high and low
signal level thresholds were established. For a signal that
was transitioning from low-to-high, the delay was determined
as the time required for the signal to reach 3.75 volts DC
measured from the 5 nsec ideal time point on the time axis
of the SPICE waveform plot (0 to 75% V_{max} output signal
swing). For a signal that was transitioning from low-to-
high, the delay was determined as the time required for the
signal to reach 1.25 volts DC measured from the 5 nsec point
on the time axis of the SPICE waveform plot (100% to 25%
V_{max} output signal swing).

SPICE simulation data are provided in Appendix A, B and
C for the test circuit configurations, the Memory/ALU
Bitslice circuit elements and the sections of the bitslice
respectively.

Also included in the appendices, for each simulated
circuit configuration, is a numbered node cifplot and
SPICE/mextra node cross reference provided to aid the reader

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in following this analysis and for future duplication of the simulations presented in this thesis.

B. General Observations

Some general observations can be made from review of the SPICE data.

The 2 nsec precharge pulse is clearly visible on many of the waveform plots as a high transitioning spike around the 5 nsec point on the time axis. In many cases the pulse fails to cause the circuit to switch because the circuit was active (beginning to perform its function, based on the input), at the time the pulse was applied. The output waveforms display the effect of the precharge, both when it is suppressed (circuit trying to reach 0 volts) and also when the waveform is transitioning high after the precharge has been applied.

In order to provide an adequate precharge pulse to the selected precharge nodes, oversized transmission gates were used to provide enough current to precharge the nodes. This was accomplished by increasing the gate widths of the transmission gate PMOS and NMOS devices.

Simulations were performed using different widths for the transmission gates. The cases where the widths were increased shows a considerable increase in the strength of the precharge pulse as it was applied to the different nodes. Simulations were performed using gate widths two, three and four times the width of the basic transmission gates designed by Sommars.

The test circuit simulations were performed with transmission gates four times the basic gate width, and the chip elements and bitslice sections were simulated using gate widths of one, two and three times the basic gate widths. These simulations were performed to demonstrate that when a sufficiently large current pulse could be provided, the precharge method did indeed precharge the specific nodes as desired. However, due to the capacitance of interconnect wiring, addition of precharge circuitry can slow the circuit down. This effect can be eliminated if the circuitry is laid out with short wiring runs and consideration is given to insuring sufficiently large transistor sizes within the precharge circuit.

C. Test Circuit Simulation

The test circuit described in Chapter VI was composed of a single nand gate and two inverters in series. This test circuit was implemented with the CMOS/SOS gates available in Sommars' library. The test circuit simulations were performed to demonstrate the basic technique of precharging, to determine its impact on positive and negative signal transitions, and from these results determine a methodology for applying precharging to circuits in general. The results of these initial simulations were applied to the Memory/ALU Bitslice circuit element and Bitslice section simulations. Twelve separate simulations were performed on the test circuit. Two initial simulations

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(one for a high-tolow signal transiton and the other for a
low-to-high signal transition) were run on the circuit,
before any precharging techniques were applied, to establish
a baseline to which the other simulation results could be
compared. Three nodes were available for precharge
application, the output of the nand gate, the output of the
first inverter and the output of the second inverter. The
remaining ten simulations selectively precharged these
outputs individually or in combinations.

For the test circuit, the inputs to the nand gate were
selected to provide a low-going pulse, 101, at the output
(identical nand inputs of 010) for the first simulation and
to provide a high going pulse 010 at the output (identical
nand inputs of 101) for the second simulation. The
outputs from the nand and both inverters were monitored and
plotted for each SPICE simulation. On each waveform plot,
the nand output is depicted by the equal sign (=) waveform,
the first inverter output by the plus sign (+) waveform and
the second inverter output by the asterisk (*) waveform. Of
primary interest is the second inverter output waveform.
Since this is the final circuit output it suffers from the
total circuit delay generated by the circuit and is the
signal provided to subsequent circuits or circuit elements
in a more complex circuit configuration.

1. Basic Test Circuit

The SPICE simulation data is provided on pages A-3
through A-7 of Appendix A.

The delays associated with the input signals' first
transition for this circuit simulation are presented in
Table VII-1.

Table VII-1

Basic Test Circuit Delays

Nand Inputs	Nand Output (nsec)	First Inverter Output (nsec)	Second Inverter Output (nsec)
010	2.5	3.0	4.0
101	1.5	2.5	3.0

2. Precharging Nand Output

The delaytimes presented in Table VII-2 were
determined from the SPICE waveform data in Appendix A, pages
A-8 through A-12.

Table VII-2

Test Circuit Delays with Precharged Nand Output

Nand Inputs	Nand Output (nsec)	First Inverter Output (nsec)	Second Inverter Output (nsec)
010	5.5	6.0	7.0
101	0.5	1.5	2.0

Results

The nand output high-to-low transition delay is
increased, which substantially delays the transition for
each subsequent gate output. The nand output low-to-high

transition delay is reduced by 1.0 nsec, which causes an earlier transition in each subsequent gate, when compared to the basic test circuit.

3. Precharging First Inverter Output

The SPICE data for this circuit simulation is provided in Appendix A, pages A-13 through A-17. The delay times of interest to this analysis are presented in Table VII-3.

Table VII-3
Circuit Delays - Precharged First Inverter Output

Nand Inputs	Nand Output (nsec)	First Inverter Output (nsec)	Second Inverter Output (nsec)
010	3.0	1.5	2.0
101	2.0	3.5	4.5

Results

The nand output high-to-low transition delay is increased while the transition times are reduced for both inverter outputs. The nand output low-to-high transition delay and each subsequent gate output transition times are all increased.

4. Precharging Second Inverter Output

The SPICE data for this circuit simulation is provided in Appendix A, pages A-18 through A-22. The delay times for the circuit are presented in Table VII-4.

Table VII-4
Circuit Delays - Precharged Second Inverter Output

Nand Inputs	Nand Output (nsec)	First Inverter Output (nsec)	Second Inverter Output (nsec)
010	2.5	3.5	9.0
101	1.5	2.5	5.5

Results

For the nand output, high-to-low transition, the first inverter output shows a 0.5 nsec delay increase, while the second inverter output delay increases by 5.0 nsec, as compared to the basic test circuit.

For the nand output low-to-high transition delay, the nand and first inverter outputs occur at the same time as for the basic test circuit, however the second inverter output transition time is increased by 2.5 nsec.

Examination of the extracted circuit parameters, used in the SPICE simulation, shows that the addition of the precharge circuitry to the output of the second inverter increased the load capacitance by a factor of seven, thus slowing down the transitions greatly.

5. Precharging Nand and First Inverter Outputs

The SPICE data for this simulation is provided
in Appendix A, pages A-23 through A-27. The circuit delays
are presented in Table VII-5.

Table VII-5

Circuit Delays - Precharged Nand and First Inverter Outputs

Nand Inputs	Nand Output (nsec)	First Inverter Output (nsec)	Second Inverter Output (nsec)
010	5.5	6.5	7.5
101	0.5	3.0	4.0

Results

The precharge increases the delay for the nand output
high-to-low transitioning signal which then degrades the
transition time for both subsequent inverters. Although a
1.0 nsec delay reduction is achieved at the nand output for
its low-to-high transitioning signal, both the first and
second inverter output delays increase by 0.5 and 1.0 nsec
respectively, due to the detrimental effect of the precharge
on the first inverter output high-to-low transition.

6. Precharging Nand and Second Inverter Outputs

The SPICE data for this circuit simulation is
provided in Appendix A, pages A-28 through A-32. The
circuit delays are presented in Table VII-6.

Table VII-6

Precharged Nand and Second Inverter Output

Nand Inputs	Nand Output (nsec)	First Inverter Output (nsec)	Second Inverter Output (nsec)
010	5.5	6.0	11.5
101	0.5	1.5	3.5

Results

The nand output high-to-low transition delay and hence the subsequent inverter transition times are significantly increased by the application of precharge. The nand output low-to-high transition delay is reduced and hence the first inverter outputs also. However, in spite of the precharge signal, a 0.5 nsec delay increase is evidenced at the output of the second inverter due to the previously mentioned large capacitance load created at the circuit output by the particular precharge interconnection.

Overall Results

As already discussed, the output of the second inverter is of primary interest. If its delay can be reduced, by reducing the delays of the gates affecting that node, then the overall speed of the circuit can be increased.

The second inverter output delays are presented again together in Table VII-7. The respective increases or decreases in delay times are shown as percentages.

<div align="center">

Table VII-7

Total Circuit Delays

</div>

Nand Input	Total Circuit Delay (nsec)	Node Precharged	Delay Change
010	4.0	none	baseline (no change)
101	3.0	none	baseline (no cahnge)
010	7.0	NAND	+75.0%
101	2.0	NAND	-33.3%
010	2.0	INV1	-50.0%
101	4.5	INV1	+50.0%
010	9.0	INV2	+125.0%
101	5.5	INV2	+83.3%
010	7.5	NAND,INV1	+87.5%
101	4.0	NAND,INV1	+33.3%
010	11.5	NAND,INV2	+187.5%
101	3.5	NAND,INV2	+16.7%

D. Memory/ALU Bitslice Circuit Element Simulation

Three elements of the Memory/ALU Bitslice circuit were simulated; the decoder, the B register, and a single static RAM cell. The data from the SPICE simulations for each of these elements is provided in Appendix B.

1. 2x4 Decoder Simulation

Three decoder configurations were simulated, the basic decoder to establish a baseline for comparison, the decoder with precharge of each nand-inverter interconnect line, and the decoder with precharge of each output line. Three output lines were monitored for each

simulation. On the SPICE waveforms, the 00 selected line is represented by the asterisk (*), the 11 selected output line is represented by the plus (+) sign, and the 01 selected output line is represented by the equal (=) sign.

The inputs to the decoder are identical 010 pulses. Onlyone simulation was performed for each configuration, since the 00 and 11 select lines are monitiored and the 010 inputs cause a high-to-low and a low-to-high transiton on the same SPICE output plot.

The 010 input waveform is of the same format as presented in the sample waveforms in Figure VII-1.

A 010 input to each decoder input corresponds to a selection of the 00 output line, then the 11 output line, and then the 00 output line again.

For each simulation, the 01 and 10 output line should remain constantly low for all the simulations since the input never causes either one to be selected. For the decoder simulations it can be seen that the 01 output line was constantly low, indicating that the decoder operated correctly for non-selected lines, based on the decoder input, since the line was never selected (never went high).

For the precharge configurations, simulations were performed for precharge transmission gate device widths using the basic widths, and two and three times the basic widths. The intent is to show the effect of a deficiency of current (narrow width transmission gate) and increasingly larger current precharge pulses (wider gate transistors) on

the effectiveness of the precharge technique. In the
tables, results from circuits using transmission gates
transistors with these dimensions are represented by x1
(times 1), x2 (times 2) and x3 (times three) respectively.

    a. Basic Decoder Simulation
        (Refer to Figures B-6)

       To determine decoder delay times, the analysis
was performed by first observing the transition of the
output lines as the two decoder inputs changed from 00 to 11
(based on an input sequence of 010 at both inputs). After
the decoder input changes to 11 at the 5 nsec point, the 11
selected output line reaches the 3.75 volt minimum value at
the 9.0 nsec point. The 00 output line achieves the 1.25
volt, non-selected condition at the 9.0 nsec point. This
data is tabulated in Table VII-8.

Table VII-8

Basic Decoder Delays

Inputs	High-to-Low Delay	Low-to-High Delay
010	4.5 nsec	4.0 nsec

    b. Precharged Decoder
        (Refer to Figures B-4 through B-10)

       Two different precharge configurations were
simulated to determine the best approach to precharging the
decoder. These simulation results demonstrate the need to
carefuly select the nodes to be precharged within individual
circuits and circuit elements.

1. <u>Precharged Decoder (Internal nodes)</u>
(Refer to Figures B-4 through B-6)

The application of precharge at the internal node between the nand gates and the inverters causes the outputs of all the select lines to be driven low after the precharge. This accounts for the output node high-to-low transition delay reduction for the x2 and x3 gate widths data presented in Table VII-9. The original transmission gate transistor size does not produce an appreciable reduction in transition delay. The low-to-high output transition is degraded due to the precharge causing the outputs to be pulled low during the first part of the input signal.

<u>Table VII-9</u>

<u>Precharged Decoder (Internal node) Delays</u>

<u>Input</u>	<u>Decoder Output Transition Delay</u>					
	<u>High-to-Low</u>			<u>Low-to-High</u>		
	<u>x1</u>	<u>x2</u>	<u>x3</u>	<u>x1</u>	<u>x2</u>	<u>x3</u>
010	4.0	3.5	2.5	7.5	7.5	8.0

2. <u>Precharged Decoder (Output Nodes)</u>
(Refer to Figures B-8 through B-10)

This precharge configuration degrades the performance of the high-to-low transitioning waveform, however, this is not a serious drawback, since it is a "high" select decoder. The low-to-high transition delay is reduced by 1.5 nsec in the best case, and by 0.5 nsec in the worst case, when compared to the basic decoder delay

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results. The results are presented in Table VII-10.

Table VII-10

Precharged Decoder (Output Nodes) Delay

Input	High-to-Low Decoder Output			Low-to-High Transition Delay		
	x1	x2	x3	x1	x2	x3
010	5.0	5.0	5.0	4.0	3.5	3.0

2.B Register Simulation
   (Refer to Figures B-11 through B-16)

   a. Basic B Register
       (Refer to Figure B-12)

       For the basic B register, the output
lines float until 5.5 nsec after the input signal
transitions (input finally propagates to output), then
gradually approach their final values. However, the
monitored high signal output line fails to reach the
minimum 3.75 volt level and the low signal output line fails
to reach the 1.25 volt level. Instead, the high driven
output reaches a maximum value of 3.6 volts at 11.5 nsec
after the input signal transition and the low driven output
reaches a minimum of 1.35 volts at 11.5 nsec after the input
signal transitions. The B register fails to operate
correctly, but the effective signal delays (time to reach
maximum/minimum values) will be used for comparison to the
precharged register configuration delays. These effective

delays are tabulated in Table VII-11.

Table VII-11

B Register Delays

Input	High-to-Low Delay	Low-to-High Delay
1	11.5 nsec	--------
0	--------	11.5 nsec

b. Precharged B Register
(Refer to Figures B-14 through B16)

The circuit fails to operate correctly after the precharge is applied, however the effecs of the precharge are clearly visible on the waveform plot. the precharge favors the low-to-high transitioning signal. The delay (actual and effective) results are presented in Table VII-12.

Table VII-12

Precharged B Register Delays

Input	Delay		
	x1	x2	x3
1	12.0	11.5	7.5
0	12.0	12.0	12.0

3. RAM Cell Simulation
(Refer to Figures B-17 through B-26)

The ram cell was not simulated directly, since simulation of the flip-flop itself would have been necessary and would have unnecessarily complicated the

precharge simulation. The precharge of the RAM cell was set up as a precharge of the "data" line and was designed to take place only during a read of the data, when data is read from the "data" line of the memory cell. With cascaded cells, making up the entire 4x4 memory, the data lines are common to all the RAM cells. To precharge the data line on a read of the memory, isolation of the precharged node is required to prevent the indescriminate writing of a high data signal into the flip-flop memory cells, due to the precharge, when a specific row of the memory was selected. Therefore isolation inverters were added to the data lines of the RAM. These inverters limit the precharge to only the data line outputs.

The simulation of the memory was limited to a single cell with an isolation inverter attached to its data line output. The simulation of the cell entailed application of a signal to the inverter input and a precharge of the inverter output. This represented a selection of the cell on a memory read, the flip-flop data being output to the data line andthedata signal propagating to the isolation inverter output. Therefore, the only delay being simulated was that across the isolation inverter.

The 4x4 memory supplies data to the A and B registers. Since the isolation inverters inverted the data signal from the flip-flop, memory cells, the registers were designed to account for this inversion.

For the precharge configurations, the precharge

simulations were performed for the basic device width

transmission gate, and widths two and three times the basic

width. In the tables, these widths are represented by x1,

x2 and x3 respectively.

a. Basic RAM Cell
(Refer to Figure B-17 through B-19)

A 010 waveform, as presented in Figure

VII-1, was applied to the data line of the RAM cell driving

a 101 output waveform at the output of the inverter. Then a

101 input was applied driving a 010 at the output of the

inverter. The delays are presented in Table VII-13.

TABLE VII-13

Basic RAM Cell Delays

Input	Delay
010	5.5 nsec
101	5.5 nsec

b. Precharged RAM Cell
(Refer to Figures B-20 and B-26)

When the output transitions from high-to-low,

a delay increase results when the precharge is applied.

When the output transitions from low-to-high, the transition

delay is reduced by 0.5, 1.5 and 2.5 nsec respectively for

the original, 2x and 3x widths of the transmission gate

devices. Again the effectiveness of precharging is

increased when the transmission gate transistors are large

enough to supply an appreciable amount of current.

TABLE VII-14

Precharged RAM Cell Delays

Input	x1	x2	x3
		Delay	
010	6.0	6.0	7.0
101	5.0	4.0	3.5

These simulations indicate the following:

- Precharging can enhance the operation of a circuit, i.e. more clearly define high and low signal levels

- The results of precharging must be carefully analyzed to determine if it has any effect on the circuit to which it was applied, i.e. the basic RAM cell circuit displayed no positive or negative effects of precharging for the original size transmission gate, but did show an effect as the transmission gate transistors were increased in size, allowing a greater precharge current pulse.

- Selection of the nodes to which precharge is applied is critical, i.e. as displayed by the two different decoder precharge configurations. One circuit displayed a marked enhancement in operation while the other precharged circuit displyed degraded operation due to the difference in the nodes that were precharged.

D.   ALU Bitslice Simulation

Simulation of the entire bitslice was attempted but failed. The simulator produced error statements. The reason for the failure was not determined. However, incrementally increased circuit size simulations that were performed by adding portions of the bitslice circuit (individual gates), indicated that SPICE was not capable of simulating a circuit that was comprised of more than thirteen gates. As an alternative simulation approach, the bitslice was divided into three separate sections. The bitslice design provided three independent sections that were tested for high and low transitioning output waveforms.

Two different precharge configurations were simulated on the bitslice sections. In the first, all the nodes selected were internal to the individual sections. this included four nodes in the first section, two nodes in the second section and four nodes in the third section.   In the second simulation, the precharged nodes were the respective outputs of each section. Thus only two nodes in the first section, one node in the second section, and one node in the third section were precharged. Simulations using the basic transmission gate transistor width, a transmission gate with a 2x transistor width and a 3x transistor width were perfoormedThe SPICE simulation data are provided in Appendix C. Numbered node cifplots and node cross reference list are also provided in the appendix. For the bitslice section simulations, the input waveforms are of

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the same format as presented in Figure VII-1 and the 3.75 volt and 1.25 volt levels apply to high and low transitioning output signals.

Simulation of the sections of the bitslice completes the basic testing of the precharge concept, since the test circuit was a series combination of gates and the bitslice sections offer parallel combinations of the gates.

To clearly follow this analysis, the reader will need to refer to the appendix.

1. First Section Simulation

The first section of the bitslice requires eight inputs to operate:

A - operator

B - operator

PHI1 - Phase 1 Transmission gate pass signal

PHI1BAR - Inverse of PHI1

S0 -> S3 - ALU Control Inputs

For these simulations these inputs had the following values:

Table VII-15

Section 1 Simulation Input Values

A - 010/101

B - 000

PHI1 - 111

PHI1BAR - 000

S0 - 000

S1 - 000

S2 - 111

S3 - 111

Two simulations were performed, one for A = 101 and the other with A = 010. The ALU control signals S0-S3 caused these inputs to produce outputs of 010 and 101 (the inverse of whatever A was) respectively. The same outputs existed at each of the two section 1 output nodes. Although the outputs from each node were logically the same, they were not identical since one output came from a two-input nand gate and one came from a three-input nand gate. The two different input sequences for A insured both high and low transitioning waveform outputs for comparison and analysis. On each SPICE waveform output, the two-input nand output is represented by the asterisk (*) waveform and the three-input nand output is represented by the plus sign (+) waveform.

The A input did not *conform* exactly to the waveforms of Figure VII-1 for these simulations. Instead of waiting for 5 nsec for a change from high-to-low or low-to-high, the signal transitions at 0 nsec on the time axis. The input was modified in this manner since initial SPICE waveform outputs indicated that the delays associated with the first section caused an approximate 5 nsec delay before a section one output waveform transition and the output waveform exceeded the 40 nsec total simulation time before reaching equilibrium when the standard 5 nsec delay waveform was used

as input. To encompass the entire waveform the inputs had to be provided at an earlier timeframe during the simulation. The precharge pulse was maintained at the same time frame (4 to 6 nsec). The standard precharge pulse was maintained since the 5 nsec internal circuit delay of the first section permitted the precharge pulse to coincide directly with the output waveform transition when the 5 nsec delay on the inputs was eliminated.

The result of this earlier application of the A input is that the transitions from low-to-high or high-to-low occur slightly earlier than the 5 nsec time point which had been characteristic of the previous simulation waveforms.

For the precharge configurations, simulations were performed with the basic transmission gate, and the transmission gate with its device widths two and three times the widths of the basic transmission gate device widths. These are represented by x1, x2 and x3 respectively in the Data Table VII-16.

a. Basic First Section
   (Refer to Figures C-3 and C-4)

For a 010 input for A, the expected output is a 101 at both monitored output nodes. The 2-input nand gate output is high, then begins its transition to a low threshold. It achieves the 1.25 volt threshold after11.0 nsec. The 3-input nand output achieves the 1.25 volt threshold after 7.5 nsec.

For a 101 A input, a 010 output was expected. The 2-

input nand output reaches the 3.75 volt threshold after 10.5 nsec and the 3-input nand output fails to reach the threshold and reaches a maximum of 2.55 volts after 11.5 nsec.

b. <u>First Section Precharged at Two Output Nodes</u>
(Refer to Figures C-7 through C-12)

For an A input of 010, both the two and the three input nand outputs achieve the 1.25 volt threshold for the simulations.

For a 101 A input, the two-input nand output achieves the 3.75 volt threshold for each simulation, however the three-input nand output only achieves the threshold for the simulation with transmission gate device widths three times the width of the basic transmission gate.

c. <u>First Section Precharged at Four Internal Nodes</u>
(Refer to Figures C-15 through C-20)

For an A input of 010, both outputs achieve the established 1.25 volt threshold.

For a 101 A input, the two-input nand achieves the 3.75 volt threshold, but the three-input nand still fails to achieve the threshold for all the simulations.

Table VII-16 summarizes the delays for the first section of the bitslice.

Table VII-16

First Bitslice Section Delays

A Input	Pre-charge		Output Delays 2-Input Nand/3-Input Nand		
			x1	x2	x3
010	none	6.0/2.5	————	————	————
101	none	5.5/6.5			
010	2 nodes	——————	12.5/9.5	13.0/10.0	13.0/10.0
101	2 nodes	——————	10.5/11.5	8.5/11.5	6.5/7.0
010	4 nodes	——————	10.5/7.5	9.0/6.5	8.5/7.5
101	4 nodes	——————	13.0/11.5	13.0/11.5	13.5/11.5

2. Second Section Simulation

The second bitslice section had only two inputs and was the least complex of the sections. One input was held at a constant high for each simulation while the other was varied to obtain a high and a low transitioning output waveform. The values are presented in Table VII-17. Refer to Figures C-21 and C-22 in Appendix C.

Table VII-17

Section 2 Inputs

```
VIN1 - 111
VIN2 - 010/101
```

These simulation inputs conform to those specified in Figure VII-1.

a. Basic Second Section
(Refer to Figures C-23 and C-24)

With input 010, the expected output was 101. The output reaches the 1.25 volt threshold after 6.0 nsec.

For input 101, the waveform reaches the 3.75 volt threshold after 6.5 nsec.

b. Second Section Precharged at One Output Node
(Refer to Figures C-27 through C-32)

For inputs of 010 and 101 the outputs achieve the established 1.25 and 3.75 volt thresholds. The low-to-high delays are reduced and the high-to-low transition delays are increased.

c. Second Section Precharged at Two Internal Nodes
(Refer to Figures C-35 through C-40)

For 010 and 101 inputs, the output waveforms also achieve the threshold voltages. However, the precharge reduces the delay of the high-to-low transition in this precharge configuration, since the precharge of both inputs to the two-input nand gate drives the output low after the precharge, thereby favoring the high-to-low transition and hindering the low-to-high transition.

Table VII-18 tabulates the delays each of these circuit configurations.

Table VII-18
Second Bitslice Section Delays

Input	Precharge		Output Delay		
			x1	x2	x3
010	none	6.0	____	____	____
101	none	6.5			
010	1 node	----	7.5	7.5	7.5
101	1 node	----	6.0	5.5	4.0
010	2 nodes	----	6.0	4.5	3.5
101	2 nodes	----	9.5	9.5	9.5

3. Third Section Simulation

The third bitslice section had three inputs; a carry bit, an ALU select signal and the input from the second bitslice section. The carry signal was kept constant at zero, the select signal was kept at a constant high and the third input was varied to produce a transitioning waveform at the circuit output. Table VII-19 summarizes the inputs. Refer to Figures C-41 and C-42 in Appendix C.

Table VII-19
Bitslice Third Section Inputs

Carry - 000
Select - 111
VIN1 - 010/101

The expected output is 101 for a VIN1 = 010 and 010 for VIN1 = 101. VIN1 conforms to the waveforms presented in Figure VII-1.

a. Basic Third Section
(Refer to Figures C-43 and C-44)

For a 010 input, the output reaches the 1.25 volt threshold after 7.0 nsec.

For a 101 input, the output reaches the 3.75 volt threshold after 6.5 nsec.

b. Third Section Precharged at One Output Node
(Refer to Figures C-47 through C-52)

For a 010 input, the output delays are all increased by at least 1.5 nsec.

For a 101 input, the output delay is initially increased for the x1 case, but is reduced by 0.5 nsec in the

x3 case.

    c.   <u>Third</u> <u>Section</u> <u>Precharged</u> <u>at</u> <u>Four</u> <u>Internal</u> <u>Nodes</u>
          (Refer to Figures C-55 and C-60)

For the 010 input, all cases reflect an output delay increase of 3.5 nsec.

For an input of 101, the output delay is initially increased by 2.5 nsec for the x1 case, but is reduced by 1.5 nsec for the x3 case when enough current is supplied to the node during precharge.

Table VII-20
Third Section Bitslice Delays

Input	Precharge		Output Delay		
			x1	x2	x3
010	none	7.0			
101	none	6.5			
010	1 node		8.5	8.5	9.0
101	1 node		8.5	7.5	6.0
010	4 nodes		10.0	10.5	10.5
101	4 nodes		9.0	7.0	5.0

E. <u>Results</u> <u>Summary</u>

The results of these simulations indicate the following:

- Precharge reduces the circuit delay when applied to nodes that are transitioning from a low to a high level.

- Precharge has a negative effect when applied to

nodes where the signal level is transitioning from high-to-low.

- Precharge can be applied to both series and parallel combinational circuits.

- In circuits, such as the logic high select decoder, the detremental effect of the precharge on the high-to-low transition is not a serious drawback, since the decoder operates only on high select (low-to-high) transitions. Circuits such as the decoder, and other "high only" type circuits, would benefit from precharge application.

- The effect of the precharge at a node, is dtermined by the amount of current that is applied to the node during the precharge.

- Nodes considered for precharge application must be carefully selected to prevent degradation of circuit operation.

VIII. Conclusions and Reccommendations

A. Conclusions

The intent of this thesis was to investigate and generate a single reference document of techniques to speed-up electronic circuit operation, select a specific technique that could be applied to CMOS/SOS technology, apply the technique to existing and new CMOS/SOS circuit designs, and through simulation, determine if the technique actually speeds up the operation of the circuit to which it was applied, and subsequently determine a methodology for applying the technique to circuits in general.

When reviewing the circuit simulations, it should be emphasized that, overlapping the precharge pulse with the input signal transition is not an accurate reflection of the standard two-phase clocking used in CMOS circuit design at AFIT. This experimental approach insured that the precharge pulse would be available at the time of input signal transition and eased analysis and evaluation of the precharge technique.

1. Activities Performed

The following activities were performed during this thesis:

- Data was collected on known circuit speed-up techniques.

- Precharging (a specific speed-up technique) was

evaluated to determine if it applied to CMOS/SOS circuits
and if it increased circuit operating speed, since it was
the most commonly used method in the literature for speeding
up circuits.

- To expand the AFIT CMOS/SOS technology base, a
chip circuit was designed, using Sommars' CMOS/SOS library,
that made use of the first bitslice of his ALU and required
the design and development of additional circuit elements.

- Precharging was applied to the bitslice, and some
of the newly designed circuit elements.

- SPICE circuit simulation was performed on a test
circuit, the bitslice and the newly designed circuit
elements.

- Through the simulations, precharging was applied
to indivdual circuits and the effects of the precharge were
determined.

2. Circuit Simulation Conclusions

The following conclusions were drawn from the
circuit simulations performed:

- Precharging reduced the delays of signals that
were transitioning from low to high.

- Increased output delay occurs when consecutive
levels of inversion, e.g. the outputs of two series

inverters, are both precharged.

- Precharge can increase the signal delay at a node when the node is subsequently driven low by circuit function.

- Poor selection of candidate precharge nodes can have a detremental effect on circuit operating speed.

- It is difficult to determine which nodes within a circuit to precharge to obtain the maximum benefits of precharge application.

- The results of precharging must be carefully analyzed to determine the effect on the circuit to which it was applied. The addition of precharge circuitry increases the capacitance of the nodes to which the precharge is applied due to the capacitance of the interconnect wiring. To insure the effectiveness of the precharge, a sufficient amount of current must be applied to the selected nodes to overcome this increase in capacitance.

- Since it is difficult to determine which precharge approach to use, either precharging internal nodes or by charging only circuit outputs, then it is essential that circuits under consideration for precharge application be simulated using SPICE or some other method to determine the optimum approach.

3. Suggested Precharge Approach

The following procedure is recommended if a circuit is being considered as a subject for precharge application:

- Select candidate precharge nodes.

- Through signal analysis, determine the signal levels expected at the candidate nodes during normal circuit operation.

- If signals are predominantly high at specific nodes, then these nodes should be considered for precharge. An excellent example of this is the high select 2x4 decoder designed during this thesis.

- If neither high nor low levels dominate, then perform a simulation to determine the effect of precharge and apply precharge in accordance with the simulation results.

- Implement one transmission gate for each node to be precharged and determine the best place to locate the gates, to save maximum chip area.

4. Special Problems Encountered

In addition to these precharge results, several problems were encountered with some of the tools used to prepare the SPICE simulation files.

- SPICE fails to simulate a circuit consisting of more than thirteen gates.

- Available SPICE reference documentation is not adequate, especially in the preparation of input files.

- The extractor, Mextra, fails to correctly calculate the capacitance of output nodes that are "floating poly", and some other node capacitances calculated by Mextra are not obvious when the circuit layout is examined.

B. Recommendations

The following are recommendations for future research on topics related to this thesis:

- Determine why the extractor, Mextra, fails to calculate correct capacitances on outputs when a "floating" polysilicon line is connected and research the algorithm for other node capacitances to verify correct parameters for SPICE analyses.

- Investigate the operation of SPICE and determine its limitations for circuit simulation, specifically, why it simulates only a limited number of CMOS gates

- Since only a limited analysis was performed during this thesis, expand the analysis and apply precharge to more advanced/complex circuits

- Investigate delays in large capacitance lines

- Investigate the impact of implementing the output precharge circuit described in chapter 4, which applies to delay reduction in high capacitance lines

- Simulate the entire bitslice circuit, then simulate Sommars' entire ALU verifying its logical correctness

- Complete the chip design and submit the Memory/ALU Bitslice chip fabrication specifications, and test the operation of the chip after manufacture

- Fabricate portions of the bitslice that were enhanced by precharge and determine the impact of precharge on an actual simple circuit

- Fabricate the output precharged decoder circuit and the basic circuit and determine the effect of precharging on the circuit through physical performance evaluation of the circuit

- Precharge the ALU, then fabricate both the basic and precharged configurations, test each version and compare the results

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Appendix A

SPICE analyses data are presented for the test circuit discussed in Chapter VI. Five different precharge configurations were used to determine the basic function of precharging:

    a. Precharge only the Nand output

    b. Precharge only the first inverter output

    c. Precharge only the second inverter output

    d. Precharge the nand output and the first inverter output at the same time

    e. Precharge the nand output and the second inverter output

A simulation was run on the basic test circuit to act as a baseline for comparison to the precharged configurations.

There were two simulations run for each test circuit configuration. The first was with identical nand input signals pulsed high from 0 - 5NS, low from 5 - 15NS and high from 15 - 40NS. The second simulation inverted the identical inputs to the nand (low - high - low) for the same time frames. A standard precharge pulse was used for each configuration; a high pulse from 4NS to 6NS and low for the remainder of the simulation.

To evaluate the SPICE simulation data, a mextra/SPICE node number cross reference list and a node cifplot are provided for each test circuit configuration. The SPICE

A-1

input data refers to SPICE nodes and the cifplot refers to mextra nodes. In the reference list, the mextra nodes are in the first column and the corresponding SPICE nodes are presented in the second column.

The waveform plots are also based on SPICE reference nodes. To determine which node is being monitored for output, look at the ".PLOT" line of the input listing, find the node number in the "V( )" expression (there may be more than one V() expression, since multiple node output waveforms can be plotted) refer to the node list, look at the right column and find the number you retrieved from the input listing. Then find the corresponding mextra node number and locate this node on the circuit node cifplot. This can be repeated for any node on the input listing or the circuit cifplot.
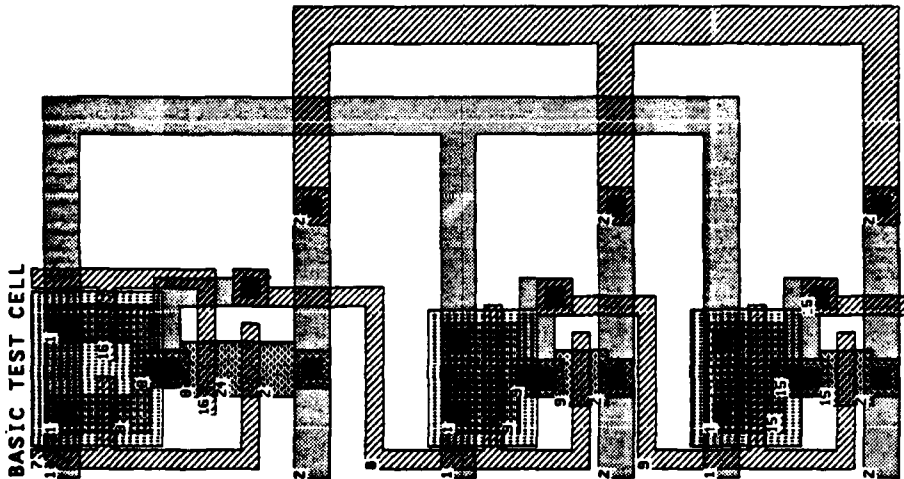
BASIC TEST CELL

Figure A-1.   Basic Test Circuit Node Plot.

Table A-1

BASIC TEST CELL NODE CROSS REFERENCE LIST

GIT	Ø
Vc	1
NMOS	Ø
PMOS	1
8	2
16	3
1	4
2	5
7	6
24	7
15	8
9	9

Ø   CMOS/SOS TEST CELL CONFIGURATION

Ø****   INPUT LISTING   TEMPERATURE =   27.000 DEG C

Ø**

```
.WIDTH OUT=80
.OPTIONS ITL1=500 ITL5=0
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
+LEVEL=1
VDD 1 Ø DC 5V
M1 1 3 2 1 PMOS L=5.0U W=10.0U
M2 7 6 Ø Ø NMOS L=5.0U W=15.0U
M3 2 3 7 Ø NMOS L=5.0U W=15.0U
M4 8 9 Ø Ø NMOS L=5.0U W=15.0U
M5 9 2 Ø Ø NMOS L=5.0U W=15.0U
M6 1 9 8 1 PMOS L=5.0U W=30.0U
M7 1 2 9 1 PMOS L=5.0U W=30.0U
M8 1 6 2 1 PMOS L=5.0U W=10.0U
C9 1 Ø 0.2PF
C10 Ø Ø 0.3PF
C11 2 Ø 0.1PF
C12 9 Ø 0.1PF
C13 8 Ø 0.1PF
VIN1 6 Ø PULSE (ØV 5V 5NS ØNS ØNS 10NS)
VIN2 3 Ø PULSE (ØV 5V 5NS ØNS ØNS 10NS)
.TRAN 0.5NS 40NS
.PLOT TRAN V(8) V(9) V(2) (ØV,5V)
.END
```

```
!*******11/27/84 ********  SPICE 2G.1 (15OCT88)  *********18:82:36*****

#      CMOS/SOS TEST CELL CONFIGURATION

#****     TRANSIENT ANALYSIS                 TEMPERATURE =   27.### DEG C

#******************************************************************

#LEGEND:

*: V(8)
+: V(3)
=: V(2)
X
     TIME       V(8)

X(*+=)----------- #.    d+##    1.25#d+##    2.5##d+##    3.75#d+##  5.###d+##
#.     d+##   5.###d+##  *                 :            :            :          X
5.###d-1#   5.###d+##  *                 :            :            :          X
1.###d-#9   5.###d+##  *                 :            :            :          X
1.5##d-#9   5.###d+##  *                 :            :            :          X
2.###d-#9   5.###d+##  *                 :            :            :          X
2.5##d-#9   5.###d+##  *                 :            :            :          X
3.###d-#9   5.###d+##  *                 :            :            :          X
3.5##d-#9   5.###d+##  *                 :            :            :          X
4.###d-#9   5.###d+##  *                 :            :            :          X
4.5##d-#9   5.###d+##  *                 :            :            :          X
5.###d-#9   5.###d+##  *                 :            :            :          X
5.5##d-#9   5.###d+##  *                 :            :          .  :     .    X
6.###d-#9   5.###d+##  *                 :            :            :          .
6.5##d-#9   5.###d+##  . +               :         .  :     .      :          .
7.###d-#9   4.9##d+##  .          +      :   .      :            :    .      .
7.5##d-#9   4.595d+##  .          .      :        . :          .X           .
8.###d-#9   3.799d+##  .            +    :       .  :            :X        .
8.5##d-#9   2.231d+##  .  +       .      :            :        . :          .
9.###d-#9   8.318d-#1  . = +   .         :            :            :
9.5##d-#9   1.817d-#1  . = +              :            :            :
1.###d-#8   2.883d-#2  X                 :            :            :
1.#5#d-#8   6.949d-#3  X                 :            :            :
1.1##d-#8   1.#31d-#3  X                 :            :            :
1.15#d-#8   2.436d-#4  X                 :            :            :
1.2##d-#8  -3.952d-#5  X                 :            :            :
1.25#d-#8  -8.726d-#6  X                 :            :            :
1.3##d-#8   2.664d-#6  X                 :            :            :
1.35#d-#8  -4.618d-#7  X                 :            :            :
1.4##d-#8  -1.#64d-#7  X                 :            :            :
1.45#d-#8   8.747d-#8  X                 :            :            :
1.5##d-#8   2.151d-#8  X                 :            :            :
1.55#d-#8   2.156d-#8  *                 :            :            :
1.6##d-#8   2.227d-#8  *           .     :            :            :
1.65#d-#8   2.291d-#8  *                 :          . :            :
1.7##d-#8   2.881d-#2  *                 :            :      .X    :
1.75#d-#8   3.982d-#1  *     .        .  :       .    :     .      :     .
1.8##d-#8   1.777d+##  *           .     :      .     :            :        .
1.85#d-#8   3.637d+##  . +               :            :          . :
1.9##d-#8   4.671d+##  .                 :            :            :      .
1.95#d-#8   4.919d+##  .                 :            :            :        .:
2.###d-#8   4.987d+##  *                 :            :            :          X
2.#5#d-#8   4.99#d+##  *                 :            :            :          X
2.1##d-#8   5.###d+##  *                 :            :            :          X
2.15#d-#8   5.###d+##  *                 :            :            :          X
2.2##d-#8   5.###d+##  *                 :            :            :          X
2.25#d-#8   5.###d+##  *                 :            :            :          X
2.3##d-#8   5.###d+##  *                 :            :            :          X
2.35#d-#8   5.###d+##  *                 :            :            :          X
2.4##d-#8   5.###d+##  *                 :            :            :          X
2.45#d-#8   5.###d+##  *                 :            :            :          X
2.5##d-#8   5.###d+##  *                 :            :            :          X
2.55#d-#8   5.###d+##  *                 :            :            :          X
2.6##d-#8   5.###d+##  *                 :            :            :          X
2.65#d-#8   5.###d+##  *                 :            :            :          X
2.7##d-#8   5.###d+##  *                 :            :            :          X
2.75#d-#8   5.###d+##  *                 :            :            :          X
2.8##d-#8   5.###d+##  *                 :            :            :          X
2.85#d-#8   5.###d+##  *                 :            :            :          X
2.9##d-#8   5.###d+##  *                 :            :            :          X
2.95#d-#8   5.###d+##  *                 :            :            :          X
3.###d-#8   5.###d+##  *                 :            :            :          X
3.#5#d-#8   5.###d+##  *                 :            :            :          X
3.1##d-#8   5.###d+##  *                 :            :            :          X
3.15#d-#8   5.###d+##  *                 :            :            :          X
3.2##d-#8   5.###d+##  *                 :            :            :          X
3.25#d-#8   5.###d+##  *                 :            :            :          X
3.3##d-#8   5.###d+##  *                 :            :            :          X
3.35#d-#8   5.###d+##  *                 :            :            :          X
3.4##d-#8   5.###d+##  *                 :            :            :          X
3.45#d-#8   5.###d+##  *                 :            :            :          X
3.5##d-#8   5.###d+##  *                 :            :            :          X
3.55#d-#8   5.###d+##  *                 :            :            :          X
3.6##d-#8   5.###d+##  *                 :            :            :          X
3.65#d-#8   5.###d+##  *                 :            :            :          X
3.7##d-#8   5.###d+##  *                 :            :            :          X
3.75#d-#8   5.###d+##  *                 :            :            :          X
3.8##d-#8   5.###d+##  *                 :            :            :          X
3.85#d-#8   5.###d+##  *                 :            :            :          X
3.9##d-#8   5.###d+##  *                 :            :            :          X
3.95#d-#8   5.###d+##  *                 :            :            :          X
4.###d-#8   5.###d+##  *                 :            :            :          X
```

Figure A-2. SPICE Waveform Plot of Basic Test
            Circuit with Input 010.

A-5

```
*** SPICE DECK CREATED FROM TESTCELL.SIM, TECH=CMOS
.WIDTH OUT=8Ø
.OPTIONS ITL1=5ØØ ITL5=Ø
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
+LEVEL=1
VDD 1 Ø DC 5V
M1 1 3 2 1 PMOS L=5.ØU W=1Ø.ØU
M2 7 6 Ø Ø NMOS L=5.ØU W=15.ØU
M3 2 3 7 Ø NMOS L=5.ØU W=15.ØU
M4 8 9 Ø Ø NMOS L=5.ØU W=15.ØU
M5 9 2 Ø Ø NMOS L=5.ØU W=15.ØU
M6 1 9 8 1 PMOS L=5.ØU W=3Ø.ØU
M7 1 2 9 1 PMOS L=5.ØU W=3Ø.ØU
M8 1 6 2 1 PMOS L=5.ØU W=1Ø.ØU
C9 1 Ø Ø.2PF
C1Ø Ø Ø Ø.3PF
C11 2 Ø Ø.1PF
C12 9 Ø Ø.1PF
C13 8 Ø Ø.1PF
VIN1 6 Ø PULSE (5V ØV 5NS ØNS ØNS 1ØNS)
VIN2 3 Ø PULSE (5V ØV 5NS ØNS ØNS 1ØNS)
.TRAN Ø.5NS 4ØNS
.PLOT TRAN V(8) V(9) V(2) (ØV,5V)
.END
```

```
!********11/27/84 ********  SPICE 2G.1 (15OCT8#)  ********18:#2:47*****

#       CMOS/SOS TEST CELL CONFIGURATION

#****    TRANSIENT ANALYSIS              TEMPERATURE =   27.### DEG C

#**********************************************************************


#LEGEND:

 *: V(8)
 +: V(9)
 =: V(2)
X
     TIME     V(8)

X(*+=)----------- #.    d+##     1.25#d+##     2.5##d+##     3.75#d+##  5.###d+##
                       -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -
 #.   d+##  2.259d-## X                   .            .            .            *
 5.###d-1#  2.259d-## X                   .            .            .            *
 1.###d-#9  2.259d-## X                   .            .            .            *
 1.5##d-#9  2.259d-## X                   .            .            .            *
 2.###d-#9  2.259d-## X                   .            .            .            *
 2.5##d-#9  2.259d-## X                   .            .            .            *
 3.###d-#9  2.259d-## X                   .            .            .            *
 3.5##d-#9  2.259d-## X                   .            .            .            *
 4.###d-#9  2.259d-## X                   .            .            .            *
 4.5##d-#9  2.259d-## X                   .            .            .            *
 5.###d-#9  2.259d-## X                   .            .            .            *
 5.5##d-#9  2.259d-## #         .         .            .            .            *
 6.###d-#9  2.296d-## #         .         .            .            .            +
 6.5##d-#9  2.881d-#2 *         .         .            .          .X             +
 7.###d-#9  3.962d-#1 .    *    .         .        *   +            .        *    .
 7.5##d-#9  1.777d+##  .       *.         .     *      .            .            =.
 8.###d-#9  3.637d+##  .        .  +      .            .            .          *  =.
 8.5##d-#9  4.671d+##  +        .         .            .            .        *    =
 9.###d-#9  4.919d+##  +        .         .            .            .            *=
 9.5##d-#9  4.987d+##  +        .         .            .            .            X
 1.###d-#8  4.998d+##  +        .         .            .            .            X
 1.#5#d-#8  5.###d+##  +        .         .            .            .            X
 1.1##d-#8  5.###d+##  +        .         .            .            .            X
 1.15#d-#8  5.###d+##  +        .         .            .            .            X
 1.2##d-#8  5.###d+##  +        .         .            .            .            X
 1.25#d-#8  5.###d+##  +        .         .            .            .            X
 1.3##d-#8  5.###d+##  +        .         .            .            .            X
 1.35#d-#8  5.###d+##  +        .         .            .            .            X
 1.4##d-#8  5.###d+##  +        .         .            .            .            X
 1.45#d-#8  5.###d+##  +        .         .            .            .            X
 1.5##d-#8  5.###d+##  +        .         .            .            .            X
 1.55#d-#8  5.###d+##  +        .         .            .            .            X
 1.6##d-#8  5.###d+##  +        .         .            .            .            X
 1.65#d-#8  5.###d+##  +        .         .            .          .              *
 1.7##d-#8  5.###d+##  +   .    .         .            .            .            *
 1.75#d-#8  4.968d+##  .     *  .         .         *  .            .            =
 1.8##d-#8  4.595d+##  .        .   *     .            .        +   .            =
 1.85#d-#8  3.799d+##  .        .    *    .            .          .X             +
 1.9##d-#8  2.231d+##  .=       .         .            .        *  .            +
 1.95#d-#8  8.318d-#1  .=   *   .    *    .            .            .            .
 2.###d-#8  1.817d-#1 .=  *     .         .            .            .            .
 2.#5#d-#8  2.883d-#2 X         .         .            .            .            *
 2.1##d-#8  6.949d-#3 X         .         .            .            .            *
 2.15#d-#8  1.#31d-#3 X         .         .            .            .            *
 2.2##d-#8  2.436d-#4 X         .         .            .            .            *
 2.25#d-#8 -3.952d-#5 X         .         .            .            .            *
 2.3##d-#8 -5.726d-#6 X         .         .            .            .            *
 2.35#d-#8  2.684d-#6 X         .         .            .            .            *
 2.4##d-#8 -4.618d-#7 X         .         .            .            .            *
 2.45#d-#8 -1.#84d-#7 X         .         .            .            .            *
 2.5##d-#8  5.747d-#8 X         .         .            .            .            *
 2.55#d-#8  2.151d-#8 X         .         .            .            .            *
 2.6##d-#8  2.#49d-#8 X         .         .            .            .            *
 2.65#d-#8  2.3#3d-#8 X         .         .            .            .            *
 2.7##d-#8  2.265d-#8 X         .         .            .            .            *
 2.75#d-#8  2.256d-#8 X         .         .            .            .            *
 2.8##d-#8  2.259d-## X         .         .            .            .            *
 2.85#d-#8  2.259d-## X         .         .            .            .            *
 2.9##d-#8  2.259d-## X         .         .            .            .            *
 2.95#d-#8  2.259d-## X         .         .            .            .            *
 3.###d-#8  2.259d-## X         .         .            .            .            *
 3.#5#d-#8  2.259d-## X         .         .            .            .            *
 3.1##d-#8  2.259d-## X         .         .            .            .            *
 3.15#d-#8  2.259d-## X         .         .            .            .            *
 3.2##d-#8  2.259d-## X         .         .            .            .            *
 3.25#d-#8  2.259d-## X         .         .            .            .            *
 3.3##d-#8  2.259d-## X         .         .            .            .            *
 3.35#d-#8  2.259d-## X         .         .            .            .            *
 3.4##d-#8  2.259d-## X         .         .            .            .            *
 3.45#d-#8  2.259d-## X         .         .            .            .            *
 3.5##d-#8  2.259d-## X         .         .            .            .            *
 3.55#d-#8  2.259d-## X         .         .            .            .            *
 3.6##d-#8  2.259d-## X         .         .            .            .            *
 3.65#d-#8  2.259d-## X         .         .            .            .            *
 3.7##d-#8  2.259d-## X         .         .            .            .            *
 3.75#d-#8  2.259d-## X         .         .            .            .            *
 3.8##d-#8  2.259d-## X         .         .            .            .            *
 3.85#d-#8  2.259d-## X         .         .            .            .            *
 3.9##d-#8  2.259d-## X         .         .            .            .            *
 3.95#d-#8  2.259d-## X         .         .            .            .            *
 4.###d-#8  2.259d-## X         .         .            .            .            *
                       -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -
```

Figure A-3. SPICE Waveform Plot Of Basic
            Test Circuit with Inputs 101.

A-7

PRECHARGE NAND OUTPUT ONLY

Figure A-4. Node Plot of Test CIrcuit Precharged
at the Nand Output.

Table A-2

PRECHARGE NAND OUTPUT ONLY - NODE REFERENCE LIST

GND	0
Vdd	1
NMOS	0
PMOS	1
03	2
45	3
1	4
3	5
30	6
16	7
2	8
7	9
2	10
15	11
0	12

A-8

```
 .WIDTH OUT=8Ø
 .OPTIONS ITL1=5ØØ ITL5=Ø
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
 +LEVEL=1
 VDD 1 Ø DC 5V
 *M1 1 3 2 Ø NMOS L=5.ØU W=5.ØU
 M2 1 3 5 Ø NMOS L=5.ØU W=2Ø.ØU
 *M3 2 6 1 1 PMOS L=5.ØU W=1Ø.ØU
 M4 5 6 1 1 PMOS L=5.ØU W=4Ø.ØU
 M5 1 7 5 1 PMOS L=5.ØU W=1Ø.ØU
 M6 1Ø 9 Ø Ø NMOS L=5.ØU W=15.ØU
 M7 1Ø 7 5 Ø NMOS L=5.ØU W=15.ØU
 M8 Ø 12 11 Ø NMOS L=5.ØU W=15.ØU
 M9 Ø 5 12 Ø NMOS L=5.ØU W=15.ØU
 M1Ø 1 12 11 1 PMOS L=5.ØU W=3Ø.ØU
 M11 1 5 12 1 PMOS L=5.ØU W=3Ø.ØU
 M12 1 9 5 1 PMOS L=5.ØU W=1Ø.ØU
 C13 1 Ø Ø.425PF
 C14 Ø Ø Ø.3Ø5PF
 C15 5 Ø Ø.243PF
 C16 12 Ø Ø.1Ø9PF
 C17 11 Ø Ø.1PF
 *C18 2 Ø Ø.68PF
 VIN1 7 Ø PULSE (ØV 5V 5NS ØNS ØNS 1ØNS)
 VIN2 9 Ø PULSE (ØV 5V 5NS ØNS ØNS 1ØNS)
 VP1 3 Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS)
 VP2 6 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
 .TRAN Ø.5NS 4ØNS
 .PLOT TRAN V(11) V(12) V(5) (ØV,5V)
 .END
```

0 CMOS/SOS TEST CELL PRECHARGE NAND OUTPUT - INPUT 010 - STANDARD D4.P2

0****   TRANSIENT ANALYSIS   TEMPERATURE =   27.000 DEG C

0***

0LEGEND:

```
*: V(11)
+: V(12)
=: V(5)
X
     TIME      V(11)
X(*+=)----------  0.   d+00    1.250d+00    2.500d+00    3.750d+00 5.000d+00
         0.   d+00   5.000d+00 .                  .                  .         X
         5.000d-10   5.000d+00 +                  .                  .         X
         1.000d-09   5.000d+00 +                  .                  .         X
         1.500d-09   5.000d+00 +                  .                  .         X
         2.000d-09   5.000d+00 +                  .                  .         X
         2.500d-09   5.000d+00 +                  .                  .         X
         3.000d-09   5.000d+00 +                  .                  .         X
         3.500d-09   5.000d+00 +                  .                  .         X
         4.000d-09   5.000d+00 +                  .                  .        XX
         4.500d-09   5.000d+00 +                  .                  .         X
         5.000d-09   5.000d+00 +                  .                  .         X
         5.500d-09   5.000d+00 +                  .                  .         *
         6.000d-09   5.000d+00 +                  .                  .       *
         6.500d-09   5.000d+00 +                  .                  .     *
         7.000d-09   5.000d+00 +                  .                  .   *
         7.500d-09   5.000d+00 +                  .                  .  *
         8.000d-09   5.000d+00 +                  .               *
         8.500d-09   5.000d+00 . +                .            *
         9.000d-09   5.000d+00 .    +             .         *
         9.500d-09   4.987d+00 .       +          .      *
         1.000d-08   4.925d+00 .          +       . **
         1.050d-08   4.425d+00 .            +    *+
         1.100d-08   3.638d+00 .        *     +         .        *          .
         1.150d-08   2.150d+00 .      *          +      .              *
         1.200d-08   8.984d-01 .   *             .     +              .     *
         1.250d-08   1.587d-01 . *               .            +      .
         1.300d-08   2.673d-02 *                 .                +  .
         1.350d-08   5.063d-03 *                 .                   +
         1.400d-08   6.328d-04 *                 .                 *  +
         1.450d-08   1.235d-04 *=                .             *         +
         1.500d-08   9.268d-06 *=                .          *
         1.550d-08   -1.525d-06 *=               .        *
         1.600d-08   -3.085d-07 * =              .      *
         1.650d-08   -5.228d-08 . *              .    *                   +
         1.700d-08   5.864d-09 *                 .  *
         1.750d-08   2.314d-00 *                 .*
         1.800d-08   8.678d-03 .                 . *          *          . +
         1.850d-08   2.519d-01 .      *           .              *
         1.900d-08   9.687d-01 .          *       .                  *
         1.950d-08   2.273d+00 . +            *   .                       *
         2.000d-08   3.847d+00 . +                .      *                   .*
         2.050d-08   4.735d+00 . +                .          *              X
         2.100d-08   4.946d+00 +                  .              *          ::
         2.150d-08   4.999d+00 +                  .                   *     .:
         2.200d-08   4.999d+00 +     _____       .                         ::
         2.250d-08   5.000d+00 +                  .                         ::
         2.300d-08   5.000d+00 +                  .                  .         X
         2.350d-08   5.000d+00 +                  .                  .         X
         2.400d-08   5.000d+00 +                  .                  .         X
         2.450d-08   5.000d+00 +                  .                  .         X
         2.500d-08   5.000d+00 +                  .                  .         X
         2.550d-08   5.000d+00 +                  .                  .         X
         2.600d-08   5.000d+00 +                  .                  .         X
         2.650d-08   5.000d+00 +                  .                  .         X
         2.700d-08   5.000d+00 +                  .                  .         X
         2.750d-08   5.000d+00 +                  .                  .         X
         2.800d-08   5.000d+00 +                  .                  .         X
         2.850d-08   5.000d+00 +                  .                  .         X
         2.900d-08   5.000d+00 +                  .                  .         X
         2.950d-08   5.000d+00 +                  .                  .         X
         3.000d-08   5.000d+00 +                  .                  .         X
         3.050d-08   5.000d+00 +                  .                  .         X
         3.100d-08   5.000d+00 +                  .                  .         X
         3.150d-08   5.000d+00 +                  .                  .         X
         3.200d-08   5.000d+00 +                  .                  .         X
         3.250d-08   5.000d+00 +                  .                  .         X
         3.300d-08   5.000d+00 +                  .                  .         X
         3.350d-08   5.000d+00 +                  .                  .         X
         3.400d-08   5.000d+00 +                  .                  .         X
         3.450d-08   5.000d+00 +                  .                  .         X
         3.500d-08   5.000d+00 +                  .                  .         X
         3.550d-08   5.000d+00 +                  .                  .         X
         3.600d-08   5.000d+00 +                  .                  .         X
         3.650d-08   5.000d+00 +                  .                  .         X
         3.700d-08   5.000d+00 +                  .                  .         X
         3.750d-08   5.000d+00 +                  .                  .         X
         3.800d-08   5.000d+00 +                  .                  .         X
         3.850d-08   5.000d+00 +                  .                  .         X
         3.900d-08   5.000d+00 +                  .                  .         X
         3.950d-08   5.000d+00 +                  .                  .         X
         4.000d-08   5.000d+00 +                  .                  .         X
```

Figure A-5.   SPICE Waveform Plot of Precharged
Nand Output with input 010.

```
1*******11/27/84 ********  SPICE 2G.1 (15OCT80)  ********23:57:23*****

Ø         CMOS/SOS TEST CELL PRECHARGING ONLY THE NAND OUTPUT

Ø****     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

Ø*********************************************************************


 .WIDTH OUT=80
 .OPTIONS ITL1=500 ITL5=Ø
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=Ø.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=Ø.7UM)
 +LEVEL=1
 VDD 1 Ø DC 5V
 *M1 1 3 2 Ø NMOS L=5.ØU W=5.ØU
 M2 1 3 5 Ø NMOS L=5.ØU W=20.ØU
 *M3 2 6 1 1 PMOS L=5.ØU W=10.ØU
 M4 5 6 1 1 PMOS L=5.ØU W=40.ØU
 M5 1 7 5 1 PMOS L=5.ØU W=10.ØU
 M6 10 9 Ø Ø NMOS L=5.ØU W=15.ØU
 M7 10 7 5 Ø NMOS L=5.ØU W=15.ØU
 M8 Ø 12 11 Ø NMOS L=5.ØU W=15.ØU
 M9 Ø 5 12 Ø NMOS L=5.ØU W=15.ØU
 M10 1 12 11 1 PMOS L=5.ØU W=30.ØU
 M11 1 5 12 1 PMOS L=5.ØU W=30.ØU
 M12 1 9 5 1 PMOS L=5.ØU W=10.ØU
 C13 1 Ø Ø.425PF
 C14 Ø Ø Ø.305PF
 C15 5 Ø Ø.243PF
 C16 12 Ø Ø.109PF
 C17 11 Ø Ø.1PF
 *C18 2 Ø Ø.68PF
 VIN1 7 Ø PULSE (5V ØV 5NS ØNS ØNS 10NS)
 VIN2 9 Ø PULSE (5V ØV 5NS ØNS ØNS 10NS)
 VP1 3 Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS)
 VP2 6 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
 .TRAN Ø.5NS 40NS
 .PLOT TRAN V(11) V(12) V(5) (ØV,5V)
 .END
```

```
1********11/27/84 ********  SPICE 2G.1 (15OCT88)  ********23:57:23*****
#        CMOS/SOS TEST CELL PRECHARGING ONLY THE NAND OUTPUT
#****    TRANSIENT ANALYSIS              TEMPERATURE =  27.### DEG C
#*****************************************************************************

#LEGEND:

 *: V(11)
 +: V(12)
 =: V(5)
X
      TIME      V(11)

X(*+=)----------- #.    d+##     1.25#d+##    2.5##d+##     3.75#d+## 5.###d+##
       #.   d+##  2.259d-##  X                .            .            .
       5.###d-1#  2.259d-##  X                .            .            .
       1.###d-#9  2.259d-##  X                .            .            .
       1.5##d-#9  2.259d-##  X                .            .            .
       2.###d-#9  2.259d-##  X                .            .            .
       2.5##d-#9  2.259d-##  X                .            .            .
       3.###d-#9  2.259d-##  X                .            .            .
       3.5##d-#9  2.259d-##  X                .            .            .
       4.###d-#9  2.259d-##  X                .            .            .
       4.5##d-#9  2.259d-##  .          *     .            .            .
       5.###d-#9  2.272d-##  *                .        +   .            *
       5.5##d-#9  2.429d-##  *                .            .    =    *
       6.###d-#5  9.115d-#2  .*               .     +      .    =      *
       6.5##d-#9  1.#72d+##  .           +*   .            .
       7.###d-#9  3.155d+##  .  +             .     *      .         =.
       7.5##d-#9  4.466d+##  .  .+            .            .      *  =.
       8.###d-#9  4.89#d+##  +                .            .          =
       8.5##d-#9  4.976d+##  +                .            .          X
       9.###d-#9  4.996d+##  +                .            .          X
       9.5##d-#9  5.###d+##  +                .            .          X
       1.###d-#8  5.###d+##  +                .            .          X
       1.#5#d-#8  5.###d+##  +                .            .          X
       1.1##d-#8  5.###d+##  +                .            .          X
       1.15#d-#8  5.###d+##  +                .            .          X
       1.2##d-#8  5.###d+##  +                .            .          X
       1.25#d-#8  5.###d+##  +                .            .          X
       1.3##d-#8  5.###d+##  +                .            .          X
       1.35#d-#8  5.###d+##  +                .            .          X
       1.4##d-#8  5.###d+##  +                .            .          X
       1.45#d-#8  5.###d+##  +                .            .          X
       1.5##d-#8  5.###d+##  +                .            .          X
       1.55#d-#8  5.###d+##  +                .            .          X
       1.6##d-#8  5.###d+##  +                .            .          =.
       1.65#d-#8  5.###d+##  +                .            .      =
       1.7##d-#8  5.###d+##  +                .            .  =
       1.75#d-#8  5.###d+##  .+               .         =  .
       1.8##d-#8  5.###d+##  . +              .     =      .
       1.85#d-#8  5.###d+##  .    +           .   =        .
       1.9##d-#8  5.###d+##  .       +        . =          .
       1.95#d-#8  4.954d+##  .          =     *            .
       2.###d-#8  4.76#d+##  .            =       *        .           *
       2.#5#d-#8  3.937d+##  .         =          .   *    .       +
       2.1##d-#8  2.74#d+##  .    =              .        *.       +
       2.15#d-#8  1.351d+##  .  =          *     .            .      +
       2.2##d-#8  3.428d-#1  .  =    *          .            .*
       2.25#d-#8  5.738d-#2  .*=              .            .          *
       2.3##d-#8  1.142d-#2  *=               .            .          *
       2.35#d-#8  2.592d-#3  *=              .            .           *
       2.4##d-#8  3.#83d-#4  *=              .            .           *
       2.45#d-#8  1.#95d-#6  *=              .            .           *
       2.5##d-#8 -1.#53d-#6  *=              .            .           *
       2.55#d-#8  4.571d-#7  *=              .            .           *
       2.6##d-#8  5.244d-#8  X               .            .           *
       2.65#d-#8 -5.293d-#9  X               .            .           *
       2.7##d-#8  2.79#d-#8  X               .            .           *
       2.75#d-#8  2.375d-#8  X               .            .           *
       2.8##d-#8  2.221d-#8  X               .            .           *
       2.#5#d-#8  2.264d-#8  X               .            .           *
       2.9##d-#8  2.261d-#8  X               .            .           *
       2.95#d-#8  2.25#d-#8  X               .            .           *
       3.###d-#8  2.259d-#8  X               .            .           *
       3.#5#d-#8  2.259d-#8  X               .            .           *
       3.1##d-#8  2.259d-#8  X               .            .           *
       3.15#d-#8  2.259d-#8  X               .            .           *
       3.2##d-#8  2.259d-#9  X               .            .           *
       3.25#d-#8  2.259d-#8  X               .            .           *
       3.3##d-#8  2.259d-#9  X               .            .           *
       3.35#d-#8  2.259d-#8  X               .            .           *
       3.4##d-#8  2.259d-#8  X               .            .           *
       3.45#d-#8  2.259d-#8  X               .            .           *
       3.5##d-#8  2.259d-#8  X               .            .           *
       3.55#d-#8  2.259d-#8  X               .            .           *
       3.6##d-#8  2.259d-#8  X               .            .           *
       3.65#d-#8  2.259d-#8  X               .            .           *
       3.7##d-#8  2.259d-#8  X               .            .           *
       3.75#d-#8  2.259d-#8  X               .            .           *
       3.8##d-#8  2.259d-#8  X               .            .           *
       3.#5#d-#8  2.259d-#8  X               .            .           *
       3.9##d-#8  2.259d-#8  X               .            .           *
       3.95#d-#8  2.259d-#8  X               .            .           *
       4.###d-#8  2.259d-#8  X               .            .           *
```

Figure A-6.   SPICE Waveform Plot of Precharged
               Nand Output with Inputs 101.

A-12

Figure A-7. Node Plot of Test Circuit Precharged
at First Inverter Output.

Table A-3

PRECHARGE INV1 OUTPUT ONLY - NODE REFERENCE LIST

GND	Ø
Vcc	1
... S	0
?NOS	1
0	2
41	3
1	4
37	5
3	6
16	7
2	0
7	0
24	1Ø
15	11

A-13

Ø   CMOS/SOS - PRECHARGE INV1 ONLY - INPUT Ø1Ø - STANDARD D4,P2

Ø****   INPUT LISTING   TEMPERATURE =   27.ØØØ DEG C

Ø***

```
 .WIDTH OUT=8Ø
 .OPTIONS ITL1=5ØØ ITL5=Ø
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
 +LEVEL=1
 VDD 1 Ø DC 5V
 M1 1 3 2 Ø NMOS L=5.ØU W=2Ø.ØU
 M2 2 5 1 1 PMOS L=5.ØU W=4Ø.ØU
 M3 1 7 6 1 PMOS L=5.ØU W=1Ø.ØU
 M4 1Ø 9 Ø Ø NMOS L=5.ØU W=15.ØU
 M5 1Ø 7 6 Ø NMOS L=5.ØU W=15.ØU
 M6 Ø 2 11 Ø NMOS L=5.ØU W=15.ØU
 M7 Ø 6 2 Ø NMOS L=5.ØU W=15.ØU
 M8 1 2 11 1 PMOS L=5.ØU W=3Ø.ØU
 M9 1 6 2 1 PMOS L=5.ØU W=3Ø.ØU
 M1Ø 1 9 6 1 PMOS L=5.ØU W=1Ø.ØU
 C11 1 Ø Ø.4Ø5PF
 C12 Ø Ø Ø.3Ø5PF
 C13 6 Ø Ø.129PF
 C14 2 Ø Ø.248PF
 C15 11 Ø Ø.1PF
 VIN1 7 Ø PULSE (ØV 5V 5NS ØNS ØNS 1ØNS)
 VIN2 9 Ø PULSE (ØV 5V 5NS ØNS ØNS 1ØNS)
 VP1 3 Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS)
 VP2 5 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
 .TRAN Ø.5NS 4ØNS
 .PLOT TRAN V(11) V(2) V(6) (ØV,5V)
 .END
```

```
0      CMOS/SOS - PRECHARGE INV1 ONLY - INPUT 010 - STANDARD D4,P2

0****   TRANSIENT ANALYSIS                TEMPERATURE =  27.000 DEG C

0**************************************************************************

0LEGEND:

 *: V(11)
 +: V(2)
 =: V(6)
x
     TIME      V(11)

X(*+=)----------  0.     d+00     1.250d+00     2.500d+00     3.750d+00  5.000d+00
                 - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
 0.     d+00  5.000d+00  +                                                     X
 5.000d-10  5.000d+00  +                                                       X
 1.000d-09  5.000d+00  +                                                       X
 1.500d-09  5.000d+00  +                                                       X
 2.000d-09  5.000d+00  +                                                       X
 2.500d-09  5.000d+00  +                                                       X
 3.000d-09  5.000d+00  +                                                       X
 3.500d-09  5.000d+00  +                                                       X
 4.000d-09  5.000d+00  +                                                       X
 4.500d-09  5.000d+00  .                                                       X
 5.000d-09  4.961d+00  .          +              .              .            X
 5.500d-09  4.773d+00  .                     +        .        +       .
 6.000d-09  4.365d+00  .                              .       +   .    .    X
 6.500d-09  3.445d+00  .                         .       +  .    .  .  +
 7.000d-09  1.978d+00  .                 +  .       .    .    .  . .  +
 7.500d-09  8.471d-01  .          +      .      .         .         .
 8.000d-09  3.174d-01  .       +      .      .          .            .
 8.500d-09  5.494d-02  .+   +      .                              .
 9.000d-09  1.304d-02  .+  .                                         .
 9.500d-09  2.382d-03  * .                                             .
 1.000d-08  4.351d-04  *=                                                .
 1.050d-08  5.927d-05  *=                                                  .
 1.100d-08  6.835d-06  X                                                     .
 1.150d-08 -5.598d-08  X
 1.200d-08  2.170d-08  X
 1.250d-08  2.500d-08  X
 1.300d-08  2.200d-08  X
 1.350d-08  2.253d-08  X
 1.400d-08  2.263d-08  X
 1.450d-08  2.258d-08  X
 1.500d-08  2.259d-08  X
 1.550d-08  2.259d-08  X
 1.600d-08  2.259d-08  *      .                                             .
 1.650d-08  2.265d-08  *                .                 .                  .
 1.700d-08  1.802d-04  *                                        .          +
 1.750d-08  1.305d-03  *                                             +    ++
 1.800d-08  1.067d-01  .*                                            +
 1.850d-08  2.930d-01  .       *                 .          +           .
 1.900d-08  1.211d+00  .                 +         .          .       .    =
 1.950d-08  2.350d+00  .          *      +          .         .          .
 2.000d-08  3.736d+00  .                              .          .
 2.050d-08  4.483d+00  .            *                 .            .
 2.100d-08  4.969d+00  .                                                     X
 2.150d-08  4.995d+00  .*                                                    X
 2.200d-08  4.999d+00  +                                                     X
 2.250d-08  5.000d+00  +                                                     X
 2.300d-08  5.000d+00  +                                                     X
 2.350d-08  5.000d+00  +                                                     X
 2.400d-08  5.000d+00  +                                                     X
 2.450d-08  5.000d+00  +                                                     X
 2.500d-08  5.000d+00  +                                                     X
 2.550d-08  5.000d+00  +                                                     X
 2.600d-08  5.000d+00  +                                                     X
 2.650d-08  5.000d+00  +                                                     X
 2.700d-08  5.000d+00  +                                                     X
 2.750d-08  5.000d+00  +                                                     X
 2.800d-08  5.000d+00  +                                                     X
 2.850d-08  5.000d+00  +                                                     X
 2.900d-08  5.000d+00  +                                                     X
 2.950d-08  5.000d+00  +                                                     X
 3.000d-08  5.000d+00  +                                                     X
 3.050d-08  5.000d+00  +                                                     X
 3.100d-08  5.000d+00  +                                                     X
 3.150d-08  5.000d+00  +                                                     X
 3.200d-08  5.000d+00  +                                                     X
 3.250d-08  5.000d+00  +                                                     X
 3.300d-08  5.000d+00  +                                                     X
 3.350d-08  5.000d+00  +                                                     X
 3.400d-08  5.000d+00  +                                                     X
 3.450d-08  5.000d+00  +                                                     X
 3.500d-08  5.000d+00  +                                                     X
 3.550d-08  5.000d+00  +                                                     X
 3.600d-08  5.000d+00  +                                                     X
 3.650d-08  5.000d+00  +                                                     X
 3.700d-08  5.000d+00  +                                                     X
 3.750d-08  5.000d+00  +                                                     X
 3.800d-08  5.000d+00  +                                                     X
 3.850d-08  5.000d+00  +                                                     X
 3.900d-08  5.000d+00  +                                                     X
 3.950d-08  5.000d+00  +                                                     X
 4.000d-08  5.000d+00  +                                                     X
```

Figure A-8. SPICE Waveform Plot of Precharged
First Inverter with Inputs 010.

A-15

```
.WIDTH OUT=8Ø
.OPTIONS ITL1=5ØØ ITL5=Ø
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
+LEVEL=1
VDD 1 Ø DC 5V
M1 1 3 2 Ø NMOS L=5.ØU W=2Ø.ØU
M2 2 5 1 1 PMOS L=5.ØU W=4Ø.ØU
M3 1 7 6 1 PMOS L=5.ØU W=1Ø.ØU
M4 1Ø 9 Ø Ø NMOS L=5.ØU W=15.ØU
M5 1Ø 7 6 Ø NMOS L=5.ØU W=15.ØU
M6 Ø 2 11 Ø NMOS L=5.ØU W=15.ØU
M7 Ø 6 2 Ø NMOS L=5.ØU W=15.ØU
M8 1 2 11 1 PMOS L=5.ØU W=3Ø.ØU
M9 1 6 2 1 PMOS L=5.ØU W=3Ø.ØU
M1Ø 1 9 6 1 PMOS L=5.ØU W=1Ø.ØU
C11 1 Ø Ø.4Ø5PF
C12 Ø Ø Ø.3Ø5PF
C13 6 Ø Ø.129PF
C14 2 Ø Ø.248PF
C15 11 Ø Ø.1PF
VIN1 7 Ø PULSE (5V ØV 5NS ØNS ØNS 1ØNS)
VIN2 9 Ø PULSE (5V ØV 5NS ØNS ØNS 1ØNS)
VP1 3 Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS)
VP2 5 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
.TRAN Ø.5NS 4ØNS
.PLOT TRAN V(11) V(2) V(6) (ØV,5V)
.END
```

```
l*******11/27/84 ********  SPICE 2G.1 (15OCT88)  ********23:59:34*****

#        CMOS/SOS - PRECHARGE INV1 ONLY - INPUT 101 - STANDARD D4.P2

#****    TRANSIENT ANALYSIS              TEMPERATURE =  27.### DEG C

#**********************************************************************


#LEGEND:

 *: V(11)
 +: V(2)
 =: V(6)
X
     TIME      V(11)

X(*+=)----------- #.   d+##    1.25#d+##   2.5##d+##    3.75#d+##  5.###d+##
       #.   d+##  2.259d-## X                :                :              *
       5.###d-1# 2.259d-## X                :                :              *
       1.###d-#9 2.259d-## X                :                :              *
       1.5##d-#9 2.259d-## X                :                :              *
       2.###d-#9 2.259d-## X                :                :              *
       2.5##d-#9 2.259d-## X                :                :              *
       3.###d-#9 2.259d-## X                :                :              *
       3.5##d-#9 2.259d-## X                :                :              *
       4.###d-#9 2.259d-## X                :                :              *
       4.5##d-#9 2.259d-## X                :                :              *
       5.###d-#9 2.259d-## X                :                :              *
       5.5##d-#9 2.259d-## *             .  :                :      .       *
       6.###d-#9 2.263d-## *                :                :          .   *
       6.5##d-#9 2.3#6d-## *                :                :   .      . . *
       7.###d-#9 2.478d-## =                :                :   .        . *
       7.5##d-#9 1.961d-#2 =                :          .     :         . *
       8.###d-#9 2.291d-#1   .              :                :    .       =
       8.5##d-#9 9.828d-#1     .      :     :      .         :       .    =
       9.###d-#9 2.224d+##      .           :              . :          . =
       9.5##d-#9 3.66#d+##       .    :     :                :       .    +
       1.###d-#8 4.427d+##                  :                :        +
       1.#5#d-#8 4.963d+##                  :                :            X
       1.1##d-#8 4.993d+##  .               :                :            X
       1.15#d-#8 4.999d+##  +               :                :            X
       1.2##d-#8 5.###d+##  +               :                :            X
       1.25#d-#8 5.###d+##  +               :                :            X
       1.3##d-#8 5.###d+##  +               :                :            X
       1.35#d-#8 5.###d+##  +               :                :            X
       1.4##d-#8 5.###d+##  +               :                :            X
       1.45#d-#8 5.###d+##  +               :                :            X
       1.5##d-#8 5.###d+##  +               :                :            X
       1.55#U-#8 5.###d+##  +               :                :            X
       1.6##d-#8 5.###d+##  +               :           .    :          . X
       1.65#d-#8 5.###d+##  +               :                :            X
       1.7##d-#8 5.###d+##  +               :          .     :        .
       1.75#d-#8 5.###d+##  +               :        .       :      .
       1.###d-#8 5.###d+##  :           +   .       .        :    .
       1.85#d-#8 4.987d+##  :         .     + .              :  .
       1.9##d-#8 4.866d+##           .   .  :   +            :        .
       1.95#d-#8 4.412d+##        .         :          +     :      .+.
       2.###d-#8 3.638d+##    .             :                :   .+
       2.#5#d-#8 2.22#d+##   .    :     .   :                :       . +
       2.1##d-#8 9.473d-#1 :.   .          :       .        :            +
       2.15#d-#8 2.621d-#1 .  .            :                :            .
       2.2##d-#8 4.662d-#2 =*   ____._____..                :             .

       2.25#d-## 1.#65d-#2 X                :                :              *
       2.3##d-## 2.112d-#3 X                :                :              *
       2.35#d-## 3.5#4d-#4 X                :                :              *
       2.4##d-## -1.##5d-#5 X               :                :              *
       2.45#d-## -4.8#4d-#6 X               :                :              *
       2.5##d-## 1.356d-#6 X                :                :              *
       2.55#d-## -5.9#2d-#8 X               :                :              *
       2.6##d-## -5.539d-#8 X               :                :              *
       2.65#d-#8 3.937d-#8 X                :                :              *
       2.7##d-#8 2.469d-#8 X                :                :              *
       2.75#d-## 2.16#d-#8 X                :                :              *
       2.8##d-#8 2.281d-#8 X                :                :              *
       2.85#d-#8 2.264d-#8 X                :                :              *
       2.9##d-#8 2.257d-#8 X                :                :              *
       2.95#U-#8 2.259d-#8 X                :                :              *
       3.###d-#8 2.259d-#8 X                :                :              *
       3.#5#U-#8 2.259d-#8 X                :                :              *
       3.1##d-#8 2.259d-#8 X                :                :              *
       3.15#d-#8 2.259d-#8 X                :                :              *
       3.2##d-#8 2.259d-#8 X                :                :              *
       3.25#d-#8 2.259d-#8 X                :                :              *
       3.3##d-#8 2.259d-#8 X                :                :              *
       3.35#d-## 2.259d-#8 X                :                :              *
       3.4##d-#8 2.259d-#8 X                :                :              *
       3.45#U-#8 2.259d-#8 X                :                :              *
       3.5##U-#8 2.259d-#8 X                :                :              *
       3.55#d-#8 2.259d-#8 X                :                :              *
       3.6##d-#8 2.259d-#8 X                :                :              *
       3.65#d-#8 2.259d-#8 X                :                :              *
       3.7##d-#8 2.259d-#8 X                :                :              *
       3.75#d-8# 2.259d-#8 X                :                :              *
       3.8##d-#8 2.259d-#8 X                :                :              *
       3.85#d-#8 2.259d-#8 X                :                :              *
       3.9##d-#8 2.259d-#8 X                :                :              *
       3.95#U-#8 2.259d-#8 X                :                :              *
       4.###d-#8 2.259d-#8 X------.---------:----------------:--------------*
```

Figure A-9. SPICE Waveform of Precharged First
           Inverter with Inputs 101.

A-17
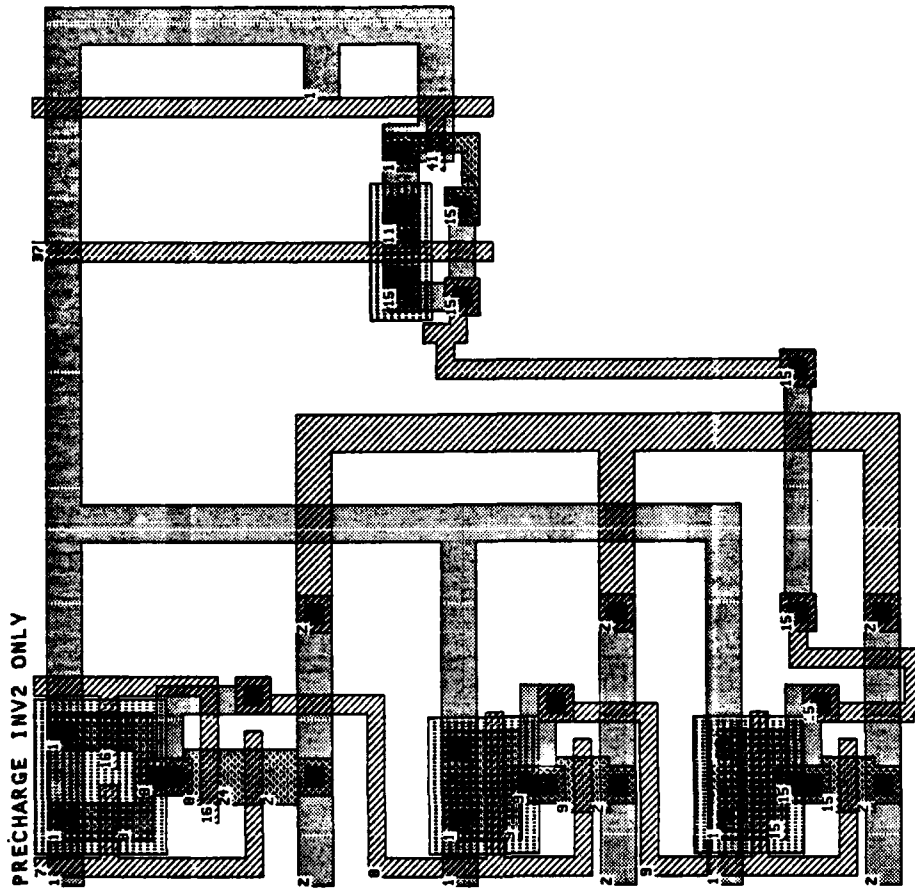
Figure A-10.   Node Plot of Test Circuit Precharged
at Second Inverter Output.

Table A-4

PRECHARGE INV2 ONLY - NODE REFERENCE LIST

GND	0
Vdd	1
NMOS	0
PMOS	1
15	2
41	3
1	4
37	5
3	6
16	7
2	8
7	9
24	10
9	11

Ø   CMOS/SOS PRECHARGE INV2 ONLY - INPUT Ø1Ø - STANDARD D4,P2

Ø****   INPUT LISTING   TEMPERATURE =   27.ØØØ DEG C

Ø***

```
 .WIDTH OUT=8Ø
 .OPTIONS ITL1=5ØØ ITL5=Ø
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
+LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
+LEVEL=1
VDD 1 Ø DC 5V
M1  1  3  2 Ø NMOS L=5.ØU W=2Ø.ØU
M2  2  5  1 1 PMOS L=5.ØU W=4Ø.ØU
M3  1  7  6 1 PMOS L=5.ØU W=1Ø.ØU
M4  1Ø 9  Ø Ø NMOS L=5.ØU W=15.ØU
M5  1Ø 7  6 Ø NMOS L=5.ØU W=15.ØU
M6  Ø  11 2 Ø NMOS L=5.ØU W=15.ØU
M7  Ø  6  11 Ø NMOS L=5.ØU W=15.ØU
M8  1  11 2 1 PMOS L=5.ØU W=3Ø.ØU
M9  1  6  11 1 PMOS L=5.ØU W=3Ø.ØU
M1Ø 1  9  6 1 PMOS L=5.ØU W=1Ø.ØU
C11 1  Ø Ø.4Ø5PF
C12 Ø  Ø Ø.3Ø5PF
C13 6  Ø Ø.129PF
C14 11 Ø Ø.1Ø9PF
C15 2  Ø Ø.77PF
VIN1 7 Ø PULSE (ØV 5V 5NS ØNS ØNS 1ØNS)
VIN2 9 Ø PULSE (ØV 5V 5NS ØNS ØNS 1ØNS)
VP1 3 Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS)
VP2 5 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
.TRAN Ø.5NS 4ØNS
.PLOT TRAN V(2) V(11) V(6) (ØV,5V)
.END
```

```
1*******11/28/84 ******** SPICE 2G.1 (15OCT88) *********88:88:55*****

#        CMOS/SOS PRECHARGE INV2 ONLY - INPUT 010 - STANDARD D4.P2

#****     TRANSIENT ANALYSIS              TEMPERATURE =   27.888 DEG C

#***************************************************************************

#LEGEND:

 *: V(2)
 +: V(11)
 =: V(6)
X
    TIME       V(2)

X(*+=)----------- #.    d+88    1.258d+88    2.558d+88    3.758d+88  5.888d+88
    #.   d+88  5.888d+88 +          .            .            .            X
    5.888d-18  5.888d+88 +          .            .            .            X
    1.888d-89  5.888d+88 +          .            .            .            X
    1.588d-89  5.888d+88 +          .            .            .            X
    2.888d-89  5.888d+88 +          .            .            .            X
    2.588d-89  5.858d+88 +          .            .            .            X
    3.888d-89  5.888d+88 +          .            .            .            X
    3.588d-89  5.888d+88 +          .            .            .            X
    4.888d-89  5.888d+88 +          .            .            .            X
    4.588d-89  5.888d+88 +          .            .            .            X
    5.888d-89  5.888d+88 +          .            .            .            X
    5.588d-89  5.888d+88 +          .            .            .            X
    6.888d-89  5.888d+88 +          .            .            .       *     X
    6.588d-89  5.888d+88 .+         .            .            .       .     *
    7.888d-89  5.888d+88 .  +       .            .        *   .       .     *
    7.588d-89  4.998d+88 .          .    + .     *            .       .     *
    8.888d-89  4.956d+88 .          .          * .            .   *   .     *
    8.588d-89  4.829d+88 .          .      *     .            .       .   * *
    9.888d-89  4.558d+88 .      *    .            .            .      *.  * .
    9.588d-89  4.227d+88 .    *      .            .            .         *. .
    1.888d-88  3.848d+88 .* .        .            .         *  .          .+
    1.858d-88  3.446d+88 .=          .            .      *     .          .+
    1.188d-88  3.865d+88 =           .            .   *        .          .+
    1.158d-88  2.782d+88 =           .            . *          .          .+
    1.288d-88  2.359d+88 =           .          * .            .          .+
    1.258d-88  2.841d+88 =           .        *   .            .          .+
    1.388d-88  1.759d+88 =           .      *     .            .          .+
    1.358d-88  1.496d+88 =           .    *       .            .          .+
    1.488d-88  1.272d+88 =           .   *        .            .          .+
    1.458d-88  1.874d+88 =           .  *         .            .          .+
    1.588d-88  8.953d-81 =           . *          .            .          .+
    1.558d-88  7.478d-81 =           .*           .            .          .+
    1.688d-88  6.233d-81 .  *        .            .            .          .+
    1.658d-88  5.192d-81 .    *      .            .            .          .+
    1.788d-88  4.426d-81 .      *    .            .     +      .      .    .+
    1.758d-88  4.176d-81 .      *    .            .            .      .    .+
    1.888d-88  4.899d-81 .         * .   +        .            .      .    .+
    1.858d-88  6.727d-81 .           .*+          .            .          .+
    1.988d-88  1.886d+88 .  +        . *          .            .          .=
    1.958d-88  1.387d+88 +          .  *         .            .          .=
    2.888d-88  1.774d+88 +          .    *       .            .          .=
    2.858d-88  2.148d+88 +          .      *     .            .          .=
    2.188d-88  2.588d+88 +          .        *   .            .          .=
    2.158d-88  2.822d+88 +          .          * .            .          .=
    2.288d-88  3.126d+88 +          .            *            .          .=
    2.258d-88  3.394d+88 +          .            . *          .          .=
    2.388d-88  3.632d+88 +          .            .   *        .          .=
    2.358d-88  3.852d+88 +          .            .     *      .          .=
    2.488d-88  4.827d+88 +          .            .       *    .          .=
    2.458d-88  4.187d+88 +          .            .         *  .          .=
    2.588d-88  4.324d+88 +          .            .           *.          .=
    2.558d-88  4.435d+88 +          .            .            . *        .=
    2.688d-88  4.534d+88 +          .            .            .   *      .=
    2.658d-88  4.613d+88 +          .            .            .     *    .=
    2.788d-88  4.688d+88 +          .            .            .       *  .=
    2.758d-88  4.739d+88 +          .            .            .         *.=
    2.888d-88  4.783d+88 +          .            .            .          .*
    2.858d-88  4.822d+88 +          .            .            .          .*
    2.988d-88  4.854d+88 +          .            .            .          .*
    2.958d-88  4.888d+88 +          .            .            .          .*
    3.888d-88  4.982d+88 +          .            .            .          .:
    3.858d-88  4.919d+88 +          .            .            .          .:
    3.188d-88  4.934d+88 +          .            .            .          .:
    3.158d-88  4.946d+88 +          .            .            .          .:
    3.288d-88  4.955d+88 +          .            .            .          .*
    3.258d-88  4.964d+88 +          .            .            .          X
    3.388d-88  4.978d+88 +          .            .            .          X
    3.358d-88  4.976d+88 +          .            .            .          X
    3.488d-88  4.988d+88 +          .            .            .          X
    3.458d-88  4.984d+88 +          .            .            .          X
    3.588d-88  4.987d+88 +          .            .            .          X
    3.558d-88  4.989d+88 +          .            .            .          X
    3.688d-88  4.991d+88 +          .            .            .          X
    3.658d-88  4.993d+88 +          .            .            .          X
    3.788d-88  4.994d+88 +          .            .            .          X
    3.758d-88  4.995d+88 +          .            .            .          X
    3.888d-88  4.996d+88 +          .            .            .          X
    3.858d-88  4.997d+88 +          .            .            .          X
    3.988d-88  4.997d+88 +          .            .            .          X
    3.958d-88  4.998d+88 +          .            .            .          X
    4.888d-88  4.998d+88 +          .            .            .          X
```

Figure A-11. SPICE Waveform Plot of Precharged
Second Inverter with Input 010.

Ø   CMOS/SOS PRECHARGE INV2 ONLY - INPUT 101 - STANDARD D4.P2

Ø****   INPUT LISTING   TEMPERATURE =   27.000 DEG C

Ø***


```
.WIDTH OUT=80
.OPTIONS ITL1=500 ITL5=0
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
+LEVEL=1
VDD 1 Ø DC 5V
M1 1 3 2 Ø NMOS L=5.ØU W=20.ØU
M2 2 5 1 1 PMOS L=5.ØU W=40.ØU
M3 1 7 6 1 PMOS L=5.ØU W=10.ØU
M4 1Ø 9 Ø Ø NMOS L=5.ØU W=15.ØU
M5 1Ø 7 6 Ø NMOS L=5.ØU W=15.ØU
M6 Ø 11 2 Ø NMOS L=5.ØU W=15.ØU
M7 Ø G 11 Ø NMOS L=5.ØU W=15.ØU
M8 1 11 2 1 PMOS L=5.ØU W=30.ØU
M9 1 6 11 1 PMOS L=5.ØU W=30.ØU
M1Ø 1 9 6 1 PMOS L=5.ØU W=10.ØU
C11 1 Ø Ø.4Ø5PF
C12 Ø Ø Ø.3Ø5PF
C13 6 Ø Ø.129PF
C14 11 Ø Ø.1Ø9PF
C15 2 Ø Ø.77PF
VIN1 7 Ø PULSE (5V ØV 5NS ØNS ØNS 1ØNS)
VIN2 9 Ø PULSE (5V ØV 5NS ØNS ØNS 1ØNS)
VP1 3 Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS)
VP2 5 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
.TRAN Ø.5NS 4ØNS
.PLOT TRAN V(2) V(11) V(6) (ØV,5V)
.END
```

```
1********11/28/84 ********  SPICE 2G.1 (15OCT8#)  ********##:##:42*****

#        CMOS/SOS PRECHARGE INV2 ONLY - INPUT 1#1 - STANDARD D4.P2

#****    TRANSIENT ANALYSIS              TEMPERATURE =  27.### DEG C

#*************************************************************************

#LEGEND:

 *: V(2)
 +: V(11)
 =: V(6)
X
     TIME      V(2)

X(*+=)----------  #.   d+##     1.25#d+##     2.5##d+##      3.75#d+## 5.###d+##
                                - - - - - -  - - - - - -  - - - - - -  - - - - -
     #.   d+##  4.518d-##  X                 .            .            .        +
     5.##8d-1#  4.518d-##  X                 .            .            .        +
     1.###d-#9  4.518d-##  X                 .            .            .        +
     1.5##d-#9  4.518d-##  X                 .            .            .        +
     2.###d-#9  4.518d-##  X                 .            .            .        +
     2.5##d-#9  4.518d-##  X                 .            .            .        +
     3.###d-#9  4.518d-##  X                 .            .            .        +
     3.5##d-#9  4.518d-##  X                 .            .            .        +
     4.###d-#9  4.518d-##  X                 .            .            .        +
     4.5##d-#9  2.58#d-#1  =      *          .            .            .        +
     5.###d-#9  9.371d-#1  =           *     .            .            .        +
     5.5##d-#9  1.377d+##        =          *.            .            .        +
     6.###d-#9  1.696d+##            =       .  *         .   *        .        +
     6.5##d-#9  1.967d+##              =     .            .     *      .  *     +
     7.###d-#9  1.928d+##             =      .            .    *       . *      +
     7.5##d-#9  1.967d+##              =     .    *       .    *       .        +
     8.###d-#9  2.195d+##                 +  .            .   *        .        +
     8.5##d-#9  2.5#2d+##                 +  .            .            .        +
     9.###d-#9  2.824d+##                    .+           .            .       =
     9.5##d-#9  3.12#d+##                    .   +        .            .       =
     1.###d-#8  3.39#d+##                    .      +     .            .      =
     1.#5#d-#8  3.627d+##                    .         +  .            .     =
     1.1##d-#8  3.844d+##                    .            +            .    =
     1.15#d-#8  4.#22d+##                    .            . +          .   =
     1.2##d-#8  4.184d+##                    .            .    +       .  =
     1.25#d-#8  4.319d+##                    .            .      +     . =
     1.3##d-#8  4.431d+##                    .            .        +   .=
     1.35#d-#8  4.532d+##                    .            .          + =
     1.4##d-#8  4.61#d+##                    .            .           +=
     1.45#d-#8  4.678d+##                    .            .            =+
     1.5##d-#8  4.737d+##                    .            .            = +
     1.55#d-#8  4.784d+##                    .            .            =  +
     1.6##d-#8  4.822d+##                    .            .            =   +
     1.65#d-#8  4.853d+##                    .            .            =    +
     1.7##d-#8  4.879d+##                   .+            .            .     =
     1.75#d-#8  4.9##d+##               *    .            .            .      =
     1.8##d-#8  4.9#7d+##           *        .            .            .       =
     1.85#d-#8  4.876d+##       =            .            .            .      =
     1.9##d-#8  4.737d+##     =              .            .            .   = +
     1.95#d-#8  4.491d+##   =                .            .            .  X  +
     2.###d-#8  4.17#d+##  =                 .            .            .  +
     2.#5#d-#8  3.779d+##  =                 .            .            .+
     2.1##d-#8  3.388d+##  =                 .            .            +
     2.15#d-#8  3.###d+##  =                 .            .          + .
     2.2##d-#8  2.649d+##  =                 .            .        +   .
     2.25#d-#8  2.3#4d+##  =                 .            .      +     .
     2.3##d-#8  1.999d+##  =                 .            .    +       .
     2.35#d-#8  1.716d+##  =                 .            .  +         .
     2.4##d-#8  1.459d+##  =                 .            .+           .
     2.45#d-#8  1.242d+##  =                 .          + .            .
     2.5##d-#8  1.#42d+##  =                 .        + .              .
     2.55#d-#8  8.764d-#1  =               .       + .                 .
     2.6##d-#8  7.335d-#1  =              .    + .                     .
     2.65#d-#8  6.#53d-#1  =             .  + .                        .
     2.7##d-#8  5.#7#d-#1  =           . + .                           .
     2.75#d-#8  4.169d-#1  =         . + .                             .
     2.8##d-#8  3.448d-#1  =       .  + .                              .
     2.85#d-#8  2.#62d-#1  = .    + .                                  .
     2.9##d-#8  2.342d-#1  = .  + .                                    .
     2.95#d-#8  1.933d-#1  = .+ .                                      .
     3.###d-#8  1.592d-#1  =  +.                                       .
     3.#5#d-#8  1.293d-#1  =.*                                         .
     3.1##d-#8  1.#73d-#1  =.*                                         .
     3.15#d-#8  8.773d-#2  ==*                                         .
     3.2##d-#8  7.162d-#2  ==*                                         .
     3.25#d-#8  5.91#d-#2  ==*                                         .
     3.3##d-#8  4.##7d-#2  =*                                          .
     3.35#d-#8  3.952d-#2  X                                           .
     3.4##d-#8  3.242d-#2  X                                           .
     3.45#d-#8  2.624d-#2  X                                           .
     3.5##d-#8  2.172d-#2  X                                           .
     3.55#d-#8  1.773d-#2  X                                           .
     3.6##d-#8  1.445d-#2  X                                           .
     3.65#d-#8  1.191d-#2  X                                           .
     3.7##d-#8  9.674d-#3  X                                           .
     3.75#d-#8  7.946d-#3  X                                           .
     3.8##d-#8  6.514d-#3  X                                           .
     3.85#d-#8  5.269d-#3  X                                           .
     3.9##d-#8  4.36#d-#3  X                                           .
     3.95#d-#8  3.553d-#3  X                                           .
     4.###d-#8  2.883d-#3  X  - - - - - -  - - - - - -  - - - - - -  - - - - -
```

Figure A-12.   SPICE Waveform Plot of Precharged
               Second Inverter with Input 101.

A-22
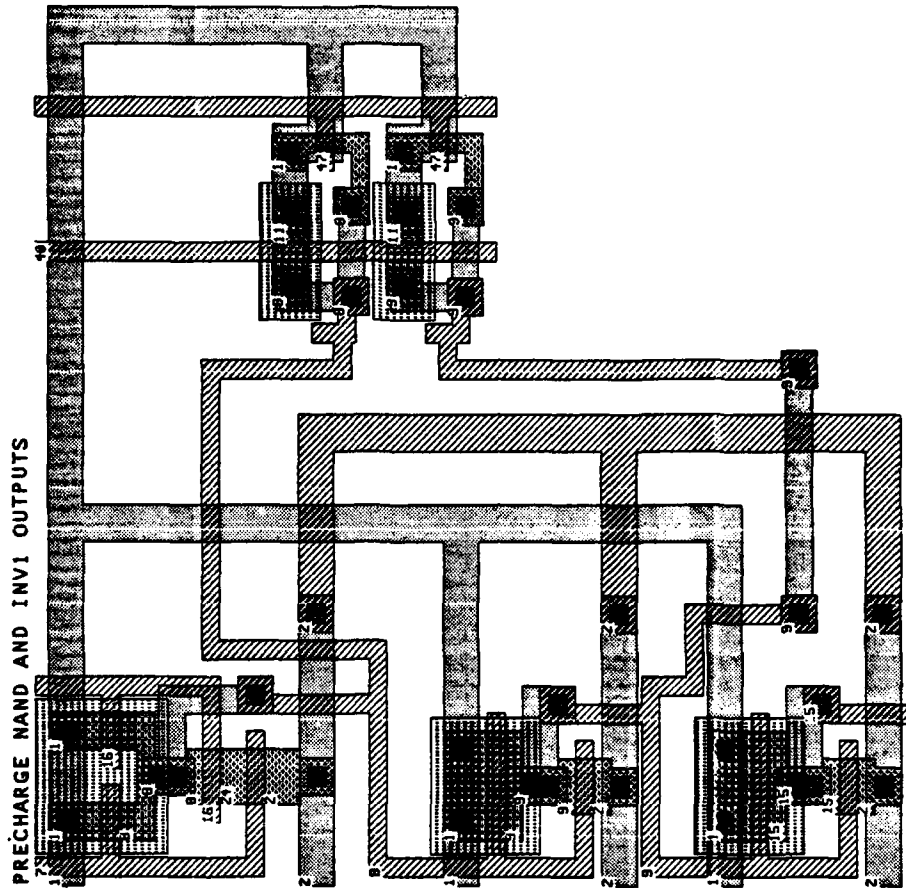
Figure A-13. Node Plot of Test Circuit Precharged
at Nand and First Inverter Outputs.

Table A-5

PRECHARGE NAND AND INV1 OUTPUTS NODE CROSS REFERENCE LIST

GND	0
VDD	1
NMOS	0
PMOS	1
9	2
47	3
1	4
3	5
40	6
16	7
2	8
7	9
24	10
15	11

```
.WIDTH OUT=8Ø
.OPTIONS ITL1=5ØØ ITL5=Ø
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
+LEVEL=1
VDD 1 Ø DC 5V
M1 1 3 2 Ø NMOS L=5.ØU W=2Ø.ØU
M2 1 3 5 Ø NMOS L=5.ØU W=2Ø.ØU
M3 2 6 1 1 PMOS L=5.ØU W=4Ø.ØU
M4 5 6 1 1 PMOS L=5.ØU W=4Ø.ØU
M5 1 7 5 1 PMOS L=5.ØU W=1Ø.ØU
M6 1Ø 9 Ø Ø NMOS L=5.ØU W=15.ØU
M7 1Ø 7 5 Ø NMOS L=5.ØU W=15.ØU
M8 Ø 2 11 Ø NMOS L=5.ØU W=15.ØU
M9 Ø 5 2 Ø NMOS L=5.ØU W=15.ØU
M1Ø 1 2 11 1 PMOS L=5.ØU W=3Ø.ØU
M11 1 5 2 1 PMOS L=5.ØU W=3Ø.ØU
M12 1 9 5 1 PMOS L=5.ØU W=1Ø.ØU
C13 1 Ø Ø.452PF
C14 Ø Ø Ø.3Ø5PF
C15 5 Ø Ø.243PF
C16 2 Ø Ø.248PF
C17 11 Ø Ø.1PF
VIN1 7 Ø PULSE (ØV 5V 5NS ØNS ØNS 1ØNS)
VIN2 9 Ø PULSE (ØV 5V 5NS ØNS ØNS 1ØNS)
VP1 3 Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS)
VP2 6 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
.TRAN Ø.5NS 4ØNS
.PLOT TRAN V(11) V(2) V(5) (ØV,5V)
.END
```

```
1********11/28/84 ********  SPICE 2G.1 (15OCT80)  *********88:82:11*****

0    CMOS/SOS - PRECHARGE NAND AND INV1 - INPUT 010 - STANDARD D4,P2

0****    TRANSIENT ANALYSIS              TEMPERATURE =  27.000 DEG C

0*****************************************************************************

0LEGEND:

*: V(11)
+: V(2)
=: V(5)
X
    TIME      V(11)

X(*+=)----------- 0.    d+00    1.250d+00    2.500d+00    3.750d+00  5.000d+00
    0.   d+00   5.000d+00 +                                                  X
    5.000d-10  5.000d+00 +                                                   X
    1.000d-09  5.000d+00 +                                                   X
    1.500d-09  5.000d+00 +                                                   X
    2.000d-09  5.000d+00 +                                                   X
    2.500d-09  5.000d+00 +                                                   X
    3.000d-09  5.000d+00 +                                                   X
    3.500d-09  5.000d+00 +                                                   X
    4.000d-09  5.000d+00 +                                                   X
    4.500d-09  5.000d+00 .       +                                           X
    5.000d-09  4.961d+00 .            +                                      X
    5.500d-09  4.775d+00 .                +                               .
    6.000d-09  4.430d+00 .                       +                   .  .
    6.500d-09  3.872d+00 .                            +         .   .   .
    7.000d-09  3.361d+00 .                         +     .   .       .
    7.500d-09  3.607d+00 .                      .    +     .
    8.000d-09  4.131d+00 .                    .        +              .
    8.500d-09  4.549d+00 .              +   .              .
    9.000d-09  4.852d+00 .          =  .          +
    9.500d-09  4.913d+00 .        =           +                          .
    1.000d-08  4.896d+00 .       =         + .
    1.050d-08  4.759d+00 .     =                          +
    1.100d-08  4.255d+00 .    =                         +
    1.150d-08  3.523d+00 .  =                      +     .+
    1.200d-08  2.260d+00 . =            +                      +
    1.250d-08  1.149d+00 .=         +
    1.300d-08  2.803d-01 . =.
    1.350d-08  5.896d-02 .=.
    1.400d-08  1.315d-02 *.=
    1.450d-08  2.914d-03 *.=
    1.500d-08  4.101d-04 *.=
    1.550d-08  4.067d-05 *.=
    1.600d-08  8.769d-06 *  =
    1.650d-08  2.807d-06 *        =.
    1.700d-08  4.737d-07 *                =
    1.750d-08  5.493d-08 *                      =
    1.800d-08  1.019d-04 *                            =
    1.850d-08  5.510d-03 *                    =
    1.900d-08  0.307d-02 .=
    1.950d-08  2.548d-01 . =
    2.000d-08  1.016d+00 .     =     +
    2.050d-08  2.005d+00 . =      +
    2.100d-08  3.354d+00 .   =        +
    2.150d-08  4.280d+00 . =                   +            .
    2.200d-08  4.941d+00 . +
    2.250d-08  4.988d+00 .+                                             X
    2.300d-08  4.999d+00 .+                                             X
    2.350d-08  5.000d+00 +                                              X
    2.400d-08  5.000d+00 +                                              X
    2.450d-08  5.000d+00 +                                              X
    2.500d-08  5.000d+00 +                                              X
    2.550d-08  5.000d+00 +                                              X
    2.600d-08  5.000d+00 +                                              X
    2.650d-08  5.000d+00 +                                              X
    2.700d-08  5.000d+00 +                                              X
    2.750d-08  5.000d+00 +                                              X
    2.800d-08  5.000d+00 +                                              X
    2.850d-08  5.000d+00 +                                              X
    2.900d-08  5.000d+00 +                                              X
    2.950d-08  5.000d+00 +                                              X
    3.000d-08  5.000d+00 +                                              X
    3.050d-08  5.000d+00 +                                              X
    3.100d-08  5.000d+00 +                                              X
    3.150d-08  5.000d+00 +                                              X
    3.200d-08  5.000d+00 +                                              X
    3.250d-08  5.000d+00 +                                              X
    3.300d-08  5.000d+00 +                                              X
    3.350d-08  5.000d+00 +                                              X
    3.400d-08  5.000d+00 +                                              X
    3.450d-08  5.000d+00 +                                              X
    3.500d-08  5.000d+00 +                                              X
    3.550d-08  5.000d+00 +                                              X
    3.600d-08  5.000d+00 +                                              X
    3.650d-08  5.000d+00 +                                              X
    3.700d-08  5.000d+00 +                                              X
    3.750d-08  5.000d+00 +                                              X
    3.800d-08  5.000d+00 +                                              X
    3.850d-08  5.000d+00 +                                              X
    3.900d-08  5.000d+00 +                                              X
    3.950d-08  5.000d+00 +                                              X
    4.000d-08  5.000d+00 +                                              X
```

Figure A-14.   SPICE Waveform Plot of Precharged Nand
and First Inverter with Inputs 010.

MICROCOPY RESOLUTION TEST CHART

NATIONAL BUREAU OF STANDARDS-1963-A

Ø   CMOS/SOS - PRECHARGE NAND AND INV1 - INPUT 1Ø1 - STANDARD D4,P2

Ø****   INPUT LISTING   TEMPERATURE =   27.ØØØ DEG C

Ø***

```
.WIDTH OUT=8Ø
.OPTIONS ITL1=5ØØ ITL5=Ø
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
+LEVEL=1
VDD 1 Ø DC 5V
M1  1 3 2 Ø NMOS L=5.ØU W=2Ø.ØU
M2  1 3 5 Ø NMOS L=5.ØU W=2Ø.ØU
M3  2 6 1 1 PMOS L=5.ØU W=4Ø.ØU
M4  5 6 1 1 PMOS L=5.ØU W=4Ø.ØU
M5  1 7 5 1 PMOS L=5.ØU W=1Ø.ØU
M6  1Ø 9 Ø Ø NMOS L=5.ØU W=15.ØU
M7  1Ø 7 5 Ø NMOS L=5.ØU W=15.ØU
M8  Ø 2 11 Ø NMOS L=5.ØU W=15.ØU
M9  Ø 5 2 Ø NMOS L=5.ØU W=15.ØU
M1Ø 1 2 11 1 PMOS L=5.ØU W=3Ø.ØU
M11 1 5 2 1 PMOS L=5.ØU W=3Ø.ØU
M12 1 9 5 1 PMOS L=5.ØU W=1Ø.ØU
C13 1 Ø Ø.452PF
C14 Ø Ø Ø.3Ø5PF
C15 5 Ø Ø.243PF
C16 2 Ø Ø.248PF
C17 11 Ø Ø.1PF
VIN1 7 Ø PULSE (5V ØV 5NS ØNS ØNS 1ØNS)
VIN2 9 Ø PULSE (5V ØV 5NS ØNS ØNS 1ØNS)
VP1 3 Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS)
VP2 6 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
.TRAN Ø.5NS 4ØNS
.PLOT TRAN V(11) V(2) V(5) (ØV,5V)
.END
```

```
|********11/28/84 ********  SPICE 2G.1 (150CT88)  *********88:82:82*****

#    CMOS/SOS - PRECHARGE NAND AND INV1 - INPUT 101 - STANDARD D4.P2

#****    TRANSIENT ANALYSIS              TEMPERATURE =   27.888 DEG C

#***************************************************************************

#LEGEND:

 *: V(11)
 +: V(2)
 =: V(5)
X
    TIME      V(11)

X(*+=)-----------  8.     d+88     1.258d+88    2.588d+88    3.758d+88  5.888d+88
    8.    d+88   2.259d-88 X           .            .            .           .
    5.888d-18   2.259d-88 X           .            .            .           .
    1.888d-89   2.259d-88 X           .            .            .           .
    1.588d-89   2.259d-88 X           .            .            .           .
    2.888d-89   2.259d-88 X           .            .            .           .
    2.588d-89   2.259d-88 X           .            .            .           .
    3.888d-89   2.259d-88 X           .            .            .           .
    3.588d-89   2.259d-88 X           .            .            .           .
    4.888d-89   2.259d-88 X           .            .            .           .
    4.588d-89   2.259d-88         .   .            .            .           .
    5.888d-89   2.264d-88 *          .            .            .           .
    5.588d-89   2.316d-88 *          .            .            .     .      .
    6.888d-89   2.581d-88 *          .            .            .        .  .
    6.588d-89   3.934d-84 .          .            .            .         .  =
    7.888d-89   4.615d-82 .*         .            .            .           =
    7.588d-89   4.256d-81       .    .      .     .            .           =
    8.888d-89   1.472d+88   .        .*   .       .            .           =
    8.588d-89   2.958d+88   .   .    .            .            .           =
    9.888d-89   4.853d+88    .  .    .            .            .          =.
    9.588d-89   4.873d+88   .       .             .            .          =.
    1.888d-88   4.979d+88   .*       .            .            .           X
    1.858d-88   4.997d+88   .*       .            .            .           X
    1.188d-88   5.888d+88   *        .            .            .           X
    1.158d-88   5.888d+88   *        .            .            .           X
    1.288d-88   5.888d+88   *        .            .            .           X
    1.258d-88   5.888d+88   *        .            .            .           X
    1.388d-88   5.888d+88   *        .            .            .           X
    1.358d-88   5.888d+88   *        .            .            .           X
    1.488d-88   5.888d+88   *        .            .            .           X
    1.458d-88   5.088d+88   *        .            .            .           X
    1.588d-88   5.888d+88   *        .            .            .           X
    1.558d-88   5.888d+88   *        .            .            .           X
    1.688d-88   5.888d+88   *        .            .            .          =.
    1.658d-88   5.888d+88   *        .            .            .           .
    1.788d-88   5.888d+88   *        .            .            .           .
    1.758d-88   5.888d+88   *        .            .            .           .
    1.888d-88   5.888d+88   *        .            .            .           .
    1.858d-88   5.888d+88   .*       .            .            .           .
    1.988d-88   5.888d+88   *        .            .       .    .           .
    1.958d-88   4.999d+88       .    .      .     .            .           .
    2.888d-88   4.996d+88       .    .            .            .           .
    2.858d-88   4.926d+88        .  .:           .            .            .
    2.188d-88   4.799d+88       .    .            .     .      .            .
    2.158d-88   4.168d+88   .   .    .            .            .      .     .
    2.288d-88   3.231d+88   .        .            .      .     .            .
    2.258d-88   1.917d+88   .     .  .            .            .            .
    2.388d-88   8.671d-81   .     .     .         .      .     .            .
    2.358d-88   1.958d-81   .  X     .            .            .            .
    2.488d-88   3.885d-82   .= .     .            .            .            .
    2.458d-88   7.988d-83   .= .     .            .            .           .
    2.588d-88   1.192d-83   .= .     .            .            .           .
    2.558d-88   1.658d-84   .= .     .            .            .           .
    2.688d-88   3.987d-85 X          .            .            .           .
    2.658d-88  -1.132d-85 X          .            .            .           .
    2.788d-88   1.212d-86 X          .            .            .           .
    2.758d-88   6.613d-87 X          .            .            .           .
    2.888d-88  -1.199d-87 X          .            .            .           .
    2.858d-88   9.211d-89 X          .            .            .           .
    2.988d-88   3.186d-88 X          .            .            .           .
    2.958d-88   2.863d-88 X          .            .            .           .
    3.888d-88   2.218d-88 X          .            .            .           .
    3.858d-88   2.271d-88 X          .            .            .           .
    3.188d-88   2.257d-88 X          .            .            .           .
    3.158d-88   2.258d-88 X          .            .            .           .
    3.288d-88   2.259d-88 X          .            .            .           .
    3.258d-88   2.259d-88 X          .            .            .           .
    3.388d-88   2.259d-88 X          .            .            .           .
    3.358d-88   2.259d-88 X          .            .            .           .
    3.488d-88   2.259d-88 X          .            .            .           .
    3.458d-88   2.259d-88 X          .            .            .           .
    3.588d-88   2.259d-88 X          .            .            .           .
    3.558d-88   2.259d-88 X          .            .            .           .
    3.688d-88   2.259d-88 X          .            .            .           .
    3.658d-88   2.259d-88 X          .            .            .           .
    3.788d-88   2.259d-88 X          .            .            .           .
    3.758d-88   2.259d-88 X          .            .            .           .
    3.888d-88   2.259d-88 X          .            .            .           .
    3.858d-88   2.259d-88 X          .            .            .           .
    3.988d-88   2.259d-88 X          .            .            .           .
    3.958d-88   2.259d-88 X          .            .            .           .
    4.888d-88   2.259d-88 X  -  -  -  -  -  -  -  -  -  -  -  -  -  -  .  .
```

Figure A-15.   SPICE Waveform Plot of Precharged
               Nand and First Inverter with Inputs
               101.

A-27

PRECHARGE NAND AND INV2 OUTPUTS
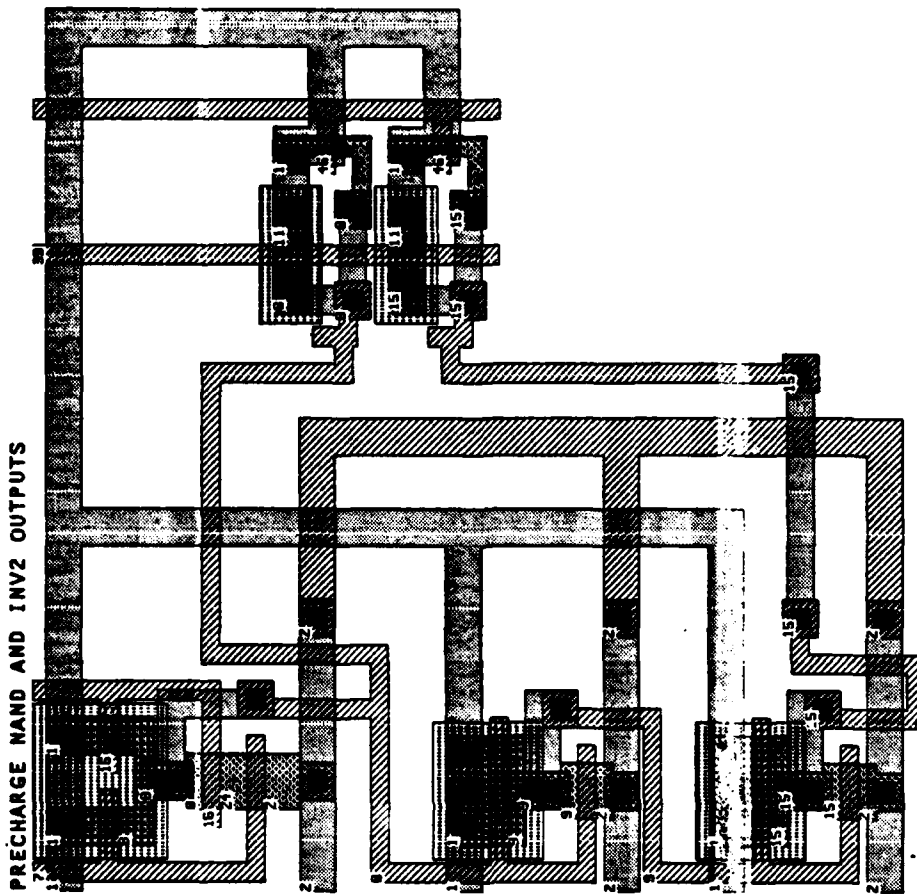
Figure A-16. Node Plot of Precharged Nand and
Second Inverter Output.

Table A-6

PRECHARGE NAND AND INV2 OUTPUTS - NODE REFERENCE LIST

GND	Ø
Vdd	1
NMOS	Ø
PMOS	1
15	2
46	3
1	4
8	5
39	6
16	7
2	8
7	9
24	1Ø
9	11

```
.WIDTH OUT=80
.OPTIONS ITL1=500 ITL5=0
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
+LEVEL=1
VDD 1 0 DC 5V
M1 1 3 2 0 NMOS L=5.0U W=20.0U
M2 1 3 5 0 NMOS L=5.0U W=20.0U
M3 2 6 1 1 PMOS L=5.0U W=40.0U
M4 5 6 1 1 PMOS L=5.0U W=40.0U
M5 1 7 5 1 PMOS L=5.0U W=10.0U
M6 10 9 0 0 NMOS L=5.0U W=15.0U
M7 10 7 5 0 NMOS L=5.0U W=15.0U
M8 0 11 2 0 NMOS L=5.0U W=15.0U
M9 0 5 11 0 NMOS L=5.0U W=15.0U
M10 1 11 2 1 PMOS L=5.0U W=30.0U
M11 1 5 11 1 PMOS L=5.0U W=30.0U
M12 1 9 5 1 PMOS L=5.0U W=10.0U
C13 1 0 0.452PF
C14 0 0 0.305PF
C15 5 0 0.243PF
C16 11 0 0.109PF
C17 2 0 0.77PF
VIN1 7 0 PULSE (0V 5V 5NS 0NS 0NS 10NS)
VIN2 9 0 PULSE (0V 5V 5NS 0NS 0NS 10NS)
VP1 3 0 PULSE (0V 5V 4NS 0NS 0NS 2NS)
VP2 6 0 PULSE (5V 0V 4NS 0NS 0NS 2NS)
.TRAN 0.5NS 40NS
.PLOT TRAN V(2) V(11) V(5) (0V,5V)
.END
```

```
!********11/28/84 ********  SPICE 2G.1 (15OCT08)  *********88:87:47*****

#   CMOS/SOS TEST CELL PRECHARGE INV2 AND NAND - INPUT #10 - STANDARD D4,P2

#****    TRANSIENT ANALYSIS              TEMPERATURE =   27.888 DEG C

#*****************************************************************************

#LEGEND:

*: V(2)
+: V(11)
=: V(5)
X
     TIME      V(2)

X(*+=)----------- #.    d+88     1.258d+88    2.588d+88    3.758d+88  5.888d+88
```

TIME	V(2)					
#. d+88	5.888d+88	*				X
5.888d-18	5.888d+88	*				X
1.888d-89	5.888d+88	*				X
1.588d-89	5.888d+88	*				X
2.888d-89	5.888d+88	*				X
2.588d-89	5.888d+88	*				X
3.888d-89	5.888d+88	*				X
3.588d-89	5.888d+88	*				X
4.888d-89	5.888d+88	*				X
4.588d-89	5.888d+88	*				X
5.888d-89	5.888d+88	*				X
5.588d-89	5.888d+88	*				=
6.888d-89	5.888d+88	*				=
6.588d-89	5.888d+88	*				
7.888d-89	5.888d+88	*				
7.588d-89	5.888d+88	*				
8.888d-89	5.888d+88	*				
0.588d-89	5.888d+88	*				
9.888d-89	5.888d+88	*				
9.588d-89	4.998d+08	*				
1.888d-88	4.986d+88	*				
1.858d-88	4.917d+88	*				
1.188d-88	4.818d+88	*				
1.158d-88	4.538d+88					
1.288d-88	4.223d+88					
1.258d-88	3.846d+88					
1.388d-88	3.468d+88					
1.358d-88	3.877d+88					
1.488d-88	2.713d+88					
1.458d-88	2.372d+88	=				
1.588d-88	2.847d+88	=				
1.558d-88	1.758d+08	=				
1.688d-88	1.588d+88	=				
1.688d-88	1.273d+88					
1.788d-88	1.879d+88					
1.758d-88	9.234d-81					
1.888d-88	7.984d-81					
1.858d-88	7.638d-81					
1.988d-88	8.263d-81					
1.958d-88	1.883d+88					
2.888d-88	1.315d+88	*				
2.858d-88	1.681d+88	*				
2.188d-88	2.857d+88	*				
2.158d-08	2.414d+88	*				
2.288d-88	2.751d+88	*				
2.258d-88	3.858d+88	*				
2.388d-88	3.329d+88	*				
2.358d-88	3.579d+88	*				
2.488d-88	3.793d+88	*				
2.458d-88	3.988d+88	*				
2.588d-88	4.149d+88	*				
2.558d-88	4.289d+08	*				
2.688d-88	4.413d+88	*				
2.658d-88	4.589d+88	*				
2.788d-08	4.594d+08	*				
2.758d-88	4.666d+08	*				
2.888d-88	4.723d+88	*				
2.858d-88	4.774d+88	*				
2.988d-88	4.813d+88	*				
2.958d-88	4.846d+88	*				
3.888d-88	4.875d+88	*				
3.858d-88	4.896d+88	*				
3.188d-88	4.915d+08	*				
3.158d-88	4.931d+08	*				
3.288d-88	4.943d+88	*				
3.258d-08	4.954d+08	*				
3.388d-88	4.962d+88	*				X
3.358d-88	4.969d+88	*				X
3.488d-88	4.975d+88	*				X
3.458d-88	4.979d+88	*				X
3.588d-88	4.983d+88	*				X
3.558d-88	4.986d+88	*				X
3.688d-88	4.988d+88	*				X
3.658d-88	4.991d+08	*				X
3.788d-88	4.992d+88	*				X
3.758d-88	4.994d+88	*				X
3.888d-88	4.995d+88	*				X
3.858d-88	4.996d+08	*				X
3.988d-88	4.997d+08	*				X
3.958d-88	4.997d+08	*				X
4.888d-88	4.998d+88	*				X

Figure A-17.   SPICE Waveform Plot of Precharged
               Nand and Second Inverter with Inputs
               010.

```
 .WIDTH OUT=8Ø
 .OPTIONS ITL1=5ØØ ITL5=Ø
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
 +LEVEL=1
 VDD 1 Ø DC 5V
 M1  1 3 2 Ø NMOS L=5.ØU W=2Ø.ØU
 M2  1 3 5 Ø NMOS L=5.ØU W=2Ø.ØU
 M3  2 6 1 1 PMOS L=5.ØU W=4Ø.ØU
 M4  5 6 1 1 PMOS L=5.ØU W=4Ø.ØU
 M5  1 7 5 1 PMOS L=5.ØU W=1Ø.ØU
 M6  1Ø 9 Ø Ø NMOS L=5.ØU W=15.ØU
 M7  1Ø 7 5 Ø NMOS L=5.ØU W=15.ØU
 M8  Ø 11 2 Ø NMOS L=5.ØU W=15.ØU
 M9  Ø 5 11 Ø NMOS L=5.ØU W=15.ØU
 M1Ø 1 11 2 1 PMOS L=5.ØU W=3Ø.ØU
 M11 1 5 11 1 PMOS L=5.ØU W=3Ø.ØU
 M12 1 9 5 1 PMOS L=5.ØU W=1Ø.ØU
 C13 1 Ø Ø.452PF
 C14 Ø Ø Ø.3Ø5PF
 C15 5 Ø Ø.243PF
 C16 11 Ø Ø.1Ø9PF
 C17 2 Ø Ø.77PF
 VIN1 7 Ø PULSE (5V ØV 5NS ØNS ØNS 1ØNS)
 VIN2 9 Ø  PULSE (5V ØV 5NS ØNS ØNS 1ØNS)
 VP1 3 Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS)
 VP2 6 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
 .TRAN Ø.5NS 4ØNS
 .PLOT TRAN V(2) V(11) V(5) (ØV,5V)
 .END
```

```
|********11/28/84 ********  SPICE 2G.1 (15OCT88)  *********88:83:88*****

#   CMOS/SOS TEST CELL PRECHARGE INV2 AND NAND - INPUT 101 - STANDARD D4.P2

#****    TRANSIENT ANALYSIS              TEMPERATURE =   27.888 DEG C

#***************************************************************************

#LEGEND:

*: V(2)
+: V(11)
=: V(5)
X
      TIME      V(2)

X(*+=)----------   #.   d+88    1.258d+88    2.588d+88     3.758d+88  5.888d+88
```

```
#.    d+88   4.518d-88 X                :             :             :          *
5.888d-18   4.518d-88 X                :             :             :          *
1.888d-89   4.518d-88 X                :             :             :          *
1.588d-89   4.518d-88 X                :             :             :          *
2.888d-89   4.518d-88 X                :             :             :          *
2.588d-89   4.518d-88 X                :             :             :          *
3.888d-89   4.518d-88 X                :             :             :          *
3.588d-89   4.518d-88 X                :             :             :          *
4.888d-89   4.518d-88 X                :             :             :          *
4.588d-89   2.588d-81 .    *      *    :             :             :        *
5.888d-89   9.379d-81 .            *   :        *        *         :      *
5.588d-89   1.395d+88 .              *       :         *         = :    *
6.888d-89   1.834d+88 .                 +   :          *    =     :
6.588d-89   2.423d+88 .                  +  :            *   =   :   *
7.888d-89   2.824d+88 .                     + :           * =    :    *
7.588d-89   3.118d+88 .*                      :            = *    :    *
8.888d-89   3.378d+88 *                       :            =    * :    *
8.588d-89   3.628d+88 +                       :            =      *:    *
9.888d-89   3.831d+88 +                       :             =      :*   *
9.588d-89   4.811d+88 +                       :             =      :  *
1.888d-88   4.176d+88 +                       :             =      :   *
1.858d-88   4.318d+88 +                       :             =      :    *
1.188d-88   4.425d+88 +                       :             =      :     *
1.158d-88   4.528d+88 +                       :             =      :     *
1.288d-88   4.685d+88 +                       :             =      :      *
1.258d-88   4.675d+88 +                       :             =      :      *
1.388d-88   4.733d+88 +                       :             =      :       *
1.358d-88   4.779d+88 +                       :             =      :       *
1.488d-88   4.819d+88 +                       :             =      :        *
1.458d-88   4.851d+88 +                       :             =      :        *
1.588d-88   4.877d+88 +                       :             =      :         *
1.558d-88   4.981d+88 +                       :             =      :         *
1.688d-88   4.918d+88 +                       :             =      :        X
1.658d-88   4.933d+88 +                       :             =      :         *
1.788d-88   4.945d+88 +                       :             =      :         *
1.758d-88   4.955d+88 +                       :             =      :        *
1.888d-88   4.963d+88 .+                      :             =    * :        *
1.858d-88   4.969d+88 .  +                    :          *        :        *
1.988d-88   4.974d+88 .       +               :       *          :        *
1.958d-88   4.978d+88 .           +         *         :          :        *
2.888d-88   4.948d+88 .                +  * =         :          :        *
2.858d-88   4.825d+88 .              *      +         =         :        *
2.188d-88   4.655d+88 .         *           :    +         =    :        *
2.158d-88   4.332d+88 .     *               :        +        = :        *
2.288d-88   3.991d+88 .   *                 :           +      =:  *
2.258d-88   3.593d+88 .  *                  :              +   : =    *
2.388d-88   3.211d+88 . *                   :                 +:    =    *
2.358d-88   2.837d+88 . *                   :            *      +        = *
2.488d-88   2.487d+88 .*                    :         *          :  +       *
2.458d-88   2.163d+88 .*               *              :          :    +     *
2.588d-88   1.856d+88 .*          *                   :          :      +   *
2.558d-88   1.595d+88 .=     *                        :          :        + *
2.688d-88   1.355d+88 =  *                            :          :          +
2.658d-88   1.142d+88 = *                             :          :          *
2.788d-88   9.653d-81 = *                             :          :          *
2.758d-88   8.845d-81 = *                             :          :          *
2.888d-88   6.726d-81 =  *                            :          :          *
2.858d-88   5.684d-81 =   *                           :          :          *
2.988d-88   4.683d-81 =    *                          :          :          *
2.958d-88   3.843d-81 =      *                        :          :          *
3.888d-88   3.166d-81 =        *                      :          :          *
3.858d-88   2.598d-81 =  *                            :          :          *
3.188d-88   2.154d-81 = *                             :          :          *
3.158d-88   1.789d-81 = *                             :          :          *
3.288d-88   1.458d-81 = *                             :          :          *
3.258d-88   1.193d-81 =*                              :          :          *
3.388d-88   9.678d-82 =*                              :          :          *
3.358d-88   8.821d-82 =*                              :          :          *
3.488d-88   6.557d-82 =*                              :          :          *
3.458d-88   5.348d-82 =*                              :          :          *
3.588d-88   4.413d-82 X                               :          :          *
3.558d-88   3.588d-82 X                               :          :          *
3.688d-88   2.948d-82 X                               :          :          *
3.658d-88   2.419d-82 X                               :          :          *
3.788d-88   1.958d-82 X                               :          :          *
3.758d-88   1.628d-82 X                               :          :          *
3.888d-88   1.322d-82 X                               :          :          *
3.858d-88   1.877d-82 X                               :          :          *
3.988d-88   8.877d-83 X                               :          :          *
3.958d-88   7.282d-83 X                               :          :          *
4.888d-88   5.878d-83 X - - - - - - - - - - - - - - - : - - - - - - - - - - *
```

Figure A-18.   SPICE Waveform Plot of Precharged Nand
                and Second Inverter with Inputs 101.

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Appendix B

SPICE analyses of the Memory/ALU Bitslice circuit elements selected for precharge are presented.

The elements selected for precharge were:

      a. 2x4 Memory Row Decoder

      b. 1-Bit RAM Cell

      c. B Register

Two simulations were run on each element. The first input was a high-low-high (5NS - 10NS - 25NS) varying pulse waveform. The second inverted the pulse waveform for the same time periods.

In addition to the two basic simulations, the precharged RAM cell and the B register were simulated for transmission gate device widths of two and three times the basic transmission gate device width. This required four more simulations for these circuits each.

To facilitate evaluation of the output waveforms, the node reference list is provided for each circuit element. The left column provides mextra node numbers and the right column provides the corresponding SPICE node numbers. The SPICE input data uses SPICE reference node numbers and the cifplot of the circuit references mextra nodes. To determine the nodes to which input voltages or ground are applied, identify a node on the cifplot circuit, find the node number on the reference list and look at the right

column and find the corresponding SPICE node.   In this way,

the SPICE input data can be directly related to the circuit

node cifplot.
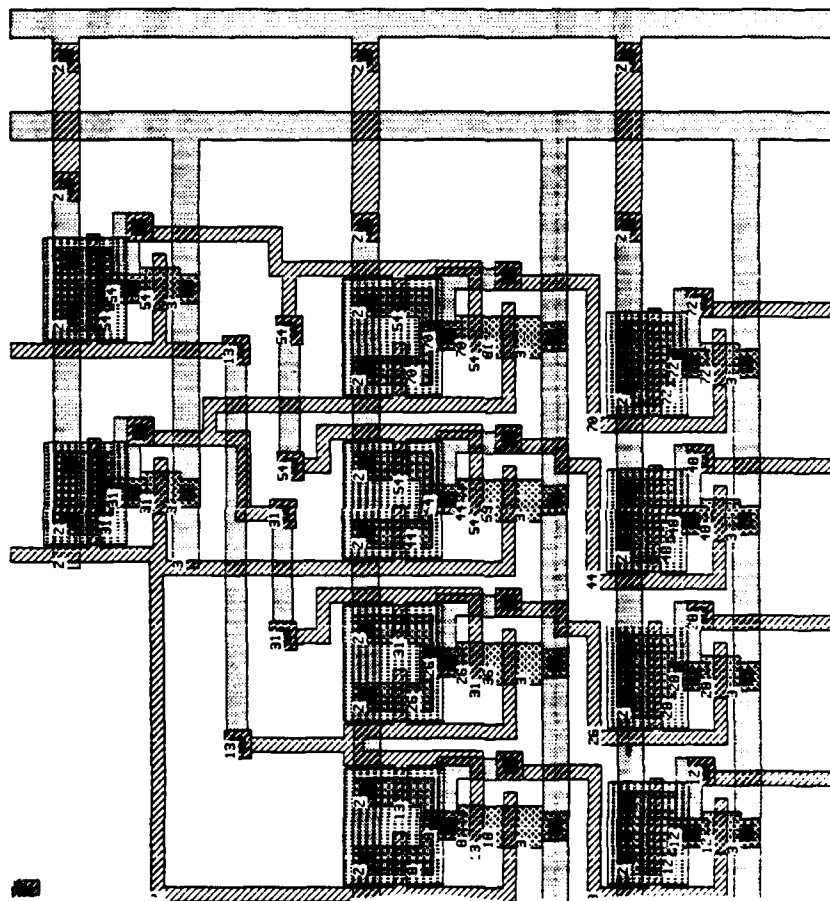
Figure B-1. Node Plot of Basic Decoder Circuit.

B-3

Table B-1

BASIC DECODER - NODE REFERENCE LIST

GND	0
Vdd	1
NMOS	0
PMOS	1
54	2
13	3
3	4
70	5
2	6
31	7
81	8
72	9
44	10
7	11
59	12
48	13
26	14
36	15
28	16
8	17
18	18
12	19

Ø   CMOS/SOS BASIC 2X4 DECODER SPICE TRANSIENT ANALYSIS

Ø****   INPUT LISTING   TEMPERATURE =   27.ØØØ DEG C

Ø***

```
.WIDTH OUT=8Ø
.OPTIONS ITL1=5ØØ ITL5=Ø
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
+LEVEL=1
VDD 1 Ø DC 5V
M1  Ø 3 2 Ø NMOS L=5.ØU W=15.ØU
M2  1 2 5 1 PMOS L=5.ØU W=1Ø.ØU
M3  1 3 2 1 PMOS L=5.ØU W=3Ø.ØU
M4  8 7 Ø Ø NMOS L=5.ØU W=15.ØU
M5  8 2 5 Ø NMOS L=5.ØU W=15.ØU
M6  Ø 5 9 Ø NMOS L=5.ØU W=15.ØU
M7  1 7 5 1 PMOS L=5.ØU W=1Ø.ØU
M8  1 5 9 1 PMOS L=5.ØU W=3Ø.ØU
M9  1 2 1Ø 1 PMOS L=5.ØU W=1Ø.ØU
M1Ø Ø 11 7 Ø NMOS L=5.ØU W=15.ØU
M11 12 11 Ø Ø NMOS L=5.ØU W=15.ØU
M12 12 2 1Ø Ø NMOS L=5.ØU W=15.ØU
M13 1 11 7 1 PMOS L=5.ØU W=3Ø.ØU
M14 Ø 1Ø 13 Ø NMOS L=5.ØU W=15.ØU
M15 1 11 1Ø 1 PMOS L=5.ØU W=1Ø.ØU
M16 1 1Ø 13 1 PMOS L=5.ØU W=3Ø.ØU
M17 1 7 14 1 PMOS L=5.ØU W=1Ø.ØU
M18 15 3 Ø Ø NMOS L=5.ØU W=15.ØU
M19 15 7 14 Ø NMOS L=5.ØU W=15.ØU
M2Ø Ø 14 16 Ø NMOS L=5.ØU W=15.ØU
M21 1 3 14 1 PMOS L=5.ØU W=1Ø.ØU
M22 1 14 16 1 PMOS L=5.ØU W=3Ø.ØU
M23 1 3 17 1 PMOS L=5.ØU W=1Ø.ØU
M24 18 11 Ø Ø NMOS L=5.ØU W=15.ØU
M25 18 3 17 Ø NMOS L=5.ØU W=15.ØU
M26 Ø 17 19 Ø NMOS L=5.ØU W=15.ØU
M27 1 17 19 1 PMOS L=5.ØU W=3Ø.ØU
M28 1 11 17 1 PMOS L=5.ØU W=1Ø.ØU
C29 1 Ø Ø.838PF
C3Ø Ø Ø Ø.561PF
C31 11 Ø Ø.157PF
C32 17 Ø Ø.126PF
C33 19 Ø Ø.18ØPF
C34 3 Ø Ø.151PF
C35 14 Ø Ø.127PF
C36 16 Ø Ø.18ØPF
C37 7 Ø Ø.132PF
C38 1Ø Ø Ø.128PF
C39 13 Ø Ø.18ØPF
C4Ø 2 Ø Ø.171PF
C41 5 Ø Ø.128PF
C42 9 Ø Ø.13ØPF
VIN1 11 Ø PULSE (ØV 5V 5NS ØNS ØNS 1ØNS)
VIN2 3 Ø PULSE (ØV 5V 5NS ØNS ØNS 1ØNS)
.TRAN Ø.5NS 4ØNS
.PLOT TRAN V(9) V(19) V(16) (ØV,5V)

.END
```

```
1********12/01/04 ********  SPICE 2G.1 (15OCT80)  ********86:45:47*****
#       CMOS/SOS BASIC 2X4 DECODER SPICE TRANSIENT ANALYSIS
#****    TRANSIENT ANALYSIS                    TEMPERATURE =  27.000 DEG C
#**************************************************************************

#LEGEND:

*: V(9)
+: V(19)
-: V(16)
X
     TIME       V(9)

X(*+=)----------- 0.    d+00      1.250d+00     2.500d+00     3.750d+00  5.000d+00
 0.    d+00   5.000d+00 X ------------.------------.------------.-----------.
 5.000d-10   5.000d+00 X            .            .            .           .
 1.000d-09   5.000d+00 X            .            .            .           .
 1.500d-09   5.000d+00 X            .            .            .           .
 2.000d-09   5.000d+00 X            .            .            .           .
 2.500d-09   5.000d+00 X            .            .            .           .
 3.000d-09   5.000d+00 X            .            .            .           .
 3.500d-09   5.000d+00 X            .            .            .           .
 4.000d-09   5.000d+00 X            .            .            .           .
 4.500d-09   5.000d+00 X            .            .            .           .
 5.000d-09   5.000d+00 X            .            .            .           .
 5.500d-09   5.000d+00 X            .            .            .           .
 6.000d-09   5.000d+00 X            .            .            .           .
 6.500d-09   5.000d+00 X            .            .            .           .
 7.000d-09   4.965d+00 = +          .            .            .           .
 7.500d-09   4.865d+00 =            .          * .            .           .
 8.000d-09   4.454d+00 =            .            .  *         .  +        .
 8.500d-09   3.570d+00 =            .            .   +        .           .
 9.000d-09   2.365d+00 =            .          * .            .  +        .
 9.500d-09   1.352d+00 =          * .            .            .         + .
 1.000d-08   6.656d-01 =        *   .            .            .           .
 1.050d-08   2.745d-01 =   *        .            .            .           .
 1.100d-08   1.126d-01 =-*          .            .            .           .
 1.150d-08   4.090d-02 =-*          .            .            .           .
 1.200d-08   1.981d-02 X            .            .            .           .
 1.250d-08   8.244d-03 X            .            .            .           .
 1.300d-08   3.558d-03 X            .            .            .           .
 1.350d-08   1.424d-03 X            .            .            .           .
 1.400d-08   3.874d-04 X            .            .            .           .
 1.450d-08   1.909d-04 X            .            .            .           .
 1.500d-08   5.754d-05 X            .            .            .           .
 1.550d-08   1.849d-05 X            .            .            .           .
 1.600d-08   7.902d-06 X            .            .            .           .
 1.650d-08   3.446d-06 X            .            .            .           .
 1.700d-08   1.511d-06 X            .            .            .     +     .
 1.750d-08   7.315d-07 X            .            .            .  +        .
 1.800d-08   1.116d-02 X            .            .        +   .           .
 1.850d-08   1.014d-01 =-*          .            .            .           .
 1.900d-08   3.595d-01 =        *   .            .            .           .
 1.950d-08   8.772d-01 =      +     .          * .            .           .
 2.000d-08   1.720d+00 =-+          .            . *          .           .
 2.050d-08   2.016d+00 =-+          .            .            .           .
 2.100d-08   3.775d+00 X            .            .            .   +       .
 2.150d-08   4.390d+00 X            .            .            .        +  .
 2.200d-08   4.712d+00 X            .            .            .           .
 2.250d-08   4.879d+00 X            .            .            .           .
 2.300d-08   4.952d+00 X            .            .            .           .
 2.350d-08   4.983d+00 X            .            .            .           .
 2.400d-08   4.992d+00 X            .            .            .           .
 2.450d-08   4.997d+00 X            .            .            .           .
 2.500d-08   4.999d+00 X            .            .            .           .
 2.550d-08   5.000d+00 X            .            .            .           .
 2.600d-08   5.000d+00 X            .            .            .           .
 2.650d-08   5.000d+00 X            .            .            .           .
 2.700d-08   5.000d+00 X            .            .            .           .
 2.750d-08   5.000d+00 X            .            .            .           .
 2.800d-08   5.000d+00 X            .            .            .           .
 2.850d-08   5.000d+00 X            .            .            .           .
 2.900d-08   5.000d+00 X            .            .            .           .
 2.950d-08   5.000d+00 X            .            .            .           .
 3.000d-08   5.000d+00 X            .            .            .           .
 3.050d-08   5.000d+00 X            .            .            .           .
 3.100d-08   5.000d+00 X            .            .            .           .
 3.150d-08   5.000d+00 X            .            .            .           .
 3.200d-08   5.000d+00 X            .            .            .           .
 3.250d-08   5.000d+00 X            .            .            .           .
 3.300d-08   5.000d+00 X            .            .            .           .
 3.350d-08   5.000d+00 X            .            .            .           .
 3.400d-08   5.000d+00 X            .            .            .           .
 3.450d-08   5.000d+00 X            .            .            .           .
 3.500d-08   5.000d+00 X            .            .            .           .
 3.550d-08   5.000d+00 X            .            .            .           .
 3.600d-08   5.000d+00 X            .            .            .           .
 3.650d-08   5.000d+00 X            .            .            .           .
 3.700d-08   5.000d+00 X            .            .            .           .
 3.750d-08   5.000d+00 X            .            .            .           .
 3.800d-08   5.000d+00 X            .            .            .           .
 3.850d-08   5.000d+00 X            .            .            .           .
 3.900d-08   5.000d+00 X            .            .            .           .
 3.950d-08   5.000d+00 X            .            .            .           .
 4.000d-08   5.000d+00 X ------------.------------.------------.-----------.
```

Figure B-2.   SPICE Waveform Plot of Basic Decoder
              with Inputs 010.

B-6
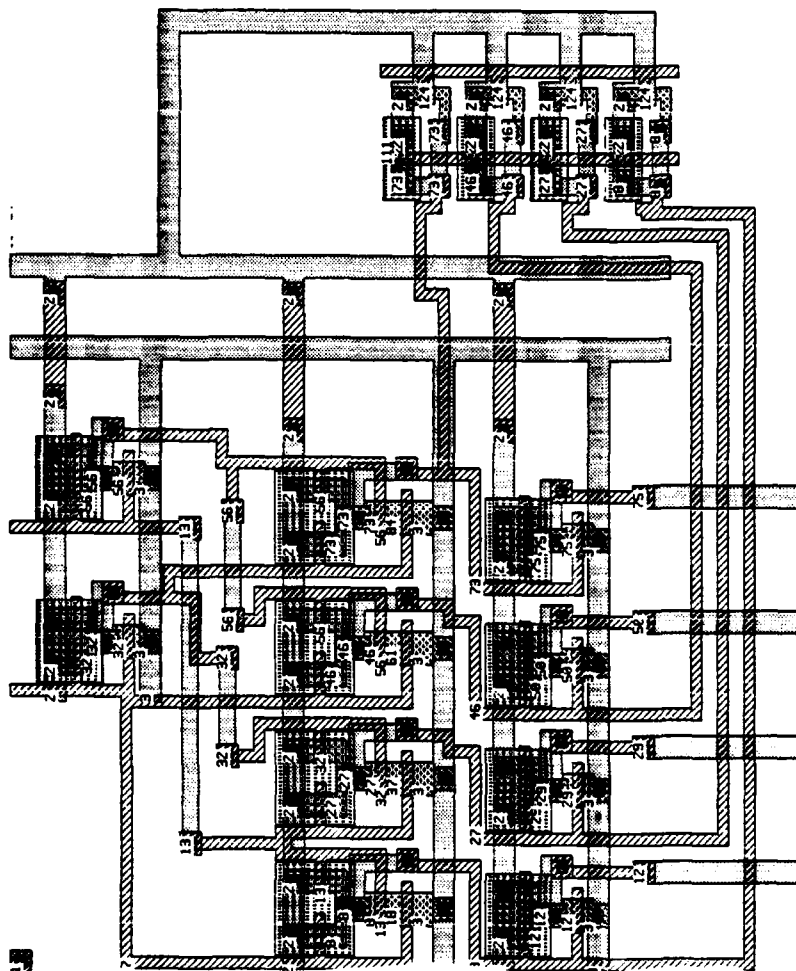
Figure B-3. Node Plot of Decoder with Internal Nodes
Precharged.

B-7

Table B-2

PRECHARGE ALL FOUR OUTPUTS OF DECODER - NODE REFERENCE LIST

```
GND       Ø
Vdd       1
NMOS      Ø
PMOS      1
8         2
124       3
2         4
27        5
46        6
73        7
111       8
56        9
13        1Ø
3         11
32        12
84        13
75        14
7         15
61        16
5Ø        17
37        18
29        19
18        2Ø
12        21
```

```
.WIDTH OUT=80
.OPTIONS ITL1=500 ITL5=0
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
+LEVEL=1
VDD 1 0 DC 5V
M1  1 3 2 0 NMOS L=5.0U W=5.0U
M2  1 3 5 0 NMOS L=5.0U W=5.0U
M3  1 3 6 0 NMOS L=5.0U W=5.0U
M4  1 3 7 0 NMOS L=5.0U W=5.0U
M5  2 8 1 1 PMOS L=5.0U W=10.0U
M6  5 8 1 1 PMOS L=5.0U W=10.0U
M7  6 8 1 1 PMOS L=5.0U W=10.0U
M8  7 8 1 1 PMOS L=5.0U W=10.0U
M9  0 10 9 0 NMOS L=5.0U W=15.0U
M10 1 9 7 1 PMOS L=5.0U W=10.0U
M11 1 10 9 1 PMOS L=5.0U W=30.0U
M12 13 12 0 0 NMOS L=5.0U W=15.0U
M13 13 9 7 0 NMOS L=5.0U W=15.0U
M14 0 7 14 0 NMOS L=5.0U W=15.0U
M15 1 12 7 1 PMOS L=5.0U W=10.0U
M16 1 7 14 1 PMOS L=5.0U W=30.0U
M17 1 9 6 1 PMOS L=5.0U W=10.0U
M18 0 15 12 0 NMOS L=5.0U W=15.0U
M19 16 15 0 0 NMOS L=5.0U W=15.0U
M20 16 9 6 0 NMOS L=5.0U W=15.0U
M21 1 15 12 1 PMOS L=5.0U W=30.0U
M22 0 6 17 0 NMOS L=5.0U W=15.0U
M23 1 15 6 1 PMOS L=5.0U W=10.0U
M24 1 6 17 1 PMOS L=5.0U W=30.0U
M25 1 12 5 1 PMOS L=5.0U W=10.0U
M26 18 10 0 0 NMOS L=5.0U W=15.0U
M27 18 12 5 0 NMOS L=5.0U W=15.0U
M28 0 5 19 0 NMOS L=5.0U W=15.0U
M29 1 10 5 1 PMOS L=5.0U W=10.0U
M30 1 5 19 1 PMOS L=5.0U W=30.0U
M31 1 10 2 1 PMOS L=5.0U W=10.0U
M32 20 15 0 0 NMOS L=5.0U W=15.0U
M33 20 10 2 0 NMOS L=5.0U W=15.0U
M34 0 2 21 0 NMOS L=5.0U W=15.0U
M35 1 2 21 1 PMOS L=5.0U W=30.0U
M36 1 15 2 1 PMOS L=5.0U W=10.0U
C37 1 0 0.1145PF
C38 0 0 0.561PF
C39 15 0 0.157PF
C40 2 0 0.312PF
C41 21 0 0.180PF
C42 10 0 0.151PF
C43 5 0 0.302PF
C44 19 0 0.180PF
C45 12 0 0.182PF
C46 6 0 0.291PF
C47 17 0 0.180PF
C48 9 0 0.171PF
C49 7 0 0.229PF
C50 14 0 0.180PF
C51 3 0 0.50PF
VIN1 15 0 PULSE (0V 5V 5NS 0NS 0NS 10NS)
VIN2 10 0 PULSE (0V 5V 5NS 0NS 0NS 10NS)
VP1 3 0 PULSE (0V 5V 4NS 0NS 0NS 2NS)
VP2 8 0 PULSE (5V 0V 4NS 0NS 0NS 2NS)
.TRAN 0.5NS 40NS
.PLOT TRAN V(14) V(21) V(17) (0V,5V)
.END
```

```
1********12/71/04 ********  SPICE 2G.1 (15OCT8#)  *********#6:47:19*****

#      CMOS/SOS DECODER FOUR OUTPUT PRECHARGE  #!

#****   TRANSIENT ANALYSIS              TEMPERATURE =   27.### DEG C

#*****************************************************************...

#LEGEND:

*: V(14)
+: V(21)
=: V(17)
X
     TIME      V(14)

X(*+=)---------- #.    d+##    1.25#d+##    2.5##d+##    3.75#d+##  5.###d+##
```

TIME	V(14)				
#. d+##	5.###d+##	X			
5.###d-1#	5.###d+##	X			
1.###d-#9	5.###d+##	X			
1.5##d-#9	5.###d+##	X			
2.###d-#9	5.###d+##	X			
2.5##d-#9	5.###d+##	X			
3.###d-#9	5.###d+##	X			
3.5##d-#9	5.###d+##	X			
4.###d-#9	5.###d+##	X			
4.5##d-#9	5.###d+##	X			
5.###d-#9	5.###d+##	X			
5.5##d-#9	5.###d+##	X			
6.###d-#9	4.99#d+##	X			
6.5##d-#9	4.9:4d+##	X			
7.###d-#9	4.767d+##	X			
7.5##d-#9	4.4#6d+##	X			
8.###d-#9	3.774d+##	X			
8.5##d-#9	2.056d+##	=+			
9.###d-#9	1.#51d+##	= +			
9.5##d-#9	1.#45d+##	= + +			
1.###d-#8	5.358d-#1	= + +			
1.#5#d-#8	2.329d-#1	= +			
1.1##d-#8	9.443d-#2	=+			
1.15#d-#8	4.#56d-#2	X			
1.2##d-#8	1.648d-#2	X			
1.25#d-#8	7.#9#d-#3	X			
1.3##d-#8	3.#55d-#3	X			
1.35#d-#8	1.146d-#3	X			
1.4##d-#8	3.8#1d-#4	X			
1.45#d-#8	1.599d-#4	X			
1.5##d-#8	4.628d-#5	X			
1.55#d-#8	1.611d-#5	X			
1.6##d-#8	6.89#d-#6	X			
1.65#d-#8	3.##5d-#6	X			
1.7##d-#8	1.3#9d-#6	X			
1.75#d-#8	6.141d-#7	X			
1.8##d-#8	6.55#d-#4	X			
1.85#d-#8	4.52#d-#3	X			
1.9##d-#8	3.862d-#2	X			
1.95#d-#8	1.256d-#1	=*			
2.###d-#8	2.661d-#1	= *			
2.#5#d-#8	6.3#9d-#1	= + +			
2.1##d-#8	1.121d+##	= + +			
2.15#d-#8	1.#27d+##	= +			
2.2##d-#8	2.661d+##	= +			
2.25#d-#8	3.557d+##	=+			
2.3##d-#8	4.2#3d+##	X			
2.35#d-#8	4.592d+##	X			
2.4##d-#8	4.817d+##	X			
2.45#d-#8	4.913d+##	X			
2.5##d-#8	4.96#d+##	X			
2.55#d-#8	4.987d+##	X			
2.6##d-#8	4.995d+##	X			
2.65#d-#8	4.99#d+##	X			
2.7##d-#8	4.999d+##	X			
2.75#d-#8	5.###d+##	X			
2.8##d-#8	5.###d+##	X			
2.85#d-#8	5.###d+##	X			
2.9##d-#8	5.###d+##	X			
2.95#d-#8	5.###d+##	X			
3.###d-#8	5.###d+##	X			
3.#5#d-#8	5.###d+##	X			
3.1##d-#8	5.###d+##	X			
3.15#d-#8	5.###d+##	X			
3.2##d-#8	5.###d+##	X			
3.25#d-#8	5.###d+##	X			
3.3##d-#8	5.###d+##	X			
3.35#d-#8	5.###d+##	X			
3.4##d-#8	5.###d+##	X			
3.45#d-#8	5.###d+##	X			
3.5##d-#8	5.###d+##	X			
3.55#d-#8	5.###d+##	X			
3.6##d-#8	5.###d+##	X			
3.65#d-#8	5.###d+##	X			
3.7##d-#8	5.###d+##	X			
3.75#d-#8	5.###d+##	X			
3.8##d-#8	5.###d+##	X			
3.85#d-#8	5.###d+##	X			
3.9##d-#8	5.###d+##	X			
3.95#d-#8	5.###d+##	X			
4.###d-#8	5.###d+##	X			

Figure B-4.   SPICE Waveform Plot of Internal Node
Precharged Decoder with Inputs 010.

```
 .WIDTH OUT=8Ø
 .OPTIONS ITL1=5ØØ ITL5=Ø
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
 +LEVEL=1
 VDD 1 Ø DC 5V
 M1  1 3 2 Ø NMOS L=5.ØU W=1Ø.ØU
 M2  1 3 5 Ø NMOS L=5.ØU W=1Ø.ØU
 M3  1 3 6 Ø NMOS L=5.ØU W=1Ø.ØU
 M4  1 3 7 Ø NMOS L=5.ØU W=1Ø.ØU
 M5  2 8 1 1 PMOS L=5.ØU W=2Ø.ØU
 M6  5 8 1 1 PMOS L=5.ØU W=2Ø.ØU
 M7  6 8 1 1 PMOS L=5.ØU W=2Ø.ØU
 M8  7 8 1 1 PMOS L=5.ØU W=2Ø.ØU
 M9  Ø 1Ø 9 Ø NMOS L=5.ØU W=15.ØU
 M1Ø 1 9 7 1 PMOS L=5.ØU W=1Ø.ØU
 M11 1 1Ø 9 1 PMOS L=5.ØU W=3Ø.ØU
 M12 13 12 Ø Ø NMOS L=5.ØU W=15.ØU
 M13 13 9 7 Ø NMOS L=5.ØU W=15.ØU
 M14 Ø 7 14 Ø NMOS L=5.ØU W=15.ØU
 M15 1 12 7 1 PMOS L=5.ØU W=1Ø.ØU
 M16 1 7 14 1 PMOS L=5.ØU W=3Ø.ØU
 M17 1 9 6 1 PMOS L=5.ØU W=1Ø.ØU
 M18 Ø 15 12 Ø NMOS L=5.ØU W=15.ØU
 M19 16 15 Ø Ø NMOS L=5.ØU W=15.ØU
 M2Ø 16 9 6 Ø NMOS L=5.ØU W=15.ØU
 M21 1 15 12 1 PMOS L=5.ØU W=3Ø.ØU
 M22 Ø 6 17 Ø NMOS L=5.ØU W=15.ØU
 M23 1 15 6 1 PMOS L=5.ØU W=1Ø.ØU
 M24 1 6 17 1 PMOS L=5.ØU W=3Ø.ØU
 M25 1 12 5 1 PMOS L=5.ØU W=1Ø.ØU
 M26 18 1Ø Ø Ø NMOS L=5.ØU W=15.ØU
 M27 18 12 5 Ø NMOS L=5.ØU W=15.ØU
 M28 Ø 5 19 Ø NMOS L=5.ØU W=15.ØU
 M29 1 1Ø 5 1 PMOS L=5.ØU W=1Ø.ØU
 M3Ø 1 5 19 1 PMOS L=5.ØU W=3Ø.ØU
 M31 1 1Ø 2 1 PMOS L=5.ØU W=1Ø.ØU
 M32 2Ø 15 Ø Ø NMOS L=5.ØU W=15.ØU
 M33 2Ø 1Ø 2 Ø NMOS L=5.ØU W=15.ØU
 M34 Ø 2 21 Ø NMOS L=5.ØU W=15.ØU
 M35 1 2 21 1 PMOS L=5.ØU W=3Ø.ØU
 M36 1 15 2 1 PMOS L=5.ØU W=1Ø.ØU
 C37 1 Ø Ø.1145PF
 C38 Ø Ø Ø.561PF
 C39 15 Ø Ø.157PF
 C4Ø 2 Ø Ø.312PF
 C41 21 Ø Ø.18ØPF
 C42 1Ø Ø Ø.151PF
 C43 5 Ø Ø.3Ø2PF
 C44 19 Ø Ø.18ØPF
 C45 12 Ø Ø.182PF
 C46 6 Ø Ø.291PF
 C47 17 Ø Ø.18ØPF
```

```
C48 9 0 0.171PF
C49 7 0 0.229PF
C50 14 0 0.180PF
C51 3 0 0.50PF
VIN1 15 0 PULSE (0V 5V 5NS 0NS 0NS 10NS)
VIN2 10 0 PULSE (0V 5V 5NS 0NS 0NS 10NS)
VP1 3 0 PULSE (0V 5V 4NS 0NS 0NS 2NS)
VP2 8 0 PULSE (5V 0V 4NS 0NS 0NS 2NS)
.TRAN 0.5NS 40NS
.PLOT TRAN V(14) V(21) V(17) (0V,5V)
.END
```

```
!********12/#1/#4 ********  SPICE 2G.1 (150CT8#)  ********#6:47:51*****

#       CMOS/SOS DECODER FOUR OUTPUT PRECHARGE  y&

#****     TRANSIENT ANALYSIS              TEMPERATURE =   27.### DEG C

#***************************************************************************

#LEGEND:

 *: V(14)
 +: V(21)
 =: V(17)
X
      TIME       V(14)

X(*+=)-----------  #.   d+##      1.25#d+##      2.5##d+##      3.75#d+## 5.###d+##
```

TIME	V(14)	plot
#. d+##	5.###d+##	X
5.###d-1#	5.###d+##	X
1.###d-#9	5.###d+##	X
1.5##d-#9	5.###d+##	X
2.###d-#9	5.###d+##	X
2.5##d-#9	5.###d+##	X
3.###d-#9	5.###d+##	X
3.5##d-#9	5.###d+##	X
4.###d-#9	5.###d+##	X
4.5##d-#9	5.###d+##	X
5.###d-#9	4.999d+##	X
5.5##d-#9	4.959d+##	X
6.###d-#9	4.82#d+##	X
6.5##d-#9	4.46#d+##	X
7.###d-#9	3.721d+##	X
7.5##d-#9	2.734d+##	X
8.###d-#9	1.719d+##	X
8.5##d-#9	9.437d-#1	
9.###d-#9	4.625d-#1	
9.5##d-#9	2.113d-#1	
1.###d-#8	8.796d-#2	
1.#5#d-#8	3.742d-#2	X
1.1##d-#8	1.591d-#2	X
1.15#d-#8	6.766d-#3	X
1.2##d-#8	2.331d-#3	X
1.25#d-#8	1.14#d-#3	X
1.3##d-#8	3.58#d-#4	X
1.35#d-#8	1.271d-#4	X
1.4##d-#8	5.#52d-#5	X
1.45#d-#8	1.459d-#5	X
1.5##d-#8	6.24#d-#6	X
1.55#d-#8	1.823d-#6	X
1.6##d-#8	7.9#9d-#7	X
1.65#d-#8	3.563d-#7	X
1.7##d-#8	1.667d-#7	X
1.75#d-#8	8.968d-#8	X
1.8##d-#8	6.513d-#4	X
1.#5#d-#8	4.5#9d-#3	X
1.9##d-#8	3.857d-#2	X
1.95#d-#8	1.255d-#1	
2.###d-#8	2.679d-#1	
2.#5#d-#8	6.3#6d-#1	
2.1##d-#8	1.121d+##	
2.15#d-#8	1.#26d+##	
2.2##d-#8	2.681d+##	
2.25#d-#8	3.556d+##	
2.3##d-#8	4.2#1d+##	X
2.35#d-#8	4.591d+##	X
2.4##d-#8	4.818d+##	X
2.45#d-#8	4.913d+##	X
2.5##d-#8	4.96#d+##	X
2.55#d-#8	4.987d+##	X
2.6##d-#8	4.995d+##	X
2.65#d-#8	4.998d+##	X
2.7##d-#8	4.999d+##	X
2.75#d-#8	5.###d+##	X
2.8##d-#8	5.###d+##	X
2.85#d-#8	5.###d+##	X
2.9##d-#8	5.###d+##	X
2.95#d-#8	5.###d+##	X
3.###d-#8	5.###d+##	X
3.#5#d-#8	5.###d+##	X
3.1##d-#8	5.###d+##	X
3.15#d-#8	5.###d+##	X
3.2##d-#8	5.###d+##	X
3.25#d-#8	5.###d+##	X
3.3##d-#8	5.###d+##	X
3.35#d-#8	5.###d+##	X
3.4##d-#8	5.###d+##	X
3.45#d-#8	5.###d+##	X
3.5##d-#8	5.###d+##	X
3.55#d-#8	5.###d+##	X
3.6##d-#8	5.###d+##	X
3.65#d-#8	5.###d+##	X
3.7##d-#8	5.###d+##	X
3.75#d-#8	5.###d+##	X
3.8##d-#8	5.###d+##	X
3.85#d-#8	5.###d+##	X
3.9##d-#8	5.###d+##	X
3.95#d-#8	5.###d+##	X
4.###d-#8	5.###d+##	X

Figure B-5.   SPICE Plot of Internal Node Precharged
             Decoder with Transmission Gate Widths
             Twice the Basic Widths.

```
 .WIDTH OUT=80
 .OPTIONS ITL1=500 ITL5=0
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
 +LEVEL=1
 VDD 1 0 DC 5V
 M1  1  3  2  0 NMOS L=5.0U W=15.0U
 M2  1  3  5  0 NMOS L=5.0U W=15.0U
 M3  1  3  6  0 NMOS L=5.0U W=15.0U
 M4  1  3  7  0 NMOS L=5.0U W=15.0U
 M5  2  8  1  1 PMOS L=5.0U W=30.0U
 M6  5  8  1  1 PMOS L=5.0U W=30.0U
 M7  6  8  1  1 PMOS L=5.0U W=30.0U
 M8  7  8  1  1 PMOS L=5.0U W=30.0U
 M9  0 10  9  0 NMOS L=5.0U W=15.0U
 M10 1  9  7  1 PMOS L=5.0U W=10.0U
 M11 1 10  9  1 PMOS L=5.0U W=30.0U
 M12 13 12  0  0 NMOS L=5.0U W=15.0U
 M13 13 9  7  0 NMOS L=5.0U W=15.0U
 M14 0  7 14  0 NMOS L=5.0U W=15.0U
 M15 1 12  7  1 PMOS L=5.0U W=10.0U
 M16 1  7 14  1 PMOS L=5.0U W=30.0U
 M17 1  9  6  1 PMOS L=5.0U W=10.0U
 M18 0 15 12  0 NMOS L=5.0U W=15.0U
 M19 16 15  0  0 NMOS L=5.0U W=15.0U
 M20 16 9  6  0 NMOS L=5.0U W=15.0U
 M21 1 15 12  1 PMOS L=5.0U W=30.0U
 M22 0  6 17  0 NMOS L=5.0U W=15.0U
 M23 1 15  6  1 PMOS L=5.0U W=10.0U
 M24 1  6 17  1 PMOS L=5.0U W=30.0U
 M25 1 12  5  1 PMOS L=5.0U W=10.0U
 M26 18 10  0  0 NMOS L=5.0U W=15.0U
 M27 18 12  5  0 NMOS L=5.0U W=15.0U
 M28 0  5 19  0 NMOS L=5.0U W=15.0U
 M29 1 10  5  1 PMOS L=5.0U W=10.0U
 M30 1  5 19  1 PMOS L=5.0U W=30.0U
 M31 1 10  2  1 PMOS L=5.0U W=10.0U
 M32 20 15  0  0 NMOS L=5.0U W=15.0U
 M33 20 10  2  0 NMOS L=5.0U W=15.0U
 M34 0  2 21  0 NMOS L=5.0U W=15.0U
 M35 1  2 21  1 PMOS L=5.0U W=30.0U
 M36 1 15  2  1 PMOS L=5.0U W=10.0U
 C37 1  0 0.1145PF
 C38 0  0 0.561PF
 C39 15 0 0.157PF
 C40 2  0 0.312PF
 C41 21 0 0.180PF
 C42 10 0 0.151PF
 C43 5  0 0.302PF
 C44 19 0 0.180PF
 C45 12 0 0.182PF
 C46 6  0 0.291PF
 C47 17 0 0.180PF
```

```
C48 9 Ø Ø.171PF
C49 7 Ø Ø.229PF
C5Ø 14 Ø Ø.18ØPF
C51 3 Ø Ø.5ØPF
VIN1 15 Ø PULSE (ØV 5V 5NS ØNS ØNS 1ØNS)
VIN2 1Ø Ø PULSE (ØV 5V 5NS ØNS ØNS 1ØNS)
VP1 3 Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS)
VP2 8 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
.TRAN Ø.5NS 4ØNS
.PLOT TRAN V(14) V(21) V(17) (ØV,5V)
.END
```

CMOS/SOS DECODER FOUR OUTPUT PRECHARGE X3

#•••• TRANSIENT ANALYSIS TEMPERATURE = 27.### DEG C

#•••

#LEGEND:

•: V(14)
+: V(21)
=: V(17)
X

```
        TIME      V(14)

X(•+=)----------- #.   d+##   1.25#d+##   2.5##d+##   3.75#d+##  5.###d+##

#.   d+##  5.###d+## X                :          :          :          •
5.###d-10  5.###d+## X                :          :          :          •
1.###d-09  5.###d+## X                :          :          :          •
1.5##d-09  5.###d+## X                :          :          :          •
2.###d-09  5.###d+## X                :          :          :          •
2.5##d-09  5.###d+## X                :          :          :          •
3.###d-09  5.###d+## X                :          :          :          •
3.5##d-09  5.###d+## X                :          :          :          •
4.###d-09  5.###d+## X                :          :          :          •
4.5##d-09  5.###d+## X                :          :          :          •
5.###d-09  4.96#d+## X                :          :          :          •
5.5##d-09  4.836d+## X                :          :          :      •
6.###d-09  4.41#d+## X                :          :          •
6.5##d-09  3.599d+## X                :          :     •
7.###d-09  2.4#5d+## X                :          •
7.5##d-09  1.383d+## X          •     :
8.###d-09  7.###d-#1 X       •
8.5##d-09  3.157d-#1 =+   •
9.###d-09  1.413d-#1 =+•
9.5##d-09  6.#94d-#2 =•  •
1.###d-#0  2.569d-#2 X •
1.#5#d-#0  1.#47d-#2 X     •
1.1##d-#0  4.616d-#3 X          •
1.15#d-#0  1.793d-#3 X               •
1.2##d-#0  5.4##d-#4 X                     •
1.25#d-#0  2.519d-#4 X                          •
1.3##d-#0  7.6##d-#5 X
1.35#d-#0  2.894d-#5 X                               •
1.4##d-#0  1.#64d-#5 X                               •
1.45#d-#0  3.#6#d-#6 X
1.5##d-#0  1.394d-#6 X
1.55#d-#0  4.#92d-#7 X
6.##u-#0  1.#76d-#7 X                                         •
1.65#u-#0  9.425d-#8 X                                        •
1.7##u-#0  6.372d-#8 X                                          •
1.75#u-#0  3.782d-#8 X
1.8##d-#8  6.5##d-#4 X                               •
1.85#d-#8  4.5#5d-#3 X                          •          •
1.9##d-#8  3.856d-02 X               •
1.95#d-#8  1.255d-#1 =+
2.###d-#8  2.679d-#1 =  •        •
2.#5#-##  6.3#4d-01 =                    :
2.1##d-#8  1.121d+## =     •     :     •
2.15#d-#8  1.826d+## =       •        •
2.2##d-#8  2.6#1d+## =+           :          •

2.25#d-##  3.5#5d+## X       :          :          :      •
2.3##d-#8  4.2##d+## X       :          :          :          •
2.35#d-#8  4.591d+## X       :          :          :          •
2.4##d-#8  4.82#d+## X       :          :          :          •
2.45#d-#8  4.913d+## X       :          :          :          •
2.5##d-#8  4.96#d+## X       :          :          :          •
2.55#d-#8  4.987d+## X       :          :          :          •
2.6##u-#8  4.995d+## X       :          :          :          •
2.65#d-#8  4.998d+## X       :          :          :          •
2.7##d-#8  4.999d+## X       :          :          :          •
2.75#d-#8  5.###d+## X       :          :          :          •
2.8##u-#0  5.###d+## X       :          :          :          •
2.85#u-#8  5.###d+## X       :          :          :          •
2.9##u-#8  5.###d+## X       :          :          :          •
2.95#u-#0  5.###d+## X       :          :          :          •
3.###u-#0  5.###d+## X       :          :          :          •
3.#5#u-#0  5.###d+## X       :          :          :          •
3.1##u-#0  5.###d+## X       :          :          :          •
3.15#u-#8  5.###d+## X       :          :          :          •
3.2##d-#0  5.###d+## X       :          :          :          •
3.25#u-#0  5.###d+## X       :          :          :          •
3.3##u-#0  5.###d+## X       :          :          :          •
3.35#u-#8  5.###d+## X       :          :          :          •
3.4##u-#8  5.###d+## X       :          :          :          •
3.45#u-#0  5.###d+## X       :          :          :          •
3.5##u-#8  5.###d+## X       :          :          :          •
3.55#u-#8  5.###d+## X       :          :          :          •
3.6##u-#8  5.###d+## X       :          :          :          •
3.65#u-#0  5.###d+## X       :          :          :          •
3.7##u-#0  5.###d+## X       :          :          :          •
3.75#u-#0  5.###d+## X       :          :          :          •
3.8##u-#0  5.###d+## X       :          :          :          •
3.#5#u-#0  5.###d+## X       :          :          :          •
3.9##u-#8  5.###d+## X       :          :          :          •
3.95#u-#0  5.###d+## X       :          :          :          •
4.###u-#8  5.###d+## X ------:----------:----------:----------:----------•
```

Figure B-6.   SPICE Plot of Internal Node Precharge
Decoder with Transmission Gate Widths
Three Times the Basic Widths.
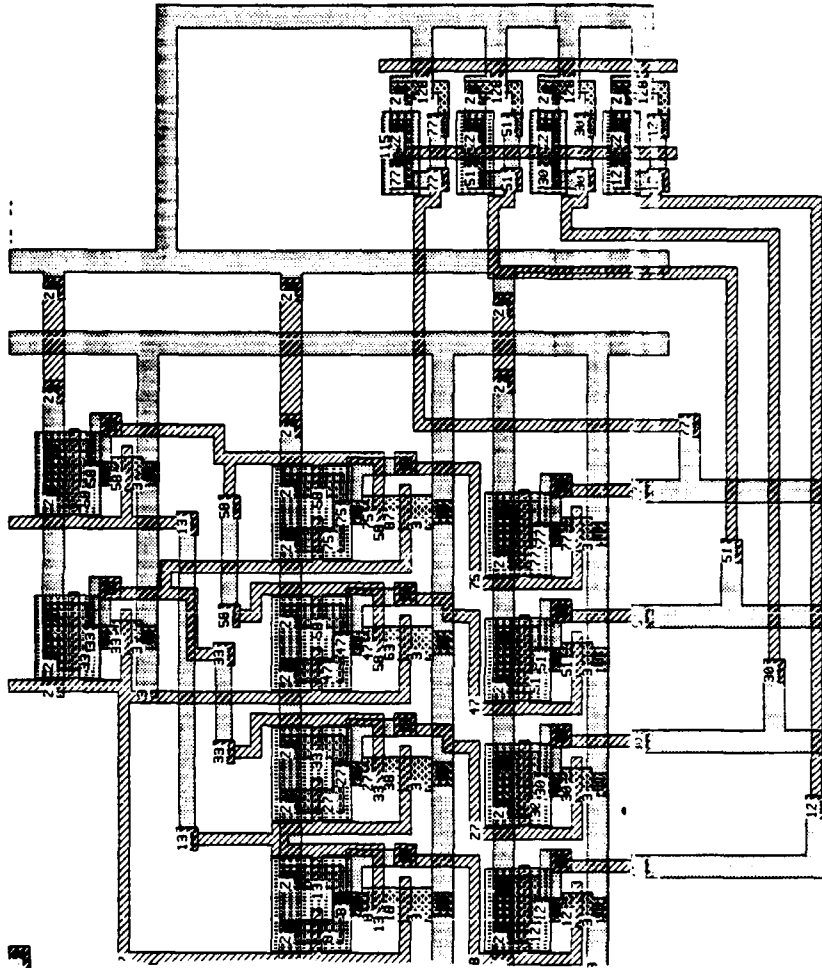
Figure B-7. Node Plot of Decoder Precharged at
External Nodes.

Table B-3

2X4 DECODER ALL OUTPUTS PRECHARGED NODE LIST

```
GND      0
Vdd      1
NMOS     0
PMOS     1
12       2
128      3
2        4
30       5
51       6
77       7
115      8
58       9
13       10
3        11
75       12
33       13
87       14
47       15
7        16
63       17
27       18
38       19
8        20
18       21
```

Ø   CMOS/SOS 2X4 DECODER WITH OUTPUTS PRECHARGED

Ø****   INPUT LISTING   TEMPERATURE =   27.000 DEG C

Ø***

```
 .WIDTH OUT=80
 .OPTIONS ITL1=500 ITL5=0
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
 +LEVEL=1
 VDD 1 Ø DC 5V
 M1  1 3 2 Ø  NMOS  L=5.ØU W=5.ØU
 M2  1 3 5 Ø  NMOS  L=5.ØU W=5.ØU
 M3  1 3 6 Ø  NMOS  L=5.ØU W=5.ØU
 M4  1 3 7 Ø  NMOS  L=5.ØU W=5.ØU
 M5  2 8 1 1  PMOS  L=5.ØU W=1Ø.ØU
 M6  5 8 1 1  PMOS  L=5.ØU W=1Ø.ØU
 M7  6 8 1 1  PMOS  L=5.ØU W=1Ø.ØU
 M8  7 8 1 1  PMOS  L=5.ØU W=1Ø.ØU
 M9  Ø 1Ø 9 Ø  NMOS  L=5.ØU W=15.ØU
 M1Ø 1 9 12 1  PMOS  L=5.ØU W=1Ø.ØU
 M11 1 1Ø 9 1  PMOS  L=5.ØU W=3Ø.ØU
 M12 14 13 Ø Ø  NMOS  L=5.ØU W=15.ØU
 M13 14 9 12 Ø  NMOS  L=5.ØU W=15.ØU
 M14 Ø 12 7 Ø  NMOS  L=5.ØU W=15.ØU
 M15 1 13 12 1  PMOS  L=5.ØU W=1Ø.ØU
 M16 1 12 7 1  PMOS  L=5.ØU W=3Ø.ØU
 M17 1 9 15 1  PMOS  L=5.ØU W=1Ø.ØU
 M18 Ø 16 13 Ø  NMOS  L=5.ØU W=15.ØU
 M19 17 16 Ø Ø  NMOS  L=5.ØU W=15.ØU
 M2Ø 17 9 15 Ø  NMOS  L=5.ØU W=15.ØU
 M21 1 16 13 1  PMOS  L=5.ØU W=3Ø.ØU
 M22 Ø 15 6 Ø  NMOS  L=5.ØU W=15.ØU
 M23 1 16 15 1  PMOS  L=5.ØU W=1Ø.ØU
 M24 1 15 6 1  PMOS  L=5.ØU W=3Ø.ØU
 M25 1 13 18 1  PMOS  L=5.ØU W=1Ø.ØU
 M26 19 1Ø Ø Ø  NMOS  L=5.ØU W=15.ØU
 M27 19 13 18 Ø  NMOS  L=5.ØU W=15.ØU
 M28 Ø 18 5 Ø  NMOS  L=5.ØU W=15.ØU
 M29 1 1Ø 18 1  PMOS  L=5.ØU W=1Ø.ØU
 M3Ø 1 18 5 1  PMOS  L=5.ØU W=3Ø.ØU
 M31 1 1Ø 2Ø 1  PMOS  L=5.ØU W=1Ø.ØU
 M32 21 16 Ø Ø  NMOS  L=5.ØU W=15.ØU
 M33 21 1Ø 2Ø Ø  NMOS  L=5.ØU W=15.ØU
 M34 Ø 2Ø 2 Ø  NMOS  L=5.ØU W=15.ØU
 M35 1 2Ø 2 1  PMOS  L=5.ØU W=3Ø.ØU
 M36 1 16 2Ø 1  PMOS  L=5.ØU W=1Ø.ØU
 C37 1 Ø Ø.1139PF
 C38 Ø Ø Ø.561PF
 C39 16 Ø Ø.157PF
 C4Ø 2Ø Ø Ø.12GPF
 C41 2 Ø Ø.234PF
 C42 1Ø Ø Ø.151PF
 C43 18 Ø Ø.127PF
 C44 5 Ø Ø.234PF
 C45 13 Ø Ø.182PF
 C46 15 Ø Ø.12ØPF
```

```
C47 6 Ø Ø.234PF
C48 9 Ø Ø.171PF
C49 12 Ø Ø.128PF
C5Ø 7 Ø Ø.234PF
C51 3 Ø Ø.5ØPF
VIN1 16 Ø PULSE (ØV ØV 5NS ØNS ØNS 1ØNS)
VIN2 1Ø Ø PULSE (ØV ØV 5NS ØNS ØNS 1ØNS)
VPHI1 3 Ø PULSE (ØV ØV 4NS ØNS ØNS 2NS)
VPHI1BAR 8 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
.TRAN Ø.5NS 4ØNS
.PLOT TRAN V(7) V(2) V(6) (ØV,5V)
.END
```

```
1*******11/30/04 ******** SPICE 2G.1 (15OCT80) ********23:26:23*****
#       CMOS/SOS 2X4 DECODER WITH OUTPUTS PRECHARGED X#

#****     TRANSIENT ANALYSIS              TEMPERATURE =   27.### DEG C

#******************************************************************

#LEGEND:

 *: V(7)
 +: V(2)
 =: V(6)
X
      TIME      V(7)

X(*+=)---------- #.    d+##    1.25#d+##    2.5##d+##     3.75#d+## 5.###d+##
                  -  -  - - - - - -  - - - - -  - - - - - -  - - - - -
#.    d+##   5.###d+## X                     .               .           :
5.###d-1#   5.###d+## X                      .               .           :
1.###d-#9   5.###d+## X                      .               .           :
1.5##d-#9   5.###d+## X                      .               .           :
2.###d-#9   5.###d+## X                      .               .           :
2.5##d-#9   5.###d+## X                      .               .           :
3.###d-#9   5.###d+## X                      .               .           :
3.5##d-#9   5.###d+## X                      .               .           :
4.###d-#9   5.###d+## X                      .               .           :
4.5##d-#9   5.###d+##  . X                    .               .          :
5.###d-#9   5.###d+##       X                 .               .          :
5.5##d-#9   5.###d+##        X                .               .          :
6.###d-#9   5.###d+##         X               .               .          :
6.5##d-#9   5.###d+##          X .            .               .          :
7.###d-#9   4.999d+##        =    .           .               .          :
7.5##d-#9   4.929d+##     .      =            .               .          :
8.###d-#9   4.584d+##   .                     .               .          :
8.5##d-#9   3.873d+##  . .                     .               .         :
9.###d-#9   2.912d+##  .             .         .               .         :
9.5##d-#9   1.343d+##  =             .         .               .         :
1.###d-#8   1.2#1d+##  =          .            .               .         :
1.#5#d-#8   6.036d-#1  =       .               .               .         :
1.1##d-#8   3.6#5d-#1  =     .                 .               .         :
1.15#d-#8   1.76#d-#1  =   .                    .               .        :
1.2##d-#8   9.#68d-#2  =-*                       .               .       :
1.25#d-#8   4.666d-#2  -*                        .               .       :
1.3##d-#8   2.329d-#2 X                          .               .       :
1.35#d-#8   1.179d-#2 X                          .               .       :
1.4##d-#8   6.457d-#3 X                          .               .       :
1.45#d-#8   3.217d-#3 X                          .               .       :
1.5##d-#8   1.374d-#3 X                          .               .       :
1.55#d-#8   6.866d-#4 X                          .               .       :
1.6##d-#8   3.567d-#4 X                          .               .       :
1.65#d-#8   1.#74d-#4 X                          .               .       :
1.7##d-#8   9.893d-#5 X                          .               .       :
1.75#d-#8   5.593d-#5 X                          .               .       :
1.8##d-#8   8.#46d-#3 X                          .               .       :
1.85#d-#8   8.#29d-#2 =*       .                 .               .       :
1.9##d-#8   2.#35d-#1 =                          .               .       :
1.95#d-#8   6.976d-#1 =     .    *=              .               .       :
2.###d-#8   1.377d### =                          .               .       :
2.#5#d-#8   2.2#5d+## =-  .                       .              .       :
2.1##d-#8   3.#65d+## =-*                         .               .      :
2.15#d-#8   3.##7d+## =-+                          .              .      :
2.2##d-#8   4.322d+## X                            .               .     :
2.25#d-#8   4.62#d+## X                             .               .    :
2.3##d-#8   4.81#d+## X                              .               .   :
2.35#d-#8   4.9#4d+## X                               .               .  :
2.4##d-#8   4.947d+## X                                 .               .:
2.45#d-#8   4.976d+## X                                  .               .
2.5##d-#8   4.988d+## X                                   .              :
2.55#d-#8   4.994d+## X                     .               .            :
2.6##d-#8   4.997d+## X                     .               .            :
2.65#d-#8   4.999d+## X                     .               .            :
2.7##d-#8   4.999d+## X                     .               .            :
2.75#d-#8   5.###d+## X                     .               .            :
2.8##d-#8   5.###d+## X                     .               .            :
2.85#d-#8   5.###d+## X                     .               .            :
2.9##d-#8   5.###d+## X                     .               .            :
2.95#d-#8   5.###d+## X                     .               .            :
3.###d-#8   5.###d+## X                     .               .            :
3.#5#d-#8   5.###d+## X                     .               .            :
3.1##d-#8   5.###d+## X                     .               .            :
3.15#d-#8   5.###d+## X                     .               .            :
3.2##d-#8   5.###d+## X                     .               .            :
3.25#d-#8   5.###d+## X                     .               .            :
3.3##d-#8   5.###d+## X                     .               .            :
3.35#d-#8   5.###d+## X                     .               .            :
3.4##d-#8   5.###d+## X                     .               .            :
3.45#d-#8   5.###d+## X                     .               .            :
3.5##d-#8   5.###d+## X                     .               .            :
3.55#d-#8   5.###d+## X                     .               .            :
3.6##d-#8   5.###d+## X                     .               .            :
3.65#d-#8   5.###d+## X                     .               .            :
3.7##d-#8   5.###d+## X                     .               .            :
3.75#d-#8   5.###d+## X                     .               .            :
3.8##d-#8   5.###d+## X                     .               .            :
3.85#d-#8   5.###d+## X                     .               .            :
3.9##d-#8   5.###d+## X                     .               .            :
3.95#d-#8   5.###d+## X                     .               .            :
4.###d-#8   5.###d+## X                     .               .            :
                  -  -  - - - - - -  - - - - -  - - - - - -  - - - - -
```

Figure B-8.   SPICE Plot of Decoder Outputs Using
               Basic Width Transmission Gates.

B-21

Ø   CMOS/SOS 2X4 DECODER WITH OUTPUTS PRECHARGED - WIDTH TIMES TWO

Ø****   INPUT LISTING   TEMPERATURE =   27.000 DEG C

Ø***

```
.WIDTH OUT=80
.OPTIONS ITL1=500 ITL5=0
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
+LEVEL=1
VDD 1 Ø DC 5V
M1  1  3  2  Ø NMOS L=5.0U W=10.0U
M2  1  3  5  Ø NMOS L=5.0U W=10.0U
M3  1  3  6  Ø NMOS L=5.0U W=10.0U
M4  1  3  7  Ø NMOS L=5.0U W=10.0U
M5  2  8  1  1 PMOS L=5.0U W=20.0U
M6  5  8  1  1 PMOS L=5.0U W=20.0U
M7  6  8  1  1 PMOS L=5.0U W=20.0U
M8  7  8  1  1 PMOS L=5.0U W=20.0U
M9  Ø 10  9  Ø NMOS L=5.0U W=15.0U
M10 1  9 12  1 PMOS L=5.0U W=10.0U
M11 1 10  9  1 PMOS L=5.0U W=30.0U
M12 14 13 Ø  Ø NMOS L=5.0U W=15.0U
M13 14 9 12  Ø NMOS L=5.0U W=15.0U
M14 Ø 12  7  Ø NMOS L=5.0U W=15.0U
M15 1 13 12  1 PMOS L=5.0U W=10.0U
M16 1 12  7  1 PMOS L=5.0U W=30.0U
M17 1  9 15  1 PMOS L=5.0U W=10.0U
M18 Ø 16 13  Ø NMOS L=5.0U W=15.0U
M19 17 16 Ø  Ø NMOS L=5.0U W=15.0U
M20 17 9 15  Ø NMOS L=5.0U W=15.0U
M21 1 16 13  1 PMOS L=5.0U W=30.0U
M22 Ø 15  6  Ø NMOS L=5.0U W=15.0U
M23 1 16 15  1 PMOS L=5.0U W=10.0U
M24 1 15  6  1 PMOS L=5.0U W=30.0U
M25 1 13 18  1 PMOS L=5.0U W=10.0U
M26 19 10 Ø  Ø NMOS L=5.0U W=15.0U
M27 19 13 18 Ø NMOS L=5.0U W=15.0U
M28 Ø 18  5  Ø NMOS L=5.0U W=15.0U
M29 1 10 18  1 PMOS L=5.0U W=10.0U
M30 1 18  5  1 PMOS L=5.0U W=30.0U
M31 1 10 20  1 PMOS L=5.0U W=10.0U
M32 21 16 Ø  Ø NMOS L=5.0U W=15.0U
M33 21 10 20 Ø NMOS L=5.0U W=15.0U
M34 Ø 20  2  Ø NMOS L=5.0U W=15.0U
M35 1 20  2  1 PMOS L=5.0U W=30.0U
M36 1 16 20  1 PMOS L=5.0U W=10.0U
C37 1 Ø Ø.1139PF
C38 Ø Ø Ø.561PF
C39 16 Ø Ø.157PF
C40 20 Ø Ø.126PF
C41 2 Ø Ø.234PF
C42 10 Ø Ø.151PF
C43 18 Ø Ø.127PF
C44 5 Ø Ø.234PF
C45 13 Ø Ø.182PF
C46 15 Ø Ø.128PF
C47 6 Ø Ø.234PF
```

```
C48 9 Ø Ø.171PF
C49 12 Ø Ø.128PF
C5Ø 7 Ø Ø.234PF
C51 3 Ø Ø.5ØPF
VIN1 16 Ø PULSE ( ØV 5V 5NS ØNS ØNS 1ØNS)
VIN2 1Ø Ø PULSE ( ØV 5V 5NS ØNS ØNS 1ØNS)
VPHI1 3 Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS)
VPHI1BAR 8 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
.TRAN Ø.5NS 4ØNS
.PLOT TRAN V(7) V(2) V(6) (ØV,5V)
.END
```

```
1********11/3#/84 ******** SPICE 2G.1 (15OCT8#) ********23:26:4#*****

#      CMOS/SOS 2X4 DECODER WITH OUTPUTS PRECHARGED - WIDTH TIMES TWO

#****    TRANSIENT ANALYSIS              TEMPERATURE =   27.### DEG C

#*******************************************************************

#LEGEND:

 *: V(7)
 +: V(2)
 =: V(6)
X
    TIME     V(7)

X(*+=)----------- #.   d+##    1.25#d+##    2.5##d+##    3.75#d+## 5.###d+##
 #.   d+##  5.###d+## X
 5.###d-1#  5.###d+## X
 1.###d-#9  5.###d+## X
 1.5##d-#9  5.###d+## X
 2.###d-#9  5.###d+## X
 2.5##d-#9  5.###d+## X
 3.###d-#9  5.###d+## X
 3.5##d-#9  5.###d+## X
 4.###d-#9  5.###d+## X
 4.5##d-#9  5.###d+## .          X
 5.###d-#9  5.###d+## .              X
 5.5##d-#9  5.###d+## .                X
 6.###d-#9  5.###d+## .                 X
 6.5##d-#9  5.###d+## .                  X .  .  .
 7.###d-#9  4.999d+## .                 .  .    .
 7.5##d-#9  4.914d+##       .    .     .          .
 8.###d-#9  4.571d+##                 .          +
 8.5##d-#9  3.885d+##      .          .              X    .
 9.###d-#9  2.92#d+##   .            .          .        .
 9.5##d-#9  1.964d+## .            .     +        .        +
 1.###d-#8  1.191d+## X         .         .          .
 1.#5#d-#8  6.661d-#1 =       .   .       .
 1.1##d-#8  3.455d-#1 =     .  .         .
 1.15#d-#8  1.872d-#1 =    .            .
 1.2##d-#8  9.395d-#2 =*   .           .          .
 1.25#d-#8  4.769d-#2 =*                              .
 1.3##d-#8  2.45#d-#2 X
 1.35#d-#8  1.252d-#2 X
 1.4##d-#8  6.#26d-#3 X
 1.45#d-#8  2.923d-#3 X
 1.5##d-#8  1.59#d-#3 X
 1.55#d-#8  6.8#5d-#4 X
 1.6##d-#8  3.5#4d-#4 X
 1.65#d-#8  1.841d-#4 X
 1.7##d-#8  9.7#4d-#5 X
 1.75#d-#8  1.294d-#3 X
 1.8##d-#8  6.333d-#3 X
 1.85#d-#8  8.19#d-#2 =*   .
 1.9##d-#8  2.92#d-#1 =   .      .       .
 1.95#d-#8  7.#68d-#1 =    .    **       .
 2.###d-#8  1.367d+## =     .   .       .
 2.#5#d-#8  2.2#2d+## =* .
 2.1##d-#8  3.#6#d+## =*
 2.15#d-#8  3.611d+## =*
 2.2##d-#8  4.316d+## X
 2.25#d-#8  4.626d+## X                            .
 2.3##d-#8  4.8#3d+## X
 2.35#d-#8  4.9#8d+## X
 2.4##d-#8  4.947d+## X
 2.45#d-#8  4.976d+## X
 2.5##d-#8  4.988d+## X
 2.55#d-#8  4.994d+## X
 2.6##d-#8  4.997d+## X
 2.65#d-#8  4.999d+## X
 2.7##d-#8  4.999d+## X
 2.75#d-#8  5.###d+## X
 2.8##d-#8  5.###d+## X
 2.85#d-#8  5.###d+## X
 2.9##d-#8  5.###d+## X
 2.95#d-#8  5.###d+## X
 3.###d-#8  5.###d+## X
 3.#5#d-#8  5.###d+## X
 3.1##d-#8  5.###d+## X
 3.15#d-#8  5.###d+## X
 3.2##d-#8  5.#8#d+## X
 3.25#d-#8  5.###d+## X
 3.3##d-#8  5.###d+## X
 3.35#d-#8  5.###d+## X
 3.4##d-#8  5.###d+## X
 3.45#d-#8  5.###d+## X
 3.5##d-#8  5.###d+## X
 3.55#d-#8  5.###d+## X
 3.6##d-#8  5.###d+## X
 3.65#d-#8  5.###d+## X
 3.7##d-#8  5.###d+## X
 3.75#d-#8  5.###d+## X
 3.8##d-#8  5.###d+## X
 3.85#d-#8  5.###d+## X
 3.9##d-#8  5.###d+## X
 3.95#d-#8  5.###d+. # X
 4.###d-#8  5.###d+## X
```

Figure B-9.   SPICE Plot of Precharged Decoder Outputs
             Transmission Gate Widths Doubled.

Ø   CMOS/SOS 2X4 DECODER WITH OUTPUTS PRECHARGED

Ø****   INPUT LISTING   TEMPERATURE =   27.000 DEG C

Ø***

```
 .WIDTH OUT=80
 .OPTIONS ITL1=500 ITL5=0
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
 +LEVEL=1
 VDD 1 0 DC 5V
 M1  1  3  2  0 NMOS L=5.0U W=15.0U
 M2  1  3  5  0 NMOS L=5.0U W=15.0U
 M3  1  3  6  0 NMOS L=5.0U W=15.0U
 M4  1  3  7  0 NMOS L=5.0U W=15.0U
 M5  2  8  1  1 PMOS L=5.0U W=30.0U
 M6  5  8  1  1 PMOS L=5.0U W=30.0U
 M7  6  8  1  1 PMOS L=5.0U W=30.0U
 M8  7  8  1  1 PMOS L=5.0U W=30.0U
 M9  0  10  9  0 NMOS L=5.0U W=15.0U
 M10 1  9  12  1 PMOS L=5.0U W=10.0U
 M11 1  10  9  1 PMOS L=5.0U W=30.0U
 M12 14 13  0  0 NMOS L=5.0U W=15.0U
 M13 14  9  12  0 NMOS L=5.0U W=15.0U
 M14  0 12  7  0 NMOS L=5.0U W=15.0U
 M15  1 13 12  1 PMOS L=5.0U W=10.0U
 M16  1 12  7  1 PMOS L=5.0U W=30.0U
 M17  1  9 15  1 PMOS L=5.0U W=10.0U
 M18  0 16 13  0 NMOS L=5.0U W=15.0U
 M19 17 16  0  0 NMOS L=5.0U W=15.0U
 M20 17  9 15  0 NMOS L=5.0U W=15.0U
 M21  1 16 13  1 PMOS L=5.0U W=30.0U
 M22  0 15  6  0 NMOS L=5.0U W=15.0U
 M23  1 16 15  1 PMOS L=5.0U W=10.0U
 M24  1 15  6  1 PMOS L=5.0U W=30.0U
 M25  1 13 18  1 PMOS L=5.0U W=10.0U
 M26 19 10  0  0 NMOS L=5.0U W=15.0U
 M27 19 13 18  0 NMOS L=5.0U W=15.0U
 M28  0 18  5  0 NMOS L=5.0U W=15.0U
 M29  1 10 18  1 PMOS L=5.0U W=10.0U
 M30  1 18  5  1 PMOS L=5.0U W=30.0U
 M31  1 10 20  1 PMOS L=5.0U W=10.0U
 M32 21 16  0  0 NMOS L=5.0U W=15.0U
 M33 21 10 20  0 NMOS L=5.0U W=15.0U
 M34  0 20  2  0 NMOS L=5.0U W=15.0U
 M35  1 20  2  1 PMOS L=5.0U W=30.0U
 M36  1 16 20  1 PMOS L=5.0U W=10.0U
 C37  1  0  0.1139PF
 C38  0  0  0.561PF
 C39 16  0  0.157PF
 C40 20  0  0.126PF
 C41  2  0  0.234PF
 C42 10  0  0.151PF
 C43 18  0  0.127PF
 C44  5  0  0.234PF
 C45 13  0  0.182PF
 C46 15  0  0.120PF
 C47  6  0  0.234PF
```

```
C48 9 0 0.171PF
C49 12 0 0.120PF
C50 7 0 0.234PF
C51 3 0 0.50PF
VIN1 16 0 PULSE (0V 5V 5NS 0NS 0NS 10NS)
VIN2 10 0 PULSE (5V 0V 5NS 0NS 0NS 10NS)
VPHI1 3 0 PULSE (0V 5V 4NS 0NS 0NS 2NS)
VPHI1BAR 8 0 PULSE (5V 0V 4NS 0NS 0NS 2NS)
.TRAN 0.5NS 40NS
.PLOT TRAN V(7) V(2) V(6) (0V,5V)
.END
```

```
1********11/30/84 ********  SPICE 2G.1 (15OCT80)  *********23:26:55*****
#         CMOS/SOS 2X4 DECODER WITH OUTPUTS PRECHARGED  X3
#****     TRANSIENT ANALYSIS                 TEMPERATURE =   27.000 DEG C
#****************************************************************************

#LEGEND:

 *: V(7)
 +: V(2)
 =: V(6)
X
     TIME      V(7)

X(*+=)----------   0.     d+00      1.250d+00      2.500d+00      3.750d+00   5.000d+00
```
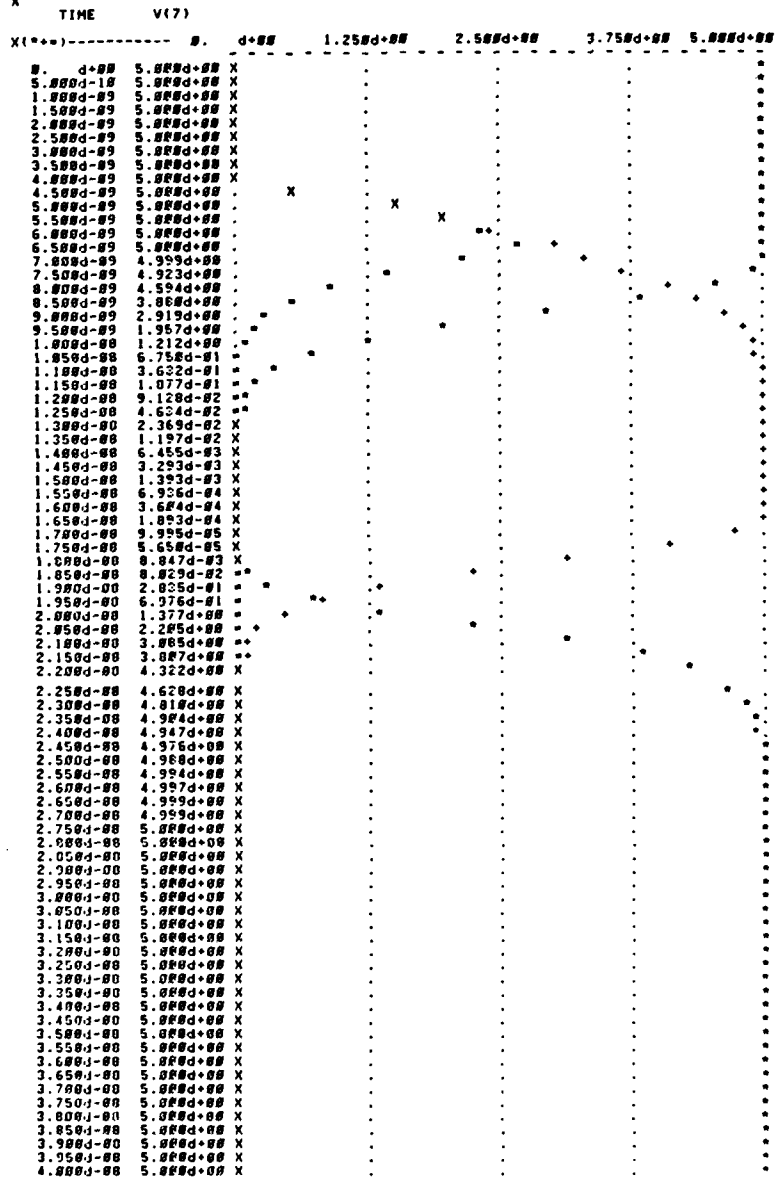

Figure B-10.   SPICE Plot of Precharged Decoder Outputs
               Transmission Gate Widths Tripled.

B-27
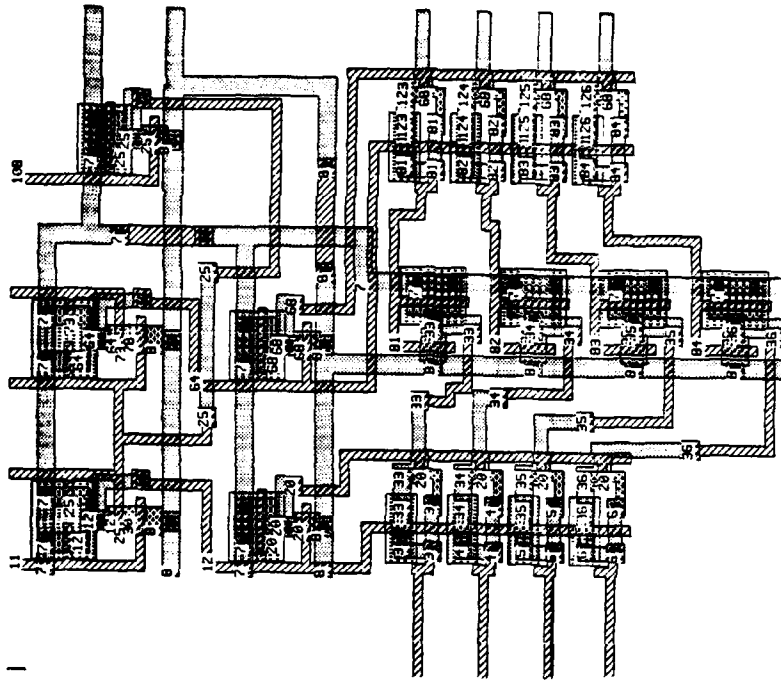
Figure B-11.   Basic B Register Node Plot.

Table B-4

BASIC B REGISTER NODE LIST

GND	0
Vdd	1
NMOS	0
PMOS	1
34	2
68	3
126	4
33	5
125	6
32	7
124	8
31	9
123	10
64	11
25	12
103	13
8	14
7	15
36	16
35	17
37	18
38	19
73	20
70	21
69	23
5	24
6	25
9	26
12	27
11	28
30	29

```
.WIDTH OUT=8Ø
.OPTIONS ITL1=5ØØ ITL5=Ø
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
+LEVEL=1
VDD 1 Ø DC 5V
M1  4  3  2  Ø NMOS L=5.ØU W=5.ØU
M2  6  3  5  Ø NMOS L=5.ØU W=5.ØU
M3  8  3  7  Ø NMOS L=5.ØU W=5.ØU
M4 1Ø  3  9  Ø NMOS L=5.ØU W=5.ØU
M5  2 11  4  1 PMOS L=5.ØU W=1Ø.ØU
M6  5 11  6  1 PMOS L=5.ØU W=1Ø.ØU
M7  7 11  8  1 PMOS L=5.ØU W=1Ø.ØU
M8  9 11 1Ø  1 PMOS L=5.ØU W=1Ø.ØU
M9  Ø 13 12  Ø NMOS L=5.ØU W=15.ØU
M1Ø 1 13 12  1 PMOS L=5.ØU W=3Ø.ØU
M11 16  2  1  1 PMOS L=5.ØU W=3Ø.ØU
M12 17  5  1  1 PMOS L=5.ØU W=3Ø.ØU
M13 18  7  1  1 PMOS L=5.ØU W=3Ø.ØU
M14 19  9  1  1 PMOS L=5.ØU W=3Ø.ØU
M15 1 2Ø 11  1 PMOS L=5.ØU W=1Ø.ØU
M16 Ø  2 16  Ø NMOS L=5.ØU W=15.ØU
M17 Ø  5 17  Ø NMOS L=5.ØU W=15.ØU
M18 Ø  7 18  Ø NMOS L=5.ØU W=15.ØU
M19 Ø  9 19  Ø NMOS L=5.ØU W=15.ØU
M2Ø 21 12  Ø  Ø NMOS L=5.ØU W=15.ØU
M21 21 2Ø 11  Ø NMOS L=5.ØU W=15.ØU
M22 Ø 11  3  Ø NMOS L=5.ØU W=15.ØU
M23 1 11  3  1 PMOS L=5.ØU W=3Ø.ØU
M24 1 12 11  1 PMOS L=5.ØU W=1Ø.ØU
M25 16 23 22  Ø NMOS L=5.ØU W=5.ØU
M26 17 23 24  Ø NMOS L=5.ØU W=5.ØU
M27 18 23 25  Ø NMOS L=5.ØU W=5.ØU
M28 19 23 26  Ø NMOS L=5.ØU W=5.ØU
M29 1 12 27  1 PMOS L=5.ØU W=1Ø.ØU
M3Ø 22 27 16  1 FMOS L=5.ØU W=1Ø.ØU
M31 24 27 17  1 FMOS L=5.ØU W=1Ø.ØU
M32 25 27 18  1 FMOS L=5.ØU W=1Ø.ØU
M33 26 27 19  1 FMOS L=5.ØU W=1Ø.ØU
M34 29 28  Ø  Ø NMOS L=5.ØU W=15.ØU
M35 29 12 27  Ø NMOS L=5.ØU W=15.ØU
M36 Ø 27 23  Ø NMOS L=5.ØU W=15.ØU
M37 1 27 23  1 PMOS L=5.ØU W=3Ø.ØU
M38 1 23 27  1 PMOS L=5.ØU W=1Ø.ØU
C39 26 Ø Ø.84PF
C4Ø 25 Ø Ø.84PF
C41 24 Ø Ø.84PF
C42 22 Ø Ø.84PF
C43 1 Ø Ø.7ØØPF
C44 Ø Ø Ø.5Ø5PF
C45 27 Ø Ø.181PF
C46 23 Ø Ø.128PF
```

```
C47  12  0  0.230PF
C48  19  0  0.135PF
C49  18  0  0.139PF
C50  17  0  0.145PF
C51  16  0  0.151PF
C52  11  0  0.200PF
C53   3  0  0.155PF
C54   9  0  0.111PF
C55   7  0  0.109PF
C56   5  0  0.114PF
C57   2  0  0.120PF
C58  10  0  0.54PF
C59   8  0  0.54PF
C60   6  0  0.54PF
C61   4  0  0.54PF
VREGSEL 13 0 PULSE (0V 0V 0NS 0NS 0NS 30NS)
VIN1 20 0 PULSE (0V 5V 5NS 0NS 0NS 30NS)
VIN2 28 0 PULSE (0V 5V 5NS 0NS 0NS 30NS)
VDAT1 10 0 PULSE (5V 0V 5NS 0NS 0NS 10NS)
VDAT2  8 0 PULSE (0V 5V 5NS 0NS 0NS 10NS)
VDAT3  6 0 PULSE (0V 5V 5NS 0NS 0NS 10NS)
VDAT4  4 0 PULSE (5V 0V 5NS 0NS 0NS 10NS)
.TRAN 0.5NS 40NS
.PLOT TRAN V(26) V(25) (0V,5V)
.END
```

\# CMOS/SOS B REGISTER BASIC TRANSIENT ANALYSIS

\#•••• TRANSIENT ANALYSIS TEMPERATURE = 27.### DEG C

\#•••

\#LEGEND:

*: V(26)
+: V(25)
X

TIME	V(26)					
X(*+)------------	#.	d+##	1.25#d+##	2.5##d+##	3.75#d+## 5.###d+##

```
#.        d+##    2.5##d+##  :                   :        X             :
5.###d-1#  2.5##d+##  :                   :        X             :
1.###d-#9  2.5##d+##  :                   :        X             :
1.5##d-#9  2.5##d+##  :                   :        X             :
2.###d-#9  2.5##d+##  :                   :        X             :
2.5##d-#9  2.5##d+##  :                   :        X             :
3.###d-#9  2.5##d+##  :                   :        X             :
3.5##d-#9  2.5##d+##  :                   :        X             :
4.###d-#9  2.5##d+##  :                   :        X             :
4.5##d-#9  2.5##d+##  :                   :        X             :
5.###d-#9  2.5##d+##  :                   :        X             :
5.5##d-#9  2.5##d+##  :                   :        X             :
6.###d-#9  2.5##d+##  :                   :        X             :
6.5##d-#9  2.5##d+##  :                   :        X             :
7.###d-#9  2.5##d+##  :                   :        X             :
7.5##d-#9  2.5##d+##  :                   :        X             :
8.###d-#9  2.5#1d+##  :                   :        X             :
8.5##d-#9  2.5#4d+##  :                   :        X             :
9.###d-#9  2.51#d+##  :                   :        X             :
9.5##d-#9  2.521d+##  :                   :        X             :
1.###d-#8  2.538d+##  :                   :        X             :
1.#5#d-#8  2.56#d+##  :                   :        X.            :
1.1##d-#8  2.598d+##  :                   :       *  *           :
1.15#d-#8  2.644d+##  :                   :      *    *          :
1.2##d-#8  2.7#2d+##  :                   :     *      *         :
1.25#d-#8  2.764d+##  :                   :    *        *        :
1.3##d-#8  2.83#d+##  :                   :   *          *       :
1.35#d-#8  2.896d+##  :                   :  *            *      :
1.4##d-#8  2.962d+##  :                   : *              *     :
1.45#d-#8  3.#26d+##  :                   :*                *    :
1.5##d-#8  3.#9#d+##  :                  *:                  *   :
1.55#d-#8  3.153d+##  :                 * :                   *  :
1.6##d-#8  3.214d+##  :                *  :                    * :
1.65#d-#8  3.27#d+##  :               *   :                     *:
1.7##d-#8  3.312d+##  :              *    :                      :*
1.75#d-#8  3.332d+##  :             *     :                      : *
1.8##d-#8  3.332d+##  :             *     :                      : *
1.85#d-#8  3.318d+##  :             *     :                      : *
1.9##d-#8  3.269d+##  :              *    :                      :*
1.95#d-#8  3.2#9d+##  :               *   :                     *:
2.###d-#8  3.132d+##  :                *  :                    * :
2.#5#d-#8  3.#5#d+##  :                 * :                   *  :
2.1##d-#8  2.969d+##  :                  *:                  *   :
2.15#d-#8  2.88#d+##  :                   :*                *    :
2.2##d-#8  2.8#9d+##  :                   : *              *     :
2.25#d-#8  2.732d+##  :                   :  *            *      :
2.3##d-#8  2.656d+##  :                   :   *          *       :
2.35#d-#8  2.562d+##  :                   :    *        *        :
2.4##d-#8  2.5#9d+##  :                   :     X              :
2.45#d-#8  2.428d+##  :                   :    *  *           :
2.5##d-#8  2.368d+##  :                  *:        *          :
2.55#d-#8  2.3##d+##  :                 * :         *         :
2.6##d-#8  2.233d+##  :               * :           *        :
2.65#d-#8  2.167d+##  :              *   :            *       :
2.7##d-#8  2.1#3d+##  :            *     :             *      :
2.75#d-#8  2.#48d+##  :           *      :              *     :
2.8##d-#8  1.978d+##  :         *        :               *    :
2.85#d-#8  1.918d+##  :        *         :                *   :
2.9##d-#8  1.858d+##  :       *          :                 *  :
2.95#d-#8  1.8##d+##  :      *           :                  * :
3.###d-#8  1.743d+##  :     *            :                   *:
3.#5#d-#8  1.687d+##  :    *             :                    :*
3.1##d-#8  1.632d+##  :   *              :                    : *
3.15#d-#8  1.579d+##  :  *               :                    : *
3.2##d-#8  1.527d+##  : *                :                    : *
3.25#d-#8  1.476d+##  :.*                :                    : *
3.3##d-#8  1.426d+##  :*                 :                    :  *
3.35#d-#8  1.377d+##  *                  :                    :  *
3.4##d-#8  1.33#d+##  :                  :                    :  *
3.45#d-#8  1.283d+##  :                  :                    :   *
3.5##d-#8  1.238d+##  :                  :                    :   *
3.55#d-#8  1.194d+##  *                  :                    :   *
3.6##d-#8  1.152d+##  :                  :                    :    *
3.65#d-#8  1.11#d+##  *                  :                    :    *
3.7##d-#8  1.#7#d+##  :                  :                    :    *
3.75#d-#8  1.#31d+##  :                  :                    :     *
3.8##d-#8  9.941d-#1  :                  :                    :     *
3.85#d-#8  9.6#6d-#1  :                  :                    :     *
3.9##d-#8  9.3#4d-#1  :                  :                    :     *
3.95#d-#8  9.#97d-#1  :                  :                    :     *
4.###d-#8  8.973d-#1  :                  :                    :     *
```

Figure B-12. SPICE Plot of Basic B Register Output.
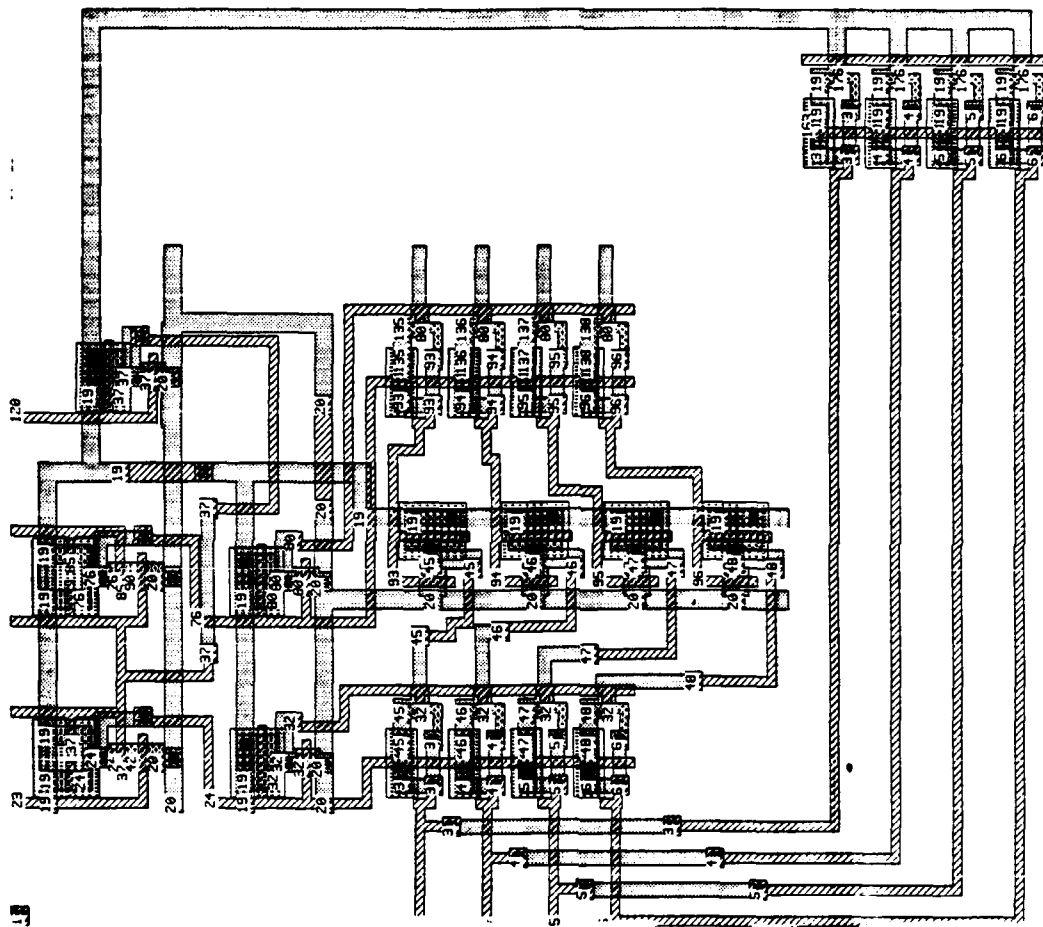
Figure B-13.   Precharged B Register Node Plot.

Table B-5

PRECHARGED 3 REGISTER NODE LIST

GND	0
Vdd	1
NMOS	0
PMOS	1
6	2
176	3
19	4
5	5
4	6
3	7
163	8
96	9
80	10
138	11
95	12
137	13
94	14
136	15
93	16
135	17
76	18
37	19
120	20
20	21
48	22
47	23
46	24
45	25
85	26
90	27
32	28
24	29
23	30
42	31

Ø   CMOS/SOS PRECHARGED B REGISTER TRANSIENT ANALYSIS

Ø****   INPUT LISTING   TEMPERATURE =   27.ØØØ DEG C

Ø***


```
.WIDTH OUT=8Ø
.OPTIONS ITL1=5ØØ ITL5=Ø
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
+LEVEL=1
VDD 1 Ø DC 5V
M1  1  3  2  Ø NMOS L=5.ØU W=5.ØU
M2  1  3  5  Ø NMOS L=5.ØU W=5.ØU
M3  1  3  6  Ø NMOS L=5.ØU W=5.ØU
M4  1  3  7  Ø NMOS L=5.ØU W=5.ØU
M5  2  8  1  1 PMOS L=5.ØU W=1Ø.ØU
M6  5  8  1  1 PMOS L=5.ØU W=1Ø.ØU
M7  6  8  1  1 PMOS L=5.ØU W=1Ø.ØU
M8  7  8  1  1 PMOS L=5.ØU W=1Ø.ØU
M9  11 1Ø 9  Ø NMOS L=5.ØU W=5.ØU
M1Ø 13 1Ø 12 Ø NMOS L=5.ØU W=5.ØU
M11 15 1Ø 14 Ø NMOS L=5.ØU W=5.ØU
M12 17 1Ø 16 Ø NMOS L=5.ØU W=5.ØU
M13 9  18 11 1 PMOS L=5.ØU W=1Ø.ØU
M14 12 18 13 1 PMOS L=5.ØU W=1Ø.ØU
M15 14 18 15 1 PMOS L=5.ØU W=1Ø.ØU
M16 16 18 17 1 PMOS L=5.ØU W=1Ø.ØU
M17 Ø 2Ø 19 Ø NMOS L=5.ØU W=15.ØU
M18 1 2Ø 19 1 PMOS L=5.ØU W=3Ø.ØU
M19 22 9  1  1 PMOS L=5.ØU W=3Ø.ØU
M2Ø 23 12 1  1 PMOS L=5.ØU W=3Ø.ØU
M21 24 14 1  1 PMOS L=5.ØU W=3Ø.ØU
M22 25 16 1  1 PMOS L=5.ØU W=3Ø.ØU
M23 1  26 18 1 PMOS L=5.ØU W=1Ø.ØU
M24 Ø 9  22 Ø NMOS L=5.ØU W=15.ØU
M25 Ø 12 23 Ø NMOS L=5.ØU W=15.ØU
M26 Ø 14 24 Ø NMOS L=5.ØU W=15.ØU
M27 Ø 16 25 Ø NMOS L=5.ØU W=15.ØU
M28 27 19 Ø Ø NMOS L=5.ØU W=15.ØU
M29 27 26 18 Ø NMOS L=5.ØU W=15.ØU
M3Ø Ø 18 1Ø Ø NMOS L=5.ØU W=15.ØU
M31 1 18 1Ø 1 PMOS L=5.ØU W=3Ø.ØU
M32 1 19 13 1 PMOS L=5.ØU W=1Ø.ØU
M33 22 28 2  Ø NMOS L=5.ØU W=5.ØU
M34 23 28 5  Ø NMOS L=5.ØU W=5.ØU
M35 24 28 6  Ø NMOS L=5.ØU W=5.ØU
M36 25 28 7  Ø NMOS L=5.ØU W=5.ØU
M37 1  19 29 1 PMOS L=5.ØU W=1Ø.ØU
M38 2  29 22 1 PMOS L=5.ØU W=1Ø.ØU
M39 5  29 23 1 PMOS L=5.ØU W=1Ø.ØU
M4Ø 6  29 24 1 PMOS L=5.ØU W=1Ø.ØU
M41 7  29 25 1 PMOS L=5.ØU W=1Ø.ØU
M42 31 3Ø 3  Ø NMOS L=5.ØU W=15.ØU
M43 31 19 29 Ø NMOS L=5.ØU W=15.ØU
M44 Ø 29 23 Ø NMOS L=5.ØU W=15.ØU
M45 1 29 23 1 PMOS L=5.ØU W=3Ø.ØU
M46 1 3Ø 29 1 PMOS L=5.ØU W=1Ø.ØU
C47 7 Ø Ø.94PF
```

```
C48 6 Ø Ø.94PF
C49 5 Ø Ø.94PF
C50 2 Ø Ø.94PF
C51 1 3 Ø.1103PF
C52 Ø Ø Ø.505PF
C53 29 Ø Ø.181PF
C54 28 Ø Ø.128PF
C55 19 Ø Ø.230PF
C56 25 Ø Ø.135PF
C57 24 Ø Ø.139PF
C58 23 Ø Ø.145PF
C59 22 Ø Ø.151PF
C60 18 Ø Ø.208PF
C61 10 Ø Ø.155PF
C62 16 Ø Ø.111PF
C63 14 Ø Ø.109PF
C64 12 Ø Ø.114PF
C65 9 Ø Ø.120PF
C66 17 Ø Ø.54PF
C67 15 Ø Ø.54PF
C68 13 Ø Ø.54PF
C69 11 Ø Ø.54PF
C70 3 Ø Ø.50PF
VREGSEL 20 Ø PULSE (ØV ØV ØNS ØNS ØNS 30NS)
VIN1 26 Ø PULSE (ØV 5V 5NS ØNS ØNS 30NS)
VIN2 30 Ø PULSE (ØV 5V 5NS ØNS ØNS 30NS)
VDAT1 17 Ø PULSE (5V ØV 5NS ØNS ØNS 10NS)
VDAT2 15 Ø PULSE (ØV 5V 5NS ØNS ØNS 10NS)
VDAT3 13 Ø PULSE (ØV 5V 5NS ØNS ØNS 10NS)
VDAT4 11 Ø PULSE (5V ØV 5NS ØNS ØNS 10NS)
VP1 3 Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS)
VP1BAR 8 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
.TRAN Ø.5NS 40NS
.PLOT TRAN V(7) V(6) (ØV.5V)
.END
```

0   CMOS/SOS PRECHARGED B REGISTER TRANSIENT ANALYSIS *1

0****   TRANSIENT ANALYSIS   TEMPERATURE = 27.000 DEG C

0***

0LEGEND:

 *: V(7)
 +: V(6)
 X

     TIME   V(7)

X(*+)------------ 0.   d+00   1.250d+00   2.500d+00   3.750d+00 5.000d+00

```
0.    d+00   2.500d+00 .                                    X
5.000d-10   2.500d+00 .                                     X
1.000d-09   2.500d+00 .                                     X
1.500d-09   2.500d+00 .                                     X
2.000d-09   2.500d+00 .                                     X
2.500d-09   2.500d+00 .                                     X
3.000d-09   2.500d+00 .                                     X
3.500d-09   2.500d+00 .                                     X
4.000d-09   2.500d+00 .                                     X
4.500d-09   2.529d+00 .                                     X
5.000d-09   2.621d+00 .                                      .X
5.500d-09   2.711d+00 .                                       .X
6.000d-09   2.799d+00 .                                        X
6.500d-09   2.885d+00 .                                         X
7.000d-09   2.912d+00 .                                    .     X
7.500d-09   2.912d+00 .                                          X
8.000d-09   2.912d+00 .                                          X
8.500d-09   2.916d+00 .                                          X
9.000d-09   2.919d+00 .                                          X
9.500d-09   2.927d+00 .                                          X
1.000d-08   2.939d+00 .                                          .
1.050d-08   2.954d+00 .                                          .
1.100d-08   2.985d+00 .                                           .
1.150d-08   3.021d+00 .                                           .
1.200d-08   3.067d+00 .                                            .
1.250d-08   3.118d+00 .                                             .
1.300d-08   3.171d+00 .                                              .
1.350d-08   3.224d+00 .                                               .
1.400d-08   3.276d+00 .                                                .
1.450d-08   3.328d+00 .                                                 .
1.500d-08   3.379d+00 .                                                  .
1.550d-08   3.429d+00 .                                                   .
1.600d-08   3.478d+00 .                                                   .
1.650d-08   3.523d+00 .                                                    .
1.700d-08   3.556d+00 .                                                    .
1.750d-00   3.568d+00 .                                                    .
1.800d-08   3.578d+00 .                                                    .
1.850d-08   3.542d+00 .                                                   .
1.900d-08   3.502d+00 .                                                  .
1.950d-08   3.445d+00 .                                                 .
2.000d-08   3.371d+00 .                                                .
2.050d-08   3.294d+00 .                                               .
2.100d-08   3.216d+00 .                                              .
2.150d-08   3.139d+00 .                                             .
2.200d-08   3.063d+00 .                                            .
2.250d-08   2.989d+00 .                                           .

2.300d-08   2.916d+00 .                                          .
2.350d-08   2.945d+00 .                                          .
2.400d-08   2.775d+00 .                                       X
2.450d-08   2.786d+00 .                                       .
2.500d-08   2.638d+00 .                                      .
2.550d-08   2.572d+00 .                                     .
2.600d-08   2.507d+00 .                                    .
2.650d-08   2.443d+00 .                                   .
2.700d-08   2.381d+00 .                                  .
2.750d-08   2.319d+00 .                                 .
2.800d-08   2.259d+00 .                                .
2.850d-08   2.200d+00 .                               .
2.900d-08   2.142d+00 .                              .
2.950d-08   2.085d+00 .                             .
3.000d-08   2.028d+00 .                            .
3.050d-08   1.973d+00 .                           .
3.100d-08   1.919d+00 .                          .
3.150d-08   1.866d+00 .                         .
3.200d-08   1.814d+00 .                        .
3.250d-08   1.763d+00 .                       .
3.300d-08   1.712d+00 .                      .
3.350d-08   1.663d+00 .                     .
3.400d-08   1.614d+00 .                    .
3.450d-08   1.567d+00 .                   .
3.500d-08   1.520d+00 .                  .
3.550d-08   1.474d+00 .                 .
3.600d-08   1.430d+00 .                .
3.650d-08   1.386d+00 .               .
3.700d-08   1.343d+00 .              .
3.750d-08   1.302d+00 .             .
3.800d-08   1.262d+00 .            .
3.850d-08   1.226d+00 .           .
3.900d-08   1.197d+00 .          .
3.950d-00   1.172d+00 .         .
4.000d-08   1.168d+00 .        .
```

Figure B-14.   SPICE Plot of Precharged B Register
               Output Using Basic transmission Gates.

```
 .WIDTH OUT=8Ø
 .OPTIONS ITL1=5ØØ ITL5=Ø
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
 +LEVEL=1
 VDD 1 Ø DC 5V
 M1  1  3  2  Ø NMOS L=5.ØU W=1Ø.ØU
 M2  1  3  5  Ø NMOS L=5.ØU W=1Ø.ØU
 M3  1  3  6  Ø NMOS L=5.ØU W=1Ø.ØU
 M4  1  3  7  Ø NMOS L=5.ØU W=1Ø.ØU
 M5  2  8  1  1 PMOS L=5.ØU W=2Ø.ØU
 M6  5  8  1  1 PMOS L=5.ØU W=2Ø.ØU
 M7  6  8  1  1 PMOS L=5.ØU W=2Ø.ØU
 M8  7  8  1  1 PMOS L=5.ØU W=2Ø.ØU
 M9  11 1Ø 9  Ø NMOS L=5.ØU W=5.ØU
 M1Ø 13 1Ø 12 Ø NMOS L=5.ØU W=5.ØU
 M11 15 1Ø 14 Ø NMOS L=5.ØU W=5.ØU
 M12 17 1Ø 16 Ø NMOS L=5.ØU W=5.ØU
 M13 9  18 11 1 PMOS L=5.ØU W=1Ø.ØU
 M14 12 18 13 1 FMOS L=5.ØU W=1Ø.ØU
 M15 14 18 15 1 FMOS L=5.ØU W=1Ø.ØU
 M16 16 18 17 1 FMOS L=5.ØU W=1Ø.ØU
 M17 Ø  2Ø 19 Ø NMOS L=5.ØU W=15.ØU
 M18 1  2Ø 19 1 PMOS L=5.ØU W=3Ø.ØU
 M19 22 9  1  1 PMOS L=5.ØU W=3Ø.ØU
 M2Ø 23 12 1  1 PMOS L=5.ØU W=3Ø.ØU
 M21 24 14 1  1 PMOS L=5.ØU W=3Ø.ØU
 M22 25 16 1  1 PMOS L=5.ØU W=3Ø.ØU
 M23 1  2G 13 1 PMOS L=5.ØU W=1Ø.ØU
 M24 Ø  9  22 Ø NMOS L=5.ØU W=15.ØU
 M25 Ø  12 23 Ø NMOS L=5.ØU W=15.ØU
 M2G Ø  14 24 Ø NMOS L=5.ØU W=15.ØU
 M27 Ø  16 25 Ø NMOS L=5.ØU W=15.ØU
 M2З 27 19 Ø  Ø NMOS L=5.ØU W=15.ØU
 M29 27 26 18 Ø NMOS L=5.ØU W=15.ØU
 M3Ø Ø  18 1Ø Ø NMOS L=5.ØU W=15.ØU
 M31 1  13 1Ø 1 PMOS L=5.ØU W=3Ø.ØU
 M32 1  19 13 1 PMOS L=5.ØU W=1Ø.ØU
 M33 22 28 2  Ø NMOS L=5.ØU W=5.ØU
 M34 23 28 5  Ø NMOS L=5.ØU W=5.ØU
 M35 24 28 6  Ø NMOS L=5.ØU W=5.ØU
 M36 25 28 7  Ø NMOS L=5.ØU W=5.ØU
 M37 1  19 29 1 PMOS L=5.ØU W=1Ø.ØU
 M3З 2  29 22 1 PMOS L=5.ØU W=1Ø.ØU
 M39 5  29 23 1 PMOS L=5.ØU W=1Ø.ØU
 M4Ø 6  29 24 1 PMOS L=5.ØU W=1Ø.ØU
 M41 7  29 25 1 PMOS L=5.ØU W=1Ø.ØU
 M42 31 3Ø Ø  Ø NMOS L=5.ØU W=15.ØU
 M43 31 19 29 Ø NMOS L=5.ØU W=15.ØU
 M44 Ø  29 23 Ø NMOS L=5.ØU W=15.ØU
 M45 1  29 23 1 PMOS L=5.ØU W=3Ø.ØU
 M46 1  3Ø 29 1 PMOS L=5.ØU W=1Ø.ØU
 C47 7 Ø Ø.94PF
```

```
C48 6 Ø Ø.94PF
C49 5 Ø Ø.94PF
C5Ø 2 Ø Ø.94PF
C51 1 Ø Ø.11Ø3PF
C52 Ø Ø Ø.5Ø5PF
C53 29 Ø Ø.181PF
C54 28 Ø Ø.128PF
C55 19 Ø Ø.23ØPF
C56 25 Ø Ø.135PF
C57 24 Ø Ø.139PF
C58 23 Ø Ø.145PF
C59 22 Ø Ø.151PF
C6Ø 18 Ø Ø.2Ø8PF
C61 1Ø Ø Ø.155PF
C62 16 Ø Ø.111PF
C63 14 Ø Ø.1Ø9PF
C64 12 Ø Ø.114PF
C65 9 Ø Ø.12ØPF
C66 17 Ø Ø.54PF
C67 15 Ø Ø.54PF
C68 13 Ø Ø.54PF
C69 11 Ø Ø.54PF
C7Ø 3 Ø Ø.5ØPF
VREGSEL 2Ø Ø PULSE (ØV ØV ØNS ØNS ØNS 3ØNS)
VIN1 26 Ø PULSE (ØV 5V 5NS ØNS ØNS 3ØNS)
VIN2 3Ø Ø PULSE (ØV 5V 5NS ØNS ØNS 3ØNS)
VDAT1 17 Ø PULSE (5V ØV 5NS ØNS ØNS 1ØNS)
VDAT2 15 Ø PULSE (ØV 5V 5NS ØNS ØNS 1ØNS)
VDAT3 13 Ø PULSE (ØV 5V 5NS ØNS ØNS 1ØNS)
VDAT4 11 Ø PULSE (5V ØV 5NS ØNS ØNS 1ØNS)
VP1 3 Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS)
VP1BAR 8 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
.TRAN Ø.5NS 4ØNS
.PLOT TRAN V(7) V(6) (ØV,5V)
.END
```

```
#        CMOS/SOS PRECHARGED B REGISTER TRANSIENT ANALYSIS - WIDTH TIMES TWO

#****    TRANSIENT ANALYSIS                TEMPERATURE =  27.### DEG C

#****************************************************************************

#LEGEND:

 *: V(7)
 +: V(6)
X
      TIME        V(7)
X(*+)------------- #.   d+##    1.25#d+##    2.5##d+##    3.75#d+## 5.###d+##
#.    d+##  2.5##d+##                        X
5.###d-1#  2.5##d+##                         X
1.###d-#9  2.5##d+##                         X
1.5##d-#9  2.5##d+##                         X
2.###d-#9  2.5##d+##                         X
2.5##d-#9  2.5##d+##                         X
3.###d-#9  2.5##d+##                         X
3.5##d-#9  2.5##d+##                         X
4.###d-#9  2.5##d+##                         X
4.5##d-#9  2.55#d+##                        .X
5.###d-#9  2.739d+##                          X
5.5##d-#9  2.911d+##                           X
6.###d-#9  3.#74d+##                            X
6.5##d-#9  3.229d+##                             X
7.###d-#9  3.279d+##                              X
7.5##d-#9  3.279d+##                              X
8.###d-#9  3.279d+##                              X
8.5##d-#9  3.28#d+##                              X
9.###d-#9  3.263d+##                              X
9.5##d-#9  3.267d+##                              X
1.###d-#8  3.295d+##                            +
1.#5#d-#8  3.3#6d+##                            +
1.1##d-#8  3.332d+##                            +
1.15#d-#8  3.363d+##                            +
1.2##d-#8  3.4#3d+##                             +
1.25#d-#8  3.448d+##                             +
1.3##d-#8  3.494d+##                              +
1.35#d-#8  3.54#d+##                              +
1.4##d-#8  3.565d+##                               +
1.45#d-#8  3.63#d+##                               +
1.5##d-#8  3.674d+##                                +
1.55#d-#8  3.717d+##                                +
1.6##d-#8  3.759d+##                                 +
1.65#d-#8  3.797d+##                                  +
1.7##d-#8  3.822d+##                                  +
1.75#d-#8  3.836d+##                                  +
1.8##d-#8  3.822d+##                                  +
1.85#d-#8  3.793d+##                                  +
1.9##d-#8  3.749d+##                                 +
1.95#d-#8  3.662d+##                                +
2.###d-#8  3.6#7d+##                               +
2.#5#d-#8  3.525d+##                              +
2.1##d-#8  3.442d+##                             +
2.15#d-#8  3.361d+##                            +
2.2##d-#8  3.281d+##                           +
2.25#d-#8  3.2#2d+##                          +
2.3##d-#8  3.125d+##                         +
2.35#d-#8  3.#49d+##                        +
2.4##d-#8  2.975d+##                        :
2.45#d-#8  2.9#2d+##                       :
2.5##d-#8  2.831d+##                      :
2.55#d-#8  2.761d+##                     :
2.6##d-#8  2.692d+##                    :
2.65#d-#8  2.625d+##                   :
2.7##d-#8  2.559d+##                  :
2.75#d-#8  2.494d+##                 :
2.8##d-#8  2.431d+##               +
2.85#d-#8  2.369d+##              +
2.9##d-#8  2.3#7d+##             +
2.95#d-#8  2.247d+##            +
3.###d-#8  2.188d+##           +
3.#5#d-#8  2.13#d+##          +
3.1##d-#8  2.#73d+##         +
3.15#d-#8  2.#17d+##        +
3.2##d-#8  1.963d+##       +
3.25#d-#8  1.9#9d+##      +
3.3##d-#8  1.856d+##     +
3.35#d-#8  1.8#4d+##     +
3.4##d-#8  1.753d+##    +
3.45#d-#8  1.7#2d+##   +
3.5##d-#8  1.653d+##   +
3.55#d-#8  1.6#5d+##  +
3.6##d-#8  1.557d+##  +
3.65#d-#8  1.511d+## +
3.7##d-#8  1.466d+## +
3.75#d-#8  1.422d+## +
3.8##d-#8  1.379d+##+
3.85#d-#8  1.341d+##+
3.9##d-#8  1.31#d+##+
3.95#d-#8  1.284d+##+
4.###d-#8  1.271d+##+
```

Figure B-15.   SPICE Plot of Precharged B Register Output
                Using Transmission Gate Widths Twice the
                Basic Widths.

```
.WIDTH OUT=80
.OPTIONS ITL1=500 ITL5=0
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
+LEVEL=1
VDD 1 0 DC 5V
M1  1  3  2  0 NMOS L=5.0U W=15.0U
M2  1  3  5  0 NMOS L=5.0U W=15.0U
M3  1  3  6  0 NMOS L=5.0U W=15.0U
M4  1  3  7  0 NMOS L=5.0U W=15.0U
M5  2  8  1  1 PMOS L=5.0U W=30.0U
M6  5  8  1  1 PMOS L=5.0U W=30.0U
M7  6  8  1  1 PMOS L=5.0U W=30.0U
M8  7  8  1  1 PMOS L=5.0U W=30.0U
M9  11 10 9  0 NMOS L=5.0U W=5.0U
M10 13 10 12 0 NMOS L=5.0U W=5.0U
M11 15 10 14 0 NMOS L=5.0U W=5.0U
M12 17 10 16 0 NMOS L=5.0U W=5.0U
M13 9  18 11 1 PMOS L=5.0U W=10.0U
M14 12 18 13 1 FMOS L=5.0U W=10.0U
M15 14 18 15 1 FMOS L=5.0U W=10.0U
M16 16 18 17 1 FMOS L=5.0U W=10.0U
M17 0  20 19 0 NMOS L=5.0U W=15.0U
M18 1  20 19 1 PMOS L=5.0U W=30.0U
M19 22 9  1  1 PMOS L=5.0U W=30.0U
M20 23 12 1  1 PMOS L=5.0U W=30.0U
M21 24 14 1  1 PMOS L=5.0U W=30.0U
M22 25 16 1  1 PMOS L=5.0U W=30.0U
M23 1  26 13 1 PMOS L=5.0U W=10.0U
M24 0  9  22 0 NMOS L=5.0U W=15.0U
M25 0  12 23 0 NMOS L=5.0U W=15.0U
M26 0  14 24 0 NMOS L=5.0U W=15.0U
M27 0  16 25 0 NMOS L=5.0U W=15.0U
M28 27 19 0  0 NMOS L=5.0U W=15.0U
M29 27 26 18 0 NMOS L=5.0U W=15.0U
M30 0  18 19 0 NMOS L=5.0U W=15.0U
M31 1  18 10 1 PMOS L=5.0U W=30.0U
M32 1  19 13 1 PMOS L=5.0U W=10.0U
M33 22 28 2  0 NMOS L=5.0U W=5.0U
M34 23 28 5  0 NMOS L=5.0U W=5.0U
M35 24 28 6  0 NMOS L=5.0U W=5.0U
M36 25 28 7  0 NMOS L=5.0U W=5.0U
M37 1  19 29 1 PMOS L=5.0U W=10.0U
M38 2  29 22 1 PMOS L=5.0U W=10.0U
M39 5  29 23 1 PMOS L=5.0U W=10.0U
M40 6  29 24 1 PMOS L=5.0U W=10.0U
M41 7  29 25 1 PMOS L=5.0U W=10.0U
M42 31 30 0  0 NMOS L=5.0U W=15.0U
M43 31 19 29 0 NMOS L=5.0U W=15.0U
M44 0  29 23 0 NMOS L=5.0U W=15.0U
M45 1  29 23 1 PMOS L=5.0U W=30.0U
M46 1  30 29 1 PMOS L=5.0U W=10.0U
C47 7  0  0.34PF
```

```
C43 6 0 0.94PF
C49 5 0 0.94PF
C50 2 0 0.94PF
C51 1 0 0.1103PF
C52 0 0 0.505PF
C53 29 0 0.181PF
C54 23 0 0.128PF
C55 19 0 0.230PF
C56 25 0 0.135PF
C57 24 0 0.139PF
C58 23 0 0.145PF
C59 22 0 0.151PF
C60 18 0 0.208PF
C61 10 0 0.155PF
C62 16 0 0.111PF
C63 14 0 0.109PF
C64 12 0 0.114PF
C65 9 0 0.120PF
C66 17 0 0.54PF
C67 15 0 0.54PF
C68 13 0 0.54PF
C69 11 0 0.54PF
C70 3 0 0.50PF
VREGSEL 20 0 PULSE (0V 0V 0NS 0NS 0NS 30NS)
VIN1 26 0 PULSE (0V 5V 5NS 0NS 0NS 30NS)
VIN2 30 0 PULSE (0V 5V 5NS 0NS 0NS 30NS)
VDAT1 17 0 PULSE (5V 0V 5NS 0NS 0NS 10NS)
VDAT2 15 0 PULSE (0V 5V 5NS 0NS 0NS 10NS)
VDAT3 13 0 PULSE (0V 5V 5NS 0NS 0NS 10NS)
VDAT4 11 0 PULSE (5V 0V 5NS 0NS 0NS 10NS)
VP1 3 0 PULSE (0V 5V 4NS 0NS 0NS 2NS)
VP1BAR 8 0 PULSE (5V 0V 4NS 0NS 0NS 2NS)
.TRAN 0.5NS 40NS
.PLOT TRAN V(7) V(6) (0V,5V)
.END
```

```
#LEGEND:

 *: V(7)
 +: V(6)
X
     TIME       V(7)

X(*+)------------ #.    d+##    1.25#d+##    2.5##d+##    3.75#d+## 5.###d+##
     #.    d+##  2.5##d+##  .                           X
     5.###d-1#   2.5##d+##  .                           X
     1.###d-#9   2.5##d+##  .                           X
     1.5##d-#9   2.5##d+##  .                           X
     2.###d-#9   2.5##d+##  .                           X
     2.5##d-#9   2.5##d+##  .                           X
     3.###d-#9   2.5##d+##  .                           X
     3.5##d-#9   2.5##d+##  .                           X
     4.###d-#9   2.5##d+##  .                          X
     4.5##d-#9   2.567d+##  .                         .X
     5.###d-#9   2.853d+##  .                              X
     5.5##d-#9   3.#99d+##  .                                  X
     6.###d-#9   3.325d+##  .                                    X
     6.5##d-#9   3.532d+##  .                                       X
     7.###d-#9   3.598d+##  .                                       X
     7.5##d-#9   3.598d+##  .                                       X
     8.###d-#9   3.597d+##  .                                       X
     8.5##d-#9   3.597d+##  .                                       X
     9.###d-#9   3.596d+##  .                                       X
     9.5##d-#9   3.596d+##  .                                       X
     1.###d-#8   3.6##d+##  .                                      .
     1.#5#d-#8   3.6#7d+##  .                                      .
     1.1##d-#8   3.627d+##  .                                       .
     1.15#d-#8   3.654d+##  .                                        .
     1.2##d-#8   3.688d+##  .                                         .
     1.25#d-#8   3.727d+##  .                                          .
     1.3##d-#8   3.766d+##  .                                           .
     1.35#d-#8   3.8#6d+##  .                                            .
     1.4##d-#8   3.845d+##  .                                             .
     1.45#d-#8   3.883d+##  .                                              .
     1.5##d-#8   3.92#d+##  .                                              .
     1.55#d-#8   3.957d+##  .                                               .
     1.6##d-#8   3.992d+##  .                                               .
     1.65#d-#8   4.#24d+##  .                                                .
     1.7##d-#8   4.#47d+##  .                                                .
     1.75#d-#8   4.#48d+##  .                                                .
     1.8##d-#8   4.#38d+##  .                                                .
     1.85#d-#8   4.##2d+##  .                                                .
     1.9##d-#8   3.95#d+##  .                                               .
     1.95#d-#8   3.886d+##  .                                              .
     2.###d-#8   3.8#3d+##  .                                             .
     2.#5#d-#8   3.717d+##  .                                            .
     2.1##d-#8   3.63#d+##  .                                           .
     2.15#d-#8   3.545d+##  .                                          .
     2.2##d-#8   3.461d+##  .                                         .
     2.25#d-#8   3.378d+##  .                                        .
     2.3##d-#8   3.298d+##  .                                       .
     2.35#d-#8   3.219d+##  .                                      .
     2.4##d-#8   3.141d+##  .                                     .
     2.45#d-#8   3.#65d+##  .                                    .
     2.5##d-#8   2.99#d+##  .                                   .
     2.55#d-#8   2.917d+##  .                                  .
     2.6##d-#8   2.846d+##  .                                 .
     2.65#d-#8   2.775d+##  .                                .
     2.7##d-#8   2.7#7d+##  .                               .
     2.75#d-#8   2.639d+##  .                              .
     2.8##d-#8   2.573d+##  .                             .
     2.85#d-#8   2.5#8d+##  .                            .
     2.9##d-#8   2.444d+##  .                           .
     2.95#d-#8   2.381d+##  .                          .
     3.###d-#8   2.32#d+##  .                         .
     3.#5#d-#8   2.259d+##  .                        .
     3.1##d-#8   2.2##d+##  .                       .
     3.15#d-#8   2.142d+##  .                      .
     3.2##d-#8   2.#85d+##  .                     .
     3.25#d-#8   2.#29d+##  .                    .
     3.3##d-#8   1.974d+##  .                   .
     3.35#d-#8   1.92#d+##  .                  .
     3.4##d-#8   1.867d+##  .                 .
     3.45#d-#8   1.815d+##  .                .
     3.5##d-#8   1.763d+##  .               .
     3.55#d-#8   1.713d+##  .              .
     3.6##d-#8   1.663d+##  .             .
     3.65#d-#8   1.615d+##  .            .
     3.7##d-#8   1.567d+##  .           .
     3.75#d-#8   1.521d+##  .          .
     3.8##d-#8   1.477d+##  .         .
     3.85#d-#8   1.437d+##  .        .
     3.9##d-#8   1.4#9d+##  .       .
     3.95#d-#8   1.377d+##  .      .
     4.###d-#8   1.364d+##  . . . . .
```

Figure B-16.   SPICE Plot of Precharged B Register
               Output Using Transmission gate Widths
               Three Times the Basic Widths.

B-42
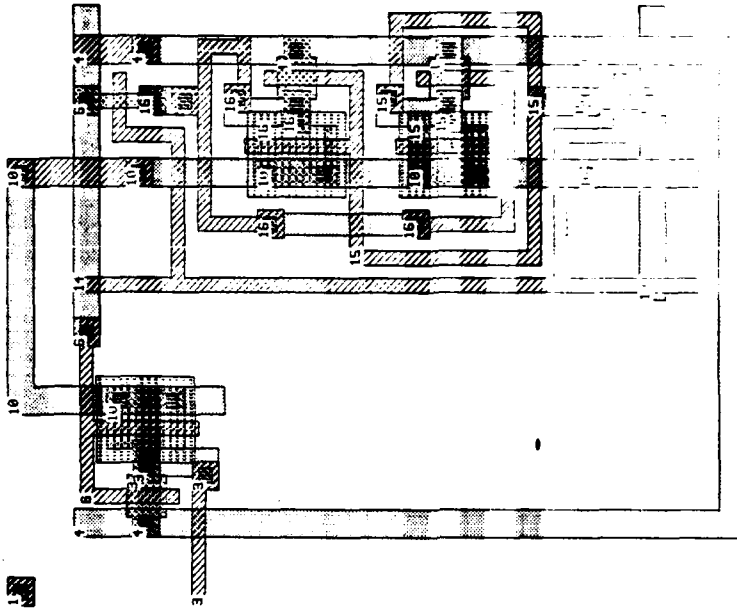
Figure B-17. Basic RAM Cell Node Plot.

Table B-6

BASIC RAM CELL NODE LIST

```
GND        Ø
Vcc        1
NMOS       Ø
PMOS       1
4          2
16         3
15         4
13         5
14         6
G          7
10         8
3          9
```

```
  .WIDTH OUT=8Ø
  .OPTIONS ITL1=5ØØ ITL5=Ø
  .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
  +LEVEL=1
  .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
  +LEVEL=1
  VDD 1 Ø DC 5V
  M1 4 3 Ø Ø NMOS L=5.ØU W=15.ØU
  M2 3 4 Ø Ø NMOS L=5.ØU W=15.ØU
  M3 4 6 5 Ø NMOS L=5.ØU W=5.ØU
  M4 7 6 3 Ø NMOS L=5.ØU W=5.ØU
  M5 1 3 4 1 PMOS L=5.ØU W=3Ø.ØU
  M6 1 4 3 1 PMOS L=5.ØU W=3Ø.ØU
  M7 9 7 1 1 PMOS L=5.ØU W=3Ø.ØU
  M8 Ø 7 9 Ø NMOS L=5.ØU W=15.ØU
  C9 9 Ø Ø.71PF
  C1Ø Ø Ø Ø.291PF
  C11 7 Ø Ø.92PF
  C12 1 Ø Ø.292PF
  C13 6 Ø Ø.1Ø8PF
  C14 4 Ø Ø.182PF
  C15 3 Ø Ø.185PF
  VIN1 7 Ø PULSE (ØV 5V 5NS ØNS ØNS 1ØNS)
  VIN2 5 Ø PULSE (5V ØV 5NS ØNS ØNS 5NS)
  VPASS 6 Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
  .TRAN Ø.5NS 4ØNS
  .PLOT TRAN V(9) (ØV,5V)
  .END
```

```
  .WIDTH OUT=8Ø
  .OPTIONS ITL1=5ØØ ITL5=Ø
  .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
  +LEVEL=1
  .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
  +LEVEL=1
  VDD 1 Ø DC 5V
  M1 4 3 Ø Ø NMOS L=5.ØU W=15.ØU
  M2 3 4 Ø Ø NMOS L=5.ØU W=15.ØU
  M3 4 6 5 Ø NMOS L=5.ØU W=5.ØU
  M4 7 6 3 Ø NMOS L=5.ØU W=5.ØU
  M5 1 3 4 1 PMOS L=5.ØU W=3Ø.ØU
  M6 1 4 3 1 PMOS L=5.ØU W=3Ø.ØU
  M7 9 7 1 1 PMOS L=5.ØU W=3Ø.ØU
  M8 Ø 7 9 Ø NMOS L=5.ØU W=15.ØU
  C9 9 Ø Ø.71PF
  C1Ø Ø Ø Ø.291PF
  C11 7 Ø Ø.92PF
  C12 1 Ø Ø.292PF
  C13 6 Ø Ø.1ØØPF
  C14 4 Ø Ø.182PF
  C15 3 Ø Ø.1Ø5PF
  VIN1 7 Ø PULSE (5V ØV 5NS ØNS ØNS 1ØNS)
  VIN2 5 Ø PULSE (5V ØV 5NS ØNS ØNS 5NS)
  VPASS 6 Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
  .TRAN Ø.5NS 4ØNS
  .PLOT TRAN V(9) (ØV,5V)
  .END
```

●   CMOS/SOS BASIC RAM CELL TRANSIENT ANALYSIS - #1# INPUT

●****   TRANSIENT ANALYSIS   TEMPERATURE = 27.### DEG C

●●●

X
    TIME   V(9)

X   #.   d+##   1.25#d+##   2.5##d+##   3.75#d+## 5.###d+##

TIME	V(9)
#. d+##	5.###d+##
5.###d-1#	5.###d+##
1.###d-#9	5.###d+##
1.5##d-#9	5.###d+##
2.###d-#9	5.###d+##
2.5##d-#9	5.###d+##
3.###d-#9	5.###d+##
3.5##d-#9	5.###d+##
4.###d-#9	5.###d+##
4.5##d-#9	5.###d+##
5.###d-#9	5.###d+##
5.5##d-#9	4.872d+##
6.###d-#9	4.44#d+##
6.5##d-#9	4.##9d+##
7.###d-#9	3.581d+##
7.5##d-#9	3.166d+##
8.###d-#9	2.76#d+##
8.5##d-#9	2.392d+##
9.###d-#9	2.#4#d+##
9.5##d-#9	1.732d+##
1.###d-#8	1.464d+##
1.#5#d-#8	1.213d+##
1.1##d-#8	1.##7d+##
1.15#d-#0	8.327d-#1
1.2##d-#8	6.86#d-#1
1.25#d-#8	5.649d-#1
1.3##d-#0	4.572d-#1
1.35#d-#8	3.757d-#1
1.4##d-#8	3.#34d-#1
1.45#d-#8	2.459d-#1
1.5##d-#8	2.###d-#1
1.55#d-#8	1.594d-#1
1.6##d-#8	2.758d-#1
1.65#d-#8	7.#62d-#1
1.7##d-#8	1.14#d+##
1.75#d-#8	1.563d+##
1.8##d-#8	1.979d+##
1.85#d-#8	2.367d+##
1.9##d-#8	2.738d+##
1.95#d-#8	3.#73d+##
2.###d-#0	3.368d+##
2.#5#d-#8	3.625d+##
2.1##d-#8	3.853d+##
2.15#d-#8	4.#56d+##
2.2##d-#8	4.216d+##
2.25#d-#8	4.359d+##
2.3##d-#8	4.476d+##
2.35#d-#8	4.571d+##
2.4##d-#8	4.654d+##
2.45#d-#8	4.717d+##
2.5##d-#8	4.771d+##
2.55#d-#8	4.817d+##
2.6##d-#8	4.85#d+##
2.65#d-#8	4.88#d+##
2.7##d-#8	4.9#3d+##
2.75#d-#8	4.921d+##
2.8##d-#8	4.937d+##
2.85#d-#8	4.949d+##
2.9##d-08	4.959d+##
2.95#d-#8	4.967d+##
3.###d-#8	4.973d+##
3.#5#d-#0	4.979d+##
3.1##d-#8	4.983d+##
3.15#d-#0	4.986d+##
3.2##d-#8	4.989d+##
3.25#d-#0	4.991d+##
3.3##d-#0	4.993d+##
3.35#d-#0	4.994d+##
3.4##d-#0	4.995d+##
3.45#d-#0	4.996d+##
3.5##d-#8	4.997d+##
3.55#d-#0	4.998d+##
3.6##d-#8	4.998d+##
3.65#d-#8	4.998d+##
3.7##d-#8	4.999d+##
3.75#d-#0	4.999d+##
3.0##d-#8	4.999d+##
3.85#d-#8	4.999d+##
3.9##d-#0	4.999d+##
3.95#d-08	5.###d+##
4.###d-08	5.###d+##

Figure B-18.   SPICE Plot of RAM Cell with Input 010.

CMOS/SOS BASIC RAM CELL TRANSIENT ANALYSIS - 101 INPUT

#····   TRANSIENT ANALYSIS   TEMPERATURE =   27.000 DEG C

#***

```
X
     TIME      V(9)

X                  0.      d+00     1.250d+00    2.500d+00     3.750d+00  5.000d+00
  0.    d+00   2.259d-08 *- - - - - - - - - - - - - - - - - - - - - - - - - - -
  5.000d-10   2.259d-08 *
  1.000d-09   2.259d-08 *
  1.500d-09   2.259d-08 *
  2.000d-09   2.259d-08 *
  2.500d-09   2.259d-08 *
  3.000d-09   2.259d-08 *
  3.500d-09   2.259d-08 *
  4.000d-09   2.259d-08 *
  4.500d-09   2.259d-08 *
  5.000d-09   2.259d-08 *
  5.500d-09   1.198d-01  .*
  6.000d-09   5.521d-01        .
  6.500d-09   9.845d-01             .
  7.000d-09   1.411d+00                 .
  7.500d-09   1.829d+00                    .
  8.000d-09   2.230d+00                       .
  8.500d-09   2.600d+00                          .
  9.000d-09   2.953d+00                             .
  9.500d-09   3.257d+00                               .
  1.000d-08   3.534d+00                                 .
  1.050d-08   3.763d+00                                   .
  1.100d-08   3.990d+00                                     .
  1.150d-08   4.164d+00                                      .
  1.200d-08   4.310d+00                                       .
  1.250d-08   4.423d+00                                        .
  1.300d-08   4.541d+00                                         .
  1.350d-08   4.623d+00                                          .
  1.400d-08   4.695d+00                                           .
  1.450d-08   4.753d+00                                           .
  1.500d-08   4.799d+00                                            .
  1.550d-08   4.840d+00                                            .
  1.600d-08   4.727d+00                                           .
  1.650d-08   4.295d+00                                         .
  1.700d-08   3.863d+00                                      .
  1.750d-08   3.440d+00                                    .
  1.600d-08   3.027d+00                                  .
  1.850d-08   2.623d+00                               .
  1.900d-08   2.263d+00                            .
  1.950d-08   1.922d+00                          .
  2.000d-08   1.638d+00                       .
  2.050d-08   1.373d+00                     .
  2.100d-08   1.150d+00                   .
  2.150d-08   9.473d-01               .
  2.200d-08   7.838d-01             .
  2.250d-08   6.443d-01           .
  2.300d-08   5.211d-01          .
  2.350d-08   4.297d-01         .
  2.400d-08   3.462d-01        .
  2.450d-08   2.816d-01       .
  2.500d-08   2.296d-01      .
  2.550d-08   1.841d-01     .
  2.600d-08   1.496d-01    .
  2.650d-08   1.209d-01   .
  2.700d-08   9.622d-02  .
  2.750d-08   7.863d-02  .
  2.800d-08   6.309d-02  .
  2.850d-08   5.063d-02  .
  2.900d-08   4.187d-02 *
  2.950d-08   3.275d-02 *
  3.000d-08   2.651d-02 *
  3.050d-08   2.136d-02 *
  3.100d-08   1.695d-02 *
  3.150d-08   1.363d-02 *
  3.200d-08   1.107d-02 *
  3.250d-08   8.875d-03 *
  3.300d-08   7.191d-03 *
  3.350d-08   5.729d-03 *
  3.400d-08   4.635d-03 *
  3.450d-08   3.722d-03 *
  3.500d-08   2.960d-03 *
  3.550d-08   2.414d-03 *
  3.600d-08   1.933d-03 *
  3.650d-08   1.549d-03 *
  3.700d-08   1.255d-03 *
  3.750d-08   9.994d-04 *
  3.800d-08   8.064d-04 *
  3.850d-08   6.500d-04 *
  3.900d-08   5.161d-04 *
  3.950d-08   4.210d-04 *
  4.000d-08   3.327d-04 *- - - - - - - - - - - - - - - - - - - - - - - - - - -
```

Figure B-19.   SPICE Plot of RAM Cell with Input 101.

Figure B-20.   Precharged RAM Cell Node Plot.

Table B-7

PRECHARGED RAM CELL NODE LIST

Gr	0
V.	1
..'S	0
PHOS	1
4	2
24	3
23	4
21	5
22	6
5	7
12	8
3	9
10	10
12	11

```
 .WIDTH OUT=8Ø
 .OPTIONS ITL1=5ØØ ITL5=Ø
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
 +LEVEL=1
 VDD  1  Ø DC 5V
 M1   4  3  Ø  Ø NMOS L=5.ØU W=15.ØU
 M2   3  4  Ø  Ø NMOS L=5.ØU W=15.ØU
 M3   4  6  5  Ø NMOS L=5.ØU W=5.ØU
 M4   7  6  3  Ø NMOS L=5.ØU W=5.ØU
 M5   1  3  4  1 PMOS L=5.ØU W=3Ø.ØU
 M6   1  4  3  1 PMOS L=5.ØU W=3Ø.ØU
 M7   1 1Ø  9  Ø NMOS L=5.ØU W=5.ØU
 M8   9  7  1  1 PMOS L=5.ØU W=3Ø.ØU
 M9   9 11  1  1 PMOS L=5.ØU W=1Ø.ØU
 M1Ø  Ø  7  9  Ø NMOS L=5.ØU W=15.ØU
 C11  9  Ø Ø.31PF
 C12  Ø  Ø Ø.243PF
 C13  7  Ø Ø.92PF
 C14  1  Ø Ø.389PF
 C15  6  Ø Ø.1Ø8PF
 C16  4  Ø Ø.182PF
 C17  3  Ø Ø.185PF
 VIN1  7  Ø PULSE (ØV 5V 5NS ØNS ØNS 1ØNS)
 VIN2  5  Ø PULSE (5V ØV 5NS ØNS ØNS 5NS)
 VPASS 6  Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
 VP1  1Ø  Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS)
 VP1BAR 11 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
 .TRAN Ø.5NS 4ØNS
 .PLOT TRAN V(9) (ØV,5V)
 .END
```

```
1*******11/28/84 ********  SPICE 2G.1 (15OCT8#)  *********13:49:45*****
#         CMOS/SOS PRECHARGED RAM CELL TRANSIENT ANALYSIS - #1# INPUT
                                                      M1
#****     TRANSIENT ANALYSIS                TEMPERATURE -  27.### DEG C
#*********************************************************************

X
     TIME       V(9)

X                      #.    d+##     1.25#d+##   2.5##d+##    3.75#d+## 5.###d+##
  #.   d+##   5.###d+##  .                  .          .          .          ....
  5.###d-1#   5.###d+##  .                  .          .          .          ....
  1.###d-#9   5.###d+##  .                  .          .          .          ....
  1.5##d-#9   5.###d+##  .                  .          .          .          ....
  2.###d-#9   5.###d+##  .                  .          .          .          ....
  2.5##d-#9   5.###d+##  .                  .          .          .          ....
  3.###d-#9   5.###d+##  .                  .          .          .          ....
  3.5##d-#9   5.###d+##  .                  .          .          .          ....
  4.###d-#9   5.###d+##  .                  .          .          .          ....
  4.5##d-#9   5.###d+##  .                  .          .          .          ....
  5.###d-#9   5.###d+##  .                  .          .          .          ....
  5.5##d-#9   4.893d+##  .                  .          .          .          . .
  6.###d-#9   4.533d+##  .                  .          .          .         .
  6.5##d-#9   4.189d+##  .                  .          .          .      .  .
  7.###d-#9   3.828d+##  .                  .          .          .    .
  7.5##d-#9   3.453d+##  .                  .          .          .  .
  8.###d-#9   3.#9#d+##  .                  .          .         .  .
  8.5##d-#9   2.744d+##  .                  .          .       .
  9.###d-#9   2.4#9d+##  .                  .          .     .
  9.5##d-#9   2.11#d+##  .                  .          .   .
  1.###d-#8   1.826d+##  .                  .       .  .
  1.#5#d-#8   1.569d+##  .                  .     . .
  1.1##d-#8   1.344d+##  .                  .   .
  1.15#d-#8   1.146d+##  .                  . .
  1.2##d-#8   9.758d-#1  .                .   .
  1.25#d-#8   8.263d-#1  .              . .
  1.3##d-#8   6.918d-#1  .            . .
  1.35#d-#8   5.848d-#1  .          .  .
  1.4##d-#8   4.868d-#1  .        .   .
  1.45#d-#8   4.#76d-#1  .       .    .
  1.5##d-#8   3.412d-#1  .     .      .
  1.65#d-#8   2.813d-#1  .   .        .
  1.6##d-#8   3.745d-#1  .  .         .
  1.65#d-#8   7.535d-#1  .    .       .
  1.7##d-#8   1.132d+##  .      .     .
  1.75#d-#8   1.5#5d+##  .        .   .
  1.8##d-#8   1.87#d+##  .         .  .
  1.#5#d-#8   2.224d+##  .           .  .
  1.9##d-#8   2.555d+##  .              .  .
  1.95#d-#8   2.865d+##  .                 .  .
  2.###d-#8   3.147d+##  .                    .  .
  2.#5#d-#8   3.4#3d+##  .                      .   .
  2.1##d-#8   3.626d+##  .                         .  .
  2.15#d-#8   3.828d+##  .                           .  .
  2.2##d-#8   4.#1#d+##  .                             .  .
  2.25#d-#8   4.158d+##  .                               .  .
  2.3##d-#8   4.293d+##  .                                .  .
  2.35#d-#8   4.4#6d+##  .                                 .  .
  2.4##d-#8   5.5#1d+##  .                                  .  .
  2.45#d-#8   4.586d+##  .                                   .  .
  2.5##d-#8   4.653d+##  .                                    .  .
  2.55#d-#8   4.711d+##  .                                     .  .
  2.6##d-#8   4.761d+##  .                                      . .
  2.65#d-#8   4.8##d+##  .                                       . .
  2.7##d-#8   4.835d+##  .                                       .  .
  2.75#d-#8   4.863d+##  .                                        .  .
  2.8##d-#8   4.886d+##  .                                        .  .
  2.85#d-#8   4.9#6d+##  .                                         . .
  2.9##d-#8   4.922d+##  .                                         .  .
  2.95#d-##   4.935d+##  .                                         .  .
  3.###d-##   4.947d+##  .                                          . .
  3.#5#d-##   4.956d+##  .                                          .  .
  3.1##d-##   4.963d+##  .                                          .  .
  3.15#d-#8   4.97#d+##  .                                          .   .
  3.2##d-#8   4.975d+##  .                                          .   .
  3.25#d-#8   4.979d+##  .                                          .   .
  3.3##d-#8   4.983d+##  .                                          .   .
  3.35#d-#8   4.986d+##  .                                          .   .
  3.4##d-#8   4.988d+##  .                                          .   .
  3.45#d-##   4.99#d+##  .                                          .    .
  3.5##d-#8   4.992d+##  .                                          .    .
  3.55#d-#8   4.993d+##  .                                          .    .
  3.6##d-##   4.995d+##  .                                          .    .
  3.65#d-##   4.996d+##  .                                          .    .
  3.7##d-##   4.996d+##  .                                          .    .
  3.75#d-#8   4.997d+##  .                                          .    .
  3.8##d-#8   4.997d+##  .                                          .    .
  3.#5#d-#8   4.998d+##  .                                          .    .
  3.9##d-#8   4.998d+##  .                                          .    .
  3.95#d-#8   4.999d+##  .                                          .    .
  4.###d-#8   4.999d+##  .                                          .    .
```

Figure B-21.   SPICE Plot of Precharged RAM Output
               Using Basic Transmission Gate Widths
               and Input 010.

B-49

```
.WIDTH OUT=80
.OPTIONS ITL1=500 ITL5=0
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
+LEVEL=1
VDD I Ø DC 5V
M1  4  3  Ø  Ø NMOS L=5.ØU W=15.ØU
M2  3  4  Ø  Ø NMOS L=5.ØU W=15.ØU
M3  4  6  5  Ø NMOS L=5.ØU W=5.ØU
M4  7  6  3  Ø NMOS L=5.ØU W=5.ØU
M5  1  3  4  1 PMOS L=5.ØU W=3Ø.ØU
M6  1  4  3  1 PMOS L=5.ØU W=3Ø.ØU
M7  1 1Ø  9  Ø NMOS L=5.ØU W=5.ØU
M8  9  7  1  1 PMOS L=5.ØU W=3Ø.ØU
M9  9 11  1  1 PMOS L=5.ØU W=1Ø.ØU
M1Ø Ø  7  9  Ø NMOS L=5.ØU W=15.ØU
C11 9 Ø Ø.31PF
C12 Ø Ø Ø.243PF
C13 7 Ø Ø.92PF
C14 1 Ø Ø.389PF
C15 6 Ø Ø.1Ø8PF
C16 4 Ø Ø.132PF
C17 3 Ø Ø.185PF
VIN1 7 Ø PULSE (5V ØV 5NS ØNS ØNS 1ØNS)
VIN2 5 Ø PULSE (5V ØV 5NS ØNS ØNS 5NS)
VPASS 6 Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VP1 1Ø Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS)
VP1BAR 11 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
.TRAN Ø.5NS 4ØNS
.PLOT TRAN V(9) (ØV,5V)
.END
```

```
1********11/28/84 ********  SPICE 2G.1 (15OCT8#)  *********13:49:57*****
#        CMOS/SOS PRECHARGED RAM CELL TRANSIENT ANALYSIS - 1#1 INPUT
#****     TRANSIENT ANALYSIS                 TEMPERATURE -   27.### DEG C
#...........................................................................

X
    TIME      V(9)

X              #.   d+##      1.25#d+##      2.5##d+##      3.75#d+## 5.###d+##
             --------------------------------------------------------------
#.   d+##   4.51#d-#8  *
5.###d-1#   4.51#d-#8  *
1.###d-#9   4.51#d-#8  *
1.5##d-#9   4.51#d-#8  *
2.###d-#9   4.51#d-#8  *
2.5##d-#9   4.51#d-#8  *
3.###d-#9   4.51#d-#8  *
3.5##d-#9   4.51#d-#8  *
4.###d-#9   4.51#d-#8  *
4.5##d-#9   6.57#d-#2   *
5.###d-#9   2.656d-#1    *
5.5##d-#9   5.62#d-#1      *
6.###d-#9   1.111d+##         *
6.5##d-#9   1.63#d+##             *
7.###d-#9   2.#27d+##                *
7.5##d-#9   2.37#d+##                   *
8.###d-#9   2.689d+##                      *
8.5##d-#9   2.9#4d+##                         *
9.###d-#9   3.261d+##                            *
9.5##d-#9   3.495d+##                              *
1.###d-#8   3.72#d+##                                *
1.#5#d-#8   3.915d+##                                  *
1.1##d-#8   4.#6#d+##                                    *
1.15#d-#8   4.223d+##                                     *
1.2##d-#8   4.343d+##                                      *
1.25#d-#8   4.448d+##                                       *
1.3##d-#8   4.541d+##                                        *
1.35#d-#8   4.614d+##                                         *
1.4##d-#8   4.679d+##                                          *
1.45#d-#8   4.733d+##                                           *
1.5##d-#8   4.777d+##                                            *
1.55#d-#8   4.#17d+##                                           *
1.6##d-#8   4.72#d+##                                          *
1.65#d-#8   4.341d+##                                        *
1.7##d-#8   3.962d+##                                     *
1.75#d-#8   3.58#d+##                                  *
1.8##d-#8   3.22#d+##                               *
1.85#d-#8   2.#63d+##                            *
1.9##d-#8   2.525d+##                         *
1.95#d-#8   2.2#9d+##                       *
2.###d-#8   1.921d+##                     *
2.#5#d-#8   1.657d+##                   *
2.1##d-#8   1.429d+##                 *
2.15#d-#8   1.219d+##               *
2.2##d-#8   1.#32d+##             *
2.25#d-#8   8.78#d-#1           *
2.3##d-#8   7.373d-#1          *
2.35#d-#8   6.2#5d-#1        *
2.4##d-#8   5.213d-#1       *
2.45#d-#8   4.324d-#1      *
2.5##d-#8   3.636d-#1     *
2.55#d-#8   3.#25d-#1     *
2.6##d-#8   2.5#5d-#1    *
2.65#d-#8   2.#96d-#1    *
2.7##d-#8   1.731d-#1   *
2.75#d-#8   1.439d-#1   *
2.8##d-#8   1.196d-#1   *
2.85#d-#8   9.#15d-#2   *
2.9##d-#8   8.199d-#2  *
2.95#d-#8   6.777d-#2  *
3.###d-#8   5.579d-#2  *
3.#5#d-#8   4.6#5d-#2  *
3.1##d-#8   3.824d-#2  *
3.15#d-#8   3.169d-#2 *
3.2##d-#8   2.628d-#2 *
3.25#d-#8   2.152d-#2 *
3.3##d-#8   1.795d-#2 *
3.35#d-#8   1.461d-#2 *
3.4##d-#8   1.218d-#2 *
3.45#d-#8   1.#14d-#2 *
3.5##d-#8   8.334d-#3 *
3.55#d-#8   6.9#2d-#3 *
3.6##d-#8   5.719d-#3 *
3.65#d-#8   4.681d-#3 *
3.7##d-#8   3.9#4d-#3 *
3.75#d-#8   3.22#d-#3 *
3.8##d-#8   2.647d-#3 *
3.85#d-#8   2.2#4d-#3 *
3.9##d-#8   1.811d-#3 *
3.95#d-#8   1.499d-#3 *
4.###d-#8   1.23#d-#3 *
```

Figure B-22.   SPICE Plot of Precharged RAM Cell
                Output Using Basic Transmission Gate
                and Input 101.

```
.WIDTH OUT=8Ø
.OPTIONS ITL1=5ØØ ITL5=Ø
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
+LEVEL=1
VDD 1 Ø DC 5V
M1 4 3 Ø Ø NMOS L=5.ØU W=15.ØU
M2 3 4 Ø Ø NMOS L=5.ØU W=15.ØU
M3 4 6 5 Ø NMOS L=5.ØU W=5.ØU
M4 7 6 3 Ø NMOS L=5.ØU W=5.ØU
M5 1 3 4 1 PMOS L=5.ØU W=3Ø.ØU
M6 1 4 3 1 PMOS L=5.ØU W=3Ø.ØU
M7 1 1Ø 9 Ø NMOS L=5.ØU W=1Ø.ØU
M8 9 7 1 1 PMOS L=5.ØU W=3Ø.ØU
M9 9 11 1 1 PMOS L=5.ØU W=2Ø.ØU
M1Ø Ø 7 9 Ø NMOS L=5.ØU W=15.ØU
C11 9 Ø Ø.81PF
C12 Ø Ø Ø.243PF
C13 7 Ø Ø.92PF
C14 1 Ø Ø.389PF
C15 6 Ø Ø.1Ø8PF
C16 4 Ø Ø.182PF
C17 3 Ø Ø.185PF
VIN1 7 Ø PULSE (ØV 5V 5NS ØNS ØNS 1ØNS)
VIN2 5 Ø PULSE (5V ØV 5NS ØNS ØNS 5NS)
VPASS 6 Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VP1 1Ø Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS)
VP1BAR 11 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
.TRAN Ø.5NS 4ØNS
.PLOT TRAN V(9) (ØV,5V)
.END
```

[********11/28/84 ******** SPICE 2G.1 (15OCT8#) ********12:44:46******

CMOS/SOS PRECHARGED RAM CELL TRANSIENT ANALYSIS - #1# INPUT - WIDTH X2

#***** TRANSIENT ANALYSIS TEMPERATURE = 27.### DEG C

#**

```
X
     TIME      V(9)
X               #.    d+##     1.25#d+##    2.5##d+##      3.75#d+## 5.###d+##
#.    d+##   5.###d+##
5.###d-1#   5.###d+##
1.###d-#9   5.###d+##
1.5##d-#9   5.###d+##
2.###d-#9   5.###d+##
2.5##d-#9   5.###d+##
3.###d-#9   5.###d+##
3.5##d-#9   5.###d+##
4.###d-#9   5.###d+##
4.5##d-#9   5.###d+##
5.###d-#9   5.###d+##
5.5##d-#9   4.894d+##
6.###d-#9   4.552d+##
6.5##d-#9   4.241d+##
7.###d-#9   3.896d+##
7.5##d-#9   3.52#d+##
8.###d-#9   3.154d+##
8.5##d-#9   2.8#4d+##
9.###d-#9   2.467d+##
9.5##d-#9   2.163d+##
1.###d-#8   1.874d+##
1.#5#d-#8   1.612d+##
1.1##d-#8   1.382d+##
1.15#d-#8   1.16#d+##
1.2##d-#8   1.##5d+##
1.25#d-#8   8.517d-#1
1.3##d-#8   7.125d-#1
1.35#d-#8   6.#34d-#1
1.4##d-#8   5.#37d-#1
1.45#d-#8   4.21#d-#1
1.5##d-#8   3.525d-#1
1.55#d-#8   2.9#7d-#1
1.6##d-#8   3.#32d-#1
1.65#d-#8   7.622d-#1
1.7##d-#8   1.141d+##
1.75#d-#8   1.513d+##
1.8##d-#8   1.878d+##
1.85#d-#8   2.232d+##
1.9##d-#8   2.563d+##
1.95#d-#8   2.872d+##
2.###d-#8   3.153d+##
2.#5#d-#8   3.4##d+##
2.1##d-#8   3.631d+##
2.15#d-#8   3.833d+##
2.2##d-#8   4.#14d+##
2.25#d-#8   4.162d+##
2.3##d-#8   4.296d+##
2.35#d-#8   4.4#9d+##
2.4##d-#8   4.5#3d+##
2.45#d-#8   4.588d+##

2.5##d-#8   4.654d+##
2.55#d-#8   4.712d+##
2.6##d-#8   4.762d+##
2.65#d-#8   4.8#1d+##
2.7##d-#8   4.835d+##
2.75#d-#8   4.863d+##
2.8##d-#8   4.886d+##
2.85#d-#8   4.9#7d+##
2.9##d-#8   4.922d+##
2.95#d-#8   4.936d+##
3.###d-#8   4.947d+##
3.#5#d-#8   4.956d+##
3.1##d-#8   4.964d+##
3.15#d-#8   4.97#d+##
3.2##d-#8   4.975d+##
3.25#d-#8   4.98#d+##
3.3##d-#8   4.983d+##
3.35#d-#8   4.986d+##
3.4##d-#8   4.988d+##
3.45#d-#8   4.99#d+##
3.5##d-#8   4.992d+##
3.55#d-#8   4.993d+##
3.6##d-#8   4.995d+##
3.65#d-#8   4.996d+##
3.7##d-#8   4.996d+##
3.75#d-#8   4.997d+##
3.8##d-#8   4.997d+##
3.85#d-#8   4.998d+##
3.9##d-#8   4.998d+##
3.95#d-#8   4.999d+##
4.###d-#8   4.999d+##
```

Figure B-23.   SPICE Plot of Precharged RAM Cell
                Output with Input 010 and Transmission
                Gate Widths Twice the Basic Widths.

B-53

```
.WIDTH OUT=8Ø
.OPTIONS ITL1=5ØØ ITL5=Ø
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
+LEVEL=1
VDD 1 Ø DC 5V
M1 4 3 Ø Ø NMOS L=5.ØU W=15.ØU
M2 3 4 Ø Ø NMOS L=5.ØU W=15.ØU
M3 4 6 5 Ø NMOS L=5.ØU W=5.ØU
M4 7 6 3 Ø NMOS L=5.ØU W=5.ØU
M5 1 3 4 1 PMOS L=5.ØU W=3Ø.ØU
M6 1 4 3 1 PMOS L=5.ØU W=3Ø.ØU
M7 1 1Ø 9 Ø NMOS L=5.ØU W=1Ø.ØU
M8 9 7 1 1 PMOS L=5.ØU W=3Ø.ØU
M9 9 11 1 1 PMOS L=5.ØU W=2Ø.ØU
M1Ø Ø 7 9 Ø NMOS L=5.ØU W=15.ØU
C11 9 Ø Ø.81PF
C12 Ø Ø Ø.243PF
C13 7 Ø Ø.92PF
C14 1 Ø Ø.389PF
C15 6 Ø Ø.1Ø8PF
C16 4 Ø Ø.182PF
C17 3 Ø Ø.185PF
VIN1 7 Ø PULSE (5V ØV 5NS ØNS ØNS 1ØNS)
VIN2 5 Ø PULSE (5V ØV 5NS ØNS ØNS 5NS)
VPASS 6 Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VP1 1Ø Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS)
VP1BAR 11 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
.TRAN Ø.5NS 4ØNS
.PLOT TRAN V(9) (ØV,5V)
.END
```

```
 8        CMOS/SOS PRECHARGED RAM CELL TRANSIENT ANALYSIS - 101 INPUT - WIDTH X2
                                                          x2
 8••••   TRANSIENT ANALYSIS              TEMPERATURE =  27.888 DEG C

 8•••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••

 X
     TIME       V(9)
 X            8.   d+88     1.258d+88     2.588d+88     3.758d+88  5.888d+88

   8.   d+88  4.518d-88 •
   5.888d-18  4.518d-88 •
   1.888d-89  4.518d-88 •
   1.588d-89  4.518d-88 •
   2.888d-89  4.518d-88 •
   2.588d-89  4.518d-88 •
   3.888d-89  4.518d-88 •
   3.588d-89  4.518d-88 •
   4.888d-89  4.518d-88 •
   4.588d-89  1.286d-81  •
   5.888d-89  4.994d-81  .        •
   5.588d-89  9.369d-81  .           •
   6.888d-89  1.683d+88  .               •
   6.588d-89  2.211d+88  .                  •
   7.888d-89  2.689d+88  .                     •
   7.588d-89  2.913d+88  .                       •
   8.888d-89  3.188d+88  .                         •
   8.588d-89  3.436d+88  .                          •
   9.888d-89  3.667d+88  .                            •
   9.588d-89  3.858d+88  .                             •
   1.888d-88  4.835d+88  .                              •
   1.858d-88  4.188d+88  .                               •
   1.188d-88  4.316d+88  .                                •
   1.158d-88  4.425d+88  .                                 •
   1.288d-88  4.516d+88  .                                  •
   1.258d-88  4.595d+88  .                                  •
   1.388d-88  4.664d+88  .                                   •
   1.358d-88  4.718d+88  .                                    •
   1.488d-88  4.767d+88  .                                    •
   1.458d-88  4.886d+88  .                                     •
   1.588d-88  4.839d+88  .                                     •
   1.558d-88  4.868d+88  .                                     •
   1.688d-88  4.767d+88  .                                    •
   1.658d-88  4.368d+88  .                                 •
   1.788d-88  4.889d+88  .                               •
   1.758d-88  3.634d+88  .                            •
   1.888d-88  3.265d+88  .                         •
   1.858d-86  2.986d+88  .                       •
   1.988d-88  2.566d+88  .                     •
   1.958d-88  2.247d+88  .                  •
   2.888d-88  1.956d+88  .                •
   2.858d-88  1.688d+88  .              •
   2.188d-88  1.456d+88  .            •
   2.158d-88  1.244d+88  .           •
   2.288d-08  1.854d+88  .          •
   2.258d-88  8.966d-81  .         •
   2.388d-88  7.532d-81  .        •
   2.358d-88  6.341d-81  .       •
   2.488d-88  5.329d-81  .      •
   2.458d-88  4.421d-81  .     •
   2.588d-88  3.718d-81  .    •
   2.558d-88  3.894d-81  .    •
   2.688d-88  2.563d-81  .   •
   2.658d-88  2. .45d-81  .   •
   2.788d-88  1.771d-81  .  •
   2.758d-88  1.472d-81  . •
   2.888d-88  1.224d-81  . •
   2.858d-88  1.885d-81  •
   2.988d-88  8.393d-82  •
   2.958d-88  6.937d-82  •
   3.888d-88  5.711d-82  •
   3.858d-88  4.768d-82  •
   3.188d-88  3.915d-82  •
   3.158d-88  3.246d-82  •
   3.288d-88  2.698d-82  •
   3.258d-88  2.283d-82  •
   3.388d-88  1.838d-82  •
   3.358d-88  1.517d-82  •
   3.488d-88  1.247d-82  •
   3.458d-88  1.838d-82  •
   3.588d-88  8.533d-83  •
   3.558d-88  7.867d-83  •
   3.688d-88  5.866d-83  •
   3.658d-88  4.793d-83  •
   3.788d-88  3.997d-83  •
   3.758d-88  3.297d-83  •
   3.888d-88  2.718d-83  •
   3.858d-88  2.257d-83  •
   3.988d-88  1.864d-83  •
   3.958d-88  1.525d-83  •
   4.888d-88  1.259d-83  •
```

Figure B-24.   SPICE Plot of Precharged RAM Cell
               with Input 101, and Transmission
               Gate Widths Twice the Basic Widths.

```
.WIDTH OUT=80
.OPTIONS ITL1=500 ITL5=0
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
+LEVEL=1
VDD 1 0 DC 5V
M1  4  3  0  0 NMOS L=5.0U W=15.0U
M2  3  4  0  0 NMOS L=5.0U W=15.0U
M3  4  6  5  0 NMOS L=5.0U W=5.0U
M4  7  6  3  0 NMOS L=5.0U W=5.0U
M5  1  3  4  1 PMOS L=5.0U W=30.0U
M6  1  4  3  1 PMOS L=5.0U W=30.0U
M7  1 10  9  0 NMOS L=5.0U W=15.0U
M8  9  7  1  1 PMOS L=5.0U W=30.0U
M9  9 11  1  1 PMOS L=5.0U W=30.0U
M10 0  7  9  0 NMOS L=5.0U W=15.0U
C11 9 0 0.81PF
C12 0 0 0.243PF
C13 7 0 0.92PF
C14 1 0 0.389PF
C15 6 0 0.108PF
C16 4 0 0.182PF
C17 3 0 0.185PF
VIN1 7 0 PULSE (0V 5V 5NS 0NS 0NS 10NS)
VIN2 5 0 PULSE (5V 0V 5NS 0NS 0NS 5NS)
VPASS 6 0 PULSE (0V 0V 0NS 0NS 0NS 10NS)
VP1 10 0 PULSE (0V 5V 4NS 0NS 0NS 2NS)
VP1BAR 11 0 PULSE (5V 0V 4NS 0NS 0NS 2NS)
.TRAN 0.5NS 40NS
.PLOT TRAN V(9) (0V,5V)
.END
```

```
1********11/28/84 ********   SPICE 2G.1 (15OCT8#)   ********12:44:57*****
#          CMOS/SOS PRECHARGED RAM CELL TRANSIENT ANALYSIS - #1# INPUT - WIDTH X3
                                                            X3
#****      TRANSIENT ANALYSIS                 TEMPERATURE -   27.### DEG C
#****************************************************************************
```

```
X
     TIME      V(9)
X               #.    d+##    1.25#d+##    2.5##d+##    3.75#d+##  5.###d+##
```

TIME	V(9)
#. d+##	5.###d+##
5.###d-1#	5.###d+##
1.###d-#9	5.###d+##
1.5##d-#9	5.###d+##
2.###d-#9	5.###d+##
2.5##d-#9	5.###d+##
3.###d-#9	5.###d+##
3.5##d-#9	5.###d+##
4.###d-#9	5.###d+##
4.5##d-#9	5.###d+##
5.###d-#9	5.###d+##
5.5##d-#9	4.896d+##
6.###d-#9	4.57#d+##
6.5##d-#9	4.2##d+##
7.###d-#9	3.957d+##
7.5##d-#9	3.58#d+##
8.###d-#9	3.213d+##
8.5##d-#9	2.86#d+##
9.###d-#9	2.519d+##
9.5##d-#9	2.212d+##
1.###d-#8	1.919d+##
1.#5#d-#8	1.652d+##
1.1##d-#8	1.418d+##
1.15#d-#8	1.211d+##
1.2##d-#8	1.#33d+##
1.25#d-#8	8.75#d-#1
1.3##d-#8	7.339d-#1
1.35#d-#8	6.2#9d-#1
1.4##d-#8	5.166d-#1
1.45#d-#8	4.335d-#1
1.5##d-#8	3.631d-#1
1.55#d-#8	2.995d-#1
1.6##d-#8	3.914d-#1
1.65#d-#8	7.7#4d-#1
1.7##d-#8	1.149d+##
1.75#d-#8	1.521d+##
1.8##d-#8	1.886d+##
1.85#d-#8	2.239d+##
1.9##d-#8	2.57#d+##
1.95#d-#8	2.878d+##
2.###d-#8	3.159d+##
2.#5#d-#8	3.413d+##
2.1##d-#8	3.636d+##
2.15#d-#8	3.837d+##
2.2##d-#8	4.#18d+##
2.25#d-#8	4.165d+##
2.3##d-#8	4.299d+##
2.35#d-#8	4.411d+##
2.4##d-#8	4.5#5d+##
2.45#d-#8	4.589d+##
2.5##d-#8	4.656d+##
2.55#d-#8	4.713d+##
2.6##d-#8	4.763d+##
2.65#d-#8	4.8#2d+##
2.7##d-#8	4.836d+##
2.75#d-#8	4.864d+##
2.8##d-#8	4.887d+##
2.85#d-##	4.9#7d+##
2.9##d-#8	4.922d+##
2.95#d-#8	4.936d+##
3.###d-#8	4.947d+##
3.#5#d-#8	4.956d+##
3.1##d-#8	4.964d+##
3.15#d-#8	4.97#d+##
3.2##d-#8	4.975d+##
3.25#d-#8	4.98#d+##
3.3##d-#8	4.983d+##
3.35#d-#8	4.986d+##
3.4##d-#8	4.989d+##
3.45#d-#8	4.99#d+##
3.5##d-#8	4.992d+##
3.55#d-#8	4.993d+##
3.6##d-#8	4.995d+##
3.65#d-#8	4.996d+##
3.7##d-#8	4.996d+##
3.75#d-#8	4.997d+##
3.8##d-#8	4.998d+##
3.85#d-#8	4.998d+##
3.9##d-#8	4.998d+##
3.95#d-#8	4.999d+##
4.###d-#8	4.999d+##

Figure B-25.   SPICE Plot of Precharged RAM Cell
               Output, with Input 010 and Transmission
               Gate Widths Tripled.

```
.WIDTH OUT=80
.OPTIONS ITL1=500 ITL5=0
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
+LEVEL=1
VDD 1 Ø DC 5V
M1  4 3 Ø Ø NMOS L=5.0U W=15.0U
M2  3 4 Ø Ø NMOS L=5.0U W=15.0U
M3  4 6 5 Ø NMOS L=5.0U W=5.0U
M4  7 6 3 Ø NMOS L=5.0U W=5.0U
M5  1 3 4 1 PMOS L=5.0U W=30.0U
M6  1 4 3 1 PMOS L=5.0U W=30.0U
M7  1 10 9 Ø NMOS L=5.0U W=15.0U
M8  9 7 1 1 PMOS L=5.0U W=30.0U
M9  9 11 1 1 PMOS L=5.0U W=30.0U
M10 Ø 7 9 Ø NMOS L=5.0U W=15. U
C11 9 Ø 0.81PF
C12 Ø Ø 0.243PF
C13 7 Ø 0.92PF
C14 1 Ø 0.389PF
C15 6 Ø 0.108PF
C16 4 Ø 0.182PF
C17 3 Ø 0.185PF
VIN1 7 Ø PULSE (5V ØV 5NS ØNS ØNS 10NS)
VIN2 5 Ø PULSE (5V ØV 5NS ØNS ØNS 5NS)
VPASS 6 Ø PULSE (ØV ØV ØNS ØNS ØNS 10NS)
VP1 10 Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS)
VP1BAR 11 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
.TRAN Ø.5NS 40NS
.PLOT TRAN V(9) (ØV,5V)
.END
```

```
1********11/20/84 ********  SPICE 2G.1 (15OCT8#)  ********12:51:#3*****
#       CMOS/SOS PRECHARGED RAM CELL TRANSIENT ANALYSIS - 1# 1INPUT - WIDTH X3
                                                          X3
#****    TRANSIENT ANALYSIS              TEMPERATURE =  27.### DEG C
#**********************************************************************

X
   TIME      V(9)
X            #.     d+##     1.25#d+##     2.5##d+##     3.75#d+##  5.###d+##
   #.   d+##  4.51#d-##  *
   5.###d-1#  4.51#d-##  *
   1.###d-#9  4.51#d-##  *
   1.5##d-#9  4.51#d-##  *
   2.###d-#9  4.51#d-##  *
   2.5##d-#9  4.51#d-##  *
   3.###d-#9  4.51#d-##  *
   3.5##d-#9  4.51#d-##  *
   4.###d-#9  4.51#d-##  *
   4.5##d-#9  1.###d-#1   .   *
   5.###d-#9  7.1#1d-#1       .    *
   5.5##d-#9  1.263d+##                 *
   6.###d-#9  2.#25d+##                        *
   6.5##d-#9  2.692d+##                            *
   7.###d-#9  3.###d+##                             .
   7.5##d-#9  3.342d+##                               .
   #.###d-#9  3.573d+##                                .
   #.5##d-#9  3.7##d+##                                 .
   9.###d-#9  3.96#d+##                                  .
   9.5##d-#9  4.122d+##                                   .
   1.###d-##  4.263d+##                                    .
   1.#5#d-##  4.3#3d+##                                     .
   1.1##d-##  4.4#3d+##                                      .
   1.15#d-##  4.566d+##                                       .
   1.2##d-##  4.626d+##                                        .
   1.25#d-##  4.696d+##                                        .
   1.3##d-##  4.749d+##                                         .
   1.35#d-##  4.79#d+##                                          .
   1.4##d-##  4.#26d+##                                          .
   1.45#d-##  4.#56d+##                                          .
   1.5##d-##  4.###d+##                                           .
   1.55#d-##  4.9#2d+##                                          .
   1.6##d-##  4.79#d+##                                          .
   1.65#d-##  4.419d+##                                         .
   1.7##d-##  4.#4#d+##                                       .
   1.75#d-##  3.665d+##                                     .
   1.###d-##  3.295d+##                                  .
   1.85#d-##  2.925d+##                               .
   1.9##d-##  2.593d+##                            .
   1.95#d-##  2.273d+##                          .
   2.###d-##  1.979d+##                        .
   2.#5#d-##  1.71#d+##                      .
   2.1##d-##  1.475d+##                    .
   2.15#d-##  1.26#d+##                  .
   2.2##d-##  1.#6#d+##                .
   2.25#d-##  9.#92d-#1              .
   2.3##d-##  7.642d-#1            .
   2.35#d-##  6.424d-#1          .
   2.4##d-##  5.4##d-#1         .
   2.45#d-##  4.469d-#1       .
   2.5##d-##  3.775d-#1      .
   2.55#d-##  3.142d-#1     .
   2.6##d-##  2.6#2d-#1    .
   2.65#d-##  2.17#d-#1    .
   2.7##d-##  1.799d-#1   .
   2.75#d-##  1.495d-#1   .
   2.###d-##  1.243d-#1  .
   2.85#d-##  1.#21d-#1  .
   2.9##d-##  8.526d-#2  *
   2.95#d-##  7.#4#d-#2  *
   3.###d-##  5.#92d-#2  *
   3.#5#d-##  4.836d-#2  *
   3.1##d-##  3.978d-#2  *
   3.15#d-##  3.297d-#2  *
   3.2##d-##  2.733d-#2  *
   3.25#d-##  2.269d-#2  *
   3.3##d-##  1.867d-#2  *
   3.35#d-##  1.541d-#2  *
   3.4##d-##  1.267d-#2  *
   3.45#d-##  1.#55d-#2  *
   3.5##d-##  8.67#d-#3  *
   3.55#d-##  7.1##d-#3  *
   3.6##d-##  5.95#d-#3  *
   3.65#d-##  4.#71d-#3  *
   3.7##d-##  4.#61d-#3  *
   3.75#d-##  3.35#d-#3  *
   3.8##d-##  2.754d-#3  *
   3.85#d-##  2.293d-#3  *
   3.9##d-##  1.8#4d-#3  *
   3.95#d-##  1.56#d-#3  *
   4.###d-##  1.279d-#3  *
```

Figure B-26.   SPICE Plot of Precharged RAM Cell with
               Input 101 and Transmission Gate Widths
               Tripled.

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Appendix C

This appendix contains SPICE simulation data on the three sections of the ALU bitslice circuit.

Each basic section was simulated first, then two different precharge configurations were simulated for each section. The first section was simulated with precharge of its two output lines and with precharge of four internal nodes. The second section was simulated with precharge of its single output node and with precharge of two internal nodes. The third section was simulated with precharge of its single output and with precharge of four internal nodes. For each precharge configuration, simulations were performed using basic transmission gates, transmission gates with twice the basic transmission gate widths and with transmission gate widths three times the basic widths.

For each circuit configuration, both 010 and 101 inputs were applied to the circuit inputs to permit evaluation of the low-to-high and high-to-low signal waveform transitions.
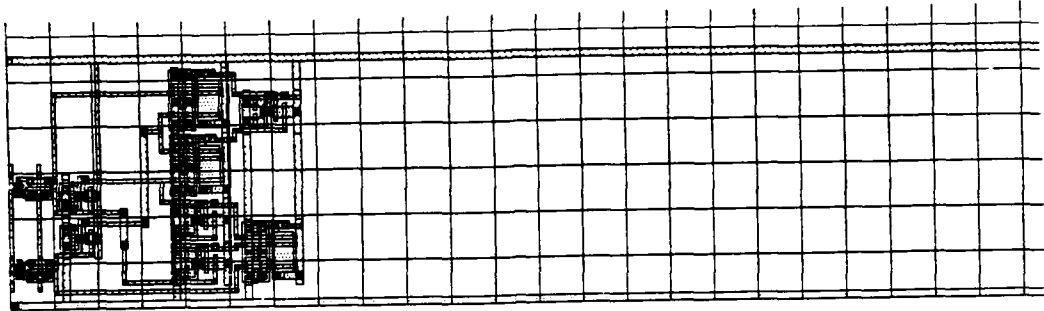
Figure C-1.   Basic Section 1 CLL Plot.
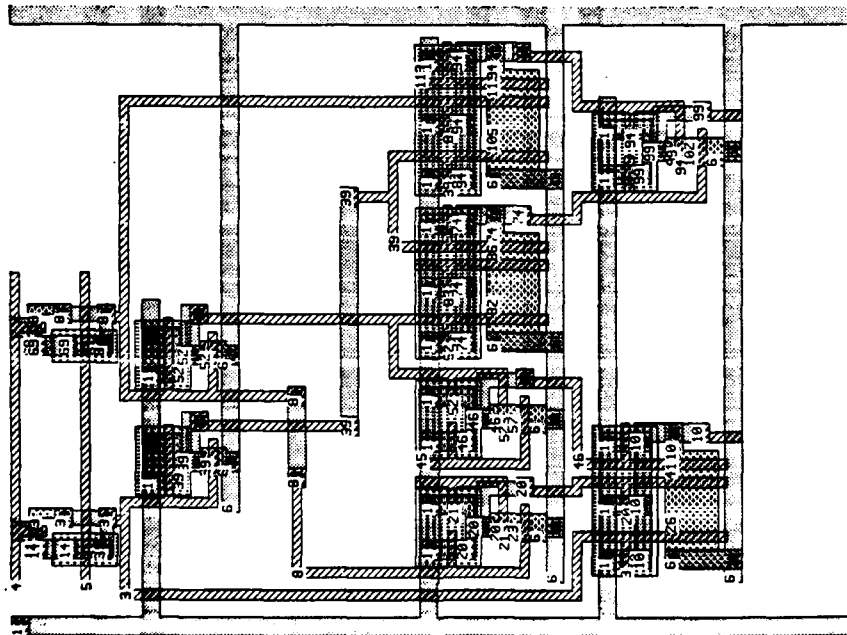
Figure C-2.   Basic Bitslice Section 1 Node Plot.

Table C-1

BASIC BITSLICE SECTION 1 NODE REFERENCE LIST

GND	0
Vdd	1
NMOS	0
PMOS	1
94	2
113	3
1	4
112	5
8	6
105	7
99	8
39	9
6	10
74	11
102	12
86	13
83	14
82	15
52	16
4	17
69	18
5	19
46	20
45	21
57	22
10	23
41	24
3	25
20	26
26	27
21	28
14	29
23	30

```
.WIDTH OUT=80
.OPTIONS ITL1=500 ITL5=0
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
+LEVEL=1
VDD 1 0 DC 5V
M1  1 3 2 1 PMOS L=5.0U W=10.0U
M2  5 3 2 0 NMOS L=5.0U W=30.0U
M3  7 6 5 0 NMOS L=5.0U W=30.0U
M4  1 6 2 1 PMOS L=5.0U W=10.0U
M5  1 2 8 1 PMOS L=5.0U W=10.0U
M6  0 9 7 0 NMOS L=5.0U W=30.0U
M7  12 11 0 0 NMOS L=5.0U W=15.0U
M8  12 2 8 0 NMOS L=5.0U W=15.0U
M9  1 11 8 1 PMOS L=5.0U W=10.0U
M10 1 9 2 1 PMOS L=5.0U W=10.0U
M11 1 9 11 1 PMOS L=5.0U W=10.0U
M12 13 9 11 0 NMOS L=5.0U W=30.0U
M13 15 14 13 0 NMOS L=5.0U W=30.0U
M14 1 14 11 1 PMOS L=5.0U W=10.0U
M15 0 16 15 0 NMOS L=5.0U W=30.0U
M16 18 17 6 0 NMOS L=5.0U W=5.0U
M17 1 16 11 1 PMOS L=5.0U W=10.0U
M18 18 19 6 1 PMOS L=5.0U W=10.0U
M19 0 6 16 0 NMOS L=5.0U W=15.0U
M20 1 6 16 1 PMOS L=5.0U W=30.0U
M21 1 16 20 1 PMOS L=5.0U W=10.0U
M22 22 21 0 0 NMOS L=5.0U W=15.0U
M23 22 16 20 0 NMOS L=5.0U W=15.0U
M24 1 20 23 1 PMOS L=5.0U W=10.0U
M25 1 21 20 1 PMOS L=5.0U W=10.0U
M26 24 20 23 0 NMOS L=5.0U W=30.0U
M27 0 25 9 0 NMOS L=5.0U W=15.0U
M28 27 26 24 0 NMOS L=5.0U W=30.0U
M29 1 25 9 1 PMOS L=5.0U W=30.0U
M30 1 26 23 1 PMOS L=5.0U W=10.0U
M31 1 28 26 1 PMOS L=5.0U W=10.0U
M32 29 17 25 0 NMOS L=5.0U W=5.0U
M33 0 25 27 0 NMOS L=5.0U W=30.0U
M34 30 6 0 0 NMOS L=5.0U W=15.0U
M35 30 28 26 0 NMOS L=5.0U W=15.0U
M36 1 6 26 1 PMOS L=5.0U W=10.0U
M37 29 19 25 1 PMOS L=5.0U W=10.0U
M38 1 25 23 1 PMOS L=5.0U W=10.0U
C39 1 0 0.1143PF
C40 25 0 0.207PF
C41 17 0 0.51PF
C42 0 0 0.1174PF
C43 6 0 0.297PF
C44 23 0 0.134PF
C45 26 0 0.111PF
C46 27 0 0.36PF
C47 9 0 0.202PF
```

```
C48 20 0 0.121PF
C49 16 0 0.151PF
C50 11 0 0.171PF
C51 15 0 0.36PF
C52 2 0 0.172PF
C53 8 0 0.134PF
C54 7 0 0.36PF
VA0 29 0 PULSE (0V 5V 0NS 0NS 0NS 10NS)
VB0 18 0 PULSE (0V 0V 0NS 0NS 0NS 10NS)
VPHI1 17 0 PULSE (5V 5V 0NS 0NS 0NS 10NS)
VPHI1BAR 19 0 PULSE (0V 0V 0NS 0NS 0NS 10NS)
VS0 28 0 PULSE (0V 0V 0NS 0NS 0NS 10NS)
VS1 21 0 PULSE (0V 0V 0NS 0NS 0NS 10NS)
VS2 3 0 PULSE (5V 5V 0NS 0NS 0NS 10NS)
VS3 14 0 PULSE (5V 5V 0NS 0NS 0NS 10NS)
.TRAN 0.5NS 40NS
.PLOT TRAN V(8) V(23) (0V,5V)
.END
```

```
1********12/#1/84 ********  SPICE 2G.1 (15OCT##)  *********##:19:16*****
#         CMOS/SOS BASIC SECTION 1 TRANSIENT ANALYSIS - OUTPUT 1#1
#****     TRANSIENT ANALYSIS                  TEMPERATURE = 27.### DEG C
#*********************************************************************

#LEGEND:

 *: V(8)
 +: V(23)
X
     TIME        V(8)

X(*+)------------ #.     d+##     1.25#d+##     2.5##d+##     3.75#d+##  5.###d+##
     #.   d+##  5.###d+##  .                :                :            X
     5.###d-1#  5.###d+##  .                :                :            X
     1.###d-#9  5.###d+##  .                :                :            X
     1.5##d-#9  5.###d+##  .                :                :            X
     2.###d-#9  5.###d+##  .                :                :            X
     2.5##d-#9  5.###d+##  .                :                :            X
     3.###d-#9  5.###d+##  .                :                :            X
     3.5##d-#9  5.###d+##  .                :                :          . X
     4.###d-#9  5.###d+##  .                :                :         .  +
     4.5##d-#9  5.###d+##  .                :                :        .  +
     5.###d-#9  5.###d+##  .                :                :       .  +
     5.5##d-#9  5.###d+##  .                :                :      .  +
     6.###d-#9  5.###d+##  .                :                :     .  +
     6.5##d-#9  5.###d+##  .                :                :   .  +
     7.###d-#9  4.968d+##  .                :           .    :  .  +
     7.5##d-#9  4.879d+##  .                :         +      :    . +
     8.###d-#9  4.658d+##  .               +     .           :      .
     8.5##d-#9  4.296d+##  .            .  +                  :    .
     9.###d-#9  3.796d+##  .          .     +                 :  .
     9.5##d-#9  3.184d+##  .        .           +             :.
     1.###d-#8  2.547d+##  .+     .               +         .
     1.#5#d-#8  1.897d+##  .+   .                     +   .
     1.1##d-#8  1.315d+##  .+  .                   .      +
     1.15#d-#8  8.644d-#1  .+ .                 .           +
     1.2##d-#8  5.343d-#1  .+.               .
     1.25#d-#8  3.257d-#1  .+.            .
     1.3##d-#8  1.88#d-#1  .X          .
     1.35#d-#8  1.151d-#1  .+X       .
     1.4##d-#8  6.#16d-#2  .+ X    .
     1.45#d-#8  3.269d-#2  *  X  .
     1.5##d-#8  1.9#4d-#2  *    .
     1.55#d-#8  1.126d-#2  *  .
     1.6##d-#8  1.246d-#2  * .
     1.65#d-#8  4.#28d-#2  *.
     1.7##d-#8  1.449d-#1  .+
     1.75#d-#8  3.#76d-#1  .+  .
     1.8##d-#8  6.727d-#1  .    +      .
     1.85#d-#8  1.116d+##  .       +          .
     1.9##d-#8  1.666d+##  .          X              .
     1.95#d-#8  2.262d+##  .             +    .
     2.###d-#8  2.842d+##  .                +      .
     2.#5#d-#8  3.354d+##  .                   +        .
     2.1##d-#8  3.754d+##  .                      +       .
     2.15#d-#8  4.#97d+##  .                        +        .
     2.2##d-#8  4.363d+##  .                         +          .
     2.25#d-#8  4.544d+##  .                          +            .

     2.3##d-#8  4.69#d+##  .                :          :+            .
     2.35#d-#8  4.764d+##  .                :          :  +            .
     2.4##d-#8  4.851d+##  .                :          :    +           .
     2.45#d-#8  4.9#3d+##  .                :          :      +          .
     2.5##d-#8  4.931d+##  .                :          :        +        .
     2.55#d-#8  4.954d+##  .                :          :          +       .
     2.6##d-#8  4.969d+##  .                :          :           +      .
     2.65#d-#8  4.979d+##  .                :          :            +      .
     2.7##d-08  4.986d+##  .                :          :             +     .
     2.75#d-#8  4.99#d+##  .                :          :              +    .
     2.8##d-#8  4.993d+##  .                :          :               +   .
     2.85#d-#8  4.996d+##  .                :          :                +  .
     2.9##d-#8  4.997d+##  .                :          :                 + .
     2.95#d-#8  4.998d+##  .                :          :                 + .
     3.###d-#8  4.999d+##  .                :          :                  +.
     3.#5#d-#8  4.999d+##  .                :          :                  +.
     3.1##d-08  4.999d+##  .                :          :                  +.
     3.15#d-#8  5.###d+##  .                :          :                  +.
     3.2##d-00  5.###d+##  .                :          :                  +.
     3.25#d-#8  5.###d+##  .                :          :                  +.
     3.3##d-#8  5.###d+##  .                :          :                  +.
     3.35#d-#8  5.###d+##  .                :          :                  +.
     3.4##d-#0  5.###d+##  .                :          :                  +.
     3.45#d-#8  5.###d+##  .                :          :                  +.
     3.5##d-#8  5.###d+##  .                :          :                  +.
     3.55#d-#8  5.###d+##  .                :          :                  +.
     3.6##d-#8  5.###d+##  .                :          :                  +.
     3.65#d-#8  5.###d+##  .                :          :                  +.
     3.7##d-#8  5.###d+##  .                :          :                  +.
     3.75#d-#0  5.###d+##  .                :          :                  +.
     3.8##d-#8  5.###d+##  .                :          :                  +.
     3.85#d-#8  5.###d+##  .                :          :                  +.
     3.9##d-#8  5.###d+##  .                :          :                  +.
     3.95#d-#8  5.###d+##  .                :          :                  +.
     4.###d-#8  5.###d+##  .  .  .  .  .  . : .  .  .  : .  .  .  .  .  . +.
```

Figure C-3.   SPICE Plot Basic Section 1 Input 010.

C-6

```
 .WIDTH OUT=8Ø
 .OPTIONS ITL1=5ØØ ITL5=Ø
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
 +LEVEL=1
 VDD 1 Ø DC 5V
 M1  1  3  2  1 PMOS L=5.ØU W=1Ø.ØU
 M2  5  3  2  Ø NMOS L=5.ØU W=3Ø.ØU
 M3  7  6  5  Ø NMOS L=5.ØU W=3Ø.ØU
 M4  1  6  2  1 PMOS L=5.ØU W=1Ø.ØU
 M5  1  2  8  1 PMOS L=5.ØU W=1Ø.ØU
 M6  Ø  9  7  Ø NMOS L=5.ØU W=3Ø.ØU
 M7  12 11 Ø  Ø NMOS L=5.ØU W=15.ØU
 M8  12 2  8  Ø NMOS L=5.ØU W=15.ØU
 M9  1  11 8  1 PMOS L=5.ØU W=1Ø.ØU
 M1Ø 1  9  2  1 PMOS L=5.ØU W=1Ø.ØU
 M11 1  9  11 1 PMOS L=5.ØU W=1Ø.ØU
 M12 13 9  11 Ø NMOS L=5.ØU W=3Ø.ØU
 M13 15 14 13 Ø NMOS L=5.ØU W=3Ø.ØU
 M14 1  14 11 1 PMOS L=5.ØU W=1Ø.ØU
 M15 Ø  16 15 Ø NMOS L=5.ØU W=3Ø.ØU
 M16 18 17 6  Ø NMOS L=5.ØU W=5.ØU
 M17 1  16 11 1 PMOS L=5.ØU W=1Ø.ØU
 M18 18 19 6  1 PMOS L=5.ØU W=1Ø.ØU
 M19 Ø  6  16 Ø NMOS L=5.ØU W=15.ØU
 M2Ø 1  6  16 1 PMOS L=5.ØU W=3Ø.ØU
 M21 1  16 2Ø 1 PMOS L=5.ØU W=1Ø.ØU
 M22 22 21 Ø  Ø NMOS L=5.ØU W=15.ØU
 M23 22 16 2Ø Ø NMOS L=5.ØU W=15.ØU
 M24 1  2Ø 23 1 PMOS L=5.ØU W=1Ø.ØU
 M25 1  21 2Ø 1 PMOS L=5.ØU W=1Ø.ØU
 M26 24 2Ø 23 Ø NMOS L=5.ØU W=3Ø.ØU
 M27 Ø  25 9  Ø NMOS L=5.ØU W=15.ØU
 M28 27 26 24 Ø NMOS L=5.ØU W=3Ø.ØU
 M29 1  25 9  1 PMOS L=5.ØU W=3Ø.ØU
 M3Ø 1  26 23 1 PMOS L=5.ØU W=1Ø.ØU
 M31 1  23 26 1 PMOS L=5.ØU W=1Ø.ØU
 M32 29 17 25 Ø NMOS L=5.ØU W=5.ØU
 M33 Ø  25 27 Ø NMOS L=5.ØU W=3Ø.ØU
 M34 3Ø 6  Ø  Ø NMOS L=5.ØU W=15.ØU
 M35 3Ø 23 26 Ø NMOS L=5.ØU W=15.ØU
 M36 1  6  26 1 PMOS L=5.ØU W=1Ø.ØU
 M37 29 19 25 1 FMOS L=5.ØU W=1Ø.ØU
 M38 1  25 23 1 PMOS L=5.ØU W=1Ø.ØU
 C39 1  Ø  Ø.1143PF
 C4Ø 25 Ø  Ø.2Ø7PF
 C41 17 Ø  Ø.51PF
 C42 Ø  Ø  Ø.1174PF
 C43 6  Ø  Ø.297PF
 C44 23 Ø  Ø.134PF
 C45 26 Ø  Ø.111PF
 C46 27 Ø  Ø.86PF
```

```
C47 9 0 0.202PF
C48 20 0 0.121PF
C49 16 0 0.151PF
C50 11 0 0.171PF
C51 15 0 0.3GPF
C52 2 0 0.172PF
C53 8 0 0.134PF
C54 7 0 0.36PF
VA0 29 0 PULSE (5V 0V 0NS 0NS 0NS 10NS)
VB0 18 0 PULSE (0V 0V 0NS 0NS 0NS 10NS)
VPHI1 17 0 PULSE (5V 5V 0NS 0NS 0NS 10NS)
VPHI1BAR 19 0 PULSE (0V 0V 0NS 0NS 0NS 10NS)
VS0 28 0 PULSE (0V 0V 0NS 0NS 0NS 10NS)
VS1 21 0 PULSE (0V 0V 0NS 0NS 0NS 10NS)
VS2 3 0 PULSE (5V 5V 0NS 0NS 0NS 10NS)
VS3 14 0 PULSE (5V 5V 0NS 0NS 0NS 10NS)
.TRAN 0.5NS 40NS
.PLOT TRAN V(8) V(23) (0V,5V)
.END
```

```
1********12/31/84 ********  SPICE 2G.1 (15OCT88)  ********88:19:89****

8       CMOS/SOS BASIC SECTION 1 TRANSIENT ANALYSIS - OUTPUT 818

8****    TRANSIENT ANALYSIS              TEMPERATURE =   27.888 DEG C

8******************************************************************************

8LEGEND:

 *: V(8)
 +: V(23)
X
      TIME        V(8)

X(*+)------------ 8.     d+88     1.25@d+88    2.5@@d+88    3.75@d+88  5.@@@d+88
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
 8.    d+88   9.835d-88 X
 5.@@@d-1@    9.835d-88 X
 1.@@@d-89    9.835d-88 X
 1.5@@d-89    9.835d-88 X
 2.@@@d-89    9.835d-88 X
 2.5@@d-89    9.835d-88 *.
 3.@@@d-89    9.835d-88   *.
 3.5@@d-89    9.84@d-88   *
 4.@@@d-89    9.866d-88   *
 4.5@@d-89    9.135d-88   *
 5.@@@d-89    2.153d-85   *
 5.5@@d-89    2.957d-83     *
 6.@@@d-89    3.877d-82      *
 6.5@@d-89    1.198d-81   .*
 7.@@@d-89    2.668d-81   .     *
 7.5@@d-89    6.131d-81   .         *
 8.@@@d-89    1.@33d+@@  .              *
 8.5@@d-89    1.579d+@@  .                 *
 9.@@@d-89    2.168d+@@  .                     *
 9.5@@d-89    2.755d+@@  .                         *
 1.@@@d-88    3.274d+@@  .                            *
 1.@5@d-88    3.728d+@@  .                                *
 1.1@@d-88    4.@68d+@@  .                                   *
 1.15@d-88    4.33@d+@@  .                                     *
 1.2@@d-88    4.52@d+@@  .                                       *
 1.25@d-88    4.663d+@@  .
 1.3@@d-88    4.774d+@@  .
 1.35@d-88    4.84@d+@@  .
 1.4@@d-88    4.893d+@@  .
 1.45@d-88    4.927d+@@  .
 1.5@@d-88    4.95@d+@@  .
 1.55@d-88    4.967d+@@  .
 1.6@@d-88    4.976d+@@  .
 1.65@d-88    4.984d+@@  .
 1.7@@d-88    4.981d+@@  .
 1.75@d-88    4.956d+@@  .
 1.8@@d-88    4.848d+@@  .
 1.85@d-88    4.626d+@@  .                                  *
 1.9@@d-88    4.241d+@@  .
 1.95@d-88    3.733d+@@  .+
 2.@@@d-88    3.122d+@@  .+
 2.@5@d-88    2.489d+@@  .+
 2.1@@d-88    1.855d+@@  .+
 2.15@d-88    1.315d+@@  +
 2.2@@d-88    8.356d-81   +
 2.25@d-88    5.442d-81   +
 2.3@@d-88    3.2@4d-81  +
 2.35@d-88    1.791d-81  +  *
 2.4@@d-88    1.@43d-81  +*
 2.45@d-88    5.72@d-82  +*
 2.5@@d-88    3.185d-82 X
 2.55@d-88    1.695d-82 X
 2.6@@d-88    1.@19d-82 X
 2.65@d-88    5.344d-83 X
 2.7@@d-88    2.8@@d-83 X
 2.75@d-88    1.615d-83 X
 2.8@@d-88    8.149d-84 X
 2.85@d-88    4.599d-84 X
 2.9@@d-88    2.5@5d-84 X
 2.95@d-88    1.227d-84 X
 3.@@@d-88    7.356d-85 X
 3.@5@d-88    3.837d-85 X
 3.1@@d-88    2.@@@d-85 X
 3.15@d-88    1.16@d-85 X
 3.2@@d-88    6.@81d-86 X
 3.25@d-88    3.356d-86 X
 3.3@@d-88    1.867d-86 X
 3.35@d-88    9.59@d-87 X
 3.4@@d-88    6.11@d-87 X
 3.45@d-88    3.616d-87 X
 3.5@@d-88    2.32@d-87 X
 3.55@d-88    1.719d-87 X
 3.6@@d-88    1.314d-87 X
 3.65@d-88    1.135d-87 X
 3.7@@d-88    1.@29d-87 X
 3.75@d-88    9.661d-88 X
 3.8@@d-88    9.4@4d-88 X
 3.@5@d-88    9.227d-88 X
 3.9@@d-88    9.135d-88 X
 3.95@d-88    9.@93d-88 X
 4.@@@d-88    9.@63d-88 X
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
```

Figure C-4.   SPICE Plot Basic Section 1 with Input 101.
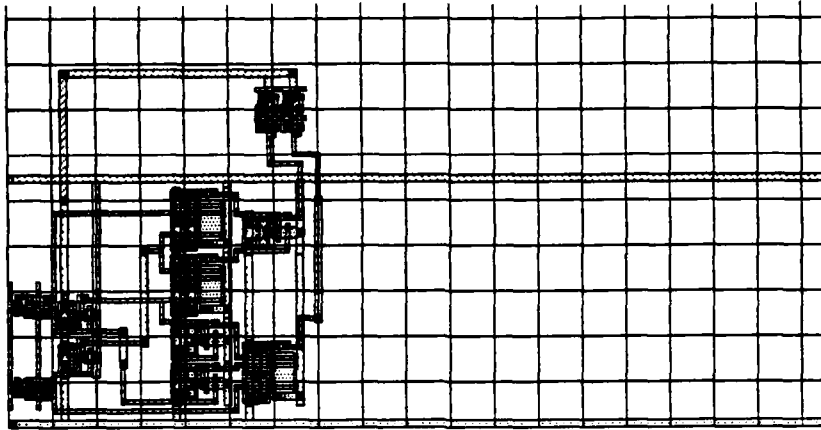
Figure C-5.   CLL Plot Section 1 with Two Node Precharge.
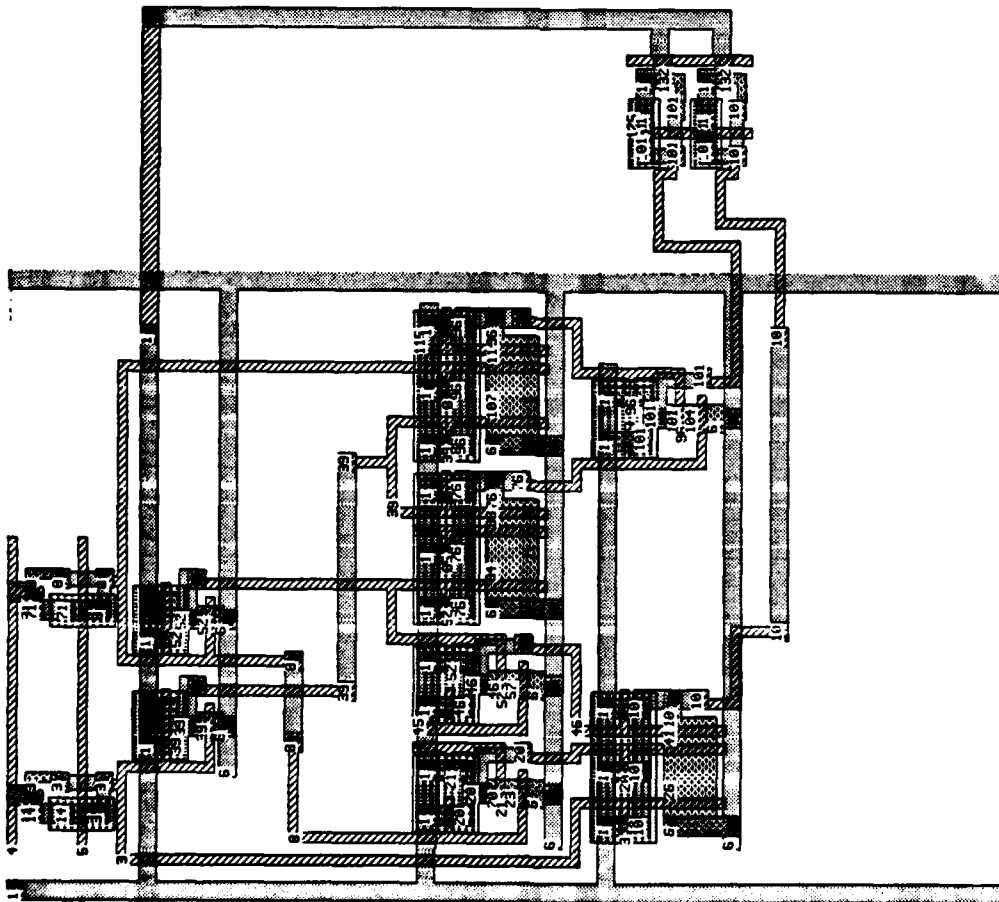
Figure C-6.   Node Plot Section 1 With Two Nodes Precharged

Table C-2

BITSLICE SECTION 1 PRECHARGED AT TWO NODES - NODE REFERENCE LIST

GND	0
Vdd	1
NMOS	0
PMOS	1
10	2
132	3
1	4
101	5
125	6
96	7
115	8
114	9
8	10
107	11
39	12
6	13
76	14
104	15
88	16
85	17
84	18
52	19
4	20
71	21
5	22
46	23
45	24
57	25
41	26
3	27
20	28
26	29
21	30
14	31
23	32

Ø   CMOS/SOS BITSLICE SECTION 1 PRERCHARGED AT TWO NODES - OUTPUT 1Ø1

Ø****   INPUT LISTING   TEMPERATURE =   27.ØØØ DEG C

Ø***

```
 .WIDTH OUT=8Ø
 .OPTIONS ITL1=5ØØ ITL5=Ø
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
 +LEVEL=1
 VDD 1 Ø DC 5V
 M1  1  3  2  Ø NMOS L=5.ØU W=5.ØU
 M2  1  3  5  Ø NMOS L=5.ØU W=5.ØU
 M3  2  6  1  1 PMOS L=5.ØU W=1Ø.ØU
 M4  5  6  1  1 PMOS L=5.ØU W=1Ø.ØU
 M5  1  8  7  1 PMOS L=5.ØU W=1Ø.ØU
 M6  9  8  7  Ø NMOS L=5.ØU W=3Ø.ØU
 M7  11 1Ø 9  Ø NMOS L=5.ØU W=3Ø.ØU
 M8  1  1Ø 7  1 PMOS L=5.ØU W=1Ø.ØU
 M9  1  7  5  1 PMOS L=5.ØU W=1Ø.ØU
 M1Ø Ø  12 11 Ø NMOS L=5.ØU W=3Ø.ØU
 M11 15 14 Ø  Ø NMOS L=5.ØU W=15.ØU
 M12 15 7  5  Ø NMOS L=5.ØU W=15.ØU
 M13 1  14 5  1 PMOS L=5.ØU W=1Ø.ØU
 M14 1  12 7  1 PMOS L=5.ØU W=1Ø.ØU
 M15 1  12 14 1 PMOS L=5.ØU W=1Ø.ØU
 M16 16 12 14 Ø NMOS L=5.ØU W=3Ø.ØU
 M17 1Ø 17 16 Ø NMOS L=5.ØU W=3Ø.ØU
 M18 1  17 14 1 PMOS L=5.ØU W=1Ø.ØU
 M19 Ø  19 18 Ø NMOS L=5.ØU W=3Ø.ØU
 M2Ø 21 2Ø 1Ø Ø NMOS L=5.ØU W=5.ØU
 M21 1  19 14 1 PMOS L=5.ØU W=1Ø.ØU
 M22 21 22 1Ø 1 FMOS L=5.ØU W=1Ø.ØU
 M23 Ø  1Ø 19 Ø NMOS L=5.ØU W=15.ØU
 M24 1  1Ø 19 1 PMOS L=5.ØU W=3Ø.ØU
 M25 1  19 23 1 PMOS L=5.ØU W=1Ø.ØU
 M26 25 24 Ø  Ø NMOS L=5.ØU W=15.ØU
 M27 25 19 23 Ø NMOS L=5.ØU W=15.ØU
 M28 1  23 2  1 PMOS L=5.ØU W=1Ø.ØU
 M29 1  24 23 1 PMOS L=5.ØU W=1Ø.ØU
 M3Ø 26 23 2  Ø NMOS L=5.ØU W=3Ø.ØU
 M31 Ø  27 12 Ø NMOS L=5.ØU W=15.ØU
 M32 2Ø 28 26 Ø NMOS L=5.ØU W=3Ø.ØU
 M33 1  27 12 1 PMOS L=5.ØU W=3Ø.ØU
 M34 1  28 2  1 PMOS L=5.ØU W=1Ø.ØU
 M35 1  3Ø 28 1 PMOS L=5.ØU W=1Ø.ØU
 M36 31 2Ø 27 Ø NMOS L=5.ØU W=5.ØU
 M37 Ø  27 29 Ø NMOS L=5.ØU W=3Ø.ØU
 M38 32 1Ø Ø  Ø NMOS L=5.ØU W=15.ØU
 M39 32 3Ø 28 Ø NMOS L=5.ØU W=15.ØU
 M4Ø 1  1Ø 23 1 PMOS L=5.ØU W=1Ø.ØU
 M41 31 22 27 1 FMOS L=5.ØU W=1Ø.ØU
 M42 1  27 2  1 PMOS L=5.ØU W=1Ø.ØU
 C43 1  Ø  Ø.1478PF
 C44 27 Ø  Ø.2Ø7PF
 C45 2Ø Ø  Ø.51PF
 C46 Ø  Ø  Ø.1174PF
 C47 1Ø Ø  Ø.297PF
```

```
C48 2 0 0.234PF
C49 28 0 0.111PF
C50 29 0 0.86PF
C51 12 0 0.202PF
C52 23 0 0.121PF
C53 19 0 0.151PF
C54 14 0 0.171PF
C55 18 0 0.86PF
C56 7 0 0.172PF
C57 5 0 0.234PF
C58 11 0 0.86PF
VA0 31 0 PULSE (0V 5V 0NS 0NS 0NS 10NS)
VB0 21 0 PULSE (0V 0V 0NS 0NS 0NS 10NS)
VPHI1 20 0 PULSE (5V 5V 0NS 0NS 0NS 10NS)
VPHI1BAR 22 0 PULSE (0V 0V 0NS 0NS 0NS 10NS)
VS0 30 0 PULSE (0V 0V 0NS 0NS 0NS 10NS)
VS1 24 0 PULSE (0V 0V 0NS 0NS 0NS 10NS)
VS2 8 0 PULSE (5V 5V 0NS 0NS 0NS 10NS)
VS3 17 0 PULSE (5V 5V 0NS 0NS 0NS 10NS)
VP1 3 0 PULSE (0V 5V 4NS 0NS 0NS 2NS)
VP1BAR 6 0 PULSE (5V 0V 4NS 0NS 0NS 2NS)
.TRAN 0.5NS 40NS
.PLOT TRAN V(5) V(2) (0V,5V)
.END
```

```
1********12/01/84 ********  SPICE 2G.1 (15OCT8#)  ********#5:##:19******

#       CMOS/SOS BITSLICE SECTION 1 PRERCHARGED AT TWO NODES - OUTPUT 1#1
                                                          X1
#****       TRANSIENT ANALYSIS                 TEMPERATURE =   27.### DEG C

#********************************************************************************

#LEGEND:

 *: V(5)
 +: V(2)
X
    TIME        V(5)

X(*+)------------  #.      d+##      1.25#d+##     2.5##d+##     3.75#d+## 5.###d+##
```


Figure C-7.   SPICE Plot Section 1 with Input 010 and
              Two Node Precharge Basic Gate Widths

C-14

```
 .WIDTH OUT=8Ø
 .OPTIONS ITL1=5ØØ ITL5=Ø
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
 +LEVEL=1
 VDD 1 Ø DC 5V
 M1  1  3  2  Ø NMOS L=5.ØU W=5.ØU
 M2  1  3  5  Ø NMOS L=5.ØU W=5.ØU
 M3  2  6  1  1 PMOS L=5.ØU W=1Ø.ØU
 M4  5  6  1  1 PMOS L=5.ØU W=1Ø.ØU
 M5  1  8  7  1 PMOS L=5.ØU W=1Ø.ØU
 M6  9  8  7  Ø NMOS L=5.ØU W=3Ø.ØU
 M7  11 1Ø 9  Ø NMOS L=5.ØU W=3Ø.ØU
 M8  1  1Ø 7  1 PMOS L=5.ØU W=1Ø.ØU
 M9  1  7  5  1 PMOS L=5.ØU W=1Ø.ØU
 M1Ø Ø  12 11 Ø NMOS L=5.ØU W=3Ø.ØU
 M11 15 14 Ø  Ø NMOS L=5.ØU W=15.ØU
 M12 15 7  5  Ø NMOS L=5.ØU W=15.ØU
 M13 1  14 5  1 PMOS L=5.ØU W=1Ø.ØU
 M14 1  12 7  1 PMOS L=5.ØU W=1Ø.ØU
 M15 1  12 14 1 PMOS L=5.ØU W=1Ø.ØU
 M16 16 12 14 Ø NMOS L=5.ØU W=3Ø.ØU
 M17 18 17 16 Ø NMOS L=5.ØU W=3Ø.ØU.
 M18 1  17 14 1 PMOS L=5.ØU W=1Ø.ØU
 M19 Ø  19 18 Ø NMOS L=5.ØU W=3Ø.ØU
 M2Ø 21 2Ø 19 Ø NMOS L=5.ØU W=5.ØU
 M21 1  19 14 1 PMOS L=5.ØU W=1Ø.ØU
 M22 21 22 1Ø 1 PMOS L=5.ØU W=1Ø.ØU
 M23 Ø  1Ø 19 Ø NMOS L=5.ØU W=15.ØU
 M24 1  1Ø 19 1 PMOS L=5.ØU W=3Ø.ØU
 M25 1  19 23 1 PMOS L=5.ØU W=1Ø.ØU
 M26 25 24 Ø  Ø NMOS L=5.ØU W=15.ØU
 M27 25 19 23 Ø NMOS L=5.ØU W=15.ØU
 M28 1  23 2  1 PMOS L=5.ØU W=1Ø.ØU
 M29 1  24 23 1 PMOS L=5.ØU W=1Ø.ØU
 M3Ø 26 23 2  Ø NMOS L=5.ØU W=3Ø.ØU
 M31 Ø  27 12 Ø NMOS L=5.ØU W=15.ØU
 M32 29 28 26 Ø NMOS L=5.ØU W=3Ø.ØU
 M33 1  27 12 1 PMOS L=5.ØU W=3Ø.ØU
 M34 1  28 2  1 PMOS L=5.ØU W=1Ø.ØU
 M35 1  3Ø 23 1 PMOS L=5.ØU W=1Ø.ØU
 M36 31 2Ø 27 Ø NMOS L=5.ØU W=5.ØU
 M37 Ø  27 29 Ø NMOS L=5.ØU W=3Ø.ØU
 M38 32 1Ø Ø  Ø NMOS L=5.ØU W=15.ØU
 M39 32 3Ø 23 Ø NMOS L=5.ØU W=15.ØU
 M4Ø 1  1Ø 23 1 PMOS L=5.ØU W=1Ø.ØU
 M41 31 22 27 1 PMOS L=5.ØU W=1Ø.ØU
 M42 1  27 2  1 PMOS L=5.ØU W=1Ø.ØU
 C43 1  Ø Ø.1478PF
 C44 27 Ø Ø.2Ø7PF
 C45 2Ø Ø Ø.51PF
 C46 Ø  Ø Ø.1174PF
 C47 1Ø Ø Ø.297PF
```

```
C48 2 Ø Ø.234PF
C49 28 Ø Ø.111PF
C5Ø 29 Ø Ø.86PF
C51 12 Ø Ø.2Ø2PF
C52 23 Ø Ø.121PF
C53 19 Ø Ø.151PF
C54 14 Ø Ø.171PF
C55 18 Ø Ø.86PF
C56 7 Ø Ø.172PF
C57 5 Ø Ø.234PF
C58 11 Ø Ø.86PF
VAØ 31 Ø PULSE (5V ØV ØNS ØNS ØNS 1ØNS)
VBØ 21 Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VPHI1 2Ø Ø PULSE (5V 5V ØNS ØNS ØNS 1ØNS)
VPHI1BAR 22 Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VSØ 3Ø Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VS1 24 Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VS2 8 Ø PULSE (5V 5V ØNS ØNS ØNS 1ØNS)
VS3 17 Ø PULSE (5V 5V ØNS ØNS ØNS 1ØNS)
VP1 3 Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS)
VP1BAR 6 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
.TRAN Ø.5NS 4ØNS
.PLOT TRAN V(5) V(2) (ØV,5V)
.END
```

```
#        CMOS/SOS BITSLICE SECTION 1 PRERCHARGED AT TWO NODES - OUTPUT #1#
                                                            x1
#••••      TRANSIENT ANALYSIS              TEMPERATURE =  27.ØØØ DEG C

#•••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••

#LEGEND:

 •: V(5)
 •: V(2)
 X
     TIME      V(5)

X(•+)------------ #.    d+## 	1.25#d+##     2.5##d+##     3.75#d+##  5.###d+##
     #.    d+##  1.355d-#7 X                :            :            :
     5.###d-1#  1.355d-#7 X                :            :            :
     1.###d-#9  1.355d-#7 X                :            :            :
     1.5##d-#9  1.355d-#7 X                :            :            :
     2.###d-#9  1.355d-#7 X                :            :            :
     2.5##d-#9  1.355d-#7 •+               :            :            :
     3.###d-#9  1.355d-#7 #+               :            :            :
     3.5##d-#9  1.356d-#7 # •              :            :            :
     4.###d-#9  1.357d-#7 #  •             :            :            :
     4.5##d-#9  2.1#3d-#1 .  •             :            :            :
     5.###d-#9  7.524d-#1   •    •         :            :            :
     5.5##d-#9  1.113d+##  .    • +        :            :            :
     6.###d-#9  1.42#d+##  .        • +    :            :            :
     6.5##d-#9  1.743d+##  .            • +:            :            :
     7.###d-#9  1.9#2d+##  .              •:  +         :            :
     7.5##d-#9  2.#94d+##  .               :  X         :            :
     8.###d-#9  2.356d+##  .               :    • +     :            :
     8.5##d-#9  2.652d+##  .               :       • +  :            :
     9.###d-#9  2.948d+##  .               :         •  : +          :
     9.5##d-#9  3.228d+##  .               :            :•  +        :
     1.###d-#8  3.497d+##  .               :            :  •    +    :
     1.#5#d-#8  3.737d+##  .               :            :    •      +:
     1.1##d-#8  3.945d+##  .               :            :       •    : +
     1.15#d-#8  4.124d+##  .               :            :         •  :  +
     1.2##d-#8  4.275d+##  .               :            :            :•  +
     1.25#d-#8  4.4#3d+##  .               :            :            : •   +
     1.3##d-#8  4.517d+##  .               :            :            :   •  +
     1.35#d-#8  4.6#3d+##  .               :            :            :     •  +
     1.4##d-#8  4.679d+##  .               :            :            :      •  +
     1.45#d-#8  4.74#d+##  .               :            :            :        •+
     1.5##d-#8  4.789d+##  .               :            :            :         •+
     1.55#d-#8  4.821d+##  .               :            :            :          •+
     1.6##d-#8  4.861d+##  .               :            :            :           •+
     1.65#d-#8  4.866d+##  .               :            :            :           •+
     1.7##d-#8  4.899d+##  .               :            :            :            •+
     1.75#d-#8  4.895d+##  .               :            :            :            •+
     1.8##d-#8  4.838d+##  .               :            :            :           •+
     1.85#d-#8  4.718d+##  .               :            :            :         •  +
     1.9##d-#8  4.466d+##  .               :            :            :      •     +
     1.95#d-#8  4.194d+##  •               :            :            :   •       +
     2.###d-#8  3.841d+##  •               :            :            : •        +
     2.#5#d-#8  3.464d+##  •               :            :            :•       +
     2.1##d-#8  3.#54d+##  •               :            :         •  :      +
     2.15#d-#8  2.63#d+##  .•              :            :      •     :    +
     2.2##d-#8  2.228d+##  .•              :            :   •        :  +
     2.25#d-#8  1.833d+##  .•              :            : •          :+
     2.3##d-#8  1.475d+##  .•              :         •  :            +
     2.35#d-#8  1.154d+##  •               :       •    :         +
     2.4##d-#8  9.#1#d-#1  •               :     •      :      +
     2.45#d-#8  6.779d-#1  •               :   •        :    +
     2.5##d-#8  5.1#3d-#1  •               : •          :  +
     2.55#d-#8  3.#82d-#1  •              .:•           + 
     2.6##d-#8  2.725d-#1  •           • .:          +
     2.65#d-#8  2.#37d-#1  •        •   .:        +
     2.7##d-#8  1.469d-#1  •     •     .:      +
     2.75#d-#8  1.#49d-#1  •+   •     .:    +
     2.8##d-#8  7.7##d-#2  •+ •      .:  +
     2.85#d-#8  5.441d-#2  •+•      .:+
     2.9##d-#8  3.944d-#2 X         :            :            :
     2.95#d-#8  2.844d-#2 X         :            :            :
     3.###d-#8  1.979d-#2 X         :            :            :
     3.#5#d-#8  1.46#d-#2 X         :            :            :
     3.1##d-#8  1.#37d-#2 X         :            :            :
     3.15#d-#8  7.326d-#3 X         :            :            :
     3.2##d-#8  5.353d-#3 X         :            :            :
     3.25#d-#8  3.755d-#3 X         :            :            :
     3.3##d-#8  2.713d-#3 X         :            :            :
     3.35#d-#8  1.951d-#3 X         :            :            :
     3.4##d-#8  1.354d-#3 X         :            :            :
     3.45#d-#8  9.9#1d-#4 X         :            :            :
     3.5##d-#8  7.#82d-#4 X         :            :            :
     3.55#d-#8  5.##1d-#4 X         :            :            :
     3.6##d-#8  3.653d-#4 X         :            :            :
     3.65#d-#8  2.562d-#4 X         :            :            :
     3.7##d-#8  1.851d-#4 X         :            :            :
     3.75#d-#8  1.331d-#4 X         :            :            :
     3.8##d-#8  9.241d-#5 X         :            :            :
     3.85#d-#8  6.814d-#5 X         :            :            :
     3.9##d-#8  4.839d-#5 X         :            :            :
     3.95#d-#8  3.42#d-#5 X         :            :            :
     4.###d-#8  2.425d-#5 X - - - - - - - - - - - - - - - - - :
```

Figure C-8.   SPICE Plot Section 1 Input 101 and Two
             Node Precharge with Basic Gate Widths

```
.WIDTH OUT=80
.OPTIONS ITL1=500 ITL5=0
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
+LEVEL=1
VDD 1 0 DC 5V
M1  1  3  2  0  NMOS L=5.0U W=10.0U
M2  1  3  5  0  NMOS L=5.0U W=10.0U
M3  2  6  1  1  PMOS L=5.0U W=20.0U
M4  5  6  1  1  PMOS L=5.0U W=20.0U
M5  1  8  7  1  PMOS L=5.0U W=10.0U
M6  9  8  7  0  NMOS L=5.0U W=30.0U
M7  11 10 9  0  NMOS L=5.0U W=30.0U
M8  1  10 7  1  PMOS L=5.0U W=10.0U
M9  1  7  5  1  PMOS L=5.0U W=10.0U
M10 0  12 11 0  NMOS L=5.0U W=30.0U
M11 15 14 0  0  NMOS L=5.0U W=15.0U
M12 15 7  5  0  NMOS L=5.0U W=15.0U
M13 1  14 5  1  PMOS L=5.0U W=10.0U
M14 1  12 7  1  PMOS L=5.0U W=10.0U
M15 1  12 14 1  PMOS L=5.0U W=10.0U
M16 16 12 14 0  NMOS L=5.0U W=30.0U
M17 10 17 16 0  NMOS L=5.0U W=30.0U
M18 1  17 14 1  PMOS L=5.0U W=10.0U
M19 0  19 18 0  NMOS L=5.0U W=30.0U
M20 21 20 10 0  NMOS L=5.0U W=5.0U
M21 1  19 14 1  PMOS L=5.0U W=10.0U
M22 21 22 10 1  PMOS L=5.0U W=10.0U
M23 0  10 19 0  NMOS L=5.0U W=15.0U
M24 1  10 19 1  PMOS L=5.0U W=30.0U
M25 1  19 23 1  PMOS L=5.0U W=10.0U
M26 25 24 0  0  NMOS L=5.0U W=15.0U
M27 25 19 23 0  NMOS L=5.0U W=15.0U
M28 1  23 2  1  PMOS L=5.0U W=10.0U
M29 1  24 23 1  PMOS L=5.0U W=10.0U
M30 26 23 2  0  NMOS L=5.0U W=30.0U
M31 0  27 12 0  NMOS L=5.0U W=15.0U
M32 29 23 26 0  NMOS L=5.0U W=30.0U
M33 1  27 12 1  PMOS L=5.0U W=30.0U
M34 1  23 2  1  PMOS L=5.0U W=10.0U
M35 1  30 23 1  PMOS L=5.0U W=10.0U
M36 31 20 27 0  NMOS L=5.0U W=5.0U
M37 0  27 29 0  NMOS L=5.0U W=30.0U
M38 32 10 0  0  NMOS L=5.0U W=15.0U
M39 32 30 23 0  NMOS L=5.0U W=15.0U
M40 1  10 23 1  PMOS L=5.0U W=10.0U
M41 31 22 27 1  PMOS L=5.0U W=10.0U
M42 1  27 2  1  PMOS L=5.0U W=10.0U
C43 1  0  0.1470PF
C44 27 0  0.07PF
C45 20 0  0.51PF
C46 0  0  0.1174PF
C47 10 0  0.297PF
```

C-18

```
C48 2 0 0.234PF
C49 28 0 0.111PF
C50 29 0 0.86PF
C51 12 0 0.202PF
C52 23 0 0.121PF
C53 19 0 0.151PF
C54 14 0 0.171PF
C55 18 0 0.86PF
C56 7 0 0.172PF
C57 5 0 0.234PF
C58 11 0 0.86PF
VA0 31 0 PULSE (0V 5V 0NS 0NS 0NS 10NS)
VB0 21 0 PULSE (0V 0V 0NS 0NS 0NS 10NS)
VPHI1 20 0 PULSE (5V 5V 0NS 0NS 0NS 10NS)
VPHI1BAR 22 0 PULSE (0V 0V 0NS 0NS 0NS 10NS)
VS0 30 0 PULSE (0V 0V 0NS 0NS 0NS 10NS)
VS1 24 0 PULSE (0V 0V 0NS 0NS 0NS 10NS)
VS2 8 0 PULSE (5V 5V 0NS 0NS 0NS 10NS)
VS3 17 0 PULSE (5V 5V 0NS 0NS 0NS 10NS)
VP1 3 0 PULSE (0V 5V 4NS 0NS 0NS 2NS)
VP1BAR 6 0 PULSE (5V 0V 4NS 0NS 0NS 2NS)
.TRAN 0.5NS 40NS
.PLOT TRAN V(5) V(2) (0V,5V)
.END
```

```
1*******12/01/04 ********  SPICE 2G.1 (15OCT8#)  ********#5:2#:29*****

#         CMOS/SOS BITSLICE SECTION 1 PRERCHARGED AT TWO NODES - OUTPUT 1#1
                                                            x2
#****     TRANSIENT ANALYSIS              TEMPERATURE =   27.### DEG C

#*****************************************************************************


#LEGEND:

 *: V(5)
 +: V(2)
X
     TIME       V(5)

X(*+)------------ #,     d+##     1.25#d+##      2.5##d+##     3.75#d+## 5.###d+##
    #.   d+##  5.###d+## - - - - - - - - - - - - - - - - - - - - - - - - - - - X
  5.###d-1#  5.###d+##  .                 .              .             .       X
  1.###d-#9  5.###d+##  .                 .              .             .       X
  1.5##d-#9  5.###d+##  .                 .              .             .       X
  2.###d-#9  5.###d+##  .                 .              .             .       X
  2.5##d-#9  5.###d+##  .                 .              .             .       X
  3.###d-#9  5.###d+##  .                 .              .             .       X
  3.5##d-#9  5.###d+##  .                 .              .             .     X X
  4.###d-#9  5.###d+##  .                 .              .             .       X
  4.5##d-#9  5.###d+##  .                 .              .             .      *
  5.###d-#9  5.###d+##  .                 .              .             .     *
  5.5##d-#9  5.###d+##  .                 .              .             .    *
  6.###d-#9  5.###d+##  .                 .              .             .   *
  6.5##d-#9  5.###d+##  .                 .              .             .  *
  7.###d-#9  4.991d+##  .                 .              .             . *
  7.5##d-#9  4.933d+##  .                 .              .             .*
  8.###d-#9  4.787d+##  .                 .              .            *
  8.5##d-#9  4.562d+##  .                 .              .         *
  9.###d-#9  4.274d+##  .                 .              .      *
  9.5##d-#9  3.928d+##  .                 .              .   *
  1.###d-#8  3.549d+##  .                 .            *
  1.#5#d-#8  3.14#d+##  .                 .         *
  1.1##d-#8  2.714d+##  .               *
  1.15#d-#8  2.291d+##  .            *
  1.2##d-#8  1.886d+##  .         *
  1.25#d-#8  1.521d+##  .      *
  1.3##d-#8  1.197d+##  .   *
  1.35#d-#8  9.387d-#1  . *
  1.4##d-#8  7.1#4d-#1  *
  1.45#d-#8  5.343d-#1  X
  1.5##d-#8  4.#25d-#1  *
  1.55#d-#8  2.968d-#1  *
  1.6##d-#8  2.322d-#1  *
  1.65#d-#8  2.#74d-#1  *
  1.7##d-#8  2.127d-#1  *
  1.75#d-#8  3.4##d-#1  *
  1.##8d-#8  5.211d-#1  *
  1.85#d-#8  7.842d-#1   *
  1.9##d-#8  1.1#7d+##    *
  1.95#d-#8  1.453d+##       *
  2.###d-#8  1.824d+##  .      *
  2.#5#d-#8  2.197d+##  .        *
  2.1##d-#8  2.56#d+##  .          *
  2.15#d-#8  2.895d+##  .            *
  2.2##d-#8  3.2#7d+##  .              *
  2.25#d-#8  3.46#d+##  .                *
  2.3##d-#8  3.734d+##  .                  *
  2.35#d-#8  3.943d+##  .                    *
  2.4##d-#8  4.126d+##  .                      *
  2.45#d-#8  4.28#d+##  .                       *
  2.5##d-#8  4.411d+##  .                         *
  2.55#d-#8  4.522d+##  .                          *
  2.6##d-#8  4.612d+##  .                           *
  2.65#d-#8  4.684d+##  .                            *
  2.7##d-#8  4.747d+##  .                             *
  2.75#d-#8  4.794d+##  .                              *
  2.8##d-#8  4.824d+##  .                              *
  2.85#d-#8  4.868d+##  .                               *
  2.9##d-#8  4.892d+##  .                                *
  2.95#d-#8  4.914d+##  .                                *
  3.###d-#8  4.931d+##  .                                 *
  3.#5#d-#8  4.944d+##  .                                  *
  3.1##d-#8  4.955d+##  .                                  *
  3.15#d-#8  4.964d+##  .                                   *
  3.2##d-#8  4.971d+##  .                                   *
  3.25#d-#8  4.977d+##  .                                    *
  3.3##d-#8  4.981d+##  .                                    *
  3.35#d-#8  4.985d+##  .                                    *
  3.4##d-#8  4.988d+##  .                                     *
  3.45#d-#8  4.99#d+##  .                                     *
  3.5##d-#8  4.992d+##  .                                     *
  3.55#d-#8  4.994d+##  .                                     *
  3.6##d-#8  4.995d+##  .                                     *
  3.65#d-#8  4.996d+##  .                                     *
  3.7##d-#8  4.997d+##  .                                     *
  3.75#d-#8  4.997d+##  .                                     *
  3.8##d-#8  4.998d+##  .                                     *
  3.85#d-#8  4.998d+##  .                                     *
  3.9##d-#8  4.999d+##  .                                     *
  3.95#d-#8  4.999d+##  .                                     *
  4.###d-#8  4.999d+##  - - - - - - - - - - - - - - - - - - - - - - - - - - - *
```

Figure C-9.   SPICE Plot Section 1 Input 010 and Two
              Node Precharge with Basic Widths x2

C-20

```
1*******12/Ø1/84 ******** SPICE 2G.1 (15OCT8Ø) *******Ø5:2Ø:29*****

Ø          CMOS/SOS BITSLICE SECTION 1 PRERCHARGED AT TWO NODES - OUTPUT 1Ø1

J****     INPUT LISTING                      TEMPERATURE =   27.ØØØ DEG C

Ø*********************************************************************************


 .WIDTH OUT=8Ø
 .OPTIONS ITL1=5ØØ ITL5=Ø
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
 +LEVEL=1
 VDD 1 Ø DC 5V
 M1  1  3  2  Ø NMOS L=5.ØU W=1Ø.ØU
 M2  1  3  5  Ø NMOS L=5.ØU W=1Ø.ØU
 M3  2  6  1  1 PMOS L=5.ØU W=2Ø.ØU
 M4  5  6  1  1 PMOS L=5.ØU W=2Ø.ØU
 M5  1  8  7  1 PMOS L=5.ØU W=1Ø.ØU
 M6  9  8  7  Ø NMOS L=5.ØU W=3Ø.ØU
 M7  11 1Ø 9  Ø NMOS L=5.ØU W=3Ø.ØU
 M8  1  1Ø 7  1 PMOS L=5.ØU W=1Ø.ØU
 M9  1  7  5  1 PMOS L=5.ØU W=1Ø.ØU
 M1Ø Ø  12 11 Ø NMOS L=5.ØU W=3Ø.ØU
 M11 15 14 Ø  Ø NMOS L=5.ØU W=15.ØU
 M12 15 7  5  Ø NMOS L=5.ØU W=15.ØU
 M13 1  14 5  1 PMOS L=5.ØU W=1Ø.ØU
 M14 1  12 7  1 PMOS L=5.ØU W=1Ø.ØU
 M15 1  12 14 1 PMOS L=5.ØU W=1Ø.ØU
 M16 16 12 14 Ø NMOS L=5.ØU W=3Ø.ØU
 M17 18 17 16 Ø NMOS L=5.ØU W=3Ø.ØU
 M18 1  17 14 1 PMOS L=5.ØU W=1Ø.ØU
 M19 Ø  19 18 Ø NMOS L=5.ØU W=3Ø.ØU
 M2Ø 21 2Ø 1Ø Ø NMOS L=5.ØU W=5.ØU
 M21 1  19 14 1 PMOS L=5.ØU W=1Ø.ØU
 M22 21 22 1Ø 1 FMOS L=5.ØU W=1Ø.ØU
 M23 Ø  1Ø 19 Ø NMOS L=5.ØU W=15.ØU
 M24 1  1Ø 19 1 PMOS L=5.ØU W=3Ø.ØU
 M25 1  19 23 1 PMOS L=5.ØU W=1Ø.ØU
 M26 25 24 Ø  Ø NMOS L=5.ØU W=15.ØU
 M27 25 19 23 Ø NMOS L=5.ØU W=15.ØU
 M28 1  23 2  1 PMOS L=5.ØU W=1Ø.ØU
 M29 1  24 23 1 PMOS L=5.ØU W=1Ø.ØU
 M3Ø 26 23 2  Ø NMOS L=5.ØU W=3Ø.ØU
 M31 Ø  27 12 Ø NMOS L=5.ØU W=15.ØU
 M32 29 28 26 Ø NMOS L=5.ØU W=3Ø.ØU
 M33 1  27 12 1 PMOS L=5.ØU W=3Ø.ØU
 M34 1  28 2  1 PMOS L=5.ØU W=1Ø.ØU
 M35 1  3Ø 23 1 PMOS L=5.ØU W=1Ø.ØU
 M36 31 2Ø 27 Ø NMOS L=5.ØU W=5.ØU
 M37 Ø  27 29 Ø NMOS L=5.ØU W=3Ø.ØU
 M38 32 1Ø Ø  Ø NMOS L=5.ØU W=15.ØU
 M39 32 3Ø 28 Ø NMOS L=5.ØU W=15.ØU
 M4Ø 1  1Ø 23 1 PMOS L=5.ØU W=1Ø.ØU
 M41 31 22 27 1 PMOS L=5.ØU W=1Ø.ØU
 M42 1  27 2  1 PMOS L=5.ØU W=1Ø.ØU
 C43 1  Ø Ø.1478PF
 C44 27 Ø Ø.2Ø7PF
 C45 2Ø Ø Ø.51PF
 C46 Ø  Ø Ø.1174PF
 C47 1Ø Ø Ø.297PF
```

```
C48 2 Ø Ø.234PF
C49 28 Ø Ø.111PF
C5Ø 29 Ø Ø.86PF
C51 12 Ø Ø.2Ø2PF
C52 23 Ø Ø.121PF
C53 19 Ø Ø.151PF
C54 14 Ø Ø.171PF
C55 18 Ø Ø.86PF
C56 7 Ø Ø.172PF
C57 5 Ø Ø.234PF
C58 11 Ø Ø.86PF
VAØ 31 Ø PULSE (5V ØV ØNS ØNS ØNS 1ØNS)
VBØ 21 Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VPHI1 2Ø Ø PULSE (5V 5V ØNS ØNS ØNS 1ØNS)
VPHI1BAR 22 Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VSØ 3Ø Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VS1 24 Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VS2 8 Ø PULSE (5V 5V ØNS ØNS ØNS 1ØNS)
VS3 17 Ø PULSE (5V 5V ØNS ØNS ØNS 1ØNS)
VP1 3 Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS)
VP1BAR 6 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
.TRAN Ø.5NS 4ØNS
.PLOT TRAN V(5) V(2) (ØV,5V)
.END
```

```
1********12/#1/#4 ********   SPICE 2G.1 (15OCT8#)  ********#5:21:25*****

#        CMOS/SOS BITSLICE SECTION 1 PRERCHARGED AT TWO NODES - OUTPUT #1#
                                                            x2
#****     TRANSIENT ANALYSIS              TEMPERATURE =   27.### DEG C

#*************************************************************************

#LEGEND:

 *: V(5)
 +: V(2)
X
     TIME      V(5)

X(*+)----------- #.     d+##    1.25#d+##    2.5##d+##    3.75#d+##  5.###d+##
     #.    d+##  1.355d-#7 X
     5.###d-1#  1.355d-#7 X
     1.###d-#9  1.355d-#7 X
     1.5##d-#9  1.355d-#7 X
     2.###d-#9  1.355d-#7 X
     2.5##d-#9  1.355d-#7 *+
     3.###d-#9  1.355d-#7 *+
     3.5##d-#9  1.356d-#7 *
     4.###d-#9  1.357d-#7 *
     4.5##d-#9  3.951d-#1     *    *
     5.###d-#9  1.326d+##  .
     5.5##d-#9  1.932d+##         *+         *
     6.###d-#9  2.451d+##                        *   *
     6.5##d-#9  2.991d+##
     7.###d-#9  3.234d+##                              X
     7.5##d-#9  3.395d+##                                *  *
     8.###d-#9  3.592d+##  .
     8.5##d-#9  3.786d+##  .
     9.###d-#9  3.969d+##  .
     9.5##d-#9  4.136d+##  .
     1.###d-#8  4.279d+##  .
     1.#5#d-#8  4.411d+##  .
     1.1##d-#8  4.517d+##  .
     1.15#d-#8  4.6#4d+##  .
     1.2##d-#8  4.675d+##  .
     1.25#d-#8  4.738d+##  .
     1.3##d-#8  4.766d+##  .
     1.35#d-#8  4.828d+##  .
     1.4##d-#8  4.861d+##  .
     1.45#d-#8  4.888d+##  .
     1.5##d-#8  4.911d+##  .
     1.55#d-#8  4.927d+##  .
     1.6##d-#8  4.941d+##  .
     1.65#d-#8  4.952d+##  .
     1.7##d-#8  4.959d+##  .
     1.75#d-#8  4.952d+##  .
     1.8##d-#8  4.886d+C#  .
     1.85#d-#8  4.751d+##  .
     1.9##d-#8  4.529d+##  .
     1.95#d-#8  4.236d+##  .
     2.###d-#8  3.86#d+##             *
     2.#5#d-#8  3.512d+#8
     2.1##d-#8  3.#98d+##  .  *
     2.15#d-#8  2.682d+##
     2.2##d-#8  2.262d+##
     2.25#d-#8  1.872d+##  .:          *
     2.3##d-#8  1.5#4d+##  .:
     2.35#d-#8  1.169d+##  .+
     2.4##d-#8  9.23#d-#1  .+
     2.45#d-#8  6.9#3d-#1  .+
     2.5##d-#8  5.277d-#1  .+
     2.55#d-#8  3.894d-#1  .+
     2.6##d-#8  2.835d-#1  .+       *
     2.65#d-#8  2.1#4d-#1  .+
     2.7##d-#8  1.5##d-#1  .+   *
     2.75#d-#8  1.#96d-#1  .+*
     2.8##d-#8  7.931d-#2  .+*
     2.85#d-#8  5.537d-#2  .+*
     2.9##d-#8  4.#99d-#2  X
     2.95#d-##  2.915d-#2  X
     3.###d-#8  2.#67d-#2  X
     3.#5#d-##  1.5#9d-#2  X
     3.1##d-##  1.#59d-#2  X
     3.15#d-#8  7.668d-#3  X
     3.2##d-##  5.51#d-#3  X
     3.25#d-##  3.821d-#3  X
     3.3##d-#8  2.822d-#3  X
     3.35#d-#8  2.###d-#3  X
     3.4##d-##  1.415d-#3  X
     3.45#d-#8  1.#32d-#3  X
     3.5##d-#8  7.2#1d-#4  X
     3.55#d-#8  5.2#4d-#4  X
     3.6##d-#8  3.76#d-#4  X
     3.65#d-#8  2.6#7d-#4  X
     3.7##d-#8  1.925d-#4  X
     3.75#d-#8  1.364d-#4  X
     3.8##d-#8  9.659d-#5  X
     3.85#d-##  7.#47d-#5  X
     3.9##d-##  4.9#8d-#5  X
     3.95#d-##  3.579d-#5  X
     4.###d-#8  2.5#2d-#5  X
```

Figure C-10.   SPICE Plot Section 1 Input 101 Two Node
               Precharge with Gate Widths x2

```
.WIDTH OUT=8Ø
.OPTIONS ITL1=5ØØ ITL5=Ø
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
+LEVEL=1
VDD 1 Ø DC 5V
M1  1 3 2 Ø NMOS L=5.ØU W=15.ØU
M2  1 3 5 Ø NMOS L=5.ØU W=15.ØU
M3  2 6 1 1 PMOS L=5.ØU W=3Ø.ØU
M4  5 6 1 1 PMOS L=5.ØU W=3Ø.ØU
M5  1 8 7 1 PMOS L=5.ØU W=1Ø.ØU
M6  9 8 7 Ø NMOS L=5.ØU W=3Ø.ØU
M7  11 1Ø 9 Ø NMOS L=5.ØU W=3Ø.ØU
M8  1 1Ø 7 1 PMOS L=5.ØU W=1Ø.ØU
M9  1 7 5 1 PMOS L=5.ØU W=1Ø.ØU
M1Ø Ø 12 11 Ø NMOS L=5.ØU W=3Ø.ØU
M11 15 14 Ø Ø NMOS L=5.ØU W=15.ØU
M12 15 7 5 Ø NMOS L=5.ØU W=15.ØU
M13 1 14 5 1 PMOS L=5.ØU W=1Ø.ØU
M14 1 12 7 1 PMOS L=5.ØU W=1Ø.ØU
M15 1 12 14 1 PMOS L=5.ØU W=1Ø.ØU
M16 16 12 14 Ø NMOS L=5.ØU W=3Ø.ØU
M17 1Ø 17 16 Ø NMOS L=5.ØU W=3Ø.ØU
M18 1 17 14 1 PMOS L=5.ØU W=1Ø.ØU
M19 Ø 19 18 Ø NMOS L=5.ØU W=3Ø.ØU
M2Ø 21 2Ø 1Ø Ø NMOS L=5.ØU W=5.ØU
M21 1 19 14 1 PMOS L=5.ØU W=1Ø.ØU
M22 21 22 1Ø 1 FMOS L=5.ØU W=1Ø.ØU
M23 Ø 1Ø 19 Ø NMOS L=5.ØU W=15.ØU
M24 1 1Ø 19 1 PMOS L=5.ØU W=3Ø.ØU
M25 1 19 23 1 PMOS L=5.ØU W=1Ø.ØU
M26 25 24 Ø Ø NMOS L=5.ØU W=15.ØU
M27 25 19 23 Ø NMOS L=5.ØU W=15.ØU
M28 1 23 2 1 PMOS L=5.ØU W=1Ø.ØU
M29 1 24 23 1 PMOS L=5.ØU W=1Ø.ØU
M3Ø 26 23 2 Ø NMOS L=5.ØU W=3Ø.ØU
M31 Ø 27 12 Ø NMOS L=5.ØU W=15.ØU
M32 29 28 26 Ø NMOS L=5.ØU W=3Ø.ØU
M33 1 27 12 1 PMOS L=5.ØU W=3Ø.ØU
M34 1 28 2 1 PMOS L=5.ØU W=1Ø.ØU
M35 1 3Ø 23 1 PMOS L=5.ØU W=1Ø.ØU
M36 31 2Ø 27 Ø NMOS L=5.ØU W=5.ØU
M37 Ø 27 29 Ø NMOS L=5.ØU W=3Ø.ØU
M38 32 1Ø Ø Ø NMOS L=5.ØU W=15.ØU
M39 32 3Ø 23 Ø NMOS L=5.ØU W=15.ØU
M4Ø 1 1Ø 23 1 PMOS L=5.ØU W=1Ø.ØU
M41 31 22 27 1 FMOS L=5.ØU W=1Ø.ØU
M42 1 27 2 1 PMOS L=5.ØU W=1Ø.ØU
C43 1 Ø Ø.1478PF
C44 27 Ø Ø.2Ø7PF
C45 2Ø Ø Ø.51PF
C46 Ø Ø Ø.1174PF
C47 1Ø Ø Ø.297PF
```

```
C48 2 Ø Ø.234PF
C49 28 Ø Ø.111PF
C5Ø 29 Ø Ø.86PF
C51 12 Ø Ø.2Ø2PF
C52 23 Ø Ø.121PF
C53 19 Ø Ø.151PF
C54 14 Ø Ø.171PF
C55 18 Ø Ø.86PF
C56 7 Ø Ø.172PF
C57 5 Ø Ø.234PF
C58 11 Ø Ø.86PF
VAØ 31 Ø PULSE (ØV 5V ØNS ØNS ØNS 1ØNS)
VBØ 21 Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VPHI1 2Ø Ø PULSE (5V 5V ØNS ØNS ØNS 1ØNS)
VPHI1BAR 22 Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VSØ 3Ø Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VS1 24 Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VS2 8 Ø PULSE (5V 5V ØNS ØNS ØNS 1ØNS)
VS3 17 Ø PULSE (5V 5V ØNS ØNS ØNS 1ØNS)
VP1 3 Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS)
VP1BAR 6 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
.TRAN Ø.5NS 4ØNS
.PLOT TRAN V(5) V(2) (ØV,5V)
.END
```

```
1*******12/01/04 ********  SPICE 2G.1 (15OCT80)  ********05:22:28*****

#          CMOS/SOS BITSLICE SECTION 1 PRERCHARGED AT TWO NODES - OUTPUT 101
                                                                    x3
#****      TRANSIENT ANALYSIS                 TEMPERATURE =   27.000 DEG C

#*******************************************************************************

#LEGEND:

 *: V(5)
 +: V(2)
 x
       TIME      V(5)
X(*+)-----------  #.   d+00      1.250d+00      2.500d+00      3.750d+00  5.000d+00
      #.   d+00   5.000d+00   :              :              :              :      x
    5.000d-10   5.000d+00   :              :              :              :      x
    1.000d-09   5.000d+00   :              :              :              :      x
    1.500d-09   5.000d+00   :              :              :              :      x
    2.000d-09   5.000d+00   :              :              :              :      x
    2.500d-09   5.000d+00   :              :              :              :      x
    3.000d-09   5.000d+00   :              :              :              :      x
    3.500d-09   5.000d+00   :              :              :              :      x
    4.000d-09   5.000d+00   :              :              :              :      x
    4.500d-09   5.000d+00   :              :              :              :      +
    5.000d-09   5.000d+00   :              :              :              :      .
    5.500d-09   5.000d+00   :              :              :              :      .
    6.000d-09   5.000d+00   :              :              :              :      .
    6.500d-09   5.000d+00   :              :              :              :      .
    7.000d-09   4.991d+00   :              :              :              :     .
    7.500d-09   4.933d+00   :              :              :              :    .
    8.000d-09   4.787d+00   :              :              :             .     .
    8.500d-09   4.563d+00   :              :              :            .    .
    9.000d-09   4.274d+00   :              :              :          .    .
    9.500d-09   3.928d+00   :              :              :       .    .
    1.000d-08   3.549d+00   :              :            .       .
    1.050d-08   3.148d+00   :             .           .
    1.100d-08   2.714d+00   :        .           .
    1.150d-08   2.291d+00   :     .           .
    1.200d-08   1.866d+00   :   .          .
    1.250d-08   1.521d+00   : .         .
    1.300d-08   1.197d+00   .        .
    1.350d-08   9.368d-01   x      .
    1.400d-08   7.164d-01   .     .
    1.450d-08   5.343d-01   .    x
    1.500d-08   4.025d-01   . .
    1.550d-08   2.968d-01  . .
    1.600d-08   2.322d-01  .  .
    1.650d-08   2.074d-01  .   .
    1.700d-08   2.127d-01  .   .
    1.750d-08   3.400d-01   .   .
    1.800d-08   5.211d-01   .    .
    1.850d-08   7.842d-01    .    .
    1.900d-08   1.187d+00     .    .
    1.950d-08   1.453d+00      .    .
    2.000d-08   1.824d+00       .    .
    2.050d-08   2.197d+00         .    .
    2.100d-08   2.560d+00          .    .
    2.150d-08   2.898d+00            .    .
    2.200d-08   3.204d+00              .    .
    2.250d-08   3.461d+00                .    .
    2.300d-08   3.737d+00                 .     .
    2.350d-08   3.942d+00                    .    .
    2.400d-08   4.127d+00                      .    .
    2.450d-08   4.285d+00                        .    .
    2.500d-08   4.411d+00                          .    .
    2.550d-08   4.524d+00                            .    .
    2.600d-08   4.611d+00                              .    .
    2.650d-08   4.684d+00                                .    .
    2.700d-08   4.748d+00                                  .   .
    2.750d-08   4.794d+00                                    .  .
    2.800d-08   4.834d+00                                     . .
    2.850d-08   4.867d+00                                       ..
    2.900d-08   4.892d+00                                        .
    2.950d-08   4.914d+00                                         .
    3.000d-08   4.928d+00                                         .
    3.050d-08   4.944d+00                                          .
    3.100d-08   4.956d+00                                          .
    3.150d-08   4.964d+00                                           .
    3.200d-08   4.971d+00                                           .
    3.250d-08   4.977d+00                                           .
    3.300d-08   4.981d+00                                            .
    3.350d-08   4.985d+00                                            .
    3.400d-08   4.988d+00                                            .
    3.450d-08   4.990d+00                                            .
    3.500d-08   4.992d+00                                            .
    3.550d-08   4.994d+00                                            .
    3.600d-08   4.995d+00                                            .
    3.650d-08   4.996d+00                                            .
    3.700d-08   4.997d+00                                            .
    3.750d-08   4.997d+00                                            .
    3.800d-08   4.998d+00                                            .
    3.850d-08   4.998d+00                                            .
    3.900d-08   4.999d+00                                            .
    3.950d-08   4.999d+00                                            .
    4.000d-08   4.999d+00   :              :              :              :     .
```

Figure C-11.   SPICE Plot Section 1 Input 010 Two Node
               Precharge with Gate Widths x3

Ø   CMOS/SOS BITSLICE SECTION 1 PRERCHARGED AT TWO NODES - OUTPUT Ø1Ø

Ø****   INPUT LISTING   TEMPERATURE =   27.ØØØ DEG C

Ø**

```
 .WIDTH OUT=8Ø
 .OPTIONS ITL1=5ØØ ITL5=Ø
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
 +LEVEL=1
 VDD 1 Ø DC 5V
 M1  1  3  2  Ø NMOS L=5.ØU W=15.ØU
 M2  1  3  5  Ø NMOS L=5.ØU W=15.ØU
 M3  2  6  1  1 PMOS L=5.ØU W=3Ø.ØU
 M4  5  6  1  1 PMOS L=5.ØU W=3Ø.ØU
 M5  1  8  7  1 PMOS L=5.ØU W=1Ø.ØU
 M6  9  8  7  Ø NMOS L=5.ØU W=3Ø.ØU
 M7  11 1Ø 9  Ø NMOS L=5.ØU W=3Ø.ØU
 M8  1  1Ø 7  1 PMOS L=5.ØU W=1Ø.ØU
 M9  1  7  5  1 PMOS L=5.ØU W=1Ø.ØU
 M1Ø Ø  12 11 Ø NMOS L=5.ØU W=3Ø.ØU
 M11 15 14 Ø  Ø NMOS L=5.ØU W=15.ØU
 M12 15 7  5  Ø NMOS L=5.ØU W=15.ØU
 M13 1  14 5  1 PMOS L=5.ØU W=1Ø.ØU
 M14 1  12 7  1 PMOS L=5.ØU W=1Ø.ØU
 M15 1  12 14 1 PMOS L=5.ØU W=1Ø.ØU
 M16 16 12 14 Ø NMOS L=5.ØU W=3Ø.ØU
 M17 1Ø 17 16 Ø NMOS L=5.ØU W=3Ø.ØU
 M18 1  17 14 1 PMOS L=5.ØU W=1Ø.ØU
 M19 Ø  19 18 Ø NMOS L=5.ØU W=3Ø.ØU
 M2Ø 21 2Ø 1Ø Ø NMOS L=5.ØU W=5.ØU
 M21 1  19 14 1 PMOS L=5.ØU W=1Ø.ØU
 M22 21 22 1Ø 1 FMOS L=5.ØU W=1Ø.ØU
 M23 Ø  1Ø 19 Ø NMOS L=5.ØU W=15.ØU
 M24 1  1Ø 19 1 PMOS L=5.ØU W=3Ø.ØU
 M25 1  19 23 1 PMOS L=5.ØU W=1Ø.ØU
 M26 25 24 Ø  Ø NMOS L=5.ØU W=15.ØU
 M27 25 19 23 Ø NMOS L=5.ØU W=15.ØU
 M28 1  23 2  1 PMOS L=5.ØU W=1Ø.ØU
 M29 1  24 23 1 PMOS L=5.ØU W=1Ø.ØU
 M3Ø 26 23 2  Ø NMOS L=5.ØU W=3Ø.ØU
 M31 Ø  27 12 Ø NMOS L=5.ØU W=15.ØU
 M32 29 28 26 Ø NMOS L=5.ØU W=3Ø.ØU
 M33 1  27 12 1 PMOS L=5.ØU W=3Ø.ØU
 M34 1  28 2  1 PMOS L=5.ØU W=1Ø.ØU
 M35 1  3Ø 23 1 PMOS L=5.ØU W=1Ø.ØU
 M36 31 2Ø 27 Ø NMOS L=5.ØU W=5.ØU
 M37 Ø  27 29 Ø NMOS L=5.ØU W=3Ø.ØU
 M38 32 1Ø Ø  Ø NMOS L=5.ØU W=15.ØU
 M39 32 3Ø 23 Ø NMOS L=5.ØU W=15.ØU
 M4Ø 1  1Ø 23 1 PMOS L=5.ØU W=1Ø.ØU
 M41 31 22 27 1 FMOS L=5.ØU W=1Ø.ØU
 M42 1  27 2  1 PMOS L=5.ØU W=1Ø.ØU
 C43 1  Ø  Ø.1478PF
 C44 27 Ø  Ø.2Ø7PF
 C45 2Ø Ø  Ø.51PF
 C46 Ø  Ø  Ø.1174PF
 C47 1Ø Ø  Ø.297PF
```

```
C48 2 Ø Ø.234PF
C49 28 Ø Ø.111PF
C5Ø 29 Ø Ø.86PF
C51 12 Ø Ø.2Ø2PF
C52 23 Ø Ø.121PF
C53 19 Ø Ø.151PF
C54 14 Ø Ø.171PF
C55 18 Ø Ø.86PF
C56 7 Ø Ø.172PF
C57 5 Ø Ø.234PF
C58 11 Ø Ø.86PF
VAØ 31 Ø PULSE (5V ØV ØNS ØNS ØNS 1ØNS)
VBØ 21 Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VPHI1 2Ø Ø PULSE (5V 5V ØNS ØNS ØNS 1ØNS)
VPHI1BAR 22 Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VSØ 3Ø Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VS1 24 Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VS2 8 Ø PULSE (5V 5V ØNS ØNS ØNS 1ØNS)
VS3 17 Ø PULSE (5V 5V ØNS ØNS ØNS 1ØNS)
VP1 3 Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS)
VP1BAR 6 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
.TRAN Ø.5NS 4ØNS
.PLOT TRAN V(5) V(2) (ØV,5V)
.END
```

CMOS/SOS BITSLICE SECTION 1 PRERCHARGED AT TWO NODES - OUTPUT #1#
                                                           x3
#****   TRANSIENT ANALYSIS   TEMPERATURE =   27.### DEG C

#***

#LEGEND:

*: V(5)
+: V(2)
X
      TIME   V(5)

X(*+)----------- #.   d+##   1.25#d+##   2.5##d+##   3.75#d+## 5.###d+##
    #.   d+## 1.355d-#7 X   .   .   .
    5.###d-1# 1.355d-#7 X   .   .   .
    1.###d-#9 1.355d-#7 X   .   .   .
    1.5##d-#9 1.355d-#7 X   .   .   .
    2.###d-#9 1.355d-#7 X   .   .   .
    2.5##d-#9 1.355d-#7 *   .   .   .
    3.###d-#9 1.355d-#7 *+   .   .   .
    3.5##d-#9 1.356d-#7 * +   .   .   .
    4.###d-#9 1.357d-#7 *   +   *   *   .   .   .
    4.5##d-#9 5.615d-#1 .   .   * + .   .
    5.###d-#9 1.82#d+## .   .   .   *+   .
    5.5##d-#9 2.642d+## .   .   .   *+ .
    6.###d-#9 3.3#2d+## .   .   .   .*+
    6.5##d-#9 3.89#d+## .   .   .   . *
    7.###d-#9 4.1#2d+## .   .   .   X . +
    7.5##d-#9 4.19#d+## .   .   .   . .
    8.###d-#9 4.31#d+## .   .   .   . +
    8.5##d-#9 4.415d+## .   .   .   . +
    9.###d-#9 4.512d+## .   .   .   .+
    9.5##d-#9 4.597d+## .   .   .   .+
    1.###d-#8 4.667d+## .   .   .   .+
    1.#5#d-#0 4.731d+## .   .   .   .+
    1.1##d-#8 4.761d+## .   .   .   .+
    1.15#d-#8 4.822d+## .   .   .   .+
    1.2##d-#8 4.855d+#9 .   .   .   .+
    1.25#d-#8 4.883d+## .   .   .   .+
    1.3##d-#8 4.9#5d+## .   .   .   .+
    1.35#d-#0 4.924d+## .   .   . .+
    1.4##d-#8 4.939d+## .   .   . .+
    1.45#d-#8 4.951d+## .   .   . +
    1.5##d-#8 4.961d+## .   .   .+
    1.55#d-#8 4.968d+## .   .   +
    1.6##d-#8 4.974d+## .   .   .+
    1.65#d-#8 4.979d+## .   .   +
    1.7##d-#9 4.982d+## .   .   .+
    1.75#d-#0 4.972d+## .   .   .+
    1.8##d-#8 4.9#4d+## .   .   .+
    1.#5#d-#9 4.768d+## .   .   .+
    1.9##d-#8 4.545d+## .   .   .+
    1.95#d-#8 4.252d+## .   . .+
    2.###d-#8 3.9#3d+## .   .+
    2.#5#d-#8 3.527d+## .   .+
    2.1##d-#8 3.113d+## .   .+
    2.15#d-#8 2.697d+## .   .+
    2.2##d-#8 2.276d+## .+   .+
    2.25#d-#8 1.865d+## .:+   .+
    2.3##d-#8 1.515d+## .:+   .+
    2.35#d-#8 1.198d+## .:+   .+
    2.4##d-#8 9.316d-#1 .:   .+
    2.45#d-#0 6.966d-#1 .: +
    2.5##d-#8 5.327d-#1 .: +
    2.55#d-#8 3.932d-#1 .:+
    2.6##d-#0 2.863d-#1 .:+
    2.65#d-#8 2.125d-#1 .:+
    2.7##d-#8 1.515d-#1 +:
    2.75#d-#0 1.1#7d-#1 +*
    2.8##d-## 8.#15d-#2 +*
    2.#5#d-#8 5.596d-#2 +*
    2.9##d-#0 4.143d-#2 X
    2.95#d-#8 2.946d-#2 X
    3.###d-## 2.#9#d-#2 X
    3.#5#d-#8 1.526d-#2 X
    3.1##d-## 1.#7#d-#2 X
    3.15#d-## 7.751d-#3 X
    3.2##d-## 5.56#d-#3 X
    3.25#d-## 3.862d-#3 X
    3.3##d-## 2.852d-#3 X
    3.35#d-## 2.#21d-#3 X
    3.4##d-## 1.4#1d-#3 X
    3.45#d-## 1.#43d-#3 X
    3.5##d-## 7.3#9d-#4 X
    3.55#d-## 5.291d-#4 X
    3.6##d-## 3.8##d-#4 X
    3.65#d-## 2.635d-#4 X
    3.7##d-## 1.946d-#4 X
    3.75#d-## 1.379d-#4 X
    3.8##d-#8 9.764d-#5 X
    3.85#d-## 7.123d-#5 X
    3.9##d-## 4.993d-#5 X
    3.95#d-## 3.618d-#5 X
    4.###d-## 2.529d-#5 X

Figure C-12.   SPICE Plot Section 1 Input 101 Two Node
               Precharge with Gate Widths x3
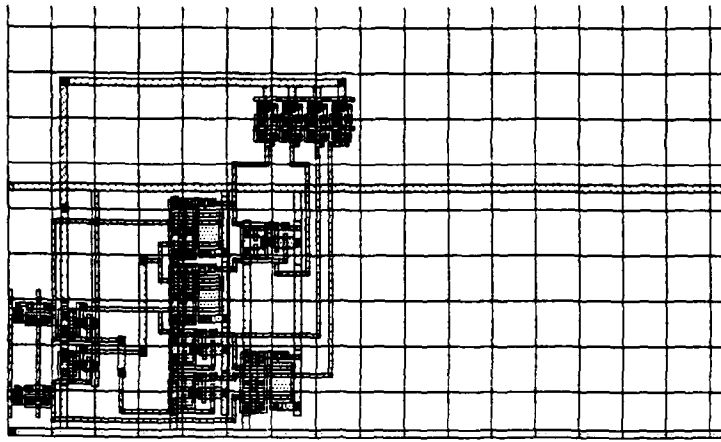
Figure C-13.   CLL Plot Section 1 Four Node Precharge
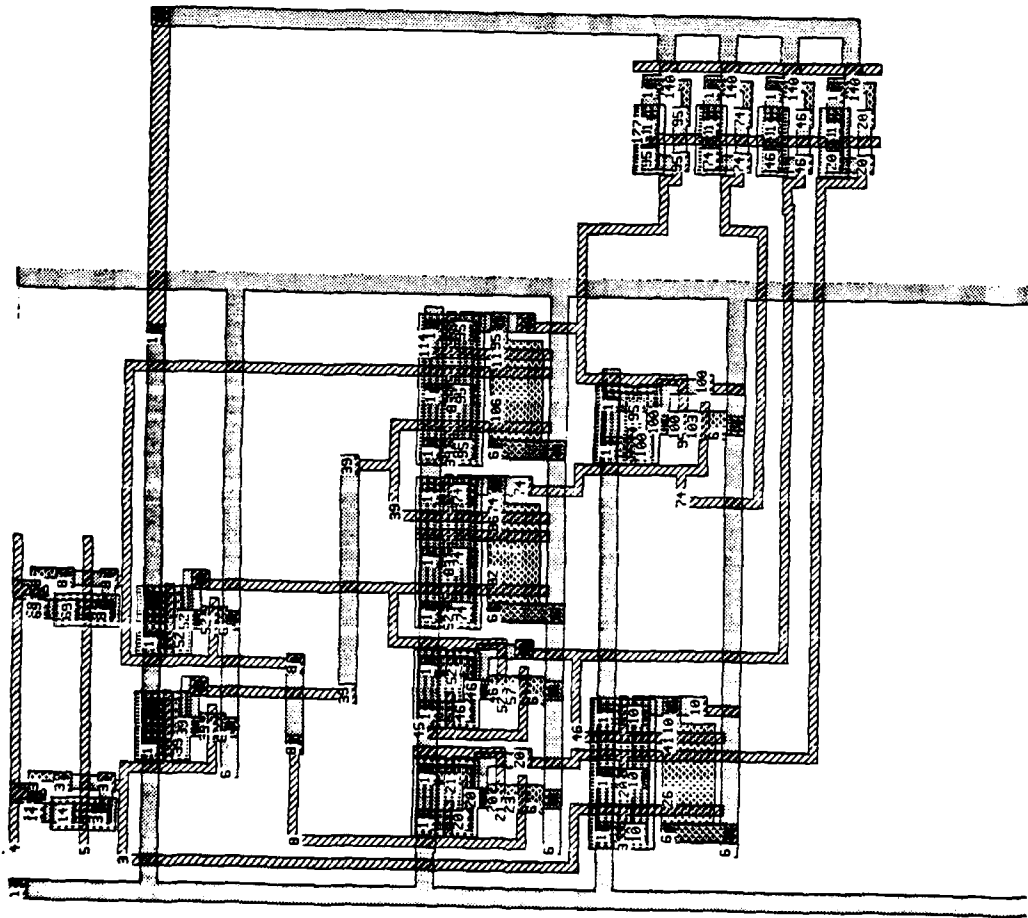
Figure C-14.   Section 1 Four Node Precharge Node Plot
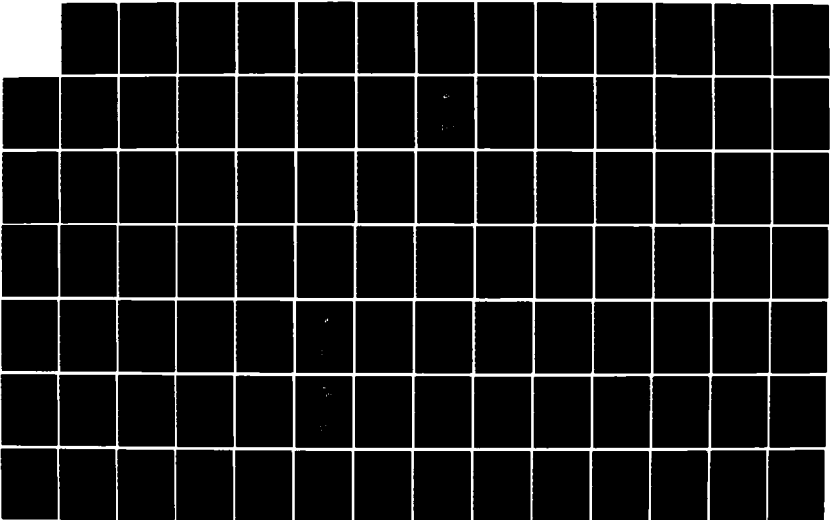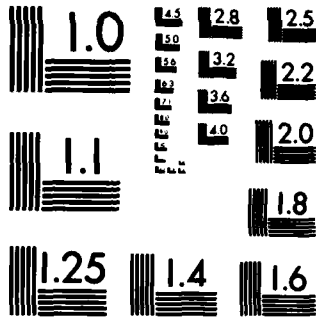
MICROCOPY RESOLUTION TEST CHART

NATIONAL BUREAU OF STANDARDS-1963-A

Table C-3

BITSLICE FIRST SECTION WITH FOUR NODES PRECHARGED - NODE REFERENCE LIST

GND	0
Vdd	1
NMOS	0
PMOS	1
20	2
140	3
1	4
46	5
74	6
95	7
127	8
114	9
113	10
8	11
106	12
100	13
39	14
6	15
103	16
86	17
83	18
82	19
52	20
4	21
69	22
5	23
45	24
57	25
10	26
41	27
3	28
26	29
21	30
14	31
23	32

Ø   CMOS/SOS BITSLICE SECTION 1 WITH FOUR NODES PRECHARGED

Ø****   INPUT LISTING   TEMPERATURE =   27.ØØØ DEG C

Ø***

```
 .WIDTH OUT=8Ø
 .OPTIONS ITL1=5ØØ ITL5=Ø
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
 +LEVEL=1
 VDD 1 Ø DC 5V
 M1  1  3  2  Ø NMOS L=5.ØU W=5.ØU
 M2  1  3  5  Ø NMOS L=5.ØU W=5.ØU
 M3  1  3  6  Ø NMOS L=5.ØU W=5.ØU
 M4  1  3  7  Ø NMOS L=5.ØU W=5.ØU
 M5  2  8  1  1 PMOS L=5.ØU W=1Ø.ØU
 M6  5  8  1  1 PMOS L=5.ØU W=1Ø.ØU
 M7  6  8  1  1 PMOS L=5.ØU W=1Ø.ØU
 M8  7  8  1  1 PMOS L=5.ØU W=1Ø.ØU
 M9  1  9  7  1 PMOS L=5.ØU W=1Ø.ØU
 M1Ø 1Ø 9  7  Ø NMOS L=5.ØU W=3Ø.ØU
 M11 12 11 1Ø Ø NMOS L=5.ØU W=3Ø.ØU
 M12 1 11  7  1 PMOS L=5.ØU W=1Ø.ØU
 M13 1  7 13  1 PMOS L=5.ØU W=1Ø.ØU
 M14 Ø 14 12  Ø NMOS L=5.ØU W=3Ø.ØU
 M15 16 6  Ø  Ø NMOS L=5.ØU W=15.ØU
 M16 16 7 13  Ø NMOS L=5.ØU W=15.ØU
 M17 1  G 13  1 PMOS L=5.ØU W=1Ø.ØU
 M18 1 14  7  1 PMOS L=5.ØU W=1Ø.ØU
 M19 1 14  6  1 PMOS L=5.ØU W=1Ø.ØU
 M2Ø 17 14 6  Ø NMOS L=5.ØU W=3Ø.ØU
 M21 19 18 17 Ø NMOS L=5.ØU W=3Ø.ØU
 M22 1 18  6  1 PMOS L=5.ØU W=1Ø.ØU
 M23 Ø 2Ø 19 Ø NMOS L=5.ØU W=3Ø.ØU
 M24 22 21 11 Ø NMOS L=5.ØU W=5.ØU
 M25 1 2Ø  6  1 PMOS L=5.ØU W=1Ø.ØU
 M26 22 23 11 1 FMOS L=5.ØU W=1Ø.ØU
 M27 Ø 11 2Ø Ø NMOS L=5.ØU W=15.ØU
 M28 1 11 2Ø 1 PMOS L=5.ØU W=3Ø.ØU
 M29 1 2Ø  5  1 PMOS L=5.ØU W=1Ø.ØU
 M3Ø 25 24 Ø Ø NMOS L=5.ØU W=15.ØU
 M31 25 2Ø  5  Ø NMOS L=5.ØU W=15.ØU
 M32 1  5 26  1 PMOS L=5.ØU W=1Ø.ØU
 M33 1 24  5  1 PMOS L=5.ØU W=1Ø.ØU
 M34 27 5 26  Ø NMOS L=5.ØU W=3Ø.ØU
 M35 Ø 23 14 Ø NMOS L=5.ØU W=15.ØU
 M36 2Ø 2 27 Ø NMOS L=5.ØU W=3Ø.ØU
 M37 1 23 14 1 PMOS L=5.ØU W=3Ø.ØU
 M38 1  2 26  1 PMOS L=5.ØU W=1Ø.ØU
 M39 1 3Ø  2  1 PMOS L=5.ØU W=1Ø.ØU
 M4Ø 31 21 28 Ø NMOS L=5.ØU W=5.ØU
 M41 Ø 23 29 Ø NMOS L=5.ØU W=3Ø.ØU
 M42 32 11 Ø Ø NMOS L=5.ØU W=15.ØU
 M43 32 3Ø  2  Ø NMOS L=5.ØU W=15.ØU
 M44 1 11  2  1 PMOS L=5.ØU W=1Ø.ØU
 M45 31 23 28 1 FMOS L=5.ØU W=1Ø.ØU
 M46 1 23 26 1 PMOS L=5.ØU W=1Ø.ØU
 C47 1 Ø Ø.16Ø2PF
```

```
C48 28 Ø Ø.2Ø7PF
C49 21 Ø Ø.51PF
C5Ø Ø Ø Ø.1174PF
C51 11 Ø Ø.297PF
C52 2G Ø Ø.134PF
C53 2 Ø Ø.274PF
C54 29 Ø Ø.86PF
C55 14 Ø Ø.2Ø2PF
C56 5 Ø Ø.283PF
C57 2Ø Ø Ø.151PF
C58 6 Ø Ø.3Ø3PF
C59 19 Ø Ø.86PF
C6Ø 7 Ø Ø.271PF
C61 13 Ø Ø.134PF
C62 12 Ø Ø.86PF
C63 3 Ø Ø.5ØPF
VAØ 31 Ø PULSE (ØV 5V ØNS ØNS ØNS 1ØNS)
VBØ 22 Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VPHI1 21 Ø PULSE (5V 5V ØNS ØNS ØNS 1ØNS)
VPHI1BAR 23 Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VSØ 3Ø Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VS1 24 Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VS2 9 Ø PULSE (5V 5V ØNS ØNS ØNS 1ØNS)
VS3 18 Ø PULSE (5V 5V ØNS ØNS ØNS 1ØNS)
VP1 3 Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS)
VP1BAR 8 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
.TRAN Ø.5NS 4ØNS
.PLOT TRAN V(13) V(26) (ØV,5V)
.END
```

CMOS/SOS BITSLICE SECTION 1 WITH FOUR NODES PRECHARGED X#

#••••   TRANSIENT ANALYSIS   TEMPERATURE -   27.### DEG C

#••

#LEGEND:

 •: V(13)
 +: V(26)
X
    TIME   V(13)

X(•+)------------ #.   d+##   1.25#d+##   2.5##d+##   3.75#d+## 5.###d+##

```
 #.    d+##   5.###d+##                                              X
 5.###d-1#   5.##d+##                                                X
 1.###d-#9   5.###d+##                                               X
 1.5##d-#9   5.###d+##                                               X
 2.###d-#9   5.###d+##                                               X
 2.5##d-#9   5.###d+##                                               X
 3.###d-#9   5.###d+##                                               X
 3.5##d-#9   5.###d+##                                               X
 4.###d-#9   5.###d+##                                               .
 4.5##d-#9   5.###d+##                                              .
 5.###d-#9   5.###d+##                                            .
 5.5##d-#9   4.996d+##                                          .
 6.###d-#9   4.957d+##                                       .
 6.5##d-#9   4.811d+##                                    .
 7.###d-#9   4.524d+##                                 .
 7.5##d-#9   4.157d+##                             .
 8.###d-#9   3.712d+##                         .
 8.5##d-#9   3.197d+##                     .
 9.###d-#9   2.629d+##                  .
 9.5##d-#9   2.#47d+##              .
 1.###d-#8   1.526d+##          .
 1.#5#d-##   1.#38d+##       .
 1.1##d-##   6.816d-#1    .
 1.15#d-##   4.348d-#1   .
 1.2##d-#8   2.632d-#1  .
 1.25#d-#8   1.59#d-#1 .
 1.3##d-#8   9.263d-#2 .
 1.35#d-#8   5.611d-#2 .
 1.4##d-#8   3.167d-#2 .
 1.45#d-#8   1.656d-#2 .
 1.5##d-#8   1.##3d-#2 .
 1.55#d-#8   5.69#d-#3 .
 1.6##d-#8   3.#63d-#3 .
 1.65#d-##   #.441d-#3 .
 1.7##d-#8   2.583d-#2 .
 1.75#d-## 6.522d-#2 .
 1.8##d-##   1.562d-#1 .
 1.85#-1-## 2.876d-#1 .
 1.9##d-##   5.241d-#1 .
 1.95#d-##   #.399d-#1 .
 2.###d-#8   1.222d+## .
 2.#5#d-#8   1.7#6d+## .
 2.1##d-#8   2.21#d+## .
 2.15#d-#8   2.738d+## .
 2.2##d-#8   3.217d+## .
 2.25#d-#8   3.639d+## .
 2.3##d-#8   3.98#d+## .
 2.35#d-#8   4.275d+## .
 2.4##d-#8   4.471d+## .
 2.45#d-#8   4.629d+## .
 2.5##d-#8   4.747d+## .
 2.55#d-#8   4.82#d+## .
 2.6##d-#0   4.879d+## .
 2.65#d-#8   4.917d+## .
 2.7##d-#8   4.943d+## .
 2.75#d-#0   4.963d+## .
 2.8##d-08   4.974d+## .
 2.85#d-#0   4.982d+## .
 2.9##d-#8   4.98#d+## .
 2.95#d-#8   4.992d+## .
 3.###d-#8   4.995d+## .
 3.#5#d-#8   4.996d+## .
 3.1##d-#0   4.997d+## .
 3.15#d-#8   4.998d+## .
 3.2##d-#8   4.999d+## .
 3.25#d-#8   4.999d+## .
 3.3##d-#8   4.999d+## .
 3.35#d-#8   5.###d+## .
 3.4##d-#0   5.###d+## .
 3.45#d-#8   5.###d+## .
 3.5##d-#8   5.###d+## .
 3.55#d-#8   5.###d+## .
 3.6##d-#8   5.###d+## .
 3.65#d-#8   5.###d+## .
 3.7##d-#8   5.###d+## .
 3.75#d-#0   5.###d+## .
 3.8##d-#8   5.###d+## .
 3.85#d-#8   5.###d+## .
 3.9##d-#8   5.###d+## .
 3.95#d-#0   5.###d+## .
 4.###d-#8   5.###d+## .
```

Figure C-15.   SPICE Plot Section 1 Input 010 Four
                 Node Precharge with Basic Gate Widths

```
 .WIDTH OUT=8Ø
 .OPTIONS ITL1=5ØØ ITL5=Ø
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
 +LEVEL=1
 VDD 1 Ø DC 5V
 M1  1  3  2  Ø NMOS L=5.ØU W=5.ØU
 M2  1  3  5  Ø NMOS L=5.ØU W=5.ØU
 M3  1  3  6  Ø NMOS L=5.ØU W=5.ØU
 M4  1  3  7  Ø NMOS L=5.ØU W=5.ØU
 M5  2  8  1  1 PMOS L=5.ØU W=1Ø.ØU
 M6  5  8  1  1 PMOS L=5.ØU W=1Ø.ØU
 M7  6  8  1  1 PMOS L=5.ØU W=1Ø.ØU
 M8  7  8  1  1 PMOS L=5.ØU W=1Ø.ØU
 M9  1  9  7  1 PMOS L=5.ØU W=1Ø.ØU
 M1Ø 1Ø 9  7  Ø NMOS L=5.ØU W=3Ø.ØU
 M11 12 11 1Ø Ø NMOS L=5.ØU W=3Ø.ØU
 M12 1  11 7  1 PMOS L=5.ØU W=1Ø.ØU
 M13 1  7  13 1 PMOS L=5.ØU W=1Ø.ØU
 M14 Ø  14 12 Ø NMOS L=5.ØU W=3Ø.ØU
 M15 16 6  Ø  Ø NMOS L=5.ØU W=15.ØU
 M16 16 7  13 Ø NMOS L=5.ØU W=15.ØU
 M17 1  6  13 1 PMOS L=5.ØU W=1Ø.ØU
 M18 1  14 7  1 PMOS L=5.ØU W=1Ø.ØU
 M19 1  14 6  1 PMOS L=5.ØU W=1Ø.ØU
 M2Ø 17 14 6  Ø NMOS L=5.ØU W=3Ø.ØU
 M21 19 18 17 Ø NMOS L=5.ØU W=3Ø.ØU
 M22 1  13 6  1 PMOS L=5.ØU W=1Ø.ØU
 M23 Ø  2Ø 19 Ø NMOS L=5.ØU W=3Ø.ØU
 M24 22 21 11 Ø NMOS L=5.ØU W=5.ØU
 M25 1  2Ø 6  1 PMOS L=5.ØU W=1Ø.ØU
 M26 22 23 11 1 FMOS L=5.ØU W=1Ø.ØU
 M27 Ø  11 2Ø Ø NMOS L=5.ØU W=15.ØU
 M28 1  11 2Ø 1 PMOS L=5.ØU W=3Ø.ØU
 M29 1  2Ø 5  1 PMOS L=5.ØU W=1Ø.ØU
 M3Ø 25 24 Ø  Ø NMOS L=5.ØU W=15.ØU
 M31 25 2Ø 5  Ø NMOS L=5.ØU W=15.ØU
 M32 1  5  26 1 PMOS L=5.ØU W=1Ø.ØU
 M33 1  24 5  1 PMOS L=5.ØU W=1Ø.ØU
 M34 27 5  26 Ø NMOS L=5.ØU W=3Ø.ØU
 M35 Ø  23 14 Ø NMOS L=5.ØU W=15.ØU
 M36 29 2  27 Ø NMOS L=5.ØU W=3Ø.ØU
 M37 1  23 14 1 PMOS L=5.ØU W=3Ø.ØU
 M38 1  2  26 1 PMOS L=5.ØU W=1Ø.ØU
 M39 1  3Ø 2  1 PMOS L=5.ØU W=1Ø.ØU
 M4Ø 31 21 28 Ø NMOS L=5.ØU W=5.ØU
 M41 Ø  23 29 Ø NMOS L=5.ØU W=3Ø.ØU
 M42 32 11 Ø  Ø NMOS L=5.ØU W=15.ØU
 M43 32 3Ø 2  Ø NMOS L=5.ØU W=15.ØU
 M44 1  11 2  1 PMOS L=5.ØU W=1Ø.ØU
 M45 31 23 28 1 FMOS L=5.ØU W=1Ø.ØU
 M46 1  23 26 1 PMOS L=5.ØU W=1Ø.ØU
 C47 1  Ø  Ø.16Ø2PF
```

```
C48 2C Ø Ø.207PF
C49 21 Ø Ø.51PF
C5Ø Ø Ø Ø.1174PF
C51 11 Ø Ø.297PF
C52 26 Ø Ø.134PF
C53 2 Ø Ø.274PF
C54 29 Ø Ø.86PF
C55 14 Ø Ø.2Ø2PF
C56 5 Ø Ø.283PF
C57 2Ø Ø Ø.151PF
C58 6 Ø Ø.3Ø3PF
C59 19 Ø Ø.86PF
C6Ø 7 Ø Ø.271PF
C61 13 Ø Ø.134PF
C62 12 Ø Ø.86PF
C63 3 Ø Ø.5ØPF
VAØ 31 Ø PULSE (5V ØV ØNS ØNS ØNS 1ØNS)
VBØ 22 Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VPHI1 21 Ø PULSE (5V 5V ØNS ØNS ØNS 1ØNS)
VPHI1BAR 23 Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VSØ 3Ø Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VS1 24 Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VS2 9 Ø PULSE (5V 5V ØNS ØNS ØNS 1ØNS)
VS3 18 Ø PULSE (5V 5V ØNS ØNS ØNS 1ØNS)
VP1 3 Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS)
VP1BAR 8 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
.TRAN Ø.5NS 4ØNS
.PLOT TRAN V(13) V(26) (ØV,5V)
.END
```

```
1••••••••12/#1/84 •••••••• SPICE 2G.1 (150CT8#) •••••••••##:32:#4•••••
#        CMOS/SOS BITSLICE SECTION 1 WITH FOUR NODES PRECHARGED ×|
#••••      TRANSIENT ANALYSIS              TEMPERATURE =  27.### DEG C
#•••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••

#LEGEND:

•: V(13)
+: V(26)
X
    TIME      V(13)

X(•+)------------   #.    d+##     1.25#d+##    2.5##d+##    3.75#d+##  5.###d+##
```

TIME	V(13)	plot
#. d+##	9.#35d-#8	X
5.###d-1#	9.#35d-#8	X
1.###d-#9	9.#35d-#8	X
1.5##d-#9	9.#35d-#8	X
2.###d-#9	9.#35d-#8	X
2.5##d-#9	9.#35d-#8	•+
3.###d-#9	9.#35d-#8	•+
3.5##d-#9	9.#38d-#8	•
4.###d-#9	9.#44d-#8	•
4.5##d-#9	9.#71d-#8	•
5.###d-#9	9.16#d-#8	•
5.5##d-#9	9.345d-#8	•
6.###d-#9	9.621d-#8	•
6.5##d-#9	3.478d-#4	•
7.###d-#9	6.#77d-#3	•
7.5##d-#9	3.257d-#2	•
8.###d-#9	9.636d-#2	•
8.5##d-#9	2.233d-#1	•
9.###d-#9	3.929d-#1	•
9.5##d-#9	6.676d-#1	•
1.###d-#8	1.#29d+##	•
1.#5#d-#8	1.445d+##	•
1.1##d-#8	1.946d+##	•
1.15#d-#8	2.477d+##	•
1.2##d-#8	2.969d+##	•
1.25#d-#8	3.436d+##	•
1.3##d-#8	3.825d+##	•
1.35#d-#8	4.134d+##	•
1.4##d-#8	4.371d+##	•
1.45#d-#8	4.566d+##	•
1.5##d-#8	4.687d+##	•
1.55#d-#8	4.763d+##	•
1.6##d-#8	4.852d+##	•
1.65#d-#8	4.893d+##	•
1.7##d-#9	4.926d+##	•
1.75#d-#8	4.945d+##	•
1.C##d-#8	4.949d+##	•
1.85#d-#8	4.927d+##	•
1.9##d-#8	4.855d+##	•
1.95#d-#8	4.711d+##	•
2.###d-#8	4.469d+##	•
2.#5#d-#8	4.158d+##	•
2.1##d-#8	3.75#d+##	+
2.15#d-#8	3.261d+##	+
2.2##d-#8	2.731d+##	+
2.25#d-#8	2.162d+##	+
2.3##d-#8	1.629d+##	+
2.35#d-#8	1.137d+##	+
2.4##d-#8	7.828d-#1	+
2.45#d-#8	4.897d-#1	+
2.5##d-#8	3.#35d-#1	+
2.55#d-#8	1.842d-#1	+
2.6##d-#8	9.956d-#2	+•
2.65#d-#8	5.9#5d-#2	+•
2.7#7d-#8	3.472d-#2	X
2.75#d-#8	1.863d-#2	X
2.8##d-#8	1.#43d-#2	X
2.85#d-#8	6.149d-#3	X
2.9##d-#8	3.166d-#3	X
2.95#d-#8	1.814d-#3	X
3.###d-#8	9.9#5d-#4	X
3.#5#d-#8	4.952d-#4	X
3.1##d-#8	2.992d-#4	X
3.15#d-#8	1.571d-#4	X
3.2##d-#8	8.3#5d-#5	X
3.25#d-#8	4.769d-#5	X
3.3##d-#8	2.425d-#5	X
3.35#d-#8	1.381d-#5	X
3.4##d-#8	7.56#d-#6	X
3.45#d-#8	3.753d-#6	X
3.5##d-#8	2.293d-#6	X
3.55#d-#8	1.238d-#6	X
3.6##d-#8	6.9#4d-#7	X
3.65#d-#8	4.366d-#7	X
3.7##d-#8	2.645d-#7	X
3.75#d-#8	1.891d-#7	X
3.C##d-#8	1.44#d-#7	X
3.#5#d-#8	1.166d-#7	X
3.9##d-#8	1.#62d-#7	X
3.95#d-#8	9.#55d-#8	X
4.###d-#8	9.453d-#8	X

Figure C-16.   SPICE Plot Section 1 Input 101 Four
                Node Precharge With Basic Widths

C-37

```
.WIDTH OUT=8Ø
.OPTIONS ITL1=5ØØ ITL5=Ø
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
+LEVEL=1
VDD 1 Ø DC 5V
M1  1  3  2  Ø NMOS L=5.ØU W=1Ø.ØU
M2  1  3  5  Ø NMOS L=5.ØU W=1Ø.ØU
M3  1  3  6  Ø NMOS L=5.ØU W=1Ø.ØU
M4  1  3  7  Ø NMOS L=5.ØU W=1Ø.ØU
M5  2  8  1  1 PMOS L=5.ØU W=2Ø.ØU
M6  5  8  1  1 PMOS L=5.ØU W=2Ø.ØU
M7  6  8  1  1 PMOS L=5.ØU W=2Ø.ØU
M8  7  8  1  1 PMOS L=5.ØU W=2Ø.ØU
M9  1  9  7  1 PMOS L=5.ØU W=1Ø.ØU
M1Ø 1Ø 9  7  Ø NMOS L=5.ØU W=3Ø.ØU
M11 12 11 1Ø Ø NMOS L=5.ØU W=3Ø.ØU
M12 1  11 7  1 PMOS L=5.ØU W=1Ø.ØU
M13 1  7  13 1 PMOS L=5.ØU W=1Ø.ØU
M14 Ø  14 12 Ø NMOS L=5.ØU W=3Ø.ØU
M15 16 6  Ø  Ø NMOS L=5.ØU W=15.ØU
M16 16 7  13 Ø NMOS L=5.ØU W=15.ØU
M17 1  6  13 1 PMOS L=5.ØU W=1Ø.ØU
M18 1  14 7  1 PMOS L=5.ØU W=1Ø.ØU
M19 1  14 6  1 PMOS L=5.ØU W=1Ø.ØU
M2Ø 17 14 6  Ø NMOS L=5.ØU W=3Ø.ØU
M21 19 18 17 Ø NMOS L=5.ØU W=3Ø.ØU
M22 1  18 6  1 PMOS L=5.ØU W=1Ø.ØU
M23 Ø  2Ø 19 Ø NMOS L=5.ØU W=3Ø.ØU
M24 22 21 11 Ø NMOS L=5.ØU W=5.ØU
M25 1  2Ø 6  1 PMOS L=5.ØU W=1Ø.ØU
M26 22 23 11 1 FMOS L=5.ØU W=1Ø.ØU
M27 Ø  11 2Ø Ø NMOS L=5.ØU W=15.ØU
M28 1  11 2Ø 1 PMOS L=5.ØU W=3Ø.ØU
M29 1  2Ø 5  1 PMOS L=5.ØU W=1Ø.ØU
M3Ø 25 24 Ø  Ø NMOS L=5.ØU W=15.ØU
M31 25 2Ø 5  Ø NMOS L=5.ØU W=15.ØU
M32 1  5  26 1 PMOS L=5.ØU W=1Ø.ØU
M33 1  24 5  1 PMOS L=5.ØU W=1Ø.ØU
M34 27 5  26 Ø NMOS L=5.ØU W=3Ø.ØU
M35 Ø  28 14 Ø NMOS L=5.ØU W=15.ØU
M36 29 2  27 Ø NMOS L=5.ØU W=3Ø.ØU
M37 1  28 14 1 PMOS L=5.ØU W=3Ø.ØU
M38 1  2  26 1 PMOS L=5.ØU W=1Ø.ØU
M39 1  3Ø 2  1 PMOS L=5.ØU W=1Ø.ØU
M4Ø 31 21 28 Ø NMOS L=5.ØU W=5.ØU
M41 Ø  28 29 Ø NMOS L=5.ØU W=3Ø.ØU
M42 32 11 Ø  Ø NMOS L=5.ØU W=15.ØU
M43 32 3Ø 2  Ø NMOS L=5.ØU W=15.ØU
M44 1  11 2  1 PMOS L=5.ØU W=1Ø.ØU
M45 31 23 28 1 FMOS L=5.ØU W=1Ø.ØU
M4G 1  28 26 1 PMOS L=5.ØU W=1Ø.ØU
C47 1  Ø  Ø.16Ø2PF
```

```
C48 28 Ø Ø.2Ø7PF
C49 21 Ø Ø.51PF
C5Ø Ø Ø Ø.1174PF
C51 11 Ø Ø.297PF
C52 26 Ø Ø.134PF
C53 2 Ø Ø.274PF
C54 29 Ø Ø.36PF
C55 14 Ø Ø.2Ø2PF
C56 5 Ø Ø.283PF
C57 2Ø Ø Ø.151PF
C58 6 Ø Ø.3Ø3PF
C59 19 Ø Ø.86PF
C6Ø 7 Ø Ø.271PF
C61 13 Ø Ø.134PF
C62 12 Ø Ø.86PF
C63 3 Ø Ø.5ØPF
VAØ 31 Ø PULSE (ØV 5V ØNS ØNS ØNS 1ØNS)
VBØ 22 Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VPHI1 21 Ø PULSE (5V 5V ØNS ØNS ØNS 1ØNS)
VPHI1BAR 23 Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VSØ 3Ø Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VS1 24 Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VS2 9 Ø PULSE (5V 5V ØNS ØNS ØNS 1ØNS)
VS3 18 Ø PULSE (5V 5V ØNS ØNS ØNS 1ØNS)
VP1 3 Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS)
VP1BAR 3 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
.TRAN Ø.5NS 4ØNS
.PLOT TRAN V(13) V(26) (ØV,5V)
.END
```

```
0          CMOS/SOS BITSLICE SECTION 1 WITH FOUR NODES PRECHARGED X2

0****       TRANSIENT ANALYSIS                    TEMPERATURE =   27.000 DEG C

0*****************************************************************************

0LEGEND:

 *: V(13)
 +: V(26)
X
      TIME      V(13)

X(*+)----------    0.     d+00      1.250d+00    2.500d+00     3.750d+00  5.000d+00
      0.   d+00   5.000d+00 .                                                     X
      5.000d-10   5.000d+00 .                                                     X
      1.000d-09   5.000d+00 .                                                     X
      1.500d-09   5.000d+00 .                                                     X
      2.000d-09   5.000d+00 .                                                     X
      2.500d-09   5.000d+00 .                                                     X
      3.000d-09   5.000d+00 .                                                     X
      3.500d-09   5.000d+00 .                                                     X
      4.000d-09   5.000d+00 .                                                    .
      4.500d-09   5.000d+00 .                                                   .
      5.000d-09   4.998d+00 .                                                 .
      5.500d-09   4.924d+00 .                                              .
      6.000d-09   4.663d+00 .                                         .
      6.500d-09   4.214d+00 .                                   .    .     .
      7.000d-09   3.683d+00 .                          .
      7.500d-09   2.948d+00 .                  .            .        .
      8.000d-09   2.292d+00 .           .
      8.500d-09   1.687d+00 .      .               .
      9.000d-09   1.166d+00 .   .         .
      9.500d-09   7.662d-01 .  .                .
      1.000d-08   4.768d-01 . ..
      1.050d-08   2.803d-01 . .
      1.100d-08   1.668d-01 .:.
      1.150d-08   9.899d-02 :X          .*
      1.200d-08   5.648d-02 :X
      1.250d-08   3.294d-02 *:
      1.300d-08   1.842d-02 * .
      1.350d-08   1.112d-02 * .
      1.400d-08   5.777d-03 * .
      1.450d-08   3.231d-03 *
      1.500d-08   1.811d-03 *
      1.550d-08   9.483d-04 *
      1.600d-08   5.678d-04 *
      1.650d-08   4.678d-03 *
      1.700d-08   1.219d-02 *
      1.750d-08   5.338d-02 :.
      1.800d-08   1.228d-01 *.
      1.850d-08   2.386d-01 *    .
      1.900d-08   4.518d-01 . *
      1.950d-08   7.187d-01 .  .        .
      2.000d-08   1.186d+00 . .              .
      2.050d-08   1.553d+00 .         .
      2.100d-08   2.045d+00 .                .
      2.150d-08   2.576d+00 .                    .
      2.200d-08   3.062d+00 .                        .
      2.250d-08   3.587d+00 .                           .
      2.300d-08   3.865d+00 .                             .
      2.350d-08   4.189d+00 .                                .
      2.400d-08   4.469d+00 .                                  .
      2.450d-08   4.592d+00 .                                    .
      2.500d-08   4.718d+00 .                                     .
      2.550d-08   4.799d+00 .                                      .
      2.600d-08   4.867d+00 .                                       .
      2.650d-08   4.985d+00 .                                        .
      2.700d-08   4.936d+00 .                                        .
      2.750d-08   4.957d+00 .                                         .
      2.800d-08   4.976d+00 .                                         .
      2.850d-08   4.986d+00 .                                         .
      2.900d-08   4.986d+00 .                                         .
      2.950d-08   4.991d+00 .                                         .
      3.000d-08   4.994d+00 .                                         .
      3.050d-08   4.996d+00 .                                         .
      3.100d-08   4.997d+00 .                                         .
      3.150d-08   4.998d+00 .                                         .
      3.200d-08   4.999d+00 .                                         .
      3.250d-08   4.999d+00 .                                         .
      3.300d-08   4.999d+00 .                                         .
      3.350d-08   5.000d+00 .                                         .
      3.400d-08   5.000d+00 .                                         .
      3.450d-08   5.000d+00 .                                         .
      3.500d-08   5.000d+00 .                                         .
      3.550d-08   5.000d+00 .                                         .
      3.600d-08   5.000d+00 .                                         .
      3.650d-08   5.000d+00 .                                         .
      3.700d-08   5.000d+00 .                                         .
      3.750d-08   5.000d+00 .                                         .
      3.800d-08   5.000d+00 .                                         .
      3.850d-08   5.000d+00 .                                         .
      3.900d-08   5.000d+00 .                                         .
      3.950d-08   5.000d+00 .                                         .
      4.000d-08   5.000d+00 .                                         .
```

Figure C-17.   SPICE Plot Section 1 Input 010 Four
              Node Precharge with Gate Widths x2

```
 .WIDTH OUT=80
 .OPTIONS ITL1=500 ITL5=0
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
 +LEVEL=1
 VDD 1 0 DC 5V
 M1  1 3 2 0 NMOS L=5.0U W=10.0U
 M2  1 3 5 0 NMOS L=5.0U W=10.0U
 M3  1 3 6 0 NMOS L=5.0U W=10.0U
 M4  1 3 7 0 NMOS L=5.0U W=10.0U
 M5  2 8 1 1 PMOS L=5.0U W=20.0U
 M6  5 8 1 1 PMOS L=5.0U W=20.0U
 M7  6 8 1 1 PMOS L=5.0U W=20.0U
 M8  7 8 1 1 PMOS L=5.0U W=20.0U
 M9  1 9 7 1 PMOS L=5.0U W=10.0U
 M10 10 9 7 0 NMOS L=5.0U W=30.0U
 M11 12 11 10 0 NMOS L=5.0U W=30.0U
 M12 1 11 7 1 PMOS L=5.0U W=10.0U
 M13 1 7 13 1 PMOS L=5.0U W=10.0U
 M14 0 14 12 0 NMOS L=5.0U W=30.0U
 M15 16 6 0 0 NMOS L=5.0U W=15.0U
 M16 16 7 13 0 NMOS L=5.0U W=15.0U
 M17 1 6 13 1 PMOS L=5.0U W=10.0U
 M18 1 14 7 1 PMOS L=5.0U W=10.0U
 M19 1 14 6 1 PMOS L=5.0U W=10.0U
 M20 17 14 6 0 NMOS L=5.0U W=30.0U
 M21 19 13 17 0 NMOS L=5.0U W=30.0U
 M22 1 18 6 1 PMOS L=5.0U W=10.0U
 M23 0 20 19 0 NMOS L=5.0U W=30.0U
 M24 22 21 11 0 NMOS L=5.0U W=5.0U
 M25 1 20 6 1 PMOS L=5.0U W=10.0U
 M26 22 23 11 1 PMOS L=5.0U W=10.0U
 M27 0 11 7 0 NMOS L=5.0U W=15.0U
 M28 1 11 20 1 PMOS L=5.0U W=30.0U
 M29 1 20 5 1 PMOS L=5.0U W=10.0U
 M30 25 24 0 0 NMOS L=5.0U W=15.0U
 M31 25 20 5 0 NMOS L=5.0U W=15.0U
 M32 1 5 26 1 PMOS L=5.0U W=10.0U
 M33 1 24 5 1 PMOS L=5.0U W=10.0U
 M34 27 5 26 0 NMOS L=5.0U W=30.0U
 M35 0 23 14 0 NMOS L=5.0U W=15.0U
 M36 20 2 27 0 NMOS L=5.0U W=30.0U
 M37 1 23 14 1 PMOS L=5.0U W=30.0U
 M38 1 2 26 1 PMOS L=5.0U W=10.0U
 M39 1 30 2 1 PMOS L=5.0U W=10.0U
 M40 31 21 28 0 NMOS L=5.0U W=5.0U
 M41 0 23 30 0 NMOS L=5.0U W=30.0U
 M42 32 11 0 0 NMOS L=5.0U W=15.0U
 M43 32 30 2 0 NMOS L=5.0U W=15.0U
 M44 1 11 2 1 PMOS L=5.0U W=10.0U
 M45 31 23 28 1 PMOS L=5.0U W=10.0U
 M46 1 23 26 1 PMOS L=5.0U W=10.0U
 C47 1 0 0.1602PF
```

```
C48 23 0 0.207PF
C49 21 0 0.51PF
C50 0 0 0.1174PF
C51 11 0 0.297PF
C52 26 0 0.134PF
C53 2 0 0.274PF
C54 29 0 0.86PF
C55 14 0 0.202PF
C56 5 0 0.283PF
C57 20 0 0.151PF
C58 6 0 0.303PF
C59 19 0 0.86PF
C60 7 0 0.271PF
C61 13 0 0.134PF
C62 12 0 0.86PF
C63 3 0 0.50PF
VA0 31 0 PULSE (5V 0V 0NS 0NS 0NS 10NS)
VB0 22 0 PULSE (0V 0V 0NS 0NS 0NS 10NS)
VPHI1 21 0 PULSE (5V 5V 0NS 0NS 0NS 10NS)
VPHI1BAR 23 0 PULSE (0V 0V 0NS 0NS 0NS 10NS)
VS0 30 0 PULSE (0V 0V 0NS 0NS 0NS 10NS)
VS1 24 0 PULSE (0V 0V 0NS 0NS 0NS 10NS)
VS2 9 0 PULSE (5V 5V 0NS 0NS 0NS 10NS)
VS3 18 0 PULSE (5V 5V 0NS 0NS 0NS 10NS)
VP1 3 0 PULSE (0V 5V 4NS 0NS 0NS 2NS)
VP1BAR 8 0 PULSE (5V 0V 4NS 0NS 0NS 2NS)
.TRAN 0.5NS 40NS
.PLOT TRAN V(13) V(26) (0V,5V)
.END
```
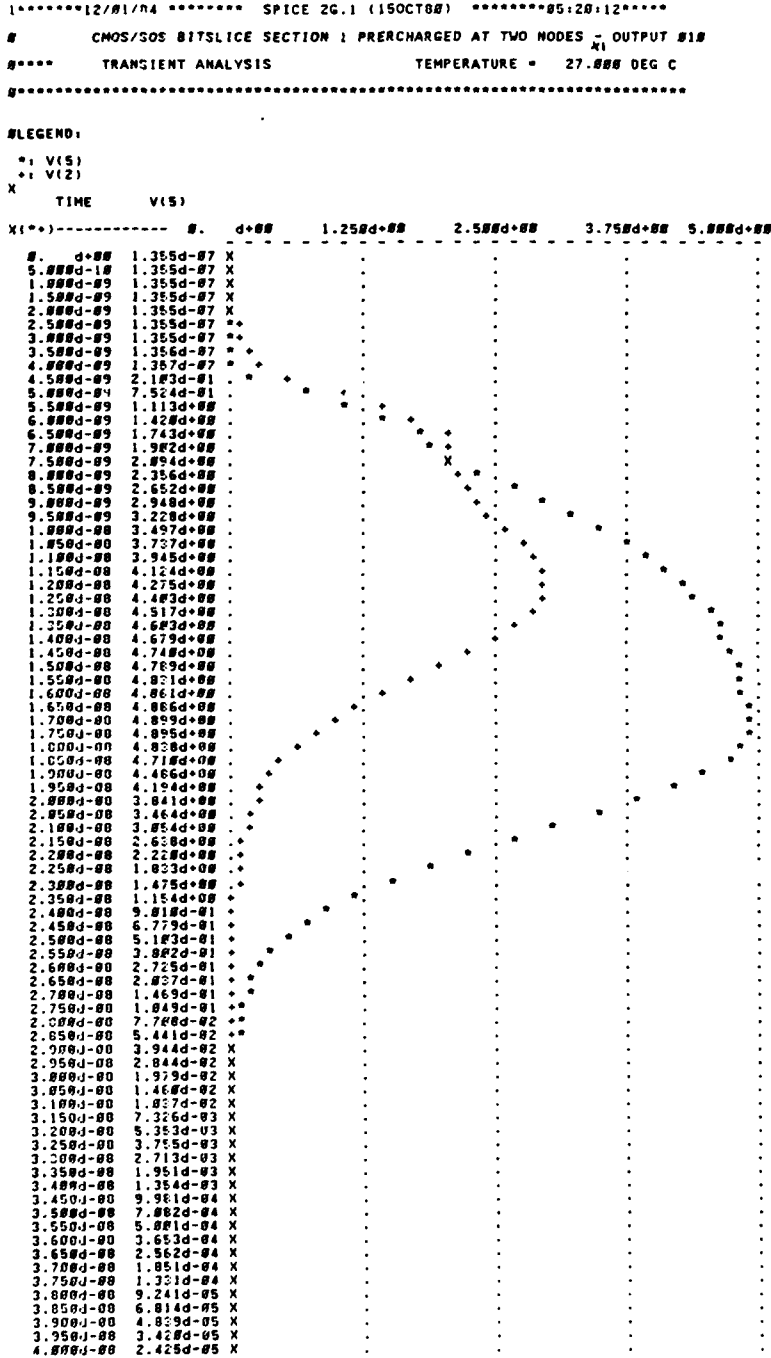
```
1********12/01/84 ********  SPICE 2G.1 (15OCT80)  *********05:46:23*****
0          CMOS/SOS BITSLICE SECTION 1 WITH FOUR NODES PRECHARGED x2
0****      TRANSIENT ANALYSIS                TEMPERATURE =  27.000 DEG C
0*******************************************************************************

0LEGEND:

 *: V(13)
 +: V(26)
X
     TIME      V(13)

X(*+)------------  0.    d+00     1.250d+00     2.500d+00     3.750d+00 5.000d+00
 0.    d+00  9.035d-08 X
 5.000d-10  9.035d-08 X
 1.000d-09  9.035d-08 X
 1.500d-09  9.035d-08 X
 2.000d-09  9.035d-08 X
 2.500d-09  9.035d-08 *.
 3.000d-09  9.035d-08 *
 3.500d-09  9.038d-08 *
 4.000d-09  9.044d-08 *
 4.500d-09  9.078d-08 *
 5.000d-09  9.149d-08 *
 5.500d-09  9.300d-08 *
 6.000d-09  9.514d-08 *
 6.500d-09  9.774d-08 *
 7.000d-09  8.300d-04 *
 7.500d-09  1.319d-02 *
 8.000d-09  5.397d-02 .*
 8.500d-09  1.453d-01 .* .
 9.000d-09  2.743d-01 .    *
 9.500d-09  4.903d-01 .        *
 1.000d-08  7.977d-01 .            *
 1.050d-08  1.160d+00 .               *
 1.100d-08  1.624d+00 .                    *
 1.150d-08  2.141d+00 .                        *
 1.200d-08  2.669d+00 .                            *
 1.250d-08  3.154d+00 .                                *
 1.300d-08  3.597d+00 .                                    *
 1.350d-08  3.926d+00 .                                       *
 1.400d-08  4.229d+00 .                                         *
 1.450d-08  4.480d+00 .                                          *
 1.500d-08  4.685d+00 .                                            *
 1.550d-08  4.731d+00 .                                             *
 1.600d-08  4.847d+00 .                                              *
 1.650d-08  4.864d+00 .                                              *
 1.700d-08  4.905d+00 .                                             *
 1.750d-08  4.926d+00 .                                             *
 1.800d-08  4.937d+00 .                                            *
 1.850d-08  4.917d+00 .                                           *
 1.900d-08  4.843d+00 .+                                        *
 1.950d-08  4.692d+00 .+                                     *
 2.000d-08  4.454d+00 .+                                 *
 2.050d-08  4.149d+00 .+                              *
 2.100d-08  3.728d+00 .+                          *
 2.150d-08  3.247d+00 .+                      *
 2.200d-08  2.780d+00 +                    *
 2.250d-08  2.143d+00 +                 *

 2.300d-08  1.594d+00 +             *
 2.350d-08  1.137d+00 +          *
 2.400d-08  7.648d-01 +      *
 2.450d-08  4.789d-01 +    *
 2.500d-08  3.037d-01 + *
 2.550d-08  1.744d-01 +*
 2.600d-08  1.023d-01 +*
 2.650d-08  5.832d-02 +*
 2.700d-08  3.330d-02 X
 2.750d-08  1.777d-02 X
 2.800d-08  1.079d-02 X
 2.850d-08  5.866d-03 X
 2.900d-08  3.073d-03 X
 2.950d-08  1.799d-03 X
 3.000d-08  9.229d-04 X
 3.050d-08  5.227d-04 X
 3.100d-08  2.862d-04 X
 3.150d-08  1.428d-04 X
 3.200d-08  8.559d-05 X
 3.250d-08  4.584d-05 X
 3.300d-08  2.355d-05 X
 3.350d-08  1.369d-05 X
 3.400d-08  6.981d-06 X
 3.450d-08  3.967d-06 X
 3.500d-08  2.211d-06 X
 3.550d-08  1.132d-06 X
 3.600d-08  7.126d-07 X
 3.650d-08  4.158d-07 X
 3.700d-08  2.596d-07 X
 3.750d-08  1.883d-07 X
 3.800d-08  1.398d-07 X
 3.850d-08  1.182d-07 X
 3.900d-08  1.056d-07 X
 3.950d-08  9.783d-08 X
 4.000d-08  9.447d-08 X
```

Figure C-18.   SPICE Plot Section 1 Input 101 Four
                Node Precharge with Widths x2

C-43

0   CMOS/SOS BITSLICE SECTION 1 WITH FOUR NODES PRECHARGED

0****   INPUT LISTING   TEMPERATURE =   27.000

0**

```
.WIDTH OUT=80
.OPTIONS ITL1=500 ITL5=0
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
+LEVEL=1
VDD 1 0 DC 5V
M1  1 3 2 0 NMOS L=5.0U W=15.0U
M2  1 3 5 0 NMOS L=5.0U W=15.0U
M3  1 3 6 0 NMOS L=5.0U W=15.0U
M4  1 3 7 0 NMOS L=5.0U W=15.0U
M5  2 8 1 1 PMOS L=5.0U W=30.0U
M6  5 8 1 1 PMOS L=5.0U W=30.0U
M7  6 8 1 1 PMOS L=5.0U W=30.0U
M8  7 8 1 1 PMOS L=5.0U W=30.0U
M9  1 9 7 1 PMOS L=5.0U W=10.0U
M10 10 9 7 0 NMOS L=5.0U W=30.0U
M11 12 11 10 0 NMOS L=5.0U W=30.0U
M12 1 11 7 1 PMOS L=5.0U W=10.0U
M13 1 7 13 1 PMOS L=5.0U W=10.0U
M14 0 14 12 0 NMOS L=5.0U W=30.0U
M15 16 6 0 0 NMOS L=5.0U W=15.0U
M16 16 7 13 0 NMOS L=5.0U W=15.0U
M17 1 6 13 1 PMOS L=5.0U W=10.0U
M18 1 14 7 1 PMOS L=5.0U W=10.0U
M19 1 14 6 1 PMOS L=5.0U W=10.0U
M20 17 14 6 0 NMOS L=5.0U W=30.0U
M21 19 13 17 0 NMOS L=5.0U W=30.0U
M22 1 18 6 1 PMOS L=5.0U W=10.0U
M23 0 20 19 0 NMOS L=5.0U W=30.0U
M24 22 21 11 0 NMOS L=5.0U W=5.0U
M25 1 20 6 1 PMOS L=5.0U W=10.0U
M26 22 23 11 1 FMOS L=5.0U W=10.0U
M27 0 11 20 0 NMOS L=5.0U W=15.0U
M28 1 11 20 1 PMOS L=5.0U W=30.0U
M29 1 20 5 1 PMOS L=5.0U W=10.0U
M30 25 24 0 0 NMOS L=5.0U W=15.0U
M31 25 20 5 0 NMOS L=5.0U W=15.0U
M32 1 5 26 1 PHOS L=5.0U W=10.0U
M33 1 24 5 1 PMOS L=5.0U W=10.0U
M34 27 5 26 0 NMOS L=5.0U W=30.0U
M35 0 23 14 0 NMOS L=5.0U W=15.0U
M36 29 2 27 0 NMOS L=5.0U W=30.0U
M37 1 28 14 1 PMOS L=5.0U W=30.0U
M38 1 2 26 1 PMOS L=5.0U W=10.0U
M39 1 30 2 1 PMOS L=5.0U W=10.0U
M40 31 21 28 0 NMOS L=5.0U W=5.0U
M41 0 23 29 0 NMOS L=5.0U W=30.0U
M42 32 11 0 0 NMOS L=5.0U W=15.0U
M43 32 30 2 0 NMOS L=5.0U W=15.0U
M44 1 11 2 1 PMOS L=5.0U W=10.0U
M45 31 23 28 1 FMOS L=5.0U W=10.0U
M46 1 23 26 1 PMOS L=5.0U W=10.0U
C47 1 0 0.1602PF
```

```
C48 29 0 0.207PF
C49 21 0 0.51PF
C50 0 0 0.1174PF
C51 11 0 0.297PF
C52 26 0 0.134PF
C53 2 0 0.274PF
C54 29 0 0.86PF
C55 14 0 0.202PF
C56 5 0 0.283PF
C57 20 0 0.151PF
C58 6 0 0.303PF
C59 19 0 0.86PF
C60 7 0 0.271PF
C61 13 0 0.134PF
C62 12 0 0.86PF
C63 3 0 0.50PF
VA0 31 0 PULSE (0V 5V 0NS 0NS 0NS 10NS)
VB0 22 0 PULSE (0V 0V 0NS 0NS 0NS 10NS)
VPHI1 21 0 PULSE (5V 5V 0NS 0NS 0NS 10NS)
VPHI1BAR 23 0 PULSE (0V 0V 0NS 0NS 0NS 10NS)
VS0 30 0 PULSE (0V 0V 0NS 0NS 0NS 10NS)
VS1 24 0 PULSE (0V 0V 0NS 0NS 0NS 10NS)
VS2 9 0 PULSE (5V 5V 0NS 0NS 0NS 10NS)
VS3 18 0 PULSE (5V 5V 0NS 0NS 0NS 10NS)
VP1 3 0 PULSE (0V 5V 4NS 0NS 0NS 2NS)
VP1BAR 8 0 PULSE (5V 0V 4NS 0NS 0NS 2NS)
.TRAN 0.5NS 40NS
.PLOT TRAN V(13) V(26) (0V,5V)
.END
```

```
#LEGEND:
 *: V(13)
 +: V(26)
 X
     TIME      V(13)

X(*+)------------ #.    d+##    1.25#d+##    2.5##d+##    3.75#d+##  5.###d+##
```


Figure C-19. SPICE Plot Section 1 Input 010 Four
Node Precharge with Widths x3

```
 .WIDTH OUT=8Ø
 .OPTIONS ITL1=5ØØ ITL5=Ø
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
 +LEVEL=1
 VDD 1 Ø DC 5V
 M1  1  3  2  Ø NMOS L=5.ØU W=15.ØU
 M2  1  3  5  Ø NMOS L=5.ØU W=15.ØU
 M3  1  3  6  Ø NMOS L=5.ØU W=15.ØU
 M4  1  3  7  Ø NMOS L=5.ØU W=15.ØU
 M5  2  8  1  1 PMOS L=5.ØU W=3Ø.ØU
 M6  5  8  1  1 PMOS L=5.ØU W=3Ø.ØU
 M7  6  8  1  1 PMOS L=5.ØU W=3Ø.ØU
 M8  7  8  1  1 PMOS L=5.ØU W=3Ø.ØU
 M9  1  9  7  1 PMOS L=5.ØU W=1Ø.ØU
 M1Ø 1Ø 9  7  Ø NMOS L=5.ØU W=3Ø.ØU
 M11 12 11 1Ø Ø NMOS L=5.ØU W=3Ø.ØU
 M12 1 11  7  1 PMOS L=5.ØU W=1Ø.ØU
 M13 1  7 13  1 PMOS L=5.ØU W=1Ø.ØU
 M14 Ø 14 12  Ø NMOS L=5.ØU W=3Ø.ØU
 M15 16 6  Ø  Ø NMOS L=5.ØU W=15.ØU
 M16 16 7 13  Ø NMOS L=5.ØU W=15.ØU
 M17 1  6 13  1 PMOS L=5.ØU W=1Ø.ØU
 M18 1 14  7  1 PMOS L=5.ØU W=1Ø.ØU
 M19 1 14  6  1 PMOS L=5.ØU W=1Ø.ØU
 M2Ø 17 14 6  Ø NMOS L=5.ØU W=3Ø.ØU
 M21 19 1Ø 17 Ø NMOS L=5.ØU W=3Ø.ØU
 M22 1 18  6  1 PMOS L=5.ØU W=1Ø.ØU
 M23 Ø 2Ø 19  Ø NMOS L=5.ØU W=3Ø.ØU
 M24 22 21 11 Ø NMOS L=5.ØU W=5.ØU
 M25 1 2Ø  6  1 PMOS L=5.ØU W=1Ø.ØU
 M26 22 23 11 1 PMOS L=5.ØU W=1Ø.ØU
 M27 Ø 11 2Ø  Ø NMOS L=5.ØU W=15.ØU
 M28 1 11 2Ø  1 PMOS L=5.ØU W=3Ø.ØU
 M29 1 2Ø  5  1 PMOS L=5.ØU W=1Ø.ØU
 M3Ø 25 24 Ø  Ø NMOS L=5.ØU W=15.ØU
 M31 25 2Ø 5  Ø NMOS L=5.ØU W=15.ØU
 M32 1  5 26  1 PMOS L=5.ØU W=1Ø.ØU
 M33 1 24  5  1 PMOS L=5.ØU W=1Ø.ØU
 M34 27 5 26  Ø NMOS L=5.ØU W=3Ø.ØU
 M35 Ø 28 14  Ø NMOS L=5.ØU W=15.ØU
 M36 29 2 27  Ø NMOS L=5.ØU W=3Ø.ØU
 M37 1 28 14  1 PMOS L=5.ØU W=3Ø.ØU
 M38 1  2 26  1 PMOS L=5.ØU W=1Ø.ØU
 M39 1 3Ø  2  1 PMOS L=5.ØU W=1Ø.ØU
 M4Ø 31 21 2Ø Ø NMOS L=5.ØU W=5.ØU
 M41 Ø 28 29  Ø NMOS L=5.ØU W=3Ø.ØU
 M42 32 11 Ø  Ø NMOS L=5.ØU W=15.ØU
 M43 32 3Ø  2  Ø NMOS L=5.ØU W=15.ØU
 M44 1 11  2  1 PMOS L=5.ØU W=1Ø.ØU
 M45 31 23 28 1 PMOS L=5.ØU W=1Ø.ØU
 M46 1 28 26  1 PMOS L=5.ØU W=1Ø.ØU
 C47 1  Ø Ø.16Ø2PF
```

```
C48  28  0  0.207PF
C49  21  0  0.51PF
C50  0  0  0.1174PF
C51  11  0  0.297PF
C52  26  0  0.134PF
C53  2  0  0.274PF
C54  29  0  0.86PF
C55  14  0  0.202PF
C56  5  0  0.283PF
C57  20  0  0.151PF
C58  6  0  0.303PF
C59  19  0  0.86PF
C60  7  0  0.271PF
C61  13  0  0.134PF
C62  12  0  0.86PF
C63  3  0  0.50PF
VA0  31  0  PULSE (5V 0V 0NS 0NS 0NS 10NS)
VB0  22  0  PULSE (0V 0V 0NS 0NS 0NS 10NS)
VPHI1  21  0  PULSE (5V 5V 0NS 0NS 0NS 10NS)
VPHI1BAR  23  0  PULSE (0V 0V 0NS 0NS 0NS 10NS)
VS0  30  0  PULSE (0V 0V 0NS 0NS 0NS 10NS)
VS1  24  0  PULSE (0V 0V 0NS 0NS 0NS 10NS)
VS2  9  0  PULSE (5V 5V 0NS 0NS 0NS 10NS)
VS3  18  0  PULSE (5V 5V 0NS 0NS 0NS 10NS)
VP1  3  0  PULSE (0V 5V 4NS 0NS 0NS 2NS)
VP1BAR  8  0  PULSE (5V 0V 4NS 0NS 0NS 2NS)
.TRAN 0.5NS 40NS
.PLOT TRAN V(13) V(26) (0V,5V)
.END
```

```
1*******12/01/84 ******** SPICE 2G.1 (15OCT80) *********05:54:47*****
#          CMOS/SOS BITSLICE SECTION 1 WITH FOUR NODES PRECHARGED  X3
#****      TRANSIENT ANALYSIS                    TEMPERATURE -   27.000 DEG C
#********************************************************************************

#LEGEND:

 *: V(13)
 +: V(26)
 X
    TIME      V(13)

X(*+)------------ #.    d+00     1.250d+00    2.500d+00     3.750d+00  5.000d+00
        #.   d+00   9.035d-00 X
   5.000d-10   9.035d-00 X
   1.000d-09   9.035d-00 X
   1.500d-09   9.035d-00 X
   2.000d-09   9.035d-00 X
   2.500d-09   9.035d-00 X
   3.000d-09   9.035d-00  .
   3.500d-09   9.038d-00  .
   4.000d-09   9.044d-00  .
   4.500d-09   9.069d-00  .
   5.000d-09   9.140d-00   .
   5.500d-09   9.266d-00    .
   6.000d-09   9.437d-00     .
   6.500d-09   9.634d-00   .
   7.000d-09   4.441d-05    .
   7.500d-09   5.658d-03     .
   8.000d-09   3.342d-02      .
   8.500d-09   1.035d-01   .
   9.000d-09   2.086d-01    .
   9.500d-09   3.820d-01     .
   1.000d-08   6.505d-01      .
   1.050d-08   9.712d-01       .
   1.100d-08   1.407d+00        .
   1.150d-08   1.904d+00         .
   1.200d-08   2.431d+00          .
   1.250d-08   2.947d+00           .
   1.300d-08   3.399d+00            .
   1.350d-08   3.781d+00             .
   1.400d-08   4.121d+00              .
   1.450d-08   4.350d+00               .
   1.500d-08   4.541d+00                .
   1.550d-08   4.680d+00               .
   1.600d-08   4.770d+00              .
   1.650d-08   4.841d+00             .
   1.700d-08   4.884d+00            .
   1.750d-08   4.911d+00           .
   1.800d-08   4.927d+00          .
   1.850d-08   4.960d+00         .
   1.900d-08   4.834d+00        .
   1.950d-08   4.681d+00      .
   2.000d-08   4.459d+00     .
   2.050d-08   4.119d+00    .
   2.100d-08   3.789d+00   .
   2.150d-08   3.238d+00  .
   2.200d-08   2.683d+00 .
   2.250d-08   2.128d+00 .
   2.300d-08   1.583d+00 .
   2.350d-08   1.133d+00 .
   2.400d-08   7.382d-01 .
   2.450d-08   4.837d-01 .
   2.500d-08   2.965d-01 .
   2.550d-08   1.660d-01 .
   2.600d-08   1.039d-01 .
   2.650d-08   5.638d-02  .
   2.700d-08   3.094d-02 X
   2.750d-08   1.848d-02 X
   2.000d-08   1.055d-02 X
   2.860d-08   6.315d-03 X
   2.900d-08   3.230d-03 X
   2.950d-08   1.711d-03 X
   3.000d-08   9.100d-04 X
   3.050d-08   5.270d-04 X
   3.100d-08   2.679d-04 X
   3.150d-08   1.527d-04 X
   3.200d-08   8.344d-05 X
   3.250d-08   4.111d-05 X
   3.300d-08   2.461d-05 X
   3.350d-08   1.300d-05 X
   3.400d-08   6.892d-06 X
   3.450d-08   3.997d-06 X
   3.500d-08   2.057d-06 X
   3.550d-08   1.206d-06 X
   3.600d-08   6.961d-07 X
   3.650d-08   3.868d-07 X
   3.700d-08   2.687d-07 X
   3.750d-08   1.831d-07 X
   3.800d-08   1.392d-07 X
   3.850d-08   1.184d-07 X
   3.900d-08   1.045d-07 X
   3.950d-08   9.838d-08 X
   4.000d-08   9.439d-08 X
```

Figure C-20.   SPICE Plot Section 1 Input 101 Four
              Node Precharge with Widths x3

C-49
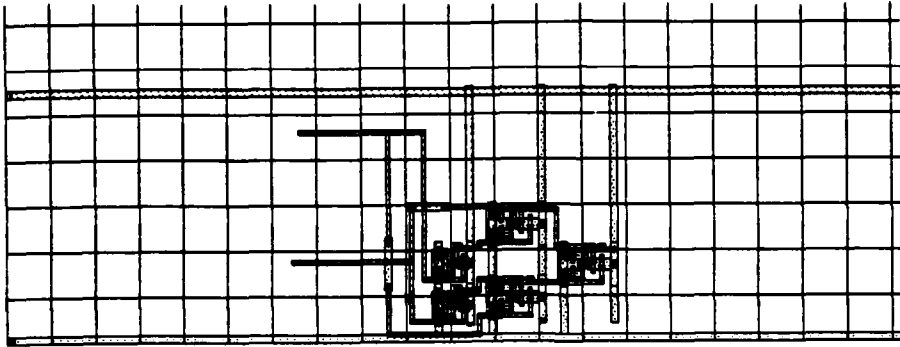
Figure C-21.   Basic Section 2 CLL Plot.
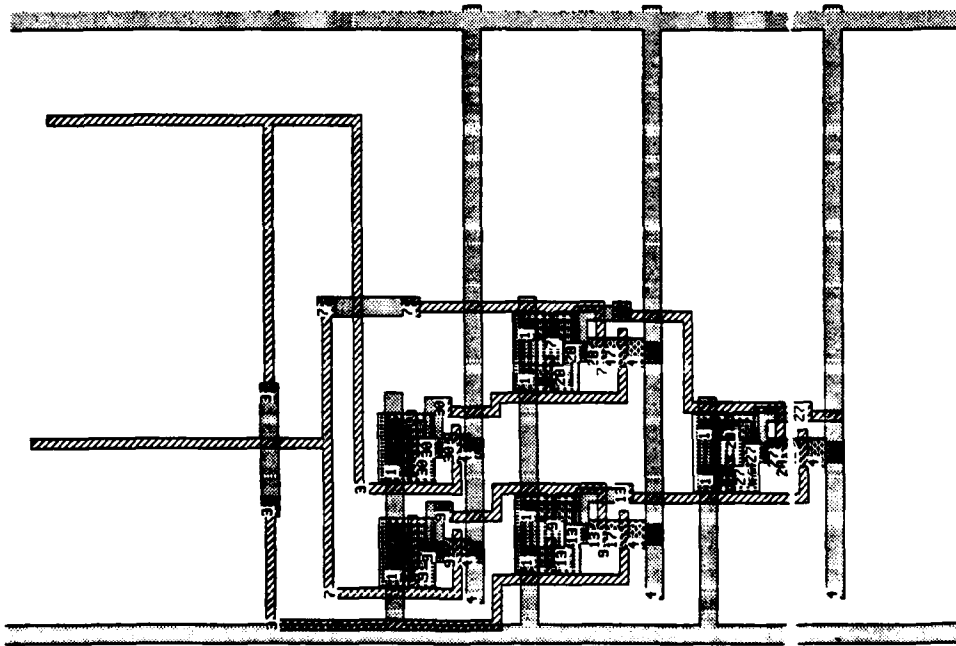
Figure C-22.   Basic Section 2 Node Plot.

Table C-4

BITSLICE BASIC SECTION 2 NODE REFERENCE LIST

GND	0
Vdd	1
NMOS	0
PMOS	1
28	2
7	3
1	4
4	5
30	6
47	7
27	8
3	9
13	10
32	11
9	12
17	13

```
 .WIDTH OUT=80
 .OPTIONS ITL1=500 ITL5=0
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
 +LEVEL=1
 VDD 1 0 DC 5V
 M1  1  3  2  1 PMOS L=5.0U W=10.0U
 M2  7  6  0  0 NMOS L=5.0U W=15.0U
 M3  7  3  2  0 NMOS L=5.0U W=15.0U
 M4  1  6  2  1 PMOS L=5.0U W=10.0U
 M5  1  2  8  1 PMOS L=5.0U W=10.0U
 M6  0  9  6  0 NMOS L=5.0U W=15.0U
 M7  11 10  0  0 NMOS L=5.0U W=15.0U
 M8  11  2  8  0 NMOS L=5.0U W=15.0U
 M9  1  9  6  1 PMOS L=5.0U W=30.0U
 M10 1 10  8  1 PMOS L=5.0U W=10.0U
 M11 1 12 10  1 PMOS L=5.0U W=10.0U
 M12 13  9  0  0 NMOS L=5.0U W=15.0U
 M13 13 12 10  0 NMOS L=5.0U W=15.0U
 M14 1  9 10  1 PMOS L=5.0U W=10.0U
 M15 0  3 12  0 NMOS L=5.0U W=15.0U
 M16 1  3 12  1 PMOS L=5.0U W=30.0U
 C17 1  0  0.877PF
 C18 9  0  0.279PF
 C19 0  0  0.951PF
 C20 3  0  0.183PF
 C21 12 0  0.100PF
 C22 10 0  0.116PF
 C23 8  0  0.134PF
 C24 2  0  0.125PF
 C25 6  0  0.101PF
 VIN1 3 0 PULSE (5V 5V 5NS 0NS 0NS 10NS)
 VIN2 9 0 PULSE (0V 5V 5NS 0NS 0NS 10NS)
 .TRAN 0.5NS 40NS
 .PLOT TRAN V(3) (0V,5V)
 .END
```

```
#        CMOS/SOS BASIC BITSLICE SECTION 2 TRANSIENT ANALYSIS

#••••     TRANSIENT ANALYSIS              TEMPERATURE =   27.### DEG C
#••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••

X
    TIME        V(8)

X                    #.     d+##      1.25#d+##      2.5##d+##      3.75#d+##   5.###d+##
    #.    d+##    5.###d+##  .                                                         •
    5.###d-1#    5.###d+##  .                                                         •
    1.###d #9    5.###d+##  .                                                         •
    1.5##d-#9    5.###d+##  .                                                         •
    2.###d-#9    5.###d+##  .                                                         •
    2.5##d-#9    5.###d+##  .                                                         •
    3.###d-#9    5.###d+##  .                                                         •
    3.5##d-#9    5.###d+##  .                                                         •
    4.###d-#9    5.###d+##  .                                                         •
    4.5##d-#9    5.###d+##  .                                                         •
    5.###d-#9    5.###d+##  .                                                         •
    5.5##d-#9    5.###d+##  .                                                         •
    6.###d-#9    5.###d+##  .                                                         •
    6.5##d-99    5.###d+##  .                                                         •
    7.###d-#9    4.996d+##  .                                                         •
    7.5##d-#9    4.937d+##  .                                                       •
    8.###d-#9    4.768d+##  .                                                     •
    8.5##d-#9    4.438d+##  .                                                 •
    9.###d-#9    4.##3d+##  .                                             •
    9.5##d-#9    3.428d+##  .                                         •
    1.###d-#8    2.81#d+##  .                                     •
    1.#5#d-#8    2.145d+##  .                                •
    1.1##d-#8    1.547d+##  .                           •
    1.15#d-#8    9.961d-#1  .                  •
    1.2##d-#8    6.5#7d-#1  .           •
    1.25#d-#8    3.825d-#1  .     •
    1.3##d-#8    2.136d-#1  . •
    1.35#d-#8    1.238d-#1  .•
    1.4##d-#8    6.7##d-#2  .•
    1.45#d-#8    3.736d-#2  •
    1.5##d-#8    1.966d-#2  •
    1.55#d-#8    1.###d-#2  •
    1.6##d-#8    6.149d-#3  •
    1.65#d-#8    3.495d-#3  •
    1.7##d-#8    2.121d-#3  •
    1.75#d-#8    2.319d-#2  •
    1.8##d-#8    1.1##d-#1  .•
    1.85#d-#8    3.221d-#1  .     •
    1.9##d-#8    6.529d-#1  .          •
    1.95#d-#8    1.168d+##  .                •
    2.###d-#8    1.741d+##  .                      •
    2.#5#d-#8    2.361d+##  .                           •
    2.1##d-#8    2.952d+##  .                                •
    2.15#d-#8    3.465d+##  .                                    •
    2.2##d-#8    3.874d+##  .                                       •
    2.25#d-#8    4.181d+##  .                                         •
    2.3##d-#8    4.436d+##  .                                           •
    2.35#d-#8    4.6##d+##  .                                            •
    2.4##d-#8    4.725d+##  .                                             •
    2.45#d-#8    4.817d+##  .                                              •
    2.5##d-#8    4.871d+##  .                                              •
    2.55#d-#8    4.914d+##  .                                               •
    2.6##d-#8    4.942d+##  .                                               •
    2.65#d-#8    4.96#d+##  .                                               •
    2.7##d-#8    4.974d+##  .                                               •
    2.75#d-#8    4.982d+##  .                                               •
    2.8##d-#8    4.988d+##  .                                               •
    2.85#d-#8    4.992d+##  .                                               •
    2.9##d-#8    4.994d+##  .                                               •
    2.95#d-#8    4.996d+##  .                                               •
    3.###d-#8    4.997d+##  .                                               •
    3.#5#d-#8    4.998d+##  .                                               •
    3.1##d-#8    4.999d+##  .                                               •
    3.15#d-#8    4.999d+##  .                                               •
    3.2##d-#8    4.999d+##  .                                               •
    3.25#d-#8    5.###d+##  .                                               •
    3.3##d-#8    5.###d+##  .                                               •
    3.35#d-#8    5.###d+##  .                                               •
    3.4##d-#8    5.###d+##  .                                               •
    3.45#d-#8    5.###d+##  .                                               •
    3.5##d-#8    5.###d+##  .                                               •
    3.55#d-#8    5.###d+##  .                                               •
    3.6##d-#8    5.###d+##  .                                               •
    3.65#d-#8    5.###d+##  .                                               •
    3.7##d-#8    5.###d+##  .                                               •
    3.75#d-#8    5.###d+##  .                                               •
    3.8##d-#8    5.###d+##  .                                               •
    3.85#d-#8    5.###d+##  .                                               •
    3.9##d-#8    5.###d+##  .                                               •
    3.95#d-#8    5.###d+##  .                                               •
    4.###d-#8    5.###d+##  .                                               •
```

Figure C-23.   SPICE Plot Basic Section 2 Input 010.

```
.WIDTH OUT=80
.OPTIONS ITL1=500 ITL5=0
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
+LEVEL=1
VDD 1 0 DC 5V
M1 1 3 2 1 PMOS L=5.0U W=10.0U
M2 7 6 0 0 NMOS L=5.0U W=15.0U
M3 7 3 2 0 NMOS L=5.0U W=15.0U
M4 1 6 2 1 PMOS L=5.0U W=10.0U
M5 1 2 3 1 PMOS L=5.0U W=10.0U
M6 0 9 6 0 NMOS L=5.0U W=15.0U
M7 11 10 0 0 NMOS L=5.0U W=15.0U
M8 11 2 8 0 NMOS L=5.0U W=15.0U
M9 1 9 6 1 PMOS L=5.0U W=30.0U
M10 1 10 8 1 PMOS L=5.0U W=10.0U
M11 1 12 10 1 PMOS L=5.0U W=10.0U
M12 13 9 0 0 NMOS L=5.0U W=15.0U
M13 13 12 10 0 NMOS L=5.0U W=15.0U
M14 1 9 10 1 PMOS L=5.0U W=10.0U
M15 0 3 12 0 NMOS L=5.0U W=15.0U
M16 1 3 12 1 PMOS L=5.0U W=30.0U
C17 1 0 0.877PF
C18 9 0 0.279PF
C19 0 0 0.951PF
C20 3 0 0.183PF
C21 12 0 0.100?F
C22 10 0 0.116PF
C23 8 0 0.134PF
C24 2 0 0.125PF
C25 6 0 0.101PF
VIN1 3 0 PULSE (5V 5V 5NS 0NS 0NS 10NS)
VIN2 9 0 PULSE (5V 0V 5NS 0NS 0NS 10NS)
.TRAN 0.5NS 40NS
.PLOT TRAN V(8) (0V,5V)
.END
```

```
#       CMOS/SOS BASIC BITSLICE SECTION 2 TRANSIENT ANALYSIS

#••••    TRANSIENT ANALYSIS                TEMPERATURE =  27.### DEG C

#•••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••


X
     TIME      V(8)

X                  #.      d+##      1.25#d+##    2.5##d+##    3.75#d+## 5.###d+##

   #.  d+##   9.#35d-#8 •
 5.###d-1#   9.#35d-#8 •
 1.###d-#9   9.#35d-#8 •
 1.5##d-#9   9.#25d-#8 •
 2.###d-#9   9.#35d-#8 •
 2.5##d-#9   9.#35d-#8 •
 3.###d-#9   9.#35d-#8 •
 3.5##d-#9   9.#35d-#8 •
 4.###d-#9   9.#35d-#8 •
 4.5##d-#9   9.#35d-#8 •
 5.###d-#9   9.#35d-#8 •
 5.5##d-#9   9.#35d-#8 •
 6.###d-#9   9.#65d-#8 •
 6.5##d-#9   6.#81d-#5 •
 7.###d-#9   2.151d-#2 •
 7.5##d-#9   1.#63d-#1  .•
 8.###d-#9   3.2#2d-#1      .•
 8.5##d-#9   6.526d-#1          .•
 9.###d-#9   1.165d+##             .•
 9.5##d-#9   1.738d+##                  •
 1.###d-#8   2.358d+##                      •
 1.#5#d-#8   2.95#d+##                         •
 1.1##d-#8   3.464d+##                            •
 1.15#d-#8   3.873d+##                               •
 1.2##d-#8   4.16#d+##                                •
 1.25#d-#8   4.435d+##                                  •
 1.3##d-#8   4.6##d+##                                    •
 1.35#d-#8   4.724d+##                                     •
 1.4##d-#8   4.818d+##                                      •
 1.45#d-#8   4.871d+##                                       •
 1.5##d-#8   4.914d+##                                       •
 1.55#d-#8   4.943d+##                                       .•
 1.6##d-#8   4.961d+##                                       •
 1.65#d-#8   4.973d+##                                       •
 1.7##d-#8   4.981d+##                                      •
 1.75#d-#8   4.983d+##                                     •
 1.8##d-#8   4.927d+##                                    •
 1.85#d-#8   4.757d+##                                  •
 1.9##d-#8   4.427d+##                                •
 1.#5#d-#8   3.994d+##                             •
 2.###d-#8   3.418d+##                         •
 2.#5#d-#8   2.8##d+##                      •
 2.1##d-#8   2.135d+##                  •
 2.15#d-#8   1.539d+##              •
 2.2##d-#8   9.91#d-#1          •
 2.25#d-#8   6.46#d-#1       •
 2.3##d-#8   3.8#1d-#1    •
 2.35#d-#8   2.115d-#1  .•
 2.4##d-#8   1.22#d-#1 .•
 2.45#d-#8   6.651d-#2 •
 2.5##d-#8   3.711d-#2 •
 2.55#d-#8   1.981d-#2 •
 2.6##d-#8   1.159d-#2 •
 2.65#d-#8   6.31#d-#3 •
 2.7##d-#8   3.#94d-#3 •
 2.75#d-#8   1.872d-#3 •
 2.8##d-#8   9.644d-#4 •
 2.85#d-#8   5.173d-#4 •
 2.9##d-#8   2.921d-#4 •
 2.95#d-#8   1.457d-#4 •
 3.###d-#8   8.386d-#5 •
 3.#5#d-#8   4.49#d-#5 •
 3.1##d-#8   2.2#3d-#5 •
 3.15#d-#8   1.336d-#5 •
 3.2##d-#8   6.922d-#6 •
 3.25#d-#8   3.754d-#6 •
 3.3##d-#8   2.158d-#6 •
 3.35#d-#8   1.121d-#6 •
 3.4##d-#8   6.8#8d-#7 •
 3.45#d-#8   4.#85d-#7 •
 3.5##d-#8   2.459d-#7 •
 3.55#d-#8   1.#44d-#7 •
 3.6##d-#8   1.388d-#7 •
 3.65#d-#8   1.163d-#7 •
 3.7##d-#8   1.#5#d-#7 •
 3.75#d-#8   9.766d-#8 •
 3.8##d-#8   9.456d-#8 •
 3.85#d-#8   9.2##d-#8 •
 3.9##d-#8   9.145d-#8 •
 3.95#d-#8   9.1#2d-#8 •
 4.###d-#8   9.#67d-#8 •
```

Figure C-24.   SPICE Plot Basic Section 2 Input 101.

Figure C-25.   Section 2 One Node Precharge CLL Plot
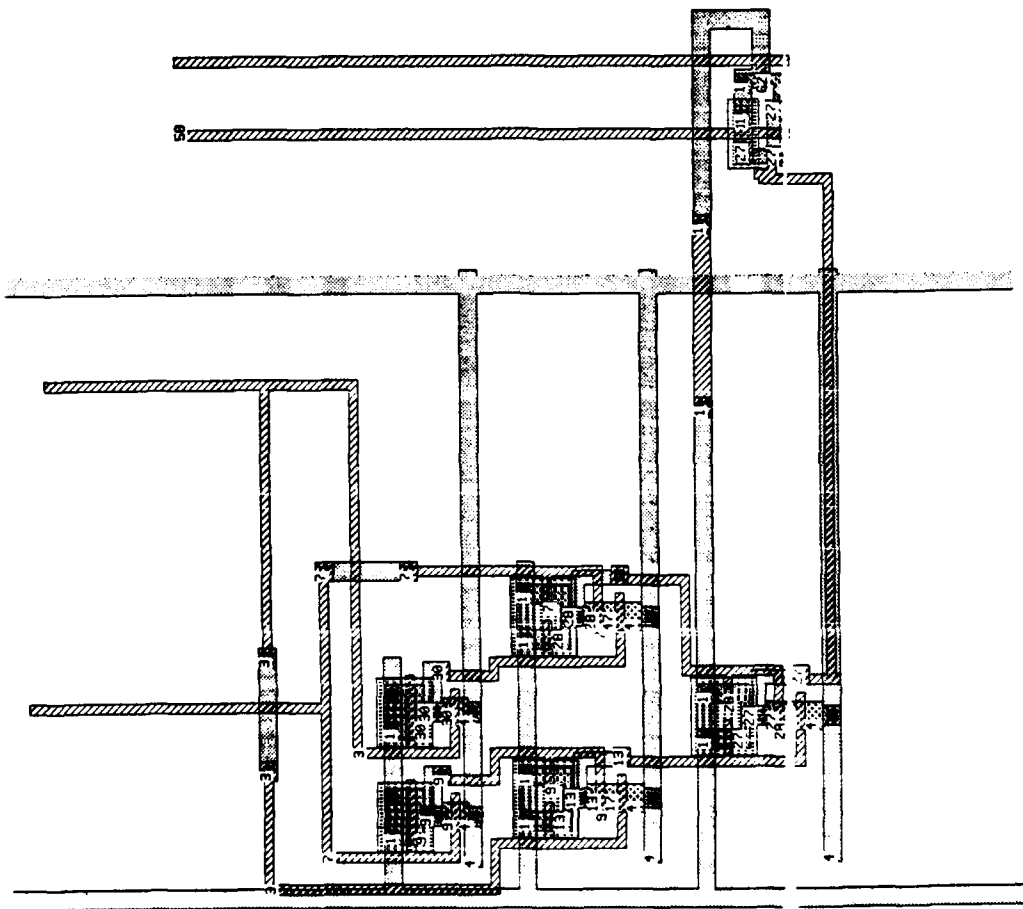
Figure C-26.   Section 2 One Node Precharge Node Plot.

Table C-5

BITSLICE SECTION 2 NODE REFERENCE LIST - ONE NODE PRECHARGE

```
GND    Ø
Vdd    1
NMOS   Ø
PMOS   1
27     2
62     3
1      4
58     5
28     6
7      7
4      8
3Ø     9
47     1Ø
3      11
13     12
32     13
9      14
17     15
```

Ø   CMOS/SOS BITSLICE SECTION 2 PRECHARGED AT ONE NODE

Ø****   INPUT LISTING   TEMPERATURE =   27.ØØØ DEG C

Ø***

```
.WIDTH OUT=8Ø
.OPTIONS ITL1=5ØØ ITL5=Ø
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
+LEVEL=1
VDD 1 Ø DC 5V
M1  1  3  2  Ø NMOS L=5.ØU W=5.ØU
M2  2  5  1  1 PMOS L=5.ØU W=1Ø.ØU
M3  1  7  6  1 PMOS L=5.ØU W=1Ø.ØU
M4  1Ø 9  Ø  Ø NMOS L=5.ØU W=15.ØU
M5  1Ø 7  6  Ø NMOS L=5.ØU W=15.ØU
M6  1  9  6  1 PMOS L=5.ØU W=1Ø.ØU
M7  1  6  2  1 PMOS L=5.ØU W=1Ø.ØU
M8  Ø  11 9  Ø NMOS L=5.ØU W=15.ØU
M9  13 12 Ø  Ø NMOS L=5.ØU W=15.ØU
M10 13 5  2  Ø NMOS L=5.ØU W=15.ØU
M11 1  11 9  1 PMOS L=5.ØU W=3Ø.ØU
M12 1  12 2  1 PMOS L=5.ØU W=1Ø.ØU
M13 1  14 12 1 PMOS L=5.ØU W=1Ø.ØU
M14 15 11 Ø  Ø NMOS L=5.ØU W=15.ØU
M15 15 14 12 Ø NMOS L=5.ØU W=15.ØU
M16 1  11 12 1 PMOS L=5.ØU W=1Ø.ØU
M17 Ø  7  14 Ø NMOS L=5.ØU W=15.ØU
M18 1  7  14 1 PMOS L=5.ØU W=3Ø.ØU
C19 1  Ø  Ø.1Ø74PF
C2Ø 11 Ø  Ø.279PF
C21 Ø  Ø  Ø.951PF
C22 7  Ø  Ø.183PF
C23 14 Ø  Ø.1ØØPF
C24 12 Ø  Ø.116PF
C25 2  Ø  Ø.234PF
C26 6  Ø  Ø.125PF
C27 9  Ø  Ø.1Ø1PF
C28 5  Ø  Ø.1Ø3PF
C29 3  Ø  Ø.1Ø3PF
VIN1 11 Ø PULSE (5V 5V 5NS ØNS ØNS 1ØNS)
VIN2 7 Ø PULSE (ØV 5V 5NS ØNS ØNS 1ØNS)
VP1 3 Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS)
VP1BAR 5 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
.TRAN Ø.5NS 4ØNS
.PLOT TRAN V(2) (ØV,5V)
.END
```

```
•      CMOS/SOS BITSLICE SECTION 2 PRECHARGED AT ONE NODE  X1

•••••    TRANSIENT ANALYSIS              TEMPERATURE -  27.••• DEG C

•••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••

X
   TIME      V(2)

X                    •.    d+••    1.25•d+••    2.5••d+••    3.75•d+•• 5.•••d+••

•.   d+••   5.•••d+••
5.•••d-1•   5.•••d+••
1.•••d-•9   5.•••d+••
1.5••d-•9   5.•••d+••
2.•••d-•9   5.•••d+••
2.5••d-•9   5.•••d+••
3.•••d-•9   5.•••d+••
3.5••d-•9   5.•••d+••
4.•••d-•9   5.•••d+••
4.5••d-•9   5.•••d+••
5.•••d-•9   5.•••d+••
5.5••d-•9   5.•••d+••
6.•••d-•9   5.•••d+••
6.5••d-•9   5.•••d+••
7.•••d-•9   4.997d+••
7.5••d-•9   4.92•d+••
8.•••d-•9   4.733d+••
8.5••d-•9   4.43•d+••
9.•••d-•9   4.•62d+••
9.5••d-•9   3.65•d+••
1.•••d-•8   3.223d+••
1.•5•d-•8   2.777d+••
1.1••d-•8   2.343d+••
1.15•d-•8   1.916d+••
1.2••d-•8   1.551d+••
1.25•d-•8   1.218d+••
1.3••d-•8   9.34•d-•1
1.35•d-•8   7.172d-•1
1.4••d-•8   5.296d-•1
1.45•d-•8   3.95•d-•1
1.5••d-•8   2.914d-•1
1.55•d-•8   2.•65d-•1
1.6••d-•8   1.5•6d-•1
1.65•d-•8   1.1•1d-•1
1.7••d-•8   •.292d-•2
1.75•d-•8   7.983d-•2
1.8••d-•8   1.154d-•1
1.85•d-•8   2.241d-•1
1.9••d-•8   4.468d-•1
1.95•d-•8   7.16•d-•1
2.•••d-•8   1.•76d+••
2.•5•d-•8   1.461d+••
2.1••d-•8   1.863d+••
2.15•d-•8   2.262d+••
2.2••d-•8   2.637d+••
2.25•d-•8   2.98•d+••
2.3••d-•8   3.282d+••
2.35•d-•8   3.563d+••
2.4••d-•8   3.8••d+••
2.45•d-•8   4.••4d+••
2.5••d-•8   4.18•d+••
2.55•d-•8   4.32•d+••
2.6••d-•8   4.452d+••
2.65•d-•8   4.556d+••
2.7••d-•8   4.637d+••
2.75•d-•8   4.7•9d+••
2.8••d-•8   4.763d+••
2.85•d-•8   4.8•9d+••
2.9••d-•8   4.848d+••
2.95•d-•8   4.87•d+••
3.•••d-•8   4.9••d+••
3.•5•d-•8   4.92•d+••
3.1••d-•8   4.935d+••
3.15•d-•8   4.949d+••
3.2••d-•8   4.959d+••
3.25•d-•8   4.967d+••
3.3••d-•8   4.974d+••
3.35•d-•8   4.978d+••
3.4••d-•8   4.983d+••
3.45•d-•8   4.986d+••
3.5••d-•8   4.989d+••
3.55•d-•8   4.991d+••
3.6••d-•8   4.993d+••
3.65•d-•8   4.994d+••
3.7••d-•8   4.995d+••
3.75•d-•8   4.996d+••
3.8••d-•8   4.997d+••
3.85•d-•8   4.998d+••
3.9••d-•8   4.998d+••
3.95•d-•8   4.998d+••
4.•••d-•8   4.999d+••
```

Figure C-27.   SPICE Plot Section 2 Input 010 One
             Node Precharge with Basic Gate Widths

0   CMOS/SOS BITSLICE SECTION 2 PRECHARGED AT ONE NODE

0****   INPUT LISTING   TEMPERATURE =   27.000 DEG C

0***

```
.WIDTH OUT=80
.OPTIONS ITL1=500 ITL5=0
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
+LEVEL=1
VDD 1 0 DC 5V
M1 1 3 2 0 NMOS L=5.0U W=5.0U
M2 2 5 1 1 PMOS L=5.0U W=10.0U
M3 1 7 6 1 PMOS L=5.0U W=10.0U
M4 10 9 0 0 NMOS L=5.0U W=15.0U
M5 10 7 6 0 NMOS L=5.0U W=15.0U
M6 1 9 6 1 PMOS L=5.0U W=10.0U
M7 1 6 2 1 PMOS L=5.0U W=10.0U
M8 0 11 9 0 NMOS L=5.0U W=15.0U
M9 13 12 0 0 NMOS L=5.0U W=15.0U
M10 13 6 2 0 NMOS L=5.0U W=15.0U
M11 1 11 9 1 PMOS L=5.0U W=30.0U
M12 1 12 2 1 PMOS L=5.0U W=10.0U
M13 1 14 12 1 PMOS L=5.0U W=10.0U
M14 15 11 0 0 NMOS L=5.0U W=15.0U
M15 15 14 12 0 NMOS L=5.0U W=15.0U
M16 1 11 12 1 PMOS L=5.0U W=10.0U
M17 0 7 14 0 NMOS L=5.0U W=15.0U
M18 1 7 14 1 PMOS L=5.0U W=30.0U
C19 1 0 0.1074PF
C20 11 0 0.279PF
C21 0 0 0.951PF
C22 7 0 0.183PF
C23 14 0 0.100PF
C24 12 0 0.116PF
C25 2 0 0.234PF
C26 6 0 0.125PF
C27 9 0 0.101PF
C28 5 0 0.103PF
C29 3 0 0.103PF
VIN1 11 0 PULSE (5V 5V 5NS 0NS 0NS 10NS)
VIN2 7 0 PULSE (5V 0V 5NS 0NS 0NS 10NS)
VP1 3 0 PULSE (0V 5V 4NS 0NS 0NS 2NS)
VP1BAR 5 0 PULSE (5V 0V 4NS 0NS 0NS 2NS)
.TRAN 0.5NS 40NS
.PLOT TRAN V(2) (0V,5V)
.END
```

```
#        CHOS/SOS BITSLICE SECTION 2 PRECHARGED AT ONE NODE  X]

#••••     TRANSIENT ANALYSIS                    TEMPERATURE =   27.### DEG C

#••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••

X
     TIME      V(2)

X              #.    d+##      1.25#d+##     2.5##d+##     3.75#d+##  5.###d+##
              - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
#.   d+##  1.355d-#7  •
5.###d-1#  1.355d-#7  •
1.###d-#9  1.355d-#7  •
1.5##d-#9  1.355d-#7  •
2.###d-#9  1.355d-#7  •
2.5##d-#9  1.355d-#7  •
3.###d-#9  1.355d-#7  •
3.5##d-#9  1.355d-#7  •
4.###d-#9  1.355d-#7  •
4.5##d-#9  2.1#1d-#1     •
5.###d-#9  7.489d-#1         •
5.5##d-#9  1.#73d+##          •
6.###d-#9  1.292d+##            •
6.5##d-#9  1.473d+##              •
7.###d-#9  1.34#d+##            •
7.5##d-#9  1.211d+##          •
8.###d-#9  1.26#d+##           •
8.5##d-#9  1.495d+##              •
9.###d-#9  1.768d+##                •
9.5##d-#9  2.1#6d+##                  •
1.###d-#8  2.465d+##                    •
1.#5#d-#8  2.#15d+##                       •
1.1##d-#8  3.134d+##                         •
1.15#d-#8  3.423d+##                           •
1.2##d-#8  3.67#d+##                             •
1.25#d-#8  3.9#7d+##                               •
1.3##d-#8  4.#93d+##                                •
1.35#d-#8  4.254d+##                                 •
1.4##d-#8  4.395d+##                                  •
1.45#d-#8  4.5#2d+##                                   •
1.5##d-#8  4.598d+##                                    •
1.55#d-#8  4.676d+##                                     •
1.6##d-#8  4.738d+##                                      •
1.65#d-#8  4.787d+##                                      •
1.7##d-#8  4.824d+##                                       •
1.75#d-#8  4.845d+##                                       •
1.8##d-#8  4.791d+##                                       •
1.85#d-#8  4.6#4d+##                                      •
1.9##d-#8  4.3#4d+##                                     •
1.95#d-#8  3.935d+##                                   •
2.###d-#8  3.525d+##                                 •
2.#5#d-#8  3.#99d+##                               •
2.1##d-#8  2.656d+##                            •
2.15#d-#8  2.22#d+##                         •
2.2##d-#8  1.812d+##                      •
2.25#d-#8  1.459d+##                   •
2.3##d-#8  1.13#d+##                 •
2.35#d-#8  8.725d-#1              •
2.4##d-#8  6.653d-#1           •
2.45#d-#8  4.#79d-#1         •
2.5##d-#8  3.669d-#1        •
2.55#d-#8  2.67#d-#1       •
2.6##d-#8  1.91#d-#1      •
2.65#d-#8  1.419d-#1     •
2.7##d-#8  1.#1#d-#1     •
2.75#d-#8  7.279d-#2   •
2.8##d-#8  5.29#d-#2  •
2.#5#d-#8  3.7#1d-#2  •
2.9##d-#8  2.712d-#2  •
2.95#d-#8  1.93#d-#2  •
3.###d-#8  1.357d-#2  •
3.#5#d-#8  9.983d-#3  •
3.1##d-#8  7.#37d-#3  •
3.15#d-#8  5.#41d-#3  •
3.2##d-#8  3.64#d-#3  •
3.25#d-#8  2.542d-#3  •
3.3##d-#8  1.#59d-#3  •
3.35#d-#8  1.326d-#3  •
3.4##d-#8  9.271d-#4  •
3.45#d-#8  6.818d-#4  •
3.5##d-#8  4.##3d-#4  •
3.55#d-#8  3.44#d-#4  •
3.6##d-#8  2.489d-#4  •
3.65#d-#8  1.734d-#4  •
3.7##d-#8  1.269d-#4  •
3.75#d-#8  9.#51d-#5  •
3.8##d-#8  6.33#d-#5  •
3.85#d-#8  4.659d-#5  •
3.9##d-#8  3.285d-#5  •
3.95#d-#8  2.356d-#5  •
4.###d-#8  1.65#d-#5  •
              - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
```

Figure C-28.   SPICE Plot Section 2 Input 101 One
                Node Precharge with Basic Widths

C-61

Ø   CMOS/SOS BITSLICE SECTION 2 PRECHARGED AT ONE NODE

Ø****   INPUT LISTING   TEMPERATURE =   27.ØØØ DEG C

Ø***

```
.WIDTH OUT=8Ø
.OPTIONS ITL1=5ØØ ITL5=Ø
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
+LEVEL=1
VDD 1 Ø DC 5V
M1 1 3 2 Ø NMOS L=5.ØU W=1Ø.ØU
M2 2 5 1 1 PMOS L=5.ØU W=2Ø.ØU
M3 1 7 6 1 PMOS L=5.ØU W=1Ø.ØU
M4 1Ø 9 Ø Ø NMOS L=5.ØU W=15.ØU
M5 1Ø 7 6 Ø NMOS L=5.ØU W=15.ØU
M6 1 9 6 1 PMOS L=5.ØU W=1Ø.ØU
M7 1 6 2 1 PMOS L=5.ØU W=1Ø.ØU
M8 Ø 11 9 Ø NMOS L=5.ØU W=15.ØU
M9 13 12 Ø Ø NMOS L=5.ØU W=15.ØU
M1Ø 13 6 2 Ø NMOS L=5.ØU W=15.ØU
M11 1 11 9 1 PMOS L=5.ØU W=3Ø.ØU
M12 1 12 2 1 PMOS L=5.ØU W=1Ø.ØU
M13 1 14 12 1 PMOS L=5.ØU W=1Ø.ØU
M14 15 11 Ø Ø NMOS L=5.ØU W=15.ØU
M15 15 14 12 Ø NMOS L=5.ØU W=15.ØU
M16 1 11 12 1 PMOS L=5.ØU W=1Ø.ØU
M17 Ø 7 14 Ø NMOS L=5.ØU W=15.ØU
M18 1 7 14 1 PMOS L=5.ØU W=3Ø.ØU
C19 1 Ø Ø.1Ø74PF
C2Ø 11 Ø Ø.279PF
C21 Ø Ø Ø.951PF
C22 7 Ø Ø.183PF
C23 14 Ø Ø.1ØØPF
C24 12 Ø Ø.116PF
C25 2 Ø Ø.234PF
C26 6 Ø Ø.125PF
C27 9 Ø Ø.1Ø1PF
C28 5 Ø Ø.1Ø3PF
C29 3 Ø Ø.1Ø3PF
VIN1 11 Ø PULSE (5V 5V 5NS ØNS ØNS 1ØNS)
VIN2 7 Ø PULSE (ØV 5V 5NS ØNS ØNS 1ØNS)
VP1 3 Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS
VP1BAR 5 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
.TRAN Ø.5NS 4ØNS
.PLOT TRAN V(2) (ØV,5V)
.END
```

```
1*******12/01/84 ********  SPICE 2G.1 (150CT80)  ********04:55:19****
#        CMOS/SOS BITSLICE SECTION 2 PRECHARGED AT ONE NODE  X2
#****    TRANSIENT ANALYSIS              TEMPERATURE =  27.000 DEG C
#****************************************************************
X
   TIME       V(2)
X                #.   d+00    1.250d+00    2.500d+00    3.750d+00  5.000d+00
#.      d+00   5.000d+00 :
5.000d-10   5.000d+00 .
1.000d-09   5.000d+00 .
1.500d-09   5.000d+00 .
2.000d-09   5.000d+00 .
2.500d-09   5.000d+00 .
3.000d-09   5.000d+00 .
3.500d-09   5.000d+00 .
4.000d-09   5.000d+00 .
4.500d-09   5.000d+00 .
5.000d-09   5.000d+00 .
5.500d-09   5.000d+00 .
6.000d-09   5.000d+00 .
6.500d-09   5.000d+00 .
7.000d-09   4.997d+00 .
7.500d-09   4.928d+00 .
8.000d-09   4.753d+00 .
8.500d-09   4.438d+00 .
9.000d-09   4.062d+00 .
9.500d-09   3.658d+00 .
1.000d-08   3.223d+00 .
1.050d-08   2.777d+00 .
1.100d-08   2.343d+00 .
1.150d-08   1.916d+00 .
1.200d-08   1.551d+00 .
1.250d-08   1.210d+00 .
1.300d-08   9.348d-01 .
1.350d-08   7.172d-01 .
1.400d-08   5.296d-01 .
1.450d-08   3.958d-01 .
1.500d-08   2.914d-01 .
1.550d-08   2.065d-01 .
1.600d-08   1.566d-01 .
1.650d-08   1.181d-01 .
1.700d-08   8.292d-02 .
1.750d-08   7.983d-02 .
1.800d-08   1.154d-01 .
1.850d-08   2.241d-01 .
1.900d-08   4.468d-01 .
1.950d-08   7.168d-01 .
2.000d-08   1.076d+00 .
2.050d-08   1.461d+00 .
2.100d-08   1.863d+00 .
2.150d-08   2.262d+00 .
2.200d-08   2.637d+00 .
2.250d-08   2.988d+00 .
2.300d-08   3.282d+00 .
2.350d-08   3.563d+00 .
2.400d-08   3.800d+00 .
2.450d-08   4.004d+00 .
2.500d-08   4.168d+00 .
2.550d-08   4.328d+00 .
2.600d-08   4.452d+00 .
2.650d-08   4.556d+00 .
2.700d-08   4.637d+00 .
2.750d-08   4.709d+00 .
2.800d-08   4.763d+00 .
2.850d-08   4.809d+00 .
2.900d-08   4.848d+00 .
2.950d-08   4.876d+00 .
3.000d-08   4.900d+00 .
3.050d-08   4.920d+00 .
3.100d-08   4.935d+00 .
3.150d-08   4.949d+00 .
3.200d-08   4.959d+00 .
3.250d-08   4.967d+00 .
3.300d-08   4.974d+00 .
3.350d-08   4.978d+00 .
3.400d-08   4.983d+00 .
3.450d-08   4.986d+00 .
3.500d-08   4.989d+00 .
3.550d-08   4.991d+00 .
3.600d-08   4.993d+00 .
3.650d-08   4.994d+00 .
3.700d-08   4.995d+00 .
3.750d-08   4.996d+00 .
3.800d-08   4.997d+00 .
3.850d-08   4.998d+00 .
3.900d-08   4.998d+00 .
3.950d-08   4.998d+00 .
4.000d-08   4.999d+00 .
```

Figure C-29.   SPICE Plot Section 2 Input 010 One
Node Precharge with Widths x2

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```
.WIDTH OUT=80
.OPTIONS ITL1=500 ITL5=0
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
+LEVEL=1
VDD 1 0 DC 5V
M1  1  3  2 0 NMOS L=5.0U W=10.0U
M2  2  5  1 1 PMOS L=5.0U W=20.0U
M3  1  7  6 1 PMOS L=5.0U W=10.0U
M4  10 9  0 0 NMOS L=5.0U W=15.0U
M5  10 7  6 0 NMOS L=5.0U W=15.0U
M6  1  9  6 1 PMOS L=5.0U W=10.0U
M7  1  6  2 1 PMOS L=5.0U W=10.0U
M8  0  11 9 0 NMOS L=5.0U W=15.0U
M9  13 12 0 0 NMOS L=5.0U W=15.0U
M10 13 6  2 0 NMOS L=5.0U W=15.0U
M11 1  11 9 1 PMOS L=5.0U W=30.0U
M12 1  12 2 1 PMOS L=5.0U W=10.0U
M13 1  14 12 1 PMOS L=5.0U W=10.0U
M14 15 11 0 0 NMOS L=5.0U W=15.0U
M15 15 14 12 0 NMOS L=5.0U W=15.0U
M16 1  11 12 1 PMOS L=5.0U W=10.0U
M17 0  7  14 0 NMOS L=5.0U W=15.0U
M18 1  7  14 1 PMOS L=5.0U W=30.0U
C19 1  0 0.1074PF
C20 11 0 0.279PF
C21 0  0 0.951PF
C22 7  0 0.183PF
C23 14 0 0.100PF
C24 12 0 0.116PF
C25 2  0 0.234PF
C26 6  0 0.125PF
C27 9  0 0.101PF
C28 5  0 0.103PF
C29 3  0 0.103PF
VIN1 11 0 PULSE (5V 5V 5NS 0NS 0NS 10NS)
VIN2 7  0 PULSE (5V 0V 5NS 0NS 0NS 10NS)
VP1 3 0 PULSE (0V 5V 4NS 0NS 0NS 2NS)
VP1BAR 5 0 PULSE (5V 0V 4NS 0NS 0NS 2NS)
.TRAN 0.5NS 40NS
.PLOT TRAN V(2) (0V,5V)
.END
```

```
#          CMOS/SOS BITSLICE SECTION 2 PRECHARGED AT ONE NODE   X2
#****      TRANSIENT ANALYSIS              TEMPERATURE =   27.### DEG C
#************************************************************************

X
     TIME       V(2)
X                #.       d+##       1.25#d+##     2.5##d+##     3.75#d+##  5.###d+##
   #.   d+##    1.355d-#7  *
   5.###d-1#    1.355d-#7  *
   1.###d-#9    1.355d-#7  *
   1.5##d-#9    1.355d-#7  *
   2.###d-#9    1.355d-#7  *
   2.5##d-#9    1.355d-#7  *
   3.###d-#9    1.355d-#7  *
   3.5##d-#9    1.355d-#7  *
   4.###d-#9    1.355d-#7  *
   4.5##d-#9    3.924d-#1
   5.###d-#9    1.321d+##
   5.5##d-#9    1.867d+##
   6.###d-#9    2.261d+##
   6.5##d-#9    2.6##d+##
   7.###d-#9    2.499d+##
   7.5##d-#9    2.323d+##
   8.###d-#9    2.367d+##
   8.5##d-#9    2.578d+##
   9.###d-#9    2.85#d+##
   9.5##d-#9    3.129d+##
   1.###d-#8    3.4#7d+##
   1.#5#d-#8    3.659d+##
   1.1##d-#8    3.882d+##
   1.15#d-#8    4.#74d+##
   1.2##d-#8    4.232d+##
   1.25#d-#8    4.375d+##
   1.3##d-#8    4.48#d+##
   1.35#d-#8    4.583d+##
   1.4##d-#8    4.666d+##
   1.45#d-#8    4.726d+##
   1.5##d-#8    4.76#d+##
   1.55#d-#8    4.824d+##
   1.6##d-#8    4.85#d+##
   1.65#d-#8    4.885d+##
   1.7##d-#8    4.9#6d+##
   1.75#d-#8    4.914d+##
   1.8##d-#8    4.854d+##
   1.85#d-#8    4.662d+##
   1.9##d-#8    4.36#d+##
   1.95#d-#8    3.996d+##
   2.###d-#8    3.564d+##
   2.#5#d-#8    3.157d+##
   2.1##d-#8    2.713d+##
   2.15#d-#8    2.282d+##
   2.2##d-#8    1.861d+##
   2.25#d-#8    1.5#1d+##
   2.3##d-#8    1.176d+##
   2.35#d-#8    8.998d-#1
   2.4##d-#8    6.896d-#1
   2.45#d-#8    5.#65d-#1
   2.5##d-#8    3.791d-#1
   2.55#d-#8    2.791d-#1
   2.6##d-#8    1.977d-#1
   2.65#d-#8    1.475d-#1
   2.7##d-#8    1.#56d-#1
   2.75#d-#8    7.54#d-#2
   2.8##d-#8    5.517d-#2
   2.85#d-#8    3.879d-#2
   2.9##d-#8    2.817d-#2
   2.95#d-#8    2.#25d-#2
   3.###d-#8    1.4#Gd-#2
   3.#5#d-#8    1.#4#d-#2
   3.1##d-#8    7.367d-#3
   3.15#d-#8    5.223d-#3
   3.2##d-#8    3.#?6d-#3
   3.25#d-#8    2.665d-#3
   3.3##d-#8    1.931d-#3
   3.35#d-#8    1.386d-#3
   3.4##d-#8    9.6#4d-#4
   3.45#d-#8    7.#99d-#4
   3.5##d-#8    5.#27d-#4
   3.55#d-#8    3.563d-#4
   3.6##d-#8    2.596d-#4
   3.65#d-#8    1.81#d-#4
   3.7##d-#8    1.318d-#4
   3.75#d-#8    9.459d-#5
   3.8##d-#8    6.557d-#5
   3.85#d-#8    4.#5#d-#5
   3.9##d-#8    3.438d-#5
   3.95#d-#8    2.441d-#5
   4.###d-#8    1.728d-#5
```

Figure C-30.   SPICE Plot Section 2 Input 101 One
Node Precharge with Widths x2.

```
.WIDTH OUT=8Ø
.OPTIONS ITL1=5ØØ ITL5=Ø
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
+LEVEL=1
VDD 1 Ø DC 5V
M1  1  3  2  Ø NMOS L=5.ØU W=15.ØU
M2  2  5  1  1 PMOS L=5.ØU W=3Ø.ØU
M3  1  7  6  1 PMOS L=5.ØU W=1Ø.ØU
M4  1Ø 9  Ø  Ø NMOS L=5.ØU W=15.ØU
M5  1Ø 7  6  Ø NMOS L=5.ØU W=15.ØU
M6  1  9  6  1 PMOS L=5.ØU W=1Ø.ØU
M7  1  6  2  1 PMOS L=5.ØU W=1Ø.ØU
M8  Ø  11 9  Ø NMOS L=5.ØU W=15.ØU
M9  13 12 Ø  Ø NMOS L=5.ØU W=15.ØU
M1Ø 13 6  2  Ø NMOS L=5.ØU W=15.ØU
M11 1  11 9  1 PMOS L=5.ØU W=3Ø.ØU
M12 1  12 2  1 PMOS L=5.ØU W=1Ø.ØU
M13 1  14 12 1 PMOS L=5.ØU W=1Ø.ØU
M14 15 11 Ø  Ø NMOS L=5.ØU W=15.ØU
M15 15 14 12 Ø NMOS L=5.ØU W=15.ØU
M16 1  11 12 1 PMOS L=5.ØU W=1Ø.ØU
M17 Ø  7  14 Ø NMOS L=5.ØU W=15.ØU
M18 1  7  14 1 PMOS L=5.ØU W=3Ø.ØU
C19 1  Ø Ø.1Ø74PF
C2Ø 11 Ø Ø.279PF
C21 Ø  Ø Ø.951PF
C22 7  Ø Ø.183PF
C23 14 Ø Ø.1ØØPF
C24 12 Ø Ø.116PF
C25 2  Ø Ø.234PF
C26 6  Ø Ø.125PF
C27 9  Ø Ø.1Ø1PF
C28 5  Ø Ø.1Ø3PF
C29 3  Ø Ø.1Ø3PF
VIN1 11 Ø PULSE (5V 5V 5NS ØNS ØNS 1ØNS)
VIN2 7 Ø PULSE (ØV 5V 5NS ØNS ØNS 1ØNS)
VP1 3 Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS)
VP1BAR 5 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
.TRAN Ø.5NS 4ØNS
.PLOT TRAN V(2) (ØV,5V)
.END
```

CHOS/SOS BITSLICE SECTION 2 PRECHARGED AT ONE NODE X3

#••••   TRANSIENT ANALYSIS   TEMPERATURE • 27.0## DEG C

#•••

```
X
    TIME      V(2)

X              #.   d+##      1.25#d+##     2.5##d+##      3.75#d+## 5.###d+##
   #.   d+##  5.###d+## .                                                    •
   5.###d-1#  5.###d+## .                                                    •
   1.###d-#9  5.###d+## .                                                    •
   1.5##d-#9  5.###d+## .                                                    •
   2.###d-#9  5.###d+## .                                                    •
   2.5##d-#9  5.###d+## .                                                    •
   3.###d-#9  5.###d+## .                                                    •
   3.5##d-#9  5.###d+## .                                                    •
   4.###d-#9  5.###d+## .                                                    •
   4.5##d-#9  5.###d+## .                                                    •
   5.###d-#9  5.###d+0# .                                                    •
   5.5##d-#9  5.###d+## .                                                    •
   6.###d-#9  5.###d+## .                                                    •
   6.5##d-#9  5.###d+## .                                                    •
   7.###d-#9  4.997d+## .                                                    •
   7.5##d-#9  4.92#d+## .                                                   •
   8.###d-#9  4.733d+## .                                                 •
   8.5##d-#9  4.43#d+## .                                               •
   9.###d-#9  4.#62d+0# .                                             •
   9.5##d-#9  3.65#d+## .                                         •
   1.###d-#8  3.223d+## .                                     •
   1.#5#d-#8  2.777d+## .                                  •
   1.1##d-#8  2.343d+## .                               •
   1.15#d-#8  1.916d+## .                            •
   1.2##d-#8  1.551d+## .                         •
   1.25#d-#8  1.218d+## .                      •
   1.3##d-#8  9.348d-#1 .                   •
   1.35#d-#8  7.172d-#1 .                •
   1.4##d-#8  5.296d-#1 .              •
   1.45#d-#8  3.9#8d-#1 .            •
   1.5##d-#8  2.914d-#1 .          •
   1.55#d-#8  2.#65d-#1 .         •
   1.6##d-#8  1.5#Gd-#1 .       •
   1.65#d-#8  1.1#1d-#1 .      •
   1.7##d-#8  8.292d-#2 .     •
   1.75#d-#8  7.983d-#2 .     •
   1.8##d-#0  1.154d-#1 .      •
   1.85#d-#0  2.241d-#1 .       •
   1.9##d-#8  4.46#d-#1 .         •
   1.95#d-#8  7.18#d-#1 .           •
   2.###d-#8  1.#76d+## .             •
   2.#5#d-#8  1.461d+## .               •
   2.1##d-#8  1.863d+## .                 •
   2.15#d-#8  2.262d+## .                   •
   2.2##d-#8  2.6#7d+## .                     •
   2.25#d-#8  2.9##d+## .                      •
   2.3##d-#8  3.282d+## .                        •
   2.35#d-#8  3.563d+## .                          •
   2.4##d-#8  3.8##d+## .                            •
   2.45#d-#8  4.##4d+## .                              •
   2.5##d-#8  4.188d+## .                               •
   2.55#d-#8  4.328d+## .                                 •
   2.6##d-#8  4.452d+## .                                  •
   2.65#d-#8  4.556d+## .                                    •
   2.7##d-#8  4.637d+## .                                     •
   2.75#d-#8  4.7#9d+## .                                      •
   2.8##d-#8  4.763d+## .                                       •
   2.85#d-#8  4.8#9d+## .                                        •
   2.9##d-#8  4.848d+## .                                         •
   2.95#d-#8  4.876d+## .                                          •
   3.###d-#8  4.9##d+## .                                          •
   3.#5#d-#8  4.92#d+## .                                           •
   3.1##d-#8  4.935d+## .                                           •
   3.15#d-#8  4.949d+## .                                            •
   3.2##d-#8  4.959d+## .                                            •
   3.25#d-#8  4.967d+## .                                            •
   3.3##d-#8  4.974d+## .                                            •
   3.35#d-#8  4.978d+## .                                            •
   3.4##d-#8  4.983d+## .                                            •
   3.45#d-#8  4.986d+## .                                            •
   3.5##d-#8  4.989d+## .                                            •
   3.55#d-#8  4.991d+## .                                            •
   3.6##d-#8  4.993d+## .                                            •
   3.65#d-#8  4.994d+## .                                            •
   3.7##d-#8  4.995d+## .                                            •
   3.75#d-#8  4.996d+## .                                            •
   3.8##d-#8  4.997d+## .                                            •
   3.85#d-#8  4.998d+## .                                            •
   3.9##d-#8  4.998d+## .                                            •
   3.95#d-#8  4.99#d+## .                                            •
   4.###d-#8  4.999d+## .                                            •
```

Figure C-31.   SPICE Plot Section 2 Input 010 One
               Node Precharge with Widths x3.

```
.WIDTH OUT=80
.OPTIONS ITL1=500 ITL5=0
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
+LEVEL=1
VDD 1 0 DC 5V
M1  1  3  2  0 NMOS L=5.0U W=15.0U
M2  2  5  1  1 PMOS L=5.0U W=30.0U
M3  1  7  6  1 PMOS L=5.0U W=10.0U
M4  10 9  0  0 NMOS L=5.0U W=15.0U
M5  10 7  6  0 NMOS L=5.0U W=15.0U
M6  1  9  6  1 PMOS L=5.0U W=10.0U
M7  1  6  2  1 PMOS L=5.0U W=10.0U
M8  0  11 9  0 NMOS L=5.0U W=15.0U
M9  13 12 0  0 NMOS L=5.0U W=15.0U
M10 13 6  2  0 NMOS L=5.0U W=15.0U
M11 1  11 9  1 PMOS L=5.0U W=30.0U
M12 1  12 2  1 PMOS L=5.0U W=10.0U
M13 1  14 12 1 PMOS L=5.0U W=10.0U
M14 15 11 0  0 NMOS L=5.0U W=15.0U
M15 15 14 12 0 NMOS L=5.0U W=15.0U
M16 1  11 12 1 PMOS L=5.0U W=10.0U
M17 0  7  14 0 NMOS L=5.0U W=15.0U
M18 1  7  14 1 PMOS L=5.0U W=30.0U
C19 1  0  0.1074PF
C20 11 0  0.279PF
C21 0  0  0.951PF
C22 7  0  0.183PF
C23 14 0  0.100PF
C24 12 0  0.116PF
C25 2  0  0.234PF
C26 6  0  0.125PF
C27 9  0  0.101PF
C28 5  0  0.103PF
C29 3  0  0.103PF
VIN1 11 0 PULSE (5V 5V 5NS 0NS 0NS 10NS)
VIN2 7  0 PULSE (5V 0V 5NS 0NS 0NS 10NS)
VP1  3  0 PULSE (0V 5V 4NS 0NS 0NS 2NS)
VP1BAR 5 0 PULSE (5V 0V 4NS 0NS 0NS 2NS)
.TRAN 0.5NS 40NS
.PLOT TRAN V(2) (0V.5V)
.END
```

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```
1********12/81/84 ********  SPICE 2G.1 (15OCT80)  ********84:56:88*****

#       CMOS/SOS BITSLICE SECTION 2 PRECHARGED AT ONE NODE   x3

#****    TRANSIENT ANALYSIS              TEMPERATURE =  27.888 DEG C

#...............................................................................


X
    TIME     V(2)

X              #.   d+88     1.258d+88     2.588d+88     3.758d+88  5.888d+88
              -------------------------------------------------------------------
#.   d+88  1.355d-87 *
5.888d-18  1.355d-87 *
1.888d-89  1.355d-87 *
1.588d-89  1.355d-87 *
2.888d-89  1.355d-87 *
2.588d-89  1.355d-87 *
3.888d-29  1.355d-87 *
3.588d-89  1.355d-87 *
4.888d-89  1.355d-87 *
4.588d-89  5.572d-81 .        *
5.888d-89  1.811d+88 .                  *
5.588d-89  2.568d+88 .                         *
6.888d-89  3.117d+88 .                            *
6.588d-89  3.548d+88 .                               *
7.888d-89  3.466d+88 .                              *
7.588d-89  3.294d+88 .                            *
8.888d-89  3.328d+88 .                            *
8.588d-89  3.498d+88 .                             *
9.888d-89  3.697d+88 .                              *
9.588d-89  3.889d+88 .                               *
1.888d-88  4.875d+88 .                                *
1.858d-88  4.235d+88 .                                 *
1.188d-88  4.372d+U8 .                                  *
1.158d-88  4.486d+88 .                                   *
1.288d-88  4.578d+88 .                                    *
1.258d-88  4.668d+88 .                                    *
1.388d-88  4.723d+88 .                                     *
1.358d-88  4.776d+88 .                                     *
1.488d-88  4.822d+88 .                                      *
1.458d-88  4.854d+88 .                                      *
1.588d-88  4.883d+88 .                                      *
1.558d-88  4.987d+88 .                                       *
1.688d-88  4.925d+88 .                                       *
1.658d-88  4.948d+88 .                                       *
1.788d-88  4.958d+88 .                                       *
1.758d-88  4.953d+88 .                                       *
1.888d-88  4.889d+88 .                                      *
1.858d-88  4.694d+88 .                                     *
1.988d-88  4.391d+88 .                                   *
1.958d-88  4.827d+88 .                                 *
2.888d-88  3.616d+88 .                             *
2.858d-88  3.188d+88 .                          *
2.188d-88  2.743d+88 .                        *
2.158d-88  2.311d+88 .                     *
2.288d-88  1.868d+88 .                  *
2.258d-88  1.525d+88 .               *
2.388d-88  1.196d+88 .            *
2.358d-88  9.161d-81 .          *
2.488d-88  7.827d-81 .         *
2.458d-88  5.187d-81 .       *
2.588d-88  3.869d-81 .     *
2.558d-88  2.849d-81 .    *
2.688d-88  2.828d-81 .   *
2.658d-88  1.587d-81 . *
2.788d-88  1.879d-81 . *
2.758d-88  7.786d-82 .*
2.888d-88  5.648d-82 .*
2.858d-88  3.966d-82 *
2.988d-88  2.888d-82 *
2.958d-88  2.871d-82 *
3.888d-88  1.437d-82 *
3.858d-88  1.863d-82 *
3.188d-88  7.533d-83 *
3.158d-88  5.341d-83 *
3.288d-88  3.892d-83 *
3.258d-88  2.725d-83 *
3.388d-88  1.975d-83 *
3.358d-88  1.417d-83 *
3.488d-88  9.821d-84 *
3.458d-88  7.259d-84 *
3.588d-88  5.141d-84 *
3.558d-88  3.643d-84 *
3.688d-88  2.655d-84 *
3.658d-88  1.859d-84 *
3.788d-88  1.347d-84 *
3.758d-88  9.671d-85 *
3.888d-88  6.785d-85 *
3.858d-88  4.959d-85 *
3.988d-88  3.515d-85 *
3.958d-88  2.495d-85 *
4.888d-88  1.766d-85 *
              -------------------------------------------------------------------
```

Figure C-32. SPICE Plot Section 2 Input 101 One
             Node Precharge with Widths x3.

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Figure C-33.   Section 2 Precharge Two Node CLL Plot

Figure C-34.   Section 2 Two Node Precharge Node Plot.

Table C-6

BITSLICE PRECHARGED SECTION 2 NODE REFERENCE LIST

GND	0
Vdd	1
NMOS	0
PMOS	1
13	2
67	3
1	4
28	5
60	6
7	7
4	8
30	9
47	10
27	11
3	12
32	13
9	14
17	15

```
.WIDTH OUT=80
.OPTIONS ITL1=500 ITL5=0
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
+LEVEL=1
VDD 1 0 DC 5V
M1 1 3 2 0 NMOS L=5.0U W=5.0U
M2 1 3 5 0 NMOS L=5.0U W=5.0U
M3 2 6 1 1 PMOS L=5.0U W=10.0U
M4 5 6 1 1 PMOS L=5.0U W=10.0U
M5 1 7 5 1 PMOS L=5.0U W=10.0U
M6 10 9 0 0 NMOS L=5.0U W=15.0U
M7 10 7 5 0 NMOS L=5.0U W=15.0U
M8 1 9 5 1 PMOS L=5.0U W=10.0U
M9 1 5 11 1 PMOS L=5.0U W=10.0U
M10 0 12 9 0 NMOS L=5.0U W=15.0U
M11 13 2 0 0 NMOS L=5.0U W=15.0U
M12 13 5 11 0 NMOS L=5.0U W=15.0U
M13 1 12 9 1 PMOS L=5.0U W=30.0U
M14 1 2 11 1 PMOS L=5.0U W=10.0U
M15 1 14 2 1 PMOS L=5.0U W=10.0U
M16 15 12 0 0 NMOS L=5.0U W=15.0U
M17 15 14 2 0 NMOS L=5.0U W=15.0U
M18 1 12 2 1 PMOS L=5.0U W=10.0U
M19 0 7 14 0 NMOS L=5.0U W=15.0U
M20 1 7 14 1 PMOS L=5.0U W=30.0U
C21 1 0 0.1135PF
C22 12 0 0.279PF
C23 0 0 0.951PF
C24 7 0 0.183PF
C25 14 0 0.100PF
C26 2 0 0.288PF
C27 11 0 0.134PF
C28 5 0 0.260PF
C29 9 0 0.101PF
C30 6 0 0.103PF
C31 3 0 0.103PF
VIN1 12 0 PULSE (5V 5V 5NS 0NS 0NS 10NS)
VIN2 7 0 PULSE (0V 5V 5NS 0NS 0NS 10NS)
VP1 3 0 PULSE (0V 5V 4NS 0NS 0NS 2NS)
VP1BAR 6 0 PULSE (5V 0V 4NS 0NS 0NS 2NS)
.TRAN 0.5NS 40NS
.PLOT TRAN V(11) (0V,5V)
.END
```

```
#        CMOS/SOS PRECHARGED BITSLICE SECTION 2 TRANSIENT ANALYSIS *)

#****     TRANSIENT ANALYSIS                 TEMPERATURE =   27.### DEG C

#........................................................................

X
    TIME       V(11)
X              #.   d+##     1.25#d+##    2.5##d+##     3.75#d+## 5.###d+##
       8.   d+##   5.###d+##
       5.###d-1#   5.###d+##
       1.###d-#9   5.###d+##
       1.5##d-#9   5.###d+##
       2.###d-#9   5.###d+##
       2.5##d-#9   5.###d+##
       3.###d-#9   5.###d+##
       3.5##d-#9   5.###d+##
       4.###d-#9   5.###d+##
       4.5##d-#9   5.###d+##
       5.###d-#9   5.###d+##
       5.5##d-#9   5.###d+##
       6.###d-#9   4.994d+##
       6.5##d-#9   4.934d+##
       7.###d-#9   4.767d+##
       7.5##d-#9   4.5##d+##
       8.###d-#9   4.147d+##
       8.5##d-#9   3.7#1d+##
       9.###d-#9   3.198d+##
       9.5##d-#9   2.623d+##
       1.###d-#8   2.#57d+##
       1.#5#d-#8   1.5#7d+##
       1.1##d-#8   1.#67d+##
       1.15#d-#8   6.877d-#1
       1.2##d-#8   4.427d-#1
       1.25#d-#8   2.7##d-#1
       1.3##d-#8   1.477d-#1
       1.35#d-#8   9.263d-#2
       1.4##d-#8   5.#46d-#2
       1.45#d-#8   2.738d-#2
       1.5##d-#8   1.6#6d-#2
       1.55#d-#8   8.476d-#3
       1.6##d-#8   4.#55d-#3
       1.65#d-#8   2.8#6d-#3
       1.7##d-#8   1.665d-#3
       1.75#d-#8   1.6#4d-#3
       1.8##d-#8   2.188d-#3
       1.85#d-#8   1.542d-#2
       1.9##d-#8   4.477d-#2
       1.95#d-#8   9.227d-#2
       2.###d-#8   1.9#9d-#1
       2.#5#d-#8   3.244d-#1
       2.1##d-#8   5.317d-#1
       2.15#d-#8   8.29#d-#1
       2.2##d-#8   1.179d+##
       2.25#d-#8   1.637d+##
       2.3##d-#8   2.121d+##
       2.35#d-#8   2.642d+##
       2.4##d-#8   3.131d+##
       2.45#d-#8   3.554d+##

       2.5##d-#8   3.917d+##
       2.55#d-#8   4.223d+##
       2.6##d-#8   4.431d+##
       2.65#d-#8   4.6#5d+##
       2.7##d-#8   4.724d+##
       2.75#d-#8   4.8#7d+##
       2.8##d-#8   4.872d+##
       2.#5#d-#8   4.91#d+##
       2.9##d-#8   4.939d+##
       2.#5#d-#8   4.96#d+##
       3.###d-#8   4.972d+##
       3.#5#d-#8   4.981d+##
       3.1##d-#8   4.987d+##
       3.15#d-#8   4.991d+##
       3.2##d-#8   4.994d+##
       3.25#d-#8   4.996d+##
       3.3##d-#8   4.997d+##
       3.35#d-#8   4.998d+##
       3.4##d-#8   4.999d+##
       3.45#d-#8   4.999d+##
       3.5##d-#8   4.999d+##
       3.55#d-#8   5.###d+##
       3.6##d-#8   5.###d+##
       3.65#d-#8   5.###d+##
       3.7##d-#8   5.###d+##
       3.75#d-#8   5.###d+##
       3.8##d-#8   5.###d+##
       3.#5#d-#8   5.###d+##
       3.9##d-#8   5.###d+##
       3.95#d-#8   5.###d+##
       4.###d-#8   5.###d+##
```

Figure C-35.   SPICE Plot Section 2 Input 010 Two
Node Precharge Using Basic Widths

```
.WIDTH OUT=30
.OPTIONS ITL1=500 ITL5=0
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
+LEVEL=1
VDD 1 0 DC 5V
M1 1 3 2 0 NMOS L=5.0U W=5.0U
M2 1 3 5 0 NMOS L=5.0U W=5.0U
M3 2 6 1 1 PMOS L=5.0U W=10.0U
M4 5 6 1 1 PMOS L=5.0U W=10.0U
M5 1 7 5 1 PMOS L=5.0U W=10.0U
M6 10 9 0 0 NMOS L=5.0U W=15.0U
M7 10 7 5 0 NMOS L=5.0U W=15.0U
M8 1 9 5 1 PMOS L=5.0U W=10.0U
M9 1 5 11 1 PMOS L=5.0U W=10.0U
M10 0 12 9 0 NMOS L=5.0U W=15.0U
M11 13 2 0 0 NMOS L=5.0U W=15.0U
M12 13 5 11 0 NMOS L=5.0U W=15.0U
M13 1 12 9 1 PMOS L=5.0U W=30.0U
M14 1 2 11 1 PMOS L=5.0U W=10.0U
M15 1 14 2 1 PMOS L=5.0U W=10.0U
M16 15 12 0 0 NMOS L=5.0U W=15.0U
M17 15 14 2 0 NMOS L=5.0U W=15.0U
M18 1 12 2 1 PMOS L=5.0U W=10.0U
M19 0 7 14 0 NMOS L=5.0U W=15.0U
M20 1 7 14 1 PMOS L=5.0U W=30.0U
C21 1 0 0.1135PF
C22 12 0 0.279PF
C23 0 0 0.951PF
C24 7 0 0.183PF
C25 14 0 0.100PF
C26 2 0 0.298PF
C27 11 0 0.134PF
C28 5 0 0.260PF
C29 9 0 0.101PF
C30 6 0 0.103PF
C31 3 0 0.103PF
VIN1 12 0 PULSE (5V 5V 5NS 0NS 0NS 10NS)
VIN2 7 0 PULSE (5V 0V 5NS 0NS 0NS 10NS)
VP1 3 0 PULSE (0V 5V 4NS 0NS 0NS 2NS)
VP1BAR 6 0 PULSE (5V 0V 4NS 0NS 0NS 2NS)
.TRAN 0.5NS 40NS
.PLOT TRAN V(11) (0V,5V)
.END
```

```
#          CMOS/SOS PRECHARGED BITSLICE SECTION 2 TRANSIENT ANALYSIS Xi

#****      TRANSIENT ANALYSIS                    TEMPERATURE =   27.### DEG C

#*****************************************************************************

X
     TIME        V(11)

X                   #.     d+##      1.25#d+##      2.5##d+##      3.75#d+##  5.###d+##
       *-------------------------------------------------------------------------*
#.    d+##   9.#35d-##  *
5.###d-1#   9.#35d-##  *
1.###d-#9   9.#35d-##  *
1.5##d-#9   9.#36d-##  *
2.###d-#9   9.#35d-##  *
2.5##d-#9   9.#35d-##  *
3.###d-#9   9.#35d-##  *
3.5##d-#9   9.#35d-##  *
4.###d-#9   9.#35d-##  *
4.5##d-#9   9.#35d-##  *
5.###d-#9   9.#35d-##  *
5.5##d-#9   9.#35d-##  *
6.###d-#9   9.#4#d-##  *
6.5##d-#9   9.142d-##  *
7.###d-#9   9.35#d-##  *
7.5##d-#9   1.251d-#4  *
8.###d-#9   5.694d-#3  *
8.5##d-#9   2.594d-#2  *
9.###d-#9   5.831d-#2  *
9.5##d-#9   1.355d-#1  *
1.###d-#8   2.424d-#1   ·
1.#5#d-#8   4.#44d-#1     ·
1.1##d-#8   6.58#d-#1        ·
1.15#d-#8   9.629d-#1            ·
1.2##d-#8   1.363d+##  .
1.25#d-#8   1.839d+##                 ·
1.3##d-#8   2.355d+##                     ·
1.35#d-#8   2.866d+##                        ·
1.4##d-#8   3.321d+##                           ·
1.45#d-#8   3.743d+##                              ·
1.5##d-#8   4.#54d+##                                ·
1.55#d-#8   4.334d+##                                  ·
1.6##d-#8   4.526d+##                                   ·
1.65#d-#8   4.665d+##                                    ·
1.7##d-#8   4.762d+##                                     ·
1.75#d-#8   4.82#d+##                                      ·
1.8##d-#8   4.872d+##                                      ·
1.#5#d-#8   4.889d+##                                      ·
1.9##d-#8   4.857d+##                                      ·
1.95#d-#8   4.749d+##                                     ·
2.###d-#8   4.575d+##                                    ·
2.#5#d-#8   4.298d+##                                  ·
2.1##d-#8   3.92#d+##                                ·
2.15#d-#8   3.464d+##                             ·
2.2##d-#8   2.941d+##                          ·
2.25#d-#8   2.384d+##                      ·
2.3##d-#8   1.812d+##                  ·
2.35#d-#8   1.324d+##              ·
2.4##d-#8   8.93#d-#1         ·
2.45#d-#8   5.#79d-#1      ·
2.5##d-#8   3.669d-#1    ·
2.55#d-#8   2.#65d-#1   ·
2.6##d-#8   1.28#d-#1  ·
2.65#d-#8   7.123d-#2  ·
2.7##d-#8   3.98#d-#2  ·
2.75#d-#8   2.2#4d-#2  ·
2.8##d-#8   1.326d-#2  ·
2.85#d-#8   6.973d-#3  *
2.9##d-#8   3.966d-#3  *
2.95#d-#8   2.2#1d-#3  *
3.###d-#8   1.#97d-#3  *
3.#5#d-#8   6.5#2d-#4  *
3.1##d-#8   3.476d-#4  *
3.15#d-#8   1.#15d-#4  *
3.2##d-#8   1.#56d-#4  *
3.25#d-#8   5.369d-#5  *
3.3##d-#8   3.#24d-#5  *
3.35#d-#8   1.662d-#5  *
3.4##d-#8   8.2##d-#6  *
3.45#d-#8   4.949d-#6  *
3.5##d-#8   2.636d-#6  *
3.55#d-#8   1.411d-#6  *
3.6##d-#8   8.556d-#7  *
3.65#d-#8   4.77#d-#7  *
3.7##d-#8   3.#73d-#7  *
3.75#d-#8   2.#9#d-#7  *
3.8##d-#8   1.466d-#7  *
3.85#d-#8   1.251d-#7  *
3.9##d-#8   1.#86d-#7  *
3.95#d-#8   9.981d-#8  *
4.###d-#8   9.537d-#8  *
       *-------------------------------------------------------------------------*
```

Figure C-36.   SPICE Plot Section 2 Input 101 Two
               Node Precharge with Basic Widths.

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0   CMOS/SOS PRECHARGED BITSLICE SECTION 2 TRANSIENT ANALYSIS

0****   INPUT LISTING   TEMPERATURE =   27.000 DEG C

0***

```
 .WIDTH OUT=80
 .OPTIONS ITL1=500 ITL5=0
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
+LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
+LEVEL=1
VDD 1 0 DC 5V
M1  1 3 2 0 NMOS L=5.0U W=10.0U
M2  1 3 5 0 NMOS L=5.0U W=10.0U
M3  2 6 1 1 PMOS L=5.0U W=20.0U
M4  5 6 1 1 PMOS L=5.0U W=20.0U
M5  1 7 5 1 PMOS L=5.0U W=10.0U
M6  10 9 0 0 NMOS L=5.0U W=15.0U
M7  10 7 5 0 NMOS L=5.0U W=15.0U
M8  1 9 5 1 PMOS L=5.0U W=10.0U
M9  1 5 11 1 PMOS L=5.0U W=10.0U
M10 0 12 9 0 NMOS L=5.0U W=15.0U
M11 13 2 0 0 NMOS L=5.0U W=15.0U
M12 13 5 11 0 NMOS L=5.0U W=15.0U
M13 1 12 9 1 PMOS L=5.0U W=30.0U
M14 1 2 11 1 PMOS L=5.0U W=10.0U
M15 1 14 2 1 PMOS L=5.0U W=10.0U
M16 15 12 0 0 NMOS L=5.0U W=15.0U
M17 15 14 2 0 NMOS L=5.0U W=15.0U
M18 1 12 2 1 PMOS L=5.0U W=10.0U
M19 0 7 14 0 NMOS L=5.0U W=15.0U
M20 1 7 14 1 PMOS L=5.0U W=30.0U
C21 1 0 0.1135PF
C22 12 0 0.279PF
C23 0 0 0.951PF
C24 7 0 0.183PF
C25 14 0 0.100PF
C26 2 0 0.288PF
C27 11 0 0.134PF
C28 5 0 0.260PF
C29 9 0 0.101PF
C30 6 0 0.103PF
C31 3 0 0.103PF
VIN1 12 0 PULSE (5V 5V 5NS 0NS 0NS 10NS)
VIN2 7 0 PULSE (0V 5V 5NS 0NS 0NS 10NS)
VP1 3 0 PULSE (0V 5V 4NS 0NS 0NS 2NS)
VP1BAR 6 0 PULSE (5V 0V 4NS 0NS 0NS 2NS)
.TRAN 0.5NS 40NS
.PLOT TRAN V(11) (0V,5V)
.END
```

```
1*******12/#1/#4 ******** SPICE 2G.1 (15OCT##)  ********#4:23:#9*****

#       CMOS/SOS PRECHARGED BITSLICE SECTION 2 TRANSIENT ANALYSIS X2

#****    TRANSIENT ANALYSIS              TEMPERATURE =  27.### DEG C

#*************************************************************************

X
    TIME      V(11)

X               #.     d+##      1.25#d+##     2.5##d+##     3.75#d+##  5.###d+##
 #.    d+##   5.###d+##  .                                                    ..
 5.###d-1#   5.###d+##  .                                                     :
 1.###d-#9   5.###d+##  .                                                     :
 1.5##d-#9   5.###d+##  .                                                     :
 2.###d-#9   5.###d+##  .                                                     :
 2.5##d-#9   5.###d+##  .                                                     :
 3.###d-#9   5.###d+##  .                                                     :
 3.5##d-#9   5.###d+##  .                                                     :
 4.###d-#9   5.###d+##  .                                                     :
 4.5##d-#9   5.###d+##  .                                                     :
 5.###d-#9   5.###d+##  .                                                     :
 5.5##d-#9   4.973d+##  .                                                    .
 6.###d-#9   4.#46d+##  .                                                  . .
 6.5##d-#9   4.517d+##  .                                              .  .
 7.###d-#9   3.999d+##  .                                          .
 7.5##d-#9   3.4#9d+##  .                                     .
 #.###d-#9   2.777d+##  .                                .
 #.5##d-#9   2.142d+##  .                           .
 9.###d-#9   1.565d+##  .                       .
 9.5##d-#9   1.##6d+##  .                    .
 1.###d-##   6.941d-#1  .                 .
 1.#5#d-##   4.49#d-#1  .             .
 1.1##d-##   2.665d-#1  .           .
 1.15#d-##   1.496d-#1  .         .
 1.2##d-##   8.93#d-#2  .        .
 1.25#d-##   5.#12d-#2  . .
 1.3##d-##   2.766d-#2  .
 1.35#d-##   1.533d-#2  .
 1.4##d-##   9.13#d-#3  .
 1.45#d-##   4.713d-#3  .
 1.5##d-##   2.662d-#3  .
 1.55#d-##   1.35#d-#3  .
 1.6##d-##   7.724d-#4  .
 1.65#d-##   4.437d-#4  .
 1.7##d-##   2.61#d-#4  .
 1.75#d-##   4.4##d-#4  .
 1.8##d-##   8.487d-#4  .
 1.85#d-##   1.161d-#2  .
 1.9##d-##   3.7##d-#2  .
 1.95#d-##   7.912d-#2  .
 2.###d-##   1.692d-#1  . .
 2.#5#d-##   2.918d-#1  .   .
 2.1##d-##   4.#26d-#1  .      .
 2.15#d-##   7.624d-#1  .        .
 2.2##d-##   1.#95d+##  .          .
 2.25#d-##   1.541d+##  .             .
 2.3##d-##   2.#16d+##  .                .
 2.35#d-##   2.536d+##  .                   .
 2.4##d-##   3.#39d+##  .                      .
 2.45#d-##   3.46#d+##  .                        .
 2.5##d-##   3.#54d+##  .                          .
 2.55#d-##   4.161d+##  .                            .
 2.6##d-##   4.39#d+##  .                              .
 2.65#d-##   4.56#d+##  .                               .
 2.7##d-C#   4.7##d+##  .                                .
 2.75#d-##   4.793d+##  .                                 .
 2.8##d-##   4.861d+##  .                                  .
 2.85#d-##   4.9#2d+##  .                                   .
 2.9##d-##   4.935d+##  .                                   .
 2.95#d-##   4.95#d+##  .                                    .
 3.###d-##   4.969d+##  .                                    .
 3.#5#d-##   4.98#d+##  .                                    :
 3.1##d-##   4.986d+##  .                                    :
 3.15#d-##   4.991d+##  .                                    :
 3.2##d-##   4.994d+##  .                                    :
 3.25#d-##   4.996d+##  .                                    :
 3.3##d-##   4.997d+##  .                                    :
 3.35#d-##   4.998d+##  .                                    :
 3.4##d-##   4.999d+##  .                                    :
 3.45#d-##   4.999d+##  .                                    :
 3.5##d-##   4.999d+##  .                                    :
 3.55#d-##   5.###d+##  .                                    :
 3.6##d-##   5.###d+##  .                                    :
 3.65#d-##   5.###d+##  .                                    :
 3.7##d-##   5.###d+##  .                                    :
 3.75#d-##   5.###d+##  .                                    :
 3.8##d-##   5.###d+##  .                                    :
 3.85#d-##   5.###d+##  .                                    :
 3.9##d-##   5.###d+##  .                                    :
 3.95#d-##   5.###d+##  .                                    :
 4.###d-08   5.###d+##  .                                    .
```

Figure C-37.   SPICE Plot Section 2 Input 010 Two
              Node Precharge with Widths x2.

Ø   CMOS/SOS PRECHARGED BITSLICE SECTION 2 TRANSIENT ANALYSIS

Ø****   INPUT LISTING   TEMPERATURE =   27.ØØØ DEG C

Ø***

```
.WIDTH OUT=8Ø
.OPTIONS ITL1=5ØØ ITL5=Ø
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
+LEVEL=1
VDD 1 Ø DC 5V
M1  1  3  2  Ø NMOS L=5.ØU W=1Ø.ØU
M2  1  3  5  Ø NMOS L=5.ØU W=1Ø.ØU
M3  2  6  1  1 PMOS L=5.ØU W=2Ø.ØU
M4  5  6  1  1 PMOS L=5.ØU W=2Ø.ØU
M5  1  7  5  1 PMOS L=5.ØU W=1Ø.ØU
M6  1Ø 9  Ø  Ø NMOS L=5.ØU W=15.ØU
M7  1Ø 7  5  Ø NMOS L=5.ØU W=15.ØU
M8  1  9  5  1 PMOS L=5.ØU W=1Ø.ØU
M9  1  5  11 1 PMOS L=5.ØU W=1Ø.ØU
M1Ø Ø  12 9  Ø NMOS L=5.ØU W=15.ØU
M11 13 2  Ø  Ø NMOS L=5.ØU W=15.ØU
M12 13 5  11 Ø NMOS L=5.ØU W=15.ØU
M13 1  12 9  1 PMOS L=5.ØU W=3Ø.ØU
M14 1  2  11 1 PMOS L=5.ØU W=1Ø.ØU
M15 1  14 2  1 PMOS L=5.ØU W=1Ø.ØU
M16 15 12 Ø  Ø NMOS L=5.ØU W=15.ØU
M17 15 14 2  Ø NMOS L=5.ØU W=15.ØU
M18 1  12 2  1 PMOS L=5.ØU W=1Ø.ØU
M19 Ø  7  14 Ø NMOS L=5.ØU W=15.ØU
M2Ø 1  7  14 1 PMOS L=5.ØU W=3Ø.ØU
C21 1  Ø Ø.1135PF
C22 12 Ø Ø.279PF
C23 Ø  Ø Ø.951PF
C24 7  Ø Ø.183PF
C25 14 Ø Ø.1ØØPF
C26 2  Ø Ø.288PF
C27 11 Ø Ø.134PF
C28 5  Ø Ø.26ØPF
C29 9  Ø Ø.1Ø1PF
C3Ø 6  Ø Ø.1Ø3PF
C31 3  Ø Ø.1Ø3PF
VIN1 12 Ø PULSE (5V 5V 5NS ØNS ØNS 1ØNS)
VIN2 7  Ø PULSE (5V ØV 5NS ØNS ØNS 1ØNS)
VP1 3  Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS)
VP1BAR 6 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
.TRAN Ø.5NS 4ØNS
.PLOT TRAN V(11) (ØV,5V)
.END
```

```
0       CMOS/SOS PRECHARGED BITSLICE SECTION 2 TRANSIENT ANALYSIS X2

0****     TRANSIENT ANALYSIS              TEMPERATURE =   27.000 DEG C

0*************************************************************************

x
    TIME      V(11)

x              0.   d+00   1.250d+00    2.500d+00    3.750d+00  5.000d+00
    0.   d+00  9.035d-00  *
    5.000d-10  9.035d-00  *
    1.000d-09  9.035d-00  *
    1.500d-09  9.035d-00  *
    2.000d-09  9.035d-00  *
    2.500d-09  9.035d-00  *
    3.000d-09  9.035d-00  *
    3.500d-09  9.035d-00  *
    4.000d-09  9.035d-00  *
    4.500d-09  9.035d-00  *
    5.000d-09  9.035d-00  *
    5.500d-09  9.035d-00  *
    6.000d-09  9.047d-00  *
    6.500d-09  9.133d-00  *
    7.000d-09  9.326d-00  *
    7.500d-09  4.210d-05  *
    8.000d-09  4.550d-03  *
    8.500d-09  2.254d-02  *
    9.000d-09  6.160d-02  .*
    9.500d-09  1.240d-01  .*
    1.000d-08  2.246d-01     .
    1.050d-08  3.779d-01       .
    1.100d-08  6.209d-01         .
    1.150d-08  9.148d-01            .
    1.200d-08  1.325d+00              .
    1.250d-08  1.773d+00                 .
    1.300d-08  2.263d+00                    .
    1.350d-08  2.798d+00                       .
    1.400d-08  3.263d+00                          .
    1.450d-08  3.686d+00                            .
    1.500d-08  4.012d+00                              .
    1.550d-08  4.303d+00                               .
    1.600d-08  4.503d+00                                .
    1.650d-08  4.648d+00                                 .
    1.700d-08  4.749d+00                                  .
    1.750d-08  4.820d+00                                  .
    1.800d-08  4.865d+00                                   .
    1.850d-08  4.885d+00                                   .
    1.900d-08  4.847d+00                                  .
    1.950d-08  4.755d+00                                 .
    2.000d-08  4.564d+00                                .
    2.050d-08  4.279d+00                              .
    2.100d-08  3.933d+00                            .
    2.150d-08  3.451d+00                         .
    2.200d-08  2.933d+00                      .
    2.250d-08  2.364d+00                   .
    2.300d-08  1.815d+00                .
    2.350d-08  1.299d+00             .
    2.400d-08  8.966d-01          .
    2.450d-08  5.831d-01       .
    2.500d-08  3.406d-01     .
    2.550d-08  2.184d-01   .
    2.600d-08  1.243d-01  .
    2.650d-08  6.978d-02  .*
    2.700d-08  4.068d-02  *
    2.750d-08  2.285d-02  *
    2.800d-08  1.178d-02  *
    2.850d-08  7.297d-03  *
    2.900d-08  3.014d-03  *
    2.950d-08  2.069d-03  *
    3.000d-08  1.183d-03  *
    3.050d-08  5.984d-04  *
    3.100d-08  3.459d-04  *
    3.150d-08  1.072d-04  *
    3.200d-08  9.195d-05  *
    3.250d-08  5.594d-05  *
    3.300d-08  2.903d-05  *
    3.350d-08  1.562d-05  *
    3.400d-08  8.094d-06  *
    3.450d-08  4.496d-06  *
    3.500d-08  2.624d-06  *
    3.550d-08  1.452d-06  *
    3.600d-08  7.548d-07  *
    3.650d-08  4.935d-07  *
    3.700d-08  2.984d-07  *
    3.750d-08  2.018d-07  *
    3.800d-08  1.534d-07  *
    3.850d-08  1.219d-07  *
    3.900d-08  1.085d-07  *
    3.950d-08  1.041d-07  *
    4.000d-08  9.512d-08  *
```

Figure C-38.   SPICE Plot Section 2 Input 101 Two
              Node Precharge with Widths x2.

Ø   CMOS/SOS PRECHARGED BITSLICE SECTION 2 TRANSIENT ANALYSIS

Ø****   INPUT LISTING   TEMPERATURE =   27.ØØØ DEG C

Ø***

```
.WIDTH OUT=8Ø
.OPTIONS ITL1=5ØØ ITL5=Ø
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
+LEVEL=1
VDD 1 Ø DC 5V
M1 1 3 2 Ø NMOS L=5.ØU W=15.ØU
M2 1 3 5 Ø NMOS L=5.ØU W=15.ØU
M3 2 6 1 1 PMOS L=5.ØU W=3Ø.ØU
M4 5 6 1 1 PMOS L=5.ØU W=3Ø.ØU
M5 1 7 5 1 PMOS L=5.ØU W=1Ø.ØU
M6 1Ø 9 Ø Ø NMOS L=5.ØU W=15.ØU
M7 1Ø 7 5 Ø NMOS L=5.ØU W=15.ØU
M8 1 9 5 1 PMOS L=5.ØU W=1Ø.ØU
M9 1 5 11 1 PMOS L=5.ØU W=1Ø.ØU
M1Ø Ø 12 9 Ø NMOS L=5.ØU W=15.ØU
M11 13 2 Ø Ø NMOS L=5.ØU W=15.ØU
M12 13 5 11 Ø NMOS L=5.ØU W=15.ØU
M13 1 12 9 1 PMOS L=5.ØU W=3Ø.ØU
M14 1 2 11 1 PMOS L=5.ØU W=1Ø.ØU
M15 1 14 2 1 PMOS L=5.ØU W=1Ø.ØU
M16 15 12 Ø Ø NMOS L=5.ØU W=15.ØU
M17 15 14 2 Ø NMOS L=5.ØU W=15.ØU
M18 1 12 2 1 PMOS L=5.ØU W=1Ø.ØU
M19 Ø 7 14 Ø NMOS L=5.ØU W=15.ØU
M2Ø 1 7 14 1 PMOS L=5.ØU W=3Ø.ØU
C21 1 Ø Ø.1135PF
C22 12 Ø Ø.279PF
C23 Ø Ø Ø.951PF
C24 7 Ø Ø.183PF
C25 14 Ø Ø.1ØØPF
C26 2 Ø Ø.288PF
C27 11 Ø Ø.134PF
C28 5 Ø Ø.25ØPF
C29 9 Ø Ø.1Ø1PF
C3Ø 6 Ø Ø.1Ø3PF
C31 3 Ø Ø.1Ø3PF
VIN1 12 Ø PULSE (5V 5V 5NS ØNS ØNS 1ØNS)
VIN2 7 Ø PULSE (ØV 5V 5NS ØNS ØNS 1ØNS)
VP1 3 Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS)
VPIBAR 6 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
.TRAN Ø.5NS 4ØNS
.PLOT TRAN V(11) (ØV,5V)
.END
```

\# CMOS/SOS PRECHARGED BITSLICE SECTION 2 TRANSIENT ANALYSIS *X3*

#•••• TRANSIENT ANALYSIS TEMPERATURE • 27.### DEG C

#•••

```
X
    TIME      V(11)

X             #.    d+##     1.25#d+##     2.5##d+##     3.75#d+## 5.###d+##
      #.   d+##  5.###d+##  - - - - - - - - - - - - - - - - - - - - - - - - •
    5.###d-1#  5.###d+##                                                   •
    1.###d-#9  5.###d+##                                                   •
    1.5##d-#9  5.###d+##                                                   •
    2.###d-#9  5.###d+##                                                   •
    2.5##d-#9  5.###d+##                                                   •
    3.###d-#9  5.###d+##                                                   •
    3.5##d-#9  5.###d+##                                                   •
    4.###d-#9  5.###d+##                                                   •
    4.5##d-#9  5.###d+##                                                   •
    5.###d-#9  4.989d+##                                                 •
    5.5##d-#9  4.864d+##                                               •
    6.###d-#9  4.52#d+##                                            •
    6.5##d-#9  3.959d+##                                        •
    7.###d-#9  3.261d+##                                    •
    7.5##d-#9  2.544d+##                                •
    8.###d-#9  1.87#d+##                            •
    8.5##d-#9  1.3#6d+##                        •
    9.###d-#9  8.474d-#1                     •
    9.5##d-#9  5.412d-#1                  •
    1.###d-#8  3.26#d-#1               •
    1.#5#d-#8  1.753d-#1             •
    1.1##d-#8  1.#64d-#1          •
    1.15#d-#8  5.895d-#2        •
    1.2##d-#8  3.322d-#2       •
    1.25#d-#8  1.787d-#2      •
    1.3##d-#8  1.#61d-#2      •
    1.35#d-#8  5.674d-#3     •
    1.4##d-#8  2.9#7d-#3     •
    1.45#d-#8  1.72#d-#3     •
    1.5##d-#8  8.73#d-#4     •
    1.55#d-#8  4.976d-#4    •
    1.6##d-#8  2.593d-#4    •
    1.65#d-#8  1.466d-#4    •
    1.7##d-#8  8.745d-#5    •
    1.75#d-#8  2.2#1d-#4    •
    1.###d-#8  4.796d-#4    •
    1.#5#d-#8  1.#1#d-#2    •
    1.9##d-#8  3.373d-#2    •
    1.95#d-#8  7.316d-#2     •
    2.###d-#9  1.592d-#1     •
    2.#5#d-#8  2.766d-#1      •
    2.1##d-#8  4.596d-#1        •
    2.15#d-#8  7.31#d-#1          •
    2.2##d-#8  1.#55d+##           •
    2.25#d-#8  1.494d+##              •
    2.3##d-#8  1.964d+##                •
    2.35#d-#8  2.4#4d+##                  •
    2.4##d-#8  2.969d+##                     •
    2.45#d-#8  3.425d+##                       •
    2.5##d-#8  3.824d+##                         •
    2.55#d-#8  4.1#8d+##                           •
    2.6##d-#8  4.37#d+##                             •
    2.65#d-#8  4.568d+##                              •
    2.7##d-#8  4.6##d+##                               •
    2.75#d-#8  4.786d+##                                 •
    2.8##d-#8  4.855d+##                                  •
    2.#5#d-#8  4.898d+##                                  •
    2.9##d-#8  4.933d+##                                   •
    2.95#d-#8  4.953d+##                                   •
    3.###d-#8  4.968d+##                                    •
    3.#5#d-#8  4.979d+##                                    •
    3.1##d-#8  4.985d+##                                    •
    3.15#d-#8  4.99#d+##                                    •
    3.2##d-#8  4.994d+##                                    •
    3.25#d-#8  4.996d+##                                    •
    3.3##d-#8  4.997d+##                                    •
    3.35#d-#8  4.998d+##                                    •
    3.1##d-#8  4.999d+##                                    •
    3.45#d-#8  4.999d+##                                    •
    3.5##d-#8  4.999d+##                                    •
    3.75#d-#8  5.###d+##                                    •
    3.6##d-#8  5.#1#d+##                                    •
    3.65#d-#8  5.###d+##                                    •
    3.7##d-#8  5.###d+##                                    •
    3.75#d-#8  5.###d+##                                    •
    3.8##d-#8  5.###d+##                                    •
    3.85#d-#8  5.###d+##                                    •
    3.9##d-#8  5.###d+##                                    •
    3.95#d-#8  5.###d+##                                    •
    4.###d-#8  5.###d+##  - - - - - - - - - - - - - - - - - - - - - - - - •
```

Figure C-39. SPICE Plot Section 2 Input 010 Two
Node Precharge with Widths x3.

```
.WIDTH OUT=8Ø
.OPTIONS ITL1=5ØØ ITL5=Ø
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
+LEVEL=1
VDD 1 Ø DC 5V
M1  1 3 2 Ø NMOS L=5.ØU W=15.ØU
M2  1 3 5 Ø NMOS L=5.ØU W=15.ØU
M3  2 6 1 1 PMOS L=5.ØU W=3Ø.ØU
M4  5 6 1 1 PMOS L=5.ØU W=3Ø.ØU
M5  1 7 5 1 PMOS L=5.ØU W=1Ø.ØU
M6  1Ø 9 Ø Ø NMOS L=5.ØU W=15.ØU
M7  1Ø 7 5 Ø NMOS L=5.ØU W=15.ØU
M8  1 9 5 1 PMOS L=5.ØU W=1Ø.ØU
M9  1 5 11 1 PMOS L=5.ØU W=1Ø.ØU
M1Ø Ø 12 9 Ø NMOS L=5.ØU W=15.ØU
M11 13 2 Ø Ø NMOS L=5.ØU W=15.ØU
M12 13 5 11 Ø NMOS L=5.ØU W=15.ØU
M13 1 12 9 1 PMOS L=5.ØU W=3Ø.ØU
M14 1 2 11 1 PMOS L=5.ØU W=1Ø.ØU
M15 1 14 2 1 PMOS L=5.ØU W=1Ø.ØU
M16 15 12 Ø Ø NMOS L=5.ØU W=15.ØU
M17 15 14 2 Ø NMOS L=5.ØU W=15.ØU
M18 1 12 2 1 PMOS L=5.ØU W=1Ø.ØU
M19 Ø 7 14 Ø NMOS L=5.ØU W=15.ØU
M2Ø 1 7 14 1 PMOS L=5.ØU W=3Ø.ØU
C21 1 Ø Ø.1135PF
C22 12 Ø Ø.279PF
C23 Ø Ø Ø.951PF
C24 7 Ø Ø.183PF
C25 14 Ø Ø.1ØØPF
C26 2 Ø Ø.288PF
C27 11 Ø Ø.134PF
C28 5 Ø Ø.26ØPF
C29 9 Ø Ø.1Ø1PF
C3Ø 6 Ø Ø.1Ø3PF
C31 3 Ø Ø.1Ø3PF
VIN1 12 Ø PULSE (5V 5V 5NS ØNS ØNS 1ØNS)
VIN2 7 Ø PULSE (5V ØV 5NS ØNS ØNS 1ØNS)
VP1 3 Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS)
VP1BAR 6 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
.TRAN Ø.5NS 4ØNS
.PLOT TRAN V(11) (ØV,5V)
.END
```

8   CMOS/SOS PRECHARGED BITSLICE SECTION 2 TRANSIENT ANALYSIS *3

0****   TRANSIENT ANALYSIS   TEMPERATURE =   27.000 DEG C

0***

```
X
   TIME      V(11)

X                    8.    d+00     1.250d+00    2.500d+00     3.750d+00  5.000d+00

0.    d+00   9.035d-08 *                    .                    .                    .
5.000d-10   9.035d-08 *                    .                    .                    .
1.000d-09   9.035d-08 *                    .                    .                    .
1.500d-09   9.035d-08 *                    .                    .                    .
2.000d-09   9.035d-08 *                    .                    .                    .
2.500d-09   9.035d-08 *                    .                    .                    .
3.000d-09   9.035d-08 *                    .                    .                    .
3.500d-09   9.035d-08 *                    .                    .                    .
4.000d-09   9.035d-08 *                    .                    .                    .
4.500d-09   9.035d-08 *                    .                    .                    .
5.000d-09   9.035d-08 *                    .                    .                    .
5.500d-09   9.035d-08 *                    .                    .                    .
6.000d-09   9.047d-08 *                    .                    .                    .
6.500d-09   9.124d-08 *                    .                    .                    .
7.000d-09   9.299d-08 *                    .                    .                    .
7.500d-09   6.693d-06 *                    .                    .                    .
8.000d-09   3.762d-03 *                    .                    .                    .
8.500d-09   2.000d-02 *                    .                    .                    .
9.000d-09   4.678d-02 .*                   .                    .                    .
9.500d-09   1.150d-01 .*                   .                    .                    .
1.000d-08   2.196d-01   *                  .                    .                    .
1.050d-08   3.569d-01     *                .                    .                    .
1.100d-08   5.913d-01        *             .                    .                    .
1.150d-08   8.761d-01           *          .                    .                    .
1.200d-08   1.278d+00              *       .                    .                    .
1.250d-08   1.727d+00                  *   .                    .                    .
1.300d-08   2.219d+00                     *.                    .                    .
1.350d-08   2.736d+00                      .   *                .                    .
1.400d-08   3.222d+00                      .       *            .                    .
1.450d-08   3.625d+00                      .          *         .                    .
1.500d-08   3.985d+00                      .             *      .                    .
1.550d-08   4.274d+00                      .                *   .                    .
1.600d-08   4.482d+00                      .                  * .                    .
1.650d-08   4.634d+00                      .                    .*                   .
1.700d-08   4.739d+00                      .                    . *                  .
1.750d-08   4.811d+00                      .                    .   *                .
1.800d-08   4.857d+00                      .                    .    *               .
1.850d-08   4.879d+00                      .                    .     *              .
1.900d-08   4.849d+00                      .                    .    *               .
1.950d-08   4.739d+00                      .                    . *                  .
2.000d-08   4.568d+00                      .                    *                    .
2.050d-08   4.284d+00                      .                  * .                    .
2.100d-08   3.987d+00                      .               *   .                    .
2.150d-08   3.472d+00                      .          *        .                    .
2.200d-08   2.925d+00                      .      *            .                    .
2.250d-08   2.368d+00                      .  *                .                    .
2.300d-08   1.798d+00                  *   .                    .                    .
2.350d-08   1.312d+00              *       .                    .                    .
2.400d-08   8.799d-01           *          .                    .                    .
2.450d-08   5.763d-01        *             .                    .                    .
2.500d-08   3.613d-01      *               .                    .                    .
2.550d-08   2.019d-01   *                  .                    .                    .
2.600d-08   1.272d-01  .*                  .                    .                    .
2.650d-08   6.983d-02 .*                   .                    .                    .
2.700d-08   3.981d-02 *                    .                    .                    .
2.750d-08   2.242d-02 *                    .                    .                    .
2.800d-08   1.309d-02 *                    .                    .                    .
2.850d-08   6.788d-03 *                    .                    .                    .
2.900d-08   3.932d-03 *                    .                    .                    .
2.950d-08   2.153d-03 *                    .                    .                    .
3.000d-08   1.065d-03 *                    .                    .                    .
3.050d-08   6.488d-04 *                    .                    .                    .
3.100d-08   3.389d-04 *                    .                    .                    .
3.150d-08   1.814d-04 *                    .                    .                    .
3.200d-08   1.037d-04 *                    .                    .                    .
3.250d-08   5.222d-05 *                    .                    .                    .
3.300d-08   2.998d-05 *                    .                    .                    .
3.350d-08   1.625d-05 *                    .                    .                    .
3.400d-08   7.998d-06 *                    .                    .                    .
3.450d-08   4.079d-06 *                    .                    .                    .
3.500d-08   2.571d-06 *                    .                    .                    .
3.550d-08   1.411d-06 *                    .                    .                    .
3.600d-08   8.412d-07 *                    .                    .                    .
3.650d-08   4.664d-07 *                    .                    .                    .
3.700d-08   3.054d-07 *                    .                    .                    .
3.750d-08   2.063d-07 *                    .                    .                    .
3.800d-08   1.469d-07 *                    .                    .                    .
3.850d-08   1.246d-07 *                    .                    .                    .
3.900d-08   1.081d-07 *                    .                    .                    .
3.950d-08   9.961d-08 *                    .                    .                    .
4.000d-08   9.528d-08 *- - - - - - - - - - . - - - - - - - - - . - - - - - - - - - .
```

Figure C-40.   SPICE Plot Section 2 Input 101 Two
                Node Precharge with Widths x3.
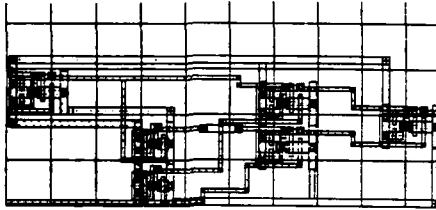
Figure C-41. Basic Section 3 CLL Plot.
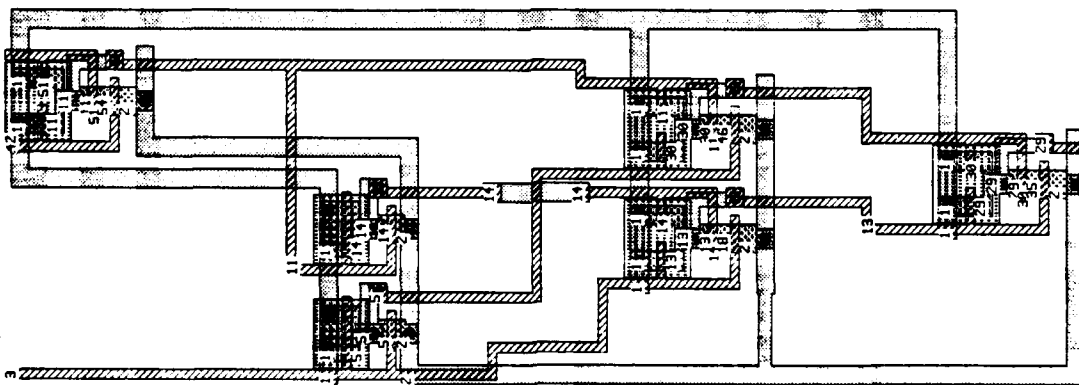
Figure C-42. Basic Section 3 Node Plot.

Table C-7

BITSLICE SECTION 3 NODE LIST

GND	Ø
Vdd	1
NMOS	Ø
PMOS	1
11	2
51	3
1	4
3Ø	5
2	6
42	7
54	8
5	9
46	1Ø
29	11
13	12
35	13
14	14
3	15
18	16

```
.WIDTH OUT=8∅
.OPTIONS ITL1=5∅∅ ITL5=∅
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4∅∅ NSUB=2.5E16 LD=∅.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2∅∅ NSUB=3E15 LD=∅.7UM)
+LEVEL=1
VDD 1 ∅ DC 5V
M1  1 3 2 1 PMOS L=5.∅U W=1∅.∅U
M2  1 2 5 1 PMOS L=5.∅U W=1∅.∅U
M3  8 7 ∅ ∅ NMOS L=5.∅U W=15.∅U
M4  8 3 2 ∅ NMOS L=5.∅U W=15.∅U
M5  1 7 2 1 PMOS L=5.∅U W=1∅.∅U
M6  1∅ 9 ∅ ∅ NMOS L=5.∅U W=15.∅U
M7  1∅ 2 5 ∅ NMOS L=5.∅U W=15.∅U
M8  1 9 5 1 PMOS L=5.∅U W=1∅.∅U
M9  1 5 11 1 PMOS L=5.∅U W=1∅.∅U
M1∅ 1∅ 12 ∅ ∅ NMOS L=5.∅U W=15.∅U
M11 1∅ 5 11 ∅ NMOS L=5.∅U W=15.∅U
M12 1 12 11 1 PMOS L=5.∅U W=1∅.∅U
M13 1 14 12 1 PMOS L=5.∅U W=1∅.∅U
M14 ∅ 2 14 ∅ NMOS L=5.∅U W=15.∅U
M15 16 15 ∅ ∅ NMOS L=5.∅U W=15.∅U
M16 16 14 12 ∅ NMOS L=5.∅U W=15.∅U
M17 1 2 14 1 PMOS L=5.∅U W=3∅.∅U
M18 1 15 12 1 PMOS L=5.∅U W=1∅.∅U
M19 ∅ 16 9 ∅ NMOS L=5.∅U W=15.∅U
M2∅ 1 15 9 1 PMOS L=5.∅U W=3∅.∅U
C21 1 ∅ ∅.5∅1PF
C22 ∅ ∅ ∅.4∅5PF
C23 15 ∅ ∅.143PF
C24 9 ∅ ∅.141PF
C25 2 ∅ ∅.2∅∅PF
C26 12 ∅ ∅.13∅PF
C27 14 ∅ ∅.1∅4PF
C28 11 ∅ ∅.134PF
C29 5 ∅ ∅.137PF
VIN1 15 ∅ PULSE (∅V 5V 5NS ∅NS ∅NS 1∅NS)
VCAP ∅ ∅ PULSE (∅V ∅V ∅NS ∅NS ∅NS 1∅NS)
VSEL 7 ∅ PULSE (5V 5V ∅NS ∅NS ∅NS 1∅NS)
.TRAN ∅.5NS 4.∅NS
.PLOT TRAN V(1∅) (∅V,5V)
.END
```

```
1********12/01/84 ********  SPICE 2G.1 (15OCT80)  ********01:15:15*****

0           CMOS/SOS BITSLICE SECTION 3 BASIC TRANSIENT ANALYSIS

0****       TRANSIENT ANALYSIS               TEMPERATURE =   27.000 DEG C

0***************************************************************************

X
     TIME       V(11)
X               0.    d+00     1.250d+00     2.500d+00     3.750d+00  5.000d+00

 0.    d+00   5.000d+00 :
 5.000d-10   5.000d+00 .
 1.000d-09   5.000d+00 .
 1.500d-09   5.000d+00 .
 2.000d-09   5.000d+00 .
 2.500d-09   5.000d+00 .
 3.000d-09   5.000d+00 .
 3.500d-09   5.000d+00 .
 4.000d-09   5.000d+00 .
 4.500d-09   5.000d+00 .
 5.000d-09   5.000d+00 .
 5.500d-09   5.000d+00 .
 6.000d-09   5.000d+00 .
 6.500d-09   5.000d+00 .
 7.000d-09   5.000d+00 .
 7.500d-09   4.990d+00 .
 8.000d-09   4.921d+00 .
 8.500d-09   4.741d+00 .
 9.000d-09   4.418d+00 .
 9.500d-09   4.009d+00 .
 1.000d-08   3.451d+00 .
 1.050d-08   2.850d+00 .
 1.100d-08   2.174d+00 .
 1.150d-08   1.541d+00 .
 1.200d-08   1.011d+00 .
 1.250d-08   6.650d-01 .
 1.300d-08   3.798d-01 .
 1.350d-08   2.342d-01 .
 1.400d-08   1.245d-01 .
 1.450d-08   6.729d-02 .
 1.500d-08   3.760d-02 *
 1.550d-08   2.075d-02 *
 1.600d-08   1.174d-02 *
 1.650d-08   6.714d-03 *
 1.700d-08   3.939d-03 *
 1.750d-08   1.174d-02 *
 1.800d-08   5.589d-02 .*
 1.850d-08   1.502d-01 .*
 1.900d-08   4.003d-01 .*
 1.950d-08   7.393d-01 .
 2.000d-08   1.245d+00 .
 2.050d-08   1.814d+00 .
 2.100d-08   2.426d+00 .
 2.150d-08   2.990d+00 .
 2.200d-08   3.490d+00 .
 2.250d-08   3.893d+00 .
 2.300d-08   4.213d+00 .
 2.350d-08   4.444d+00 .
 2.400d-08   4.607d+00 .
 2.450d-08   4.737d+00 .
 2.500d-08   4.815d+00 .
 2.550d-08   4.875d+00 .
 2.600d-08   4.918d+00 .
 2.650d-08   4.942d+00 .
 2.700d-08   4.962d+00 .
 2.750d-08   4.974d+00 .
 2.800d-08   4.982d+00 .
 2.850d-08   4.988d+00 .
 2.900d-08   4.992d+00 .
 2.950d-08   4.995d+00 .
 3.000d-08   4.996d+00 .
 3.050d-08   4.998d+00 .
 3.100d-08   4.998d+00 .
 3.150d-08   4.999d+00 .
 3.200d-08   4.999d+00 .
 3.250d-08   5.000d+00 .
 3.300d-08   5.000d+00 .
 3.350d-08   5.000d+00 .
 3.400d-08   5.000d+00 .
 3.450d-08   5.000d+00 .
 3.500d-08   5.000d+00 .
 3.550d-08   5.000d+00 .
 3.600d-08   5.000d+00 .
 3.650d-08   5.000d+00 .
 3.700d-08   5.000d+00 .
 3.750d-08   5.000d+00 .
 3.800d-08   5.000d+00 .
 3.850d-08   5.000d+00 .
 3.900d-08   5.000d+00 .
 3.950d-08   5.000d+00 .
 4.000d-08   5.000d+00 .
```
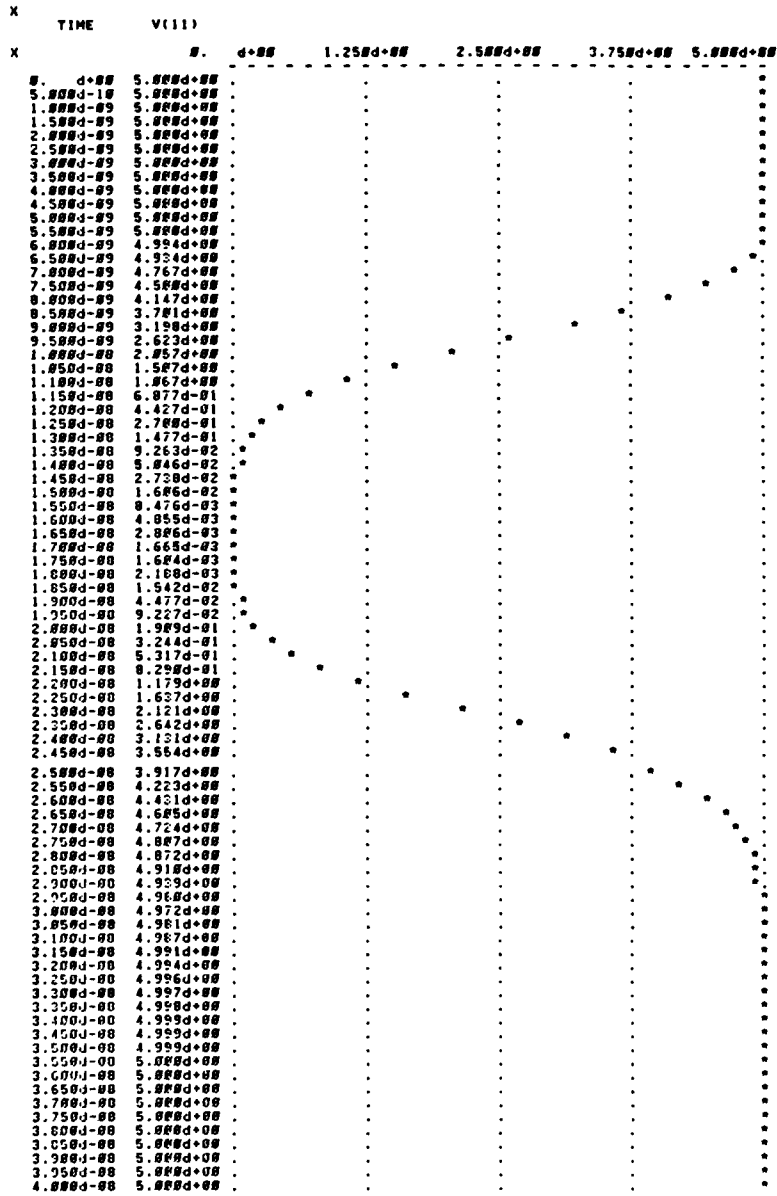
Figure C-43.   SPICE Plot Basic Section 3 Input 010.

Ø   CMOS/SOS BITSLICE SECTION 3 BASIC TRANSIENT ANALYSIS

Ø****   INPUT LISTING   TEMPERATURE =   27.ØØØ DEG C

Ø***

```
.WIDTH OUT=8Ø
.OPTIONS ITL1=5ØØ ITL5=Ø
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
+LEVEL=1
VDD I Ø DC 5V
M1  1  3  2  1 PMOS L=5.ØU W=1Ø.ØU
M2  1  2  5  1 PMOS L=5.ØU W=1Ø.ØU
M3  8  7  Ø  Ø NMOS L=5.ØU W=15.ØU
M4  8  3  2  Ø NMOS L=5.ØU W=15.ØU
M5  1  7  2  1 PMOS L=5.ØU W=1Ø.ØU
M6  1Ø 9  Ø  Ø NMOS L=5.ØU W=15.ØU
M7  1Ø 2  5  Ø NMOS L=5.ØU W=15.ØU
M8  1  9  5  1 PMOS L=5.ØU W=1Ø.ØU
M9  1  5  11 1 PMOS L=5.ØU W=1Ø.ØU
M1Ø 13 12 Ø  Ø NMOS L=5.ØU W=15.ØU
M11 13 5  11 Ø NMOS L=5.ØU W=15.ØU
M12 1  12 11 1 PMOS L=5.ØU W=1Ø.ØU
M13 1  14 12 1 PMOS L=5.ØU W=1Ø.ØU
M14 Ø  2  14 Ø NMOS L=5.ØU W=15.ØU
M15 16 15 Ø  Ø NMOS L=5.ØU W=15.ØU
M16 16 14 12 Ø NMOS L=5.ØU W=15.ØU
M17 1  2  14 1 PMOS L=5.ØU W=3Ø.ØU
M18 1  15 12 1 PMOS L=5.ØU W=1Ø.ØU
M19 Ø  15 9  Ø NMOS L=5.ØU W=15.ØU
M2Ø 1  15 9  1 PMOS L=5.ØU W=3Ø.ØU
C21 1  Ø  Ø.5Ø1PF
C22 Ø  Ø  Ø.465PF
C23 15 Ø  Ø.148PF
C24 9  Ø  Ø.141PF
C25 2  Ø  Ø.23ØPF
C26 12 Ø  Ø.138PF
C27 14 Ø  Ø.134PF
C28 11 Ø  Ø.134PF
C29 5  Ø  Ø.137PF
VIN1 15 Ø PULSE (5V ØV 5NS ØNS ØNS 1ØNS)
VCAR 3  Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VSEL 7  Ø PULSE (5V 5V ØNS ØNS ØNS 1ØNS)
.TRAN Ø.5NS 4ØNS
.PLOT TRAN V(11) (ØV,5V)
.END
```

```
1********12/*1/84 ********  SPICE 2G.1 (15OCT8*)  *********1:19:51*****
*          CMOS/SOS BITSLICE SECTION 3 BASIC TRANSIENT ANALYSIS
*****      TRANSIENT ANALYSIS              TEMPERATURE =   27.*** DEG C
*******************************************************************************

X
   TIME      V(11)

X              *.    d+**     1.25*d+**    2.5**d+**    3.75*d+**  5.***d+**
   *.   d+**  9.*35d-**  *
   5.***d-1*  9.*35d-**  *
   1.***d-*9  9.*35d-**  *
   1.5**d-*9  9.*35d-**  *
   2.***d-*9  9.*35d-**  *
   2.5**d-*9  9.*35d-**  *
   3.***d-*9  9.*35d-**  *
   3.5**d-*9  9.*35d-**  *
   4.***d-*9  9.*35d-**  *
   4.5**d-*9  9.*35d-**  *
   5.***d-*9  9.*35d-**  *
   5.5**d-*9  9.*35d-**  *
   6.***d-*9  9.*57d-**  *
   6.5**d-*9  9.275d-**  *
   7.***d-*9  8.727d-*3  *
   7.5**d-*9  5.4*9d-*2  .*
   8.***d-*9  1.45*d-*1  .  *
   8.5**d-*9  3.95*d-*1  .    *
   9.***d-*9  7.387d-*1  .      *
   9.5**d-*9  1.237d+**  .         *
   1.***d-*8  1.8*9d+**  .           *
   1.*5*d-*8  2.416d+**  .              *
   1.1**d-*8  3.*8*4d+**  .                *
   1.15*d-**  3.5*2d+**  .                  *
   1.2**d-**  3.894d+**  .                    *
   1.25*d-*8  4.2*2d+**  .                     *
   1.3**d-*8  4.451d+**  .                      *
   1.35*d-*8  4.6*7d+**  .                       *
   1.4**d-*8  4.73*4d+**  .                        *
   1.45*d-**  4.818d+**  .                         *
   1.5**d-**  4.874d+**  .                         *
   1.55*d-**  4.918d+**  .                          *
   1.6**d-**  4.944d+**  .                          *
   1.65*d-**  4.9*2d+**  .                          *
   1.7**d-**  4.973d+**  .                          *
   1.75*d-**  4.9*1d+**  .                          *
   1.8**d-**  4.974d+**  .                          *
   1.85*d-**  4.9*8d+**  .                          *
   1.9**d-**  4.729d+**  .                         *
   1.95*d-**  4.4*9d+**  .                       *
   2.***d-**  3.977d+**  .                     *
   2.*5*d-*8  3.451d+**  .                   *
   2.1**d-**  2.*26d+**  .               *
   2.15*d-**  2.19*d+**  .             *
   2.2**d-**  1.573d+**  .          *
   2.25*d-**  1.*73d+**  .        *
   2.3**d-**  6.453d-*1  .      *
   2.35*d-**  4.*99d-*1  .    *
   2.4**d-**  2.322d-*1  .  *
   2.45*d-**  1.267d-*1  . *
   2.5**d-**  7.*68d-*2  .*
   2.55*d-**  4.*5*d-*2  *
   2.6**d-**  2.166d-*2  *
   2.65*d-**  1.155d-*2  *
   2.7**d-**  6.*74d-*3  *
   2.75*d-**  3.6*9d-*3  *
   2.8**d-**  1.863d-*3  *
   2.85*d-**  1.*63d-*3  *
   2.9**d-**  5.47*d-*4  *
   2.95*d-**  3.*61d-*4  *
   3.***d-**  1.677d-*4  *
   3.*5*d-*8  8.244d-*5  *
   3.1**d-**  4.9*3d-*5  *
   3.15*d-**  2.572d-*5  *
   3.2**d-**  1.331d-*5  *
   3.25*d-**  7.769d-*6  *
   3.3**d-**  3.972d-*6  *
   3.35*d-**  2.25*d-*6  *
   3.4**d-**  1.27*d-*6  *
   3.45*d-**  6.7*8d-*7  *
   3.5**d-**  4.371d-*7  *
   3.55*d-**  2.72*d-*7  *
   3.6**d-**  1.84*d-*7  *
   3.65*d-**  1.448d-*7  *
   3.7**d-**  1.179d-*7  *
   3.75*d-**  1.*57d-*7  *
   3.8**d-**  9.*77d-*8  *
   3.85*d-**  9.449d-*8  *
   3.9**d-**  9.*81d-*8  *
   3.95*d-**  9.163d-*8  *
   4.***d-**  9.*99d-*8  *
```

Figure C-44.   SPICE Plot Basic Section 3 Input 101.
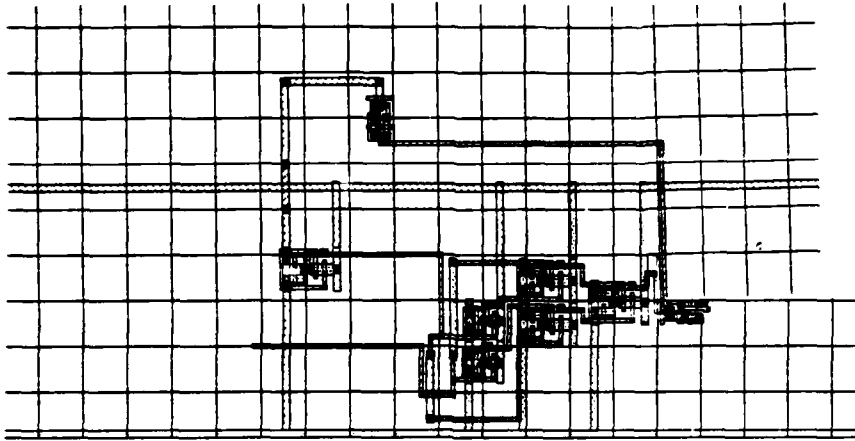
Figure C-45. CLL Plot Section 3 One Node Precharge.
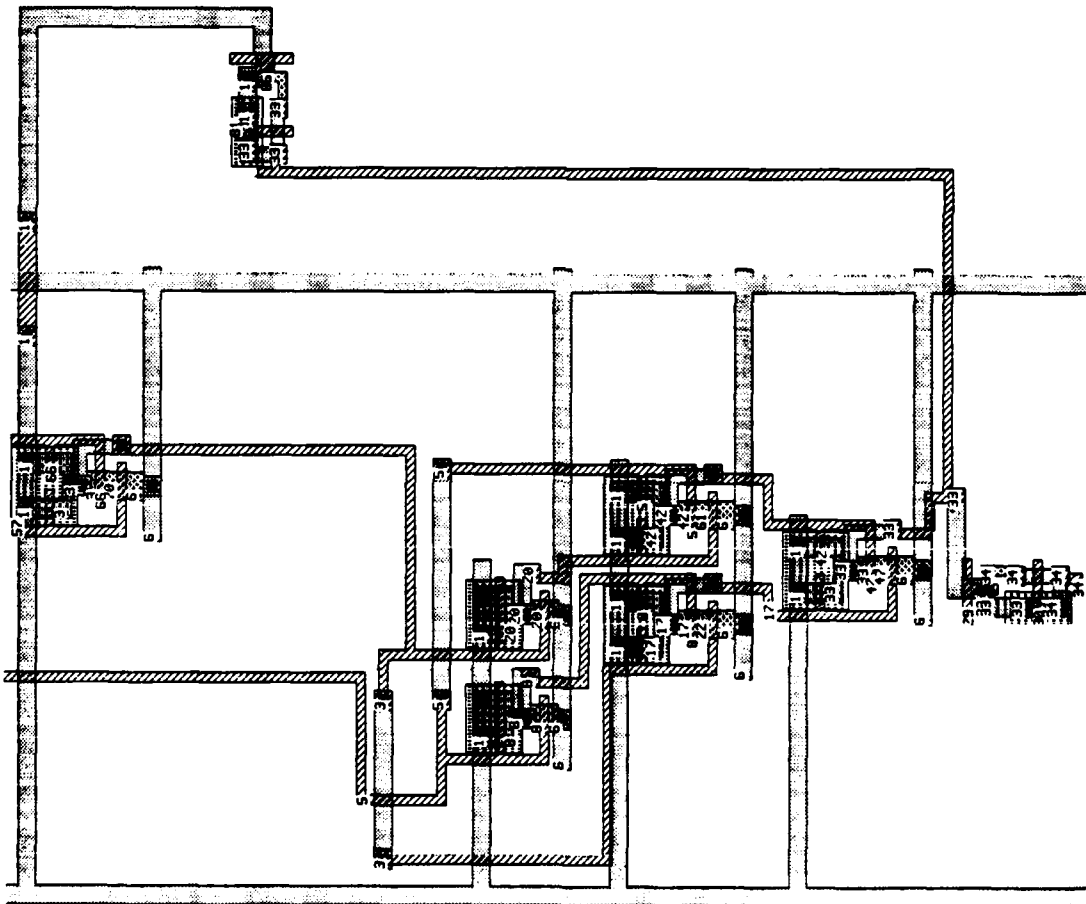
Figure C-46. Section 3 One Node Precharge Node Plot.

Table C-8

BITSLICE SECTION 3 NODE REFERENMCE LIST - ONE NODE PRECHARGE

```
GND     Ø
Vdd     1
NMOS    Ø
PMOS    1
33      2
85      3
1       4
81      5
3       6
66      7
42      8
5       9
6       1Ø
57      11
7Ø      12
2Ø      13
61      14
17      15
47      16
34      17
29      18
8       19
3Ø      2Ø
22      21
```

```
.WIDTH OUT=80
.OPTIONS ITL1=500 ITL5=0
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
+LEVEL=1
VDD 1 0 DC 5V
M1  1  3  2  0 NMOS L=5.0U W=5.0U
M2  2  5  1  1 PMOS L=5.0U W=10.0U
M3  1  7  6  1 PMOS L=5.0U W=10.0U
M4  1  9  8  1 PMOS L=5.0U W=10.0U
M5  12 11 0  0 NMOS L=5.0U W=15.0U
M6  12 7  6  0 NMOS L=5.0U W=15.0U
M7  1  11 6  1 PMOS L=5.0U W=10.0U
M8  14 13 0  0 NMOS L=5.0U W=15.0U
M9  14 9  3  0 NMOS L=5.0U W=15.0U
M10 1  13 8  1 PMOS L=5.0U W=10.0U
M11 1  3  2  1 PMOS L=5.0U W=10.0U
M12 16 15 0  0 NMOS L=5.0U W=15.0U
M13 16 8  2  0 NMOS L=5.0U W=15.0U
M14 2  13 17 0 NMOS L=5.0U W=5.0U
M15 1  15 2  1 PMOS L=5.0U W=10.0U
M16 1  19 15 1 PMOS L=5.0U W=10.0U
M17 2  20 17 1 PMOS L=5.0U W=10.0U
M18 0  8  13 0 NMOS L=5.0U W=15.0U
M19 21 6  0  0 NMOS L=5.0U W=15.0U
M20 21 19 15 0 NMOS L=5.0U W=15.0U
M21 1  6  13 1 PMOS L=5.0U W=30.0U
M22 1  6  15 1 PMOS L=5.0U W=10.0U
M23 0  9  19 0 NMOS L=5.0U W=15.0U
M24 1  9  19 1 PMOS L=5.0U W=30.0U
C25 1  0  0.123PF
C26 6  0  0.316PF
C27 9  0  0.232PF
C28 8  0  0.940PF
C29 19 0  0.111PF
C30 15 0  0.120PF
C31 13 0  0.103PF
C32 2  0  0.234PF
C33 17 0  0.1PF
C34 8  0  0.119PF
VIN1 9 0 PULSE (0V 5V 5NS 0NS 0NS 10NS)
VPI 3 0 PULSE (0V 5V 4NS 0NS 0NS 2NS)
VPIBAR 5 0 PULSE (5V 0V 4NS 0NS 0NS 2NS)
VSEL 7 0 PULSE (5V 5V 0NS 0NS 0NS 10NS)
VCAR 11 0 PULSE (0V 0V 0NS 0NS 0NS 10NS)
VPHI2 18 0 PULSE (5V 5V 0NS 0NS 0NS 20NS)
VPHI2BAR 20 0 PULSE (0V 0V 0NS 0NS 0NS 20NS)
.TRAN 1.5NS 40NS
.PLOT TRAN V(2) (0V,5V)
.END
```

```
#        CMOS/SOS BITSLICE SECTION 3 PRECHARGED AT ONE NODE X!

#••••    TRANSIENT ANALYSIS              TEMPERATURE =   27.000 DEG C

#•••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••

X
      TIME      V(2)

X             #.   d+00    1.250d+00     2.500d+00     3.750d+00  5.000d+00
                - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
#.    d+00   5.000d+00 .                                              *
5.000d-10   5.000d+00 .                                               *
1.000d-09   5.000d+00 .                                               *
1.500d-09   5.000d+00 .                                               *
2.000d-09   5.000d+00 .                                               *
2.500d-09   5.000d+00 .                                               *
3.000d-09   5.000d+00 .                                               *
3.500d-09   5.000d+00 .                                               *
4.000d-09   5.000d+00 .                                               *
4.500d-09   5.000d+00 .                                               *
5.000d-09   5.000d+00 .                                               *
5.500d-09   5.000d+00 .                                               *
6.000d-09   5.000d+00 .                                               *
6.500d-09   5.000d+00 .                                               *
7.000d-09   4.999d+00 .                                               *
7.500d-09   4.958d+00 .                                              *
8.000d-09   4.818d+00 .                                           *
8.500d-09   4.578d+00 .                                        *
9.000d-09   4.293d+00 .                                    *
9.500d-09   3.985d+00 .                                 *
1.000d-08   3.647d+00 .                             *
1.050d-08   3.303d+00 .                         *
1.100d-08   2.945d+00 .                      *
1.150d-08   2.564d+00 .                   *
1.200d-08   2.223d+00 .                *
1.250d-08   1.985d+00 .             *
1.300d-08   1.598d+00 .          *
1.350d-08   1.355d+00 .        *
1.400d-08   1.141d+00 .      *
1.450d-08   9.753d-01 .     *
1.500d-08   8.457d-01 .    *
1.550d-08   7.329d-01 .   *
1.600d-08   6.464d-01 .  *
1.650d-08   5.780d-01 .  *
1.700d-08   5.062d-01 . *
1.750d-08   4.795d-01 .*
1.800d-08   4.914d-01 .*
1.850d-08   5.626d-01 . *
1.900d-08   7.427d-01 .   *
1.950d-08   9.673d-01 .     *
2.000d-08   1.263d+00 .       *
2.050d-08   1.577d+00 .          *
2.100d-08   1.908d+00 .            *
2.150d-08   2.234d+00 .                *
2.200d-08   2.542d+00 .                  *
2.250d-08   2.821d+00 .                     *
2.300d-08   3.074d+00 .                       *
2.350d-08   3.296d+00 .                         *
2.400d-08   3.479d+00 .                          *
2.500d-08   3.768d+00 .                             *
2.550d-08   3.861d+00 .
2.600d-08   3.983d+00 .
2.650d-08   4.074d+00 .
2.700d-08   4.161d+00 .
2.750d-08   4.242d+00 .
2.800d-08   4.310d+00 .
2.850d-08   4.391d+00 .
2.900d-08   4.456d+00 .
2.950d-08   4.517d+00 .
3.000d-08   4.573d+00 .
3.050d-08   4.622d+00 .
3.100d-08   4.667d+00 .
3.150d-08   4.707d+00 .
3.200d-08   4.742d+00 .
3.250d-08   4.774d+00 .
3.300d-08   4.802d+00 .
3.350d-08   4.826d+00 .
3.400d-08   4.849d+00 .
3.450d-08   4.867d+00 .
3.500d-08   4.884d+00 .
3.550d-08   4.099d+00 .
3.600d-08   4.911d+00 .
3.650d-08   4.923d+00 .
3.700d-08   4.932d+00 .
3.750d-08   4.941d+00 .
3.800d-08   4.949d+00 .
3.850d-08   4.955d+00 .
3.900d-08   4.961d+00 .
3.950d-08   4.966d+00 .
4.000d-08   4.970d+00 .
```

Figure C-47.   SPICE Plot Section 3 Input 010 One
                Node Precharge with Basic Widths.

C-93

0   CMOS/SOS BITSLICE SECTION 3 PRECHARGED AT ONE NODE

0****   INPUT LISTING   TEMPERATURE =   27.000 DEG C

0***


```
 .WIDTH OUT=80
 .OPTIONS ITL1=500 ITL5=0
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
 +LEVEL=1
 VDD 1 0 DC 5V
 M1 1 3 2 0 NMOS L=5.0U W=5.0U
 M2 2 5 1 1 PMOS L=5.0U W=10.0U
 M3 1 7 6 1 PMOS L=5.0U W=10.0U
 M4 1 9 8 1 PMOS L=5.0U W=10.0U
 M5 12 11 0 0 NMOS L=5.0U W=15.0U
 M6 12 7 6 0 NMOS L=5.0U W=15.0U
 M7 1 11 6 1 PMOS L=5.0U W=10.0U
 M8 14 13 0 0 NMOS L=5.0U W=15.0U
 M9 14 9 8 0 NMOS L=5.0U W=15.0U
 M10 1 13 3 1 PMOS L=5.0U W=10.0U
 M11 1 3 2 1 PMOS L=5.0U W=10.0U
 M12 16 15 0 0 NMOS L=5.0U W=15.0U
 M13 16 8 2 0 NMOS L=5.0U W=15.0U
 M14 2 13 17 0 NMOS L=5.0U W=5.0U
 M15 1 15 2 1 PMOS L=5.0U W=10.0U
 M16 1 19 15 1 PMOS L=5.0U W=10.0U
 M17 2 20 17 1 PMOS L=5.0U W=10.0U
 M18 0 6 13 0 NMOS L=5.0U W=15.0U
 M19 21 6 0 0 NMOS L=5.0U W=15.0U
 M20 21 19 15 0 NMOS L=5.0U W=15.0U
 M21 1 6 13 1 PMOS L=5.0U W=30.0U
 M22 1 6 15 1 PMOS L=5.0U W=10.0U
 M23 0 0 19 0 NMOS L=5.0U W=15.0U
 M24 1 0 19 1 PMOS L=5.0U W=30.0U
 C25 1 0 0.123PF
 C26 6 0 0.316PF
 C27 9 0 0.232PF
 C28 0 0 0.940PF
 C29 19 0 0.111PF
 C30 15 0 0.120PF
 C31 13 0 0.100PF
 C32 2 0 0.231PF
 C33 17 0 0.1PF
 C34 8 0 0.110PF
 VIN1 9 0 PULSE (5V 0V 5NS 0NS 0NS 10NS)
 VP1 3 0 PULSE (0V 5V 4NS 0NS 0NS 2NS)
 VP1BAR 5 0 PULSE (5V 0V 4NS 0NS 0NS 2NS)
 VSEL 7 0 PULSE (5V 5V 0NS 0NS 0NS 10NS)
 VCAR 11 0 PULSE (0V 0V 0NS 0NS 0NS 10NS)
 VPHI2 10 0 PULSE (5V 5V 0NS 0NS 0NS 20NS)
 VPHI2BAR 20 0 PULSE (0V 0V 0NS 0NS 0NS 20NS)
 .TRAN 0.5NS 40NS
 .PLOT TRAN V(2) (0V,5V)
 .END
```

```
1********12/81/04 ********  SPICE 2G.1 (15OCT8#)  ********19:46:#1*****
#      CMOS/SOS BITSLICE SECTION 3 PRECHARGED AT ONE NODE *|
#****    TRANSIENT ANALYSIS                 TEMPERATURE =  27.### DEG C
#****************************************************************************

X
    TIME      V(2)

X              #.    d+##     1.25#d+##     2.5##d+##     3.75#d+## 5.###d+##
             -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -
#.   d+##  2.259d-#7 *
5.###d-1#  2.259d-#7 *
1.###d-#9  2.259d-#7 *
1.5##d-#9  2.259d-#7 *
2.###d-#9  2.259d-#7 *
2.5##d-#9  2.259d-#7 *
3.###d-#9  2.259d-#7 *
3.5##d-#9  2.259d-#7 *
4.###d-#9  2.259d-#7 *
4.5##d-#9  2.#21d-#1 .  *
5.###d-#9  6.#69d-#1 .    *
5.5##d-#9  9.594d-#1 .      *
6.###d-#9  1.145d+## .       *
6.5##d-#9  1.3#1d+## .        *
7.###d-#9  1.127d+## .       *
7.5##d-#9  9.766d-#1 .      *
8.###d-#9  1.##9d+## .       *
8.5##d-#9  1.155d+## .        *
9.###d-#9  1.38#d+## .          *
9.5##d-#9  1.678d+## .            *
1.###d-#8  1.99#d+## .               *
1.#5#d-#8  2.312d+## .                 *
1.1##d-#8  2.618d+## .                    *
1.15#d-#8  2.897d+## .                       *
1.2##d-#8  3.142d+## .                         *
1.25#d-#8  3.348d+## .                          *
1.3##d-#8  3.536d+## .                            *
1.35#d-#8  3.677d+## .                             *
1.4##d-#8  3.8#5d+## .                              *
1.45#d-#8  3.915d+## .                               *
1.5##d-#8  4.#11d+## .                                *
1.55#d-#8  4.1#4d+## .                                 *
1.6##d-#8  4.189d+## .                                  *
1.65#d-#8  4.267d+## .                                   *
1.7##d-#8  4.332d+## .                                    *
1.75#d-#8  4.377d+## .                                     *
1.8##d-#8  4.357d+## .                                    *
1.85#d-#8  4.225d+## .                                   *
1.9##d-#8  3.974d+## .                                 *
1.95#d-#8  3.675d+## .                               *
2.###d-#8  3.33#d+## .                             *
2.#5#d-#8  2.995d+## .                          *
2.1##d-#8  2.637d+## .                        *
2.15#d-#8  2.282d+## .                      *
2.2##d-#8  1.949d+## .                   *
2.25#d-#8  1.649d+## .                 *
2.3##d-#8  1.377d+## .               *
2.35#d-#8  1.173d+## .             *
2.4##d-#8  9.947d-#1 .           *
2.45#d-#8  8.58#d-#1 .          *
2.5##d-#8  7.497d-#1 .         *
2.55#d-#8  6.549d-#1 .        *
2.6##d-#8  5.785d-#1 .       *
2.65#d-#8  5.#74d-#1 .      *
2.7##d-#8  4.413d-#1 .     *
2.75#d-#8  3.829d-#1 .    *
2.8##d-#8  3.28#d-#1 .   *
2.85#d-#8  2.792d-#1 .  *
2.9##d-#8  2.369d-#1 .  *
2.95#d-#8  1.983d-#1 . *
3.###d-#8  1.67#d-#1 .*
3.#5#d-#8  1.394d-#1 .*
3.1##d-#8  1.153d-#1 *
3.15#d-#8  9.656d-#2 *
3.2##d-#8  7.973d-#2 *
3.25#d-#8  6.6##d-#2 *
3.3##d-#8  5.479d-#2 *
3.35#d-#8  4.4#8d-#2 *
3.4##d-#8  3.73#d-#2 *
3.45#d-#8  3.#76d-#2 *
3.5##d-#8  2.516d-#2 *
3.55#d-#8  2.#92d-#2 *
3.6##d-#8  1.715d-#2 *
3.65#d-#8  1.413d-#2 *
3.7##d-#8  1.16#d-#2 *
3.75#d-#8  9.527d-#3 *
3.8##d-#8  7.##8d-#3 *
3.85#d-#8  6.496d-#3 *
3.9##d-#8  5.3#2d-#3 *
3.95#d-#8  4.4#3d-#3 *
4.###d-#8  3.5##d-#3 *
```

Figure C-48.   SPICE Plot Section 3 Input 101 One
               Node Precharge with Basic Widths

```
.WIDTH OUT=80
.OPTIONS ITL1=500 ITL5=0
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
+LEVEL=1
VDD 1 Ø DC 5V
M1  1  3  2  Ø NMOS L=5.ØU W=10.ØU
M2  2  5  1  1 PMOS L=5.ØU W=20.ØU
M3  1  7  6  1 PMOS L=5.ØU W=10.ØU
M4  1  9  3  1 PMOS L=5.ØU W=10.ØU
M5  12 11 Ø  Ø NMOS L=5.ØU W=15.ØU
M6  12 7  6  Ø NMOS L=5.ØU W=15.ØU
M7  1  11 6  1 PMOS L=5.ØU W=10.ØU
M8  14 13 Ø  Ø NMOS L=5.ØU W=15.ØU
M9  14 9  8  Ø NMOS L=5.ØU W=15.ØU
M1Ø 1  13 3  1 PMOS L=5.ØU W=10.ØU
M11 1  8  2  1 PMOS L=5.ØU W=10.ØU
M12 16 15 Ø  Ø NMOS L=5.ØU W=15.ØU
M13 16 8  2  Ø NMOS L=5.ØU W=15.ØU
M14 2  18 17 Ø NMOS L=5.ØU W=5.ØU
M15 1  15 2  1 PMOS L=5.ØU W=10.ØU
M16 1  18 15 1 PMOS L=5.ØU W=10.ØU
M17 2  20 17 1 PMOS L=5.ØU W=10.ØU
M18 Ø  6  18 Ø NMOS L=5.ØU W=15.ØU
M19 21 6  Ø  Ø NMOS L=5.ØU W=15.ØU
M2Ø 21 19 15 Ø NMOS L=5.ØU W=15.ØU
M21 1  6  18 1 PMOS L=5.ØU W=30.ØU
M22 1  6  15 1 PMOS L=5.ØU W=10.ØU
M23 Ø  9  19 Ø NMOS L=5.ØU W=15.ØU
M24 1  9  19 1 PMOS L=5.ØU W=30.ØU
C25 1  Ø  Ø.123ØPF
C26 6  Ø  Ø.316PF
C27 9  Ø  Ø.232PF
C28 Ø  Ø  Ø.34ØPF
C29 19 Ø  Ø.111PF
C3Ø 15 Ø  Ø.12ØPF
C31 18 Ø  Ø.1ØØPF
C32 2  Ø  Ø.25ØPF
C33 17 Ø  Ø.1PF
C34 8  Ø  Ø.11ØPF
VIN1 9  Ø PULSE (ØV 5V 5NS ØNS ØNS 1ØNS)
VP1 3  Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS)
VMIBAR 5  Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
VSEL 7  Ø PULSE (5V ØV ØNS ØNS ØNS 1ØNS)
VCAR 11 Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VINIC 18 Ø PULSE (5V ØV ØNS ØNS ØNS 2ØNS)
VPHIBAR 2Ø Ø PULSE (ØV ØV ØNS ØNS ØNS 2ØNS)
.TRAN Ø.5NS 4ØNS
.PLOT TRAN V(2) (ØV,5V)
.END
```

```
1*******12/01/04 ******** SPICE 2G.1 (15OCT88) ********19:47:58*****
#       CMOS/SOS BITSLICE SECTION 3 PRECHARGED AT ONE NODE X2
0*****   TRANSIENT ANALYSIS                 TEMPERATURE =  27.000 DEG C
0***********************************************************************

X
    TIME      V(2)
X               0.   d+00    1.250d+00    2.500d+00    3.750d+00  5.000d+00
   0.   d+00  5.000d+00 .
   5.000d-10  5.000d+00 .
   1.000d-09  5.000d+00 .
   1.500d-09  5.000d+00 .
   2.000d-09  5.000d+00 .
   2.500d-09  5.000d+00 .
   3.000d-09  5.000d+00 .
   3.500d-09  5.000d+00 .
   4.000d-09  5.000d+00 .
   4.500d-09  5.000d+00 .
   5.000d-09  5.000d+00 .
   5.500d-09  5.000d+00 .
   6.000d-09  5.000d+00 .
   6.500d-09  5.000d+00 .
   7.000d-09  4.999d+00 .
   7.500d-09  4.958d+00 .
   8.000d-09  4.810d+00 .
   8.500d-09  4.578d+00 .
   9.000d-09  4.293d+00 .
   9.500d-09  3.985d+00 .
   1.000d-08  3.647d+00 .
   1.050d-08  3.303d+00 .
   1.100d-08  2.945d+00 .
   1.150d-08  2.584d+00 .
   1.200d-08  2.233d+00 .
   1.250d-08  1.905d+00 .
   1.300d-08  1.598d+00 .
   1.350d-08  1.355d+00 .
   1.400d-08  1.141d+00 .
   1.450d-08  9.753d-01 .
   1.500d-08  8.457d-01 .
   1.550d-08  7.329d-01 .
   1.600d-08  6.464d-01 .
   1.650d-08  5.748d-01 .
   1.700d-08  5.062d-01 .
   1.750d-08  4.795d-01 .
   1.800d-08  4.914d-01 .
   1.850d-08  5.626d-01 .
   1.900d-08  7.427d-01 .
   1.950d-08  9.673d-01 .
   2.000d-08  1.263d+00 .
   2.050d-08  1.577d+00 .
   2.100d-08  1.968d+00 .
   2.150d-08  2.234d+00 .
   2.200d-08  2.542d+00 .
   2.250d-08  2.821d+00 .
   2.300d-08  3.074d+00 .
   2.350d-08  3.296d+00 .
   2.400d-08  3.479d+00 .
   2.450d-08  3.642d+00 .
   2.500d-08  3.768d+00 .
   2.550d-08  3.881d+00 .
   2.600d-08  3.983d+00 .
   2.650d-08  4.074d+00 .
   2.700d-08  4.161d+00 .
   2.750d-08  4.242d+00 .
   2.800d-08  4.318d+00 .
   2.850d-08  4.391d+00 .
   2.900d-08  4.456d+00 .
   2.950d-08  4.517d+00 .
   3.000d-08  4.573d+00 .
   3.050d-08  4.622d+00 .
   3.100d-08  4.667d+00 .
   3.150d-08  4.707d+00 .
   3.200d-08  4.742d+00 .
   3.250d-08  4.774d+00 .
   3.300d-08  4.802d+00 .
   3.350d-08  4.826d+00 .
   3.400d-08  4.849d+00 .
   3.450d-08  4.867d+00 .
   3.500d-08  4.884d+00 .
   3.550d-08  4.899d+00 .
   3.600d-08  4.911d+00 .
   3.650d-08  4.923d+00 .
   3.700d-08  4.932d+00 .
   3.750d-08  4.941d+00 .
   3.800d-08  4.949d+00 .
   3.850d-08  4.955d+00 .
   3.900d-08  4.961d+00 .
   3.950d-08  4.966d+00 .
   4.000d-08  4.970d+00 .
```

Figure C-49.   SPICE Plot Section 3 Input 010 One
               Node Precharge with Widths x2.

C-97

0   CMOS/SOS BITSLICE SECTION 3 PRECHARGED AT ONE NODE

0****   INPUT LISTING   TEMPERATURE =   27.000 DEG

0***

```
 .WIDTH OUT=80
 .OPTIONS ITL1=500 ITLS=0
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
+LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
+LEVEL=1
VDD 1 0 DC 5V
M1  1 3 2 0 NMOS L=5.0U W=10.0U
M2  2 5 1 1 PMOS L=5.0U W=20.0U
M3  1 7 6 1 PMOS L=5.0U W=10.0U
M4  1 9 3 1 PMOS L=5.0U W=10.0U
M5  12 11 0 0 NMOS L=5.0U W=15.0U
M6  12 7 6 0 NMOS L=5.0U W=15.0U
M7  1 11 6 1 PMOS L=5.0U W=10.0U
M8  14 13 0 0 NMOS L=5.0U W=15.0U
M9  14 9 8 0 NMOS L=5.0U W=15.0U
M10 1 13 6 1 PMOS L=5.0U W=10.0U
M11 1 8 2 1 PMOS L=5.0U W=10.0U
M12 16 15 0 0 NMOS L=5.0U W=15.0U
M13 16 8 2 0 NMOS L=5.0U W=15.0U
M14 2 13 17 0 NMOS L=5.0U W=5.0U
M15 1 15 2 1 PMOS L=5.0U W=10.0U
M16 1 13 15 1 PMOS L=5.0U W=10.0U
M17 2 20 17 1 PMOS L=5.0U W=10.0U
M18 0 8 13 0 NMOS L=5.0U W=15.0U
M19 21 6 0 0 NMOS L=5.0U W=15.0U
M20 21 13 15 0 NMOS L=5.0U W=15.0U
M21 1 8 13 1 PMOS L=5.0U W=30.0U
M22 1 8 15 1 PMOS L=5.0U W=10.0U
M23 0 8 13 0 NMOS L=5.0U W=15.0U
M24 1 8 13 1 PMOS L=5.0U W=30.0U
C25 1 0 0.123GPF
C26 6 0 0.31GPF
C27 9 0 0.232PF
C28 0 0 0.040PF
C29 19 0 0.111PF
C30 15 0 0.120PF
C31 13 0 0.100PF
C32 2 0 0.204PF
C33 17 0 0.1PF
C34 8 0 0.110PF
VIN1 9 0 PULSE (5V 0V 5NS 0NS 0NS 10NS)
VPI 6 0 PULSE (0V 5V 0NS 0NS 0NS 2NS)
VPID 5 0 PULSE (5V 0V 0NS 0NS 0NS 2NS)
VSEL 7 0 PULSE (5V 5V 0NS 0NS 0NS 10NS)
VCAP 11 0 PULSE (0V 0V 0NS 0NS 0NS 10NS)
VPHI2 13 0 PULSE (5V 5V 0NS 0NS 0NS 20NS)
VPHI2BAR 20 0 PULSE (0V 0V 0NS 0NS 0NS 20NS)
.TRAN 1.5NS 40NS
.PLOT TRAN V(2) (0V,5V)
.END
```

● CMOS/SOS BITSLICE SECTION 3 PRECHARGED AT ONE NODE x2

●•••• TRANSIENT ANALYSIS TEMPERATURE = 27.••• DEG C

●•••*

```
X
    TIME      V(2)

X                  ●.    d+●●     1.25●d+●●    2.5●●d+●●     3.75●d+●●  5.●●●d+●●
 ●.    d+●●   2.259d-●7 ●
 5.●●●d-1●   2.259d-●7 ●
 1.●●●d-●9   2.259d-●7 ●
 1.5●●d-●9   2.259d-●7 ●
 2.●●●d-●9   2.259d-●7 ●
 2.5●●d-●9   2.259d-●7 ●
 3.●●●d-●9   2.259d-●7 ●
 3.5●●d-●9   2.259d-●7 ●
 4.●●●d-●9   2.259d-●7 ●
 4.5●●d-●9   3.8●4d-●1 .      ●            .
 5.●●●d-●9   1.222d+●●       .             .
 5.5●●d-●9   1.69●d+●●       .        ●    .
 6.●●●d-●9   2.●29d+●●       .            ●
 6.5●●d-●9   2.327d+●●       .                 ●
 7.●●●d-●9   2.132d+●●       .              ●
 7.5●●d-●9   1.869d+●●       .          ●
 8.●●●d-●9   1.875d+●●       .          ●
 8.5●●d-●9   1.987d+●●       .           ●
 9.●●●d-●9   2.227d+●●       .              ●
 9.5●●d-●9   2.5●7d+●●       .
 1.●●●d-●8   2.764d+●●       .                   ●
 1.●5●d-●8   3.●48d+●●       .
 1.1●●d-●8   3.278d+●●       .                      ●
 1.15●d-●8   3.471d+●●       .                        ●
 1.2●●d-●8   3.629d+●●       .                          ●
 1.25●d-●8   3.765d+●●       .
 1.3●●d-●8   3.856d+●●       .                            ●
 1.35●d-●8   3.987d+●●       .                              ●
 1.4●●d-●8   4.●84d+●●       .                               ●
 1.45●d-●8   4.172d+●●       .
 1.5●●d-●8   4.253d+●●       .                                ●
 1.55●d-●8   4.331d+●●       .                                 ●
 1.6●●d-●8   4.4●2d+●●       .                                  ●
 1.65●d-●8   4.467d+●●       .
 1.7●●d-●8   4.52●d+●●       .                                   ●
 1.75●d-●8   4.555d+●●       .                                   ●
 1.●●●d-●8   4.5●7d+●●       .                                   ●
 1.●5●d-●8   4.392d+●●       .                                  ●
 1.9●●d-●8   4.155d+●●       .                               ●
 1.95●d-●8   3.856d+●●       .
 2.●●●d-●8   3.536d+●●       .                            ●
 2.●5●d-●8   3.195d+●●       .                         ●
 2.1●●d-●8   2.●29d+●●       .
 2.15●d-●8   2.48●d+●●       .                      ●
 2.2●●d-●8   2.135d+●●       .                   ●
 2.25●d-●8   1.●16d+●●       .             ●
 2.3●●d-●8   1.519d+●●       .                 ●
 2.35●d-●8   1.29●d+●●       .           ●
 2.4●●d-●8   1.●●8d+●●       .
 2.45●d-●8   9.3●7d-●1       .        ●
 2.5●●d-●8   8.11●d-●1       .
 2.55●d-●8   7.●55d-●1       .      ●
 2.6●●d-●8   6.234d-●1       .
 2.65●d-●8   5.46●d-●1       .   ●
 2.7●●d-●8   4.787d-●1       .
 2.75●d-●8   4.172d-●1       .
 2.8●●d-●8   3.592d-●1       . ●
 2.●5●d-●8   3.●71d-●1       . ●
 2.9●●d-●8   2.615d-●1       .●
 2.95●d-●8   2.196d-●1       .●
 3.●●●d-●8   1.853d-●1       .
 3.●5●d-●8   1.551d-●1       ●
 3.1●●d-●8   1.285d-●1       ●    .
 3.15●d-●8   1.●77d-●1       ●.
 3.2●●d-●8   8.9●3d-●2       ●.
 3.25●d-●8   7.376d-●2       ●.
 3.3●●d-●8   6.127d-●2       ●.
 3.35●d-●8   5.●22d-●2       ●.
 3.4●●d-●8   4.176d-●2       ●
 3.45●d-●8   3.444d-●2       ●
 3.5●●d-●8   2.●19d-●2       ●
 3.55●d-●8   2.344d-●2       ●
 3.6●●d-●8   1.922d-●2       ●
 3.65●d-●8   1.563d-●2       ●
 3.7●●d-●8   1.3●9d-●2       ●
 3.75●d-●8   1.●68d-●2       ●
 3.●●●d-●8   8.●56d-●3       ●
 3.●5●d-●8   7.●64d-●3       ●
 3.9●●d-●8   5.947d-●3       ●
 3.95●d-●8   4.●38d-●3       ●
 4.●●●d-●8   4.●15d-●3       ●
```

Figure C-50. SPICE Plot Section 3 Input 101 One
Node Precharge with Widths x2.

Ø   CMOS/SOS BITSLICE SECTION 3 PRECHARGED AT ONE NODE

Ø****   INPUT LISTING   TEMPERATURE =   27.000 DEG C

Ø**

```
 .WIDTH OUT=80
 .OPTIONS ITL1=500 ITL5=0
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
 +LEVEL=1
 VDD 1 Ø DC 5V
 M1 1 3 2 Ø NMOS L=5.0U W=15.0U
 M2 2 5 1 1 PMOS L=5.0U W=30.0U
 M3 1 7 6 1 PMOS L=5.0U W=10.0U
 M4 1 9 3 1 PMOS L=5.0U W=10.0U
 M5 12 11 Ø Ø NMOS L=5.0U W=15.0U
 M6 12 7 6 Ø NMOS L=5.0U W=15.0U
 M7 1 11 6 1 PMOS L=5.0U W=10.0U
 M8 14 13 Ø Ø NMOS L=5.0U W=15.0U
 M9 14 9 8 Ø NMOS L=5.0U W=15.0U
 M10 1 13 8 1 PMOS L=5.0U W=10.0U
 M11 1 8 2 1 PMOS L=5.0U W=10.0U
 M12 16 15 Ø Ø NMOS L=5.0U W=15.0U
 M13 16 3 2 Ø NMOS L=5.0U W=15.0U
 M14 2 18 17 Ø NMOS L=5.0U W=5.0U
 M15 1 15 2 1 PMOS L=5.0U W=10.0U
 M16 1 19 15 1 PMOS L=5.0U W=10.0U
 M17 2 20 17 1 PMOS L=5.0U W=10.0U
 M18 Ø 8 13 Ø NMOS L=5.0U W=15.0U
 M19 21 6 Ø Ø NMOS L=5.0U W=15.0U
 M20 21 19 15 Ø NMOS L=5.0U W=15.0U
 M21 1 6 13 1 PMOS L=5.0U W=30.0U
 M22 1 6 15 1 PMOS L=5.0U W=10.0U
 M23 Ø 8 19 Ø NMOS L=5.0U W=15.0U
 M24 1 8 19 1 PMOS L=5.0U W=30.0U
 C25 1 Ø Ø.1239PF
 C26 6 Ø Ø.316PF
 C27 9 Ø Ø.232PF
 C28 Ø Ø Ø.940PF
 C29 19 Ø Ø.111PF
 C30 15 Ø Ø.120PF
 C31 13 Ø Ø.103PF
 C32 2 Ø Ø.234PF
 C33 17 Ø Ø.1PF
 C34 8 Ø Ø.119PF
 VIN1 9 Ø PULSE (ØV 5V 5NS ØNS ØNS 10NS)
 VP1 3 Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS)
 VP1BAR 5 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
 VSEL 7 Ø PULSE (5V 5V ØNS ØNS ØNS 10NS)
 VCAP 11 Ø PULSE (ØV ØV ØNS ØNS ØNS 10NS)
 VPHI2 18 Ø PULSE (5V 5V ØNS ØNS ØNS 20NS)
 VPHI2BAR 20 Ø PULSE (ØV ØV ØNS ØNS ØNS 20NS)
 .TRAN Ø.5NS 40NS
 .PLOT TRAN V(2) (ØV,5V)
 .END
```

0   CMOS/SOS BITSLICE SECTION 3 PRECHARGED AT ONE NODE x3

0••••   TRANSIENT ANALYSIS   TEMPERATURE =   27.000 DEG C

0•••

```
X
     TIME      V(2)

X                 0.   d+00    1.250d+00    2.500d+00    3.750d+00  5.000d+00
0.     d+00  5.000d+00 :                                                  *
5.000d-10  5.000d+00 :                                                    *
1.000d-09  5.000d+00 :                                                    *
1.500d-09  5.000d+00 :                                                    *
2.000d-09  5.000d+00 :                                                    *
2.500d-09  5.000d+00 :                                                    *
3.000d-09  5.000d+00 :                                                    *
3.500d-09  5.000d+00 :                                                    *
4.000d-09  5.000d+00 :                                                    *
4.500d-09  5.000d+00 :                                                    *
5.000d-09  5.000d+00 :                                                    *
5.500d-09  5.000d+00 :                                                    *
6.000d-09  5.000d+00 :                                                    *
6.500d-09  5.000d+00 :                                                    *
7.000d-09  4.999d+00 :                                                    *
7.500d-09  4.958d+00 :                                                   *
8.000d-09  4.818d+00 :                                                 *
8.500d-09  4.578d+00 :                                               *
9.000d-09  4.293d+00 :                                            *
9.500d-09  3.965d+00 :                                         *
1.000d-08  3.647d+00 :                                      *
1.050d-08  3.383d+00 :                                   *
1.100d-08  2.945d+00 :                                *
1.150d-08  2.564d+00 :                             *
1.200d-08  2.233d+00 :                          *
1.250d-08  1.965d+00 :                       *
1.300d-08  1.598d+00 :                    *
1.350d-08  1.355d+00 :                 *
1.400d-08  1.141d+00 :              *
1.450d-08  9.753d-01 :            *
1.500d-08  8.457d-01 :          *
1.550d-08  7.329d-01 :         *
1.600d-08  6.464d-01 :        *
1.650d-08  5.708d-01 :       *
1.700d-08  5.082d-01 :       *
1.750d-08  4.795d-01 :      *
1.800d-08  4.914d-01 :      *
1.850d-08  5.626d-01 :       *
1.900d-08  7.427d-01 :        *
1.950d-08  9.673d-01 :          *
2.000d-08  1.263d+00 :             *
2.050d-08  1.577d+00 :               *
2.100d-08  1.908d+00 :                  *
2.150d-08  2.234d+00 :                     *
2.200d-08  2.542d+00 :                        *
2.250d-08  2.821d+00 :                          *
2.300d-08  3.074d+00 :                            *
2.350d-08  3.296d+00 :                              *
2.400d-08  3.479d+00 :                                *
2.450d-08  3.642d+00 :                                 *
2.500d-08  3.768d+00 :                                  *
2.550d-08  3.881d+00 :                                   *
2.600d-08  3.963d+00 :                                    *
2.650d-08  4.074d+00 :                                     *
2.700d-08  4.161d+00 :                                      *
2.750d-08  4.242d+00 :                                       *
2.800d-08  4.318d+00 :                                        *
2.850d-08  4.391d+00 :                                        *
2.900d-08  4.456d+00 :                                         *
2.950d-08  4.517d+00 :                                          *
3.000d-08  4.573d+00 :                                           *
3.050d-08  4.622d+00 :                                           *
3.100d-08  4.667d+00 :                                            *
3.150d-08  4.707d+00 :                                            *
3.200d-08  4.742d+00 :                                             *
3.250d-08  4.774d+00 :                                             *
3.300d-08  4.802d+00 :                                             *
3.350d-08  4.826d+00 :                                              *
3.400d-08  4.849d+00 :                                              *
3.450d-08  4.867d+00 :                                              *
3.500d-08  4.884d+00 :                                              *
3.550d-08  4.899d+00 :                                               *
3.600d-08  4.911d+00 :                                               *
3.650d-08  4.923d+00 :                                               *
3.700d-08  4.932d+00 :                                               *
3.750d-08  4.941d+00 :                                               *
3.800d-08  4.949d+00 :                                                *
3.850d-08  4.955d+00 :                                                *
3.900d-08  4.961d+00 :                                                *
3.950d-08  4.966d+00 :                                                *
4.000d-08  4.970d+00 :                                                *
```

Figure C-51.   SPICE Plot Section 3 Input 010 One
               Node Precharge with Widths x3.

```
 .WIDTH OUT=80
 .OPTIONS ITL1=500 ITL5=0
 .MODEL NMOS NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
 +LEVEL=1
 .MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
 +LEVEL=1
 VDD 1 0 DC 5V
 M1 1 3 2 0 NMOS L=5.0U W=15.0U
 M2 2 5 1 1 PMOS L=5.0U W=30.0U
 M3 1 7 6 1 PMOS L=5.0U W=10.0U
 M4 1 9 3 1 PMOS L=5.0U W=10.0U
 M5 12 11 0 0 NMOS L=5.0U W=15.0U
 M6 12 7 6 0 NMOS L=5.0U W=15.0U
 M7 1 11 6 1 PMOS L=5.0U W=10.0U
 M8 14 13 0 0 NMOS L=5.0U W=15.0U
 M9 14 9 3 0 NMOS L=5.0U W=15.0U
 M10 1 13 3 1 PMOS L=5.0U W=10.0U
 M11 1 3 2 1 PMOS L=5.0U W=10.0U
 M12 16 15 0 0 NMOS L=5.0U W=15.0U
 M13 16 3 2 0 NMOS L=5.0U W=15.0U
 M14 2 13 17 0 NMOS L=5.0U W=5.0U
 M15 1 15 2 1 PMOS L=5.0U W=10.0U
 M16 1 19 15 1 PMOS L=5.0U W=10.0U
 M17 2 20 17 1 PMOS L=5.0U W=10.0U
 M18 0 6 13 0 NMOS L=5.0U W=15.0U
 M19 21 6 0 0 NMOS L=5.0U W=15.0U
 M20 21 19 15 0 NMOS L=5.0U W=15.0U
 M21 1 6 13 1 PMOS L=5.0U W=30.0U
 M22 1 6 15 1 PMOS L=5.0U W=10.0U
 M23 0 9 19 0 NMOS L=5.0U W=15.0U
 M24 1 9 19 1 PMOS L=5.0U W=30.0U
 C25 1 0 0.123PF
 C26 6 0 0.316PF
 C27 9 0 0.232PF
 C28 0 0 0.940PF
 C29 19 0 0.111PF
 C30 15 0 0.120PF
 C31 13 0 0.103PF
 C32 2 0 0.234PF
 C33 17 0 0.1PF
 C34 8 0 0.119PF
 VIN1 9 0 PULSE (5V 0V 5NS 0NS 0NS 10NS)
 VP1 3 0 PULSE (0V 5V 4NS 0NS 0NS 2NS)
 VP1BAR 5 0 PULSE (5V 0V 4NS 0NS 0NS 2NS)
 VSEL 7 0 PULSE (5V 5V 0NS 0NS 0NS 10NS)
 VCAR 11 0 PULSE (0V 0V 0NS 0NS 0NS 10NS)
 VPHI2 18 0 PULSE (5V 5V 0NS 0NS 0NS 20NS)
 VPHI2BAR 20 0 PULSE (0V 0V 0NS 0NS 0NS 20NS)
 .TRAN 0.5NS 40NS
 .PLOT TRAN V(2) (0V,5V)
 .END
```

```
#        CMOS/SOS BITSLICE SECTION 3 PRECHARGED AT ONE NODE  X3

#****       TRANSIENT ANALYSIS              TEMPERATURE -   27.### DEG C

#*****************************************************************************

X
      TIME      V(2)

X               #.   d+##      1.25#d+##     2.5##d+##       3.75#d+##  5.##d+##

#.     d+##   2.259d-#7  *
5.###d-1#   2.259d-#7  *
1.###d-#9   2.259d-#7  *
1.5##d-#9   2.259d-#7  *
2.###d-#9   2.259d-#7  *
2.5##d-#9   2.259d-#7  *
3.###d-#9   2.259d-#7  *
3.5##d-#9   2.259d-#7  *
4.###d-#9   2.259d-#7  *
4.5##d-#9   5.414d-#1  .         *
5.###d-#9   1.685d+##  .              *
5.5##d-#9   2.341d+##  .                    *
6.###d-#9   2.#35d+##  .                         *    *
6.5##d-#9   3.232d+##  .                              *     *
7.###d-#9   3.#45d+##  .                                   *   *
7.5##d-#9   2.764d+##  .                              *
#.###d-#9   2.732d+##  .                             *
8.5##d-#9   2.822d+##  .                              *
9.###d-#9   3.#19d+##  .                                *
9.5##d-#9   3.222d+##  .                                 *
1.###d-#8   3.414d+##  .                                   *
1.#5#d-#8   3.59#d+##  .                                      *
1.1##d-#8   3.737d+##  .                                       *
1.15#d-##   3.864d+##  .                                          *
1.2##d-#8   3.975d+##  .                                           *
1.25#d-#8   4.#76d+##  .                                            *
1.3##d-#8   4.17#d+##  .                                             *
1.35#d-#8   4.253d+##  .                                              *
1.4##d-#8   4.332d+##  .                                               *
1.45#d-#8   4.4#4d+##  .                                                *
1.5##d-#8   4.469d+##  .                                                 *
1.55#d-#8   4.53#d+##  .                                                  *
1.6##d-##   4.584d+##  .                                                   *
1.65#d-##   4.633d+##  .                                                    *
1.7##d-#8   4.671d+##  .                                                     *
1.75#d-##   4.697d+##  .                                                      *
1.8##d-#8   4.674d+##  .                                                      *
1.85#d-#8   4.52#d+##  .                                                     *
1.9##d-#8   4.295d+##  .                                                  *
1.95#d-#8   4.###d+##  .                                               *
2.###d-##   3.684d+##  .                                          *
2.#5#d-#8   3.346d+##  .                                      *
2.1##d-#8   2.993d+##  .                                  *
2.15#d-#8   2.633d+##  .                              *
2.2##d-##   2.281d+##  .                         *
2.25#d-#8   1.95#d+##  .                    *
2.3##d-#8   1.637d+##  .               *
2.35#d-#8   1.388d+##  .           *
2.4##d-#8   1.168d+##  .       *
2.5##d-##   9.###d-##  .     *
2.5##d-##   8.62#d-#1  .    *
2.55#d-#8   7.467d-#1  .   *
2.6##d-#8   6.591d-#1  .  *
2.65#d-#8   5.797d-#1  . *
2.7##d-##   5.#78d-#1  . *
2.75#d-#8   4.441d-#1  .*
2.8##d-#8   3.838d-#1  *
2.C5#d-##   3.292d-#1  *
2.9##d-#8   2.812d-#1  *
2.95#d-#8   2.368d-#1  *
3.###d-##   2.#72d-#1  *
3.#5#d-##   1.678d-#1  *
3.1##d-#8   1.392d-#1  *
3.15#d-##   1.16#d-#1  *
3.2##d-#8   9.666d-#2  *
3.25#d-##   8.#14d-#2  *
3.3##d-##   6.6C1d-#2  .*
3.35#d-#8   5.463d-#2  .*
3.4##d-##   4.544d-#2  .*
3.45#d-#8   3.749d-#2  *
3.5##d-#8   3.#C9d-#2  *
3.55#d-#8   2.5#3d-#2  *
3.6##d-##   2.#94d-#2  *
3.65#d-##   1.725d-#2  *
3.7##d-##   1.426d-#2  *
3.75#d-##   1.1#4d-#2  *
3.8##d-#8   9.#49d-#3  *
3.85#d-#8   7.937d-#3  *
3.9##d-##   6.48#d-#3  *
3.95#d-##   5.382d-#3  *
4.###d-#8   4.376d-#3  *
```

Figure C-52.   SPICE Plot Section 3 Input 101 One
               Node Precharge with Widths x3.

Figure C-53. Section 3 Four Node Precharge CLL Plot.
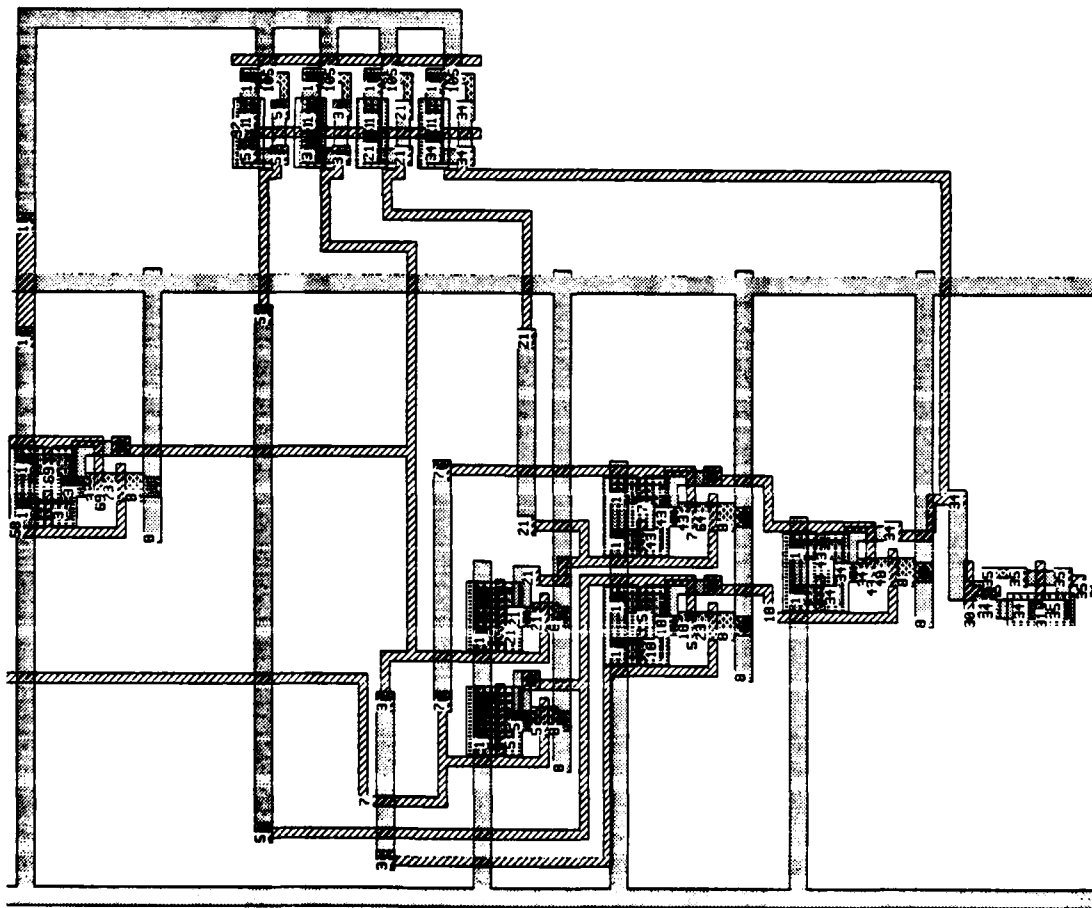
Figure C-54. Section 3 Four Node Precharge Node Plot.

Table C-9

BITSLICE PRECHARGED SECTION 3 NODE REFERENCE LIST

GND	0
Vdd	1
NMOS	0
PMOS	1
34	2
105	3
1	4
21	5
3	6
5	7
92	8
69	9
43	10
7	11
8	12
58	13
73	14
64	15
18	16
48	17
35	18
30	19
31	20
23	21

```
.WIDTH OUT=8Ø
.OPTIONS ITL1=5ØØ ITL5=Ø
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
+LEVEL=1
VDD 1 Ø DC 5V
M1  1 3 2 Ø NMOS L=5.ØU W=5.ØU
M2  1 3 5 Ø NMOS L=5.ØU W=5.ØU
M3  1 3 6 Ø NMOS L=5.ØU W=5.ØU
M4  1 3 7 Ø NMOS L=5.ØU W=5.ØU
M5  2 8 1 1 PMOS L=5.ØU W=1Ø.ØU
M6  5 8 1 1 PMOS L=5.ØU W=1Ø.ØU
M7  6 8 1 1 PMOS L=5.ØU W=1Ø.ØU
M8  7 8 1 1 PMOS L=5.ØU W=1Ø.ØU
M9  1 9 6 1 PMOS L=5.ØU W=1Ø.ØU
M1Ø 1 11 1Ø 1 PMOS L=5.ØU W=1Ø.ØU
M11 14 13 Ø Ø NMOS L=5.ØU W=15.ØU
M12 14 9 6 Ø NMOS L=5.ØU W=15.ØU
M13 1 13 6 1 PMOS L=5.ØU W=1Ø.ØU
M14 15 5 Ø Ø NMOS L=5.ØU W=15.ØU
M15 15 11 1Ø Ø NMOS L=5.ØU W=15.ØU
M16 1 5 1Ø 1 PMOS L=5.ØU W=1Ø.ØU
M17 1 1Ø 2 1 PMOS L=5.ØU W=1Ø.ØU
M18 17 16 Ø Ø NMOS L=5.ØU W=15.ØU
M19 17 1Ø 2 Ø NMOS L=5.ØU W=15.ØU
M2Ø 2 19 13 Ø NMOS L=5.ØU W=5.ØU
M21 1 16 2 1 PMOS L=5.ØU W=1Ø.ØU
M22 1 7 16 1 PMOS L=5.ØU W=1Ø.ØU
M23 2 2Ø 13 1 PMOS L=5.ØU W=1Ø.ØU
M24 Ø 6 5 Ø NMOS L=5.ØU W=15.ØU
M25 21 6 Ø Ø NMOS L=5.ØU W=15.ØU
M26 21 7 16 Ø NMOS L=5.ØU W=15.ØU
M27 1 6 5 1 PMOS L=5.ØU W=3Ø.ØU
M28 1 6 16 1 PMOS L=5.ØU W=1Ø.ØU
M29 Ø 11 7 Ø NMOS L=5.ØU W=15.ØU
M3Ø 1 11 7 1 PMOS L=5.ØU W=3Ø.ØU
C31 1 Ø Ø.1416PF
C32 6 Ø Ø.433PF
C33 7 Ø Ø.359PF
C34 11 Ø Ø.232PF
C35 Ø Ø Ø.94ØPF
C36 16 Ø Ø.12ØPF
C37 5 Ø Ø.266PF
C33 2 Ø Ø.234PF
C39 18 Ø Ø.1PF
C4Ø 1Ø Ø Ø.119PF
C41 3 Ø Ø.5ØPF
VIN1 11 Ø PULSE (ØV 5V 5NS ØNS ØNS 1ØNS)
VCAR 9 Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VSEL 13 Ø PULSE (5V 5V ØNS ØNS ØNS 1ØNS)
VP1 3 Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS)
VP1BAR 3 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
VPHI2 19 Ø PULSE (ØV 5V 5NS ØNS ØNS 2ØNS)

VPHI2CAR 2Ø Ø PULSE (5V ØV 5NS ØNS ØNS 2ØNS)
.TRAN Ø.5NS 4ØNS
.PLOT TRAN V(2) (ØV,5V)
.END
```

```
#       CMOS/SOS PRECHARGED BITSLICE SECTION 3 TRANSIENT ANALYSIS *|

#····      TRANSIENT ANALYSIS                 TEMPERATURE =   27.000 DEG C

#·········································································

X
    TIME        V(2)

X                     0.    d+00      1.250d+00      2.500d+00      3.750d+00  5.000d+00
     0.    d+00   5.000d+00 .                                                       .
     5.000d-10   5.000d+00 .                                                        *
     1.000d-09   5.000d+00 .                                                        *
     1.500d-09   5.000d+00 .                                                        *
     2.000d-09   5.000d+00 .                                                        *
     2.500d-09   5.000d+00 .                                                        *
     3.000d-09   5.000d+00 .                                                        *
     3.500d-09   5.000d+00 .                                                        *
     4.000d-09   5.000d+00 .                                                        *
     4.500d-09   5.000d+00 .                                                        *
     5.000d-09   5.000d+00 .                                                        *
     5.500d-09   4.985d+00 .                                                       *
     6.000d-09   4.724d+00 .                                                     *
     6.500d-09   4.668d+00 .                                                    *
     7.000d-09   4.645d+00 .                                                    *
     7.500d-09   4.638d+00 .                                                    *
     8.000d-09   4.658d+00 .                                                    *
     8.500d-09   4.668d+00 .                                                    *
     9.000d-09   4.674d+00 .                                                    *
     9.500d-09   4.636d+00 .                                                   *
     1.000d-08   4.584d+00 .                                                   *
     1.050d-08   4.380d+00 .                                                  *
     1.100d-08   4.017d+00 .                                               *
     1.150d-08   3.699d+00 .                                             *
     1.200d-08   3.361d+00 .                                          *
     1.250d-08   3.013d+00 .                                       *
     1.300d-08   2.658d+00 .                                    *
     1.350d-08   2.309d+00 .                                 *
     1.400d-08   1.973d+00 .                              *
     1.450d-08   1.665d+00 .                           *
     1.500d-08   1.427d+00 .                         *
     1.550d-08   1.174d+00 .                       *
     1.600d-08   1.002d+00 .                      *
     1.650d-08   8.657d-01 .                     *
     1.700d-08   7.565d-01 .                   *
     1.750d-08   6.718d-01 .                  *
     1.800d-08   5.965d-01 .                 *
     1.850d-08   5.378d-01 .                *
     1.900d-08   5.044d-01 .                *
     1.950d-08   4.934d-01 .               *
     2.000d-08   5.641d-01 .                *
     2.050d-08   7.011d-01 .                 *
     2.100d-08   8.992d-01 .                   *
     2.150d-08   1.181d+00 .                      *
     2.200d-08   1.462d+00 .                         *
     2.250d-08   1.887d+00 .                             *
     2.300d-08   2.134d+00 .                               *
     2.350d-08   2.449d+00 .                                  *
     2.400d-08   2.742d+00 .                                     *
     2.450d-08   2.996d+00 .                                       *
     2.500d-08   3.231d+00 .                                         *
     2.550d-08   3.434d+00 .                                           *
     2.600d-08   3.679d+00 .                                             *
     2.650d-08   3.981d+00 .                                                *
     2.700d-08   4.088d+00 .                                                 *
     2.750d-08   4.249d+00 .                                                  *
     2.800d-08   4.398d+00 .                                                   *
     2.850d-08   4.498d+00 .                                                   *
     2.900d-08   4.594d+00 .                                                    *
     2.950d-08   4.671d+00 .                                                    *
     3.000d-08   4.733d+00 .                                                     *
     3.050d-08   4.786d+00 .                                                     *
     3.100d-08   4.826d+00 .                                                     *
     3.150d-08   4.860d+00 .                                                      *
     3.200d-08   4.860d+00 .                                                      *
     3.250d-08   4.909d+00 .                                                      *
     3.300d-08   4.927d+00 .                                                      *
     3.350d-08   4.942d+00 .                                                      *
     3.400d-08   4.953d+00 .                                                      *
     3.450d-08   4.963d+00 .                                                      *
     3.500d-08   4.970d+00 .                                                      *
     3.550d-08   4.976d+00 .                                                      *
     3.600d-08   4.981d+00 .                                                      *
     3.650d-08   4.984d+00 .                                                      *
     3.700d-08   4.988d+00 .                                                      *
     3.750d-08   4.990d+00 .                                                      *
     3.800d-08   4.992d+00 .                                                      *
     3.850d-08   4.994d+00 .                                                      *
     3.900d-08   4.995d+00 .                                                      *
     3.950d-08   4.996d+00 .                                                      *
     4.000d-08   4.997d+00 .                                                      *
```

Figure C-55. SPICE Plot Section 3 Input 010 Four
Node Precharge with Basic Widths.

```
.WIDTH OUT=80
.OPTIONS ITL1=500 ITL5=0
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
+LEVEL=1
VDD 1 0 DC 5V
M1 1 3 2 0 NMOS L=5.0U W=5.0U
M2 1 3 5 0 NMOS L=5.0U W=5.0U
M3 1 3 6 0 NMOS L=5.0U W=5.0U
M4 1 3 7 0 NMOS L=5.0U W=5.0U
M5 2 8 1 1 PMOS L=5.0U W=10.0U
M6 5 8 1 1 PMOS L=5.0U W=10.0U
M7 6 8 1 1 PMOS L=5.0U W=10.0U
M8 7 8 1 1 PMOS L=5.0U W=10.0U
M9 1 9 6 1 PMOS L=5.0U W=10.0U
M10 1 11 10 1 PMOS L=5.0U W=10.0U
M11 14 13 0 0 NMOS L=5.0U W=15.0U
M12 14 9 6 0 NMOS L=5.0U W=15.0U
M13 1 13 6 1 PMOS L=5.0U W=10.0U
M14 15 5 0 0 NMOS L=5.0U W=15.0U
M15 15 11 10 0 NMOS L=5.0U W=15.0U
M16 1 5 10 1 PMOS L=5.0U W=10.0U
M17 1 10 2 1 PMOS L=5.0U W=10.0U
M18 17 16 0 0 NMOS L=5.0U W=15.0U
M19 17 10 2 0 NMOS L=5.0U W=15.0U
M20 2 19 13 0 NMOS L=5.0U W=5.0U
M21 1 16 2 1 PMOS L=5.0U W=10.0U
M22 1 7 16 1 PMOS L=5.0U W=10.0U
M23 2 20 18 1 PMOS L=5.0U W=10.0U
M24 0 6 5 0 NMOS L=5.0U W=15.0U
M25 21 6 0 0 NMOS L=5.0U W=15.0U
M26 21 7 16 0 NMOS L=5.0U W=15.0U
M27 1 6 5 1 PMOS L=5.0U W=30.0U
M28 1 6 16 1 PMOS L=5.0U W=10.0U
M29 0 11 7 0 NMOS L=5.0U W=15.0U
M30 1 11 7 1 PMOS L=5.0U W=30.0U
C31 1 0 0.1416PF
C32 6 0 0.433PF
C33 7 0 0.359PF
C34 11 0 0.232PF
C35 0 0 0.940PF
C36 16 0 0.120PF
C37 5 0 0.266PF
C38 2 0 0.234PF
C39 10 0 0.1PF
C40 10 0 0.119PF
C41 3 0 0.50PF
VIN1 11 0 PULSE (5V 0V 5NS 0NS 0NS 10NS)
VCAR 9 0 PULSE (0V 0V 0NS 0NS 0NS 10NS)
VSEL 13 0 PULSE (5V 5V 0NS 0NS 0NS 10NS)
VP1 3 0 PULSE (0V 5V 4NS 0NS 0NS 2NS)
VP1BAR 8 0 PULSE (5V 0V 4NS 0NS 0NS 2NS)
VPHI2 19 0 PULSE (0V 5V 5NS 0NS 0NS 20NS)
VPHI2BAR 20 0 PULSE (5V 0V 5NS 0NS 0NS 20NS)
.TRAN 0.5NS 40NS
.PLOT TRAN V(2) (0V,5V)
.END
```

```
#        CMOS/SOS PRECHARGED BITSLICE SECTION 3 TRANSIENT ANALYSIS *!

#****     TRANSIENT ANALYSIS               TEMPERATURE =   27.### DEG C

#********************************************************************

X
     TIME      V(2)

X                       #.   d+##   1.25#d+##   2.5##d+##    3.75#d+##  5.###d+##
   #.   d+##  1.8#7d-#7 *    -   -   -   .   -   -   -   .   -   -   -   .   -   -
   5.###J-1#  1.8#7d-#7 *                .                .                .
   1.###J-#9  1.8#7d-#7 *                .                .                .
   1.5##J-#9  1.8#7d-#7 *                .                .                .
   2.###d-#9  1.#27d-#7 *                .                .                .
   2.5##J-#9  1.8#7d-#7 *                .                .                .
   3.###J-#9  1.8#7d-#7 *                .                .                .
   3.5##J-#9  1.#87d-#7 *                .                .                .
   4.###J-#9  1.#87d-#7 *                .                .                .
   4.5##J-#9  2.1#6d-#1       *          .                .                .
   5.###J-#9  7.487d-#1          *       .                .                .
   5.5##J-#9  1.#68d+##              *   .                .                .
   6.###d-#9  1.37#d+##                *  .               .                .
   6.5##J-#9  1.553d+##                  * .              .                .
   7.###d-#9  1.364d+##                 *  .              .                .
   7.5##d-#9  1.172d+##               *    .              .                .
   8.###d-#9  1.#55d+##              *     .              .                .
   8.5##d-#9  1.#59d+##              *     .              .                .
   9.###d-#9  1.16#d+##               *    .              .                .
   9.5##d-#9  1.372d+##                 *  .              .                .
   1.###d-#8  1.656d+##                    *              .                .
   1.#5#d-##  1.977d+##                    .  *           .                .
   1.1##d-#8  2.311d+##                    .     *        .                .
   1.15#d-##  2.628d+##                    .        *     .                .
   1.2##d-#8  2.913d+##                    .           *  .                .
   1.25#d-##  3.157d+##                    .              *                .
   1.3##d-##  3.382d+##                    .              . *              .
   1.35#d-##  3.552d+##                    .              .   *            .
   1.4##d-##  3.7#3d+##                    .              .     *          .
   1.45#d-##  3.831d+##                    .              .       *        .
   1.5##d-##  3.937d+##                    .              .        *       .
   1.55#d-##  4.#38d+##                    .              .         *      .
   1.6##d-##  4.128d+##                    .              .          *     .
   1.65#d-##  4.213d+##                    .              .           *    .
   1.7##d-#8  4.292d+##                    .              .            *   .
   1.75#d-#8  4.364d+##                    .              .             *  .
   1.8##d-##  4.426d+##                    .              .              * .
   1.85#d-##  4.477d+##                    .              .               *.
   1.9##J-#8  4.517d+##                    .              .                .*
   1.95#d-##  4.515d+##                    .              .                .*
   2.###J-#8  4.442d+##                    .              .               *.
   2.#5#d-##  4.312d+##                    .              .             *  .
   2.1##J-#8  4.#55d+##                    .              .           *    .
   2.15#J-##  3.771d+##                    .              .        *       .
   2.2##J-##  3.447d+##                    .              .     *          .
   2.25#J-##  3.1#3d+##                    .              .  *             .
   2.3##d-##  2.753d+##                    .              *                .
   2.35#d-##  2.399d+##                    .          *   .                .
   2.4##J-##  2.#61d+##                    .       *      .                .
   2.45#d-##  1.736d+##                    .    *         .                .
   2.5##d-##  1.472d+##                    .  *           .                .
   2.55#-##   1.228d+##                    . *            .                .
   2.6##d-##  9.551d-#1                   *.              .                .
   2.65#J-##  7.273d-#1                 * .               .                .
   2.7##d-##  5.6##d-#1               *   .               .                .
   2.75#d-##  4.11#d-#1             *     .               .                .
   2.8##d-##  2.964d-#1           *       .               .                .
   2.85#d-##  2.212d-#1          *        .               .                .
   2.9##d-##  1.5#4d-#1        *          .               .                .
   2.95#d-##  1.147d-#1       *           .               .                .
   3.###J-##  #.35#d-#2     *             .               .                .
   3.#5#J-#8  5.855d-#2    *              .               .                .
   3.1##d-##  4.298d-#2   *               .               .                .
   3.15#J-##  3.#73d-#2  *                .               .                .
   3.2##d-##  2.155d-#2  *                .               .                .
   3.25#J-##  1.585d-#2 *                 .               .                .
   3.3##d-##  1.118d-#2 *                 .               .                .
   3.35#J-##  8.#15d-#3 *                 .               .                .
   3.4##J-##  5.79#d-#3 *                 .               .                .
   3.45#J-##  4.#4#d-#3 *                 .               .                .
   3.5##J-##  2.957d-#3 *                 .               .                .
   3.55#J-##  2.1#8d-#3 *                 .               .                .
   3.6##J-##  1.475d-#3 *                 .               .                .
   3.65#J-##  1.#64d-#3 *                 .               .                .
   3.7##d-##  7.635d-#4 *                 .               .                .
   3.75#J-##  5.472d-#4 *                 .               .                .
   3.8##J-##  3.957d-#4 *                 .               .                .
   3.85#J-##  2.756d-#4 *                 .               .                .
   3.9##J-##  2.#18d-#4 *                 .               .                .
   3.95#J-##  1.436d-#4 *                 .               .                .
   4.###J-##  1.###d-#4 *    -   -   -   .   -   -   -   .   -   -   -   .   -   -
```

Figure C-56.   SPICE Plot Section 3 Input 101 Four
                Node precharge with Basic Widths.

C-109

```
.WIDTH OUT=80
.OPTIONS ITL1=500 ITL5=0
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
+LEVEL=1
VDD 1 0 DC 5V
M1 1 3 2 0 NMOS L=5.0U W=10.0U
M2 1 3 5 0 NMOS L=5.0U W=10.0U
M3 1 3 6 0 NMOS L=5.0U W=10.0U
M4 1 3 7 0 NMOS L=5.0U W=10.0U
M5 2 8 1 1 PMOS L=5.0U W=20.0U
M6 5 8 1 1 PMOS L=5.0U W=20.0U
M7 6 8 1 1 PMOS L=5.0U W=20.0U
M8 7 8 1 1 PMOS L=5.0U W=20.0U
M9 1 9 6 1 PMOS L=5.0U W=10.0U
M10 1 11 10 1 PMOS L=5.0U W=10.0U
M11 14 13 0 0 NMOS L=5.0U W=15.0U
M12 14 9 6 0 NMOS L=5.0U W=15.0U
M13 1 13 6 1 PMOS L=5.0U W=10.0U
M14 15 5 0 0 NMOS L=5.0U W=15.0U
M15 15 11 10 0 NMOS L=5.0U W=15.0U
M16 1 5 10 1 PMOS L=5.0U W=10.0U
M17 1 10 2 1 PMOS L=5.0U W=10.0U
M18 17 16 0 0 NMOS L=5.0U W=15.0U
M19 17 10 2 0 NMOS L=5.0U W=15.0U
M20 2 19 13 0 NMOS L=5.0U W=5.0U
M21 1 16 2 1 PMOS L=5.0U W=10.0U
M22 1 7 16 1 PMOS L=5.0U W=10.0U
M23 2 20 13 1 PMOS L=5.0U W=10.0U
M24 0 6 5 0 NMOS L=5.0U W=15.0U
M25 21 5 0 0 NMOS L=5.0U W=15.0U
M26 21 7 16 0 NMOS L=5.0U W=15.0U
M27 1 6 5 1 PMOS L=5.0U W=30.0U
M28 1 6 16 1 PMOS L=5.0U W=10.0U
M29 0 11 7 0 NMOS L=5.0U W=15.0U
M30 1 11 7 1 PMOS L=5.0U W=30.0U
C31 1 0 0.1416PF
C32 6 0 0.433PF
C33 7 0 0.359PF
C34 11 0 0.232PF
C35 0 0 0.040PF
C36 16 0 0.129PF
C37 5 0 0.266PF
C38 2 0 0.234PF
C39 18 0 0.1PF
C40 10 0 0.119PF
C41 3 0 0.50PF
VIN1 11 0 PULSE (0V 5V 5NS 0NS 0NS 10NS)
VCAR 9 0 PULSE (0V 0V 0NS 0NS 0NS 10NS)
VSEL 13 0 PULSE (5V 5V 0NS 0NS 0NS 10NS)
VP1 3 0 PULSE (0V 5V 4NS 0NS 0NS 2NS)
VP1BAR 3 0 PULSE (5V 0V 4NS 0NS 0NS 2NS)
VPHI2 19 0 PULSE (0V 5V 5NS 0NS 0NS 20NS)
VPHI2BAR 20 0 PULSE (5V 0V 5NS 0NS 0NS 20NS)
.TRAN 0.5NS 40NS
.PLOT TRAN V(2) (0V,5V)
.END
```

!••••••••12/#1/84 •••••••• SPICE 2G.1 (15OCT8#) ••••••••19:43:55•••••

CMOS/SOS PRECHARGED BITSLICE SECTION 3 TRANSIENT ANALYSIS #2

#•••• TRANSIENT ANALYSIS TEMPERATURE = 27.### DEG C

#•••

```
x
    TIME      V(2)
x               #.   d+##    1.25#d+##    2.5##d+##     3.75#d+## 5.###d+##
#.    d+##   5.###d+##                      .                     .            :
5.###d-1#   5.###d+##  .                    .                     .           .:
1.###d-#9   5.###d+##  .                    .                     .           .:
1.5##d-#9   5.###d+##  .                    .                     .           .:
2.###d-#9   5.###d+##  .                    .                     .           .:
2.5##d-#9   5.###d+##  .                    .                     .           .:
3.###d-#9   5.###d+##  .                    .                     .           .:
3.5##d-#9   5.###d+##  .                    .                     .           .:
4.###d-#9   5.###d+##  .                    .                     .           .:
4.5##d-#9   5.###d+##  .                    .                     .           .:
5.###d-#9   5.###d+##  .                    .                     .           .:
5.5##d-#9   4.91#d+##  .                    .                     .          . :
6.###d-#9   4.759d+##  .                    .                     .        .   :
6.5##d-#9   4.73#d+##  .                    .                     .        .   :
7.###d-#9   4.7#4d+##  .                    .                     .       .    :
7.5##d-#9   4.685d+##  .                    .                     .       .    :
8.###d-#9   4.692d+##  .                    .                     .       .    :
8.5##d-#9   4.7#4d+##  .                    .                     .       .    :
9.###d-#9   4.71#d+##  .                    .                     .       .    :
9.5##d-#9   4.693d+##  .                    .                     .       .    :
1.###d-#8   4.592d+##  .                    .                     .      .     :
1.#5#d-#8   4.4#7d+##  .                    .                     .     .       :
1.1##d-#8   4.129d+##  .                    .                     .   .         :
1.15#d-#8   3.83#d+##  .                    .                     . .           :
1.2##d-#8   3.49#d+##  .                    .                     .             :
1.25#d-#8   3.154d+##  .                    .                   . .             :
1.3##d-#8   2.8#1d+##  .                    .                 .   .             :
1.35#d-#8   2.448d+##  .                    .              .      .             :
1.4##d-#8   2.1#5d+##  .                    .           .         .             :
1.45#d-#8   1.763d+##  .                    .        .            .             :
1.5##d-#8   1.5##d+##  .                    .     .               .             :
1.55#d-#8   1.256d+##  .                    . .                   .             :
1.6##d-#8   1.#67d+##  .                 .  .                     .             :
1.65#d-#8   9.174d-#1  .             .      .                     .             :
1.7##d-#8   7.983d-#1  .           .        .                     .             :
1.75#d-#8   7.#76d-#1  .         .          .                     .             :
1.8##d-#8   6.278d-#1  .        .           .                     .             :
1.85#d-#8   5.662d-#1  .       .            .                     .             :
1.9##d-#8   5.326d-#1  .      .             .                     .             :
1.95#d-#8   5.213d-#1  .      .             .                     .             :
2.###d-#8   5.932d-#1  .      .             .                     .             :
2.#5#d-#8   7.32#d-#1  .       .            .                     .             :
2.1##d-#8   9.323d-#1  .         .          .                     .             :
2.15#d-#8   1.216d+##  .            .       .                     .             :
2.2##d-#8   1.518d+##  .               .    .                     .             :
2.25#d-#8   1.844d+##  .                  . .                     .             :
2.3##d-#8   2.17#d+##  .                    . .                   .             :
2.35#d-#8   2.484d+##  .                    .    .                .             :
2.4##d-#8   2.773d+##  .                    .       .             .             :
2.45#d-#8   3.#26d+##  .                    .          .          .             :
2.5##d-#8   3.254d+##  .                    .            .        .             :
2.55#d-#8   3.456d+##  .                    .              .      .             :
2.6##d-#8   3.696d+##  .                    .                .    .             :
2.65#d-#8   3.916d+##  .                    .                   . .             :
2.7##d-#8   4.1#1d+##  .                    .                     .             :
2.75#d-#8   4.26#d+##  .                    .                     . .           :
2.8##d-#8   4.399d+##  .                    .                     .  .          :
2.85#d-#8   4.5#6d+##  .                    .                     .   .         :
2.9##d-#8   4.6#6d+##  .                    .                     .     .       :
2.95#d-#8   4.676d+##  .                    .                     .      .      :
3.###d-#8   4.737d+##  .                    .                     .       .     :
3.#5#d-#8   4.79#d+##  .                    .                     .        .    :
3.1##d-#8   4.829d+##  .                    .                     .        .    :
3.15#d-#8   4.#62d+##  .                    .                     .         .   :
3.2##d-#8   4.89#d+##  .                    .                     .         .   :
3.25#d-#8   4.911d+##  .                    .                     .          .  :
3.3##d-#8   4.929d+##  .                    .                     .          .  :
3.35#d-#8   4.943d+##  .                    .                     .           . :
3.4##d-#8   4.954d+##  .                    .                     .           . :
3.45#d-#8   4.963d+##  .                    .                     .            .:
3.5##d-#8   4.97#d+##  .                    .                     .            .:
3.55#d-#8   4.976d+##  .                    .                     .            .:
3.6##d-#8   4.981d+##  .                    .                     .            .:
3.65#d-#8   4.985d+##  .                    .                     .            .:
3.7##d-#8   4.988d+##  .                    .                     .            .:
3.75#d-#8   4.99#d+##  .                    .                     .            .:
3.8##d-#8   4.992d+##  .                    .                     .            .:
3.85#d-#8   4.994d+##  .                    .                     .            .:
3.9##d-#8   4.995d+##  .                    .                     .            .:
3.95#d-#8   4.996d+##  .                    .                     .            .:
4.###d-#8   4.997d+##  .                    .                     .            .:
```

Figure C-57. SPICE Plot Section 3 Input 010 Four
Node Precharge with Widths x2.

C-111

Ø   CMOS/SOS PRECHARGED BITSLICE SECTION 3 TRANSIENT ANALYSIS

Ø****   INPUT LISTING   TEMPERATURE =   27.ØØØ DEG C

Ø**

```
.WIDTH OUT=8Ø
.OPTIONS ITL1=5ØØ ITL5=Ø
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
+LEVEL=1
VDD 1 Ø DC 5V
M1  1 3 2 Ø NMOS L=5.ØU W=1Ø.ØU
M2  1 3 5 Ø NMOS L=5.ØU W=1Ø.ØU
M3  1 3 6 Ø NMOS L=5.ØU W=1Ø.ØU
M4  1 3 7 Ø NMOS L=5.ØU W=1Ø.ØU
M5  2 8 1 1 PMOS L=5.ØU W=2Ø.ØU
M6  5 8 1 1 PMOS L=5.ØU W=2Ø.ØU
M7  6 8 1 1 PMOS L=5.ØU W=2Ø.ØU
M8  7 8 1 1 PMOS L=5.ØU W=2Ø.ØU
M9  1 9 6 1 PMOS L=5.ØU W=1Ø.ØU
M1Ø 1 11 1Ø 1 PMOS L=5.ØU W=1Ø.ØU
M11 14 13 Ø Ø NMOS L=5.ØU W=15.ØU
M12 14 9 6 Ø NMOS L=5.ØU W=15.ØU
M13 1 13 6 1 PMOS L=5.ØU W=1Ø.ØU
M14 15 5 Ø Ø NMOS L=5.ØU W=15.ØU
M15 15 11 1Ø Ø NMOS L=5.ØU W=15.ØU
M16 1 5 1Ø 1 PMOS L=5.ØU W=1Ø.ØU
M17 1 1Ø 2 1 PMOS L=5.ØU W=1Ø.ØU
M18 17 16 Ø Ø NMOS L=5.ØU W=15.ØU
M19 17 1Ø 2 Ø NMOS L=5.ØU W=15.ØU
M2Ø 2 19 18 Ø NMOS L=5.ØU W=5.ØU
M21 1 16 2 1 PMOS L=5.ØU W=1Ø.ØU
M22 1 7 16 1 PMOS L=5.ØU W=1Ø.ØU
M23 2 2Ø 13 1 PMOS L=5.ØU W=1Ø.ØU
M24 Ø 6 5 Ø NMOS L=5.ØU W=15.ØU
M25 21 6 Ø Ø NMOS L=5.ØU W=15.ØU
M26 21 7 16 Ø NMOS L=5.ØU W=15.ØU
M27 1 6 5 1 PMOS L=5.ØU W=3Ø.ØU
M28 1 6 16 1 PMOS L=5.ØU W=1Ø.ØU
M29 Ø 11 7 Ø NMOS L=5.ØU W=15.ØU
M3Ø 1 11 7 1 PMOS L=5.ØU W=3Ø.ØU
C31 1 Ø Ø.1416PF
C32 6 Ø Ø.433PF
C33 7 Ø Ø.359PF
C34 11 Ø Ø.232PF
C35 Ø Ø Ø.94ØPF
C36 16 Ø Ø.12ØPF
C37 5 Ø Ø.266PF
C38 2 Ø Ø.234PF
C39 18 Ø Ø.1PF
C4Ø 1Ø Ø Ø.119PF
C41 3 Ø Ø.5ØPF
VIN1 11 Ø PULSE (5V ØV 5NS ØNS ØNS 1ØNS)
VCAR 9 Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VSEL 1Ø Ø PULSE (5V 5V ØNS ØNS ØNS 1ØNS)
VP1 3 Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS)
VP1BAR 3 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
VPHI2 19 Ø PULSE (ØV 5V 5NS ØNS ØNS 2ØNS)
VPHI2BAR 2Ø Ø PULSE (5V ØV 5NS ØNS ØNS 2ØNS)
.TRAN Ø.5NS 4ØNS
.PLOT TRAN V(2) (ØV,5V)
.END
```

```
1********12/#1/84 ********  SPICE 2G.1 (15OCT8#)  *********19:44:18******

#         CMOS/SOS PRECHARGED BITSLICE SECTION 3 TRANSIENT ANALYSIS X2

#****     TRANSIENT ANALYSIS              TEMPERATURE =  27.### DEG C

#******************************************************************************

X
   TIME      V(2)
X
           #.   d+##    1.25#d+##    2.5##d+##    3.75#d+##  5.###d+##
#.   d+##  1.8#7d-#7 *
5.###d-1#  1.8#7d-#7 *
1.###d-#9  1.8#7d-#7 *
1.5##d-#9  1.8#7d-#7 *
2.###d-#9  1.8#7d-#7 *
2.5##d-#9  1.8#7d-#7 *
3.###d-#9  1.8#7d-#7 *
3.5##d-#9  1.8#7d-#7 *
4.###d-#9  1.8#7d-#7 *
4.5##d-#9  3.93#d-#1
5.###d-#9  1.317d+##
5.5##d-#9  1.867d+##
6.###d-#9  2.276d+##
6.5##d-#9  2.61#d+##
7.###d-#9  2.452d+##
7.5##d-#9  2.168d+##
8.###d-#9  2.#54d+##
8.5##d-#9  2.146d+##
9.###d-#9  2.3#9d+##
9.5##d-#9  2.584d+##
1.###d-#8  2.867d+##
1.#5#d-#8  3.126d+##
1.1##d-#8  3.369d+##
1.15#d-#8  3.565d+##
1.2##d-#8  3.727d+##
1.25#d-#8  3.867d+##
1.3##d-#8  3.991d+##
1.35#d-#8  4.#93d+##
1.4##d-#8  4.189d+##
1.45#d-#8  4.274d+##
1.5##d-#8  4.351d+##
1.55#d-#8  4.424d+##
1.6##d-#8  4.48#d+##
1.65#d-#8  4.546d+##
1.7##d-#8  4.599d+##
1.75#d-#8  4.645d+##
1.8##d-#8  4.684d+##
1.85#d-#8  4.717d+##
1.9##d-#8  4.733d+##
1.95#d-#8  4.726d+##
2.###d-#8  4.639d+##
2.#5#d-#8  4.5#5d+##
2.1##d-#8  4.254d+##
2.15#d-#8  3.97#d+##
2.2##d-#8  3.654d+##
2.25#d-#8  3.312d+##
2.3##d-#8  2.964d+##
2.35#d-#8  2.6#7d+##
2.4##d-#8  2.26#d+##
2.45#d-#8  1.923d+##
2.5##d-#8  1.628d+##
2.55#d-#8  1.357d+##
2.6##d-#8  1.#6#d+##
2.65#d-#8  8.118d-#1
2.7##d-#8  6.176d-#1
2.75#d-#8  4.624d-#1
2.8##d-#8  3.347d-#1
2.85#d-#8  2.5#3d-#1
2.9##d-#8  1.796d-#1
2.95#d-#8  1.3#2d-#1
3.###d-#8  9.49#d-#2
3.#5#d-#8  6.659d-#2
3.1##d-#8  4.891d-#2
3.15#d-#8  3.498d-#2
3.2##d-#8  2.454d-#2
3.25#d-#8  1.8#6d-#2
3.3##d-#8  1.273d-#2
3.35#d-#8  9.132d-#3
3.4##d-#8  6.6#6d-#3
3.45#d-#8  4.6#3d-#3
3.5##d-#8  3.3#9d-#3
3.55#d-#8  2.4#2d-#3
3.6##d-#8  1.681d-#3
3.65#d-#8  1.235d-#3
3.7##d-#8  8.69#d-#4
3.75#d-#8  6.2#4d-#4
3.8##d-#8  4.5#8d-#4
3.85#d-#8  3.14#d-#4
3.9##d-#8  2.298d-#4
3.95#d-#8  1.636d-#4
4.###d-#8  1.139d-#4
```
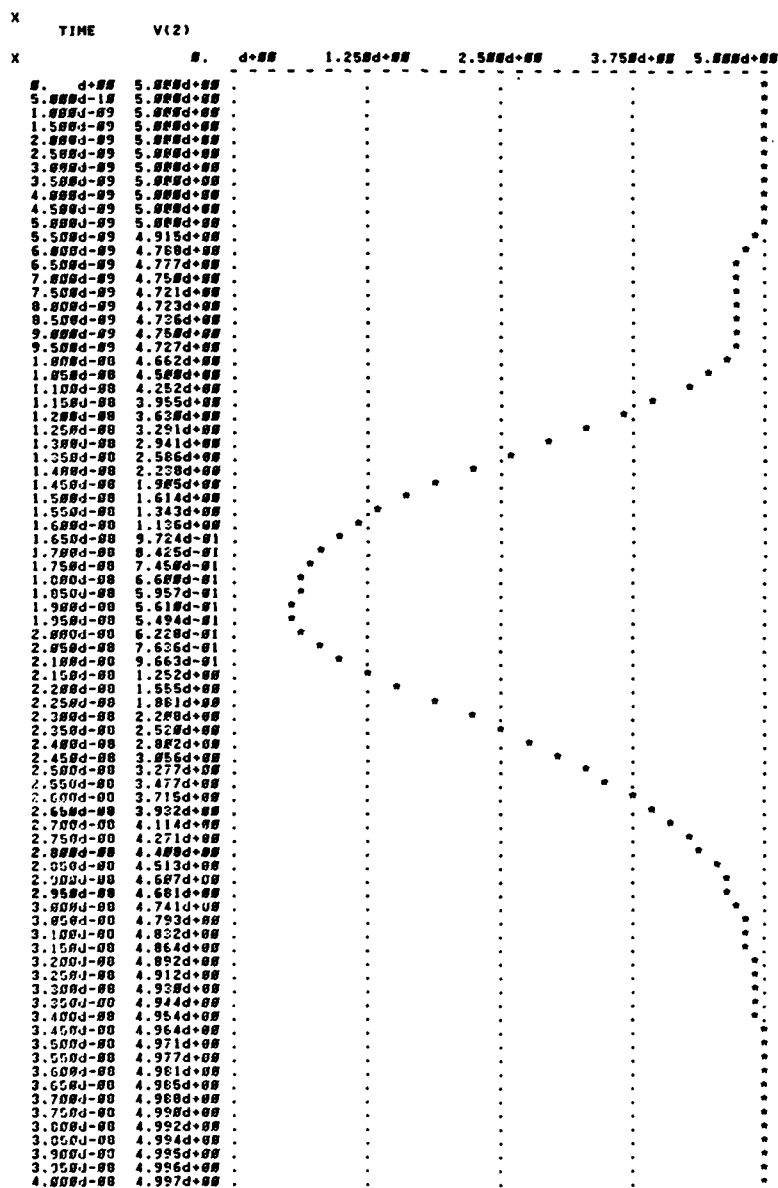
Figure C-58.   SPICE Plot Section 3 Input 101 Four
Node Precharge with Widths x2.

C-113

Ø   CMOS/SOS PRECHARGED BITSLICE SECTION 3 TRANSIENT ANALYSIS

Ø****   INPUT LISTING   TEMPERATURE =   27.ØØØ DEG C

Ø***

```
.WIDTH OUT=8Ø
.OPTIONS ITL1=5ØØ ITL5=Ø
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=4ØØ NSUB=2.5E16 LD=Ø.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=2ØØ NSUB=3E15 LD=Ø.7UM)
+LEVEL=1
VDD 1 Ø DC 5V
M1  1  3  2  Ø NMOS L=5.ØU W=15.ØU
M2  1  3  5  Ø NMOS L=5.ØU W=15.ØU
M3  1  3  6  Ø NMOS L=5.ØU W=15.ØU
M4  1  3  7  Ø NMOS L=5.ØU W=15.ØU
M5  2  8  1  1 PMOS L=5.ØU W=3Ø.ØU
M6  5  8  1  1 PMOS L=5.ØU W=3Ø.ØU
M7  6  8  1  1 PMOS L=5.ØU W=3Ø.ØU
M8  7  8  1  1 PMOS L=5.ØU W=3Ø.ØU
M9  1  9  6  1 PMOS L=5.ØU W=1Ø.ØU
M1Ø 1 11 1Ø 1 PMOS L=5.ØU W=1Ø.ØU
M11 14 13  Ø Ø NMOS L=5.ØU W=15.ØU
M12 14  9  6 Ø NMOS L=5.ØU W=15.ØU
M13 1 13  6  1 PMOS L=5.ØU W=1Ø.ØU
M14 15  5  Ø Ø NMOS L=5.ØU W=15.ØU
M15 15 11 1Ø Ø NMOS L=5.ØU W=15.ØU
M16 1  5 1Ø 1 PMOS L=5.ØU W=1Ø.ØU
M17 1 1Ø  2  1 PMOS L=5.ØU W=1Ø.ØU
M18 17 16  Ø Ø NMOS L=5.ØU W=15.ØU
M19 17 1Ø  2 Ø NMOS L=5.ØU W=15.ØU
M2Ø 2 19 18  Ø NMOS L=5.ØU W=5.ØU
M21 1 16  2  1 PMOS L=5.ØU W=1Ø.ØU
M22 1  7 16  1 PMOS L=5.ØU W=1Ø.ØU
M23 2 2Ø 18  1 PMOS L=5.ØU W=1Ø.ØU
M24 Ø  6  5  Ø NMOS L=5.ØU W=15.ØU
M25 21 6  Ø Ø NMOS L=5.ØU W=15.ØU
M26 21 7 16 Ø NMOS L=5.ØU W=15.ØU
M27 1  6  5  1 PMOS L=5.ØU W=3Ø.ØU
M28 1  6 16  1 PMOS L=5.ØU W=1Ø.ØU
M29 Ø 11  7  Ø NMOS L=5.ØU W=15.ØU
M3Ø 1 11  7  1 PMOS L=5.ØU W=3Ø.ØU
C31 1  Ø Ø.1416PF
C32 6  Ø Ø.433PF
C33 7  Ø Ø.359PF
C34 11 Ø Ø.232PF
C35 Ø  Ø Ø.94ØPF
C36 16 Ø Ø.12ØPF
C37 5  Ø Ø.266PF
C38 2  Ø Ø.234PF
C39 18 Ø Ø.1PF
C4Ø 1Ø Ø Ø.119PF
C41 3  Ø Ø.5ØPF
VIN1 11 Ø PULSE (ØV 5V 5NS ØNS ØNS 1ØNS)
VCAR 9 Ø PULSE (ØV ØV ØNS ØNS ØNS 1ØNS)
VSEL 13 Ø PULSE (5V 5V ØNS ØNS ØNS 1ØNS)
VP1 3 Ø PULSE (ØV 5V 4NS ØNS ØNS 2NS)
VP1BAR 8 Ø PULSE (5V ØV 4NS ØNS ØNS 2NS)
VPHI2 19 Ø PULSE (ØV 5V 5NS ØNS ØNS 2ØNS)

VPHI2BAR 2Ø Ø PULSE (5V ØV 5NS ØNS ØNS 2ØNS)
.TRAN Ø.5NS 4ØNS
.PLOT TRAN V(2) (ØV,5V)
.END
```

```
1********12/#1/84 ********* SPICE 2G.1 (15OCT8#) ********19:44:55*****

#        CMOS/SOS PRECHARGED BITSLICE SECTION 3 TRANSIENT ANALYSIS X3

#****       TRANSIENT ANALYSIS                    TEMPERATURE =   27.### DEG C

#********************************************************************************

X
    TIME      V(2)

X                    #.    d+##    1.25#d+##    2.5##d+##    3.75#d+##  5.###d+##
   #.    d+##  5.###d+## - - - - - - - - - - - - - - - - - - - - - - - - - - *
 5.###d-1#    5.###d+##   .                   .          .          .      *
 1.###d-#9    5.###d+##   .                   .          .          .      *
 1.5##d-#9    5.###d+##   .                   .          .          .      *
 2.###d-#9    5.###d+##   .                   .          .          .      *
 2.5##d-#9    5.###d+##   .                   .          .          .      *
 3.###d-#9    5.###d+##   .                   .          .          .      *
 3.5##d-#9    5.###d+##   .                   .          .          .      *
 4.###d-#9    5.###d+##   .                   .          .          .      *
 4.5##d-#9    5.###d+##   .                   .          .          .      *
 5.###d-#9    5.###d+##   .                   .          .          .      *
 5.5##d-#9    4.915d+##   .                   .          .          .     *
 6.###d-#9    4.7##d+##   .                   .          .          .   *
 6.5##d-#9    4.777d+##   .                   .          .          .   *
 7.###d-#9    4.75#d+##   .                   .          .          .   *
 7.5##d-#9    4.721d+##   .                   .          .          .  *
 8.###d-#9    4.723d+##   .                   .          .          .  *
 8.5##d-#9    4.736d+##   .                   .          .          .  *
 9.###d-#9    4.75#d+##   .                   .          .          .   *
 9.5##d-#9    4.727d+##   .                   .          .          .  *
 1.###d-#8    4.662d+##   .                   .          .          . *
 1.#5#d-#8    4.5##d+##   .                   .          .          *
 1.1##d-#8    4.252d+##   .                   .          .       *
 1.15#d-#8    3.955d+##   .                   .          .    *
 1.2##d-#8    3.63#d+##   .                   .          .  *
 1.25#d-#8    3.291d+##   .                   .        *
 1.3##d-#8    2.941d+##   .                   .     *
 1.35#d-#8    2.586d+##   .                   .   *
 1.4##d-#8    2.238d+##   .                   .*
 1.45#d-#8    1.9#5d+##   .                 * .
 1.5##d-#8    1.614d+##   .              *    .
 1.55#d-#8    1.343d+##   .           *       .
 1.6##d-#8    1.136d+##   .        *          .
 1.65#d-#8    9.724d-#1   .      *            .
 1.7##d-#8    8.425d-#1   .    *              .
 1.75#d-#8    7.45#d-#1   .   *               .
 1.8##d-#8    6.6##d-#1   .  *                .
 1.85#d-#8    5.957d-#1   . *                 .
 1.9##d-#8    5.618d-#1   .*                  .
 1.95#d-#8    5.494d-#1   *                   .
 2.###d-#8    6.22#d-#1   .*                  .
 2.#5#d-#8    7.636d-#1   . *                 .
 2.1##d-#8    9.663d-#1   .   *               .
 2.15#d-#8    1.252d+##   .      *            .
 2.2##d-#8    1.555d+##   .         *         .
 2.25#d-#8    1.861d+##   .            *      .
 2.3##d-#8    2.2#8d+##   .               *   .
 2.35#d-#8    2.52#d+##   .                  *.
 2.4##d-#8    2.8#2d+##   .                   . *
 2.45#d-#8    3.#56d+##   .                   .    *
 2.5##d-#8    3.277d+##   .                   .      *
 2.55#d-#8    3.477d+##   .                   .        *
 2.6##d-#8    3.715d+##   .                   .           *
 2.65#d-#8    3.932d+##   .                   .             *
 2.7##d-#8    4.114d+##   .                   .              *
 2.75#d-#8    4.271d+##   .                   .                *
 2.8##d-#8    4.4##d+##   .                   .                 *
 2.85#d-#8    4.513d+##   .                   .                  *
 2.9##d-#8    4.6#7d+##   .                   .                   *
 2.95#d-#8    4.681d+##   .                   .                    *
 3.###d-#8    4.741d+##   .                   .                     *
 3.#5#d-#8    4.793d+##   .                   .                     *
 3.1##d-#8    4.832d+##   .                   .                      *
 3.15#d-#8    4.864d+##   .                   .                      *
 3.2##d-#8    4.892d+##   .                   .                       *
 3.25#d-#8    4.912d+##   .                   .                       *
 3.3##d-#8    4.93#d+##   .                   .                        *
 3.35#d-#8    4.944d+##   .                   .                        *
 3.4##d-#8    4.954d+##   .                   .                        *
 3.45#d-#8    4.964d+##   .                   .                         *
 3.5##d-#8    4.971d+##   .                   .                         *
 3.55#d-#8    4.977d+##   .                   .                         *
 3.6##d-#8    4.981d+##   .                   .                         *
 3.65#d-#8    4.985d+##   .                   .                          *
 3.7##d-#8    4.988d+##   .                   .                          *
 3.75#d-#8    4.99#d+##   .                   .                          *
 3.8##d-#8    4.992d+##   .                   .                          *
 3.85#d-#8    4.994d+##   .                   .                          *
 3.9##d-#8    4.995d+##   .                   .                          *
 3.95#d-#8    4.996d+##   .                   .                          *
 4.###d-#8    4.997d+##   - - - - - - - - - - - - - - - - - - - - - - - *
```
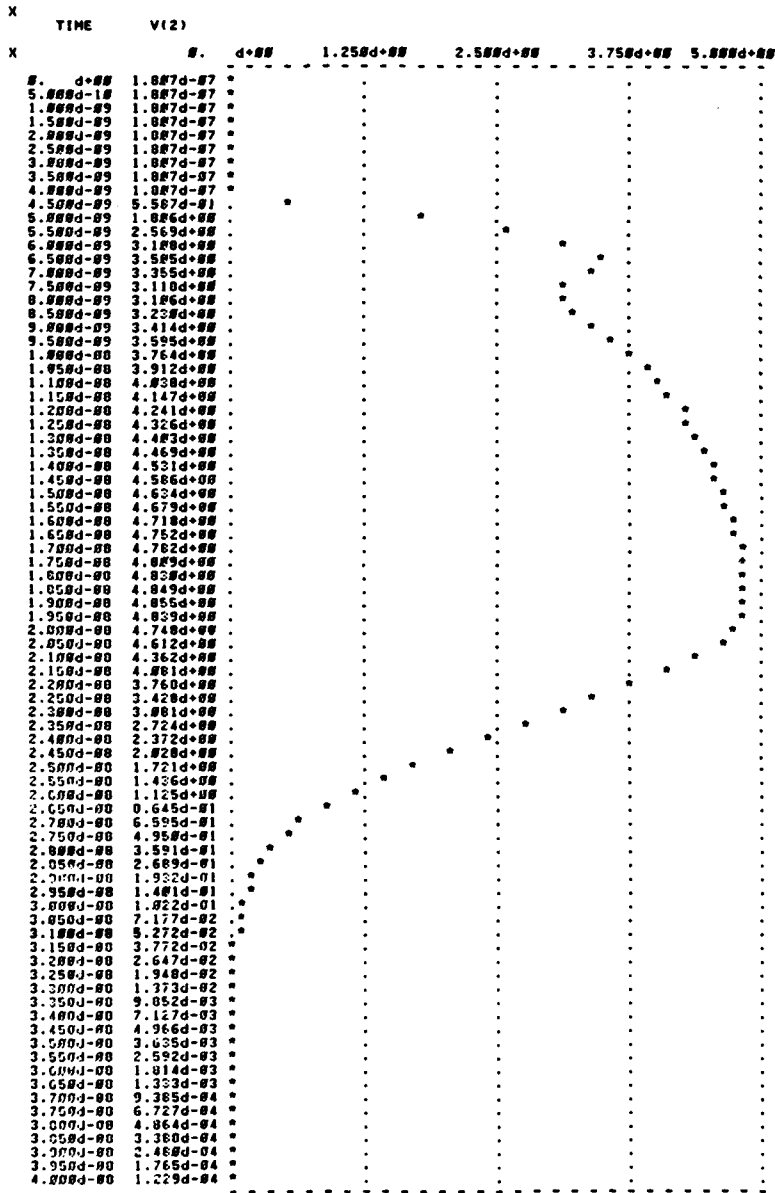
Figure C-59.   SPICE Plot Section 3 Input 010 Four
                Node Precharge with Widths x3.

```
.WIDTH OUT=80
.OPTIONS ITL1=500 ITL5=0
.MODEL NMOS NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
+LEVEL=1
.MODEL PMOS PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
+LEVEL=1
VDD 1 0 DC 5V
M1  1  3  2  0 NMOS L=5.0U W=15.0U
M2  1  3  5  0 NMOS L=5.0U W=15.0U
M3  1  3  6  0 NMOS L=5.0U W=15.0U
M4  1  3  7  0 NMOS L=5.0U W=15.0U
M5  2  8  1  1 PMOS L=5.0U W=30.0U
M6  5  8  1  1 PMOS L=5.0U W=30.0U
M7  6  8  1  1 PMOS L=5.0U W=30.0U
M8  7  8  1  1 PMOS L=5.0U W=30.0U
M9  1  9  6  1 PMOS L=5.0U W=10.0U
M10 1 11 10  1 PMOS L=5.0U W=10.0U
M11 14 13  0  0 NMOS L=5.0U W=15.0U
M12 14  9  6  0 NMOS L=5.0U W=15.0U
M13 1 13  6  1 PMOS L=5.0U W=10.0U
M14 15  5  0  0 NMOS L=5.0U W=15.0U
M15 15 11 10  0 NMOS L=5.0U W=15.0U
M16 1  5 10  1 PMOS L=5.0U W=10.0U
M17 1 10  2  1 PMOS L=5.0U W=10.0U
M18 17 16  0  0 NMOS L=5.0U W=15.0U
M19 17 10  2  0 NMOS L=5.0U W=15.0U
M20 2 19 18  0 NMOS L=5.0U W=5.0U
M21 1 16  2  1 PMOS L=5.0U W=10.0U
M22 1  7 16  1 PMOS L=5.0U W=10.0U
M23 2 20 18  1 PMOS L=5.0U W=10.0U
M24 0  6  5  0 NMOS L=5.0U W=15.0U
M25 21  6  0  0 NMOS L=5.0U W=15.0U
M26 21  7 16  0 NMOS L=5.0U W=15.0U
M27 1  6  5  1 PMOS L=5.0U W=30.0U
M28 1  6 16  1 PMOS L=5.0U W=10.0U
M29 0 11  7  0 NMOS L=5.0U W=15.0U
M30 1 11  7  1 PMOS L=5.0U W=30.0U
C31 1  0  0.1416PF
C32 6  0  0.433PF
C33 7  0  0.359PF
C34 11 0  0.232PF
C35 0  0  0.940PF
C36 16 0  0.120PF
C37 5  0  0.266PF
C38 2  0  0.234PF
C39 18 0  0.1PF
C40 10 0  0.119PF
C41 3  0  0.50PF
VIN1 11 0 PULSE (5V 0V 5NS 0NS 0NS 10NS)
VCAR 9 0 PULSE (0V 0V 0NS 0NS 0NS 10NS)
VSEL 13 0 PULSE (5V 5V 5NS 0NS 0NS 10NS)
VP1 3 0 PULSE (0V 5V 4NS 0NS 0NS 2NS)
VP1BAR 8 0 PULSE (5V 0V 4NS 0NS 0NS 2NS)
VPHI2 19 0 PULSE (0V 5V 5NS 0NS 0NS 20NS)
VPHI2BAR 20 0 PULSE (5V 0V 5NS 0NS 0NS 20NS)
.TRAN 0.5NS 40NS
.PLOT TRAN V(2) (0V,5V)
.END
```

```
#      CMOS/SOS PRECHARGED BITSLICE SECTION 3 TRANSIENT ANALYSIS X3

#****    TRANSIENT ANALYSIS              TEMPERATURE =   27.ØØØ DEG C

#***************************************************************************

X
     TIME        V(2)

X                   Ø.    d+ØØ      1.25Ød+ØØ    2.5ØØd+ØØ      3.75Ød+ØØ  5.ØØØd+ØØ
                        --------------------------------------------------------
Ø.    d+ØØ    1.8Ø7d-Ø7 *
5.ØØØd-1Ø     1.8Ø7d-Ø7 *
1.ØØØd-Ø9     1.8Ø7d-Ø7 *
1.5ØØd-Ø9     1.8Ø7d-Ø7 *
2.ØØØd-Ø9     1.8Ø7d-Ø7 *
2.5ØØd-Ø9     1.8Ø7d-Ø7 *
3.ØØØd-Ø9     1.8Ø7d-Ø7 *
3.5ØØd-Ø9     1.8Ø7d-Ø7 *
4.ØØØd-Ø9     1.8Ø7d-Ø7 *
4.5ØØd-Ø9     5.5Ø7d-Ø1          .
5.ØØØd-Ø9     1.Ø86d+ØØ              .
5.5ØØd-Ø9     2.569d+ØØ                   .
6.ØØØd-Ø9     3.1Ø8d+ØØ                      .
6.5ØØd-Ø9     3.5Ø5d+ØØ                        .
7.ØØØd-Ø9     3.355d+ØØ                       .
7.5ØØd-Ø9     3.11Ød+ØØ                      .
8.ØØØd-Ø9     3.1Ø6d+ØØ                      .
8.5ØØd-Ø9     3.238d+ØØ                       .
9.ØØØd-Ø9     3.414d+ØØ                        .
9.5ØØd-Ø9     3.595d+ØØ                         .
1.ØØØd-Ø8     3.764d+ØØ                          .
1.Ø5Ød-Ø8     3.912d+ØØ                           .
1.1ØØd-Ø8     4.Ø38d+ØØ                            .
1.15Ød-Ø8     4.147d+ØØ                             .
1.2ØØd-Ø8     4.241d+ØØ                             .
1.25Ød-Ø8     4.326d+ØØ                              .
1.3ØØd-Ø8     4.4Ø3d+ØØ                              .
1.35Ød-Ø8     4.469d+ØØ                               .
1.4ØØd-Ø8     4.531d+ØØ                               .
1.45Ød-Ø8     4.586d+ØØ                                .
1.5ØØd-Ø8     4.634d+ØØ                                .
1.55Ød-Ø8     4.679d+ØØ                                 .
1.6ØØd-Ø8     4.718d+ØØ                                 .
1.65Ød-Ø8     4.752d+ØØ                                  .
1.7ØØd-Ø8     4.782d+ØØ                                  .
1.75Ød-Ø8     4.8Ø9d+ØØ .                                .
1.8ØØd-Ø8     4.83Ød+ØØ                                  .
1.85Ød-Ø8     4.849d+ØØ                                  .
1.9ØØd-Ø8     4.855d+ØØ                                  .
1.95Ød-Ø8     4.839d+ØØ                                  .
2.ØØØd-Ø8     4.748d+ØØ                                  .
2.Ø5Ød-Ø8     4.612d+ØØ                                 .
2.1ØØd-Ø8     4.362d+ØØ                               .
2.15Ød-Ø8     4.ØØ1d+ØØ                            .
2.2ØØd-Ø8     3.76Ød+ØØ                          .
2.25Ød-Ø8     3.428d+ØØ                        .
2.3ØØd-Ø8     3.Ø81d+ØØ                      .
2.35Ød-Ø8     2.724d+ØØ                   .
2.4ØØd-Ø8     2.372d+ØØ                 .
2.45Ød-Ø8     2.Ø2Ød+ØØ               .
2.5ØØd-Ø8     1.721d+ØØ            .
2.55Ød-Ø8     1.436d+ØØ          .
2.6ØØd-Ø8     1.125d+ØØ        .
2.65Ød-Ø8     Ø.645d-Ø1      .
2.7ØØd-Ø8     6.595d-Ø1     .
2.75Ød-Ø8     4.95Ød-Ø1    .
2.8ØØd-Ø8     3.591d-Ø1   .
2.85Ød-Ø8     2.689d-Ø1  .
2.9ØØd-Ø8     1.932d-Ø1  .
2.95Ød-Ø8     1.4Ø1d-Ø1 .
3.ØØØd-Ø8     1.Ø22d-Ø1 .
3.Ø5Ød-Ø8     7.177d-Ø2 :
3.1ØØd-Ø8     5.272d-Ø2 .
3.15Ød-Ø8     3.772d-Ø2 *
3.2ØØd-Ø8     2.647d-Ø2 *
3.25Ød-Ø8     1.948d-Ø2 *
3.3ØØd-Ø8     1.373d-Ø2 *
3.35Ød-Ø8     9.Ø52d-Ø3 *
3.4ØØd-Ø8     7.127d-Ø3 *
3.45Ød-Ø8     4.966d-Ø3 *
3.5ØØd-Ø8     3.635d-Ø3 *
3.55Ød-Ø8     2.592d-Ø3 *
3.6ØØd-Ø8     1.814d-Ø3 *
3.65Ød-Ø8     1.333d-Ø3 *
3.7ØØd-Ø8     9.385d-Ø4 *
3.75Ød-Ø8     6.727d-Ø4 *
3.8ØØd-Ø8     4.864d-Ø4 *
3.85Ød-Ø8     3.38Ød-Ø4 *
3.9ØØd-Ø8     2.46Ød-Ø4 *
3.95Ød-Ø8     1.765d-Ø4 *
4.ØØØd-Ø8     1.229d-Ø4 *
                        --------------------------------------------------------
```

Figure C-60.   SPICE Plot Section 3 Input 101 Four
              Node Precharge with Widths x3.

Appendix D

This appendix is intended to serve as a practical guide for the individual who wishes to use the SPICE2 simulators available at AFIT. Much time was wasted in trying to determine how to correctly use the simulator due to lack of documentation and knowledgeable people. Much of the data was so spread throughout the users guide that it took a great amount of time to get comfortable with what it all meant. A procedure for establishing input files is presented in this appendix to reduce the confusion.

This appendix refers only to transient analysis use of the SPICE simulator.

The following information outlines the barriers encountered and overcome by this author to perform the simulations required for this thesis project. Hopefully this will benefit future users of SPICE.

The reader is expected to be familiar with the switch level simulator ESIM, since some similiar procedures are followed and the reader should refer to the SPICE users guide by Vladimirescu et al provided as reference material in the EE695 VLSI Notebook provided as a class text.

SPICE was originally intended for use with batch processing, so all the documentation makes "card" references. This is easily translated to lines of instructions in input files for an interactive system such as the VAX 11/780.

To run a SPICE simulation on a circuit, the following must be done:

1. Design a circuit using CLL or some other layout language.

2. Run cll -C filename.cll to obtain the .cif file.

3. Change all 125/1 to 125 1 in the .cif file.
    (this allows you to run mextra)

4. Run mextra on the .cif file.
    (This results in a .nodes and a .sim file)

5. Change the first line of the .sim file from tech=nmos to tech=cmos.

6. Generate a definitions file for NMOS and PMOS substrate connection nodes. This is required for sim2spice, the SPICE preprocessor which converts .sim format to .spice format. In CMOS, the depletion mode device is the PMOS device and the pull-down device is the NMOS device. Sim2spice defaults to plain NMOS technology with ENMOS and DNMOS descriptions. These must be changed in the definitions file. This file can also establish the ground and V_{dd} nodes for substrate connections. The PMOS substrate is connected to V_{dd} and the NMOS substrate is connected to ground. The file would look like this:

```
set GND 0 cmos
set Vdd 1 cmos
set PMOS 1 cmos
set NMOS 0 cmos
def PMOS DNMOS cmos
def NMOS ENMOS cmos
```

I tried changing the .cadrc file, as indicated in the sim2spice literature, but it didn't work.

7. Run sim2spice -d defintions filename filename.sim This results in a filename.spice file and a filename.names file. The .names file is a cross reference list between mextra and SPICE node names. The SPICE nodes are sequentially numbered and the mextra nodes appear at random. The SPICE filename.spice input file must refer to only SPICE nodes, not mextra nodes since the SPICE simulator will only recognize its sequential numbering of the respective nodes prepared by sim2spice.

8. The filename.spice is the input file required to run the simulation, but it does not include the command "cards" reqyuired for program control. It just contains the MOS, four node descriptions of each device in the circuit to be simulated. There should be an NMOS and PMOS device for each CMOS device. For small circuits these can be counted to verify that sim2spice has run correctly. Larger circuits are hard to verify since they contain so many devices.

This file includes all (four) the node connections for an individual NMOS or PMOS device.

However, all the nodes are <u>SPICE</u> nodes <u>not</u> mextra

nodes.

9. The next step is to modify the filename.spice file to account for the differences in the assignment of nodes between mextra and SPICE. A numbered node cifplot of the filename.cif and the filename.nodes files is required, and a copy of the filename.names file that was generated by sim2spice.

The ground node must be determined from the mextra based node plot. SPICE requires that the ground node be 0. Mextra does not use 0 as a node number. Therefore the mextra node for ground will be a number other thn 0 and in the mextra/SPICE node reference list a number other than 0 will have been assigned to the ground node by SPICE. This node must be determined and chnaged to 0 everywhere it occurs in the filename.spice file. For V_{dd}, the same procedure must be followed, but the node number is optional. However, it must be consistent with the node number assigned to the V_{dd} node when the independent DC supply voltage source is entered as a command line (card).

For all other inputs to the circuits, the input node must be selected on the mextra node cifplot, cross referenced to its respective SPICE node number and that SPICE number used in the filename.spice file when a model input voltage is applied to it for simulation.

10. The next step is to input all the required/desired command (cards) lines to run the

D-4

simulation using the node numbers from SPICE node reference list but based on the nodes assigned by mextra on the node cifplot. The required command line (card) inputs and the format rules required by SPICE are presented below.

The following command line (card) inputs must be included in the filename.spice file and the associated rules presented must be adhered to:

a. All command lines (cards) must begin with a period.

b. The first line of the input file must be a title:

     i.e.   CMOS/SOS TRANSIENT ANALYSIS

This will be printed on each page of the results output. A "dot" command on the first line will cause the run to abort, since the simulator will think it is the title and skip it as a desird command.

c. The .WIDTH command line is used next to establish the last column read on each line. It is normally established at 80.

d. The .OPTIONS command line is then used to establish program control as desired. The documentation on pages 20-21 of the original users guide is adequate for explaining the options available.

e. The user is allowed to select models of the devices that are to be simulated using the .MODEL command line. Since MOS models were used for this thesis, three possible level models were available, (see page 16 in users guide). The level 1 model was selected.

A diode, two bipolar and MOSFET and JFET models are available (see pages 13-18 in the users guide). The user can select specific parameters per device model. Since CMOS/SOS was used for this thesis, two MOSFET models were used, PMOS and NMOS.

f. After selecting models, the V_{dd} supply voltage must be established. Voltage sources are established by using ELEMENT commamd lines (cards). Resistors, capacitors, inductors, transmission lines can also be set-up using this ELEMENT command line model. An independent 5 volt DC voltage source was established (see pages 8-9 in users guide) as the supply voltage. The node to which the voltage is applied is left up to the users discretion.

g. The sim2spice file data is input after the supply voltage command line is established.

h. Input voltages to the circuit are modeled the same way. However, the PULSE option was used in this thesis to provide a varying pulsed input for transient delay analysis. This is described on page 9 of the users guide.

i. The .TRAN command line is used to establish the

time interval of the simulation, (40 nsec was used for all simulations in this thesis) and the points at which the transient waveform is traced on the output plot (0.5 nsec intervals were used for all simulations in this thesis. See page 25 of the users gyuide for further details.

j. The .PLOT comand line estbalishes that a waveform output plot is desired. The TRAN option of this command indicates that a transient plot is desired. The nodes to be monitored and their respective values plotted over the selected simulation time interval are selectable by the user.

k. The input file must be concluded with a .END command line.

11. The only other modification that may be required is a modification of the capacitance values generated by sim2spice when the filename.spice file is generated form the filename.sim file. The values are given in femtofarads and these sometimes are so small that plotted results are worhtless. Some factor of ten may be required to achieve good output results.

Some of these procedures are tedious, however no shorter, more convenient way could be determined to prepare for and perfrom the simulations using the tools that were

available at AFIT.

Example input files and simulation data are provided in previous appendices for reference.

Hopefully this user guide addendum will aid future users of SPICE2.

Appendix E

This appendix is intended to provide information on the Memory/ALU Bitslice circuit chip that was designed as part of this thesis.

The chip contains the 2x4 precharged decoder, the precharged A and B registers, the ALU input controller, the read/write controller, the 4x4 static RAM and the ALU first bitslice along with input, output, ground and V_{dd} pads.

The chip files are included under bkelley/thesis in this authors directory. The directory listing is presented below:

```
README
chip.cll
ramcell.cll
4bitword.cll
4wordmem.cll
Aregpre.cll
Bregpre.cll
alucntrl.cll
RWcontrol.cll
bslast.cll - bitslice precharged at 4 nodes
decpre4a.cll
padamp.cif
padVdd.cif
padblank.cif
padgrnd.cif
padout.cif
padin.cif
paddrve.cif
```
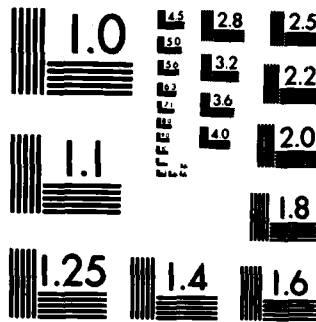
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

VITA

Brian T. Kelley was born on 6 June 1957 in Framingham, Massachusetts. He graduated from Medway Junior-Senior High School in 1975 and attended Worcestor Polytechnic Institute in Worcestor, Massachusetts, where he received the degree of Bachelor of Science in Electrical Engineering in October 1979. Upon graduation, he was commissioned a scond lieutenant in the USAF through the ROTC program. From June 1979 through May 1983 he was stationed at McClellan AFB, California where he served as a Communications Systems Engineer for the Satellite, Surveillance and Electronic Warefare Reliability Engineering branch of the Material Management Acquisition Division of Sacramento Air Logistics Center. In May 1983, he entered the School of Engineering, Air Force Institute of Technology to pursue a graduate degree in digital engineering and Very Large Scale Integration (VLSI) electronics design.

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Methods of increasing the operating speed of integrated circuits were investigated and a reference to speed-up techniques was generated. Precharging, a specific technique, was applied to existing and newly designed CMOS/SOS circuit elements and evaluated. SPICE was used for transient signal analysis.

Precharging was applied to a test circuit, the first bitslice of a previously designed ALU circuit and three newly designed chip circuit elements, to determine its effect on the operating speed of each circuit. Precharge configurations of each circuit were then simulated with SPICE.

The results of this thesis research indicate that precharging can be applied to both existing and newly designed circuits, that it significantly reduces low-to-high signaltransition delays, if applied correctly, and in general, it has a detrimental effect on high-to-low signal transitions, and increases the associated delays. In addition, the effectiveness of precharging is dependent on the amount of current applied to the precharged nodes.

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