DataGeneral

Technical Reference

microNOVA COMPUTER SYSTEMS

014-000073-00

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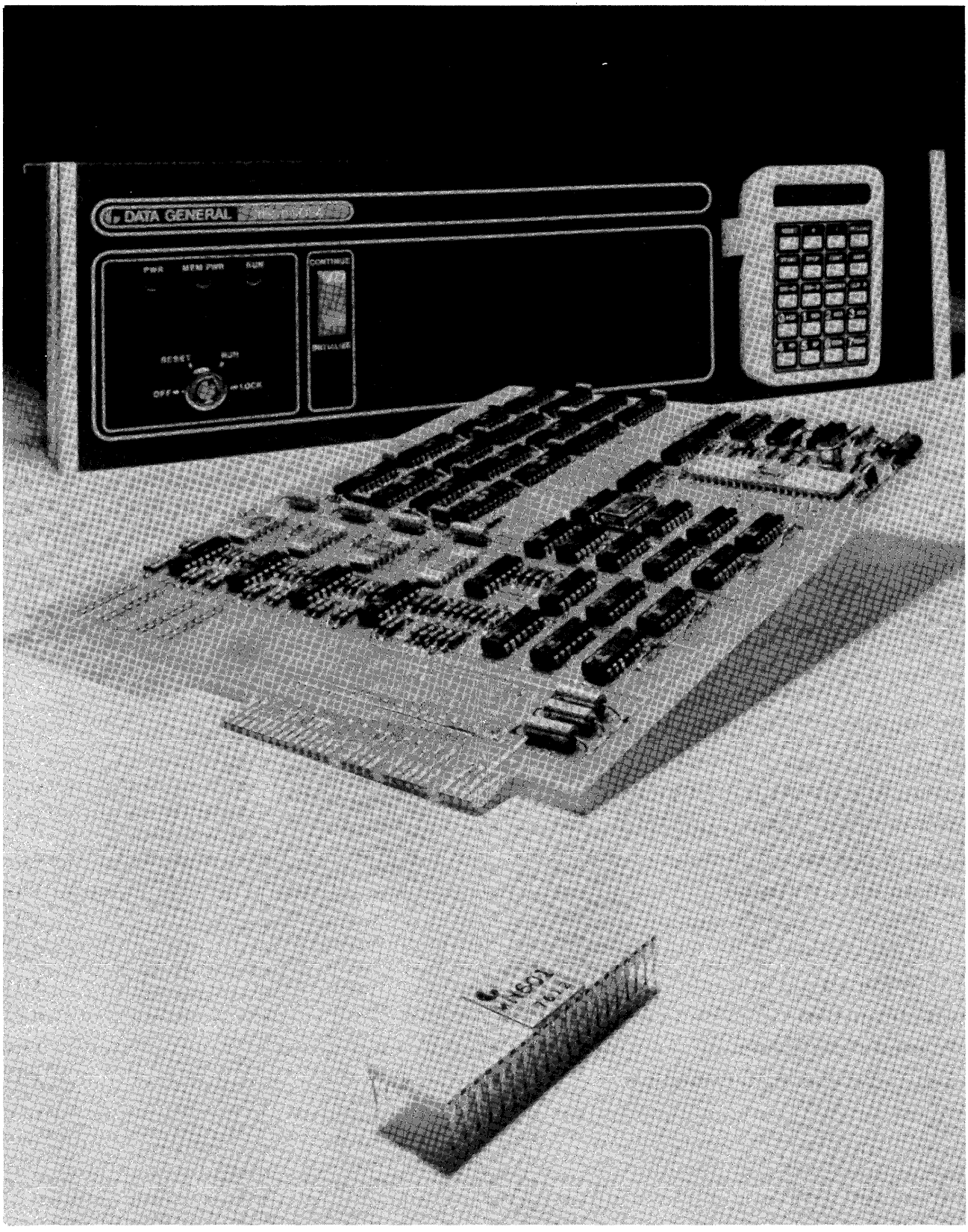
DATA GENERAL
PWR
MEM PWR
RUN
CONTINUE
RESET
RUN
OFF
LOCK

SECTION I
microNOVA
COMPUTER SYSTEMS

INTRODUCTION AND OVERVIEW

The microNOVA computer systems are organized around the microNOVA microprocessor, a general-purpose, user-programmable processor which resides on a single LSI N-channel MOS chip. The microNOVA processor has a word length of 16 bits, four accumulators for arithmetic and logical operations, and the capability to address up to 32,768 words of dynamic RAM and/or programmable ROM (PROM) memory. Two independent buses are used to communicate with memory and with I/O devices. The memory bus is used to both access and refresh memory, and consists of sixteen bidirectional data lines and four control lines. The I/O bus is capable of driving I/O devices as far as 100 feet from the microNOVA processor, and consists of a 2-bit bidirectional differential data bus, timing lines, and control lines. The microNOVA computer is software-compatible with Data General's NOVA line of computers, and has the same instruction set as the NOVA 3 computer.

The microNOVA computer is available as a complete computer system, as assemblies such as the CPU and 2K/4K RAM board, and as chips such as the CPU and the I/O Controller (IOC). The availability of the separate assemblies and chips gives the customer the flexibility either to construct a computer system tailor-made to his particular applications from the parts available or to purchase the complete microNOVA computer system packaged by Data General. The assemblies which can be purchased separately or combined to form a complete microNOVA computer system are as follows:

CPU and 2K/4K RAM Board
4K/8K MOS RAM Board
Programmable Read-Only Memory Board
Hand-held Console Subsystem
Asynchronous Interface Board
Diskette Subsystem
PROM Programmer Board
General Purpose Interface Board
General Purpose Wiring Board
Extender Board
9-slot/18-slot Main Chassis
I/O Expansion Chassis
Card Frame Assembly
Power Supply Assemblies

Each of the boards in the system is a 7.5 inch wide printed circuit board suitable for installation in the microNOVA main chassis, the microNOVA I/O expansion chassis, or the microNOVA card frame assembly. The boards vary in length from 9.9 to 11.7 inches.

CPU and 2K/4K RAM Boards

A microNOVA CPU and 2K/4K RAM board is a single 7.5 by 10.4 inch printed circuit board containing a microNOVA CPU, 2K or 4K words of dynamic N-channel MOS random access memory, a timing generator, and interface circuitry for the memory bus and the I/O bus. The word length for both the CPU and the memory is sixteen bits. The CPU contains four accumulators, a program counter, a stack pointer, a frame pointer, and a real-time clock. A general-purpose instruction set, which includes multiply and divide functions as standard features, is available for programming the microNOVA processor. The instruction set is software-compatible with the instruction set of the NOVA line of computers, and is identical to the instruction set of the NOVA 3 computers.

The memory buffering and control circuitry contained on the CPU and 2K/4K RAM board can support up to 32K words of memory within a microNOVA computer system. Memory refresh operations for dynamic RAM are totally hidden, since the memory is refreshed in parallel with processor operations during cycles in which memory is neither read nor written.

The I/O capabilities supported by the CPU and 2K/4K RAM board are programmed data transfer, 16-level programmed priority interrupts, and a data channel capability. The I/O bus can support up to 30 I/O devices, and can be up to 100 feet in length.

Edge-mounted controls and indicator lights are available as an option with the CPU and 2K/4K RAM board. The controls are start, halt, continue, and lock, and the indicator lights are run, AC power, and battery power. These controls and lights provide a means for controlling the operation of the CPU when the board is not part of a complete microNOVA computer system.

A power fail/auto-restart capability is standard with the CPU and 2K/4K RAM board. An automatic program load capability is optional. The starting addresses of the particular restart and program load procedures used are determined by jumper settings on the board. Two features are available to provide user flexibility in restart and program load procedures: 64 words of ROM which can be enabled to override memory locations $77700\text{-}77777_8$, and a jumper word associated with memory location 77776_8 or 77777_8 which can be used to establish the starting addresses of the particular routines, or the device and mode for automatic program load.

Memory Boards

The microNOVA 4K/8K MOS RAM board contains either 4K or 8K 16-bit words of dynamic random access memory and associated logic. The memory has a cycle time of 960 nanoseconds and must be refreshed once every 2.4 milliseconds. Each refresh operation will refresh a single block of 64 adjacent words. The block of addresses associated with the memory is selected with jumpers.

The programmable read-only memory (PROM) boards contain sockets for 512, 1024, 2048, or 4096 16-bit words of programmable read-only memory and associated logic. The 512 word and 1024 word PROM boards contain eight sockets for either 1024-bit (256 x 4) or 2048-bit (512 x 4) PROM chips. The 2048 word and 4096 word PROM boards contain 32 sockets for either 1024-bit (256 x 4) or 2048-bit (512 x 4) PROM chips. The block of addresses associated with the memory is selected with jumpers.

Within a microNOVA computer system, RAM and PROM can be mixed in any combination up to 32K words of memory.

Peripherals

The hand-held console subsystem consists of a hand-held programmer's console, an I/O controller on a 7.5 by 10.4 inch printed circuit board, and a 10-foot 16-conductor ribbon cable which connects the console to the controller. The hand-held console is calculator-like in appearance with 20 push-button keys and a 6-digit display area. The I/O controller contains 256 words of ROM and RAM, corresponding to and taking precedence over any other RAM associated with addresses $77400\text{-}77777_8$. The controller memory contains standard software which enables the hand-held console to be used to examine and modify the contents of memory locations and internal CPU registers, and to control the operation of the processor with functions such as start, stop, and reset. The standard software also includes an automatic program load capability. User software can be used in place of the standard software to redefine the functions associated with the console keys.

The asynchronous interface board consists of a controller for a single asynchronous terminal or communications line and, optionally, a console debugger. The controller performs full-duplex character assembly and disassembly, with the input and output signals conforming to either EIA RS232-C (CCITT V-24) or 20mA current loop specifications. Any standard transmission speed from 50 baud to 19,200 baud is available. The transmission speed, the number of data bits and stop bits per character, the type of parity associated with each character, and the line specifications (EIA RS232-C or 20mA current loop) are selected with jumpers. In addition, the controller includes a modem control capability.

The console debug option available with the asynchronous interface board allows any ASCII terminal to be used as a system debugging console. With this option, the terminal can be used to examine and modify the contents of memory locations and internal CPU registers, to control the operation of the processor with functions such as start and continue, and to set and clear breakpoints. An automatic program load capability is also included with the console debug option. The console debug option program resides in 256 words of ROM and RAM on the asynchronous interface board. This ROM and RAM correspond to and take precedence over any other RAM associated with addresses $77400\text{-}77777_8$. Since both the console debug option and the hand-held console subsystem contain ROM associated with addresses $77400\text{-}77777_8$, they are mutually exclusive options within a microNOVA computer system.

The diskette subsystem provides removable, direct access, moving head disc memory for the microNOVA computer systems. The subsystem consists of one or two drive units in a rack-mountable chassis, a controller on a 15" square printed circuit board contained within the drive unit chassis, and an external I/O bus cable for connection to the I/O bus of a microNOVA computer. Each diskette can store up to 157,696 16-bit words in blocks of 256 words. The maximum data transfer rate is 15,625 words per second.

The PROM programmer board provides the capability to program and verify a complete PROM board, one word at a time, under program control. The PROM programmer board has two female board connectors along one 7.5 inch edge of the board for connection to any of the microNOVA PROM boards. The memory on a PROM board is programmed by inserting PROM chips in the sockets of the PROM board, inserting the PROM board in the PROM programmer board connector, and issuing the appropriate I/O instructions to program and verify the contents of memory.

General Purpose Boards

The general purpose interface board provides the basic logic required by a customer building an I/O device controller for inclusion in a microNOVA computer system. The board contains an IOC, an I/O bus transceiver, and supporting logic for a generalized I/O interface including programmed I/O, program interrupts, and a data channel capability. In addition, the board has drilled holes and etched conductors to accommodate chips in 14, 16, 18, 20, 22, 24, 28, and 40-pin packages. The maximum number of chips that can be added to a general purpose interface board is 32 14-pin chips. The general purpose interface board is also available with sockets and wire wrap pins to accommodate a combination of up to 27 14-pin and 16-pin packages.

The general purpose wiring board is a 7.5 by 10.4 inch printed circuit board containing only drilled holes and etched conductors to wire wrap pins. The board is designed to be used by the customer building his own assembly for inclusion in a microNOVA computer system. The board can accommodate up to 50 chips in 14-pin packages, and can accommodate a lesser number of chips in combinations of 14, 16, 18, 20, 22, 24, 28, and 40-pin packages.

The extender board provides the capability to gain direct access to the components of another printed circuit board in a microNOVA computer system for debugging and maintenance purposes. The board has two female board connectors along one 7.5 inch edge of the board for connection to any microNOVA computer system board. The extender board is inserted in the chassis slot of the board to tested, and the board to be tested is plugged into the extender board. Etched conductors on the extender board carry all the back panel connections to the extended printed circuit board.

Chassis

The microNOVA main chassis is a 19" rack-mountable chassis available in both 9-slot and 18-slot configurations. The 9-slot chassis contains a 9-slot card frame and a power supply mounted side-by-side across the front of the chassis. The battery backup option, if present, is mounted on a support behind the power supply. The 18-slot chassis contains two 9-slot card frames mounted side-by-side across the front of the chassis, and a power supply mounted behind the left card frame. The battery backup option, if present, is mounted behind the right card frame. Both chassis have a front panel which swings aside to provide front access to the printed circuit boards. The front panel contains a power-on keylock switch, a rocker switch, three indicator lights, and a place to attach the hand-held console. I/O device cables connect directly to the I/O controller printed circuit boards at the rear of the card frames. Strain relief is provided for the I/O device cables at the rear of the chassis.

The microNOVA I/O expansion chassis is a 9-slot 19" rack-mountable chassis, similar to the 9-slot main chassis but designed to house only I/O device controller boards. The chassis contains a 9-slot card frame, a power supply, a front panel, and strain relief for I/O device cables. The front panel contains a power-on keylock switch, but does not contain the rocker switch, indicator lights, and hand-held console attachment contained on the front panel of the main chassis.

The microNOVA card frame assembly contains 9 slots for 7.5 inch wide printed circuit boards. The assembly consists of a stamped metal frame with stiffener and card guides, an etched backpanel, and female board connectors to the backpanel. The backpanel carries the memory bus signals and I/O bus signals to the boards mounted in the card frame. The memory bus signals are enabled only when a CPU and 2K/4K RAM board is mounted in the bottom slot of the card frame. The I/O bus signals can be chained from the CPU card frame to other card frames with an external I/O bus cable. Each slot has a metal retainer for attaching an I/O device cable connector. The card frame includes a DC power cable for connection to the power supply.

Power Supply

The power supply provides 18 amps at +5 volts dc, 2.5 amps at +15 volts dc, and 1.2 amps at -5 volts dc. This is sufficient power to support a fully-loaded 18-slot chassis containing standard microNOVA computer system boards. Low voltage switching regulators control the +5 volt and +15 volt portions of the power supply by independent pulse width modulation, and control the -5 volt portion of the power supply by variable pulse rate generation. An AC line filter, independent overvoltage and overcurrent sensing, and a power-fail monitor provide system protection. Any of the standard line voltages of 100 volts, 120 volts, 220 volts, or 240 volts in the frequency range of 47-63Hz may be used to drive the power supply; only the AC line cord is different for the different line voltages. The arrangement of the pins within the AC line cord/power supply connector selects the correct transformer taps for the line voltage being supplied.

A battery backup option is available with the power supply to provide sufficient power to keep up to 32K of dynamic random-access memories refreshed for as long as 45 minutes during a power failure. The battery backup option consists of two 12-volt battery packs connected in series, battery switchover circuitry, and battery recharge circuitry.

PACKAGED SYSTEMS

A microNOVA computer system can be purchased in any one of several packaged system configurations. The CPU and 4K RAM board can be purchased with either a 9-slot or 18-slot chassis. In addition, a complete microNOVA development system can be purchased, where the development system includes a CPU, 16K RAM, an 18-slot chassis with the battery backup option, a hand-held console subsystem, a dual diskette subsystem, a box of 10 diskettes, an asynchronous interface board, either an ASR33 or KSR35 Teletype®, a 72" equipment cabinet with filler panels, and all applicable system cabling.

The microNOVA development system is fully supported by Data General software. This software includes the diskette-based Disc Operating System (DOS), FORTRAN IV with real-time extensions and library routines, an editor, a macro assembler, a relocatable loader, and a symbolic debugger.

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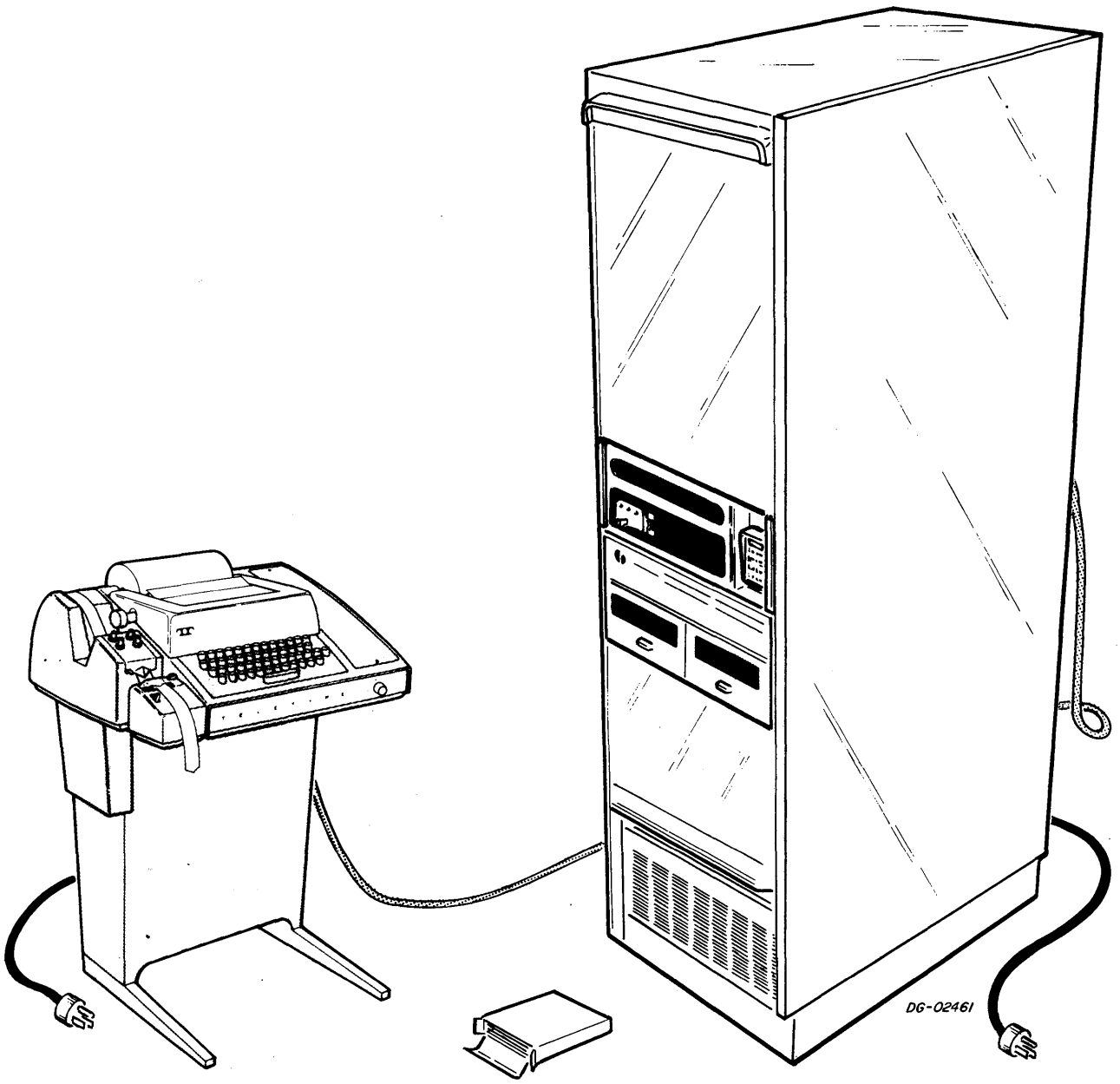
microNOVA DEVELOPMENT SYSTEM



ASR33 TELETYPE

BOX OF 10 DISKETTES

18 SLOT SYSTEM IN RACK WITH DISKETTE

CODING AIDS

In the descriptions of the separate instructions, the general form in which the instruction is coded in assembly language is given along with the instruction format and the description of the instruction. The general form in which an instruction may be coded has the following format:

MNEMONIC *[optional mnemonics]* **OPERAND STRING**

The mnemonic must be coded exactly as shown in the instruction description. Some instructions have optional mnemonics that may be appended to the main mnemonic if the option is desired. The operand string is made up of the operands for the given instruction.

Square brackets "[ ]" or *"[ ]"* along with boldface- and italic-printed symbols are used in this manual to aid in defining the instructions. These conventions are used to help describe how an instruction should be written so that it can be recognized by the assembler and translated into the correct binary, or machine language, representation. Their general definition is given below.

[ ], *[ ]* Square brackets indicate that the enclosed symbol is an optional operand or mnemonic. The operand enclosed in the brackets (e.g., *[,skip]*) may be coded or not, depending on whether or not the associated option is desired.

BOLD Operands or mnemonics printed in boldface must be coded exactly as shown. For example, the mnemonic for the MOVE instruction is coded **MOV** .

italic Operands or mnemonics printed in italics require a specific substitution. Replace the symbol with the number of a desired accumulator, or address, or with a user-defined symbol that the assembler recognizes as a specific name, address, number, or mnemonic.

The following abbreviations are used throughout this manual:

AC = Accumulator

ACS = Source Accumulator

ACD = Destination Accumulator

F = Flag Control Function

When describing the format or a word involved in an information transfer between the computer and an I/O device, the various fields and bits in the word are labeled with names descriptive of their functions. Bits in the word which are not used by the I/O device controller are shaded. Shaded bits are ignored on output and are undefined on input.

RELATED MANUALS

Two other manuals describe portions of the microNOVA computer family. The Technical Reference for microNOVA Integrated Circuits *(DGC no. 014-000074)* describes the major integrated circuits which form the basis of a microNOVA computer system, including detailed timing diagrams and electrical specifications for each integrated circuit. The Programmer's Reference Manual for microNOVA Computers *(DGC no. 015-000050)* describes the instruction set of the microNOVA computers.

SECTION II
CPU AND 2K/4K RAM BOARD

The microNOVA CPU board is an LSI minicomputer on a single 7.5 by 10.4 inch printed circuit board; it contains a complete, Data General NOVA-line, 16-bit word length, central processor in a single 40-pin package, and includes a real-time clock, Power Fail/Auto-restart, plus provision for automatic program load and on board console options. The board contains all support and interface circuits needed to connect the processor to separate, external, I/O and memory buses and to a turnkey console. It also contains 2,048 or 4,096 16-bit words of 960ns read-write memory (RAM). By itself, the CPU board can be integrated into a variety of special applications; combined with other microNOVA system pieces, it is the basis of a complete microprocessor-based computer system.

OVERVIEW AND INTRODUCTION

The quality and power of a general purpose, microprocessor-based, computer system depends to a large measure on: *i)* the flexibility of its instruction set and the power of its central processing unit (CPU); *ii)* the availability of utility and development software; *iii)* the type and structure of the information paths into and out of the CPU; and *iv)* the size and power needs of the pieces that make up the system.

Data General's microNOVA CPU board executes the proven NOVA (NOVA 3) instruction set. It is a powerful, flexible, instruction set that combines high speed, multiple operation, fixed point, logical operations with hardware multiply/divide, hardware PUSH/POP stack, and a tightly optimized I/O handling capability. Most importantly, it is an instruction set for which Data General has already developed extensive software. This means that users can develop and optimize new applications software on any NOVA line computer system with all the resources available in proven Data General operating systems, compilers, run-time libraries, and peripherals.

The microNOVA CPU board exchanges information with memory and peripherals over two independent information transfer paths: the memory bus and the I/O bus. The CPU board contains a transceiver and control buffers for the memory bus; a 16-bit wide, parallel, synchronous, TTL-level bus by which the central processor communicates with microNOVA memory boards, or with special customer-designed memories. The board also contains the drivers and control buffers for a 2-bit wide, differential, serial I/O bus by which the central processor communicates with microNOVA peripherals or customer-designed I/O interfaces containing the microNOVA IOC.

The microNOVA CPU is packaged as a complete minicomputer on a single 7.5 by 10.4 inch printed circuit board. Built around a single-chip, low power loss, microprocessor that is designed and fabricated by Data General's semiconductor division, the CPU board is compact, and it easily lends itself to special applications when used alone, or when it is combined with other pieces in the growing microNOVA famiily of computers.

SUMMARY OF CHARACTERISTICS

CENTRAL PROCESSOR		
Operations	Instruction Execution	
	Fixed Point Arithmetic	
	Logical Operations	
	Stack Manipulation	
	Program Flow Alteration	
	Input/Output	
	Interrupts	
	Power Fail/Power Restore	
	Real-time Clock	
	Stack Overflow	
	External	
	Data Channel Transfer	
	Input: 6.7microseconds/16-bit word	
	Output: 5.8microseconds/16-bit word	
	Automatic Program Load (optional)	
	Memory Refresh (hidden)	
Registers	4 16-bit accumulators	
	1 15-bit stack pointer	
	1 15-bit frame pointer	
	1 15-bit program counter	
	1 interrupt enable flag	
	1 real-time clock enable flag	
	1 carry bit	
	1 stack overlfow flag	
Buses	Memory	
	16 address/data lines	
	4 control signals	
	I/O	
	2 bit serial, synchronous, bidirectional	
	I/O clock, master cock, 2 request lines	
	2 priority lines	
	Maximum total length: 100 ft. (30.5m)	
MEMORY		
Memory Type	Dynamic MOS N-channel RAM.	
Board Capacity	2,048 or 4,096 16-bit words.	
Cycle Time	Read	960ns.
	Write	960ns.
	Read/Modify/Write	1440 ns.
	Refresh	960ns.
Maximum Refresh Period	2.4 milliseconds.	
Board Dimensions	7.5 x 9.9 in. (19 x 24.9 cm.)	
Maximum Operating Temperature	131°F (55°C)	

BLOCK DIAGRAM

The block diagram on the opposite page shows the principal components plus the data and control paths of a microNOVA CPU board. This board contains a microNOVA microprocessor (CPU), 2,048 or 4,096 words of dynamic read-write memory (RAM), and power startup and fail controls. It has connections to the memory and I/O buses and frontpanel. The board may also contain the automatic program load option.

The CPU board contains eight principal data paths and components. These paths include:

CPU to memory bus
CPU to I/O bus
Power up/fail, and run control
On board memory
Special function jumpers
CPU and turnkey console
Auto-restart
Automatic program load option

The first five of these paths and control functions encompass the basic structure of the CPU board. The turnkey console controls, auto-restart, and the program load option take effect by gaining, on an exceptional basis, overriding control over that basic structure.

CPU to Memory Bus

Communication between the processor and memory take place along a memory bus. The memory bus operates at TTL levels; it is a wired OR, half duplex, 16-bit wide, address and data path. The operations which take place on it occur synchronously, under CPU direction. Such operations include Read memory, Write memory, Read-Modify-Write memory, and Refresh memory. All information that moves on the memory bus does so in bit parallel fashion, 16-bits at a time.

The CPU connects to the memory bus through its memory interface which includes a 16-bit wide bidirectional, time multiplexed, address and data path, 4 memory control signals, a 16-bit memory transceiver, and the memory control buffer. The control signals direct the flow of information along the address and data path.

The CPU's memory interface supports the flow of information between the central processor's memory port and the microNOVA memory bus. The protocols by which the CPU communicates with memory are described in the Technical Reference for microNOVA Integrated Circuits *(DGC no. 14-000074)*.

microNOVA CPU AND 2K/4K RAM BOARD

* Mem Cntrl Signals

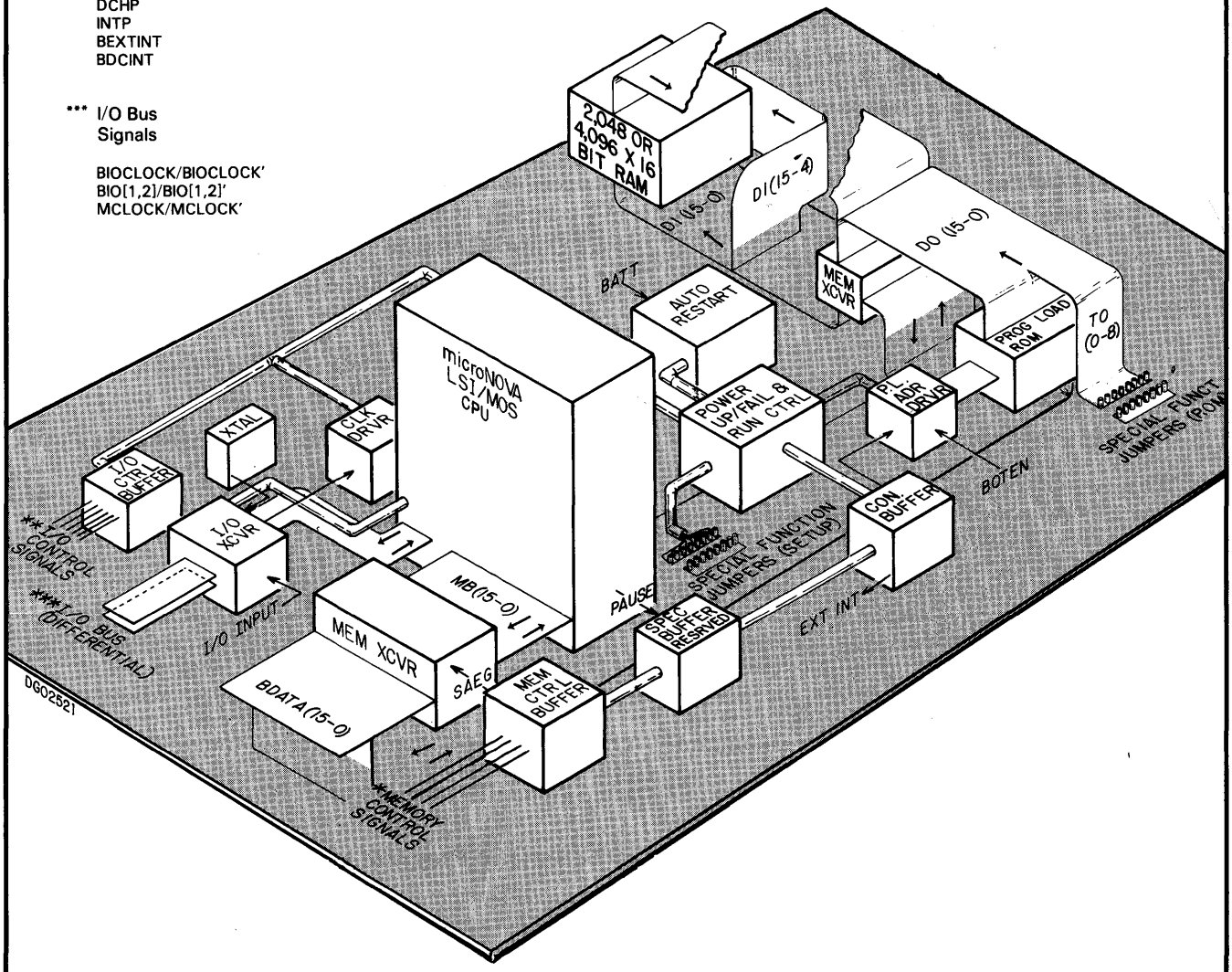
BSAEG
BWEG
BPG
PHIL

** I/O Cntrl Signals

CLEAR'
DCHP
INTP
BEXTINT
BDCINT

*** I/O Bus Signals

BIOCLOCK/BIOCLOCK'
BIO[1,2]/BIO[1,2]'
MCLOCK/MCLOCK'



CPU to I/O Bus

Communication between the processor and peripherals take place along the I/O bus. The microNOVA I/O bus is a bidirectional, 2-bit, synchronous data path from the CPU to any device that needs direct program control or data channel service. It consists of 9 signals, four of them differential. All information is placed on and read from two differential lines in conjunction with an I/O clock signal carried on a third differential line; the remaining lines carry the system clock, and a reset signal, along with priority and request lines for program interrupt and data channel service. Information moves on the bus in bit serial fashion with a coded header, two bits or 18 bits at a time. The I/O bus is carried up the chassis backpanel and may extend 100 feet from it using 16-wire ribbon cable.

The CPU connects to the I/O bus through its I/O interface which includes a 2-bit wide, bidirectional, serial data path, two clock lines, 5 I/O control lines, a 4-line TTL to differential bus transceiver, and a I/O control buffer. The master clock for a microNOVA computer system is derived from the crystal oscillator connected to the CPU's I/O transceiver.

The CPU's I/O interface supports the flow of information between the central processor's I/O port and the microNOVA I/O bus. The protocols by which the CPU communicates with peripherals is described in the technical reference cited above.

Power Up/Fail, and Run Control

The CPU board includes control circuits to direct the CPU's operation when power is first applied to the microprocessor, while it its running, and as power drops. These circuits include the a power up/fail and run control, and a CPU clock driver.

The power up monitor holds the CPU in a well defined state and resets the computer during a cold startup. It then allows the processor to start when directed to do so by the console controls. The power up requirements of the microNOVA CPU are described in the technical reference cited above. The power fail monitor signals the processor with an interrupt several milliseconds before power fails.

The CPU clock driver amplifies the system master clock which is derived from a crystal oscillator connected to the I/O bus transceiver. It provides precise, non-overlapping clock signals required to run the processor.

On Board Memory

The CPU board holds an entire read-write memory module which connects directly to the microNOVA memory bus. The memory consists of one bank of dynamic RAM with 2,048 or 4,096 16-bit words, 16-bit wide data in and data out paths, a 12-bit address path, four memory control lines, a 16-bit memory transceiver and a memory control buffer. Memory address jumpers (not shown) assign the lowest address in the module to any 4K memory address boundary in the system.

The construction of the on board memory is similar to that of other RAM modules for the microNOVA systems. The flow of information within the module and also between it and the memory bus is described in section III.

Special Function Jumpers

The board contains two groups of jumpers which define the response of the CPU to certain console functions, and define its action during auto-restart. One group of jumpers is an 8 bit ROM, the other group of jumpers define how that ROM is interpreted.

The 8-bit jumper ROM connects to the memory bus through the memory transceiver for the CPU memory module. Depending on the configuration of the setup jumpers, the ROM jumpers are disabled or their contents are made available to the CPU during certain memory read operations.

CPU and Console

The CPU board includes a control circuit and signal buffer for the switches and indicators of the microNOVA turnkey console; the board may optionally have a group of switches and indicator lights for console functions.

Signals from the console switches and indicators pass through the console buffer to the power up/fail, and run monitor, to the program load address driver and the auto-restart monitor.

Auto-restart

Auto-restart includes a circuit that monitors the conditions of a backup battery, the position of the LOCK switch of the turnkey console, and the configuration of the setup jumpers. When power returns after a power failure, this circuit can initiate an automatic restart by gaining control over selected I/O and memory control lines and directly manipulating the value of bit 15 on the memory bus.

Automatic Program Load Option

When the automatic program load option is installed, it includes a 16-bit information path through the CPU memory transceiver to the memory bus, control lines to the console buffer and the power up/fail and run control, a 64 word ROM, and a a 6-bit address driver. When an automatic program load is initiated, the option gains control over selected I/O and memory control lines. The CPU executes a series of instructions stored in the program load ROM, and transfers the microNOVA bootstrap program from there to memory locations $2\text{-}32_8$.

PROGRAMMING

The microNOVA CPU processes information one word at a time, where a word is 16 bits in length. The CPU has four accumulators which are also 16 bits in length and are used for arithmetic and logical operations. Furthermore, two of the accumulators can be used as index registers. Memory can be addressed either directly or by using indirect addressing. Chains of indirect addresses may be up to eight addresses long.

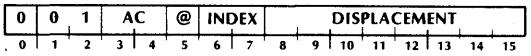
The instruction set for the CPU contains instructions that perform fixed point arithmetic and logical operations between accumulators, transfer of operands between accumulators and memory, transfer of program control, stack manipulations, I/O operations, and processor control operations. All instructions are one word in length. The instruction set of the microNOVA computer is software-compatible with the instruction set of the NOVA line of computers, and is identical to the instruction set of the NOVA 3 computers.

The table on the following pages summarizes the instruction set of the microNOVA computer. For a more detailed description of the instructions, consult the Programmer's Reference Manual for microNOVA Computers *(DGC no. 015-000050)*.

FIXED POINT ARITHMETIC

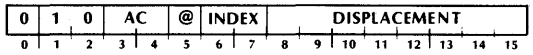
Load Accumulator

LDA *ac,[@]displacement[,index]*



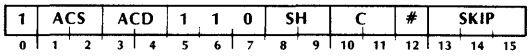
Store Accumulator

STA *ac,[@]displacement[,index]*



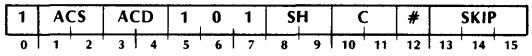
Add

ADD *[c][sh][#] acs,acd[,skip]*



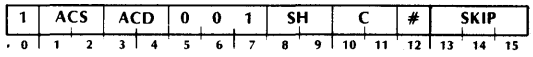
Subtract

SUB *[c][sh][#] acs,acd[,skip]*



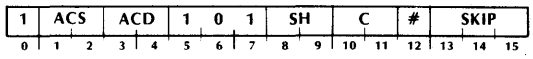
Negate

NEG *[c][sh][#] acs,acd[,skip]*



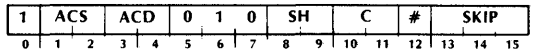
Add Complement

ADC *[c][sh][#] acs,acd[,skip]*



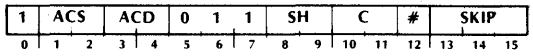
Move

MOV *[c][sh][#] acs,acd[,skip]*



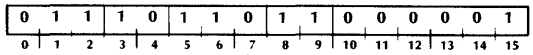
Increment

INC *[c][sh][#] acs,acd[,skip]*



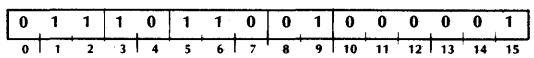
Multiply

MUL



Divide

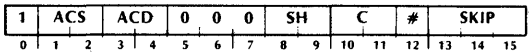
DIV



LOGICAL OPERATIONS

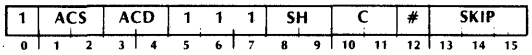
Complement

COM *[c][sh][#] acs,acd[,skip]*



And

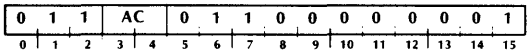
AND *[c][sh][#] acs,acd[,skip]*



STACK MANIPULATION

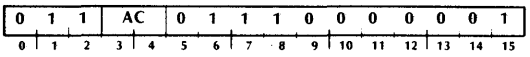
Push Accumulator

PSHA *ac*



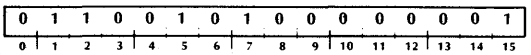
Pop Accumulator

POPA *ac*



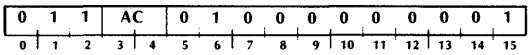
Save

SAV



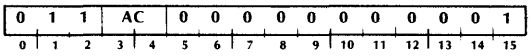
Move To Stack Pointer

MTSP *ac*



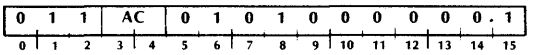
Move To Frame Pointer

MTFP *ac*



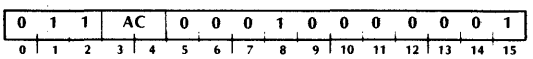
Move From Stack Pointer

MFSP *ac*



Move From Frame Pointer

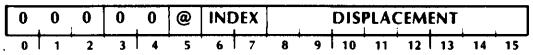
MFFP *ac*



PROGRAM FLOW ALTERATION

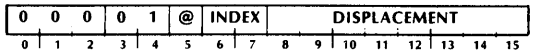
Jump

JMP *[@]displacement[,index]*



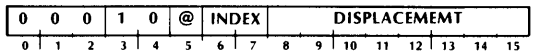
Jump To Subroutine

JSR *[@]displacement[,index]*



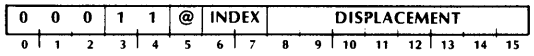
Increment And Skip If Zero

ISZ *[@]displacement[,index]*



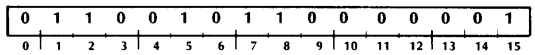
Decrement And Skip If Zero

DSZ *[@]displacement[,index]*



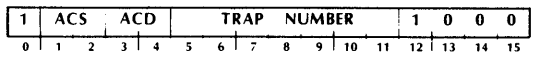
Return

RET



Trap

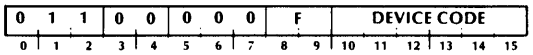
TRAP *acs,acd,trap number*



INPUT/OUTPUT

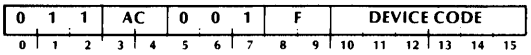
No I/O Transfer

NIO *[f] device*



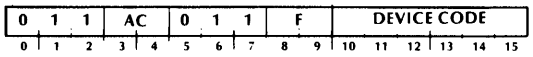
Data In A

DIA *[f] ac,device*



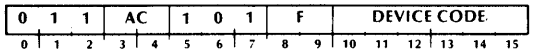
Data In B

DIB *[f] ac,device*



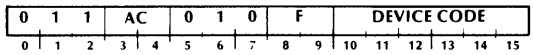
Data In C

DIC *[f] ac,device*



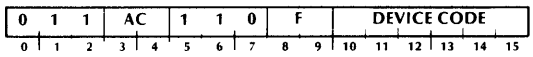
Data Out A

DOA *[f] ac,device*



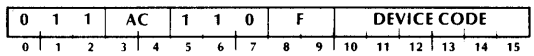
Data Out B

DOB *[f] ac,device*



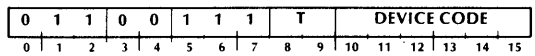
Data Out C

DOC *[f] ac,device*



I/O Skip

SKP *[t] device*

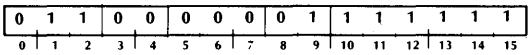


CENTRAL PROCESSOR FUNCTIONS

Interrupt Enable

INTEN

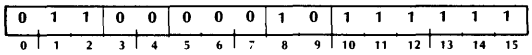
NIOS CPU



Interrupt Disable

INTDS

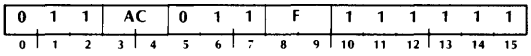
NIOC CPU



Interrupt Acknowledge

INTA *ac*

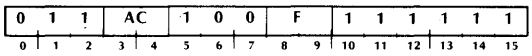
DIB *[f]* *ac*, **CPU**



Mask Out

MSKO *ac*

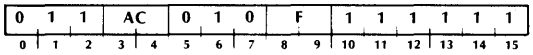
DOB *[f]* *ac*, **CPU**



Reset

IORST

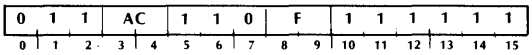
DOA *[f]* **0,CPU**



Halt

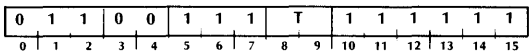
HALT

DOC 0,CPU



CPU Skip

SKP *[t]* **CPU**

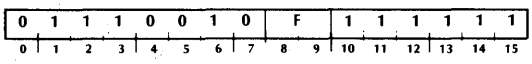


REAL TIME CLOCK

Real-time Clock Enable

RCTEN

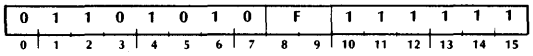
DOA *[f]* **2,CPU**



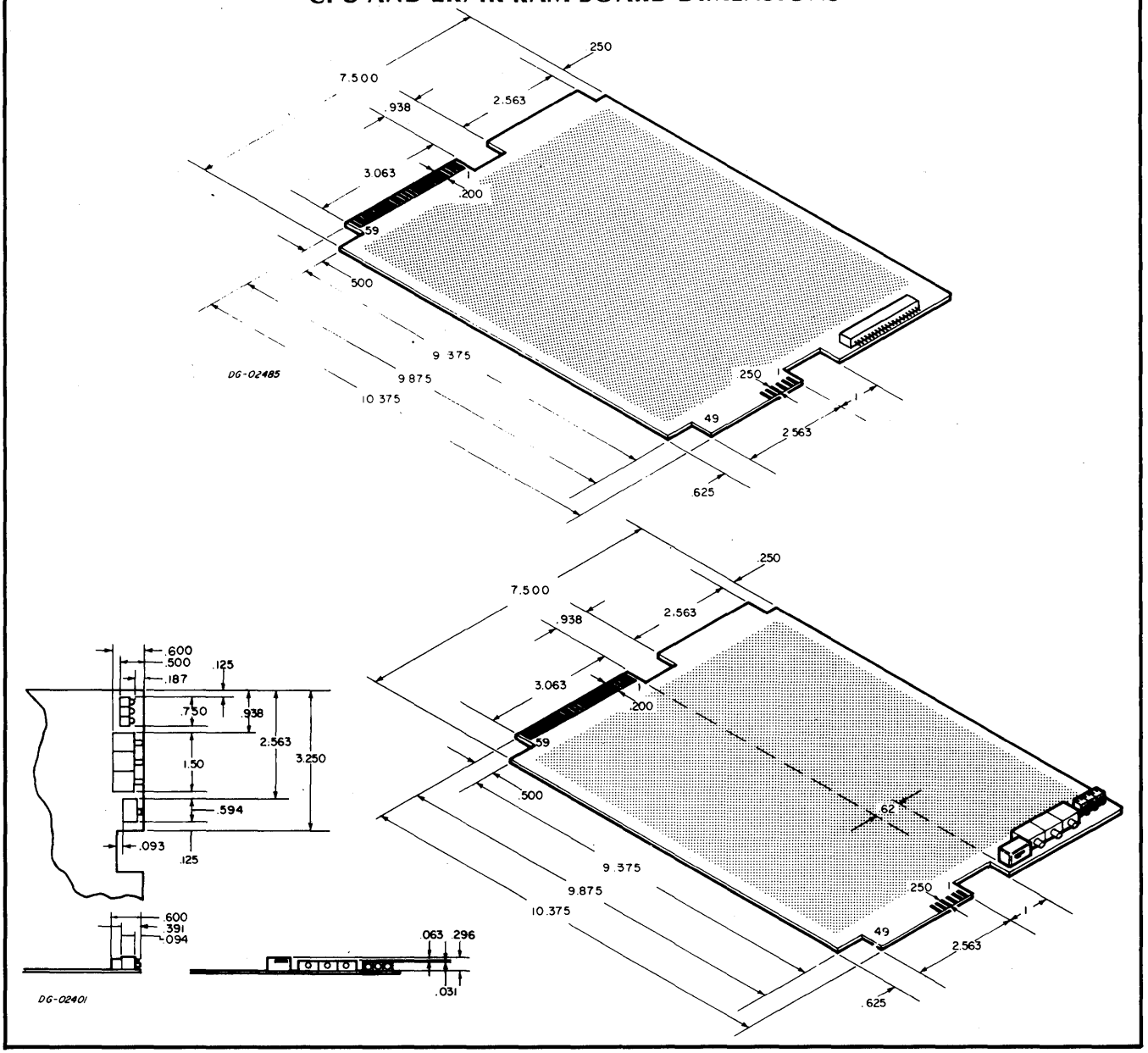
Real-time Clock Disable

RTCDS

DOA *[f]* **1,CPU**



CPU AND 2K/4K RAM BOARD DIMENSIONS



JUMPER WORD ADDRESS

ADDRESS	INSERT JUMPER
077776_8	W5
077777_8	W6

JUMPER WORD REGISTER

BIT POSITION	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CONTENTS (INSERT JUMPER TO SPECIFY 1)	W9	W10	W11	W12	W13	W14	W15	W16	0	0	0	0	0	0	0	1

ADDRESS SELECTION JUMPERS

BIT POSITIONS OF STARTING ADDRESS	1	2	3
INSERT JUMPER TO SPECIFY 1	W1	W2	W3

OTHER JUMPERS

JUMPER	FUNCTION
W4	Insert jumper to enable jumper word register and/or 64 words of local ROM.
W7	Insert jumper to disable auto-restart after a power failure if power is not being supplied by battery backup.
W8	Insert jumper to enable 64 words of local ROM associated with addresses 077700-077777_8.

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SECTION III
RANDOM ACCESS MEMORY BOARDS

Data General's model 8572 and model 8573 random access memory (RAM) boards contain either 4K or 8K of dynamic MOS read/write memory and the circuitry to interface that memory to the microNOVA memory bus. Model 8572 contains 4,096 16-bit words and model 8573 contains 8,192 16-bit words of RAM. These RAM modules, built around the mN606 4K RAM chip perform read, write, and refresh operations in 960ns. A read-modify-write operation is performed in 1440ns.

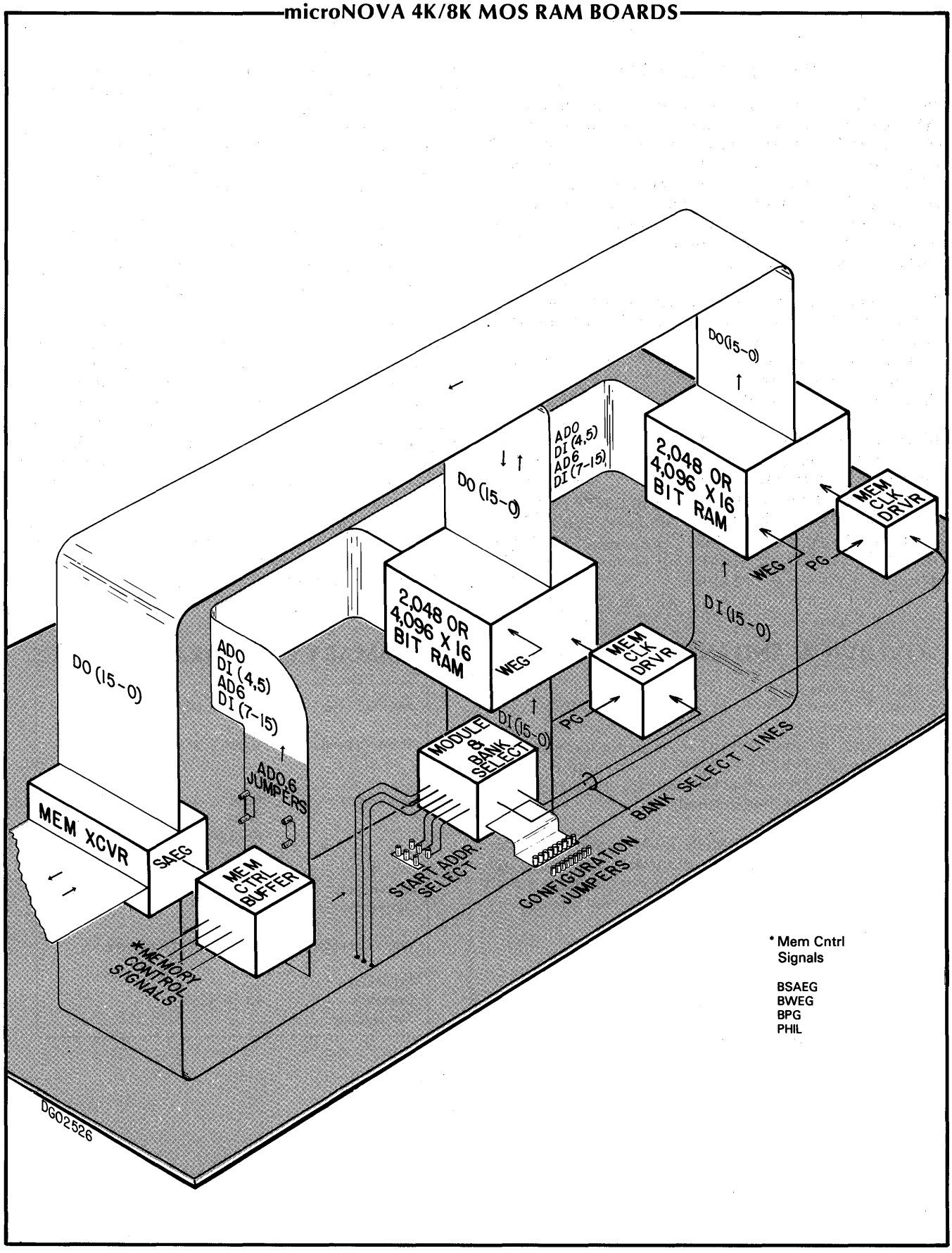
OVERVIEW AND INTRODUCTION

Random access memory (RAM) is a local storage medium whose contents can be read and modified, one word at a time. Dynamic MOS RAM is random access memory that has been constructed using metal-oxide semiconductor (MOS) technology. Dynamic MOS RAM must be refreshed at frequent intervals in order for its contents to be maintained.

The microNOVA 4K/8K MOS RAM board contains 4K or 8K 16-bit words of dynamic MOS random access memory. A microNOVA computer system can access up to 32K words of memory; all 32K words of memory may be RAM.

SUMMARY OF CHARACTERISTICS

Memory Type	Dynamic MOS N-channel RAM.	
Board Capacity	4,096 or 8,192 16-bit words.	
Cycle Time	Read	960ns.
	Write	960ns.
	Read/Modify/Write	1440 ns.
	Refresh	960ns.
Maximum Refresh Period	2.4 milliseconds.	
Board Dimensions	7.5 x 9.9 in. (19 x 24.9 cm.)	
Maximum Operating Temperature	131°F (55°C)	



* Mem Cntrl Signals

BSAEG
BWEG
BPG
PHIL

BLOCK DIAGRAM

The block diagram on the opposite page shows the principal components plus the control and data paths of microNOVA RAM boards. The board is organized into two banks of dynamic RAM memory, each with 2,048 or 4,096 16-bit memory locations. The board contains clock drivers for each memory bank, an address selection/configuration network, a memory bus transceiver, a control buffer, and address data paths for moving information within the board.

The memory transceiver and memory control buffer connect the RAM board to the microNOVA memory bus. The protocols by which the microNOVA CPU communicates with memory are detailed in the Technical Reference for microNOVA Integrated Circuits *(DGC no. 014-000074)*.

When an address appears on the memory bus at the start of a memory operation, the board and bank selection network enables the board if the address on the bus falls within the range of addresses assigned to the board by the placement of its starting address jumpers. The network enables the clock driver for the appropriate memory bank, and the twelve low-order bits of the address are driven onto the RAM address lines. The action taken next by the board depends on the type of memory operation to be performed.

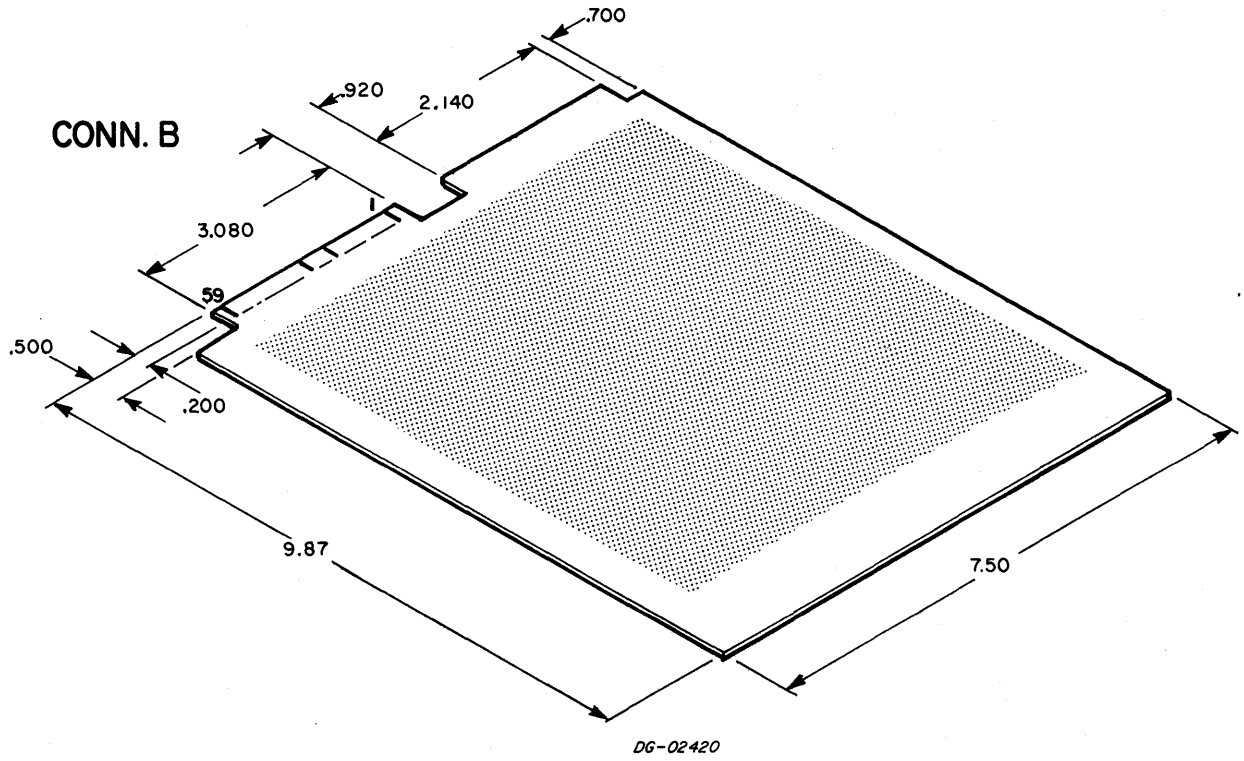
If the operation is a memory read, the memory control signals drive the contents of the addressed memory location onto the board's data out lines to the memory transceiver. If the RAM disable signal **PHIL** has not been asserted by a ROM board assigned to the same address, the memory transceiver places the 16-bit memory word on the memory bus.

If the operation is a memory write, the memory control signals drive the 16-bit word to be written in memory onto the the board's data in **(DI)** path and load it into the addressed memory location.

If the operation is a memory read-modify-write, the memory control signals first drive the contents of the addressed memory location onto the data out **(DO)** path and onto the bus if no ROM is assigned to the same address. The location read remains active until the new data for that address arrives on the bus, and moves onto the boards's data in path; then, the memory control signals load the new data into the memory location just read.

If the operation is a memory refresh, the memory control signals initiate a refresh operation simultaneously on 64 memory locations; no data moves on either the data input or output paths.

RAM MEMORY BOARD DIMENSIONS



ADDRESS SELECTION JUMPERS

BIT POSITIONS OF STARTING ADDRESS	1	2	3
INSERT JUMPER TO SPECIFY 1	W1	W2	W3

SECTION IV
PROGRAMMABLE READ-ONLY MEMORY BOARDS

Data General's microNOVA read-only memories are programmable, 960ns, semiconductor, PROM boards containing from 512 to 4096 16-bit words of directly accessible memory. Any amount of PROM, up to the maximum system memory size of 32K words, may be placed in a microNOVA system; board starting addresses can be assigned to any 2K boundary in memory. PROM may overlay any alterable (RAM) memory locations, where a RAM/ROM priority line arbitrates memory conflicts in favor of ROM. ROM/ROM conflicts (e.g. 4K PROM at the top of memory conflicts with both the hand-held console and the console debug option) can be avoided by programming all ones in the conflicting locations in one of the memories.

OVERVIEW AND INTRODUCTION

Certain programs and data contained in a computer system are never changed, but are used frequently enough to justify their being permanently located within the address space of the CPU. Read-only memory (ROM) provides a medium on which such information can be stored. The contents of a ROM location cannot be changed under program control while the ROM is in the address space of the CPU. However, since the contents of ROM cannot be changed, the information contained in ROM is protected from software and hardware malfunctions.

Some ROM is programmable; that is, the contents of the ROM are initially all zeros or all ones, and the appropriate ones or zeros can be "programmed" or "burned" into the ROM after the memory is purchased. Such programmable ROM is called PROM.

The microNOVA programmable read-only memory boards contain sockets for 512 to 4096 16-bit words of PROM available in 256 by 4 bit or 512 by 4 bit packages. The contents of the memory on a microNOVA PROM board can be programmed, one word at a time, using the microNOVA PROM programmer board.

SUMMARY OF CHARACTERISTICS

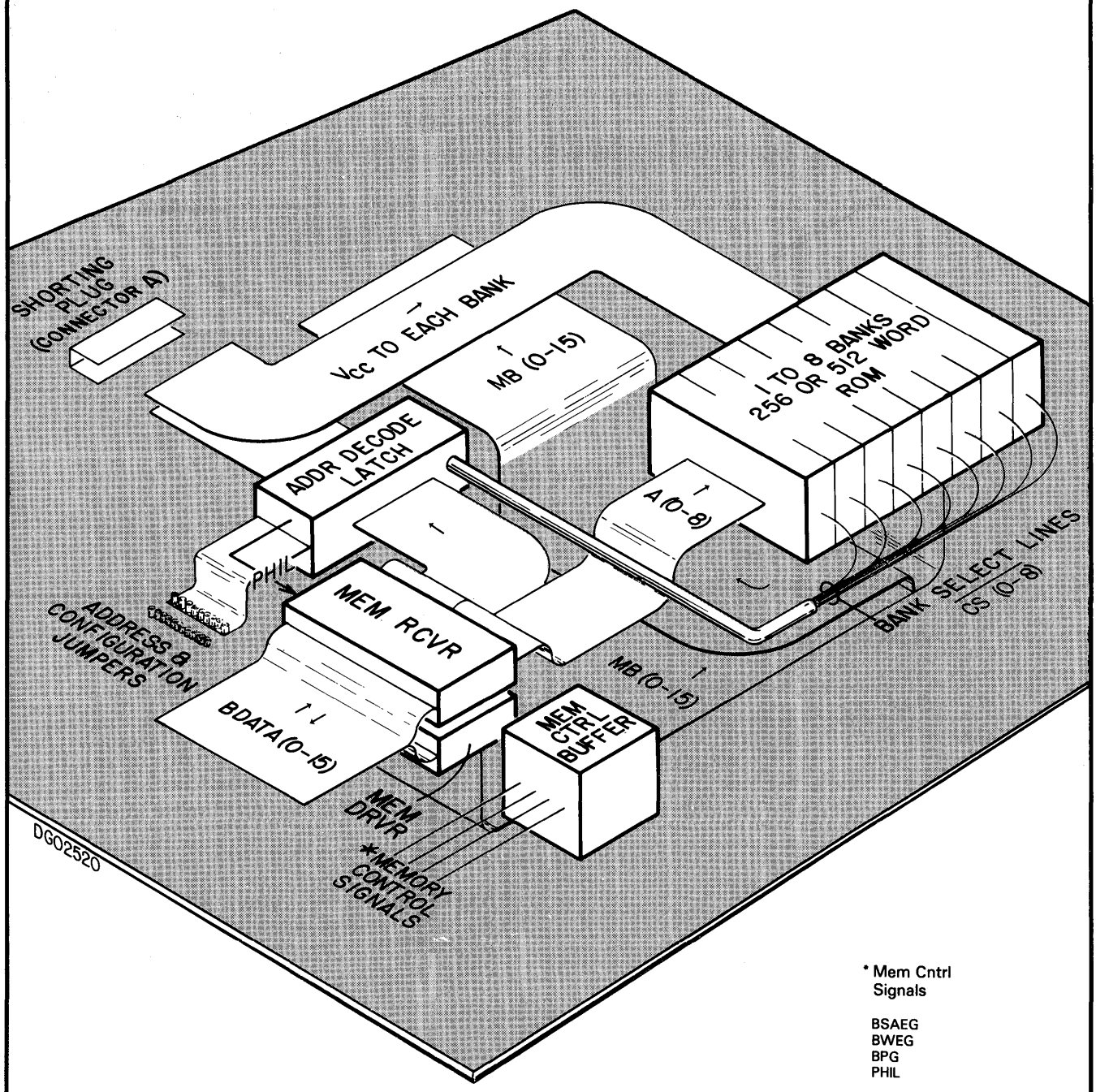
PROM Type	Signetics 82S126, 82S130, or equivalent.
Board Capacity	512; 1,024; 2,048; or 4,096 16-bit words.
Cycle Time	960ns.
Board Dimensions	7.5 x 9.9 in. (19 x 24.9cm.)
Maximum Operating Temperature	131°F (55°C)

BLOCK DIAGRAM

The block diagram on the opposite page shows the principal components plus the control and data paths of microNOVA ROM boards. The board contains a memory bus address receiver and latch, from 1 to 8 banks of PROM, each with 256 or 512 16-bit words, a memory driver, and a memory control buffer. For normal PROM operation, there is also a shorting block located on connector "A".

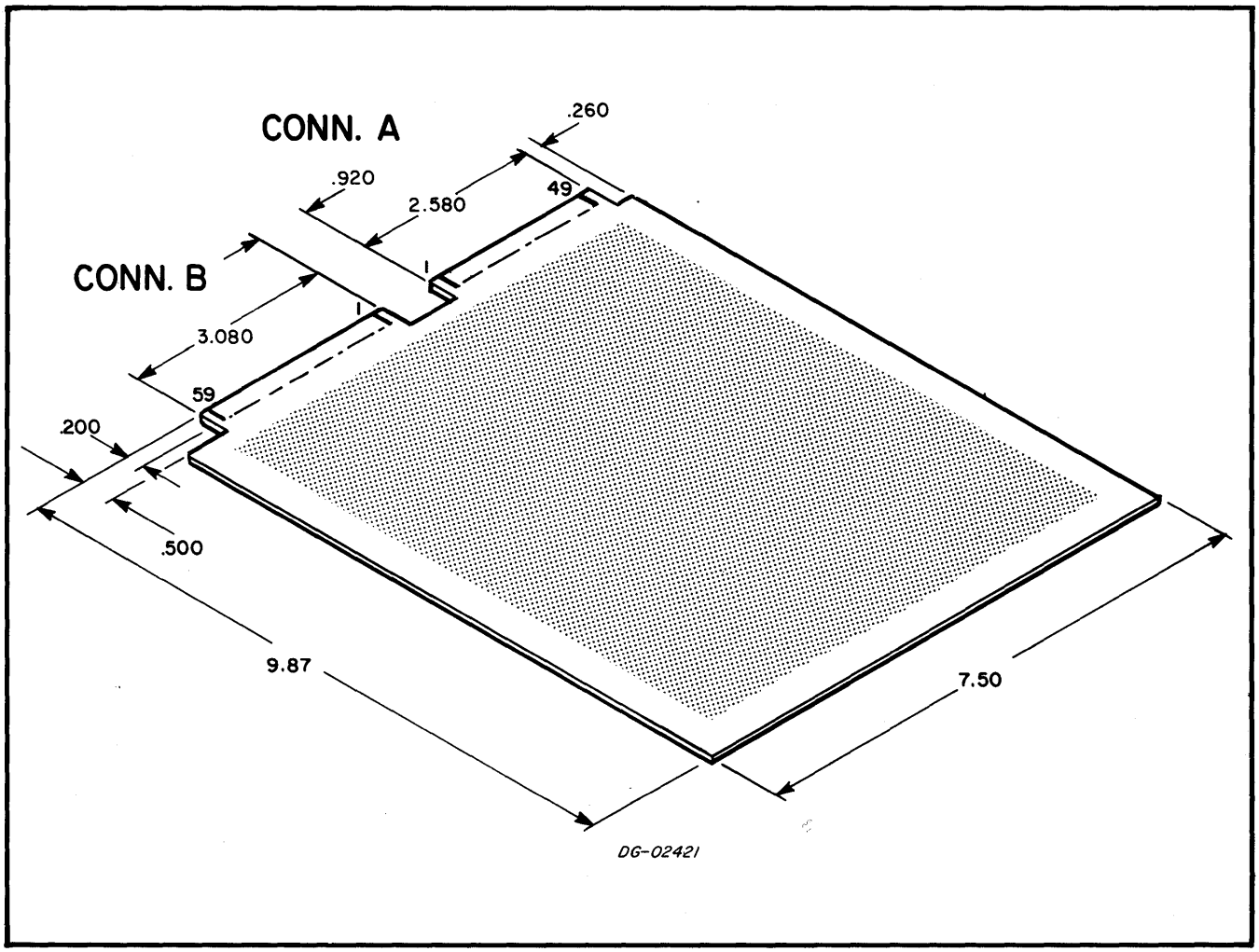
When an address appears on the memory bus at the start of a Read operation, the address latches in the address receiver if the address lies within the range established by the starting address and memory size jumpers. The high-order 6 bits select one of the eight banks by applying power (V_{CC}) through the shorting block to that bank, while the low-order 8 bits of the address pass directly to all PROM banks. (To reduce dc power dissipation, the PROM banks remain unpowered when not being read). The addressed word is driven onto the memory bus while the memory control buffer asserts the signal **PHIL** to disable any RAM in the system from placing data on the bus.

The PROM board is designed so that PROMS can be programmed on the board using the microNOVA PROM programmer. (The programmer plugs directly into the microNOVA chassis, and the PROM board plugs directly into the programmer.) Two groups of signals, the bank select signals and taps from the data out lines of the PROM banks, are carried to connector "A" because they are used by the microNOVA PROM programmer when "burning" PROMS. For the PROM board's normal use, a shorting plug must be installed on the "A" connector to close the internal paths carried to that connector.



* Mem Cntrl Signals

BSAEG
BWEG
BPG
PHIL



PROM SIZE JUMPERS

SIZE OF PROM CHIPS	INSERT JUMPERS
256 x 4 bits	W1, W3, W6
512 x 4 bits	W2, W4, W5, W7

ADDRESS SELECTION JUMPERS

BIT POSITIONS OF STARTING ADDRESS	1	2	3	4*
INSERT JUMPER TO SPECIFY 1	W13	W15	W11	W9
INSERT JUMPER TO SPECIFY 0	W12	W14	W10	W8

*Jumpers W8 and W9 are ignored on the 4K PROM board.

NOTE *All of the address selecton jumpers must be removed when the board is being programmed with the microNOVA PROM programmer.*

SECTION V
HAND-HELD CONSOLE SUBSYSTEM

Data General's model 8564 hand-held console is a portable device that mounts on the chassis front panel and is connected by a 10' ribbon cable to its IOC-based controller, which occupies a single slot in the main chassis. Data is retrieved from the 20-key pad via programmed I/O on an interrupt-per-key basis. The contents of memory location 077576_8 are constantly displayed as 6 octal digits via the 7-segment LED display. The standard console software, supplied in 256 16-bit word of ROM/RAM on the controller board, provides reset, program load, start/stop/continue, and octal examination and modification of memory and CPU registers. With suitable software, the actions of all keys may be redefined by the user.

OVERVIEW AND INTRODUCTION

Computer consoles usually are hard-wired extensions of the central processor used to monitor system performance and to aid in fault finding when the system malfunctions. For large computer systems, the processor console is the province of the field serviceman. With the advent of minicomputers, the processor console has also been used by programmers both as an aid in debugging programs and as an I/O device. As an I/O device, the minicomputer processor console is sometimes used to enter information into the system and to display the status of an application program.

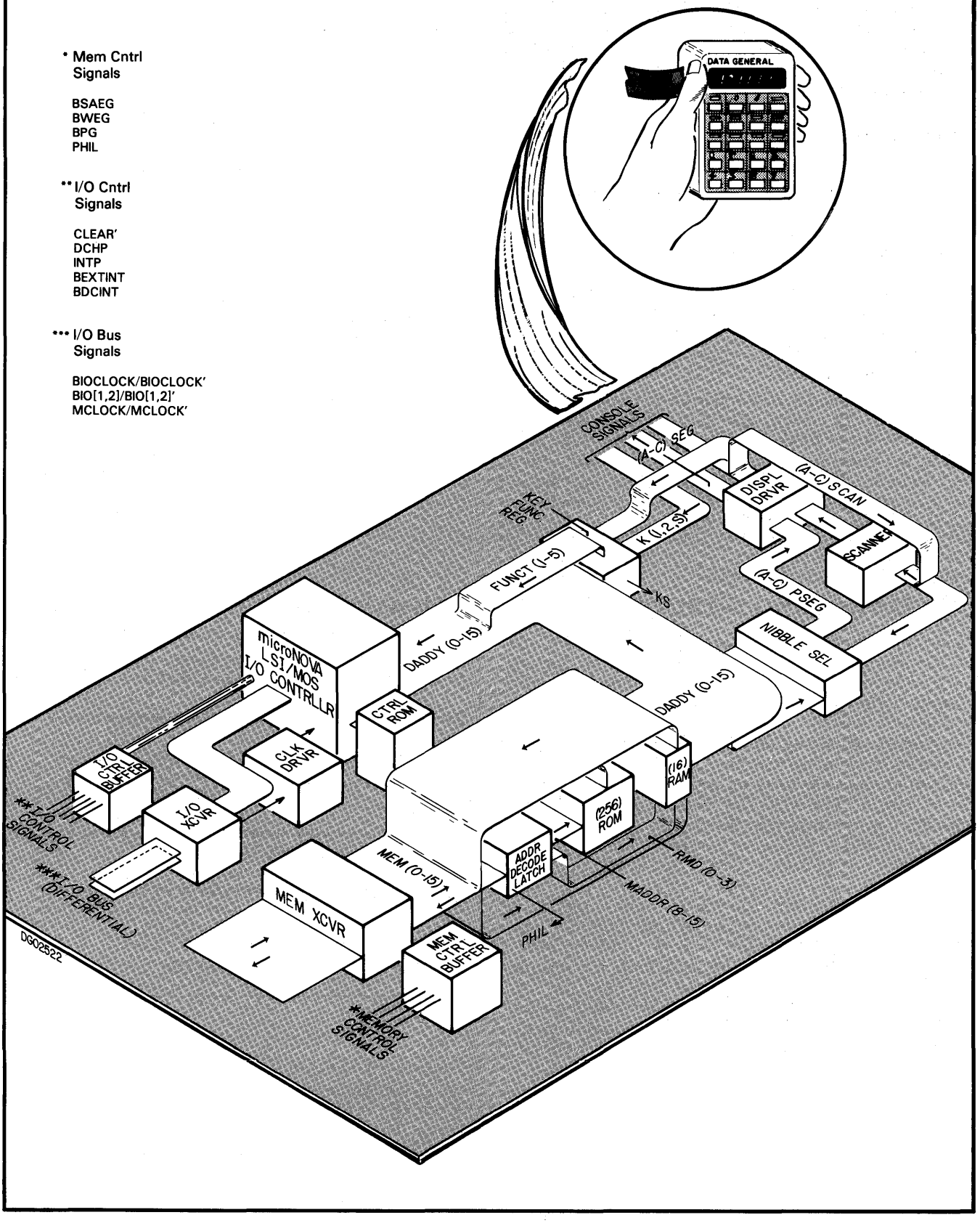
The microNOVA hand-held console, when used with the standard console software, provides all the functions normally found on a minicomputer processor console and can be used both for trouble shooting and program debugging. The fact that the hand-held console is fully user-programmable means that it is extremely versatile and may be used in many application environments as a key-entry/visual-response I/O device.

The hand-held console subsystem consists of a lightweight, portable console which contains a 20-key pad and a digital readout which displays the contents of one 16-bit word of memory as 6 octal digits. The console controller is designed around the mN603 IOC circuit and occupies one slot in the main computer chassis. The controller contains the standard console software in 256 16-bit words of ROM/RAM.

SUMMARY OF CHARACTERISTICS

Key Pad:	20-key, calculator format. Keys are 0.425in(w) by 0.250in(h) on centers of 0.625in.
Display:	6-digit, 7-segment LED. Each digit is 0.3in(h).
Interface Requirements:	IOC-based controller occupies 1 slot in main chassis. Controller connects to console via 16-conductor 10' ribbon cable.
Packaging:	Injected molded, 2-piece case with living hinge key pad as part of top.
Mounting:	Attaches to depression in front panel with Dzus fastener. Cable is held on rewinder behind front panel.
Dimensions:	4.85in(h), 3.30in(w), 1.2(d).

microNOVA HAND-HELD CONSOLE SUBSYSTEM



BLOCK DIAGRAM

The block diagram on the opposite page shows the principal components plus the data and control paths of the microNOVA hand-held console (HHC) subsystem. The subsystem functions as three distinct units: the I/O interface, HHC memory, and the display and keyboard unit and controller.

I/O Interface

The I/O Interface comprises the IOC and its support circuits, a 5-bit key function register, and a 16-bit data path whereby the contents of a selected RAM location in the memory section can be transferred in bit-parallel fashion to the IOC.

The IOC and its clock driver, the I/O bus transceiver and the I/O control buffer interface the HHC subsystem to the I/O bus of a microNOVA CPU. The protocols by which the CPU communicates with peripherals is detailed in the technical reference cited above.

The control ROM contains control codes that translate IOC function codes into command signals that initiate transfer operations in all sections of the HHC subsystem. It initiates a control sequence whereby the memory section places a single word from RAM on the 16-bit input path to the IOC, and it initiates a program interrupt request when the keyboard controller places the function code resulting from a keystrike into the key function register. It also places the contents of the key function register on the input lines of the IOC when a Read Function command is received from the I/O bus.

HHC Memory

The memory section of the HHC subsystems consists of a 256 16-bit word memory module containing ROM overlaid with sixteen 16-bit words of RAM. The section includes memory, an address decoder and latch, and a memory transceiver and control buffer.

The memory transceiver and control buffer interface the memory section of the HHC subsystem to the memory bus of a microNOVA CPU. The protocols by which the CPU communicates with memory are detailed in the technical reference cited above. The starting address of the memory section is 077400_8; any RAM elsewhere in the microNOVA system assigned to addresses 077400_8 - 077777_8 is overridden by the HHC memory section and will not return any data in Read or Read-Modify-Write operations.

When a memory address appears on the bus at the beginning of a memory operation, the address decoder latches the 8 low-order bits of that address if it exceeds 077377_8. If the operation is a memory read, the latched address is presented to the ROM module and driven onto the module's data out lines through the memory transceiver and onto the memory bus. When the 8 bits latched lie in the range 160_8 - 177_8, the 16 word RAM is also enabled. The low-order 4 bits from the address latch select a word from RAM, and it is driven onto the module out lines at the same time as the word retrieved from ROM.

> **NOTE** *Those sixteen words in the HHC ROM having the same addresses as the RAM overlay are programmed to return all 1's when read. The module is arranged so that the word returned to the processor when both RAM and ROM are read at the same time is the logical AND of the two retrieved words.*

As the 16-bit data word is driven onto the memory bus, the HHC asserts the signal **PHIL** which disables any RAM in the system having the same addresses as those used by the HHC. If the memory operation is a Write operation, the operation takes place normally only if the address lies within the 16 word overlay; otherwise the operation is ignored. Because the 16 word overlay is built from bipolar memory, the Refresh operation is ignored.

Display and Keyboard

The display and keyboard section includes the display and keyboard in the hand-held console, a display register, and a key function register. The display and keyboard section also contains a controller with multiplexors and scanners that drives and refreshes the display and detects and decodes each keystrike at the keyboard.

Display and Control

The console digital display is a 6 digit 7-segment optoelectric readout, driven one digit at a time by an octal to seven-segment decoder; a 6-step scanner in the subsystem sequentially selects a 3-bit nibble from the word to be displayed, and simultaneously enables the appropriate readout cell in the display for that nibble.

The display control repetitively displays the contents of memory location 77576_8. It frequently retrieves that word from HHC memory independently of the CPU

when the memory is not performing a memory operation with the CPU. In synchronism with an internal clock the control initiates a sequence wherein memory places the contents of location 775767_8 on its memory's data out lines and into the nibble selector.

As the scanner steps through each digit, the scan number as well as the octal nibble for that scan latch into the display line driver. The HHC decodes the scan number and enables one readout cell, while it decodes the octal nibble and lights appropriate segments in that cell.

Keyboard and Control

The keyboard is a 4 column by 5 row switch matrix with its row lines driven by the display scanner; 4 column lines are encoded to a 2-bit function code and presented with a strobe signal to the key control. The key control debounces the strobe signal and latches the value of the scan number and the column code into the key function register. The key control then initiates a program interrupt request. The key control latches the value of the 5 function lines each time a key strobe is detected.

PROGRAMMING

The microNOVA hand-held console is a light-weight, portable, key-entry/visual-response data terminal. The console subsystem, which consists of a controller and the console itself, makes the function code of each key struck available to any applications program and also allows the console display to be easily updated. The standard console software uses these capabilities to provide a mechanism for controlling and monitoring the actions of a microNOVA computer system.

There are two well-defined entry points in the standard console software. Location 077777_8 contains the address which should receive control upon system initialization and auto-restart. Location 077776_8 contains the address which should receive control when a console key has been struck.

When using the standard console software from a system interrupt handler, restore the accumulators and the carry bit before transferring control. The console software assumes that the accumulators and the carry bit that it receives are those of the interrupted program.

The standard console software maintains a console switches register in its local RAM. Retrieve this information either by issuing an instruction to the hand-held console or by reading memory location 077577_8.

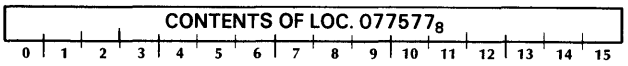
To use the hand-held console as a key-entry/visual-response terminal, read the function code when an interrupt comes from the console and perform whatever function you want to associate with that code. To alter the 6 digits in the display, store the desired value in location 077576_8. Alternatively, location 077576_8 can be changed via the data channel from a special-purpose I/O device of your own making.

PROGRAMMING SUMMARY

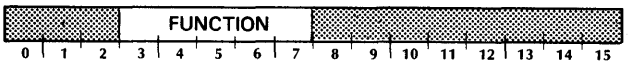
Mnemonic	HHC
Device Code	4
Priority Mask Bit	5
Display Word Location	077576_8
Console Switches Location	077577_8
Auto-restart Location	077777_8
Normal Interrupt Location	077776_8

ACCUMULATOR FORMATS

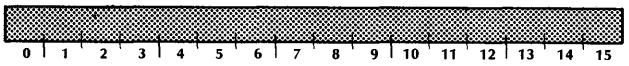
Read Switches **(DIA)**



Read Function **(DIC)**



Light Decimal Point **(DOC)**



The device flag commands control the hand-held console controller's Busy and Done flags in the following manner:

f=S Set the Busy flag to 1 and the Done flag to 0.

f=C Set the Busy flag to 0 and the Done flag to 0.

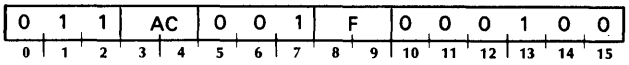
f=P Set the Done flag to 0.

Instructions

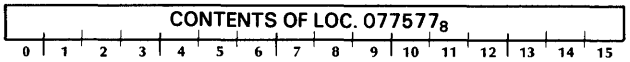
Read Switches

READS *ac*

DIA *[f]* *ac*, **HHC**



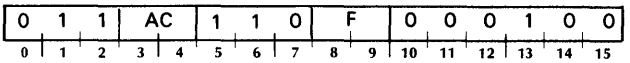
The current value of the console switches register is retrieved from memory location 077577_8 and placed in the specified AC. After the transfer, the function specified by F is performed. The format of the specified AC is as follows:



Bits	Name	Contents
0-15	Switches	Contents of memory location 077577_8.

Light Decimal Point

DOC *[f]* *ac*, **HHC**

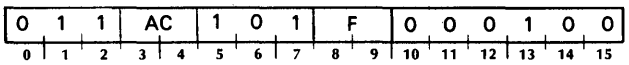


The decimal point to the right of the left-hand digit on the console is lit. The contents of the specified AC are ignored and remain unchanged. After the transfer, the function specified by F is performed.

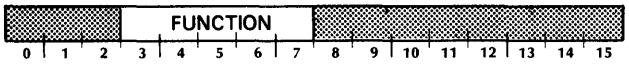
NOTE *In order to keep the decimal point visible, this instruction must be issued at least once every 16 milliseconds.*

Read Function

DIC *[f]* *ac*, **HHC**

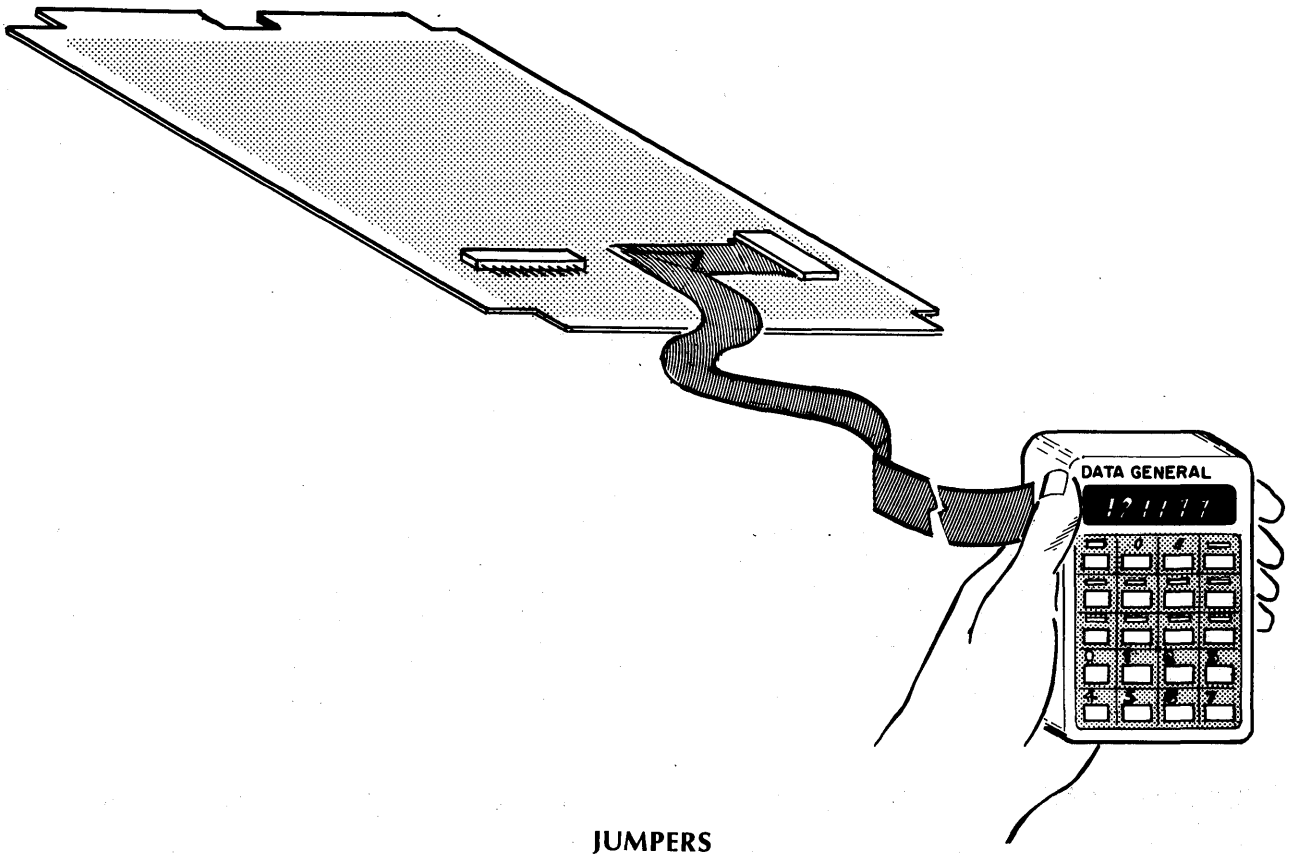


The function code of the most recently struck console key is placed in bits 3-7 of the specified AC. Bits 0-2 are set to 0. Bits 8-15 are unpredictable. After the transfer, the function specified by F is peformed. The format of the specified AC is as follows:



Bits	Name	Contents
0-2	----	Reserved for future use.
3-7	Function	Function code of the most recently struck console key.
	00 000	0/AC0
	00 001	1/AC1
	00 010	2/AC2
	00 011	3/AC3
	00 100	4/FP
	00 101	5/SP
	00 110	6/SWITCHES
	00 111	7/ADDR
	01 000	LAST
	01 001	NEXT
	01 010	MEM
	01 011	CLR D
	01 100	START
	01 101	STOP
	01 110	CONT
	01 111	DEP
	10 000	RESET
	10 001	*
	10 010	/
	10 011	PR LOAD
8-15	----	Reserved for future use.

microNOVA HANDHELD PROGRAMMER'S CONSOLE



JUMPERS

JUMPER	FUNCTION
W1	Insert jumper to enable hand-held console subsystem memory.

SECTION VI
ASYNCHRONOUS INTERFACE BOARD

Data General's model 4207 asynchronous interface board is an IOC- and UAR/T-based, interrupt driven, programmed I/O controller that provides the capability for full-duplex communication between a microNOVA computer system and an asynchronous terminal over either 20mA current loop or EIA RS232-C lines at speeds ranging from 50 to 19,200 baud with a character format of 1 start bit; 5, 6, 7, or 8 data bits; even, odd, or no parity; and 1, 1.5, or 2 stop bits. The choice of line type, line speed, number of data bits, type of parity, and number of stop bits are all jumper-selectable. The controller has a modem control capability including auto-answer. The model 4208 console debug option is an octal debugger contained in 256 16-bit words of ROM/RAM which are on the controller board.

OVERVIEW AND INTRODUCTION

In order to perform useful work, a computer system needs some way to communicate with the outside world. By the same token, in order to communciate with the computer system, the user needs some convenient method to give both data and commands to the system. With the advent of low-cost, asynchronous terminals, both these needs have been met by a single device. An asynchronous terminal may be used as a system console device to control the actions of the system or to interact with the user via an applications program. Using multiple terminals, one system, with suitable software, can service many users at the same time.

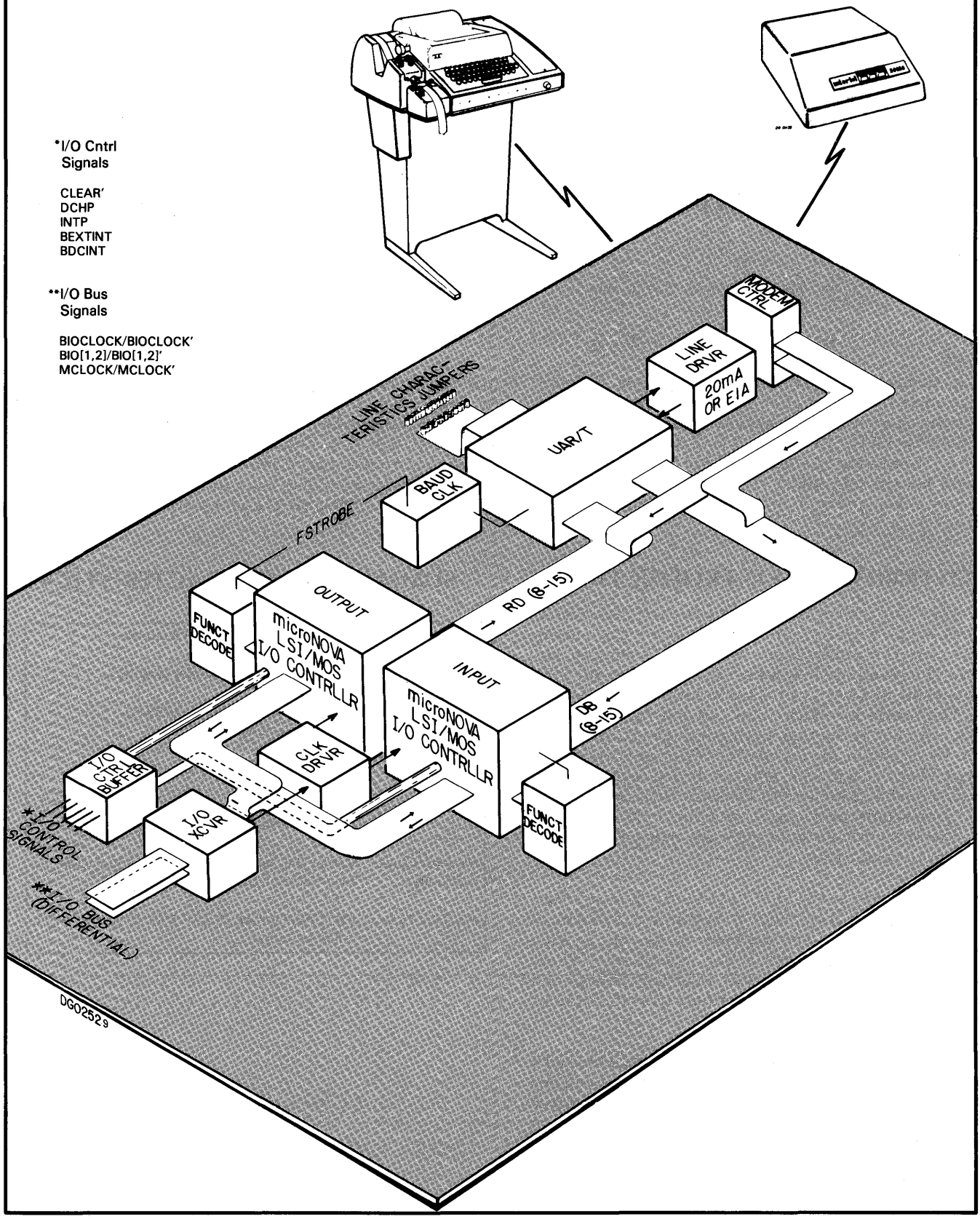
Data General's model 4207 asynchronous interface board allows a microNOVA computer system to communicate with the outside word via a wide assortment of asynchronous terminals. These terminals may range from teletypewriters and teletypewriter-compatible terminals to asynchronous serial printers to video displays.

The model 4208 console debug option available with the asynchronous interface board is an octal debugger with full memory and CPU register examination/modification capability and a software breakpoint facility. This option allows the terminal connected to the asynchronous controller to be not only a system console, but also to be a debugging and program development tool.

SUMMARY OF CHARACTERISTICS

Comm. type:	Asynchronous, bit serial full-duplex.
Line Speed:	50 to 19,200 baud, jumper-selectable.
Line Type:	20ma current loop or EIA-RS232C, jumper-selectable.
Data Structure:	1 start bit; 5, 6, 7, or 8 data bits, jumper-selectable; even, odd, or no parity, jumper-selectable; 1, 1.5, or 2 stop bits, jumper-selectable.
Modem Signals Available:	Carrier On, Data Set Ready, Data Terminal Ready, Ring Indicator, Break Indicator
Interface Type:	IOC/UAR/T-based: 1 UAR/T plus 1 IOC for input, 1 IOC for output.

microNOVA ASYNCHRONOUS INTERFACE BOARD WITHOUT CONSOLE DEBUG OPTION



BLOCK DIAGRAM

The block diagram on the opposite page shows the principal components and the data and control paths in the asynchronous serial interface without the console debug option. The drawing on the next page shows the same block diagram with the console debug option installed. The console debug option and the serial interface sections of the board function independently of each other.

Asynchronous, Serial Interface

To allow full-duplex operation, the interface responds to two I/O device codes, one for input data and one for output data. The circuit includes input and output IOC's with a clock driver and function decoders, a UAR/T, a baud rate clock derived from the computer system clock, a line driver/receiver for a 20mA current loop or EIA RS232-C transmission line, and modem control including automatic answer capability.

The IOC's interface the UAR/T to the I/O bus according to the protocols by which the CPU communicates with peripherals. These protocols are described in detail in the Technical Reference for microNOVA Integrated Circuits *(DGC no. 014-000074)*.

The UAR/T accepts 5,6,7 or 8-bit wide data bytes from the output IOC via the write bus, and serializes the data, adding start, parity, and stop bits as selected by line characteristics jumpers. The resulting bit serial data stream is passed to an external data terminal, communication modem or other device from the output connector ("A" connector) via 20mA current loop or EIA RS232-C line drivers.

Asynchronous serial input data enters via the "A" connector, and passes via the 20mA current loop or EIA line receiver to the UAR/T. The UAR/T strips format bits from the data stream and presents an 8-bit parallel data byte to the input IOC via the read bus.

Console Debug Option

The console debug option to the asynchronous serial interface board consists of a 256 16-bit word memory module comprising ROM overlaid with sixteen 16-bit words of RAM. The option includes memory, an address decoder and latch and the memory transceiver and control buffer that connects the memory module to the microNOVA memory bus.

The memory transceiver and control buffer interface the memory section of the console debug option to the memory bus of a microNOVA CPU. The protocols by which the CPU communicates with memory are detailed in the technical reference cited above.

The starting address of the 256-word address area is 077400_8. Any RAM in the system assigned to the same memory addresses as the console debug option is overridden by the console debug option memory, and will not return any data during Read and Read-Modify-Write memory operations.

When a memory address appears on the bus at the beginning of a memory operation, the address decoder latches the 8 low-order bits of that address if it exceeds 077377_8.

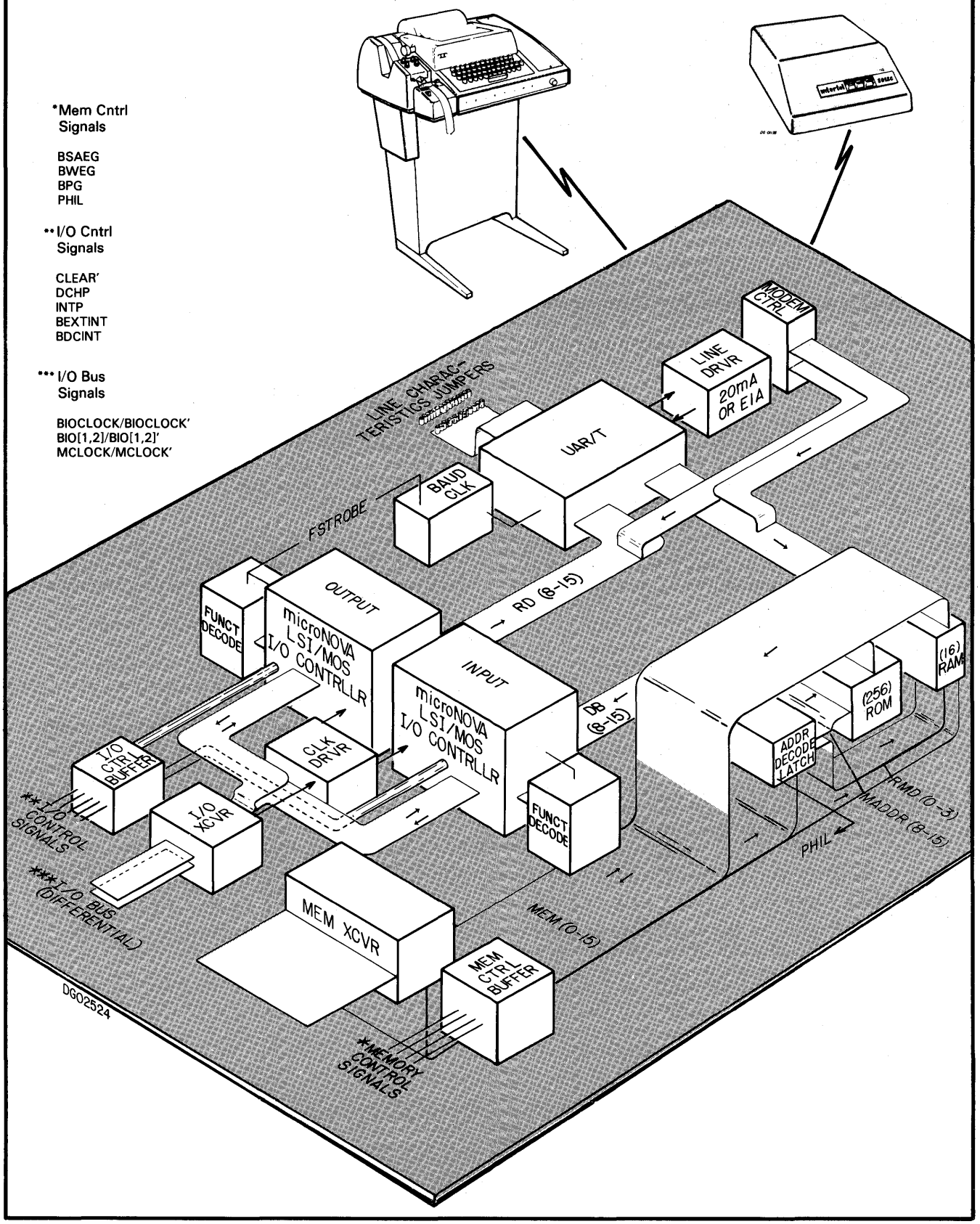
If the operation is a memory read, the latched address is presented to the ROM module and driven onto the module's data out lines through the memory transceiver and onto the memory bus. When the 8 bits latched lie in the range 160_8 - 177_8, the 16 word RAM is also enabled. The low order 4 bits from the address latch select a word from RAM, and it is driven onto the module out lines at the same time as the word retrieved from ROM.

> **NOTE** *Those sixteen words in the console debug option ROM having the same addresses as the RAM overlay are programmed to return all 1's when read. The module is arranged so that the word returned to the processor when both RAM and ROM are read at the same time is the logical AND of the two retrieved words.*

As the 16-bit data word is driven onto the memory bus, the console debug option asserts the signal **PHIL** to disable any RAM located in the system and assigned the same addresses as those used by the console debug option.

If the memory operation is a Write operation, the operation takes place normally only if the address lies within the 16 word overlay; otherwise the operation is ignored. Because the 16 word overlay is built from bipolar memory, the Refresh operation is ignored.

microNOVA ASYNCHRONOUS INTERFACE BOARD WITH CONSOLE DEBUG OPTION



PROGRAMMING

The microNOVA asynchronous interface board allows communication between a microNOVA computer system and a serial asynchronous terminal. When equipped with the console debug option, the asynchronous interface board gives the capability for an asynchronous terminal to be not only the system console but also a debugging and program development tool. To this end, the controller takes care of character assembly and disassembly, parity generation and checking, and character buffering. The controller allows characters to be received from and transmitted to the terminal, and provides program control of various modem status and control signals.

To transmit a character, load the character into the transmiter buffer, and direct the controller to transmit it by giving a Start command. The controller waits until the modem signal Clear To Send is asserted; adds the required start, parity, and stop bits; and then transmits the character serially to the terminal. After the transmission is complete, the controller initiates an I/O interrupt request.

Reception of a character requires no initiating action. The controller detects a character being transmitted from the terminal; assembles it; strips the start and stop bits; and then initiates an I/O interrupt request. Read the character before one full character time has elapsed to avoid the character being over written by the next character on the line. To read a character from a teletypewriter paper tape reader, give a Start command to initiate the transfer of the next character.

To answer calls from a modem that is configured for auto-answer, periodically read the modem status register and check for the presence of the Ring Indicator. If the Ring Indicator is a 1, assert the signal Data Terminal Ready. This will complete the connection and allow communication to begin.

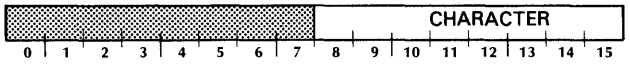
The console debug option is a stand-alone program contained in 256 16-bit words of ROM/RAM on the controller board. The console debug option cannot be programmed.

PROGRAMMING SUMMARY

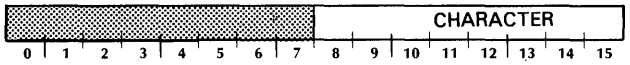
Primary Mnemonic	
Transmitter	TTI
Receiver	TTO
Primary Device Code	
Transmitter	10
Reciever	11
Secondary Mnemonic	
Transmitter	TTI1
Reciever	TTO1
Secondary Device Code	
Transmitter	50
Receiver	51
Priority Mask Bit	
Transmitter	14
Receiver	15

ACCUMULATOR FORMATS

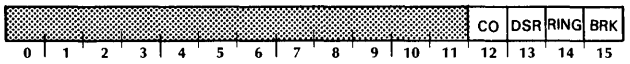
Read Character **(DIA to TTI)**



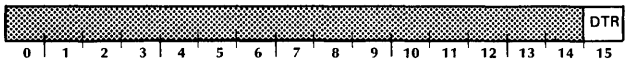
Write Character **(DOA to TTO)**



Read Modem Status **(DIB to TTI)**



Control Data Terminal Ready **(DOB to TTO)**



The device flag commands control the receiver's Busy and Done flags in the following manner:

f=S Set the Busy flag to 1 and the Done flag to 0.

f=C Set the Busy flag to 0 and the Done flag to 0.

f=P Set the Done flag to 0, and set the Break Indicator in the modem status register to 0.

The device flag commands control the transmitter's Busy and Done flags in the following manner:

f=S Set the Busy flag to 1 and the Done flag to 0. Turn on Request to Send and begin transmitting the contents of the transmit buffer as soon as Clear to Send is received from the modem.

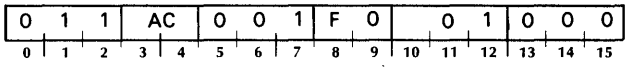
f=C Set the Busy flag to 0 and the Done flag to 0. Turn off the transmitter and Request to Send.

f=P Set the Done flag to 0.

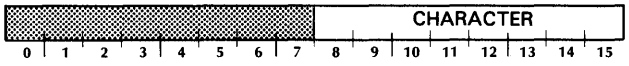
Instructions

Read Character

DIA *[f]* *ac*, TTI



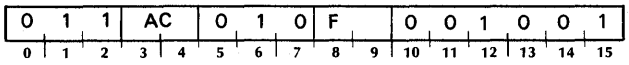
The contents of the receiver buffer are placed in bits 8-15 of the specified accumulator. If the character has less than 8 data bits, it is placed right-justified in bits 8-15. Bits 0-7 are set to 0. After the transfer, the function specified by F is performed. The format of the specified AC is as follows:



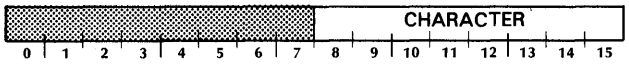
Bits	Name	Contents
0-7	----	Reserved for future use.
8-15	Character	The character most recently received (right-justified).

Write Character

DOA *[f]* *ac*, TTO



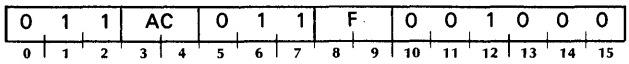
Bits 8-15 of the specified accumulator are placed in the transmitter buffer. If the character has less than 8 data bits, it should be placed right-justified in bits 8-15. Bits 0-7 of the AC are ignored. After the transfer, the function specified by F is performed. The contents of the specified AC remain unchanged. The format of the specified AC is as follows:



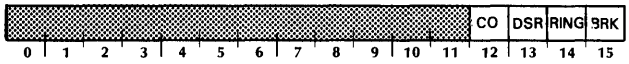
Bits	Name	Contents
0-7	----	Reserved for future use.
8-15	Character	The character to be transmitted (right-justified).

Read Modem Status

DIB *[f]* *ac*, TTI



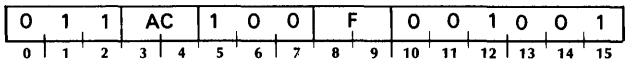
The contents of the modem status register are placed in bits 12-15 of the specified accumulator. Bits 0-11 of the AC are set to 0. After the transfer, the function specified by F is performed. The format of the specified AC is as follows.



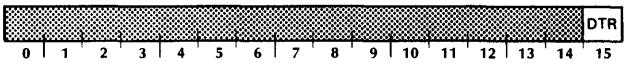
Bits	Name	Contents
0-11	----	Reserved for future use.
12	Carrier On	The state of the Carrier On signal (0=off, 1=on).
13	Dataset Ready	The state of the Dataset Ready signal (0=off, 1=on).
14	Ring Indicator	The state of the Ring Indicator signal (0=off, 1=on).
15	Break Indicator	If the bit is 1, a break condition (line open and spacing) has been detected by the receiver.

Control Data Terminal Ready

DOB *[f]* *ac*, TTO

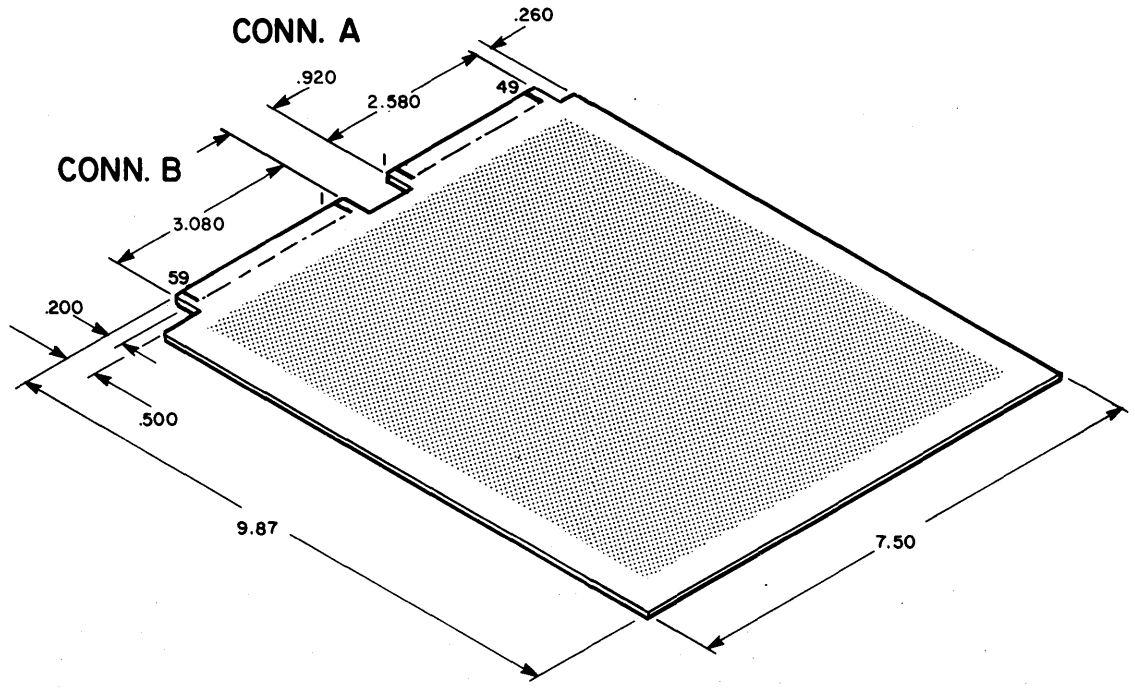


Bit 15 of the specified accumulator is used to set the Data Terminal Ready signal. If bit 15 is 1, the Data Terminal Ready signal is turned on. If bit 15 is 0, the Data Terminal Ready signal is turned off. Bits 0-14 of the AC are ignored. After the state of the signal has been set, the function specified by F is performed. The contents of the specified AC remain unchanged. The format of the specified AC is as follows:



Bits	Name	Contents
0-14	----	Reserved for future use.
15	Data Terminal Ready	The state of the Data Terminal Ready signal (0=off, 1=on).

ASYNCRONOUS INTERFACE BOARD DIMENSIONS



DEVICE CODE JUMPERS

BIT POSITIONS OF DEVICE CODE (Insert jumper to specify 1)	0	1	2	3	4	5
RECEIVER	W1	W2	W3	W4	W5	0*
TRANSMITTER	W6	W7	W8	W9	W10	1*

*The low-order bit of the device code of the receiver is 0, and the low-order bit of the device code of the transmitter is 1.

BAUD RATE JUMPERS

BAUD RATE	W11	W12	W13	W14
50	in	in	out	in
75	in	in	out	out
110	out	out	out	out
134.5	in	out	in	in
150	out	out	out	in
200	in	out	in	out
300	out	out	in	out
600	in	out	out	in
1200	out	in	out	out
1800	out	in	out	in
2400	out	out	in	in
4800	out	in	in	out
9600	out	in	in	in
19,200	in	in	in	out

TYPE OF TRANSMISSION JUMPERS

TYPE OF TRANSMISSION	INSERT JUMPERS
20mA Current Loop	W20, W22, W23, W25
EIA RS232-C	W21, W24

CHARACTER LENGTH JUMPERS

LENGTH OF CHARACTER	W18	W19
5 bits	in	in
6 bits	out	in
7 bits	in	out
8 bits	out	out

PARITY JUMPERS

TYPE OF PARITY	W17	W15
EVEN	out	in
ODD	in	in
NONE	out	out

STOP BIT JUMPERS

NUMBER OF STOP BITS	W16
1	in
2	out

OTHER JUMPERS

JUMPER	FUNCTION
W26	Insert jumper to enable the console debug option memory.
W27	Insert jumper to disable the use of the modem status signal Clear To Send.

SECTION VII
DISKETTE SUBSYSTEM

Data General's model 6038 and model 6039 diskette subsystems are self-contained, IOC-based, mass storage, software-driven subsystems providing direct access, moving head disc memory for microNOVA computers. Subsystems store 157,696 16-bit computer words in single block (256 word) transfers at 15,625wps to hard/soft format diskettes that are fully compatible with DGC's 6030 series subsystems (for NOVA and ECLIPSE line computers). Multiple 2-drive subsystems may connect on the microNOVA's extended I/O bus (max. 100 ft bus). Software support includes a disc operating system subset of Data General RDOS.

OVERVIEW AND INTRODUCTION

Mass storage provides the capability of maintaining very large amounts of machine readable data at a fraction of the cost of main, or random access memory. Diskette subsystems provide mass storage on compact, inexpensive, easily handled, direct access media. They offer faster data access and higher transcription speed than sequential media (e.g. paper and magnetic tape and cards). They are useful for online system applications not requiring the capacity and speed of higher performance direct access systems. The direct access diskette subsystem can support a powerful operating system; this can lead to an appreciable reduction in application program development time.

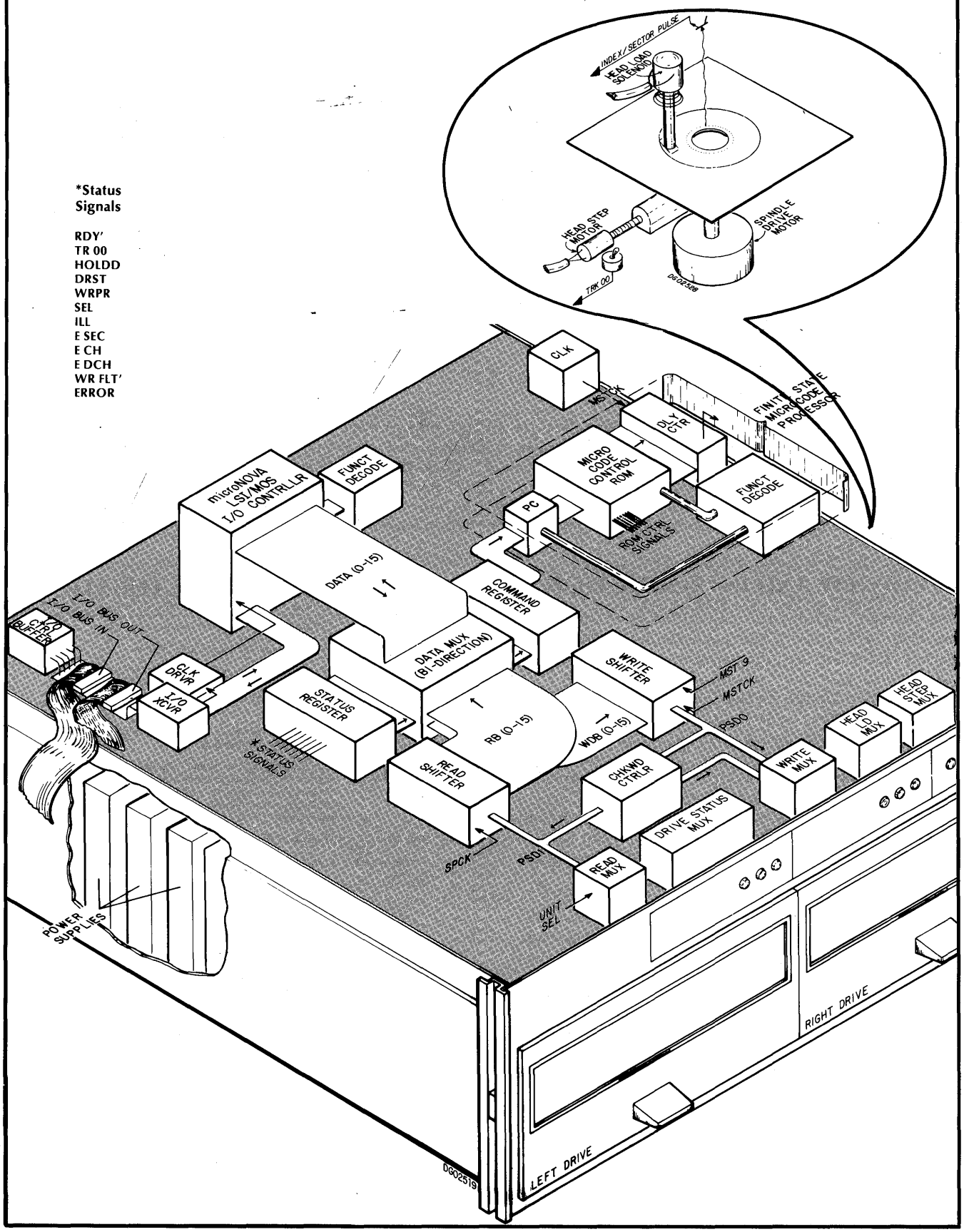
Data General's microNOVA series diskette subsystems provide powerful reliable, data storage capability for microNOVA computers. They are available in single and dual drive units.

These diskette subsystems combine a drive mechanism, power supply an packaging scheme proven in Data General's 6030 series diskette subsystems. They include a synchronous interface designed around the microNOVA system IOC.

SUMMARY OF CHARACTERISTICS

Max. Storage:	157,696 16-bit words per diskette.
Transfer Rate:	15,625 words/second via data channel.
Data Format:	77 tracks, 8 sectors each with 256 16-bit words plus address and check fields Hard sector marks prepunched in media Soft sector format prewritten to media.
Packaging:	Single or Dual Drive enclosure, either drive may be assigned unit number 0.
Interface Requirements:	Couples directly to extended I/O bus of microNOVA system and requires no space in the computer chassis. Four enclosures each with 2 drives may be cabled on bus with maximum total bus length 100 feet or less.
Seek Time:	10ms each, step in or step out 1 track.
Sector Access:	166ms (max) 1.2ms (min) ±3.5% (360rpm).
Head Load/Settle Time:	60ms, minimum (automatic head load implied on all head positioning commands); 10ms, after last step in or out command; 170ms, after changing unit selection.
Default Head Unload Time:	320ms (nominal) after last operation; immediately, upon unit deselection.
Diskette Type:	Industry standard 7.88in dia. 3mil mylar media with Data General specified punched sector and write protect holes.
Write Compensation:	Two level write current compensation for head to disc speed and effective data density variation with track position.
Head Type:	Single gap, ceramic.
Data Density:	3268bpi (inner track)/1836bpi (outer).
Power Required:	100/115/220/240Vac (±10%) 50/60Hz.
MTBF/MTTR:	4000 hours operating (after initial 200hrs)/20 minutes.
Dimensions:	19in(w), 7in(h), 24in(d) slide rail mounting in 19in NEMA cabinet.
Weight:	54lbs (single drive), 67lbs (dual).

microNOVA DISKETTE SUBSYSTEM



BLOCK DIAGRAM

The subsystem block diagram shows the principal elements in the diskette subsystem. All information transfers between the diskette subsystem and CPU occur via the extended microNOVA I/O bus. (The microNOVA serial I/O bus is described in the CPU section of this publication; its functional protocols are detailed in the Technical Reference for microNOVA Integrated Circuits *(DGC no. 014-000074)*.

Subsystem Interface and Controller

The I/O bus transceiver, the IOC, and a function decoder perform level translation, format conversion and control syncrhonization between the high speed, differential, serial, I/O bus and the internal control and data registers in the diskette subsystem.

The diskette command register decodes the operation specified by the program and initializes the micro-coded timing and state generator. The state generator is a ROM-controlled microcode processor that steps the diskette subsystem in an ordered sequence through all operations in synchronism with a crystal-controlled master clock. The ROM microcode enables the required paths through the multiplexor, identifies illegal commands, delineates precise time intervals, controls format and address checking during data transfers, unloads the read/write head during lapses in subsystem activity, and requests data channel and program interrupt service when needed for a diskette operation.

Data Format

A track contains 8 sectors. Each sector contains address and data fields, and each field includes a sync bit. The last word in the data field is a cyclic check word used to check the accuracy of data when read from disc.

2F Data Transcription

Data transcription to and from diskette employs the 2F technique which combines both data and clocking information in a serial bit stream. The microcode processor combines serial data from the write shifter with clock pulses, forming a 2F encoded data writing stream. During reading, 2F encoded data from the read head is separated into clock and data streams in the drive's data separator. Flow of the data reading stream into the read shifter is controlled by the microcode processor.

Dual Drive Multiplexors

Principal signals to and from each diskette drive pass through dual drive multiplexors and ultimately share most of the major subsystem control and data path resources. The contents of **UNIT SELECT** in the subsystem command register control the state of the drive multiplexors. A selection jumper (not shown) establishes drive identities by assigning unit number 0 to the left or the right drive.

Information Flow and Control Sequences

Diskette operations include set up and status transfers (Specify Diskette Address, Specify Diskette Operation, Specify Memory Address, Read Status) head positioning (Step In, Step Out, Load and/or Settle Head), address verification (Read Preamble) and data transfers (Read Next Sector, Write Next Sector, Write Format). Each kind of operation implies a distinct sequence of events and a unique routing of information. The following summaries typify the data paths and control sequences for each category of operation.

Setup and Status Transfers

All setup and status transfers are one-step operations that involve the transfer of a single data word between a CPU accumulator and some register in the subsystem. In all cases a programmed I/O instruction specifies the transfer, and control signals from the function decoder enable the appropriate data path through the diskette multiplexor.

Destination registers in the subsystem for Setup and Status Transfers include Starting Memory Address Register (for the data channel), and Command Register. Source registers in the subsystem include Sector Preamble Register (read shifter), Memory Address Register and Status Register.

Head Positioning

A Device Flag Control signal from the function decoder, together with the contents of the diskette command register control head positioning. When the program issues any head positioning command, the read/write head load (if unloaded) and the Step In or Step Out operation is initiated by the microcode controller; no additional operations may be initiated for another 10ms. If the program issues no additional command within two disc rotations, the controller unloads the head.

Address Verification

Data transfer operations may be directed only to the *next* sector to pass under the transcription head. The Read Preamble operation allows the program to determine which disc sector is presently under the head.

When the program initiates the command, the microcode processor waits for the next hard sector mark to occur, and then enables the read circuits to scan for the soft sector mark or sync bit. The processor strips the address sync bit and loads the next 16 bits (those of the sector address field) into the read shifter and terminates the operation.

The program must then initiate a register transfer operation to move the contents of the shifter (Disc Preamble) through the multiplexor to a CPU accumulator.

Data Writing

The Write operation transfers one sector (256 16-bit words) of data from memory to the next diskette sector to pass under the write head if and only if the sector address read from the preamble of that sector matches the sector address specified in the subsystem command register. Data transfers occur independently of direct program control via the microNOVA data channel.

The microcode generator directs the flow of data during the write operation. When the program initiates the operation, the controller requests data channel to place the first word from memory into the data channel output register. The microcode processor waits for the next hard sector mark, enables the read scanner to detect and strip the address field sync bit, and then shifts the sector preamble into the read shifter. If the sector address matches that specified in the command register, the microcode processor initializes the data writing circuits, the sync bit and leader generators and the checkword calculator.

Approximately 75 microseconds after the address field passes under the head, the controller begins writing the data field leader; approximately 60 microseconds later it writes the sync bit, moves the first data word from the data channel register into the write shifter, requests another word from the data channel, and then begins shifting data to the write drivers and to the checkword generator. Data moves from memory through the data channel to the data channel buffer and then into the shifter until all 256 data words have been written. The 16-bit checkword in the checkword calculator is then shifted to the write drivers and the microcode processor terminates the operation.

Data Reading

The Read operation initiates the transfer of data from the next sector to pass under the read head if and only if the sector address of the preamble read from the address field of that sector matches the sector address specified in the subsystem Command Register. If the addresses match, the subsystem reads 257 16-bit (data plus checkword) words from that sector. The subsystem transfers 256 data words to memory via the data channel.

When the program initiates the operation, the microcode processor waits for the next hard sector mark, enables the read scanner to detect and strip the sync bit, and then reads the 16-bit address field into the read shifter. If the sector address matches the address specified in the command register, the microcode processor initializes the data reader, detects and strips the data sync bit and begins shifting data into the read shifter. It also enables the read checkword calculator. After the processor loads 16 data bits into the shifter, it loads that word into the subsystem storage multiplexor and requests service from the microNOVA data channel. The microcode processor repeatedly shifts a 16-bit word into the shifter and moves it into the temporary register; should the data channel fail to retrieve a word from the temporary register before the next word fills the shifter, data is lost and the Data Late error flag is set to 1 in the subsystem status register

As each data bit passes the checkword calculator it recomputes the cyclic polynomial. When the 256'th data word moves from the shifter to the data channel register, one additional word (the checkword) is read from the diskette, and compared with the checkword computed by the subsystem during the read operation. If the computed and retrieved checkwords do not match the Checkword Error flag is set to 1 in the subsystem status register.

Drive Interlocks and Status Flags

A comprehensive collection of interlocks monitor the operations of the subsystem. When the program specifies an illogical or illegal operation, an interlock stops the operation; both the data in memory and that on the diskette will remain unchanged. In the event of power failure, or if an operator opens the drive door, during a data transfer, that operation halts and the appropriate error flags are set to 1 in the subsystem status register.

Status signals from the diskette drive include Write Protect, Door Open, and Write Fault. Status signals generated in the subsystem include Head Loaded, Illegal Operation, Head Home (Track 0), Not Ready, Not Ready Latch, Address Error, Checkword Error and Data Channel Late.

PROGRAMMING

The microNOVA diskette subsystems provide a straight-forward method in which to store data on an online direct-access media. To assist in accomplishing this task, the controller gives extensive control over the actions of the drives. The status of several error circuits are available to indicate what happened if a data transfer was aborted by the controller.

In general, after deciding which sector of which track on which drive to read or write, and what portion of main memory to read into or write from, give the controller the starting address of the memory area and the number of the desired sector and drive. Then, move the head to the desired track, wait until the desired sector is under the read/write head, and then direct the controller to read or write.

To move the head, step the head in or out, one track at a time, until the head is over the desired track. The controller will initiate an I/O interrupt request after each completed head step. After the last head step, find out which track and sector is currently under the head by giving a Read Preamble command. The controller will initiate an I/O interrupt request when the track and sector information is available. If the head really is over the desired track, keep giving Read Preamble commands until the sector immediately previous to the desired sector is under the head. At this point, give either a Read Next Sector or Write Next Sector command. The controller will wait until the next sector is under the head and check that this really is the desired sector by comparing the current sector number to the desired sector number. If they match, the controller will transfer 256 words of data (1 sector), via the data channel, either into or out of memory beginning at the specified memory address. The controller will initiate an I/O interrupt request after the data has been transferred.

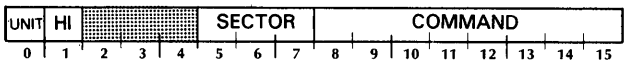
After the data transfer is complete, read the status register and check the error bits to ensure that the transfer terminated without error.

PROGRAMMING SUMMARY

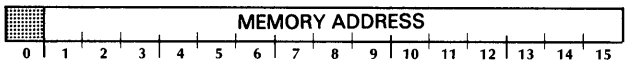
Mnemonic (first subsystem)	DKT
Device Code (first subsystem)	33
Mnemonic (2-4th subsystems)	DKT1, DKT2, DKT3
Device Code (2-4th subsystems)	73, 30, 70
Priority Mask Bit	10
Units/subsystem	1 or 2
Surfaces/unit	1
Tracks/surface	77
Sectors/track	8
16-bit words/sector	256
16-bit words/unit	157,696
Maximum Transfer Rate (words/second)	15,625
Allowable Dat Channel Latency (microseconds)	63.9
Head Step Time/track (ms)	10
Min. Head Load Time-overlaps any step command (ms)	60
Head Settle Time After Last Step (ms)	10
Head Settle Time After Unit Selection Change (ms)	170
Sector Access Time-min/max (ms)	1.2/160

ACCUMULATOR FORMATS

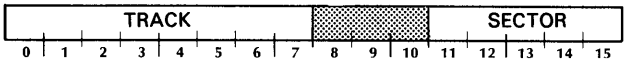
Specify Command and Diskette Address (DOA)



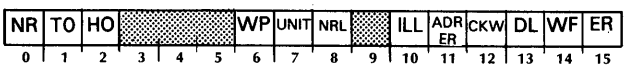
Load Memory Address Counter (DOB)



Read Current Address (DIC)



Read Status (DIA)



The device flag commands control the diskette's Busy and Done flags in the following manner:

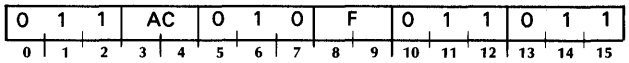
f=S Set the Busy flag to 1; set the Done flag to 0; set the Error, Write Fault, Data Late, Checkword, Address Error Illegal, and Not Ready flags to 0; and initiate the operation specified by the contents of the Command Register.

f=C Set the Busy flag to 0, set the Done flag to 0, set all error flags to 0, and stop all data transfer operations.

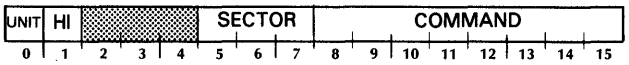
f=P Set the Done flag to 0.

Specify Command and Diskette Address

DOA *[f]* *ac,* **DKT**



Bits 0-15 of the specified AC are loaded into the diskette subsystem command register. After the transfer, the function specified by F is performed. The contents of the specified AC remain unchanged. The format of the specified AC is as follows:

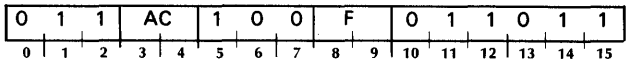


Bits	Name	Contents
0	Unit	Select the Drive (0 or 1)
1	Hi Trk	Must be set to one if the track address is strictly greater than 42_8 for any transfer specified by this command.
5-7	Sector	Sector address (0-7) if this command specifies a data transfer; if not, these bits are ignored.
8-15	Command	Specify the subsystem operation as follows:
	000	Settle 10ms
	001	Step out (toward Track 0)
	002	Step in (toward Track 77)
	010	Read preamble
	020	Read data, next sector *
	040	Write data, next sector *
	240	Format sector 0
	241	Format next sector

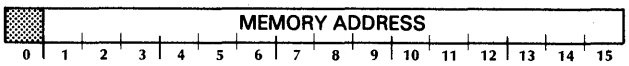
* Specified operation will not be attempted if the sector address read from the next sector does not match bits 5-7.

Load Memory Address Counter

DOB *[f]* *ac,* **DKT**



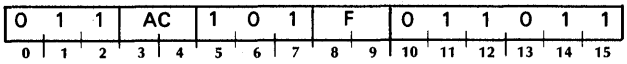
Bits 1-15 of the specified AC are loaded into the subsystem's Memory Address Register. After the transfer, the function specified by F is performed. The contents of the specified AC remain unchanged. The format of the specified AC is as follows:



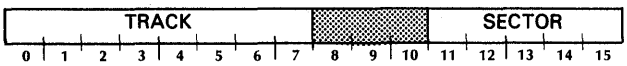
Bits	Name	Contents
0	----	Reserved for future use.
1-15	Memory Address	Location of the next word in memory to be used for a data channel transfer.

Read Current Address

DIC *[f]* *ac,* **DKT**



The current track and sector are placed the specified AC. After the transfer, the function specified by F is performed. The format of the specified ac is as follows:



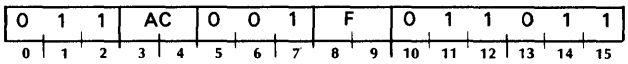
Bits	Name	Contents
0-7	Track	Identifies the track presently under the read head ($0\text{-}114_8$)
8-10	----	Reserved for future use.
11-13	Sector	Identifies the track presently under the read head ($0\text{-}7_8$)

NOTE *The address returned by the Read Current Address instruction accurately identifies the sector presently under the read head only if certain sequence and timing restrictions are met:*

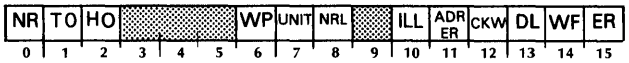
1. *The command has been preceeded* **recently** *by a Specify Command and Diskette Address instruction with a value of 010_8 in bits 8-15 of the specified address; AND*
2. *A* **single** *Start flag control command is issued to the subsystem along with or after the Read Current Address instruction in (1) is given; AND*
3. *The Read Current Address instruction is issued* **after** *the Done flag is set to 1 in response to (2), above, AND*
4. *The Read Current Address instruction is issued* **before** *the end of the current sector passes under the head (approximately 17-18ms after the Done flag is set to 1 in response to (2), above.*

Read Status

DIA *[f]* *ac,* **DKT**

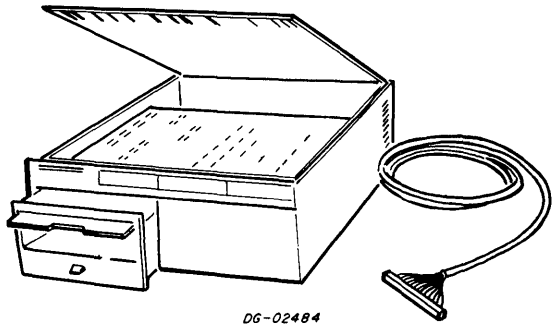


The contents of the diskette Status Register are placed in bits 0-15 of the specified AC. After the transfer, the function specified by F is performed. The format of the specified AC is as follows:

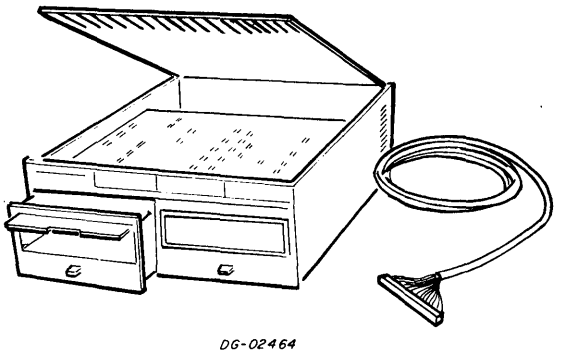


Bits	Name	Contents
0	Not Ready	The selected drive is not ready
1	Track 0	The head is positioned over track 0; this bit is meaningless if bit 0 is 1.
2	Head On	The head is loaded on the diskette media.
3-5	----	Reserved for future use
6	Write Protect	The diskette in the selected drive is write protected.
7	Unit	Indicates number of the selected drive (0 or 1).
8	Not Ready Latch	The Not Ready flag for the specified drive has had the value 1 at some time since the last Clear command was issued.
10	Illegal	An illegal command or sequence of commands was issued to the subsystem.
11	Address Error	The sector address read from the preamble of the sector specified for a read or write sector command does not match bits 5-7 of the command register.
12	Checkword	The checkword calculated by the subsystem did not match that read in the last sector transferred.
13	Data Late	The data channel failed to respond in time to a data channel request.
14	Write Fault	A failure in the transport, or an operator error has occurred. The fault may or may not be cleared by a Clear command or I/O RESET instruction.
15	Error	Any of bits 10-14 is 1; or if none of the error flags are 1, no data was read from the diskette.

ONE DRIVE DISKETTE SUBSYSTEM WITH CABLE



TWO DRIVE DISKETTE SUBSYSTEM WITH CABLE



DEVICE CODE JUMPERS

BIT POSITIONS OF DEVICE CODE	0	1	2	3	4	5
INSERT JUMPER TO SPECIFY 1	W10	W9	W8	W7	W6	W5

DRIVE 0 JUMPERS

DRIVE 0	INSERT JUMPER
LEFT DRIVE	W1
RIGHT DRIVE	W11

NOTE *The settings of jumpers W2, W3, W4, W12, and W13 are ignored.*

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SECTION VIII
PROM PROGRAMMER BOARD

Data General's model 8574 PROM programmer is an IOC-based controller capable of programming Signetics 82S126 (256x4 bits) and 82S130 (512x4 bits) PROM chips in an online mode when inserted in the sockets of a microNOVA PROM memory board. A full PROM board containing 512, 1,024, 2,048, or 4,096 16-bit words of PROM can be programmed and verified, one word at a time, under program control, using the PROM programmer. Programming a bit to 1 takes approximately 20 milliseconds, while programming a bit to 0 takes approximately 400 nanoseconds.

OVERVIEW AND INTRODUCTION

Any computer system that contains read-only memory (ROM) must have some method for initializing the contents of that memory. One method is to purchase ROM with the contents of the memory already initialized by the manufacturer. Another method is to purchase programmable ROM (PROM) which is initialized to contain all zeros or all ones, and to "program" the memory by "burning" ones or zeros in the appropriate bit positions. Once a bit has been programmed to contain a value different from the value to which it was initialized, the value of that bit can no longer be changed. In particular, if a PROM has been initialized to contain all zeros, once a bit has been set to 1 its value can not be changed back to 0. The contents of the PROM can be changed, however, by programming additional bits to be set to 1.

The microNOVA computer system includes a PROM programmer board for programming the contents of PROM that has been initialized to contain all zeros. The PROM programmer board provides the capability to program PROM, one word at a time, under program control. PROM is programmed by inserting PROM chips in the sockets of a PROM board, inserting the PROM board in the female board connectors of the PROM programmer board, and issuing the appropriate I/O instructions to the PROM programmer board to program and verify the contents of the memory.

SUMMARY OF CHARACTERISTICS

Applicable PROM Types	Signetics 82S126 and 82S130.
Board Dimensions	7.5 x 9.9in. (19 x 24.9cm.)
Maximum Operating Temperature	131°F (55°C)

BLOCK DIAGRAM

The block diagram on the opposite page shows the principal components plus data and control paths of the microNOVA system PROM programmer. It comprises an IOC and support circuits, a 16-bit data register, a 16-bit verification driver (non-latching), a 12-bit address register, and two banks of reed relays for driving the programming voltage to a PROM board.

The IOC, its clock driver, the function decoder, the I/O bus transceiver and the bus control buffer interface the PROM programmer to the I/O bus of a microNOVA CPU. The protocols by which the CPU communicates with peripherals is detailed in the Technical Reference for microNOVA Integrated Circuits *(DGC no. 014-000031)*.

Data is routed in bit parallel fashion out the IOC to latch in the address or data register, or it is routed from the data out lines of the PROM board through the verification driver into the IOC.

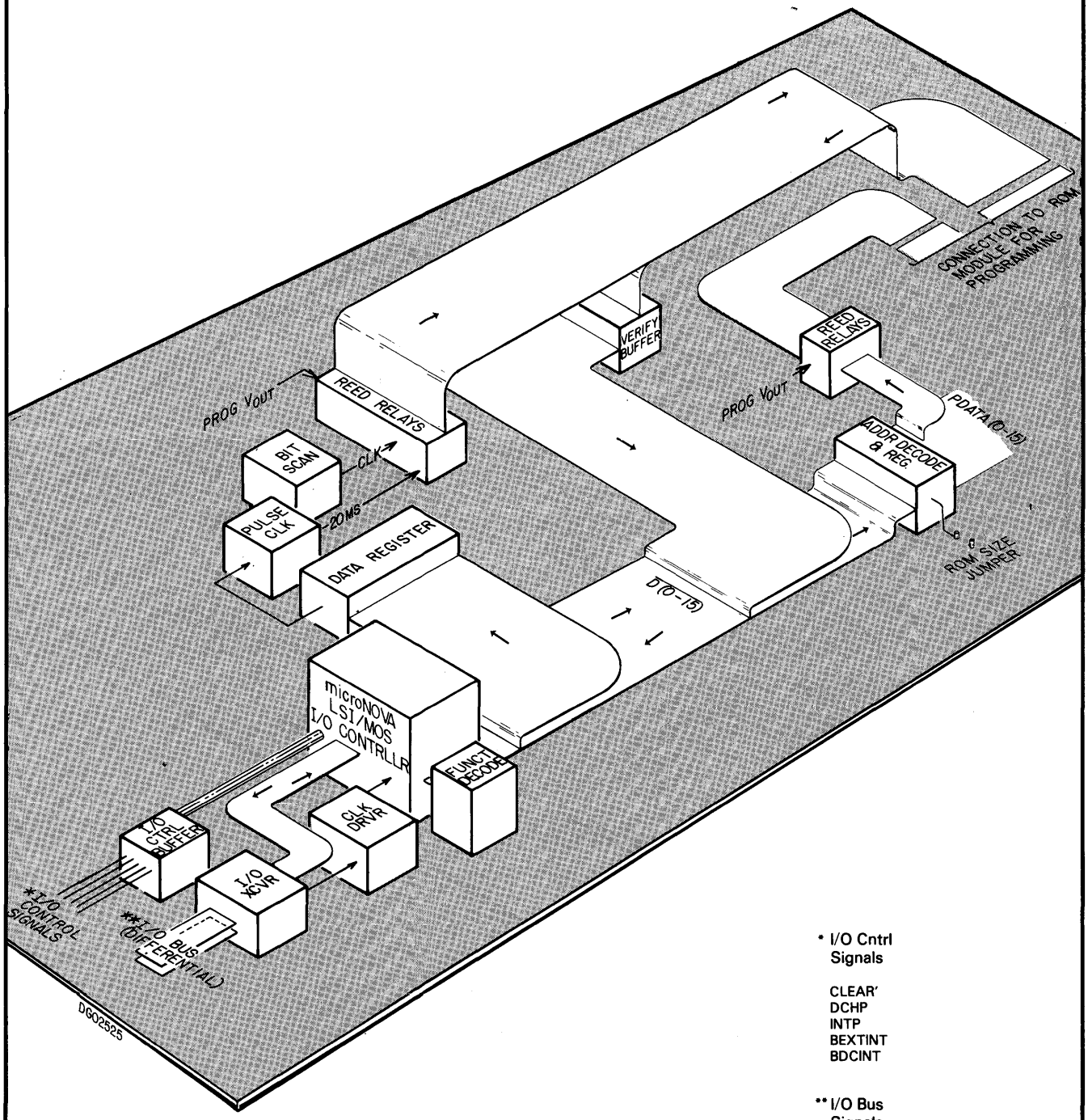
When a programming operation begins, the contents of three of the high-order four bits of the address register (depending on the PROM bank size) select and enable one of eight banks of PROM on the PROM board by applying a high level programming voltage to the V_{CC} input of that bank through input connector "A" of the PROM board; simultaneously, the entire 12-bit address is passed to the memory input latch on the PROM board. Depending on the size of the PROM board, the low-order 8 or 9 bits select an address within the bank that will be programmmed.

> **NOTE** *When programming a PROM board, the address selection jumpers on that board must be removed entirely. When this is done, all of memory locations on the board to be programmed lie in the range 000000 through the number of memory locations on the board.*

The contents of the data register are shifted left one bit at a time while the line scanner pulses each reed relay to apply a programming voltage to each bit in the addressed PROM location. The duration of the pulse determines whether the corresponding bit is programmed to a 1 or not (the PROMs are initially programmed to all 0's). For each bit value of 0 shifted out of the data register, the line scanner drives the reed relay for the corresponding data bit for 400ns, insufficient time to burn a 1. For each bit value of 1 shifted out of the data register, the line scanner drives the reed relay 20ms.

After the last bit is shifted out of the data register, the contents of the address register continue to select the word in PROM that was programmed for an additional 5ms. During that time the contents of the addressed word remains on the PROM board data out lines, at the input to the verification transmitter.

microNOVA PROM PROGRAMMER BOARD



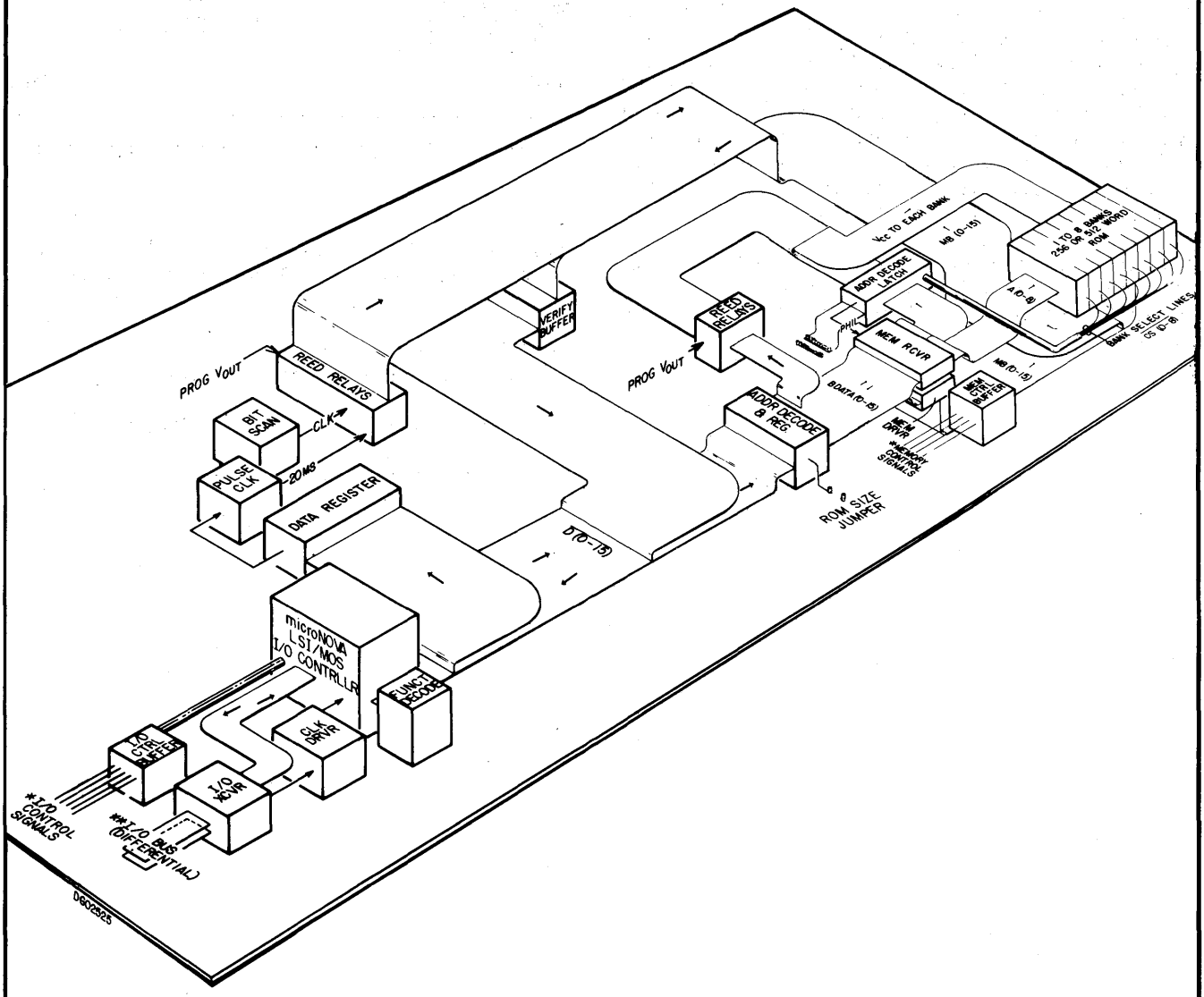
* I/O Cntrl Signals

CLEAR'
DCHP
INTP
BEXTINT
BDCINT

** I/O Bus Signals

BIOCLOCK/BIOCLOCK'
BIO[1,2]/BIO[1,2]'
MCLOCK/MCLOCK'

microNOVA PROM PROGRAMMER BOARD CONNECTED TO PROM BOARD



PROGRAMMING

The microNOVA PROM programmer board provides a method for online programming of PROM's on a module-by-module basis, without resorting to time-consuming programming on a chip-by-chip basis as with other PROM programmers. To achieve this goal, the PROM programmer gives control over the address to be programmed and the data to be written into that location. The programmed location can be read back so that one can verify whether or not the location was written correctly.

To program a location, specify the address and the information to be programmed. The ordering of these instructions is unimportant. Then, direct the PROM programmer to write the information into the location by giving a Start command with the second instruction. Programming of a 16-bit word takes approximately 20 milliseconds for each 1 in the word, and approximately 400 nanoseconds for each 0. After the PROM programming cycle is complete, the PROM programmer will initiate an I/O interrupt request and you have 5 milliseconds to read the location just written. This gives an opportunity to verify that the location programmed correctly.

To verify a location without changing its contents, go through a complete PROM programming cycle with an all-zero data word and then read the contents of the location.

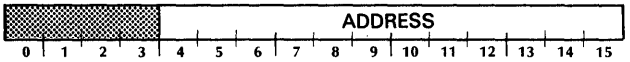
PROGRAMMING SUMMARY

Mnemonic	PROG
Device Code	5
Priority Mask Bit	12

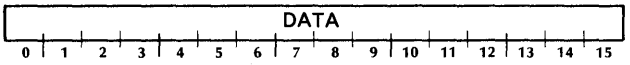
ACCUMULATOR FORMATS

Load Programming Buffer **(DOA)**

Specify Address **(DOB)**



Verify **(DIA)**



The device flag commands control the PROM programmer's Busy and Done flags in the following manner:

f=S Set the Busy flag to 1, set the Done flag to 0, and initiate a PROM programming cycle.

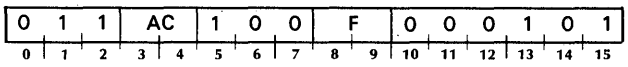
f=C Set the Busy flag and the Done flag to 0.

f=P Set the Done flag to 0.

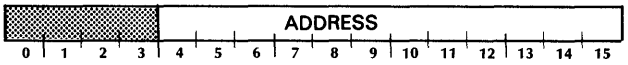
Instructions

Specify Address

DOB *[f]* *ac,* **PROG**



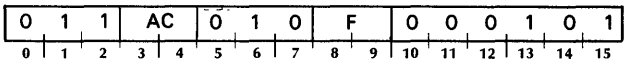
Bits 4-15 of the specified AC are placed in the PROM programmer's address register. After the transfer, the function specified by F is performed. The format of the specified AC is as follows:



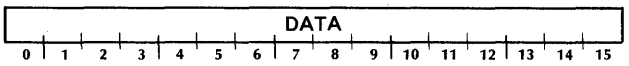
Bits	Name	Contents
0-3		Reserved for future use.
4-15	Address	Address of the PROM location to be programmed.

Load Programming Buffer

DOA *[f]* *ac,* **PROG**



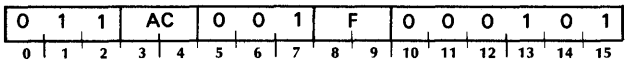
The contents of bits 0-15 of the specified AC are placed in the PROM programmer's data register. After the transfer, the function specified by F is performed. The format of the specified AC is as follows:



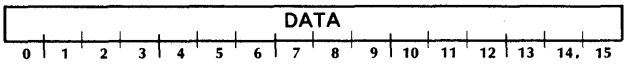
Bits	Name	Contents
0-15	Data	The information to programmed into the specified PROM location.

Verify

DIA *[f]* *ac,* **PROG**



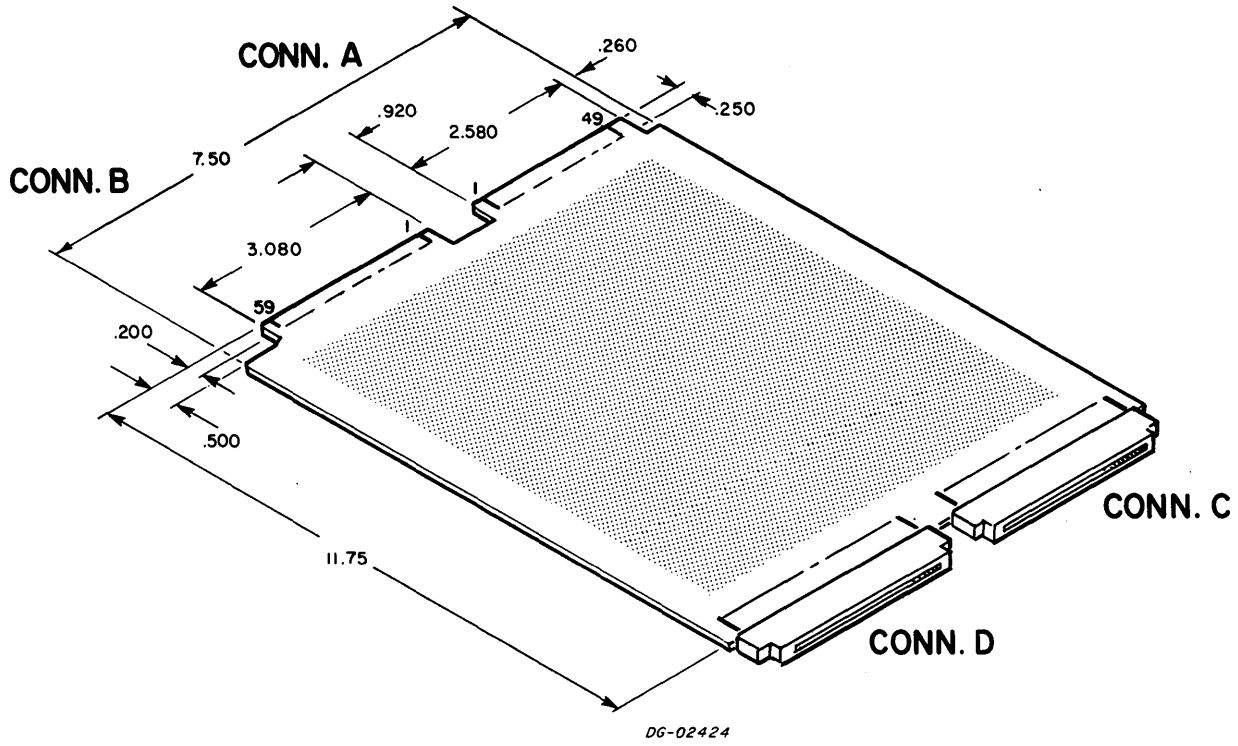
The contents of the most recently programmed PROM location are placed in bits 0-15 of the specified AC. After the transfer, the function specified by F is performed. The format of the specified AC is as follows:



Bits	Name	Contents
0-15	Data	Contents of the most recently programmed PROM location.

NOTE *For the data returned to be meaningful, this instruction must be issued within 5 milliseconds of the completion of a PROM programming cycle.*

PROM PROGRAMMER BOARD DIMENSIONS



DEVICE CODE JUMPERS

BIT POSITIONS OF DEVICE CODE	0	1	2	3	4	5
INSERT JUMPER TO SPECIFY 1	W1	W2	W3	W4	W5	W6

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SECTION IX
GENERAL PURPOSE INTERFACE BOARDS

Data General's model 4210 and model 4211 general purpose interface boards are IOC-based interfacing aids. Both boards contain an IOC module capable of providing a generalized front end to the microNOVA I/O bus. The IOC module handles all Busy/Done/interrupt processing and data channel interfacing. Model 4210 has pre-drilled holes and etched conductors, to assist in the building of an interface. Model 4211 has DIP sockets and wire wrap pins installed in the pre-drilled holes.

OVERVIEW AND INTRODUCTION

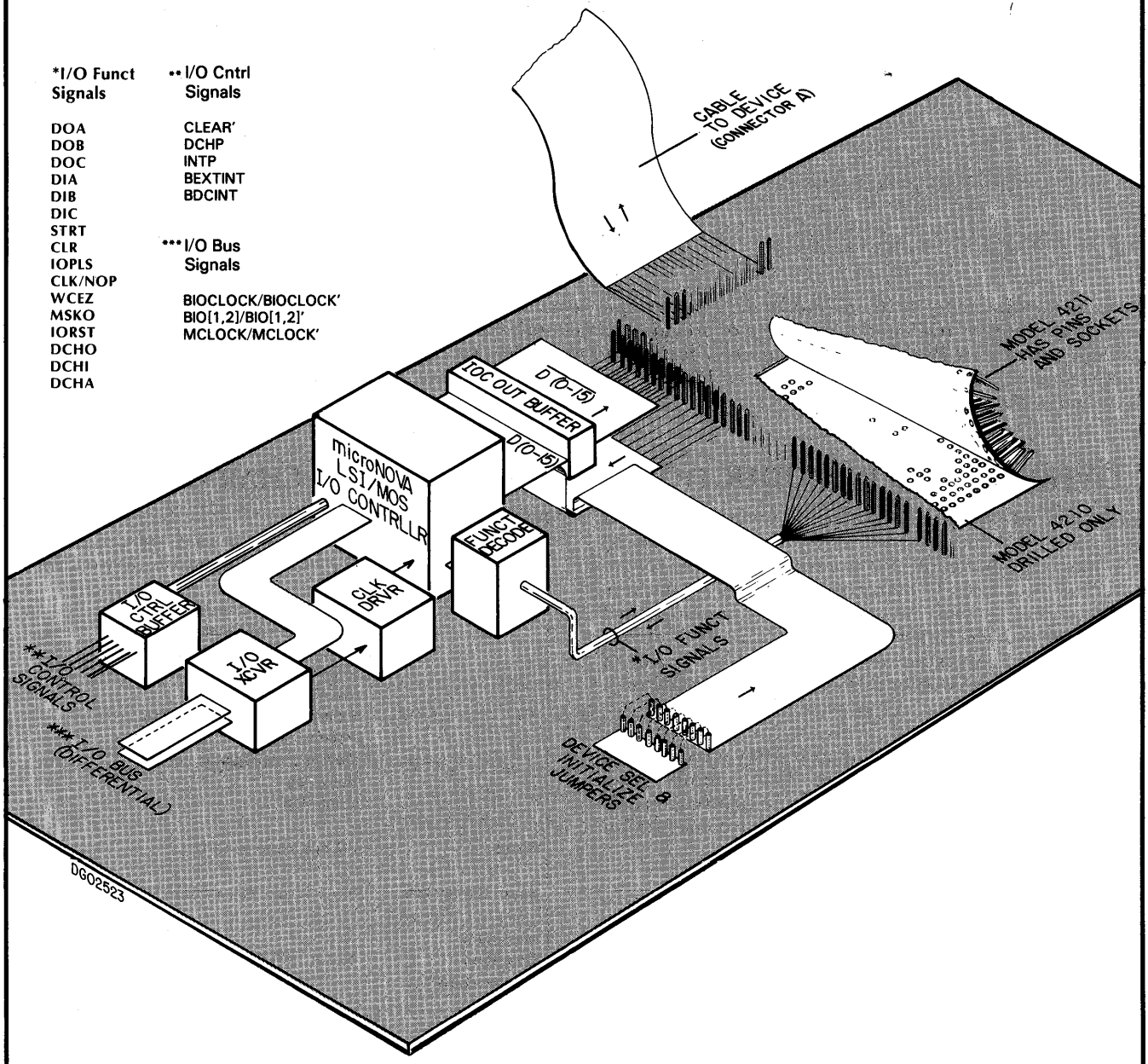
Microcomputers are used in a wide variety of applications from interactive information retrieval systems to systems for the monitoring and control of real-time processes. In many of these applications, it is necessary for the customer to interface non-standard equipment to the microcomputer. If no I/O device controller is available for a particular piece of equipment, the customer is forced to design his own controller.

Much of the logic contained in an I/O device controller is the same for every I/O device. This common logic can be designed once, laid out on a printed circuit board, and then used by customers in the construction of their own I/O device controllers.

A general purpose interface board is included in Data General's microNOVA family of computer assemblies. This board contains those logic elements that are common to most I/O device controllers, including an IOC and an I/O bus transceiver from the microNOVA family of integrated circuits. Drilled holes or sockets and wire wrap pins are provided for the customer to add those elements and interconnnections that are needed to control his particular equipment.

SUMMARY OF CHARACTERISTICS

Operations	I/O command decoding, interrupt and data channel requests, and data channel transfers.
Registers	15-bit data channel address 16-bit data channel word count Data channel request flag Interrupt request flag Interrupt disable flag External register enable flag Polarity flag Device code register Busy flag Done flag
Buses	I/O bus same as CPU.
Board Dimensions	7.5 x 10.4in. (19 x 26cm.)
Maximum Operating Temperature	131°F (55°C)


*I/O Funct Signals
DOA
DOB
DOC
DIA
DIB
DIC
STRT
CLR
IOPLS
CLK/NOP
WCEZ
MSKO
IORST
DCHO
DCHI
DCHA
**I/O Cntrl Signals
CLEAR'
DCHP
INTP
BEXTINT
BDCINT
***I/O Bus Signals
BIOCLOCK/BIOCLOCK'
BIO[1,2]/BIO[1,2]'
MCLOCK/MCLOCK'
CABLE TO DEVICE (CONNECTOR A)
MODEL 4211 PINS AND SOCKETS
MODEL 4210 DRILLED ONLY
IOC OUT BUFFER
D (0-15)
D(0-15)
microNOVA LSI/MOS I/O CONTRLLR
FUNCT DECODR
CLK DRVR
I/O CTRL BUFFER
I/O XCVR
**I/O CONTROL SIGNALS
***I/O BUS (DIFFERENTIAL)
*I/O FUNCT SIGNALS
DEVICE SEL INITIALIZE JUMPERS
DG02523

BLOCK DIAGRAM

The block diagram on the opposite page shows the principal components plus data and control paths for the microNOVA system General Purpose Interface (GPI). The GPI contains an IOC and its support circuits, plus a function decoder, and data buffer, plus sockets for device select and IOC initialization jumpers. All data lines, and control signals available for device use are brought to wire wrap pins. The I/O transceiver, IOC, clock driver and I/O control buffer connect the GPI to the I/O bus. The protocols by which the CPU communicates with peripherals are described in detail in the Technical Reference for microNOVA Integrated Circuits *(DGC no. 014-000074).*

Sixteen bidirectional data lines (bit parallel) extend from the IOC in two groups. One group passes via a 16-bit buffer to wire wrap pins and normally is used for output signals from the CPU to customer designed circuits. The buffer provides TTL fanout capacity without overloading the IOC. The other group of data lines passes directly to wire wrap pins and normally is used for input signals from the customer circuit to the CPU. The input lines are designed to be driven by a single low-leakage TTL driver so that the IOC will not be overloaded.

The Interface Designer's Reference Manual, *(DGC no. 015-000031),* provides information for the de igner of special interfaces. Written chiefly to describe the I/O buses of Data General ECLIPSE and NOVA line computers, it contains detailed discussions about those I/O systems, and provides insight for the designer building special interfaces to them; since the IOC output signals emulate the the ECLIPSE and NOVA line I/O buses, the information in the interface manual will prove helpful to those designing microNOVA interfaces.

PROGRAMMING

The microNOVA general purpose interface board consists of an IOC module and space in which the rest of an I/O interface can be implemented. The IOC module contains a B register which can be loaded and retrieved and a C register which can be loaded. When the general purpose interface board is used to implement a data channel controller, the B register can be used as the Memory Address register and the the C register can be used as the Word Count register. Alternatively, the IOC module can directly control the loading and retrieving of up to three input and three output registers.

On the general purpose interface board, an I/O instruction sequence consists of asserting the appropriate I/O command line, performing the data transfer, and then performing the appropriate device flag command.

The device flag commands control the IOC module's Busy and Done flags in the following manner:

f=S Set the Busy flag to 1, set the Done flag to 0, and assert the STRT command line.

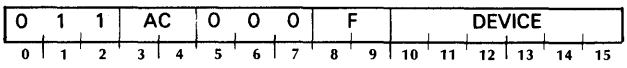
f=C Set the Busy flag to 0, set the Done flag to 0, and assert the CLR command line.

f=P Set the Done flag to 0 and assert the IOPLS command line.

Instructions

No I/O Transfer

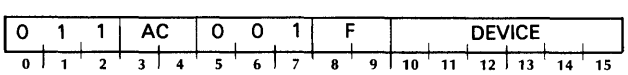
NIO *[f] ac,device*



The NOP command line is asserted. Then the function specified by F is performed.

Data In A

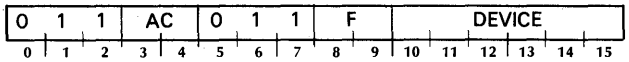
DIA *[f] ac,device*



The DATIA command line is asserted and then the contents of the data lines are placed in the specified accumulator. After the transfer, the function specified by F is performed.

Data In B

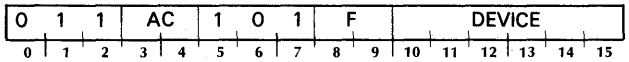
DIB *[f] ac,device*



The DATIB command line is asserted and then the contents of the data lines are placed in the specified accumulator. After the transfer, the function specified by F is performed.

Data In C

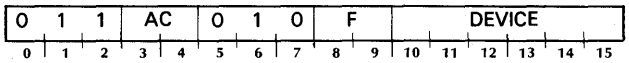
DIC *[f] ac,device*



The DATIC command line is asserted and then the contents of the data lines are placed in the specified accumulator. After the transfer, the function specified by F is performed.

Data Out A

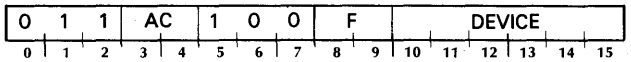
DOA *[f] ac,device*



The DATOA command line is asserted and then the contents of the specified accumulator are placed on the data lines. After the transfer, the function specified by F is performed.

Data Out B

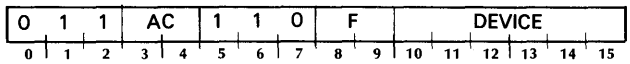
DOB *[f] ac,device*



The DATOB command line is asserted and then the contents of the specified accumulator are placed on the data lines. After the transfer, the function specified by F is performed.

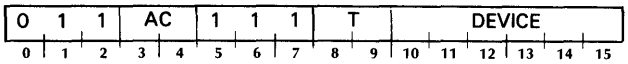
Data Out C

DOC *[f] ac,device*



The DATOC command line is asserted and then the contents of the specified accumulator are placed on the data lines. After the transfer, the function specified by F is performed.

SKP *[t] device*

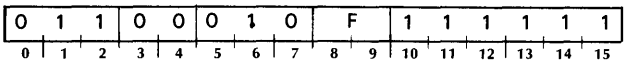


The IOC module asserts the SELB and SELD lines depending upon the condition of its Busy and Done flags. If the test condition specified by T is true, the CPU skips the next sequential instruction.

I/O Reset

IORST

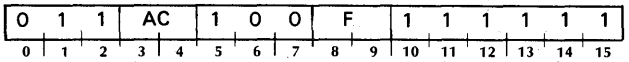
DOA *[f]* **0,CPU**



The Busy and Done flags in the IOC module are set to 0. The IOC module initializes its device code and logic polarity.

Mask Out

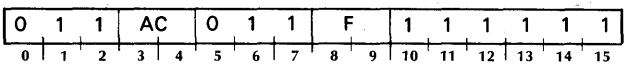
DOB *[f] ac,* **CPU**



The MSKO command line is asserted. Then the IOC module AND's the contents of its input data lines with the contents of the specified AC. If any of the result bits is a 1, the IOC module will not initiate an I/O interrupt request when its Done flag is set to 1.

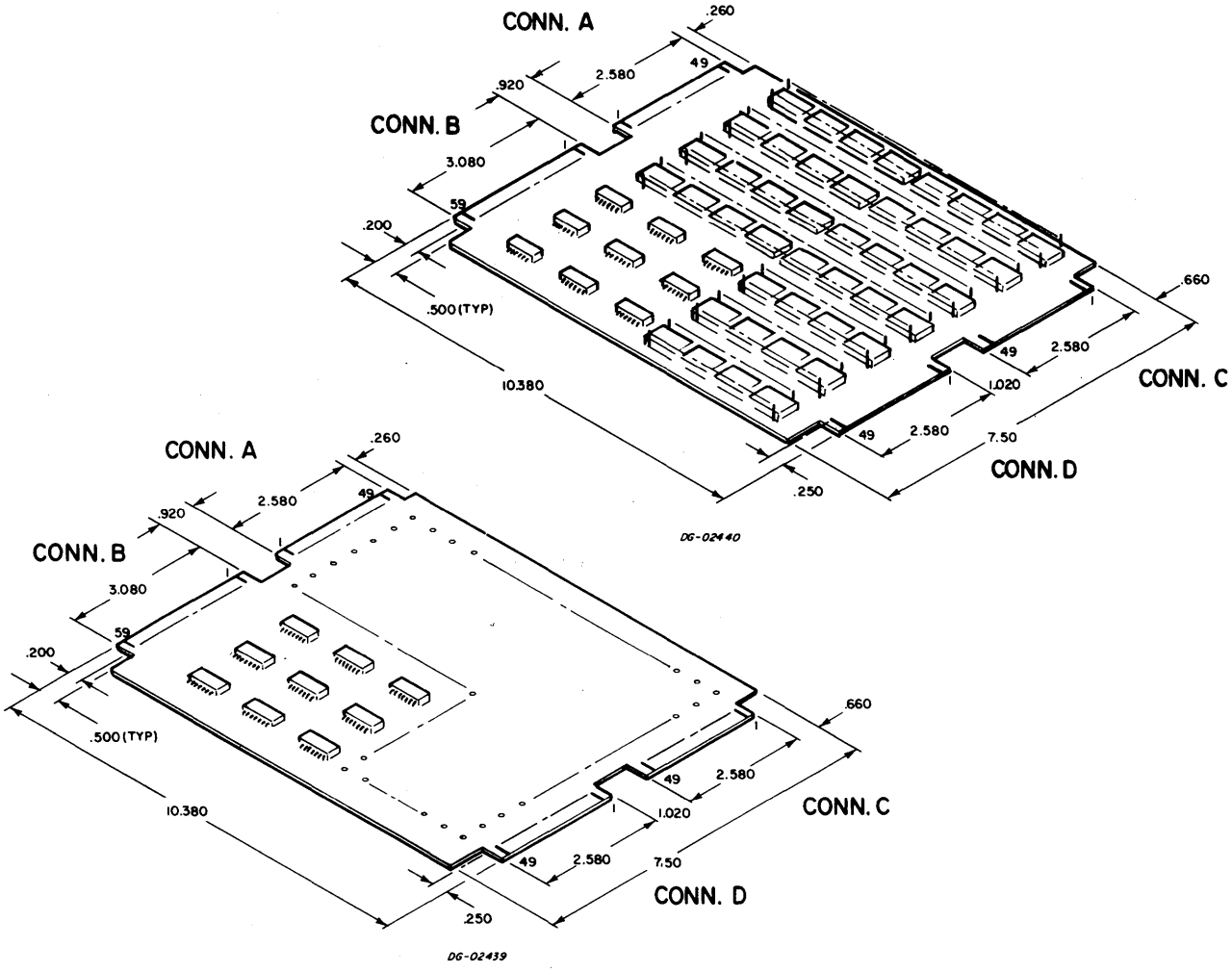
Interrupt Acknowledge

DIB *[f] ac,* **CPU**



The IOC module places its device code on the data lines if it is requesting an interrupt and it is the highest priority device that is requesting an interrupt.

GENERAL PURPOSE INTERFACE BOARD DIMENSIONS



DEVICE CODE JUMPERS

BIT POSITIONS OF DEVICE CODE	0	1	2	3	4	5
INSERT JUMPER TO SPECIFY 1	W3	W4	W5	W6	W7	W8

OTHER JUMPERS

JUMPER	NAME	FUNCTION
W1	EXTERNAL	Omit jumper if the address and word count registers internal to the IOC are to be used in data channel operations and with the DIB instruction.
W2	POLARITY	Insert jumper if positive logic is to be used in interfacing to the IOC.

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SECTION X
MISCELLANEOUS PRINTED CIRCUIT BOARDS

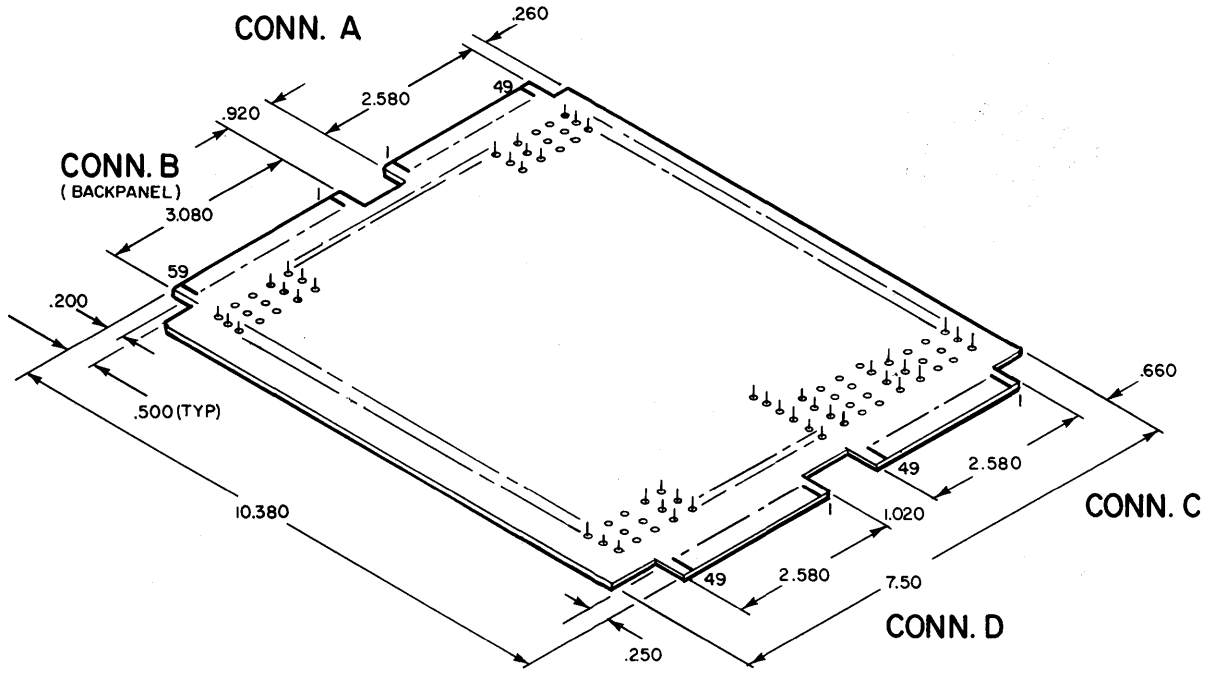
Models 1114 and 2301 boards available for custom applications and maintenance with the microNOVA computer. the model 1114 general purpose wiring board is drilled and etched, with wire wrap pins, to accept up to fifty 14-pin integrated circuits. The model 2301 extender board carries the backpanel signals to female edge connectors on the front of the board.

OVERVIEW AND INTRODUCTION

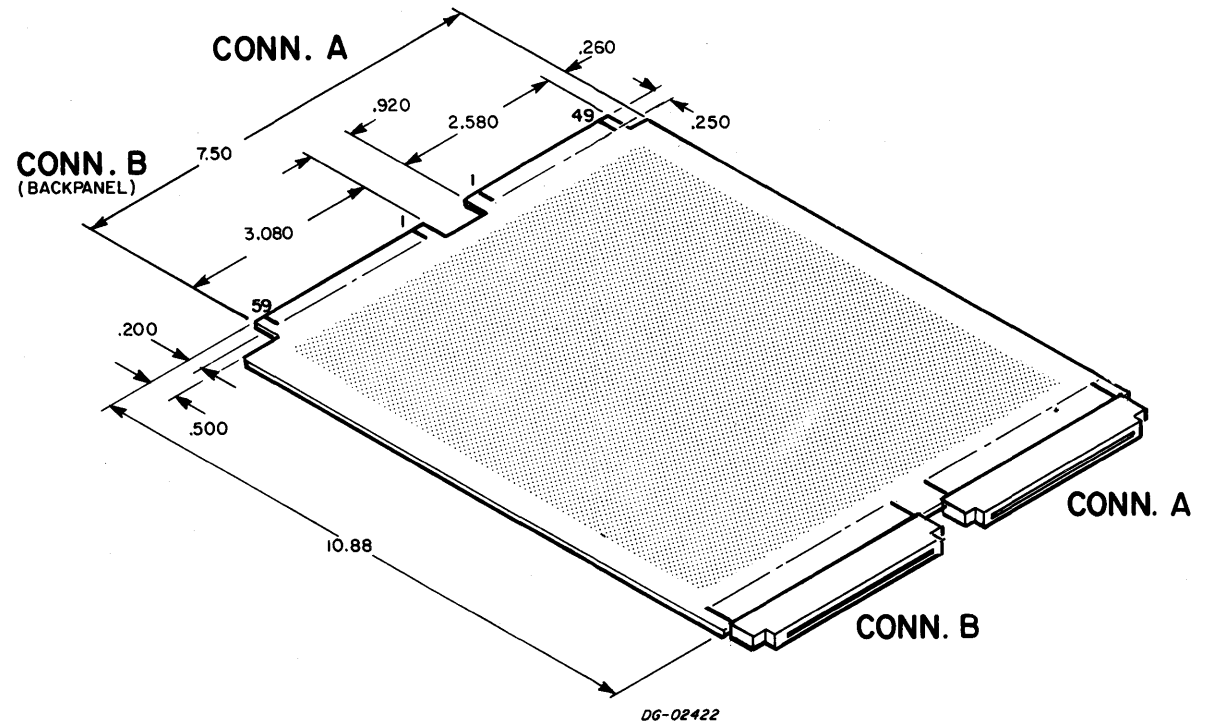
The Model 1114 Pre-Drilled Circuit Board is a general purpose wiring board suitable for the user who wishes to build a special purpose, custom interface to a microNOVA computer. The board has two male edge connectors on the backpanel edge, one of which plugs into the printed circuit backpanel socket; the other plugs into a device cable connector, in the event the board is used as an I/O device controller. The backpanel connector has 60 contacts, and the device connector has 50 contacts. Two additional 50 contact edge connectors are included on the forward edge of the board to provide flexibility to the interface designer. A series of holes in the card is designed to accept standard integrated circuit packages. Up to fifty 14-pin packages may be installed on one board, and an even larger number of smaller packages may be used. Each hole and each connector finger is connected by etch to an adjacent wire wrap pin.

The Model 2301 Extender Board is used for maintenance of any board in the microNOVA product line. The board has edge connectors which plug into the backpanel and a device cable connector. Etched conductors on the board carry backpanel and I/O signals to two female edge connectors on the forward edge of the board. Any microNOVA board may plug into the extender board and operate in this position, giving access for testing and maintenance.

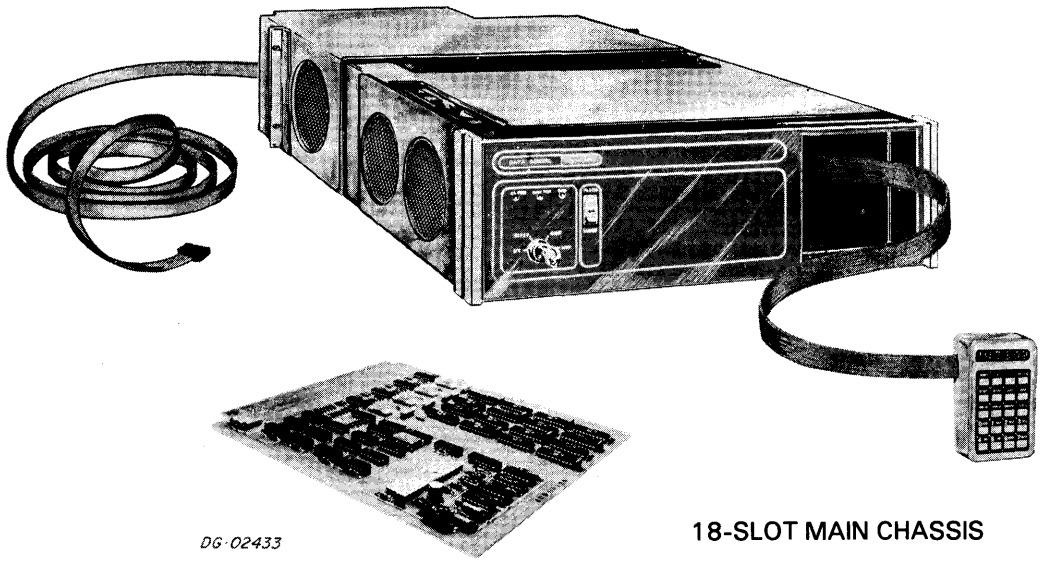
PREDRILLED CIRCUIT BOARD



EXTENDER BOARD

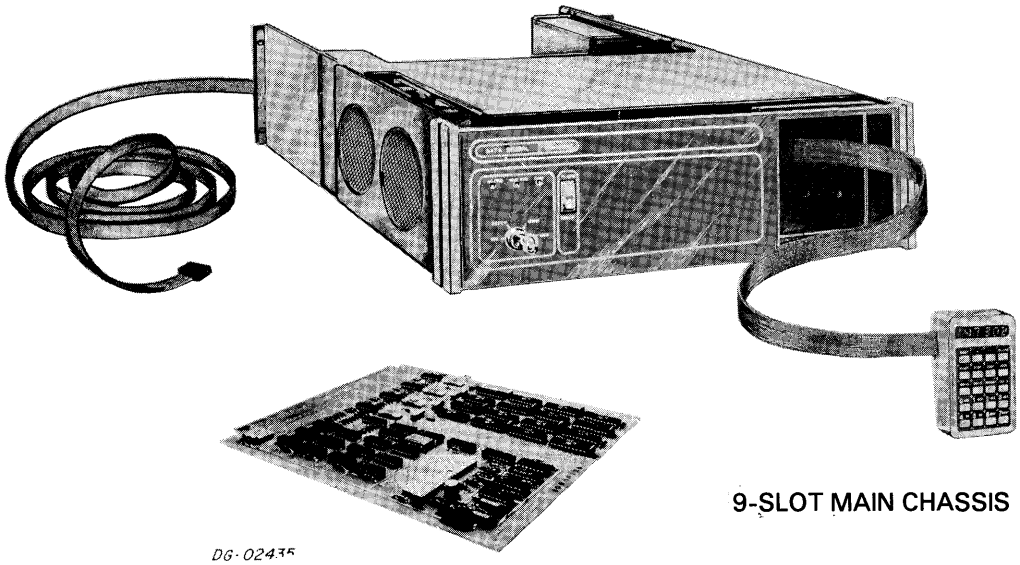


microNOVA CHASSIS



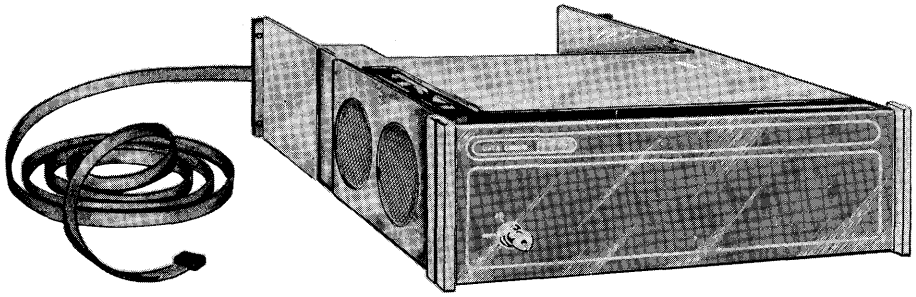
DG-02433

18-SLOT MAIN CHASSIS



DG-02435

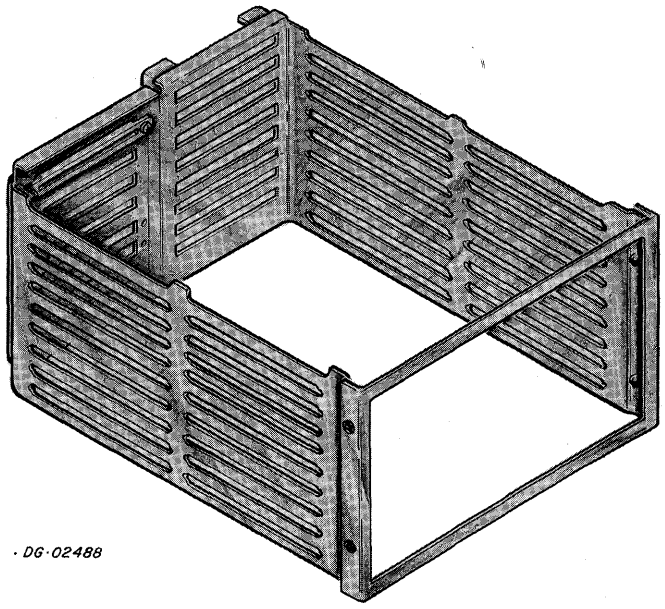
9-SLOT MAIN CHASSIS



DG-02477

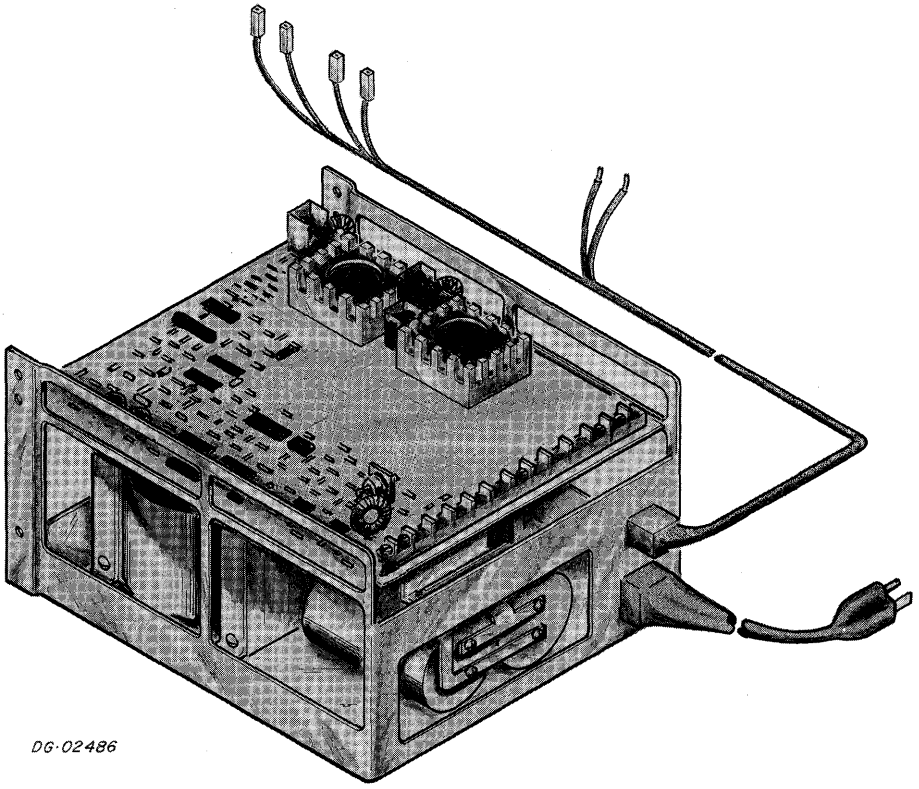
9-SLOT I/O EXPANSION CHASSIS

microNOVA CARDFRAME



DG·02488

microNOVA POWER SUPPLY



DG·02486

SECTION XI
microNOVA CHASSIS

Data General uses three distinct chassis to package microNOVA printed circuit boards. The chassis are rack-mountable, stamped metal enclosures which interconnect and supply power to the microNOVA line of printed circuit boards. Each includes cardframes, a power supply with optional battery backup capability, cooling fans, and a front panel. A printed circuit backpanel carries the memory bus, I/O bus, and necessary power from board to board. There are ttwo main chassis for microNOVA computer systems, and a 9-slot I/O expansion chassis. Major chassis components may be ordered separately for special applications.

OVERVIEW AND INTRODUCTION

Data General offers two microNOVA computers and an I/O expansion chassis as standard products for use with the microNOVA line of printed circuit boards. Three distinct chassis, especially designed to accept microNOVA computer boards, are used for these three models. The chassis differ in board capacity, overall size, and application. Models 8560 and 8561 are complete microNOVA computers with open slots available for additional memory and/or I/O control boards from the microNOVA product line. Each of these models contains a CPU board (microNOVA CPU and 4K words of MOS memory) installed in the chassis, and therefore constitutes a basic microNOVA computer. The chassis used with these models contain one or two 9-slot cardframes for additional boards, a front panel with operator controls, a power supply and internal cabling, and are available with optional battery backup units. These chassis are denoted as 9- or 18-slot main chassis. Model 8571 is a system expansion chassis, with 9 slots available for I/O control boards. It contains one cardframe, a front panel, a power supply, and internal cabling. This chassis is denoted as a 9-slot I/O expansion chassis. All models mount in a standard 19" equipment cabinet.

SUMMARY OF CHARACTERISTICS

8560 Chassis	17 available slots (8 memory and/or I/O and 9 I/O), includes CPU and 4K MOS; battery optional
8561 Chassis	8 available slots (memory and/or I/O), includes CPU and 4K MOS; battery optional
8571 Chassis	9 available slots (I/O only)
4212 Cardframe	Accepts up to nine microNOVA printed circuit boards. Includes backpanel and stiffening frame
4213, 4214 Power Supply	Provides power for up to 18 microNOVA printed circuit boards. Includes power cord, fuses, and internal cable for ac power distribution.
	The Model 8560 main chassis contains two Model 4212 cardframes with a Model 8563 CPU board,a power supply, and a front panel with power/reset/run switch, indicator lights, and program load/continue switch
	The Model 8561 main chassis is identical to the Model 8560, but contains only one Model 4212 cardframe.
	The Model 8571 I/O expansion chassis contains one Model 4212 cardframe, a power supply, and a front panel with power on/off switch.

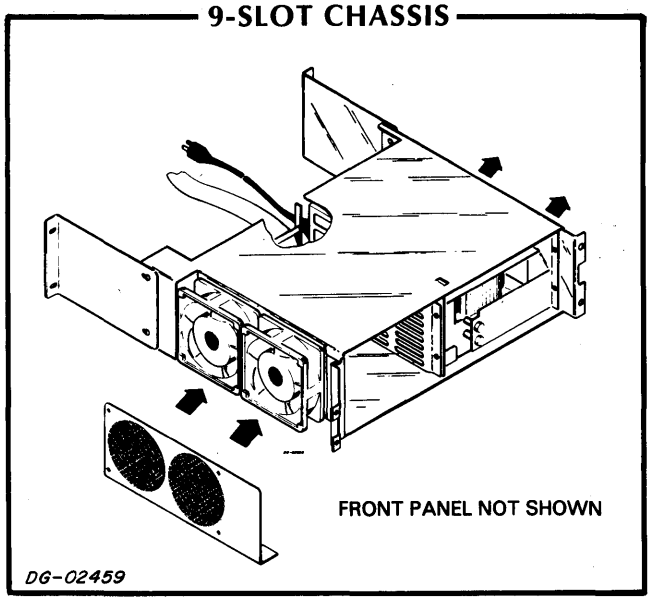
The cardframe and power supply may be ordered separately, for those customers who desire to install a microNOVA computer in custom equipment. The Model 4212 Cardframe is designed to accept and interconnect up to 9 printed circuit boards from the microNOVA product line. The Models 4213 and 4214 Power Supplies are designed to provide all necessary power for up to two fully occupied cardframes. Overall dimensions and electrical specifications are identical for both power supplies. Either supply may be installed in a 9- or 18-slot microNOVA chassis. The Model 4214 includes a battery unit, which supplies operating power during loss of primary line voltage, and charging and switchover circuits to support the battery service.

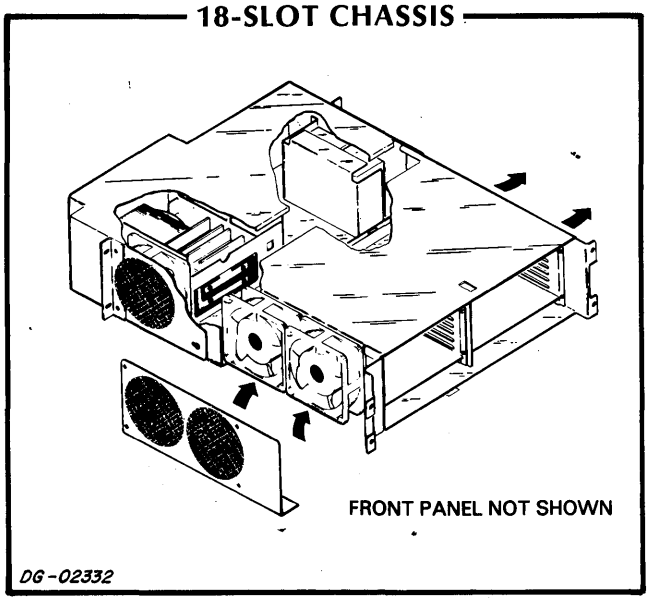
The remainder of this section describes, in more detail, the characteristics of each model.

CHASSIS

The microNOVA chassis are sheet metal enclosures containing a power supply, one or two 9-slot cardframes, an optional battery backup unit, a front panel, and interconnecting cables. Ventilation fans on the left side of the enclosure provide air flow to cool the printed circuit boards and power supply. The fans draw air in from the left, across the power components, and out the right side of the enclosure.

The chassis mounts in a standard 19in. equipment cabinet, and occupies 5 1/4in. of rack space. The front face of the sheet metal enclosure is open, and is covered by a hinged front panel as described below. Cardframes mount inside the enclosure, facing forward to give front access to remove and install microNOVA boards. The 18-slot main chassis contains two cardframes, mounted side-by-side inside the enclosure. The 9-slot chassis contain one cardframe, mounted on the left side of the enclosure. The physical size of the enclosure varies, depending on the number of cardframes in the chassis. The main component is an open frame which bolts to the forward cabinet rails, and is the same unit for one or two cardframe applications. The enclosure's rear support member varies according to the number of cardframes installed. The single cardframe in the 9-slot chassis is located on the left next to the cooling fans, and the power supply is located in the space on the right side. In this case, sheet metal extensions are attached to the rear of the enclosure and bolt to the rear cabinet rails. The 18-slot chassis has an additional sheet metal housing, fastened to the rear of the main enclosure frame, which houses the power supply in addition to providing rear support to the enclosure. An additional ventilation fan is included on the left side of this housing to cool the power supply. This housing increases the overall depth of the enclosure; overall dimensions are shown in figures at the end of this section.



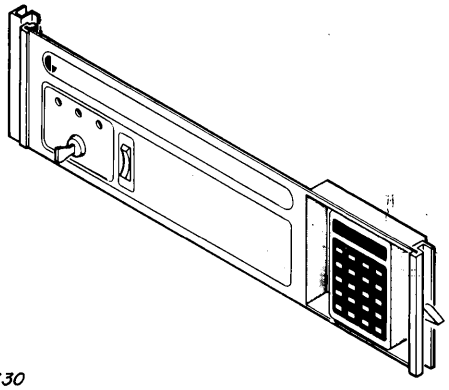


A strain relief bracket fastened to the rear of the enclosure behind the cardframes provides mechanical support for I/O and device cables and prevents inadvertent damage to the printed circuit boards. The bracket accepts from 1 to 20 ribbon cables.

A hinged front panel, containing certain operator controls, covers the front of the enclosure and provides convenient access to the microNOVA printed circuit boards. The panel hinge is on the left side, and allows the panel to swing open fully. A latch on the right side holds the panel securely closed. There are two types of front panel, which differ in the number of operator controls which they contain. The front panel used with the 9- or 18- slot main chassis contains a four-position power/run/reset keylock switch, three lights to indicate ac power, dc backup power, and CPU run condition, and a two-position program load/continue rocker switch. Additionally, a recess designed to store the handheld console is molded into this panel. The front panel used on the 9-slot I/O expansion chassis contains an on/off power keylock switch, and there is no recess for a handheld console.

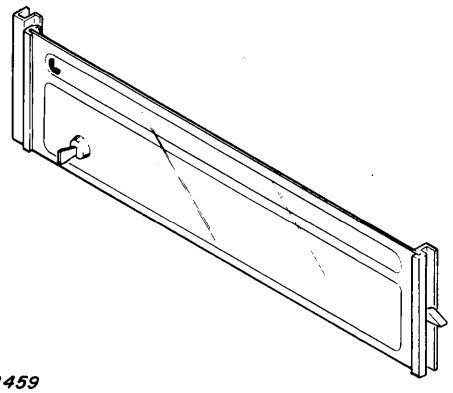
Electrical signals from the front panel controls are carried to their destinations within the enclosure by cables. All connections to the power supply and microNOVA boards are made with plugs, and the cables are tied to the rear of the front panel to provide unobstructed access when the panel is open.

MAIN CHASSIS FRONT PANEL



DG-02330

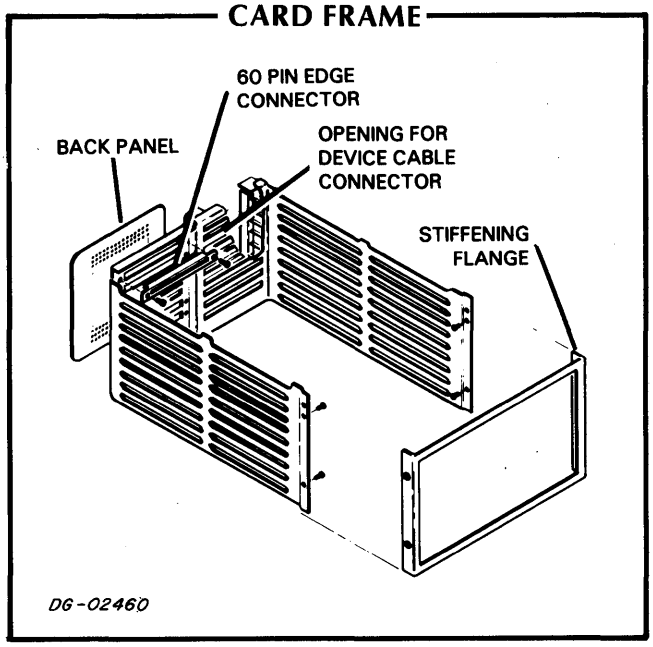
EXPANSION CHASSIS FRONT PANEL



DG-02459

CARDFRAME

The Model 4212 cardframe is the basic building block of the microNOVA chassis; it is a stamped steel enclosure with slots for nine microNOVA printed circuit boards, a printed circuit backpanel with nine 60 pin female edge connectors, nine adjacent openings in the rear for device cable connectors, and openings for cooling air flow. A printed circuit board is installed in one of the slots from the front of the cardframe. The 60 pin edge connector on the board mates with and plugs into the 60 pin socket on the backpanel; the 50 pin edge connector on the board is then aligned with the corresponding opening for a device cable connector. Spring clips on the rear of the cardframe hold the cable connectors securely in position.



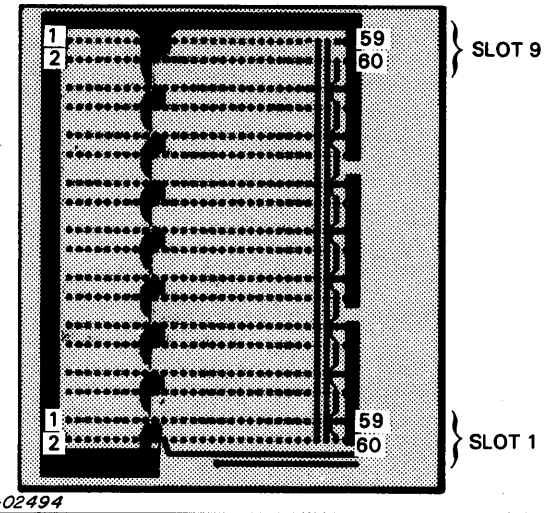
The printed circuit backpanel carries memory and I/O signals among the boards installed in the cardframe, and delivers the necessary power to the boards from the power supply. Etch on the backpanel passes all signals in parallel from one 60 pin edge connector to the next. Every contact on all edge connectors corresponds to a wire-wrap pin protruding from the rear of the backpanel; the pins are spaced so that standard plug connectors may be used to extend the I/O bus, communicate with certain peripherals, etc. The pins are numbered as shown in the diagram -- viewed from the pin side, the pins are numbered from left to right, 1 to 60, with odd numbers on the top and even numbers on the bottom. The slots are numbered 1 through 9, from bottom to top.

Two jumper wires may need to be installed on the backpanel. They are used to continue the data channel and program interrupt priority chains, which pass from slot to slot via etch on the backpanel. These priority chains are terminated at a slot when that slot does not contain a board. In order to include any boards above the empty slot in either of these priority networks, they must be continued across the empty slot with jumper wires wrapped to the appropriate backpanel pins. These pins are denoted as INTP and DCHP, and may be located by reference to the DGC engineering drawing of the backpanel layout.

Any board in the microNOVA series will fit in any slot; however, when a cardframe is contains the microNOVA CPU board, that board must be installed in slot number 1. The remaining slots may contain a mixture of memory and I/O boards, but all memory boards in the entire system must be installed in this cardframe, which is called the primary cardframe. The slot assignment diagram shows this arrangement. A microNOVA computer system may contain up to 3 fully occupied card frames. The expansion cardframes may contain any I/O board, but may not contain memory boards or an additional CPU board. When a system is expanded to include more than one cardframe, the I/O bus is extended from one frame to the next with a daisy-chain I/O cable, whether the cardframes cages are in the same enclosure or if they are in separate enclosures. An I/O terminator must be installed on the last cardframe in the system.

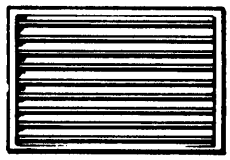
When a cardframe is ordered separately from the assembled chassis, a stiffening flange is included to reinforce the front. This flange does not interfere with installation or removal of the microNOVA printed circuit boards. The stiffening flange is not necessary when the cardframe is installed in a microNOVA chassis enclosure.

BACKPANEL PIN NUMBERING



DG-02494

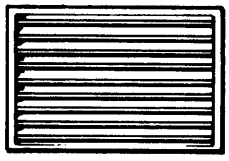
SLOT ASSIGNMENT



SLOTS 2 TO 9
microNOVA MEMORY
AND/OR I/O

SLOT 1 - microNOVA CPU

PRIMARY CARDFRAME

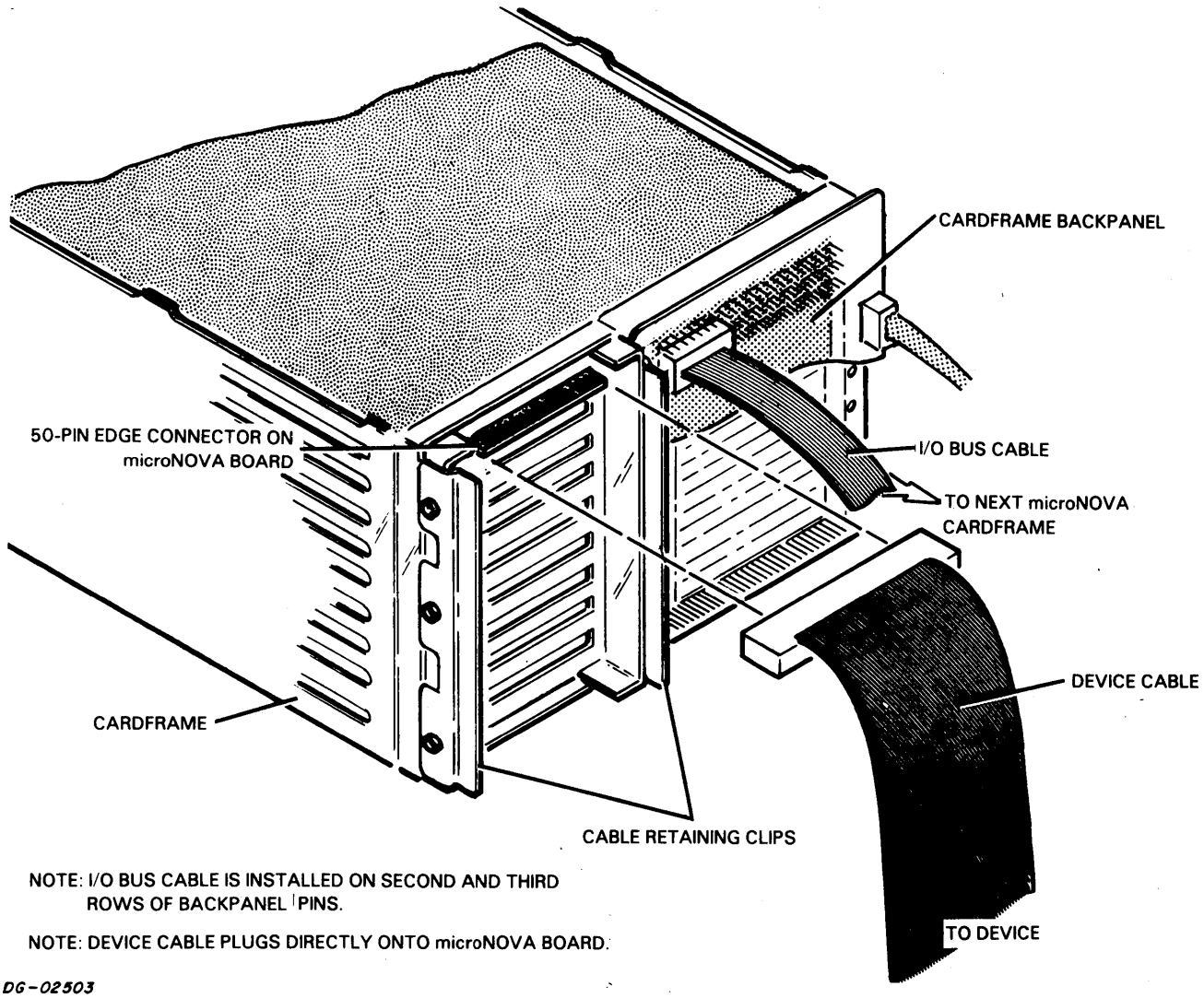


SLOTS 1 TO 9
microNOVA I/O ONLY

EXPANSION CARDFRAME

DG-02507

EXTERNAL CABLE CONNECTIONS



NOTE: I/O BUS CABLE IS INSTALLED ON SECOND AND THIRD ROWS OF BACKPANEL PINS.

NOTE: DEVICE CABLE PLUGS DIRECTLY ONTO microNOVA BOARD.

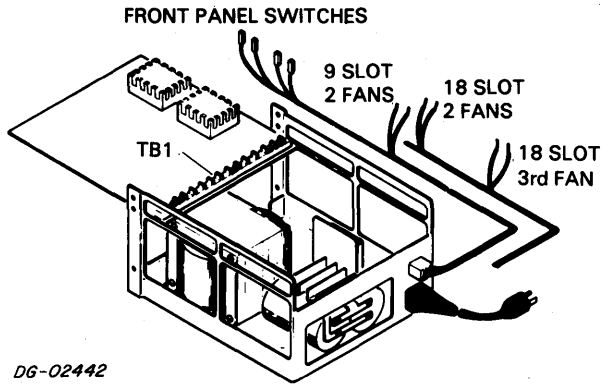
DG-02503

POWER SUPPLY

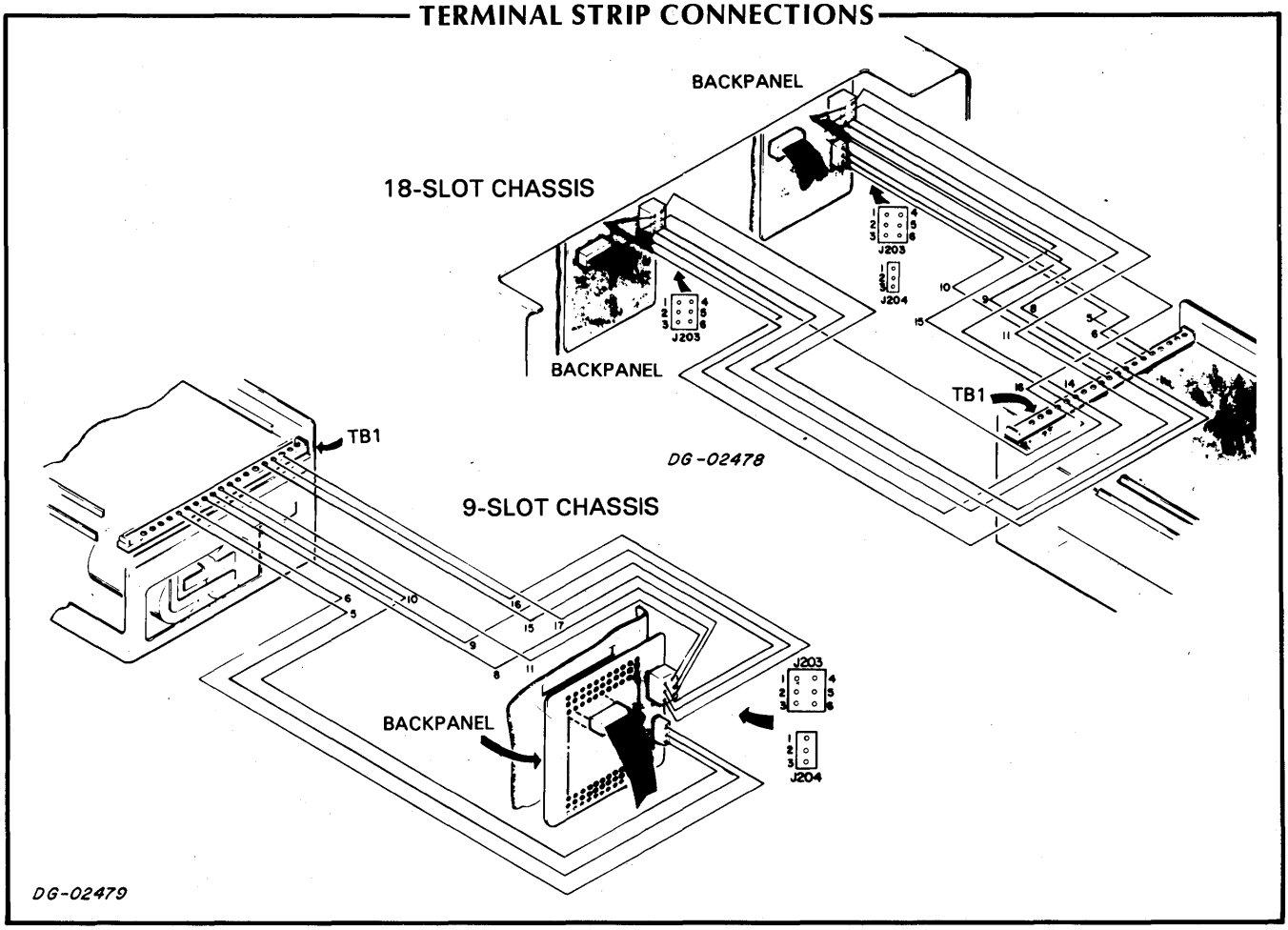
A Model 4213 or 4214 power supply provides the necessary power for one or two fully occupied cardframes, and is contained within a sheet metal box which has the same outside dimensions as a cardframe. The power supply box contains large circuit components, and a printed circuit board is fastened to the top of the box. A 19-lug terminal strip is fastened across one end of the board, and supplies power to the cardframe backpanel(s) through cables. These cables fasten to the terminal strip with standard lugs, and plug into the backpanel(s) with molded connectors. A three-conductor cable, and one or two six-conductor cables, distribute power from the supply to the cardframes. The three-conductor cable and one six-conductor cable are used to provide power to one cardframe; when two cardframes are employed, each receives power from a six-conductor cable, and the three-conductor cable is plugged into the second (I/O only) cardframe. The cabling diagram shows these connections for both cases.

The power supply is placed in two different locations within the chassis, depending on the number of cardframes in the chassis. The power supply is on the right-hand side of the 9-slot chassis, next to the single cardframe. The terminal strip is toward the rear and the fuses are accessible from the front. On the 18-slot chassis, which contains two cardframes, the power supply is fastened inside an additional housing, behind the left cardframe. In this case, the terminal strip is toward the front and the fuses are accessible from the rear. In both cases, the line supply power cord is routed out the rear of the enclosure.

POWER SUPPLY



TERMINAL STRIP CONNECTIONS

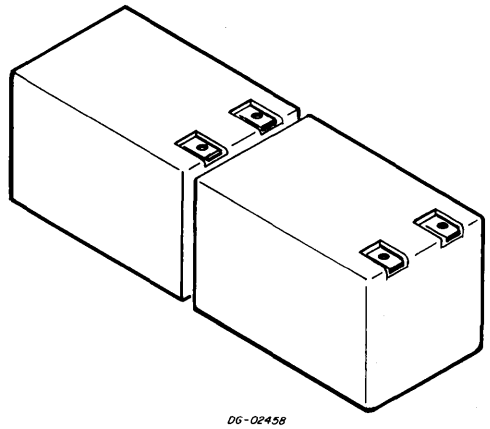


Power Supply with Battery Backup

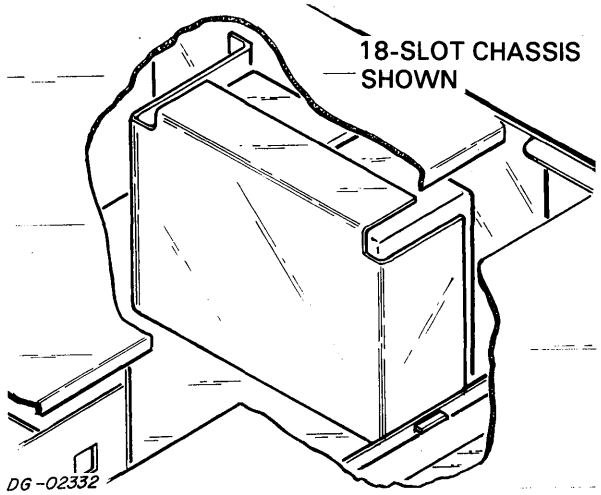
Both power supply models have identical dimensions and power ratings. Model 4214 has the required circuitry to support a battery backup unit, and this battery unit is included with the power supply. The battery backup unit consists of two sealed plastic cases containing lead-acid cells with sufficient charge to power the microNOVA CPU and MOS Memory in the event of primary power failure. A shelf, stamped into the right rear support member of the enclosure, supports the two cases and a sheet metal plate clamps them securely in place. The cases are wired in series, and two wires carry battery power to the power supply terminal strip, using faston connectors on the battery end and terminal strip lugs on the power supply end.

Battery power is normally used to maintain data in the microNOVA memory when primary power is lost. Although the battery has sufficient power to operate the system, it is good practice to ensure that the microNOVA CPU remains in the HALT state when power is lost, to minimize current drain on the battery. The customer may choose battery backup service for all 9 slots of the primary cardframe, or any of three subsets of slots of that cardframe. Slots 1-3 always receive battery backup service; slots 4-6 and/or 7-9 may be selected for battery backup service by altering the terminal strip connections on the power supply. The illustration shows the slots which are protected for various terminal strip connections. It is good practice to protect only those slots containing MOS memory boards and the microNOVA CPU, to minimize current drain and overheating (the cooling fans do not operate during battery operation).

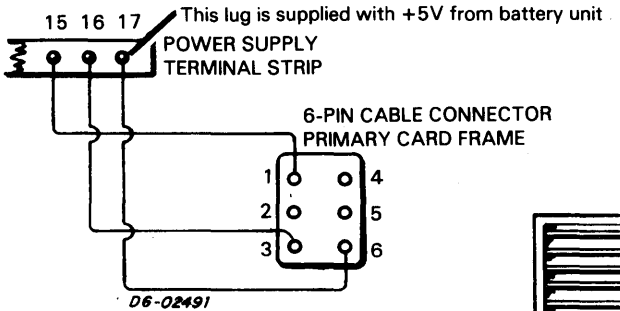
BATTERY BACKUP UNIT



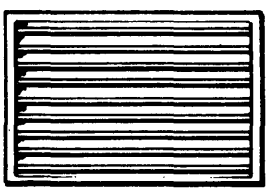
BATTERY BACKUP MOUNT



CABLE CONNECTIONS FOR ADDITIONAL BATTERY PROTECTION



STANDARD CABLING CONNECTION

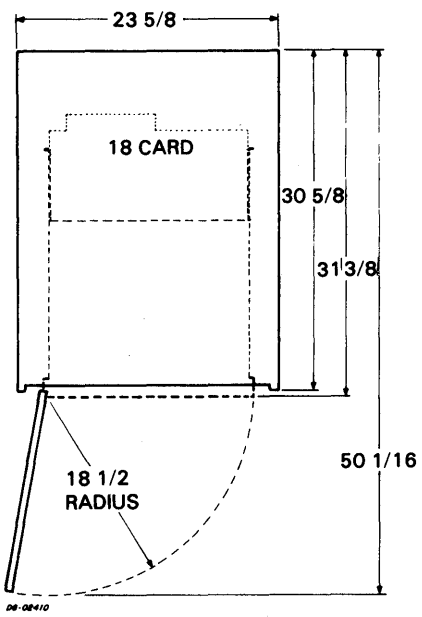


CARDFRAME SLOTS PROTECTED

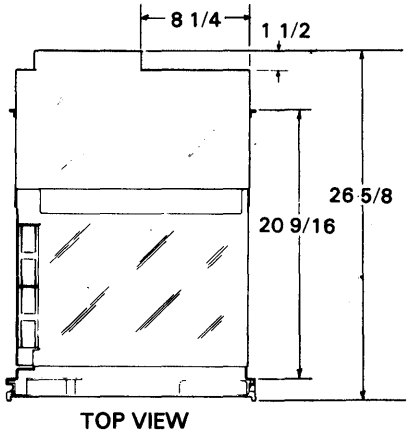
NOTE: Maximum Current at Lug 17 is 10A.

CHASSIS DIMENSIONS

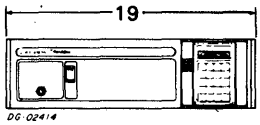
18-SLOT CHASSIS



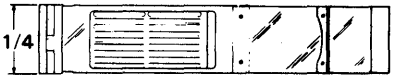
MINIMUM SERVICE CLEARANCE DIMENSIONS



TOP VIEW

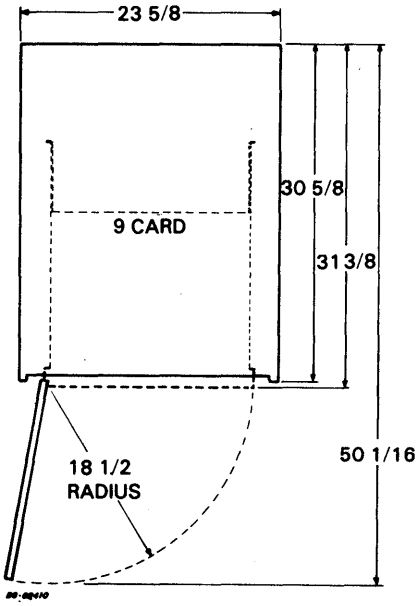


FRONT VIEW

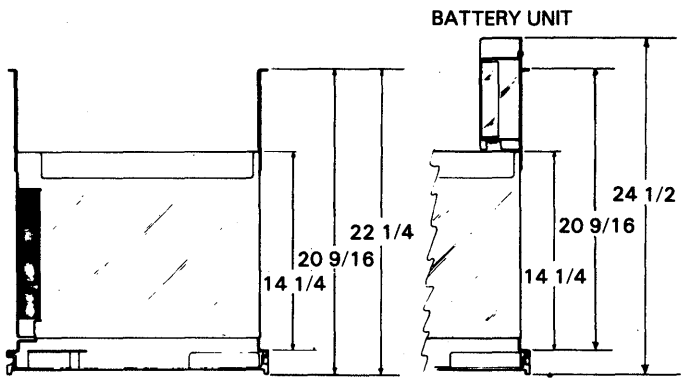


SIDE VIEW

9-SLOT CHASSIS



MINIMUM SERVICE CLEARANCE DIMENSIONS



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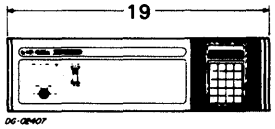

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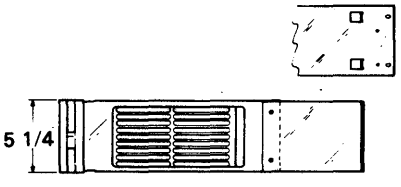

SIDE VIEW

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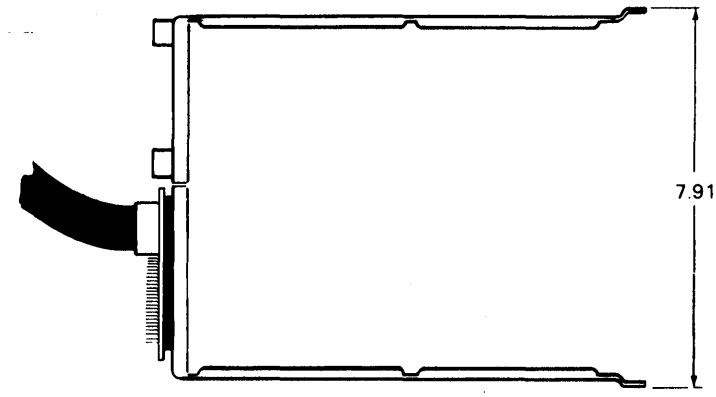

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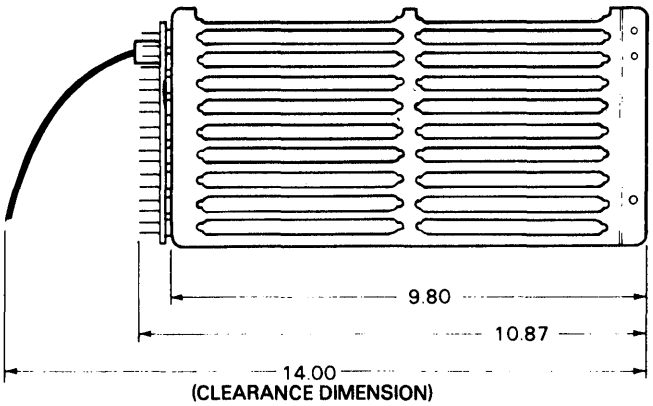

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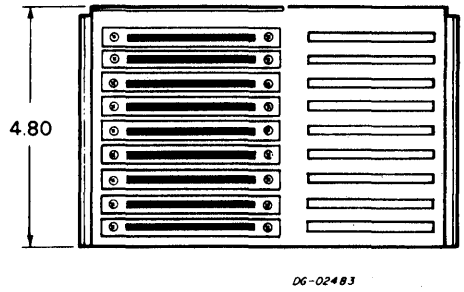
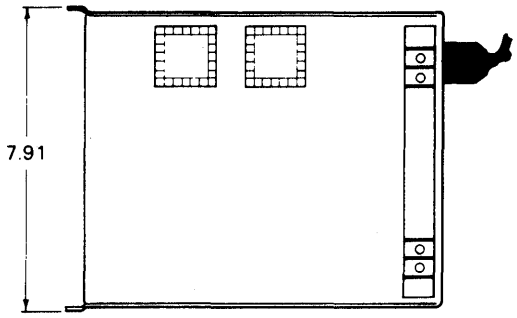


FRONT VIEW

POWER SUPPLY



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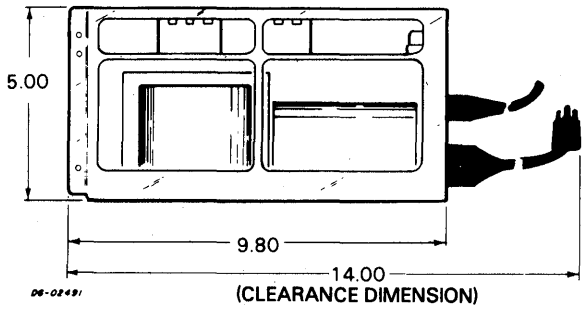

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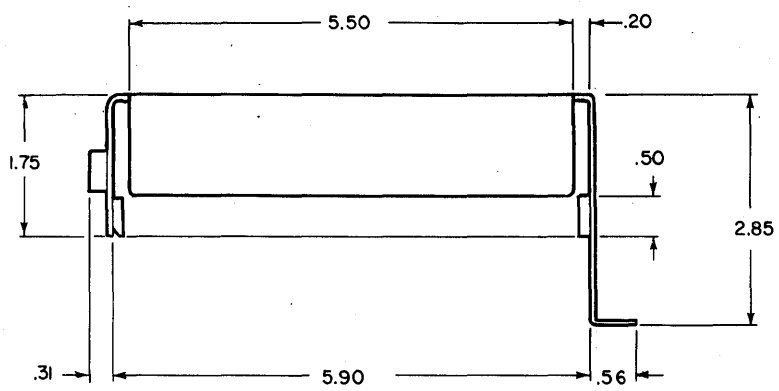
BATTERY BRACKET



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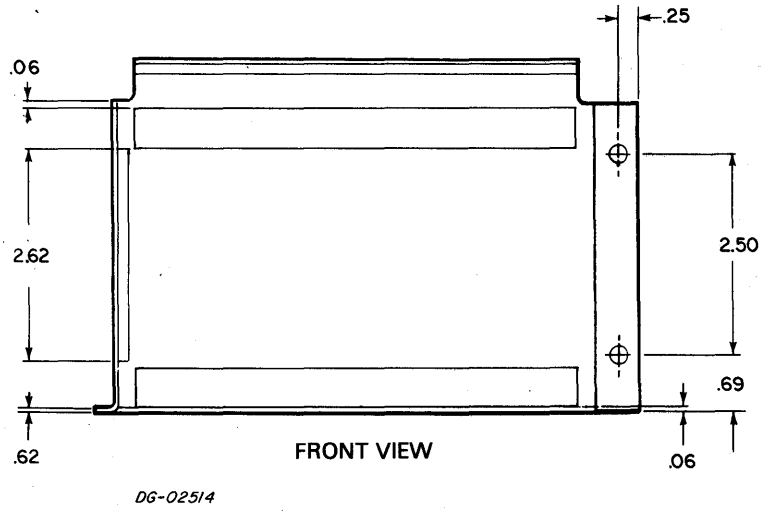

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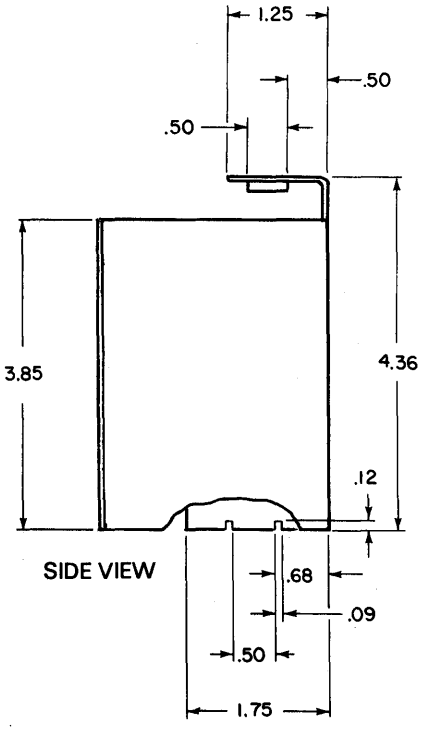

SIDE VIEW

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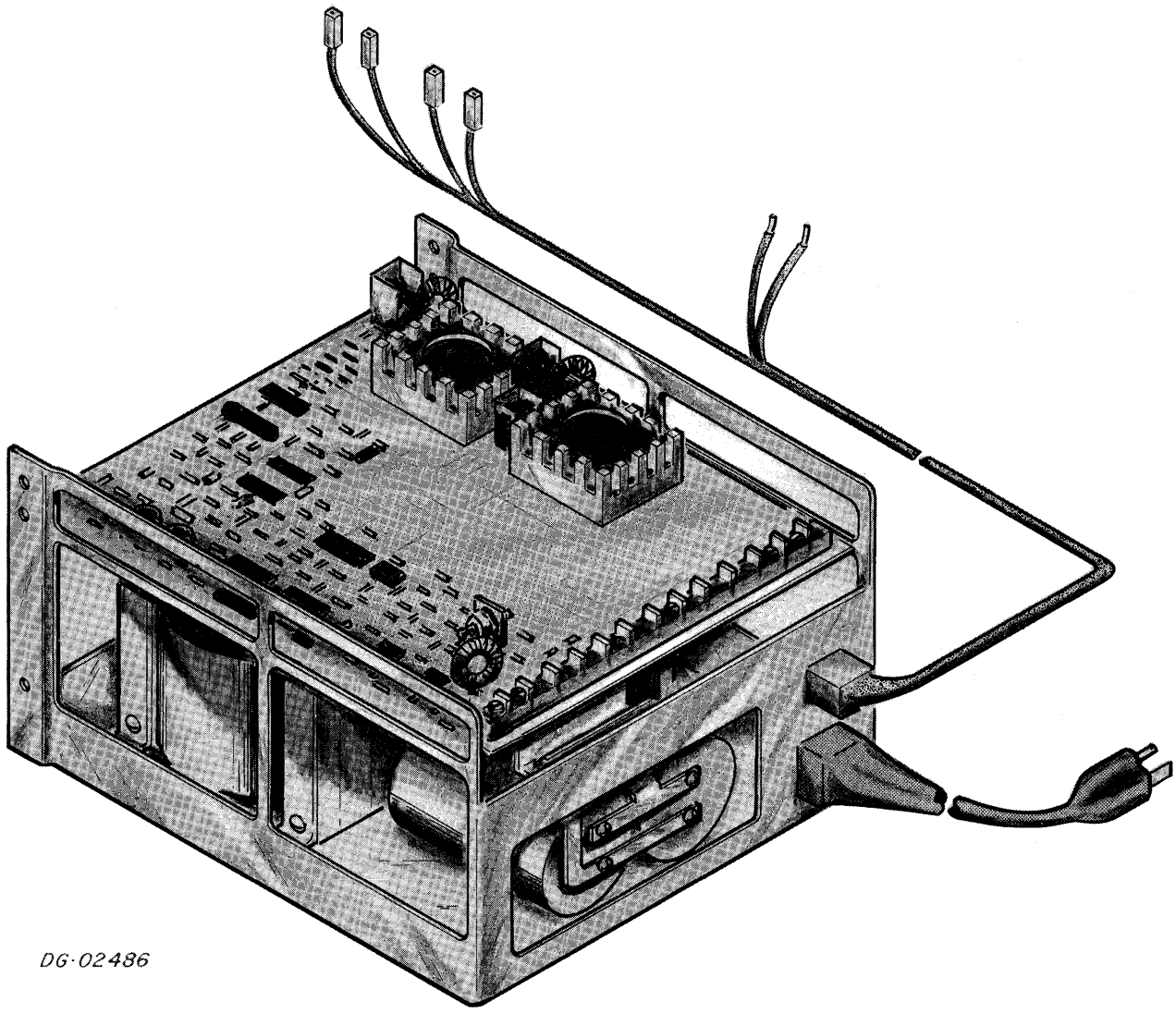

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SECTION XII
POWER SUPPLY ASSEMBLIES

The model 4213 power supply provides 18 amps @ +5VDC (± 4.4%), 2.5 amps @ 15 VDC (±1.6%), and 1.2 amps @ -5VDC (±2.8%). Low voltage switching regulators control all three; both the +5V and the +15V portions by independant pulse width modulation, the -5V portion by variable pulse rate generation. Line voltages of 100, 120, 220, and 240 volts, in the frequency range of 47-63 HZ, are accomodated using transformer taps. Line filtering, overvoltage sensing, independent overcurrent sensing for each output voltage, a power-up sequence, and a 4-way power-fail monitor provide system protection. The model 4214 power supply provides the same outputs but includes a battery charger and a backup battery pack. The battery pack contains two 12V lead-acid batteries connected in series having a capacity of 2.5 amp-hours. An AC line cord and the wiring harness for the microNOVA computer chassis are supplied.

OVERVIEW AND INTRODUCTION

Power supplies in microprocessor systems must be able to maintain regulation under rapidly varying loads, adequately protect their loads from overcurrents and overvoltages, supply a number of DC voltages, typically +5Vdc, -5Vdc, and +15Vdc, and work from the many different AC lines commonly found around the world.

One of the more accurate and efficient ways of regulating a DC voltage in the face of line and load variations is accomplished with a controlled switching regulator. The switching regulators used for two of the voltages (+5V and +15V) in both power supplies are controlled using the pulse width modulating technique (PWM). Regulation is accomplished by changing the duty cycle (on-time divided by the period x 100%) of a fixed period switched DC voltage to compensate for changes in either the input voltage or the output load. The output voltage is maintained constant by varying the duty cycle; increasing the duty cycle increases the output current; decreasing the duty cycle decreases the output current while maintaining the desired output voltage.

The switching regulator used for the third power supply voltage (-5V) is controlled using a variable pulse rate generator. Regulation is accomplished by changing the repetition rate of a pulse of constant width pulsed DC voltage to compensate for changes in either the input voltage or the output load. The output voltage is proportional to the repetition rate; increasing the repetition rate increases (makes more negative) the output voltage; decreasing the repetition rate decreases (makes more positive) the output voltage.

Since the dynamic random access memories (RAMS) used in the microNOVA system lose their contents when deprived of power, the model 4214 power supply is offered with battery backup. The batteries are charged through a controlled rate charging circuit built as an integral part of the power supply.

SUMMARY OF CHARACTERISTICS

AC INPUT:	89-114/102-132/195-251/213-275Vac 47-63Hz
+5Vdc OUTPUT:	Max Load - 18A Line Reg - <.4% Load Reg - <.8% from .25 to 18A Ripple - <240mV p-p to full load (excluding transients <10μs.)
+15Vdc OUTPUT:	Max Load - 2.5A Line Reg - <.2% Load Reg - <1.3% from 0 to 2.5A Ripple - 60mV p-p to full load (excluding transients <10μs.)
-5Vdc OUTPUT	Max Load - 1.2A Line Reg - <.8% Load Reg - <1% change from .1A to 1.2A load Ripple - <100mV p-p to full load (excluding transients <10μs.)
SHORT CIRCUIT PROTECTION:	Fuses on +5v Current limiting on all voltages
OVERVOLTAGE PROTECTION:	Trip Point (+ 5Vdc) - 5.7±.5Vdc Trip Point (+15Vdc) 17.2±.5Vdc Crowbar Blows VNR Fuse On Either Trip Point
UNDERVOLTAGE PROTECTION:	+15Vdc Disabled When -5Vdc Becomes More Positive Than -3±.2Vdc
BATTERY BACKUP:	Switch Over Points Power Down - 24± .5Vdc Power Up - 24.2± .5Vdc Switching Time ≤ 40 msec from last half cycle received Support Time 45 minutes at 25° C for CPU + 32K (8K Memories) Recharge Time 14-16 Hours From Full Discharge
EFFICIENCY:	70%
MAX OPR TEMPERATURE:	131 F/55 C
STORAGE TEMPERATURE:	-40° →+185° F/-40° →+85° C
WEIGHT:	16lbs/7.3Kg without Battery
DIMENSIONS	5.0"/12.7cm-h 7.94"/20.1cm-w 10.5"/26.7cm-d

BLOCK DIAGRAM

The block diagram on the opposite page provides a simplified representation of the operation of the power supply. The supply can be divided into seven major areas for purposes of discussion. These areas are: AC to unregulated DC conversion, reference voltage generation, +5V regulation, +15V regulation, -5V regulation, power-fail detection, and battery backup implementation. A general discussion of the operation of each of these areas follows.

AC to DC Conversion

Straightforward AC to DC conversion is accomplished using a step down transformer , a full-wave bridge rectifier, and a large smoothing capacitance. An AC line filter and 2 AC fuses are provided between the line cord and the transformer. The line cord selects the various taps on the transformer, determined by the type of line cord, allowing the use of a wide variety of main power sources. The output from this section of the power supply is a +30V unregulated power bus. Excessive voltage on either the +5VDC or the +15VDC outputs is detected by a protection circuit which removes the unregulated DC voltage from the rest of the supply. Power removal is effected by the triggering of a silicon controlled rectifier which blows the fuse for the +30V power bus.

Reference Voltage Generation

Reference voltages for controlling the three regulators and the power-fail detection circuitry are generated from the unregulated power bus using various zener diodes. This same network is also used to supply the voltages needed by the various logic elements controlling the regulators.

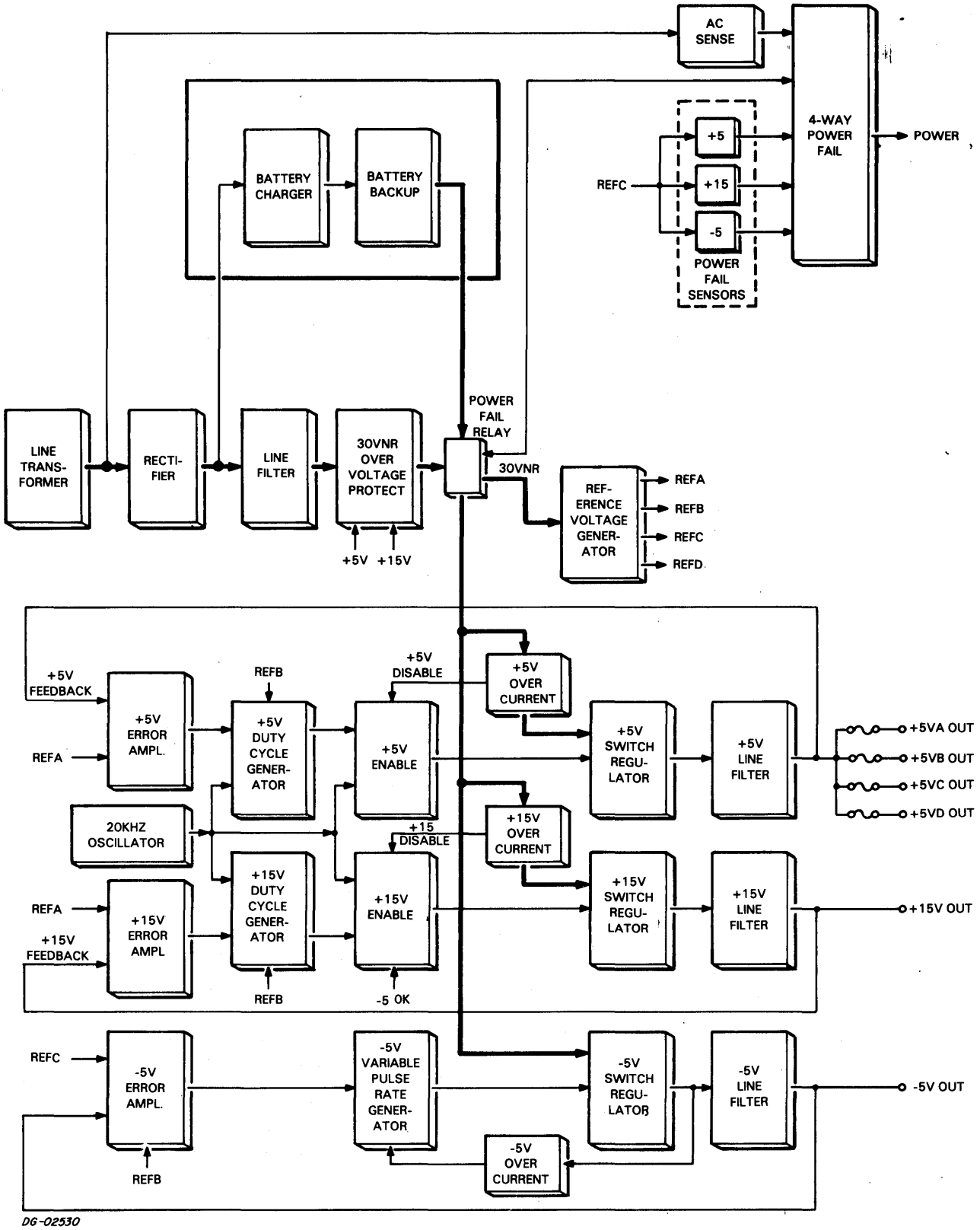
+5V Regulation

The +5V portion of the power supply contains a switching regulator which is controlled by the pulse width modulation technique. This technique is advantageous since the electrical noise generated during current switcing will have a characteristic frequency which can be more easily controlled, resulting in more predictable response characteristics.

The regulation is obtained as follows: the unregulated DC power bus is switched through a power transistor to an LC output filter. This filtered output is fed back to an error amplifier which compares the output voltage with a reference voltage. The amplifier, in conjunction with a 20khz oscillator, determines the duty cycle of the power switching transistor. Since the output voltage is proportional to the duty cycle, the control must increase the duty cycle when the output voltage is too low, and decrease the duty cycle when the output voltage is too high. The waveform of the 20khz oscillator determines the duty cycle range of the regulator. The range is always kept between 50 and 67%. The 20khz waveform, together with the error amplifier signal, forces the power transistor to assume the necessary on-time during the 20khz period for proper regulation.

An overcurrent protection circuit senses the peak current from the unregulated power bus flowing into the power transistor. If the current is excessive, a disable signal is generated, turning off the regulator's power transistor. This use of a peak current detector during every cycle provides a constant current, decreasing voltage curve as seen by the load.

microNOVA POWER SUPPLY



+15V Regulation

The regulation of the +15V portion of the power supply is also accomplished with a pulse width modulated switching regulator. This regulator operates in a similar manner to the that on the +5V portion of the supply, and, in fact, shares the 20khz oscillator with that supply. Overcurrent protection is accomplished as in the +5V supply.

Since damage could occur to some of the integrated circuits used in the microNOVA system if the +15V supply is applied before the -5V supply, the +15V output is disabled whenever the -5V output is more positive than -3V.

-5V Regulation

The -5V portion of the power supply contains a switching regulator which is controlled using the constant width, variable rate pulse technique. This technique has the advantage of producing a constant power output.

The -5V is obtained from the unregulated power bus by using a coil in the "flyback" mode; i.e., when the coil is charged with a positive voltage and that voltage is removed, the coil reverses polarity (flys back) and a negative voltage is produced.

The regulation is obtained as follows: the unregulated power bus is switched through a power transistor to the flyback coil and output filter. The filtered output is fed back to an error amplifier which compares the output voltage to a reference voltage. The output of this error amplifier triggers the constant width pulse generator. This constant width pulse is used to control the switching of the power transistor. If the output voltage is found to be too low (in this case, too negative) compared to the reference voltage, the pulse repetition rate is decreased. If the output voltage is too high compared to the reference voltage, the repetition rate is increased.

An overcurrent protection circuit senses the current flow from the supply. If the current is excessive, the pulse generator is disabled.

Power-fail Detection

The power-fail detection network samples 4 voltages in the power supply: AC line voltage, +5V, +15V, and -5V. If any of these voltages drop below their specified values, a power-fail signal is transmitted to the rest of the microNOVA system. In the case of the AC line voltage dropping, the battery backup portion of the 4214 power supply is cut into the system.

Battery Backup Implementation

The battery backup package in the model 4214 power supply is charged through one portion of the power supply. A variable rate, constant width pulse generator switches the +15V output through a step up transformer to the 24V battery pack. As long as the AC line voltage is present, the battery pack is being charged. If the line voltage drops, the power-fail monitor energizes a relay which switches the battery voltage to the unregulated power bus. The battery will supply power to the power supply until its voltage drops below 19V. This drop in voltage will occur after 2.3 ampere-hours of energy has been drawn from the battery. Battery recharge, for a totally depleted battery pack, requires 16 hours.

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