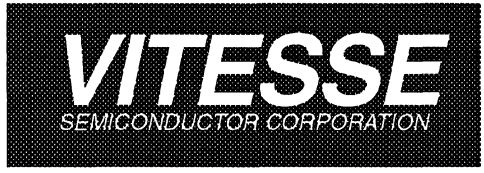
VITESSE

1996 Communications Products Data Book

Communications Products

VITESSE
SEMICONDUCTOR CORPORATION



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G54010-0-0594 3M
August 1996

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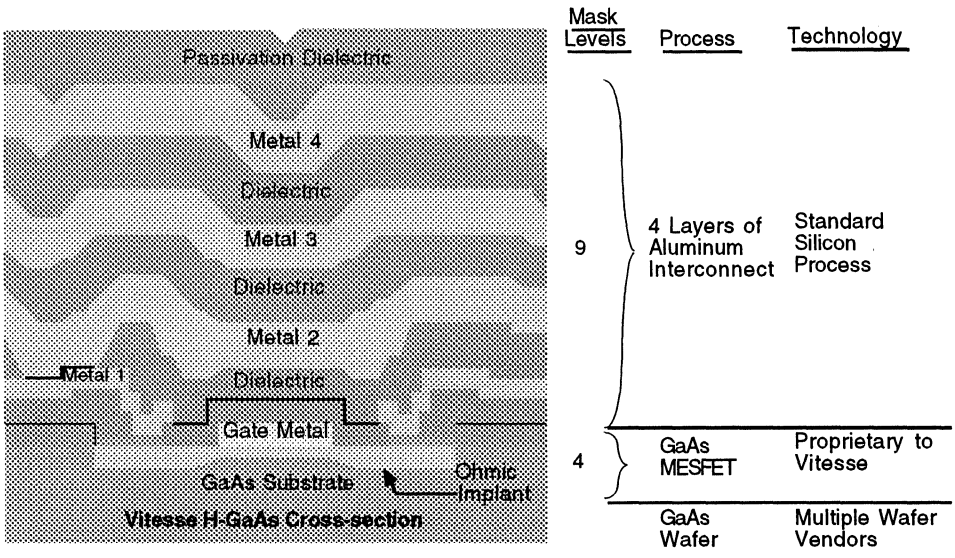

This 1996 Communications Product Data Book contains the latest information on the entire range of communications products and services from Vitesse Semiconductor Corporation. We are pleased to present you with this compilation of information in one convenient source. This book includes complete product data sheets and product previews for Vitesse communication devices. Supplementary information regarding packaging and applications is also included.

Vitesse Semiconductor Corporation is a proven leader in the design and manufacture of high performance, mixed signal, digital LSI and VLSI GaAs ICs. The company, which was founded in 1984, has developed a revolutionary process, allowing it to deliver affordable, very large scale (VLSI) gallium arsenide (GaAs) ICs.

The key to success for Vitesse has been the development of mixed signal devices and the unique H-GaAs manufacturing technology. Rather than developing a process based on existing GaAs microwave transistor technology, Vitesse chose to develop an entirely new process based on proven silicon MOS manufacturing methods. This strategy solved two major problems which had prevented GaAs ICs from receiving wide acceptance: low complexity and high cost. The result is a high yielding, proprietary process which produces circuits with a speed-power product unmatched by any other IC manufacturing technology.

The markets for Vitesse's products include applications such as computers, communications, automated test equipment, instrumentation, and general military/aerospace. In order to compete in these markets, Vitesse chose to make its products look and feel exactly like silicon products, but with significant improvements in speed, complexity, and reduced power dissipation. The combination of GaAs performance and silicon MOS manufacturing techniques is the key Vitesse advantage. The results are families of IC products that set new performance standards at prices competitive with high performance silicon products.

Vitesse is committed to providing the highest performance integrated circuits in the world. The Vitesse manufacturing process has been designed to realize this objective with a combination of process innovations

and proven MOS manufacturing techniques. The distinguishing features of the Vitesse process are: 1) excellent transistor electrical parameter control, 2) unprecedented manufacturing yields on VLSI complexity GaAs circuits, and 3) process simplicity and fast cycle time.

Vitesse has pioneered the now well-accepted concept of designing GaAs products that are compatible with existing silicon technologies. Input/output levels and power supplies found in TTL, ECL and CMOS are standard in the entire family of Vitesse products.

Datacommunications

In 1992 Vitesse introduced the G-TAXI chipset, the first generation general purpose serial link for both Fibre Channel and proprietary protocols at baud rates up to 1.25 Gb/s. This first generation chipset included a 32/40 bit TTL system interface bus, ANSI 8B/10B encoding and decoding, and completely integrated on-chip PLL clock generation and clock and data recovery circuitry.

In 1993 the second generation Fibre Channel products were introduced. The +3.3 volt supply VSC7105 and VSC7106 transmitter and receiver chipset and the VSC7107 CMOS encoder/decoder offered the functionality of the G-TAXI chipset at one half the power.

In 1995 Vitesse minimizes power in Fibre Channel designs with the introduction of the VSC7125 Fibre Channel Transceiver. Constructed using the H-GaAs IV process, this device is a single chip fully integrated Fibre Channel transceiver designed for high volume applications. The VSC7125 is the product of extensive experience in high speed PLL based clock generation, and clock and data recovery, coupled with the exceptional speed-power capabilities of the Vitesse H-GaAs IV process. In three generations, Vitesse has lowered the power required for the transmitter and receiver functions from 6.5 W to 650 mW, and package requirements from two ceramic packages to a single 10 mm PQFP.

Telecommunications

Vitesse's VS8000 family of telecommunications ICs address the needs of the newest generation of telecommunications systems incorporating data rates up to 10 Gb/s. These standard multiplexer/demultiplexer chipsets are suitable for proprietary or Synchronous Optical Network (SONET) STS-3 through STS-192 applications and are available in 4, 8 and 16 channel configurations. These products feature very low power dissipation and ECL compatibility.

In addition to the VS8000 family of multiplexer/demultiplexer chipsets, Vitesse offers a family of crosspoint switches which are ideal for high speed telecommunications data distribution, computer network and multiprocessor switching, video switching, and test equipment.

ASICs

Summary information on Vitesse ASIC products is included herein as well. Detailed specifications on Vitesse's complete line of ASICs are available in a separate ASIC Product Data Book. Contact your local Vitesse Sales office or Vitesse headquarters at (805) 388-3700 to obtain a copy of this data book.

Introduction

Document Designations

Product Preview

This is usually a one-page document describing a product to give customers a general idea of the product's functionality and use.

Target Specification

This document contains information about a proposed product during its design phase of development and is subject to change without notice at any time. All features and specifications are design goals only. Please contact Vitesse Semiconductor to obtain the latest product status and most recent version of this specification.

Advanced Product Information

This document contains information about a new product during its fabrication or early sampling phase of development. The information in this document is based on design targets, simulation results or early prototype test results. Characteristic data and other specifications are subject to change without notice.

Preliminary Data Sheet

This document contains information about a product during its preproduction phase of development. The information in this document is based on test results and initial product characterization. Characteristic data and other specifications are subject to change without notice

Data Sheet

This data sheet evolves from the Preliminary data sheet. It is a result of test information collected from fully characterized devices. This is a document used for a product which is mature enough to be considered "In Production". All specs are mature and verified by testing on multiple lots or product characterization.

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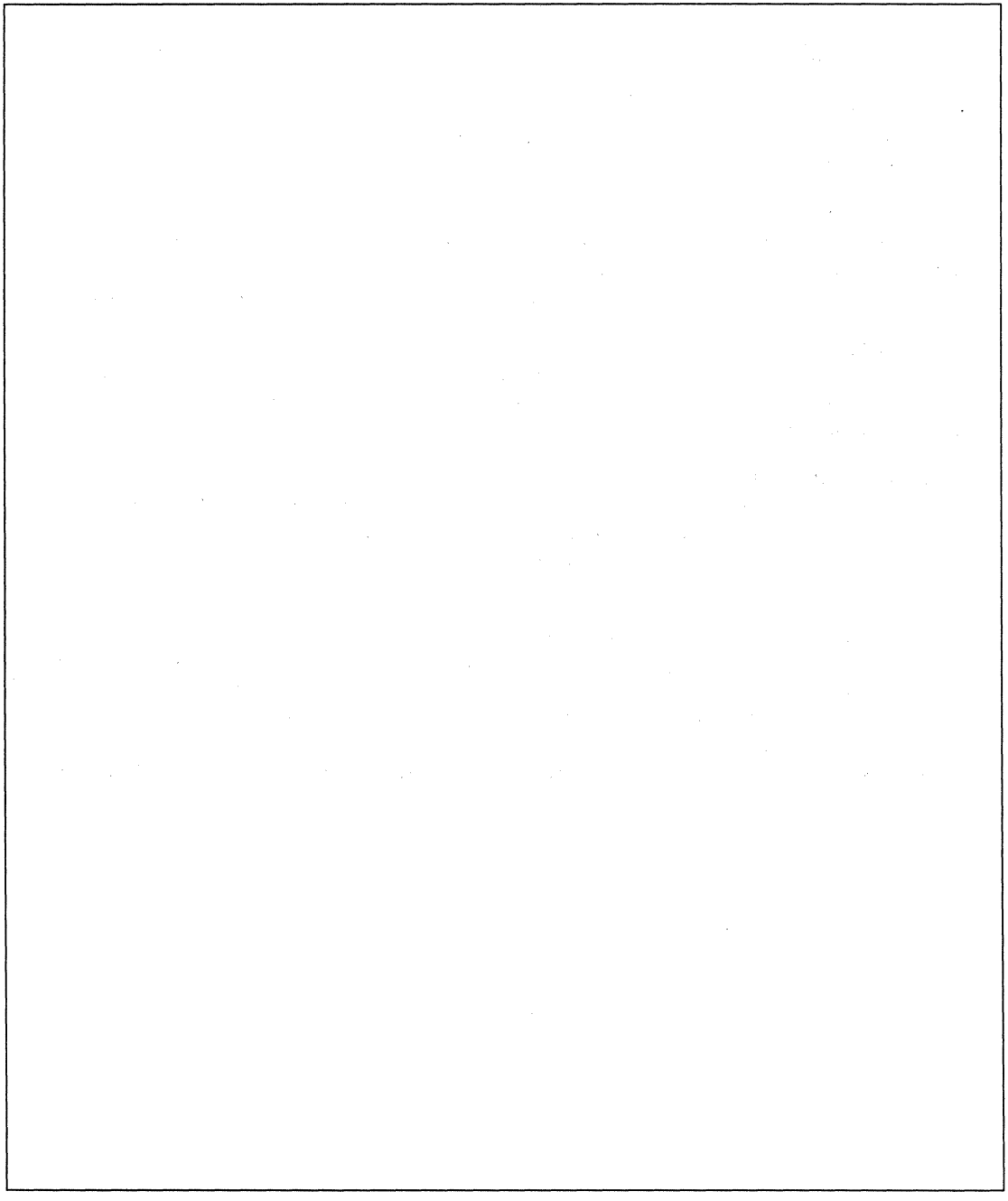
Introduction



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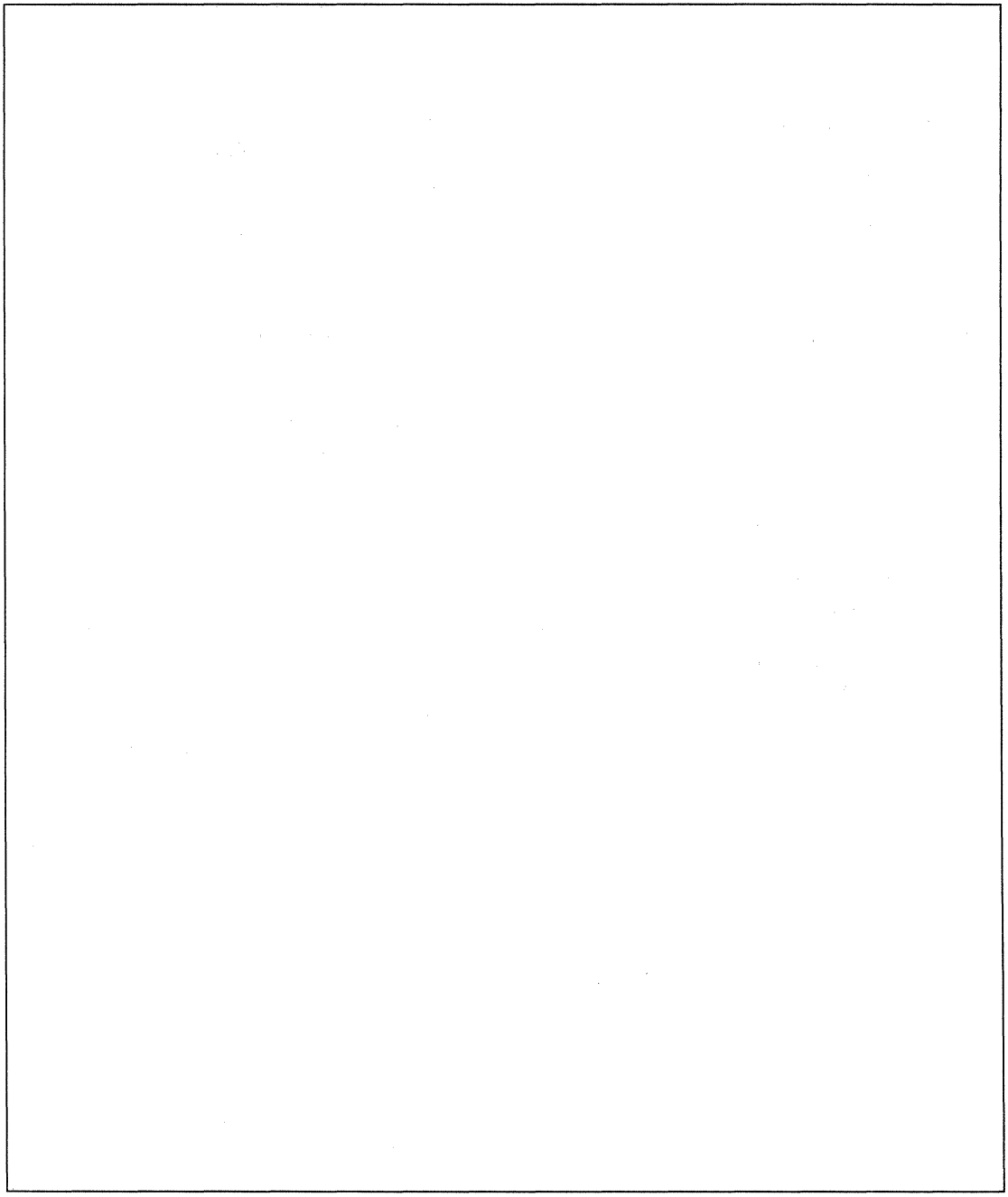
General Information



Product Summary

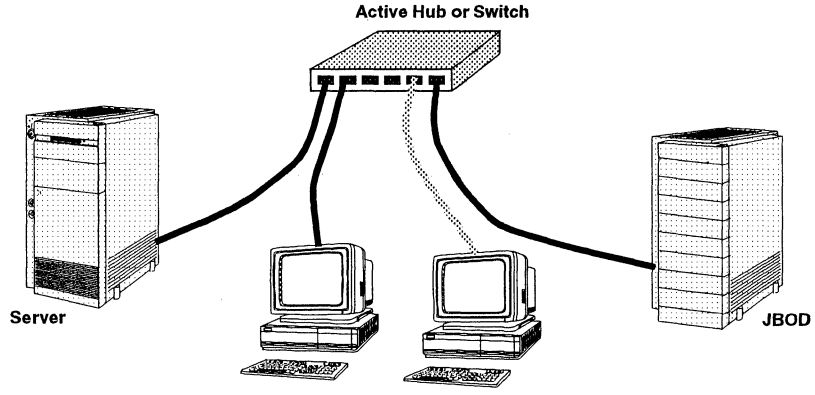
Product Family	Description	Features
VSC7105/7106	1.0625 Gbit/sec ANSI X3T11 compatible Fibre Channel transmitter and receiver chipset. Suitable for both copper and optical link applications.	**VSC7105** 1.0625 Gbit/sec Fibre Channel Transmitter Integrated PLL for Clock Multiplication **VSC7106** 1.0625 Gbit/sec Fibre Channel Receiver Integrated PLL-Based Clock Recovery Unit **Both** 106MHz Reference Clock Selectable 10-bit or 20-bit TTL Parallel Data Interface Single 3.3V Supply
VSC7107	Fibre Channel ENDEC with FC-1 link functions and FC-2 framing assistance functions. Suitable for custom Fibre Channel links to sustain up to 200 MByte/sec duplex data communication.	8B/10B Encoding 32-Bit Synchronous FIFO Data Interface CRC Calculation and Checking Fibre Channel Ordered Sets Framing Assist with CMND Bus Automatic IDLE Generation Link Error Reporting
VSC7115/7116	1.0625 Gbit/sec ANSI X3T11 compatible Fibre Channel transmitter and receiver chipset. GLM compatible interface.	**VSC7115** 1.0625 Gbit/sec Fibre Channel Transmitter Integrated PLL for Clock Multiplication **VSC7116** 1.0625 Gbit/sec Fibre Channel Receiver Integrated PLL-Based Clock Recovery Unit **Both** 53 MHz Reference Clock 20-bit TTL Compatible Parallel Data Interface Single 3.3V Supply
VSC7120	1.0625 Gbit/sec Fibre Channel Repeater for use in disk arrays and FC-AL Hubs.	Integrated PLL-Based Clock Recovery Unit Embedded Port Bypass Circuit Signal Detect Unit for Invalid 8B/10B Characters and Oscillation Detection
VSC7121	Quad Port Bypass Circuit cascaded for use in Fibre Channel Arbitrated Loop disk arrays.	Up to 1.0625 Gbit/sec Operation Four Port Bypass Circuits Low Power Consumption Low Jitter Accumulation Cascadable for Larger Loops
VSC7125	1.0625 Gbit/sec ANSI X3T11 10-Bit Fibre Channel transceiver.	10-bit Study Group TTL Compatible Parallel Interface Integrated Clock Multiplier and Clock Recovery Unit. 106 MHz Reference Clock and Transmit Byte Clock Single 3.3V Supply 650 mW Power
VSC7126	1.0625 Gbit/sec ANSI 20-bit Fibre Channel Transceiver.	GLM Compatible Single Chip Transceiver 53 MHz Reference Clock Single 3.3V Supply 750 mW Power

Product Summary

Product Family	Description	Features
VSC7135	1.25 Gbit/sec Transceiver for Gigabit Ethernet.	Single Chip Transceiver 125 MHz Reference Clock Single 3.3V Supply 780 mW Power
VSC7181	1.0625 Gbit/sec ANSI X3T11 and FCSI GLM compliant copper gigabaud link module.	1.0625 Gbit/sec Copper GLM Daughtercard ANSI Standard 9-pin D-Shell Serial Connector 20-bit TTL Compatible Parallel Interface 80-pin Samtec Parallel Connector Single 5V Supply
VSC7181EV	1.0625 Gbit/sec Fibre Channel Copper Gigabaud Link Module Evaluation Kit.	Easy to Use Kit Containing: Two (2) VSC7181 CuGLM One (1) 5m Gore Fibre Channel Duplex Cable Assembly with DB-9 Connector One (1) Female Loopback Adaptor One (1) Male Loopback Adaptor
VSC7201A	1 GByte/Sec SCI Compliant Link Controller.	Conforms to IEEE SCI Standards: IEEE Standard 1596-1992 Sends and Receives SCI Data in 2ns for 1GByte/s Data Rate High Speed Link Interface Conforms to Low Voltage Differential I/O Standard (IEEE P1596.3) 64-bit Bi-Directional GTL System Interface +3.3V and +2V Power Supplies Required 269 Tape Ball Grid Array Package (TBGA - 50 mil centers) IEEE Std 1149.1 Test Access Port for Diagnostics
VSC7203	1 GByte/s SCI Compliant Switch Node Bypass Circuit.	2-port Switch Capable of Passing SCI Packets Multiplexers Allow Bypassing Around any Port for Faulty Node Isolation Sends and Receives SCI Symbols every 2ns for 1 GByte/s Data Rate per Port +3.3V and +2V Power Supplies 301 BGA Package (50 mil spacing, 27mm/side) IEEE Std 1149.1 Test Access Port for Diagnostic and Boundary Scan
VSC7802 VSC7805 VSC7810	Fibre Channel short-wave optical detectors with integrated transimpedance amplifiers.	Three Products Supporting 266, 531, and 1063 Mbit/sec Data Rates. 770 - 850nm Detectors Integrated AGC

Fibre Channel Overview

FIBRE CHANNEL COMPUTE CLUSTER



Fibre Channel is an emerging standard for high speed, serial data communication developed by the ANSI X3T11 Technical Committee consisting of a wide breadth of the electronics industry including representatives from optical components, electrical connectors, semiconductor components, disk drive, computer systems, and network systems companies.

Fibre Channel's heritage draws from the experience of the SCSI, ESCON, HIPPI, and FDDI standards community as all were part of the original ANSI X3T9 Technical Committee. Fibre Channel provides a unifying networked, high performance I/O channel by which SCSI, IP, ESCON, and other protocols may be mapped into one interconnect to tie together supercomputers, mainframes, servers, workstations, and peripherals.

Fibre Channel is a layered transport protocol. It incorporates a physical layer transport definition (FC-0 and FC-1) and a framing and flow control definition (FC-2) with a common services layer (FC-3) and an upper layer for multi-protocol mapping onto Fibre Channel (FC-4). Refer to Fibre Channel Layers diagram.

Fibre Channel's strengths are many. Two unique strengths that differentiates Fibre Channel from other serial interconnects lies in its robust physical layer (FC-0 and FC-1) and it's support of a low-cost, arbitrated loop topology (FC-AL).

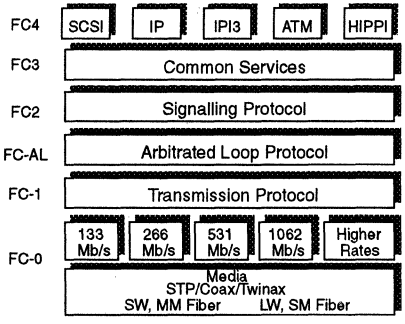
Fibre Channel's robust physical layer is based on the use of serial, point to point connections and the use of the 8B/10B encoding scheme developed and patented by IBM and licensed for use by Fibre Channel developers.

Serial, point to point links minimizes the transmission line problems and clock to data skew issues associated with data transfers over multi-drop busses at high data rates.

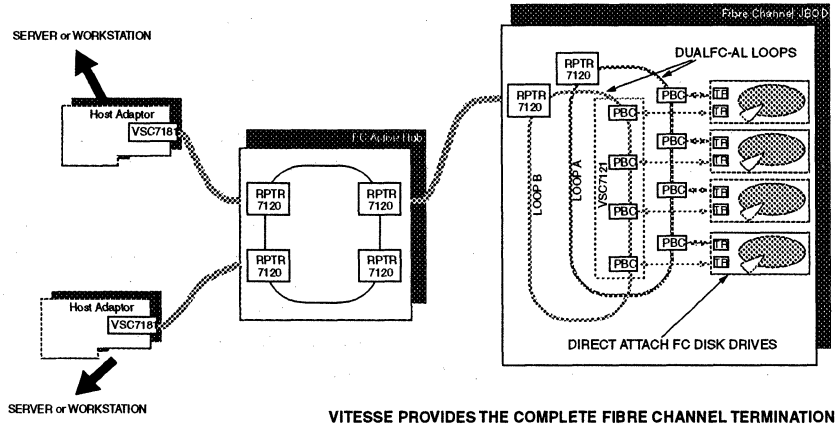
The 8B/10B encoding is a dc-balanced, run-length limited code which simplifies and cost-reduces Gbit/sec serial links with only a 20% encoding overhead. The dc-balanced code provides greater noise margins on copper links by minimizing the effects of baseline wander. The run-length limited code constrains the spectral content on the data link. This minimizes issues such as intersymbol interference and line coupling with capacitors or transformers, thus simplifying line fault detection to a digital rather than an analog problem.

Fibre Channel Overview

FIBRE CHANNEL LAYERS



FIBRE CHANNEL ARBITRATED LOOP NETWORK
PHYSICAL LAYER BLOCK DIAGRAM



VITESSE PROVIDES THE COMPLETE FIBRE CHANNEL TERMINATION

Because of these physical link attributes, Fibre Channel data transfer at 1 Gbit/sec is simpler, more reliable, with a bit error rate less than 10^{-12}, and lower in cost than other serial interconnects.

Fibre Channel's Arbitrated Loop topology retains the cost-effectiveness and user-friendliness of a multi-drop bus interconnect like ethernet and SCSI. Data rates of 1 Gbit/sec and above are permitted on copper cables over moderate distances (50meters) and on optical cables over long distance (10km). Most importantly, FC-AL does not require expensive switches and may use simple active hubs instead for reliable connectivity.

These attributes of Fibre Channel coupled with its reliable transport and flow control protocol (FC-2) and its flexible upper-layer protocol mapping (FC-4) has prompted Fibre Channel's adoption as a storage peripheral

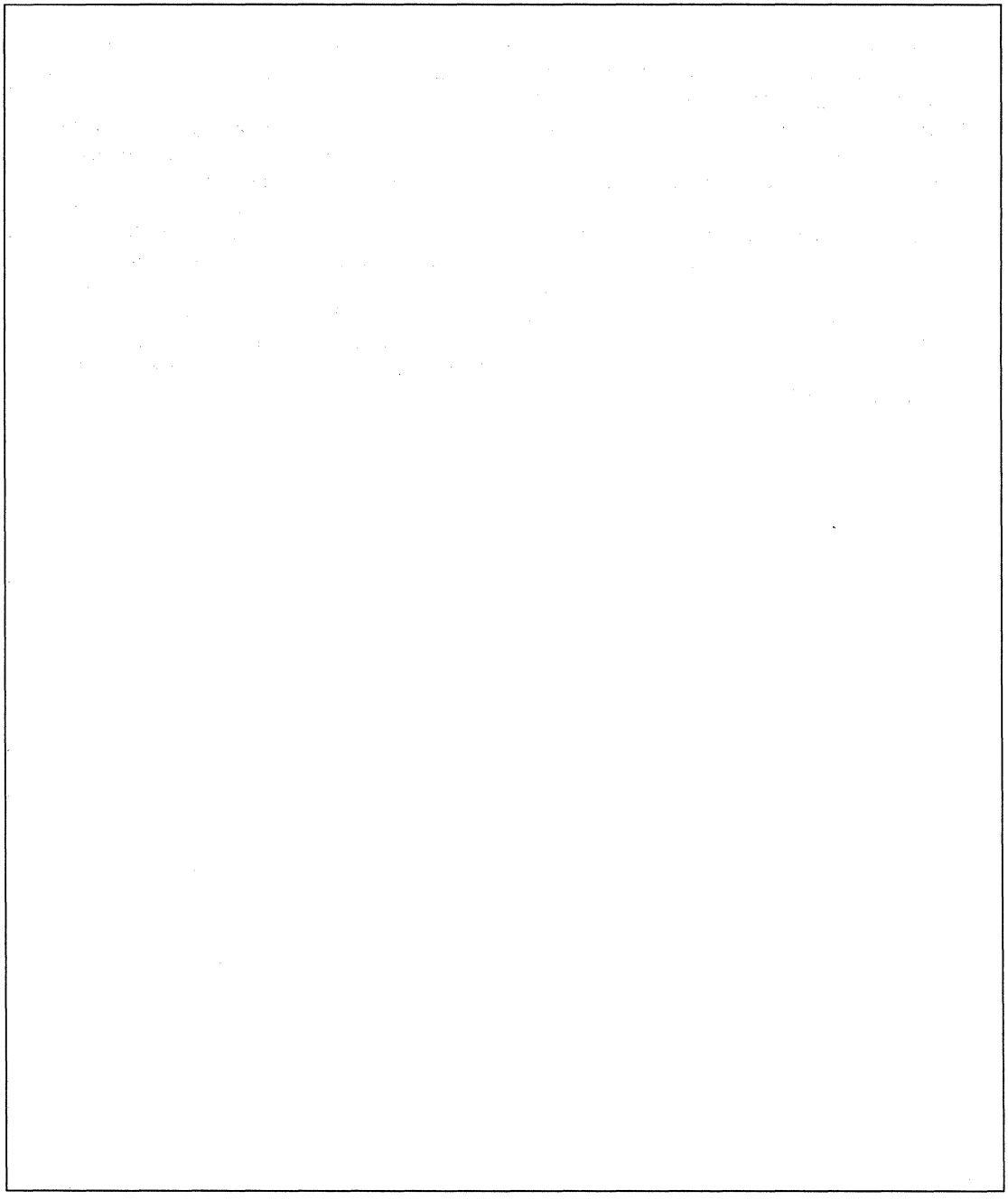
Fibre Channel Overview

interconnect not only as a connection between RAID (Redundant Array of Independent Disks) and servers, but also on individual disk drives with embedded RAID which increases performance and capacity of RAID and JBOD (Just a Bunch Of Disks) systems. High performance peripherals interconnected to servers and clients through 1 Gbit/sec Fibre Channel provide scalable, fault tolerant compute clusters and legacy LAN performance is enhanced through the use of Fibre Channel's Gbit/sec reliable transmission for a network backbone. High speed, remote data acquisition for imaging is made possible with Fibre Channel as well.

Vitesse Semiconductor has developed the most complete physical layer product offering through a family of industry compliant Fibre Channel transmitters and receivers along with Gbit/sec repeaters and bypass circuits. A physical layer block diagram, of an Arbitrated Loop cluster of Fibre Channel disk drives in a JBOD, interconnected to workstations with an active hub, is shown on the previous page. Additionally, Vitesse is working with the ANSI technical committee to ensure reliability and interoperability of GBit/sec interconnects.

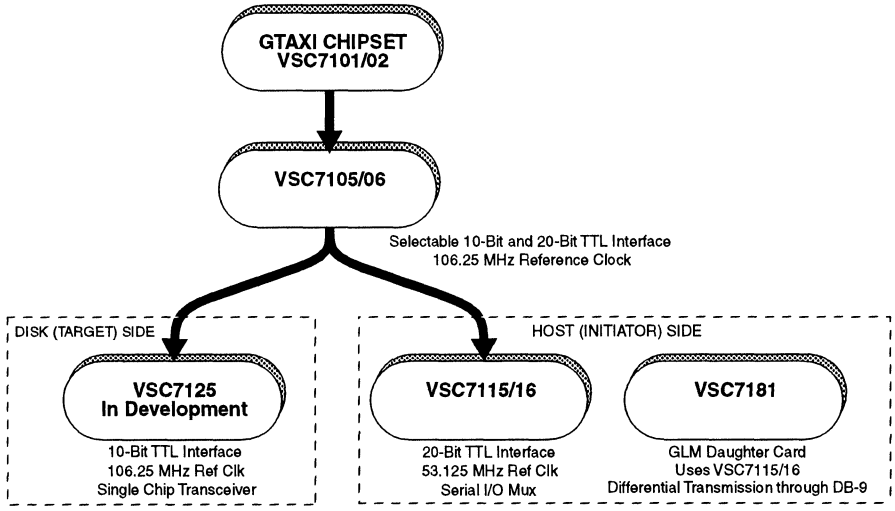
Vitesse also offers protocol products enabling the construction of custom Fibre Channel ports for such custom applications as data acquisition, RAID controllers, network backbones, and print server controllers. These products are summarized in the Product Summary.

Fibre Channel Overview



Transmitter/Receiver Overview

Fibre Channel Generations



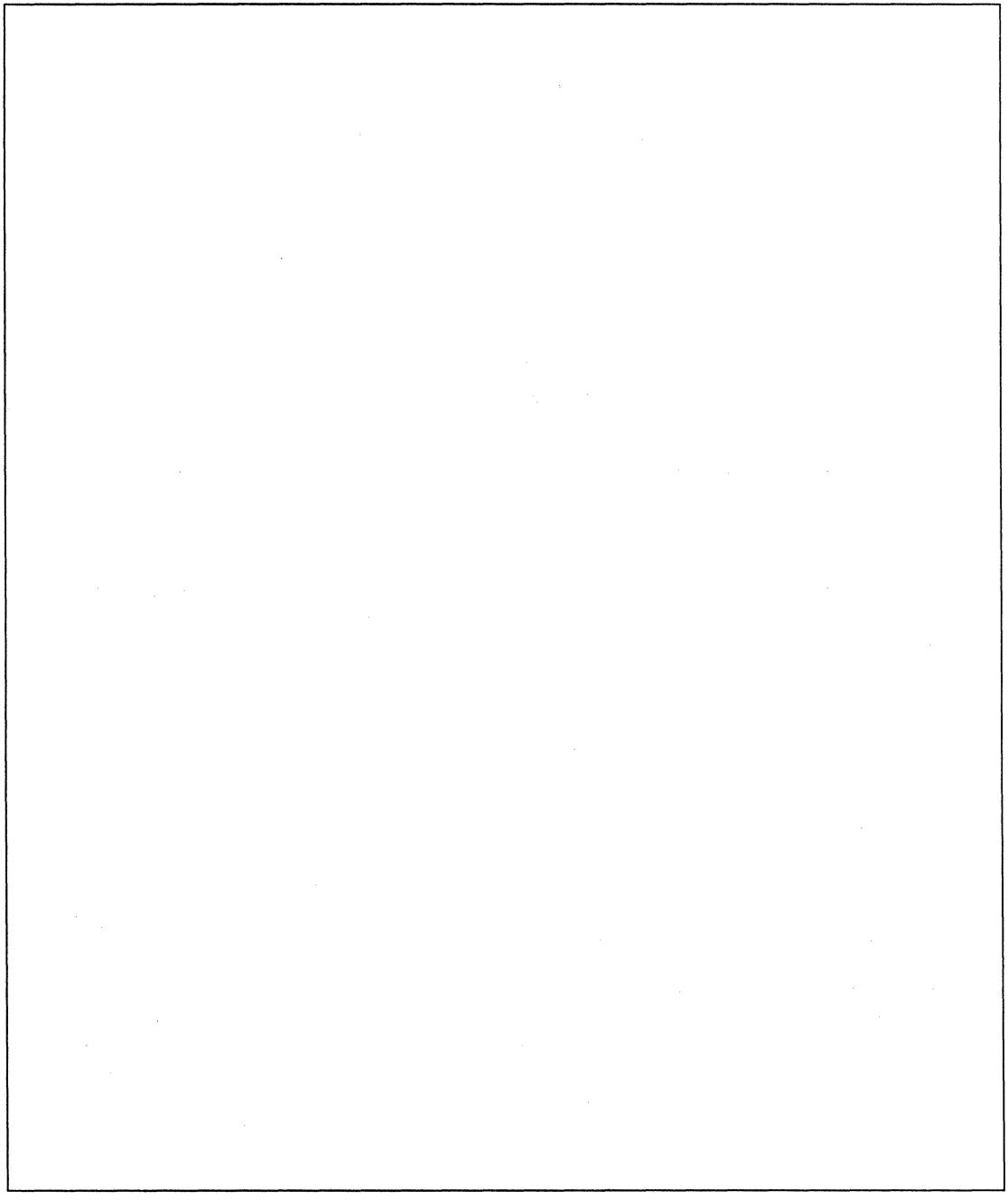
Fibre Channel transmitters and receivers implements the ANSI X3T11 Fibre Channel FC-0 layer minus the media and the optical drivers. These circuits are also referred to as Serializers and Deserializers respectively or SERDES collectively. SERDES more accurately describes the chip's function as they perform the task of serializing from and deserializing to parallel data for serial transmission.

Vitesse Semiconductor was the first to produce 1.0625 Gbit/sec transmitters and receivers predating industry standardization and our products have evolved with the Fibre Channel industry. This is why Vitesse has several similar products.

Two industry standardization efforts are significant. The first is the Gigabaud Link Module (GLM) profile established by Hewlett Packard, IBM, and Sun Microsystems as one of the profiles produced by the Fibre Channel Systems Initiative. The GLM specification's intent was to specify interchangeable daughtercard "modules" which contain all the high frequency circuits and board layouts. This will simplify the FC port design to a 53MHz TTL design and permit user speed and media selectability while ensuring multiple sources. Thus the GLM specification documents a 20-bit, 53MHz TTL timing interface as well as a physical definition. The GLM timing interface is reflected in the Vitesse VSC7115/16 product and the physical and electrical profile is implemented in the Vitesse VSC7181 product.

The second significant industry document is the 10-Bit Interface Specification which is a Technical Report published by the ANSI X3T11 Technical Committee. The driving force behind this effort is to define a lower pin count interface requested by the HDD (hard disk drive) industry due to the defacto standardization on dual-ported Fibre Channel disk drives. Reducing the I/O to 10-bit from 20-bit reduces a dual ported disk controller's pin count by 40 signals. This interface is implemented in the Vitesse VSC7125 product. Facets of the 10-Bit Interface Specification are taken from the VSC7105/06 product which predates both the GLM and 10-Bit Specification. diagram showing the Vitesse Transmitter and receiver product offering is shown above.

Transmitter/Receiver Overview



Data Sheet

1.0625 Gbit/sec Transmitter/Receiver Chipset for Fibre Channel or Proprietary Serial Links

Features

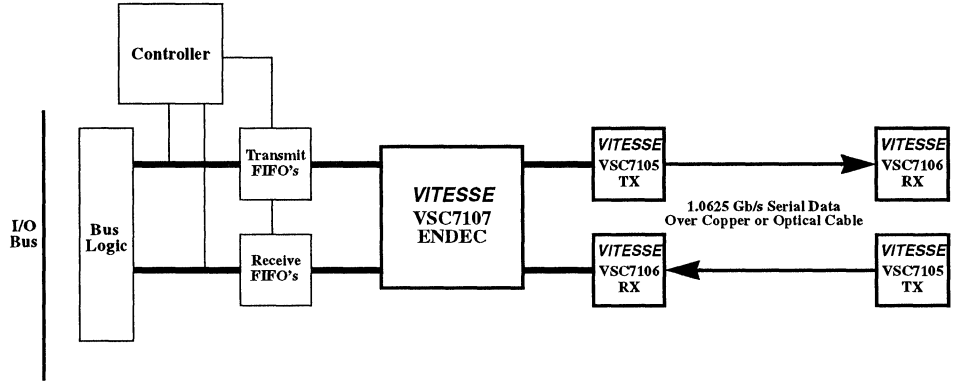
- ANSI X3T11 Fibre Channel Compatible at 1.0625 Gbit/s
- On-chip Fully Monolithic Clock Recovery and Clock Multiplication Circuits Require No External Components
- On Chip Clock Multiplication Relieves System of High Speed Clock Generation
- Single +3.3V Supply Operation
- Dual Receiver Serial Inputs and Transmitter Outputs for Loopback and Multiple Link Applications
- Selectable 10 or 20 bit TTL Compatible Parallel Interface
- High Sensitivity Differential Receiver Suitable for both Coaxial and Optical Link Applications

General Description

The VSC7105/VSC7106 chipset is compatible with the ANSI X3T11 Fibre Channel Standard. Fibre Channel is a high speed communication channel standardized by ANSI for mapping upper layer protocols (ULP) such as SCSI, IP, and HIPPI. Fibre Channel can then provide a channel over which concurrent communication of all ULP's may exist on a single interconnect between workstations, mainframes, and supercomputers, and for connection to mass storage devices and other peripherals. The Fibre Channel physical layer is also ideal for building cost effective, very high speed point-to-point communications links.

This chipset implements the Fibre Channel electrical transceiver physical layer for 1.0625 Gb/s operation. At 1.0625 Gb/s, Fibre Channel delivers 100 MByte/s of data bandwidth over a single cable. This bandwidth equals or exceeds most bus bandwidths. This chipset performs the high speed serialization and de-serialization function that makes bus-bandwidth, serial communication possible. This chipset can drive electrical cables directly or interface with optical modules.

System Block Diagram



VSC7105 Transmitter Functional Description

The VSC7105 is an ANSI X3T11 compatible Fibre Channel (FC) transmitter designed to work at the FC baud rate of 1.0625 Gb/s. The VSC7105 performs the serialization of parallel data and simplifies system design by performing clock multiplication from the parallel data clock. The VSC7105 has two modes of operation: 10-bit and 20-bit. The functional block diagrams for the 20-bit and 10-bit modes are shown in Figure 1 and Figure 2 respectively.

The VSC7105 accepts 8B/10B encoded TTL input data as one or two parallel 10 bit characters which are clocked into the device at 1/10 or 1/20 of the baud rate. User data should be encoded for transmission using the 8B/10B block code described in the Fibre Channel specification or any other equivalent coding scheme with a transition density of 40% or greater and a maximum run length of 6 consecutive 1's or 0's. The VSC7105 serializes the input data and transmits it at a baud rate of 10 times the frequency of the REFCLK input. The device includes a phase locked loop-based clock multiplier that generates the baud clock. This PLL is fully monolithic, and requires no external components.

The parallel input port timing is derived from the REFCLK input. REFCLK is internally divided by two, and driven off chip as complementary TTL outputs: TCLK and TCLKN. In 20-bit mode, the VSC7105 loads parallel data on the falling edge of TCLK. TCLK thus provides a convenient means to clock the data source. For 10 bit mode, the VSC7105 loads parallel data on the rising edge of REFCLK. The rising edge of REFCLK corresponds to the falling edges of both TCLK and TCLKN. The system designer may either use the rising edge of REFCLK or the falling edges of TCLK and TCLKN to clock the data source. Only data on T10:19 are used in 10-bit mode. The width of the input data bus is controlled by the DWS (Data Width Select) input. A logic LOW on this input places the VSC7105 in 20-bit mode and a logic HIGH places the VSC7105 in 10-bit mode.

Output Enable controls are provided for each of the serial output ports. $\overline{OE0}$ controls the primary outputs, TX, while $\overline{OE1}$ controls the secondary outputs, TLX. When an $\overline{OE}$ control is brought HIGH, the respective output is forced to a logical HIGH state. For example, a logical HIGH on the TX differential outputs will cause TX- to be LOW and TX+ to be HIGH. The secondary outputs can be used as a local loopback for system testing.

A three-level TEST signal is provided to facilitate functional testing and to select NRZ or NRZI data format. When TEST is left floating, REFCLK replaces the PLL-generated internal clock. For normal operation using the PLL-generated bit clock in Fibre Channel compliant mode which uses NRZ formatting, the TEST pin is tied to GND. For normal operation using NRZI formatting, the TEST pin is tied V_{DD}.

Figure 1: VSC7105 Transmitter Functional Block Diagram (20-Bit Mode)

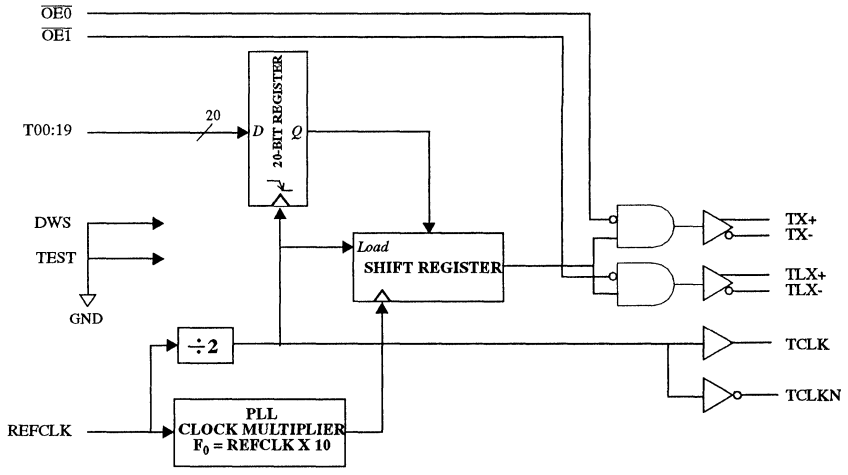
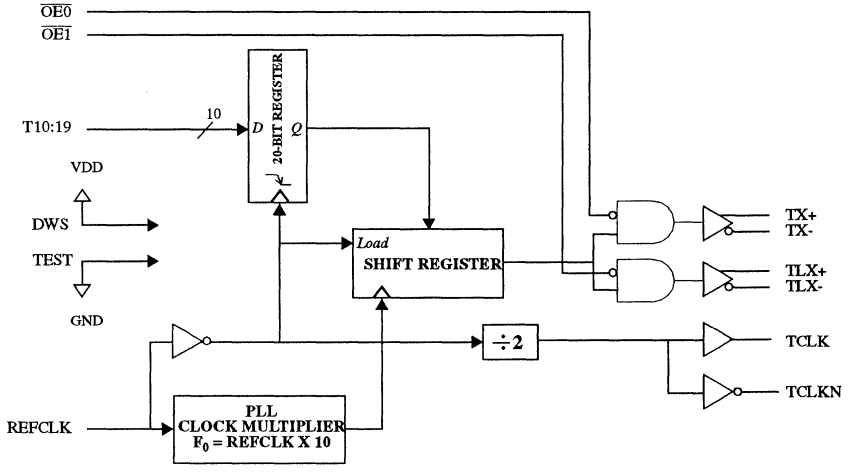


Figure 2: VSC7105 Transmitter Functional Block Diagram (10-Bit Mode)

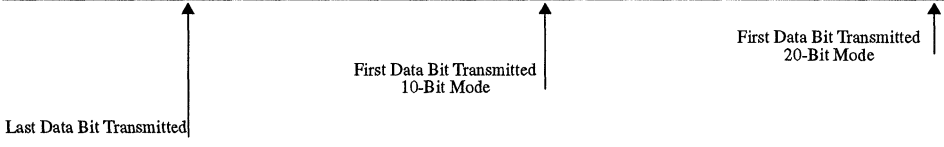


Transmission Character Interface

In Fibre Channel, an encoded byte is 10 bits and is referred to as a transmission character. A Fibre Channel word is 32 bits which is encoded into a transmission word of 40 bits. The 20 bit interface on the VSC7105 corresponds to a half transmission word. This document uses character and half-word to refer to transmission character and half transmission word respectively. Hence the VSC7105 has a selectable transmission character or half transmission word Fibre Channel interface. The bit ordering and its relationship to Fibre Channel bit position is shown in Figure 3 for the VSC7105. In 20-bit mode, T00 is transmitted first and in 10-bit mode, T10 is transmitted first.

Figure 3: Transmission Order and Mapping to Fibre Channel Character

Parallel Data Bits	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
8B/10B Bit Position	j	h	g	f	i	e	d	c	b	a	j	h	g	f	i	e	d	c	b	a



VSC7106 Receiver Functional Description

The VSC7106 is an ANSI compatible Fibre Channel (FC) receiver designed to work at the FC baud rate of 1.0625 Gb/s. The VSC7106 accepts differential high speed serial inputs, extracts the clock and retimes the data from the serial bit stream. The serial bit stream should be 8B/10B encoded data produced by a FC compatible transmitter, or any other source with a transition density of 40% or greater and a maximum run length of 6 consecutive 1's or 0's. The retimed serial bit stream is converted into either a 10 or 20-bit parallel output word. The VSC7106 provides Fibre Channel SYNC character recognition and data word alignment. The VSC7106 has internal PLL-based clock recovery circuitry which requires no external components.

Serial data is received on the RX, RLX pins as determined by LPEN. The PLL clock recovery circuit will lock to the data stream if the clock to be recovered is within 1.0% of the expected data rate. The expected data rate is 10 times the REFCLK frequency. For example if the REFCLK used is 106.25MHz, then the incoming serial baud rate must be 1.0625 Gigabaud $\pm$1.0%.

The VSC7106 provides complementary TTL recovered clock, RCLK and RCLKN, which is at one twentieth of the serial baud rate. This clock is generated by dividing down the high-speed clock which is phase locked to the serial data. If serial input data is not present, or does not meet the required transition density or baud rate, the RCLK frequency will be within +/-1.5% of half of the REFCLK.. The serial data is retimed by the internal high-speed clock, and deserialized. Parallel data is loaded into the output register on the falling edge of RCLK in 20-bit mode or on the falling edges of RCLK and RCLKN in 10 bit mode. The width of the output field can be 10 or 20-bit, under the control of the DWS (Data Width Select) pin. A logic LOW on this input causes the parallel data to be presented 20-bit wide. A logic HIGH causes a single 10-bit character to be presented on

R10:19. R00:09 are held HIGH in this mode. The functional block diagrams for operation in 20-bit or 10-bit modes are shown in Figure 4 and Figure 5 respectively.

Word synchronization is enabled in the VSC7106 by tying the SYNCEN pin to V_{DD}. When synchronization is enabled, the VSC7106 constantly examines the serial data for the presence of the Fibre Channel "Sync" character. This pattern is "0011111010" and is referred to as a K28.5 character with negative beginning disparity. The K28.5 character is not a normal data character, but a special character defined specifically for synchronization by Fibre Channel. Improper alignment occurs when a K28.5 straddles a 10 bit boundary or when a K28.5 is in the wrong 10-bit position of a half-word. When an improperly aligned sync character is encountered in 20-bit mode, the internal divider which produces RCLK and RCLKN is stalled in such a manner that the sync character is aligned in the R00:09 output field. This results in proper character and half-word alignment. In 10-bit mode, proper alignment is established when the K28.5 does not straddle a 10-bit character boundary, and appears in a character that is clocked out on the falling edge of RCLKN. Half-word synchronization is still relevant in 10-bit mode.

When the parallel data alignment changes in response to a sync pattern, some data which would have been presented on the parallel output port will be lost. The detection of the sync character is pipelined. Depending on the required new output phase, the sync character itself may be destroyed by the synchronization operation. Nonetheless, data following the sync character will be correctly aligned. Thus if downstream logic requires detection of the sync character (for example, to accomplish ordered set alignment) then more than one sync character must be transmitted in order to guarantee that one will be forwarded out of the VSC7106 incorruptible. Fibre Channel compliant systems requires the receipt of a minimum of three ordered sets for word synchronization. Ordered sets are special Fibre Channel transmission words that have the K28.5 sync character as the first character received. The first of these ordered sets will cause resynchronization in the VSC7106. The subsequent two ordered sets will be correctly aligned when they are received. In systems where synchronization is undesired, tying SYNCEN to GND will disable the sync function, and the data will be unframed.

On encountering a sync pattern, a pulse is generated on the SYNC output to inform the user that realignment of the parallel data field may have occurred. The SYNC pulse is presented one cycle in advance of the actual K28.5 character, and has a duration equal to the data. When operating the VSC7106 in 20-bit mode, the SYNC pulse spans one period of RCLK. In 10-bit mode, the pulse is HIGH for half of an RCLK period. Functional waveforms for synchronization in both modes are given in Figure 6 and Figure 7. Figure 6 shows the case when a sync character is detected and no phase adjustment is necessary. It illustrates the position of the SYNC pulse in relation to the sync character. Figure 7 shows the case where the K28.5 is detected, but out of alignment and a change in RCLK and the output data is required. Note that the VSC7106 always stretches the RCLK so it will never create a clock sliver on resynchronization.

Figure 4: VSC7106 Receiver Functional Block Diagram (20-Bit Mode)

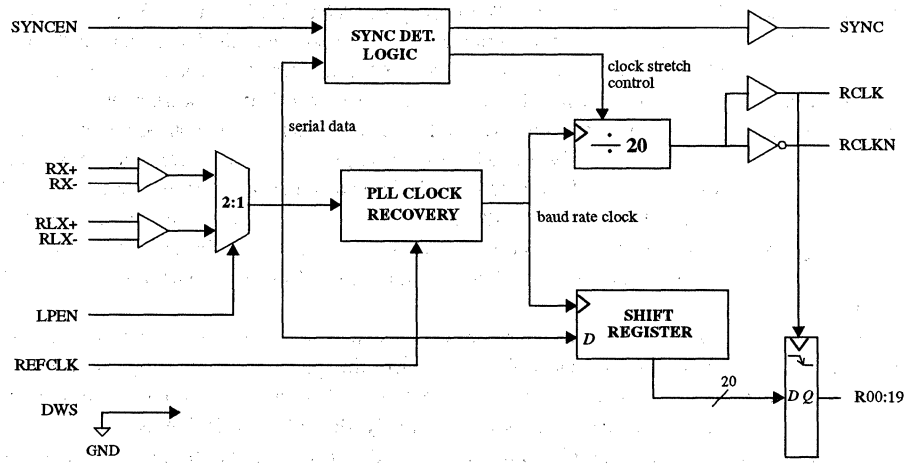


Figure 5: VSC7106 Receiver Functional Block Diagram (10-Bit Mode)

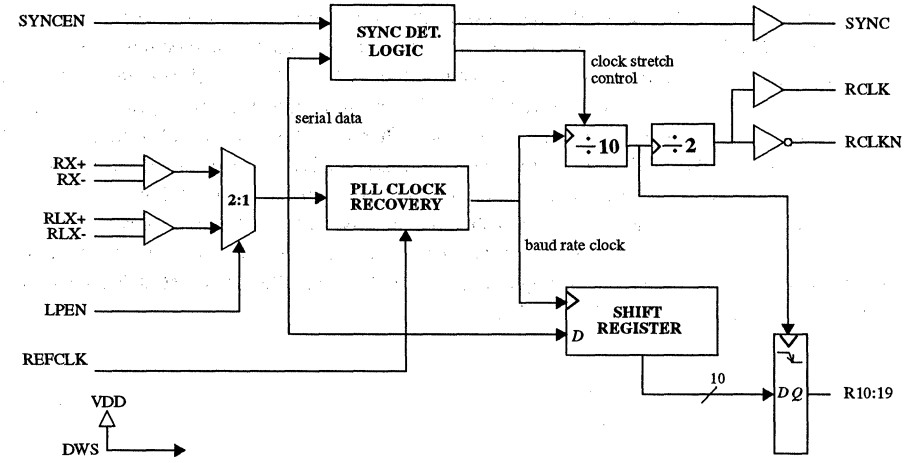
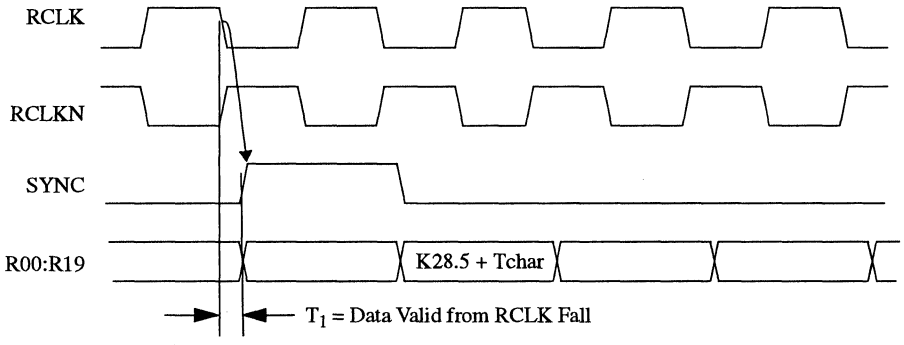
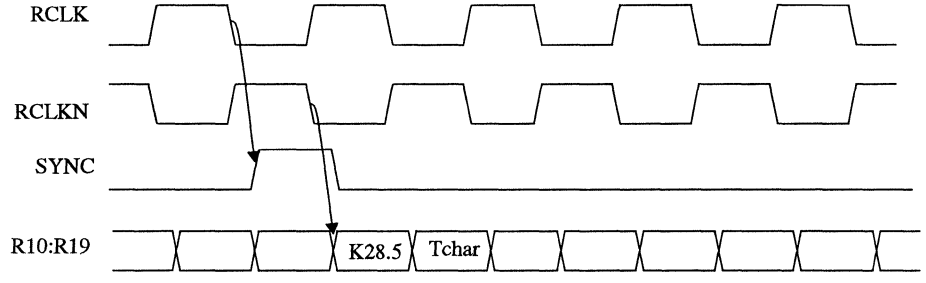


Figure 6: Sync Timing While In Sync

20 Bit Mode Timing



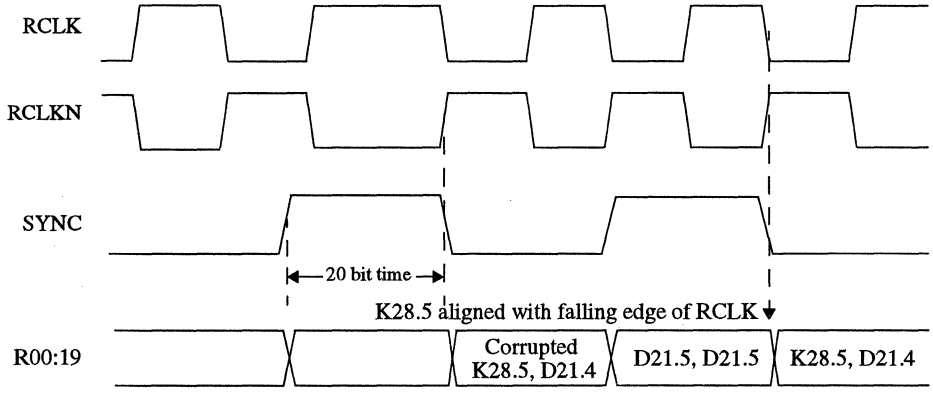
10 Bit Mode Timing



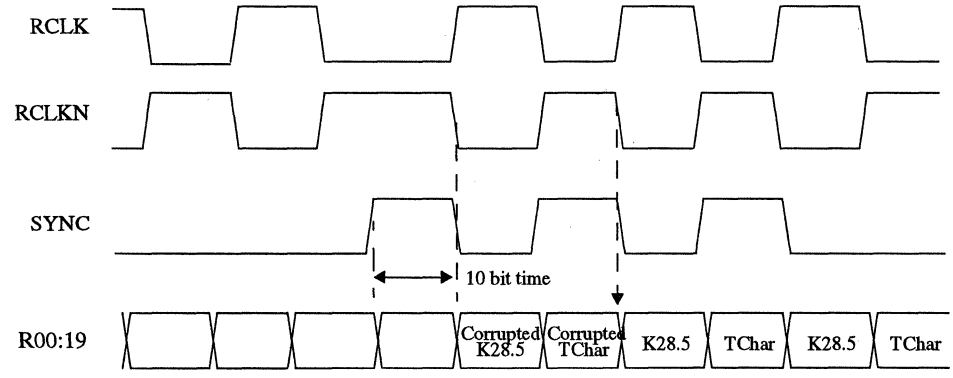
TChar: 10 bit Transmission Character

Figure 7: Sync and RCLK Timing When Resynchronizing

20 Bit Timing, Receiving Two Consecutive IDLE Words (K28.5, D21.4, D21.5, D21.5)



10 Bit Timing, Receiving Three Consecutive K28.5+TChar Half-Words



K28.5 aligned with falling edge of RCLKN

Figure 8: Transmitter Latency Waveform

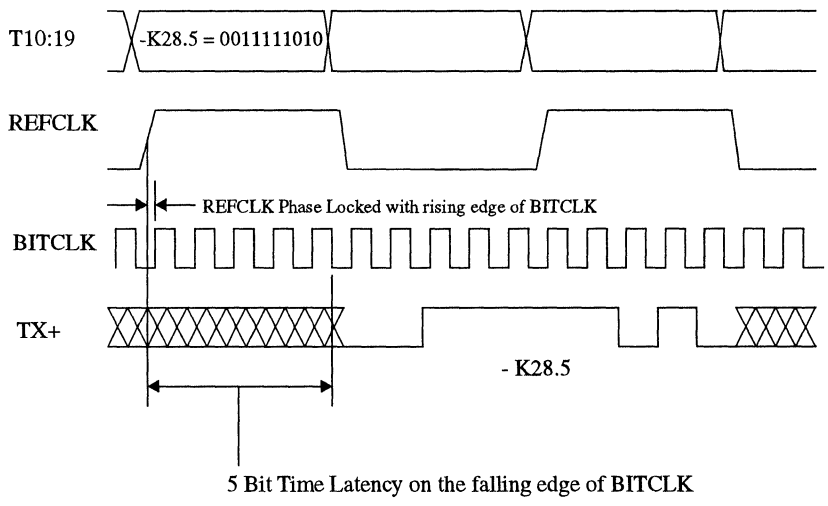


Table 1: Data Latency

VSC7105 Parallel to Serial Latency (10-Bit Mode)	5 Bit Times
VSC7105 Parallel to Serial Latency (20-Bit Mode)	5 Bit Times
VSC7106 Serial to Parallel Latency (10-Bit Mode)	26 Bit Times
VSC7106 Serial to Parallel Latency (20-Bit Mode)	46 Bit Times

Figure 9: VSC7105 Timing Waveforms

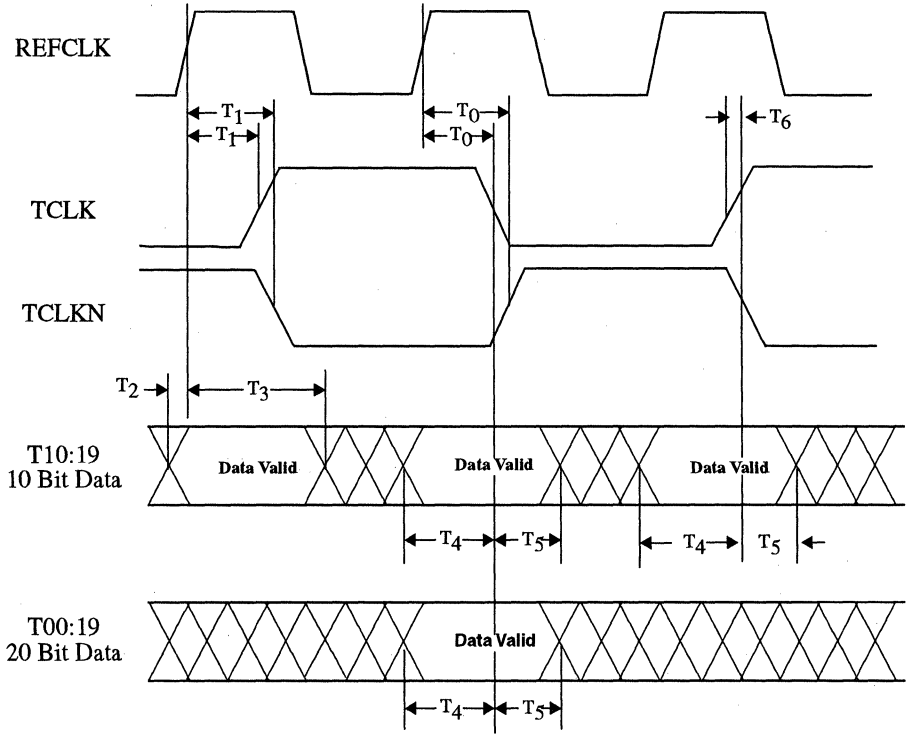


Table 2: VSC7105 AC Characteristics

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
T_0	REFCLK rise to TCLK fall and TCLKN rise	1.0	4.0	ns	—
T_1	REFCLK rise to TCLK rise and TCLKN fall	1.0	4.0	ns	—
T_2	Data setup w.r.t. REFCLK	1.0	—	ns	—
T_3	Data hold w.r.t. REFCLK	5.0	—	ns	—
T_4	Data setup w.r.t. TCLK/ TCLKN	5.0	—	ns	Derived from Data setup to REFCLK and REFCLK to TCLK/TCLKN delay
T_5	Data hold w.r.t TCLK/TCLKN	1.0	—	ns	Derived from Data hold from REFCLK and REFCLK to TCLK/TCLKN delay
T_{CR},T_{CF}	TCLK rise and fall time	—	5.0	ns	0.8V to 2.0V, tested on a sample basis Refer to TTL Rise/Fall Time vs. Loading
T_{SDR},T_{SDF}	Serial data rise and fall time	—	300	ps	20% to 80%, tested on a sample basis
T_6	TCLK to TCLKN skew	—	+/-1	ns	Tested on a sample basis
T_{DC}	TCLK, TCLKN duty cycle	45	55	%	—
Transmitter Output Jitter Allocation					
T_J (RMS)	Serial data output random jitter (RMS)	—	20	ps	RMS, tested on a sample basis (refer to Figure 13)
T_{DJ}	Serial data output deterministic jitter (p-p)	—	100	ps	Peak to peak, tested on a sample basis (refer to Figure 13)

Figure 10: VSC7106 AC Timing Waveforms

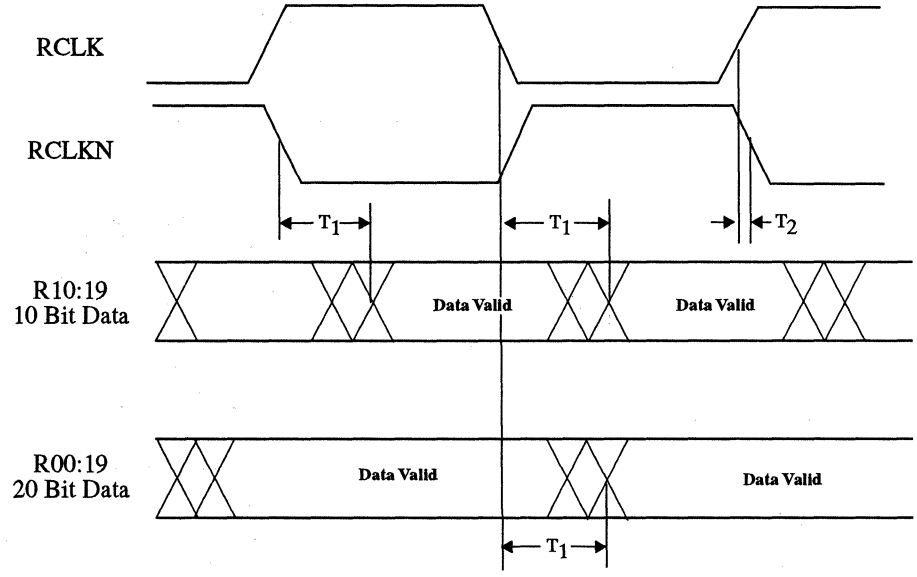
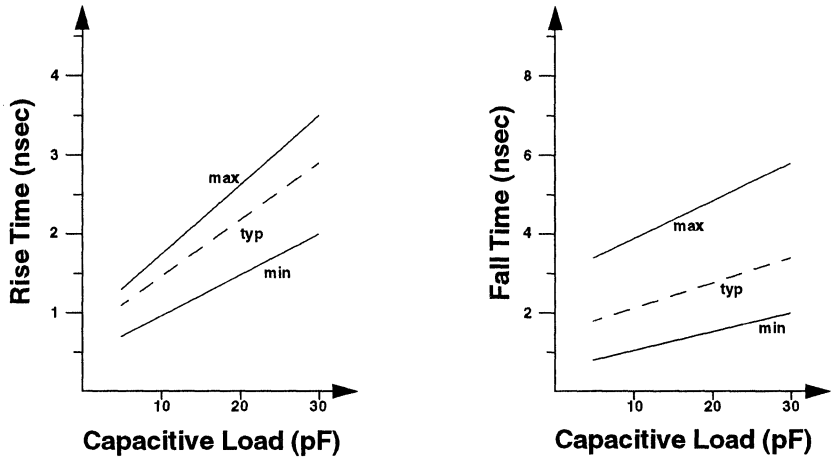


Table 3: VSC7106 AC Characteristics

Parameters	*Description*	*Min.*	*Max.*	*Units*	*Conditions*
T_1	RCLK or RCLKN fall to Data Valid	0.0	3.0	ns	—
T_2	RCLK to RCLKN skew	—	1.0	ns	Tested on sample basis
T_{RCR},T_{RCF}	RCLK rise and fall time	—	5.0	ns	Between 0.8 & 2.0V, tested on a sample basis
T_{DR},T_{DF}	Data output rise and fall time	—	5.0	ns	Between 0.8 & 2.0V,, tested on a sample basis
T_{LOCK}	Data acquisition lock time @ 1.0625Gb/s	—	2.4	µs	8B/10B IDLE pattern sample basis (refer to Figure 12).
Input Jitter Tolerance	Input data eye opening allocation at receiver input for BER≤1E-12	30%	—	bit time	As specified in Fibre Channel FC-PH standard eye diagram jitter mask (refer to Figure 13).

Figure 11: TTL Rise and Fall Time vs Output Loading



(VSC7105 TCLK/TCLKN: VSC7106 RCLK/RCLKN and R00:19)

Table 4: Reference Clock Requirements (VSC7105/VSC7106)

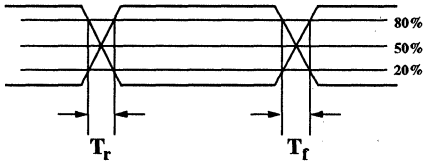
Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
FR	REFCLK Frequency Range	98	113	MHz	Tested on a sample basis
FT	REFCLK Frequency Tolerance	-100	100	ppm	Note 1
TD_{1-2}	Symmetry	40	60	%	Duty cycle at 50% pt.
SR_R,SR_F	REFCLK rise and fall slew rate.	500	—	mV/ns	Note 2
—	Random jitter	—	75	ps	peak to peak

Note 1) This value is based on typical system requirements (i.e.. Fibre Channel). The VSC7105 and VSC7106 can tolerate REFCLK mismatching of up to 0.5%.

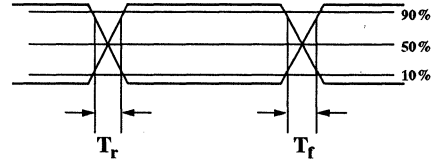
2) This value assumes an AC-coupled REFCLK. Higher slew rates will minimize REFCLK's contribution to jitter due to edge-triggering ambiguity.

Figure 12: Parametric Measurement Information

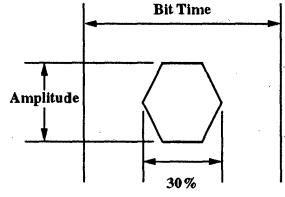
Serial Input Rise and Fall Time



TTL Input and Output Rise and Fall Time

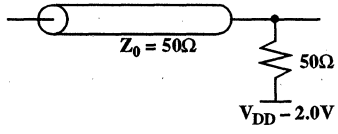


Receiver Input Eye Diagram Jitter Mask

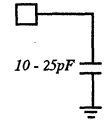


Parametric Test Load Circuit

Serial Output Load



TTL A.C. Output Load



Serial Output Load

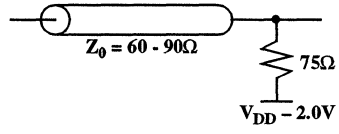
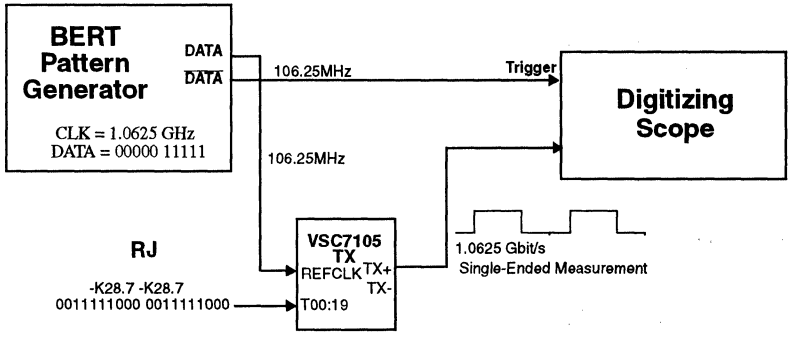


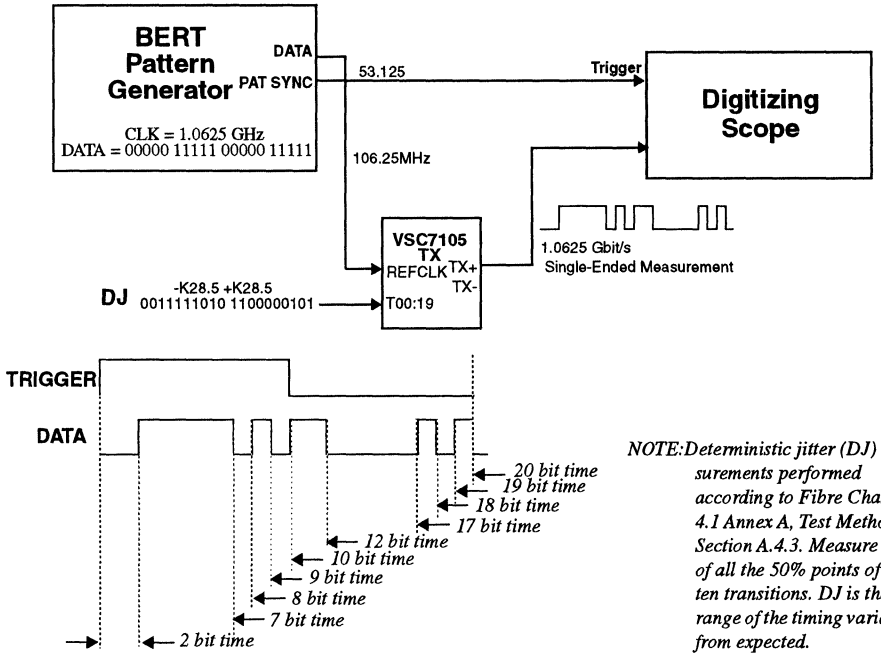
Figure 13: Transmitter Jitter Measurement Method

Random Jitter Measurement



NOTE: Random jitter (RJ) measurements performed according to Fibre Channel 4.1 Annex A, Test Methods, Section A.4.4. Measure standard deviation of all 50% crossing points. Peak to peak RJ is ± 7 sigma of distribution.

Deterministic Jitter Measurement



NOTE:Deterministic jitter (DJ) measurements performed according to Fibre Channel 4.1 Annex A, Test Methods, Section A.4.3. Measure time of all the 50% points of all ten transitions. DJ is the range of the timing variation from expected.

Absolute Maximum Ratings (1)

Power Supply Voltage, (V_{DD}) ..... 0.5V to +4V
PECL DC Input Voltage, (V_{INP}) ..... -0.5V to V_{DD} +0.5V
TTL DC Input Voltage, (V_{INT}) ..... -0.5V to 5.5V
DC Voltage Applied to Outputs for High Output State, ($V_{IN\,TTL}$) ..... -0.5V to V_{DD} + 0.5V
TTL Output Current (I_{OUT}), (DC, Output High) 50mA
PECL Output Current, (I_{OUT}), (DC, Output High) ..... -50mA
Case Temperature Under Bias, (T_C) ..... -55° to +125°C
Storage Temperature, (T_{STG}) ..... -65°C to +150°C

Recommended Operating Conditions

Power Supply Voltage, (V_{DD}) ..... +3.3V±5%
Operating Temperature Range, (T) (2) ..... 0°C to +90°C

Notes:

(1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

(2) Lower limit is ambient temperature and upper limit is case temperature.

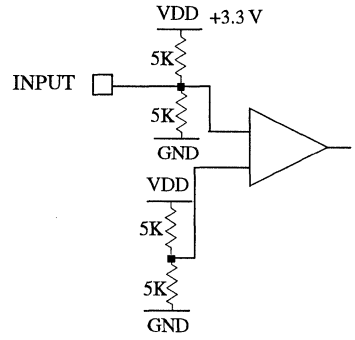
Table 5: VSC7105 DC Characteristics *(Over recommended operating conditions).*

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{OH}	Output HIGH voltage (TTL)	2.4	—	—	V	I_{OH} = -1.2 mA
V_{OL}	Output LOW voltage (TTL)	—	—	0.5	V	I_{OL} = +1.2 mA
V_{IH}	Input HIGH voltage (TTL)	2.0	—	5.5	V	$I_{IH} \leq 6.6$ mA @ V_{IH} = 5.5 V
V_{IL}	Input LOW voltage (TTL)	0	—	0.8	V	—
I_{IH}	Input HIGH current (TTL)	—	—	50	µA	V_{IN} = 2.4 V
I_{IL}	Input LOW current (TTL)	-500	—	-50	µA	V_{IN} = 0.5 V
V_{DD}	Supply voltage	3.14	3.3	3.47	V	3.3V ±+/-5%
I_{DD}	Supply current	—	—	350	mA	Outputs open V_{DD}max
P_D	Power dissipation	—	1.0	1.2	W	Outputs open, @ V_{DD} max Tcase = 20°C to 90°C.
$\Delta V_{INCLKDC}$	Single-ended Clock input swing (REFCLK)	600	—	1300	mVpp	Internally biased at $V_{DD}/2$. See Figure 14 for input structures.
ΔV_{OUT}	Serial Output differential peak to peak voltage swing (TX, TLX)	1200	—	2200	mVpp	50Ω to V_{DD} – 2.0 V

Table 6: VSC7106 DC Characteristics *(Over recommended operating conditions).*

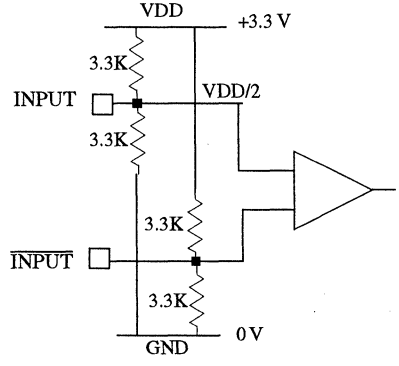
Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{OH}	Output HIGH voltage (TTL)	2.4	—	—	V	I_{OH} = -1.2 mA
V_{OL}	Output LOW voltage (TTL)	—	—	0.6	V	I_{OL} = +1.2 mA
V_{IH}	Input HIGH voltage (TTL)	2.0	—	5.5	V	$I_{IH} \leq 6.6$ mA @ V_{IH} = 5.5 V
V_{IL}	Input LOW voltage (TTL)	0	—	0.8	V	—
I_{IH}	Input HIGH current (TTL)	—	—	50	µA	V_{IN} = 2.4 V
I_{IL}	Input LOW current (TTL)	-500	—	-50	µA	V_{IN} = 0.5 V
V_{DD}	Supply voltage	3.14	3.3	3.47	V	3.3V +/-5%
I_{DD10}	Supply current - 10-Bit Mode	—	—	520	mA	Outputs open, @V_{DD} max Tcase=20°C to 90°C.
I_{DD20}	Supply current - 20-Bit Mode	—	—	560	mA	
P_{D10}	Power Dissipation - 10-bit mode	—	—	1.8	W	Outputs Open, V_{DD}=V_{DDmax}
P_{D20}	Power Dissipation - 20-bit mode	—	—	1.9	W	Outputs Open, V_{DD}=V_{DDmax}
$\Delta V_{INCLKDC}$	Single-ended REFCLK input swing	600	—	1300	mVpp	AC coupled
ΔV_{INSI}	Receiver differential peak to peak input sensitivity on RX & RLX	300	—	2600	mVpp	AC coupled. See Figure 14 for input structures.

Figure 14: Input Structures



REFCLK Input
(7105 : REFCLK)
(7106 : REFCLK)

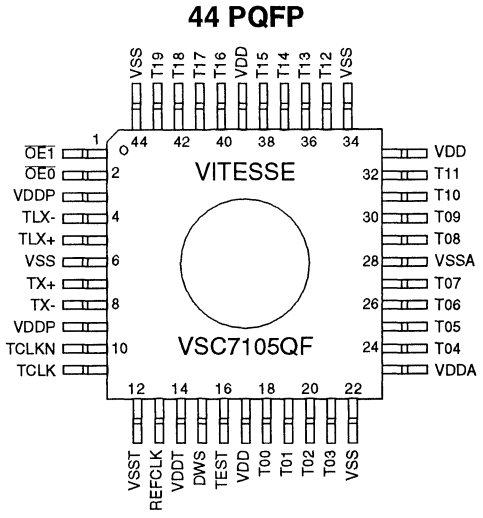
A



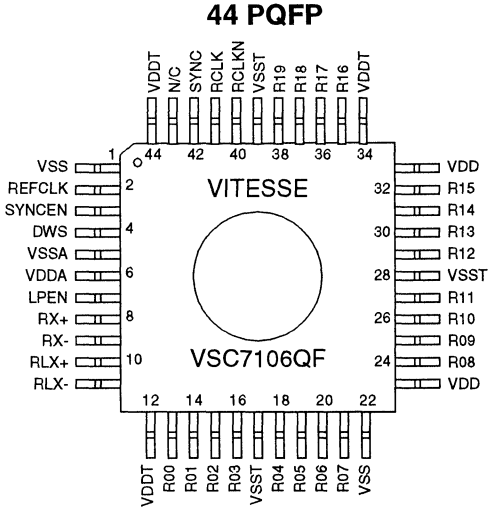
High Speed Differential Input
(7106: RX/RLX)

B

Figure 15: VSC7105/7106 Pin Diagrams



Heat Spreader Up
Top View



Note: The heat spreader is connected to V_{SS}.

Table 7: VSC7105 Pin Description

<table>
<tr><th>Pin #
44 PQFP</th><th>Name</th><th>Description</th></tr>
<tr><td>18-21,24-27
29-32,35-38
40-43</td><td>T00:19</td><td>INPUT - TTL
Parallel data on this bus is clocked in on the falling edge of TCLK in 20 bit mode, or on the falling edge of both TCLK and TCLKN in 10 bit mode. T00 is transmitted first in 20 bit mode and T10 first in 10 bit mode.</td></tr>
<tr><td>16</td><td>TEST</td><td>INPUT - Multi-Level Static Input
The level on this pin determines the serial encoding and the source of the bit clock to be used. The table below lists the effects caused by driving TEST to various levels.
<table>
<tr><th>Level</th><th>Effect</th></tr>
<tr><td>GND</td><td>PLL 10X Multiplied Clock used as bit clock and NRZ encoding used. [Fibre Channel Compatible]</td></tr>
<tr><td>Tristate
Open</td><td>Test Mode where REFCLK input is used as bit clock and NRZ encoding used</td></tr>
<tr><td>VDD</td><td>PLL 10X Multiplied Clock used as bit clock and NRZI Encoding used.</td></tr>
</table></td></tr>
<tr><td>15</td><td>DWS</td><td>INPUT - Static: TTL
This pin selects the parallel data bus width. When LOW, a 20 bit parallel bus width is selected and T00:19 are active. When HIGH, a 10 bit parallel data bus is selected, T10:19 are active and T00:09 are ignored.</td></tr>
<tr><td>2, 1</td><td>OE0
OE1</td><td>INPUT - TTL
Outputs enable inputs. Select serial output state as shown in the Table below.
<table>
<tr><th>OE0</th><th>OE1</th><th>TX+/TX-</th><th>TLX+/TLX-</th></tr>
<tr><td>LOW</td><td>LOW</td><td>active</td><td>active</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>active</td><td>HIGH/LOW</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>HIGH/LOW</td><td>active</td></tr>
<tr><td>HIGH</td><td>HIGH</td><td>HIGH/LOW</td><td>HIGH/LOW</td></tr>
</table></td></tr>
<tr><td>13</td><td>REFCLK</td><td>CLOCK INPUT - Single-Ended (Biased at VDD/2, refer to Figure 14-A)
A free running reference clock for the PLL clock multiplier. The frequency of REFCLK is 0.1x the desired baud rate.</td></tr>
<tr><td>11, 10</td><td>TCLK
TCLKN</td><td>OUTPUTS - COMPLEMENTARY TTL
Half word rate clock true and complement (frequency = REFCLK/2). In the 10 bit parallel data bus mode a new data word is clocked into the transmitter on the falling edge of both TCLK and TCLKN. In the 20 bit parallel data bus mode a new data word is clocked into the transmitter only on the falling edge of TCLK.</td></tr>
<tr><td>5,4</td><td>TLX+,
TLX-</td><td>OUTPUTS - DIFFERENTIAL Serial Output (Centered at VDD - 1.32V)
These outputs are functionally equivalent to TX+ and TX-.</td></tr>
</table>

Pin # 44 PQFP	Name	Description
7,8	TX+ TX-	OUTPUTS - DIFFERENTIAL Serial Output (Centered at VDD - 1.32V) These outputs output the serial transmitted data and drive 75Ω or 50Ω termination to VDD-2V.
12	VSST	TTL Ground
14	VDDT	TTL Power Supply
3, 9	VDDP	Differential Output Power Supply
17, 33, 39	VDD	Digital Power Supply
6, 22, 34, 44	VSS	Digital and Differential Output Ground
23	VDDA	Analog Power Supply
28	VSSA	Analog Ground

Table 8: VSC7106 Pin Description

Pin # 44 PQFP	Name	Description
13-16,18-21, 24-27, 29-32,35-38	R00:19	OUTPUTS - TTL The width of the parallel data bus is selected by the state of the DWS pin. Parallel data on this bus is clocked out on the falling edge of RCLK in 20 bit mode and on the falling edges of both RCLK and RCLKN in 10 bit mode. R00 is the first bit received in 20 bit mode and R10 is the first bit received in 10 bit mode. In 10 bit mode, R00:09 are driven high.
7	LPEN	INPUT - TTL When HIGH, LPEN selects the loopback differential serial inputs pins. When LOW, LPEN selects RX+ and RX- (normal operation).
4	DWS	INPUT - Static: TTL The level on this pin selects the parallel data bus width. When LOW, a 20 bit parallel bus width is selected and R00:19 are active. When HIGH, a 10 bit parallel data bus is selected (R10:19 are active) and R00:10 will go HIGH.
41, 40	RCLK, RCLKN	OUTPUTS - COMPLEMENTARY TTL Recovered clock rate (frequency ~ REFCLK/2). The falling edge of RCLK outputs a new word on the 20 bit data bus in the 20 bit mode. The falling edge of RCLK and RCLKN outputs a new word on R10:19 in the 10 bit mode. After a sync word is detected the period of the current RCLK and RCLKN is stretched to align with the half-word boundary.
2	REFCLK	INPUT - Single-Ended Clock (Biased at VDD/2, refer to Figure 14-A) A free running reference clock for the PLL clock multiplier. The frequency of REFCLK is within ±1.00% of 0.1x the desired baud rate.
42	SYNC	OUTPUT - TTL Upon detection of a valid sync symbol this output goes high for a RCLK period in 20 bit mode. In 10 bit mode, the SYNC output goes high for half an RCLK period.
10, 11	RLX+, RLX-	INPUT - DIFFERENTIAL Serial Input (Biased at VDD/2, refer to Figure 14-B) The serial loopback data inputs. Functionally equivalent to RX+ and RX-.
8, 9	RX+, RX-	INPUT - DIFFERENTIAL Serial Input (Biased at VDD/2, refer to Figure 14-B) The received serial data inputs.

Pin # 44 PQFP	Name	Description
3	SYNCEN	INPUT - STATIC: MULTI-LEVEL When tied to VDD, enables synch detection. Detection of the sync pattern (K28.5:0011111010, negative beginning running disparity) will establish the word boundary for the data to follow. When open (not connected) or tri-state, REFCLK replaces internal bit clock to facilitate factory testing. In this mode of operation sync detection is always enabled. When tied to GND, data is treated as unframed data.
12, 34, 44	VDDT	TTL Power Supply
17, 28, 39	VSST	TTL Ground
23, 33	VDD	Digital Power Supply
1, 22	VSS	Digital Ground
6	VDDA	Analog Power Supply
5	VSSA	Analog Ground

Package Thermal Characteristics

The VSC7105 and VSC7106 are packaged into thermally enhanced plastic quad flatpacks. These packages use industry standard EIAJ footprints, but have been enhanced to improve thermal dissipation through low thermal resistance paths from the die to the exposed surface of the heat spreader and from the die to the leadframe through the heat spreader overlap of the leadframe. The construction of the package is as shown in Figure 16.

Figure 16: Package Cross Section

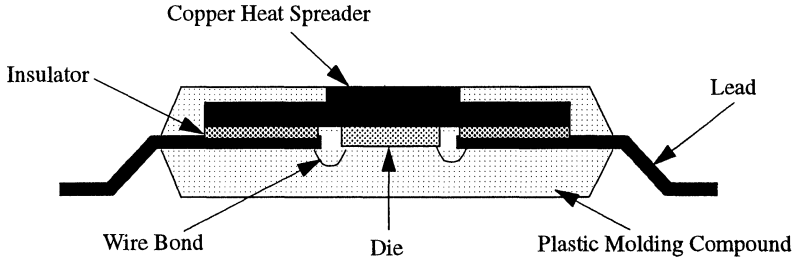


Table 9: 44 and 52 PQFP Thermal Resistance

Symbol	*Description*	44-pin Value	Units
θ_{jc}	Thermal resistance from junction to case	2.1	°C/W
$\theta_{ca\text{-}0}$	Thermal resistance from case to ambient, still air*	30	°C/W
$\theta_{ca\text{-}100}$	Thermal resistance from case to ambient, 100 LFPM air*	24	°C/W
$\theta_{ca\text{-}200}$	Thermal resistance from case to ambient, 200 LFPM air*	21	°C/W
$\theta_{ca\text{-}300}$	Thermal resistance from case to ambient, 300 LFPM air*	19	°C/W
$\theta_{ca\text{-}500}$	Thermal resistance from case to ambient, 500 LFPM air*	15	°C/W

**Note: Includes conduction through the leads of the package for a non-thermally saturated board.*

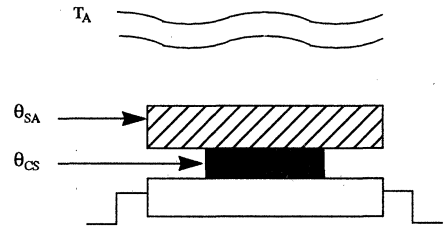
The VSC7105 and VSC7106 are designed to operate with at a case temperature up to 90°C. The user must guarantee that the case temperature specification is not violated. Given the thermal resistance of the package in still air, the user can operate the VSC7106 in still air if the ambient temperature does not exceed 36°C on a non-thermally saturated board.

If the user's environment exceeds 36°C, then the user must either provide adequate airflow, attach a heat sink, or both. Below is an example to guide the user in determining these requirements with additional airflow and with adding a heatsink.

1Thermal Resistance with Heat Sink

The determination of appropriate heat sink to use is as shown below.

Figure 17: Package Thermal Considerations



where:

q_{SA}	Thermal resistance from heatsink to ambient [airflow dependent]
q_{CS}	Thermal resistance from case to heatsink [User supplied, typically < 0.6° C/W]
$T_{A(MAX)}$	Maximum Air temperature [User supplied, 70° C for this example]
$T_{C(MAX)}$	Maximum Case temperature (90° C)
ΔT	$T_C - T_A$
$P_{(MAX)}$	Maximum Power Dissipation (1.9 W for VSC7106)

$$\therefore P = \frac{\Delta T}{\Sigma\theta} = \frac{T_C - T_A}{\theta_{SA} + \theta_{CS}}$$

$$\theta_{SA} = \frac{\Delta T}{P} - \theta_{CS}$$

If T_A = 70° C and θ_{CS} is 0.6° C/W,

$$\theta_{SA} = \frac{(90-70)°C}{1.9W} - 0.6°C/W$$

$$\theta_{SA} = 10°C/W$$

Therefore, to maintain the proper case and junction temperature, a heat sink with a θ_{SA} of 10° C/W or less must be selected at the appropriate air flow.

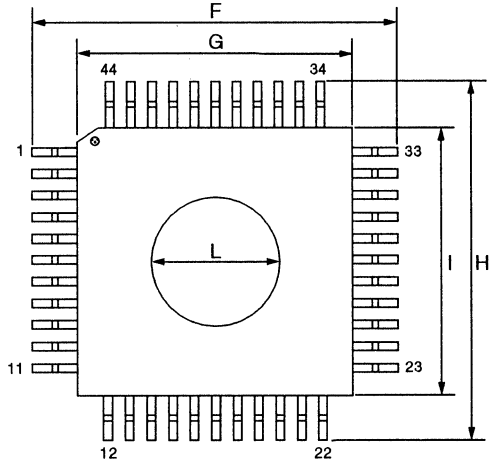
NOTE: The heat spreader is tied to V_{SS} in both the VSC7105 and VSC7106.

Data Sheet

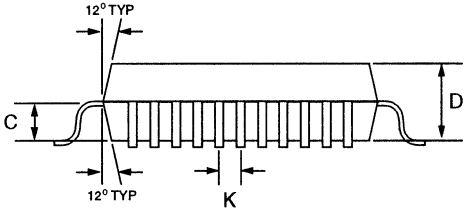
1.0625 Gbit/sec Transmitter/Receiver Chipset
for Fibre Channel or Proprietary Serial Links

Package Information

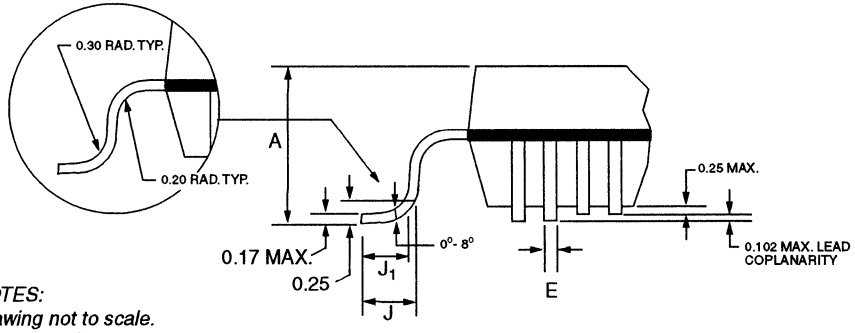
44-Pin PQFP Package Drawings



Item	*mm*	*Tol.*
A	2.35	MAX
D	2.00	+.10 / -.05
E	0.35	±.05
F	17.20	±.25
G	14.00	±.10
H	17.20	±.25
I	14.00	±.10
J	0.88	+.15 / -.10
J1	0.80	+.15 / -.10
K	1.00	BASIC
L	6.86	±.50 DIA.



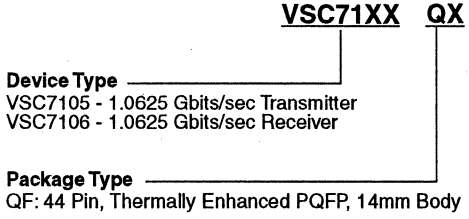
The heat spreader is tied to V_{SS}



NOTES:
Drawing not to scale.
Heat spreader up.
All units in mm unless otherwise noted.

Ordering Information

The part number for this product is formed by a combination of the device number, package type, and the operating temperature range.



Notice

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Warning

Vitesse Semiconductor Corporation's product are not intended for use in life support appliances, devices or systems. Use of a Vitesse product in such applications without the written consent is prohibited.

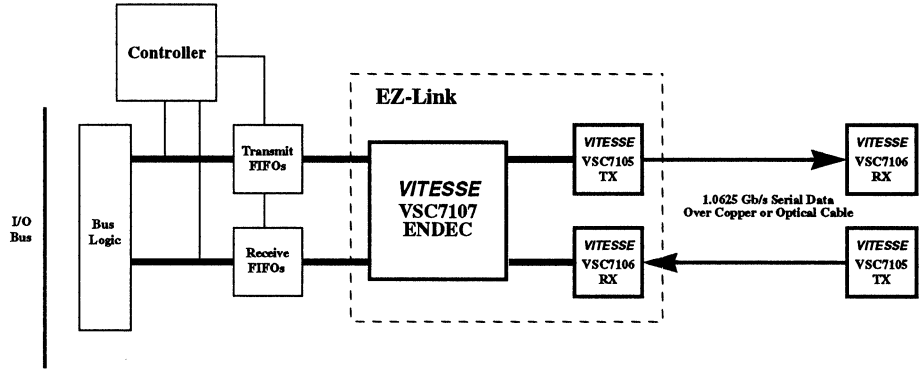
Preliminary Data Sheet

High Performance Encoder/Decoder for Fibre Channel or Proprietary Serial Links

Features

- Full ANSI X3T11 Fibre Channel (FC) Compatibility
- 8B/10B Encoding/Decoding
- 32 or 16 bit Synchronous FIFO System Interface
- 20-bit Encoded Transmission Character Interface
- CRC Calculation and Checking
- Parity Check and Generate
- Simplex (100 MByte/s) or Duplex (200 MByte/s) Mode Operation
- 6-bit CMND Port Supporting all FC-PH 4.2 Ordered Sets
- FC Receiver Loss of Synchronization State Machine
- FC Link Control State Machine
- 184 PQFP Package

System Block Diagram



General Description

The VSC7107 ENDEC is a high performance encoder/decoder designed for use in conjunction with the Vitesse VSC7105/7106 transmitter/receiver chips. The three chips can be combined with a controller and FIFO buffer memory to build a complete serial link.

The VSC7107 is a full duplex design with an encoder section for transmission and a decoder section for reception. The transmitter/encoder section accepts either a 2 or 4 byte user data word, encodes each byte into a 10 bit transmission character, and outputs transmission characters to the VSC7105 transmitter. The receiver/decoder section accepts transmission characters from the VSC7106 receiver, decodes them, and outputs a 2 or 4-byte user data word.

The VSC7107 has a system interface that emulates a synchronous FIFO for ease of use. FIFOs allow maximum sustained performance of 200 MB/s running a full duplex link. Their function is to handle the asynchronous interface between the bus data rate and the different serial data rates, and handle phase and frequency differences inherent in serial links.

The VSC7107 includes the hardware necessary for packetized data protection. Framing functions are provided through the CMND bus via Fibre Channel compliant special code symbols (ordered sets) for Start of Frame and End of Frame. CRC generation and data frame verification protect the Fibre Channel frame header and data field when these framing functions are used.

The VSC7107 provides a command interface which allows the user to manage the serial link. Signals are also provided to decode serial link error conditions and differentiate between data and commands. The VSC7107 implements all of the Fibre Channel defined link management functions through the Loss of Synchronization State Machine (LOS) and the Link Control State Machine (LCSM) as specified in FC-PH 4.2 clauses 11-16. The LOS manages receiver word synchronization. The LCSM recognizes and appropriately responds to all the primitive sequences required for generic link management such as initialization, offline, and link failure.

Vitesse's VSC7107 is a versatile part that allows the system designer to create proprietary or Fibre Channel serial links by taking advantage of some, or all, of the Fiber Channel compliant features.

Functional Description

System Data Interface

The VSC7107 supports two types of words on the system interface: 32 bit or 16 bit user data words. The system data bus emulates a synchronous FIFO interface (such as those available from Cypress and IDT) and consists of two separate buses for inputs and outputs at a duplexed data rate of 200 MByte/s.

The VSC7107 is composed of two separately timed sections. The two sections may be operated together for a duplex link or separately for a simplex link. The Encoder section of the design receives its timing from a clock source that must be in phase with the clock source for the companion VSC7105 transmitter chip. The Decoder section of the design is clocked by the recovered clock from its companion VSC7106 receiver chip. Static configuration pins and link maintenance signals span the timing boundary between the two sections.

Encoder System Interface

The purpose of the Encoder is to encode user data into transmission characters which, when transmitted serially, create a data stream that is rich in transitions and is DC balanced. A data stream rich in transitions allows robust clock recovery, and a DC balanced data stream eliminates DC drift in serial transmission. By encoding the clock into the serial data transmission, the VSC7107 eliminates the need to transmit a separate clock signal. As specified by the Fibre Channel Standard, the VSC7107 implements the 8B/10B code, which adds two bits of overhead to each byte. The VSC7107 transmits two transmission characters every EN_CLK clock period (53.1 MHz for 1.0625 Gb/s).

The VSC7107 system interface allows users to burst data at the full rate reliably and simply. If no valid data is available, the VSC7107 automatically generates an IDLE word. (Refer to the Fibre Channel Ordered Set Table for IDLE word clarification). This condition is indicated to the VSC7107 either by the EFEF# input or the HOLD# input. If a FIFO is used, the VSC7107 EFEF# input should be tied to the EMPTY flag output of the FIFO to inform the VSC7107 that no data is present in the FIFO. The VSC7107 HOLD# input is provided to restrain the VSC7107 from pulling data out of the FIFO until a complete frame or data packet is loaded into the FIFO using the HOLD# input. This prevents the insertion of IDLEs into the middle of a frame. The EFREN# signal is provided by the VSC7107 to disable the data source when the VSC7107 detects a link condition which prohibits the successful transfer of data. EFREN# goes high (disabled) when the VSC7107 is being initialized or has detected a link failure or link reset condition.

There are two data sources in the Encoder section: EN_DATA and CMND. The EN_DATA port is a 32 bit bus and CMND is a 6 bit command bus. In serial links it is useful to have a mechanism to differentiate data transmission from special characters or command transmissions with special purposes. Two mechanisms are provided to achieve this differentiation:

1. The CMND bus allows users to transmit Fibre Channel defined "ordered sets." These ordered sets are used by Fibre Channel links for link management. Refer to "CRC" on page 107 and Table 4, "Ordered Set List," on page 106 for further information.
2. An EN_KCHAR pin is provided to specify whether byte 0 is a data character or a special character. This pin is referred to as a control variable, and allows the user to issue special 8B/10B characters (K characters), called Fibre Channel ordered sets, without using the CMND bus. All Fibre Channel special characters are supported. The special character list is in Table 2. This pin can also be used to create custom commands for proprietary links.

If the CMND port is used to transmit ordered sets, the CMND data takes precedence over DATA_IN. If a valid CMND exists on the CMND port, the VSC7107 will transmit the data indicated by CMND regardless of valid data on the EN_DATA inputs.

Internally, the VSC7107 has a 16 bit data path which is clocked at 53.125 MHz to achieve the 1.0625 Gb/s serial data rate. However, as defined by the Fibre Channel Standard, the insertion of ordered sets and CRC must occur on 32 bit word boundaries. Because of this, the VSC7107 and the system designer must have a mechanism for keeping track of word boundaries operating at 26.5625 MHz. The encoder clock, EN_CLK, is the primary clock input for the encoder section. The EFCLK is the word clock used by the VSC7107. This clock is generated internally and provided to the system designer. Regardless of whether the VSC7107 is configured in 16 or 32 bit mode, EFCLK is half the EN_CLK frequency. The ESYNC input is provided to synchronize the logic to the proper clock boundary. EFCLK may be tied to ESYNC. Providing a clock signal which is half the frequency of the EN_CLK will maintain word synchronization.

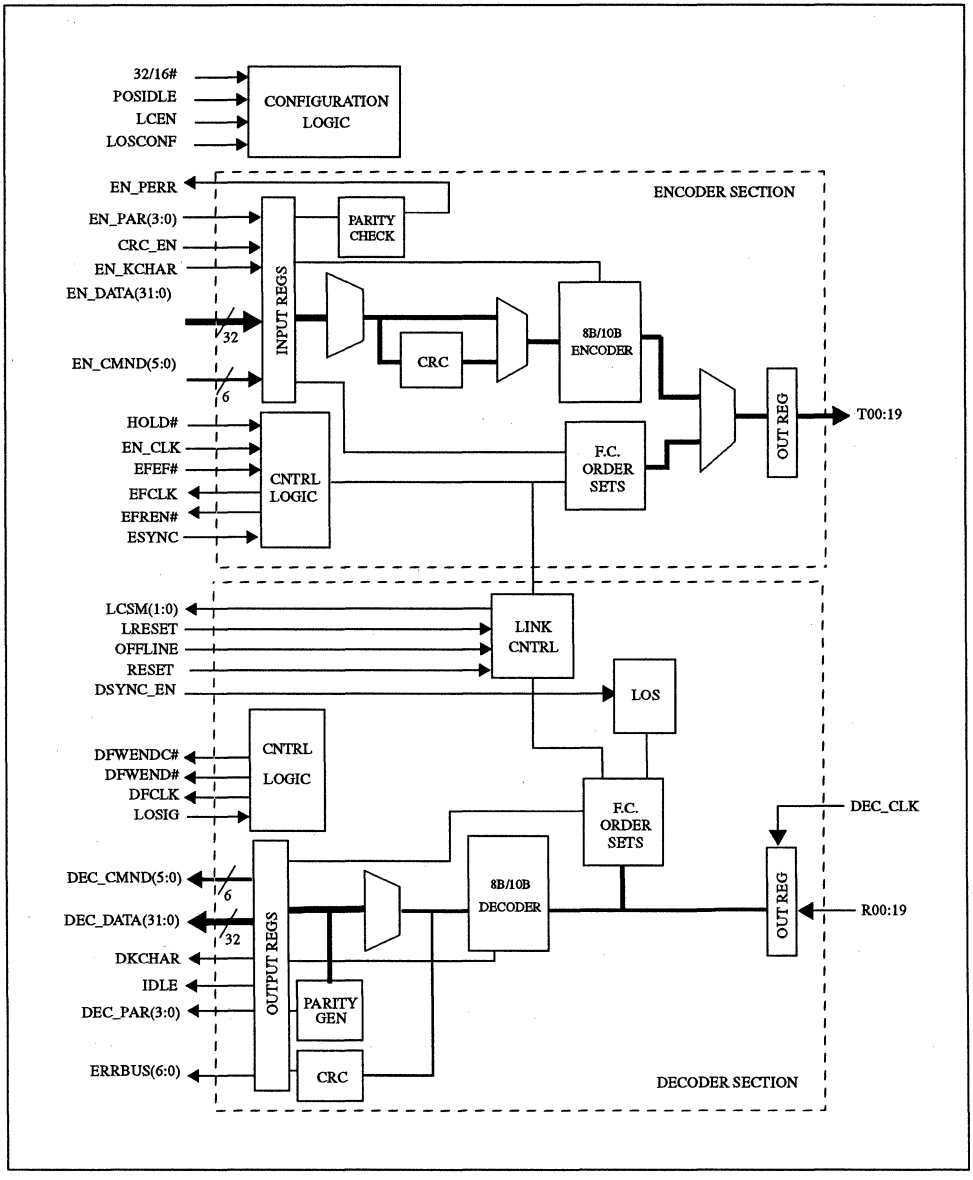
With very few exceptions, all inputs to the VSC7107 are registered to allow for the maximum available setup time. Both the EN_DATA and CMND buses must meet the setup and hold time requirements of the VSC7107 with regard to the EN_CLK. Refer to the ENCODER timing diagrams and AC Specifications for timing details. Two options are available for providing a clock source to EN_CLK. The TCLK output of the VSC7105 may be used, or the user may provide a clock in phase with the VSC7105 REFCLK.

The VSC7107 can be configured to operate with a 16 bit or a 32 bit system interface. The user selects the appropriate mode through the 32/16# select input. When the 32/16# signal is low the VSC7107 is configured to operate in 16 bit mode. When this signal is high, the VSC7107 is configured to operate in 32 bit mode.

No internal buffering is resident on the VSC7107 to hold data or to manage metastable timing caused by a data source with slightly different timing than the VSC7107. In order to manage these conditions, either FIFOs must be used for the data source or it must be phase aligned to EN_CLK.

Parity protection is provided for the encoder data source. The user provides odd byte parity to the Encoder through the EN_PAR(3:0) pins. The VSC7107 checks this parity and returns a HIGH on the PERR output if a parity error is detected. The VSC7107 returns a LOW on PERR if parity is correct.

Functional Block Diagram



Byte Transmission Order

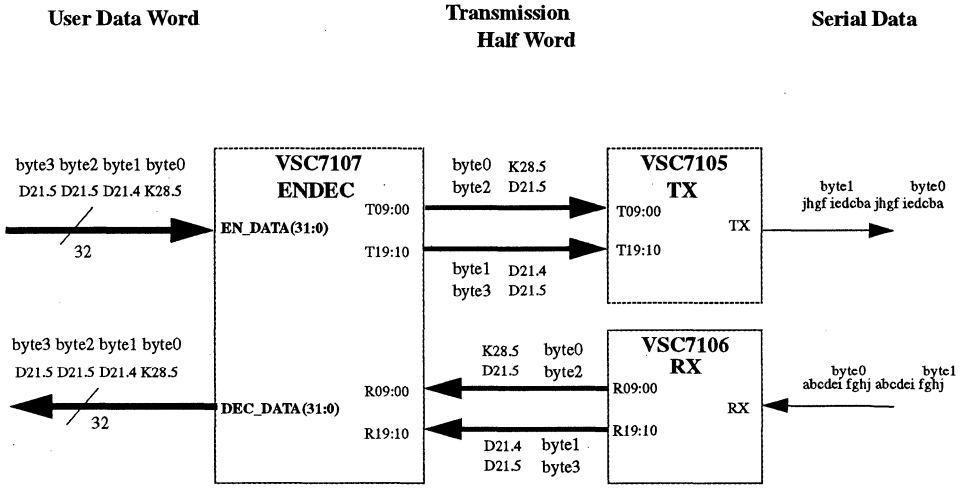
The Encoder block can accept 32 or 16 data bits at a time. EN_DATA (31:0) is four bytes organized sequentially. EN_DATA (7:0) is byte 3, EN_DATA(15:8) is byte 2, EN_DATA (23:16) is byte 1, and EN_DATA (31:24) is byte 0. The Fibre Channel Standard defines a 4 byte encoded transmission word (40 bits) and special transmission words referred to as "ordered sets." The Fibre Channel Standard also defines the transmission and reception order for these data words and ordered sets. The VSC7107 conforms to this transmission order.

In 32 bit mode, bytes 0 and 1 are encoded and transmitted first. Byte 0 will be encoded and will appear in T09:00 in the proper bit order. Byte1 will appear in T19:10 in the proper bit order.

Bytes 2 and 3 are then processed together and transmitted out with byte 2 in T09:00 and byte 3 in T19:10.

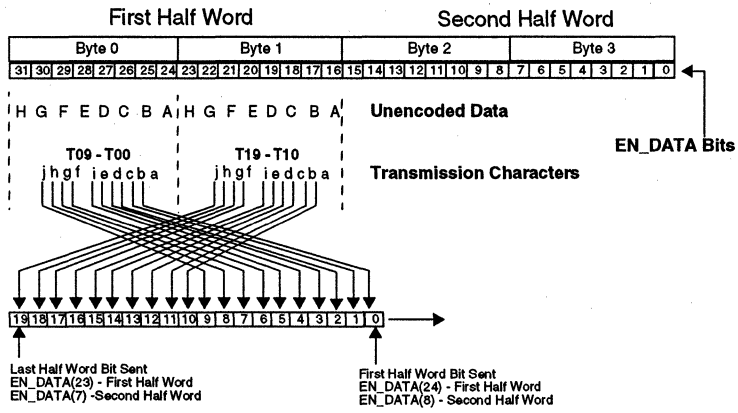
In 16 bit mode, only bytes 0 and 1 are used as data sources. Any data in EN_DATA(15:0) is ignored. The data is fed into the Encoder at the same rate at which it is processed and transmitted out. Byte 0 is transmitted out in T09:00 and byte1 is transmitted out in T19:10. Transmission byte order and bit order are shown in Figure 1 and Figure 2.

Figure 1: Fibre Channel Byte Transmission Order



Fibre Channel Idle Word: K28.5 D21.4 D21.5 D21.5

Figure 2: Half Word Transmission Order



Decoder System Interface

The Decoder section of the VSC7107 decodes the transmission characters received from the VSC7106. The Decoder requires a two transmission character input operating at 53.125MHz for 1.0625 Gb/s serial data. The transmission characters must be clocked into the Decoder on the falling edge of the recovered clock (RBC-) provided by the VSC7105. As with the Encoder, two 8B/10B decoders operate in parallel. The Decoder provides a selectable 32 or 16 bit interface to the system.

The Decoder performs the additional task of word alignment as defined by the Fibre Channel Standard. The Loss of Synchronization state machine defined by the Fibre Channel Standard is incorporated into the VSC7107 Decoder (refer to "Loss of Synchronization State Machine" on page 16). When the state machine is enabled, the Decoder recognizes a Fibre Channel IDLE word and aligns it referenced to the Fibre Channel defined byte order. An IDLE word is a special ordered set specified by the Fibre Channel Standard to perform word alignment. The Decoder expects the VSC7106 Receiver to perform byte alignment. The Fibre Channel specification expects only to recognize IDLE words with negative beginning disparity. The POSIDLE pin allows users to configure the VSC7105 to recognize only the Fibre Channel defined IDLE or recognize IDLE's with beginning negative or positive disparity. Vitesse has defined a positive beginning disparity IDLE word as listed in the Ordered Set Table. When POSIDLE is HIGH, both IDLEs are recognized. When POSIDLE is LOW, only the negative beginning disparity IDLE is recognized.

The transmission characters are decoded and sent to the system in either 32 bit or 16 bit words, as specified by the 32/16# pin. The DEC_DATA(31:0) bus sends data to the system. The Decoder outputs data in the same byte location as it was input. In 32 bit mode, all data bytes are used. In 16 bit mode, only DEC_DATA(31:16) has valid data.

The Decoder section has a synchronous FIFO system interface similar to that interface of the Encoder section. As with the Encoder section, the Decoder section outputs data on the DEC_DATA(31:0) bus with the same byte ordering. Both 32 bit and 16 bit words are supported. The DEC_CMND port informs the system if an ordered set is detected by the Decoder. The DEC_CMND reports commands with values identical to the EN_CMND commands described in Table 2.

The Decoder section is clocked by the DEC_CLK. The phase and frequency of the clock at the receiving end of a serial link is not related to the system clock of the receiver. Instead, the receive clock phase is a function of the delay caused by the cable over which the serial data is transported. The receive clock frequency is a function of the clock on the transmitter side of the link. Therefore the VSC7107 DEC_CLK input must receive its clock from the clock recovery circuit in the VSC7106 receiver chip. Because the VSC7107 can only operate with a 20 bit transmission character input, the VSC7106 must be configured to operate in 20 bit mode. The VSC7107 generates a DF_CLK to clock the receiver system FIFOs when the part is configured in 32 bit mode. The DF_CLK outputs a signal that is half of DEC_CLK frequency. The VSC7106 recovered clock may be used to clock both the Decoder section of the VSC7107 and the receive FIFOs when the system is used in 16 bit mode.

All data, ordered sets, SOF, EOF, and primitive sequences are transmitted to the DEC_DATA(31:0) bus. The DKCHAR pin is asserted HIGH if a special character appears in byte 0. Two Write Enables (DFWEND# and DFWENDC#) are provided to differentiate between data words and ordered sets. This allows the user to control what is written into the receive FIFOs. DFWENDC# allows valid data and ordered sets to be written into the receive FIFOs. DFWENDC is asserted HIGH (disable write) only when an IDLE is detected or when an error or initialization condition is present. The DFWEND# signal allows only valid data to be written into the receive FIFOs. DFWEND# is asserted HIGH when an error condition is present or when an ordered set is present at the DEC_DATA bus.

The Fibre Channel IDLE word never enables either of the Write Enables. The user can therefore avoid filling system FIFOs with ordered sets such as IDLES. When POSIDLE is enabled, neither the Fibre Channel IDLE or the Vitesse defined positive beginning disparity IDLE causes the write enables to be active. The presence of an IDLE causes the IDLE pin to be asserted HIGH. As defined by the Fibre Channel Standard, unknown ordered sets can be treated as IDLEs. LOSCONF is used to determine how unknown ordered sets are treated. When LOSCONF is HIGH, the VSC7107 will define unknown ordered sets as IDLEs if LOSCONF is LOW, unknown ordered sets will enable DFWENDC# to be active. If the write enables are LOW, the VSC7107 is allowed to write to the FIFOs.

Several signals are provided for detection of and response to transmission conditions. A DEC_CMND bus is provided which detects the presence of an ordered set and notifies the user of the ordered set type. The ERRBUS(5:0) detects errors and informs the system of the error type. Table 1 defines the error conditions decoded by the ERRBUS. The link control state machine has a 2 bit output which informs the user of the current link state. Refer to "Link Control State Machine" on page 52 for further details.

Table 1: ERRBUS Description

Bit	*Error Description*	*Bit*	*Error Description*
0	Link Failure	4	Invalid Transmission Word
1	Loss of Synchronization	5	Invalid CRC
2	Loss of Signal	6	Unrecognized Ordered Set
3	Primitive Sequence Protocol Error	—	—

Fibre Channel Transmission Protocols

The VSC7107 implements the Fibre Channel defined transmission protocol or FC-1 layer. Included in the Fibre Channel transmission protocol are 8B/10B encoding, CRC protection, the definition of ordered sets for link management, and the use of state machines for word synchronization and for link management using ordered sets.

8B/10B Encoding

The VSC7107 provides the Fibre Channel specified 8B/10B encoding and decoding with running disparity which bounds the run length of the code and maintains DC balance. This improves the quality of the transmitted data, which makes clock recovery possible at the receiver.

Fibre Channel nomenclature refers to encoded bytes as "transmission characters." The Fibre Channel Standard specifies two kinds of bytes: data bytes and special bytes. Each valid transmission character is given a name using the convention Zxx.x, where Z is the control variable of the unencoded byte. If the byte is a data byte the control character is a "D". If the byte is a special byte the control character is a "K." The VSC7107 provides a single bit for the control variable to specify or notify whether the left most byte is a data character or a special character. A "1" specifies a special character and a "0" specifies a data character.

The VSC7107 accepts the FC-1, unencoded bit notation as specified below, with H being the most significant bit in a byte.

HGFEDCBA Z

The 8B/10B encoding acts on three and five sub-blocks respectively as grouped below:

HGF EDCBA

The valid data character name is an annotation of the control character (D or K), plus the decimal value of the second sub-block (EDCBA), plus a decimal point ("."), and the decimal value of the first sub-block (HGF). Refer to the example below:

HGF	EDCBA	FC-1 Notation
101	11100	FC-1 Value
5	28	Decimal Value
K28.5		Character Name

The 8B/10B encoding adds two additional bits to the transmission character. Bit "i" is added to the five bit sub-block and bit "j" is added to the three bit sub-block. The 8 bit, FC-1 notation expands to the 10 bit encoded notation as shown below:

JHGF IEDCBA

There are two encoded characters for each transmission character. One is for a negative beginning disparity and one is for a positive beginning disparity. Positive disparity refers to more "ones" than "zeros" in the previously transmitted sub-block. Running disparity is calculated per sub-block rather than per character. The use of two encoded transmission characters results in a DC balanced transmission, in which an equal number of zeros and ones are transmitted. Some sub-blocks are disparity neutral, which means that the sub-block contains an equal number of ones and zeros. Disparity neutral sub-blocks cause no changes in current running disparity. The VSC7107 checks for the current disparity. If the proper disparity is not detected, the VSC7107 will transmit the proper disparity.

Each transmission character has four representations - character name, unencoded binary representation (FC-1 value), encoded negative running disparity representation, and encoded positive disparity representation. Table 2 shows all the valid special character values defined by the Fibre Channel Standard. Table 3 shows the valid transmission data characters.

The bits are transmitted serially with bit "A" first followed in order by bits "B," "C," "D," "E," "I," "F," "G," "H," and "J."

Table 2: Valid Special Characters

Special Code Name	*Current RD- abcdei fghj*	*Current RD+ abcdei fghj*	*Conditions*	*Special Code Name*	*Current RD- abcdei fghj*	*Current RD+ abcdei fghj*	*Conditions*
K28.0	001111 0100	110000 1011	Reserved*	K28.6	001111 0110	110000 1001	Reserved*
K28.1	001111 1001	110000 0110	Reserved*	K28.7	001111 1000	110000 0111	Test
K28.2	001111 0101	110000 1010	Reserved*	K23.7	111010 1000	000101 0111	Reserved*
K28.3	001111 0011	110000 1100	Reserved*	K27.7	110110 1000	001001 0111	Reserved*
K28.4	001111 0010	110000 1101	Reserved*	K29.7	101110 1000	010001 0111	Reserved*
K28.5	001111 1010	110000 0101	Sync	K30.7	011110 1000	100001 0111	Reserved*

*Note (1) *Reserved – Valid transmission characters which are not defined for use by the Fibre Channel standard.*

Table 3: Valid Data Characters

Data Byte Name	*Bits HGF EDCBA*	*Current RD- abcdei fghj*	*Current RD+ abcdei fghj*	*Data Byte Name*	*Bits HGF EDCBA*	*Current RD- abcdei fghj*	*Current RD+ abcdei fghj*
D0.0	000 00000	100111 0100	011000 1011	D0.1	001 00000	100111 1001	011000 1001
D1.0	000 00001	011101 0100	100010 1011	D1.1	001 00001	011101 1001	100010 1001
D2.0	000 00010	101101 0100	010010 1011	D2.1	001 00010	101101 1001	010010 1001
D3.0	000 00011	110001 1011	110001 0100	D3.1	001 00011	110001 1001	110001 1001
D4.0	000 00100	110101 0100	001010 1011	D4.1	001 00100	110101 1001	001010 1001
D5.0	000 00101	101001 1011	101001 0100	D5.1	001 00101	101001 1001	101001 1001
D6.0	000 00110	011001 1011	011001 0100	D6.1	001 00110	011001 1001	011001 1001
D7.0	000 00111	111000 1011	000111 0100	D7.1	001 00111	111000 1001	000111 1001
D8.0	000 01000	111001 0100	000110 1011	D8.1	001 01000	111001 1001	000110 1001
D9.0	000 01001	100101 1011	100101 0100	D9.1	001 01001	100101 1001	100101 1001
D10.0	000 01010	010101 1011	010101 0100	D10.1	001 01010	010101 1001	010101 1001
D11.0	000 01011	110100 1011	110100 0100	D11.1	001 01011	110100 1001	110100 1001
D12.0	000 01100	001101 1011	001101 0100	D12.1	001 01100	001101 1001	001101 1001
D13.0	000 01101	101100 1011	101100 0100	D13.1	001 01101	101100 1001	101100 1001
D14.0	000 01110	011100 1011	011100 0100	D14.1	001 01110	011100 1001	011100 1001
D15.0	000 01111	010111 0100	101000 1011	D15.1	001 01111	010111 1001	101000 1001
D16.0	000 10000	011011 0100	100100 1011	D16.1	001 10000	011011 1001	100100 1001
D17.0	000 10001	100011 1011	100011 0100	D17.1	001 10001	100011 1001	100011 1001
D18.0	000 10010	010011 1011	010011 0100	D18.1	001 10010	010011 1001	010011 1001
D19.0	000 10011	110010 1011	110010 0100	D19.1	001 10011	110010 1001	110010 1001
D20.0	000 10100	001011 1011	001011 0100	D20.1	001 10100	001011 1001	001011 1001
D21.0	000 10101	101010 1011	101010 0100	D21.1	001 10101	101010 1001	101010 1001
D22.0	000 10110	011010 1011	011010 0100	D22.1	001 10110	011010 1001	011010 1001
D23.0	000 10111	111010 0100	000101 1011	D23.1	001 10111	111010 1001	000101 1001
D24.0	000 11000	110011 0100	001100 1011	D24.1	001 11000	110011 1001	001100 1001
D25.0	000 11001	100110 1011	100110 0100	D25.1	001 11001	100110 1001	100110 1001
D26.0	000 11010	010110 1011	010110 0100	D26.1	001 11010	010110 1001	010110 1001
D27.0	000 11011	110110 0100	001001 1011	D27.1	001 11011	110110 1001	001001 1001
D28.0	000 11100	001110 1011	001110 0100	D28.1	001 11100	001110 1001	001110 1001
D29.0	000 11101	101110 0100	010001 1011	D29.1	001 11101	101110 1001	010001 1001
D30.0	000 11110	011110 0100	100001 1011	D30.1	001 11110	011110 1001	100001 1001
D31.0	000 11111	101011 0100	010100 1011	D31.1	001 11111	101011 1001	010100 1001
D0.2	010 00000	100111 0101	011000 0101	D0.3	011 00000	100111 0011	011000 1100
D1.2	010 00001	011101 0101	100010 0101	D1.3	011 00001	011101 0011	100010 1100
D2.2	010 00010	101101 0101	010010 0101	D2.3	011 00010	101101 0011	010010 1100
D3.2	010 00011	110001 0101	110001 0101	D3.3	011 00011	110001 1100	110001 0011
D4.2	010 00100	110101 0101	001010 0101	D4.3	011 00100	110101 0011	001010 1100

Preliminary Data Sheet

High Performance Encoder/Decoder for Fibre Channel or Proprietary Serial Links

Data Byte Name	Bits HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj	Data Byte Name	Bits HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj
D5.2	010 00101	101001 0101	101001 0101	D5.3	011 00101	101001 1100	101001 0011
D6.2	010 00110	011001 0101	011001 0101	D6.3	011 00110	011001 1100	011001 0011
D7.2	010 00111	111000 0101	000111 0101	D7.3	011 00111	111000 1100	000111 0011
D8.2	010 01000	111001 0101	000110 0101	D8.3	011 01000	111001 0011	000110 1100
D9.2	010 01001	100101 0101	100101 0101	D9.3	011 01001	100101 1100	100101 0011
D10.2	010 01010	010101 0101	010101 0101	D10.3	011 01010	010101 1100	010101 0011
D11.2	010 01011	110100 0101	110100 0101	D11.3	011 01011	110100 1100	110100 0011
D12.2	010 01100	001101 0101	001101 0101	D12.3	011 01100	001101 1100	001101 0011
D13.2	010 01101	101100 0101	101100 0101	D13.3	011 01101	101100 1100	101100 0011
D14.2	010 01110	011100 0101	011100 0101	D14.3	011 01110	011100 1100	011100 0011
D15.2	010 01111	010111 0101	101000 0101	D15.3	011 01111	010111 0011	101000 1100
D16.2	010 10000	011011 0101	100100 0101	D16.3	011 10000	011011 0011	100100 1100
D17.2	010 10001	100011 0101	100011 0101	D17.3	011 10001	100011 1100	100011 0011
D18.2	010 10010	010011 0101	010011 0101	D18.3	011 10010	010011 1100	010011 0011
D19.2	010 10011	110010 0101	110010 0101	D19.3	011 10011	110010 1100	110010 0011
D20.2	010 10100	001011 0101	001011 0101	D20.3	011 10100	001011 1100	001011 0011
D21.2	010 10101	101010 0101	101010 0101	D21.3	011 10101	101010 1100	101010 0011
D22.2	010 10110	011010 0101	011010 0101	D22.3	011 10110	011010 1100	011010 0011
D23.2	010 10111	111010 0101	000101 0101	D23.3	011 10111	111010 0011	000101 1100
D24.2	010 11000	110011 0101	001100 0101	D24.3	011 11000	110011 0011	001100 1100
D25.2	010 11001	100110 0101	100110 0101	D25.3	011 11001	100110 1100	100110 0011
D26.2	010 11010	010110 0101	010110 0101	D26.3	011 11010	010110 1100	010110 0011
D27.2	010 11011	110110 0101	001001 0101	D27.3	011 11011	110110 0011	001001 1100
D28.2	010 11100	001110 0101	001110 0101	D28.3	011 11100	001110 1100	001110 0011
D29.2	010 11101	101110 0101	010001 0101	D29.3	011 11101	101110 0011	010001 1100
D30.2	010 11110	011110 0101	100001 0101	D30.3	011 11110	011110 0011	100001 1100
D31.2	010 11111	101011 0101	010100 0101	D31.3	011 11111	101011 0011	010100 1100
D0.4	100 00000	100111 0010	011000 1101	D0.5	101 00000	100111 1010	011000 1010
D1.4	100 00001	011101 0010	100010 1101	D1.5	101 00001	011101 1010	100010 1010
D2.4	100 00010	101101 0010	010010 1101	D2.5	101 00010	101101 1010	010010 1010
D3.4	100 00011	110001 1101	110001 0010	D3.5	101 00011	110001 1010	110001 1010
D4.4	100 00100	110101 0010	001010 1101	D4.5	101 00100	110101 1010	001010 1010
D5.4	100 00101	101001 1101	101001 0010	D5.5	101 00101	101001 1010	101001 1010
D6.4	100 00110	011001 1101	011001 0010	D6.5	101 00110	011001 1010	011001 1010
D7.4	100 00111	111000 1101	000111 0010	D7.5	101 00111	111000 1010	000111 1010
D8.4	100 01000	111001 0010	000110 1101	D8.5	101 01000	111001 1010	000110 1010
D9.4	100 01001	100101 1101	100101 0010	D9.5	101 01001	100101 1010	100101 1010
D10.4	100 01010	010101 1101	010101 0010	D10.5	101 01010	010101 1010	010101 1010

Data Byte Name	Bits HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj	Data Byte Name	Bits HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj
D11.4	100 01011	110100 1101	110100 0010	D11.5	101 01011	110100 1010	110100 1010
D12.4	100 01100	001101 1101	001101 0010	D12.5	101 01100	001101 1010	001101 1010
D13.4	100 01101	101100 1101	101100 0010	D13.5	101 01101	101100 1010	101100 1010
D14.4	100 01110	011100 1101	011100 0010	D14.5	101 01110	011100 1010	011100 1010
D15.4	100 01111	010111 0010	101000 1101	D15.5	101 01111	010111 1010	101000 1010
D16.4	100 10000	011011 0010	100100 1101	D16.5	101 10000	011011 1010	100100 1010
D17.4	100 10001	100011 1101	100011 0010	D17.5	101 10001	100011 1010	100011 1010
D18.4	100 10010	010011 1101	010011 0010	D18.5	101 10010	010011 1010	010011 1010
D19.4	100 10011	110010 1101	110010 0010	D19.5	101 10011	110010 1010	110010 1010
D20.4	100 10100	001011 1101	001011 0010	D20.5	101 10100	001011 1010	001011 1010
D21.4	100 10101	101010 1101	101010 0010	D21.5	101 10101	101010 1010	101010 1010
D22.4	100 10110	011010 1101	011010 0010	D22.5	101 10110	011010 1010	011010 1010
D23.4	100 10111	111010 0010	000101 1101	D23.5	101 10111	111010 1010	000101 1010
D24.4	100 11000	110011 0010	001100 1101	D24.5	101 11000	110011 1010	001100 1010
D25.4	100 11001	100110 1101	100110 0010	D25.5	101 11001	100110 1010	100110 1010
D26.4	100 11010	010110 1101	010110 0010	D26.5	101 11010	010110 1010	010110 1010
D27.4	100 11011	110110 0010	001001 1101	D27.5	101 11011	110110 1010	001001 1010
D28.4	100 11100	001110 1101	001110 0010	D28.5	101 11100	001110 1010	001110 1010
D29.4	100 11101	101110 0010	010001 1101	D29.5	101 11101	101110 1010	010001 1010
D30.4	100 11110	011110 0010	100001 1101	D30.5	101 11110	011110 1010	100001 1010
D31.4	100 11111	101011 0010	010100 1101	D31.5	101 11111	101011 1010	010100 1010
D0.6	110 00000	100111 0110	011000 0110	D0.7	111 00000	100111 0001	011000 1110
D1.6	110 00001	011101 0110	100010 0110	D1.7	111 00001	011101 0001	100010 1110
D2.6	110 00010	101101 0110	010010 0110	D2.7	111 00010	101101 0001	010010 1110
D3.6	110 00011	110001 0110	110001 0110	D3.7	111 00011	110001 1110	110001 0001
D4.6	110 00100	110101 0110	001010 0110	D4.7	111 00100	110101 0001	001010 1110
D5.6	110 00101	101001 0110	101001 0110	D5.7	111 00101	101001 1110	101001 0001
D6.6	110 00110	011001 0110	011001 0110	D6.7	111 00110	011001 1110	011001 0001
D7.6	110 00111	111000 0110	000111 0110	D7.7	111 00111	111000 1110	000111 0001
D8.6	110 01000	111001 0110	000110 0110	D8.7	111 01000	111001 0001	000110 1110
D9.6	110 01001	100101 0110	100101 0110	D9.7	111 01001	100101 1110	100101 0001
D10.6	110 01010	010101 0110	010101 0110	D10.7	111 01010	010101 1110	010101 0001
D11.6	110 01011	110100 0110	110100 0110	D11.7	111 01011	110100 1110	110100 1000
D12.6	110 01100	001101 0110	001101 0110	D12.7	111 01100	001101 1110	001101 0001
D13.6	110 01101	101100 0110	101100 0110	D13.7	111 01101	101100 1110	101100 1000
D14.6	110 01110	011100 0110	011100 0110	D14.7	111 01110	011100 1110	011100 1000
D15.6	110 01111	010111 0110	101000 0110	D15.7	111 01111	010111 0001	101000 1110
D16.6	110 10000	011011 0110	100100 0110	D16.7	111 10000	011011 0001	100100 1110

Data Byte Name	Bits HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj	Data Byte Name	Bits HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj
D17.6	110 10001	100011 0110	100011 0110	D17.7	111 10001	100011 0111	100011 0001
D18.6	110 10010	010011 0110	010011 0110	D18.7	111 10010	010011 0111	010011 0001
D19.6	110 10011	110010 0110	110010 0110	D19.7	111 10011	110010 1110	110010 0001
D20.6	110 10100	001011 0110	001011 0110	D20.7	111 10100	001011 0111	001011 0001
D21.6	110 10101	101010 0110	101010 0110	D21.7	111 10101	101010 1110	101010 0001
D22.6	110 10110	011010 0110	011010 0110	D22.7	111 10110	011010 1110	011010 0001
D23.6	110 10111	111010 0110	000101 0110	D23.7	111 10111	111010 0001	000101 1110
D24.6	110 11000	110011 0110	001100 0110	D24.7	111 11000	110011 0001	001100 1110
D25.6	110 11001	100110 0110	100110 0110	D25.7	111 11001	100110 1110	100110 0001
D26.6	110 11010	010110 0110	010110 0110	D26.7	111 11010	010110 1110	010110 0001
D27.6	110 11011	110110 0110	001001 0110	D27.7	111 11011	110110 0001	001001 1110
D28.6	110 11100	001110 0110	001110 0110	D28.7	111 11100	001110 1110	001110 0001
D29.6	110 11101	101110 0110	010001 0110	D29.7	111 11101	101110 0001	010001 1110
D30.6	110 11110	011110 0110	100001 0110	D30.7	111 11110	011110 0001	100001 1110
D31.6	110 11111	101011 0110	010100 0110	D31.7	111 11111	101011 0001	010100 1110

CRC

The Fibre Channel Standard defines the insertion of a 4-byte CRC which is used to protect the Fibre Channel frame header and data field. CRC calculation is not extended to the Start of Frame or End of Frame ordered set. If SOF or EOF were corrupted in the serial data transmission, it would not be recognizable by the decoder circuit. CRC must be inserted into the Fibre Channel frame before the End of Frame word. The 32 bit CRC defined by Fibre Channel is the same CRC used by FDDI. The CRC uses the following 32 bit polynomial:

$$X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$$

The VSC7107 implements the 32 bit CRC defined by the Fibre Channel Standard. Begin CRC Calculation, End CRC Calculation, and Insert CRC are triggered by SOF and EOF commands. When CRC is enabled by asserting the CRC_EN input HIGH and a SOF ordered set is issued, CRC calculation begins. When an EOF ordered set is issued, the VSC7107 inserts CRC before sending the EOF ordered set. CRC calculation ignores IDLEs (and other ordered sets) inserted between SOF and EOF.

Fibre Channel Ordered Sets

The VSC7107 recognizes all Fibre Channel specified ordered sets. An ordered set is a sequence of characters with a specific Fibre Channel link interpretation. Table 4 contains definitions for all ordered sets recognized by the VSC7107. Each ordered set begins with byte 0 as a special K28.5 character.

The VSC7107 provides two Fibre Channel ordered sets. The user can build complete Fibre Channel packets and can differentiate between ordered sets through the use of EN_KCHAR signal. If the user provides the 28.5 byte to byte 0 and asserts EN_KCHAR HIGH, the VSC7107 will interpret the 28.5 hex "BC" as a K28.5 rather than a D28.5. The user can also use the VSC7107 CMND port to transmit Fibre Channel ordered sets.

Fibre Channel has defined ordered sets for use as frame delimiters. It also defines ordered sets such as primitive signals and primitive sequences for use in link management. Primitive signals and primitive sequences are not transmitted as part of a data frame. All Fibre Channel compliant frames have negative disparity. All primitive signals and sequences are disparity neutral, and will therefore enter and exit with the same disparity. Consequently, only the negative beginning disparity ordered sets are recognized.

The VSC7107 will transmit the IDLE primitive signal and all the primitive sequences when the appropriate condition arises. If no valid data is available for transmission, the VSC7107 will transmit the IDLE primitive signal. The decoder section of the VSC7107 will perform word synchronization based on the IDLE primitive sequence. The VSC7107 will recognize and transmit a positive beginning disparity IDLE if the POSIDLE signal is asserted high.

The VSC7107 Link Control State Machine recognizes and responds appropriately to primitive sequences. This is explained further in "Link Control State Machine" on page 52. These sequences and the IDLE sequence are the only ordered sets the VSC7107 will respond to and transmit. Refer to the ANSI X3T11 document for details on usage of other ordered sets.

Table 4: Ordered Set List

VSC7107 CMND	Ordered Set Transmission Word	Beginning RD	Description
0xxxxx	Dnn.n Dnn.n Dnn.n Dnn.n	Neg	Data
100000	K28.5 D21.5 D23.0 D23.0	Neg	SOF Connect Class1 (SOFc1)
100001	K28.5 D21.5 D23.2 D23.2	Neg	SOF Initiate Class 1 (SOFi1)
100010	K28.5 D21.5 D23.1 D23.1	Neg	SOF Normal Class 1 (SOFn1)
100011	K28.5 D21.5 D21.2 D21.2	Neg	SOF Initiate Class 2 (SOFi2)
100100	K28.5 D21.5 D21.1 D21.1	Neg	SOF Normal Class 2 (SOFn2)
100101	K28.5 D21.5 D22.2 D22.2	Neg	SOF Initiate Class 3 (SOFi3)
100110	K28.5 D21.5 D22.1 D22.1	Neg	SOF Normal Class 3 (SOFn3)
100111	K28.5 D21.5 D24.2 D24.2	Neg	SOF Fabric (SOFf)
101000	K28.5 D21.4 D21.3 D21.3 K28.5 D21.5 D21.3 D21.3	Neg Pos	EOF Terminate (EOF t)
101001	K28.5 D21.4 D21.4 D21.4 K28.5 D21.5 D21.4 D21.4	Neg Pos	EOF Disconnect-Terminate (EOF dt)
101010	K28.5 D21.4 D21.7 D21.7 K28.5 D21.5 D21.7 D21.7	Neg Pos	EOF Abort (EOF a)
101011	K28.5 D21.4 D21.6 D21.6 K28.5 D21.5 D21.6 D21.6	Neg Pos	EOF Normal (EOF n)
101100	K28.5 D10.4 D21.4 D21.4 K28.5 D10.5 D21.4 D21.4	Neg Pos	EOF Disconnect-Terminate-Invalid (EOF dti)
101101	K28.5 D10.4 D21.6 D21.6 K28.5 D10.5 D21.6 D21.6	Neg Pos	EOF Normal-Invalid (EOF ni)
110000	K28.5 D21.4 D21.5 D21.5 K28.5 D21.5 D21.5 D21.5	Neg Pos	Idle (IDLE) **POS IDLE is a non Fibre Channel compliant ordered set. It is only available if POSIDLE is asserted.
110001	K28.5 D21.4 D10.2 D10.2	Neg	Receiver Ready (R_RDY)
110010	-K28.7 K28.7 K28.7 K28.7	Neg	Negative Beginning Disparity Test
110011	+K28.7 K28.7 K28.7 K28.7	Pos	Positive Beginning Disparity Test
110100	K28.5 D17.4 AL_PD AL_PS	Neg	Open Port Full-Duplex (OPN xy) *
110100	K28.5 D17.4 AL_PD AL_PD	Neg	Open Port Half-Duplex(OPN xx)
110101	K28.5 D5.4 D21.5 D21.5	Neg	Close Port (CLS)
110111	K28.5 D20.4 AL_PA AL_PA	Neg	Arbitrate x (ARB x) *
111000	K28.5 D21.1 D10.4 D21.2	Neg	Offline (OLS)
111001	K28.5 D21.2 D31.5 D5.2	Neg	Not Operational (NOS)
111010	K28.5 D9.2 D31.5 D9.2	Neg	Link Reset (LR)
111011	K28.5 D21.2 D31.5 D9.2	Neg	Link Reset Response (LRR)
111100			Reserved
111101			Reserved
111110			Reserved for Test Mode
111111	K28.5 D21.0 D21.5 D21.5	Neg	Loop Initialization (LIP) *

*Note (1) * Fibre Channel ordered sets*

Loss of Synchronization State Machine

The Loss of Synchronization state machine is responsible for achieving word synchronization and for handling loss of word synchronization in a controlled manner. There are three stable receiver states in the Loss of Synchronization (LOS) state machine. They are:

- Loss of Synchronization
- Synchronization Acquired
- Reset

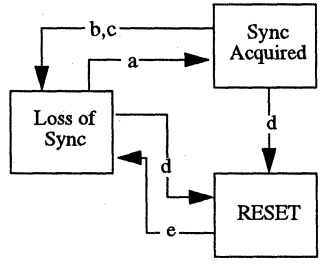
The state transition conditions are listed below:

a. Acquistion of Synchronization
b. Completion of Loss of Synchronization procedure
c. Detection of Loss of Signal condition
d. Reset condition imposed on receiver
e. Exit receiver reset condition

A receiver enters the Synchronization-Acquired state when it has detected three Ordered Sets containing commas in their leftmost bit positions without an intervening Invalid Transmission Word as specified by "Invalid Transmission Word rules" in Table 5.

The receiver state diagram is as shown in Figure 3.

Figure 3: Receiver States



Four conditions can cause a receiver in the SYNC ACQUIRED state to go into the LOSS OF SYNC state. The four conditions are:

1. Complete Loss of Sync procedure
2. Power On
3. Exit from RESET state
4. Detection of Loss of Signal

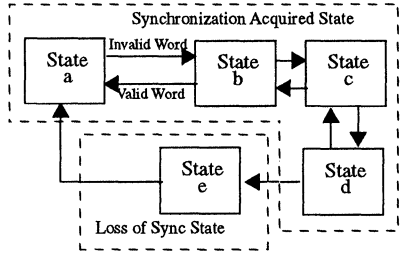
The RESET state is externally induced through the RESET signal. The RESET is a synchronous RESET and the receiver will be in the RESET state as long as RESET is high. When RESET is low and after the next word clock, the receiver will move to the LOSS OF SYNC state.

The loss of synchronization procedure defined by Fibre Channel controls the transition of the receiver state into a LOSS OF SYNC state so that single bit errors cannot cause a LOSS OF SYNC condition. The following transition states are defined in moving to a LOSS OF SYNC state. Refer to Figure 4 for further details.

State a: No-Invalid-Transmission-Word detection state.
State b: First-Invalid-Transmission-Word detection state
State c: Second-Invalid-Transmission-Word detection state
State d: Third-Invalid-Transmission-Word detection state
State e: Loss of Synchronization State

Upon detection of the fourth invalid transmission word, the receiver immediately enters the LOSS OF SYNC state and will ignore all subsequent transmission words until the receiver regains synchronization. If a valid transmission word is received prior to entry into the LOSS OF SYNC state, the state will backup one. Refer to Figure 4 for further details.

Figure 4: Loss of Sync Procedure Transition States



Three violations constitute an invalid transmission word. These violations are listed in Table 5.

Table 5: Invalid Transmission Word

Violation	*Description*
1	A code violation condition which is caused by the receipt of a transmission character not defined in Tables 22 and 23 of the FC-PH specification.
2	A valid special character is detected in the second, third, or fourth character locations.
3	A defined ordered set is received with the improper beginning disparity.

When the receiver enters the LOSS OF SYNC state, the VSC7107 notifies the system through the ERR-BUS(1). The VSC7107 also indicates to the receive FIFOs that no valid data words will be received by asserting EFREN# and the DFWEND# and DFWENDC# high. Only the decoder FIFOs are write disabled. If data is being sent, the encode FIFO signals are unaffected.

The LOS state machine is enabled and configured through the LOSCONF signal. When LOSCONF is high, all the Invalid Transmission Word rules applies. When LOSCONF is low, only a code violation will trigger an invalid word recognition. Out of place special characters or invalid beginning disparity will not be considered invalid transmission words. When POSIDLE is high, a special positive beginning disparity IDLE word (as defined in Table 4) is recognized as a valid ordered set. This positive beginning disparity is not a Fibre Channel compliant ordered set.

Link Control State Machine

The Link Control State Machine (LCSM) handles link procedures such as initialization, failure recovery, and disconnection procedures. These are useful link management functions for any serial link. The VSC7107 implements these functions as specified by the Fibre Channel Standard.

Fibre Channel is defined to be a duplexed port. The state of a given port is a function of the state of the port downstream to which it is attached. The Fibre Channel Standard defines special ordered sets (primitive sequences) to communicate port state information. Primitive sequence protocols are also defined to control the transition of a port through various port states. These protocols are initiated through time-outs, external control, or entry into a port substate.

A Fibre Channel port will be in one of four states as listed below.

1. Active State
2. Link Recovery State
3. Link Failure State
4. Offline State

The Active State is the state of an operational port. The Offline State is the state of a non-operational port. The Link Recovery State and Link Failure State are non-operational states in which a port is either attempting to recover back to an Active State or has detected an unrecoverable failed condition. The port state is indicated to the system through the LCSM(1:0) outputs on the VSC7107.

Primitive Sequences

Each state utilizes Primitive Sequence ordered sets to indicate specific conditions of the port or conditions encountered by the receiver logic of the port. A Primitive Sequence is transmitted continuously as long as the condition persists. When a primitive sequence is received and recognized, either a corresponding Primitive Sequence or IDLEs will be transmitted depending on the state of the port. Three instances of the Primitive Sequence ordered set must be received and recognized without any intervening data before the Primitive Sequence is recognized and acted upon.

Fibre Channel specifies four primitive sequences for point to point link management. These ordered sets are transmitted and received only outside a Fibre Channel frame. The LCSM transmits and recognizes these Primitive Sequences according to clauses 16.4, 16.5, and 16.6 of the ANSI FC-PH specification.

Not Operational Sequence (NOS). This primitive sequence shall be transmitted to indicate that the Port transmitting this sequence has detected a Link Failure condition or is Offline, waiting for OLS to be received. There are three defined conditions which may cause a Link Failure condition. The three conditions are:

- The Port has been in a Loss of Synchronization state for more than a Receiver-Transmitter time-out period defined to be 100 milliseconds.
- Loss of Signal is detected while not in the Offline State.
- Receiver-Transmitter time-out during Link Reset.

Offline Sequence (OLS). This primitive sequence is transmitted when a port is initiating the Link Initialization Protocol, receiving and recognizing NOS, or entering the Offline state. A port transmits the OLS primitive sequence for a minimum period of 5 milliseconds before further actions are taken. This minimum period is based on a maximum link distance of 10km.

Link Reset (LR). This primitive sequence is transmitted by a port to initiate the Link Reset Protocol or to recover from a Link time-out.

Link Reset Response (LRR). This primitive sequence is transmitted by a Port when it is receiving and recognizing the LR sequence.

Primitive Sequence Protocols

Transitioning between the four port states is accomplished through reception of a primitive sequence or through execution of one of four protocols are defined by the Fibre Channel Standard and implemented within the VSC7107. The four protocols are:

1. Link Initialization
2. On Line to Offline
3. Link Failure
4. Link Reset

Link Initialization Protocol

This protocol is required after power-on, after a hardware reset, or after an offline state. The VSC7107 powers up and executes the Link Initialization Protocol if the LCSM is enabled by setting LCEN HIGH. If LCSM is disabled, the Encoder section will not transmit the OLS primitive sequence, but will transmit what it is instructed based on the EN_DATA and EN_CMND bus. Link Initialization is also executed when either RESET, OFFLINE, or LOSIG is de-asserted from a HIGH to a LOW.

The Link Initialization Protocol causes the Port to enter the OLS Transmit State (OL1) and transmit OLS for a minimum of 5 milliseconds. After 5 milliseconds, the port should respond depending on the primitive sequence received.

Online to Offline Protocol

This protocol is executed to enter the offline state for power down or diagnostics. The VSC7107 executes the online to offline protocol by asserting the OFFLINE pin HIGH. The following series of events shall define the Online to Offline Protocol from the perspective of the Port which intends to go Offline:

1. The port enters the OLS Transmit State,
2. The Port transmits OLS for a minimum of 5 milliseconds,
3. After transmitting OLS for 5 milliseconds, the Port goes offline and diagnostics or power-down may be performed.

Link Failure

This protocol is executed when a Port has detected either a Loss of Synchronization for a period greater than the time-out period, has detected a time-out error during the Link Reset Protocol, or Loss of Signal was asserted while not in the Offline State. Upon executing the Link Failure Protocol, the Port enters the NOS Transmit State and transmit NOS while the link failure condition persists. While in the NOS Transmit State, the Port shall respond to the Primitive Sequences received according to Table 6.

Link Reset

The Link Reset Protocol will be executed following a link timeout, or upon assertion of LRESET. Upon initiation of the Link Reset, the port will enter the LR Transmit state and transmit LR. The downstream port, if functional, should respond with LR or LRR. If LR is received and recognized, the Port will enter LR Receive State and Transmit LRR. Upon receipt of LRR from the downstream port, this port will transmit IDLEs. When both ports are transmitting and recognizing IDLEs the link is reset and enters the Active State. If the appropriate response is not received within the timeout period, the Port will enter the Link Failure state.

Link Control State Transitions

The state diagram in Figure 5 shows the conditions which cause a port to transition through its various states. This state diagram only shows the state transitions caused by the reception and recognition of a primitive sequence from a distant port and does not show the sub-states. Table 6 shows a complete list of port transition conditions to all the substates. Refer to the ANSI X3T11 FC-PH specification for further information.

Figure 5: Link Control State Transitions

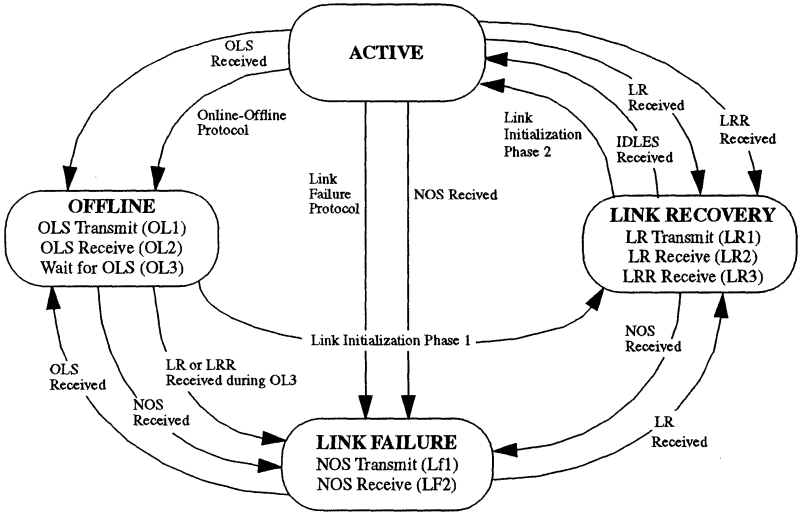


Table 6: Link Control States

	Active	*Link Recovery*			*Link Failure*		*Offline*		
	AC IDLE	*LR1 LR*	*LR2 LRR*	*LR3 IDLE*	*LF1 OLS*	*LF2 NOS*	*OL1 OLS*	*OL2 LR*	*OL3 NOS*
L >> LR	LR2	LR2	-	LR2	LR2	-	LR2	LR2	LF2
L >> LRR	LR3 Note 1	LR3	LR3	-	-	-	-	LR3	LF2
L >> IDLES			AC	AC					
L >> OLS	OL2	OL2	OL2	OL2	OL2	OL2	OL2	-	OL2
L >> NOS	LF1	LF1	LF1	LF1	-	LF1	LF1	LF1	LF1
Loss of Signal	LF2	LF2	LF2	LF2	LF2	-	OL3	OL3	-
Loss of Sync > Limit	LF2	LF2	LF2	LF2	LF2	N/A	OL3	OL3	-

	Active	*Link Recovery*			*Link Failure*		*Offline*		
	AC IDLE	*LR1 LR*	*LR2 LRR*	*LR3 IDLE*	*LF1 OLS*	*LF2 NOS*	*OL1 OLS*	*OL2 LR*	*OL3 NOS*
Event Timeout (R_T_TOV)	N/A	LF2	LF2	LF2	LF2 Note 2	N/A	OL3 Note 3 Note 4	OL3 Note 5	N/A
Link Reset	LR1	-	LR1	LR1	LR1	LR1	LR1 Note 3	LR1	LR1

LEGEND
L >> means receiving from the Link.
N/A means Not Applicable.
*A ** entry means no change in state.*

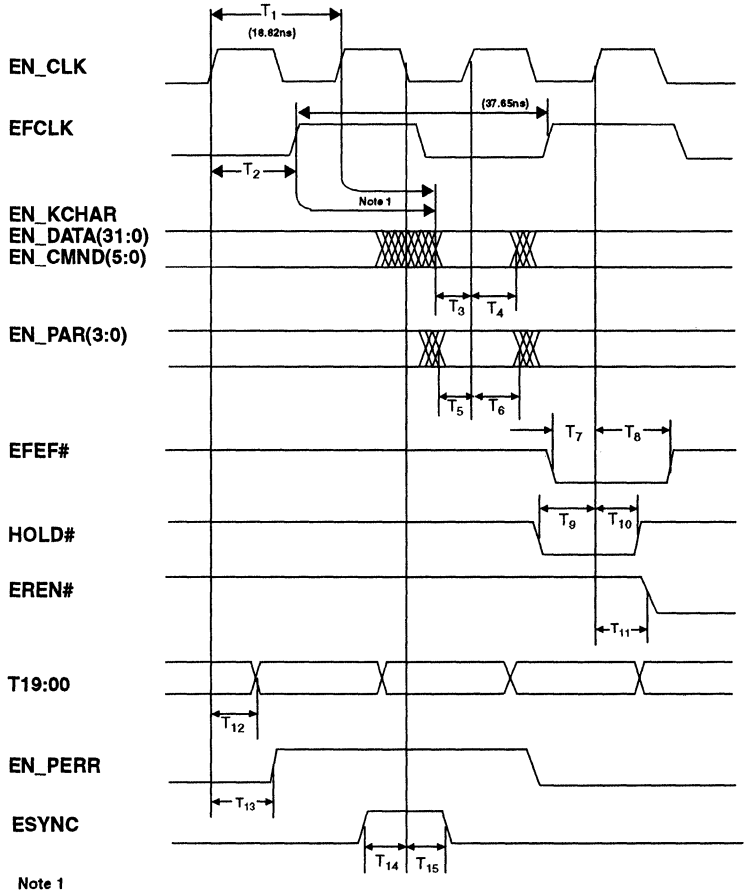
NOTES 1) A Primitive Sequence Protocol error is detected.
2) The timeout period starts timing when OLS is no longer recognized and none of the other events occur which cause a transition out of the state.
3) All events are ignored until the Port determines it is time to leave the OLS transmission state.
4) The timeout period starts timing when the Port is attempting to go online, transmits OLS, and none of the other events occur which cause a transition out of the state.
5) The timeout period starts timing when NOS is no longer recognized and none of the other events occur which cause a transition out of the state.
6) Depending on Laser safety requirements, the transmitter may enter a "pulse" transmission mode of operation when Loss of Signal is detected.

The Link Control state machine is a Fibre Channel compliant state machine. For proprietary links, this state machine may be disabled by asserting the LCEN signal LOW. Generally, LCSM forces the encoder section to send primitive sequences and asserts REN high to disable reading from the FIFO when a link failure or reset is present. When disabled, LCSM will be disconnected from the encoder section and the encoder will transmit whatever is present on the encoder inputs irrespective of a link failure. Error reporting on the ERRBUS will not be affected and the LCSM(1:0) output will continue to report LCSM states. For a proprietary link in which LCSM is disabled, no primitive sequences except IDLEs will be transmitted except under user control. The LCSM will still detect and report link failures due to loss of synchronization greater than the time-out period and loss of signal when not in the offline state. The user will then need to respond appropriately to these conditions.

AC Timing Specifications

Encoder Section

Figure 6: AC Characteristic Waveforms



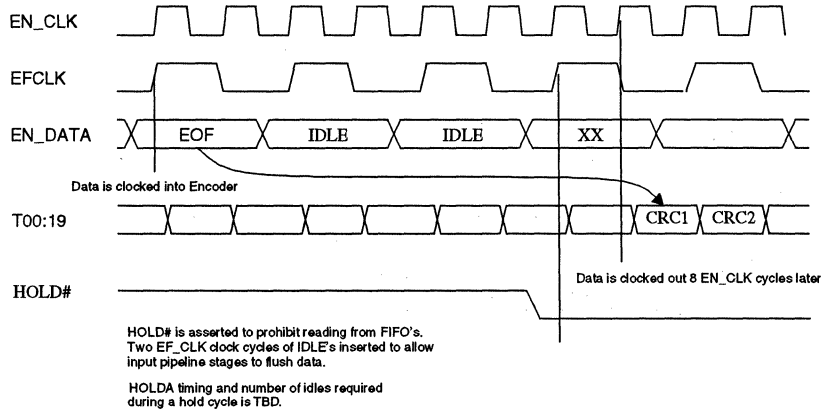
Note 1
Use EFCLK to clock system FIFO's or Data Source in 32 bit mode.
Use EN_CLK to clock system FIFO's or Data Source in 16 bit mode.
Numbers in parenthesis shows clock period for 1.0625 Gb/s operation.

Encoder Section

Table 7: Encoder AC Timing Table

Parameter	*Description*	*Min*	*Max*	*Units*	*Conditions*
T_1	Minimum Clock Period	18.0	—	ns	—
T_2	EN_CLK to EFCLK Delay	—	11.0	ns	30 pF load
T_3	Data Setup Time	5.0 7.0	— —	ns	16 bit mode 32 bit mode
T_4	Data Hold Time	1.0 1.0	— —	ns	16 bit mode 32 bit mode
T_5	EN_PAR Setup Time	4.0	—	ns	—
T_6	EN_PAR Hold Time	1.0	—	ns	—
T_7	EFEF# Setup Time	2.0	—	ns	—
T_8	EFEF# Hold Time	4.0	—	ns	—
T_9	HOLD# Setup Time	3.0	—	ns	—
T_{10}	HOLD# Hold Time	2.0	—	ns	—
T_{11}	EN_CLK to EFREN# Delay	—	11.0	ns	30 pF load
T_{12}	EN_CLK to T19:00 Delay	—	11.0	ns	20 pF load
T_{13}	EN_CLK to PERR Delay	—	14.0	ns	30 pF load
T_{14}	EN_CLK Fall to ESYNC SetupTime	2.0	—	ns	30 pF load
T_{15}	EN_CLK Fall to ESYNC Hold Time	1.0	—		—

Figure 7: Data Flow Waveforms



Decoder Section

Figure 8: Data Flow Waveforms

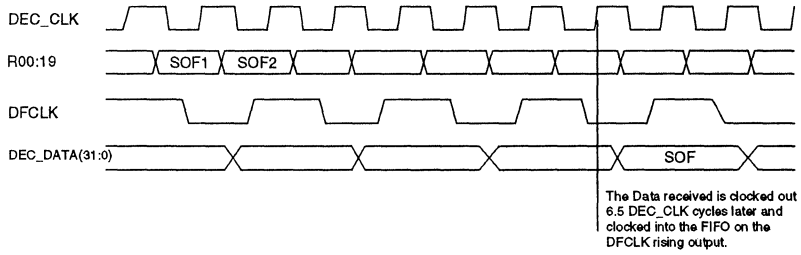
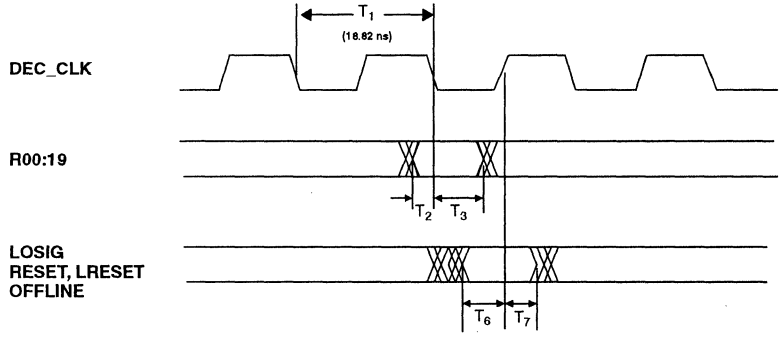


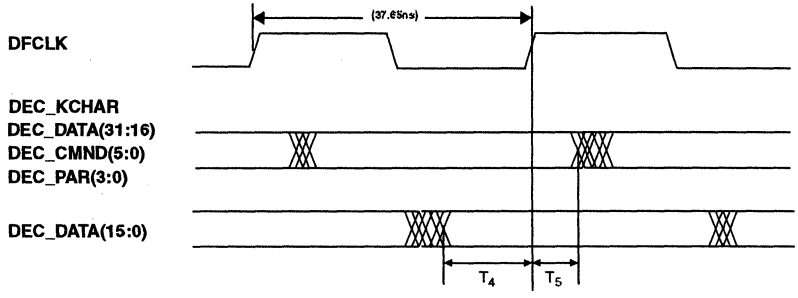
Figure 9: Receiver Timing Waveforms



Numbers in parenthesis shows clock period for 1.0625 Gb/s operation.

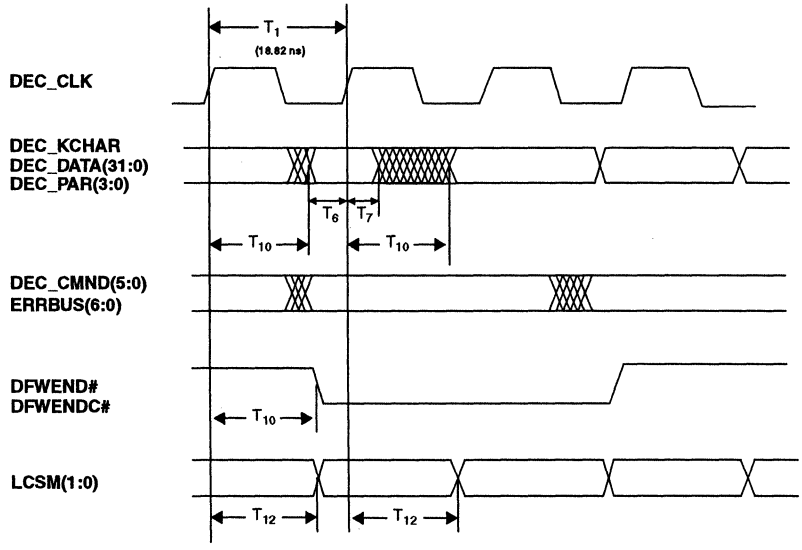
Decoder Section

Figure 10: System Timing Waveforms (32 Bit Case)



Numbers in parenthesis shows clock period for 1.0625 Gb/s operation.

Figure 11: System Timing Waveforms (16 Bit Case)



Use of DEC_CLK for clocking system FIFO's
Numbers in parenthesis shows clock period for 1.0625 Gb/s operation.

Figure 12:

Decoder Section

Figure 13: AC Timing Characteristics Waveforms (32 Bit Case)

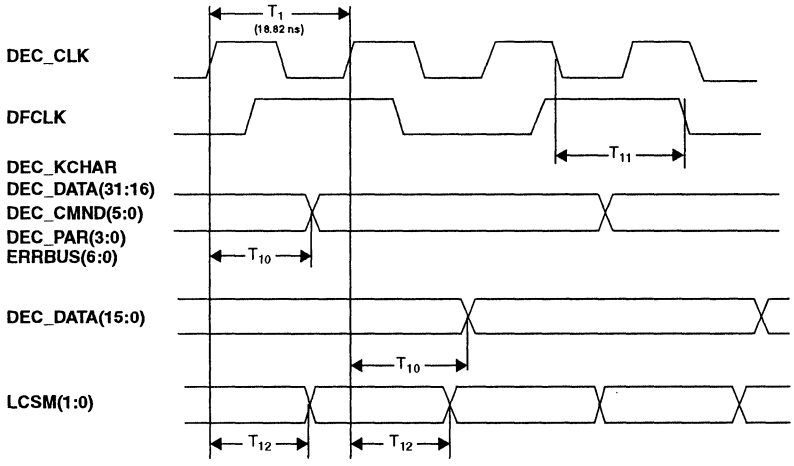


Table 8: Decoder AC Timing Table

Parameter	*Description*	*Min*	*Max*	*Units*	*Conditions*
T_1	Minimum Clock Period	18.0	—	ns	—
T_1	Duty Cycle	45	55	%	—
T_2	R19:00 Data Setup Time	1.0	—	ns	—
T_3	R19:00 Data Hold Time	5.0	—	ns	—
T_4	Data Valid Setup to DFCLK Rise	8.0	—	ns	30 pF load
T_5	Data Valid Hold from DFCLK Rise	3.0	—	ns	30 pF load
T_6	Data Valid Setup to DEC_CLK (16 Bit)	4.0	—	ns	30 pF load
T_7	Data Valid Hold from DEC_CLK (16 Bit)	2.0	—	ns	30 pF load
T_8	Control Signals Setup Time	2.0	—	ns	—
T_9	Control Signals Hold Times	2.0	—	ns	—
T_{10}	DEC_CLK to Data Out Delay	2.0	14.0	ns	30pF load
T_{11}	DEC_CLK to DFCLK Delay	—	17.0	ns	30 pF load
T_{12}	DEC_CLK to LCSM(1:0)	—	14.0	ns	20pF load

Electrical Specifications

Table 9: Absolute Maximum Ratings

Parameters	*Description*	*Limit*
V_{CC}	+5V Power Supply Voltage	-0.5V to +5.5V
V_{IN}	TTL Input Voltage Applied	-0.5V to V_{DD} + 0.5V
I_{OUT}	TTL Output Current	TBD
I_{OUT}	(DC, output High)	TBD
T_C	Cast Temperature under Bias	-55°C to +125°C
T_{STG}	Storage Temperature	TBD

Table 10: Recommended Operating Conditions

Parameters	*Description*	*Limit*
V_{DD}	Power Supply Voltage	+5.0V + 5%
T	Operating Temperature Range	0°C to +70°C(2)

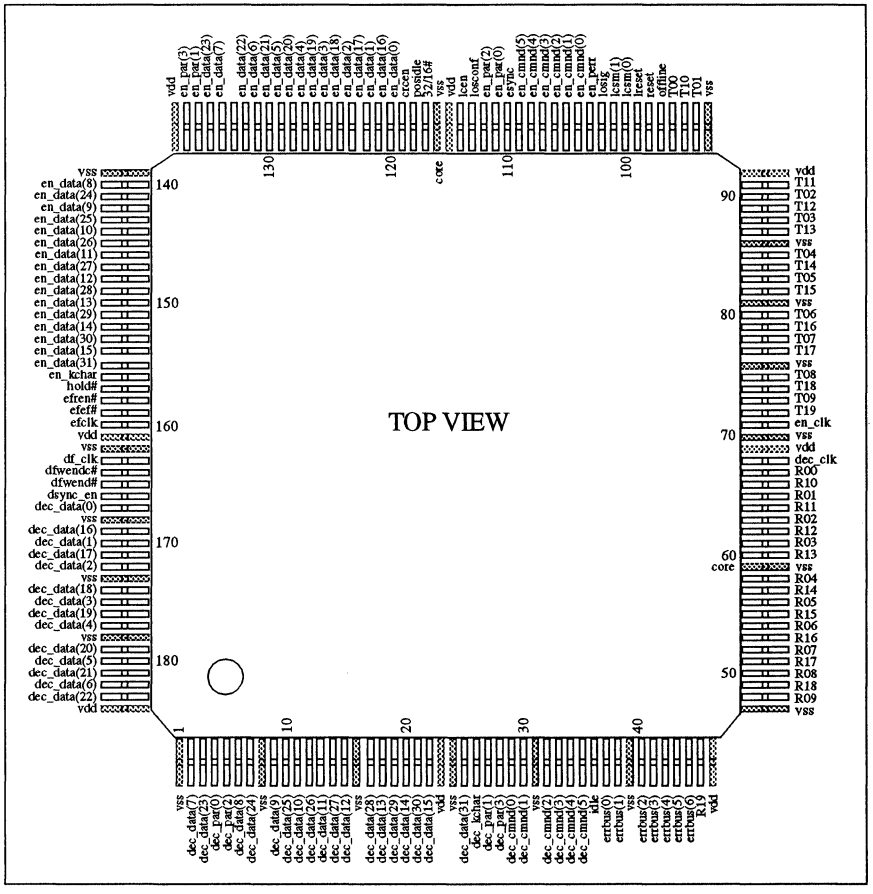
Notes: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

(2) Ambient temperature.

Table 11: DC Characteristics

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{OH}	Output HIGH TTL Voltage	2.4	—	—	V	I_{OH} = -4.0mA
V_{OL}	Output LOW TTL Voltage	—	—	0.4	V	I_{OL} = +4.0mA (for EFCLK, EFREN#, I_{OL} = +8.0mA)
V_{IH}	Input HIGH TTL Voltage	2.2	—	—	V	—
V_{IL}	Input LOW TTL Voltage	—	—	0.8	V	—
I_{IH}	TTL Output HIGH Current	-10	—	+10	µA	$V_{IN} = V_{DD}$
I_{IHP}	TTL Output HIGH Current for I/O with pull up or pull down macros	+10	—	+200	µA	$V_{IN} = V_{DD}$
I_{IL}	TTL Output LOW Current	-10	—	+10	µA	$V_{IN} = V_{SS}$
I_{ILP}	TTL Output LOW Current for I/O with pull up or pull down macros	-200	—	-10	µA	$V_{IN} = V_{SS}$
V_{DD}	Supply Voltage	4.75	5.0	5.25	V	—
I_{DD}	Supply Current	—	260	TBD	mA	Freq. = 53 MHz
P_D	Power Dissipation	—	1.3	TBD	W	—

Figure 14: Pin Connection Diagram



Pin Description Tables

Table 12: Encoder Signals

Signal Name	*Type*	*Description*
EN_DATA(31:0)	IN	32 bit Encoder Data Input Bus.
EN_KCHAR	IN	"K" Character Input which specifies to the VSC7107 whether byte0 is a special character or data character. "1" makes byte0 a special character and "0" makes byte0 a data character.
EN_PAR(3:0)	IN	Parity Inputs EN_PAR(0) - Odd Parity Input for Byte 3, EN_DATA(7:0) EN_PAR(1) - Odd Parity Input for Byte 2, EN_DATA(15:8) EN_PAR(2) - Odd Parity Input for Byte 1, EN_DATA(23:16) EN_PAR(3) - Odd Parity Input for Byte 0, EN_DATA(31:24)
EN_CMND(5:0)	IN	Six bit CMND bus for users to transmit Fibre Channel ordered sets.
EFEF#	IN	Encoder FIFO Empty Flag Input. Informs VSC7107 that there are no valid data in FIFO and the VSC7107 will issue IDLEs.
HOLD#	IN	Holds back the VSC7107 from accepting data from the FIFO. The VSC7107 will issue idles when the HOLD# is asserted low.
EFREN#	OUT	Encoder FIFO Read Enable signals the FIFO when VSC7107 is ready for data.
EN_CLK	IN	Encoder clock input. 53.125MHz for maximum data rate.
EFCLK	OUT	Encoder FIFO Clock. EN_CLK divided by 2 when configured in 32 bit mode and same as EN_CLK when configured in 16 bit mode.
ESYNC	IN	Encoder Sync. When in 16 bit mode, it informs VSC7107 which half of the word is being transmitted. High specifies first half of word. In 32 bit mode, it forces the internal state machine to the upper byte.
EN_PERR	OUT	Parity error detection output. A HIGH indicates the parity circuit has detected a parity error. In 16 bit mode, EN_PAR0 and EN_PAR1 are ignored.
T19:00	OUT	Transmission Character output of the encoder section. The 20 bit, 2 encoded byte output.

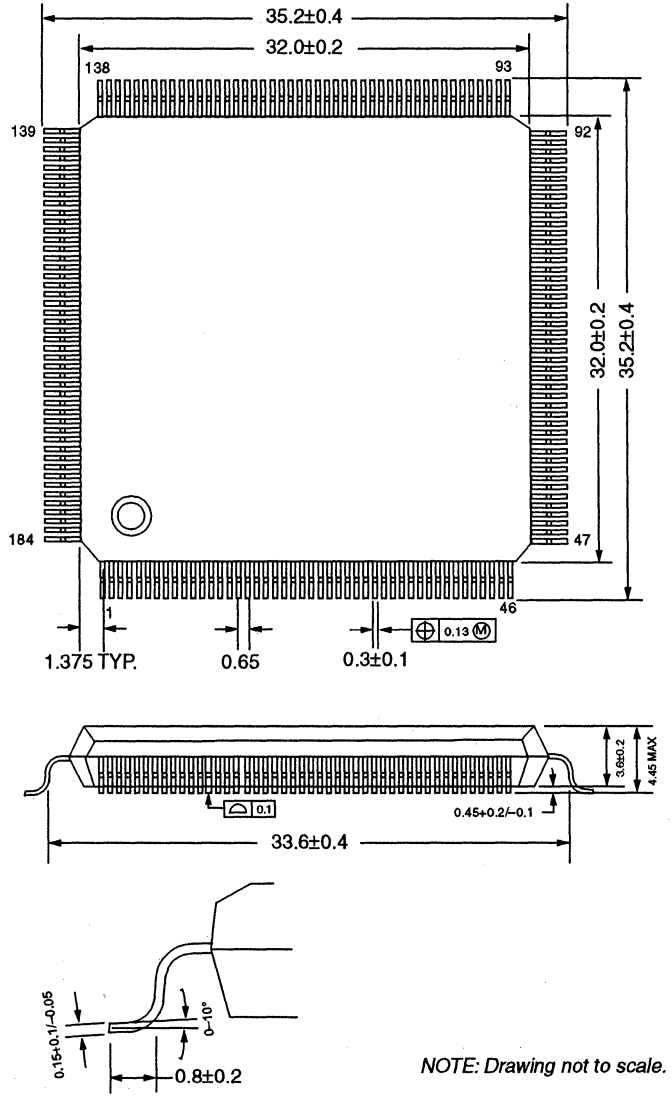
Table 13: Configuration Signals

Name	*Type*	*Description*
CRCEN	IN	Enables CRC generation and checking when asserted high.
32/16#	IN	When high configures the VSC7107 to have a 32 bit system interface and when low configures VSC7107 have a 16 bit interface.
LCEN	IN	Link Control State Machine Enabled when high.
LOSCONF	IN	Configures LOSS OF SYNCHRONIZATION state machine's invalid transmission word recognition.When high, all the Fibre Channel invalid word rules for loss of synchronization apply. When low only code violations are considered invalid words.
POSIDLE	IN	Enables generation and recognition of 32 bit positive idle when high.
DSYNC_EN	IN	Decoder Sync Enable. Enables word synchronization.

Table 14: Decoder Signals

Name	*Type*	*Description*
DEC_PAR(3:0)	OUT	Decoder parity output DEC_PAR(0) - Odd Parity Output for Byte 3, EN_DATA(7:0) DEC_PAR(1) - Odd Parity Output for Byte 2, EN_DATA(15:8) DEC_PAR(2) - Odd Parity Output for Byte 1, EN_DATA(23:16) DEC_PAR(3) - Odd Parity Output for Byte 0, EN_DATA(31:24)
DEC_DATA(31 :0)	OUT	32 bit Decoder Data Output bus.
DEC_KCHAR	OUT	Decoder K character. Informs system bus that byte0 is a "K" character.
DEC_CMND(5 :0)	OUT	Decoder Command Bus. This informs the system if data is being received or ordered sets.
IDLE	OUT	Flag when high informs the system that the VSC7107 has detected an IDLE word.
ERRBUS(6:0)	OUT	Error bus which further decodes error conditions for the system ERRBUS(0): Link Failure ERRBUS(1): Loss of Synchronization ERRBUS(2): Loss of Signal ERRBUS(3): Primitive Sequence Protocol Error ERRBUS(4): Invalid Transmission Word ERRBUS(5): Invalid CRC ERRBUS(6): Unrecognized Ordered Set
DFWENDC#	OUT	Decoder FIFO Write Enable for Data and DEC_CMND bus combined FIFO. DFWEN# is asserted when error condition exit in VSC7107 such as initialization, loss of synchronization, etc.
DFWEND#	OUT	Decoder FIFO Write Enable for Data FIFO only for systems with separate Data and Exception FIFOs. DFWEND# is asserted when error condition occurs and when ordered set is detected.
DF_CLK	OUT	Decoder FIFO Clock.
R19:00	IN	Transmission Character Input
LOSIG	IN	Loss of Signal Input
DEC_CLK	IN	Decoder Clock. Recovered clock from the VSC7106.
LCSM(1:0)	OUT	Link Control State Machine Output. LCSM(00): Active State LCSM(01): Link Recovery State LCSM(10): Offline State LCSM(11): Link Failure State
RESET	IN	Resets flip flops in state machine when HIGH. When reasserted LOW and the LCSM is enabled, the LCSM will execute Link Initialization Protocol.
LRESET	IN	Runs LCSM Link Failure Protocol when HIGH and runs the Link Reset Protocol when it is reasserted LOW.
OFFLINE	IN	Forces the Link Control State Machine to run the Online-Offline Protocol when HIGH and runs Link Initialization Protocol when reasserted LOW.

184 PQFP Package Information



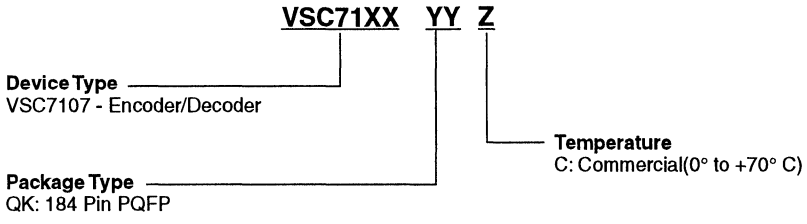
NOTE: Drawing not to scale.

Preliminary Data Sheet

High Performance Encoder/Decoder for Fibre Channel or Proprietary Serial Links

Ordering Information

The order number for this product is formed by a combination of the device number, package type, and the operating temperature range.



Note:

This preliminary data sheet does not provide all the information needed for a design. Please contact factory for additional information

Notice

This document contains information on products that are in the preproduction phase of development. The information contained in this document is based on test results and initial product characterization. Characteristic data and other specifications are subject to change without notice. Therefore, the reader is cautioned to confirm that this datasheet is current prior to placing orders.

Warning

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Data Sheet

1.0625 Gbit/sec Fibre Channel Transmitter/Receiver Chipset

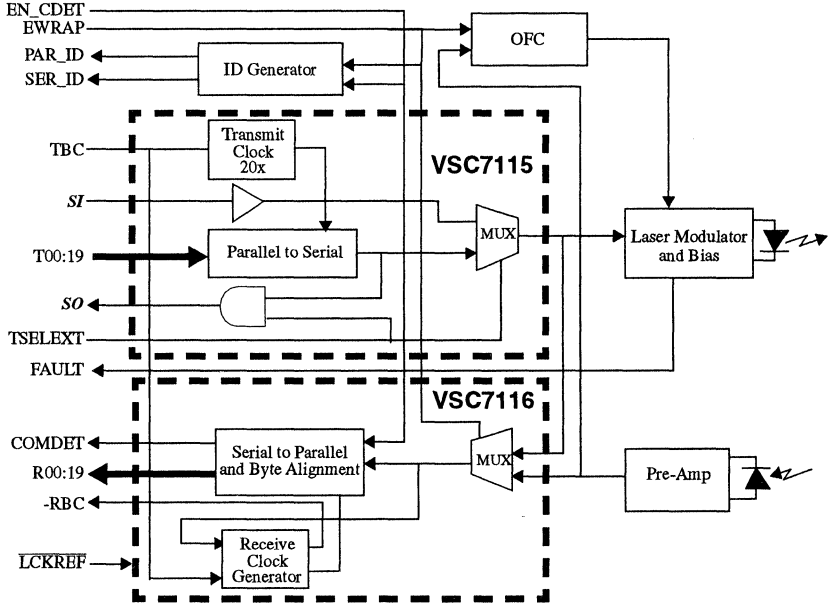
Features

- ANSI X3T11 Fibre Channel Compatible at 1.0625 Gbps
- Compliant With FCSI Gigabaud Link Module Specification
- On-chip Clock Multiplication Relieves System of High Speed Clock Generation
- 20 Bit TTL Compatible Parallel Interface
- Serial I/O Function on VSC7115 Transmitter for Class 1 Fibre Channel Switch
- High Sensitivity Differential Receiver Suitable For Both Coaxial And Optical Link Applications
- Single +3.3V Supply Operation

General Description

The VSC7115/VSC7116 chipset is compatible with the ANSI X3T11 Fibre Channel Standard and the FCSI Gigabaud Link Module specification (FCSI-301-Rev 1.0). It is ideal for building cost effective, very high speed point-to-point communications links. The chipset is designed for 1.0625 Gb/s operation. The VSC7115 accepts 8B/10B encoded TTL input data. Two parallel 10B characters are clocked into the device at 1/20 of the desired baud rate and are serialized for transmission. The VSC7116 accepts differential high speed serial inputs, extracts the clock and retimes the data from the input serial bit stream. The VSC7116 then outputs 20 bit TTL level parallel data.

Gigabaud Link Module Block Diagram



VSC7115 Transmitter Functional Description

The VSC7115 is an ANSI X3T11 (FC-PH) compatible Fibre Channel (FC) transmitter designed to work at the FC baud rate of 1.0625 Gb/s. The VSC7115 accepts 8B/10B encoded TTL input data as two parallel 10-bit characters clocked into the device at 1/20 of the desired baud rate. The VSC7115 has an on-chip PLL clock multiplier that uses the 53.125 MHz Transmit Byte Clock (TBC) to generate a 1.0625 GHz bit clock. This PLL requires no external components. Two high speed outputs are provided to facilitate loopback testing and an additional serial bypass path is provided as well. The serial bypass path is intended for use in Class I Fibre Channel switches. See Figure #1 for a block diagram of the VSC7115.

Parallel data is latched into the transmitter on the rising edge of TBC. The internally generated 53.125 MHz byte clock is the select line on a 20 to 10 bit mux which selects one of T00:09 or T10:19 to load into the 10 bit serial shift register. The shift register is clocked out to the serial outputs by the bit clock which is 20x the TBC input frequency with T00 clocked out first.

Output Enable controls are provided for each of the serial output ports. OE0 controls the primary outputs, TX+ and TX-, while OE1 controls the secondary outputs, TLX+ and TLX-. When an OE control is brought HIGH, it enables the differential output to transmit serial data. When an OE control is brought LOW, the respective output is forced to a logical HIGH state. A logical HIGH on the differential outputs will cause TX- to be LOW and TX+ to be HIGH. The secondary outputs can be used as a local loopback for system testing.

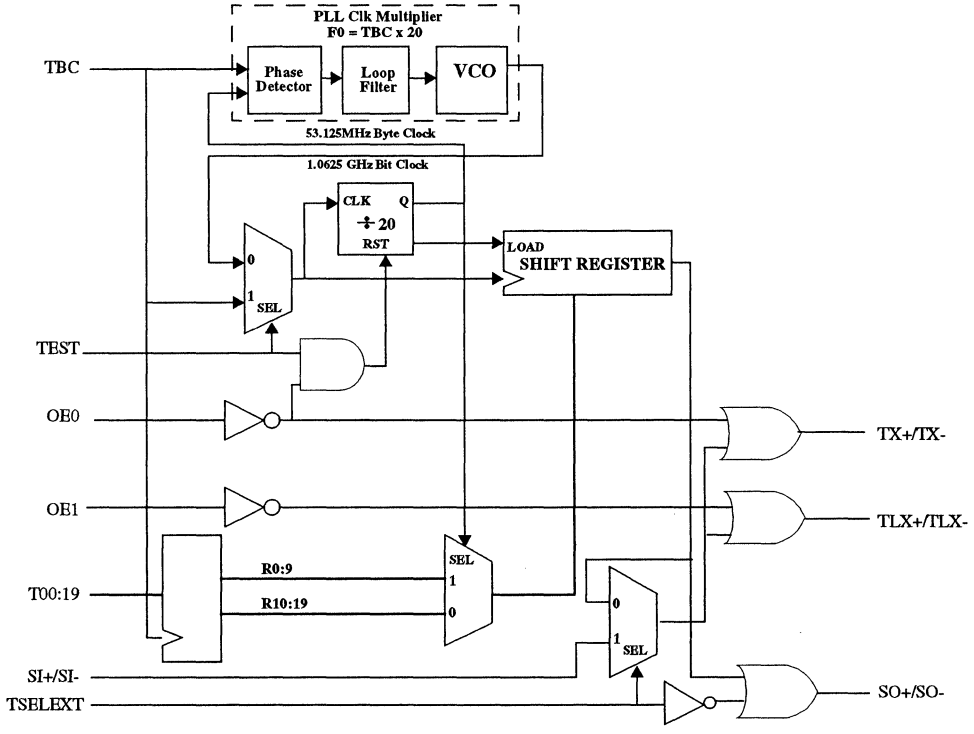
The VSC7115 controls the serial input (SI) and serial output (SO) functions defined in the Gigabaud Link Module specification through the TSELEXT signal. When TSELEXT is HIGH, data from the differential serial input, SI, is routed to the primary and loopback serial data outputs TX and TLX respectively and serialized 20-bit parallel data is routed onto the serial output SO+/SO-. When TSELEXT is LOW, the serialized 20-bit data is routed to the TX and TLX outputs and the differential SO output is set to a logical HIGH state. Shown in Table 1 are how the VSC7115 outputs are effected by TSELEXT and OE.

A TEST input is provided which replaces the PLL generated bit clock by TBC to facilitate functional testing when asserted HIGH. For normal operation, this input should be pulled LOW.

Table 15: Output Control

VSC7115 INPUTS			*VSC7115 OUTPUTS*		
TSELEXT	*OE1*	*OE0*	*SO*	*TLX*	*TX*
0	0	0	HIGH	HIGH	HIGH
0	0	1	HIGH	HIGH	T00:19
0	1	0	HIGH	T00:19	HIGH
0	1	1	HIGH	T00:19	T00:19
1	0	0	T00:19	HIGH	HIGH
1	0	1	T00:19	HIGH	SI
1	1	0	T00:19	SI	HIGH
1	1	1	T00:19	SI	SI

Figure 15: VSC7115 Transmitter Block Diagram

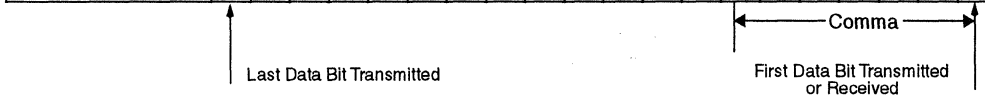


Transmission Character Interface

In Fibre Channel, an encoded byte is 10 bits and is referred to as a transmission character. A Fibre Channel word is 32 bits which is encoded into a transmission word of 40 bits. The 20 bit interface on the VSC7115 corresponds to a half transmission word. The bit ordering and its relationship to Fibre Channel bit position is shown in Figure for the VSC7115.

Figure 16: Transmission Order and Mapping to Fibre Channel Character

Parallel Data Bits	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
8B/10B Bit Position	j	h	g	f	i	e	d	c	b	a	j	h	g	f	i	e	d	c	b	a
Valid Comma Position											0	1	0	1	1	1	1	1	0	0



VSC7116 Receiver Functional Description

The VSC7116 is an ANSI compatible Fibre Channel (FC) receiver designed to work at the FC baud rate of 1.0625 Gb/s. This device is compliant with ANSI X3T11 Fibre Channel Physical Layer (FC-PH, Rev 4.4) receiver specifications. The VSC7116 accepts differential high speed serial inputs, extracts the clock and retimes the data from the input serial bit stream. The VSC7116 has internal PLL-based clock recovery circuitry which requires no external components. The serial input stream is the result of the serialization of 8B/10B encoded data by a FC compatible transmitter or any other source which produces a data stream with a transition density of 40% or greater and has a maximum run length less than 6 bit times. The retimed serial bit stream is converted into a 20 bit parallel output word. Figure 17 shows a block diagram of the VSC7116.

Serial data is received on the RX, RLX differential pairs. The PLL clock recovery circuit will lock to the serial data stream if the clock to be recovered is within 1.0% of the internally generated bit rate clock. The recovered byte clock, -RBC, is used to retime the input data stream. The 20 bit wide TTL data output (R00:19) is staggered by 5 bit times to reduce noise caused by simultaneously switching outputs. Refer to Figure 18 for the timing waveform. Staggering the 5 bit time reduces the output noise and meets the GLM receive data valid times.

Word synchronization is enabled in the VSC7116 by tying the EN_CDET pin HIGH or to V_{DD}. When synchronization is enabled, the VSC7116 constantly examines the serial data for the presence of the Fibre Channel negative beginning disparity "Comma" pattern. This pattern is "0011111". The comma pattern is not a normal data character, but the first seven bits of special characters defined specifically for synchronization or testing by Fibre Channel. Improper alignment is defined as any of the following conditions:

1) The comma sequence is not properly aligned within a the 10-bit transmission character such that R00...R06 does not equal "0011111."
2) The comma sequence straddles the boundary between two 10 bit transmission characters.

When the parallel data alignment changes in response to a comma pattern, some data which would have been presented on the parallel output port will be lost. The detection of the comma is pipelined. Depending on the required new output phase, the sync character itself may be destroyed by the synchronization operation. Nonetheless, data following the sync character will be correctly aligned. Thus if downstream logic requires detection of the sync character (for example, to accomplish ordered set alignment) then more than one sync character must be transmitted in order to guarantee that one will be forwarded out of the VSC7116 uncorrupted. Fibre Channel compliant systems require the receipt of a minimum of three ordered sets called IDLE's for word

synchronization. Ordered sets are special Fibre Channel transmission words (40-bits) that have the K28.5 sync character as the first character received. The first of these ordered sets will cause resynchronization in the VSC7116. The subsequent two ordered sets will be correctly aligned when they are received. In systems where synchronization is undesired, a LOW on EN_CDET will disable the comma detect function, and the data will be unframed.

On encountering a comma, a pulse is generated on the COM_DET output to signal that realignment of the parallel data field may have occurred. The COM_DET pulse is presented simultaneously with the actual synchronization bit sequence, (which may be corrupted as discussed above,) and has a duration equal to the data. Functional waveforms for synchronization in both modes are given in Figure 18 and Figure 19. Figure 18 shows the case when a comma is detected and no phase adjustment is necessary. It illustrates the position of the COM_DET pulse in relation to the sync character. Figure 19 shows the case where the K28.5 is detected, but out of alignment and a change in -RBC and the output data is required. Note that the VSC7116 always stretches the -RBC so it will never create a clock sliver on resynchronization.

Figure 17: VSC7116 Receiver Block Diagram

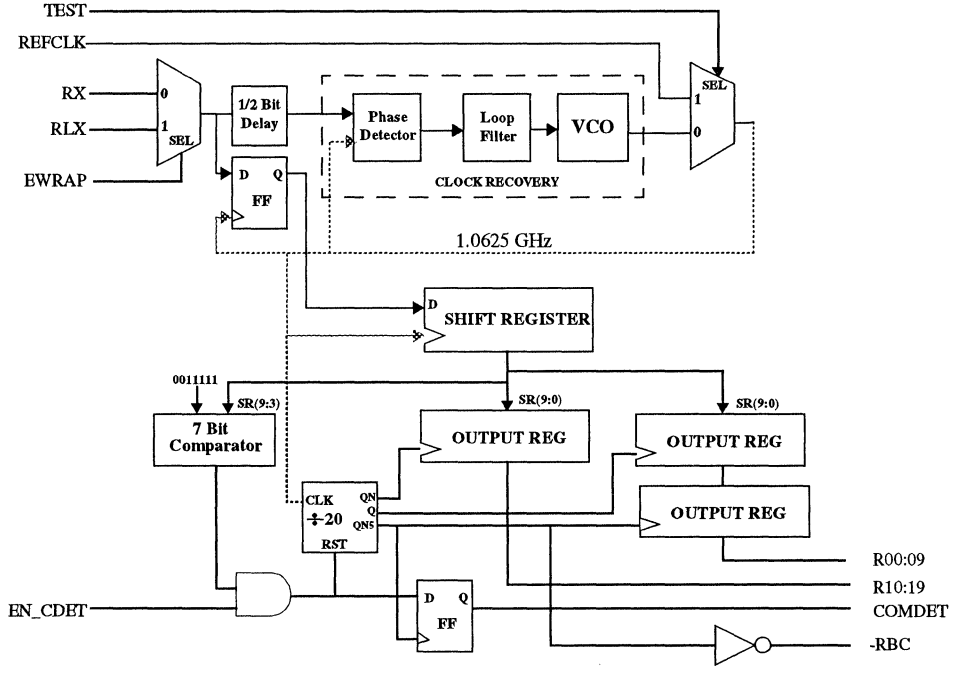


Figure 18: Data and COM_DET Timing While In Sync

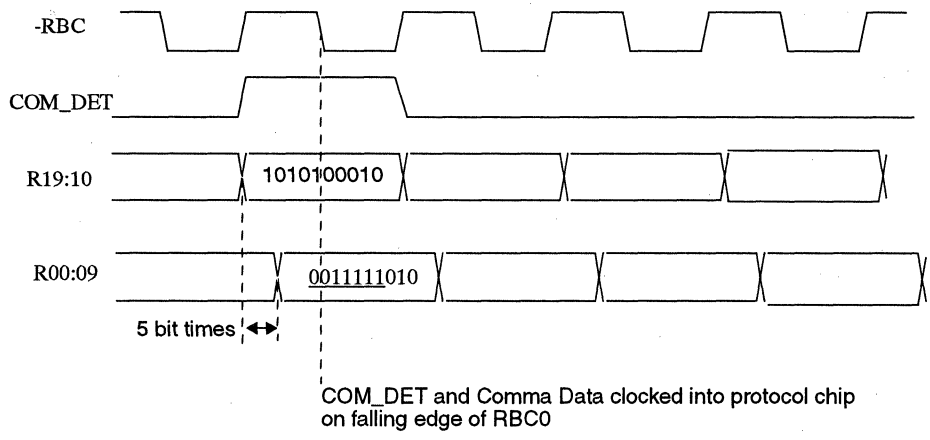
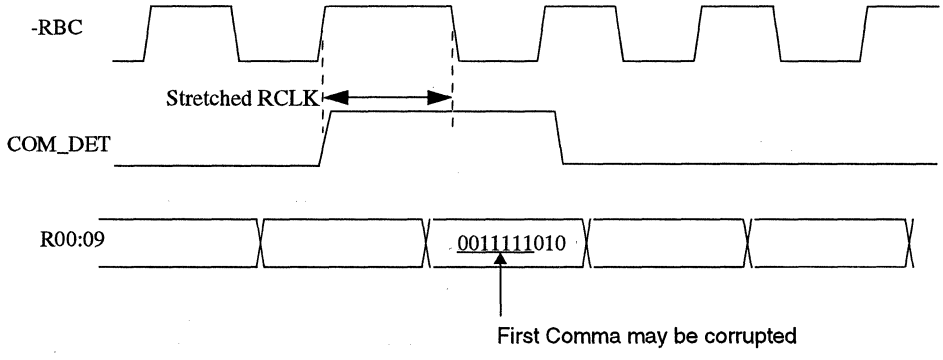


Figure 19: COM_DET and RCLK Timing When Resynchronization



-RBC is stretched and not slivered when resynchronizing

Figure 20: VSC7115 Timing Waveforms

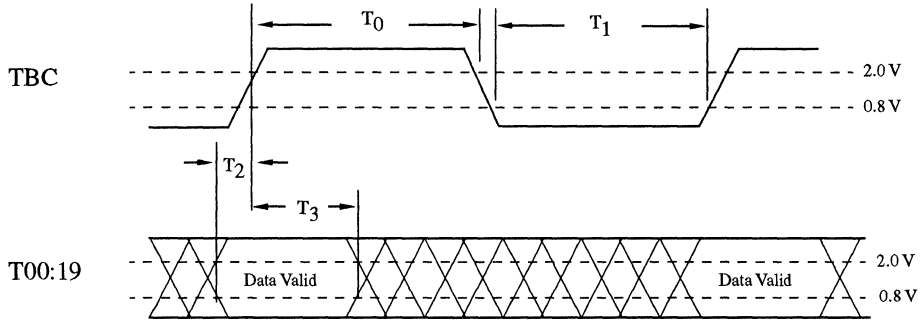
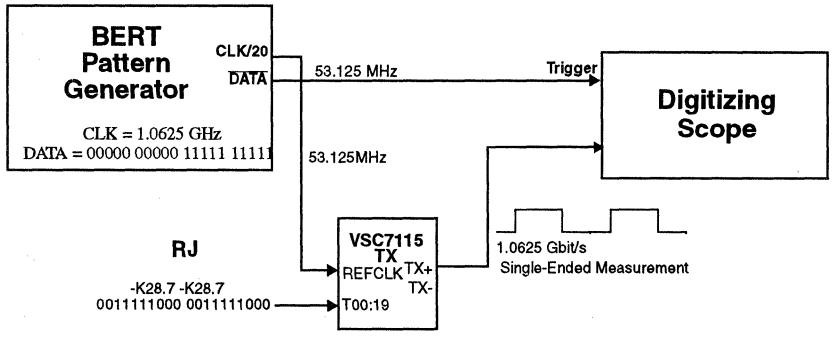


Table 16: VSC7115 AC Characteristics

Parameters	*Description*	*Min*	*Max*	*Unit*	Conditions
T_0	TBC min clock pulsewidth HIGH	6.0	—	ns	Measured 2.0V to 2.0V
T_1	TBC min clock period LOW	6.0	—	ns	Measured 0.8V to 0.8V
T_2	Data setup w.r.t. TBC rising edge	2.0	—	ns	Measured from TBC midpoint to a valid HIGH (2.0V) or valid LOW (0.8V) level.
T_3	Data hold w.r.t. TBC rising edge	3.3	—	ns	Measured from TBC midpoint to a valid HIGH (2.0V) or valid LOW (0.8V) level.
T_{TCR},T_{TCF}	TBC Rise and Fall Time	0.5	3.2	ns	0.6V to 2.2V
T_{SDR},T_{SDF}	TX+/TX-/TLX+/TLX-/SO+/SO- Rise and Fall Time		300	ps	20% to 80%, tested on a sample basis 50Ω load to V_{DD}-2V
T_{TBCJ}	TBC Jitter (Peak to Peak)		TBD	ps	
FT	TBC Frequency Tolerance		±.01	%	
T_{DC}	TBC Duty Cycle	35	65	%	Refer to GLM Duty Cycle Calculation
Transmitter Output Jitter Allocation					
T_{RJ} (RMS)	Serial data output random jitter (RMS)	—	20	ps	RMS, tested on a sample basis
T_{DJ}	Serial data output deterministic jitter (p-p)	—	100	ps	Peak to peak, tested on a sample basis

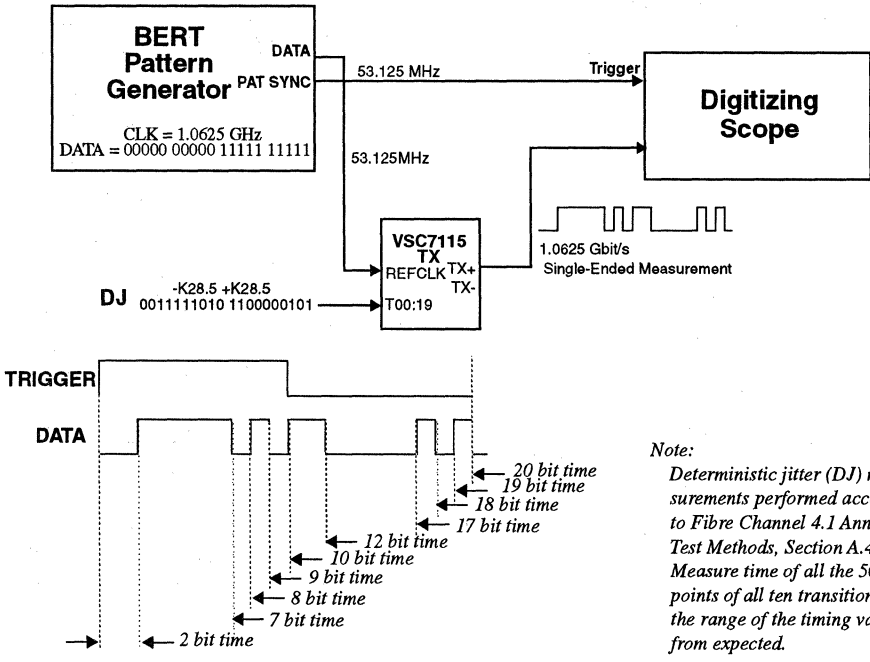
Figure 21: Jitter Measurement Method

Random Jitter Measurement



Random jitter (RJ) measurements performed according to Fibre Channel 4.1 Annex A, Test Methods, Section A.4.4. Measure standard deviation of all 50% crossing points. Peak to peak RJ is ±

Deterministic Jitter Measurement



Note:
Deterministic jitter (DJ) measurements performed according to Fibre Channel 4.1 Annex A, Test Methods, Section A.4.3. Measure time of all the 50% points of all ten transitions. DJ is the range of the timing variation from expected.

Figure 22: VSC7116 AC Timing Waveforms

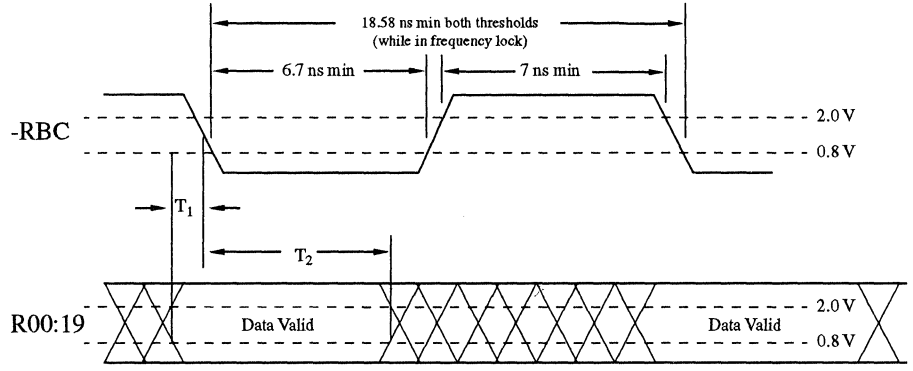


Table 17: VSC7116 AC Characteristics

Parameters	*Description*	*Min*	*Max*	*Unit*	*Conditions*
T_1	Data valid setup prior to -RBC fall	2.5	—	ns	Measured from -RBC midpoint to a valid HIGH (2.0V) or valid LOW (0.8V).
T_2	Data valid hold after -RBC fall	6.0	—	ns	Measured from -RBC midpoint to a valid HIGH(2.0V) or valid LOW (0.8V)
T_{RCR},T_{RCF}	-RBC rise and fall time	0.7	2.4	ns	0.8V to 2.0V, tested on a sample basis, 10pF load
T_{DR},T_{DF}	Data output rise and fall time	—	4.0	ns	0.8V to 2.0V, tested on a sample basis, 10pF load
T_{LOCK}	Data acquisition lock time @ 1.0625Gb/s	—	2.4	µs	8B/10B IDLE pattern, tested on a sample basis
Input Jitter Tolerance	Input data eye opening allocation at receiver input for BER ≤ 1E-12	30%	—	bit time	As specified in Fibre Channel FC-PH standard eye diagram jitter mask.

Absolute Maximum Ratings (1)

Power Supply Voltage, (V_{DD}) ..... 0.5V to +4V
PECL DC Input Voltage, (V_{INP}) ..... -0.5V to V_{DD} +0.5V
TTL DC Input Voltage, (V_{INT}) ..... -0.5V to 6.0V
DC Voltage Applied to Outputs for High Output State, ($V_{IN\ TTL}$) ..... -0.5V to V_{DD} + 0.5V
TTL Output Current (I_{OUT}), (DC, Output High) 50mA
PECL Output Current, (I_{OUT}), (DC, Output High) ..... -50mA
Case Temperature Under Bias, (T_C) ..... -55° to +125°C
Storage Temperature, (T_{STG}) ..... -65° to + 150°C
Maximum Input ESD ..... 1500 V

Recommended Operating Conditions(2)

Power Supply Voltage, (V_{DD}) ..... +3.3V ± 5%
Operating Temperature Range, (T) (3) ..... 0°C to +110°C

Notes:

1) *CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.*
2) *Vitesse guarantees the functional and parametric operation of the part under "Recommended Operating Conditions" except where specifically noted in the AC and DC Parametric Tables.*
3) *Lower limit is ambient temperature and upper limit is case temperature.*

Table 18: VSC7115 DC Characteristics *(Over recommended operating conditions).*

Parameters	*Description*	*Min*	*Typ*	*Max*	*Unit*	*Conditions*
$V_{IH(TTL)}$	Input HIGH voltage (TTL)	2.0	—	5.5	V	$I_{IH} \leq 6.6$ mA @ $V_{IH} = 5.5$ V
$V_{IL(TTL)}$	Input LOW voltage (TTL)	0	—	0.8	V	—
$I_{IH(TTL)}$	Input HIGH current (TTL)	—	—	50	µA	$V_{IN} = 2.4$ V
$I_{IL(TTL)}$	Input LOW current (TTL)	-500	—	-50	µA	$V_{IN} = 0.5$ V
V_{DD}	Supply voltage	3.14	3.3	3.47	V	±5% of $V_{DD} = 3.30$V
I_{DD}	Supply current	—	—	350	mA	Outputs open, $V_{DD} = V_{DD}$ max
P_D	Power dissipation	—	1.0	1.2	W	Outputs open, $V_{DD} = V_{DD}$ max
$\Delta V_{IN(DF)}$	Serial data differential peak to peak input swing SI+/SI-	300		2600	mVpp	AC Coupled Internally biased at $V_{DD}/2$
ΔV_{OUT}	TX+/TX-/TLX+/TLX-/SO+/SO- Single-ended output differential peak to peak voltage swing	1200	—	2200	mVpp	50Ω to $V_{DD} - 2.0$ V

Table 19: VSC7116 DC Characteristics *(Over recommended operating conditions).*

Parameters	*Description*	*Min*	*Typ*	*Max*	*Unit*	*Conditions*
$V_{OH(TTL)}$	Output HIGH voltage (TTL)	2.4	—	—	V	$I_{OH} = -1.2$ mA
$V_{OL(TTL)}$	Output LOW voltage (TTL)	—	—	0.6	V	$I_{OL} = +1.2$ mA
$V_{IH(TTL)}$	Input HIGH voltage (TTL)	2.0	—	5.5	V	$I_{IH} \leq 6.6$ mA @ $V_{IH} = 5.5$ V
$V_{IL(TTL)}$	Input LOW voltage (TTL)	0	—	0.8	V	—
I_{IH}	Input HIGH current (TTL)	—	—	50	µA	$V_{IN} = 2.4$ V
I_{IL}	Input LOW current (TTL)	-500	—	-50	µA	$V_{IN} = 0.5$ V
V_{DD}	Supply voltage	3.14	3.3	3.47	V	±5% of $V_{DD} = 3.30$v
I_{DD}	Supply current	—	—	520	mA	Outputs open, $V_{DD} = V_{DD}$ max
P_D	Power dissipation	—	1.6	1.8	W	Outputs open, $V_{DD} = V_{DD}$ max
V_{IB}	Input Bias Voltage for HS Differential Inputs	1.63 0	1.65	1.67 0	V	$V_{DD} = 3.30$V, Measure open input voltage
ΔV_{INSI}	Serial data differential peak to peak input (RX/RLX) swing	300	—	3200	mV	AC coupled Internally biased at $V_{DD}/2$

Figure 23: VSC7115 Pin Diagram

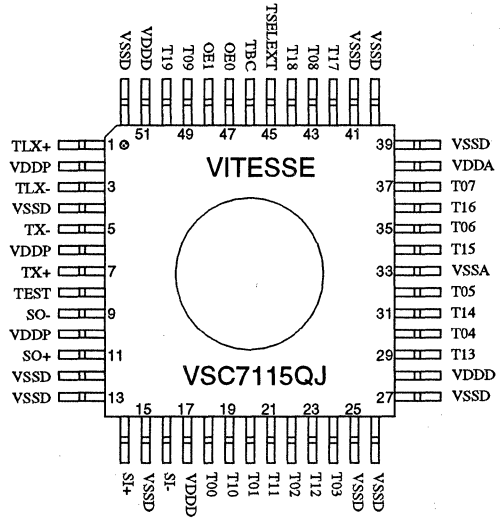
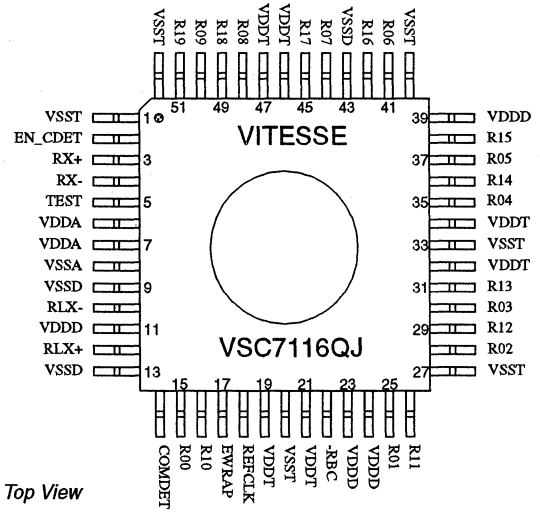


Figure 24: VSC7116 Pin Diagram



Top View

Table 20: VSC7115 Pin Description

Pin #	Name	Description
18, 20, 22, 24, 30, 32, 35, 37, 43, 49, 19, 21, 23, 29, 31, 34, 36, 42, 44, 50	T00:19	INPUT - TTL Parallel data on the T00:19 bus is clocked in on the rising edge of TBC. Bit T00 corresponding to 8b/10b bit a for the first character is transmitted first.
45	TSELEXT	INPUT - TTL Transmit SELEct EXTernal control. When HIGH, data from the serial inputs SI+, SI- is multiplexed onto the primary outputs TX and TLX, and serialized data from T00:19 is gated onto SO+, SO-. When LOW, SO+ is driven HIGH and SO- is driven LOW, and TX and TLX transmit the serialized data.
8	TEST	INPUT - TTL When HIGH, this pin puts the transmitter in test mode for factory testing. In this mode, TBC is used to serialize 20 bit input data, and the internal PLL/VCO are bypassed. In normal mode this test pin is low.
11, 9	SO+, SO-	OUTPUTS - Differential (PECL Levels Referenced to 3.3V) High speed serial outputs. When TSELEXT is high, these pins carry the serialized T00:19 data. When TSELEXT is low, these pins are gated to a valid high logic level. AC coupling recommended.
14, 16	SI+, SI-	INPUTS - Differential (Biased at VDD/2) High speed serial inputs. When TSELEXT is HIGH, this data is muxed onto the TX and TLX outputs.
47, 48	OE0, OE1	INPUT - TTL Output Enable inputs. When OE0 is high, it enables the primary outputs TX+, TX-. In test mode, when OE0 is low it is mapped to a reset for internal registers. When OE1 is high it enables the loopback outputs of TLX+, TLX-.
46	TBC	TRANSMIT BYTE CLOCK INPUT - TTL Reference Clock for the PLL clock multiplier, nominally at 53.125 MHz. Parallel data on T00:19 is latched in on the rising edge of TBC. The rising edge is also used to phase lock the internal VCO clock.
1, 3	TLX+, TLX-	OUTPUTS - DIFFERENTIAL (Biased at VDD-1.32V) Transmitter loop back outputs, enabled when OE1 is high, otherwise driven to a valid high logic level. Logic high is TLX+ = high and TLX- = low. AC coupled is required when tying TX to TLX.
7, 5	TX+, TX-	OUTPUTS - DIFFERENTIAL (Biased at VDD-1.32V) Primary transmitter outputs. These outputs carry the serialized data in the normal mode of operation. Enabled when OE0 is high. When OE0 is low, TX+ and TX- are disabled and driven to a valid high logic level. Logic high is TX+ = high and TX- = low. When TSELEXT is high, these outputs carry serial data from the SO+, SO- lines. AC coupling recommended.
17, 28, 51	VDDD	Digital Power Supply
4, 12, 13, 15, 25, 26, 27, 39, 40, 41, 52	VSSD	Digital Ground
2, 6, 10	VDDP	PECL Power Supply
38	VDDA	Analog Power Supply
33	VSSA	Analog Ground

Table 21: VSC7116 Pin Description

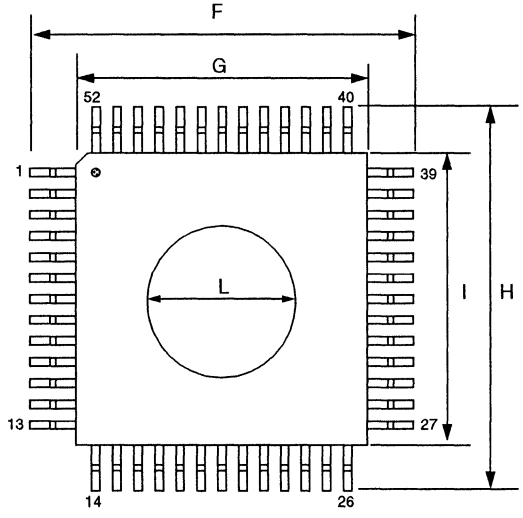
Pin #	*Name*	*Description*
15, 25, 28, 30, 35, 37, 41, 44, 48, 50, 16, 26, 29, 31, 36, 38, 42, 45, 49, 51	R00:19	OUTPUTS - TTL R0 is the first bit received on the serial data stream. The data bus R00:19 meets a setup and hold time specification with respect to the falling edge of the recovered clock -RBC. To minimize bounce due to SSO noise, bits R00:09 are clocked out 5 bit periods earlier than bits R10:19.
18	REFCLK	INPUT - TTL REFerence ClocK for the PLL clock multiplier, nominally at 53.125 MHz. The PLL will lock if the incoming serial baud rate is ±1.0% of 20X the REFCLK. For GLM applications this input will be tied to the system supplied TBC.
17	EWRAP	INPUT - TTL Loopback Enable, Electrical WRAP enable. When HIGH this pin selects the loopback serial inputs RLX for serial to parallel conversion. When low, the RX inputs are selected.
22	-RBC	OUTPUT - TTL Recovered byte clock, nominally at 53 MHz, supplied to strobe the parallel output data. On recognizing a +comma sync character in the serial data stream, -RBC is stretched, if necessary, to re-sync, and outputs the sync character on bits R00:06. The recovered clock is always extended, never truncated when resynchronization occurs
14	COMDET	OUTPUT - TTL Upon detection of a positive comma (0011111) this output goes high for one -RBC period if EN_CDET is HIGH. This output meets the same setup and hold time specified for the R00:19 parallel data outputs with respect to the falling edge of -RBC.
12, 10	RLX+, RLX-	INPUT - DIFFERENTIAL (Biased at VDD/2) Serial loopback data inputs. AC coupling recommended
3, 4	RX+, RX-	INPUT - DIFFERENTIAL (Biased at VDD/2) Received serial data inputs, AC coupling recommended.
2	EN_CDET	INPUT - TTL ENable Comma DETect. When pulled high, enables word synchronization. Word synchronization occurs when the VSC7116 detects a positive comma (0011111) in the serial data stream. In systems where the word synchronization is undesired, a low on the EN_CDET input disables the synchronization function and the data will be "un-framed".
5	TEST	INPUT - TTL When high, this pin puts the 7116 in test mode. REFCLK replaces the internal bitclk for factory testing. Normally LOW.
11, 23, 24, 39	VDDD	Digital Power Supply
9, 13, 43	VSSD	Digital Ground
19, 21, 32, 34, 46, 47	VDDT	TTL Power Supply
1, 20, 27,33, 40, 52	VSST	TTL Ground
6, 7	VDDA	Analog Power Supply
8	VSSA	Analog Ground

Data Sheet

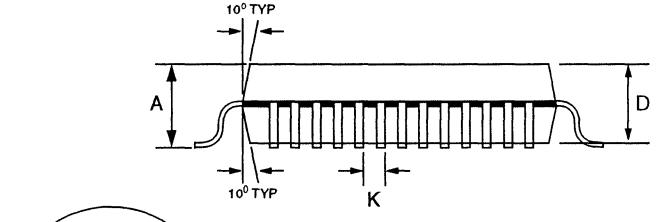
1.0625 Gbit/sec Fibre Channel Transmitter/Receiver Chipset

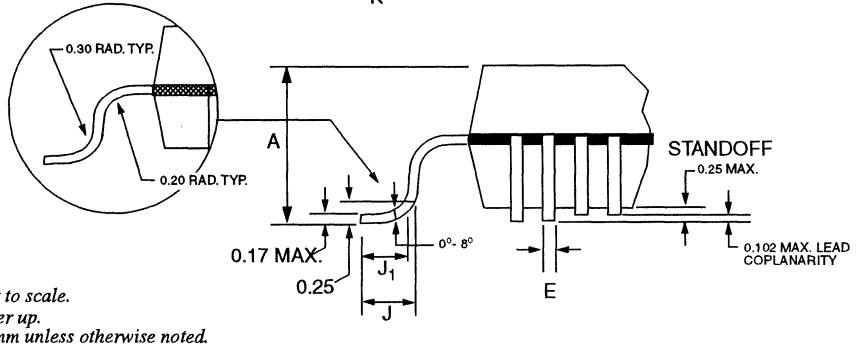
Package Information

52 Pin PQFP Package Drawings



Item	*mm*	*Tol.*
A	2.45	MAX
D	2.00	+0.10/-.05
E	0.30	±.05
F	13.20	±.25
G	10.00	±.10
H	13.20	±.25
I	10.00	±.10
J	0.88	+.15 / -.10
K	0.65	BASIC
L	3.56	±.50 DIA.

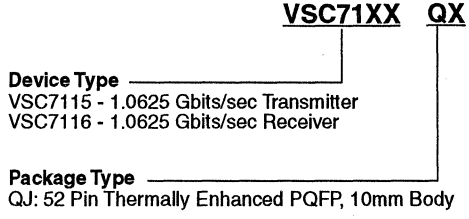




NOTES:
Drawing not to scale.
Heat spreader up.
All units in mm unless otherwise noted.
Heat spreader is connected to V_{ss}.

Ordering Information

The order number for this product is formed by a combination of the device number and package type.



Notice

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Warning

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Data Sheet

1.0625 Gbit/sec Channel Repeater / Hub Circuit

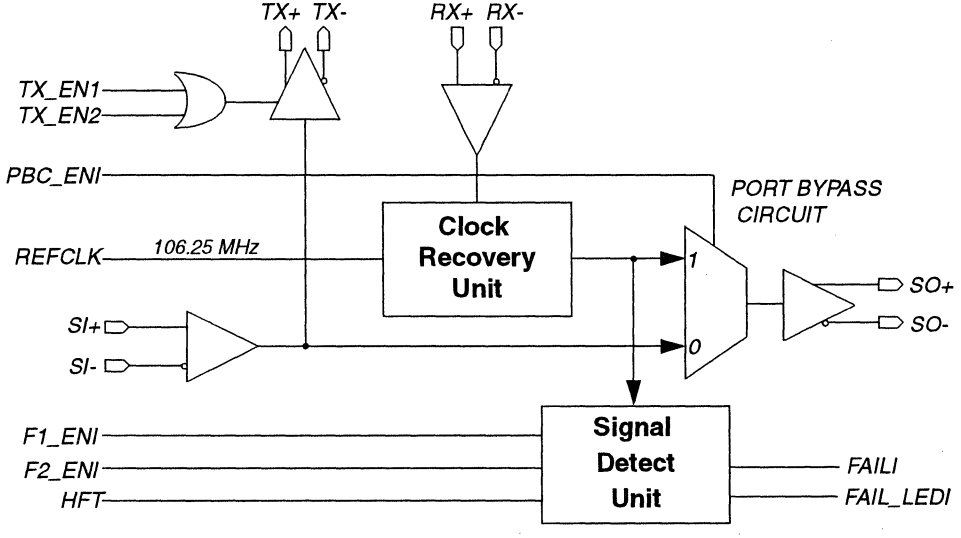
Features

- ANSI X3T11 Fibre Channel Compatible
- Monolithic Clock Recovery Unit
  - Retimes & Buffers Received Data
  - Jitter Peaking < 0.5dBNo
  - External Components
- Digital Signal Detect Unit
  - Run Length Violation Detector
  - K28.5 Detector
  - Power-Down Feature
- Port Bypass Circuit
- Suitable for Both Coaxial and Optical Link Applications
- Low Power Operation
  - < 1.3W, Typical, for Hub Mode
  - < 1.0W, Typical, for Repeater Mode
- 106.25 MHz Reference Clock
- 52-Pin, 10x10mm Thermally Enhanced PQFP
- Single 3.3V Supply

General Description

The Fibre Channel Repeater / Hub Circuit is used in full-speed (1.0625 Gb/s) Disk Arrays, Hubs and Switches. It contains a monolithic Clock Recovery Unit (CRU), a digital Signal Detect Unit (SDU) and a Port Bypass Circuit (PBC). The CRU may be used alone to implement a general purpose Repeater needed for many Disk Array and Switch applications where a retimed and buffered signal is required. The CRU, SDU and PBC may also be used together to implement a single-chip Arbitrated Loop Hub Node. As a Hub node, the VSC7120 retimes/buffers incoming serial data, detects whether a valid signal is present and allows isolation of non-functional nodes from the Loop.

VSC7120 Block Diagram



Functional Description

The VSC7120 contains three functional blocks: a Clock Recovery Unit (CRU), a Signal Detect Unit (SDU), and a Port Bypass Circuit (PBC). These circuits operate at the full 1.0625 Gb/s serial data rate and perform functions useful in Disk Arrays, Switches or Fibre Channel Arbitrated Loop (FC-AL) Hubs as repeaters and fault isolators.

The CRU is a low jitter-peaking PLL which recovers a 1.0625 GHz clock from the RX serial data input, retimes the RX data then retransmits it through the embedded PBC to the SO outputs. The CRU retimes the incoming data in order to attenuate jitter and increase the amplitude of the signal at the SO outputs. This provides downstream users of this data with a signal of known amplitude and jitter.

The SDU performs two digital checks for valid data transmission to indicate whether the external node is functional. The first check, enabled by F1_ENI being LOW, monitors the RX inputs for Fibre Channel 8B/10B run length violations. All valid 8B/10B codes have less than six consecutive identical bits so if incoming data has six or more consecutive identical bits, an error will be indicated on the FAILI/FAIL_LEDI outputs. The second method, enabled by F2_ENI, monitors the RX inputs for a bit pattern ('1111010') found in Fibre Channel Ordered Sets which should be present at least once every 20 microseconds. The SDU provides the building blocks needed by Hubs to implement an extremely reliable and repeatable mechanism for determining when to isolate the external node from the Loop and when to reconnect it to the Loop.

The PBC is a 2:1 Multiplexer which passes recovered data from the CRU to the SO outputs (if PBC_ENI is HIGH) or passes SI data to the SO outputs (if PBC_ENI is LOW). The SI inputs are always routed to the TX outputs which are gated by the TX_EN1 and TX_EN2 inputs. If both TX_EN1 and TX_EN2 are LOW, then TX+ will be HIGH and TX- will be LOW. Otherwise, the TX outputs will be enabled.

The VSC7120 has two modes of operation as follows:

Repeater Mode
Hub Mode

Repeater Mode

In Repeater Mode, the VSC7120 operates only to retime and buffer serial data from the RX inputs onto the SO output in order to attenuate jitter and amplify the signal. This mode is useful to remove high frequency jitter from the serial data and to amplify the signal to its full voltage swing. For FC-AL storage subsystems, the VSC7120 Repeater is useful in insulating the disk drive array subsystem (i.e. JBOD - Just a Bunch Of Disks) from the node connected to it as shown in Figure 1. A more detailed application example is shown in Figure 2. Input data from the upstream node may be noisy and degraded due to long cabling but the VSC7120 Repeater cleans the incoming Fibre Channel serial data prior to its use by the first disk drive. Similarly, accumulated noise inside the array may be eliminated by using a VSC7120 between the array and the downstream FC-AL device. In very large disk arrays, repeaters may be required periodically within the array to remove serial data degradation as a result of data transported over connectors, board traces, and port bypass circuits.

The Clock Recovery Unit in the VSC7120 uses an automatic lock-to-ref technique that eliminates the need for any external control logic to lock the CRU's PLL to REFCLK when data is not present on the RX input. When the RX inputs are removed, the PLL will drift away from the REFCLK frequency (i.e. 106.25 MHz +/- 100 ppm). Internal circuitry halts this drift when the PLL reaches approximately +/- 1.5% of the REFCLK fre-

quency. When RX data is reapplied, the CRU is able to lock onto the new data very quickly since the PLL is quite near the frequency of the data. This automatic Lock-to-Reference feature is extremely important in repeater applications because an intelligent state machine or microcontroller is usually not present to control this function.

Figure 25: FC-AL JBOD Application for Repeaters

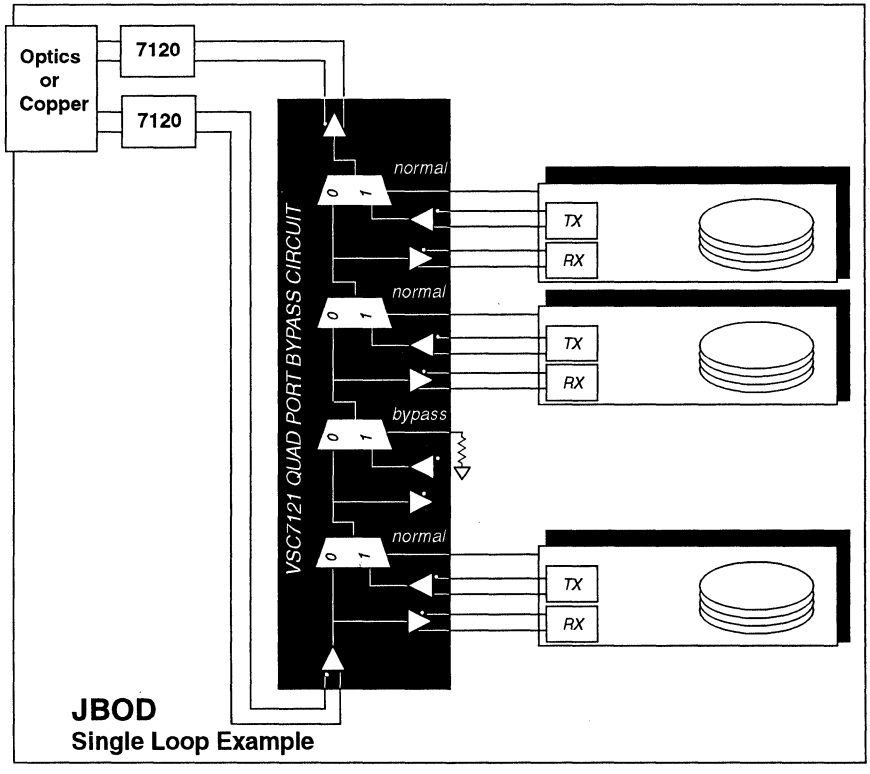
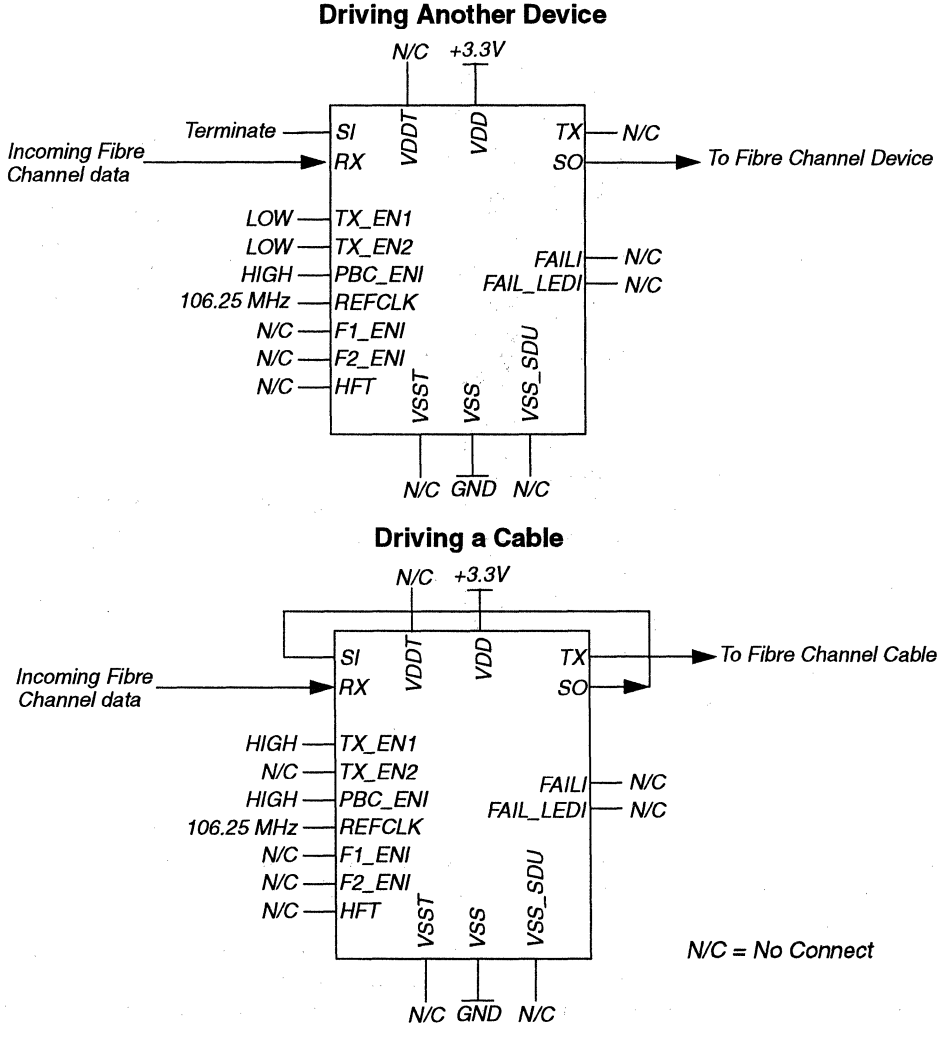


Figure 1 shows the VSC7120 being used in a repeater application. The PBC_ENI is set HIGH to pass the re-timed RX data to the SO outputs. The TX outputs would normally be disabled (TX_EN1=TX_EN2=LOW) to reduce power and noise. The SI inputs would be unused and should be terminated in order to eliminate oscillations. The SDU circuit can be powered down by disconnecting its supply pins (VSS_SDU, VSST, and VDDT) as shown in Figure 2.

Two styles of output buffers are provided on the VSC7120 to allow the user to optimize their system design. The TX outputs are full powered buffers capable of driving long cables or other Fibre Channel devices. The SO outputs are half-powered buffers which are not optimized for driving long cables but can drive Fibre

Channel devices such as O/E Modules, board traces and disk drives. In most repeater applications, SO would be adequate. However, in applications where the VSC7120 would drive long cables, the SO outputs should be connected to the SI inputs where the data will be routed to the TX outputs. This allows the user to optimize the design to reduce power and maximize signal quality.

Figure 26: VSC7120 in Repeater Mode

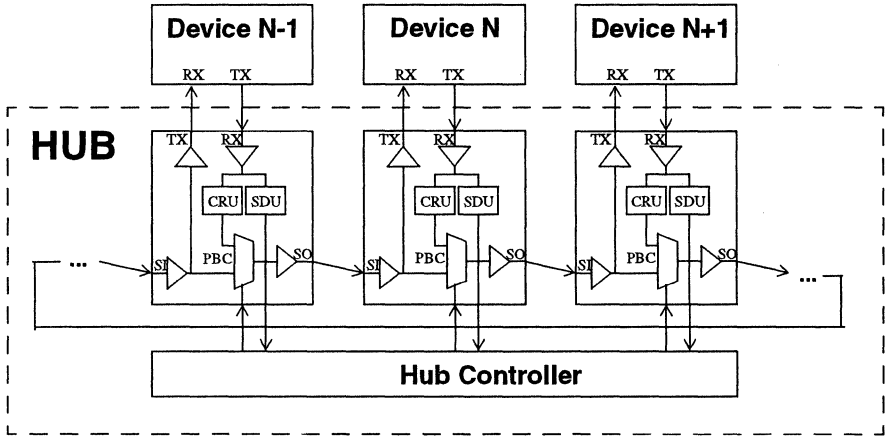


Hub Mode

The VSC7120 can act as a single-chip Hub node as shown in Figure 3. In this figure, only three Fibre Channel Arbitrated Loop nodes are shown, with each connected to external devices using point-to-point links. This implements a "Virtual Loop" using a "Physical Star" configuration. The functions of a Hub node are:

- Send data from the previous Hub node, N-1, to the external device, N (SI to TX)
- Retime / Rebuffer incoming data from the external device (RX & CRU)
- Monitor incoming data for valid Fibre Channel signals (SDU)
- Pass recovered external data to next Hub node, N+1, if valid (CRU to SO)
- Pass data from previous Hub node, N-1, to next Hub node, N+1, if external data is invalid (SI to SO)

Figure 27: FC-AL Hub Application

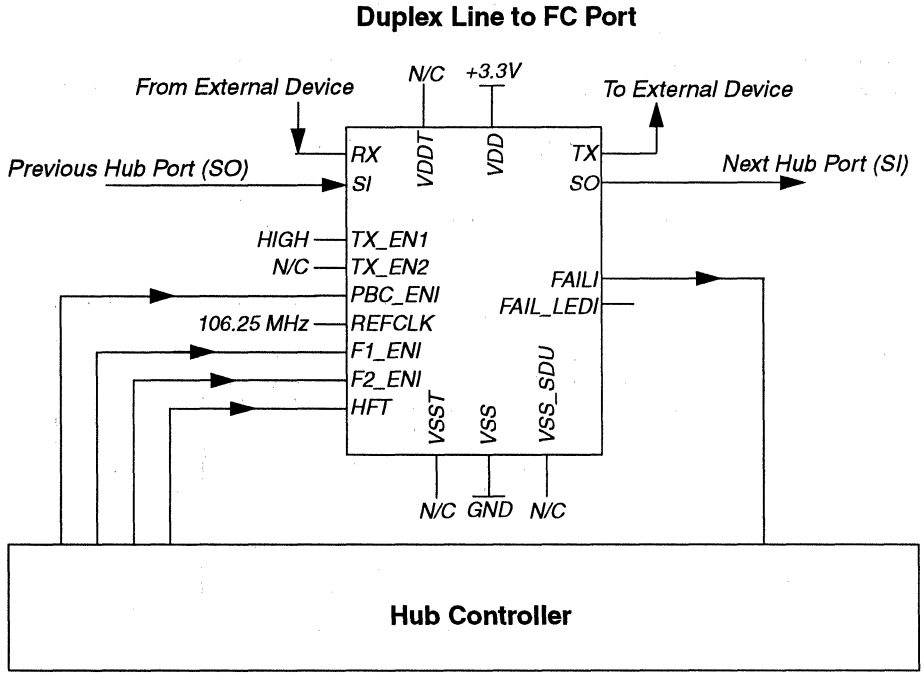


The VSC7120 implements most of the Hub node function but requires an external Hub Controller to use the SDU's outputs to control the PBC. The SDU and PBC provide the building blocks needed to isolate non-functioning external devices from the "Loop" but most customers wish to implement their own algorithms for determining when to isolate a device and when to reconnect a device. An FC-AL Hub should react only to catastrophic events such as open lines or shorts but should not respond to bit errors which are handled through standardized Fibre Channel protocols. This "Hub Controller" may be a microcontroller, FPGA or even a simple PLD-based state machine.

A more detailed view of the VSC7120 in Hub Mode is shown in Figure 4. In order to pass SI input data to TX, TX_EN1 is tied HIGH and TX_EN2 is left open. The CRU continuously locks onto RX data, retimes it and passes the recovered data to the PBC. The SDU monitors the incoming RX data under control of F1_ENI, F2_ENI and HFT (more about these signals later). The FAIL_LEDI is intended to drive an Activity LED. The FAILI output is used by the Hub Controller to configure the PBC with the PBC_ENI input. If FAILI is negated,

then the Hub would normally pass recovered RX data to the next Hub Node via the SO outputs. If FAILI is asserted, then the previous Hub Node's data on SI would normally be passed to the next Hub Node via the SO outputs. The Hub Controller should implement some sort of algorithm to qualify or filter FAILI before changing the state of PBC_ENI.

Figure 28: Fibre Channel Hub Port



Signal Detect Unit Behavior

The Signal Detect Unit indicates to the Hub Controller whether the RX input has valid Fibre Channel data. Two digital mechanisms exist to detect valid data. The first, called F1, is enabled when F1_ENI is LOW. This monitors incoming RX data for more than six consecutive ones or zeros. Valid 8B/10B data will have no more than five consecutive ones or zeros. If more than six consecutive ones or zeros are encountered, then the SDU will assert the fail outputs (FAILI and FAIL_LEDI). The second method, called F2, is enabled when F2_ENI is LOW. Valid Fibre Channel data contains K28.5 characters at least every 20 microseconds. The F2 function within the SDU looks for a 7-bit pattern found in the K28.5 ('11111010') and asserts the fail outputs if this pattern is not encountered within the 20 microsecond period.

A Fibre Channel active Hub should react only to catastrophic failure events, such as open lines, since the Fibre Channel protocol handles frame level error conditions. For this reason, the VSC7120's SDU fail outputs are designed to be asynchronously polled and processed by the Hub Controller to develop a high-level, intelligent Link Status in order to control the PBC. This allows the Hub controller, which could be a microprocessor, FPGA or even a PLD, to process all the nodes in the Hub with a common clock and simple control logic. The designer can "program" the sensitivity of the Hub Nodes to various error conditions and error rates.

The HFT, High Frequency Timer, input to the SDU controls the F1 and F2 Registers (see the Block Diagram in Figure 6). HFT is debounced internally with a clock that is one eighth of the REFCLK frequency. The HFT input is considered asynchronous to the VSC7120 since the user cannot access this internal clock but HFT does have a minimum pulse width (250 nsec). The F1_ENI and F2_ENI gate the F1 and F2 register outputs to FAILI and FAIL_LEDI.

When HFT goes low, the F1 and F2 registers are reset. The F1 detector output goes HIGH when a run length violation occurs. The F2 detector output goes LOW (indicating failure) until the K28.5 7-bit pattern is encountered within the prescribed period. F1 and F2 fault detection have different reaction times with F1 reacting quickly (<0.5 microseconds) and F2 reacting slowly (20 microseconds). Moreover, F1 and F2 operate in an opposing manner. The rising edge of HFT is commonly used to sample the fail outputs in the Hub Controller. The user must sample at the lowest rate if both are simultaneously enabled or the user may alternately poll F1 and F2 to benefit from both fast reaction time and protection from oscillating signal failures. The VSC7120 allows flexibility for the system designer to tailor fault detection for their particular system environment, failure mechanisms, and reaction requirements.

Figure 29: REFCLK Timing Waveforms

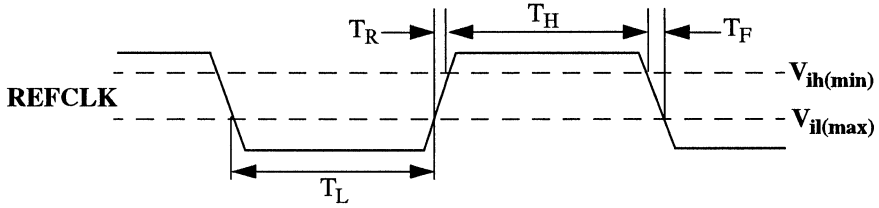


Figure 30: Block Diagram: Signal Detect Unit

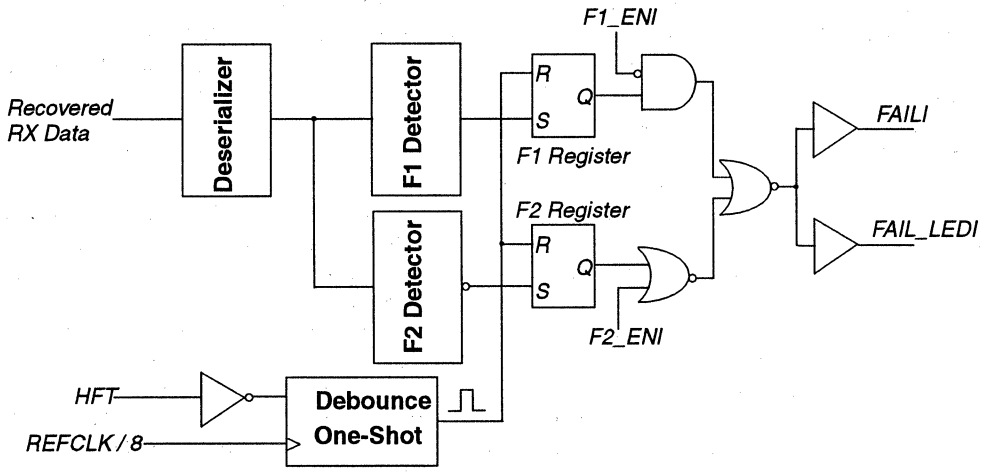
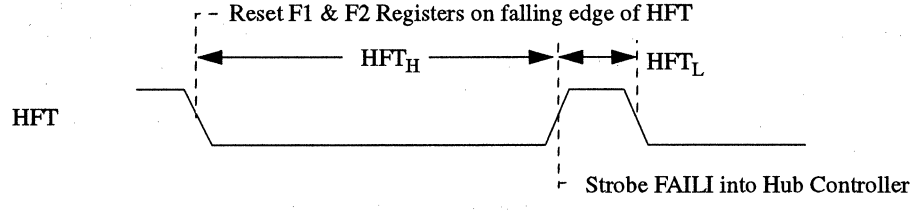


Figure 31: VSC7120 HFT Timing Waveforms



If only F1 is enabled, High and Low times should be greater than 0.5 usec.
If F2 is enabled, High and Low times should be greater than 20 usec.

AC Characteristics

Parameters	Description	Min.	Max.	Units	Conditions
HFT_H,HFT_L	HFT High and Low Time	250	—	ns	
T_H,T_L	REFCLK High and Low Time	2.5	—	ns	
T_R,T_F	REFCLK Rise and Fall Time	—	3.5	ns	
FR	REFCLK Frequency Range	100	110	MHz	Range over which both RX and Refloating be centered
FT	REFCLK Frequency Tolerance	—	100	PPM	Difference between REFCLK and RX data frequency.
DC	REFCLK Duty Cycle	40/60	—	%	
SO Jitter Allocation					
RJ	SO Random Jitter (RMS)	—	20	ps	RMS, tested on a sample basis
DJ	SO Deterministic Jitter (p-p)	—	100	ps	Peak to peak, tested on a sample basis
JT	Jitter Transfer from RX to SO	—	0.5	dB	

DC Characteristics *(Over recommended operating conditions).*

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage (TTL)	2.4	—	—	V	I_{OH} = -1.2 mA
V_{OL}	Output LOW voltage (TTL)	—	—	0.5	V	I_{OL} = +1.2 mA
V_{IH}	Input HIGH voltage (TTL)	2.0	—	—	V	
V_{IL}	Input LOW voltage (TTL)	—	—	0.8	V	
I_{IH}	Input HIGH current (TTL)	—	—	50	µA	V_{IN} = 2.4 V
I_{IL}	Input LOW current (TTL)	- 500	—	-50	µA	V_{IN} = 0.5 V
V_{DD}	Supply voltage	3.14	—	3.47	V	V_{DD} = 3.30V±5%
$I_{DD(Hub)}$	Supply Current (SDU Enabled)	—	340	450	mA	Outputs open, V_{DD} = V_{DD} max
$I_{DD(RPT)}$	Supply Current (SDU not powered)		260	350	mA	Outputs open, V_{DD} = V_{DD} max
$P_{D(HUB)}$	Power dissipation (SDU Enabled)	—	1.35	1.56	W	Outputs open, V_{DD} = V_{DD} max
$P_{D(RPT)}$	Power dissipation (SDU not powered)		0.96	1.22	W	Outputs open, V_{DD}=V_{DD} max
$\Delta V_{OUT(SO)}$	SO Output differential peak-to-peak voltage swing	1000	—	2200	mVp-p	50Ω to V_{DD} – 2.0 V
$\Delta V_{OUT(TX)}$	TX Output differential peak-to-peak voltage Swing	1200		2200	mVp-p	50Ω to V_{DD} – 2.0 V
ΔV_{IN}	Receiver differential peak-to-peak Input Sensitivity RX and SI	300	—	2600	mVp-p	V_{DD} = 3.30V, direct coupled, single ended drive, other input open

Absolute Maximum Ratings (1)

Power Supply Voltage, (V_{DD}) ..... -0.5V to +4V
PECL DC Input Voltage, (V_{INP}) ..... -0.5V to V_{DD} +0.5V
TTL DC Input Voltage, (V_{INT}) ..... -0.5V to V_{DD} + 2.5V
TTL Output Voltage, (V_{OUTT}) ..... -0.5V to V_{DD} + 0.5V
TTL Output Current (I_{OUT}), ($0V < V_{OUT} < V_{DD}$) ..... +/-50mA
PECL Output Current, (I_{OUT}), ($0V < V_{OUT} < V_{DD}$) ..... -50mA
Case Temperature Under Bias, (T_C) ..... -55° to +125°C
Storage Temperature, (T_{STG}) ..... -65° to + 150°C
Maximum Input ESD (Human Body Model) ..... 1500 V

Recommended Operating Conditions

Power Supply Voltage, (V_{DD}) ..... +3.3V ± 5%
Operating Temperature Range, (T) ..... 0°C Ambient to +110°C Case Temperature

Notes: *CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.*

Figure 32: VSC7120 Pin Identification

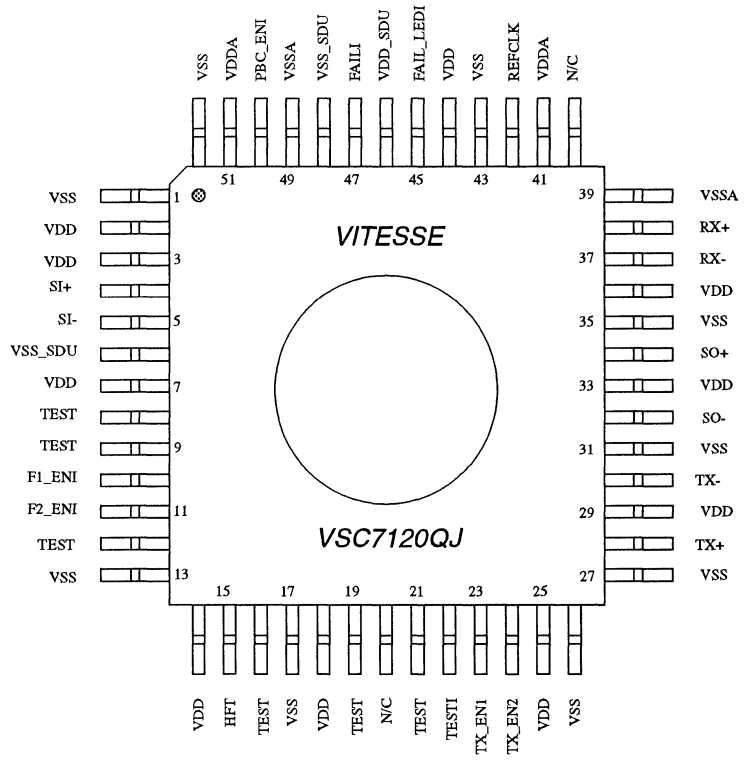


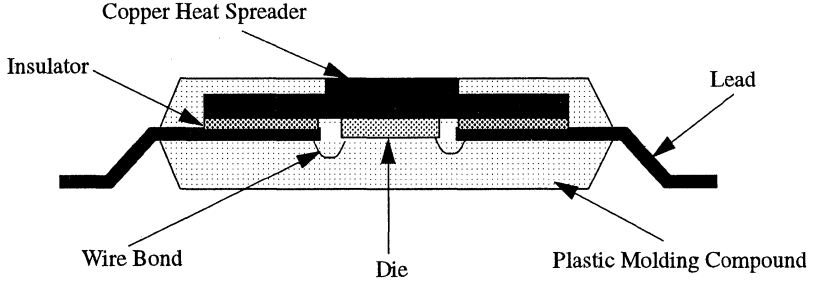
Table 22: VSC7120 Pin Description

Pin #	Name	Description
4, 5	SI+ SI-	INPUT - Differential Serial Input to TX and to the Port Bypass Circuit.
38, 37	RX+ RX-	INPUT - Differential Serial Input to the Clock Recovery Unit.
34, 32	SO+ SO-	OUTPUT - Half Power Differential (AC coupling recommended) Port Bypass Circuit output. This re-timed RX data if PBC_ENI is HIGH or SI if PBC_ENI is LOW.
28, 30	TX+ TX-	OUTPUT - Full Power Differential (AC coupling recommended) Buffered SI if TX_EN1 or TX_EN2 is HIGH. If both are LOW then TX+ is HIGH, TX- is LOW.
42	REFCLK	INPUT - TTL Reference Clock for the PLL nominally at 106.25 MHz. Rising edge active.
10	F1_ENI	INPUT - TTL Enables the F1 Detector when LOW. F1 checks RX for Run Length violations.
11	F2_ENI	INPUT - TTL Enables the F2 Detector when LOW. F2 checks RX for the presence of K28.5 Characters.
50	PBC_ENI	INPUT - TTL Controls the Port Bypass Circuit. Steers SI to SO when LOW or Recovered RX to SO when HIGH.
15	HFT	INPUT - TTL High Frequency Timer which resets the fault detection circuits to a known state. The falling edge of HFT resets the F1 and F2 RS Registers. The FAILI and FAIL_LEDI signals must be strobed prior to resetting the fault detection registers.
47, 45	FAILI FAIL_LEDI	OUTPUT - TTL When LOW, these signals indicate that the F1 or F2 Fault Detectors have detected invalid Fibre Channel data at the RX inputs. Outputs from the F1 and F2 Fault Detectors are gated by F1_ENI and F2_ENI respectively. Two identical outputs provided for fanout purposes.
23, 24	TX_EN1, TX_EN2	INPUT - TTL Disables TX outputs when both TX_EN1 and TX_EN2 are LOW. TX_EN1 has a 20K pull-up resistor and TX_EN2 has a 20K pull-down resistor.
8, 9, 12, 16, 19, 21	TEST	INPUT - TTL Factory TEST Function when HIGH. Normal operating mode when LOW.
22	TESTI	INPUT - TTL Factory Test Function when LOW. Normal operating mode when HIGH.
1,13,17,26,27,31 , 35,43,52	VSS	Ground
39,49	VSSA	Analog Ground for the CRU
6,48	VSS_SDU	Ground for SDU. Leave open during SDU power-down mode.
2,3,7,14,18,25,2 9, 33,36,44	VDD	+3.3V Power Supply
41,51	VDDA	Analog +3.3V Power Supply for the CRU
46	VDD_SDU	3.3V Power Supply for SDU. Leave open during SDU power-down mode
20,40	N/C	User No Connect pin. Do not connect these pins.

Package Thermal Characteristics

The VSC7120 is packaged into a thermally-enhanced plastic quad flatpack. This package adheres to the industry-standard EIAJ footprint for a 10x10mm body but has been enhanced to improve thermal dissipation with the inclusion of an exposed Copper Heat Spreader. The package construction is as shown in Figure 9.

Figure 33: Package Cross Section



The thermal resistance for the VSC7120 package is improved through low thermal resistance paths from the die to the exposed surface of the heat spreader and from the die to the leadframe through the heat spreader overlap of the leadframe.

Table 23: 52 PQFP Thermal Resistance

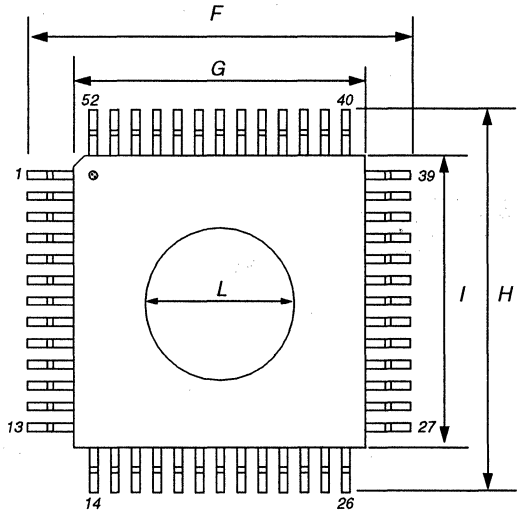
Symbol	*Description*	*Value*	*Units*
θ_{jc}	Thermal resistance from junction to case	2.5	°C/W
θ_{ca}	Thermal resistance from case to ambient in still air including conduction through the leads for a non-thermally saturated board.	37.0	°C/W
$\theta_{ca\text{-}100}$	Thermal resistance from case to ambient in 100 LPFM air	31.0	°C/W
$\theta_{ca\text{-}200}$	Thermal resistance from case to ambient in 200 LPFM air	28.0	°C/W
$\theta_{ca\text{-}400}$	Thermal resistance from case to ambient in 400 LPFM air	24.0	°C/W
$\theta_{ca\text{-}600}$	Thermal resistance from case to ambient in 600 LPFM air	22.0	°C/W

The VSC7120 is designed to operate at a maximum case temperature of up to 110 °C. The user must guarantee that the maximum case temperature specification is not violated. Given the thermal resistance of the package in still air, the user can operate the VSC7120 in still air if the ambient temperature does not exceed 60.0 °C in Hub Mode (60.0 ° C = 110 °C - 0.39 A * 3.47 V) or 73 °C in Repeater Mode (73.0 °C = 110 °C - 0.29 A * 3.47 V).

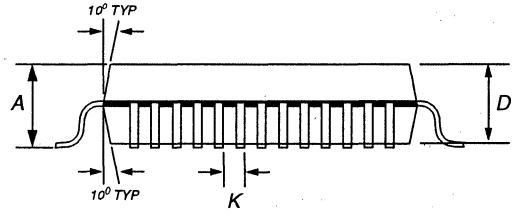
If operation above these ambient temperatures is required, then an appropriate heatsink must be used with the part or adequate airflow must be provided.

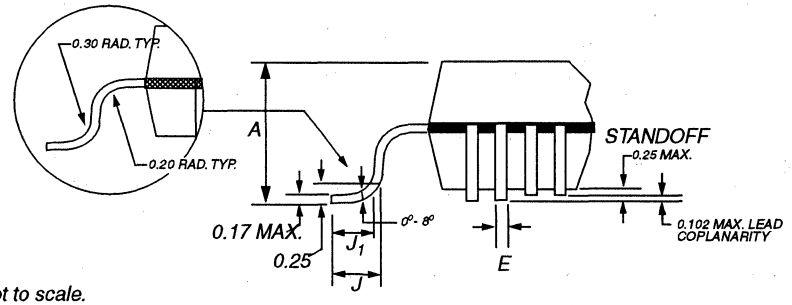
Package Information

52 PQFP Package Drawing



Item	mm	Tol.
A	2.45	MAX
D	2.00	+0.10/-.05
E	0.30	±.05
F	13.20	±.25
G	10.00	±.10
H	13.20	±.25
I	10.00	±.10
J	0.88	+.15 / -.10
K	0.65	BASIC
L	3.56	±.50 DIA.





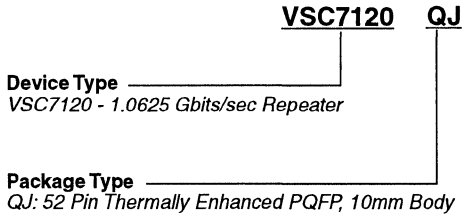
NOTES:
Drawing not to scale.
Heat spreader up.
All units in mm unless otherwise noted.

Data Sheet

1.0625 Gbit/sec Channel Repeater / Hub Circuit

Ordering Information

The order number for this product is formed by a combination of the device number and package type as shown below:

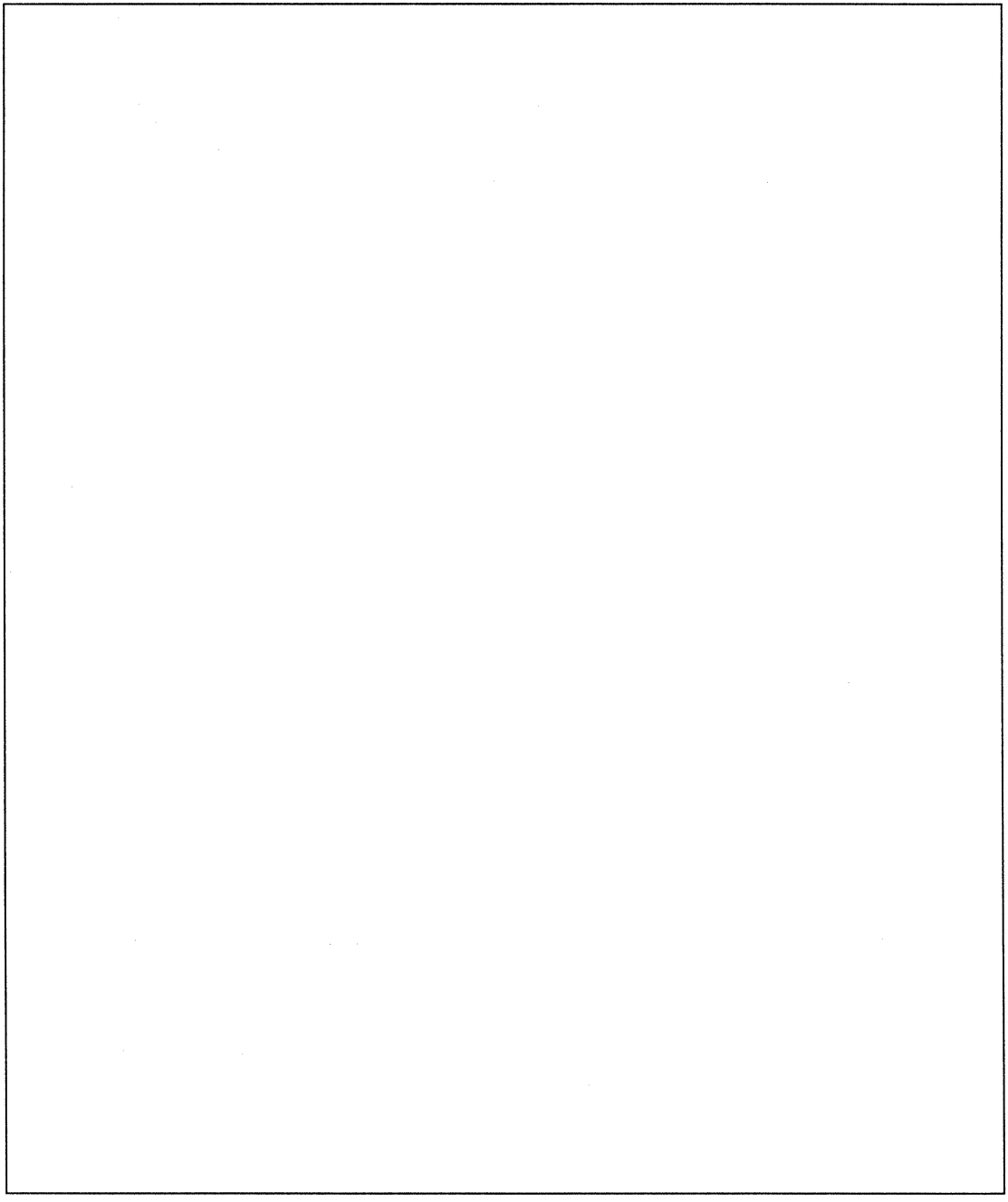


Notice

Vitesse Semiconductor Corporation reserves the right to make changes in its products specifications or other information at any time without prior notice. Therefore, the reader is cautioned to confirm that this datasheet is current prior to placing any orders. The company assumes no responsibility for any circuitry described other than circuitry entirely embodied in a Vitesse product.

Warning

Vitesse Semiconductor Corporation's product are not intended for use in life support appliances, devices or systems. Use of a Vitesse product in such applications without the written consent of the appropriate Vitesse officer is prohibited.



Data Sheet

Quad Port Bypass Circuit for 1.0625 Gbit/sec Fibre Channel Arbitrated Loop Disk Arrays

Features

- Supports ANSI X3T11 1.0625 Gbit/sec FC-AL Disk Attach for Resiliency
- Fully Differential for Minimum Jitter Accumulation.
- Quad PBC's in Single Package
- TTL Bypass Select
- High Speed, PECL I/O's Referenced to V_{DD}.
- 0.5W Typical Power Dissipation
- 3.3V Power Supply
- 44-Pin, 10mm PQFP

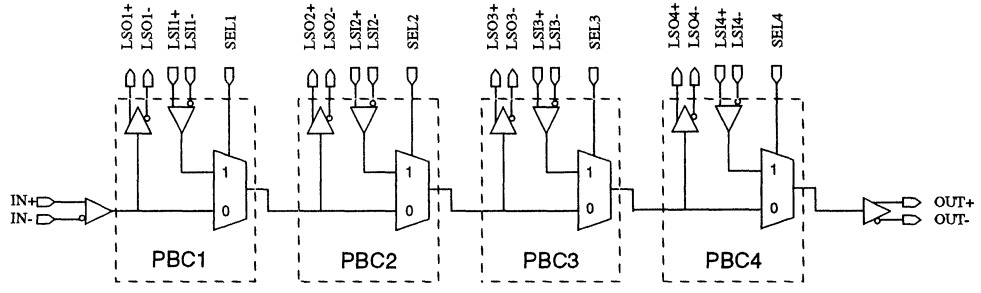
General Description

The VSC7121 is a Quad Port Bypass Circuit (PBC). Four Fibre Channel PBC's are cascaded into a single part to minimize part count, cost, high frequency routing, and jitter accumulation. Port Bypass Circuits are used to provide resiliency in Fibre Channel Arbitrated Loop (FC-AL) architectures. PBC's are used within FC-AL disk arrays to allow for resiliency and hot swapping of FC-AL drives.

A Port Bypass Circuit is a 2:1 Multiplexer with two modes of operation: NORMAL and BYPASS. In NORMAL mode, the disk drive is connected to the loop. Data goes from the 7121's L_SOn pin to the Disk Drive RX input and data from the disk drive TX output goes to the 7121's L_SIn pin. Refer to Figure 35 for disk drive application. In BYPASS mode, the disk drive is either absent or non-functional and data bypasses to the next available disk drive. Normal mode is enabled with a HIGH on the SEL pin and BYPASS mode is enabled by a LOW on the SEL pin. Direct Attach Fibre Channel Disk Drives have an "LRC Interlock" signal defined to control the SEL function.

Using a VSC7121 in a single loop of a disk array is illustrated in Figure 35: "Disk Array Application". FC-AL drives are all expected to be dual loop. The VSC7121 is cascaded in a manner such that all the 7121's internal PBC's are used in the same loop. For dual loop implementations, two or more VSC7121's should be used. Allocating each VSC7121 to only one of two loops preserves redundancy, prevents a single point of failure and lends itself to on-line maintainability.

7121 Block Diagram



The VSC7121 can be cascaded through the IN and OUT pins for arrays of disk drives greater than 4. For disk arrays with a noninteger multiple of 4 disk drives, the unused PBC's can be hardwired to bypass with a external pulldown resistor.

Table 24 is a truth table detailing the data flow through the VSC7121. Figure 1 shows a timing diagram of the data relationship in the VSC7121. There are no critical timing (setup, hold, or delay) parameters for the VSC7121 as this part routes the serial data encoded with the baud clock that is extracted by a Fibre Channel receiver. The primary AC parameter of importance is the jitter or data eye degradation inserted by the port bypass circuit. The design of the VSC7121 minimizes jitter accummulation by using fully differential circuits. This provides for symmetric rise and fall delays as well as noise rejection.

Table 24: Truth Table

SELECT STATE				*DATA OUTPUTS*				
SEL1	*SEL2*	*SEL3*	*SEL4*	*OUT*	*SO4*	*SO3*	*SO2*	*SO1*
L	L	L	L	IN	IN	IN	IN	IN
L	L	L	H	SI4	IN	IN	IN	IN
L	L	H	L	SI3	SI3	IN	IN	IN
L	H	L	L	SI2	SI2	SI2	IN	IN
H	L	L	L	SI1	SI1	SI1	SI1	IN
H	H	H	H	SI4	SI3	SI2	SI1	IN

Figure 34: Timing Waveforms

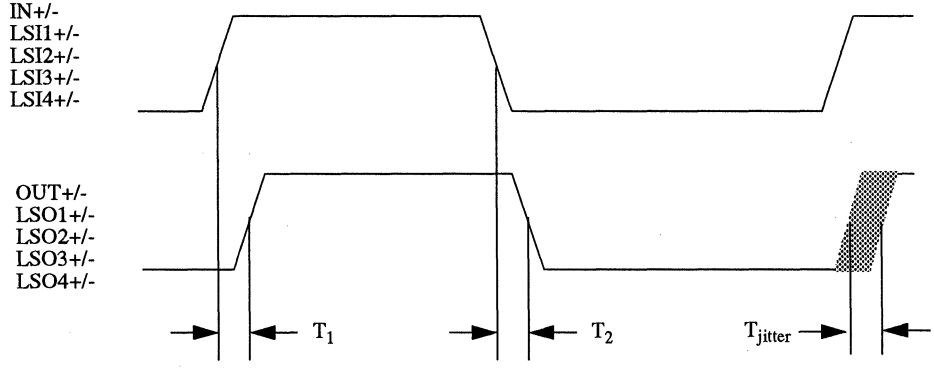


Figure 35: Disk Array Application

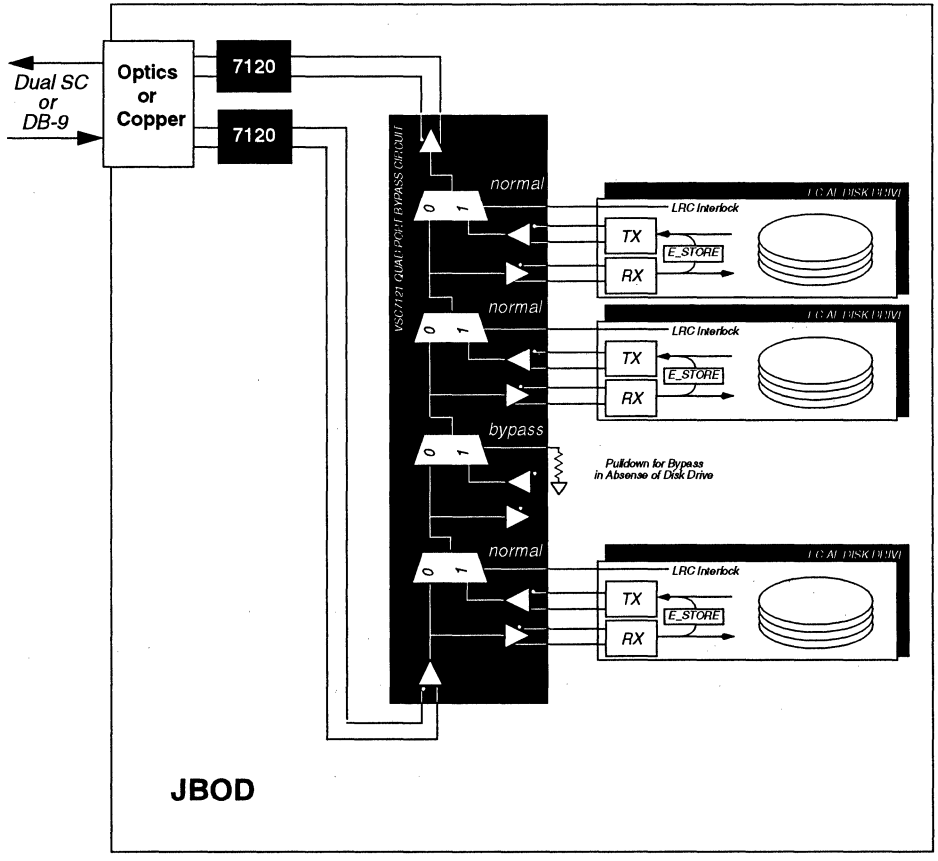


Table 25: AC Characteristics *(Over recommended operating conditions).*

Parameters	*Description*	*Min.*	*Max.*	*Units*	*Conditions*
T_1	Flow-Through Propagation Delay Rising Edge to Rising Edge		7.0	ns	Delay with all circuits bypassed. 75 Ohm Load
T_2	Flow through Propagation Delay Falling Edge to Falling Edge		7.0	ns	Delay with all circuits bypassed. 75 Ohm load.
T_{SDR}, T_{SDF}	Serial data rise and fall time	—	300	ps.	20% to 80%, tested on a sample basis
T_{jitter}	Data Jitter Accummulation		TBD	ps	RMS Output jitter accumulated with Valid 8B/10B code from IN to OUT - all PBC stages bypassed. Tested on sample basis.

Table 26: DC Characteristics *(Over recommended operating conditions).*

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
$V_{IH(TTL)}$	Input HIGH voltage (SEL - TTL)	2.0	—	5.5	V	$I_{IH} < 6.6$ mA @ $V_{IH} = 5.5$ V
$V_{IL(TTL)}$	Input LOW voltage (SEL - TTL)	0	—	0.8	V	—
$I_{IH(TTL)}$	Input HIGH current (SEL- TTL)	—	—	50	µA	$V_{IN} = 2.4$ V
$I_{IL(TTL)}$	Input LOW current (SEL - TTL)	-500	—	-50	µA	$V_{IN} = 0.5$ V
V_{DD}	Supply voltage	3.10	—	3.50	V	$V_{DD} = 3.30V \pm 5\%$
I_{DD}	Supply current	—	—	170	mA	Outputs open, $V_{DD} = V_{DD}$ max
P_D	Power Dissipation			0.6	W	Outputs open, $V_{DD} = V_{DD}$ max
$\Delta V_{IN(DF)}$	Receiver differential peak-to-peak Input Sensitivity, IN+/- & L_SIn+/-	300		2600	mVp-p	AC Coupled. Internally biased at $V_{DD}/2$
$\Delta V_{OUT(L\_SO)}$	L_SOn+/- output differential peak-to-peak voltage swing	1000	—	2200	mVp-p	50Ω to $V_{DD} - 2.0$ V
$\Delta V_{OUT(OUT)}$	OUT+/- output differential peak-to-peak voltage swing	1200		2200	mVp-p	50Ω to $V_{DD} - 2.0$ V

Absolute Maximum Ratings [1]

TTL Power Supply Voltage, (V_{DD}) ..... 0.5V to +4V
PECL DC Input Voltage, (V_{INP}) ..... -0.5V to V_{DD} +0.5V
TTL DC Input Voltage, (V_{INT}) ..... -0.5V to 5.5V
DC Voltage Applied to Outputs for High Output State, ($V_{IN\ TTL}$) ..... -0.5V to V_{DD} + 0.5V
TTL Output Current (I_{OUT}), (DC, Output High) 50mA
PECL Output Current, (I_{OUT}), (DC, Output High) ..... -50mA
Case Temperature Under Bias, (T_C) ..... -55° to +125°C
Storage Temperature, (T_{STG}) ..... -65° to + 150°C
Maximum Input ESD ..... 1500 V

Recommended Operating Conditions[2]

Power Supply Voltage, (V_{DD}) ..... +3.1V to 3.5V
Ambient Operating Temperature Range, (T) ..... 0°C to +70°C

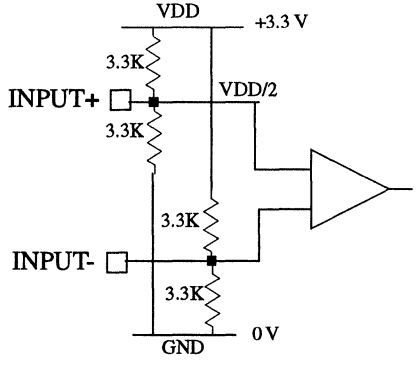
Notes:

1) *CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.*
2) *Vitesse guarantees the functional and parametric operation of the part under "Recommended Operating Conditions: except where specifically noted in the AC and DC Parametric Tables*

Input Structures

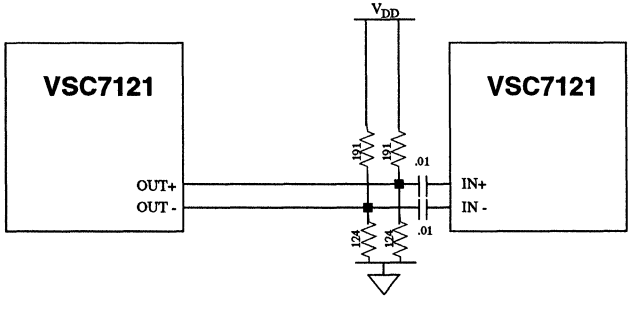
Two input structures exists in this part; TTL and High Speed, Differential Inputs. The TTL Inputs will interface with any TTL or 3.3V or 5V CMOS outputs. The High Speed, Differential Inputs are intended to be AC Coupled per the FC-PH specification. Being AC Coupled, the High Speed, Differential Input buffers are biased at $V_{DD}/2$. Refer to Figure 36 for High Speed, Differential Input structure.

Figure 36: High Speed, Differential Inputs (L_SIn/IN)



Because the VSC7121 output buffers are PECL outputs referenced to V_{DD}, the High Speed Differential outputs may not be direct coupled to the high speed differential inputs. One example of how to differentially cascade the two VSC7121 is shown in Figure 37.

Figure 37: Cascading Two VSC7121



75 Ohm Board/Termination Example

Figure 38: Pin Diagram

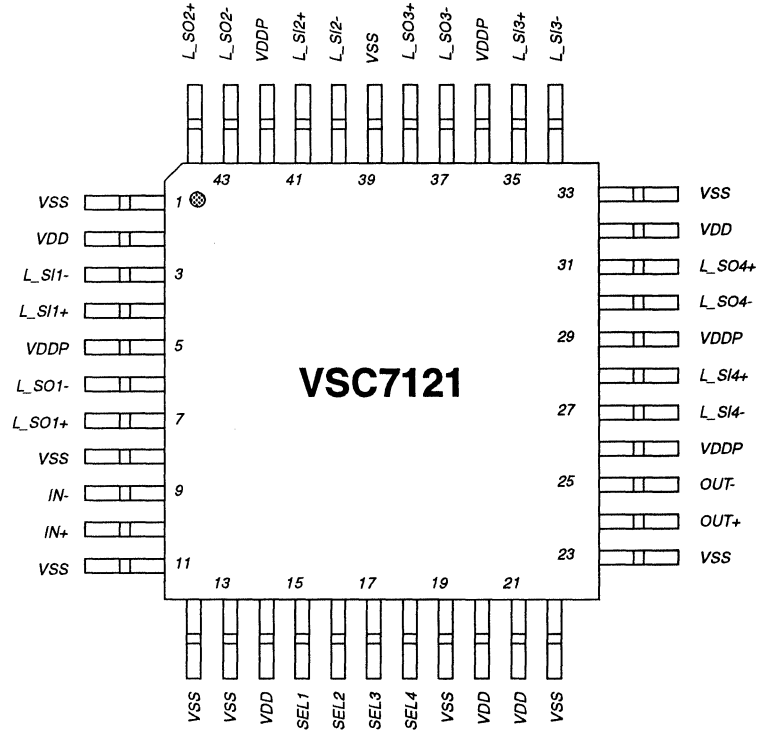


Table 27: Pin Description

Pin #	*Name*	*Description*
9, 10	IN-, IN+	INPUT - Differential (Biased at VDD/2). Differential inputs from the downstream PBC port.
3, 4	L_SI1-, L_SI1+	INPUT - Differential (Biased at VDD/2). Serial input from the local transmitter on PBC port 1.
40, 41	L_SI2-, L_SI2+	INPUT - Differential (Biased at VDD/2). Serial input from the local transmitter on PBC port 2.
34, 35	L_SI3-, L_SI3+	INPUT - Differential (Biased at VDD/2). Serial input from the local transmitter on PBC port 3.
27, 28	L_SI4-, L_SI4+	INPUT - Differential (Biased at VDD/2). Serial input from the local transmitter on PBC port 4.
15-18	SEL1, SEL2, SEL3, SEL4	INPUT - TTL. A HIGH selects the "BYPASS" mode causing the output of the previous port to propagate to next port or OUT. When LOW, this signal selects "NORMAL" mode which routes the previous port to the local output, L_SOn, and routes the local input, L_SIn, to the next port or OUT .
6, 7	L_SO1-, L_SO1+	OUTPUT - Differential (Biased at VDD-1.32V). Serial output driving the local receiver corresponding to PBC port 1.
43, 44	L_SO2-, L_SO2+	OUTPUT - Differential (Biased at VDD-1.32V) Serial output driving the local receiver corresponding to PBC port 2.
37, 38	L_SO3-, L_SO3+	OUTPUT - Differential (Biased at VDD-1.32V) Serial output driving the local receiver corresponding to PBC port 3.
30, 31	L_SO4-, L_SO4+	OUTPUT - Differential (Biased at VDD-1.32V) Serial output driving the local receiver corresponding to PBC port 4.
25, 24	OUT-, OUT+	OUTPUT - Differential (Biased at VDD - 1.32V) Serial output driving the upstream PBC port.
2, 14, 20-21, 32	VDD	Digital Logic Power Supply. 3.3V Supply for digital logic.
5, 26, 29 36, 42	VDDP	High-Speed Output Power Supply. 3.3V Supply for PECL drivers.
1, 8, 11-13, 19, 22-23, 33, 39	VSS	Ground. Ground pins are physically attached to the die mounting surface, and are an important part of the thermal path. For best thermal performance, all ground pins should be connected to a ground plane, using multiple vias if possible.

Package Thermal Characteristics

The VSC7121 is packaged into a standard plastic quad flatpack with an embedded, but unexposed thermal slug. This package adheres to industry standard EIAJ footprints for a 10x10mm body, 44 lead PQFP. The package construction is as shown in Figure 6. The 44 PQFP with embedded slug has the thermal properties shown in Table 5. This package allows the VSC7121 to operate with ambient temperatures up to 70°C in still air.

Figure 39: Package Cross Reference

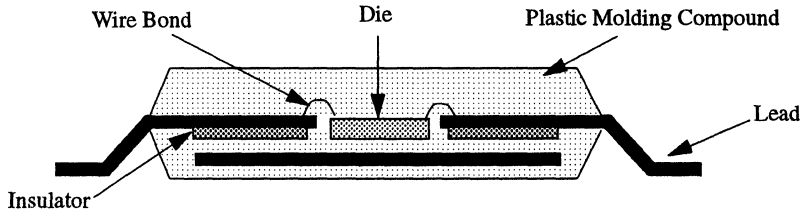
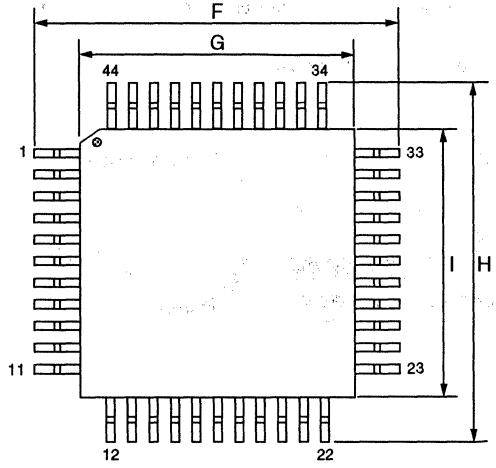


Table 28: 44 PQFP Thermal Resistance

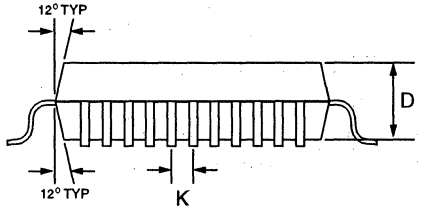
Symbol	*Description*	*Value*	*Units*
θ_{ca-0}	Thermal resistance from case to ambient, still air	50	°C/W
θ_{ca-100}	Thermal resistance from case to ambient, 100 LFPM air	43	°C/W
θ_{ca-200}	Thermal resistance from case to ambient, 200 LFPM air	39	°C/W
θ_{ca-400}	Thermal resistance from case to ambient, 400 LFPM air	36	°C/W
θ_{ca-600}	Thermal resistance from case to ambient, 600 LFPM air	34	°C/W

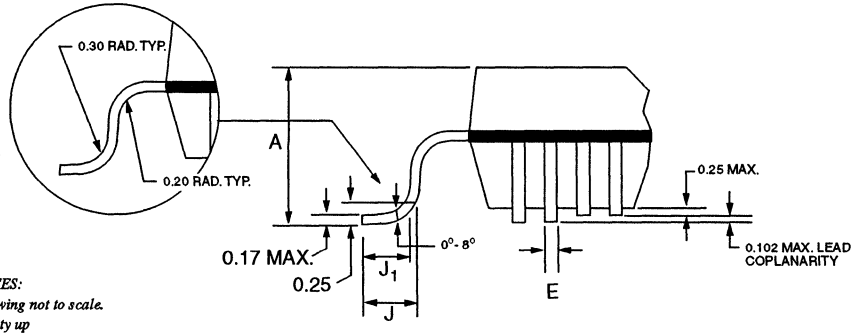
Package Information

44-Pin PQFP 10 x 10 mm



Item	*mm*	*Tol.*
A	2.45	MAX
D	2.00	+0.10
E	0.35	±.05
F	13.20	±.25
G	10.00	±.10
H	13.20	±.25
I	10.00	±.10
J	0.88	+.15 / -.10
K	0.80	BASIC





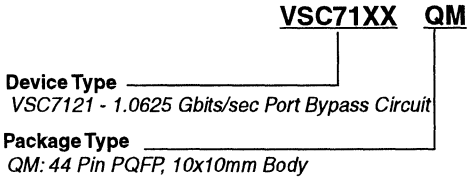
NOTES:
Drawing not to scale.
Cavity up
All units in mm unless otherwise noted.

Data Sheet

Quad Port Bypass Circuit for 1.0625 Gbit/sec Fibre Channel Arbitrated Loop Disk Arrays

Ordering Information

The order number for this product is formed by a combination of the device number and package type.



Notice

Vitesse Semiconductor Corporation reserves the right to make changes in its products specifications or other information at any time without prior notice. Therefore, the reader is cautioned to confirm that this datasheet is current prior to placing any orders. The company assumes no responsibility for any circuitry described other than circuitry entirely embodied in a Vitesse product.

Warning

Vitesse Semiconductor Corporation's product are not intended for use in life support appliances, devices or systems. Use of a Vitesse product in such applications without the written consent is prohibited.

Data Sheet

1.0625 Gbits/sec Fibre Channel Transceiver

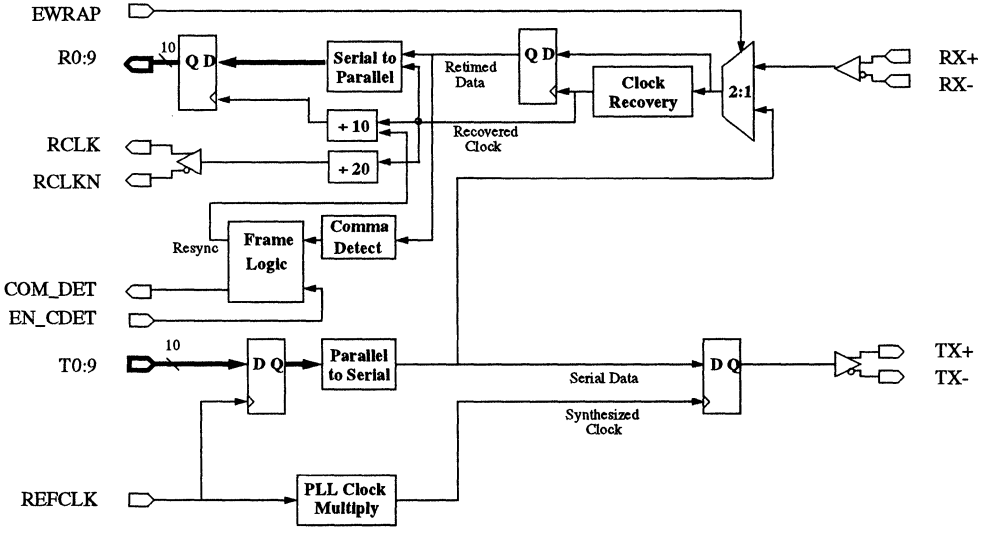
Features

- ANSI X3T11 Fibre Channel Compatible 1.0625 Gbps Full-duplex Transceiver
- 10 Bit TTL Interface for Transmit and Receive Data
- Monolithic Clock Synthesis and Clock Recovery - No External Components
- 106.25 MHz TTL Reference Clock
- Low Power Operation - 650 mW
- Suitable for Both Coaxial and Optical Link Applications
- 64 Pin, 10 mm or 14 mm PQFP
- Single +3.3V Power Supply

General Description

The VSC7125 is a full-speed Fibre Channel Transceiver optimized for Disk Drive and other space constrained applications. It accepts 10-bit 8B/10B encoded transmit data, latches it on the rising edge of REFCLK and serializes it onto the TX PECL differential outputs at a baud rate which is ten times the REFCLK frequency. The VSC7125 also samples serial receive data on the RX PECL differential inputs, recovers the clock and data, deserializes it onto the 10-bit receive data bus, outputs two recovered clocks at one twentieth of the incoming baud rate and detect Fibre Channel "Comma" characters. The VSC7125 contains on-chip PLL circuitry for synthesis of the baud-rate transmit clock, and extraction of the clock from the received serial stream. These circuits are fully monolithic and require no external components.

Block Diagram



Functional Description

Clock Synthesizer

The VSC7125 clock synthesizer multiplies the reference frequency provided on the REFCLK pin by 10 to achieve a baud rate clock at nominally 1.0625 GHz. The clock synthesizer contains a fully monolithic PLL which does not require any external components.

Serializer

The VSC7125 accepts TTL input data as a parallel 10 bit character on the T0:9 bus which is latched into the input latch on the rising edge of REFCLK. This data will be serialized and transmitted on the TX PECL differential outputs at a baud rate of ten times the frequency of the REFCLK input, with bit T0 transmitted first. User data should be encoded for transmission using the 8B/10B block code described in the Fibre Channel specification, or an equivalent, edge rich, DC-balanced code.

Transmission Character Interface

In Fibre Channel, an encoded byte is 10 bits and is referred to as a transmission character. The 10 bit interface on the VSC7125 corresponds to a transmission character. This mapping is illustrated below.

Figure 40: Transmission Order and Mapping to Fibre Channel Character

Parallel Data Bits	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0
8B/10B Bit Position	j	h	g	f	i	e	d	c	b	a
Comma Character	X	X	X	1	1	1	1	1	0	0

Last Data Bit Transmitted

First Data Bit Transmitted

Clock Recovery

The VSC7125 accepts differential high speed serial inputs on the RX+/RX- pins, extracts the clock and retimes the data. The serial bit stream should be encoded to provide DC balance and limited run length by a Fibre Channel compatible 8B/10B transmitter or equivalent. The VSC7125 clock recovery circuitry is completely monolithic and requires no external components. For proper operation, the baud rate of the data stream to be recovered should be within 0.01% of ten times the REFCLK frequency. For example if the REFCLK used is 106.25MHz, then the incoming serial baud rate must be 1.0625 gigabaud $\pm$0.01%.

Deserializer

The retimed serial bit stream is converted into a 10-bit parallel output character. The VSC7125 provides complementary TTL recovered clocks, RCLK and RCLKN, which are at one twentieth of the serial baud rate. This architecture is designed to simplify demultiplexing of the 10-bit data characters into a 20-bit halfword in the downstream controller chip. The clocks are generated by dividing down the high-speed clock which is phase locked to the serial data. The serial data is retimed by the internal high-speed clock, and deserialized. The

resulting parallel data will be captured by the adjoining protocol logic on the rising edges of RCLK and RCLKN. In order to maximize the setup and hold times available at this interface, the parallel data is loaded into the output register at a point nominally midway between the transition edges of RCLK and RCLKN.

If serial input data is not present, or does not meet the required baud rate, the VSC7125 will continue to produce a recovered clock so that downstream logic may continue to function. The RCLK and RCLKN output frequency under these circumstances may differ from their expected frequency by no more than ±1%.

Word Alignment

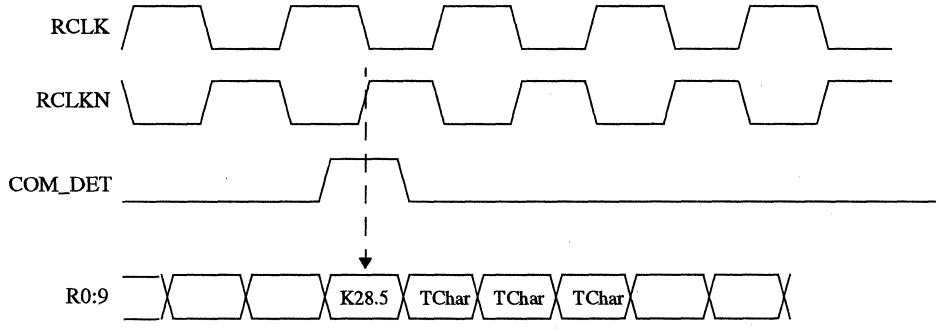
The VSC7125 provides 7-bit Fibre Channel comma character recognition and data word alignment. Word synchronization is enabled by asserting EN_CDET HIGH. When synchronization is enabled, the VSC7125 constantly examines the serial data for the presence of the Fibre Channel "comma" character. This pattern is "0011111XXX", where the leading zero corresponds to the first bit received. The comma sequence is not contained in any normal 8B/10B coded data character or pair of adjacent characters. It occurs only within special characters, known as K28.1, K28.5 and K28.7, which is defined specifically for synchronization in Fibre Channel systems. Improper alignment of the comma character is defined as any of the following conditions:

1) The comma is not aligned within the 10-bit transmission character such that T0...T6 = "0011111"
2) The comma straddles the boundary between two 10-bit transmission characters.
3) The comma is properly aligned but occurs in the received character presented during the rising edge of RCLK rather than RCLKN.

When EN_CDET is HIGH and an improperly aligned comma is encountered, the internal data is shifted in such a manner that the comma character is aligned properly in R0:9. This results in proper character and half-word alignment. When the parallel data alignment changes in response to an improperly aligned comma pattern, some data which would have been presented on the parallel output port may be lost. However, the synchronization character and subsequent data will be output correctly and properly aligned. When EN_CDET is LOW, the current alignment of the serial data is maintained indefinitely, regardless of data pattern.

On encountering a comma character, COM_DET is driven HIGH to inform the user that realignment of the parallel data field may have occurred. The COM_DET pulse is presented simultaneously with the comma character and has a duration equal to the data, or half of an RCLK period. The COM_DET signal is timed such that it can be captured by the adjoining protocol logic on the rising edge of RCLKN. Functional waveforms for synchronization are given in Figure 2 and Figure 3. Figure 2 shows the case when a comma character is detected and no phase adjustment is necessary. It illustrates the position of the COM_DET pulse in relation to the comma character on R0:9. Figure 3 shows the case where the K28.5 is detected, but it is out of phase and a change in the output data alignment is required. Note that up to three characters prior to the comma character may be corrupted by the realignment process.

Figure 41: Detection of a Properly Aligned Comma Character



TChar: 10 bit Transmission Character

Figure 42: Detection and Resynchronization of an Improperly Aligned Comma

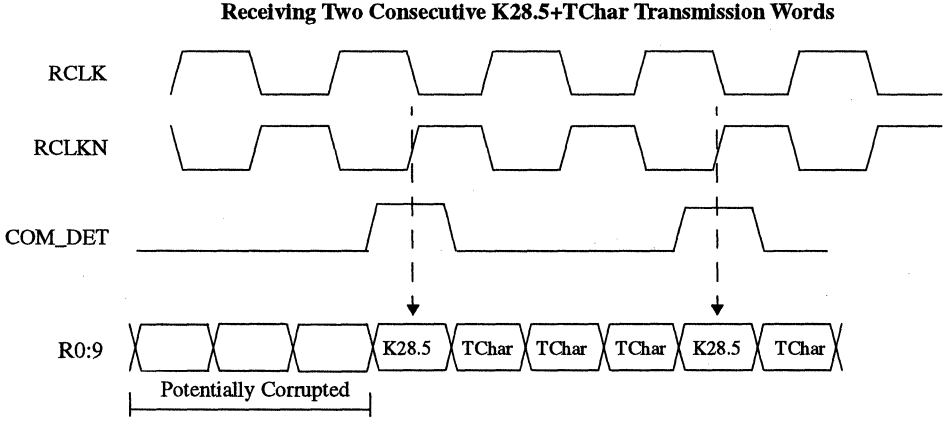


Figure 43: Transmit Timing Waveforms

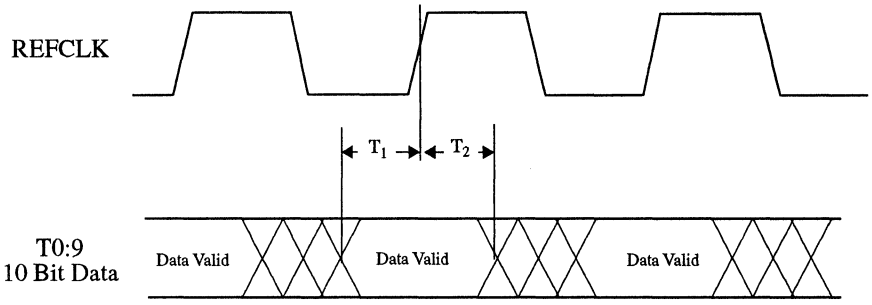


Table 29: Transmit AC Characteristics

Parameters	Description	Min	Max	Units	Conditions
T_1	T0:9 Setup time to the rising edge of REFCLK	1.0	—	ns.	Measured between the valid data level of T0:9 to the 1.4V point of REFCLK
T_2	T0:9 hold time after the rising edge of REFCLK	1.5	—	ns.	
T_{SDR},T_{SDF}	TX+/TX- rise and fall time	—	300	ps.	20% to 80%, 75 Ohm load to Vss, Tested on a sample basis
T_{LAT}	Latency from rising edge of REFCLK to T0 appearing on TX+/TX-	11bc - 1ns		ns.	bc = Bit clocks ns = Nano second
Transmitter Output Jitter Allocation					
T_{rj}	Serial data output random jitter (RMS)	—	20	ps.	RMS, tested on a sample basis (refer to Figure 8)
T_{DJ}	Serial data output deterministic jitter (p-p)	—	100	ps.	Peak to peak, tested on a sample basis (refer to Figure 8)

Table 30: Receive AC Characteristics

Parameters	Description	Min.	Max.	Units	Conditions
T_1	Data or COM_DET Valid prior to RCLK/RCLKN rise	4.0	—	ns.	Measured between the 1.4V point of RCLK or RCLKN and a valid level of R0:9. All outputs driving 10pF load.
T_2	Data or COM_DET Valid after RCLK or RCLKN rise	3.0	—	ns.	
T_3	Deviation of RCLK rising edge to RCLKN rising edge delay from nominal. $delay = \frac{f_{baud}}{10} \pm T_3$	-500	500	ps.	Nominal delay is 10 bit times. Tested on sample basis
T_4	Deviation of RCLK, RCLKN frequency from nominal. $f_{RCLK} = \frac{f_{REFCLK}}{2} \pm T_4$	-1.0	1.0	%	Whether or not locked to serial data
T_R, T_F	R0:9, COM_DET, RCLK, RCLKN rise and fall time	—	2.4	ns.	Between $V_{il(max)}$ and $V_{ih(min)}$, into 10 pf. load.
R_{lat}	Latency from RX to R0:9	15bc + 2ns	34bc + 2ns		bc = Bit clock ns = Nano second
T_{LOCK}	Data acquisition lock time @ 1.0625Gb/s	—	2.4	µs.	8B/10B IDLE pattern. Tested on a sample basis
Receive Data Jitter	Receive Data Jitter Power $\int_{100KHz}^{\frac{1}{2 \times BitTime}} PhaseNoise$	—	40	ps.	dBc, RMS for 10^{-12} Bit Error Ratio Tested on a sample basis

Figure 44: Receive Timing Waveforms

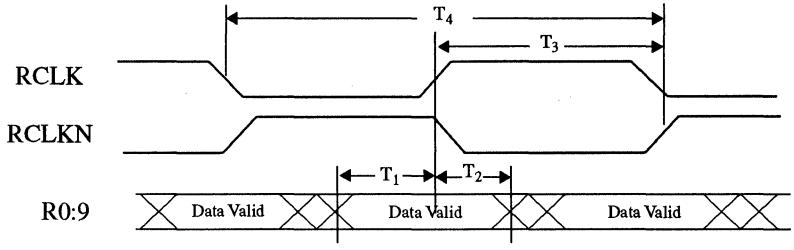


Figure 45: REFCLK Timing Waveforms

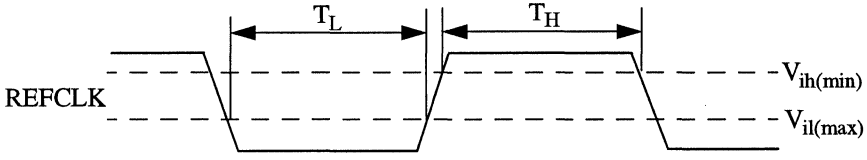
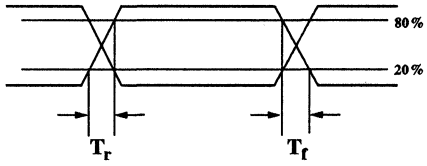


Table 31: Reference Clock Requirements

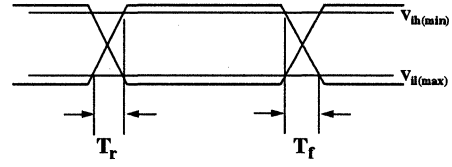
Parameters	Description	Min	Max	Units	Conditions
FR	Frequency Range	100	110	MHz	Range over which both transmit and receive reference clocks on any link may be centered
FO	Frequency Offset	-200	200	ppm.	Maximum frequency offset between transmit and receive reference clocks on one link
DC	REFCLK duty cycle	30	70	%	Measured at 1.5V
T_{RCR}, T_{RCF}	REFCLK rise and fall time	—	1.0	ns.	Between $V_{il(max)}$ and $V_{ih(min)}$
REFCLK Jitter	REFCLK Jitter Power $\int_{100Hz}^{5MHz} PhaseNoise$	—	2	ps.	dbc, RMS for FC compliant output data jitter
REFCLK Jitter	REFCLK Jitter Power $\int_{100Hz}^{5MHz} PhaseNoise$	—	40	ps.	dbc, RMS for 10^{-12} Bit Error Ratio with zero length external path. Tested on a sample basis

Figure 46: Parametric Measurement Information

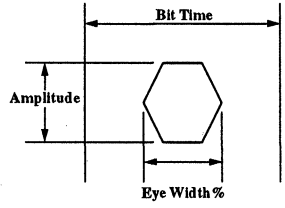
Serial Input Rise and Fall Time



TTL Input and Output Rise and Fall Time

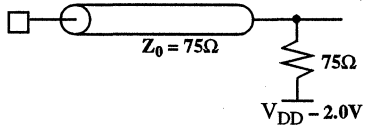


Receiver Input Eye Diagram Jitter Tolerance Mask



Parametric Test Load Circuit

Serial Output Load



TTL A.C. Output Load

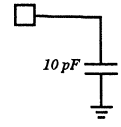
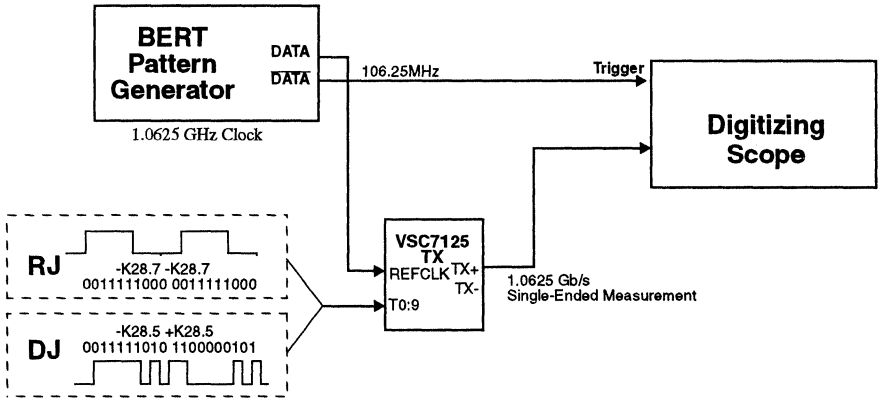


Figure 47: Transmitter Jitter Measurement Method



Random jitter (RJ) measurements performed according to Fibre Channel 4.3 Annex A, Test Methods, Section A.4.4. Measure standard deviation of all 50% crossing points. Peak to peak RJ is ± 7 sigma of distribution.

Deterministic jitter (DJ) measurements performed according to Fibre Channel 4.3 Annex A, Test Methods, Section A.4.3. Measure time of all the 50% points of all ten transitions. DJ is the range of the timing variations.

Absolute Maximum Ratings (1)

Power Supply Voltage, (V_{DD}) ..... -0.5V to +4V
DC Input Voltage (PECL inputs) ..... -0.5V to V_{DD} +0.5V
DC Input Voltage (TTL inputs) ..... -0.5V to 5.5V
DC Output Voltage (TTL Outputs) ..... -0.5V to V_{DD} + 0.5V
Output Current (TTL Outputs) ..... +/-50mA
Output Current (PECL Outputs) ..... +/-50mA
Case Temperature Under Bias ..... -55° to +125°C
Storage Temperature ..... -65°C to +150°C
Maximum Input ESD (Human Body Model) ..... 1500 V

Recommended Operating Conditions

Power Supply Voltage, (V_{DD}) ..... +3.3V±5%
Operating Temperature Range ..... 0°C Ambient to +100°C Case Temperature

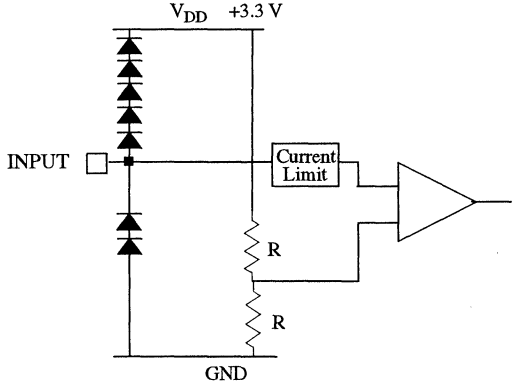
Notes:

(1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

DC Characteristics *(Over recommended operating conditions).*

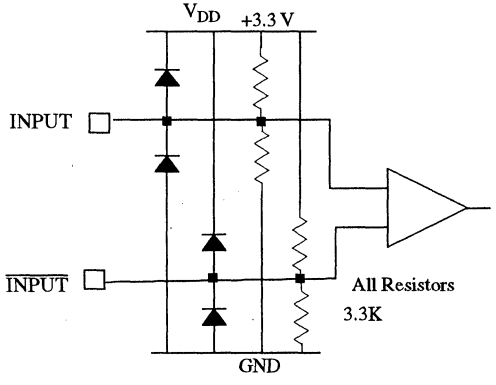
Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage (TTL)	2.4	—	—	V	I_{OH} = -1.0 mA
V_{OL}	Output LOW voltage (TTL)	—	—	0.5	V	I_{OL} = +1.0 mA
ΔV_{OUT75}	TX Output differential peak-to-peak voltage swing	1200	—	2200	mVp-p	75Ω to V_{DD} – 2.0 V
ΔV_{OUT50}	TX Output differential peak-to-peak voltage swing		—	2200	mVp-p	50Ω to V_{DD} – 2.0 V
ΔV_{IN}	Receiver differential peak-to-peak Input Sensitivity RX	300	—	2600	mVp-p	Internally biased to Vdd/2
V_{IH}	Input HIGH voltage (TTL)	2.0	—	5.5	V	
V_{IL}	Input LOW voltage (TTL)	0	—	0.8	V	—
I_{IH}	Input HIGH current (TTL)	—	50	500	µA	V_{IN} =2.4V
I_{IL}	Input LOW current (TTL)	—	—	-500	µA	V_{IN} =0.5V
V_{DD}	Supply voltage	3.14	—	3.47	V	3.3V±5%
P_D	Power dissipation	—	625	900	mW	Outputs open, V_{DD} = V_{DD} max
I_{DD}	Supply Current	—	190	260	mA	Outputs open, V_{DD} = V_{DD} max

Figure 48: Input Structures



REFCLK and TTL Inputs

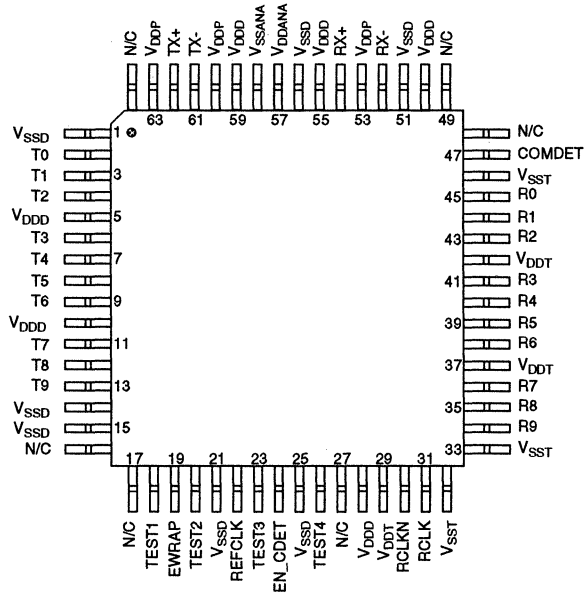
A



High Speed Differential Input (RX+/RX-)

B

Figure 49: Pin Diagram



(Top View)

Table 32: Pin Description

Pin #	Name	Description
2-4, 6-9, 11-13	T0:9	INPUTS - TTL 10-bit transmit character. Parallel data on this bus is clocked in on the rising edge of REFCLK. The data bit corresponding to T0 is transmitted first.
22	REFCLK	INPUT - TTL This rising edge of this clock latches T0:9 into the input register. It also provides the reference clock, at one tenth the baud rate to the PLL.
62, 61	TX+, TX-	OUTPUTS - Differential PECL (AC Coupling recommended) These pins output the serialized transmit data when EWRAP is LOW. When EWRAP is HIGH, TX+ is HIGH and TX- is LOW.
45-43, 41-38, 36-34	R0:9	OUTPUTS - TTL 10-bit received character. Parallel data on this bus is clocked out on the rising edges of RCLK and RCLKN. R0 is the first bit received on RX+/RX-.

Pin #	Name	Description
19	EWRAP	INPUT - TTL LOW for Normal Operation. When HIGH, an internal loopback path from the transmitter to the receiver is enabled and the TX outputs are held HIGH.
54, 52	RX+, RX-	INPUTS - Differential PECL (AC Coupling recommended) The serial receive data inputs selected when EWRAP is LOW. Internally biased tot VDD/2, with 3.3KΩ resistors from each input pin to VDD and GND.
31, 30	RCLK, RCLKN	OUTPUT - Complementary TTL Recovered clocks derived from one twentieth of the RX+/- data stream. Each rising transition of RCLK or RCLKN corresponds to a new word on R0:9.
24	EN_CDET	INPUT - TTL Enables COMDET and word resynchronization when HIGH. When LOW, keeps current word alignment and disables COMDET.
47	COMDET	OUTPUT - TTL This output goes HIGH for half of an RCLK period to indicate that R0:9 contains a Comma Character ('0011111XXX'). COMDET will go HIGH only during a cycle when RCLKN is rising. COMDET is enabled by EN_CDET being HIGH.
18,20,23	TEST1 TEST2 TEST3	INPUT These signals are used for factory test. For normal operation, tie to VDD.
26	TEST_4	OUTPUT This signal is used for factory test. For normal operation, leave open.
57	VDDANA	Analog Power Supply
58	VSSANA	Analog Ground
5, 10, 28, 50, 55, 59	VDDD	Digital Logic Power Supply
1, 14, 15, 21, 25, 51, 56	VSSD	Digital Logic Ground
29, 37, 42	VDDT	TTL Output Power Supply
32, 33, 46	VSST	TTL Output Ground
53, 60, 63	VDDP	PECL I/O Power Supply
16,17,27, 48,49,64	N/C	No Connection. These pins are not internally connected.

Thermal Considerations

The VSC7125 is packaged in either a 10 mm PQFP or a 14 mm PQFP with internal heat spreaders. These packages use industry-standard EIAJ footprints, but have been enhanced to improve thermal dissipation. The construction of the packages is as shown in Figure 11.

Figure 50: Package Cross Section

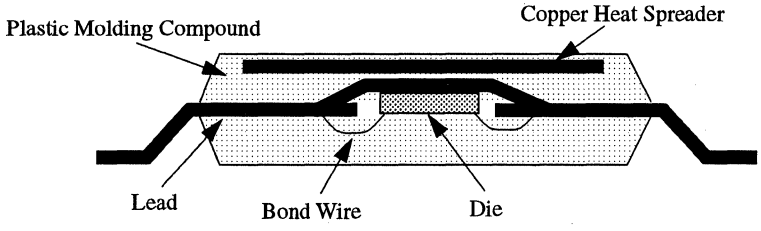


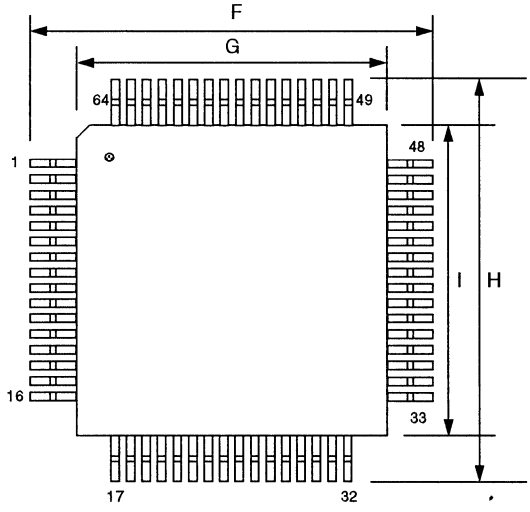
Table 33: Thermal Resistance

Symbol	*Description*	*10mm Value*	*14mm Value*	*Units*
θ_{jc}	Thermal resistance from junction to case	10.5	10	°C/W
θ_{ca}	Thermal resistance from case to ambient in still air including conduction through the leads.	53	32	°C/W
$\theta_{ca\text{-}100}$	Thermal resistance from case to ambient with 100 LFM airflow	44	28	°C/W
$\theta_{ca\text{-}200}$	Thermal resistance from case to ambient with200 LFM airflow	39	25	°C/W
$\theta_{ca\text{-}400}$	Thermal resistance from case to ambient with 400 LFM airflow	34	22	°C/W
$\theta_{ca\text{-}600}$	Thermal resistance from case to ambient with 600 LFM airflow	31	20	°C/W

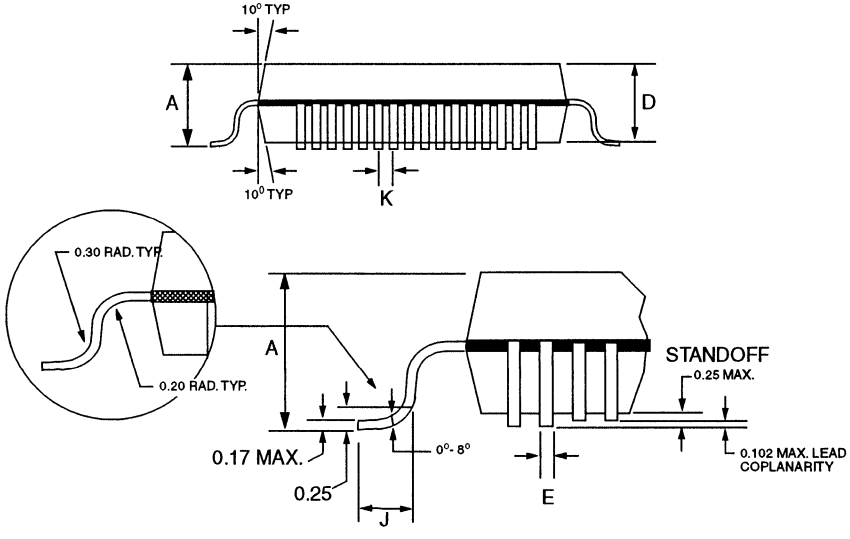
The VSC7125 is designed to operate with a junction temperature up to 110°C. The user must guarantee that the temperature specification is not violated. With the Thermal Resistances shown above, the 10x10mm PQFP can operate in still air ambient temperatures of 53°C [53°C=110°C-0.9W*(10.5°C/W+53°C/W)] while the 14x14 PQFP can operate in still air ambient temperatures of 73°C [73°C=110°C-0.9W*(10°C/W+32°C/W)]. If the ambient air temperature exceeds these limits then some form of cooling through a heatsink or an increase in airflow must be provided.

Package Information

64-pin PQFP Package Drawing



Item	10 mm	14 mm	Tol.
A	2.45	2.45	MAX
D	2.00	2.00	+0.10
E	0.30	0.35	±.05
F	13.20	17.20	±.25
G	10.00	14.00	±.10
H	13.20	17.20	±.25
I	10.00	14.00	±.10
J1	TBD	TBD	TBD
J	0.88	0.80	±.15
K	0.50	0.80	BASIC



NOTES:
Drawing not to scale.
All units in mm unless otherwise noted.

Ordering Information

The part number for this product is formed by a combination of the device number and the package style:

VSC7125xx

Device Type:

VSC7125: 1.0625 Gbps Transceiver

Package Style (64-pin)

QN: 14x14mm PQFP

QU: 10x10mm PQFP

Notice

Vitesse Semiconductor Corporation reserves the right to make changes in its products specifications or other information at any time without prior notice. Therefore, the reader is cautioned to confirm that this datasheet is current prior to placing any orders. The company assumes no responsibility for any circuitry described other than circuitry entirely embodied in a Vitesse product.

Warning

Vitesse Semiconductor Corporation's product are not intended for use in life support appliances, devices or systems. Use of a Vitesse product in such applications without the written consent is prohibited.

Product Preview

1.0625 Gbits/sec
Fibre Channel Transceiver

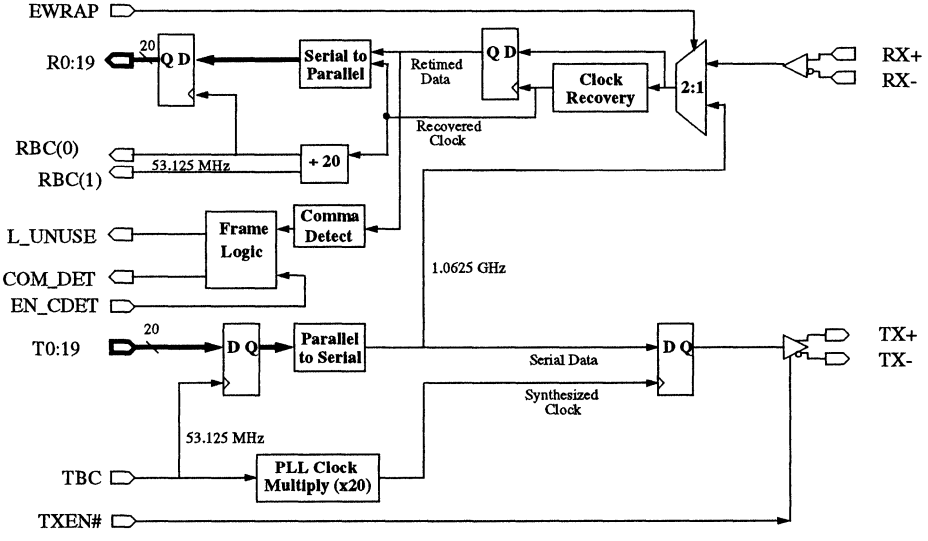
Features

- ANSI X3T11 Fibre Channel Compatible 1.0625 Gbps Full-duplex Transceiver
- GLM Compatible (FCSI-301-Rev 1.0)
- 20 Bit TTL Interface for Transmit and Receive Data
- Monolithic Clock Synthesis and Clock Recovery - No External Components
- 53.125 MHz TTL Reference Clock
- Automatic Lock-to-Reference Function
- Suitable for Both Coaxial and Optical Link Applications
- Low Power Operation - 750 mW
- 80 Pin, 14x14 mm PQFP Package
- Single +3.3V Power Supply

General Description

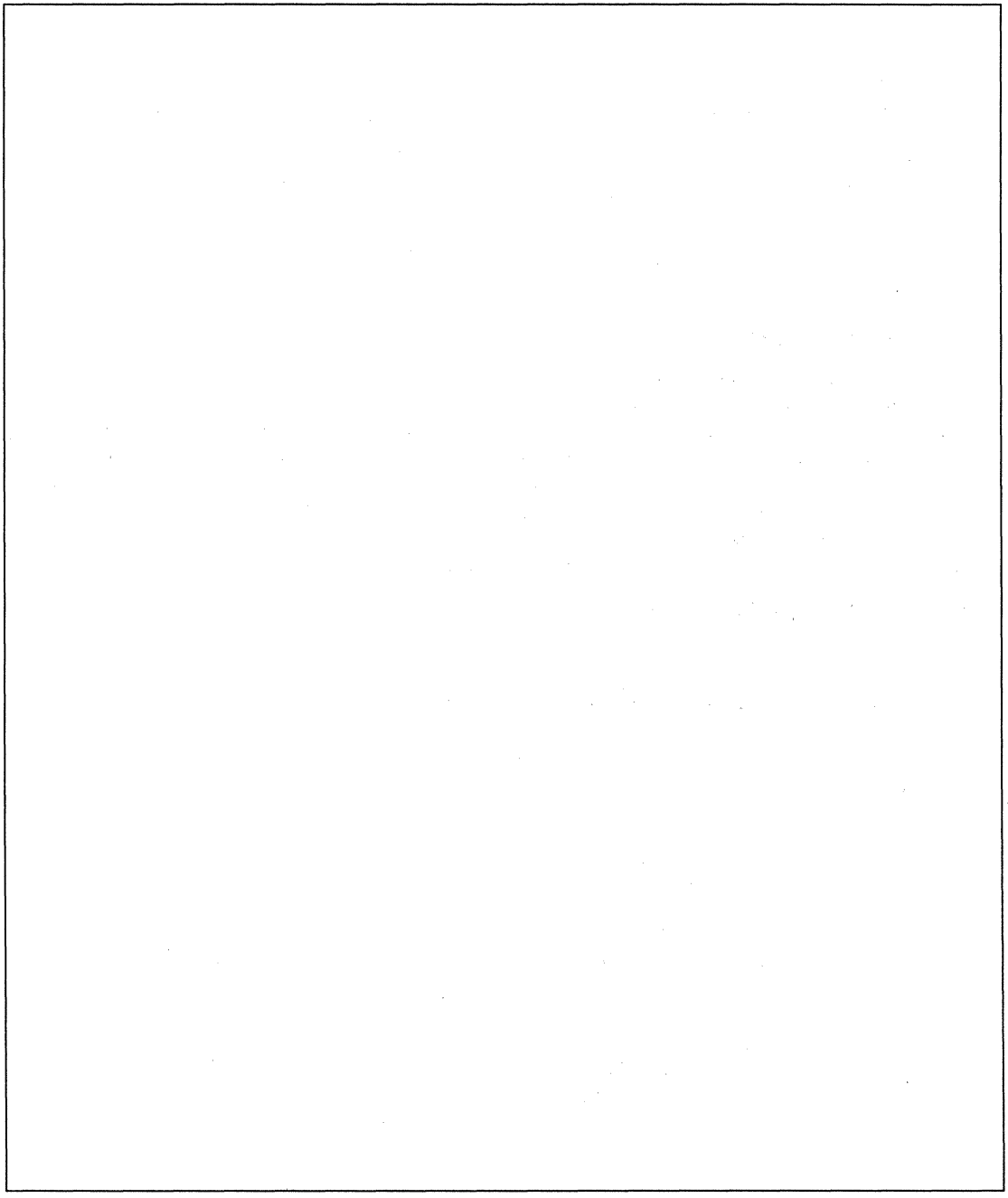
The VSC7126 is a full-speed Fibre Channel Transceiver optimized for Host Adapter and other space-constrained applications. It accepts two 10-bit 8B/10B encoded transmit characters, latches them on the rising edge of TBC and serializes the data onto the TX+/- PECL differential outputs at a baud rate which is twenty times the TBC frequency. It also samples serial receive data on the RX+/- PECL differential inputs, recovers the clock and data, deserializes it onto two 10-bit receive characters, outputs a recovered clocs at one twentieth of the incoming baud rate and detects Fibre Channel "Comma" characters. The VSC7126 contains on-chip PLL circuitry for synthesis of the baud-rate transmit clock, and extraction of the clock from the received serial stream. These circuits are fully monolithic and require no external components.

VSC7126 Block Diagram



1.0625 Gbits/sec
Fibre Channel Transceiver

Product Preview



Preliminary Data Sheet

1.25 Gbits/sec
Gigabit Ethernet Transceiver

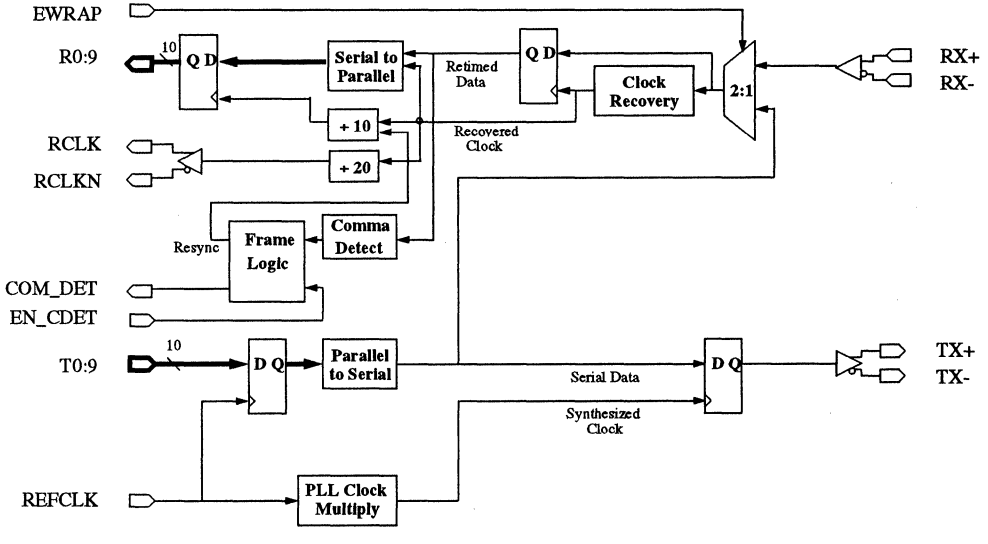
Features

- Gigabit Ethernet Transceiver @ 1.25 Gb/s
- 10 Bit TTL Interface for Transmit and Receive Data
- Monolithic Clock Synthesis and Clock Recovery - No External Components
- 125 MHz TTL Reference Clock
- Low Power Operation - 700 mW
- Suitable for Both Coaxial or Optical Link Applications
- 64 Pin, 14 mm Standard PQFP
- Single +3.3V Supply

General Description

The VSC7135 is a 1.25 Gb/s Ethernet Transceiver optimized for Gigabit Ethernet or 1000Base-T applications. It accepts 10-bit 8B/10B encoded transmit data, latches it on the rising edge of REFCLK and serializes it onto the TX PECL differential outputs at a baud rate which is ten times the REFCLK frequency. The VSC7135 also samples serial receive data on the RX PECL differential inputs, recovers the clock and data, deserializes it onto the 10-bi receive data bus, outputs two recovered clocks at one twentieth of the incoming baud rate and detect "Comma" characters. The VSC7135 contains on-chip PLL circuitry for synthesis of the baud-rate transmit clock, and extraction of the clock from the received serial stream. These circuits are fully monolithic and require no external components. This product is directly derived from the VSC7125 1.0625 Gb/s Fibre Channel Transceiver aimed at full-speed Fibre Channel Disk Drives, Host Adaptors and RAID systems.

Figure 1: Block Diagram



Functional Description

Clock Synthesizer

The VSC7135 clock synthesizer multiplies the reference frequency provided on the REFCLK pin by 10 to achieve a baud rate clock at nominally 1.25 GHz. The clock synthesizer contains a fully monolithic PLL which does not require any external components.

Serializer

The VSC7135 accepts TTL input data as a parallel 10 bit character on the T0:9 bus which is latched into the input latch on the rising edge of REFCLK. This data will be serialized and transmitted on the TX PECL differential outputs at a baud rate of ten times the frequency of the REFCLK input, with bit T0 transmitted first. User data should be encoded for transmission using the 8B/10B block code described in the Fibre Channel specification, or an equivalent, edge rich, DC-balanced code.

Transmission Character Interface

An encoded byte is 10 bits and is referred to as a transmission character. The 10 bit interface on the VSC7135 corresponds to a transmission character. This mapping is illustrated in Figure 2.

Figure 2: Transmission Order and Mapping of an 8B/10B Character

Parallel Data Bits	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0
8B/10B Bit Position	j	h	g	f	i	e	d	c	b	a
Comma Character	X	X	X	1	1	1	1	1	0	0

Last Data Bit Transmitted

First Data Bit Transmitted

Clock Recovery

The VSC7135 accepts differential high speed serial inputs on the RX+/RX- pins, extracts the clock and retimes the data. The serial bit stream should be encoded so as to provide DC balance and limited run length by an 8B/10B transmitter or equivalent. The VSC7135 clock recovery circuitry is completely monolithic and requires no external components. For proper operation, the baud rate of the data stream to be recovered should be within 0.01% of ten times the REFCLK frequency. For example if the REFCLK used is 125MHz, then the incoming serial baud rate must be 1.25 gigabaud $\pm$0.01%.

Deserializer

The retimed serial bit stream is converted into a 10-bit parallel output character. The VSC7135 provides complementary TTL recovered clocks, RCLK and RCLKN, which are at one twentieth of the serial baud rate. This architecture is designed to simplify demultiplexing of the 10-bit data characters into a 20-bit halfword in the downstream controller chip. The clocks are generated by dividing down the high-speed clock which is phase locked to the serial data. The serial data is retimed by the internal high-speed clock, and deserialized.

The resulting parallel data will be captured by the adjoining protocol logic on the rising edges of RCLK and RCLKN. In order to maximize the setup and hold times available at this interface, the parallel data is loaded into the output register at a point nominally midway between the transition edges of RCLK and RCLKN.

If serial input data is not present, or does not meet the required baud rate, the VSC7135 will continue to produce a recovered clock so that downstream logic may continue to function. The RCLK and RCLKN output frequency under these circumstances may differ from their expected frequency by no more than ±1%.

Word Alignment

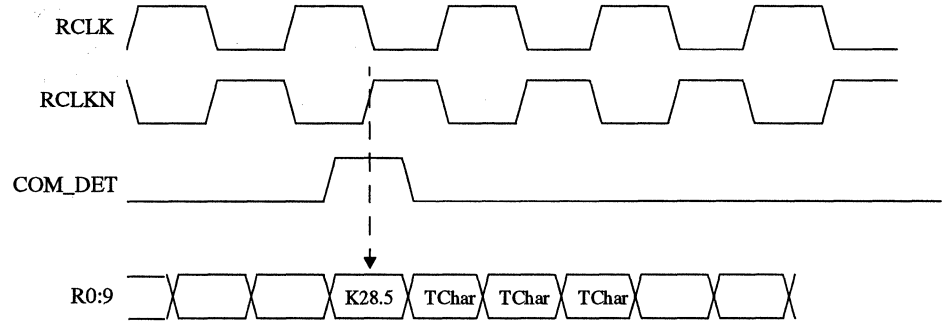
The VSC7135 provides 7-bit comma character recognition and data word alignment. Word synchronization is enabled by asserting EN_CDET HIGH. When synchronization is enabled, the VSC7135 constantly examines the serial data for the presence of the "Comma" character. This pattern is "0011111XXX", where the leading zero corresponds to the first bit received. The comma sequence is not contained in any normal 8B/10B coded data character or pair of adjacent characters. It occurs only within a special characters, known as K28.1, K28.5 and K28.7, which is defined specifically for synchronization purposes. Improper alignment of the comma character is defined as any of the following conditions:

1) The comma is not aligned within a the 10-bit transmission character such that T0...T6 = "0011111"
2) The comma straddles the boundary between two 10-bit transmission characters.
3) The comma is properly aligned but occurs in the received character presented during the rising edge of RCLK rather than RCLKN.

When EN_CDET is HIGH and an improperly aligned comma is encountered, the internal data is shifted in such a manner that the comma character is aligned properly in R0:9. This results in proper character and half-word alignment. When the parallel data alignment changes in response to a improperly alligned comma pattern, some data which would have been presented on the parallel output port may be lost. However, the syncronization character and subsequent data will be output correctly and properly aligned. When EN_CDET is LOW, the current alignment of the serial data is maintained indefinitiely, regardless of data pattern.

On encountering a comma character, COM_DET is driven HIGH to inform the user that realignment of the parallel data field may have occurred. The COM_DET pulse is presented simultaneously with the comma character and has a duration equal to the data, or half of an RCLK period. The COM_DET signal is timed such that it can be captured by the adjoining protocol logic on the rising edge of RCLKN. Functional waveforms for synchronization are given in Figure 3 and Figure 4. Figure 3 shows the case when a comma character is detected and no phase adjustment is necessary. It illustrates the position of the COM_DET pulse in relation to the comma character on R0:9. Figure 4 shows the case where the K28.5 is detected, but it is out of phase and a change in the output data alignment is required. Note that up to three characters prior to the comma character may be corrupted by the realignment process.

Figure 3: Detection of a Properly Aligned Comma Character



TChar: 10 bit Transmission Character

Figure 4: Detection and Resynchronizatoin of an Improperly Aligned Comma

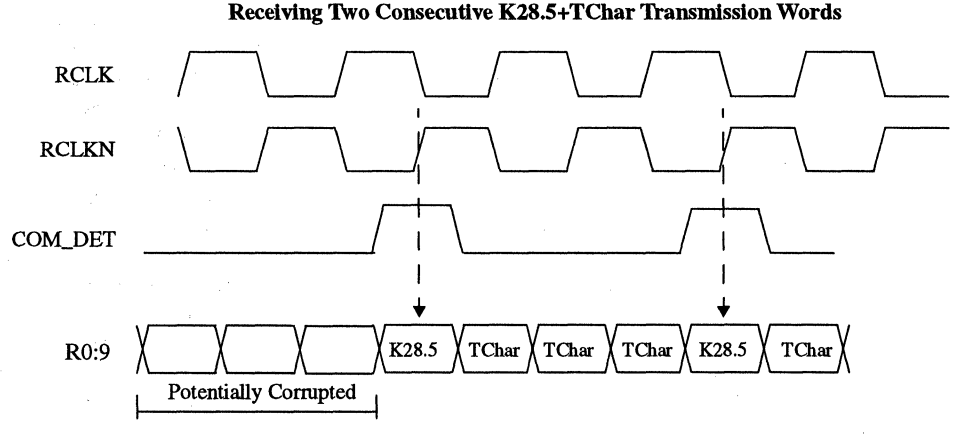


Figure 5: Transmit Timing Waveforms

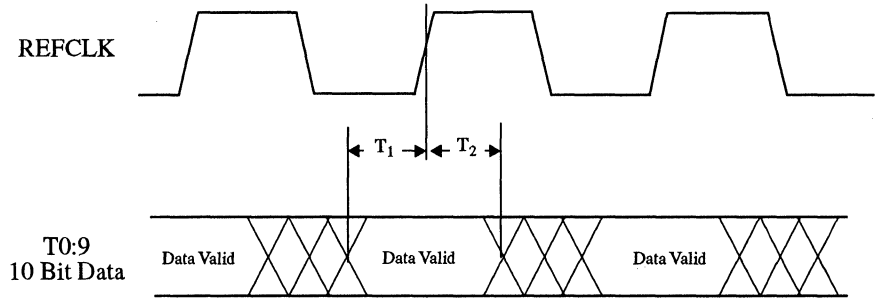


Table 1: Transmit AC Characteristics

Parameters	Description	Min	Max	Units	Conditions
T_1	T0:9 Setup time to the rising edge of REFCLK	1.0	—	ns.	Measured between thevalid data level of T0:9 to the 1.4V point of REFCLK
T_2	T0:9 hold time after the rising edge of REFCLK	1.5	—	ns.	
T_{SDR},T_{SDF}	TX+/TX- rise and fall time	—	300	ps.	20% to 80%, 75 Ohm load to Vss, Tested on a sample basis
T_{LAT}	Latentcy from rising edge of REFCLK to T0 appearing on TX+/TX-	11bc - 1ns		ns.	bc = Bit clocks ns = Nano second
Transmitter Output Jitter Allocation					
T_{rj}	Serial data output random jitter (RMS)	—	20	ps.	RMS, tested on a sample basis (refer to Figure 9)
T_{DJ}	Serial data output deterministic jitter (p-p)	—	100	ps.	Peak to peak, tested on a sample basis (refer to Figure 9)

Figure 6: Receive Timing Waveforms

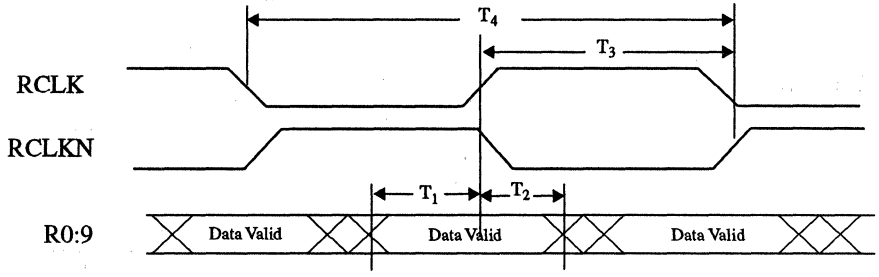


Table 2: Receive AC Characteristics

Parameters	Description	Min.	Max.	Units	Conditions
T_1	Data or COM_DET Valid prior to RCLK/RCLKN rise	3.0	—	ns.	Measured between the 1.4V point of RCLK or RCLKN and a valid level of R0:9. All outputs driving 10pF load.
T_2	Data or COM_DET Valid after RCLK or RCLKN rise	2.0	—	ns.	
T_3	Deviation of RCLK rising edge to RCLKN rising edge delay from nominal. $delay = \frac{f_{baud}}{10} \pm T_3$	-500	500	ps.	Nominal delay is 10 bit times. Tested on sample basis
T_4	Deviation of RCLK, RCLKN frequency from nominal. $f_{RCLK} = \frac{f_{REFCLK}}{2} \pm T_4$	-1.0	1.0	%	Whether or not locked to serial data
T_R, T_F	R0:9, COM_DET, RCLK, RCLKN rise and fall time	—	2.4	ns.	Between $V_{il(max)}$ and $V_{ih(min)}$, into 10 pf. load.
R_{lat}	Latency from RX to R0:9	15bc + 2ns	34bc + 2ns		bc = Bit clock ns = Nano second
T_{LOCK}	Data acquisition lock time @ 1.25 Gb/s	—	2.4	µs.	8B/10B IDLE pattern. Tested on a sample basis
Receive Data Jitter	Receive Data Jitter Power $\int_{100KHz}^{\frac{1}{2 \times BitTime}} PhaseNoise$	—	40	ps.	dBc, RMS for 10^{-12} Bit Error Ratio Tested on a sample basis

Figure 7: REFCLK Timing Waveforms

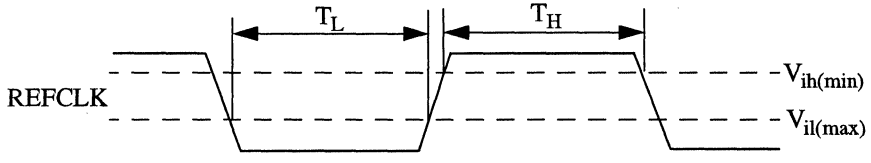
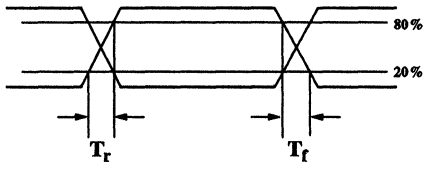


Table 3: Reference Clock Requirements

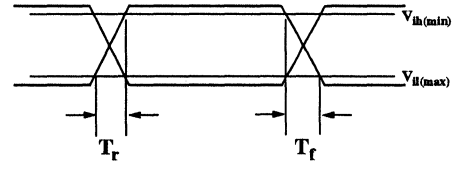
Parameters	Description	Min	Max	Units	Conditions
FR	Frequency Range	118	127	MHz	Range over which both transmit and receive reference clocks on any link may be centered
FO	Frequency Offset	-200	200	ppm.	Maximum frequency offset between transmit and receive reference clocks on one link
DC	REFCLK duty cycle	30	70	%	Measured at 1.5V
T_{RCR},T_{RCF}	REFCLK rise and fall time	—	1.0	ns.	Between $V_{il(max)}$ and $V_{ih(min)}$
REFCLK Jitter	REFCLK Jitter Power $\int_{100Hz}^{5MHz} PhaseNoise$	—	2	ps.	dbc, RMS for FC compliant output data jitter
REFCLK Jitter	REFCLK Jitter Power $\int_{100Hz}^{5MHz} PhaseNoise$	—	40	ps.	dbc, RMS for 10^{-12} Bit Error Ratio with zero length external path. Tested on a sample basis

Figure 8: Parametric Measurement Information

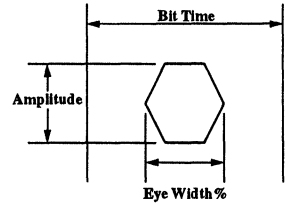
Serial Input Rise and Fall Time



TTL Input and Output Rise and Fall Time

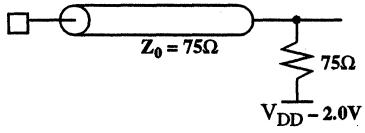


Receiver Input Eye Diagram Jitter Tolerance Mask



Parametric Test Load Circuit

Serial Output Load



TTL A.C. Output Load

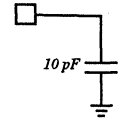
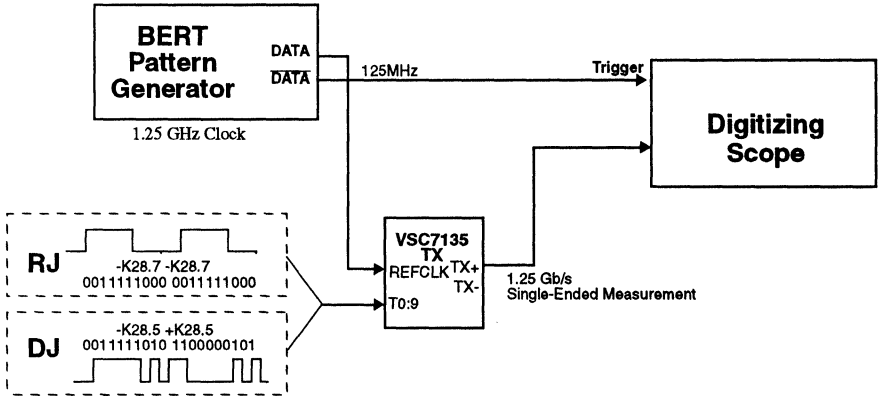


Figure 9: Transmitter Jitter Measurement Method



Random jitter (RJ) measurements performed according to Fibre Channel 4.3 Annex A, Test Methods, Section A.4.4. Measure standard deviation of all 50% crossing points. Peak to peak RJ is ± 7 sigma of distribution.

Deterministic jitter (DJ) measurements performed according to Fibre Channel 4.3 Annex A, Test Methods, Section A.4.3. Measure time of all the 50% points of all ten transitions. DJ is the range of the timing variations.

Absolute Maximum Ratings (1)

Power Supply Voltage, (V_{DD}) ..... -0.5V to +4V
DC Input Voltage (PECL inputs) ..... -0.5V to V_{DD} +0.5V
DC Input Voltage (TTL inputs) ..... -0.5V to 5.5V
DC Output Voltage (TTL Outputs) ..... -0.5V to V_{DD} + 0.5V
Output Current (TTL Outputs) ..... +/-50mA
Output Current (PECL Outputs) ..... +/-50mA
Case Temperature Under Bias ..... -55° to +125°C
Storage Temperature ..... -65°C to +150°C
Maximum Input ESD (Human Body Model) ..... 1500 V

Recommended Operating Conditions

Power Supply Voltage, (V_{DD}) ..... +3.3V±5%
Operating Temperature Range ..... 0°C Ambient to +95°C Case Temperature

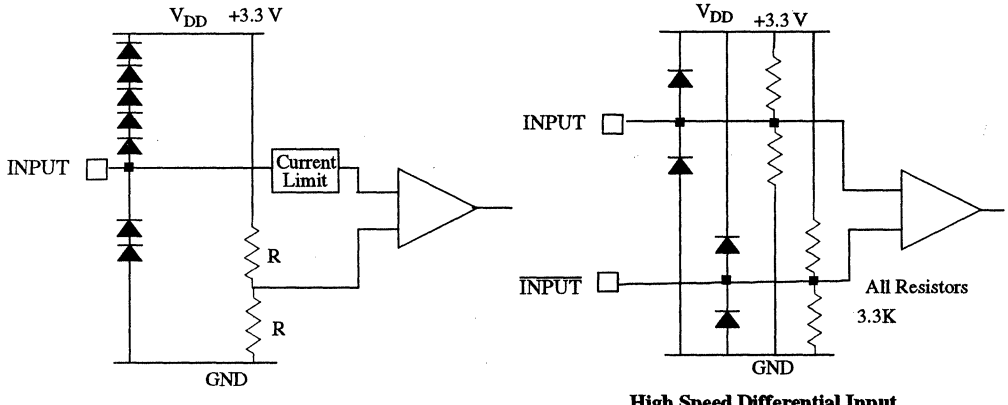
Notes:

(1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

DC Characteristics *(Over recommended operating conditions).*

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage (TTL)	2.4	—	—	V	I_{OH} = -1.0 mA
V_{OL}	Output LOW voltage (TTL)	—	—	0.5	V	I_{OL} = +1.0 mA
ΔV_{OUT75}	TX Output differential peak-to-peak voltage swing	1200	—	2200	mVp-p	75Ω to V_{DD} – 2.0 V
ΔV_{OUT50}	TX Output differential peak-to-peak voltage swing	1200	—	2200	mVp-p	50Ω to V_{DD} – 2.0 V
ΔV_{IN}	Receiver differential peak-to-peak Input Sensitivity RX	400	—	3200	mVp-p	Internally biased to Vdd/2
V_{IH}	Input HIGH voltage (TTL)	2.0	—	5.5	V	
V_{IL}	Input LOW voltage (TTL)	0	—	0.8	V	—
I_{IH}	Input HIGH current (TTL)	—	50	500	µA	V_{IN} =2.4V
I_{IL}	Input LOW current (TTL)	—	—	-500	µA	V_{IN} =0.5V
V_{DD}	Supply voltage	3.14	—	3.47	V	3.3V±5%
P_D	Power dissipation	—	700	1000	mW	Outputs open, V_{DD} = V_{DD} max
I_{DD}	Supply Current	—	210	290	mA	Outputs open, V_{DD} = V_{DD} max

Figure 10: Input Structures



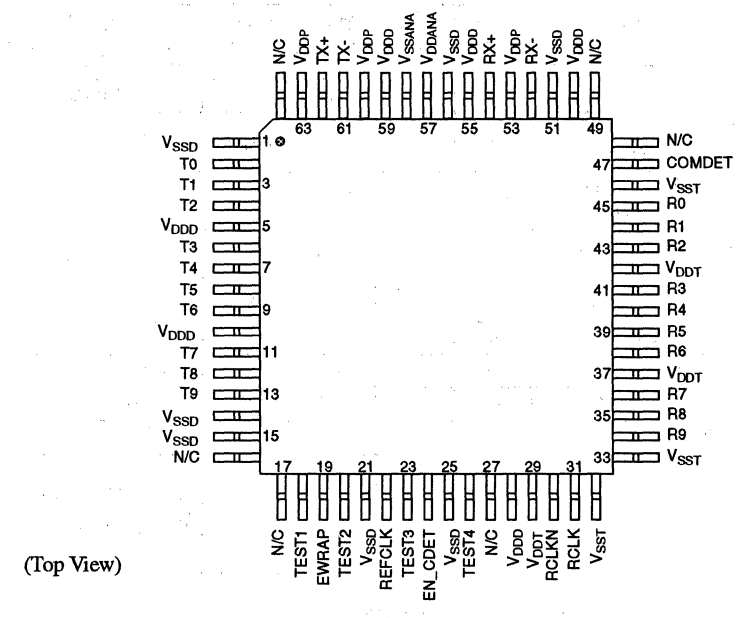
REFCLK and TTL Inputs

A

High Speed Differential Input (RX+/RX-)

B

Figure 11: Pin Diagram



(Top View)

Table 4: Pin Description

Pin #	Name	Description
2-4, 6-9, 11-13	T0:9	INPUTS - TTL 10-bit transmit character. Parallel data on this bus is clocked in on the rising edge of REFCLK. The data bit corresponding to T0 is transmitted first.
22	REFCLK	INPUT - TTL This rising edge of this clock latches T0:9 into the input register. It also provides the reference clock, at one tenth the baud rat,e to the PLL.
62, 61	TX+, TX-	OUTPUTS - Differential PECL (AC Coupling recommended) These pins output the serialized transmit data when EWRAP is LOW. When EWRAP is HIGH, TX+ is HIGH and TX- is LOW.
45-43, 41-38, 36-34	R0:9	OUTPUTS - TTL 10-bit received character. Parallel data on this bus is clocked out on the rising edges of RCLK and RCLKN. R0 is the first bit received on RX+/RX-.

Pin #	Name	Description
19	EWRAP	INPUT - TTL LOW for Normal Operation. When HIGH, an internal loopback path from the transmitter to the receiver is enabled and the TX outputs are held HIGH.
54, 52	RX+, RX-	INPUTS - Differential PECL (AC Coupling recommended) The serial receive data inputs selected when EWRAP is LOW. Internally biased tot VDD/2, with 3.3KΩ resistors from each input pin to VDD and GND.
31, 30	RCLK, RCLKN	OUTPUT - Complementary TTL Recovered clocks derived from one twentieth of the RX+/- data stream. Each rising transition of RCLK or RCLKN corresponds to a new word on R0:9.
24	EN_CDET	INPUT - TTL Enables COMDET and word resynchronization when HIGH. When LOW, keeps current word alignment and disables COMDET.
47	COMDET	OUTPUT - TTL This output goes HIGH for half of an RCLK period to indicate that R0:9 contains a Comma Character ('0011111XXX'). COMDET will go HIGH only during a cycle when RCLKN is rising. COMDET is enabled by EN_CDET being HIGH.
18,20,23	TEST1 TEST2 TEST3	INPUT These signals are used for factory test. For normal operation, tie to VDD.
26	TEST_4	OUTPUT This signal is used for factory test. For normal operation, leave open.
57	VDDANA	Analog Power Supply
58	VSSANA	Analog Ground
5, 10, 28, 50, 55, 59	VDDD	Digital Logic Power Supply
1, 14, 15, 21, 25, 51, 56	VSSD	Digital Logic Ground
29, 37, 42	VDDT	TTL Output Power Supply
32, 33, 46	VSST	TTL Output Ground
53, 60, 63	VDDP	PECL I/O Power Supply
16,17,27, 48,49,64	N/C	No Connection. These pins are not internally connected.

Thermal Considerations

The VSC7135 is packaged in a 14 mm conventional PQFP with an internal heat spreader. This package use an industry-standard EIAJ footprint, but have been enhanced to improve thermal dissipation. The construction of the packages are as shown in Figure 12.

Figure 12: Package Cross Section - 14 mm package

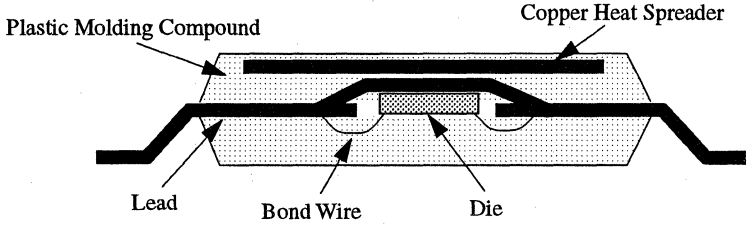
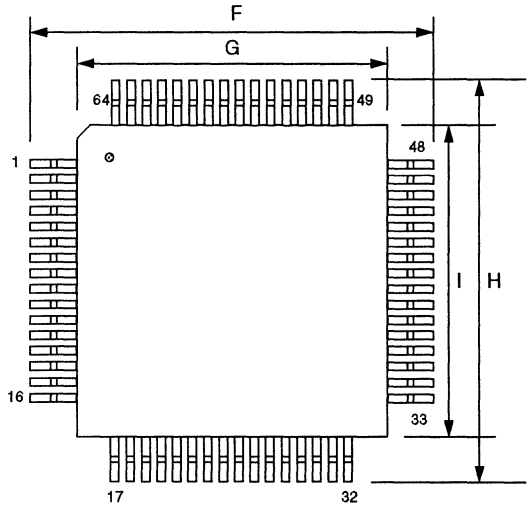


Table 5: Thermal Resistance

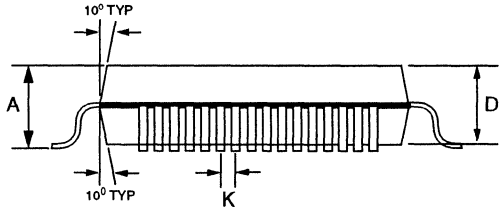
Symbol	*Description*	*14mm Value*	*Units*
θ_{jc}	Thermal resistance from junction to case	17	°C/W
θ_{ca}	Thermal resistance from case to ambient in still air including conduction through the leads.	40	°C/W
$\theta_{ca\text{-}100}$	Thermal resistance from case to ambient with 100 LFM airflow	34	°C/W
$\theta_{ca\text{-}200}$	Thermal resistance from case to ambient with200 LFM airflow	31	°C/W
$\theta_{ca\text{-}400}$	Thermal resistance from case to ambient with 400 LFM airflow	27	°C/W
$\theta_{ca\text{-}600}$	Thermal resistance from case to ambient with 600 LFM airflow	24.5	°C/W

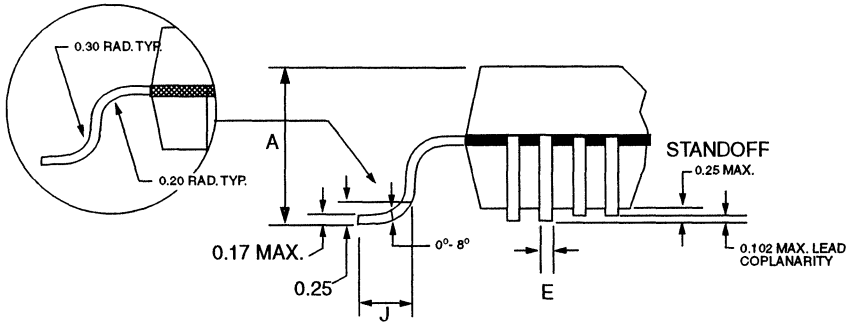
The VSC7135 is designed to operate with a junction temperature up to 110°C. The user must guarantee that the temperature specification is not violated. With the Thermal Resistances shown above, the 14x14 PQFP can operate in still air ambient temperatures of 59°C [59°C=110°C-0.9W*(17°C/W+40°C/W)]. If the ambient air temperature exceeds these limits then some form of cooling through a heatsink or an increase in airflow must be provided.

Package Information: 64-pin PQFP



Item	14 mm	Tol.
A	2.45	MAX
D	2.00	+0.10
E	0.35	±.05
F	17.20	±.25
G	14.00	±.10
H	17.20	±.25
I	14.00	±.10
J1	TBD	TBD
J	0.80	±.15
K	0.80	BASIC





NOTES:
Drawing not to scale.
All units in mm unless otherwise noted.

Ordering Information

The part number for this product is formed by a combination of the device number and the package style:

VSC7135xx

Device Type:

VSC7135: 1.25 Gbps Transceier

Package Style (64-pin)

QN: 14x14mm PQFP

Revision History

Rev. 1.1: Changed Frequency Range to 118-127 MHz

Notice

This document contains information on products that are in the preproduction phase of development. The information contained in this document is based on test results and initial product characterization. Characteristic data and other specifications are subject to change without notice. Therefore, the reader is cautioned to confirm that this datasheet is current prior to placing orders.

Warning

Vitesse Semiconductor Corporation's product are not intended for use in life support appliances, devices or systems. Use of a Vitesse product in such applications without the written consent is prohibited.

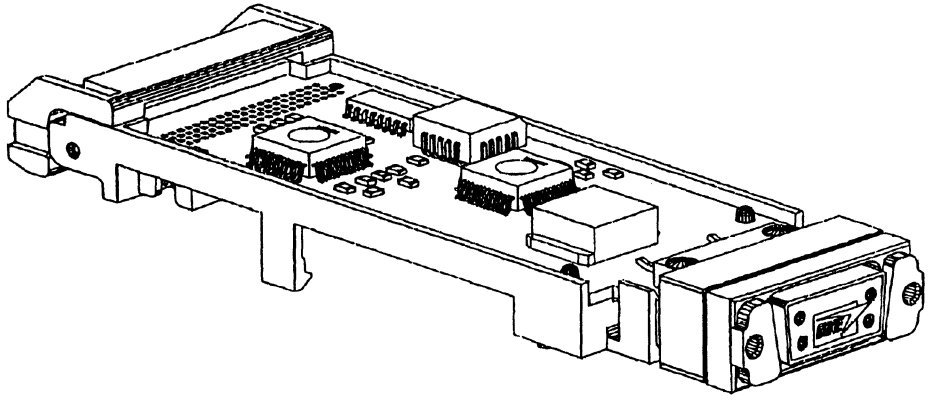
Preliminary Data Sheet

1.0625 Gbit/sec Fibre Channel
Copper Cable Gigabaud Link Module

Features

- Integrated Daughter Card Implementing 1.0625 Gb/s Physical Layer for Transmission Over Copper Cable
- ANSI X3T11 Compliant
- Interchangeable with Boards Designed Using FCSI Gigabaud Link Module Specification
- Duplex (TX and RX) Connection
- System Serial I/O Supported
- 80 Pin Samtec Connector for 20-bit TTL System Interface
- DB9 Connector for Differential Serial Transmission over 150 Ohm, Duplex Cable.
- Parallel and Serial ID Supported
- 5V Power Supply

Copper GLM Module



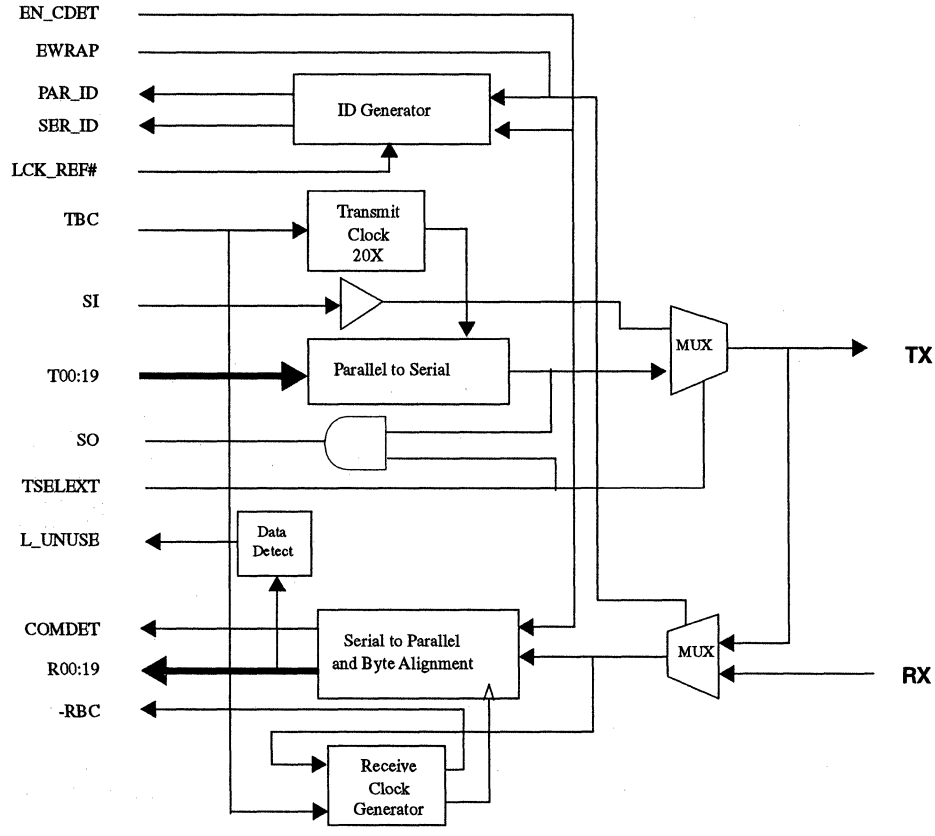
General Description

The VSC7181 is a daughter card "module" fitting the form factor and functionality of the Fibre Channel Systems Initiative's (FCSI) Gigabaud Link Module (GLM) specification operating at full serial data rate of 1.0625 Gb/s over a balanced, twinaxial cable. This product is an extension of the FCSI-301-Rev 1.0 Gigabaud Link Module Specification in that the GLM Rev 1.0 specification only addresses a fiber optic media and this product implements operation over a copper media. Because of this, this product is often generically referred to as a "copper GLM" and abbreviated as CuGLM.

The VSC7181 implements the entire Fibre Channel FC-0 and part of the FC-1 protocol layers for a duplex data link. It accepts a 20-bit parallel data interface; serializes it; and differentially transmits the serialized data over duplex, copper cable on the transmitter side. The VSC7181 receives the serialized data, deserializes it, recovers a clock, and provides 20-bit data and clock back to the system. Please refer to Figure 1 for a functional block diagram.

The VSC7181 uses an 80 pin Samtec connector (MOLC-120-01-F-Q) consisting of 4 rows of 20 pins on a 0.050" x 0.050" grid for the parallel data interface. The VSC7181 uses a DB-9 connector for the serial data interface. Signal placement conforms to the GLM specification on the 80 pin side and to the ANSI X3T11 FC-PH document for the DB-9 side. Refer to the mechanical and electrical sections for detailed information.

Figure 1: Functional Block Diagram



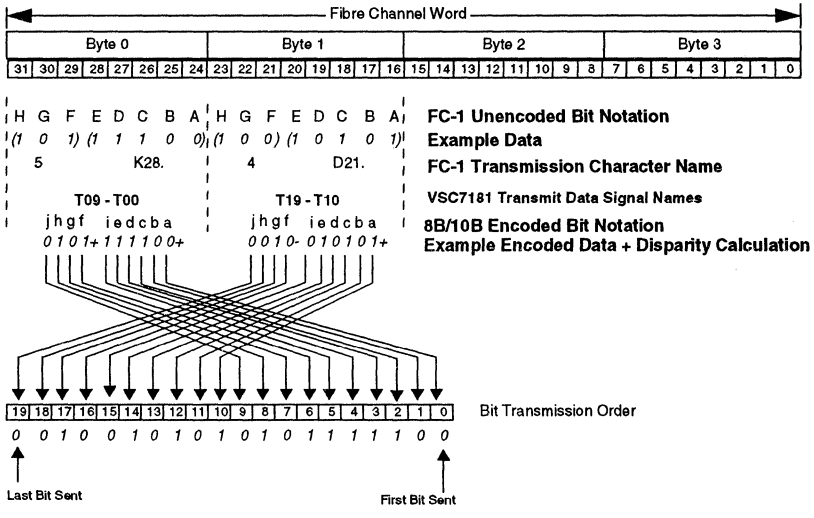
Functional Description

The functional block diagram for VSC7181 is shown in Figure 1. The VSC7181 is a full duplex link. The VSC7181 contains all the high frequency circuits to serialize and transmit and to receive and deserialize data at a 1.0625 Gigabaud rate. The system provides 20-bit data (T19:00) and a 53.125 MHz clock (TBC) for transmission to the VSC7181 and the VSC7181 will provide received 20-bit data and a recovered 53.125MHz clock back to the system. The VSC7181 contains PLL circuits for multiplying the 53.125MHz clock to clock out data at the serial baud rate with low jitter and PLL circuits to reliably receive the serial data and return a half-word clock. The system timing characteristics are described in the Electrical Interface section.

All of the system interface signals (left side signals) are industry standard TTL levels except for the SI and SO signals which are AC-coupled, differential PECL levels. The Gb/s serial transmit and receive signals are AC-coupled, differential levels. The serializer/deserializer chips used in the VSC7181 are Vitesse's VSC7115 and VSC7116 chips respectively.

The VSC7181 accepts 20-bit, 8B/10B or similarly encoded data. The 20-bit interface is two encoded bytes of 10-bits each. For Fibre Channel applications, the bits must correspond to the Fibre Channel bit mapping shown in Figure 2. Fibre Channel maps 32-bit words to a serial transmission and uses a special control character, K28.5, for synchronization and for recognition of special transmission words for link management. As the VSC7181 uses a 20-bit or half-word interface, the position of the K28.5 character in the half-word is important. The position of the K28.5 character must be in pins T09:00 as prescribed in Figure 2.

Figure 2: Fibre Channel Bit Mapping

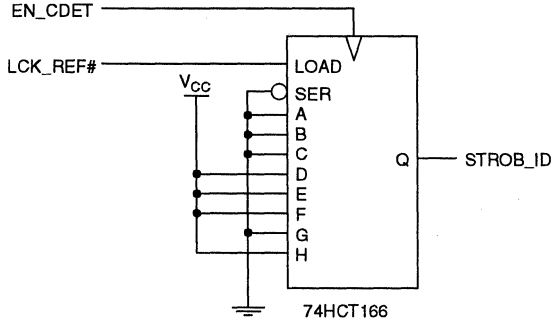


The 20-bit parallel data is serialized and transmitted differentially through the TX+/TX- signals in the bit order shown in Figure 2: "Fibre Channel Bit Mapping" and the incoming serial data is received differentially on the RX+/RX- signal. On the receive end, the VSC7181 will recognize the "comma" character for bit synchronization. The comma character is bits "abcdeif" of the Fibre Channel sync character (K28.5). In a Fibre Channel compliant system, the K28.5 is always expected to have a negative beginning disparity as all Fibre Channel ordered sets end in negative disparity. Hence bits "abcdeif" with negative beginning disparity is "0011111" and the VSC7181 will byte align based on the reception of "0011111" in the bit location corresponding to R00:06. The first time the VSC7181 receives and recognizes a comma, it will align, but the data is not guaranteed to be uncorrupted. Fibre Channel and the VSC7181 expects to receive three commas appropriately placed before guaranteeing good data. Appropriately placed means no more than one comma per half word. Fibre Channel defines transmitting one comma per each 40-bit, ordered set.

Upon the detection of a comma, the VSC7181 will assert the COM_DET signal HIGH and if data was misaligned, the VSC7181 will stretch the recovered clock (-RBC). By stretching the recovered clock, the VSC7181 does not burden the system with a temporarily higher than expected baud rate clock frequency. Additionally, the VSC7181 will not exceed 1.5% of the expected baud frequency even if no data exists on the RX inputs or if a high frequency noise greater than the 20X the REFCLK frequency is present on the RX inputs. If no data is present on the RX inputs, the VSC7181 will issue a indicate link failure by asserting the L_UNUSE signal HIGH. Upon re-connection of good serial data onto the RX inputs, the VSC7181 will lock to the serial data stream within 2500 bit cycles without requiring any additional time to lock to the reference clock. The lock to reference timing is not necessary for synchronizing the PLL on the VSC7181.

The VSC7181 supports the parallel ID and strobed ID defined in the FCSI GLM specification. The PAR_ID(1:0) is set to a 11B value with pullup resistors to VCC. This signifies 1 Gbit/sec operation. A shift register is used to implement the strobed ID. Serial ID data is loaded into the shift register when EN_CDET is clocked while LCK_REF is asserted LOW. Once loaded LCK_REF is asserted HIGH and EN_CDET is used to strobe the contents of the ID register out. The values assigned to each bits are as shown in Figure 3.

Figure 3: Strobed ID Definition



A: LOW 50 meters maximum
B: LOW Unit = Meters
C: LOW No OFC
D: HIGH 1 Gbit/sec
E: HIGH 1 Gbit/sec
F: HIGH 20-bit data
G: LOW Copper
H: HIGH GLM Compliant

H: First data bit transmitted

Several signals impact the routing of data from the parallel inputs or serial inputs to the primary serial output (TX) and the loopback test mode. These signals are EWRAP, TSELEXT, and LRCPBE#. EWRAP is used to select normal operation mode (LOW) from loopback mode (HIGH). TSELEXT is used to control the routing of the system serial I/O (SI) to the primary output (TX) (LOW) or to the system serial output (SO) (HIGH). LRCPBE# is used in conjunction with an FC-AL Hub, so that the host can cause the remote hub to bypass this port and the host can still monitor the previous port through the RX input for PBE or PBD ordered sets. The behavior of these signals are shown in Table 1.

Table 1: Signal Routing Control Behavior

LRCPBE#	*TSELEXT*	*EWRAP*	*SO*	*TX*	*R00:19*	*Explanation*
High	Low	Low	Static	T(00:19)	RX	Normal Host Mode
High	Low	High	Static	T(00:19)	TX	Loopback Mode
High	High	Low	T(00:19)	SI	RX	
High	High	High	T(00:19)	Static	SI	
Low	x	Low	SI	Static	RX	FC-AL Monitoring

Physical Description

The VSC7181 is completely form compatible with the FCSI GLM document for the system side and is form compatible with the bracket opening without shorting bar on the external faceplate with a few exceptions. An I/O card can be designed to be interchangeable with fiber optic GLMs by making the faceplate opening 0.5mm wider than specified in the GLM document. The overall mechanical outline and connectors of the VSC7181 is shown in Figure 5. The bracket opening details are shown in Figure 4.

The VSC7181 serial connector is a custom version of a 9 pin shielded D connector for edge mounting on the daughter card. This connector is the female connector with pin assignments compatible with the X3T11 STP connector described in section 7.3.3 of FC-PH Rev 4.3 and shown in Figure 4. The DB-9 connector is a widely used connector. To minimize user confusion, the male DB-9 connector on the VSC7181 has all non-functional holes plugged. The cable assemblies will then be only populated with the four signals required by FC-PH.

Figure 4: Bracket Opening

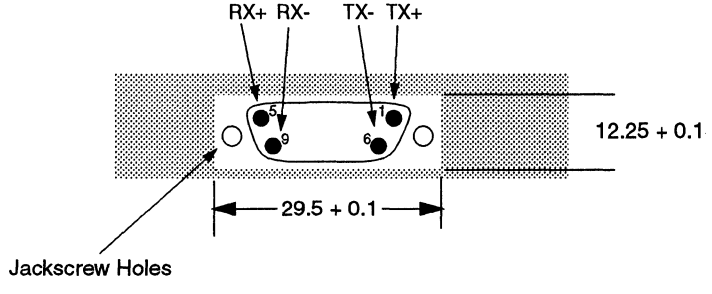
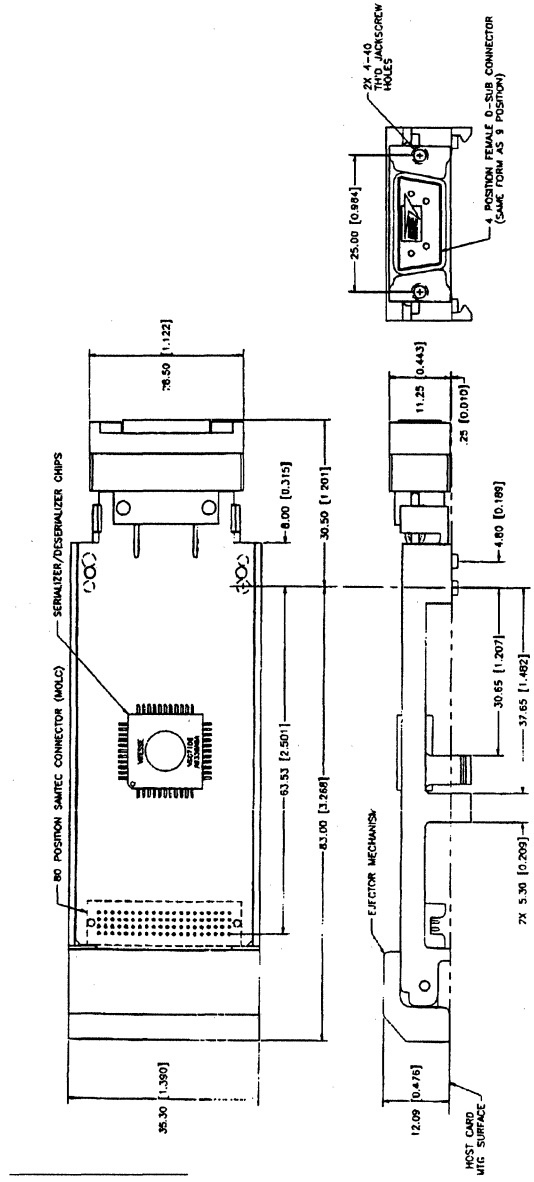


Figure 5: Mechanical Drawing

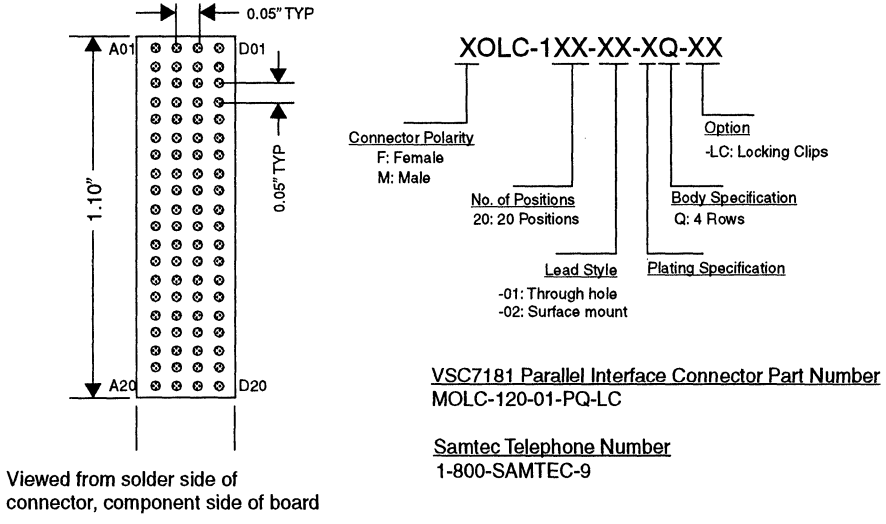


The VSC7181 will support a variety of bracket types (microchannel, ISA, etc.) by accommodating a range of DB-9 protrusions. At a minimum the DB-9 must protrude 2.0mm distance from the faceplate and at a maximum the DB-9 can protrude 6.0mm distance from the bracket faceplate. The DB-9 block design was engineered for galvanic compatibility with common faceplate materials and provides electrical contact to the chassis on the top and bottom to suppress EMI emissions.

The alignment pegs for the VSC7181 that mounts the VSC7181 to the PC board will support back to back mounting of the VSC7181's on a board. The pegs are staggered such that they will not prohibit back to back usage.

The VSC7181 uses a small profile, 80 pin shrouded connector from Samtec. General details on the Samtec connector used for the parallel interface is shown in Figure 6. The VSC7181 uses the male, through-hole mount connector with locking clips. The VSC7181 uses P/N MOLC-120-01-PQ-LC. The user must procure a female connector to mate with the VSC7181. Samtec offers various options for the connector. Detail information on the connector should be procured directly from Samtec at 1-800-SAMTEC-9.

Figure 6: Parallel Interface Connector General Mechanical



The system connector pin out is shown in Table 2. The VSC7181 uses a pinout that is a superset of the one described in the FCSI GLM specification. The VSC7181 adds support for an arbitrated loop hub by using a GLM reserved input pin for a LRCPBE signal. The signal differences are noted in bold, italic font in Table 2.

Table 2: Connector Pin Definition

Pin	*Name*	*Pin*	*Name*	*Pin*	*Name*	*Pin*	*Name*
A01	SO+	B01	SO-	C01	GND	D01	SI+
A02	GND	B02	GND	C02	GND	D02	SI-
A03	+5V	B03	T10	C03	T00	D03	+5V
A04	T12	B04	T11	C04	T02	D04	T01
A05	T14	B05	T13	C05	T04	D05	T03
A06	T16	B06	T15	C06	T06	D06	T05
A07	T18	B07	T17	C07	T08	D07	T07
A08	GND	B08	T19	C08	T09	D08	GND
A09	STROB_ID	B09	GND	C09	GND	D09	+5V
A10	+5V	B10	L-UNUSE	C10	FAULT	D10	TBC
A11	PAR_ID1	B11	RSV	C11	TX_SI	D11	PAR_ID0
A12	RBC0	B12	EWRAP	C12	COM_DET	D12	+5V
A13	+5V	B13	GND	C13	LRCPBE	D13	N/C
A14	GND	B14	R10	C14	R00	D14	GND
A15	R12	B15	R11	C15	R02	D15	R01
A16	R14	B16	R13	C16	R04	D16	R03
A17	R16	B17	R15	C17	R06	D17	R05
A18	R18	B18	R17	C18	R08	D18	R07
A19	+5V	B19	R19	C19	R09	D19	+5V
A20	EN_CDET	B20	GND	C20	GND	D20	LCKREF#

Electrical Interface

The AC timing and signal DC characteristics are shown in this section. The system must provide data and TBC meeting the setup and hold time shown in the Transmit Timing figures and tables. The VSC7181 will provide RBC meeting the data valid window shown in the Receive Timing figures and tables.

Figure 7: Transmit Timing Waveforms

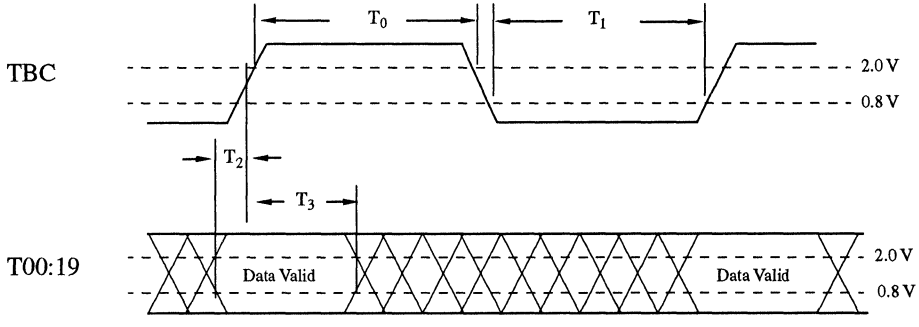


Table 3: Transmit Timing

Parameter	*Description*	*Min*	*Max*	*Unit*	*Conditions*
T_2	Data setup w.r.t. TBC rising edge	2.0	—	ns	Measured from a Data valid HIGH (2.0V) or valid LOW (0.8V) level to TBC midpoint.
T_3	Data hold w.r.t. TBC rising edge	3.3	—	ns	Measured from TBC midpoint to a valid HIGH (2.0V) or valid LOW (0.8V) level.

Table 4: TBC Timing Characteristics

Parameters	*Description*	*Min.*	*Max*	*Unit*	*Conditions*
T_0	TBC min clock pulsewidth HIGH	6.0	—	ns	Measured 2.0V to 2.0V
T_1	TBC min clock period LOW	6.0	—	ns	Measured 0.8V to 0.8V
T_{TCR},T_{TCF}	TBC Rise and Fall Time	1.0	3.2	ns	0.8V to 2.0V
FT	TBC Frequency Tolerance		±200	ppm	TBC Frequency of the two oscillators in a link must meet this tolerance.
T_{DC}	TBC Duty Cycle	35	65	%	Refer to GLM Duty Cycle Calculation

Figure 8: Receive Timing Waveforms

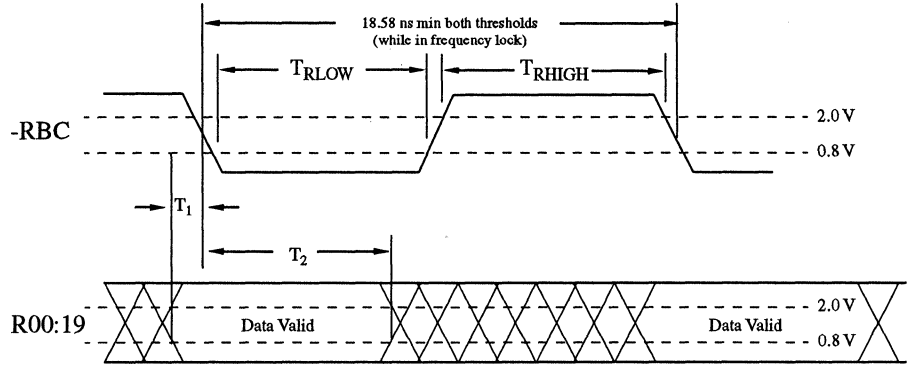
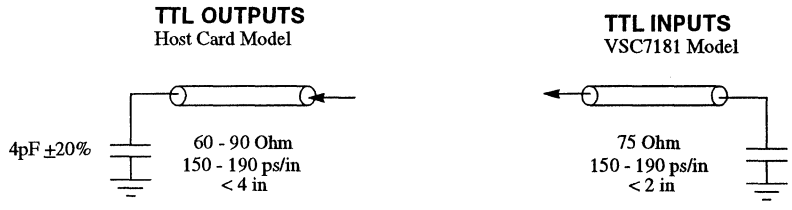


Table 5: Receive Timing

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
T_1	Data valid setup prior to -RBC fall	2.50	—	ns	Measured from -RBC midpoint to a valid HIGH (2.0V) or valid LOW (0.8V).
T_2	Data valid hold after -RBC fall	6.0	—	ns	Measured from -RBC midpoint to a valid HIGH(2.0V) or valid LOW (0.8V)
T_p	-RBC Period when in frequency lock	18.83		ns	
T_{oolp}	-RBC Period when out of lock	18.40		ns	
T_{RDC}	-RBC Duty Cycle when in frequency lock	40	60	%	
T_{RHIGH}	-RBC Min Clock Pulse HIGH	7.0		ns	Measured from Valid HIGH to Valid HIGH (2.0V)
T_{RLOW}	-RBC Min Clock Pulse LOW	6.7		ns	Measured from Valid LOW to Valid LOW (0.8V)
T_{RCR},T_{RCF}	-RBC rise and fall time	1.0	3.2	ns	0.6V to 2.2V, tested on a sample basis, 10pF load
T_{DR},T_{DF}	Data output rise and fall time	—	4.0	ns	0.6V to 2.2V, tested on a sample basis, 10pF load
T_{LOCK}	Data acquisition lock time @ 1.0625Gb/s	—	2.4	µs	8B/10B IDLE pattern sample basis
Input Jitter Tolerance	Input data eye opening allocation at receiver input for BER ≤ 1E-12	30%	—	bit time	As specified in Fibre Channel FC-PH standard eye diagram jitter mask.

Figure 9: Interface Equivalent Circuit for TTL I/O's



Note: All output timing measurements made with 10pF load.

Table 6: DC Characteristics *(Over recommended operating conditions).*

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
$V_{IH\text{-}TTL}$	TTL Valid Input HIGH voltage	2.0	—	5.5	V	$I_{IH} \leq 6.6$ mA @ $V_{IH} = 5.5$ V
$V_{IL\text{-}TTL}$	TTL Valid Input LOW voltage	0	—	0.8	V	—
$V_{OH\text{-}TTL}$	TTL Output HIGH Voltage	2.4	—	3.8[1]	V	$I_{OH} = 0.5$mA
$V_{OL\text{-}TTL}$	TTL Output LOW Voltage	—	—	0.6	V	$I_{OL} = -1.0$ mA
$I_{IH\text{-}TTL}$	Input HIGH current (TTL)	—	—	50	µA	$V_{IN} = 2.4$ V
$I_{IL\text{-}TTL}$	Input LOW current (TTL)	-500	—	-50	µA	$V_{IN} = 0.5$ V
I_D	Power Supply Current	—	0.80	0.95	A	Outputs open, $V_{CC} = V_{CC}$ max
P_D	Power Dissipation	—	4.5	5.2	W	Outputs open, $V_{CC} = V_{CC}$ max
ΔV_{IN}	Serial data differential peak-to-peak input swing SI+/- & RX+/-	300	—	3200	mVp-p	AC Coupled Internally biased at $V_{DD}/2$
ΔV_{OUTTX}	TX+/- differential peak-to-peak output voltage swing	1200	—	3200	mVp-p	75Ω to $V_{DD} - 2.0$ V
ΔV_{OUTSO}	SO+/- differential peak-to-peak output voltage swing	1200	—	3200	mVp-p	50Ω to $V_{DD} - 2.0$ V

Note: [1] Applies to R00:19 only.

Absolute Maximum Ratings (1)

Power Supply Voltage, (+5V) ..... -0.5V to +7.0V
DC Input Voltage, (V_{INT}) ..... -0.5V to 5.5V
DC Voltage Applied to Outputs for High Output State, (V_{out}) ..... -0.5V to V_{DD} + 0.5V
TTL Output Current (I_{OUT}), (DC, Output High) 50mA
PECL Output Current, (I_{OUT}), (DC, Output High) ..... -50mA
Case Temperature Under Bias, (T_C) ..... -55° to +125°C
Storage Temperature, (T_{STG}) ..... -65° to + 150°C
Maximum Input ESD ..... 1500 V

Recommended Operating Conditions(2)

Power Supply Voltage, (V_{DD}) ..... 5V+/-10%
Ambient Operating Temperature Range, (T) (3) ..... 0°C to +110°C

Notes:

1) *CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.*
2) *Vitesse guarantees the functional and parametric operation of the part under "Recommended Operating Conditions: except where specifically noted in the AC and DC Parametric Tables*
3) *Lower limit is ambient temperature. Upper limit is case temperature on the VSC7115 and/or VSC7116.*

Table 7: Input Pin Description

Pin #	Name	Description
C03, D04, C04, D05, C05, D06, C06, D07, C07, C08, B03, B04, A04, B05, A05, B06, A06, B07, A07, B08	T00:19	INPUT - TTL Parallel data on the T00:19 bus is clocked in on the rising edge of TBC. Bit T00 corresponding to 8b/10b bit a. T00 is the first character transmitted. The bit ordering with respect to 8B/10B code is shown below. T00:09 - First Data Byte: 00 01 02 03 04 05 06 07 08 09 8B/10B code character bit: a b c d e i f g h j T10:19 - Second Data Byte: 10 11 12 13 14 15 16 17 18 19 8B/10B code character bit: a b c d e i f g h j
D10	TBC	INPUT - TTL Transmit Byte Clock. This is the 53.125 MHz reference clock provided by the system. The rising edge of TBC is used to clock in the 20-bit parallel data and provides a reference clock for clock recovery on the receive side.
B12	EWRAP	INPUT - TTL Enable Wrap/Enable Strobe ID. Applying a HIGH level to this pin will route serial data output to the deserializer port of the VSC7181 by enabling the TLX outputs of the VSC7115 and enabling the RLX inputs of the VSC7116. This connection is internal to the daughter card. When a LOW level is applied, wrap mode is off, and the serial data is sent out the TX pins and received by the RX pins.
C11	TSELEXT	INPUT - TTL Transmit SI. This signal determines the source of the TX data and the routing of the SI data. When LOW, TX will output the serialized data from T00:19 and SO will be static. When HIGH will output the 1.0625 Gbit/s serial data on the SI pins. and SO will output the serialized data on T00:19.
C13	LRCPBE#	INPUT - TTL Loop Redundancy Circuit Port Bypass Enable. This will disable the TX outputs to a static level when LOW. A 1K pullup is applied to this signal so that if a user does not drive this signal, the TX outputs are enabled.
D20	LCK_REF#	INPUT - TTL Lock to Reference. The receiver in the CuGLM does not require time spent in locking to reference. LCK_REF is used only to load data into the STRO_ID shift register.
A20	EN_CDET	INPUT - TTL ENable Comma DETect. This signal provides control over the byte alignment function of the VSC7181. When LOW, the comma detect and resynchronization circuit is disabled. When HIGH, the VSC7181 will synchronize based on the detection of a comma character. When the link is not operational, EN_CDET is also used to clock data out of the STROB_ID shift register.
DB9 - 5 DB9 - 9	RX+ RX-	INPUT - High Speed, Differential, AC-coupled Receives the 1.0625 Gbit/.s encoded, serial data from the twinax cable. This input is active based on the state of the EWRAP signal.
D01, D02	SI+ SI-	INPUT - AC Coupled, High Speed, Differential Receives the 1.0625 Gbit/s serial data from the system. SI input is transmitted out to SO or TX or deserialized and output on the R00:19 signals based on the state of TX_SI and EWRAP signals.

Table 8: Output Pin Description

Pin #	Name	Description
C14, D15, C15, D16, C16, D17, C17, D18, C18, C19, B14, B15, A15, B16, A16, B17, A17, B18, A18, B19	R00:19	OUTPUT - TTL Parallel receive data on the R00:19 bus for the encode logic in the host system. R00:09 and R10:19 data outputs are staggered by 4.7ns (5 bit times) to minimize TTL switching noise on the daughter card. When synchronized, the bit ordering with respect to 8B/10B code is shown below.

R00:09 - First Data Byte	00	01	02	03	04	05	06	07	08	09
8B/10B code character bit	a	b	c	d	e	i	f	g	h	j
R10:19 - Second Data Byte	10	11	12	13	14	15	16	17	18	19
8B/10B code character bit	a	b	c	d	e	i	f	g	h	j

A12	RBC0	OUTPUT - TTL Recovered Byte Clock. This is the 53.125 MHz recovered byte clock provided by the VSC7181. The data valid window is referenced to the falling edge of RBC0. When resyncing, RBC will be stretched only so no clock slivering will occur. When no data is present at the input or when high frequency noise is present on the input, RBC will remain within 1.5% of the expected baud rate.
C12	COM_DET	OUTPUT - TTL If EN_CDET is HIGH, this signal will be asserted HIGH when a positive comma (0011111) is detected. The K28.5 or other special character containing a comma will appear at R00:09 on the same cycle as EN_CDET is driven HIGH.
B10	L_UNUSE	OUTPUT - TTL This signal indicates to the host system, that no incoming serial data is detected when HIGH.
D11, A11	PAR_ID[0:1]	Static - Pullup Parallel ID. Pullup resistors are tied to these pins to indicate to the host system that a 1.0625 Gbit/s GLM is attached.
A09	STROB_ID	OUTPUT - TTL STROBE ID. This is the output for the 8-bit serial ID register on the VSC7181. Data is strobed out using EN_CDET as the shift register clock.
C10	FAULT	OUTPUT - Resistor Pulldown Not used in the VSC7181. A 1K pulldown is attached to this pin, so it is always LOW. This signal is intended for laser safety which is irrelevant for a VSC7181.
DB9 - 1 DB9 - 6	TX+ TX-	OUTPUT - High Speed, Differential - 75 Ohm Differential serial outputs driving the twinax cable with serialized T00:19 data or SI data. These are outputs are at 75 ohm impedance to ground and 150 ohm differential impedance. When in a static state, TX+ is LOW and TX- is HIGH corresponding to a logic LOW level.
A01 B01	SO+ SO-	OUTPUT - High Speed, Differential - 50 Ohm Differential serial outputs to the host system. TX_SI determines whether serialized T00:19 data is routed to SO or SO is held to a static level. When held to a static level, SO will output a logical LOW which is SO+ LOW and SO- is HIGH.

Preliminary Data Sheet

1.0625 Gbit/sec Fibre Channel
Copper Cable Gigabaud Link Module

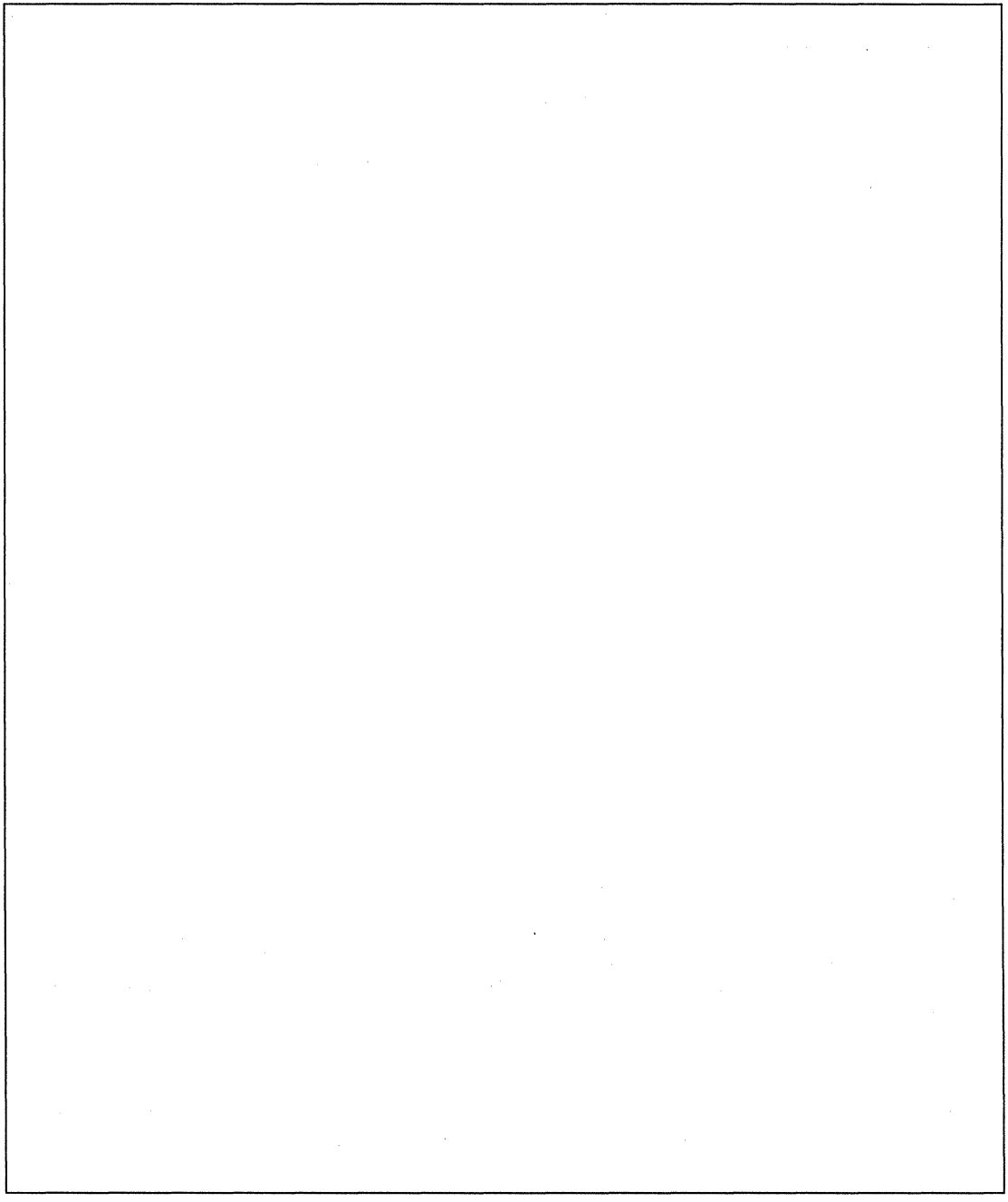
Ordering Information

Notice

This document contains information about a product during its preproduction phase of development. The information contained in this document is based on test results and initial product characterization. Characteristic data and other specifications are subject to change without notice. Therefore the reader is cautioned to confirm that this datasheet is current prior to placing orders.

Warning

Vitesse Semiconductor Corporation's product are not intended for use in life support appliances, devices or systems. Use of a Vitesse product in such applications without the written consent is prohibited.



Product Preview

1.0625 Gbit/sec Fibre Channel
CuGLM Evaluation Kit

Contents

- Two (2) VSC7181 CuGLM
- One (1) 5m Gore Fibre Channel Duplex Cable Assembly with DB-9 Connector
- Optional 24m Cable Available
- One (1) Female Loopback Adaptor
- One (1) Male Loopback Adaptor
- *Fibre Channel: Connection to the Future* Book by FCA
- Vitesse and Gore Fibre Channel Products Documentation

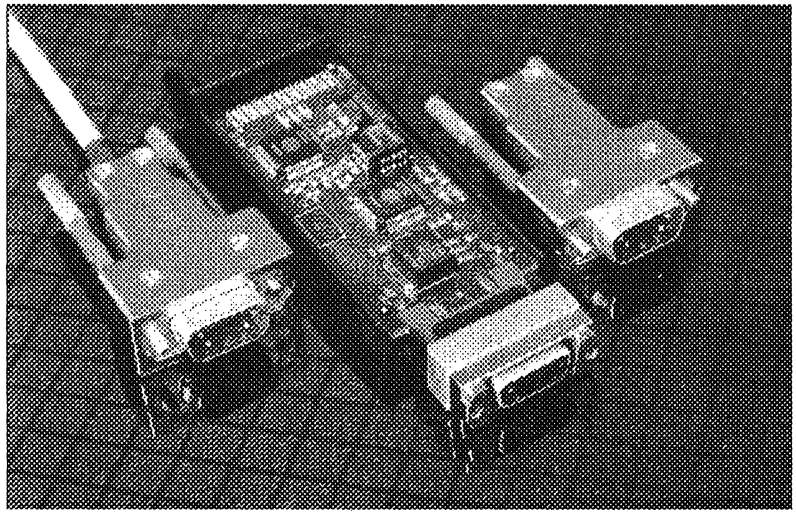
Benefits

- FCSI GLM Interchangeability with Optics
- ANSI Compliance
- Robust and Integral EMI Connection to the Chassis
- Embedded Equalization in Cable Assembly
- Low Cost
- Compatible with Lower-cost, Non-GLM, DB-9 Implementations
- Compatible with Resilient FC-AL Logical Loop - Physical Star Implementation

General Description

This kit contains a complete ANSI FC-PH compliant link solution for transporting data at 1.0625 Gbit/sec rate over an electrical media and is made available through the cooperative efforts of Vitesse Semiconductor and W.L. Gore and Associates, Inc. This solution is based on the DB-9 connector transported over an wide-band-width, full -duplex cable assembly in the configuration defined in the ANSI FC-PH 4.3 section 7.3.3. document. Additionally, this solution is an extension of and is compatible with the Fibre Channel System Initiative's (FCSI) Gigabaud Link Module (GLM) specification for optical daughter cards.

CuGLM Evaluation Kit



1.0625 Gbit/sec Fibre Channel
CuGLM Evaluation Kit

Product Preview

This kit consists of two copper-based GLM daughter cards hereafter referred to as CuGLM and a 5 meter length of the Gore duplex cable assembly along with both female and male loopback plugs for testing. Additionally, documentation is included to provide information on how to use Vitesse and Gore solutions for low-cost, high reliability, copper-based interconnection for Fibre Channel's storage and clustered computing work group applications as well as general Fibre Channel information.

The basis of this solution is applying the robust characteristics of differential transmission to the already robust 8B/10B encoding adopted by Fibre Channel to enable 30 - 50m transmission over copper cabling to provide lower than 10^{-12} bit error rate without EMI problems for 1.0625 gigabaud data transmission. Differential data transmission has several advantages. The added cost for transformer coupling is not required. Differential signaling provides for greater noise immunity with a smaller connector and cable diameter by taking advantage of the inherent mutual coupling. Differential transmission provides a return current through the signal conductor, so very little current is sent over the shield easing the problems of EMI grounding.

The DB-9 connector solution was selected due to its low-cost, but good 360° shielding characteristics. The ubiquitous DB-9 connector is seldom seen as a high frequency connector, but given differential transmission and the DB-9's 360° shielding, it actually performs extremely well while providing the additional benefits of fitting a slightly larger faceplate opening used by optical GLM's and of being a low-cost and mature connector infrastructure.

By merging the requirements of both the ANSI standards body and the industry FCSI group, this interconnect solution provides the most versatile and complete solution for gigabaud data transport over a copper media.

Order Information

VSC7181EV - X

Product Name

Option
5: 5V Supply

VSC7181EV - LC

Product Name

Option
LC: 24m Cable

Preliminary Data Sheet

1 GByte/Sec SCI Compliant Link Controller

Features

- Conforms to IEEE SCI Standards: IEEE Standard 1596-1992
- Sends and Receives SCI Data in 2ns for 1GByte/s Data Rate
- 18 Signal Parallel Link Interface
- High Speed Link Interface Conforms to Low Voltage Differential I/O Standard (IEEE P1596.3)
- 64-Bit Bi-Directional GTL System Interface
- +3.3V and +2V Power Supplies Required
- 4 Entry Send Queue, 8 Entry Receive Queue Buffers
- 269 Tape Ball Grid Array Package (TBGA - 50 mil centers)
- IEEE Std 1149.1 Test Access Port for Diagnostics

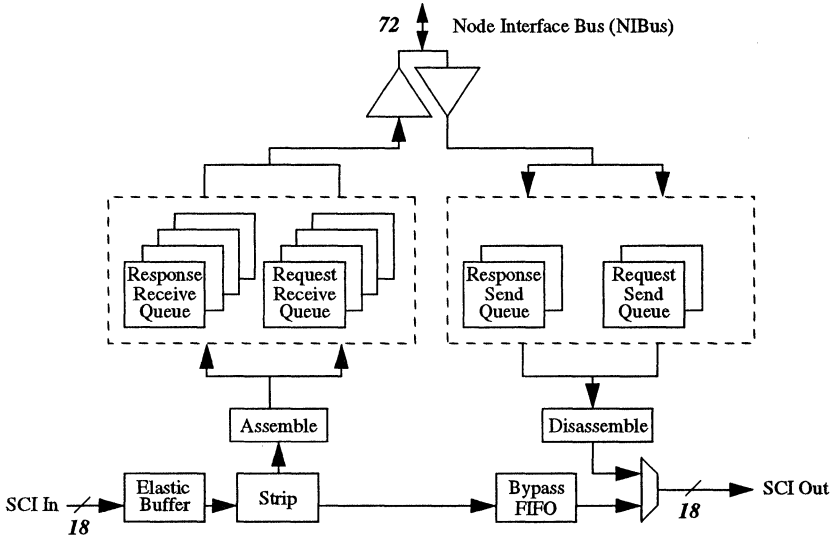
1.0 Introduction

The Scalable Coherent Interface (SCI) provides services similar to those commonly offered in a computer bus architecture. In a multiprocessor environment, however, the scalability of a traditional bus is limited by physics; specifically, problems associated with tapped transmission lines, reflections and capacitive loading. To overcome these problems SCI uses a collection of fast point-to-point unidirectional links instead of a physical bus.

A packet transfer protocol is used by SCI to implement various transactions on the high speed links. This arrangement scales very well from a small number of nodes to a large number of nodes. And SCI has specified protocol and link management to guarantee deadlock free transmission ensuring forward progress on all nodes.

The VSC7201A SCI DataPump implements the link physical transport layer of SCI including guaranteed delivery and forward progress protocol.

VSC7201A - Block Diagram



2.0 Terms and Conventions

For reference consult the following documents;
1) IEEE Std 1149.1-1990 IEEE Standard Test Access Port And Boundary-Scan Architecture.
2) IEEE Std 1212-1991 IEEE Standard Control and Status Register Architecture for Microcomputer Buses.
3) IEEE Std 1596-1992 IEEE Standard for Scalable Coherent Interface (SCI).

2.1 Bit and Byte Ordering

The addressable unit in SCI is the byte. SCI packets are constructed from 2-byte (doublet) symbols.

Bit zero is always the most significant bit of a symbol, byte zero is always the most significant byte of a symbol, and the most significant doublet of the address always comes first. Bytes within a packet progress from byte[0] to byte[N] with increasing time. This is big-endian packet notation.

Registers on the DataPump are defined as 4 bytes (quadlet) in size. Data transfers on the NIbus between the DataPump and node interface logic are 8 bytes (octlet) in size. For address invariance, the mapping of bytes within a packet to bytes within a quadlet or octlet is always the same, with byte[0] being the most significant. On the NIBus this means that DATA[0] maps to bit[0] of byte[0] and DATA[63] maps to bit[7] of byte[7]. Within a register, byte[0] is the most significant and byte[3] is the least significant. This big-endian notation implies that smaller address values are more significant than larger ones.

For the defined packets and registers, the sizes of all fields within the data unit (e.g. doublet, quadlet, octlet) are specified; the bit position of each field is implied by the size of the fields to its right or left with the leftmost bit position being 0, or most significant. This labelling convention is more compact than bit-position labels, and avoids the question of whether 0 should be used to label the most or least-significant bit.

2.2 Numerical Values

Decimal, hexadecimal, and binary numbers are used within this specification. Decimal numbers are represented in their standard 0, 1, 2, ... format. Hexadecimal numbers are represented by a string of one or more hexadecimal (0-9, A-F) digits followed by the subscript 16. Binary numbers are represented by a string of one or more binary (0,1) digits followed by the subscript 2. The character x or X is sometimes used as a character in hexadecimal and binary formats and represents the "don't care" value. Each x or X is one digit in size.

3.0 Quick Signal Pin Reference

3.1 Node Interface Bus (NIBus) Signals

Signal	Type	Level	# Pins	Description
PDATA[0:63]	IO	GTL	64	Data for packet transfer.
PPARITY[0:7]	IO	GTL	8	Byte parity on PDATA. Good parity is odd. PPARITYO corresponds to PDATA [0:7]
NDPSEL	In	GTL	1	DataPump chip select.
PCMND[0:2]	In	GTL	3	DataPump access command for queue and register reads and writes.
NNIACK	In	GTL	1	From node interface logic indicating successful access command completion.
NNIRDY	In	GTL	1	Transfer flow control from node interface logic. Assert equals ready to transfer. De-assert for wait.
NDPACK	Out	GTL	1	From DataPump indicating successful access command completion.
PRCVREQ	Out	GTL	1	Indicates Receive Request Queue has data.
PRCVRSP	Out	GTL	1	Indicates Receive Response Queue has data.
PSNDREQ	Out	GTL	1	Indicates Send Request Queue has space.
PSNDRSP	Out	GTL	1	Indicates Send Response Queue has space.
NINTRNI	Out	GTL	1	Node interface logic interrupt for asynchronous link events and errors.
NERRNI	Out	GTL	1	Asserted low when a node interface bus error occurs.
PCLKSTB	Out	GTL	1	Indicates clockStrobe packet was output on the SCI link.
NRESET	In	GTL	1	Resets DataPump and SCI link.
NSYNCRQ	In	GTL	1	Request to send Sync packet.
NSCRUB	In	GTL	1	Selects DataPump as SCI link scrubber.
PPC[0,1]	Out	GTL	2	Performance counters outputs.
CLKNI	In	TTL	1	Input Clock for NIBus.
CLKHI, NCLKHI	In	Diff.GTL	2	Differential SCI clock input for multiplication to 500Mhz.
PCKHMPY[0:1]	In	GTL	2	Divider value for CLKHI to produce internal SCI clock. See SCI clock divide table in Section 5.1.17.
PCLK250	In	TTL	1	Works in conjunction with PCKHMPY[0:1] to determine internal clock rate. See SCI clock divide table in Section 5.1.17.
VGREF	In	ANALOG	1	GTL external reference input

3.2 SCI Link Interface Signals

Signal	Type	Level	# Pins	Description
PSCISI, NSCISI	In	LVDS	2	SCI differential input strobe.
PSCIFI,NSCIFI	In	LVDS	2	SCI differential input flag.
PSCIDI[0:15], NSCIDI[0:15]	In	LVDS	32	SCI differential input data.
PSCISO, NSCISO	Out	LVDS	2	SCI differential output strobe.
PSCIFO, NSCIFO	Out	LVDS	2	SCI differential output flag.
PSCIDO[0:15], NSCIDO[0:15]	Out	LVDS	32	SCI differential output data.

3.3 Test Access Port and Internal Scan Test Signals

Signal	Type	Level	# Pins	Description
PTDI	In	TTL	1	JTAG Test Access Port (TAP) Test Data In.
PTMS	In	TTL	1	TAP Test Mode Select
PTCK	In	TTL	1	TAP Test Clock.
PTDO	Out	TTL	1	TAP Test Data Out.
NTRST	In	TTL	1	TAP Test Reset.
PCKHSEL	In	TTL	1	CLKHI bypass select mux. When asserted CLKHI input will bypass the PLL and drive the internal SCI clock directly.
PTSTMD	In	TTL	1	Not used. Always assert low.
PSTEP	In	TTL	1	Not used. Always assert low.
PSTOP	In	GTL	1	Not used. Always assert low.
PMAINTMD[0:1]	In	TTL	2	PMAINTMD0 toggles NIBus parity checking. PMAINTMD1 modifies initialization sequence for test purposes.
PDIV10OUT	Out	TTL	1	Internal 1GHz PLL clock divided by 10 test output.
IPNC	In	TTL	1	Factory test scan input. Tie to VCC.
OPNC	Out	TTL	1	Factory test scan output. Do not connect.
TE	In	TTL	1	Factory test enable. Tie to VCC.

Total Signal Pins = 181

4.0 SCI Overview

The objective of the Scalable Coherent Interface (SCI) standard is to provide a high performance interconnect system between processors and processor elements for tightly coupled, cache coherent data communication.

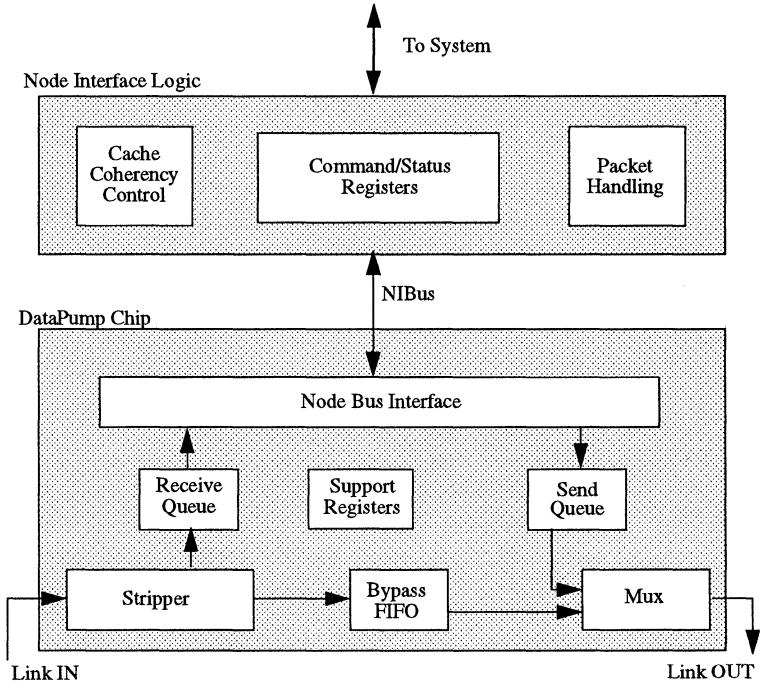
SCI utilizes point-to-point links and passes data packets to avoid the problems of bus design such as shared resource bandwidth bottlenecks and design of multi-drop, high speed backplane transmission lines.

The DataPump chip provides high speed SCI links, sends and receives packets, and manages the data transfer on the SCI physical layer.

4.1 SCI Node Model

A complete SCI node consists of high speed SCI input and output links, queues for receiving and sending packets, a bypass FIFO for storage when the node is sending a packet, and upper level protocol management for transaction handling. Figure 4.1 shows a block diagram of an SCI node.

Figure 4.1 : SCI Node Mode



The SCI function is broken into two distinct blocks. The physical link interface and queues for packets are handled on the DataPump chip, also known as a link controller. The higher level protocol such as packet handling, cache coherence, CSR (control and status register) register support, and interface to the system is handled in node-specific interface logic.

Therefore, the DataPump chip takes care of getting data packets on and off the high speed SCI link and transferring those packets to and from the node interface logic.

4.2 DataPump Block Description

The basic block diagram of the DataPump is shown in Figure 4.1. Data is received at the stripper block on the link inputs.

The start of a data packet contains header information. The first 16-bit symbol in the header is the nodeId address of the target node to receive the packet. The stripper block checks this targetId to see if the packet is for this node. If so, the packet is stripped off the ringlet. If there is receive queue space available, the packet will be stored for later unloading by the node controller. If there is no queue space available the received packet will be discarded and a message will be sent to the sender to retry the packet again later.

The receive queue block is split into storage for two types of packets, requests and responses. There is room for up to four packets of each type. Within receive request or response queues, slots are assigned on a first-in/ first-out basis.

If the packet is not intended for this node it is sent through the bypass FIFO. The bypass FIFO is required to store a packet as it is received if the DataPump is sending data at the same time. The send queue can only begin to transmit a packet if the bypass FIFO is empty. It is only allowed to transmit one packet at a time before it must again check the bypass FIFO. Therefore, the storage size of the bypass FIFO must be large enough to buffer the largest packet size which can be sent.

The send queue is also split into two types, requests and responses, of which there are two queue slots for each type. The queue slots are loaded from the node interface logic and the slot loading order and transmission order is based on packet age.

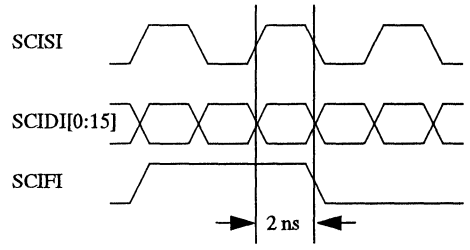
The DataPump also contains bus interface logic for communication with the node interface logic and on-board registers for node control and status register (CSR) support. However, on-chip registers are only provided to control the operation of the DataPump - full CSR support according to IEEE Std 1212-1991 must be provided by the node interface logic.

4.3 Physical Layer Connection

The SCI physical layer connection consists of 18 differential input and output signals. The inputs consist of 16 data signals (PSCIDI[0:15]), a flag bit (PSCIFI) used to delimit packets, and a strobe signal (PSCISI) for latching incoming data. The outputs consist of 16 data (PSCIDO[0:15]), a flag (PSCIFO), and strobe (PSCISO).

Each 16-bit data quantity transferred is called a symbol and is clocked on each rising and falling edge of the strobe signal. The 16 data plus flag signals transition in phase every 2ns (250 MHz) giving an effective data transfer rate of 1Gbyte/sec. Figure 4.2 illustrates these signals using single-ended notation.

Figure 4.2 : SCI Link Signals

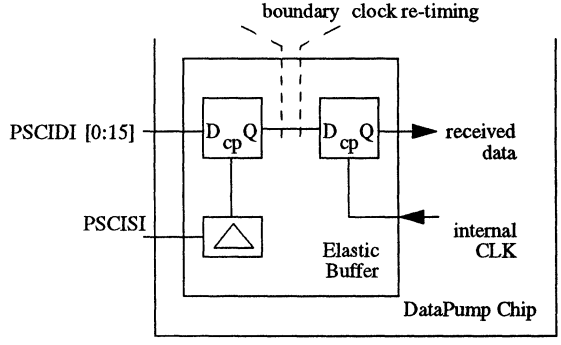


The received strobe PSCISI is used for latching data and flag, but is not used for generating the output strobe PSCISO. The DataPump chip generates its own internal clock for clocking data through the high speed data path and driving out PSCIDO[0:15], PSCISO, and PSCIFO.

The internally generated clock is not guaranteed to be in phase with nor at precisely the same frequency as the incoming PSCISI. Therefore, all SCI link input signals are received on chip through the elastic buffer which re-times the signals to the internal high speed clock and inserts or deletes symbols with a logic state machine to account for small frequency differences between incoming symbols and the internal clock. The clocking boundaries and elastic buffer data re-timing function are shown in Figure 4.3.

Symbols called idle symbols are transmitted between data packets or if no packets are being sent. The elastic buffer will only delete idle symbols, not symbols within a packet. Every packet must be followed by at least one idle symbol. This guarantees that there will always be enough idle symbols received which can be deleted in order to make up for the worst case clock frequency difference.

Figure 4.3 : Elastic Buffer Data Re-timing



4.4 Packet Formats

SCI defines two groups of packet types; those packets involved in the logical protocol (send and echo packets), and other special link related packets.

The VSC7201A does not support any of the special init packets except for the SYNC packet.

4.4.1 Basic Send and Echo Packets

The packets involved in the logical protocol consist of four types; request-send, request-echo, response-send, and response-echo.

Logical protocol transactions are initiated with a requester and completed by a responder. Each transaction consists of two sub-actions; a request sub-action wherein command and possibly data are passed to the responder and a response sub-action where completion status and possibly data are returned to the requester.

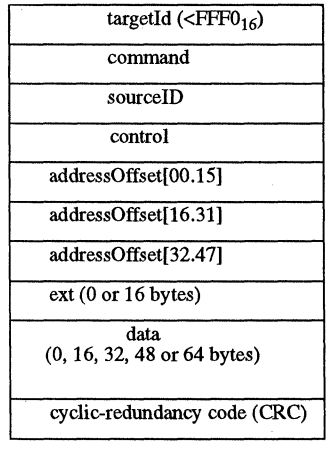
Each sub-action involves two packet transfers. One is a send packet initiated at the output link of a producer node and the second is an echo packet returned by the consumer node and received on the input link of the producer node.

Hence, normal SCI transactions are usually four-way transactions initiated with a send-request packet from a requester. The target of the request (the responder) sends an acknowledgment of receipt of the request packet by returning a request-echo packet. When the responder is ready with the requested data, it sends a response-send packet and the original requester acknowledges with a response-echo packet.

All packets are an integer multiple of four symbols in length. The DataPump supports all SCI packet types except 256-byte block sizes. Therefore, the largest packet size is 96-bytes, or 48 16-bit symbols.

The DataPump also uses full 16-bit nodeIds for targetId and sourceId decoding.

Figure 4.4 : Request Send Packet Format



The basic request-send packet construction is shown in Figure 4.4. Each block in Figure 4.4 comprises a 16-bit symbol value. The targetId is the 16-bit nodeId of the target node. Node ID values above $FFF0_{16}$ are special reserved values.

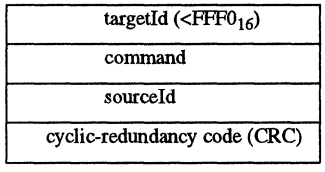
The command and control fields contain command and flow-control information. Some of the bits used for flow-control are modified by the DataPump chip. See sections 4.6 and 4.7. The sourceId is the 16-bit node ID of the sending node. The 48-bit address offset is interpreted by the responder.

A packet may also contain a 16-byte extended header. The presence of extended header is indicated by a bit (com.eh) in the command field.

The CRC (cyclic redundancy code) symbol at the end of the packet allows for error checking the entire data packet upon reception.

When transmitting a packet from the send queue, the DataPump forms the CRC and appends it to the end of the packet. When receiving a packet into the receive queue, the DataPump forms the CRC as the packet is being received and checks the generated value against this transmitted value to ensure data correctness.

Figure 4.5 : Request-Echo and Response-Echo Packet Format



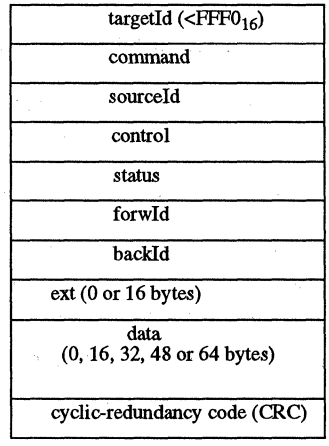
The node interface logic external to the DataPump does not need to check or generate the CRC.

Echo packets are 4 symbols long containing the source and target IDs exchanged, a command symbol which is a modified version of the send command, and the CRC.

The DataPump automatically generates all required echo packets as a result of received packets. The node interface logic external to the DataPump cannot generate or receive echo packets.

The basic echo packet is shown in Figure 4.5.

Figure 4.6 : Response-Send Packet Format



The basic response packet is shown in Figure 4.6. The response packet is similar to request packet except a status symbol and two nodeId pointers called forwId and backId are returned. These are used in the cache coherency scheme.

The DataPump does not, however, handle any upper level cache coherency protocol management. Response packets are simply queued with a length of packet indicator.

The DataPump also manages data flow control information contained within packets and idle symbols. When no packet is being received, 16-bit idle symbols are received. The DataPump stores and transmits these idles, while checking and managing flow control information contained in the idle symbol. For more detailed information about packet types and fields within packets, consult the IEEE Std 1596-1992.

4.4.2 Command and Control Symbols

The DataPump uses certain bits in the command and control fields for transaction and flow control. The format for these fields is defined in Figure 4.7. These fields are explained briefly in Table 4.1

Figure 4.7 : .Command and Control Symbols

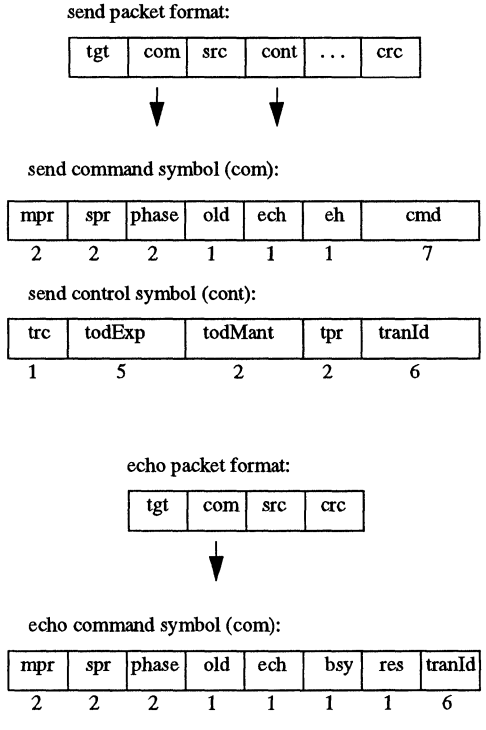


Table 4.1: Command and Control Bit Fields

Bit Field	*Description*
com.mpr	Maximum ringlet priority field. Passed but not used by DataPump.
com.spr	Send priority. Passed but not used by DataPump.
com.phase	Used by queue control on DataPump. See 4.7 Queue Allocation.
com.old	Packet aging used by scrubber DataPump to remove old packets.
com.ech	Indicates echo packet; com.ech=0 for send, com.ech=1 for echo. Set by DataPump during transmission.
com.eh	Indicates use of extended header. If set to 1 a 16-byte extended header is present.
com.cmd	Specifies transaction command.
com.bsy	Used in echo packet to indicate no queue space available on target node. See 4.7 Queue Allocation.
com.res	In echo packet indicates request or response echo; com.res=0 for request, com.res=1 for response.
com.tranId cont.tranId	Transaction Id set by requester in send-request packet. This tranId value is used in all subaction packets related to the request.
cont.trc	Trace bit. Passed but not used by DataPump.
cont.todExp	Time-of-death; exponent. Passed by but not used by DataPump.
cont.todMant	Time-of-death; exponent. Passed by but not used by DataPump.
cont.tpr	Transmit priority, set by node interface. Passed but not used by DataPump.

4.4.3 Idle Symbols

Idle symbols fill the spaces between packets. They contain bits associated with ringlet flow control which the DataPump uses to manage the SCI link. Figure 4.8 shows the bit fields and Table 4.2 defines these fields. The least significant byte is the complement of the most significant byte and is used for a simple parity check.

Figure 4.8 : Idle Symbol Fields

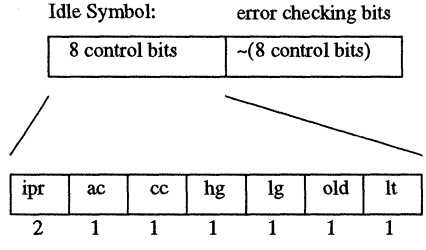


Table 4.2: Idle Symbol Field Descriptions

Bit Field	*Description*
idle.ipr	Idle-priority used for ringlet priority; not used. Set to low.
idle.ac	Allocation count, toggles when all nodes are enabled to transmit.
idle.cc	Circulation count, indicates when idle has circulated around ringlet.
idle.hg	High go bit; not used. Set to low.
idle.lg	Low go bit; see Section 4.6 Bandwidth Allocation.
idle.old	Packet aging bit - used by scrubber to remove old packets from ringlet
idle.lt	Low type priority class bit; not used. Set to low.

4.4.4 SYNC Packet and its Flag Encoding

The sync packet is used during initialization for synchronizing the link and can also be sent during normal operation by asserting the NSYNCRQ pin. Although the VSC7201A doesn't have autodeskewing on its input pins, future versions may use the received SYNC packet for deskewing SCI inputs. The format for the SYNC packet is shown in Figure 4.9. No other SCI defined special packets (e.g. ABORT, RESET, etc.) are supported or needed by the VSC7201A. For further information on reset and initialization and the use of the SYNC packet, see sections 4.10 DataPump Reset.

Figure 4.9 : SYNC Packet Format

Symbol		Flag
0	1111111111111111	1
1	0000000000000000	0
2	0000000000000000	0
3	0000000000000000	0
4	0000000000000000	0
5	0000000000000000	0
6	0000000000000000	0
7	0000000000000000	0

SYNC Packet

4.4.5 Packet and Idle Alignment to SCI Strobe

For performance reasons the DataPump aligns all packet transmisions to start with the first symbol driven when PSCISO (strobe out) is high. The DataPump also expects to receive packets aligned so that the first symbol is received when PSCISI (strobe in) is high.

Therefore, the minimum number of idle symbols between packets will be 2 and idle deletion and insertion will be done on idle pairs. Idle pairs are also aligned with strobe high followed by strobe low.

4.5 Transaction Commands

The command in an SCI send packet identifies one of four main types of transactions. Those are response-expected request, move request, event request, and response. The DataPump only decodes the transaction command to determine if it is greater or less than 124 indicating a response versus request packet, or if it is an event00 (clockStrobe) command.

Data payload size within a send packet is only checked for the SCI legal multiple of 8 symbols and for excessive length. When the end of a send packet is received it is checked for length equal to a multiple of 8 symbols and if not is rounded out to 8 symbols, then processed normally.

A send packet not targeted for this VSC7201A is not stripped and is only checked for size less than or equal to 48 symbols. Packets of this length will be bypassed without error as long as they are a multiple of 8 symbols.

Packets which are stripped by the DataPump are checked for length less than or equal to the maximum queue buffer size of 48 symbols. As long as stripped packets are of this size and are a multiple of 8 symbols they will be queued normally.

The transaction types uniquely treated by the DataPump are summarized in Table 4.3. Packet sizes for these commands are only checked as outlined above. For example, a nread256 command implies a data payload of 256-bytes but is not checked for that payload size by the DataPump and could in fact be only 64-bytes.

Table 4.3: DataPump Receive Packet Handling

Received Packet Type	*Packet Handling*	*Comments*
response-expected request	strip if targeted node and generate echo; else bypass	DataPump only checks command value is less than 124 and not event00
response	strip if targeted node and generate echo; else bypass	DataPump only checks that command value is greater than or equal to 124
directed move (dmovexx)	strip if targeted node and generate echo; else bypass	Command value not distinguished from response-expected request
broadcast move (rmovexx, smovexx)	not supported	Command value not distinguished from response-expected request
clockStrobe (event00, time-of-day clock)	strip and toss if targeted node; else bypass	See Section 4.5.1 Event00 (clockStrobe) Transaction
event16, event64	not supported	Command value not distinguished from event00
echo packet	strip if targeted node; else bypass	stripped echo packet information is used to determine send packet status; see send packet handling in 4.7 Queue Allocation

4.5.1 Event00 (clockStrobe) Transaction

The event00 transaction is supported by the DataPump as the (time-of-day) clockStrobe signal. If targeted to a DataPump, the Event00 packet is accepted immediately and no echo is generated. If received and not targeted to the DataPump, it bypasses the packet.

The DataPump which transmits an event00 targeted to itself from its send queue is called the clockStrobe master. Datapumps which bypass the event00 are clockStrobe slaves. When the event00 packet is transmitted from the send queue it is immediately removed from the queue. When the event00 packet completes its trip around the ringlet and returns to the clockStrobe master, it is stripped and discarded.

When an event00 packet is transmitted on the DataPump's outputs, the clockStrobe pin PCLKSTB is asserted to the node interface logic. PCLKSTB is deasserted when the event00 is received and stripped. The node interface logic can use this signal to enable a timer to measure time around the ringlet.

When an event00 packet is bypassed through a DataPump the PCLKSTB signal is asserted for a duration of approximately 48ns, then deasserted. The through time taken to bypass the packet is also measured by counting SCI clock cycles in the DP_CLKTHRU register described in Section 4.8. Other event packets are treated like event00 packets.

4.6 Bandwidth Allocation and the Low-go Bit

Since SCI nodes are connected in ringlets, multiple transactions may be transmitted concurrently. Since there is no arbitration for access to the ringlet, certain bandwidth allocation protocols have been defined to guarantee bandwidth to all nodes.

Bandwidth allocation is managed by two mechanisms. These are; 1) transmission flow control through the use of a token, or "go" bit, in idle symbols which determine when a node is allowed to transmit, and 2) priority schemes using command.mpr, command.spr, control.tpr, and idle.ipr fields which allow unfair nodes to determine the priority for transmission of unsent packets.

The DataPump uses the idle.lg "low-go" bit for flow control but does not support any priority allocation mechanisms. Since idles are always received in aligned pairs (see Section 4.4.5) the idle.lg bits in idle pairs are essentially or'ed together.

A DataPump can only transmit a packet from its send queue when its bypass FIFO is empty and it can postpend the transmission packet to an idle pair with the low-go bit set. If no idles with low-go set are passed through to the transmitter then the DataPump is disabled from sending packets from the send queue.

The low-go bit in outgoing idles is blocked (set to zero) whenever the DataPump's bypass FIFO is not empty. This prevents a downstream DataPump from transmitting and will eventually free up ringlet bandwidth so the blocked DataPump can empty its bypass FIFO.

While the DataPump is blocking low-go, any idle received with low-go set will set the saved value of low-go which will be transmitted in the first pair of idle symbols after the DataPump is no longer blocked (i.e. bypass FIFO is emptied).

Finally, if a node is not blocked and an idle pair with low-go set is transmitted, the idle pair immediately following will also have their low-gos set. These low-go extensions will prevent a complete loss of low-go bits in a ringlet.

If all low-go bits in all idles are cleared (thus no one is allowed to transmit), the scrubber will detect this and set an error condition.

4.6.1 Allocation Count and Circulation Count

Two flag bits in the idle symbols, idle.ac and idle.cc, keep track of when all producers have had the opportunity to transmit and when an idle symbol has circulated completely around the ringlet. These bits are controlled by the scrubber.

Circulation count is passed by non-scrubber nodes and toggled by the scrubber. When a non-scrubber node is transmitting idles, the value of idle.cc on output is set to the most recently received idle.cc value. In a scrubber node, output idle.cc is the complement of the most recently received idle.cc value. Thus, idle.cc acts as a token which takes roughly the latency of the ringlet to circulate.

The allocation count bit, idle.ac, is similar to idle.cc except it is a token which indicates when all nodes have had an opportunity to transmit. When the idle.ac bit toggles, a time interval has elapsed in which all nodes have had the opportunity to transmit.

The idle.ac bit is passed by a node when its output is not blocked. When its output is blocked (i.e. transmitting from its send queue or emptying bypass FIFO), it must output the idle.ac value saved from the last idle received before transmission began. Therefore, idle.ac cannot change at the output of a blocked node. It can only change after the node has recovered and is enabled for transmission. A non-scrubber node will pass the value of idle.ac which was last received. The scrubber will output the complement of this value. The allocation count and circulation count flags are used to detect error conditions or set time-outs as described in following sections.

4.7 Queue Allocation

Bandwidth allocation protocols guarantee that all nodes get bandwidth to transmit packets. However, if the queues on a consumer node become filled, then new send packets for this node are echoed with a "busy" status and must be re-sent until queue space is available and they are accepted. Queue allocation protocol includes a simple reservation scheme insuring all producer's packets eventually get accepted by consumers.

This reservation mechanism is described in the SCI standard. There are four queue allocation states which the ringlet may be in at any time. These are SERVE_NA, SERVE_A, SERVE_NB, and SERVE_B. Also, send packets and busy echo packets contain a phase field which has values NOTRY, DOTRY, RETRY_A, and RETRY_B.

The DataPump implements this A/B aging protocol. In states SERVE_NA or SERVE_NB, basically all packets are accepted if queue space is available. If any packets are busied, the queue will transition to SERVE_A or SERVE_B.

In SERVE_A and SERVE_B states, the DataPump will only accept packets with phase RETRY_A or RETRY_B respectively. Exiting either SERVE_A or SERVE_B is handled by maintaining counters for phase A and B which accumulate the number of busied packets for retry and decrementing the counter every time a packet is accepted (the count is incremented every time a packet sent with DOTRY phase is returned busied of type A or B). When the count is back to zero, the queue transitions back to SERVE_NA or SERVE_NB.

The busied counter is 4-bits. If the number of busied packets is less than 15 then the DataPump will exit SERVE_A or SERVE_B when all busied packets have been accepted.

If the number of busied packets equals or exceeds 15, exiting SERVE_A or SERVE_B will be accomplished by a time-out on the allocation count counter. The allocation counter increments each time all nodes on the ringlet have had the opportunity to transmit. If no more RETRY_A or RETRY_B packets have been received within 4 allocation intervals, the queue times out and transitions to SERVE_NA or SERVE_NB.

A time-out on the allocation counter when the busied packet counter did not overflow is a ringlet state error and is described in the error handling Section 4.9.

Separate state machines for request and response queues process packet reservations separately to avoid deadlock situations.

For more detailed descriptions of the A/B reservation scheme or the com.phase, com.bsy, or idle.ac fields refer to the SCI standard, Section 3.7.

Queue selection protocol specifies that for a node with multiple request or response send queue entries only one packet at a time may be sent with DOTRY phase for each queue type, request or response. Also, the pro-

ducer should alternate transmission order between request and response so that both queues are serviced equally. For more information on queue selection, see Section 5.3 Send Queue SCI Transmission Order.

4.8 Control and Status Support Registers

SCI follows the CSR (Control and Status Register) architecture as defined in IEEE Std 1212-1991. An SCI node must have the defined registers and behavior as outlined in the standards.

The DataPump does not contain any CSRs but has configuration and status registers modeled after the CSR standard to provide the functionality required to implement full CSR compliance on the node interface logic.

CSR registers are software visible to both the processor elements connected to a node and to remote nodes through the SCI links. CSRs are address mapped into memory address space as defined by the 64-bit fixed address model, which allocates the most significant 256Mbyte space to registers.

Remote access through SCI is provided by read and write request transactions to that address space. The DataPump does not, however, decode requests to CSR address space. It simply queues request packets and sends them up to the node interface logic. The node interface logic is responsible for servicing the CSR requests (both local and remote).

The node interface logic must use the support registers on the DataPump to set state and values in the node CSRs. For example, the DP_STATE register indicates the operational state of the DataPump. If the DataPump has been reset from the SCI link, it will enter the "initializing" state reflected by the DP_STATE resetIinc bit. The logical SCI node's STATE CSR is then the combination of the DataPump state and the rest of the node interface logic state.

The CSR support registers can also be accessed through the Test Access Port scan port. See 9.0 Test Access Port for details.

These registers are initialized by toggling the NRESET pin. A complete description of chip reset is given in Section 4.10 DataPump Reset. A summary of the CSR support registers on the DataPump is given in Table 4.6.

Table 4.6: DataPump CSR Support Registers

Register	*Offset*	*Description*
DP_STATE	000_{16}	The DP_STATE register contains the current status of the DataPump. It also contains the chip revision number.
DP_NODEID	008_{16}	Contains nodeId value and distanceId value from reset initialization.
DP_CLKTHRU	070_{16}	Contains the time interval between arrival and departure of the clockStrobe transaction. Measured in 4ns increments.
DP_ERRLOG	184_{16}	Contains error codes and diagnostic information.
DP_SENDQ_TAG[3:0]	300_{16},304_{16}, 308_{16},$30C_{16}$	Provide read access to the send queue tranId and targetId values for each packet in the queue.
DP_PC_CONFIG0	320_{16}	PPC0 output pin selection/configuration and mask/compare values for performance counters.
DP_PC_CONFIG1	328_{16}	PPC1 output pin selection/configuration.

These registers are detailed in the following sections. Tables for each register indicate the register functionality and use the following code for access restrictions; RO - read only; RW - read or write value to 1 or 0; RC - read or clear value on write. The clear function is NOT a bitwise clear. Just writing the CSR register with any data value will clear the register if it is RC.

4.8.1 DP_STATE (Offset 000_{16})

Table 4.7: DP_STATE Register

Name	Bits	Access	Description
rev_num[0:3]	0:3	RO	Hardwired chip revision number; 0001 for this chip.
reserved	4:7	-	(Test usage only: timeadj[7:4])
stayrun	8	RW	Stay in running state if a fatal link error occurs when set.
reserved	9:11	-	(Test usage only: timeadj[2:0])
insync[0:1]	12:13	RO	Count of the number of valid sync pakets received during initialization state INIT.
not used	15:14	-	
gotodead	16	RW	When asserted forces DataPump to DEAD state.
not used	17	-	
ruup	18	RO	When true indicates SCI input strobe is running.
runlinc	19	RO	When asserted indicates DataPump is in the RUN state.
initlinc	20	RO	When asserted indicates DataPump is in the INIT state.
sngerr	21	RW	Capture first fatal error only (single error; see Section 4.9.)
not used	22	-	
sigrst	23	RW	Used during initialization.
deadlinc	24	RO	When asserted indicates DataPump is in the DEAD state.
resetlinc	25	RO	When asserted indicates DataPump is in the RESET state.
inscrub	26	RO	Indicates this DataPump is the scrubber when asserted.
not used	27:30	-	
dreq	31	RW	Disable requests. DataPump will not accept packets from the NIBus when set.

4.8.2 DP_NODEID (Offset 008_{16})

Table 4.8: DP_NODEID Register

Name	Bits	Access	Description
nodeid[0:15]	0:15	RW	Node ID value for this DataPump. Should be set before normal operation.
not used	16:25	-	
clkthru[0:5]	26:31	RO	Count of SCI clock cycles elapsed while an event00 packet was bypassed through a clockStrobe slave DataPump (see Section 5.1.11 on the PCLKSTB signal)

4.8.3 DP_CLKTHRU (Offset 070_{16})

Table 4.9: DP_CLKTHRU Register

Name	Bits	Access	Description
nodeid[0:15]	0:15	RO	Node ID value for this DataPump, read-only.
not used	16:25	-	
clkthru[0:5]	26:31	RO	Count of SCI clock cycles elapsed while an event00 packet was bypassed through a clockStrobe slave DataPump (see Section 5.1.11 on the PCLKSTB signal)

4.8.4 DP_ERRLOG (Offset 184_{16})

NOTE: A CSR register write to this address clears all register bits.

Table 4.10: DP_ERRLOG Register

Name	Bits	Access	Description
not used	0:2	-	
sqfrz[0:3]	3:6	RC	Send queue slot "freeze" bits. A set bit indicates an error occurred on the packet in that send queue slot and it was "frozen". Slot is freed when bit is cleared. Tag information for each slot is contained in the DP_SENDQ_TAG registers. The correspondence is as follows; sqfrz0 -> DP_SENDQ_TAG0 sqfrz1 -> DP_SENDQ_TAG1 sqfrz2 -> DP_SENDQ_TAG2 sqfrz3 -> DP_SENDQ_TAG3
tcode[0:7]	7:14	RC	NIBus transfer errors - (see Table 4.18) bit 7 (sendQfull) - load attempted to full send Q bit 8 (dupTranId) - send req packet had a duplicate tranId bit 9 (sizeErr) - send packet size error bit 10 (NIregPar) - NIBus parity error on register read/write bit 11 (NIsendqPar) - NIBus parity error on send Q load bit 12 - not used bit 13 (rcvQempty) - read attempted from empty receive Q bit 14 (regAddrErr) - register access to bad address
notruup	15	RC	Lost input SCI strobe signal.
flgerr	16	RC	Received packet had a flag error
not used	17	-	
strperr[0:6]	18:24	RC	SCI input linc stripper errors - bit 18 (badIdle) - idle symbol had a parity error bit 19 (badThruCrc) - bad CRC in bypassed packet bit 20 (badStrpCrc) - bad CRC in stripped packet bit 21 (strpTooLong) - stripped packet greater than 48 symbols bit 22 (tossClkStb) - received extra clockStrobe packet bit 23 (reqAcTmo) - request Q reservation early ac timeout bit 24 (rspAcTmo) - response Q reservation early ac timeout
fatalerr[0:6]	25:31	RC	Fatal linc errors - (except for tooLong which is NOT fatal) bit 25 (noInSync) - elastic buffer lost synchronization bit 26 (tooLong) - bypassed packet greater than 48 symbols bit 27 (scrbLgTmr) - scrubber detected no low-go bits in ringlet bit 28 (reqRsvErr) - bad retry phase on request Q bit 29 (rspRsvErr) - bad retry phase on response Q bit 30 (acFail) - ac toggled more than once while output blocked bit 31 (echoUnkn) - stripped echo doesn't match any in send Q

4.8.5 DP_SENDQ_TAG[0:3]

Table 4.11: DP_SENDQ_TAG3 Register Offset 300_{16} (Request Queue Slot 0)

Name	*Bits*	*Access*	*Description*
not used	0	-	
reserved	1:4	RO	(Test usage only: rqvld_s[3:0])
reserved	5	RO	(Test usage only: sqvld_s0)
echoNo	6	RO	target node for packet doesn't reply, packet scrubbed
sndQpar	7	RO	parity error occurred on packet transmission from send Q
sndQto	8	RO	cc timeout on packet, no echo received in 4 cc times
validbit	9	RO	valid bit for send Q slot 3
not used	10:25	-	
tranid[0:5]	26:31	RO	transaction ID in send Q slot 3 (request slot 0)

Table 4.12: DP_SENDQ_TAG2 Register Offset 304_{16} (Request Queue Slot 1)

Name	*Bits*	*Access*	*Description*
not used	0	-	
reserved	1:4	RO	(Test usage only: rqvld_s[7:4])
reserved	5	RO	(Test usage only: sqvld_s1)
echoNo	6	RO	target node for packet doesn't reply, packet scrubbed
sndQpar	7	RO	parity error occurred on packet transmission from send Q
sndQto	8	RO	cc timeout on packet, no echo received in 4 cc times
validbit	9	RO	valid bit for send Q slot 2
not used	10:25	-	
tranid[0:5]	26:31	RO	transaction ID in send Q slot 2 (request slot 1)

Table 4.13: DP_SENDQ_TAG1 Register Offset 308_{16} (Response Queue Slot 0)

Name	*Bits*	*Access*	*Description*
not used	0:5	-	
reserved	1:4	RO	(Test usage only: rqvld_sf[3:0])
reserved	5	RO	(Test usage only: sqvld_s2)
echoNo	6	RO	target node for packet doesn't reply, packet scrubbed
sndQpar	7	RO	parity error occurred on packet transmission from send Q
sndQto	8	RO	cc timeout on packet, no echo received in 4 cc times
validbit	9	RO	valid bit for send Q slot 1
not used	10:25	-	
tranid[0:5]	26:31	RO	transaction ID in send Q slot 1 (response slot 0)

Table 4.14: DP_SENDQ_TAG0 Register Offset $30C_{16}$ (Response Queue Slot 1)

Name	*Bits*	*Access*	*Description*
not used	0:5	-	
reserved	1:4	RO	(Test usage only: rqvld_f[7:4])
reserved	5	RO	(Test usage only: sqvld_s3)
echoNo	6	RO	target node for packet doesn't reply, packet scrubbed
sndQpar	7	RO	parity error occurred on packet transmission from send Q
sndQto	8	RO	cc timeout on packet, no echo received in 4 cc times
validbit	9	RO	valid bit for send Q slot 0
not used	10:25	-	
tranid[0:5]	26:31	RO	transaction ID in send Q slot 0 (response slot 1)

4.8.6 DP_PC_CONFIG0 (offset 320_{16})

The detailed function of these register bits is described in Section 8.0 Performance Counters.

Table 4.15: DP_PC_CONFIG0 Register

Name	*Bits*	*Access*	*Description*
pc0mask[0:4]	0:4	RW	Selector for the PPC0 output pin. Assert only one at a time; bit 0 (pktSlot0Rs) - PPC0 toggles when a packet is transmitted from the send-response Q slot 0 and the packet matches the command mask/ compare value. bit 1 (pktSlot0Rq) -PPC0 toggles when a packet is transmitted from the send-request Q slot 0 and the packet matches the comand mask/compare value. bit 2 (pktRcv) - PPC0 toggles when a packet is received and targeted to this node. bit 3 (pktByp) - PPC0 toggles when a packet is bypassed. bit 4 (pktSent) - PPC0 toggles when a packet is sent.
rcvVldMask	5	RW	Used to qualify the PPC1 output pin RcvPkt when a received packet is actually stripped and the packet is entered into the receive Q (as opposed to tossed for Q reservations or other reasons).
extMask[0:4]	6:10	RW	Masks the command symbol bits 4,5,7,8,9 from the extended comparison for PPC1 matching. These bits correspond to the command phase, ech, bsy, and res bits as follows; bit 6 (extMask0) - com.phase0 bit 7 (extMask1) - com.phase1 bit 8 (extMask2) - com.ech bit 9 (extMask3) - com.bsy (for echo packets) bit 10 (extMask4) - com.res (for echo packets)
extCmp[0:4]	11:15	RW	Compare values for command symbol bits 4,5,7,8,9 as described above.
cmdSns	16	RW	Command sense bit which, when asserted, inverts the cmd field match signal to allow qualifying PPC1 counters on mis-match instead of match.
cmdMask[0:6]	17:23	RW	Masks the command symbol bits 9:15 from the command comparison for PPC1 matching. These bits correspond to the com.cmd field of send packets (not echos).
cmdCmp[0:6]	24:30	RW	Comparison value for the com.cmd bits.
refMask	31		When asserted forces the PPC0 pktRcv signal to be qualified with the ext mask/compare value. If the ext mask/compare is set to match echos, then refMask is used to cause pktRcv to count only echo packets or only send packets.

4.8.7 DP_PC_CONFIG1 (Offset 328_{16})

DP_PC_CONFIG1 is the selector for driving the PPC1 pin. The following table lists the function of the PPC1 pin when that bit of DP_PC_CONFIG1 is asserted. Only one bit of this register should be set at a time. Setting more than one bit will produce undefined results. See Section 8.0 Performance Counters for a more complete description of these bits.

Table 4.16: DP_PC_CONFIG1 Register

Name	*Bits*	*Access*	*Description*
not used	0:18	-	
rsRsvPhs	19	RW	PPC1 asserted while the receive-response reservation state machine state phase matches ext bits 0:1 (extMask[0:4] set to 11000 and extCmp[0:1] set to the desired phase)
rqRsvPhs	20	RW	PPC1 asserted while the receive-request reservation state machine state phase matches ext bits 0:1
rsSlot0Tm	21	RW	PPC1 asserted while a packet matching the cmd mask/compare is entered in send-response queue slot 0.
rqSlot0Tm	22	RW	PPC1 asserted while a packet matching the cmd mask/compare is entered in send-request queue slot 0.
outputCc	23	RW	PPC1 toggles each time the idle.cc bit changes at the SCI output link.
outputAc	24	RW	PPC1 toggles each time the idle.ac bit changes at the SCI output link.
rRspDepth	25	RW	PPC1 toggles at a rate proportional to the number of q entries in the receive-response queue (see Section 8 Performance Counters)
rReqDepth	26	RW	PPC1 toggles at a rate proportional to the number of q entries in the receive-request queue (see Section 8 Performance Counters)
sRspDepth	27	RW	PPC1 toggles at a rate proportional to the number of q entries in the send-response queue (see Section 8 Performance Counters)
sReqDepth	28	RW	PPC1 toggles at a rate proportional to the number of q entries in the send-response queue (see Section 8 Performance Counters)
RcvPkt	29	RW	PPC1 toggles each time a packet matching both ext and cmd mask/ compare values is received and targeted to this node.
BypPkt	30	RW	PPC1 toggles each time a packet matching both ext and cmd mask/ compare values is bypassed through this node.
SndPkt	31	RW	PPC1 toggles each time a packet matching both ext and cmd mask/ compare values is transmitted by this node.

4.9 Error Handling

The DataPump checks and maintains an error log which records various error types. Errors fall into two categories; 1) SCI link related errors logged in the DP_ERRLOG fields notruup, flgerr, and strperr[0:6]; and 2) NIBus (node interface bus) transfer errors. SCI link related errors are logged in the DP_ERRLOG fields notruup, flgerr, strperr[0:6], and fatalerr[0:6]. NIBus errors are logged in the DP_ERRLOG.tcode[0:7] field. Multiple errors can occur and will all be logged unless the DP_STATE.sngerr bit is set.

4.9.1 SCI Link Related Errors

Errors in the SCI link occur due to protocol or ringlet state errors. Some of these are fatal and cause the link to enter the "dead" state. Fatal errors are listed in Table 4.17. Going to "dead" on fatal errors can be prevented by setting the DP_STATE.stayrun bit. Others are not fatal and will be logged while the SCI link remains in the "running" state.

Any SCI link error will assert the node interface logic interrupt pin NINTRNI. It remains asserted until the DP_ERRLOG register is cleared by a CSR write.

Table 4.17: Fatal SCI Link Errors

Error	*Bit*	*Description*
notruup	15	Lost input SCI strobe signal.
echoUnkn	31	Received echo with no corresponding send packet in send queue.
acFail	30	Allocation count bit flipped more than once while node was blocking.
rspRsvErr	29	Retry packet received with wrong reservation phase for response queue.
reqRsvErr	28	Retry packet received with wrong reservation phase for request queue.
scrbLgTmr	27	No idle.lg bits set in ringlet detected by the scrubber.
noInSync	25	Lost input sync (elastic buffer).

Non-fatal SCI link related errors include errors detected at the input link and send queue related errors. Non-fatal input link errors are listed in Table 4.18. Multiple errors can occur and will be logged unless the DP_STATE.sngerr bit is set.

Table 4.18: Non-fatal Input Link Errors

Error	*Bit*	*Description*
flgerr	16	Received packet was not properly framed.
tooLong	26	Bypassed packet greater than 48 symbols. Packet is truncated to 48 and correctly framed. Outgoing CRC is stomped.
badIdle	18	Received idle with bad parity. Replaced with last good idle symbol.
badThruCrc	19	Bypassed packet had bad CRC. Outgoing CRC is stomped.
badStrpCrc	20	Stripped packet for receive queue had bad CRC. Packet tossed and echo CRC stomped.
strpTooLong	21	Stripped packet for receive queue greater than 48 symbols. Was tossed and echo CRC stomped.
tossClkStb	22	Received clockStrobe while still bypassing a clockStrobe. Packet tossed.
rspAcTmo	23	Allocation counter timed out (acTmr=4) on response Q reservation before all outstanding reservations completed.
reqAcTmo	24	Allocation counter timed out (acTmr=4) on request Q reservation before all outstanding reservations completed.

The send queue releated errors are of three types listed in Table 4.19. These errors are non-fatal and are indicated by bits in the appropriate DP_SENDQ_TAG registers listed in 4.8.5. Also given in the tag register is the valid bit for the slot indicating whether the packet is actually valid, plus the packet's tranId value allowing identification of the packet with the error.

If a send queue related error occurs on a packet in a queue slot, the packet will be held ("frozen") in the slot so that its DP_SENDQ_TAG register can be examined. This "freeze" indication is provided in the DP_ERRLOG.sqfrz[0:3] field. These send queue errors also assert the NINTRNI pin.

Table 4.19: Send Q Tag Error Flags

SendQ error	*Bit*	*Description*
sndQto	8	Send queue packet time out. Occurs when packet has waited 4 cc counts without receiving a matching echo.
sndQpar	7	Send queue parity error. Upon transmission from send queue if a parity error is detected on the packet data.
echoNo	6	Echo NONE status returned. If packet receives echo with NONE status indicating targetId addressed no node.

These errors are or'ed together to assert the NERRNI signal pin. This pin will remain asserted until all DP_ERRLOG tcode bits are cleared by a register write.

Transfer errors are summarized in Table 4.20.

Table 4.20: NI Transfer Errors

Error	*Bit*	*Description*
sendQfull	7	Tried to transfer to full send queue.
dupTranId	8	Send req packet has duplicate tranId to packet already in the req queue.
sizeErr	9	Node interface transfer length not multiple of 8 symbols or greater than max 48 symbols.
NIregPar	10	Parity error detected on register write transfer to DataPump.
NIsendqPar	11	Parity error detected on send queue transfer to DataPump.
rcvQempty	13	Tried to transfer from empty receive queue.
regAddrErr	14	Register offset address supplied from node interface on register read or write doesn't match any register.

4.10 DataPump Reset and Initialization

SCI auto-initialization as described in the IEEE SCI specification is not supported on this DataPump chip. Instead, a greatly simplified initialization scheme has been implemented which requires some software intelligence to start the linc. The DataPump sequences through four valid chip states described below:

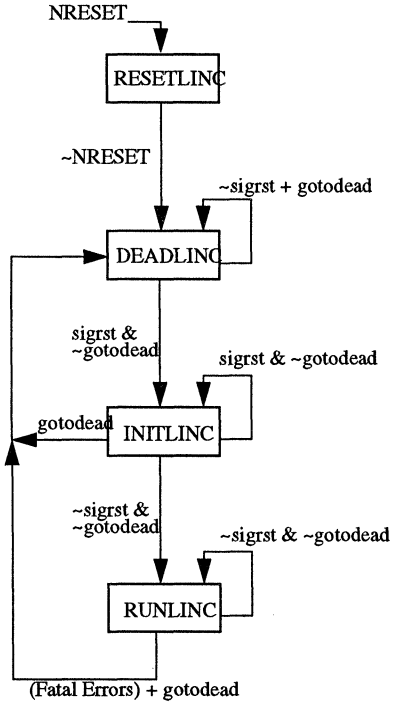
RESETLINC - A hard reset of all registers in the DataPump is performed (NRESET asserted).

DEADLINC - Internal chip clocks are running and the DataPump is waiting for the upstream strobe to start. In this state, the state-machines in the linc portion of the chip is frozen. Valid idles are sent from the linc.

INITLINC - In this state, the upstream strobe has been received, and we are waiting for upstream synchronization. The bypass FIFO has now been re-synchronized but is locked so that no bypass traffic is let through. The output unit sends valid sync and idle packets to the downstream linc. Also, valid and freeze bits are cleared to free up used queue slots (i.e. for a warm restart).

RUNLINC - DataPump initialization sequence complete, ready for normal chip operation. The initialization flow Diagram for the VSC7201A is shown in fig. 4.10. The "~" used in the figure indicates the false value of the signal. The "&" means the logical AND and the "+" means the logical OR of the listed signals. The only signals required to cycle through initialization are the NRESET pin and the DP_STATE register bits sigrst and gotodead. However, the following sequence is recommended for reliable synchronization.

Figure 4.10 : Initialization Flow Diagram



1. The NRESET pin should be asserted for at least 8 NICLK cycles then deasserted. The DataPump then proceeds to DEADLINC.
2. The DP_STATE.ruup bit is monitored which, when set, indicates that upstream clock is running. When ruup is detected, DP_STATE.sigrst is set. The DataPump state then advances from DEADLINC to INITLINC. Note that DP_STATE.gotodead was cleared by NRESET and should not be set or else the DataPump will remain in DEADLINC.
3. In the INITLINC state, software should monitor the DP_STATE.insync value which indicates that the upstream block is running and has detected a certain number of sync packets. Once DP_STATE.insync reaches value "11" (it is a 2 bit field and indicates three sync packets received), then DP_STATE.sigrst is de-asserted and the DataPump enters the RUNLINC state.

Setting of the NodeID values and scrubber selection should also be done during initialization. The DP_NODEID value can be set anytime after RESETLINC but MUST be done for all DataPumps in the ringlet before any packets are loaded into any send queues for transmission.

The ringlet should also have one and ONLY one scrubber selected (by asserting the NSCRUB pin) before entering the RUNLINC state.

The DP_STATE register contains many useful signals related to chip state, initialization, and error control (stayrun and gotodead). See 4.8.1 for a description of this register.

5.0 Node Interface Bus (NIBus)

The DataPump communicates with the node controller via a bidirectional GTL interface called the NIBus. The DataPump informs the node controller when receive queues contain data or when send queues have available slots for transmission. The node controller can initiate various commands with the DataPump to read and write packets across this interface.

Signal names are prepended with an N or P indicating negative true or positive true signals.

5.1 Interface Protocol and Signal Description

The NIBus is a synchronous 64-bit data bus plus 8 bits of byte parity plus control signals. All signals are sampled or driven on the rising edge of CLKNI.

The bus master is assumed to be the node interface logic. The DataPump chip is a slave on this bus controlled by asserting chip select, NDPSEL, and a 3-bit command on the PCMND pins.

PCMND selected transfers of data can be from 2 to 12 sequential 64-bit data transfers for SCI packets and register reads and writes.

5.1.1 PDATA[0:63], PPARITY[0:7]

PDATA is bidirectional data bus for use in transferring data to and from the DataPump. PPARITY indicates byte parity on PDATA. Good parity is odd (all ones give parity of one).

PDATA and PPARITY are floated at the end of the transfer or one cycle after NDPSEL goes false and remain floated until NDPSEL is asserted.

PDATA[0:63] are also floated by the DataPump starting one cycle after PCMND is sampled, when it responds to a transfer command from the node interface to the DataPump (sendReq, sendResp, and regWrite). PDATA[32:63] are floated similarly when the DataPump responds to a regRead transfer.

5.1.2 NDPSEL- Datapump Chip Select

The NDPSEL input is used to chip select the DataPump and allow it to execute transfers and drive the data and control signals. The cycle in which NDPSEL is asserted, the DataPump will sample its PCMND inputs and begin executing commands.

If NDPSEL goes false during any clock cycle of a DataPump command, the DataPump will abort the command cleanly without an error condition. This is an acceptable protocol for aborting DataPump command sequences.

One cycle after NDPSEL goes false, all outputs will be floated except PRCVREQ, PRCVRSP, PSNDREQ, PSNDRSP, PCLKSTB, NERRNI, and NINTRNI.

5.1.3 PCMND[0:2] - Transfer Command

The PCMND inputs select the DataPump transfer command as listed in Table 5.1. The PCMND value is sampled in the cycle NDPSEL is asserted.

If NDPSEL remains asserted after a transfer has completed, the DataPump will wait until NDPSEL is toggled before sampling a new PCMND. Therefore, NDPSEL acts as a strobe for latching a new PCMND value

Table 5.1: .PCMND Commands

Command	*PCMND [0:2]*	*Description*
rcvReq	000	Transfer from the receive-request queue (5-15 cycles).
rcvResp	001	Transfer from the receive-response queue (5-15 cycles).
regRead	010	Read contents of target register (4 cycles).
reserved	011	Reserved for future use.
sendReq	100	Transfer to the send-request queue (5-15 cycles).
sendResp	101	Transfer to the send-response queue (5-15 cycles).
regWrite	110	Write contents of target CSR (4 clock cycles, 64 bits max.).
reserved	111	Reserved for future use.

5.1.4 NNIACK - Node Interface Acknowledge

NNIACK is an input used to indicate valid end of transfer on send, receive, and register transfers.

Transfers from the node interface to the DataPump are acknowledged valid by asserting NNIACK simultaneously with the last data transfer cycle.

The packet size is determined by the DataPump based on receiving NNIACK with last data. The NNIRDY flow control can be used to delay NNIACK from the end of data if necessary.

Aborting a transfer from the node interface to the DataPump should be done with NDPSEL, not NNIACK.

Transfers from the DataPump to the node interface are acknowledged received as valid by asserting NNIACK one cycle after the last data transfer. If this acknowledge is provided, the DataPump will remove the packet from its queue after receiving NNIACK.

NNIACK false one cycle after the last data transfer indicates invalid transfer and abort without error condition. In this case, the DataPump will not remove the transferred packet from the receive queue.

5.1.5 NDPACK - DataPump Acknowledge

NDPACK is an output used to indicate valid end of transfer by the DataPump on send, receive, and register transfers.

Transfers from the DataPump to the Node Interface are acknowledged valid by asserting NDPACK in the same cycle as the last data transfer.

NDPACK false in this case indicates an error condition and the transfer should be disregarded. If the packet had a parity error, it will be discarded after the last cycle of the transfer (based on packet size). If NDPSEL was deasserted aborting the transfer before the end, the packet will not be removed from the queue regardless of parity error.

Data transfer length must be determined by the node interface by saving the "size" value from the header field in the packet and counting cycles. See Section 5.3.1 Condensed Request/Response Packets for more on the "size" value.

Transfers to the DataPump from the node interface are acknowledged valid by asserting NDPACK two cycles after the last data transfer cycle. The extra cycle is necessary for parity checking.

NDPACK false in this case indicates an error condition and that the transferred packet cannot be accepted and was not queued. See Section 4.9 for interface error conditions.

NDPACK is floated at the end of the transfer or starting one cycle after NDPSEL goes false and remains floated until NDPSEL is asserted.

5.1.6 NNIRDY - Node Interface Flow Control

NNIRDY is an input to the DataPump. Flow control is provided through NNIRDY.

NNIRDY applies to data transfers and NNIACK acknowledge of transfers in either direction. A false NNIRDY will cause the DataPump to hold its state in the next cycle. It will continue to hold until NNIRDY goes true.

The DataPump also qualifies PCMND sampling with NNIRDY.

5.1.7 PRCVREQ, PRCVRSP - Rcv Queue Flags

These receive queue flags are outputs from the DataPump indicating the presence of a received packet from the SCI link. These queue flags will not be asserted until the entire packet has been received and the CRC has checked without error.

The flags go false (queue empty) two cycles after receiving a receive queue transfer command if the packet being transferred is the last in the queue.

If the transfer doesn't complete (aborted or error detected) and the packet is not freed from the receive queue, the queue flag will be asserted again at the end of the transfer.

These receive flags are always driven and do not float when the DataPump is deselected.

5.1.8 PSNDREQ, PSNDRSP - Send Queue Flags

The send queue flags are outputs from the DataPump indicating at least one available queue slot in each queue type (request or response) when asserted true.

They will go false (indicating queue full) two cycles after receiving a send queue transfer command and if the queue will fill up as a result of the transfer. If the transfer doesn't complete and the packet isn't queued, the queue flag will go true again at the end of the transfer.

They will go true indicating that a queue slot has freed up only after receiving a normal echo packet from the target SCI node of the send packet which was freed from the queue.

The send queue flags are always driven and do not float when the DataPump is deselected.

5.1.9 NINTRNI - Interrupt Node Interface

NINTRNI is an output of the DataPump and is asserted whenever an error occurs synchronous to the SCI link. These errors are logged in the DP_ERRLOG register not including the tcode error field. NINTRNI remains asserted until the DP_ERRLOG is cleared.

NINTRNI is always driven and is not floated when the DataPump is deselected.

5.1.10 NERRNI - NIBus Error Flag

NERRNI is an output of the DataPump which is asserted whenever an NIBus transfer error occurs. These errors are listed in Section 4.9.

NERRNI remains asserted until the DP_ERRLOG tcode field is cleared.

5.1.11 PCLKSTB - Clock Strobe

PCLKSTB is an output of the DataPump and is asserted in response to an event00 packet and whether the DataPump is the clockStrobe master or slave.

The DataPump is the clockStrobe master when the event00 packet is loaded into its send request queue for transmission. This packet should be targeted to the clock strobe master's DataPump targetId address so the event00 makes a complete trip around the ringlet and is stripped and tossed by the clockStrobe master.

Other DataPumps in the ringlet which pass the event00 through are clockStrobe slaves.

The clockStrobe master will assert PCLKSTB when the event00 is transmitted on its output link and will deassert PCLKSTB when the packet is stripped at its input link.

The clockStrobe slave will assert PCLKSTB for 13 CLKNI cycles when it receives and bypasses the event00 packet. The slave will also start the DP_CLKTHRU register to count 4ns SCI clock cycles when the event00 is received and will stop the counter when the event00 is transmitted on its output link.

PCLKSTB is always driven and is not floated when the DataPump is deselected.

5.1.12 NRESET

NRESET is an input to the DataPump. Reset initialization of the DataPump occurs when the NRESET pin is driven from low to high. This rising edge transition must be synchronous to the NIBus clock, CLKNI. NRESET must be asserted for at least 8 CLKNI cycles.

For a description of reset initialization see sections 4.10 DataPump Reset and 5.7 NIBus Reset and State Sync to the SCI Link.

5.1.13 NSYNCRQ - Send Sync Packet Request

The NSYNCRQ pin is used to cause the DataPump to transmit a SYNC packet on its output. A SYNC packet will be scheduled for transmission if a one to zero transition is registered on the NSYNCRQ pin. Additional SYNC packets will only be scheduled after the first is transmitted and if, after that transmission, another one to zero transition is registered on the NSYNCRQ pin.

Therefore, NSYNCRQ is intended to be asserted on the order of milliseconds in periodicity. Since the DataPump does not implement any pin-to-pin deskewing, no SYNC packets are required periodically and no NSYNCRQ assertions are required.

5.1.14 NSCRUB - Scrubber Selection

The NSCRUB pin is used to select the DataPump as the scrubber in an SCI ringlet. For a description of scrubber selection and initialization see Section 4.10.

For information on scrubber operation see the SCI standard Section 3.9.2 Scrubber maintenance.

5.1.15 PPC[0,1] - Performance Counters

The PPC output pins provide performance counter signals for monitoring internal events in the DataPump. See Section 8.0 Performance Counters for details.

These outputs are synchronous to the internal 250 MHz SCI clock (however, maximum toggle frequency is 66MHz). They are not synchronized in the DataPump to the NIBus clock, CLKNI.

5.1.16 CLKNI - Node Interface Clock

CLKNI is the interface clock supplied by the node interface logic. All NIBus signals are synchronous with this clock.

5.1.17 CLKHI, PCKHSEL, PCLK250, PCKHMPY[0:1], SCI Link Clock and Control

CLKHI (and NCLKHI) is the master differential clock input for generating the internal 250Mhz SCI clock. It is not required to be phase or frequency related to the node interface clock, CLKNI.

The DataPump has an onboard PLL for frequency multiplication to generate 250MHz. The CLKHI reference frequency for the PLL is 100MHz.

The internal SCI clock is intended to be 250MHz but can be programmed to different values using the PCKHSEL, PCLK250, and PCKHMPY[0:1] inputs for debug and diagnostic purposes. The values higher than 250MHz are not supported.

PCKHSEL is a PLL bypass control input. When asserted the PLL is bypassed and the internal SCI clock is connected directly to the CLKHI input. Any frequency up to 250MHz can be provided in bypass mode.

PCLK250 and PCKHMPY[0:1] provide divisions from the PLL generated 500MHz value. The divide options and available internal SCI clock rates are given in Table 5.2. The values higher than 250MHz are documented for completeness but are not supported.

Table 5.2: SCI Clock Values

PCLK250	PCKHMPY [0:1]	Divide Value	SCI clk (MHz)
1	10	1	500
1	00	2	250
1	01	4	125

5.2 Transfer Packet Formats

The packet formats for transfers between the DataPump and node interface differ slightly from the sequential SCI packet format mainly for ease of data alignment to the 64-bit interface. These formats define the sequence of transfer data pertaining to a particular PCMND request from the node interface logic.

5.2.1 Condensed Request/Response Packets

There are four condensed transfer packet formats corresponding to the PCMND[0:2] transfer command requests- rcvReq, rcvResp, sendReq, sendResp. These condensed packet formats are shown in figures 5.2 - 5.5.

Send Queue transfer packets are always transferred from the node interface logic to the DataPump sequentially from header (octlet 0, figs. 5.2, 5.4) to last octlet. Receive-request queue packet transfers from the DataPump to the node interface logic are also always sequential from header to tail.

The header information has been condensed to the lower 48-bits of the PDATA bus so that if the node interface logic is split into separate controller and datapath elements the controller need only connect to those 48-bits.

In both send packets, only the targetId of the destination node is required since the sourceId is provided by the DataPump and cannot be changed.

In the receive packets, the targetId is provided in the most significant 16-bits as a matter of completeness, but this value will always be the nodeId of the DataPump.

The control symbol contains the fields tranId, tpr, trc, todExp, and todMant. Only the tranId value is really required and used by the DataPump. The trace bit, trc, tpr, time of death count, todExp and todMant, are provided for completeness and are passed but not used by the DataPump.

Finally, the packet size, "size", in pairs of octlets (16-bytes) is given in the header of the receive packets to allow the node interface to determine packet length for the transfer.

This size value is not required on the send side since the DataPump computes packet length based on when the node interface finishes the send queue transfer with NNIACK asserted.

5.2.2 Register Read and Write Formats

Registers on the DataPump are accessed using register read and write CMND transfer commands.

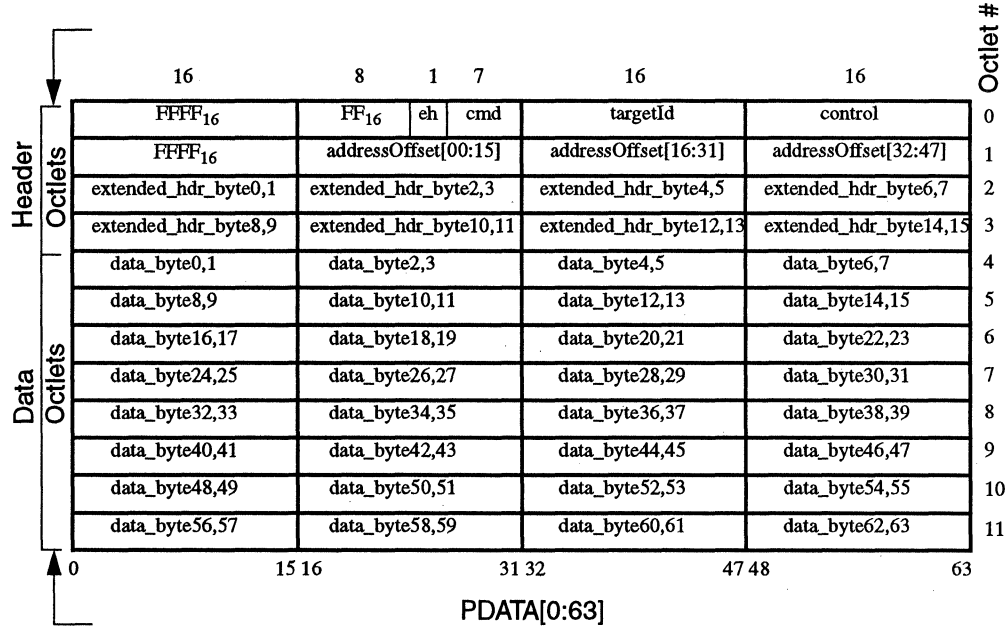
On regRead commands, the most-significant 32-bits of the data bus, PDATA[0:31], are driven by the DataPump with the contents of the register specified by the 12-bit register address offset supplied on PDATA[36:47]. In this case, the DataPump floats its PDATA[32:63] pins to allow the node interface logic to drive register address offset on PDATA[36:47]. Of course PDATA[32:35], PDATA[48:63], and PPARITY[6:7] must be driven to ones by the node interface logic to give correct parity.

On regWrite commands, PDATA[0:31] specify the write data and PDATA[36:47] specify the register address offset. Again PDATA[32:35], PDATA[48:63], and PPARITY[6:7] must be driven to ones by the node interface logic to give correct parity.

The effects of the write vary depending on the register. See Section 4.8 Control and Status Support Registers.

The data transfer formats for register commands are summarized in Figure 5.6.

Figure 5.2 : Send-Request Condensed Transfer Packet Format



Field Descriptions:

targetId - target node ID;

eh - extended header flag from control symbol;
cmd - command field from control symbol;

control - control symbol, tranId (required), tpr, trc, todExp, todMant (all optional);

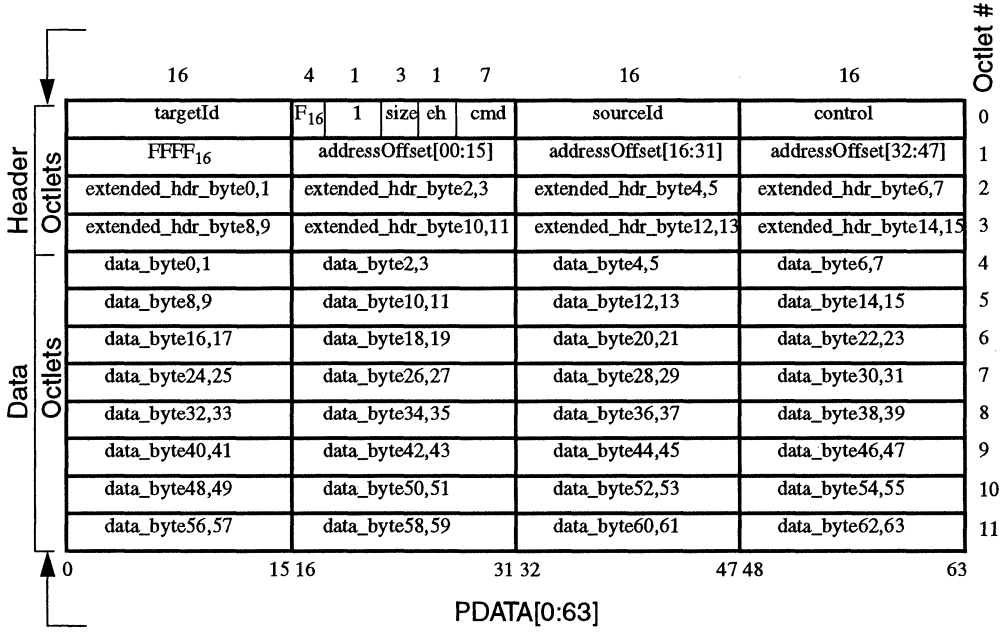
addressOffset[00:47] - 48-bit address;

extended_hdr - either 0 or 16 bytes depending on value of eh flag bit

data_byte0-63 - data packet either 0, 16, 32, 48, or 64 bytes

Fields set to ones (e.g. $FFFF_{16}$) are specified to give known parity. These fields are reserved.

Figure 5.3 : Receive Request Condensed Transfer Packet Format



Field Descriptions:

targetId - target node ID, i.e. this node;

size - size of complete packet in pairs of octlets, from 1 to 6;
eh - extended header flag from control symbol;
cmd - command field from control symbol;
sourceId - node ID of producer of this packet;
control - control symbol, tranId (required), tpr, trc, todExp, todMant (all optional);

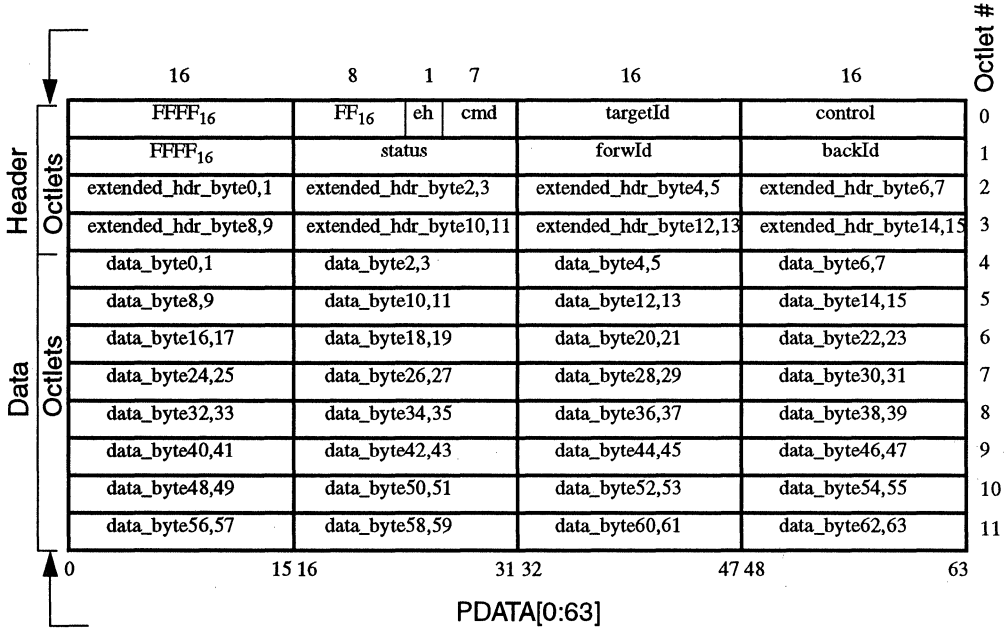
addressOffset[00:47] - 48-bit address;

extended_hdr - either 0 or 16 bytes depending on value of eh flag bit

data_byte0-63 - data packet either 0, 16, 32, 48, or 64 bytes

Fields set to ones (e.g. $FFFF_{16}$) are specified to give known parity. These fields are reserved.

Figure 5.4 : Send-Response Condensed Transfer Packet Format



Field Descriptions:

targetId - target node ID;

eh - extended header flag from control symbol;
cmd - command field from control symbol;

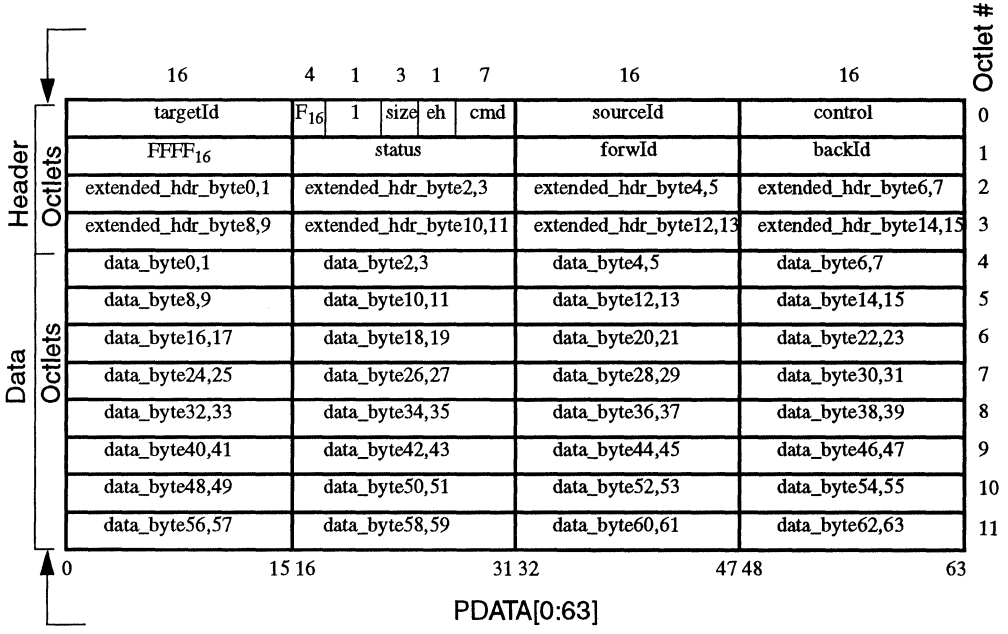
control - control symbol, tranId (required), tpr, trc, todExp, todMant (all optional);
status - response packet status;
forwId, backId - for cache coherency control; transmitted but not used by DataPump

extended_hdr - either 0 or 16 bytes depending on value of eh flag bit

data_byte0-63 - data packet either 0, 16, 32, 48, or 64 bytes

Fields set to ones (e.g. $FFFF_{16}$) are specified to give known parity. These fields are reserved.

Figure 5.5 : Receive-Response Condensed Transfer Packet Format



Field Descriptions:

targetId - target node ID, i.e. this node;

size - size of complete packet in pairs of octlets, from 1 to 6;
eh - extended header flag from control symbol;
cmd - command field from control symbol;
sourceId - node ID of producer of this packet;
control - control symbol, tranId (required), tpr, trc, todExp, todMant (all optional);
status - response packet status;
forwId, backId - for cache coherency control; transmitted but not used by DataPump

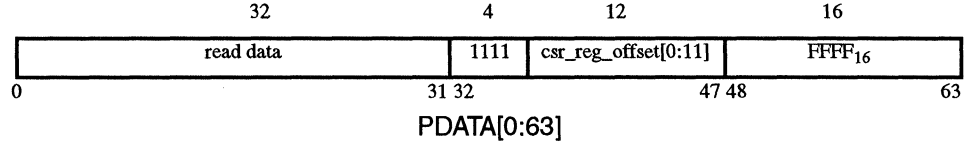
extended_hdr - either 0 or 16 bytes depending on value of eh flag bit

data_byte0-63 - data packet either 0, 16, or 64 bytes

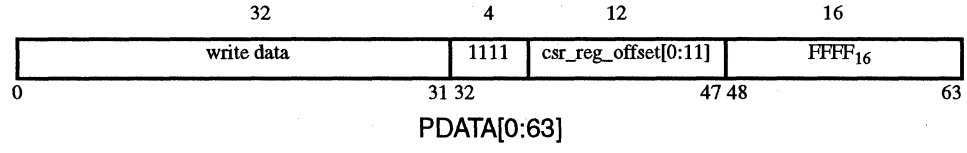
Fields set to ones (e.g. $FFFF_{16}$) are specified to give known parity. These fields are reserved.

Figure 5.6 : CSR Transfer Formats

Register Address Transfer Format:



Register Read/Write Transfer Format:



csr_reg_offset[0:11]:

meaning: Register offset address driven from the node interface logic on both register reads and writes.

read data:

meaning: Register read data driven by DataPump.

write data:

meaning: Register write data driven by node interface logic.

5.2.3 32-Byte Line Packet Support

SCI provides the capability for sending a 32-byte payload in a 64-byte packet. This does not mean that the 64-byte packet contains a first 32-bytes which is meaningful and another 32-bytes of padding out to 64-bytes.

The payload of a 64-byte command can in fact be any multiple of 16-bytes and still be SCI compliant. The DataPump supports these payload sizes.

To send 32-byte packets (can be any of the coherent or non-coherent commands) the node interface logic simply loads the packet into the send queue and indicates the end of the data transfer with the NNIACK signal. The DataPump will check for legal payload size (0, 16, 32, 48, or 64 bytes) and send the packet normally.

To receive 32-byte packets, the node interface logic unloads the receive queue and determines data length by looking at the "size" field in the first 64-bit transfer.

If 32-byte lines are used, one of the addressOffset bits should be allocated to select one of two 32-byte lines within a 64-byte data size.

5.3 Send Queue SCI Transmission Order

Once either of the send queues has been loaded with a packet, the DataPump is responsible for getting the packet sent out on the SCI link. Each request and response queue has up to two packet entries, which may be unsent. The queues may also contain packets which have been sent but have not been received as acknowledged by an echo with DONE or NONE (i.e. non-busy) returned phase.

To determine the order of transmission of the queue entries, the DataPump keeps three state bits and an age bit for each request and response queue entry. Table 5.3 summarizes these bits.

The highest transmission priority for unsent packets is the one with tryReserve set. The selection of request or response queues is done in alternating order so that both queues are serviced equally. The next priority of ordering for transmission is based on packetAge. For more information on send packet transmissions and flow control see 4.6 Bandwidth Allocation and 4.7 Queue Allocation.

Table 5.3: Send Queue State Tags

Tag Bit	*Description*
ready	After a packet is entered into the send queue by the node interface logic, it is ready for transmission with phase NOTRY.
tryReserve	One packet from each queue is allowed to be transmitted with DOTRY phase in order to reserve receive queue space. If no packet has tryReserve set, the oldest packet based on packetAge will get tryReserve set. TryReserve remains set on a packet until the packet is removed from the queue.
packetAge	Each packet entry will have an age which gets updated whenever packets are removed from the queue or when new packets are loaded by the node interface logic.
check	This flag indicates packet has been sent and is waiting for echo.
freeze	This flag indicates the packet has experienced either a parity error on transmission, has timed out waiting for echo, or received echo with NONE status. See 4.9.

5.4 Receive Queue Transfer Order

Data transfers from the DataPump receive queues to the node controller can start if one of the queue flags is true (PRCVREQ, PRCVRSP), after the node controller has selected the DataPump for receive packet transfer.

If more than one packet is in the queues, the order which the DataPump will unload them in is in the order they were received on the SCI link for that packet type, request or response.

Since the order packets are received from SCI nodes cannot be guaranteed, the node interface logic must check the tranId of the packet to determine which outstanding request it is for.

5.5 NIBus State Machine

The basic flow diagram for the NIBus is shown in Figure 5.7. This is an approximation to the actual logic and should be used for general understanding only. Refer to the bus cycles in figures 5.8 to 5.25 for actual signal transitions.

The DataPump starts in the IDLE state and waits for NDPSEL falling edge and NNIRDY true. Once this is true, the PCMND value is sampled and the DataPump enters the CMD state.

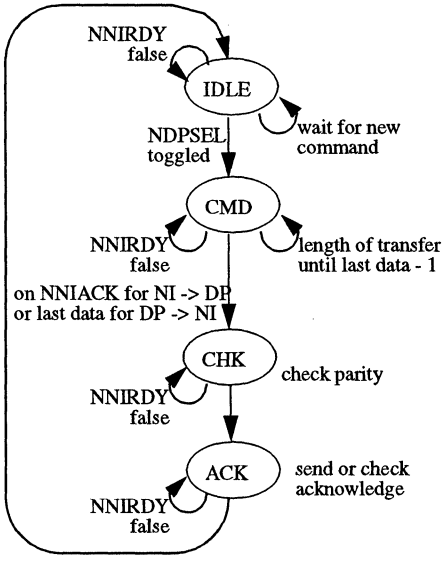
In the CMD state, data is either read out of or written into registers or queues up to but not including the last data transfer. While in the CMD state, NNIRDY is sampled every cycle and if asserted false, the state will freeze the next cycle.

Also, if NDPSEL is de-asserted, the DataPump goes back to IDLE and aborts the transfer without error. No packets are affected and no configuration registers are written.

The parity check state, CHK, is entered on receiving NNIACK for node interface to DataPump transfers or when driving the last data on receive queue transfers or on reading configuration registers on regRead transfers.

The ACK state is always entered after CHK if NNIRDY is true. In ACK the DataPump will drive NDPACK on node interface to DataPump transfers and check NNIACK on DataPump to node interface transfers.Finally, ACK goes to IDLE if NNIRDY was true.

Figure 5.7 : Basic NIBus Flow Diagram



5.6 Bus Cycles and Use of Signals

Send queue transfers from the node interface to the DataPump are shown in figures 5.8 through 5.17. While these examples show accesses to the send request queue, the transfers are identical for the send response queue.

Also, bus cycles with wait states using NNIRDY and aborts using NDPSEL are shown. These examples are applicable to receive queue and register transfers also.

Receive queue transfers are shown in figures 5.18 through 5.21. Register reads and writes are shown in figures 5.22 through 5.25.

These are not the complete set of bus cycle possibilities but indicate the operation of all the signals for all the various operations.

Send Queue Transfers and Use of NDPSEL

Figures 5.8 and 5.9 illustrate basic send queue transfer bus cycles plus the use of NDPSEL to initiate transfer commands.

Figure 5.8 specifically shows a send request queue packet transfer to the DataPump. Firstly, the queue flag PSNDREQ goes true indicating a slot has opened up in the send request queue for a new packet.

The node interface logic can then initiate a sendReq packet transfer to that queue. It does so in cycle T2 by driving NDPSEL from high to low while supplying the command code for sendReq, 100_2, on the PCMND pins. The DataPump transitions from the IDLE state to the CMD state.

The transfer commences (CMD state) as long as NDPSEL remains low up until NNIACK is asserted indicating end of data. This is done in cycle T7. The DataPump then completes checking the packet (CHK state) for correct size and length and correct parity.

These checks are completed and NDPACK is asserted (ACK state) in cycle T8 indicating successful transfer and the packet is validated in the send queue.

NDPSEL is allowed to transition from low to high in the acknowledge cycle, ACK. If it remains low, as shown in Figure 5.9 in cycle T9, the DataPump remains in the IDLE state and will not accept new commands.

NDPSEL must be driven high for a cycle then low again simultaneously with a new command, as shown in Figure 5.8 cycle T10 or Figure 5.9 cycle T11, to start a new transfer.

5.6.1 Using NNIRDY to Add Wait Cycles

NNIRDY false freezes the state of the DataPump. This is illustrated in figures 5.10 through 5.13.

While these diagrams are shown for sendReq transfers, the same behavior relative to NNIRDY occurs for all transfers.

Figures 5.10 and 5.11 show wait cycles in the CMD state. Figure 5.12 shows a wait cycle in the CHK state. Figure 5.13 show a wait cycle in the ACK state.

5.6.2 Using NDPESL to Abort Transfers

Figures 5.14, 5.15, 5.16, and 5.20 illustrate using NDPSEL to abort a transfer command before it is finished.

Aborting a send queue transfer in the CMD or CHK states will cause the DataPump not to enter the packet into the send queue and sends it into the IDLE state.

Aborting a register write in the CMD or CHK states will cause the DataPump not to write the selected register and sends it into the IDLE state.

Aborting a register read in the CMD or CHK states causes the DataPump to go into IDLE and not drive out the read data.

Figure 5.14 show aborting a send queue transfer during the CMD state. The cycle in which NDPSEL goes high, T7, the DataPump goes to the IDLE state.

Figure 5.15 shows aborting during the CHK state. NDPSEL goes high in T8 and the DataPump goes to the IDLE state.

Aborting a send queue transfer, a register write, or a register read during the ACK state has the effect of sending the DataPump into the IDLE state regardless of the value of NNIRDY. This is shown in Figure 5.16.

Whenever NDPSEL goes high on send queue transfers or register reads or writes, NNIRDY and NNIACK are not sampled and are don't cares.

Aborting a receive queue transfer in the CMD, CHK, or ACK states causes the DataPump not to remove the packet being transferred from the receive queue and to enter the IDLE state. The abort from the ACK state is shown in Figure 5.20.

In the case of receive queue transfers, NNIRDY and NNIACK must be true in the ACK cycle in order to remove the packet just transferred from the receive queue upon entering the IDLE state. This is shown in Figure 5.18, cycle T8. NDPSEL may be going high at this time, as shown.

5.6.3 Transfer Errors Indicated by NDPACK

Errors in the transfer detected by the DataPump will be indicated by not asserting NDPACK when it is supposed to be asserted. This is shown in Figure 17 for send queue transfers, Figure 21 for receive queue transfers, Figure 23 for register writes, and Figure 25 for register reads.

In each of these cases, NDPACK has a particular cycle in which it should be asserted and which the node interface logic can determine before hand.

In the case of send queue transfers, NDPACK should occur in the ACK cycle as shown in cycle T8 of Figure 5.17. This location may move out depending on wait cycles inserted by NNIRDY false.

In the case of the receive queue transfers, NDPACK should be asserted with the last data transfer. This cycle is determined by the node interface logic by counting data transfer cycles until the "size" value is reached. "size" is the packet size in octlet pairs given in the header octlet (i.e. the first octlet transferred, see figures 5.3 and 5.5). Figure 5.21 shows the error indication for receive queue transfers.

Register transfers always have the same number of cycles (if NNIRDY always true) and NDPACK should always be asserted in the appropriate cycle. Figures 5.23 and 5.25 show the cycle timing for error conditions in the register reads and writes.

5.6.4 Receive Queue Transfers

A basic receive queue transfer from the DataPump to the node interface logic is shown in Figure 5.18. This example shows the receive request queue going from empty to having received one packet in cycle T1 as indicated by PRCVREQ. The node interface responds with a rcvReq transfer command in T2. The PRCVREQ queue flag goes false again when the DataPump begins the transfer. A packet with 16-bytes of data is transferred and ends successfully in cycle T8. The node interface logic could issue a new command as soon as T9.

5.6.5 Register Read and Write Bus Cycles

A basic Register write transfer from the node interface to the DataPump is shown in Figure 5.22. The node interface sends the regWrite command in cycle T2 and write data on PDATA[0:31] (writes to registers only use the most significant 32-bits) and write address on PDATA[36:47] in cycle T3. The node interface must also drive the other bits in PDATA[32:63] and correct parity on PPARITY[4:7] to ensure that a false parity error doesn't occur. The DataPump acknowledges the successful write completion in cycle T5. A new command could be issued in T6.

A basic register read transfer is shown in Figure 5.24. The node interface sends the regRead command in cycle T2 and read address on PDATA[36:47] in cycle T3. The DataPump sends read data back on PDATA[0:31] in cycle T5. A new command could be issued in T6.

Note that the PDATA bus direction is split into different directions on the upper 32-bits and lower 32-bits in this transfer. This is the only transfer sequence where this happens

Also note that when the node interface drives address on PDATA[36:47] it must also drive all other bits in PDATA[32:63] and correct parity on PPARITY[4:7] or else a false parity error might be detected.

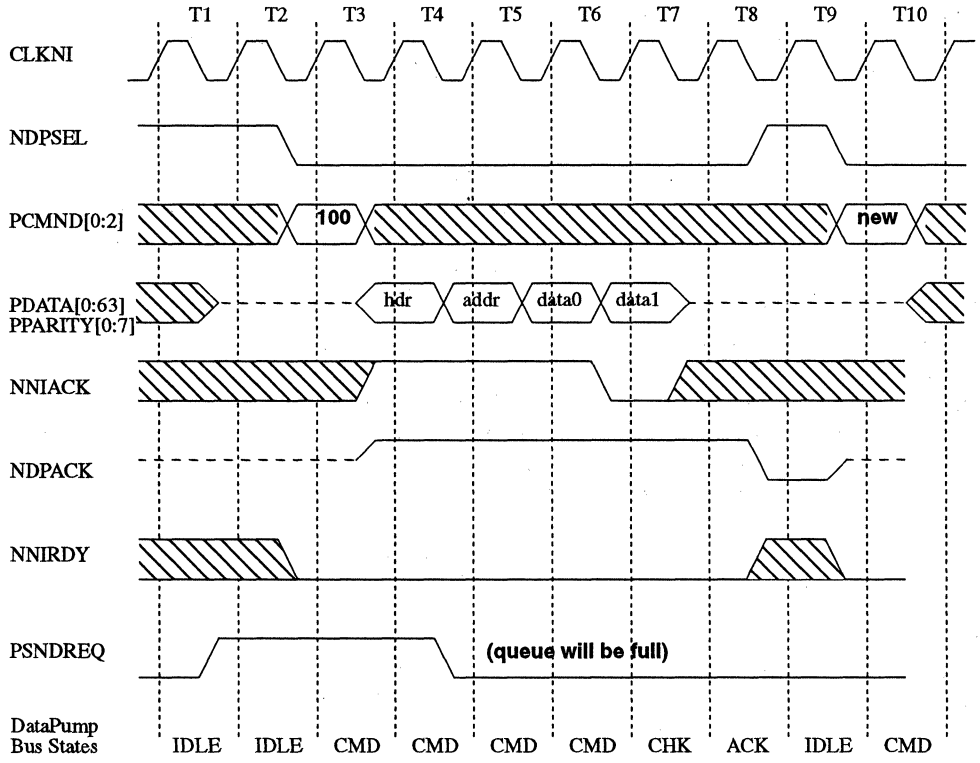
5.7 NIBus Reset and State Sync to the SCI Link

After toggling NRESET the NIBus state machine immediately enters the IDLE state, aborting any transfer it might have been in. At this point, new commands will be accepted from the node interface logic. Access to the queues and registers is not blocked, so the state of the SCI link should be checked before packets are put into the send queue (see 4.10, 4.11, and 4.12 sections on link initialization).

5.7.1 Node Interface Transfer Errors

Errors which occur directly related to transfers or protocol between the DataPump and node interface logic are logged by the DP_ERRLOG tcode field.

Figure 5.8 : SendReq Queue Transfer Initiated by PSNDREQ Flag

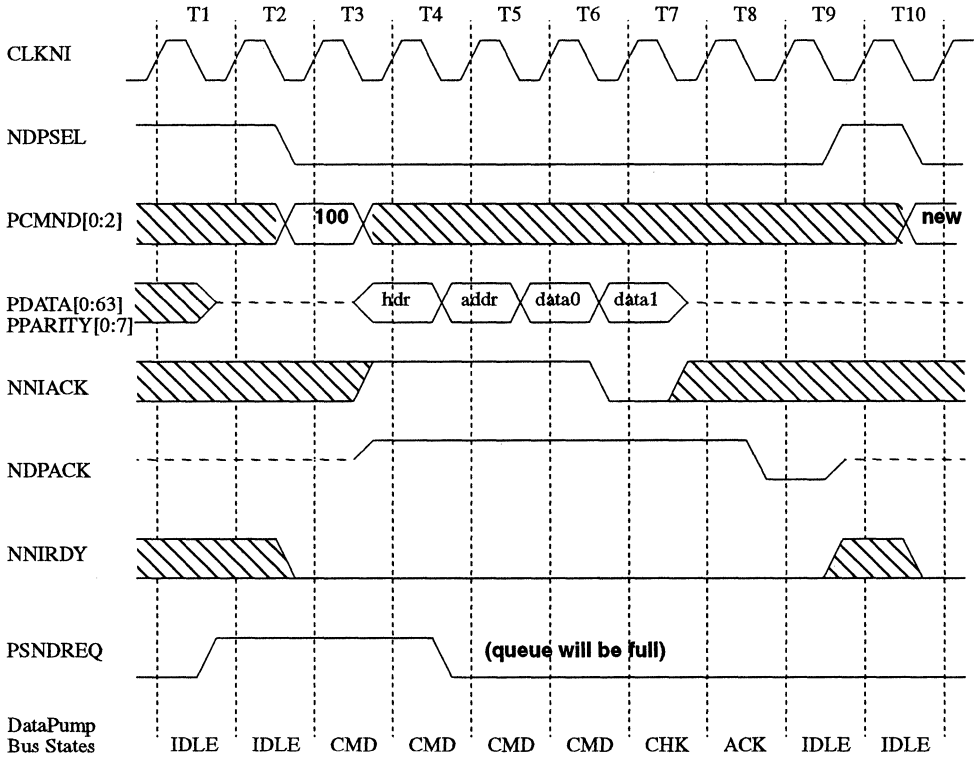


This diagram shows a normal send packet transfer to the DataPump. In this case, the packet contains the required header information and 16 bytes of data. Larger data payloads simply extend the number of cycles. NNIACK is used to indicate the end of transfer.

The DataPump never drives PDATA or PPARITY during a send queue transfer.

This diagram illustrates minimum cycle timing of all signals with no hold cycles.

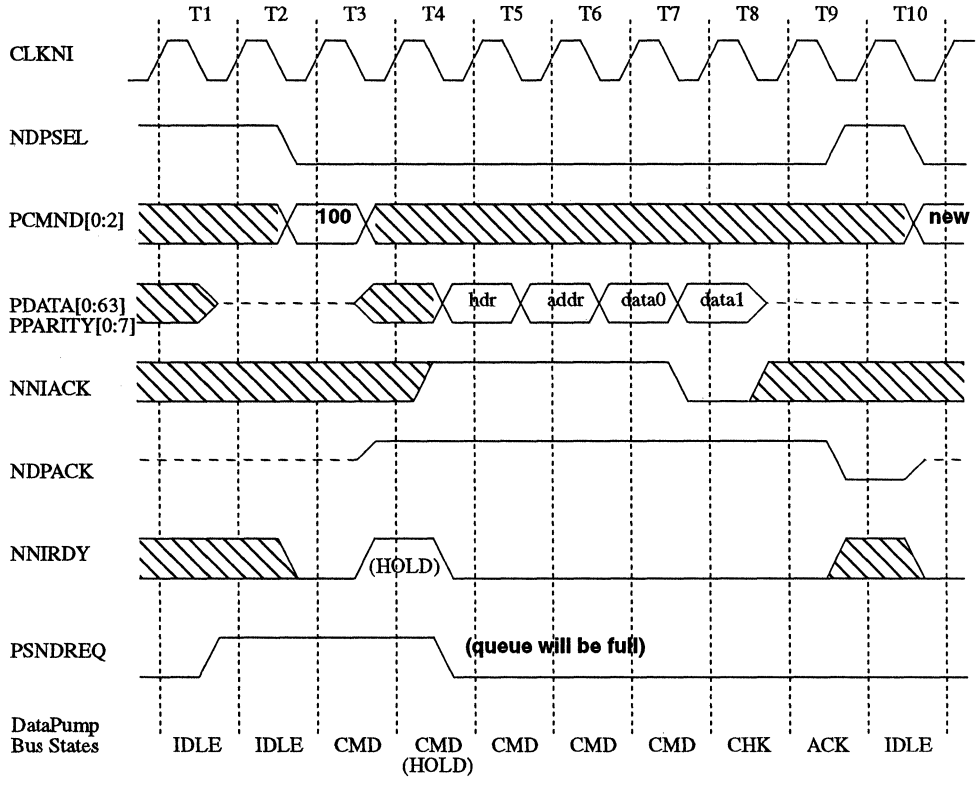
Figure 5.9 : SendReq Queue Transfer Followed by Extra IDLE Cycle Due to NDPSEL Low



This diagram illustrates the end of cycle transition to the IDLE state in cycle T9. The DataPump remains in IDLE until NDPSEL makes a high to low transition as shown in T10. In T11 the DataPump enters the CMD state as a result of NDPSEL transitioning from high to low in T10 and meeting input low set-up time before the transition to T11.

In order to load in a new command, NDPSEL must be driven high and low again as shown in this diagram. Otherwise, the DataPump remains in the IDLE state.

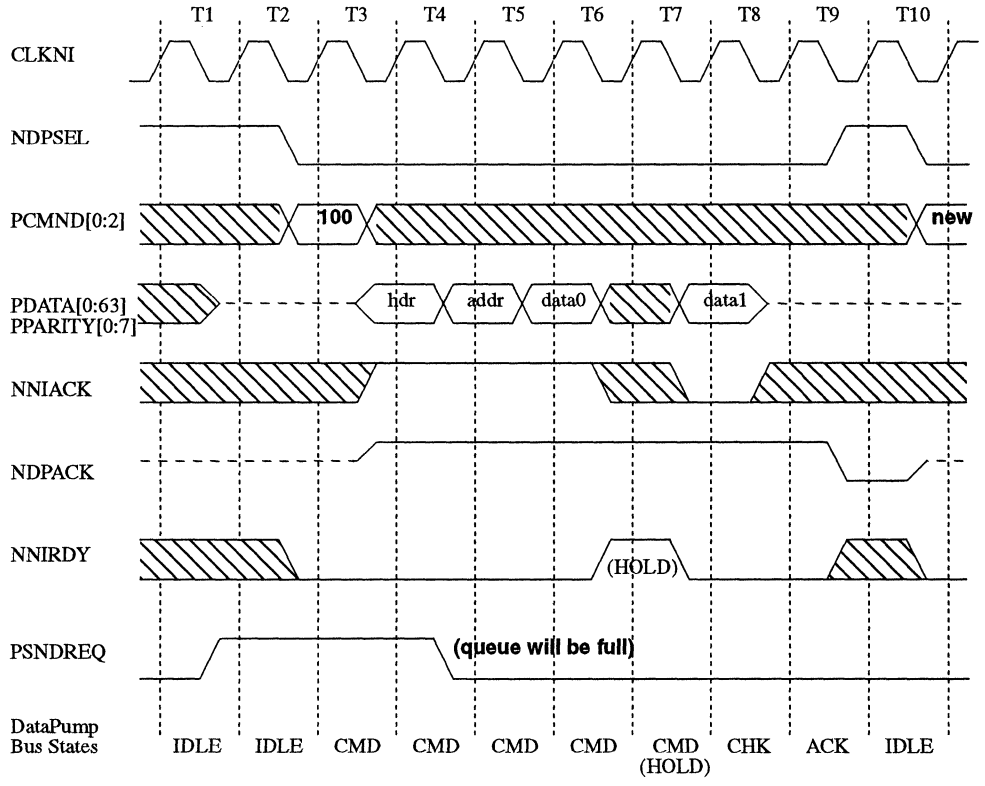
Figure 5.10 : SendReq Queue Transfer with Hold on First Data Transfer



This diagram illustrates the use of NNIRDY for flow control on providing data to the DataPump. NNIRDY false in the cycle first data is expected, T4, will cause the DataPump to hold for as many cycles as it remains false. In the cycle NNIRDY goes true again, T5, the DataPump begins loading the first data, i.e. "hdr".

Of course, NNIRDY false can be used to hold any cycle during the transfer.

Figure 5.11 : SendReq Queue Transfer with Hold on Last Data Transfer

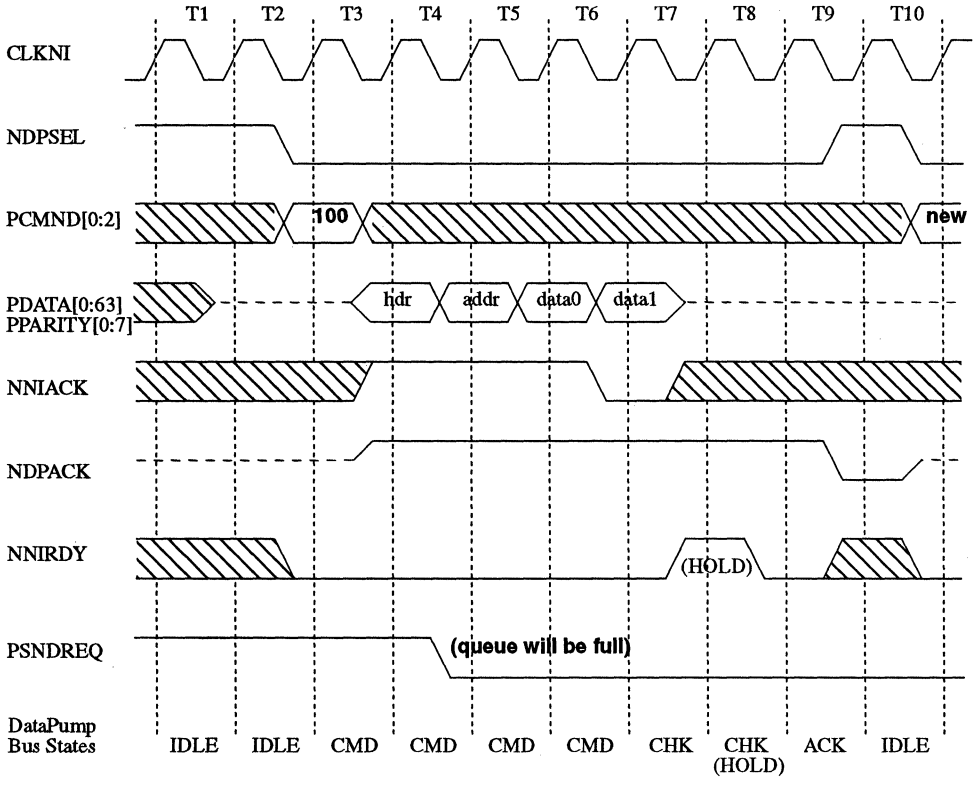


This diagram illustrates the use of NNIRDY to delay providing the last piece of data of the packet. NNIRDY false in T7 causes the DataPump to hold that cycle. Once NNIRDY goes true again in T8 the DataPump expects to see last data in T8 along with NNIACK.

This is a way to delay the assertion of NNIACK at the end of a packet if more time is needed in the node interface logic to compute NNIACK.

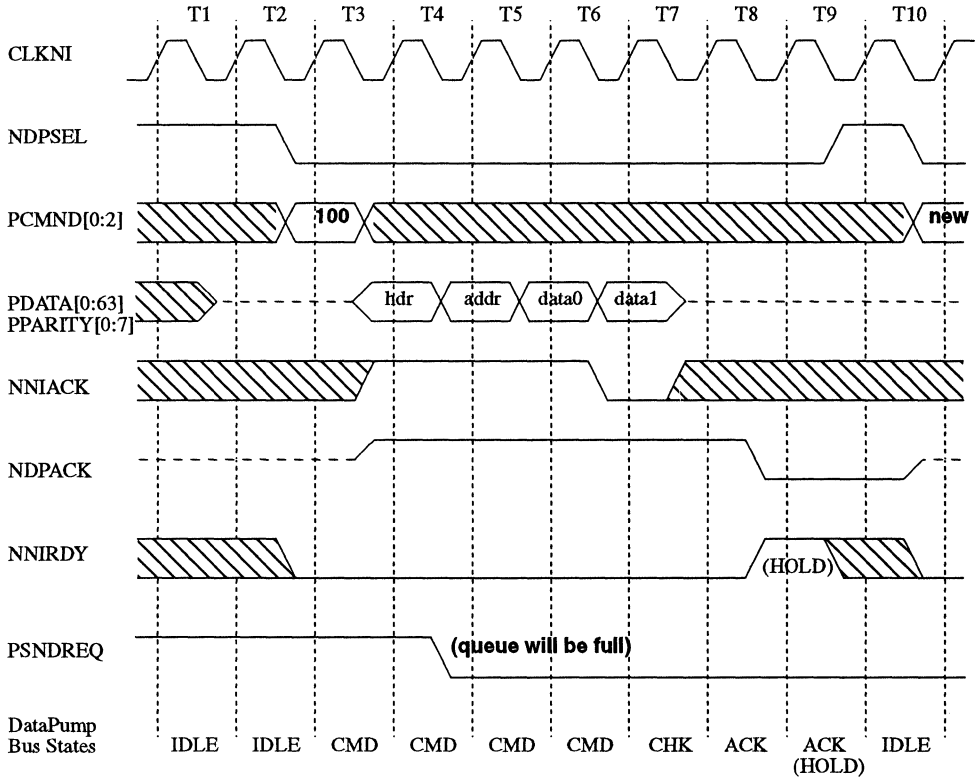
Of course, NNIRDY false can be used to hold any cycle during the transfer.

Figure 5.12 : SendReq Queue Transfer with Hold Before NDPACK.



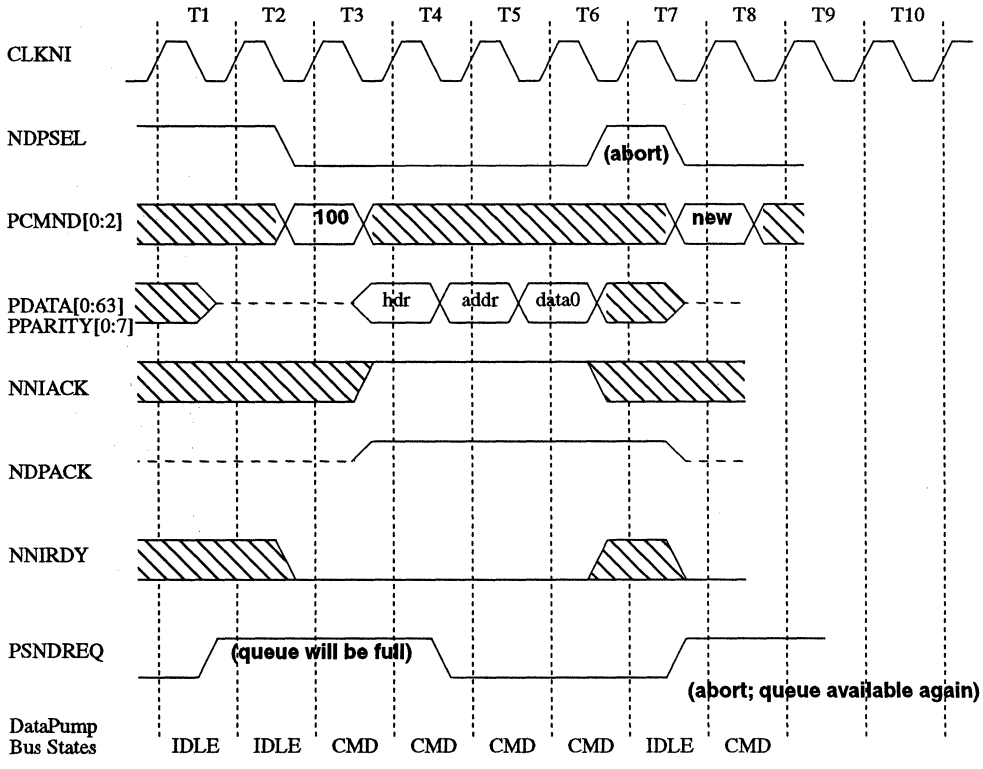
This diagram illustrates hold using NNIRDY false in the CHK cycle to hold off the assertion of NDPACK.

Figure 5.13 : SendReq Queue Transfer with Hold on NDPACK



This diagram illustrates hold using NNIRDY false in the ACK cycle to extend NDPACK one cycle.

Figure 5.14 : SendReq Queue Transfer Abort During CMD State



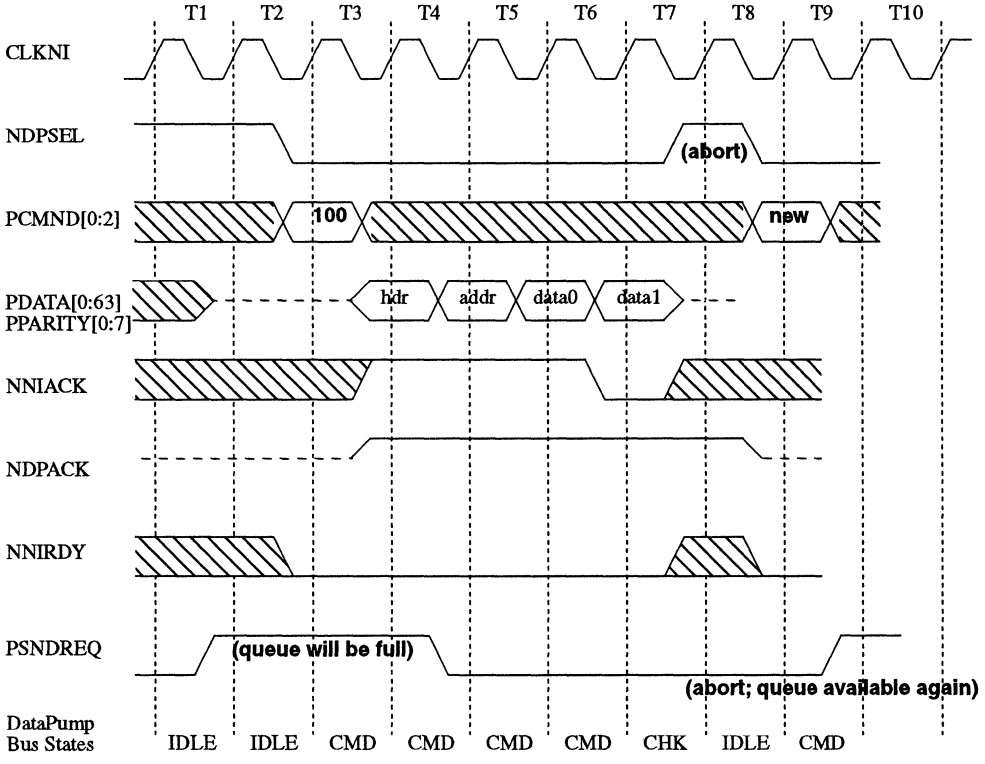
This diagram illustrates the use of NDPSEL driven false during a transfer to abort the transfer. During the transfer the DataPump is in the CMD state. A normal end of packet transfer occurs when NNIACK is asserted. The DataPump then transitions from the CMD state to the CHK state, then from CHK to ACK and IDLE again.

If NDPSEL is driven false during CMD state as shown in cycle T6, the DataPump aborts and goes to IDLE. The packet is not entered into the send queue.

If the packet transfer being executed would have filled the queue, the queue flag goes false as shown in cycle T4. Since the abort frees the queue slot again, the queue flag goes true again. It does take an additional cycle after the abort, as shown in cycle T8, to drive the queue flag true again.

If a new sendReq command is attempted in T8 (where "new" is indicated) then a sendQfull transfer

Figure 5.15 : SendReq Queue Transfer Abort During CHK State



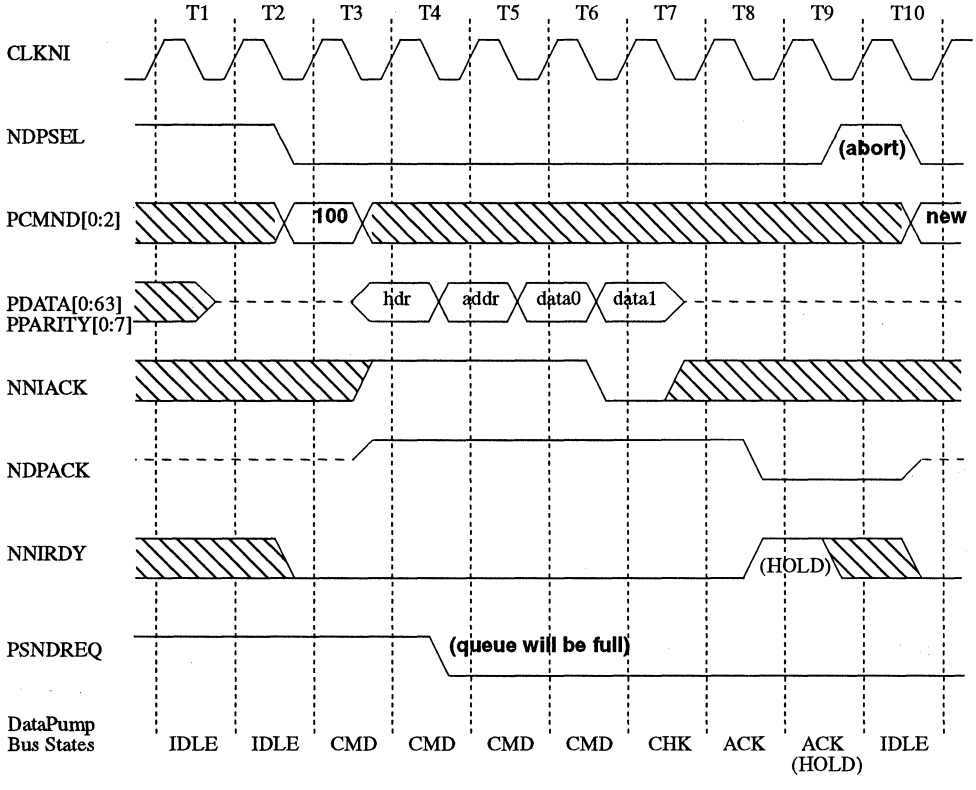
This diagram illustrates the use of NDPSEL driven false after the end of transfer to abort the entry into the queue. During the transfer the DataPump is in the CMD state. A normal end of packet transfer occurs when NNIACK is asserted. The DataPump then transitions from the CMD state to the CHK state, as shown in cycle T7.

If NDPSEL is driven false during CHK state as shown in cycle T7, the DataPump aborts and goes to IDLE. The packet is not entered into the send queue.

If the packet transfer being executed would have filled the queue, the queue flag goes false as shown in cycle T4. Since the abort frees the queue slot again, the queue flag goes true again. It does take an additional cycle after the abort, as shown in cycle T9, to drive the queue flag true again.

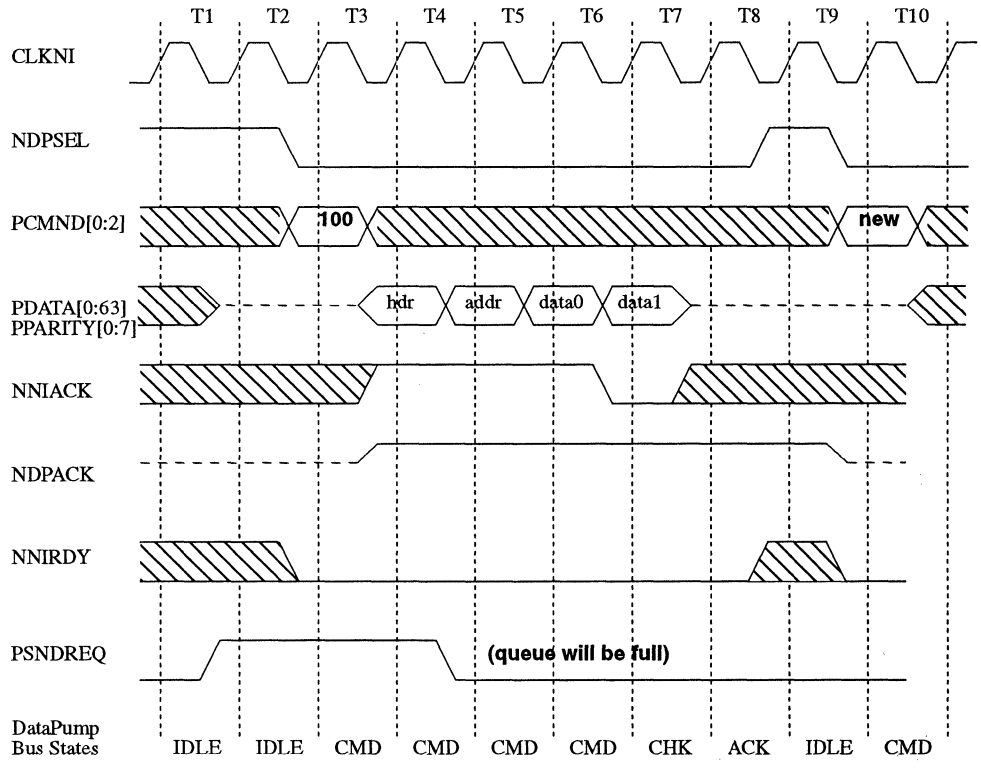
If a new sendReq command is attempted in T9 (where "new" is indicated) then a sendQfull transfer error will occur since the queue is not logically available, due to the abort, until T10.

Figure 5.16 : SendReq Queue Transfer with Abort During ACK Hold



This diagram illustrates how NDPSEL going high during ACK always aborts and sends the DataPump to IDLE. In the case of send queue transfers, however, there is no side effect of this abort. The send queue packet has already been validated in the queue by T8. NDPSEL going high after that only has the effect of overriding NNIRDY false (in T9) and sending the DataPump to IDLE.

Figure 5.17 : SendReq Queue Transfer with DataPump Detected Transfer Error



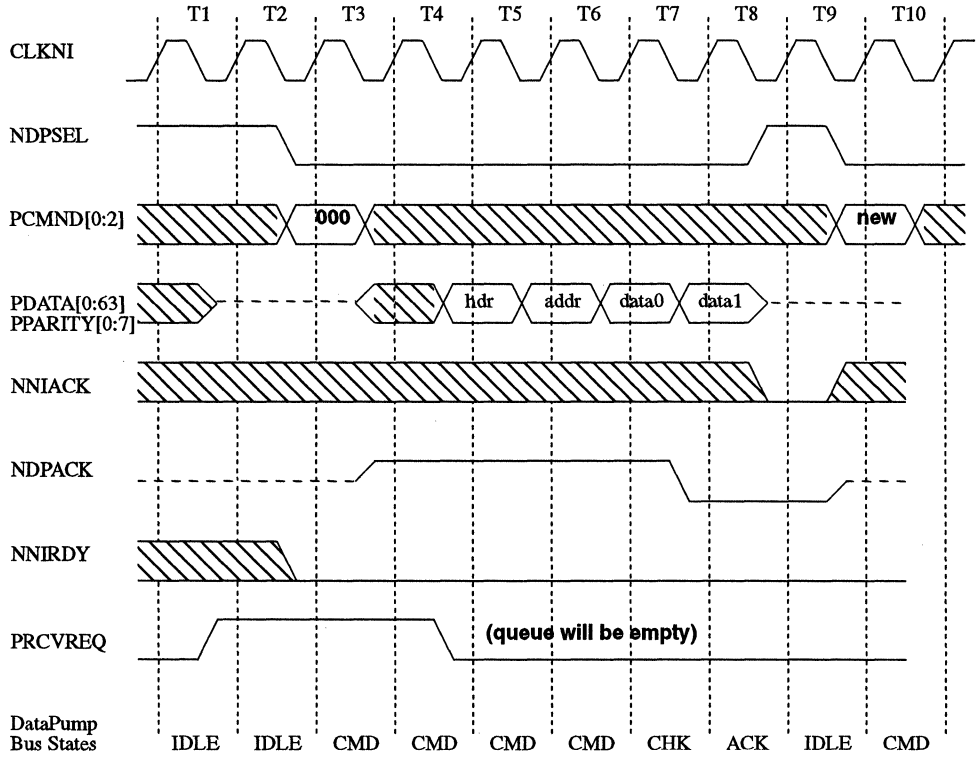
This diagram shows a send packet transfer to the DataPump with a DataPump detected error in the transfer. The error could be due to bad parity in the transfer, trying to write a full queue (not in this case since the PSNDREQ queue flag shows room), packet size not a multiple of two octlets or greater than 12 octlets (this example shows a valid packet size and even number of octlets), or request packet has a duplicate tranId to a request packet already in the queue.

The error is indicated by NDPACK false in cycle T8 when it should have been asserted true. The NDPACK signal always follows two cycles after NNIACK true (in the ACK state) unless NNIRDY is used to add wait cycles.

The packet is not entered into the queue and the DP_ERRLOG register records the transfer error and should be inspected by the node interface logic.

This diagram illustrates minimum cycle timing of all signals with no hold cycles.

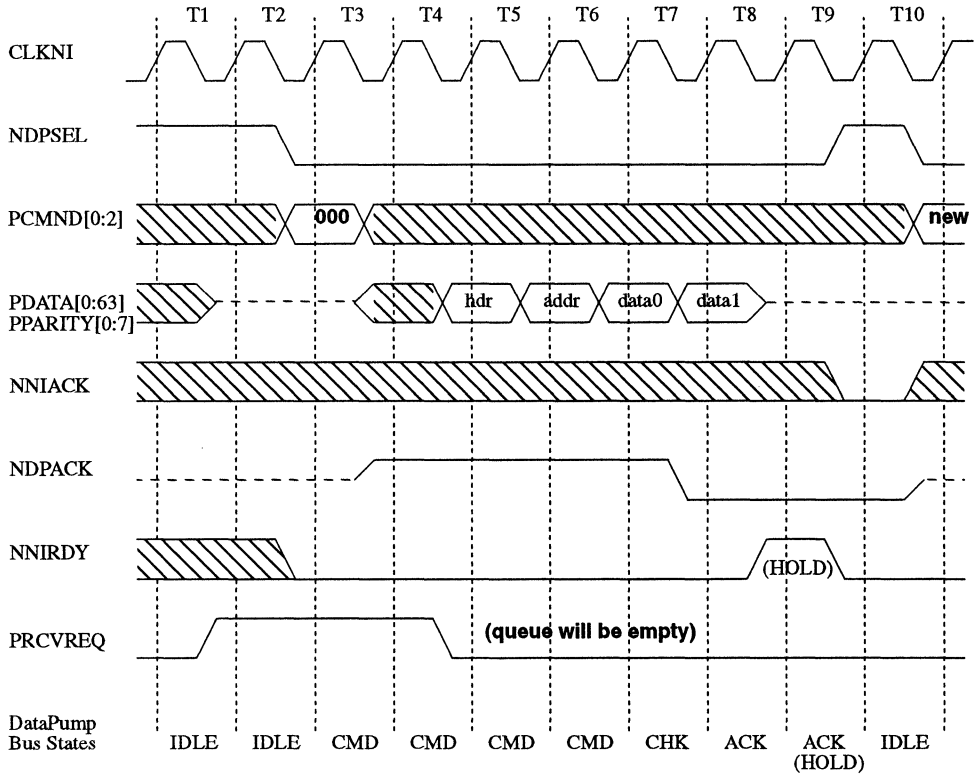
Figure 5.18 : RcvReq Queue Transfer Initiated by PRCVREQ Flag



This diagram shows a normal packet transfer from the DataPump to the node interface logic. In this case, the packet contains the required header information and 16 bytes of data. Larger data payloads simply extend the number of cycles. NDPACK is used to indicate the end of transfer.

This diagram illustrates minimum cycle timing of all signals with no hold cycles.

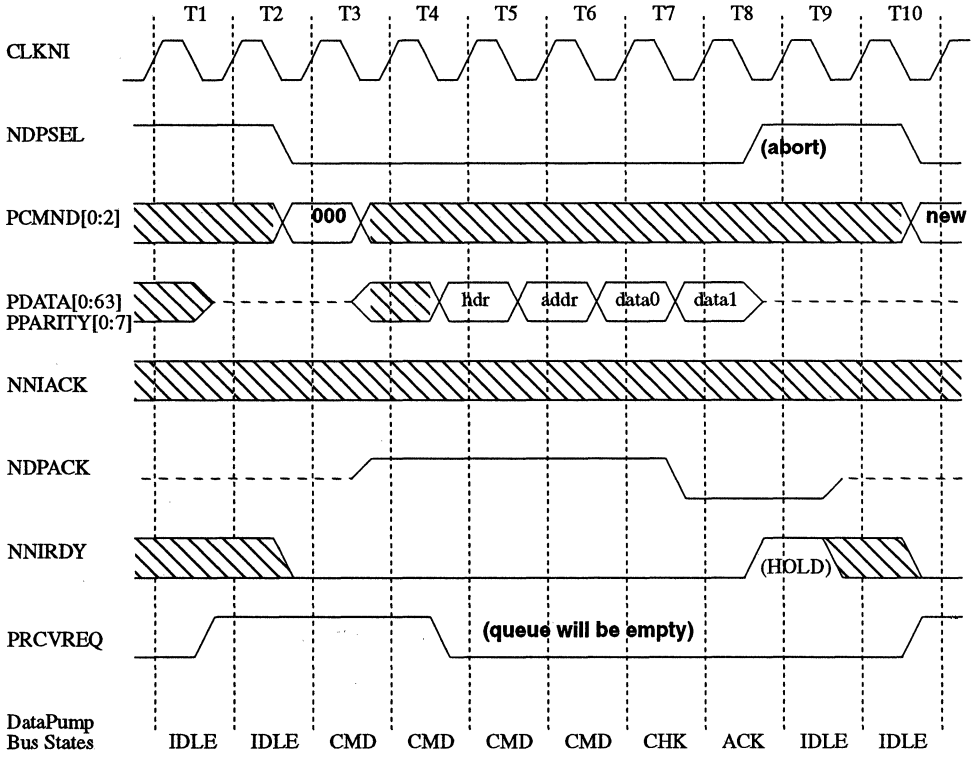
Figure 5.19 : RcvReq Queue Transfer with Hold for NNIACK



This diagram shows the use of NNIRDY to hold off the assertion of NNIACK for one cycle at the end of a transfer to the node interface logic. This may occur if the node interface logic needs an extra clock cycle to verify the transfer and check parity before sending acknowledge, NNIACK. NNIRDY false in T9 causes the DataPump to hold in the ACK state and wait on sampling NNIACK until NNIRDY goes true again in T10. Once the DataPump sees NNIACK in T10, it goes into the IDLE state and removes the packet just transferred from the receive queue.

If NNIACK had not been asserted in T10, the DataPump would not remove the packet from its receive queue and the PRCVREQ flag would go true again in cycle T11.

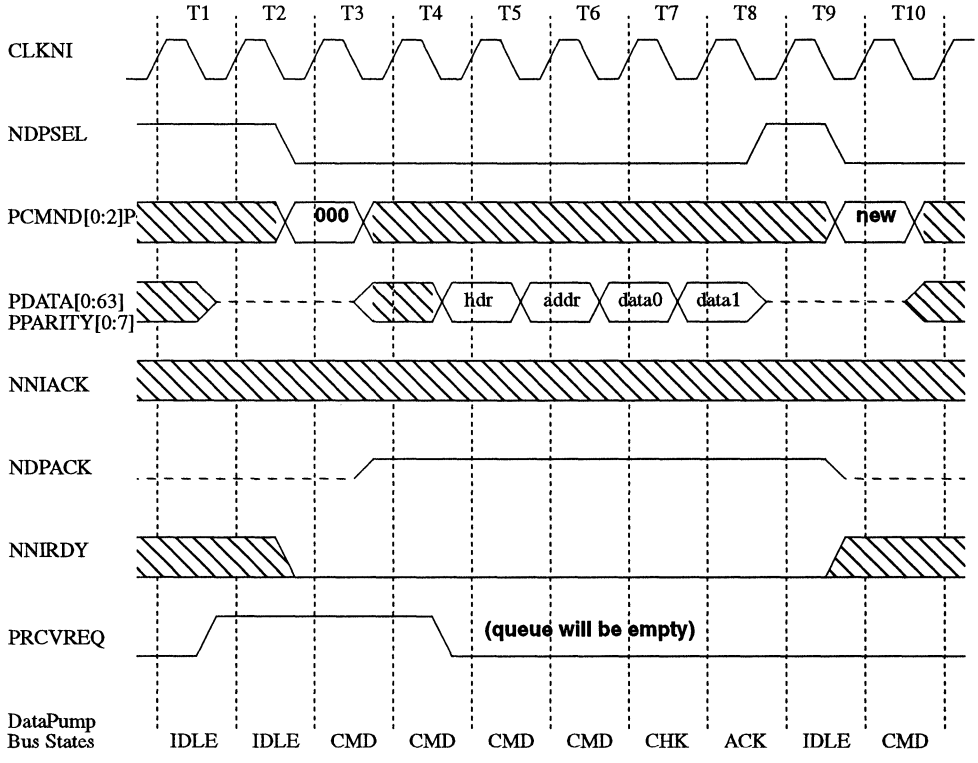
Figure 5.20 : RcvReq Queue Transfer with Abort During ACK Hold



This diagram shows how NDPSEL going high in the ACK state overrides NNIRDY false (as in T8). At the end of a receive queue transfer the DataPump checks for NNIRDY true and NNIACK true in the ACK cycle (beginning T9) in order to remove the just transferred receive packet from the receive queue.

Since NDPSEL aborted the end of the transfer in T9 before the DataPump received NNIACK and NNIRDY true, the packet would not be removed from the queue. This is reflected by the PRCVREQ flag going true again in T10 indicating a packet still present in the queue.

Figure 5.21 : RcvReq queue Transfer with DataPump Detected Transfer Error

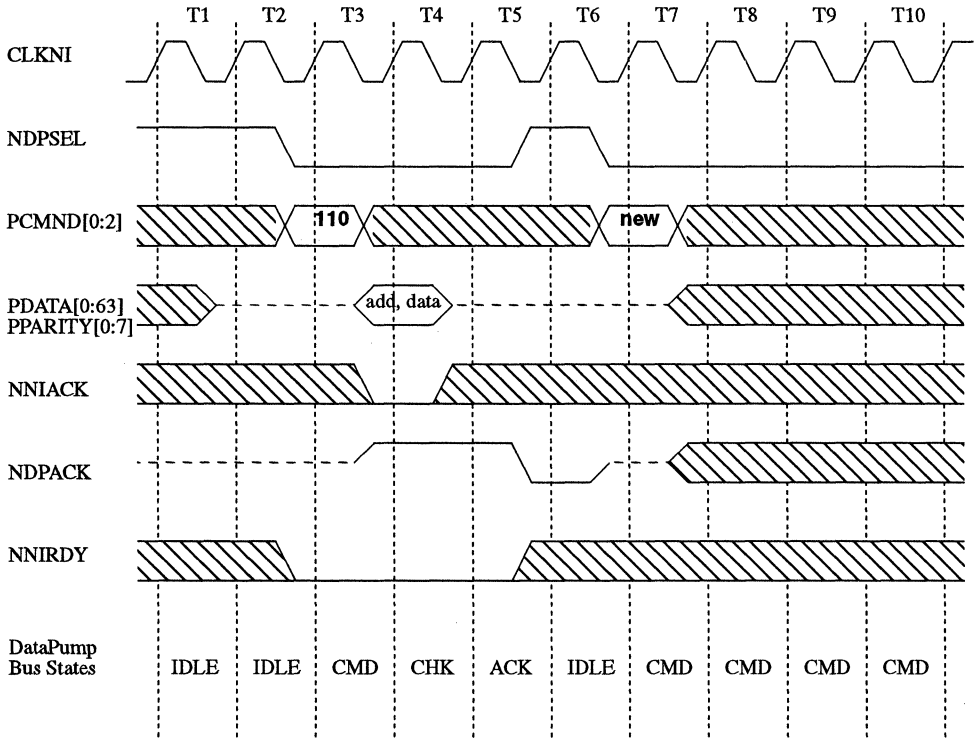


This diagram shows a packet transfer from the DataPump with a DataPump detected error in the transfer. The error could be due to bad parity in the packet in the receive queue or trying to read an empty queue (not in this case since the PRCVREQ queue flag shows a packet to be read).

The error is indicated by NDPACK false beginning in cycle T8 when it should have been asserted true. The NDPACK signal always occurs in the last data transfer cycle as indicated by counting octlets transferred up to the "size" value provided in the header octlet.

If the error was due to a parity error in the packet, it is removed from the receive queue in the ACK cycle even if the bad parity were detected in cycle T4, first data. However, if NDPSEL goes false anytime before ACK the transfer will abort and the packet will be retained in the queue even if it had bad parity. This gives the same behavior due to abort if an error occurred or not. The DP_ERRLOG register records the transfer error and should be inspected by the node interface logic.

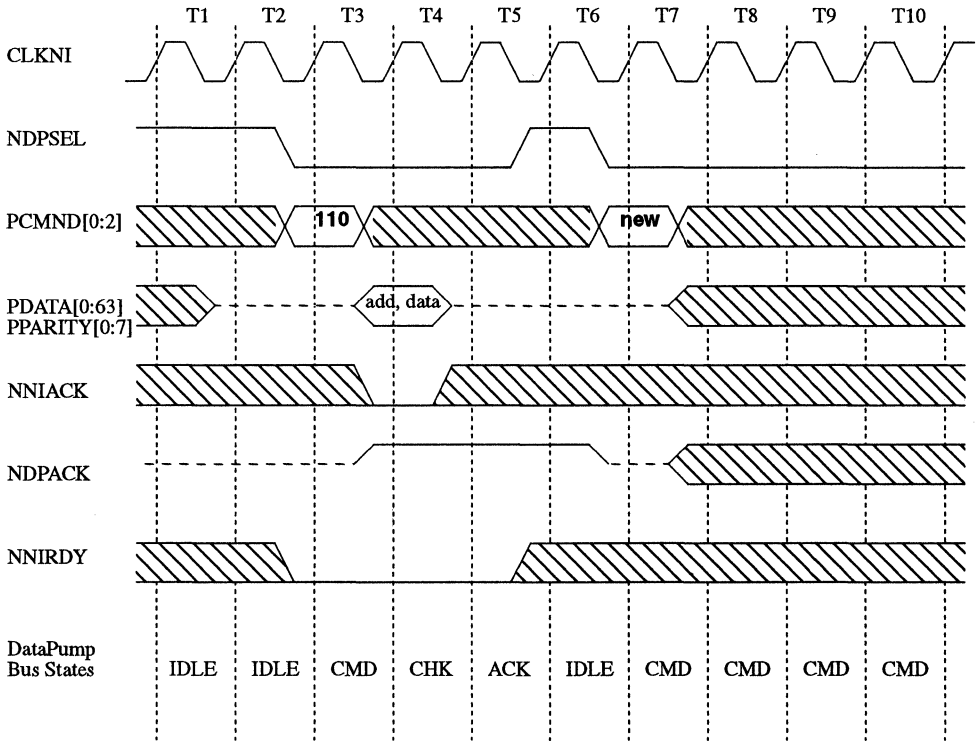
Figure 5.22 : RegWrite Transfer



This diagram shows a normal register write transfer from the node interface logic to the DataPump. In this case, register address offset and data are provided in T4 along with NNIACK. NDPACK is used to acknowledge the end of transfer in T6.

This diagram illustrates minimum cycle timing of all signals with no hold cycles.

Figure 5.23 : RegWrite Transfer with DataPump Detected Transfer Error

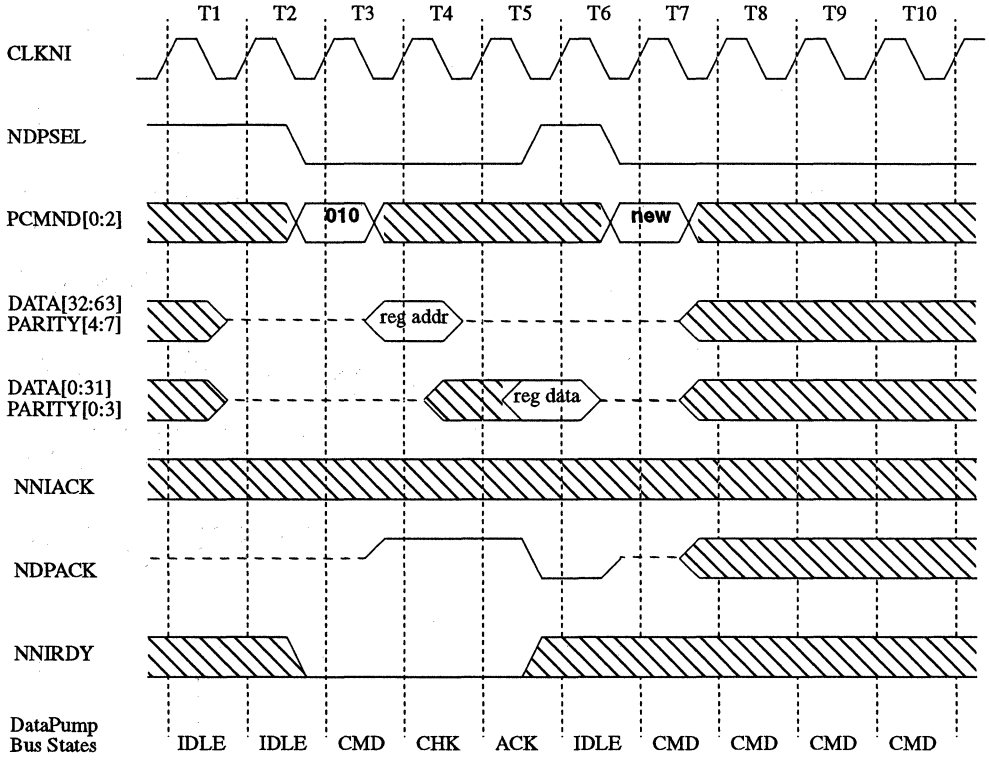


This diagram shows a register write transfer from the node interface logic to the DataPump with a DataPump detected transfer error. Errors of this type could be bad parity in the transfer or bad register offset address. In either case, the error is indicated by NDPACK false in T5 when it should have been asserted true.

No register is written and the DP_ERRLOG register records the transfer error and should be inspected by the node interface logic.

This diagram illustrates minimum cycle timing of all signals with no hold cycles.

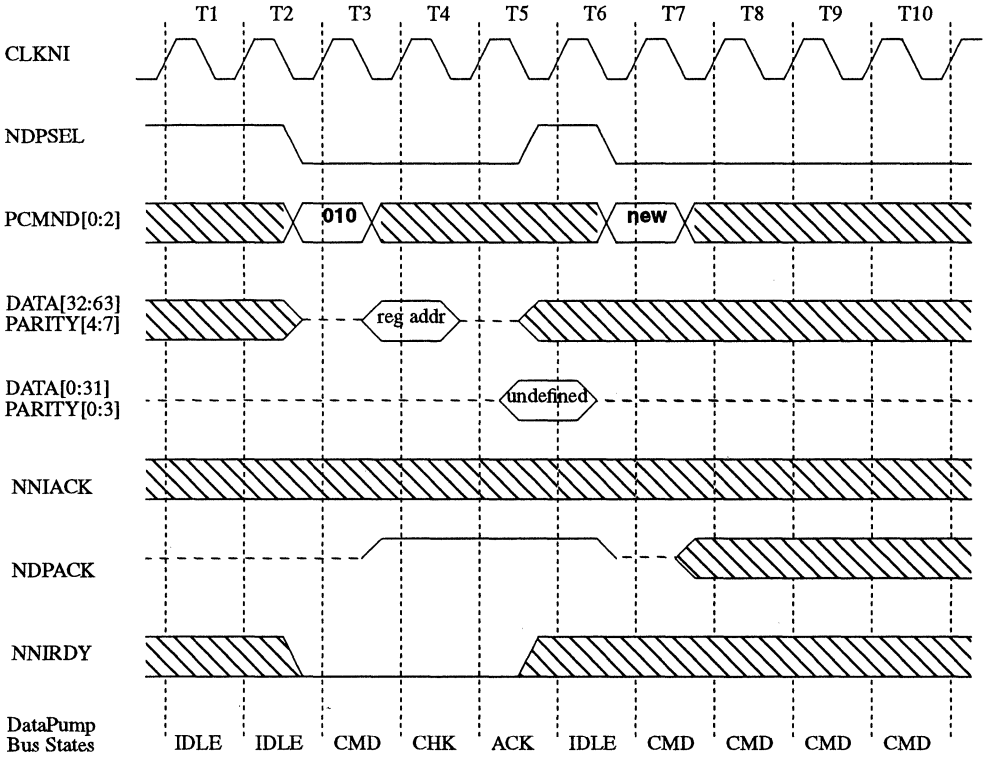
Figure 5.24 : RegRead Transfer



This diagram shows a normal register read transfer from the node interface logic to the DataPump. In this case, register address offset is provided in T4. The DataPump provides register read data back in cycle T5 along with NDPACK. NNIACK is not required in this case since the DataPump would take no action based on a true or false NNIACK.

This diagram illustrates minimum cycle timing of all signals with no hold cycles.

Figure 5.25 : RegRead transfer with DataPump detected error



This diagram shows a register read transfer with a DataPump detected transfer error. This type of error could only be a bad register offset address. The error is indicated by NDPACK false in T5 when it should have been asserted true. The data provided by the DataPump in T5 is undefined.

The DP_ERRLOG register records the transfer error and should be inspected by the node interface logic.

This diagram illustrates minimum cycle timing of all signals with no hold cycles.

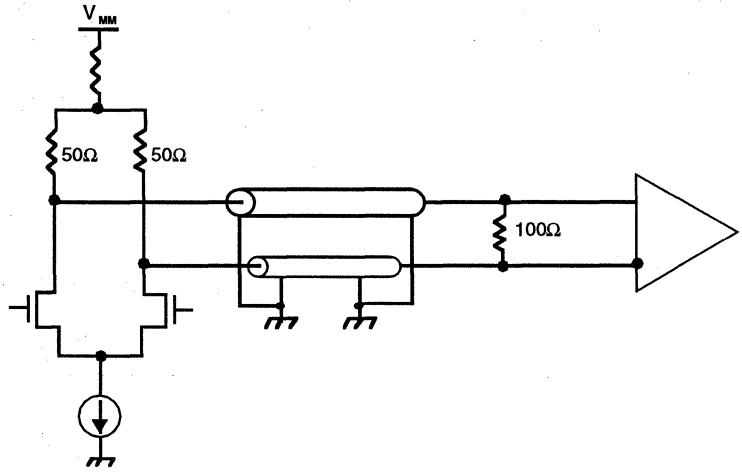
6.0 SCI High Speed Link Signals

The high speed interface on the DataPump chip complies with the Low Voltage Differential Signals proposed IEEE Std 1596.4. These are unidirectional, fully differential signals. The DC and AC electrical specifications are given in Section 11.0 Electrical Specifications.

6.1 PSCIDI[0:15] and PSCIDO[0:15] - Data

These are the 16-bit parallel data in and data output signals. The outputs have 50 ohm output impedance in each differential output. The inputs are terminated between true and complement inputs with on-chip nominal 100 ohms as shown in Figure 6-1.

Figure 6.1: PSCIDI and PSCIDO Terminations



6.2 PSCISI, PSCISO - SCI Strobe

This is the input and output strobe signal. The strobe transitions at the same time as data and flag and is used to latch data and flag into the DataPump on both edges. The DataPump has internal delay between strobe and data, flag to generate a clock signal for the input registers.

6.3 PSCIFI, PSCIFO - Flag Bit Encoding

Flag is asserted at the beginning of a packet to indicate packet start.

Flag is de-asserted near the end of a packet to indicate packet end. The number of cycles flag remains asserted depends on packet type.

If flag remains asserted at least 4 cycles, the packet must be a send packet (or an ABORT packet in which flag stays high 6 cycles and causes a noInSync error). The minimum send packet is 8 symbols. Flag will be deasserted 4 symbols before the end of the packet (indicating when to begin creating an echo packet if necessary).

An echo packet has a sequence of 3 cycles when flag is asserted. Flag goes false on the last cycle of the echo packet.

Sync packets have 8 symbols and flag is asserted on the first symbol only.

The ABORT packet (see Section 4.4.4 Special Packets and Flag Encoding) is 8 symbols long and the flag is asserted for the first 6 symbols.

7.0 Latency

(this section intentionally left blank)

8.0 Performance Counters

Two output pins, PPC0 and PPC1, are provided for monitoring certain internal events in the DataPump and which can be used along with external counters to monitor various performance aspects. There are two CSR registers which control the events which drive the PPC0 and PPC1 signals. Performance metrics are usually calculated by accumulating a reference count and dividing that into a qualified count with the ratio representing the performance metric. PPC0 is the output pin used to generate the reference count and PPC1 is used for the qualified count. For example, PPC0 may be set up to count all packets sent by the DataPump and PPC1 may be set to count all packets sent with a retry phase. The ratio of PPC1 to PPC0 is then the percentage of transmissions by this DataPump which were retrys. Another example would be to set PPC0 to count all bypassed packets and PPC1 to count bypassed packets which were coherent memory read requests. The ratio of PPC1 to PPC0 would then represent the percentage of those type packets out of all packets travelling to other nodes around the ringlet.

8.1 Command Field Mask/Compare

There are three 7-bit mask/compare functions located in the DataPump for performing a match on a packet's command field value. There is one comparator in the SCI input block, one in the SCI transmission block, and one at the send queue. A match out of these comparators occurs according to the following logic;

cmdMatch = ((packet.cmd[9:15] & cmdMask[0:6]) ==
(cmdCmp[0:6] & cmdMask[0:6]))

Thus, a bitwise equal comparison is made between the cmdCmp value in the DP_PC_CONFIG0 register and the packet's command field cmd value (bits 9 through 15). The cmdMask value masks off the comparison on a bitwise basis if the corresponding cmdMask bit is set to one. "cmdMatch" then goes true if all bits of the packet's command.cmd value is equal to the cmdCmp value for the bits which are not masked off by cmdMask.

A DP_PC_CONFIG0 register bit is also provided to invert the sense of "cmdMatch" called cmdSns. If cmdSns is set to one, "cmdMatch" will go true for mismatches instead of matches.

These comparators located in the SCI input, SCI transmission block, and the send queue are used to qualify the counting of packets to match user specified command values. For example, the "cmdMatch" result will go true only for response packets if cmdCmp is set to 1111100 and cmdMask is set to 0000011 and cmdSns is 0 since response packets can have only the command field values of 1111100, 111101, 1111110, or 1111111. If cmdSns is set then to 1 then "cmdMatch" will go true for non-response packets (requests, moves, and events). In this way, the command comparator can be set up to match any type of packets.

8.2 Extended Command Field Mask/Compare

In addition to the command field mask/compare functions there are two extended command field mask/compare functions. One is located in the SCI input block and one in the SCI transmission block. The extended command field comparator is 5-bits wide and operates on the command symbol bits 4,5,7,8, and 9. Bits 4 and 5 are the com.phase0 and com.phase1 bits which are used by the queue reservation protocol. Bit 7 indicates the packet is an echo when set. Bits 8 and 9 are the com.bsy and com.res bits respectively when the packet is an echo. Therefore, the extended command field mask/compare is useful for looking at the phase of packets to check for retry traffic and also for distinguishing echos from send packets. The logic for this mask/compare is as follows;

extMatch = ((packet.cmd[4,5,7-9] & extMask[0:4]) ==
(extCmp[0:4] & extMask[0:4]))

The values of extMask[0:4] and extCmp[0:4] are put into the DP_PC_CONFIG0 register. The mask/compare functions exactly like the command field mask/compare except on different bits of the command field.

8.3 PPC0 Functionality

The reference counter PPC0 can be set to monitor one of five events. The PPC0 output will toggle every time one of these events occurs. A resetable external counter should be connected to the PPC0 pin to accumulate a reference count over some time interval. These countable events are;

1. pktRcv - Packets received (i.e. target ID of packet matches this DataPump's nodeid) including echoes. Echoes can be excluded from this count by using the DP_PC_CONFIG0 refMask bit. This bit enables the extended command field mask/compare result to qualify the pktRcv PPC0 signal. Therefore, to exclude echoes from the pktRcv count the refMask bit is set, the extMask value is set to 11011 and the extCmp value is set to 00000. This will cause pktRcv to toggle only on received send packets.
2. Packets bypassed, including echo packets.
3. Packets sent, not including generated echoes.
4. Number of packets transmitted from the send-request queue.
5. Number of packets transmitted from the send-response queue.

Thus, the counter connected to PPC0 can be used to count all packets received, sent, or bypassed by this DataPump over a particular time interval or can count the number of packets transmitted from either of the send queues over a time interval. This count value will be used as the refernce value to measure some other qualified count value against. The qualified count value is generated by the PPC1 signal.

8.4 PPC1 Functionality

The qualified counter PPC1 can be set to monitor one of 13 different events. These events are broken down into the following categories;

1. Toggle whenever a matching packet is received, bypassed, or sent. These are used to monitor the packet traffic and bandwidth utilization on the SCI links.
2. Toggle at a rate proportional to the current number of packets in one of the four queues. This can be used to measure average queue depth and utilization.
3. Toggle whenever cc or ac changes. These give a measure of time around the ringlet and allocation time around the ringlet.
4. Assert whenever a matching packet is entered into one of the send queues. This is used to measure latency of a packet in the send queue; that is, the amount of time a packet spends in the send queue from the time it is entered until it is finally accepted at the other end and removed from the queue.
5. Assert whenever the current reservation phase matches the extended mask/compare value in the phase bits.

This is used to measure the amount of time the DataPump spends in each of the reservation phases.

The DP_PC_CONFIG1 register selects which of the 13 signals drives the PPC1 output pin. A value of one in that register corresponding to a particular signal will selct that signal to drive PPC1. If more than one bit of DP_PC_CONFIG1 is set to one the PPC1 output will be unpredictable.

8.4.1 Toggle on Matching Packet

There are three signals which will toggle when detecting a matching packet. These are;

1. RcvPkt - toggle when a matching packet is received at the SCI input link and the target ID matches this DataPump. This includes received echo packets but not generated echo packets. An additional qualifier bit in the DP_PC_CONFIG0 register is the rcvVldMask bit. When set to one, RcvPkt will toggle only on matching receive packets which in fact get entered into the receive queue. This would eliminate toggling on receive matching packets which are tossed because the receive queue is full or for other reasons such as bad CRC, etc.
2. BypPkt - toggle when a matching packet is bypassed from the input link to the bypass FIFO. This includes received echo packets but not generated echos.
3. SndPkt - toggle when a matching packet is transmitted from the send queue to the SCI output link, e.g. this does not include echos generated by the input link on retry echos.

All three of these signals use both the cmdMatch and extMatch results to qualify the toggling of the signal. The result of these comparators is anded together to generate the qualifier. There is a cmdMatch and extMatch comparator in both the SCI input link (used to qualify RcvPkt and BypPkt) and the SCI output link (used to qualify SndPkt).

8.4.2 Average Queue Depth Measurement

When PPC1 is set to monitor one of the four queue depth signals (rRspDepth, rReqDepth, sRspDepth, sReqDepth) it will toggle at a rate proportional to the number of packets in that queue. If there are four packets in the queue PPC1 will rise and fall 4 times during an 8 cycle CLKNI period. If there are three packets it will rise and fall 3 times in that same 8 cycle interval, for 2 packets it will rise and fall twice, and for 1 packet it will rise and fall only once. Therefore, a counter should be connected to PPC1 and a seperate counter to CLKNI. Average queue depth could then be calculated by first resetting both counters, letting them run for an interval while normal SCI operation occurs, then stoping them and using the following formula;

average queue depth = (PPC1 count)/((CLKNI count)/8)

In this way, the average queue depth can be determined for any queue under various loading conditions, etc.

8.4.3 CC and AC Ringlet Time Measurement

PPC1 can also be connected to signals monitoring the idle.cc and idle.ac bits going through the DataPump. When PPC1 is connected to either of these signals, it will basically reflect the value of idle.cc or idle.ac in the DataPump.

8.4.4 Send Queue Latency Measurement

The amount of time a send packet resides in the send queue can be monitored by connecting PPC1 to one of the signals, rsSlot0Tm or rqSlot0Tm. These signals are asserted as long as a packet is validated in either the request or response queue slot 0 location. Slot 0 is the first queue slot to be used after the queue starts from reset. By counting real time with one counter and elapsed time as qualified by PPC1 with another counter, the average latency of slot 0 for request or response send queues can be measured. The cmdMatch comparator is also applied to the command field of the packet in slot 0 for this signal. If the cmdMatch is false, PPC1 will not be asserted even if a packet is validated in slot 0. This allows the user to only measure latency of certain types of packets in the send queue; for example, cmdMatch coul be set to only match cache coherent traffic, thus giving latency for only cache coherent traffic.

8.4.5 Receive Queue Reservation State

The amount of time spent in one of the queue reservation states (SERVE_NA, SERVE_A, SERVE_NB, SERVE_B) can be determined by using the rsRsvPhs and rqRsvPhs signals connected to PPC1. These signals will be asserted whenever the reservation state matches the phase in extCmp[0:1]. The extMask[0:1] will also mask off either or both bits if desired. By using a real time counter and a second elapsed time counter connected to PPC1 the user can measure average time spent in a particular reservation phase, or by using extMask the average time spent in a reservation phase (SERVE_A and SERVE_B) versus a non-reservation phase (SERVE_NA and SERVE_NB).

9.0 Test Access Port

The DataPump conforms to the IEEE Std 1149.1 Standard Test Access Port and Boundary Scan Architecture. This allows access to all the inputs and outputs of the DataPump as well as on-line scan access to the CSR support registers using scan shadow registers. Also provided is access to internal RAMs.

The Test Access Port uses the pins PTCK, PTMS, NTRST, PTDI, and PTDO to perform serial shifting of data and control for testing the DataPump.

The internal DataPump clocks are all connected to PTCK to perform boundary scan or RAM testing. The clocks run normally for CSR shadow register access. The DataPump registers can be read and written through JTAG while the part is running normal operation.

A block diagram of the various scan chains accessible through JTAG is shown in Figure 9.1.

These registers operate like dual rank registers. That is, they have a shift register part and a parallel loading register part. In the case of boundary scan, the dual rank register is specified by the IEEE std.

The CSR shadow register is a single rank parallel load and shift register. For shadow register read operations the shadow register parallel loads from a selected internal CSR register and the data is then shifted out. For write operations the shadow register is shifted into and the data parallel loaded into the selected internal register.

The instruction register is a dual rank register made up of the shift register and a parallel load register. The outputs of the parallel load register actually provide the instruction data

9.0.1 Test-Logic_Reset State

Test logic is disabled in this state so normal operation of the DataPump can proceed unhindered. This state is entered asynchronously when NTRST is asserted or as long as PTMS is logic 1 for 5 consecutive PTCK rising edges. This state is unaffected by NRESET.

9.0.2 Run-Test/Idle State

This is the idle state between scan operations. No scan activity takes place during this state.

9.0.3 Select-DR-Scan State

This is the initial entry state for data register scan operations. No actual operations take place during this state, but it is necessary to go through this state to do data register scan operations.

9.0.4 Capture-DR State

In this state, a specific instruction register selected data scan register parallel loads from a given source.

In the case of the boundary scan EXTEST instruction the boundary scan register parallel loads from the input pins (and from chip internal signals on output pins).

In the case of a CSR read the internal register selected for read parallel loads into the shadow register.

No shifting of data takes place in this state.

9.0.5 Shift-DR State

In this state, the data register currently connected between PTDI and PTDO as defined by the instruction register is shifted one stage toward PTDO on PTCK rising edge. If PTMS remains logic 0, data will continue to shift with each PTCK rising edge.

9.0.6 Exit1-DR State

This is a temporary state during which no scan operations take place and no registers change value.

Figure 9.1 : Scan Test Access Port Block Diagram

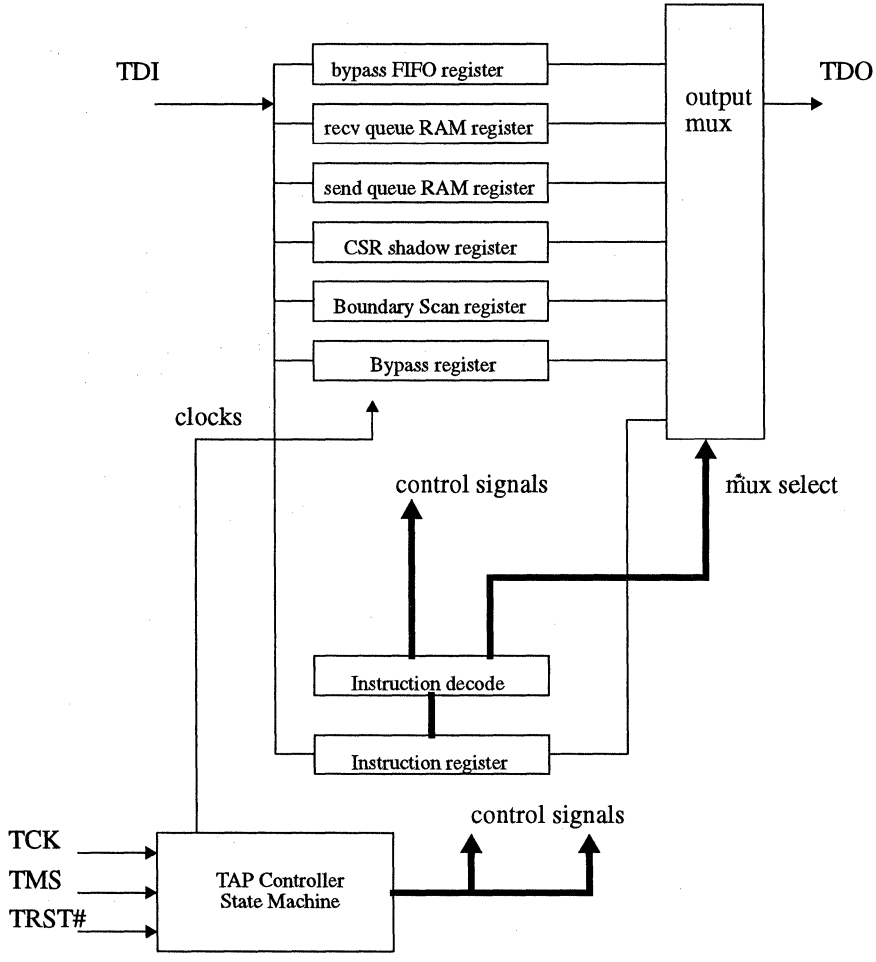
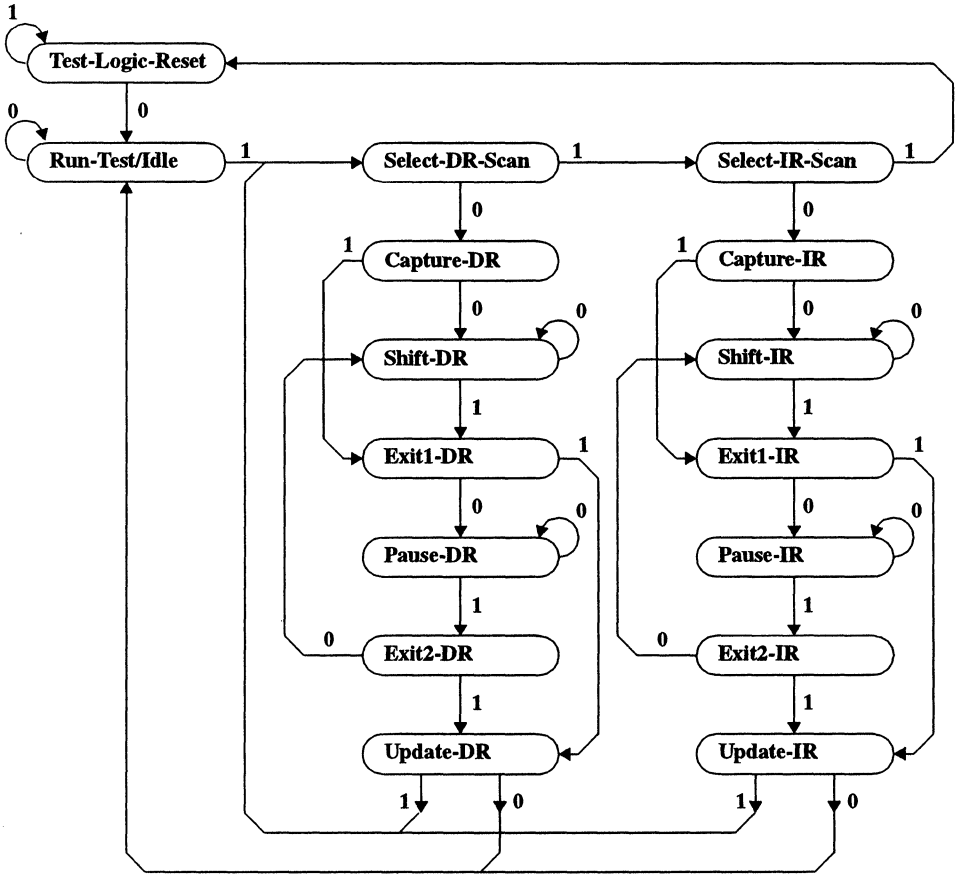


Figure 9.2 : Test Access Port State Diagram



Note: The value (0 or 1) shown adjacent to each state transition represents the value of TMS sampled on the rising edge of TCK.

9.1 TAP Controller State Machine

The TAP controller state machine is clocked by PTCK and controlled by PTMS. It is asynchronously reset by NTRST. Figure 9.2 shows the TAP controller state diagram. The various states are described below.

9.1.1 Test-Logic_Reset State

Test logic is disabled in this state so normal operation of the DataPump can proceed unhindered. This state is entered asynchronously when NTRST is asserted or as long as PTMS is logic 1 for 5 consecutive PTCK rising edges. This state is unaffected by NRESET.

9.1.2 Run-Test/Idle State

This is the idle state between scan operations. No scan activity takes place during this state.

9.1.3 Select-DR-Scan State

This is the initial entry state for data register scan operations. No actual operations take place during this state, but it is necessary to go through this state to do data register scan operations.

9.1.4 Capture-DR State

In this state, a specific instruction register selected data scan register parallel loads from a given source.

In the case of the boundary scan EXTEST instruction the boundary scan register parallel loads from the input pins (and from chip internal signals on output pins).

In the case of a CSR read the internal register selected for read parallel loads into the shadow register.

No shifting of data takes place in this state.

9.1.5 Shift-DR State

In this state, the data register currently connected between PTDI and PTDO as defined by the instruction register is shifted one stage toward PTDO on PTCK rising edge. If PTMS remains logic 0, data will continue to shift with each PTCK rising edge.

9.1.6 Exit1-DR State

This is a temporary state during which no scan operations take place and no registers change value.

9.1.7 Pause-DR State

This state allows the TAP controller to temporarily halt the shifting of data through the data register connected between PTDI and PTDO. If PTMS remains logic 0, the TAP controller will remain paused in this state.

This is a temporary state during which no scan operations take place and no registers change value.

9.1.8 Exit2-DR State

This is a temporary state during which no scan operations take place and no registers change value.

9.1.9 Update-DR State

In this state a specific instruction register selected data register parallel loads.

In the case of the boundary scan EXTEST instruction the output pin drivers parallel load from the boundary scan chain.

In the case of a CSR write instruction, the selected internal register parallel loads from the shadow register.

No shifting of data takes place during this state.

9.1.10 Select-IR-Scan State

This is the initial entry state for instruction register scan operations. No actual operations take place during this state, but it is necessary to go through this state to do instruction register scan operations.

9.1.11 Capture-IR State

In this state, the shift register in the instruction register is loaded with the previous instruction value on the rising edge of PTCK. The instruction register retains its previous value.

9.1.12 Shift-IR State

In this state, the shift register in the instruction register is connected between PTDI and PTDO and is shifted one stage toward PTDO on PTCK rising edge. If PTMS remains logic 0, data will continue to shift with each PTCK rising edge. The current instruction register value retains its previous value.

9.1.13 Exit1-IR State

This is a temporary state during which no scan operations take place and no registers change value.

9.1.14 Pause-IR State

This state allows the TAP controller to temporarily halt the shifting of data through the instruction shift register connected between PTDI and PTDO. If PTMS remains logic 0, the TAP controller will remain paused in this state.

This is a temporary state during which no scan operations take place and no registers change value.

9.1.15 Exit2-IR State

This is a temporary state during which no scan operations take place and no registers change value.

9.1.16 Update-IR State

The new instruction shifted into the instruction shift register is parallel loaded into the instruction register on the rising edge of PTCK in this state. This value becomes the current instruction.

9.2 TAP Controller Instructions

Instructions are shifted into the instruction register using the IR (instruction register) state machine operations. The instructions supported include TAP mandatory BYPASS, SAMPLE/PRELOAD, and EXTEST. DataPump specific instructions are also included.

The instruction register is 8-bits long and each instruction code (inst[7:0]) is given in hex form in Table 9.1. The shift order for inst[0:15] is inst7 to inst0.

The basic instructions are listed in Table 9.1.

Table 9.1: TAP Controller Instructions

Instruction	*Inst [0:15]*	*Description*
EXTEST	00_{16}	Provides external pin and board testing.
SAMPLE/ PRELOAD	01_{16}	Allows sampling inputs and preloading outputs without affecting normal operation.
RD_STATE	05_{16}	Read DP_STATE register
WR_STATE	06_{16}	Write DP_STATE register
RD_NODEID	15_{16}	Read DP_NODEID register
WR_NODEID	16_{16}	Write DP_NODEID register
RD_CLKTHRU	25_{16}	Read DP_CLKTHRU
RD_ERRLOG	45_{16}	Read DP_ERRLOG
WR_ERRLOG	46_{16}	Write DP_ERRLOG
RD_PC_CONFIG	55_{16}	Read DP_PC_CONFIG
WR_PC_CONFIG	56_{16}	Write DP_PC_CONFIG
RD_SQTAG0	65_{16}	Read DP_SENDQ_TAG0
RD_SQTAG1	75_{16}	Read DP_SENDQ_TAG1
RD_SQTAG2	85_{16}	Read DP_SENDQ_TAG2
RD_SQTAG3	95_{16}	Read DP_SENDQ_TAG3
BYPASS	FF_{16}	Connects TDI to bypass register to TDO.

9.3 BYPASS Instruction

The BYPASS instruction selects the single stage BYPASS shift register to be connected between PTDI and PTDO. This allows for a minimum delay shift path through the DataPump in the Shift-DR state. Capture-DR and Update-DR have no effect during this instruction. Execution of this instruction do not affect normal DataPump operation.

9.4 CSR Register Read/Write Instructions

These instructions provide shadow register access to the CSR support registers. The CSR support registers are a maximum of 32-bits in size. A 40-bit shift register (called a shadow register) is provided which is connected to PTDI and PTDO when CSR read/write instructions are loaded into the instruction register.

The register read instructions parallel load data from the selected CSR register into the shadow shift register on Capture-DR. The CSR register data is parallel loaded in with bit 0 corresponding to bit 0 of the shadow register. The data is then shifted out on Shift-DR starting with bit 39.

Bits 33-39 are always 0. Bit 32 is the NIbusy bit and indicates that the Node Interface is currently reading a CSR register and using the register read multiplexers. If this bit is set, the read data loaded into the shadow reg-

ister is undefined and the JTAG CSR read must be tried again until NIbusy is observed 0. The remaining bit ordering shifted out (bits 31 to 0) is the same order as specified for each CSR register in Section 4.8.

The register write instructions also parallel load data from the selected register on Capture-DR the same as a register read. During Shift-DR this read data is shifted out while the data to be written is shifted in. The write data is applied to the selected register on Update-DR.

The write data should be shifted in starting with 8 zeros (shadow register bits 32-39) followed by the write data starting with bit 31.

The write functionality applied on Update-DR is the same as if the data were written from the NIBus with a CSR write transaction. That is, if a bit of a register is read-only, the Update-DR won't change the bit. If a bit is clear-able, it will be cleared on Update-DR if the corresponding write data bit is set to one. Finally, if the bit is write-able, that bit will take the value of the corresponding bit in the write data on Update-DR. Full specification of each register bit and its access types are given in Section 4.8.

9.5 EXTEST Instruction

The EXTEST instruction allows testing of off-chip connections to the I/O and PC-board interconnections. Data at the input pins is captured in the boundary scan shift register in the Capture-DR state.

Data is shifted in the boundary scan shift register in the Shift-DR state.

The boundary scan output registers are parallel loaded and the outputs of the DataPump driven on the rising edge of PTCK in the Update-DR state.

9.6 SAMPLE/PRELOAD Instruction

The SAMPLE/PRELOAD instruction operates identically to the EXTEST instruction in the DataPump.

9.7 Boundary Scan Register and Ordering

The boundary scan register consists of a bit for each I/O plus three extra bits which control the tristate and bi-directional outputs. These three control bits are called Q_TRIDPACK, Q_TRI6332, and Q_TRI310.

PDATA[0:63] and PPARITY[0:7] are bidirectional I/O and NDPACK is a tri-stateable output.

Table 9.2 gives the boundary scan ordering.

Signal pin TSTMD must be grounded during boundary scan testing. Signal pin PTDI connects to the head of the boundary scan list. PTDI feeds Q_TRIDPACK. Signal pin PTDO is fed from the tail of the boundary scan list. Signal PSCIDO15 feeds PTDO.

The boundary scan ordering is as follows: PTDI → Q_TRIDPACK →.....→ PSCIDO15→ PTDO.

I/O's not sampled in the boundary scan mode are the following: PTCLK, PTMS, PTDI, NTRST, CLKHI, NCLKHI, and PTDO.

Table 9.2: Boundary Scan Chain Ordering

Name	*Type*	*Position in B.S. Chain*	*Control Pin*
Q_TRIDPACK	Control	1	—
Q_TRI6332	Control	2	—
Q_TRI310	Control	3	—
NO CONNECT 1	—	4	—
NO CONNECT 2	—	5	—
NO CONNECT 3	—	6	—
NO CONNECT 4	—	7	—
NDPSEL	Input	8	—
PCMND2	Input	9	—
PCMND1	Input	10	—
PCMND0	Input	11	—
NNIACK	Input	12	—
NNIRDY	Input	13	—
PCKHMPY0	Input	14	—
PCKHMPY1	Input	15	—
NRESET	Input	16	—
PSTOP	Input	17	—
CLKNI	Input	18	—
PCKHSEL	Input	19	—
PTSTMD	Input	20	—
PSTEP	Input	21	—
PMAINTMD0	Input	22	—
PMAINTMD1	Input	23	—
PCLK250	Input	24	—
NSYNCRQ	Input	25	—
NSCRUB	Input	26	—
NDPACK	Output	27	Q_TRIDPACK
PRCVREQ	Output	28	—
PRCVRSP	Output	29	—
PSNDREQ	Output	30	—
PSNDRSP	Output	31	—
NINTRNI	Output	32	—
PCLKSTB	Output	33	—
PPC0	Output	34	—
PPC1	Output	35	—
NERRNI	Output	36	—
PPARITY0	I/O	37	Q_TRI6332

Name	Type	Position in B.S. Chain	Control Pin
PPARITY1	I/O	38	Q_TRI6332
PPARITY2	I/O	39	Q_TRI6332
PPARITY3	I/O	40	Q_TRI6332
PPARITY4	I/O	41	Q_TRI310
PPARITY5	I/O	42	Q_TRI310
PPARITY6	I/O	43	Q_TRI310
PPARITY7	I/O	44	Q_TRI310
PDATA0	I/O	45	Q_TRI6332
PDATA1	I/O	46	Q_TRI6332
PDATA2	I/O	47	Q_TRI6332
PDATA3	I/O	48	Q_TRI6332
PDATA4	I/O	49	Q_TRI6332
PDATA5	I/O	50	Q_TRI6332
PDATA6	I/O	51	Q_TRI6332
PDATA7	I/O	52	Q_TRI6332
PDATA8	I/O	53	Q_TRI6332
PDATA9	I/O	54	Q_TRI6332
PDATA10	I/O	55	Q_TRI6332
PDATA11	I/O	56	Q_TRI6332
PDATA12	I/O	57	Q_TRI6332
PDATA13	I/O	58	Q_TRI6332
PDATA14	I/O	59	Q_TRI6332
PDATA15	I/O	60	Q_TRI6332
PDATA16	I/O	61	Q_TRI6332
PDATA17	I/O	62	Q_TRI6332
PDATA18	I/O	63	Q_TRI6332
PDATA19	I/O	64	Q_TRI6332
PDATA20	I/O	65	Q_TRI6332
PDATA21	I/O	66	Q_TRI6332
PDATA22	I/O	67	Q_TRI6332
PDATA23	I/O	68	Q_TRI6332
PDATA24	I/O	69	Q_TRI6332
PDATA25	I/O	70	Q_TRI6332
PDATA26	I/O	71	Q_TRI6332
PDATA27	I/O	72	Q_TRI6332
PDATA28	I/O	73	Q_TRI6332
PDATA29	I/O	74	Q_TRI6332
PDATA30	I/O	75	Q_TRI6332
PDATA31	I/O	76	Q_TRI6332

Name	Type	Position in B.S. Chain	Control Pin
PDATA32	I/O	77	Q_TRI310
PDATA33	I/O	78	Q_TRI310
PDATA34	I/O	79	Q_TRI310
PDATA35	I/O	80	Q_TRI310
PDATA36	I/O	81	Q_TRI310
PDATA37	I/O	82	Q_TRI310
PDATA38	I/O	83	Q_TRI310
PDATA39	I/O	84	Q_TRI310
PDATA40	I/O	85	Q_TRI310
PDATA41	I/O	86	Q_TRI310
PDATA42	I/O	87	Q_TRI310
PDATA43	I/O	88	Q_TRI310
PDATA44	I/O	89	Q_TRI310
PDATA45	I/O	90	Q_TRI310
PDATA46	I/O	91	Q_TRI310
PDATA47	I/O	92	Q_TRI310
PDATA48	I/O	93	Q_TRI310
PDATA49	I/O	94	Q_TRI310
PDATA50	I/O	95	Q_TRI310
PDATA51	I/O	96	Q_TRI310
PDATA52	I/O	97	Q_TRI310
PDATA53	I/O	98	Q_TRI310
PDATA54	I/O	99	Q_TRI310
PDATA55	I/O	100	Q_TRI310
PDATA56	I/O	101	Q_TRI310
PDATA57	I/O	102	Q_TRI310
PDATA58	I/O	103	Q_TRI310
PDATA59	I/O	104	Q_TRI310
PDATA60	I/O	105	Q_TRI310
PDATA61	I/O	106	Q_TRI310
PDATA62	I/O	107	Q_TRI310
PDATA63	I/O	108	Q_TRI310
PSCIDI0	Input	109	—
PSCIDI1	Input	110	—
PSCIDI2	Input	111	—
PSCIDI3	Input	112	—
PSCIDI4	Input	113	—
PSCIDI5	Input	114	—
PSCIDI6	Input	115	—

Name	Type	Position in B.S. Chain	Control Pin
PSCIDI7	Input	116	—
PSCIDI8	Input	117	—
PSCIDI9	Input	118	—
PSCIDI10	Input	119	—
PSCIDI11	Input	120	—
PSCIDI12	Input	121	—
PSCIDI13	Input	122	—
PSCIDI14	Input	123	—
PSCIDI15	Input	124	—
PSCIFI	Input	125	—
PSCISI	Input	126	—
PSCISO	Output	127	—
PSCIFO	Output	128	—
PSCIDO0	Output	129	—
PSCIDO1	Output	130	—
PSCIDO2	Output	131	—
PSCIDO3	Output	132	—
PSCIDO4	Output	133	—
PSCIDO5	Output	134	—
PSCIDO6	Output	135	—
PSCIDO7	Output	136	—
PSCIDO8	Output	137	—
PSCIDO9	Output	138	—
PSCIDO10	Output	139	—
PSCIDO11	Output	140	—
PSCIDO12	Output	141	—
PSCIDO13	Output	142	—
PSCIDO14	Output	143	—
PSCIDO15	Output	144	—

10.0 Internal Scan Test and Diagnostics

Scan test of on-chip RAMs through JTAG can be performed but is not documented here. No other internal chip state is available for scan. There is no built-in self test either.

11.0 Electrical Specifications

11.1 DC Specifications

Table 11.1: Absolute Maximum Ratings

Symbol	Rating	Limit
V_{MM}	+2 V power supply voltage	-0.5 to 2.6 V
V_{TTL}	+3.3 V power supply voltage	-0.5 to 4.0 V
VinA	Any pad voltage except LVDS outputs and GTL input or output	-1.0 to V_{TTL} + 1.0 V
VinB	LVDS output or GTL I/O pad voltage	-1.0 to V_{DD} + 1.0 V
I_{OUTT}	TTL output short circuit current	TBD
I_{OUTG}	GTL output short circuit current (V_{GTLOUT} = 3 V)	TBD
Tc	Case temperature under bias	-55C to +125C
Tstg	Storage temperature	-65C to +150C

Table 11.2: Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{MM}	Supply voltage +2.0 V	1.9	2.0	2.1	V
V_{TTL}	Supply voltage +3.3 V	3.1	3.3	3.5	V
Tc	Operating case temperature	0	-	75	deg C

Table 11.3: Power Dissipation

Symbol	Parameter	Min	Typ	Max	Units
I_{MM}	Power supply current from V_{MM}	-	-	12.9	A
I_{TTL}	Power supply current from V_{TTL}	-	-	0.3	A
Pd	Total Power Dissipation	-	22	28.1	W

Table 11.4: TTL Input/Output DC Electrical Specifications *(Over recommended operating conditions.)*

Symbol	Parameter	Min	Typ	Max	Units
V_{OH}	Output high, I_{OH} = -2.4 mA	2.4	-	-	V
V_{OL}	Output low, I_{OL} = 8 mA	-	-	0.4	V
V_{IH}	Input high voltage [Not 5V Tolerant]	2.0	-	V_{TTL} + 1.0	V
V_{IL}	Input low voltage	- 1.0	-	0.8	V
I_{IH}	Input high current, V_{IN} = 2.4 V	-	-	50	uA
I_{IL}	Input low current, V_{IN} = 0.4 V	-1000	-	-	uA

Table 11.5: GTL Input/Output DC Electrical Specifications *(Over recommended operating conditions. Termination resistance = 25 ohms.)*

Symbol	Parameter	Min	Typ	Max	Units
V_{TT}	Termination voltage	1.14	1.20	1.26	V
V_{GREF}	Reference voltage	(2/3)*V_{TT} - 2%	0.8	(2/3)*V_{TT} + 2%	V
I_{GREF}	Input reference current on V_{GREF}	-	-	10	mA
V_{OL}	Output low, I_{OL} = 50 mA	-	-	0.4	V
V_{IH}	Input high voltage	V_{REF} + 0.1	0.85	-	V
V_{IL}	Input low voltage	-	0.75	V_{REF} - 0.1	V
I_{ZOL}	Output leakage current, 0.0 <= V_{OUT} <= V_{TT} (output off)	-	-	+200	uA
I_{IL}	Input leakage current, 0.0 <= V_{IN} <= V_{TT}	-10	-	+10	uA

Table 11.6: LVDS Output Driver DC Electrical Specifications *(Over recommended operating conditions.)*

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output voltage high	Rload = 100 ohms	1250	1475	mV
V_{OL}	Output voltage low	Rload = 100 ohms	925	1150	mV
V_{OD}	Output differential voltage	Rload = 100 ohms	250	400	mV
V_{OS}	Output offset voltage	Rload = 100 ohms	1125	1275	mV
dV_{OD}	Change in differential voltage between complementary states.	Rload = 100 ohms	-	25	mV
dV_{OS}	Change in offset voltage between complementary states.	Rload = 100 ohms	-	25	mV
R_O	Output impedance	Iload = 2 to 2.5 mA	35	65	ohms
dR_O	Ro mismatch	Iload = 2 to 2.5 mA	-	10	%

Table 11.7: LVDS Input Receiver DC Electrical Specifications *(Over recommended operating conditions.)*

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	Input voltage high	V_{ID}= 100mV	100	2200	mV
V_{IL}	Input voltage low	V_{ID}= 100mV	0	2100	mV
+/- V_{ID}	Input differential voltage		100	500	mV
V_{ICM}	Input voltage common mode	V_{ID}= VIDMIN	50	2150	mV
		V_{ID}= VIDMAX	250	1950	
R_{IN}	Input impedance	0 < V_{IN} < 2.4V	80	120	ohm

11.2 AC Timing Specifications

Table 11.8 shows the timing specifications for all the NIBus signals plus miscellaneous GTL level signals. All signals in this group are synchronous to CLKNI.

The inputs include PDATA[0:63], PPARITY[0:7], NDPSEL, PCMND[0:2], NNIACK, NNIRDY, NRESET, and NSYNCRQ.

The outputs include PDATA[0:63], PPARITY[0:7], NDPACK, PRCVREQ, PRCVRSP, PSNDREQ, PSNDRSP, NINTRNI, NERRNI, and PCLKSTB.

Table 11.8: NIBus AC Specifications *(Over recommended operating conditions.)*

Symbol	Parameter	Min	Max	Units	Figure
f_{NICLK}	CLKNI frequency.	0	66.7	MHz	-
T_{PER}	CLKNI period.	15	-	nS	11.1
t_R	CLKNI rise time	300	1200	pS	11.1
t_F	CLKNI fall time	300	1200	pS	11.1
t_{PW}	CLKNI pulse width	6	-	nS	11.1
t_{SU}	NIBus input setup time	4	-	nS	11.2
t_{HLD}	NIBus input hold time	0.5	-	nS	11.2
t_{CKO}	NIBus clock to output delay	2.0	8.5	nS	11.3
t_R	NIBus output rise time	500	1500	pS	11.1
t_F	NIBus output fall time	500	1500	pS	11.1
t_{HIZ}	NIBus clock to output hi-Z	2.0	12.0	ns	11.4

Table 11.9 gives the timing specifications for the SCI LVDS links. The input CLKHI is GTL level and is used to generate the internal SCI clock.

The SCI inputs include PSCIDI[0:15], PSCISI, and PSCIFI.

The SCI outputs include PSCIDO[0:15], PSCISO, and PSCIFO.

Table 11.9: SCI Link AC Specifications *(Over recommended operating conditions.)*

Symbol	Parameter	Min	Max	Units	Figure
f_{CLKHI}	CLKHI frequency	99.5	100.5	MHz	-
T_{JCLKHI}	CLKHI jitter tolerance	-	100	pS	-
t_R	CLKHI rise time	300	1200	pS	11.1
t_F	CLKHI fall time	300	1200	pS	11.1
t_{DC}	CLKHI duty cycle	40	60	%	-
t_R	SCI output rise time	300	500	pS	11.1
t_F	SCI output fall time	300	500	pS	11.1
t_{OSKEW}	SCI output differential skew	-	50	pS	-
t_{OSKEW}	SCI output to output skew	-	100	pS	-
t_{OSKEW}	SCI output pulse distortion	-	200	pS	-
t_R	SCI input rise time	300	800	pS	11.1
t_F	SCI input fall time	300	800	pS	11.1
t_{ISKEW}	SCI input to input skew	-	500	pS	-
t_{CKO}	PSCISO to PSCIDO delay	1800	2200	ps	11.3

Table 11.10 gives the timing values for relevant signals during TAP testing and internal scan mode testing.

For TAP test mode, the relevant inputs have TTL levels and are the clock PTCK, mode select PTMS, NTRST, and data in PTDI. The relevant output has TTL levels and is data out PTDO.

The relevant output is TTL level, PTDO

Table 11.10: .Test Mode AC Specifications Over recommended operating conditions.

Symbol	Parameter	Min	Max	Units	Figure
f_{TSTCK}	PTCK, CLKNI, CLKHI, input frequency	0	25	MHz	-
T_{TSTCK}	PTCK input period	40	-	nS	11.1
t_R	Input PTCK rise time	2	8	nS	11.1
t_F	Input PTCK fall time	2	8	nS	11.1
t_{PW}	PTCK input pulse width	15	-	nS	11.1
t_{SU}	Scan control and data inputs setup time to PTCK	10	-	nS	11.2
t_{HLD}	Scan control and data inputs hold time from TCK	2	-	nS	11.2
t_{CKO}	Scan data clock to output delay during test	2	8	nS	11.3

Figure 11.1 : Period, Pulse Width, Rise, and Fall Time Definitions

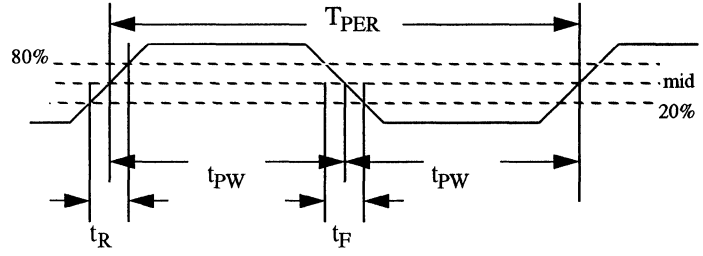


Figure 11.2: Setup and Hold Time Definitions

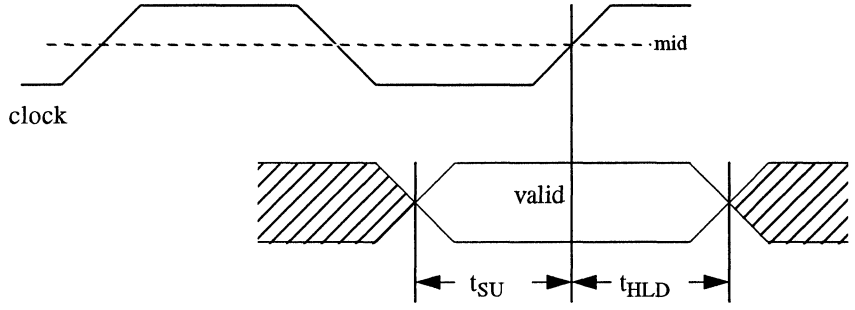
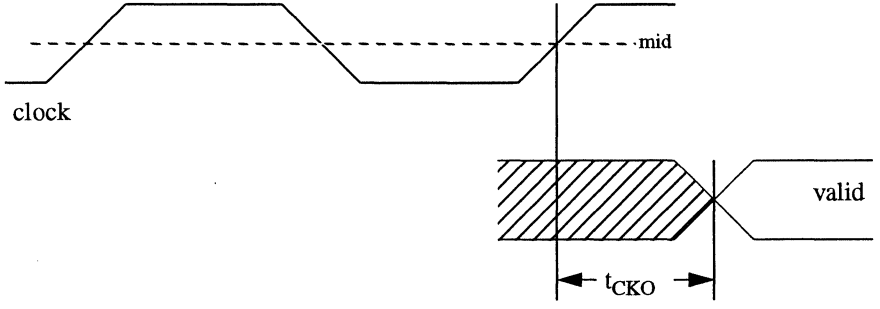


Figure 11.3 : Clock to Output Definition



12.0 Package Pin Description *[No Pin at Locations A01, L01 and L21]*

Package Pin Number	Signal Name	Package Pin Number	Signal Name	Package Pin Number	Signal Name
A02	PDATA57	B17	PDATA28	D11	VMM
A03	PDATA55	B18	VCC	D12	VMM
A04	PDATA54	B19	PDATA25	D13	PDATA35
A05	PDATA50	B20	PDATA23	D14	PDATA31
A06	VCC	B21	VCC	D15	PDATA27
A07	PPARITY5	C01	VCC	D16	PPARITY2
A08	PDATA46	C02	PPARITY7	D17	VMM
A09	PDATA44	C03	PDATA63	D18	VCC
A10	PDATA43	C04	PDATA62	D19	NSCIDI0
A11	VCC	C05	PDATA59	D20	PSCIDI1
A12	PDATA40	C06	VMM	D21	VCC
A13	PPARITY4	C07	VCC	E01	NSCIDO9
A14	PDATA38	C08	VMM	E02	PSCIDO13
A15	PDATA36	C09	VMM	E03	PSCIDO15
A16	VCC	C10	VCC	E04	VMM
A17	PDATA33	C11	PDATA42	E18	VMM
A18	PDATA30	C12	VCC	E19	PSCIDI0
A19	PDATA29	C13	VMM	E20	PSCIDI2
A20	PDATA26	C14	VMM	E21	NSCIDI4
A21	VCC	C15	VCC	F01	NSCIDO12
B01	VCC	C16	VMM	F02	PSCIDO14
B02	PDATA61	C17	PDATA24	F03	NSCIDO11
B03	PDATA58	C18	PDATA22	F04	VCC
B04	VCC	C19	PDATA21	F18	VCC
B05	PPARITY6	C20	PDATA20	F19	NSCIDI1
B06	PDATA52	C21	VCC	F20	PSCIDI3
B07	PDATA51	D01	VCC	F21	NSCISI
B08	PDATA49	D02	PSCIDO11	G01	PSCIDO12
B09	PDATA47	D03	NSCIDO15	G02	PSCIDO9
B10	PDATA45	D04	VCC	G03	NSCIDO14
B11	PDATA41	D05	VMM	G04	NSCIDO13
B12	PDATA39	D06	PDATA60	G18	NSCIDI2
B13	PDATA37	D07	PDATA56	G19	NSCIDI3
B14	PDATA34	D08	PDATA53	G20	PSCIDI4
B15	PDATA32	D09	PDATA48	G21	PSCISI
B16	PPARITY3	D10	VMM	H01	NSCISO

Package Pin Number	Signal Name	Package Pin Number	Signal Name	Package Pin Number	Signal Name
H02	NSCIDO8	N02	NSCIDO3	U21	PSCIDI15
H03	VCC	N03	PSCIDO3	V01	VCC
H04	VCC	N04	NSCIDO4	V02	PCMND2
H18	VCC	N18	NSCIDI13	V03	NDPSEL
H19	VCC	N19	PSCIDI12	V04	VCC
H20	NSCIFI	N20	NSCIDI12	V05	VMM
H21	NSCIDI6	N21	NSCIDI11	V06	VGREF
J01	PSCISO	P01	PSCIDO2	V07	NINTRNI
J02	PSCIDO10	P02	PSCIDO4	V08	PPC1
J03	NSCIDO10	P03	VCC	V09	PDATA4
J04	PSCIDO8	P04	VCC	V10	VMM
J18	PSCIFI	P18	VCC	V11	VMM
J19	NSCIDI5	P19	VCC	V12	VMM
J20	PSCIDI5	P20	PSCIDI13	V13	PDATA17
J21	PSCIDI6	P21	PSCIDI11	V14	PTDO
K01	NSCIDO6	R01	NSCIDO0	V15	PSTEP
K02	PSCIFO	R02	NSCIDO1	V16	NTRST
K03	NSCIFO	R03	NSCRUB	V17	VTTL
K04	VCC	R04	NNIACK	V18	VCC
K18	VCC	R18	PSTOP	V19	TE
K19	NSCIDI7	R19	CLKHI	V20	N/C
K20	PSCIDI7	R20	NSCIDI15	V21	VCC
K21	NSCIDI8	R21	NSCIDI14	W01	VCC
L02	NSCIDO7	T01	PSCIDO0	W02	IPNC
L03	PSCIDO6	T02	NSYNCRQ	W03	OPNC
L04	VMM	T03	PCMND1	W04	NDPACK
L18	VMM	T04	VCC	W05	PRCVRSP
L19	NSCIDI9	T18	VCC	W06	VMM
L20	PSCIDI8	T19	PCKHMPY1	W07	VCC
M01	PSCIDO7	T20	NCLKHI	W08	VMM
M02	NSCIDO5	T21	PSCIDI14	W09	VMM
M03	PSCIDO5	U01	PSCIDO1	W10	VCC
M04	VCC	U02	NNIRDY	W11	PDATA11
M18	VCC	U03	PCMND0	W12	VCC
M19	PSCIDI10	U04	VMM	W13	VMM
M20	NSCIDI10	U18	VMM	W14	VMM
M21	PSCIDI9	U19	PCKHMPY0	W15	VCC
N01	NSCIDO2	U20	NRESET	W16	VTTL

Package Pin Number	Signal Name	Package Pin Number	Signal Name	Package Pin Number	Signal Name
W17	PTCK	Y12	PDATA14	AA07	PDATA5
W18	PMAINTMD1	Y13	PPARITY1	AA08	PDATA7
W19	CLKNI	Y14	PDATA18	AA09	PDATA8
W20	N/C	Y15	N/C	AA10	PDATA9
W21	VCC	Y16	PDIV10OUT	AA11	VCC
Y01	VCC	Y17	PTSTMD	AA12	PDATA12
Y02	PRCVREQ	Y18	VCC	AA13	PDATA13
Y03	PSNDREQ	Y19	PTMS	AA14	PDATA15
Y04	VCC	Y20	PMAINTMD0	AA15	PDATA16
Y05	NERRNI	Y21	VCC	AA16	VCC
Y06	PDATA0	AA01	VCC	AA17	PDATA19
Y07	PDATA1	AA02	PSNDRSP	AA18	PCKHSEL
Y08	PDATA3	AA03	PCLKSTB	AA19	PCLK250
Y09	PDATA6	AA04	PPC0	AA20	PTDI
Y10	PPARITY0	AA05	PDATA2	AA21	VCC
Y11	PDATA10	AA06	VCC		

13.0 Signal Pin Description

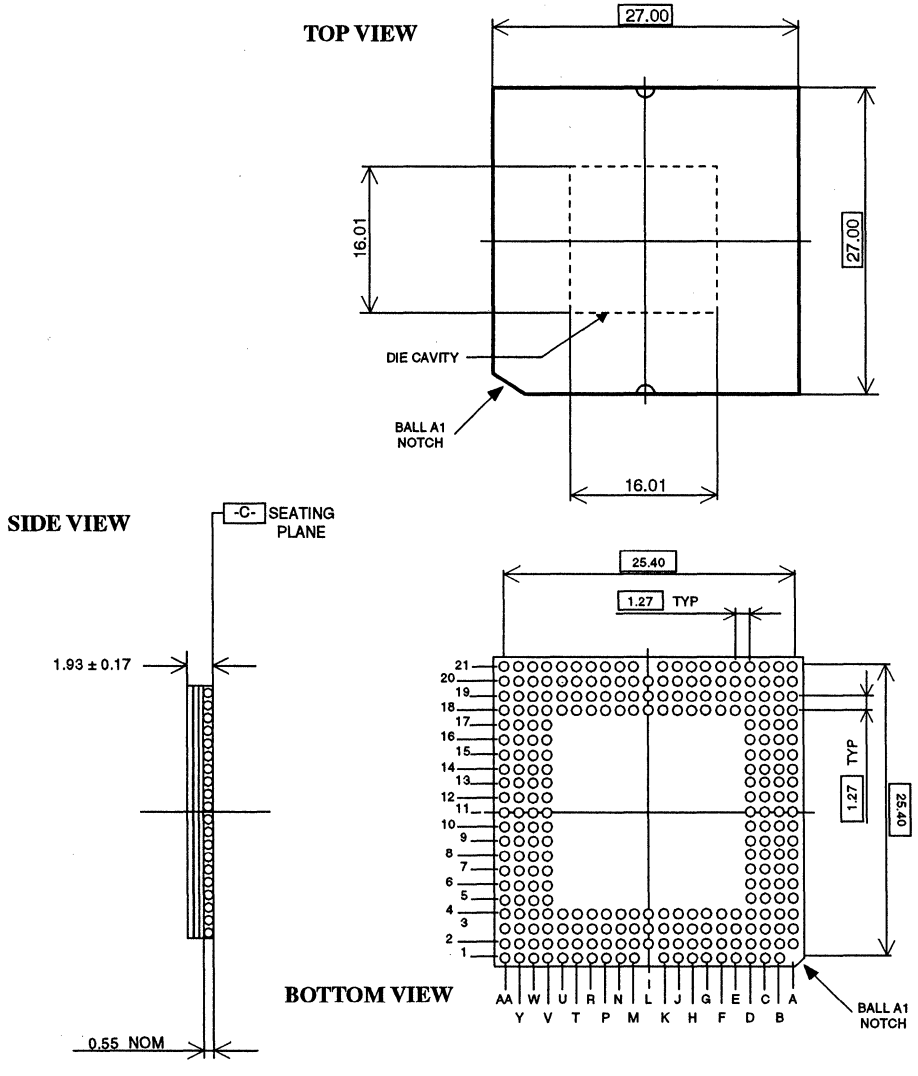
Signal Name	Package Pin Number	Signal Name	Package Pin Number	Signal Name	Package Pin Number
CLKHI	R19	NSCIDO14	G03	PDATA18	Y14
CLKNI	W19	NSCIDO15	D03	PDATA19	AA17
IPNC	W02	NSCIDO2	N01	PDATA2	AA05
N/C	V20	NSCIDO3	N02	PDATA20	C20
N/C	W20	NSCIDO4	N04	PDATA21	C19
N/C	Y15	NSCIDO5	M02	PDATA22	C18
NCLKHI	T20	NSCIDO6	K01	PDATA23	B20
NDPACK	W04	NSCIDO7	L02	PDATA24	C17
NDPSEL	V03	NSCIDO8	H02	PDATA25	B19
NERRNI	Y05	NSCIDO9	E01	PDATA26	A20
NINTRNI	V07	NSCIFI	H20	PDATA27	D15
NNIACK	R04	NSCIFO	K03	PDATA28	B17
NNIRDY	U02	NSCISI	F21	PDATA29	A19
NRESET	U20	NSCISO	H01	PDATA3	Y08
NSCIDI0	D19	NSCRUB	R03	PDATA30	A18
NSCIDI1	F19	NSYNCRQ	T02	PDATA31	D14
NSCIDI10	M20	NTRST	V16	PDATA32	B15
NSCIDI11	N21	OPNC	W03	PDATA33	A17
NSCIDI12	N20	PCKHMPY0	U19	PDATA34	B14
NSCIDI13	N18	PCKHMPY1	T19	PDATA35	D13
NSCIDI14	R21	PCKHSEL	AA18	PDATA36	A15
NSCIDI15	R20	PCLK250	AA19	PDATA37	B13
NSCIDI2	G18	PCLKSTB	AA03	PDATA38	A14
NSCIDI3	G19	PCMND0	U03	PDATA39	B12
NSCIDI4	E21	PCMND1	T03	PDATA4	V09
NSCIDI5	J19	PCMND2	V02	PDATA40	A12
NSCIDI6	H21	PDATA0	Y06	PDATA41	B11
NSCIDI7	K19	PDATA1	Y07	PDATA42	C11
NSCIDI8	K21	PDATA10	Y11	PDATA43	A10
NSCIDI9	L19	PDATA11	W11	PDATA44	A09
NSCIDO0	R01	PDATA12	AA12	PDATA45	B10
NSCIDO1	R02	PDATA13	AA13	PDATA46	A08
NSCIDO10	J03	PDATA14	Y12	PDATA47	B09
NSCIDO11	F03	PDATA15	AA14	PDATA48	D09
NSCIDO12	F01	PDATA16	AA15	PDATA49	B08
NSCIDO13	G04	PDATA17	V13	PDATA5	AA07

Signal Name	Package Pin Number	Signal Name	Package Pin Number	Signal Name	Package Pin Number
PDATA50	A05	PSCIDI15	U21	TE	V19
PDATA51	B07	PSCIDI2	E20	VCC	A06
PDATA54	A04	PSCIDI3	F20	VCC	A11
PDATA55	A03	PSCIDI4	G20	VCC	A16
PDATA56	D07	PSCIDI5	J20	VCC	A21
PDATA57	A02	PSCIDI6	J21	VCC	B01
PDATA58	B03	PSCIDI7	K20	VCC	B04
PDATA59	C05	PSCIDI8	L20	VCC	B18
PDATA6	Y09	PSCIDI9	M21	VCC	B21
PDATA60	D06	PSCIDO0	T01	VCC	C01
PDATA61	B02	PSCIDO1	U01	VCC	C07
PDATA62	C04	PSCIDO10	J02	VCC	C10
PDATA63	C03	PSCIDO11	D02	VCC	C12
PDATA7	AA08	PSCIDO12	G01	VCC	C15
PDATA8	AA09	PSCIDO13	E02	VCC	C21
PDATA9	AA10	PSCIDO14	F02	VCC	D01
PDIV10OUT	Y16	PSCIDO15	E03	VCC	D04
PMAINTMD0	Y20	PSCIDO2	P01	VCC	D18
PMAINTMD1	W18	PSCIDO3	N03	VCC	D21
PPARITY0	Y10	PSCIDO4	P02	VCC	F04
PPARITY1	Y13	PSCIDO5	M03	VCC	F18
PPARITY2	D16	PSCIDO6	L03	VCC	H03
PPARITY3	B16	PSCIDO7	M01	VCC	H04
PPARITY4	A13	PSCIDO8	J04	VCC	H18
PPARITY5	A07	PSCIDO9	G02	VCC	H19
PPARITY6	B05	PSCIFI	J18	VCC	K04
PPARITY7	C02	PSCIFO	K02	VCC	K18
PPC0	AA04	PSCISI	G21	VCC	M04
PPC1	V08	PSCISO	J01	VCC	M18
PRCVREQ	Y02	PSNDREQ	Y03	VCC	P03
PRCVRSP	W05	PSNDRSP	AA02	VCC	P04
PSCIDI0	E19	PSTEP	V15	VCC	P18
PSCIDI1	D20	PSTOP	R18	VCC	P19
PSCIDI10	M19	PTCK	W17	VCC	T04
PSCIDI11	P21	PTDI	AA20	VCC	T18
PSCIDI12	N19	PTDO	V14	VCC	V01
PSCIDI13	P20	PTMS	Y19	VCC	V04
PSCIDI14	T21	PTSTMD	Y17	VCC	V18

Signal Name	Package Pin Number	Signal Name	Package Pin Number	Signal Name	Package Pin Number
VCC	V21	VCC	AA21	VMM	L04
VCC	W01	VGREF	V06	VMM	L18
VCC	W07	VMM	C06	VMM	U04
VCC	W10	VMM	C08	VMM	U18
VCC	W12	VMM	C09	VMM	V05
VCC	W15	VMM	C13	VMM	V10
VCC	W21	VMM	C14	VMM	V11
VCC	Y01	VMM	C16	VMM	V12
VCC	Y04	VMM	D05	VMM	W06
VCC	Y18	VMM	D10	VMM	W08
VCC	Y21	VMM	D11	VMM	W09
VCC	AA01	VMM	D12	VMM	W13
VCC	AA06	VMM	D17	VMM	W14
VCC	AA11	VMM	E04	VTTL	V17
VCC	AA16	VMM	E18	VTTL	W16

14.0 Mechanical Specifications

14.1 Package Information 269 BGA - 50 mil centers



15.0 Thermal Specifications

The VSC7201A requires a heatsink and substantial airflow for most applications. The thermal resistance from junction to case (θ jc) is 1.2°C/W. With a P_{DMAX} of 27W and a targeted junction temperature of 110°C, the case temperature should be kept under 75°C (Approximately 100°C - 28W *1.2°C/W).

16.0 Ordering Information

The part number for this product is formed by a combination of the device number and the package style:

VSC7201A TL

Device Type:

VSC7201A: SCI DataPump

Package Style:

TL: 269 pin BGA; 27mm Body

Notice

This document contains information on products that are in the preproduction phase of development. The information contained in this document is based on test results and initial product characterization. Characteristic data and other specifications are subject to change without notice. Therefore, the reader is cautioned to confirm that this datasheet is current prior to placing orders.

Warning

Vitesse Semiconductor Corporation's products are not intended for use in life support appliances, devices or systems. Use of a Vitesse product in such applications without the written consent of the appropriate Vitesse officer is prohibited.

Preliminary Data Sheet

1 GByte/sec SCI Compliant Switch Node Bypass Circuit

Features

- 2-port Switch Capable of Passing SCI Packets
- Multiplexers Allow Bypassing Around any Port for Faulty Node Isolation.
- Sends and Receives SCI Symbols Every 2 ns for 1 GB/s Data Rate Per Port.
- One Port Conforms to Low Voltage Differential Signalling (LVDS) Standard (IEEE Std. 1596.3)
- +3.3V and +2V Power Supplies
- 301 BGA Package (50 mil spacing, 27mm/side)
- IEEE Std 1149.1 Test Access Port for Diagnostics and Boundary Scan

Introduction

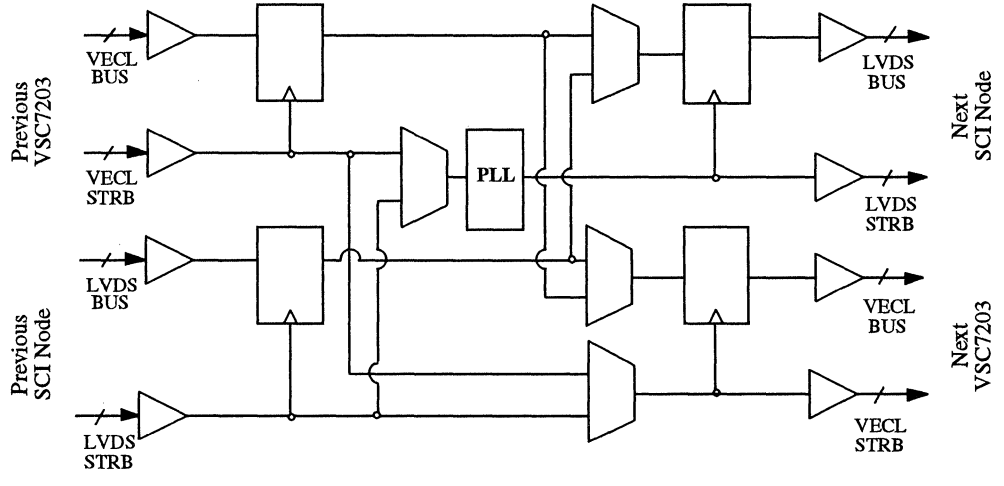
This Node Bypass circuit is intended to serve the purpose of isolation of SCI nodes. Multiple copies of this circuit would be interposed in a SCI ringlet, as required, and in normal operation pass SCI packets from one node to another while introducing minimum latency.

A faulty node can be electronically bypassed by assertion of the proper control signals.

The LVDS input and output busses are intended to connect SCI nodes controlled by VSC7201A "Data Pump" circuits. The other input and output busses use level-shifted ECL signaling (VECL) and are intended to connect to other VSC7203 Node Bypass circuits.

The node bypass circuit uses the input strobe for each input port as the source for the clock driving the two register pipeline to the selected output port. An internal 1 GHz PLL regenerates the selected input clock phase so that an unlimited number of circuits can be interconnected.

VSC7203 Functional Block Diagram



Functional Description

The node bypass circuit is a switch that has two basic modes of operation: NORMAL and BYPASS mode. In NORMAL mode, SCI packets are transmitted from the SCI node to a node bypass circuit and from a node bypass circuit to the SCI node. In BYPASS mode, SCI packets are transmitted from node bypass circuit to node bypass circuit. While in BYPASS mode, SCI packets may be sent to an SCI node, to the node bypass circuit, and back to the same SCI node for diagnostic checking without interfering with ringlet operation.

The node bypass circuit also has two modes which control clock generation through the PLL, HALFSPD and CLKSEL. The HALFSPD bit, when set high, allows the node bypass circuit to be run at 500MB/s instead of 1GB/s. This operation allows the chip to be compatible with a broader range of SCI systems. Whether in full speed or half speed mode, the LVDS BUS is two bytes wide and the VECL BUS is four bytes wide. The CLKSEL allows the user to bypass the internally generated PLL clock and use an external clock, TSTCLK, to control the LVDS STRB output. When bypassing the PLL, the externally supplied clock should be set at 500MHz regardless of the speed mode chosen.

It should be noted when the PLL output clock is being selected that, to ensure proper operation, the VECL STRB or LVDS STRB must be supplied to the node bypass circuit uninterrupted. Periodic interruption of the strobe signal to the PLL will cause the PLL to lose frequency lock and result in improper circuit operation.

The truth table in Table 1 details the operation of the node bypass circuit. LDATA represents data that is coming from the SCI node, and VDATA represents data that is coming from another node bypass circuit. PLL OUT represents an LVDS STRB generated by the PLL, and TSTCLK represents an LVDS STRB generated by the externally supplied clock. Finally, LSTRB represents a strobe signal from the SCI node, and VSTRB represents a strobe signal from another node bypass circuit.

Table 1: Truth Table

Control Inputs			*Data Outputs*				
HALFSPD	*BYPASS*	*CLKSEL*	*LVDS BUS*	*LVDS STRB*	*VECL BUS*	*VECL STRB*	*STRB SPEED*
0	0	0	VDATA	PLL OUT	LDATA	LSTRB	250MHz
1	0	0	VDATA	PLL OUT	LDATA	LSTRB	125MHz
0	1	0	LDATA	PLL OUT	VDATA	VSTRB	250MHz
1	1	0	LDATA	PLL OUT	VDATA	VSTRB	125MHz
0	0	1	VDATA	TSTCLK/2	LDATA	LSTRB	250MHz
1	0	1	VDATA	TSTCLK/4	LDATA	LSTRB	125MHz
0	1	1	LDATA	TSTCLK/2	VDATA	VSTRB	250MHz
1	1	1	LDATA	TSTCLK/4	VDATA	VSTRB	125MHz

Figure 1: Vitesse SCI Chipset, Typical Four Node Application using VSC7201A and VSC7203

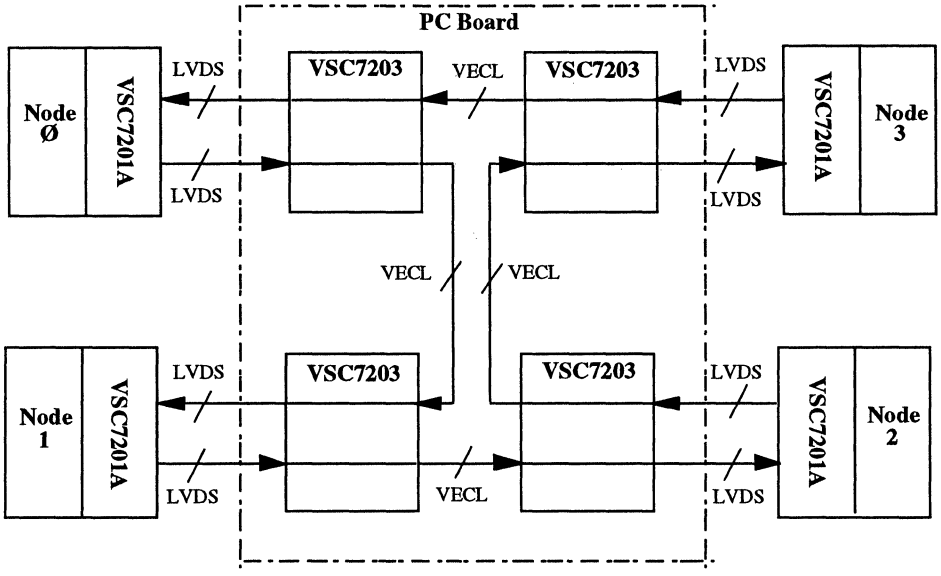


Figure 1 illustrates a typical application using the VSC7203. A 4 node ringlet is shown interconnected using VSC7203 Node Bypass Circuits. For example, in a multi-processor application, if each node contains 4 processors this configuration results in a 16 processor system. Of course this approach can be extended to a larger number by inserting additional nodes in the VECL path.

JTAG

The DataPump conforms to the IEEE Std 1149.1 Standard Test Access Port and Boundary Scan Architecture. This allows access to all the inputs and outputs of the VSC7203.

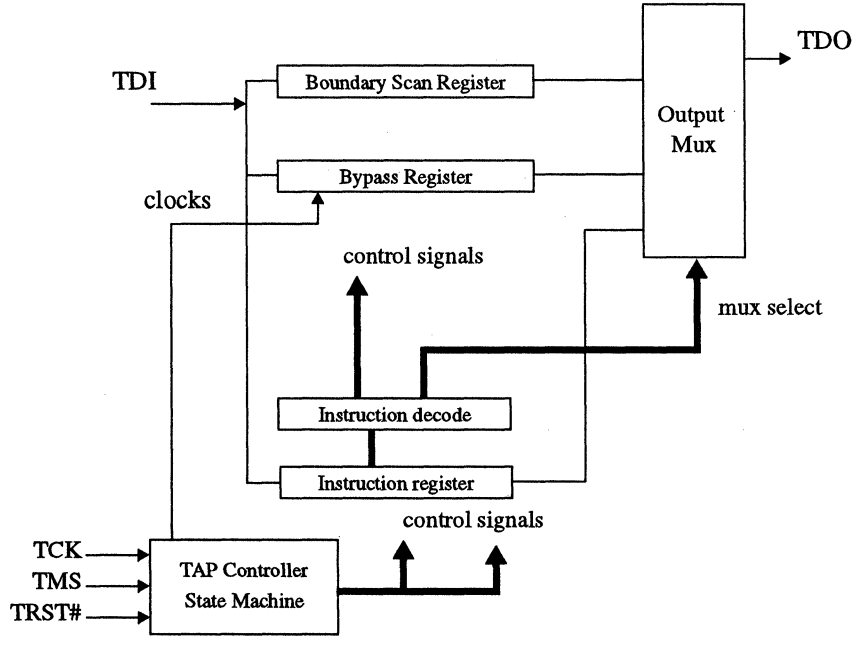
The Test Access Port uses the pins TCK, TMS, TRST, TDI, and TDO to perform serial shifting of data and control for testing the VSC7203.

A block diagram of the various scan chains accessible through JTAG is shown in Figure 2.

These registers operate like dual rank registers. That is, they have a shift register part and a parallel loading register part. In the case of boundary scan, the dual rank register is specified by the IEEE std.

The instruction register is a dual rank register made up of the shift register and a parallel load register. The outputs of the parallel load register actually provide the instruction data.

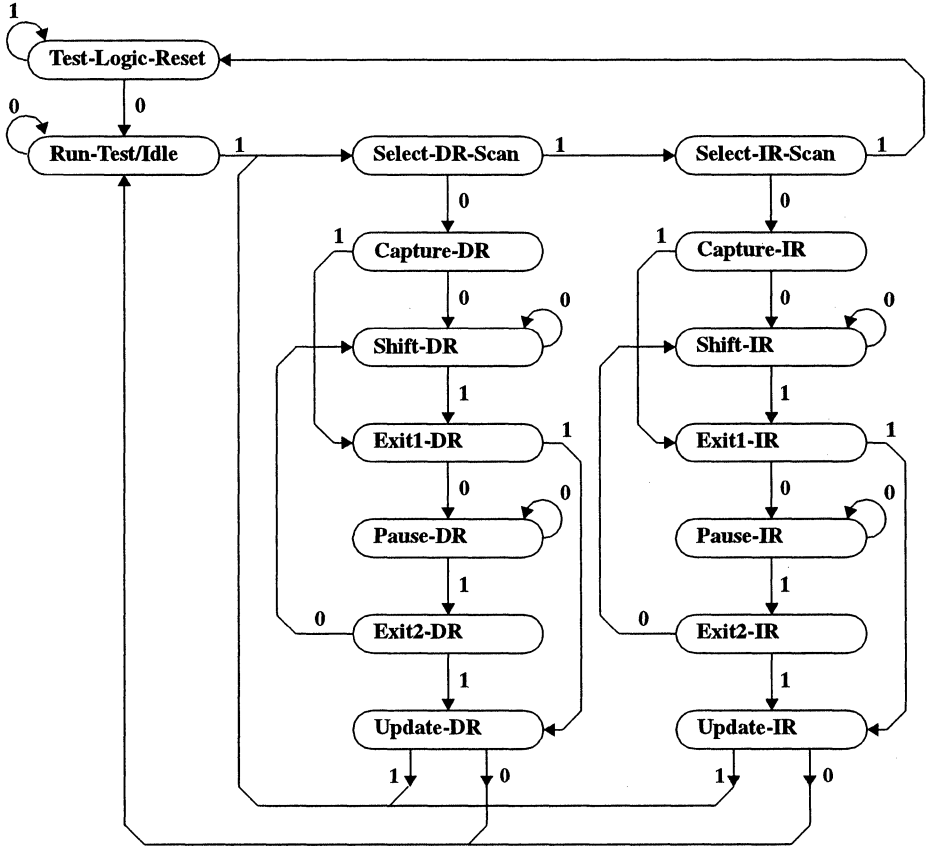
Figure 2: Scan Test Access Port Block Diagram



TAP Controller State Machine

The TAP controller state machine is clocked by TCK and controlled by TMS. It is asynchronously reset by TRST. Figure 3 shows the TAP controller state diagram. The TAP controller conforms to the specifications set forth in IEEE Std. 1149.1.

Figure 3: Test Access Port State Diagram



Note: The value (0 or 1) shown adjacent to each state transition represents the value of TMS sampled on the rising edge of TCK.

TAP Controller Instructions

Instructions are shifted into the instruction register using the IR (instruction register) state machine operations. The instructions supported include TAP mandatory BYPASS, SAMPLE/PRELOAD, and EXTEST. The instruction register is 8-bits long and each instruction code (inst[0:7] is given in hex form in Table 2. The shift order for inst[0:7] is inst0 to inst7. The basic instructions are listed in Table 2.

Table 2: TAP Controller Instructions

Instruction	*inst [7:0]*	*Description*
EXTEST	00_h	Provides external pin and board testing.
SAMPLE/ PRELOAD	$C0_h$	Allows sampling inputs and preloading outputs without affecting normal operation.
BYPASS	FF_h	Connects TDI to bypass register to TDO.

BYPASS Instruction

The BYPASS instruction selects the single stage BYPASS shift register to be connected between TDI and TDO. This allows for a minimum delay shift path through the VSC7203 in the Shift-DR state. Capture-DR and Update-DR have no effect during this instruction. Execution of this instruction does not affect normal VSC7203 operation.

EXTEST Instruction

The EXTEST instruction allows testing of off-chip connections to the I/O and PC-board interconnections. Data at the input pins is captured in the boundary scan shift register in the Capture-DR state. Data is shifted in the boundary scan shift register in the Shift-DR state. The boundary scan output registers are parallel loaded and the outputs of the DataPump driven on the rising edge of TCK in the Update-DR state.

Boundary Scan Register and Ordering

The boundary scan register consists of a bit for each I/O plus an extra bit which controls the capturing of output data by the boundary scan shift register during SAMPLE/PRELOAD. This bit is called ORCAPT. Table 3 on the following page gives the boundary scan ordering.

SAMPLE/PRELOAD Instruction

During SAMPLE/PRELOAD, inputs are registered into the boundary scan shift register in the Capture-DR state. When the ORCAPT bit is high (enabled), the outputs are registered into the boundary scan shift register as well. Otherwise, the boundary scan shift register does not load the output values when ORCAPT is low. Data is shifted in the boundary scan shift register in the Shift-DR state. The boundary scan output registers are parallel loaded and the outputs of the VSC7203 are driven on the rising edge of TCK on the Update-DR state.

Table 3: Boundary Scan Chain Ordering

Name	*Type*	*Position in B.S. Chain*
ORCAPT	internal	1
BYPASS	input	2
PSCISO	diff. output	3
PSCIFO	diff. output	4
PSCIDO[15:0]	diff. output	5-20
PSCISI	diff. input	21
PSCIFI	diff. input	22
PSCIDI[15:0]	diff. input	23-38
POCLK	diff. output	39
OFLAG[1:0]	output	40-41
ODATA[31:0]	output	42-73
PINCLK	diff. input	74
FLAG[1:0]	input	75, 76
DATA[31:0]	input	77-108

AC Characteristics

Table 4: VECL Port Specifications *(Over recommended operating conditions).*

Symbol	Parameter	Min	Max	Units
T_{PER}	INCLK period - full speed	4	-	ns
T_{PER}	INCLK period - half speed	8	-	ns
t_R	VECL input rise time	TBD	-	ps
t_F	VECL input fall time	TBD	-	ps
t_{PW}	INCLK pulse width - full speed	1.5	-	ns
t_{PW}	INCLK pulse-width - half speed	3	-	ns
t_{SU}	VECL input bus setup time	-0.40	-	ns
t_H	VECL input bus hold time	1.75	-	ns
t_{CK}	VECL clock to VECL output delay	TBD	-	ns
t_{CK}	LVDS clock to VECL output delay	.95	3.3	ns
t_R	VECL output rise time	TBD		
t_F	VECL output fall time	TBD		

Table 5: LVDS Port Specifications *(Over recommended operating conditions).*

Symbol	Parameter	Min	Max	Units
t_{R4}	LVDS output rise time	300	500	ps
t_{F4}	LVDS output fall time	300	500	ps
t_{OSKEW1}	LVDS output differential skew	-	50	ps
t_{OSKEW2}	LVDS output to output skew	-	100	ps
t_{OSKEW3}	LVDS output pulse distortion	-	200	ps
t_{R5}	LVDS input rise time	300	800	ps
t_{F5}	LVDS input fall time	300	800	ps
t_{ISKEW1}	LVDS input to input skew	-	500	ps
t_{CKO2}	PSCISO to PSCIDO and PSCIFO delay	1800	2200	ps

AC Timing Waveforms

Figure 4: Period, Pulse Width, Rise, and Fall Time Definitions

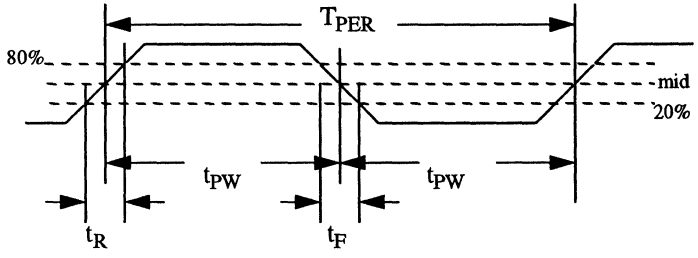
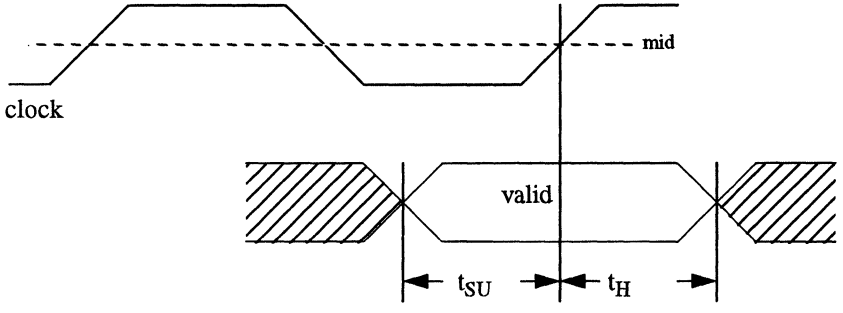


Figure 5: Setup and Hold Time Definitions



DC Characteristics

Table 6: Power Dissipation *(Over recommended operating conditions. VECL output open circuit, LVDS outputs terminated with 100 ohms.)*

Symbol	Parameter	Min	Typ	Max	Units
I_{MM}	Power supply current from V_{MM}	-	-	2.43	A
I_{TTL}	Power supply current from V_{TTL}	-	-	0.26	A
Pd	Total Power Dissipation	-	-	6.5	W

Table 7: TTL Input/Output *(Over recommended operating conditions.)*

Symbol	Parameter	Min	Typ	Max	Units
V_{OH}	Output high, I_{OH} = -2.4 mA	2.4	-	-	V
V_{OL}	Output low, I_{OL} = 8 mA	-	-	0.4	V
V_{IH}	Input high voltage [Not 5V tolerant]	2.0	-	V_{TTL} + 1.0	V
V_{IL}	Input low voltage	- 1.0	-	0.8	V
I_{IH}	Input high current, V_{IN} = 2.4 V	-	-	50	uA
I_{IL}	Input low current, V_{IN} = 0.4 V	1000	-	-	uA

Table 8: VECL Input/Output *(Over recommended operating conditions. Termination resistance = 50 ohms.)*

Symbol	Parameter	Min	Typ	Max	Units
V_{TT}	Termination voltage	-0.1	0	0.1	V
V_{OL}	Output low	0	-	0.38	V
V_{OH}	Output high	0.98	-	1.3	V
V_{IH}	Input high voltage	0.9	-	1.3	V
V_{IL}	Input low voltage	0	-	0.46	V
I_{IL}	Input low leakage current	-50	-	-	µA
I_{IH}	Input high leakage current	-	-	200	µA

Table 9: LVDS Output Driver *(Over recommended operating conditions.)*

Symbol	*Parameter*	*Conditions*	*Min*	*Max*	*Units*
V_{OH}	Output voltage high	Rload = 100 ohms	1250	1475	mV
V_{OL}	Output voltage low	Rload = 100 ohms	925	1150	mV
V_{OD}	Output differential voltage	Rload = 100 ohms	250	400	mV
V_{OS}	Output offset voltage	Rload = 100 ohms	1125	1275	mV
dV_{OD}	Change in differential voltage between complementary states.	Rload = 100 ohms	-	25	mV
dV_{OS}	Change in offset voltage between complementary states.	Rload = 100 ohms	-	25	mV
R_O	Output impedance	Iload = 2 to 2.5 mA	40	60	ohms
dR_O	Ro mismatch between	Iload = 2 to 2.5 mA	-	10	%

Table 10: LVDS Input Receiver *(Over recommended operating conditions.)*

Symbol	*Parameter*	*Conditions*	*Min*	*Max*	*Units*
V_{IH}	Input voltage high	V_{ID}= 100mV	100	2200	mV
V_{IL}	Input voltage low	V_{ID}= 100mV	0	2100	mV
+/- V_{ID}	Input differential voltage		100	500	mV
V_{ICM}	Input voltage common mode	V_{ID}= V_{IDMIN}	50	2150	mV
		V_{ID}= V_{IDMAX}	250	1950	
R_{IN}	Input impedance	$0 < V_{IN} < 2.4V$	80	120	ohm

Absolute Maximum Ratings

Symbol	Rating	Limit
V_{MM}	+2 V power supply voltage	-0.5 to 2.6 V
V_{TTL}	+3.3 V power supply voltage	-0.5 to 4.0 V
Vin	Any pad voltage except LVDS outputs	-1.0 to V_{TTL} + 1.0 V
Vin	LVDS output voltage	-1.0 to V_{DD} + 1.0 V
I_{OUTT}	TTL output short circuit current	-50mA
Tc	Case temperature under bias	-55°C to +125°C
Tstg	Storage temperature	-65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{MM}	+2 V power supply voltage	1.9	2.0	2.1	V
V_{TTL}	+3.3 V power supply voltage	3.1	3.3	3.5	V
Tc	Operating case temperature	0	-	75	°C

Notes:

1) *CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.*
2) *Vitesse guarantees the functional and parametric operation of the part under "Recommended Operating Conditions" except where specifically noted in the AC and DC Parametric Tables*

Package Pin Description

Signal	Type	Level	#Pins	Description
VSCIPNC	Input	ECL	1	Factory Test. Tie to V_{CC}
VSCOPNC	Output	ECL	1	Factory Test. Do not connect.
PSCIDI[15:0], NSCIDI[15:0]	Input	LVDS	32	SCI Link Data Bus, Complementary Pairs
PSCISI, NSCISI	Input	LVDS	2	SCI Link Strobe Input, Complementary Pairs
PSCIFI, NSCIFI	Input	LVDS	2	SCI Link Flag Input, Complementary Pairs
PSCIDO[15:0], NSCIDO[15:0]	Output	LVDS	32	SCI Link Data Bus, Complementary Pairs
PSCISO, NSCISO	Output	LVDS	2	SCI Link Strobe Output, Complementary Pairs
PSCIFO, NSCIFO	Output	LVDS	2	SCI Link Flag Output, Complementary Pairs
DATA[31:0]	Input	VECL	32	Port Input Data Bus
FLAG[1:0]	Input	VECL	2	Port Input Flag Bits
PINCLK, NINCLK	Input	VECL	2	Port Input Clock, Complementary Pairs
ODATA[31:0]	Output	VECL	32	Port Output Data Bus
OFLAG[1:0]	Output	VECL	2	Port Output Flag Bits
POCLK, NOCLK	Output	VECL	2	Port Output Clock, Complementary Pairs
CLKSEL	Input	VECL	1	Bypass PLL Selection Input
TSTCLK	Input	VECL	1	External Clock Input
HALFSPD	Input	VECL	1	Speed Selection
RESET	Input	TTL	1	Chip Reset Input
TMS	Input	TTL	1	JTAG Mode Select Input
TRST	Input	TTL	1	JTAG Reset, Active Low, Input
TDI	Input	TTL	1	JTAG Scan Input
TDO	Input	TTL	1	JTAG Scan Output
TCK	Input	TTL	1	JTAG Clock Input
BYPASS	Input	TTL	1	Chip Mode Select Input
VSCTE	Input	TTL	1	Factory Test. Tie to V_{CC}
VMM		Power	78	+2V Power Supply
VTTL		Power	4	+3.3V Power Supply (for TTL)
VCC		Ground	27	Ground
INC			31	Internally connected to an unused pad. Do not connect.
N/C			4	Not Connected

Package Pinout [by Pin Number]

Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name
A02	CLKSEL	AA17	VMM	C11	ODATA14
A03	INC	AA18	PSCIDO2	C12	VMM
A04	ODATA0	AA19	NSCIDO3	C13	ODATA18
A05	VMM	AA20	NSCIDO0	C14	ODATA22
A06	ODATA3	AA21	VMM	C15	ODATA23
A07	ODATA6	B01	INC	C16	VMM
A08	VMM	B02	TSTCLK	C17	ODATA27
A09	ODATA11	B03	VMM	C18	VMM
A10	ODATA12	B04	ODATA1	C19	ODATA31
A11	VMM	B05	ODATA2	C20	POCLK
A12	ODATA16	B06	ODATA4	C21	VMM
A13	ODATA20	B07	VMM	D01	NSCIDI15
A14	VMM	B08	ODATA7	D02	NSCIDI11
A15	ODATA24	B09	ODATA10	D03	PSCIDI11
A16	ODATA25	B10	ODATA13	D04	INC
A17	VMM	B11	ODATA15	D05	INC
A18	ODATA29	B12	ODATA17	D06	VCC
A19	OFLAG0	B13	ODATA19	D07	VCC
A20	OFLAG1	B14	ODATA21	D08	VCC
A21	VMM	B15	VMM	D09	VMM
AA01	VMM	B16	ODATA26	D10	VCC
AA02	INC	B17	ODATA28	D11	VMM
AA03	INC	B18	ODATA30	D12	VCC
AA04	NSCIDO15	B19	VMM	D13	VMM
AA05	VMM	B20	INC	D14	VCC
AA06	NSCIDO9	B21	NOCLK	D15	VCC
AA07	PSCIDO9	C01	VMM	D16	VCC
AA08	VMM	C02	INC	D17	INC
AA09	NSCIDO14	C03	HALFSPD	D18	INC
AA10	PSCIDO14	C04	VMM	D19	NINCLK
AA11	VMM	C05	INC	D20	PINCLK
AA12	NSCISO	C06	VMM	D21	FLAG1
AA13	PSCISO	C07	ODATA5	E01	VSCTE
AA14	VMM	C08	ODATA8	E02	VMM
AA15	NSCIDO6	C09	ODATA9	E03	PSCIDI15
AA16	PSCIDO6	C10	VMM	E04	NC

Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name
E05	VMM	H05	VCC	N03	VMM
E06	VTTL	H17	VCC	N04	PSCIDI2
E07	VTTL	H18	DATA3	N18	DATA14
E08	VMM	H19	DATA5	N19	VMM
E09	VMM	H20	DATA27	N20	DATA18
E10	VMM	H21	DATA28	N21	DATA22
E12	VMM	J01	PSCIDI10	P01	NSCIDI4
E13	VMM	J02	NSCIDI14	P02	NSCIDI2
E14	VMM	J03	VMM	P03	PSCIDI3
E15	VMM	J04	NSCIDI8	P04	NSCIDI3
E16	VMM	J18	DATA6	P05	VCC
E17	VMM	J19	VMM	P17	VCC
E18	NC	J20	DATA25	P18	DATA15
E19	DATA1	J21	DATA26	P19	DATA16
E20	VMM	K01	PSCIFI	P20	DATA20
E21	DATA31	K02	NSCISI	P21	DATA19
F01	NSCIDI13	K03	PSCISI	R01	VMM
F02	NSCIDI9	K04	NSCIDI10	R02	INC
F03	INC	K18	DATA7	R03	NSCIDI1
F04	VMM	K19	DATA11	R04	NSCIDI0
F05	VCC	K20	DATA8	R18	INC
F17	VCC	K21	DATA23	R19	INC
F18	VMM	L02	VCC	R20	DATA17
F19	DATA0	L03	NSCIFI	R21	VMM
F20	DATA30	L04	PSCIDI7	T01	PSCIDI1
F21	FLAG0	L18	DATA10	T02	PSCIDI0
G01	VMM	L19	DATA9	T03	RESET
G02	INC	L20	VCC	T04	VMM
G03	PSCIDI13	M01	NSCIDI7	T05	VCC
G04	PSCIDI9	M02	PSCIDI6	T17	VCC
G18	DATA2	M03	NSCIDI6	T18	VMM
G19	DATA4	M04	PSCIDI5	T19	INC
G20	DATA29	M18	DATA13	T20	INC
G21	VMM	M19	DATA12	T21	INC
H01	PSCIDI14	M20	DATA21	U01	TCK
H02	PSCIDI8	M21	DATA24	U02	VMM
H03	NSCIDI12	N01	NSCIDI5	U03	TRST
H04	PSCIDI12	N02	PSCIDI4	U04	NC

Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name
U05	VCC	V12	VCC	W18	VMM
U06	VTTL	V13	VMM	W19	NSCIDO4
U07	VTTL	V14	VCC	W20	PSCIDO1
U08	VMM	V15	VCC	W21	VMM
U09	VMM	V16	VCC	Y01	INC
U10	VMM	V17	PSCIDO4	Y02	INC
U12	VMM	V18	INC	Y03	VMM
U13	VMM	V19	INC	Y04	NSCIDO11
U14	VMM	V20	INC	Y05	PSCIDO11
U15	VMM	V21	INC	Y06	INC
U16	VMM	W01	VMM	Y07	VMM
U17	VMM	W02	VSCOPNC	Y08	PSCIDO13
U18	NC	W03	TDO	Y09	PSCIDO12
U19	INC	W04	VMM	Y10	NSCIFO
U20	VMM	W05	INC	Y11	PSCIFO
U21	INC	W06	VMM	Y12	PSCIDO8
V01	TMS	W07	PSCIDO15	Y13	NSCIDO10
V02	TDI	W08	NSCIDO13	Y14	NSCIDO7
V03	BYPASS	W09	NSCIDO12	Y15	VMM
V04	VSCIPNC	W10	VMM	Y16	INC
V05	INC	W11	NSCIDO8	Y17	NSCIDO5
V06	VCC	W12	VMM	Y18	PSCIDO5
V07	VCC	W13	PSCIDO10	Y19	VMM
V08	VCC	W14	PSCIDO7	Y20	PSCIDO0
V09	VMM	W15	NSCIDO2	Y21	NSCIDO1
V10	VCC	W16	VMM		
V11	VMM	W17	PSCIDO3		

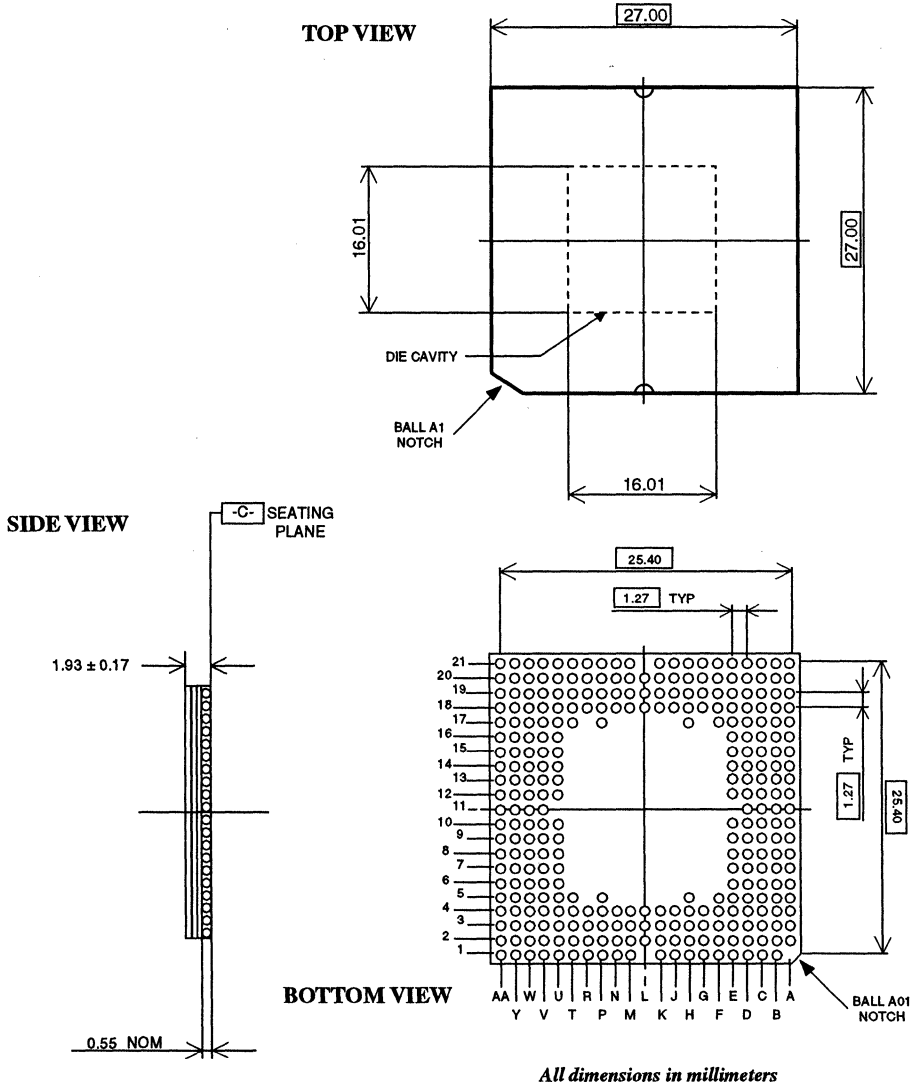
Package Pinout *[by Signal Name]*

Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number
BYPASS	V03	INC	A03	NSCIDI0	R04
CLKSEL	A02	INC	AA02	NSCIDI1	R03
DATA0	F19	INC	AA03	NSCIDI10	K04
DATA1	E19	INC	B01	NSCIDI11	D02
DATA10	L18	INC	B20	NSCIDI12	H03
DATA11	K19	INC	C02	NSCIDI13	F01
DATA12	M19	INC	C05	NSCIDI14	J02
DATA13	M18	INC	D04	NSCIDI15	D01
DATA14	N18	INC	D05	NSCIDI2	P02
DATA15	P18	INC	D17	NSCIDI3	P04
DATA16	P19	INC	D18	NSCIDI4	P01
DATA17	R20	INC	F03	NSCIDI5	N01
DATA18	N20	INC	G02	NSCIDI6	M03
DATA19	P21	INC	R02	NSCIDI7	M01
DATA2	G18	INC	R18	NSCIDI8	J04
DATA20	P20	INC	R19	NSCIDI9	F02
DATA21	M20	INC	T19	NSCIDO0	AA20
DATA22	N21	INC	T20	NSCIDO1	Y21
DATA23	K21	INC	T21	NSCIDO10	Y13
DATA24	M21	INC	U19	NSCIDO11	Y04
DATA25	J20	INC	U21	NSCIDO12	W09
DATA26	J21	INC	V05	NSCIDO13	W08
DATA27	H20	INC	V18	NSCIDO14	AA09
DATA28	H21	INC	V19	NSCIDO15	AA04
DATA29	G20	INC	V20	NSCIDO2	W15
DATA3	H18	INC	V21	NSCIDO3	AA19
DATA30	F20	INC	W05	NSCIDO4	W19
DATA31	E21	INC	Y01	NSCIDO5	Y17
DATA4	G19	INC	Y02	NSCIDO6	AA15
DATA5	H19	INC	Y06	NSCIDO7	Y14
DATA6	J18	INC	Y16	NSCIDO8	W11
DATA7	K18	NC	E04	NSCIDO9	AA06
DATA8	K20	NC	E18	NSCIFI	L03
DATA9	L19	NC	U04	NSCIFO	Y10
FLAG0	F21	NC	U18	NSCISI	K02
FLAG1	D21	NINCLK	D19	NSCISO	AA12
HALFSPD	C03	NOCLK	B21	ODATA0	A04

Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number
ODATA1	B04	PSCIDI12	H04	VCC	D06
ODATA10	B09	PSCIDI13	G03	VCC	D07
ODATA11	A09	PSCIDI14	H01	VCC	D08
ODATA12	A10	PSCIDI15	E03	VCC	D10
ODATA13	B10	PSCIDI2	N04	VCC	D12
ODATA14	C11	PSCIDI3	P03	VCC	D14
ODATA15	B11	PSCIDI4	N02	VCC	D15
ODATA16	A12	PSCIDI5	M04	VCC	D16
ODATA17	B12	PSCIDI6	M02	VCC	F05
ODATA18	C13	PSCIDI7	L04	VCC	F17
ODATA19	B13	PSCIDI8	H02	VCC	H05
ODATA2	B05	PSCIDI9	G04	VCC	H17
ODATA20	A13	PSCIDO0	Y20	VCC	L02
ODATA21	B14	PSCIDO1	W20	VCC	L20
ODATA22	C14	PSCIDO10	W13	VCC	P05
ODATA23	C15	PSCIDO11	Y05	VCC	P17
ODATA24	A15	PSCIDO12	Y09	VCC	T05
ODATA25	A16	PSCIDO13	Y08	VCC	T17
ODATA26	B16	PSCIDO14	AA10	VCC	U05
ODATA27	C17	PSCIDO15	W07	VCC	V06
ODATA28	B17	PSCIDO2	AA18	VCC	V07
ODATA29	A18	PSCIDO3	W17	VCC	V08
ODATA3	A06	PSCIDO4	V17	VCC	V10
ODATA30	B18	PSCIDO5	Y18	VCC	V12
ODATA31	C19	PSCIDO6	AA16	VCC	V14
ODATA4	B06	PSCIDO7	W14	VCC	V15
ODATA5	C07	PSCIDO8	Y12	VCC	V16
ODATA6	A07	PSCIDO9	AA07	VMM	A05
ODATA7	B08	PSCIFI	K01	VMM	A08
ODATA8	C08	PSCIFO	Y11	VMM	A11
ODATA9	C09	PSCISI	K03	VMM	A14
OFLAG0	A19	PSCISO	AA13	VMM	A17
OFLAG1	A20	RESET	T03	VMM	A21
PINCLK	D20	TCK	U01	VMM	AA01
POCLK	C20	TDI	V02	VMM	AA05
PSCIDI0	T02	TDO	W03	VMM	AA08
PSCIDI1	T01	TMS	V01	VMM	AA11
PSCIDI10	J01	TRST	U03	VMM	AA14
PSCIDI11	D03	TSTCLK	B02	VMM	AA17

Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number
VMM	AA21	VMM	E16	VMM	U20
VMM	B03	VMM	E17	VMM	V09
VMM	B07	VMM	E20	VMM	V11
VMM	B15	VMM	F04	VMM	V13
VMM	B19	VMM	F18	VMM	W01
VMM	C01	VMM	G01	VMM	W04
VMM	C04	VMM	G21	VMM	W06
VMM	C06	VMM	J03	VMM	W10
VMM	C10	VMM	J19	VMM	W12
VMM	C12	VMM	N03	VMM	W16
VMM	C16	VMM	N19	VMM	W18
VMM	C18	VMM	R01	VMM	W21
VMM	C21	VMM	R21	VMM	Y03
VMM	D09	VMM	T04	VMM	Y07
VMM	D11	VMM	T18	VMM	Y15
VMM	D13	VMM	U02	VMM	Y19
VMM	E02	VMM	U08	VSCIPNC	V04
VMM	E05	VMM	U09	VSCOPNC	W02
VMM	E08	VMM	U10	VSCTE	E01
VMM	E09	VMM	U12	VTTL	E06
VMM	E10	VMM	U13	VTTL	E07
VMM	E12	VMM	U14	VTTL	U06
VMM	E13	VMM	U15	VTTL	U07
VMM	E14	VMM	U16		
VMM	E15	VMM	U17		

Package Information



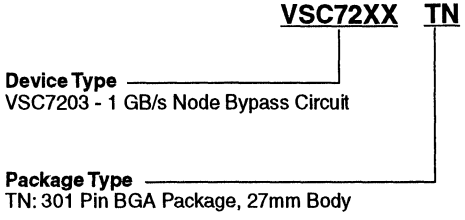
All dimensions in millimeters

Preliminary Data Sheet

1 GByte/sec SCI Compliant Switch Node Bypass Circuit

Ordering Information

The order number for this product is formed by a combination of the device number and package type.



Notice

This document contains information on products that are in the preproduction phase of development. The information contained in this document is based on test results and initial product characterization. Characteristic data and other specifications are subject to change without notice. Therefore, the reader is cautioned to confirm that this datasheet is current prior to placing orders.

Warning

Vitesse Semiconductor Corporation's products are not intended for use in life support appliances, devices or systems. Use of a Vitesse product in such applications without the written consent of the appropriate Vitesse officer is prohibited.

Preliminary Datasheet

Photodetector/Transimpedance Amplifier Family for Optical Communication

Features

- Integrated Photodetector/Transimpedance Amplifier Family Optimized for High Speed Optical Communications Applications
- Integrated AGC
- Fibre Channel Compatible Speed: [1/4 &1/2 Speed]
- High Bandwidth
- Low Input Noise Equivalent Power
- Large Optically Active Area
- Single 5V Power Supply

Part Number	*Fibre Channel Speed*	*Bandwidth (MHz)*	*Input Noise (μW rms)*	*Optically Active Area (μm diameter)*
VSC7802	1/4 Speed: 266 Mb/s	300	0.75	500
VSC7805	1/2 Speed: 531 Mb/s	650	1.0	100

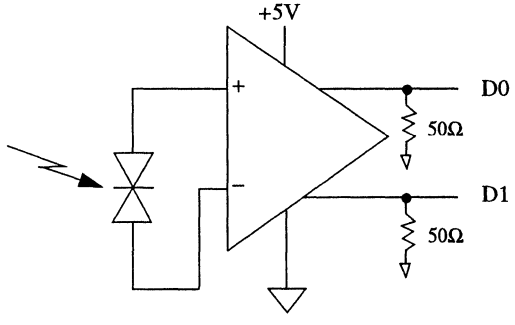
General Description

The VSC7802/VSC7805 series of integrated Photodetector/Transimpedance Amplifiers provide a highly integrated solution for converting light from a fiber optic communications channel into a differential output voltage. The benefits of Vitesse Semiconductor's Gallium Arsenide H-GaAs-III process are fully utilized to provide very high bandwidth and low noise in a product with a large optically active area for easy alignment. The sensitivity, duty cycle distortion and jitter meet or exceed all Fibre Channel application requirements. Parts are available in either die form or in flat-windowed packages.

By using an integrated MSM (Metal-Semiconductor-Metal) photodetector with an integrated transimpedance amplifier, the input capacitance is lowered which allows for a larger optically active area than in discrete photodetectors. Integration also allows superior tracking over process, temperature and voltage between the photodetector and the amplifier, resulting in higher performance. These parts can easily be used in developing Fibre Channel Electro-Optic Receivers which exhibit very high performance and ease of use.

VSC7802/7805 Block Diagram

Photodetector/Transimpedance Amplifier



Both D0 and D1 have an internal 50Ω termination resistor to GND

Photodetector/Transimpedance Amplifier Family for Optical Communication

Preliminary Datasheet

Table 1: Electro-Optical Specifications

Symbol	*Parameter*	*Part #*	*Min.*	*Typ.*	*Max.*	*Units*	*Conditions*
V_{cc}	Supply Voltage		4.5	5.0	5.5	V	
I_{cc}	Supply Current		13	30	40	mA	
PSRR	Power Supply Rejection Ratio		35	----	----	db	f = 1 to 40 MHz (Includes External Filter)
λ	Wavelength		770	840	850	nm	
F_c	Low Frequency Cutoff		----	----	1.8	MHz	-3db, P = -17 dBm @ 50 MHz
BW	Optical Modulation Bandwidth	7802	150	----	300	MHz	-3db, P = -17 dBm @ 50 MHz
		7805	350		650		
D_r	Dynamic Range	7802	24.2	----	----	db	
		7805	22.9				
S	Sensitivity	7802	-22.8	----	----	dBm	266 Mb/s
		7805	-21.5				531 Mb/s
R_o	Single Ended Output Impedance		25	----	60	Ω	
V_d	Differential Output Voltage		0.25	----	0.8	V	P = 1.4 dBm, R = 100 Ω differential
R_d	Differential Responsivity		1.2	----	----	mV/μV	R_{load} = 100 Ω P = -17 dBm @ 50 MHz
V_{dc}	Output Bias Voltage		1.0	----	2.5	V	
ΔV_{dc}	Bias Offset Voltage		----	----	150	mV	
NEP_o	Input Noise Equivalent Power	7802	----	----	0.75	μW rms	BW = 1 GHz P = 0 mW
		7805			1.0		
V_{no}	Output Noise Voltage	7802	----	----	0.6	mV rms	BW = 1 GHz P = 0 mW
		7805			1.2		
DCD	Duty Cycle Distortion		----	----	8	%	P = 1.4 dBm
T_r, T_f	Output Rise & Fall Time	7802	1300	----	----	psec.	20 - 80% P = 1.4 dBm
		7805	600				
I_{out}	Output Drive Current		2.5	----	8	mA	Normal Test Conditions 50Ω
PDJ	Pattern Dependent Jitter	7802	----	----	170	psec.	P = -5 dBm ± -10% Voltage Window
		7805			100		
----	Optically Active Area	7802	----	500	----	μm	Diameter
		7805		100			

Table 2: Absolute Maximum Ratings

Symbol	*Parameter*	*Limits*
V_{cc}	Power Supply	6V
T_{stg} (1)	Storage Temperature	-40°C to +85°C
H_{stg} (1)	Storage Humidity	5 to 95 %R.H. (Including Condensation)
T_{op} (1)	Operating Temperature	0° to 70°C
H_{op} (1)	Operating Humidity	8 to 80%R.H. (Excluding Condensation)
P_{inc}	Incident Optical Power	+3 dBm
S (1)	Impact Shock	500 G. Half Sine Wave Pulse Duration 1 +/-0.5 ms 3 Blows in each direction
V_{ib} (1)	Vibration	20 > 2000 > 20 Hz, 10 Minutes 10 G. Peak Acceleration 4 Complete Cycles, 3 Perpendicular Axes

(1) These specifications are for the 5.6mm package only.

Figure 1: MSM Spectral Response

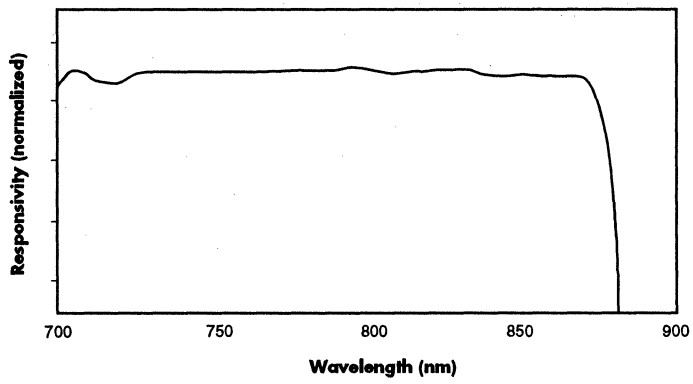


Figure 2: DIE I_{DD} vs Temperature

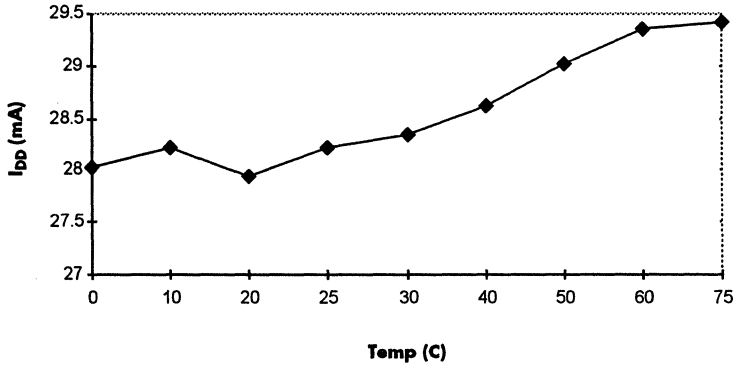
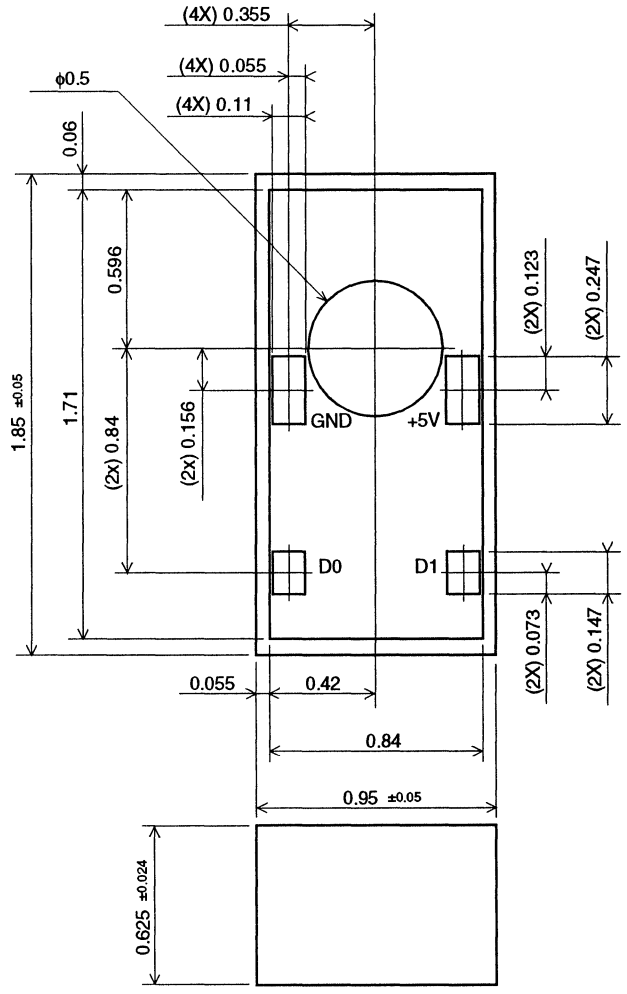


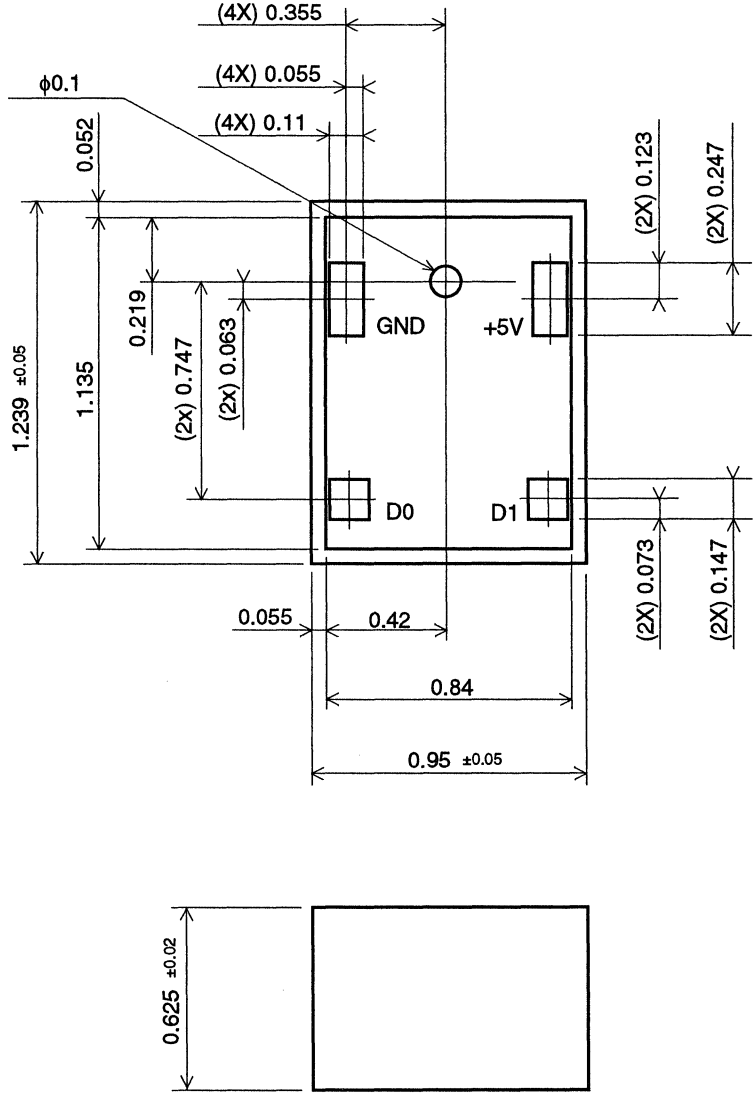
Figure 3: Mechanical Specifications (*Individual Die*)



VSC7802 DIE

Note: All measurements in mm

Figure 4: Mechanical Specifications (*Individual Die*)



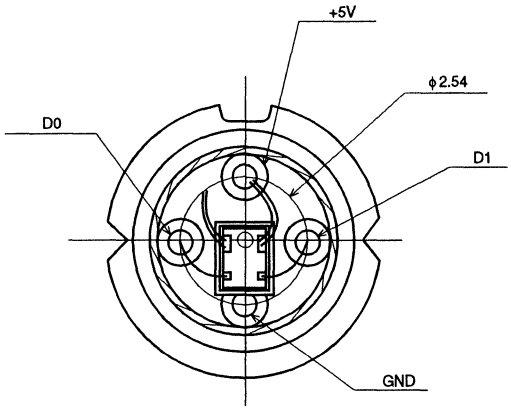
Note: All measurements in mm

VSC7805 DIE

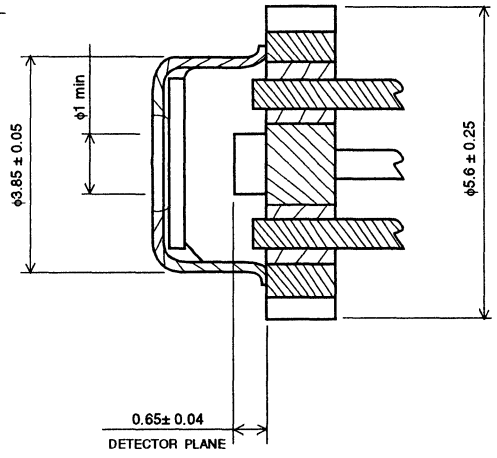
Preliminary Datasheet

Photodetector/Transimpedance Amplifier Family for Optical Communication

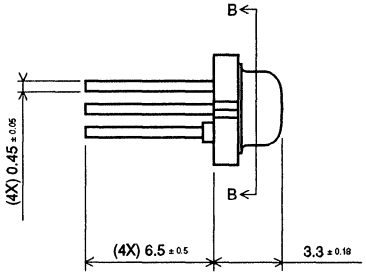
Figure 5: Mechanical Package Specifications *(5.6 mm Package)*

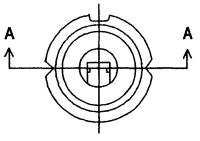


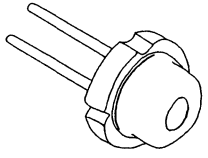
SECTION B-B
SCALE NONE



SECTION A-A
ROTATED CCW 90°
SCALE NONE







REFERENCE ISOMETRIC
SCALE NONE

Note: All measurements in mm

Ordering Information

Part Numbering Scheme:

VSC78XXYY

Where:

XX = Speed Grade

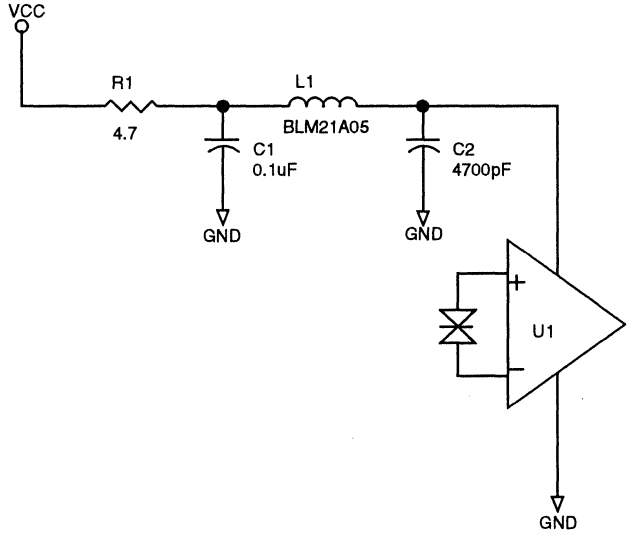
02	266 Mb/sec
05	531 Mb/sec

YY = Package Style

X	Individual Die
WB	5.6 mm Package

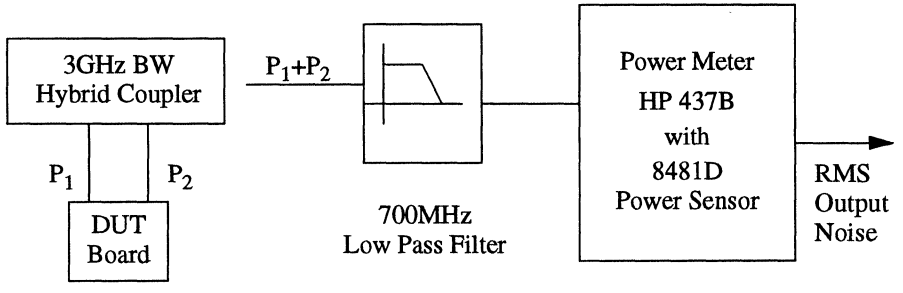
Notes on Measurement Conditions & Applications

Note 1: Bias Supply Filtering



* *The RCLC circuitry is to ensure a clean power supply line.*

Note 2: Noise Measurement Method



The noise voltage, (Vn), is calculated from the Output Noise Power, (Pn), into 50 ohm.

$$Vn = \sqrt{Pn \bullet 50}$$

The noise voltage, Vn, at the output is referred back to the noise power at the input through the responsivity R (with R in volts/watts)

$$NEP = \frac{Vn}{R}$$

The bit error rate can be expressed as

$$BER = \frac{\exp(-Q^2/2)}{\sqrt{2\pi Q}} .$$

Where:

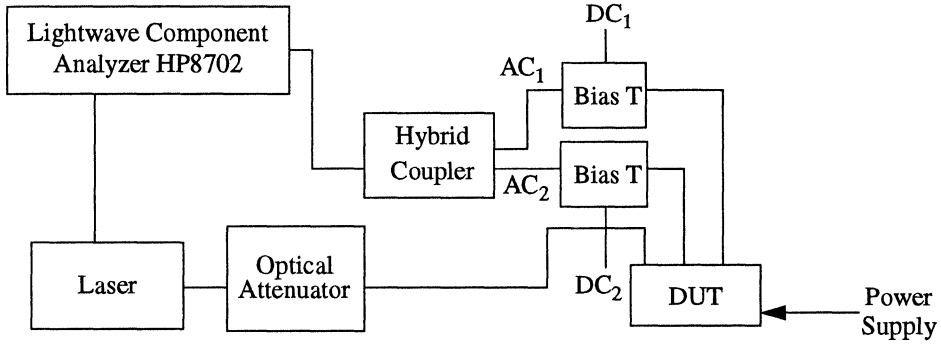
For a $BER = 1\times10^{-12}$ the parameter Q = 7.

The sensitivity(s) at a bit error rate of 1×10^{-12} is calculated as follows:

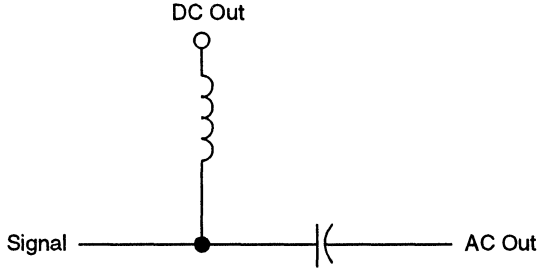
$$S = 10\ log_{10}\left(Q\frac{NEP}{1mW}\right) ,$$

where the NEP is in units of milliwatts and S is in dBm, respectively.

Note 3: Measurement Setup for Frequency Response



Note 4: Bias T Schematic



Notice

This document contains information on products that are in the preproduction phase of development. The information contained in this document is based on test results and initial product characterization. Characteristic data and other specifications are subject to change without notice. Therefore, the reader is cautioned to confirm that this datasheet is current prior to placing orders.

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Photodetector/Transimpedance Amplifier Family for Optical Communication

Preliminary Datasheet

Data Sheet

Photodetector/Transimpedance Amplifier Family for Optical Communication

Features

- Integrated Photodetector/Transimpedance Amplifier Optimized for High Speed Optical Communications Applications
- Integrated AGC
- Fibre Channel Compatible Speed: 1.06 Gb/s
- High Bandwidth
- Low Input Noise Equivalent Power
- Large Optically Active Area
- Single 5V Power Supply

Part Number	*Fibre Channel Speed*	*Bandwidth (MHz)*	*Input Noise (μW rms)*	*Optically Active Area (μm diameter)*
VSC7810	Full Speed: 1.06 Gb/s	1200	0.45	100

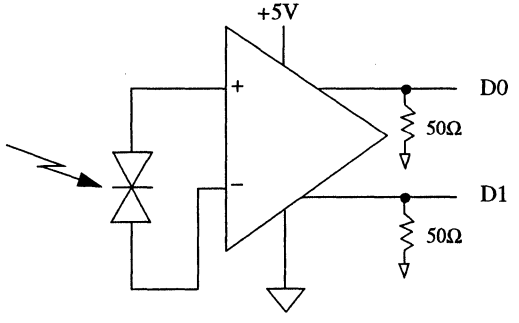
General Description

The VSC7810 integrated Photodetector/Transimpedance Amplifier provides a highly integrated solution for converting light from a fiber optic communications channel into a differential output voltage. The benefits of Vitesse Semiconductor's Gallium Arsenide H-GaAs process are fully utilized to provide very high bandwidth and low noise in a product with a large optically active area for easy alignment. The sensitivity, duty cycle distortion and jitter meet or exceed all Fibre Channel application requirements. Parts are available in either die form or in flat-windowed packages.

By using an integrated MSM (Metal-Semiconductor-Metal) photodetector with an integrated transimpedance amplifier, the input capacitance is lowered which allows for a larger optically active area than in discrete photodetectors. Integration also allows superior tracking over process, temperature and voltage between the photodetector and the amplifier, resulting in higher performance. This part can easily be used in developing Fibre Channel Electro-Optic Receivers which exhibit very high performance and ease of use.

VSC7810 Block Diagram

Photodetector/Transimpedance Amplifier



Both D0 and D1 have an internal 50Ω termination resistor to GND

Table 1: Electro-Optical Specifications

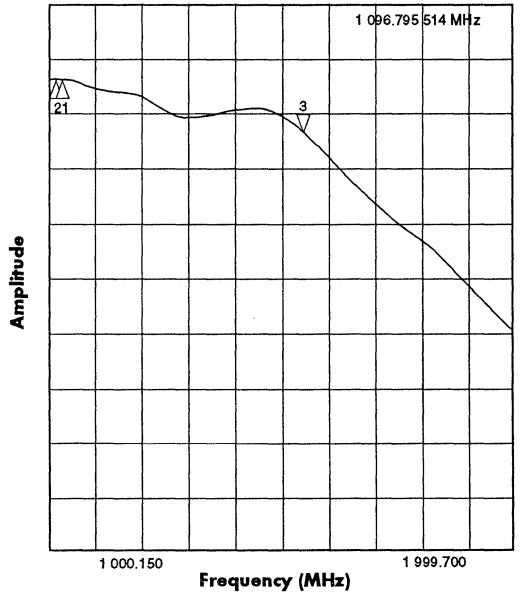
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{cc}	Supply Voltage	4.5	5.0	5.5	V	
I_{cc}	Supply Current	20	26	32	mA	
PSRR	Power Supply Rejection Ratio	35	----	----	db	f = 1 to 40 MHz (Includes External Filter)
λ	Wavelength	770	840	850	nm	
F_c	Low Frequency Cutoff	----	----	1.8	MHz	-3db, P = -17 dBm @ 50 MHz
BW	Optical Modulation Bandwidth	850	1040	1200	MHz	-3db, P = -17 dBm @ 50 MHz See note 3
D_r	Dynamic Range	19.4	----	----	db	
S	Sensitivity	-21.9	-24.8	-27	dBm	1.063Gb/s BER10^{-12}
R_o	Single Ended Output Impedance	25	----	60	Ω	
V_d	Differential Output Voltage	0.40	0.52	0.65	V	P = 1.4 dBm, R = 100 Ω differential
R_d	Differential Responsivity	0.8	1.4	2.0	mV/μW	R_{load} = 100 Ω P = -17 dBm @ 50 MHz
V_{dc}	Output Bias Voltage	1.2	1.5	1.8	V	
ΔV_{dc}	Bias Offset Voltage	----	40	120	mV	
NEP_o	Input Noise Equivalent Power	0.35	0.45	0.93	μW rms	P = 0mW BW = 1.0 GHz
V_{no}	Output Noise Voltage	0.55	0.66	0.75	mV rms	P = 0mW BW= 1.0 GHz
DCD	Duty Cycle Distortion	----	1.5	4.5	%	P = -3.5 dBm
I_{out}	Output Drive Current	2.5	----	8	mA	
PDJ	Pattern Dependent Jitter	20	40	60	psec	P = -5 dBm +/-10% Voltage Window
----	Optically Active Area	----	100	----	μm	Diameter
PPJ	PP Jitter	120	160	200	ps	
T_r	Rise Time	310	355	400	ps	20-80% P = +1.4 dBm
T_f	Fall Time	280	325	370	ps	20-80% P = –1.4 dBm

Table 2: Absolute Maximum Ratings

Symbol	*Parameter*	*Limits*
V_{cc}	Power Supply	6V
T_{stg} (1)	Storage Temperature	-40°C to +85°C
H_{stg} (1)	Storage Humidity	5 to 95%R.H. (Including Condensation)
T_{op} (1)	Operating Temperature	0° to 70°C
H_{op} (1)	Operating Humidity	8 to 80%R.H. (Excluding Condensation)
P_{inc}	Incident Optical Power	+3 dBm
S (1)	Impact Shock	500 G. Half Sine Wave Pulse Duration 1 +/-0.5 ms 3 Blows in each direction
V_{ib} (1)	Vibration	20 > 2000 > 20 Hz, 10 Minutes 10 G. Peak Acceleration 4 Complete Cycles, 3 Perpendicular Axes

(1) These specifications are for the 5.6mm package only.

Figure 1: Amplitude vs. Frequency



Frequency response of VSC7810WB upper 3db frequency is measuerd with respect to response at 50 MHz

Figure 2: MSM Spectral Response

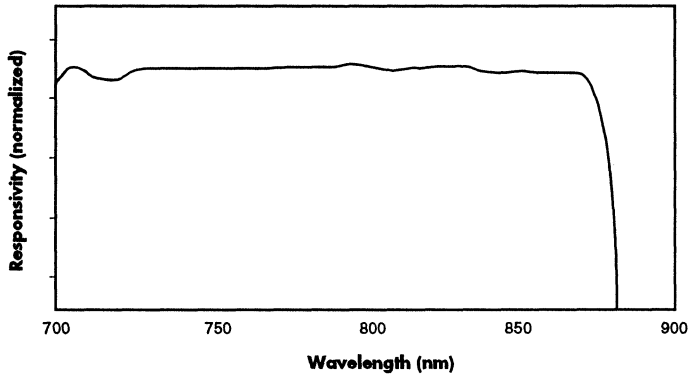


Figure 3: DIE I_{DD} vs. Temperature

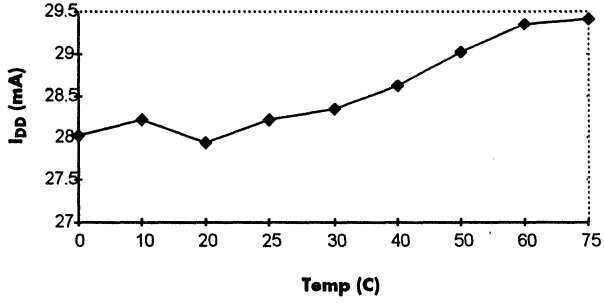


Figure 4: DIE Bandwidth vs. Temperature

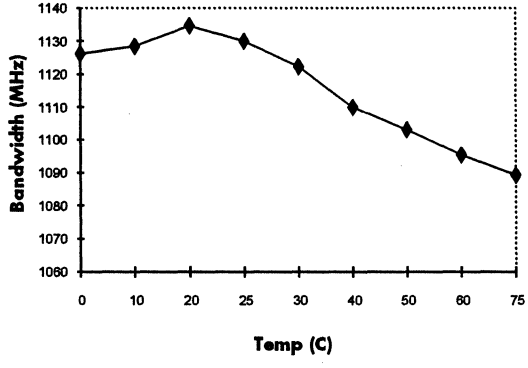


Figure 5: DIE Responsivity vs. Temperature

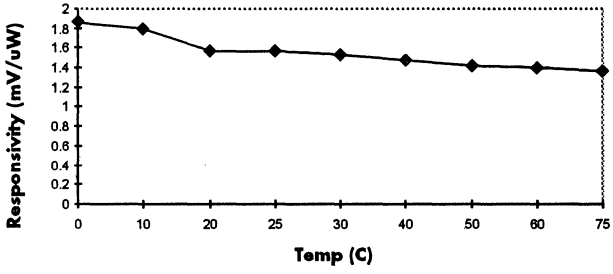


Figure 6: DIE PRBS Jitter vs. Temperature

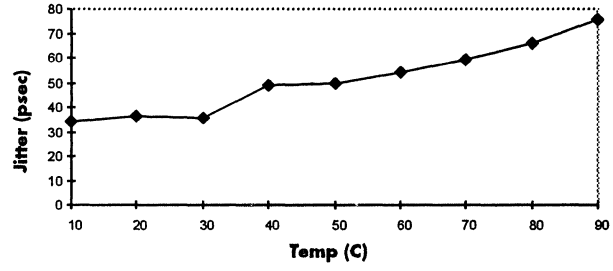


Figure 7: DIE Duty Cycle Distortion vs. Temperature

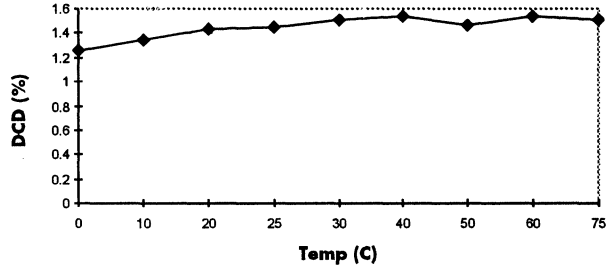
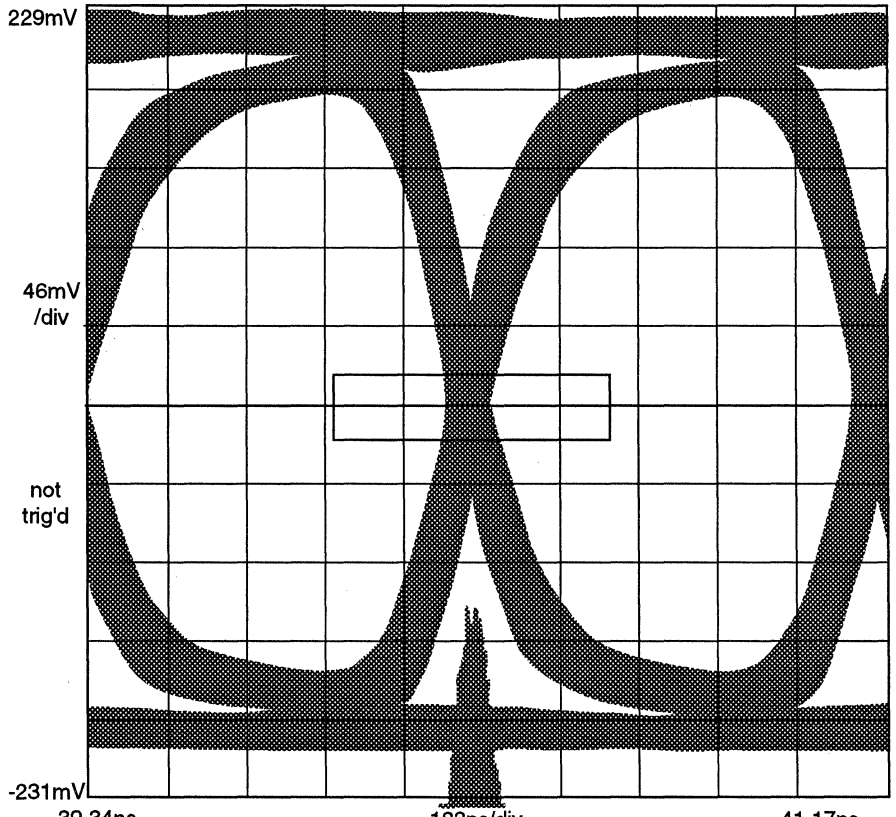


Figure 8: Eye Diagram



Top	15.56mV	Mean	40.23ns	μ±1σ	66.349%	Left	
Btm	-23.1mV	RMSΔ	25.98ps	μ±2σ	97.54%	39.90521ns	
Lft	39.91ns	PkPk	146.4ps	μ±3σ	100%	Right	
Rgt	40.55ns	Hits	6505	Wfms	1377	40.54571ns	

Figure 9: Mechanical Specifications (*Individual Die*)

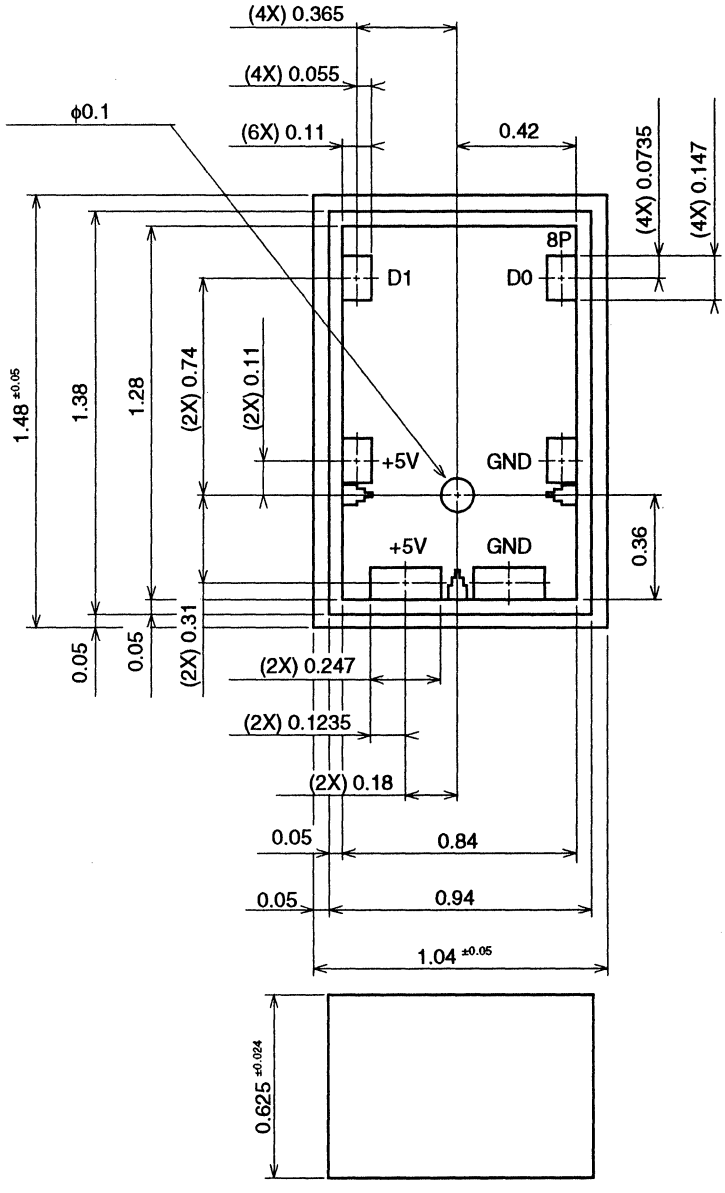
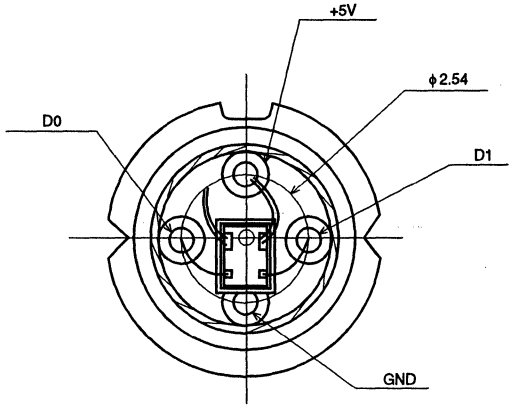
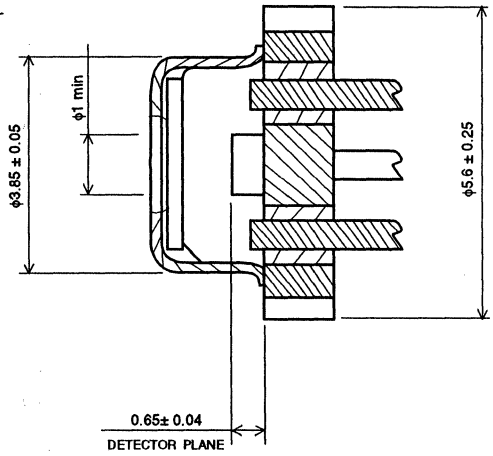


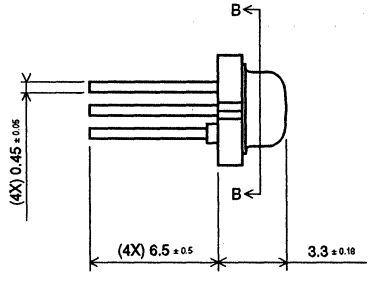
Figure 10: Mechanical Package Specifications *(5.6 mm Package)*

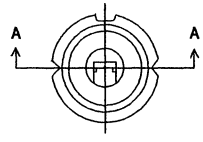


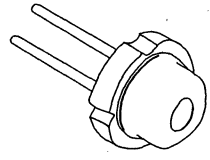
SECTION B-B
SCALE NONE



SECTION A-A
ROTATED CCW 90°
SCALE NONE



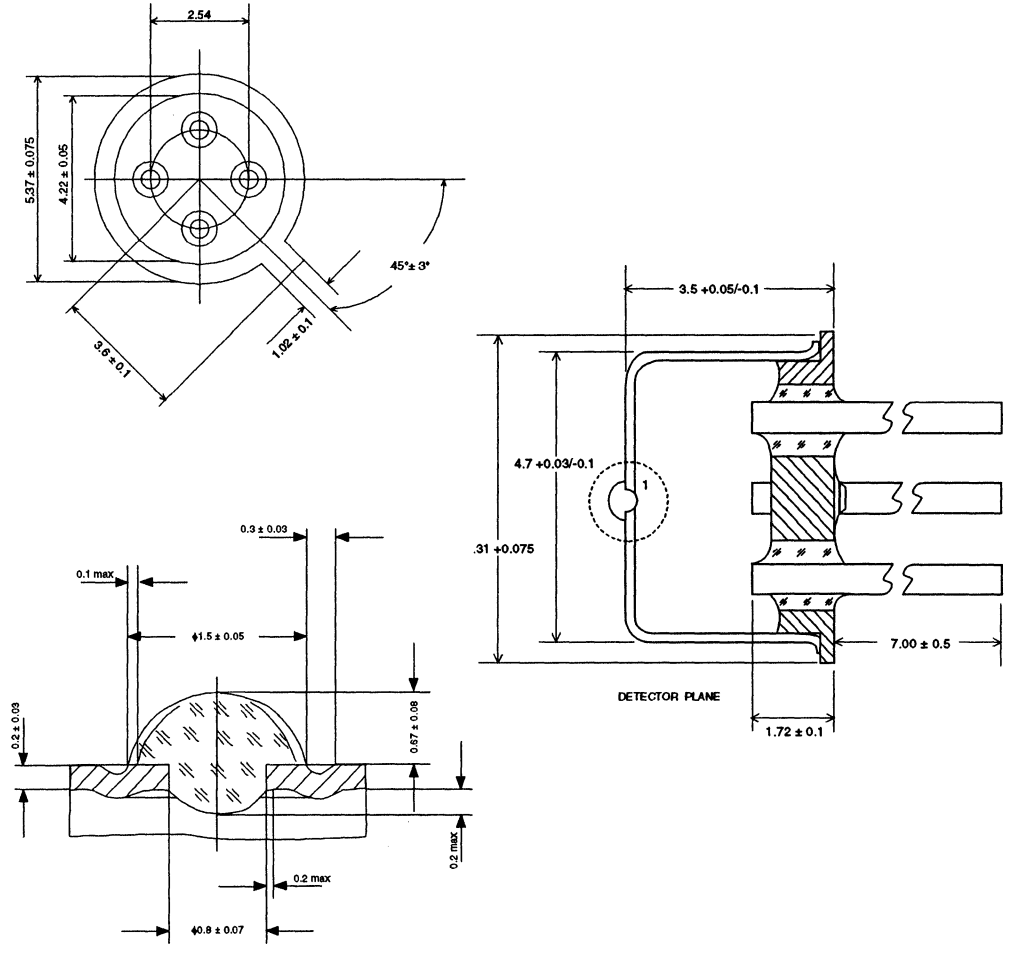




REFERENCE ISOMETRIC
SCALE NONE

Note: All measurements in mm

Figure 11: Mechanical Package Specifications (TO-46 *Ball Lens Package)*



Ordering Information

Part Numbering Scheme:

VSC78XXYY

Where:

XX = Speed Grade

10	1.0625 Gb/sec

YY = Package Style

X	Individual Die
WB	5.6 mm Package
WC	TO-46 Package with Ball Lens

Notice

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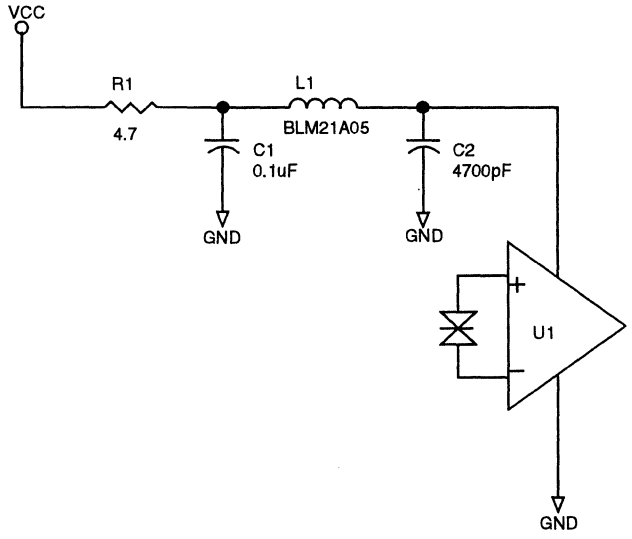
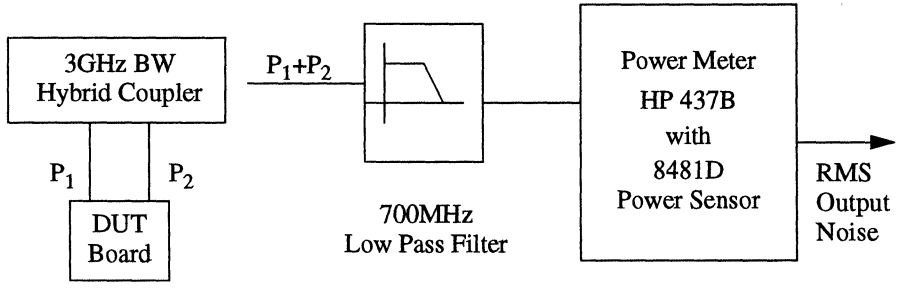
Notes on Measurement Conditions & Applications

Note 1: Bias Supply Filtering



The RCLC circuitry is to ensure a clean power supply line.

Note 2: Noise Measurement Method



The noise voltage, (Vn), is calculated from the Output Noise Power, (Pn), into 50 ohm.

$$Vn = \sqrt{Pn \bullet 50}$$

The noise voltage, Vn, at the output is referred back to the noise power at the input through the responsivity R (with R in volts/watts)

$$NEP = \frac{Vn}{R}$$

The bit error rate can be expressed as

$$BER = \frac{\exp(-Q^2/2)}{\sqrt{2\pi Q}} .$$

Where:

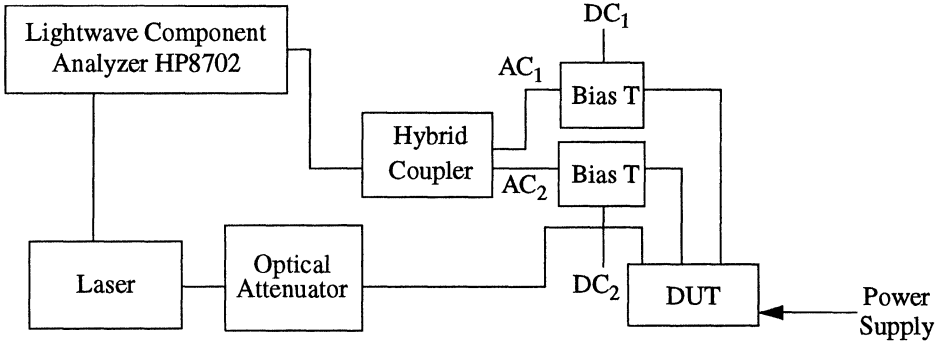
For a $BER = 1\times10^{-12}$ the parameter Q = 7.

The sensitivity(s) at a bit error rate of 1×10^{-12} is calculated as follows:

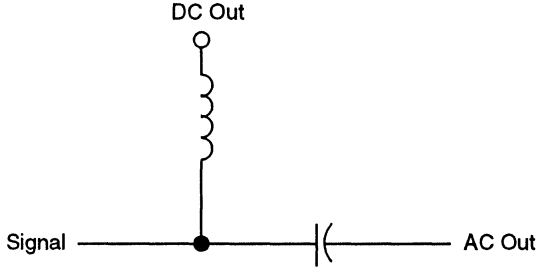
$$S = 10\ log_{10}\left(Q\frac{NEP}{1mW}\right) ,$$

where the NEP is in units of milliwatts and S is in dBm, respectively.

Note 3: Measurement Setup for Frequency Response



Note 4: Bias T Schematic



Design Guide

1.0625 Gbits/sec Fibre Channel Physical Layer Chips

Introduction

This document is intended to assist customers in using Vitesse's full-speed, Fibre Channel transmitters and receivers. Details concerning application information, circuit design, PCB layout and component selection is provided to help ensure first pass success in implementing a functional design which has optimized signal quality. This document is applicable to, but not limited to, the following Vitesse products:

VSC7105	Transmitter
VSC7106	Receiver
VSC7115	Transmitter
VSC7116	Receiver
VSC7120	Repeater/Hub Circuit
VSC7121	Quad Port Bypass Circuit
VSC7125	10-bit Transceiver

It is intended that this document be used in conjunction with the individual product datasheet and, if available, the product's design guide. An elementary knowledge of Fibre Channel and high speed printed circuit layout techniques is assumed. Please contact your local Field Applications Engineer or the Application Engineering Department at Vitesse to discuss any questions and concerns you may have.

System Interfacing

The interface between these products and the rest of the system varies significantly with each individual product. It is recommended that the designer consult the product data sheet or design guide for this information.

Clock Generation

One of the most important aspects of the design is generation of the REFCLK signal (also known as TBC in some products). This input provides the reference clock for the internal PLL which is multiplied by 10x or 20x to generate the baud rate clock.The rising edge of REFCLK is continuously phase compared to the internal baud rate clock so that the PLL will speed up or slow down the VCO in order to keep these two signals aligned. It is therefore important that the REFCLK be as jitter-free as possible in order to minimize jitter introduced into the PLL and its baud rate clock. It is also desirable to have fast rising edges on this clock to minimize the time in which the signal transitions from a LOW level to a HIGH level. A fast edge will reduce edge-detection ambiguity in the input buffer and therefore reduce jitter in the PLL. In some chips, the rising edge of this clock also latches the data on the transmit bus into the input latch so care must be taken to ensure that the transmit data bus meets the setup and hold time requirements of the transmitter.

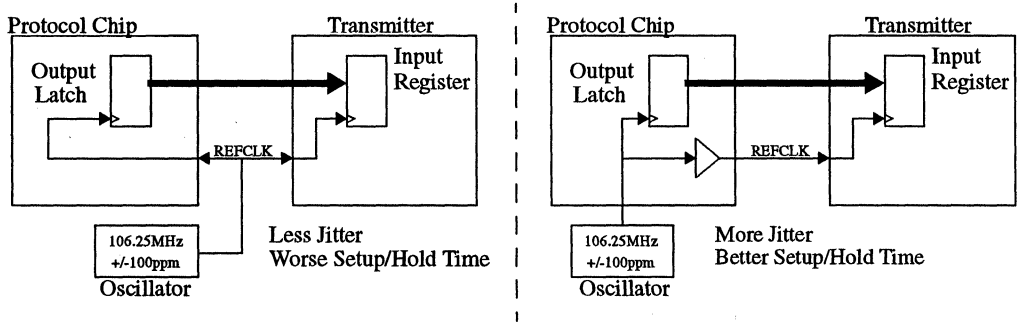
The most desirable solution for generating REFCLK is to have a crystal oscillator drive the input to the transmitter and receiver directly. In some cases, this oscillator will also have to drive a clock input to the protocol chip (i.e. the VSC7107 Encoder/Decoder) which interfaces to the transmitter and receiver. There is no need for any phase relationship to be maintained between the REFCLK(TBC) input of the transmitter and the REFCLK input of the receiver. More importantly, care must be taken to ensure that good quality signals are present at all inputs (transmitter, receiver and protocol chip) and that the proper phase relationship is maintained

between the transmitter and protocol chip if the transmitter latches data on the rising edge of this clock. Some chipsets allow the REFCLK input to be AC-coupled. This is a preferred method because the DC component of the signal will be set by the input buffer. This results in the REFCLK being centered around the trigger point of the input buffer thereby increasing noise margin and maximizing rise time. Most chipsets simply provide a TTL input buffer which does not support AC-coupling of this signal.

Although oscillators provide the cleanest source for REFCLK, oscillators over 100 MHz often cost more than may be acceptable for a specific design. In this case, customers have used clock generator chips to provide REFCLK at a lower cost than an oscillator. The cost reduction is, unfortunately accompanied by a significant increase in REFCLK jitter which adds jitter to the transmitted serial data resulting in a reduction in the maximum transmission distance. One example of such a clock generator is the IC Works' W42C26.

Another configuration is to generate the REFCLK in the protocol chip. This is sometimes desirable where the REFCLK is used to latch incoming transmit data since it may be easier to meet the setup/hold time requirements of the transmitter, especially when using a 10-bit interface at 106.25 MHz. This is illustrated below. When the oscillator drives REFCLK and the protocol chip, the clock to output delay of the protocol chip impacts on the setup/hold time of the databus with respect to the REFCLK. When the protocol chip generates REFCLK, the output buffer for REFCLK and the output latch for transmit data track each other and thereby increase setup time. However, the penalty for this scheme is increased jitter added by the protocol chip to the REFCLK. Where possible, it is recommended to let the oscillator drive both the protocol chip and the transmitter/receiver in order to provide the cleanest REFCLK.

Common REFCLK versus Separate REFCLK



High Speed Signal Termination

The differential high speed outputs of the transmitter (TX+ and TX-) are PECL outputs which require unique termination to ensure proper operation and optimize signal quality. Since these signals are clocked at 1.0625 GHz and transmit 8B/10B encoded data they carry digital signals between 106.25 MHz and 531.25 MHz. Obviously careful design and layout of the terminations and traces are required to maximize transmission distance and minimize signal degradation. The multiple media choices further complicate the use of these circuits. For the purposes of this discussion, four applications will be described for both the Transmitter Outputs (TX+/-) and the Receiver Inputs (RX+/-):

- Single Ended/Differential Coaxial Cable using 50 Ohm SMA Connectors for Test Equipment connectivity.
- Single Ended, 75 Ohm Coaxial Cable using BNC/TNC connectors for Fibre Channel Compatibility
- Differential, 150 Ohm Duplex Twinax Cable using DB-9 Connectors for Fibre Channel Compatibility.
- Fiber Optic Module interface at 50 Ohms.

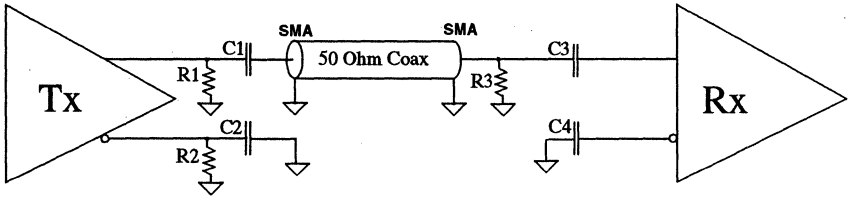
The transmitter outputs (TX+/-) are PECL outputs which are capable of sourcing current but not sinking it. Therefore a pull-down resistor (traditionally to Vdd-2.0V) is required to drive a LOW on the output when the output FET is turned off. The resistance of this pull-down is determined by the parametrics of the part and impedance of the signal trace. Since Vdd-2.0V is usually not present in the system, the output should be terminated to ground (Vss) for convenience. Also, PECL outputs do not conform to the ECL Inputs levels so all high speed I/O should be AC-coupled to eliminate mismatches in signal levels.

The receiver inputs (RX+/-) are differential PECL inputs which include resistor dividers to set the bias point of the input, usually at Vdd/2). Normally the user supplies resistors to terminate the transmission line and minimize reflections. An AC-coupling capacitor is provided to isolate the PECL input from the transmission line in order to let the input buffer set its own DC bias point. Lastly, a mechanism may be added to provide a DC offset so that if the input is open the input buffer will not oscillate. The following sections describe the designs of various termination schemes which provide some, but certainly not all of the options open to the user.

Single-Ended, 50 Ohm Termination

This application is ideal for connecting to test equipment such as oscilloscopes and BERTs but does not conform to the Fibre Channel Specification. On the transmitter outputs, a 182 ohm pull down resistor is located near the pin of the device in order to pull the signal to a LOW level when the output FET is turned off. The value of 182 ohms is used with 50 ohm impedance traces/cables. An AC-coupling capacitor (usually 0.01uF) is added in series to eliminate the DC component of the output signal allowing general purpose connectivity. On the receiver inputs, a 51.1 ohm line termination resistor is provided to match the impedance of the trace and coaxial cable in order to reduce reflections and optimize signal quality. An AC-coupling capacitor is added in series to allow the input buffer to establish the optimal DC-level provided by its internal resistor dividers to restore signal levels meeting the input requirements of the high speed input buffer. The unused receiver input is AC-coupled to ground to reduce noise susceptibility but keeps the input at the internal bias point. The 50 Ohm coaxial cable would normally be connected using SMA connectors for ease of use with test equipment. The shells of the SMA connectors are grounded.

Termination Example; 50 Ohm Single-Ended

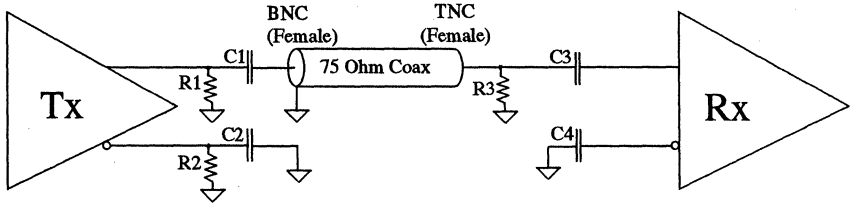


R1=R2=182 ohms, 1% R3=51.1ohms, 1%
C1=C2=C3=C4=0.01uF

Single Ended, 75 Ohm Termination

This is a Fibre Channel compatible application which is similar to the previous example. However in this example, the pull down resistor R1=R2=267 ohms instead of 182 ohms to match the 75 ohm transmission lines. Also the coaxial cabling and connectors are different in order to meet the 75 impedance required by Fibre Channel. The connector of the transmit side is a 75 ohm BNC (female on the board, male on the cable). The connector on the receive side is a 75 ohm TNC (female on the board, male on the cable). The shell of the BNC is grounded but the TNC shell is left open as specified in FC-PH Rev. 4.3 Section 7.2.3. These mismatched connectors provide built-in polarization.

Termination Example; 75 Ohm Single-Ended

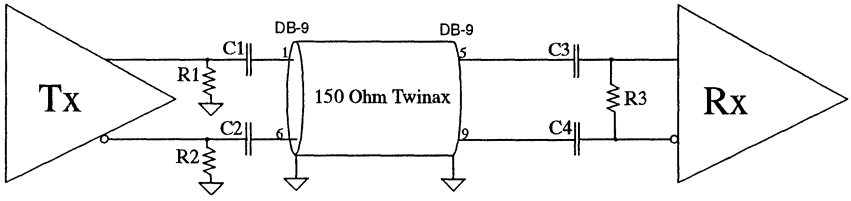


R1=R2=267 ohms, 1% R3=75 ohms, 1%
C1=C2=C3=C4=0.01uF

Differential, 150 Ohm Twinax Termination

A more popular Fibre Channel compatible application is for 150 ohm differential signals using 9-pin D-Subminiature connectors (also known as: DB-9) and duplex twinax cable. This provides better signal quality, longer transmission distance and reduced emissions as compared to single-ended configurations. Both outputs from the transmitter are terminated with 267 ohm pull downs. 1% components are used to maintain a balanced load between the two differential outputs. On the receive side, a single 150 ohm line termination resistor is used for impedance matching. This is located on the receiver side of the AC-coupling capacitors since this resistor will not affect the DC bias circuit. The connector for this application is a 9-pin D-Subminiature (female on the board, male on the cable) with TX+ on pin 1, TX- on pin 6, RX+ on pin 5 and RX- on pin 9. The shield of the cable is connected to chassis ground on both ends to provide a low impedance grounded shield. A cost effective duplex twinax cable which has an effective shielding scheme that reduces emissions to the point that systems pass FCC-B and CISPR EMI levels is available from W.L.Gore. The typical circuit for this application is shown below.

Termination Example; 150 Ohm Differential



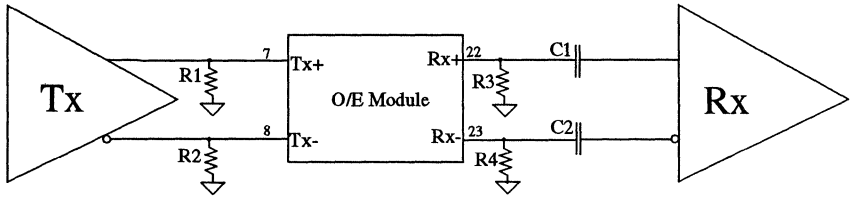
R1=R2=267 ohms, 1% R3=150 ohms, 1%
C1=C2=C3=C4=0.01uF

Fiber Optic Module Termination

Many customers wish to use Fibre Channel over fiber optic cable for increased distance, reduced EMI or other reasons. In general, this is a 50 ohm application, however, each vendor of fiber optic transceivers may have slightly unique interfacing requirements so it is recommended that the user contact the vendor prior to design. For the purposes of this example, a circuit is described which interfaces to Finisar's FTR-8510 and Methode's MTR-8510 800nm transceiver module.

No AC-coupling capacitors are required on the transmit side so only 182 ohm pull down resistors are provided. This application example assumes short traces (less than 2 inches) so that termination resistors are not required at the end of the traces on the transmit side. On the receive side, the normal 51.1 ohm and AC-coupling capacitor are provided.

Termination Example: Fiber Optic Transceiver

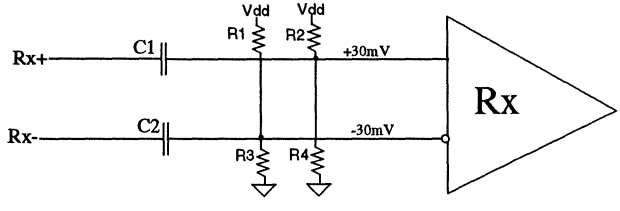


R1=R2=182 ohms, 1% R3,R4=51.1ohms, 1%
C1=C2=0.01uF

Preventing Oscillations

Since a link can be disconnected or a transmitter can be disabled, there are times when the receiver's inputs might not carry a valid signal. In the absence of a signal, both inputs of the receiver (RX+/RX-) will be at their internally determined bias points which are, by design, identical. When a differential input buffer's inputs are identical the buffer is susceptible to oscillations which could cause noise within the receiver. Vitesse's input buffers do not oscillate normally, however, in a noisy environment oscillations may occur. To prevent this problem, a Thevenin-equivalent resistor pair is used to both terminate the transmission line and to provide a small DC offset to the receiver. This offset is kept as low as possible so as not to introduce an offset under normal conditions which might add to the input jitter seen by the receiver. An example of this is shown below with values for both 50 ohm and 75 ohm impedance applications.

Termination Example; Preventing Oscillation

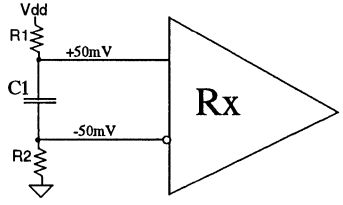


R1=R4=97.6 ohms, 1% R2=R3=102 ohms, 1% for 50 ohm impedance, [72mV offset]
R1=R4=147 ohms, 1% R2=R3=154 ohms, 1% for 75 ohm impedance, [76mV offset]
C1=C2=0.01uF

Unused Inputs

In many applications the receiver inputs might not be used. In this situation, it is important to terminate the inputs so that they will not oscillate. In a single-ended application, the unused receiver input is AC-coupled to ground to reduce noise susceptibility but keep the input at the internal bias point. If the differential inputs are not used then the circuit shown below is recommended. A variety of useful circuits may be used for this purpose but the two considerations are: provide a DC-offset and provide a low-impedance noise attenuation path. In the circuit shown, 47 Kohm external resistors are added in parallel with the internal 3 Kohm pair. This results in a 50 mV offset. The capacitor across the inputs provides a low-impedance path to reduce noise susceptibility.

Termination Example: Unused Inputs



R1=R2=47K ohms, 5%
C1=0.01uF

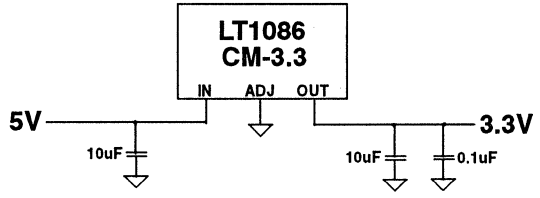
Power Supply Considerations

Generating 3.3V - Linear Regulator

All of Vitesse's Fibre Channel transmitters and receivers operate with a 3.3V +/- 5% power supply. Although the migration to 3.3V logic power supplies is underway, many system do not have an available 3.3V supply for use in powering the transmitter/receivers. The easiest, smallest and cheapest way to convert from a 5V power supply to a 3.3V level is through the use of a linear regulator. Converting from a +12V supply to a 3.3V supply is more difficult due to the additional power dissipation in the regulator which must be handled correctly. At 5V+/- 10%, the power dissipated in the regulator is calculated as (5.25V - 3.3V)*Idd(max). One nice feature of a linear regulator is that it provides a very quiet output which is isolated from the noise on the 5V supply. Since signal jitter is sensitive to power supply noise, the clean outputs of the linear regulator contribute to improved signal quality.

A readily available, multiple-sourced linear regulator is the Linear Technology LT1086CM-3.3 which is a fixed, 3.3V output voltage regulator in a surface mounted, DD-Pak package that provides up to 1.5 A output current. This is more than adequate to power a transmitter/receiver pair. A simple application circuit is shown below. Minimum values of input and output capacitance are required to provide stability to the regulator. Additional bypass capacitors must be added for additional power supply filtering at the pins of the chip. Similar linear regulators with different current limits are the LT1117CST-3.3 (800mA, SOT-223) and the LT1586CM-3.3 (4A, TO-220) both from Linear Technology.

5V to 3.3V Conversion using a Linear Regulator



Generating 3.3V - DC/DC Converter

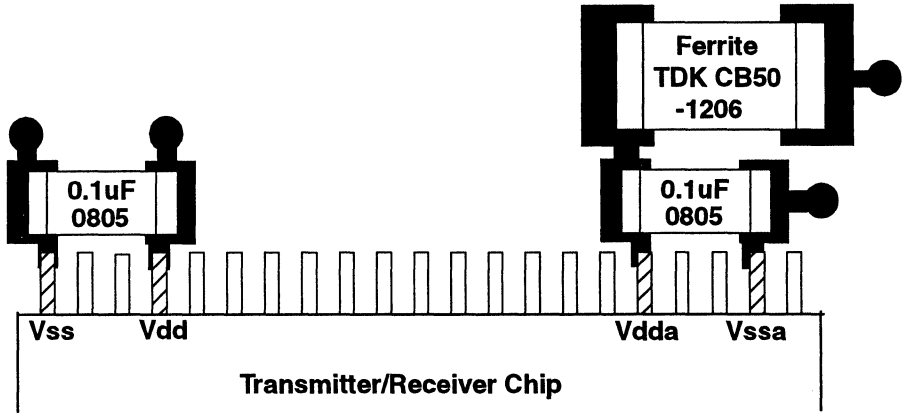
The limitation of a linear regulator is that it is not efficient so heat is generated. In applications where excessive heat is not acceptable, a DC/DC Converter may be used to convert either the 5V or 12V supplies into a 3.3V supply. The DC/DC converters available for the current levels needed in this application have excellent efficiency, between 85% and 95% which reduces heat generation. However, the DC/DC converters are more expensive, require more real estate, need several components, are not trivial to use and add noise to the 3.3V supply. The noise is a concern since power supply noise will couple into the PLL circuits and buffers of the transmitter and receiver thereby increasing jitter generation in the transmitter and reducing jitter tolerance in the receiver. If a DC/DC converter is used, extra care should be taken to reduce output noise.

An example of a DC/DC Converter which is appropriate for powering a transmitter/receiver is the Linear Technology, LT1256 1.5A part. For current levels under 450 mA, an LT 1574CS-3.3 is recommended. The DC/DC converter circuit is not shown here since these complicated parts have excellent application notes provided by the manufacturer.

Bypassing

The method in which bypass capacitors are used to filter the power supply to the transmitter and receiver has a significant impact upon signal quality. First, it is mandatory that the design include a power plane for Vss (Ground) which is at least 1 oz. copper. Secondly, a similar power plane for Vdd (3.3V) is strongly recommended. To reduce inductance, vias used to connect to these planes should not include thermal cut-outs similar to those found on Vdd/Vss connections to thru-hole components. It is strongly suggested that each power and ground pin be supplied from their own vias. Bypass capacitors are more effective when located on the same side of the PCB as the transmitter/receiver. Of course, the capacitors MUST be located as closely as possible to the Vdd and Vss pins of the chips. Furthermore, it is recommended that the capacitor be located between the pin and the via to the plane. A picture showing the preferred method for the layout of the bypassing capacitors is shown below. Since Vitesse's transmitters and receivers have roughly constant power supply current there is no need for exotic bypassing methods (i.e. two capacitors in parallel aimed at the switching frequency of the internal circuit). It is also recommended that the power and ground planes remain intact rather than attempting to steer current paths through sculpted planes. Most customers who have tried to isolate the planes for the transmitters and receivers usually produce more noise rather than reduce noise.

Bypassing Layout Example



All of the transmitter/receivers have internal PLLs which are powered from separate supply pins usually called Vdda/Vssa where the "a" denotes analog. These pins are particularly sensitive to noise so additional care must be taken to filter out noise. It is recommended that Vdd pass through a ferrite bead (i.e. TDK CB50-1206) to a bypass capacitor (at least one 0.1uF) and the power pin. The layout shown above indicates the preferred method for layout of this circuit.

Layout Considerations

When implementing a 1 Gb/s serial communications link the importance of the layout cannot be over-stressed. However, following general, simple-to-use guidelines will ensure success and prove easier than most designers anticipate. The prioritization of signals is as follows:

High Speed Serial I/O Lines

REFCLK traces

Power Supplies & Bypass Capacitors

Control Signals

Data Busses

Careful placement of components and the use of passives on both the top and bottom side will generally ensure optimal layout. As mentioned previously, a solid ground and power plane are quite useful in distributing clean power.

High Speed Serial I/O Layout Considerations

These signals contain digital data at frequencies between 106.25 to 531.125 MHz and require excellent frequency and phase response up to at least the 3rd harmonic, if not the 7th harmonic. Improved signal quality and longer practical transmission distances will result if the designer follows the general rules below:

- Keep traces as short as possible. Initial component placement should be very carefully considered.
- The impedance of the traces must match that of the termination resistors, connectors and cable in order to reduce reflections due to impedance mismatches.
- Impedance matching termination resistors (i.e. 51.1, 75 or 150 ohm) should be located as close to the input pin of the receiver as possible in order to minimize stub length. Since an AC-coupling capacitor is often inserted between the pin and the termination resistor, this is sometimes difficult to optimize.
- Differential impedance must be maintained in a 150 ohm differential application. Routing two 75 ohm traces is NOT adequate. The two traces must be separated by enough distance to maintain 150 ohm differential impedance. A good rule of thumb is that the trace separation should be at least 2.5 times the trace width.
- When routing differential pairs, keep the trace length identical between the two traces. Differences in trace lengths translate directly into signal skew. When separations occur, the differential impedance may be affected so take care when this is done.
- Keep differential pair traces on the same side of the PCB to minimize impedance discontinuities.
- Place any impedance discontinuities close to the transmitter or receiver and locate them together. This will minimize their impact on signal quality.
- Eliminate/reduce stub lengths.
- Reduce, if not eliminate, vias to minimize impedance discontinuities.
- Use rounded corners rather than 90 or 45 degree corners.
- Keep signal traces far from other signals which might capacitively couple noise into the signals. This includes the other trace of a differential pair.
- Do not route digital signals from other circuits across the area of the transmitter and receiver.
- Do not cut up the power or ground planes in an effort to steer current paths. This usually produces more noise, not less.

REFCLK Layout Considerations

The most difficult issue with regard to the REFCLK is that the signal goes to multiple inputs which all require an extremely clean clock with fast edges. This becomes a clock distribution challenge. Of course from an emissions point of view, the goal is to eliminate the high frequency harmonics in order to reduce radiated emissions. So a system developer may have contradictory goals requiring some compromise position.

One scheme used successfully in chipsets which require REFCLK only to the transmitter and receiver is to place the oscillator near the mid point between the two chips. Clock traces for each chip would then be routed from the oscillator outward to the chips with equal length traces. Daisy chaining has also been used successfully however the signal quality at the chip in the middle of the trace is somewhat difficult to optimize. A 10 or 33 ohm series resistor located at the oscillator can help but not eliminate this problem.

Power Supply Layout Considerations

These issues have been discussed previously and will not be detailed here. Vias used to connect the power planes to the Vdd and Vss pins of the chips should be at least 0.010 inches in diameter, preferably with no thermal relief, preferable plated closed with copper or solder. Also the via should be located on the opposite side of the bypass capacitor from the pin.

Control Signal Layout Considerations

There are no time-critical control signals on the transmitters/receivers. However it is important to route control lines to the chips in such a way as to avoid cross-talk and noise injection.

Data Bus Layout Considerations

The problem with the data busses is that there are a lot of signals in a small area. The only consideration here is to keep the traces roughly the same length as the clock used to latch them so that trace length differences do not reduce the setup/hold times of the chips.

Conclusion

Following the general guidelines described in this design guide will help ensure that customers integrating Fibre Channel components experience first-time success. You are encouraged to contact your local Field Applications Engineer or the Application Engineering Department at Vitesse to discuss any questions and concerns you may have. Vitesse will be happy to work with customers in any way to promote the success of their designs including schematic and layout reviews.

Component Supplier List

Below is a list of vendors who supply components of interest to Fibre Channel customers. Where applicable, a part number and description has been provided for key components required for specific applications.

Copper Cable Assemblies		
AMP	(800)52A-MP52	High Frequency Coax, Twinx & Quad Cable Assemblies
Berg	(717-764-7200	Cable Assemblies
Trompeter Electronics	(818)707-2020	Coaxial Cable Assemblies
W.L.Gore	(302)368-2575	Quad Cable, P/N FCN1008-xx where xx is distance in meters
Connectors		
AMP	(800)52A-MP52	RF, Coax, DB-9 & Fibre Channel specific (HSSDC) connectors.
E.F.Johnson	(800)247-8256	RF, Coaxial connectors
Samtec	(800)726-8329	"GLM" connector MOLC-120-01-P-Q-(LC) on the module FOLC-120-01-P-Q-(LC) on motherboard
Fiber Optic Modules		
AMP/Lytel	(800)52A-MP52	GLM Modules and O/E Modules
BCP	(407)984-3671	51T Transmitter & 51R Receiver
Finisar	(415)691-4000	Gb/s O/E Modules at 800nm, FTR-8510
Force Electronics	(703)382-0462	2684T Transmitter and 2684R Receiver
Fujikura Technology	(408)748-6991	GLM Modules and O/E Modules
Methode Electronics	(708)867-9600	Gb/s transceivers at 800nm, MTR-8510. Also GLM Modules
Fiber Optic Cable		
3M Fiber Optics	(908)544-9119	
Alcoa/Fujikura	(800)866-3953	
Methode Electronics	(800)323-6858	
Magnetics		
Coilcraft	(800)322-2654	Transformers for Line interfacing
Technitrol	(215)426-9105	Active and Passive Equalizer/Buffers
Oscillators		
Connor-Winfield	(708)851-4722	
IC Works	(408)922-0202	W42C26 Clock Generator
Motorola Semiconductor	(800)441-2447	MC88915FN-100 PLL Clock Doubler
Pletronics	(206)776-1880	A variety of oscillators,
Test Equipment		
Ancot	(415)322-5322	A Fibre Channel monitor/protocol analyzer,
Finisar	(415)691-4000	A family of Fibre Channel analyzer and monitors.
Gadzoox Microsystems	(408)866-9336	A serial data generator for receiver characterization.
Hewlett Packard	(408)435-7400	A variety of oscilloscopes, spectrum analyzers...
I-tech	(612)941-5905	A Fibre Channel emulator
Peer Protocol/Xyratex	(714)476-1916	A Fibre Channel tester for Arbitrated Loop.
Tektronix	(503)627-7111	A variety of oscilloscopes, spectrum analyzers...
Wavetek	(800)854-2708	Jitter analyzer.

Product Summary

Product Family	Description	Features
VS8004/8005	4:1 mux - 1:4 demux chipset with up to 2.5 Gb/s performance. Ideal for high speed instrumentation and test equipment, fiber optic communication, LANs, computer-to-computer interfaces.	Serial Data up to 2.5 Gb/s ECL 100K Compatible Parallel Data I/O Single ECL Power Supply: VEE = -5.2 V 1.5 W Power Dissipation (Typ.) 28-pin Ceramic LDCC Package
VS8021/8022	SONET Compatible 8:1 mux - 1:8 demux chipset with up to 2.5 Gb/s performance. Incorporates SONET frame detection and recovery circuitry and is compatible with SONET STS-3 through STS-48 applications.	Serial Data up to 2.5 Gb/s ECL 100K Compatible Parallel Data I/O Standard ECL Power Supplies: VEE = -5.2 V, VTT = -2.0 V 2.2 W Power Dissipation (Typ.) 52-pin Ceramic LDCC Package
VSC8023/8024	2.48 Gb/s ATM/SONET/SDH STM-16/STS-48 Mux/Demux and Section Terminator IC chipset. Incorporates SONET/SDH frame generation, detection and recovery. Ideal for high performance ATM physical layers, SONET/SDH transmission systems, digital-video distribution and SONET/SDH test equipment.	Byte Interleaves Four STS-12/STM-4 Data Streams to One STS-48/STM-16 Serial Stream Byte De-interleaves one STS-48/STM-16 Serial Stream into Four STS-12/STM-4 Data Streams Supports OC-48 and OC-48c Modes Performs Frame Synchronous Scrambling and Descrambling Provides Facilities and Equipment Loopbacks LOS Input and LOF Declaration Interfaces with PMC-Sierra's PM5312/5355 192 TBGA Package
VSC8023/8024EV (Data Sheet in Development)	The VSC8023/VSC8024 Evaluation Board provides users the ability to evaluate the VSC8023/VSC8024 devices and perform interoperability testing with four PM5355 S/UNI-622 devices. The board is self contained and designed to allow 2.5 Gb/s serial connections for interfacing to SONET or SDH test equipment allowing full compliance and error rate tests to be performed.	2.5 Gb/s Operation Includes Four PM5355 S/UNI-622 Devices for Interoperability Testing Flexibility to Evaluate the VSC8023/8024 in Various Operational Modes SMA Connections for High Speed Characterization Footprints Built in to Add Optic Modules Serial Connections for Interfacing to SONET/SDH Test Equipment.
VS8061/8062	16:1 mux - 1:16 demux chipset with up to 2.5 Gb/s performance. Compatible with SONET STS-3 through STS-48 applications.	Serial Data up to 2.5 Gb/s ECL 100K Compatible Parallel Data I/O Standard ECL Power Supplies: VEE = -5.2 V, VTT = -2.0 V 1.2 W Power Dissipation (Typ.) 52-pin Ceramic LDCC Package
VSC8063	A 2.5 Gb/s, 16:1 multiplexer designed for STM-16/STS-48 data rates at low power dissipation.	Serial Data Up to 2.5 Gb/s Internal PLL for Clock Synthesis with 155.52 MHz Reference Clock Frequency ECL 100K Compatible Parallel Data I/O Standard ECL Power Supplies: VEE = -5.2 V, VTT = -2.0 V 2.8W (max) Power Dissipation 52-pin PQFP Package

Product Summary

Product Family	Description	Features
VSC8071/8072	10 Gbits/sec 16-bit Mux/Demux chipset for STS-192 and STM-64 applications.	Serial Data Up to 10 Gb/s ECL 100K Compatible Parallel Data I/O Standard ECL Power Supplies VEE = -5.2V, VTT = -2.0V
VSC8101/8102	Single channel (8101) and eight channel (8102) digital clock recovery unit at 155 Mb/s (STS-3). Combines the best of PLL-based CRUs and run-length tolerant VCXO-based CRUs.	Single/Octal Channel Clock Recovery Unit ECL/PECL I/O Single 2V Power Supply 28 Pin PLCC (8101), 100PQFP (8102) 400 mW (8101), 3W (8102) Programmable Loop Bandwidth
VSC8110	ATM/SONET/SDH 155/622 Mb/s transceiver, integrating high speed clock generation with 8 bit mux/demuxing including frame detection and recovery. Ideal solution for ATM physical layers and SONET/SDH system applications.	STS-3/STM-1 or STS-12/STM-4 Data Rates Compatible with PMC-Sierra 5312/5355 Devices On Chip Clock Multiplication At Selectable Reference Frequencies Equipment and Facility Loopback Power - 1.98 Watts 100-Pin Thermally Enhanced PQFP Package
VSC8110EV	The VSC8110 evaluation board provides users the ability to evaluate the VSC8110 device and perform interoperability testing with the PM5312 STTX device. The board is self contained and includes DIP switches to exercise the various modes on the VSC8110 device. The board provides high speed serial connections for interfacing to SONET or SDH test equipment allowing full compliance and error rate tests to be performed.	155 Mb/s or 622 Mb/s Operation Includes the PM5312 STTX for Interoperability Testing Completely Self Contained for Self Test Operation Flexibility to Evaluate the VSC8110 in All Modes of Operation SMA Connections for High Speed Characterization Allows Signals to be AC or Direct Coupled into the VSC8110 ECL Buffered Interfaces Provided
VSC8111	Low power, single power supply ATM/SONET/SDH 155/622 Mb/s Transceiver Mux/Demux with integrated clock generation. Incorporates SONET/SDH frame detection and recovery. Ideal for ATM physical layers and SONET/SDH systems.	STS-3/STM-1 or STS-12/STM-4 Data Rates Compatible with PMC-Sierra PM5312/5355 Devices On-chip Clock Multiplication Selectable Reference Frequencies Bellcore, ITU and ANSI Jitter Compliance Looptiming Facilities Enhanced Equipment and Facility Loopback Single 3.3V Power Supply Low Power - 1.2W max 100 Pin Thermally Enhanced PQFP Package

Product Summary

Product Family	Description	Features
VSC8111EV (Data Sheet in Development)	The VSC8111 evaluation board provides users the ability to evaluate the VC8111 device and perform interoperability testing with the PM5355 S/UNI-622 device. The board is self contained and includes DIP switches to exercise the various modes on the VSC8111 device. The board provides high speed serial connections for interfacing to SONET or SDH test equipment allowing full compliance and error rate tests to be performed.	155 Mb/s or 622 Mb/s Operation Includes the PM5355 S/UNI-622 for Interoperability Testing Completely Self Contained for Self Test Operation Flexibility to Evaluate the VSC8111 in all Modes of Operation SMA Connections for High Speed Characterization Allows Signals to be AC or Direct Coupled into the VSC8111 ECL Buffered Interfaces Provided
VSC8112	ATM/SONET/SDH 622 Mb/s mux/demux with integrated clock generation. Provides equipment and facilities loopback. Ideally suited for high speed data distribution in ATM and SONET/SDH systems.	Operates as a Bit-serial STS-3/STM-1 to STS-12/ STM-4 Mux/Demux On-chip 622 MHz Clock Generation from 155 MHz Reference Equipment and Facility Loopback Extended Temperature Range - 0°C to 110°C Low Power - 1.5W Max 100 Pin Thermally Enhanced PQFP Package
VSC864A-2	64 x 64 crosspoint switch with up to 200 Mb/s performance and £10% duty cycle distortion. Ideal for high speed data distribution for telecommunications, computer network and multiprocessor switching, video switching, and test equipment.	200 Mb/s Operation Duty Cycle Distortion ≤10% ECL 100K Compatible Parallel Data I/O Clocked Mode Output to Output Skew <1500 ps 9.4 W Power Dissipation (Typ.) Power Supply: -2.0 V ± 5% Cascadable for Larger System Requirements 344-pin Ceramic LDCC Package

Product Summary

Data Sheet

2.5 Gbits/sec 4-Bit Multiplexer/ Demultiplexer Chipset

Features

- Serial Data Rates up to 2.5 Gb/s
- Parallel Data Rates up to 625 Mb/s
- ECL 100K Compatible Parallel Data I/Os
- Divide-by-4 Clock for Synchronization of Parallel Data to Interfacing Chips
- SKIP Input on Demux for Realignment of Output Word Boundaries
- Differential or Single-Ended Inputs and Outputs
- Low Power Dissipation: 1.5 W (Typ. Per Chip)
- Standard ECL Power Supply: VEE = -5.2 V
- Available in Commercial (0° to +70°C) or Industrial (-40° to +85°C) Temperature Ranges
- Proven E/D Mode GaAs Technology
- 28-pin Leaded Ceramic Chip Carrier

Functional Description

The VS8004 and VS8005 are data conversion devices capable of serial data rates up to 2.5 Gb/s, transforming 4-bit wide parallel data to serial data and serial data to 4-bit wide parallel data.

The VS8004/VS8005 are fabricated in gallium arsenide using the Vitesse H-GaAs™ E/D MESFET process which achieves high speed and low power dissipation. These products are packaged in a ceramic 28-pin leaded chip carrier.

VS8004

The VS8004 is a high speed 4 bit parallel to serial data converter suitable for digital voice or data communications applications. All inputs and outputs can be used differentially or single-ended. The parallel inputs [D(0:3), ND(0:3)] accept data at rates up to 625 Mb/s. The differential serial data output (SDATA, NSDATA) presents the data sequentially from the parallel data inputs at rates up to 2.5 Gb/s, synchronous with the differential high speed clock input (CLK, NCLK). An internal timing generator receives the high speed clock input and divides it by four to create a differential clock output (CLK4, NCLK4). This clock signal is provided so that incoming parallel signals can be synchronized to arrive at the input data registers simultaneously. An internal bias network is provided at all inputs to simplify capacitive coupling.

VS8005

The VS8005 is a high speed 4-bit serial to parallel data converter suitable for digital voice or data communications applications. All inputs and outputs can be used differentially or single-ended. The differential serial data inputs (SDATA, NSDATA) accept data at rates up to 2.5 Gb/s, synchronous with the differential high speed clock input (CLK, NCLK). The parallel outputs [D(0:3), ND(0:3)] present the data sequentially at rates up to 625 Mb/s. An internal timing generator receives the high speed clock input and divides it by four to create a differential clock output (CLK4, NCLK4) which is synchronous with the parallel data outputs. A control input (SKIP, NSKIP) is provided to allow realignment of the output parallel word boundaries.

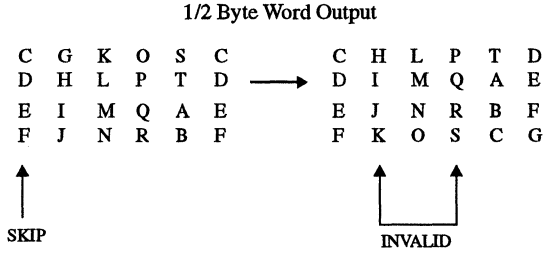
SKIP Signal

The SKIP signal is provided to allow realignment of the output parallel 4-bit word boundaries. Within the current CLK4, the rising edge of a SKIP causes an internal circuit in the VS8005 to hold the current 4-bit word output and drop the fifth output bit. The sixth output bit will become the MSB of the next 4-bit word output; and

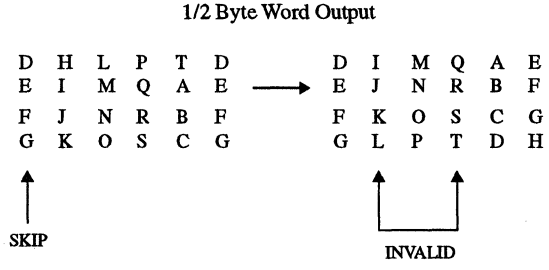
the falling edge of SKIP makes the next three parallel output words invalid (which is equal to three CLK4 or twelve CLK). After that the outputs will be valid and will have the MSB of the output realigned by one bit.

For Example, the user finds that the word boundary of the output is off by two bits, then he needs to perform two SKIPs. He needs to issue one SKIP, wait for three CLK4 cycles until the output is valid, then issue another SKIP, wait for another three CLK4 cycles. Then the outputs will have the bit positions in the right place as demonstrated in the following:

Misaligned by 2 bits:



Misaligned by 1 bit:



Realignment Done.

Applications

- High Speed Instrumentation and Test Equipment
- Fiber-optic Communication
- Local Area Networks
- Serialization of Computer Backplanes
- Computer to Computer Interfaces
- Serial Control Buses for Aerospace Environments

Data Sheet

2.5 Gbits/sec 4-Bit Multiplexer/ Demultiplexer Chipset

Figure 1: VS8004 Block Diagram

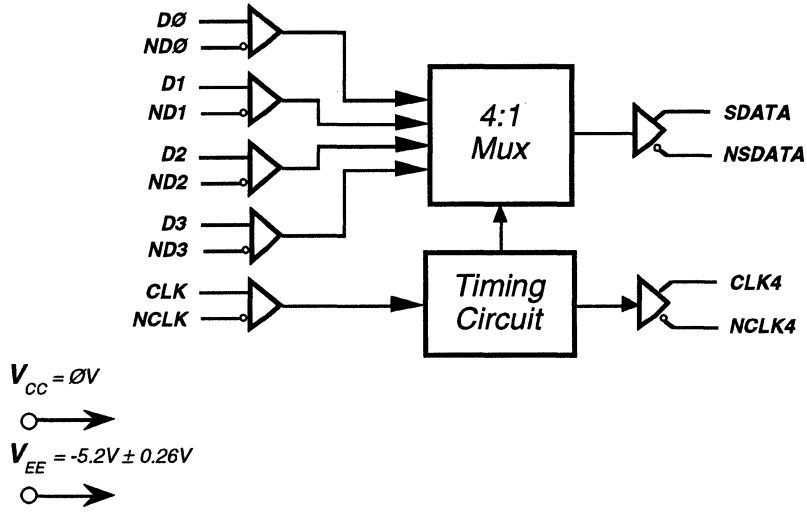
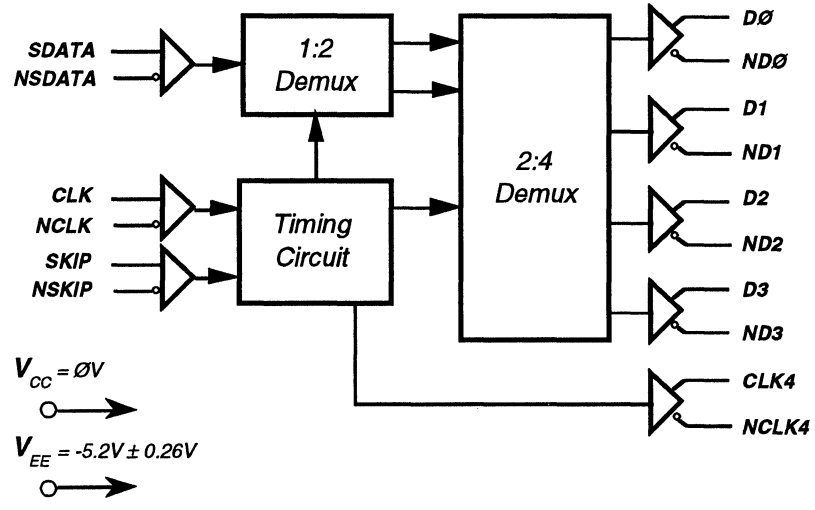


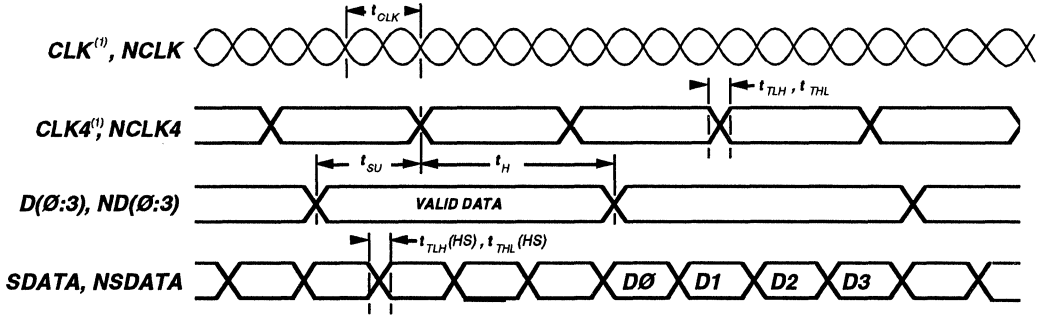
Figure 2: VS8005 Block Diagram



VS8004 AC Characteristics *(Over recommended operating conditions)*

Parameter	Description	Min	Typ	Max	Units
t_{CLK}	High Speed clock period	400	-	-	ps
t_{SU}	D(Ø:3), ND(Ø:3), set-up time with respect to CLK4, NCLK4	900	-	-	ps
t_H	D(Ø:3), ND(Ø:3), hold time with respect to CLK4, NCLK4	-300	-	-	ps
t_{TLH}(HS), t_{THL}(HS)	SDATA, NSDATA transition time (LO to HI, HI to LO) while driving 50Ω to -2.0V	-	150	-	ps
jitter(RMS)	CLK, NCLK to SDATA, NSDATA (max-min), (HI to LO), same part, same pin at constant conditions	-	<50	-	ps
t_{TLH},t_{THL}	ECL output transition time (LO to HI, HI to LO) while driving 50Ω (CLK4, NCLK4, D(0:3), ND(0:3)) to -2.0V	-	500	-	ps

Figure 3: VS8004 Waveforms

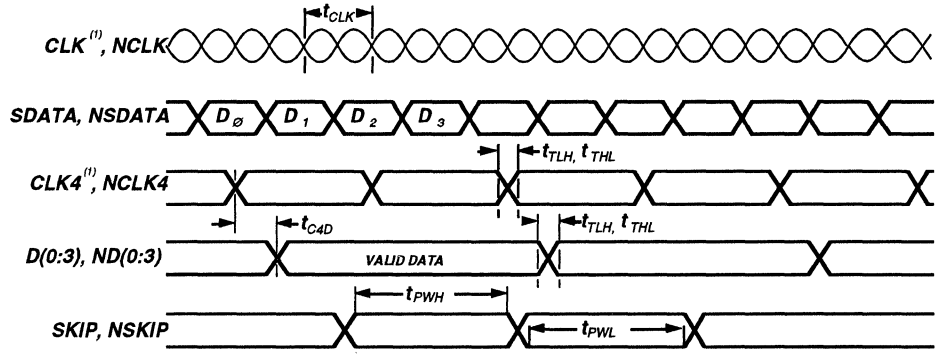


(1) Negative edge is active edge

VS8005 AC Characteristics *(Over recommended operating conditions)*

Parameter	Description	Min	Typ	Max	Units
t_{CLK}	High Speed clock period (CLK, NCLK)	400	-	-	ps
t_{CAD}	CLK4, NCLK4 to D(0:3), ND(0:3)	-	400	-	ps
t_{PWH}	SKIP, NSKIP pulse with (HIGH)	2	-	-	ns
t_{PWL}	SKIP, NSKIP pulse with (LOW)	2	-	-	ns
t_{TLH},t_{THL}	ECL output transition time (LOW to HIGH & HIGH to LOW) for D(0:3), ND(0:3) and CLK4, NCLK4 (Driving 50Ω)	-	500	-	ps
Phase Margin	SDATA, NSDATA phase timing margin with respect to CLK, NCLK input: *Phase Margin* = $\left(1-\frac{t_{SU}+t_H}{t_C}\right)360°$ where t_e is minimum clock cycle.	135	-	-	degrees

Figure 4: VS8005 Waveforms



(1) Rising edge causes serial data to be latched.

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Absolute Maximum Ratings[1]

Power Supply Voltage (V_{EE}) ..... V_{CC} (GND) to -6.0V
ECL Input Voltage Applied [2] (V_{ECLIN}) ..... -2.5V to + 0.5V
High Speed Input Voltage Applied [2] (V_{HSIN}) ..... V_{EE} -0.7V to V_{CC} + 0.7V
Output Current (output HIGH) (I_{OUT}) ..... -50 mA
Maximum Junction Temperature (T_J) ..... 150°C
Case Temperature Under Bias (T_C) ..... -55° to + 125°C
Storage Temperature (T_{STG}) ..... -65° to + 150°C

Notes: (1) Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage, but are stress ratings only. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.
(2) V_{EE} must be applied before any input signal voltage (V_{ECLIN}).

Recommended Operating Conditions

Power Supply Voltage (V_{EE}) ..... -5.2V ± 0.26V
Operating Temperature Range* (T) ..... (Commercial) 0° to 70°C, (Industrial) -40° to + 85°C

** Lower limit of specification is ambient temperature and upper limit is case temperature.*

Data Sheet

2.5 Gbits/sec 4-Bit Multiplexer/ Demultiplexer Chipset

DC Characteristics

Table 1: ECL Inputs and Outputs

(Over recommended operating conditions with internal V_{REF}, V_{CC} = GND, Output load = 50 ohms to -2.0V)

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-1020	-	-700	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
V_{OL}	Output LOW voltage	-2000	-	-1620	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
V_{IH}	Input HIGH voltage	-1040	-	-600	mV	Guaranteed HIGH signal for ECL inputs
V_{IL}	Input LOW voltage	-2000	-	-1600	mV	Guaranteed LOW signal for ECL inputs
I_{IH}	Input HIGH Current	-	500	1000	µA	$V_{IN} = V_{IH}$ (max)
I_{IL}	Input LOW Current	-1000	-500	-	µA	$V_{IN} = V_{IL}$ (min)

Note: 1) Differential ECL output pairs must be terminated identically.
2) Leakage currents exceed ECL specifications due to the internal bias network which is connected to all inputs

Table 2: Power Dissipation

(Over recommended operating conditions, V_{CC} = GND, outputs open circuit)

Parameter	Description	VS8004 (Min)	VS8004 (Typ)	VS8004 (Max)	VS8005 (Min)	VS8005 (Typ)	VS8005 (Max)	Units
I_{EE}	Power supply current from V_{EE}	-	270	350	-	310	400	mA
P_D	Power dissipation		1.5	1.9	-	1.6	2.2	W

Table 3: High Speed Inputs

(Over recommended operating conditions, V_{CC} = GND, Output load = 50 Ω to -2.0V)

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{IH}	Input HIGH voltage	-3.1	-3.0	-2.9	V	Guaranteed HIGH signal
V_{IL}	Input LOW voltage	-4.1	-4.0	-3.9	V	Guaranteed LOW signal
ΔV_{IN}	Input voltage swing	0.8	1.0	1.2	V	AC Coupled

Notes: 1) ESD protection is not provided for the high speed input pins, therefore, proper procedures should be used when handling this product.
2) A reference generator is built in to each high speed input, and these inputs are intended to be AC coupled.
3) If a high speed input is used single-ended, a 150 pF capacitor must be connected between the unused high speed or complement input and the power supply (V_{TT}).

Table 4: High Speed Outputs

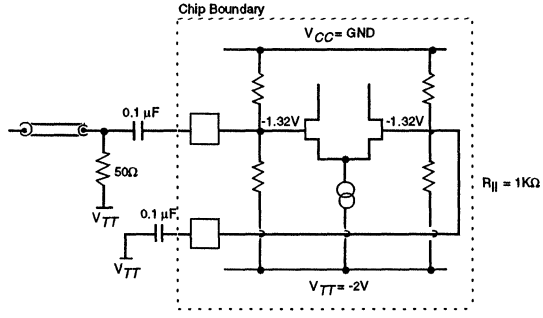
(Over recommended operating conditions, V_{CC} = GND, Output load = 50Ω to -2.0V)

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-	-0.9	-	V	Terminated to -2.0V through 50Ω
V_{OL}	Output LOW voltage	-	-1.8	-	V	Terminated to -2.0V through 50Ω
ΔV_{OUT}	Output voltage swing	0.8	1.0	1.4	V	Output Load, 50Ω to -2V

Notes: 1) ESD protection is not provided for the high speed input pins, therefore, proper procedures should be used when handling

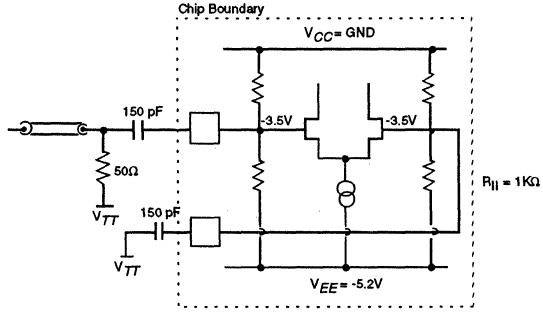
Parallel Data, CLK, NCLK, SKIP, NSKIP Inputs

ECL inputs (clock or data) provide for AC coupled operation. Internal biasing will position the reference voltage of approximately -1.32 Volts on both the true and complement inputs.



High Speed Inputs

High speed inputs (clock or data) provide for AC coupled operation. Internal biasing will position the reference voltage of approximately -3.5 Volts on both the true and complementary inputs. Single-ended, AC coupled operation is illustrated below



$V_{TT} = V_{CC}$ -2V

Figure 5: VS8004 Pin Diagram

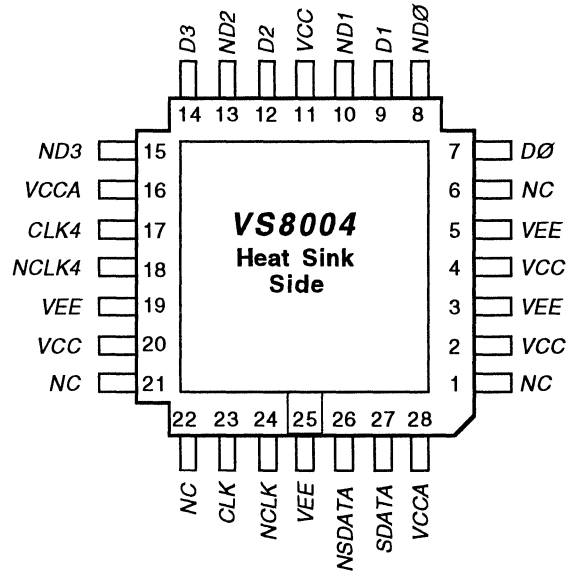


Table 5: VS8004 Pin Description

Pin #	*Name*	*I/O*	*Description*
23, 24	CLK, NCLK	I	Differential high speed clock inputs
27, 26	SDATA, NSDATA	O	Differential high speed serial data outputs
17, 18	CLK4, NCLK4	O	Differential divide by 4 clock outputs (ECL)
7-10, 12-15	D(Ø:3), ND(Ø:3)	I	Differential parallel data inputs (ECL)
3, 5, 19, 25[1]	V_{EE}		-5.2V supply voltage
2, 4, 11, 20	V_{CC}		Ø V ground connection
16, 28	V_{CCA}		Ø V output ground connection (Normally connected to V_{CC})
1, 6, 21, 22	NC		No connection

Notes: 1) The heat sink is connected V_{EE}(pin 25). To prevent a short circuit between V_{CC}, V_{CCA} (Ø V normally) and V_{EE} (-5.2V normally), do not connect this heat sink to ground. (ØV).

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Figure 6: VS8005 Pin Diagram

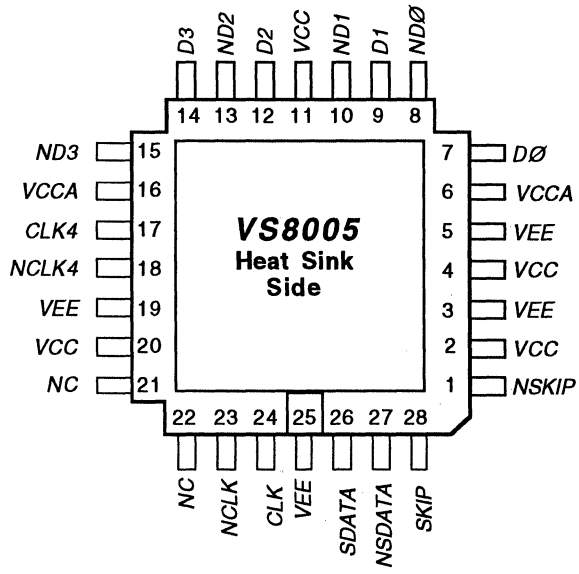


Table 6: VS8005 Pin Description

Pin #	*Name*	*I/O*	*Description*
24, 23	CLK, NCLK	I	Differential high speed clock inputs
26, 27	SDATA, NSDATA	I	Differential high speed serial data outputs
17, 18	CLK4, NCLK4	O	Differential divide by 4 clock outputs (ECL)
7-10, 12-15	D(Ø:3), ND(Ø:3)	O	Differential parallel data outputs (ECL)
28, 1	SKIP, NSKIP	I	Differential word boundary inputs (ECL)
3, 5, 19, 25	V_{EE}		-5.2V supply voltage
2, 4, 11, 20	V_{CC}		Ø V ground connection
6, 16	V_{CCA}		Ø V output ground connection
21, 22	NC		No connection

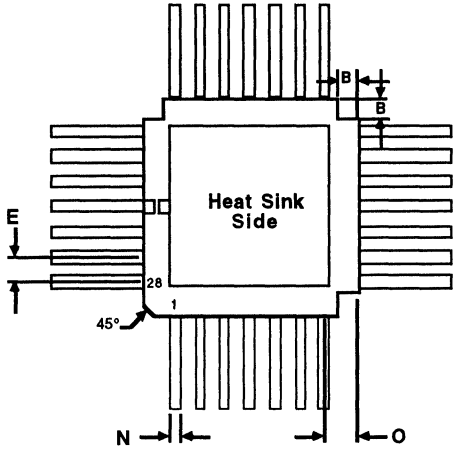
Notes: 1) The heat sink is connected to V_{EE}(pin 25). To prevent a short circuit between V_{CC}, V_{CCA} (Ø V normally) and V_{EE} (-5.2V normally), do not connect this heat sink to ground.

2) The falling edge of SKIP causes realignment of the parallel word boundary making parallel data invalid for three CLK4, NCLK4 (12 CLK, NCLK) periods.

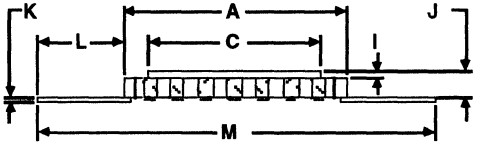
Data Sheet

2.5 Gbits/sec 4-Bit Multiplexer/ Demultiplexer Chipset

Package Information



28-Pin Leaded Ceramic Package (LDCC)



NOTES:
Drawing not to scale.
Package: Ceramic (alumina);
Heat sink: Copper-tungsten;
Leads: Alloy 42 with gold plating.

Item	mm (Min/Max)	in (Min/Max)	Item	mm (Min/Max)	in (Min/Max)
A	11.176/11.682	0.440/0.460	K	0.102/0.203	0.004/0.008
B	1.016/1.524	0.040/0.060	L	5.842/6.858	0.230/0.270
C	8.128/8.636	0.33 TYP	M	22.860/25.398	0.900/1.000
E	1.143/1.397	0.050 TYP	N	0.356/0.559	0.014/0.022
I	0.406/0.610	0.016/0.024	O	1.525/2.287	0.075 TYP
J	1.829/2.235	.072/.088	—	—	—

DUT Boards

The VS8004FDUT/VS8005FDUT evaluation boards are special purpose circuit boards which provide a test bed suitable for evaluating the high performance characteristics of the VS8004 4:1 Multiplexer or the VS8005 1:4 Demultiplexer in the 28 pin leaded ceramic chip carrier.

The figure below is a schematic representation of these circuit boards. These boards provide a controlled impedance transmission line for all signals, and suitable decoupling for the power supplies. The signal traces have a characteristic impedance of 50Ω. All ECL input lines are terminated with 50Ω (chip resistor) as close to the device package pin as possible. The high speed inputs are also provided with 150 pF blocking capacitors. Signals are launched onto the circuit board and removed by means of SMA coaxial connectors. While the input signals are terminated, the output signals are provided open circuit and are intended to be terminated in the measuring instrument.

Normally, the VS8004 and VS8005 operate in an ECL environment with standard ECL power buses: ØV and -5.2V. In order to simplify interface to standard ground referenced test equipment, however, the circuit board power buses are offset so that the shield connectors are at ground voltage. The figure below shows the arrangement of the power supply decoupling capacitors. There is a 33 µF electrolytic capacitor, as well as several 0.01 µF ceramic capacitors across each power bus.

The device to be tested is held in place with a pressure retaining fixture. The figure on the following page indicates the physical dimensions and the connection labels for the evaluation boards.

Figure 7: VS8004/VS8005 DUT Board Schematics

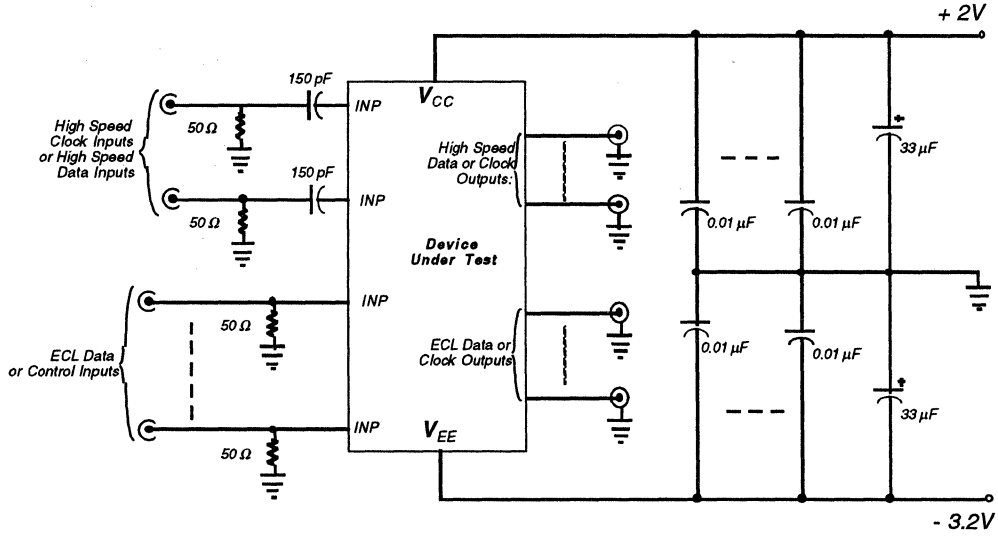
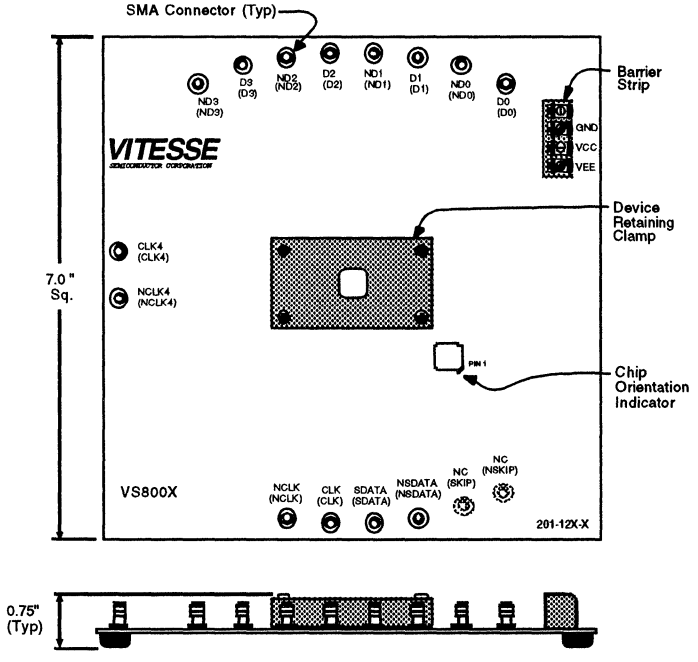


Figure 8: VS8004/VS8005 DUT Boards



Notes: 1) This drawing represents both the VS8004FDUT and VS8005FDUT configurations. (Connection labels given in parentheses are for the VS8005.)

2) NC = No connection. Note: These connectors are omitted on the VS8004FDUT version of this evaluation board.

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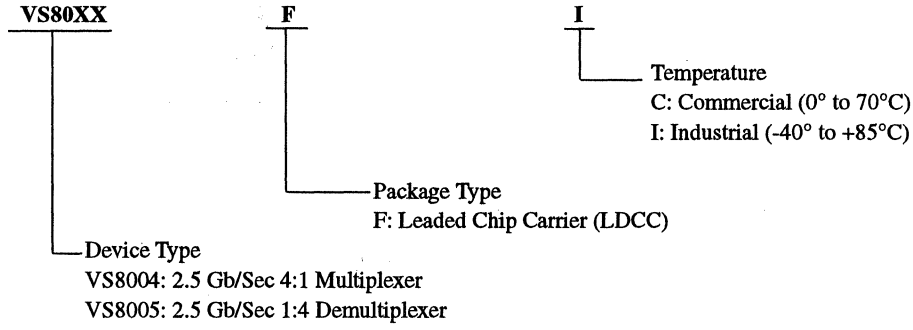
Ordering Information

Vitesse products are available in a variety of packages and operating ranges. The order number for this product is formed by using a combination of the following: *Device Type, Package Type, and Operating Temperature Range*.



Notice

Vitesse Semiconductor Corporation reserves the right to make changes in its products, specifications or other information at any time without prior notice. Therefore the reader is cautioned to confirm that this datasheet is current prior to placing any orders. The company assumes no responsibility for any circuitry described other than circuitry entirely embodied in a Vitesse product.

Warning

Vitesse Semiconductor Corporation's product are not intended for use in life support appliances, devices or systems. Use of a Vitesse product in such applications without the written consent is prohibited.

Data Sheet

2.5 Gbits/sec SONET Compatible
8-bit Mux/Demux Chipset

Features

- Serial Data Rates up to 2.5 Gb/s
- Parallel Data Rates up to 312.5 Mb/s
- ECL 100K Compatible Parallel Data I/Os
- Divide-by-8 Clock for Synchronization of Parallel Data to Interfacing Chips
- SONET Frame Recovery Circuitry (VS8022)
- Compatible with STS-3 to STS-48 SONET Applications
- Differential or Single-Ended Inputs and Outputs
- Low Power Dissipation: 2.3W (Typ. Per Chip)
- Standard ECL Power Supplies: VEE = -5.2 V, VTT = -2.0 V
- Available in Commercial (0° to +70° C) or Industrial (-40° to +85° C) Temperature Ranges
- Proven E/D Mode GaAs Technology
- 52-pin Leaded Ceramic Chip Carrier

Functional Description

The VS8021 and VS8022 are high speed SONET interface devices capable of handling serial data at rates up to 2.5 Gbits/second. These products can be used for STS-3 through STS-48 SONET applications.

These products are fabricated in gallium arsenide using the Vitesse H-GaAs™ E/D MESFET process which achieves high speed and low power dissipation. These products are packaged in a ceramic 52-pin leaded ceramic chip carrier.

VS8021

The VS8021 contains an 8:1 multiplexer and a self-positioning timer. The 8:1 multiplexer accepts 8 parallel differential ECL data inputs (D1-D8, D1N-D8N) at rates up to 312.5 Mbits/sec and multiplexes them into a serial differential bit stream output (DO, DON) at rates up to 2.5 Gbits/sec.

The internal timing of the VS8021 is built around the high speed clock (up to 2.5 GHz) delivered onto the chip through a differential input (CLKI, CLKIN). This signal is subsequently echoed at the high speed differential output (CO, CON).

The parallel data inputs are clocked to on-chip input registers with an externally supplied differential ECL input (BYCLK, BYCLKN) operating at the same rate as the data inputs. An internal byte clock, which is a divide by 8 version of the high speed clock, is used to transfer the data to a set of buffer registers. This internal byte clock is brought off chip at the ECL output CLK8, CLK8N.

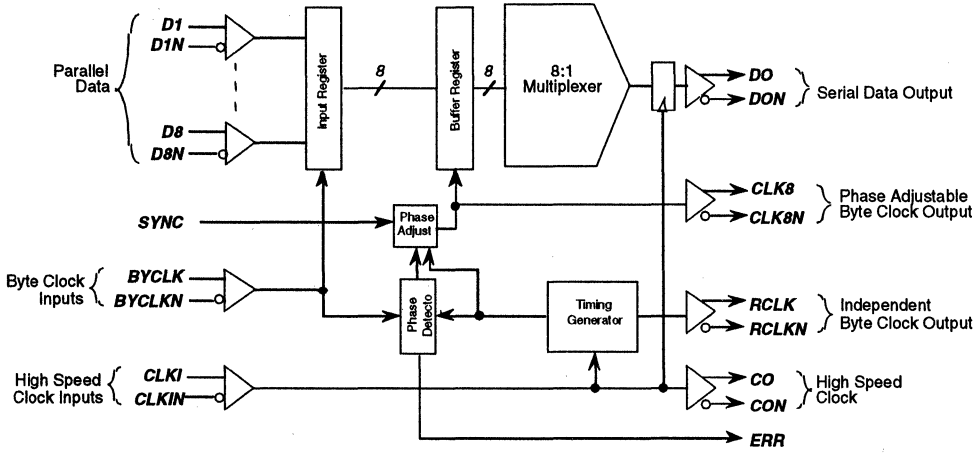
Internal circuitry monitors the internal and external byte clocks and generates an ERR signal if a timing violation is detected. This signal can be gated to the SYNC input which is edge sensitive high. An active SYNC input allows the VS8021 timing to shift, positioning it properly against the external byte clock, CLK8, CLK8N. When a CLK8 timing switch is made, normal data flow will be invalid for 1 byte.

There are two clock inputs, namely the CLKI and BYCLK, going into the VS8021. These two clocks serve as timing references for different parts of the VS8021. The BYCLK is used to trigger the input registers for the parallel data inputs, while the CLKI is used to trigger the high speed serial output register as well as some of the timing circuitry for the parallel to serial conversion. Furthermore, in order to make this part easy to use, the user is not required to assume a known phase relationship between CLKI and the BYCLK.

An internal Phase Detector and Phase Adjust Circuit are used to facilitate the two asynchronous circuits to work with each other. The Phase Detector and the Phase Adjust Circuit work together to adjust the internal clock CLK8 to make sure the set up and hold conditions are met for the internal registers. CLK8 is derived from CLKI and the RCLK is a non-phase varying byte clock output. The edge sensitive SYNC signal is simply the control signal that enables the Phase Detector circuitry.

As a summary, the CLKI is the high speed clock input. The BYCLK is the external byte clock. The CLK8 is the internal byte clock derived from CLKI, phase-adjusted if SYNC is enabled. The RCLK is a non-phase-adjusted divided-by-8 clock generated from CLKI. The phase of RCLK, RCLKN is not affected by the self-adjusting circuitry, therefore it can be used as a system reference clock. RCLK, RCLKN can be used by the system designer to generate BYCLK, BYCLKN. The self-positioning timer and RCLK, RCLKN allow for the creation of very tight parallel data timing for the VS8021.

Figure 1: VS8021 Block Diagram



Data Sheet

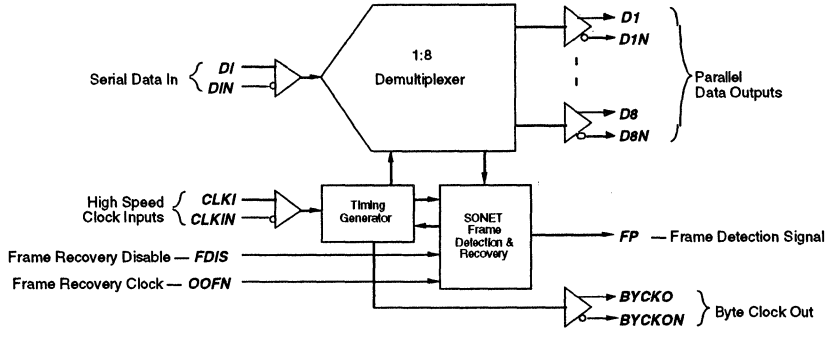
2.5 Gbits/sec SONET Compatible
8-bit Mux/Demux Chipset

VS8022

The VS8022 contains both a 1:8 demultiplexer and SONET frame recovery circuitry. The 1:8 demultiplexer accepts a serial data input (DI, DIN) at rates up to 2.5 Gbits/second and converts it into 8 parallel differential ECL data outputs (D1-D8, D1N-D8N) at rates up to 312.5 Mbits/sec. Valid parallel data outputs are indicated by the divide by 8 differential clock outputs BYCKO, BYCKON.

The VS8022 also contains a SONET frame recovery circuit. The frame recovery circuits are enabled by a falling edge on the OOFN ECL input when the FDIS input is low. Once enabled, the frame recovery circuit starts looking for the SONET framing sequence. Once the frame is detected, the word boundary is realigned, a confirmation signal is sent off-chip through the FP ECL output and the frame recovery circuits are disabled. While the frame aligner is hunting for the frame, BYCKO, BYCKON and parallel data are invalid.

Figure 2: VS8022 Block Diagram



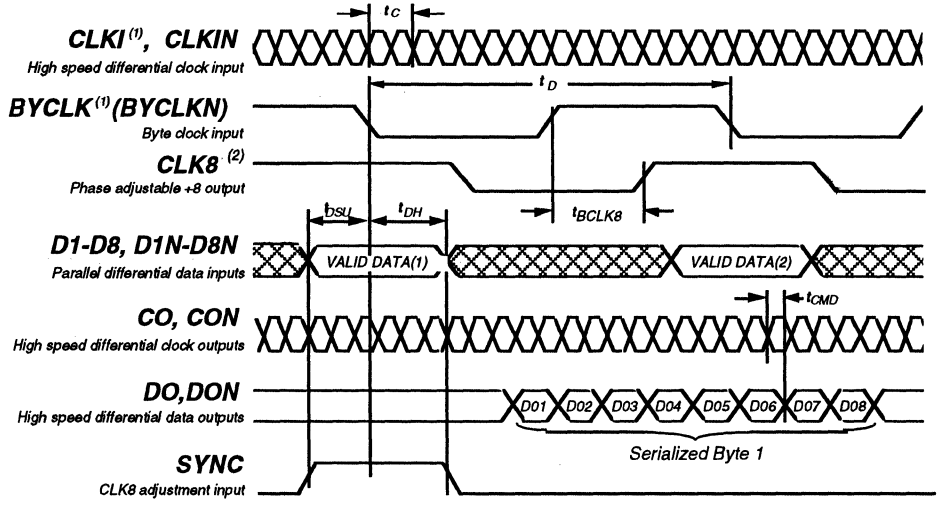
Frame recovery circuits are disabled by frame detection (resulting in FP) or by a falling edge on the OOFN input while FDIS is high.

VS8021 Multiplexer AC Characteristics *(Over recommended operating conditions)*

Parameter	Description	Min	Typ	Max	Units
t_C (1)	Clock period	400	-	-	ps
t_D	BYTE clock period ($t_D = t_C \times 8$)	3.2	-	-	ns
t_{DSU}	Parallel data set-up time	0.6	-	-	ns
t_{DH}	Data hold time	1.4	-	-	ns
t_{CMD}	High speed clock output (CO, CON) timing, falling edge of CO to muxed data output, (DO, DON) timing	220	-	350	ps
t_{BCLK8} (2)	Byte clock to CLK8 timing	0.5	1.0	1.5	ns
jitter(pk-to-pk)	CLKI, CLKIN to DO, DON (max-min), (HI to LO), same part, same pin at constant conditions	-	<50	-	ps

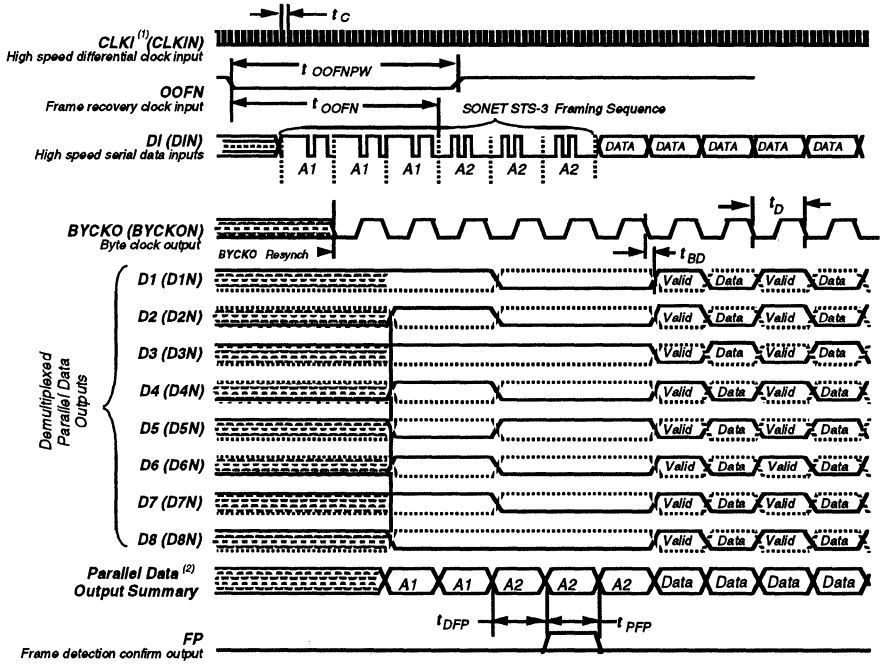
Note: (1) The parts are guaranteed by design to operate from DC to a maximum frequency of 2.5 GHz.
(2) Required when SYNC not connected to ERR

Figure 3: VS8021 Multiplexer Waveforms



NOTES: (1) Negative edge is active edge.
(2) BYCLK/CLK8 timing required when SYNC not connected to ERR.
***CLKI (CLKIN)** period x 8 = **BYCLK (BYCLKN)** period.*
= Don't care.

Figure 4: VS8022 Demultiplexer Waveforms



NOTES:

1) Negative edge is active edge.

2) The parallel data outputs only begin showing valid data after the last A2 of the SONET framing sequence. The example waveforms shown above use an STS-3 framing sequence for convenience, thus valid data is output after the third A2 in the sequence.

XXX = *Don't care.*

VS8022 Demultiplexer AC Characteristics *(Over recommended operating conditions)*

Parameter	Description	Min	Typ	Max	Units
t_C	Clock period *	400	-	-	ps
t_D	BYTE clock period ($t_D = t_C$ x 8) (framed)	3.2	-	-	ns
t_{BD}	BYTE clock output to valid data	0.5	1.0	2.0	ns
t_{DFP}	FP rising edge from parallel data output change from A1 to A2 ($t_{DFP} = t_D$)	-	3.2	-	ns
t_{PFP}	FP pulse width ($t_{PFP} = t_D$)	3.2	-	-	ns
t_{OOFN}	OOFN falling edge before A1 changes to A2 ($t_{OOFN} = t_D$ x 4)	12.8	-	-	ns
t_{OOFNPW}	OOFN pulse width ($t_{OOFNPW} = t_D$)	3.2	-	-	ns
Phase Margin	Serial data phase timing margin with respect fo high speed clock: *Phase Margin* = $\left(1 - \frac{t_{SU} + t_H}{t_C}\right)360°$	135	180	-	degrees

Note: If t_c changes, all the remaining parameters change as indicated by the equations.

VS8022 SONET Frame Recovery and Detection

The SONET framing sequence is a string of A1 bytes followed by a string of A2 bytes. (A1 = 11110110 and A2 = 00101000) The first serial bit starts at the left of the byte. The table below shows the number of A1 and A2 bytes in each SONET frame for different line rates. The VS8022 contains a frame recovery circuit and a frame detection circuit..

STS Level	Line Rate (Mb/s)	# of A1 Bytes	# of A2 Bytes
STS-3	155.520	3	3
STS-12	622.080	12	12
STS-48	2488.32	48	48

Frame Recovery Circuit

The frame recovery circuit is designed to scan the serial data stream, looking for the A1 byte. When it finds the A1 pattern, it adjusts internal timing so that the serial data is properly demultiplexed onto the eight parallel outputs. Subsequently, the MSB of the A1 byte will appear in the D1 position and LSB of the A1 byte will appear in the D8 position. This word boundary alignment causes the BYCKO, BYCKON output to be resynchronized. While the frame aligner is hunting for the frame, BYCKO and parallel data are invalid. Frame recovery circuits are disabled by frame detection (resulting in FP) or by a falling edge on the OOFN input while FDIS is high.

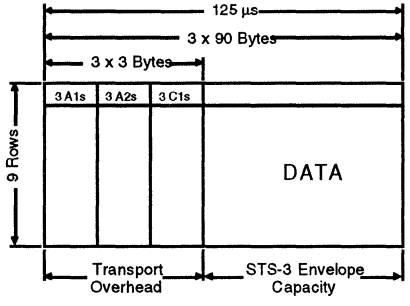
Frame Detection Circuit

The frame detection circuit monitors the demultiplexed data, and senses the boundary between A1 and A2 bytes. This pulse on the FP output will reset the frame recovery circuit, so that no further resynchronization will occur until permission is given through OOFN.

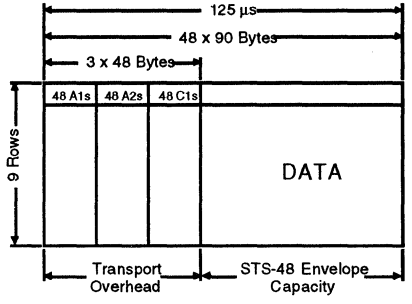
Circuit Operation

The frame recovery circuits are initialized and enabled on the falling edge of the OOFN ECL input with FDIS held low. The OOFN must be at least one byte clock period wide. It must occur at least four byte clock periods before the A1/A2 boundary. The circuit requires at least three A1 bytes followed by 3 A2 bytes for successful alignment. The first A1 byte is used by the frame recovery circuit to obtain initial word boundary alignment, while the following two A1 and three A2 bytes are used to reset the frame recovery circuit and maintain alignment for the subsequent bit stream. Frame recognition will occur for each word boundary aligned A1A1A2A2A2 sequence in the data stream. Frame recognition is signaled by a one byte clock period high pulse on the FP ECL output pin. This FP pulse will appear one byte period after the first A2 byte appears on the parallel data output pins.

STS-3 Frame



STS-48 Frame



Note: A1's and A2's: SONET framing sequence
C1's: STS Frame ID

Telecom/ATM

Absolute Maximum Ratings(1)

Power Supply Voltage (V_{TT}) ..... -3.0V to + 0.5V
Power Supply Voltage (V_{EE}) ..... V_{TT} + 0.7V to -6.0V
ECL Input Voltage Applied (2) (V_{ECLIN}) ..... -2.5V to + 0.5V
High Speed Input Voltage Applied (2) (V_{HSIN}) ..... V_{EE} -0.7V to V_{CC} + 0.7V
Output Current (DC, output HIGH) (I_{OUT}) ..... -50 mA
Case Temperature Under Bias (T_C) ..... -55° to + 125°C
Storage Temperature (3) (T_{STG}) ..... -65° to + 150°C

Recommended Operating Conditions

ECL Power Supply Voltage (4) (V_{TT}) ..... -2.0V ± 0.1V
Power Supply Voltage (V_{EE}) ..... -5.2V ± 0.26V
Operating Temperature Range (3) (T) ..... (Commercial) 0° to 70°C, (Industrial) -40° to + 85°C

Notes: (1) Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

(2) V_{TT} must be applied before any input signal voltage magnitude ($|V_{ECLIN}|$ and $|V_{HSIN}|$) can be greater than $|V_{TT}$ -0.5V.|

(3) Lower limit of specification is ambient temperature and upper limit is case temperature.

(4) When using internal ECL 100K reference level.

DC Characteristics

Table 1: Low Speed ECL Inputs and Outputs

(Over recommended operating range with internal V_{REF}, V_{CC} = GND, Output load = 50 Ω to -2.0V)

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-1020	-	-700	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
V_{OL}	Output LOW voltage	V_{TT}	-	-1620	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
V_{IH}	Input HIGH voltage	-1150	-	-600	mV	Guaranteed HIGH signal for all inputs
V_{IL}	Input LOW voltage	V_{TT}	-	-1500	mV	Guaranteed LOW signal for all inputs
ΔV_{OUT}	Output voltage swing	0.8	1.0	1.4	V	Output load 50Ω to V_{TT}

Note: Differential ECL output pins must be terminated identically.

Table 2: Power Dissipation

(Over recommended operating conditions, V_{CC} = GND, outputs open circuit)

Parameter	Description	VS8021 (Min)	VS8021 (Typ)	VS8021 (Max)	VS8022 (Min)	VS8022 (Typ)	VS8022 (Max)	Units
I_{EE}	Power supply current from V_{EE}	-	400	600	-	450	600	mA
I_{TT}	Power supply current from V_{TT}	-	110	200	-	120	200	mA
P_D	Power dissipation		2.3	3.75	-	2.6	3.75	W

Table 3: High Speed Inputs and Outputs

(Over recommended operating conditions, V_{CC} = GND, Output load = 50 Ω to -2.0V)

Parameter	Description	Min	Typ	Max	Units	Conditions
ΔV_{IN}	Input voltage swing	0.8	1.0	1.2	V	AC Coupled
V_{OH}	Output HIGH voltage	-	-0.9	-	V	Output load, 50 Ω to -2.0V
V_{OL}	Output LOW voltage	-	-1.8	-	V	Output load, 50 Ω to -2.0V
$\Delta V_{OUT(data)}$	Output voltage swing for data	0.6	0.8	1.2	V	Output load, 50 Ω to -2.0V
$\Delta V_{OUT(clk)}$	Output voltage swing for clock	0.6	0.7	1.2	V	Output load, 50 Ω to -2.0V

Notes: 1) A reference generator is built in to each high speed input, and these inputs are designed to be AC coupled.

2) If a high speed input is used single-ended, a 150 pF capacitor must be connected between the unused high speed or complement input and the power supply (V_{TT}).

3) Differential high speed outputs must be terminated identically.

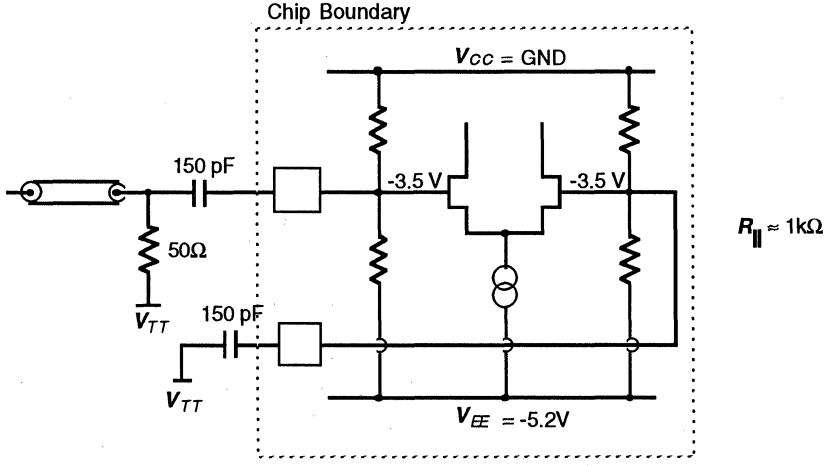
4) ESD protection is minimal for the high speed input pins, therefore, proper procedures should be used when handling this product

High Speed Inputs

In the past, the high speed inputs, which are typically used for serial data and high speed clock inputs with frequencies greater than 1Ghz, were specified with absolute minimum and maximum voltage values. Since these inputs are intended for AC coupled applications, they have been re-specified in terms of a voltage swing (ΔV_{IN}).

High speed clocks are intended for AC coupled operation. In most situations high speed serial data will have high transition density and contain no DC offsets, making them candidates for AC coupling as well. However, it is possible to employ DC coupling when the serial input data contains a DC component.

The structure of the high speed input circuit is shown below. DC coupled circuits may be used to operate this input provided that the input swing is centered around the reference voltage. Since the internal resistor divider which forms the -3.5V reference presents an attenuation factor of only 0.6 to the V_{EE} power supply, it is recommended that, in single-ended DC coupling situations, the user provide an external reference which has better temperature and power supply rejection than the simple on chip resistive attenuator. This external reference should have a nominal value of -3.5 V and can be connected to the complimentary input. This complication can be avoided in DC coupled situations by using differential signals.



Example Application: STS-48 SONET System Link

The objective in this example is to multiplex/demultiplex 8 channels at the STS-48 line rate with SONET frame recovery capability. The system can be implemented using the VS8021 and VS8022 as follows:

8:1 Multiplexer

Data at a line rate of 311.04 Mbytes/sec is registered at the inputs using the externally provided 311.04 MHz byte clock. ERR is gated into SYNC which is edge triggered for retiming of the input word. The 2488.32 MHz clock is used to generate timing signals for the mutiplexing function. The muxed output at 2488.32 Mbits/sec is generated at the serial data output of VS8021.

1:8 Demultiplexer

The 1:8 demultiplexer receives serial data at 2488.32 Mbits/sec and generates parallel data at 311.04 Mbytes/sec along with a byte clock output of 311.04 MHz. The demux also has the SONET frame recovery and detection circuitry.

During system start-up OOFN input receives a falling edge from the system control to permit recovery of the SONET frame and align on byte boundaries. Once the frame is aligned, the FP pulse is generated on every SONET frame. If for any reason the FP pulse disappears on frame boundaries then this signals the system that the frame synchronization is lost. The system then asserts the OOFN input (High to Low) to recover the SONET frame and align on byte boundaries, bringing the system back to a synchronized condition. After synchronization is achieved, the FP pulse starts again on every frame.

ESD Protection

Electrostatic discharge protection is provided for ECL I/O's and high speed clock and data I/O's to the following minimum limits:

ECL I/O *1000V*
High Speed Clock and Data Inputs *500V*

Figure 5: STS-48 SONET System Link

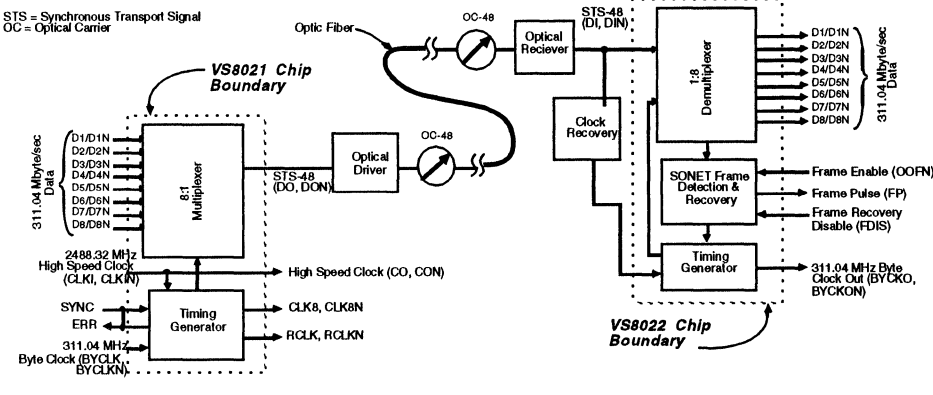


Figure 6: VS8021 Pin Diagram

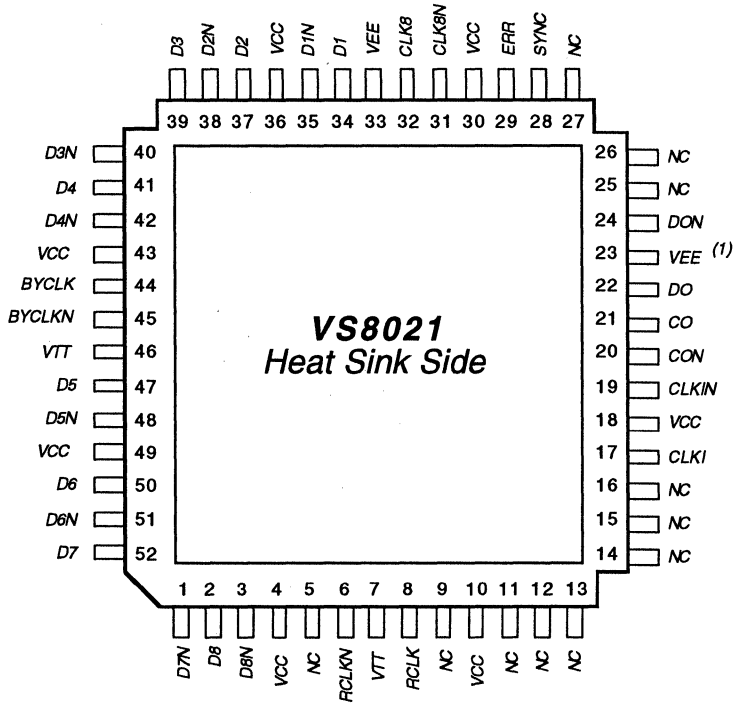


Table 4: VS8021 Pin Description.

Pin #	*Name*	*I/O*	*I/O Type*	*Description*
1-3, 34, 35, 37-42,47, 48, 50-52	D1-D8, D1N-D8N	I	ECL	Parallel ECL differential datas inputs
17, 19	CLKI, CLKIN	I	HS	High speed differential clock inputs
44, 45	BYCLK, BYCLKN	I	ECL	Divide by 8 clock ECL input
22, 24	DO, DON	O	HS	High speed serial data output
21, 20	CO, CON	O	HS	High speed differential clock output
32, 31	CLK8, CLK8N	O	ECL	Phase adjustable CLK ÷ 8 differential ECL clock output
8, 6	RCLK, RCLKN	O	ECL	Independent CLK ÷ 8 differential ECL clock output
29	ERR	O	ECL	Error detection ECL output
28	SYNC	I	ECL	Error correction ECL input
4, 10, 18, 30 ,36, 43, 49	V_{CC}			Ground connection
7, 46	V_{TT}			-2.0V supply for internal reference generation & low power logic
23(1), 33	V_{EE}			-5.2V supply for high speed logic
5, 9, 11-16, 25, 26, 27	NC			No connection

Note: 1) Pin #23 on both parts is connected to the heat sink. Connect to VEE or most negative chip voltage.

Figure 7: VS8022 Pin Diagram

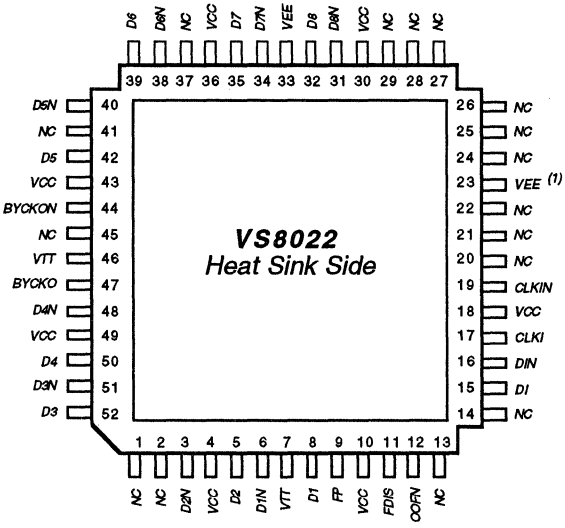


Table 5: VS8022 Pin Description

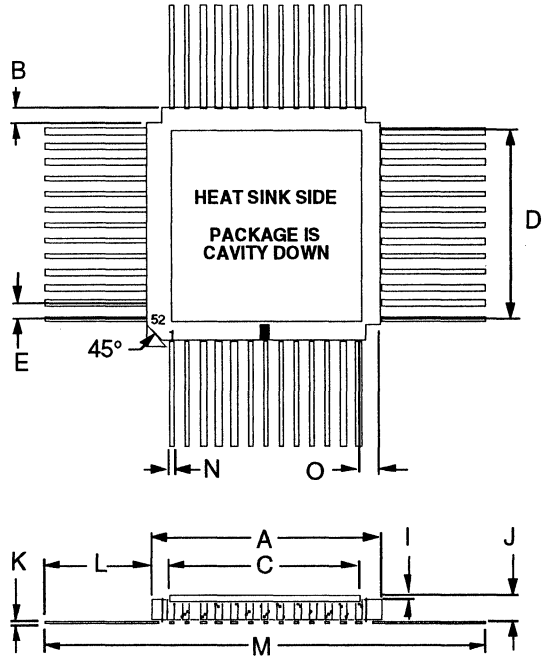
Pin #	*Name*	*I/O*	*I/O TYPE*	*Description*
3, 5, 6, 8, 31, 32, 34, 35, 38-40, 42, 48, 50-52	D1-D8, D1N-D8N	O	ECL	Parallel ECL differential data outputs
17, 19	CLKI, CLKIN	I	HS	High speed differential clock inputs
47, 44	BYCKO, BYCKON	O	ECL	Divide by 8 clock ECL outputs
15, 16	DI, DIN	I	HS	High speed differential serial data inputs
11	FDIS	I	ECL	Frame recovery disable input
12	OOFN	I	ECL	Frame recovery enable ECL input
4, 10, 18, 30, 36, 43, 49	V_{CC}	I		Ground connection
7, 46	V_{TT}			-2.0V supply for internal reference generation & low power logic
23(1), 33	V_{EE}			-5.2V supply for high speed logic
1, 2, 13, 14, 20-22, 24-29, 37, 41, 45	NC			No connection

Note: 1) Pin #23 on both parts is connected to the heat sink. Connect to VEE or most negative chip voltage.

Data Sheet

2.5 Gbits/sec SONET Compatible
8-bit Mux/Demux Chipset

Package Information



52-Pin Leaded
Ceramic Package (LDCC)

NOTES:
Drawing not to scale.
Packages: Ceramic (alumina);
Heat sink: Copper-tungsten;
Leads: Alloy 42 with gold plating.

Item	mm (Min/Max)	in (Min/Max)	Item	mm (Min/Max)	in (Min/Max)
A	18.54/19. 56	0.730/0.770	I	0.41/0.61	0.016/0.024
B	1.02/1.52	0.040/0.060	J	2.03/2.79	0.080/0.110
C*	15.49/16.51	0.610/0.650	K*	0.09/0.24	0.003/0.009
D*	15.24 TYP	0.600 TYP	L	4.57/5.34	0.180/0.210
E	1.27 TYP	0.050 TYP	M	27.69/30.22	1.090/1.190
F	0.76/1.02	0.030/0.040	N	0.36/0.56	0.014/0.022
G	16.94 TYP	0.667 TYP	O	1.75/1.90	0.069/0.075
H	1.91/2.41	0.075/0.095	—	—	—

**At package body.*

DUT Boards

The VS8021/VS8022 DUT boards are special purpose circuit boards which provide a test bed suitable for evaluating the performance characteristics of the VS8021 8:1 Multiplexer or the VS8022 1:8 Demultiplexer in the 52 pin LDCC package.

The figure below is a schematic representation of these circuit boards. These boards provide a controlled impedance transmission line for all signals, and suitable decoupling for the power supplies. The signal traces have a characteristic impedance of 50Ω. All ECL input lines are terminated with 50Ω (chip resistor) as close to the device package pin as possible. The high speed inputs are also provided with 150pF blocking capacitors as shown. These capacitors are shorted in applications which require DC connection to these inputs. Signals are launched onto the circuit board and removed by means of SMA coaxial connectors. While the input signals are terminated, the output signals are provided open circuit and are intended to be terminated in the measuring instrument such as an oscilloscope.

Normally, the VS8021 and VS8022 circuits operate in an ECL environment with standard ECL power buses: 0V, -2V, -5.2V. In order to simplify interface to standard ground referenced test equipment, however, the circuit board power buses are offset so that the shield connectors are at ground voltage. The figure below shows the arrangement of the power supply decoupling capacitors. There is a 33 µF electrolytic capacitor, as well as several 0.01 µF ceramic capacitors across each power bus. The device to be tested is held in place with a pressure retaining fixture. The figures on the following two pages indicate the physical dimensions and the connections labels for the evaluation boards.

Figure 8: VS8021/VS8022 DUT Board Schematics

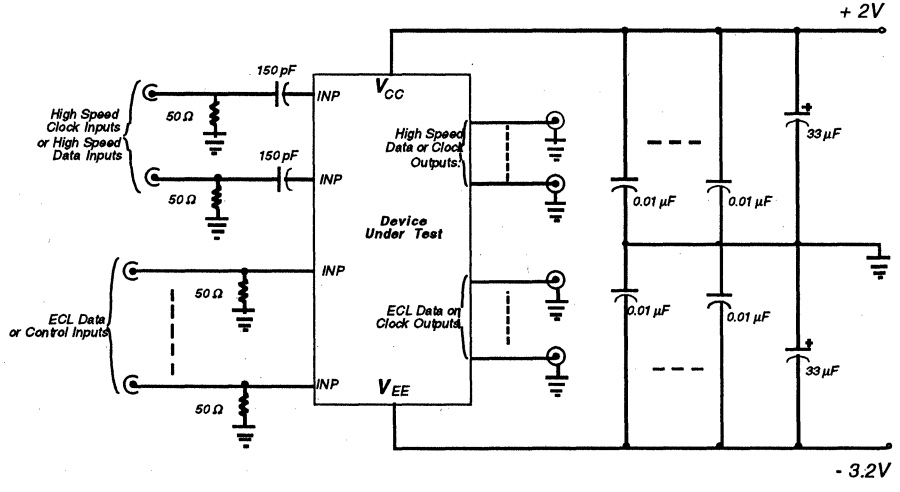


Figure 9: VS8021 DUT Dimensions and Connection Diagram

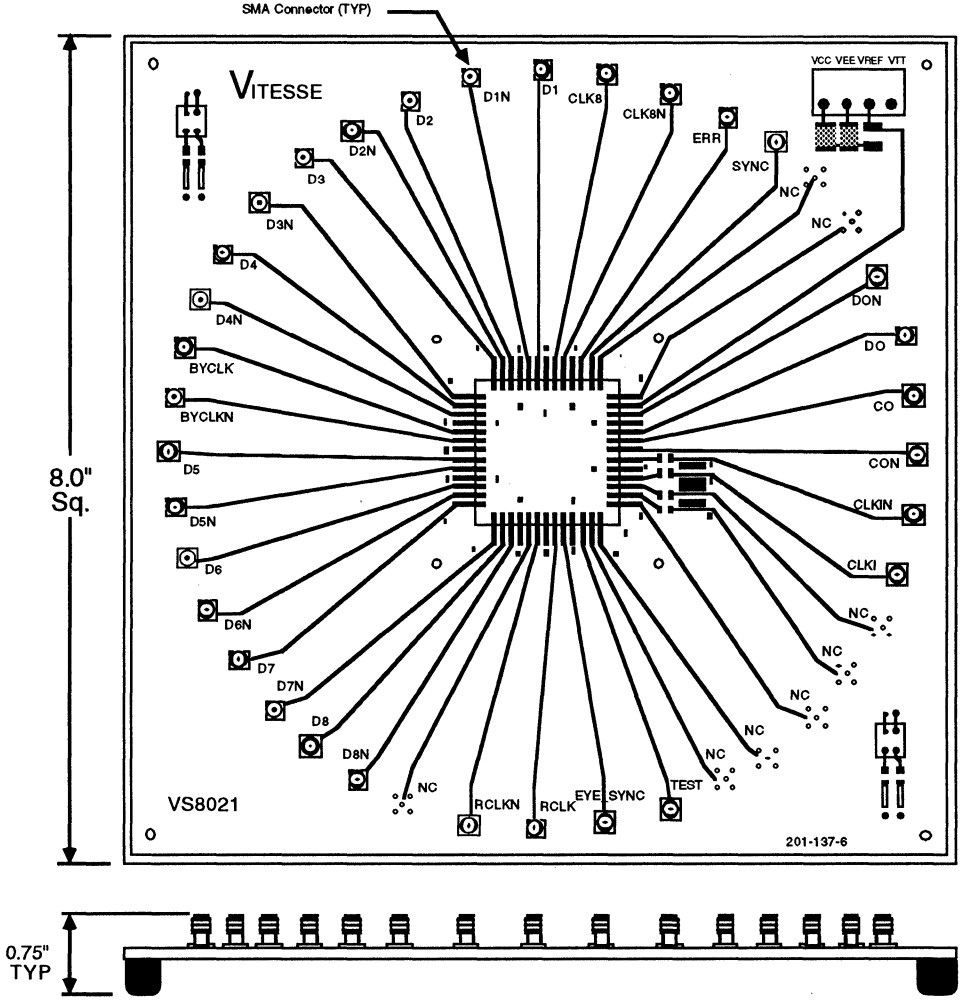
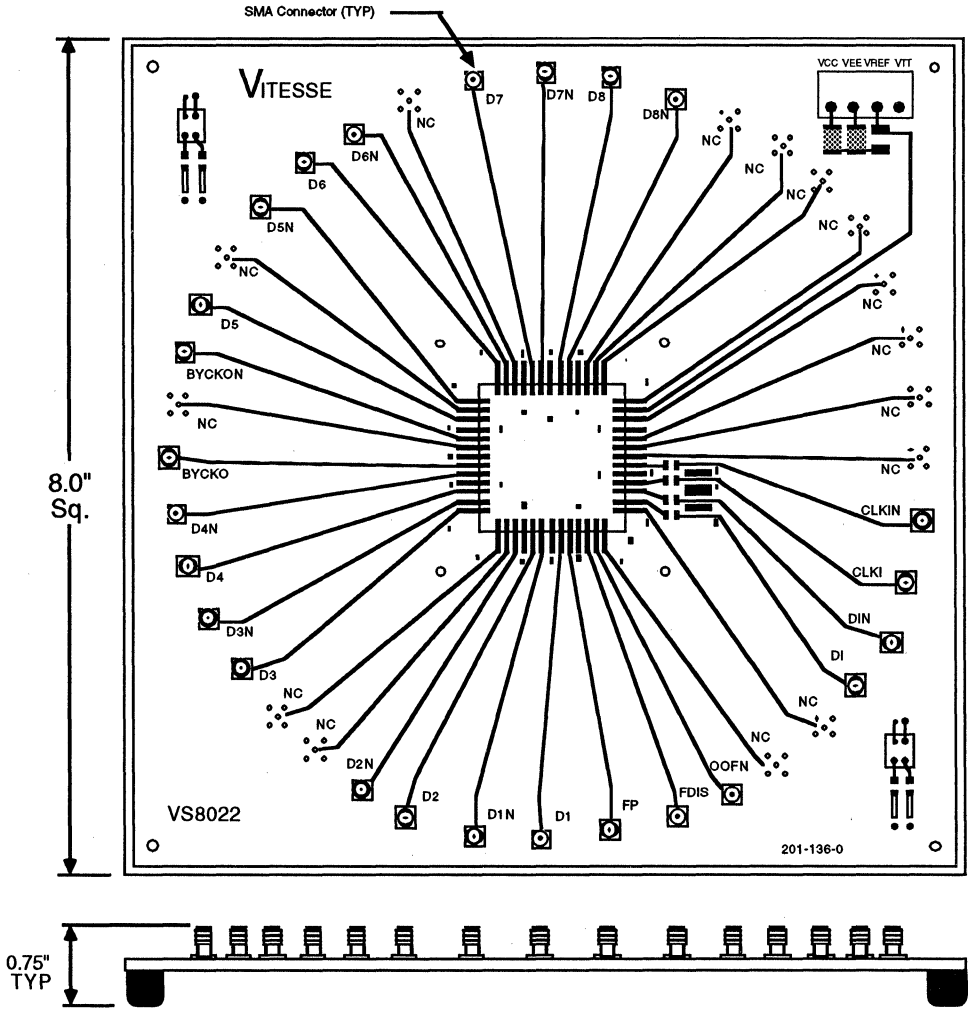


Figure 10: VS8022 DUT Dimensions and Connection Diagram



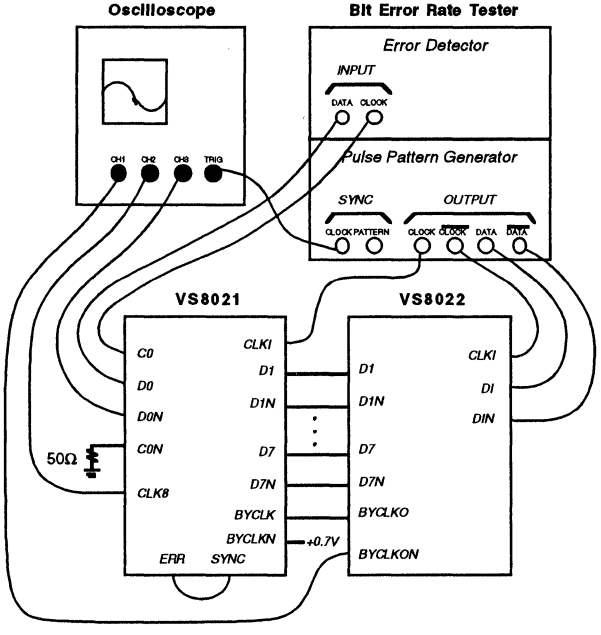
DUT Test Setup

Test equipment that is equal to or better than the following is recommended for testing the VS8021 and VS8022 DUT boards:

- 5 GHZ Oscilloscope
- 2.5 GHz Bit Error Rate Tester
- Power Supplies
  -3.2 V, 1 Amp per board
  +2.0 V, 1 Amp per board

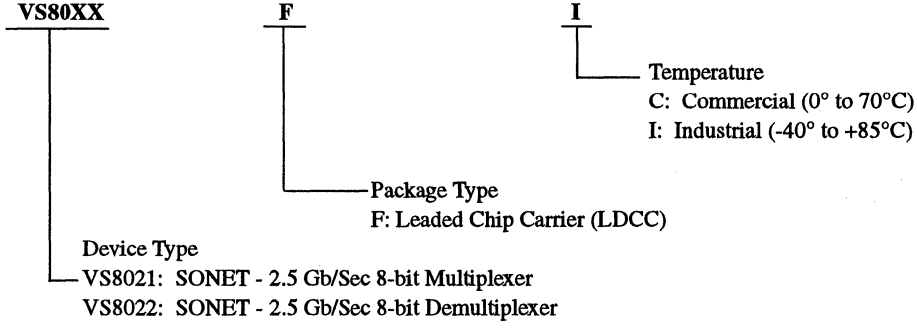
The figure below shows one possible test setup for the VS8021 and VS8022 DUT boards. In this configuration the Bit Error Rate Tester sends a clock and serial bit pattern into the VS8022 DUT board. This data is demultiplexed into a byte wide pattern which is transferred via matched cables to the VS8021 DUT board where the byte wide data is multiplexed into a serial bit stream which is sent into the error detector. The bit error rate tester will verify that the bit stream that is sent out of the generator matches the bit stream that is fed back into the error detector. Always use matched delay cables between complementary signals and between data and clock signals. The oscilloscope can be used to view signal integrity of various signals and to monitor rise and fall times.

Figure 11: VSC8021/8022 DUT Test Setup



Ordering Information

Vitesse products are available in a variety of packages and operating ranges. The order number for this product is formed by using a combination of the following: *Device Type, Package Type, and Operating Temperature Range.*



Notice

Vitesse Semiconductor Corporation reserves the right to make changes in its products, specifications or other information at any time without prior notice. Therefore the reader is cautioned to confirm that this datasheet is current prior to placing any orders. The company assumes no responsibility for any circuitry described other than circuitry entirely embodied in a Vitesse product.

Warning

Vitesse Semiconductor Corporation's product are not intended for use in life support appliances, devices or systems. Use of a Vitesse product in such applications without the written consent is prohibited.

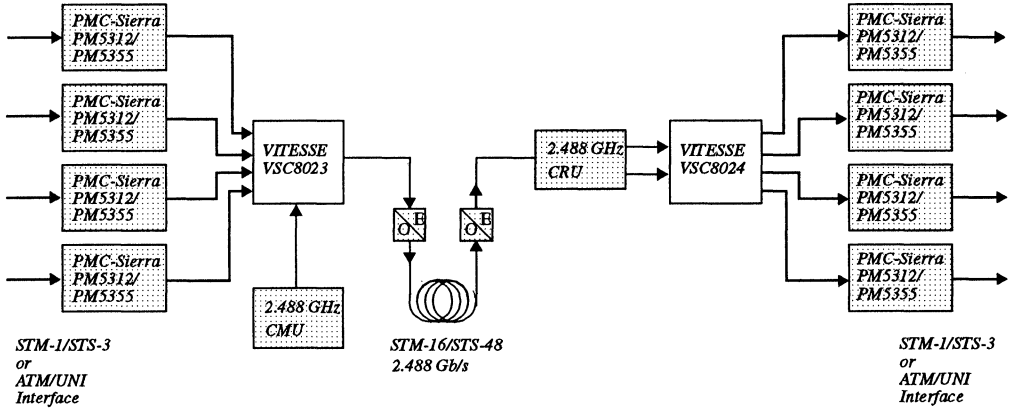
Preliminary Datasheet

2.488 Gbits/sec SDH/SONET STM-16/STS-48 Mux/Demux and Section Terminator IC Chipset

Features

- Interfaces with PMC-Sierra's PM5312/5355
- Supports STS-48c Mode (User Controlled)
- Optionally Combines Four STM-4/STS-12 Data Streams into One Serial STM-16/STS-48 Data Stream According to the SDH/SONET Spec for Intermediate-level Byte Interleaving
- Optionally Separates One Serial STM-16/STS-48 Data Stream into Four STM-4/STS-12 Data Streams According to the SDH/SONET Spec for Intermediate-level Byte De-interleaving
- Optionally Performs Frame Synchronous Scrambling and Descrambling
- Optionally Modifies J0 and Z0 Bytes (Mux)
- Supports Both Contra & Co-directional Interface Modes
- Optionally Calculates and Inserts the Bit-interleaved Parity-error Detection Code B1 into the Transmit Stream (Mux)
- Compares the B1 for the Receive Stream and Declares Errors (Demux)
- Frame Error and SEF Declaration (Demux)
- LOF Declaration for SDH or SONET Systems (Demux)
- Los Control Input (Demux)
- Provides Equipment And Facility Loopbacks
- High-speed Differential ECL I/O
- Dual Supply Operation -2, +3.3 Volts
- 192 TBGA Package

System Block Diagram



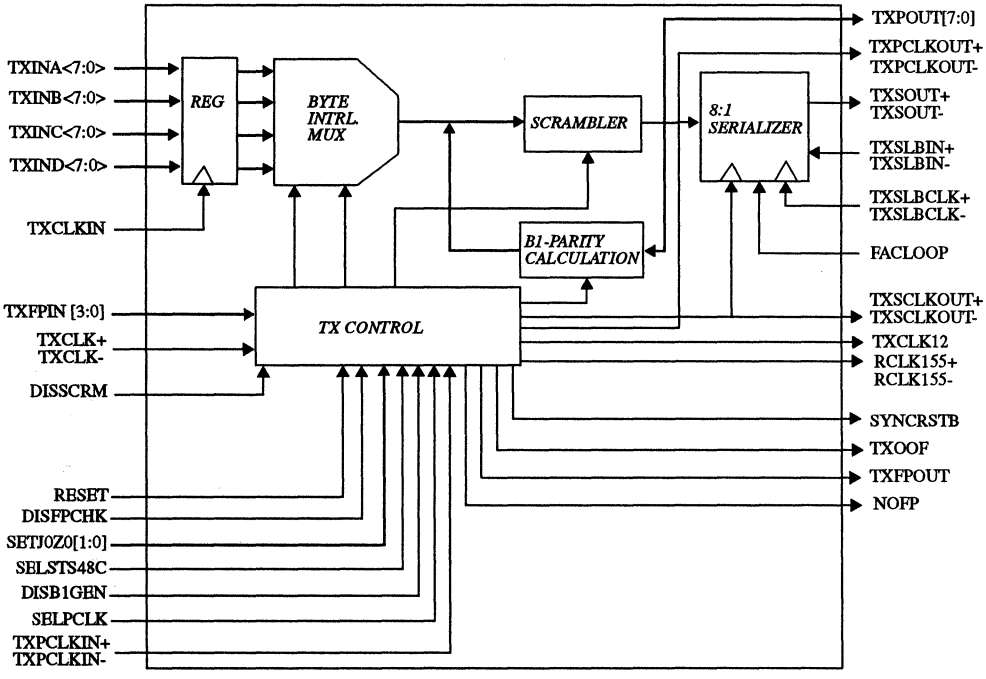
General Description

The VSC8023/VSC8024 chipset is designed to provide a SDH/SONET compliant interface between the PM5312 STTX (STM-1/STS-3 to STM-3/STS-12 mux/demux) or the PM5355 S/UNI-622 User Network Interface device and a SDH/SONET compliant 2.488 Gb/s interface, as depicted in the system block diagram above. This chipset allows one to create an ATM-UNI or STM-1/STS-3 to STM-16/STM-48 link. Both the mux (VSC8023) and the demux (VSC8024) are packaged in a 192TBGA for optimum high-speed package performance. The VSC8023/VSC8024 chipset provides an integrated solution for ATM physical layers, SDH/SONET transmission systems, digital-video distribution systems, and SDH/SONET test equipment.

VSC8023 Functional Description

The VSC8023 byte interleaves four 8-bit parallel STM-4/STS-12 data streams at 77.76MHz (from four PM5312s or four PM5355s) into a serial STM-16/STS-48 data stream at 2.488 Gb/s, consistent with the existing requirements for SONET intermediate-level multiplexing. (In order to support STS-48c, where no byte-interleaving is required, the byte-interleaver can be bypassed (straight forward muxing will occur instead) by holding the asynchronous SELSTS48C input high).

Figure 1: VSC8023 Functional Block Diagram

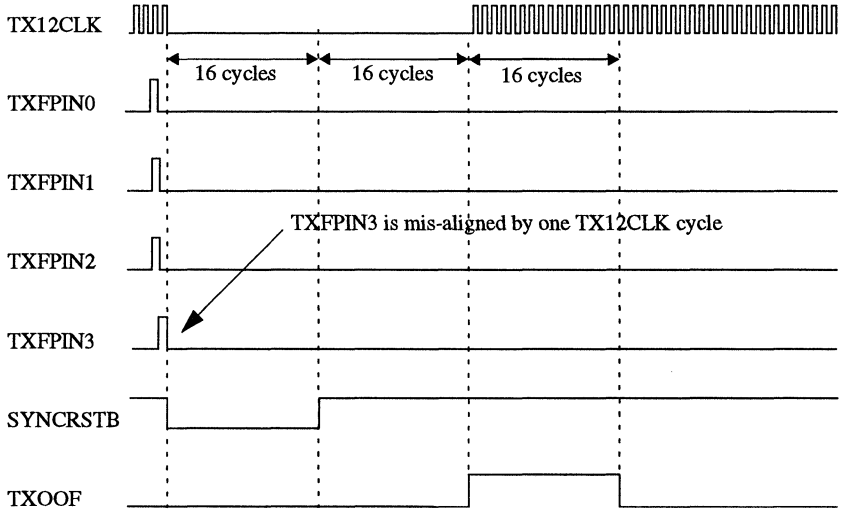


The part is clocked by a 2.488 GHz clock, which has to be provided by an external PLL. The VSC8023 is equipped with a 155.52 MHz differential ECL output clock, RCLK155+ and RCLK155-, to facilitate the creation of the external PLL circuit. The block diagram in Figure 1 shows the major functional blocks associated with the VSC8023.

Byte-wide data is presented to the TXINA<7:0>, TXINB<7:0>, TXINC<7:0>, and TXIND<7:0> input pins and is clocked into the part on the rising edge of TXCLKIN, as depicted in Figure 3. The four PM5312s or the four PM5355s each output a frame pulse aligned to the first payload byte of every frame, as shown in the functional timing diagram, Figure 3. The byte-interleave mux will be reset on the occurrence of the first valid frame pulse on TXFPIN[3:0] (active high). A valid frame pulse will only be detected if all four TXFPIN[3:0] inputs

are high at the same time. Therefore, if the four PM5312s or four PM5355s are not exactly byte aligned SYNCRSTB will be asserted low for sixteen 77.76 MHz (TXCLK12) clock cycles. TXCLK12 will be held low during these sixteen cycles and for an additional sixteen cycles thereafter. TXOOF will be held high for sixteen TXCLK12 cycles after the TXCLK12 clock starts running again to indicate that the CPU needs to reload the registers in the four PM5312s or four PM5355s. The frame-pulse check circuitry can be disabled by asserting the DISFPCHK input high. When the asynchronous DISFPCHK input is high, the output NOFP will be held high while no valid frame pulse can be detected. Please refer to Figure 2 for the Synchronous Reset timing. In Co-directional mode TXCLK12 is not connected to TXCLKIN.

Figure 2: Synchronous Reset Timing



The output of the byte-interleave mux is scrambled with the SDH/SONET scrambling polynomial $1 + x^6 + x^7$. The SDH/SONET scrambler can be disabled (on a frame wide basis only) by setting DISSCRM high. The value on the DISSCRM input is latched-in once every frame at the occurrence of the frame pulse. A logic '1' latched-in during the current frame will result in a non-scrambled current frame, and the frames thereafter.

The bit-interleaved parity byte B1 is calculated over the entire scrambled frame and inserted into the B1 location of the next frame before scrambling. This B1 generation can be disabled by setting the DISB1GEN input high. The value on this input is latched-in once every frame at the occurrence of the frame pulse. A logic '1' latched-in during the current frame will result in the B1 byte in the current frame, and in the frames thereafter, being passed on transparently.

The section-trace bytes (J0/Z0) can optionally be set to an increasing binary number from 01\hex to 30\hex by setting the SETJ0Z0[1:0] to '01'. A non-zero value on the SETJ0Z0[1:0] bus latched-in during the current

frame will result in a change of the J0/Z0 bytes in the next frame and the frames thereafter if the value on the SETJ0Z0[1:0] bus is not changed. When SETJ0Z0[1:0] is held at '00', the J0/Z0 bytes will be passed on transparently. Since the first section-trace byte, J0, could carry a section-trace message it can be passed on transparently while the Z0 bytes are set to an increasing binary number from 02\hex to 30\hex by setting SETJ0Z0[1:0] to '10'.

TXPOUT[7:0] is a parallel byte-wide STM-16/STS-48 output which can be used for an Equipment Loopback (see Figure 19) or to feed a STM-64/STS-192 MUX circuit. TXFPOUT contains a frame pulse synchronized with the parallel STM-16/STS-48 data rate. This frame pulse is aligned with the first payload byte in every STM-16/STS-48 frame. Data on TXPOUT[7:0] and TXFPOUT is clocked out on the falling edge of TXPCLKOUT+ (rising TXPCLKOUT-). When the VSC8023 is used to feed a STM-64/STS-192 MUX circuit (with byte wide data), the VSC8023 does not have to be supplied with a 2.488 GHz clock since the serial output mux is not used. Instead, a 311.04 MHz clock can be provided on the TXPCLKIN differential ECL input pins. The asynchronous SELPCLK input needs to be held high to select the TXPCLKIN.

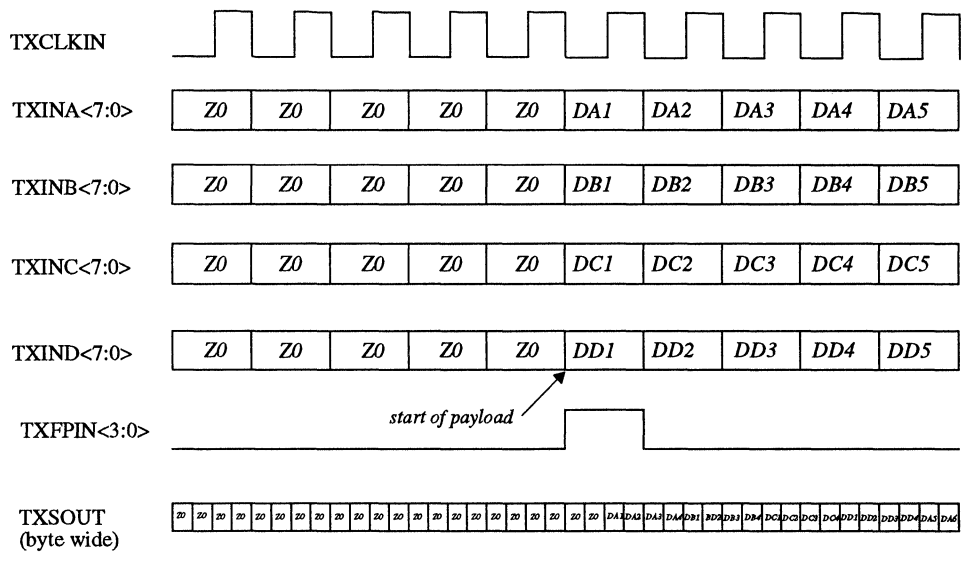
The serial STM-16/STS-48 data stream is presented at the differential TXSOUT output on the rising edge of TXSCLKOUT. To create a Facility Loopback, a high-speed clock (TXSLBCLK) and data (TXSLBIN) input have been provided. When the asynchronous FACLOOP input is held high, the data on TXSLBIN is clocked out through TXSOUT on the rising edge of the TXSLBCLK clock. Please refer to Figure 19 for a detailed Facility Loopback circuit diagram.

In order to support STS-48c, where no byte-interleaving is required, the byte-interleaver will multiplex one byte (from every STM-4/STS-12 data stream) at a time, instead of four bytes, by holding the SELSTS48C input high.

Table 1: Section-trace Byte Select Settings

SETJ0Z0[1]	*SETJ0Z0[0]*	*Function*
0	0	Transparent
0	1	J0 Transparent, Z0:02-30/hex
1	0	01-30/hex
1	1	Undefined

Figure 3: VSC8023 Functional Timing Diagram



Notes:

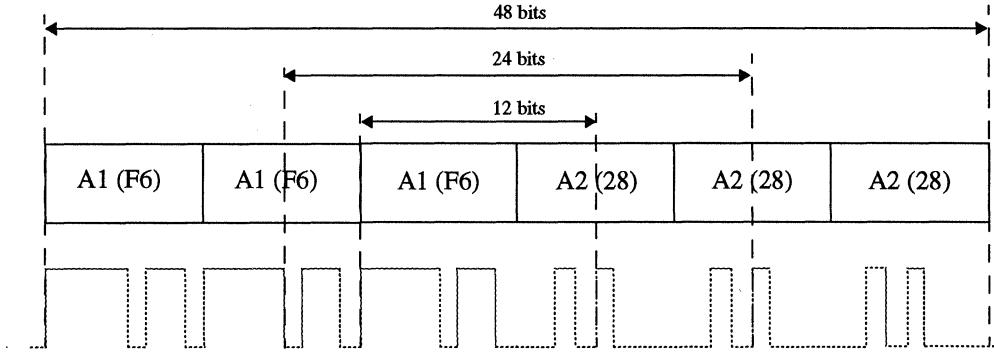
(1) The correct latency between the TXIN data-stream inputs and the TXSOUT data-stream output is NOT shown.
(2) MSB leads on TXSOUT; MSB is bit 7 on the TXINA, TXINB, TXINC and TXIND data busses.

Telecom/ATM

VSC8024 Functional Description

The VSC8024 deserializes a 2.488 Gb/s data stream into a byte-wide data stream and recovers the SDH/SONET frame boundary. The SDH/SONET frame boundary is found by detecting the inner-most 24 bits of the last two A1 bytes and the first two A2 bytes in each frame or three A1 bytes and three A2 bytes, as shown in figure 4, when the SELFRDET[1:0] input signals are held low. The frame recovery is initiated when FRDETEN is held high. This control signal is level-sensitive and the VSC8024 will continually perform frame detection as long as FRDETEN is held high.

Figure 4: Frame Boundary Detection Bits



A frame detect based on these 24 bits will result in a SEF (Severely Errored Frame) detect at an average of no more than once every 6 minutes assuming a BER of 10^{-3} as specified by the SONET Bellcore spec. As an option, one can also base the frame-boundary detect on either the three innermost A1 and the three innermost A2 bytes (48 bits) or on the last A1 byte and the first four bits of the first A2 byte (12 bits), based on the SELFRDET[1:0] settings shown in Table 2. A frame detect based on 48 or 12 bits will result in a mean time between SEF detects of 0.43 and 103 minutes, respectively. The frame-detection and recovery circuit can be disabled by holding both asynchronous SELFRDET[1:0] inputs high. In this mode, data is muxed to the output (scrambling, B1 insertion, B1 calculation, and error detection functions are disabled).

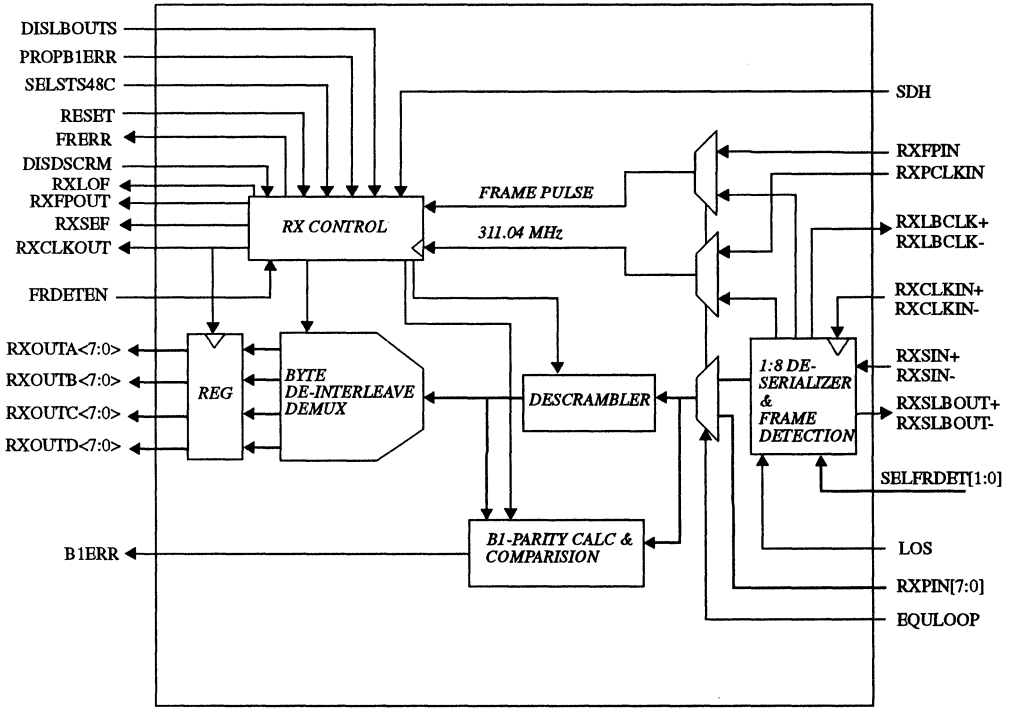
Table 2: Frame-detect Select Settings

Function	*SELFRDET1*	*SELFRDET0*
24 bits	1	0
48 bits	0	1
12 bits	0	0
Frame detection disabled	1	1

After the 1:8 Demux, the 8-bit parallel STM-16/STS-48 data stream at 311.04 MHz is byte de-interleaved into four 8-bit parallel STM-4/STS-12 data streams at 77.76 MHz (to four PM5312s or four PM5355s), consistent with the existing requirements for SDH/SONET intermediate level de-multiplexing. (In order to support STS-48c where no byte de-interleaving is required, the byte de-interleaver can be bypassed (straight forward demuxing will occur instead) by holding the asynchronous SELSTS48C input high). The part is clocked by a 2.488 GHz clock from the Clock and Data Recovery Unit (CRU). The block diagram in Figure 5 shows the major functional blocks associated with the VSC8024.

Serial STM-16/STS-48 data is presented at the differential RXSIN input on the rising edge of RXSCLKIN+; refer to Figure 12. In order to create a Facility Loopback the registered RXSIN data and the RXSCLKIN are brought out of the chip (RXSLBOUT and RXSLBCLK). These two signals should be connected to the TXSLBIN and TXSLBCLK inputs on the VSC8023 in order to create a Facility Loopback. RXSLBOUT and RXSLBCLK outputs were added to minimize the loading on the high-speed clock and data lines coming from the RX optics module. In order to minimize the jitter on the RXSIN and RXSCLKIN inputs during normal operation, the RXSLBOUT and RXSLBCLK outputs can be disabled by holding the asynchronous input DISHSOUTS high. Please refer to Figure 19 for a detailed Facility Loopback circuit diagram.

Figure 5: VSC8024 Functional Block Diagram



The incoming data is optionally descrambled with the SDH/SONET scrambling polynomial and byte de-interleaved into four byte-wide parallel data streams and presented on the RXOUTA<7:0>, RXOUTB<7:0>, RXOUTC<7:0>, and RXOUTD<7:0> output pins at the rising edge of RXCLKOUT; refer to Figure 6 for the functional timing of the receive circuit. The SDH/SONET de-scrambler is disabled (on a frame-wide basis only) by asserting DISDSCRM high. The value on the DISDSCRM input is latched-in once every frame at the occurrence of the frame pulse. If DISDSCRM is set high and latched in during the current frame, the current frame and all subsequent frames will remain scrambled until DISDSCRM is set low. On system reset, the chip will start off in the severely errored frame (SEF) state; RXSEF will be high. The byte de-interleaver will be reset on the occurrence of the first frame pulse from the SDH/SONET frame-detection circuit. The SEF will be removed when two consecutive error-free frames have been received. When errored frames are being received, SEF will be set high after four consecutive errored frames. Again, the SEF will be removed when two consecutive error-free frames have been received. The FRERR output will show a 25.72 ns wide pulse once every frame if the 12, 24 or 48 bits in the A1 and A2 frame ID bytes (used to recover the SDH/SONET frame boundary) contain one or more bit errors.

LOF (loss-of-frame) is declared (RXLOF output) after the chip has been in the SEF state for 3 ms (24 frames), for both SDH and SONET. The LOF state is cleared 1ms after terminating SEF Detect when in the SONET mode, or after only two good consecutive frames, when in the SDH mode. SDH mode is set by asserting the SDH input high. For loss-of-signal (LOS) conditions, the VSC8024 is equipped with a LOS control input. Asserting this input high will result in the propagation of all zeroes down-stream. In this mode, the VSC8024 is clocked by RXPCLKIN.

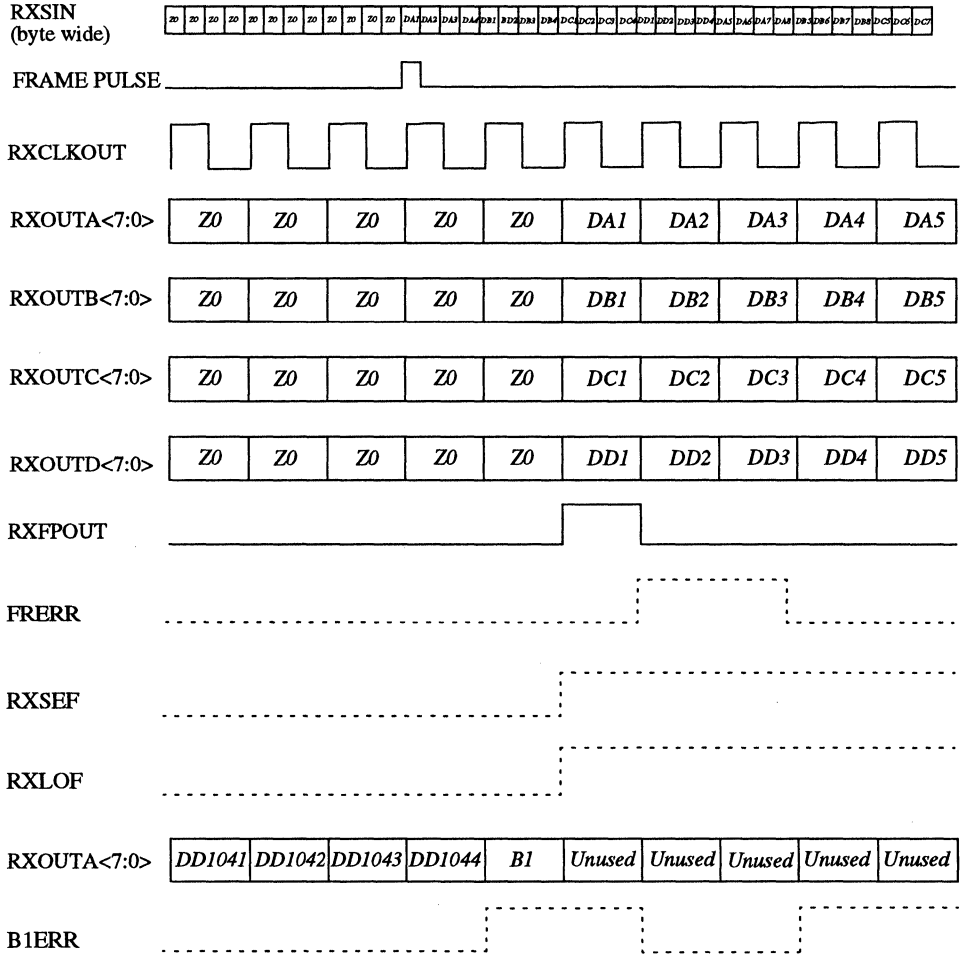
The bit-interleaved parity byte B1 will be recalculated before descrambling and compared to its extracted value after descrambling. The B1 bit errors will be presented on the B1ERR output as 25.72 ns wide pulses (up to 8 pulses per frame) and aligned at the start of the B1 byte of the current frame. Besides calculating the B1 over the entire STM-16/STS-48 frame, the VSC8024 optionally calculates the B1 based on the first STM-4/STS-12 frame interleaved into the STM-16/STS-48 frame when the PROPB1ERR input is held high. The value on the PROPB1ERR input is latched-in once every frame at the occurrence of the frame pulse. A logic '1' latched-in during the current frame will result in a non-modified $B1_{STS\text{-}12\#1}$ in the current frame and in the ones thereafter if PROPB1ERR remains high. This calculated $B1_{STS\text{-}12\#1}$ is XORed with the error-mask derived from XORing the extracted $B1_{STS\text{-}48}$ with the calculated $B1_{STS\text{-}48}$ over the entire STM-16/STS-48 frame. The result is inserted into the B1 byte position of the outgoing STM-4/STS-12 data stream RXOUTA[7:0]. This will make the B1 error count on the B1ERR output identical to the B1 error count in the first PM5312.

The VSC8024 can also receive byte-wide STM-16/STS-48 data from a STM-64/STS-192 Demux Circuit (or for loopback purposes from the VSC8023 byte-wide STM-16/STS-48 output) on the RXPIN[7:0] data bus. When SELPARIN is asserted high, the 1:8 Demux and the frame recovery circuit are bypassed. An external frame pulse aligned with the first payload byte in every frame has to be provided on the RXFPIN input. Data on RXPIN[7:0] and on RXFPIN is clocked into the VSC8024 on the rising edge of RXPCLKIN.

Preliminary Datasheet

2.488 Gbits/sec SDH/SONET STM-16/STS-48 Mux/Demux and Section Terminator IC Chipset

Figure 6: VSC8024 Functional Timing Diagram

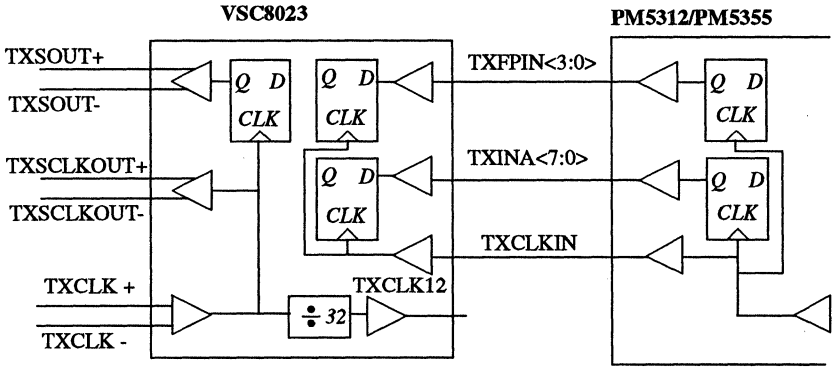


Notes:

(1) The correct latency between the RXSIN data-stream input and the RXOUT data-stream outputs is NOT shown.

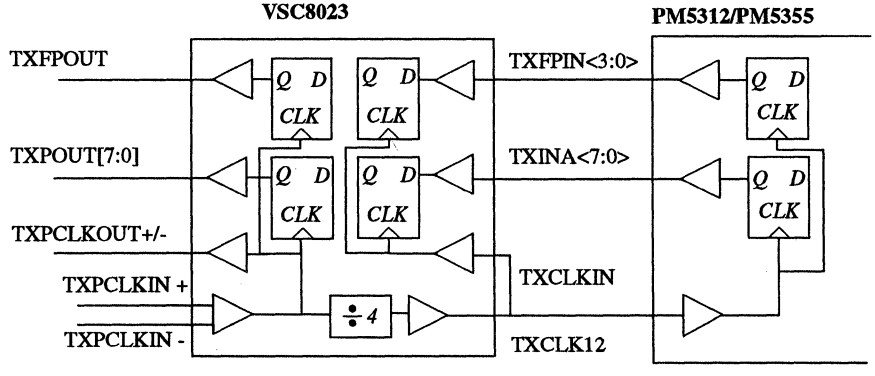
VSC8023 AC Timing Characteristics

Figure 7: VSC8023 Data and Clock Block Diagram (Serial Transmit & Co-directional Mode)



Note: TXINB<7:0>, TXINC<7:0>, and TXIND<7:0> inputs have been omitted for simplicity.

Figure 8: VSC8023 Data and Clock Block Diagram (Parallel Transmit & Contra-directional Mode)



Note: TXINB<7:0>, TXINC<7:0>, and TXIND<7:0> inputs have been omitted for simplicity.

Figure 9: VSC8023 Data Input Timing Diagram

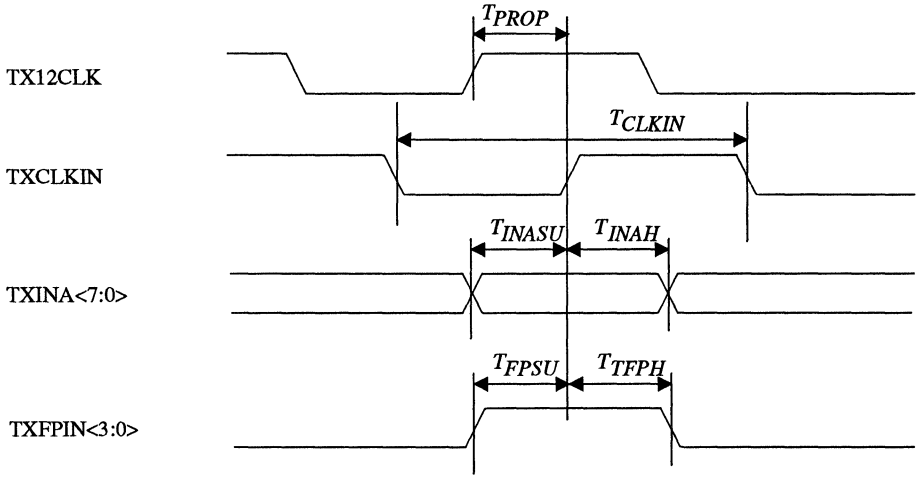
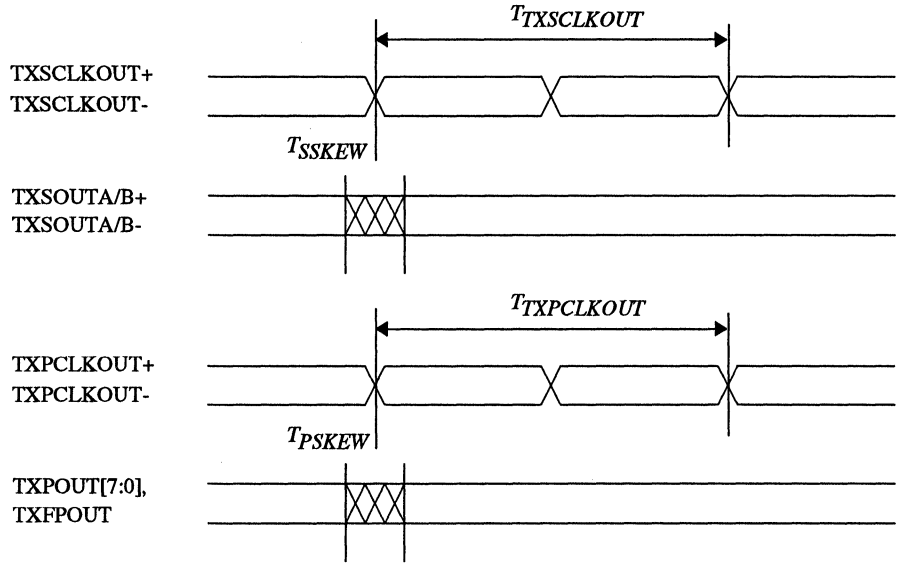


Table 3: VSC8023 Data Input Timing

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{TXCLK}	VSC8023 high-speed input clock period		401.9		ps
$T_{TXCLKIN}$	Transmit data input byte clock period	-	12.86	-	ns
$D_{TXCLKIN}$	Transmit data input byte clock duty cycle	TBD	50	TBD	%
T_{INASU}	TXINA<7:0> data setup time with respect to TXCLKIN	TBD	-	-	ns
T_{INAH}	TXINA<7:0> data hold time with respect to TXCLKIN	TBD	-	-	ns
T_{INBSU}	TXINB<7:0> data setup time with respect to TXCLKIN	TBD	-	-	ns
T_{INBH}	TXINB<7:0> data hold time with respect to TXCLKIN	TBD	-	-	ns
T_{INCSU}	TXINC<7:0> data setup time with respect to TXCLKIN	TBD	-	-	ns
T_{INCH}	TXINC<7:0> data hold time with respect to TXCLKIN	TBD	-	-	ns
T_{INDSU}	TXIND<7:0> data setup time with respect to TXCLKIN	TBD	-	-	ns
T_{INDH}	TXIND<7:0> data hold time with respect to TXCLKIN	TBD	-	-	ns
T_{FPSU}	TXFPIN<3:0> data setup time with respect to TXCLKIN	TBD	-	-	ns
T_{FPAH}	TXFPIN<3:0> data hold time with respect to TXCLKIN	TBD	-	-	ns
T_{PROP}	Maximum allowable propagation delay for connecting TX12CLK to TXCLKIN	-	-	TBD	ns

Figure 10: VSC8023 Serial and Parallel Data Output Timing Diagram



Note: TXSCLKOUT and TXPCLKOUT have not been drawn to scale.

Table 4: VSC8023 Serial and Parallel Data Output Timing

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
$T_{TXSCLKOUT}$	Serial Transmit clock period	-	401.9	-	ps
T_{SSKEW}	Skew between the falling edge of TXSCLKOUT and valid data on TXSOUTA/B	-	-	TBD	ps
$T_{TXPCLKOUT}$	Parallel Transmit clock period	-	3.215	-	ns
T_{PSKEW}	Skew between the falling edge of TXPCLKOUT and valid data on TXPFOUT[7:0] and on TXFPOUT	-	-	TBD	ps

Note: Duty cycle for TXSCLKOUT and for TXPCLKOUT is 50% +/- 5% worse case.

Figure 11: VSC8023 Facility Loopback Input Timing Diagram

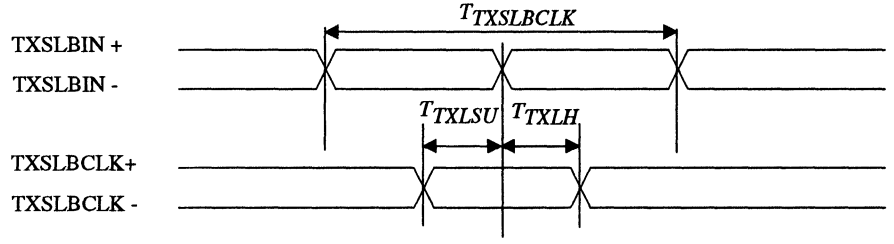


Table 5: VSC8023 Facility Loopback Input Timing

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
$T_{TXSLBCLK}$	Serial loopback clock period	-	401.9	-	ps
T_{TXLSU}	Serial loopback input data setup time with respect to rising edge of TXSLBCLK+	TBD	-	-	ps
T_{TXLSH}	Serial loopback input data hold time with respect to rising edge of TXSLBCLK+	TBD	-	-	ps

VSC8024 AC Timing Characteristics

Figure 12: VSC8024 Data and Clock Block Diagram (Serial Receive Mode)

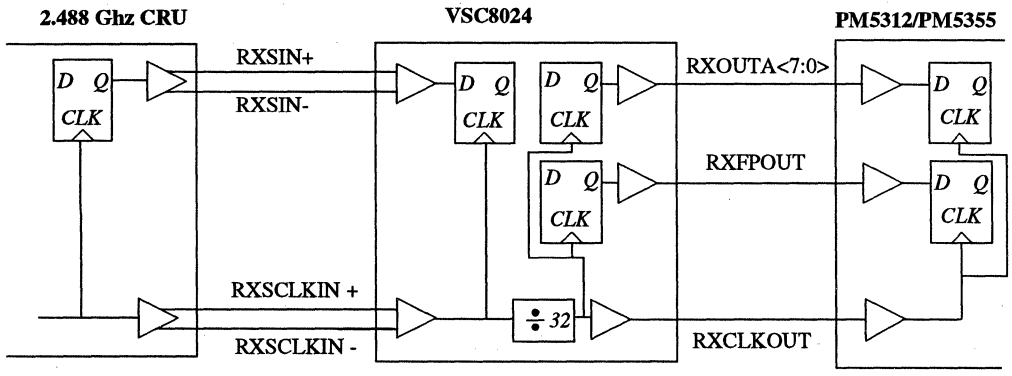


Figure 13: VSC8024 Data and Clock Block Diagram (Parallel Receive Mode)

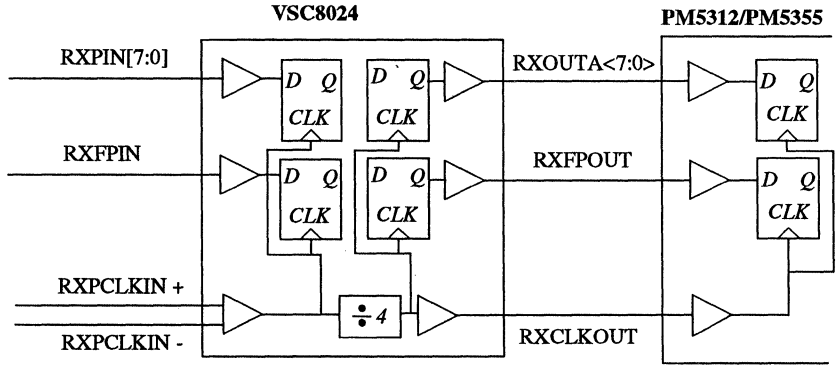
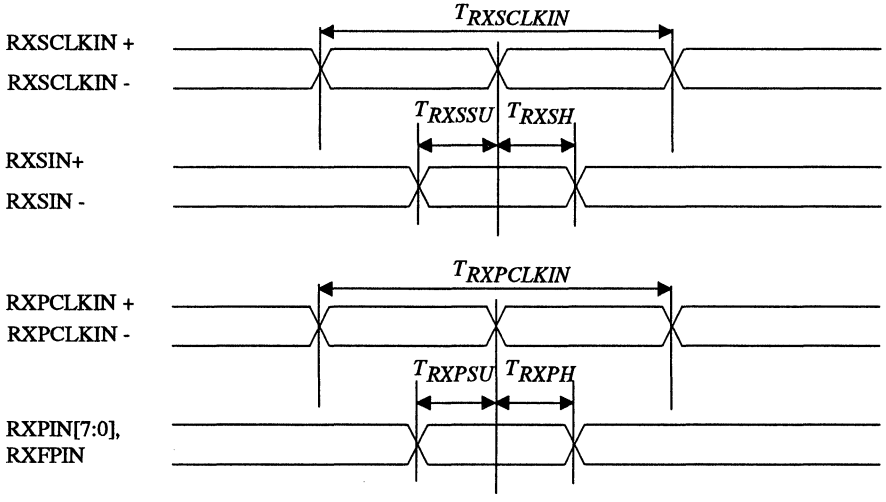


Figure 14: VSC8024 Serial and Parallel Data Input Timing Diagram

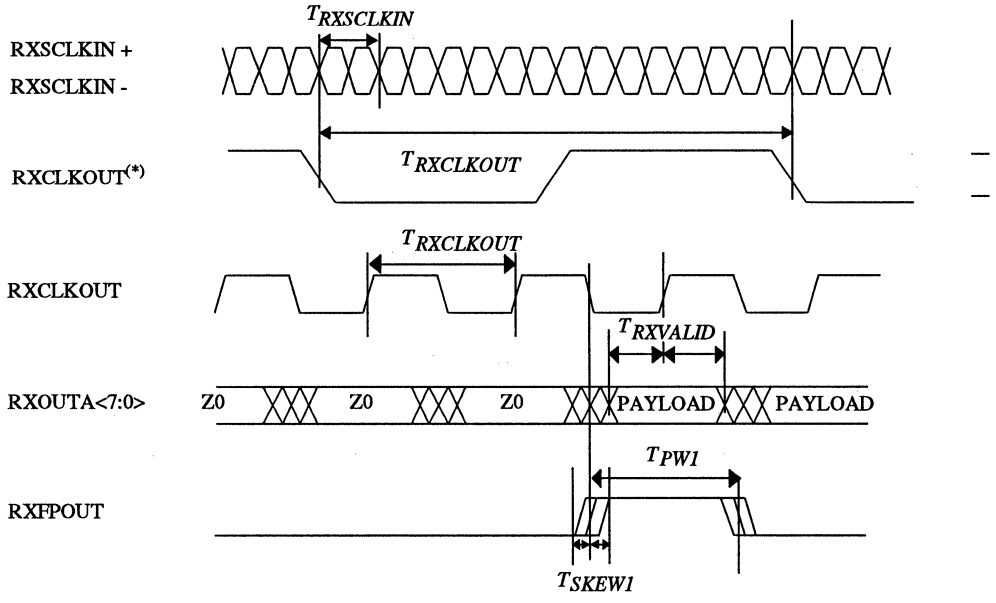


Note: RXSCLKIN and RXPCLKIN have not been drawn to scale.

Table 6: VSC8024 Serial and Parallel Data Input Timing

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
$T_{RXSCLKIN}$	Serial Receive clock period	-	401.9	-	ps
T_{RXSSU}	Serial Receive input data setup time with respect to rising edge of RXSCLKIN+	TBD	-	-	ps
T_{RXSH}	Serial Receive input data hold time with respect to rising edge of RXSCLKIN+	TBD	-	-	ps
$T_{RXPCLKIN}$	Parallel Receive clock period	-	3.215	-	ns
T_{RXPSU}	Parallel Receive input data setup time with respect to rising edge of RXPCLKIN+	TBD	-	-	ns
T_{RXPH}	Parallel Receive input data hold time with respect to rising edge of RXPCLKIN+	TBD	-	-	ns

Figure 15: VSC8024 Data Output Timing Diagram

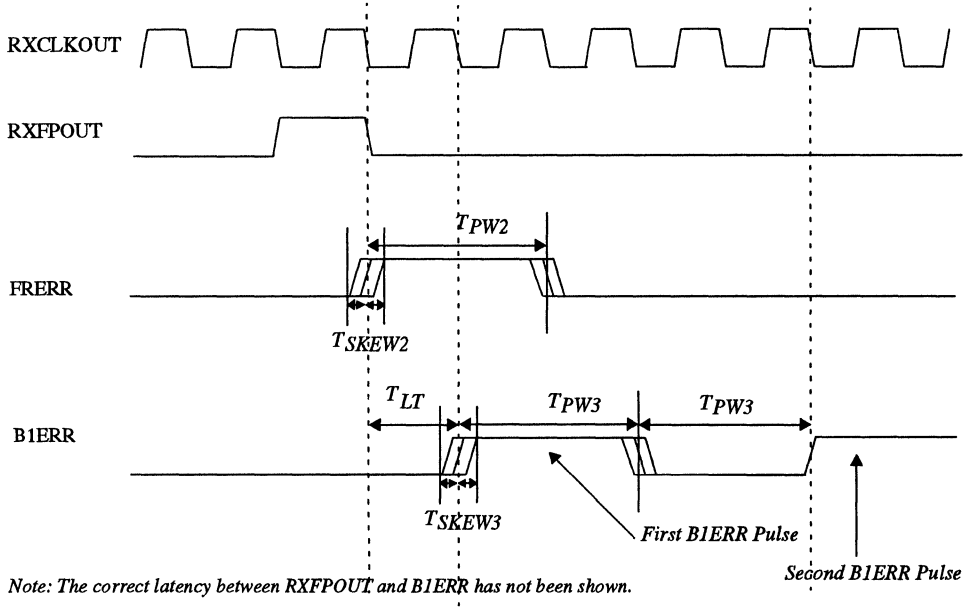


Note: RXSCLKIN and RXCLKOUT(*) have not been drawn to scale compared to the signals below them.

Table 7: VSC8024 Data Output Timing

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
$T_{RXSCLKIN}$	Serial Receive clock period	-	401.9	-	ps
$T_{RXCLKOUT}$	Receive data output byte clock period	-	12.86	-	ns
T_{SKEW1}	Range in which the rising edge of RXFPOUT will appear in relation to the falling edge of RXCLKOUT	-	-	TBD	ns
$T_{RXVALID}$	Time data on RXOUTA<7:0>, RXOUTB<7:0>, RXOUTC<7:0> and RXOUTD<7:0> is valid before and after the rising edge of RXCLKOUT	TBD	-	-	ns
T_{PW1}	Pulse width of frame detection pulse RXFPOUT	-	12.86	-	ns

Figure 16: VSC8024 Error Data Output Timing Diagram



Note: The correct latency between RXFPOUT and B1ERR has not been shown.

Table 8: VSC8024 Error Data Output Timing

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{SKEW2}	Range in which the rising edge of FRERR will appear in relation to the falling edge of RXCLKOUT	-	-	TBD	ns
T_{PW2}	Pulse width of frame error pulse FRERR	-	25.72	-	ns
T_{LT}	Latency between the rising edge of RXFPOUT and the rising edge of a B1ERR pulse	13.82	-	14.00	µs
T_{SKEW3}	Range in which the rising edge on B1ERR will appear in relation to the falling edge of RXCLKOUT	-	-	TBD	ns
T_{PW3}	Pulse width of B1 error pulse B1ERR	-	25.72	-	ns

Figure 17: VSC8024 Facility Loopback Output Timing Diagram

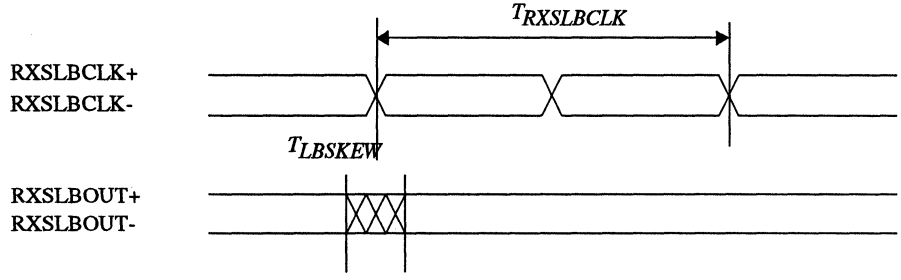


Table 9: VSC8024 Facility Loopback Output Timing

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
$T_{RXSLBCLK}$	Serial loopback clock period	-	401.9	-	ps
T_{LBSKEW}	Skew between the falling edge of RXSLBCLK and valid data on RXSLBOUT	-	-	TBD	ps

Preliminary Datasheet

2.488 Gbits/sec SDH/SONET STM-16/STS-48 Mux/Demux and Section Terminator IC Chipset

Absolute Maximum Ratings[1]

Power Supply Voltage (V_{TT}) Potential to GND ..... -2.5 V to +0.5 V
Power Supply Voltage (V_{TTL}) Potential to GND ..... -0.5 V to +4.3 V
TTL Input Voltage Applied ..... -0.5 V to + 5.5V
ECL Input Voltage Applied ..... +0.5 V to V_{TT} -0.5 V
Output Current (I_{OUT}) ..... 50 mA
Case Temperature Under Bias (T_C) ..... -55° to + 125°C
Storage Temperature (T_{STG}) ..... -65° to + 150°C

Note: Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Recommended Operating Conditions

Power Supply Voltage (V_{TT}) ..... -2.0 V±5 %
Power Supply Voltage (V_{TTL}) ..... +3.3 V±5 %
Commercial Operating Temperature Range* (T) ..... 0° to 70°C

** Lower limit of specification is ambient temperature and upper limit is case temperature.*

ESD Ratings

Proper ESD procedures should be used when handling this product. The VSC8023 and VSC8024 are rated to the following ESD voltages based on the human body model:

1. All pins are rated at or above 1500V.

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DC Characteristics

Table 10: ECL Inputs and Outputs

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-1020	-	-700	mV	50 ohm to V_{TT}
V_{OL}	Output LOW voltage	-2000	-	-1620	mV	50 ohm to V_{TT}
V_{IH}	Input HIGH voltage	-1165	-	-700	mV	Guaranteed HIGH signal for all inputs
V_{IL}	Input LOW voltage	-2000	-	-1475	mV	Guaranteed LOW signal for all inputs
I_{IH}	Input HIGH current	-	-	200	uA	$V_{IN}=V_{IH}$ (max)
I_{IL}	Input LOW current	-50	-	-	uA	$V_{IN}=V_{IL}$ (min)
V_{DIFF}	Input Voltage Differential	200	-	-	mV	
V_{CM}	Common Mode Voltage	-1.5	-	-0.5	V	

Note: Differential ECL output pins must be terminated identically.

Table 11: High-Speed Differential ECL Inputs and Outputs

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OD}	Output differential voltage	450	-	800	mV	
V_{OCM}	Output common-mode voltage	-1600	-	-1200	mV	
R_O	Output Impedance	3	-	7	ohms	Guaranteed, not tested.
V_{ID}	Input differential voltage	200	-		mV	
V_{ICM}	Input common-mode voltage	-1.5	-	-0.5	V	
V_{IT}	Input threshold matching	-25	-	25	mV	
V_{DIFF}	Input Voltage Differential	200	-	-	mV	
R_{IN}	Input resistance	40	-	60	ohms	

Table 12: TTL Inputs and Outputs

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{OH}	Output HIGH voltage	2.4	-	-	V	$V_{IN} = V_{IH}$ (max) or V_{IL} (min) I_{OH}=-2.4 mA
V_{OL}	Output LOW voltage	0	-	0.4	V	$V_{IN} = V_{IH}$ (max) or V_{IL} (min) I_{OL}=16 mA
V_{IH}	Input HIGH voltage	2.0	-	5.5	V	Guaranteed HIGH signal for all inputs
V_{IL}	Input LOW voltage	0	-	0.8	V	Guaranteed LOW signal for all inputs
I_{IH}	Input HIGH current	-	-	50	uA	$V_{IN}=V_{IH}$ (max)
I_{IL}	Input LOW current	-500	-	-	uA	$V_{IN}=V_{IL}$ (min)
I_{OZH}	3-State Output OFF current HIGH	-	-	200	uA	V_{OUT}=2.4 V
I_{OZL}	3-State Output OFF current LOW	-200	-	-	uA	V_{OUT}=0.5 V

Power Dissipation

Table 13: VSC8023 Power Supply Currents

Parameter	*Description*	*(Max)*	*Units*
I_{TT}	Power supply current from V_{TT}	TBD	mA
I_{TTL}	Power supply current from V_{TTL}	TBD	mA
P_D	Power dissipation	TBD	W

Note: Specified with outputs open circuit. The combined maximum currents (I_{TT} I_{TTL}) for any part will not exceed TBD Watts.

Table 14: VSC8024 Power Supply Currents

Parameter	*Description*	*(Max)*	*Units*
I_{TT}	Power supply current from V_{TT}	TBD	mA
I_{TTL}	Power supply current from V_{TTL}	TBD	mA
P_D	Power dissipation	TBD	W

Note: Specified with outputs open circuit. The combined maximum currents (I_{TT} I_{TTL}) for any part will not exceed TBD Watts.

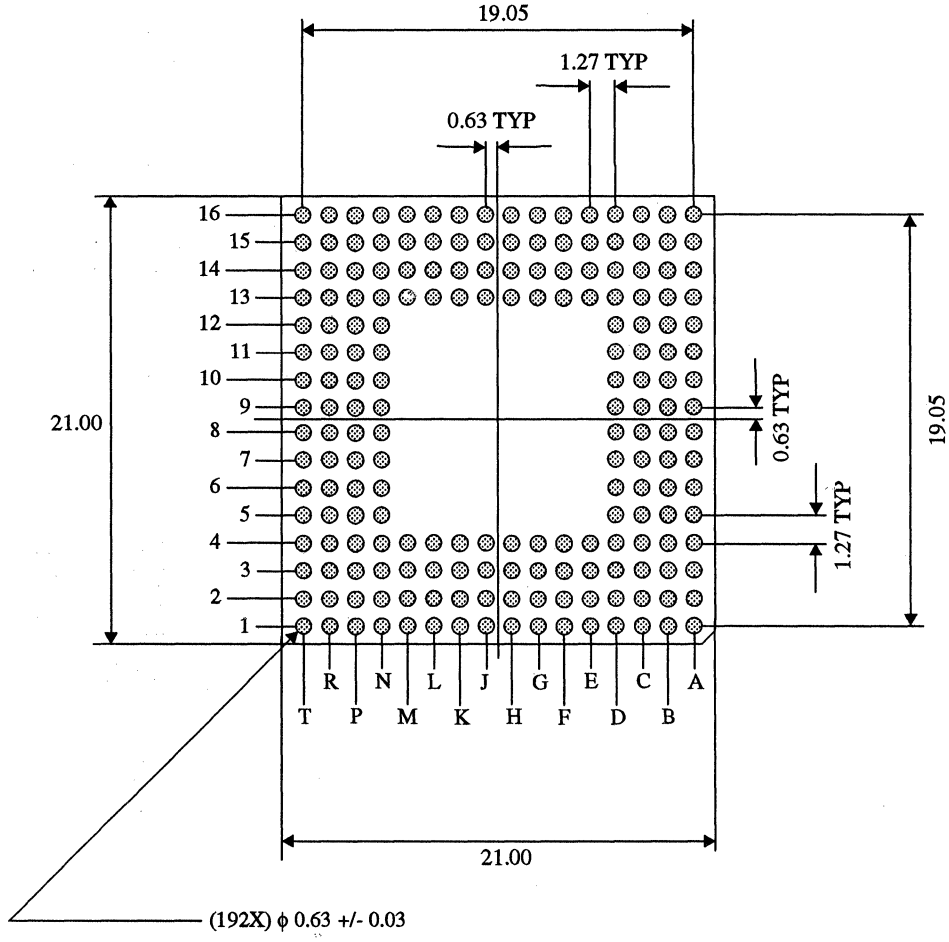
VSC8023 Package Pin Description

Table 15: TBD

VSC8024 Package Pin Description

Table 16: TBD

Figure 18: 192TBGA Package Drawing (Bottom View)



Notes:
(1) Drawings not to scale.
(2) All units in millimeters.

Application Notes

The byte clock (TXCLK12 and TXCLKIN) on the VSC8023 has been brought off-chip to allow as much flexibility in system-level clocking schemes as possible. Refer to figures 7 & 8 for connection examples.

Interconnecting the VSC8023 Byte Clocks (TXCLK12 and TXCLKIN)

Contra-Directional Connection:

In this mode, the byte clock (TXCLK12) clocks both the VSC8023 and the PMC devices. It is important to pay close attention to the routing of this signal. The PMC devices are CMOS parts which can have very wide spreads in timing (1 ns-11 ns clock in to parallel data out for the PM5355) which utilizes most of the 12.86 ns period (at 77.76 MHz), leaving little for the trace delays and set-up times required to interconnect the devices. The recommended way of routing this clock is to daisy chain it to the PMC device pins and then route it back to the VSC8023 along with the byte data. This eliminates the 1-way trace delay that would otherwise be encountered between the data and clock and thus leaves 1.86 ns for the VSC8023 setup time and for variations in trace delays and rise times between clock and data. The trace delay must be kept under 2 ns (allowing an additional 1 ns for variations in rise times and skews) to ensure proper muxing of parallel input data into the VSC8023; reference Table 2.

Co-Directional Connection:

In the co-directional mode an internal data synchronizing circuit is used to optimize the phase relationship between a supplied TXCLKIN and internal clocks. The TXCLKIN signal needs only to meet setup and hold timing relative to the data stream and frame pulses.

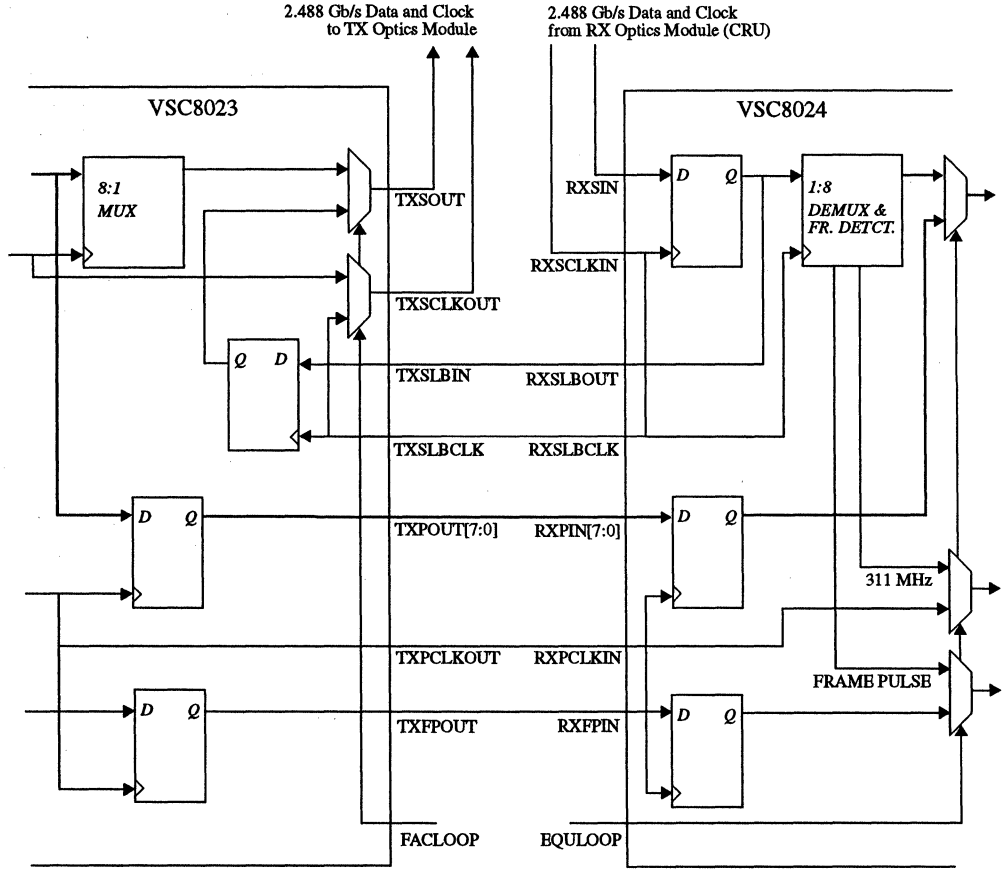
Equipment and Facility Loopbacks

In order to create an Equipment Loopback, the EQULOOP VSC8024 input is held high. The byte-wide STM-16/STS-48 data on the VSC8023 TXPOUT[7:0] outputs is clocked into the VSC8024 RXPIN[7:0] inputs with the TXPCLKOUT clock. A frame pulse aligned with the first payload byte on the TXPOUT[7:0] databus is provided to assure proper alignment. Both the Facility and the Equipment Loopbacks can be enabled simultaneously. It is possible to disable (hold at a logic low) the serial high-speed outputs on the VSC8024 by holding the DISLBOUTS input high.

Equipment and Facility Loopbacks

The diagram below (Figure 19) shows how an Equipment and a Facility Loopback are created. When in Facility Loopback mode (FACLOOP is held high) the serial 2.488 Gb/s data and clock from the RX optics module is first clocked into the VSC8024 and then fed back into the VSC8023 through TXSLBIN and TXSLBCLK. The FACLOOP input (held high) selects the data from the VSC8024 instead of the data from the 8:1 Mux. The result is a line loopback from the RX optics module back out to the TX optics module.

Figure 19: Serial Loopback Mode Block Diagram



Notes:
(1) All signals drawn as single ended instead of differential.
(2) Disable High-Speed VSC8024 Outputs Control Signal DISLBOUTS NOT shown.

Preliminary Datasheet

2.488 Gbits/sec SDH/SONET STM-16/STS-48 Mux/Demux and Section Terminator IC Chipset

Notice

This document contains information on products that are in the preproduction phase of development. The information contained in this document is based on test results and initial product characterization. Characteristic data and other specifications are subject to change without notice. Therefore, the reader is cautioned to confirm that this datasheet is current prior to placing orders.

Warning

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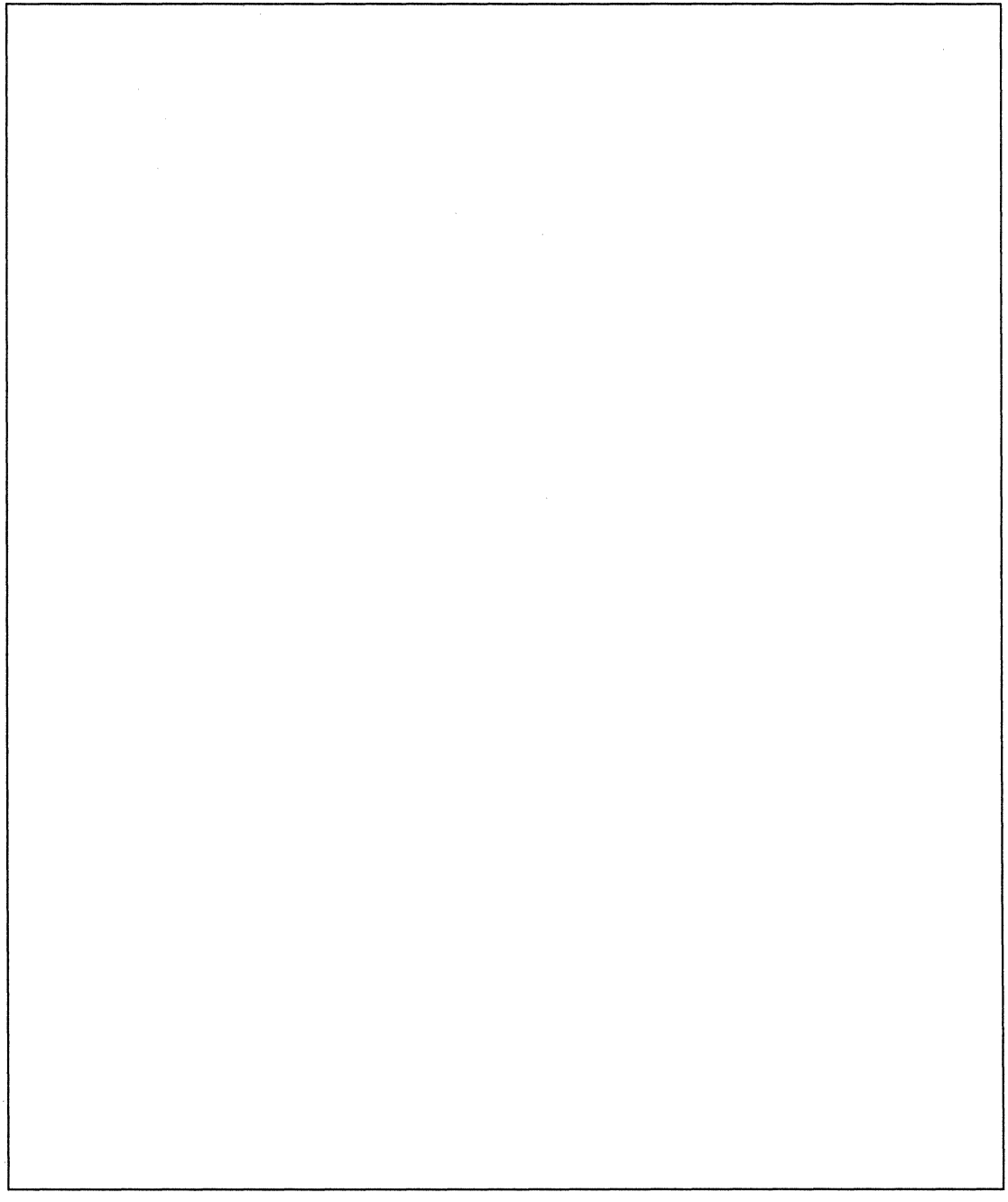


Data Sheet

2.5 Gbits/sec 16-Bit Multiplexer/ Demultiplexer Chipset

Features

- Serial Data Rate up to 2.5 Gb/s
- 16-bit Wide ECL 100K Compatible Parallel Data Interface
- Differential High Speed Data Outputs
- Differential or Single-ended High Speed Data and Clock Inputs
- On-chip Phase Detector (VS8061 Multiplexer)
- Power Dissipation: VS8061: 2.0W(max), VS8062: 1.7W(max)
- Standard ECL Power Supplies: V_{EE} = -5.2 volts, V_{TT} = -2.0 volts
- Commercial (0° to 70° C) or Industrial (-40° C to 85° C) Temperature Range
- Available in 52-pin Ceramic Leaded Chip Carrier Package or 52-pin Plastic Quad Flat Pack

Functional Description

The VS8061 and VS8062 are high speed interface devices capable of data rates up to 2.5 Gb/s. These devices are fabricated in gallium arsenide using the Vitesse H-GaAs E/D MESFET process to achieve high speed and low power dissipation. For ease of system design using these products, both devices use industry standard, -5.2V and -2V, power supplies, and have ECL compatible I/O for parallel data interfaces. Typical applications include telecommunication transmission and instrumentation.

VS8061 Multiplexer

The VS8061 consists of a 16:1 multiplexer circuit, a phase detector, and a timing circuit which generates a divide-by-16 clock from the high speed clock input. The 16:1 multiplexer accepts 16 parallel single-ended ECL compatible inputs (D0..D15) at data rates up to 156Mb/s and bitwise serializes them into a 2.5Gb/s serial output (DO/DON). The internal timing of the VS8061 is referenced to the negative going edge of the high speed clock true input (CLK). This clock is divided by 16 and is provided as an output (CLK16/CLK16N). The setup and hold time of the parallel inputs (D0..D15) are specified with respect to the falling edge of CLK16, so that CLK16/CLK16N can be used to clock the data source of D0..D15. The on-chip phase detector monitors the phase relationship between the internally generated divide by 16 clock and an externally supplied low speed reference clock input (DCLK/DCLKN). Phase difference between these two clock signals generates an up or down output (U, D) for phase lock applications. The phase detector can be used as part of an external Phase Locked Loop (PLL) to implement a clock multiplication function.

In applications where a 2.5 GHz system clock is provided, and the phase detector function is not required, it is recommended to connect one side of the DCLK/DCLKN input to V_{TT} through a 50 ohm resistor. The U and D output can be left open and unused.

VS8062 Demultiplexer

The VS8062 consists of a 1:16 demultiplexer and timing circuitry which generates a divide-by-16 clock from the high speed clock input. The demultiplexer accepts a serial data stream input (DI/DIN) at up to 2.5Gb/s and deserializes it into 16 parallel single-ended ECL compatible outputs (D0..D15) at data rates up to 156 Mb/s. The internal timing of the VS8062 is referenced to the negative going edge of the high speed clock true input (CLK). This clock is divided by 16 and provided as an output (CLK16/ CLK16N). The timing parameters of the parallel data outputs (D0..D15) are specified with respect to the falling edge of CLK16, so that CLK16/ CLK16N can be used to clock the destination of D0..D15.

Figure 1: VS8061 Block Diagram

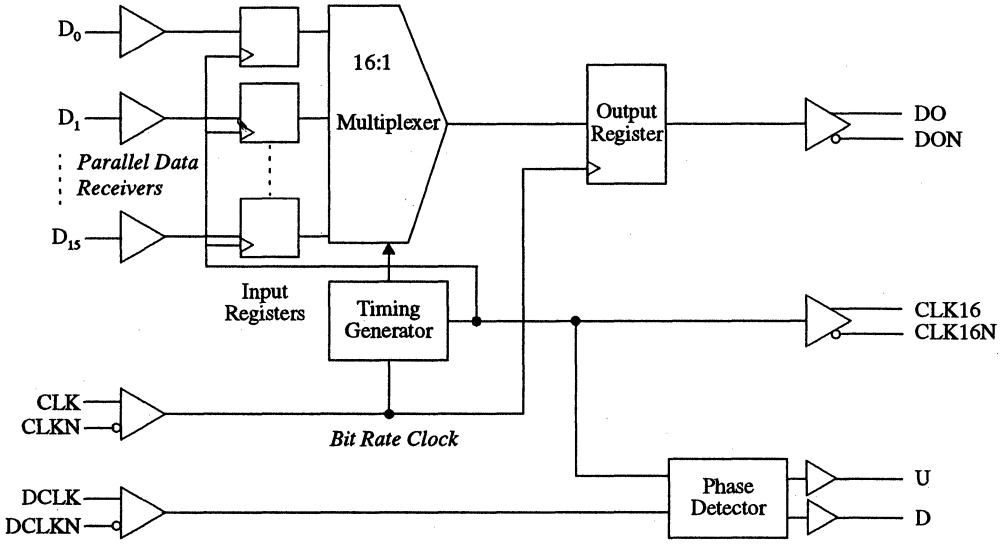
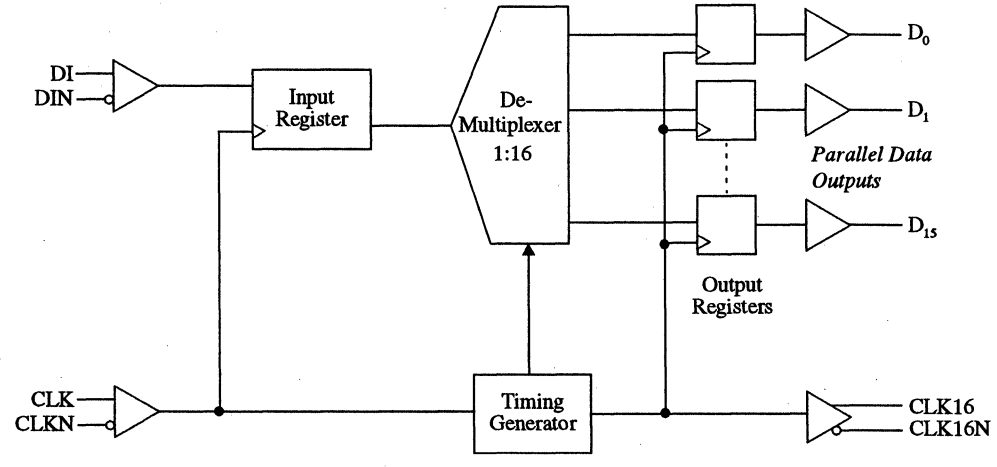


Figure 2: VS8062 Block Diagram

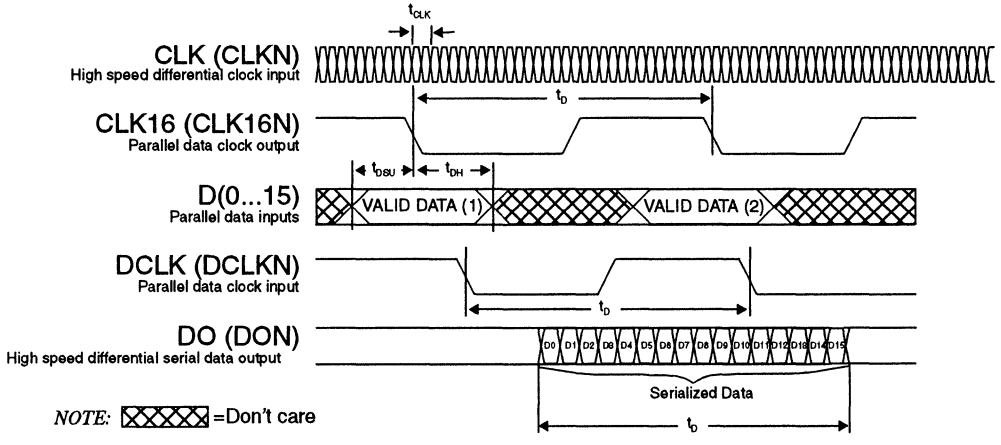


VS8061 Multiplexer AC Characteristics *(Over recommended operating range)*

Parameter	Description	Min	Typ	Max	Units
t_{CLK}	Clock period*	400	-	-	ps
t_D	CLK16, DCLK period (t_{CLK} x 16)	6.4	-	15.6	ns
t_{DSU}	Parallel data set-up time (wrt CLK16 falling edge)	2.0	-	-	ns
t_{DH}	Data hold time (wrt CLK16 falling edge)	0.5	-	-	ns
t_{DC}	CLK16 duty cycle	40	-	60	%
t_r, t_f	DCLK (DCLKN) rise and fall times (10%-90%)	-	-	1.5	ns
t_r, t_f	D(0..15) rise and fall times (10%-90%)	-	-	2.0	ns
t_r, t_f	CLK16 (CLK16N) rise and fall times (10%-90%)	-	0.5	1	ns
t_r, t_f	DO (DON) rise and fall times (20%-80%)	-	150	165	ps

**The parts are guaranteed to operate to a maximum frequency of 2.5GHz.*

Figure 3: VS8061 Multiplexer Waveforms



VS8061 Phase Detector Logic Diagram

The phase detector inside the VS8061 compares the phase difference between the internally generated divide-by-16 clock and the DCLK input. If both inputs (CLK16 and DCLK) to the phase detector are in phase, the U and D outputs will both be low. If the rising edge of CLK16 precedes DCLK, a series of pulses with pulse widths proportional to the phase difference will be present at the U output. Conversely, if DCLK precedes CLK16, then a series of pulses with widths proportional to the phase difference will be present at the D output. The other output will remain low. The Phase Detector ignores phase differences for falling edges. This circuitry is useful for implementing a Clock Multiplier Unit (CMU) function with the VS8061. For example, the DLCK can be the system reference clock at the parallel data rate. An external Voltage Controlled Oscillator (VCO) at 16X the frequency of the reference clock can be used as the CLK input for the VS8061. The phase detector outputs (U and D) can then be used by an external integrator to generate an output that controls the VCO. The generated 16X clock from the VCO will be phase-locked to the reference clock.

Figure 4: VS8061 Phase Detector Logic Diagram

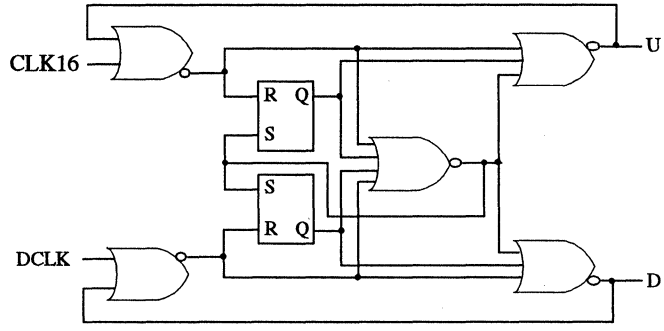
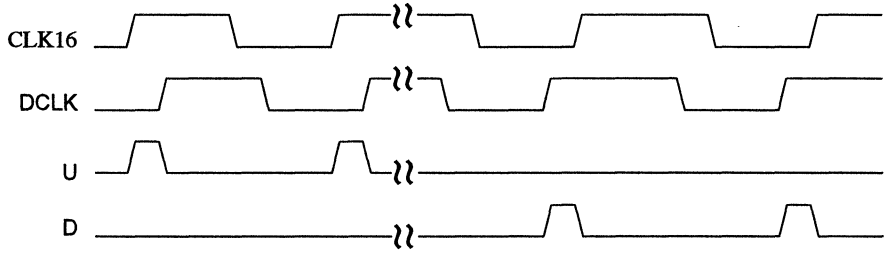


Figure 5: Phase Detector Input and Output Waveforms

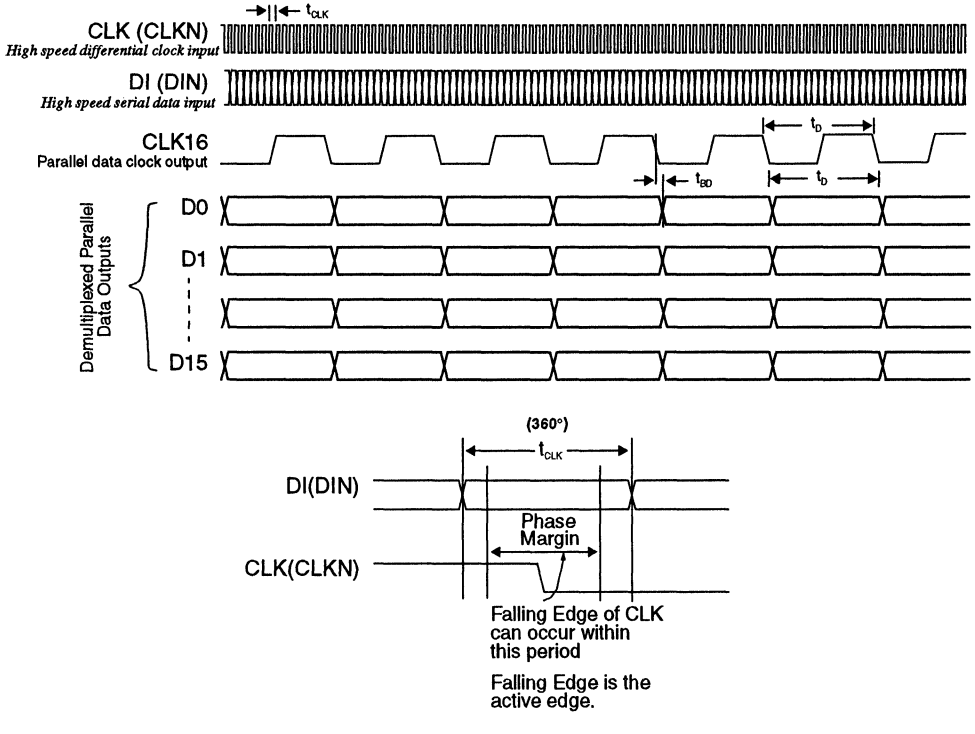


VS8062 Demultiplexer AC Characteristics *(Over recommended operating range)*

Parameter	Description	Min	Typ	Max	Units
t_{CLK}	Clock period[1]	400	-	-	ps
t_D	BYTE CLK16 period (t_{CLK} x 16)	6.4	-	-	ns
t_{BD}	CLK16 falling edge output to valid data	1.0	-	3.0	ns
phase margin	Serial data phase timing margin with respect to high speed clock: Phase Margin[3] = $\left(1-\frac{t_{SU}+t_H}{t_{CLK}}\right)\times 360°$	180[2]	-	-	degrees

(1) If t_{CLK} changes, all the remaining parameters change as indicated by the equations.
(2) At t_{CLK} = 400ps.
(3) t_{SU} and t_H are setup and hold times of the serial data input register.

Figure 6: VS8062 Timing Diagram



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Absolute Maximum Ratings[1]

Power Supply Voltage (V_{TT}) ..... -3.0V to 0.5V
Power Supply Voltage (V_{EE}) ..... VTT + 0.7V to -7.0V
Input Voltage Applied [2] (V_{ECLIN}) ..... -2.5V to 0.5V
High Speed Input Voltage Applied [2] (V_{HSIN}) ..... VEE-0.7V to VCC+0.7V
Output Current, I_{OUT} (DC, output HI) ..... -50 mA
Case Temperature Under Bias (T_C) ..... -55° to 125°C
Storage Temperature (T_{STG}) ..... -65° to 150°C

Notes: (1) Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

(2) V_{TT} must be applied before the magnitude of any input signal voltage ($|V_{IN}|$, $|V_{HSIN}|$) can be greater than $|V_{TT}$ - 0.5V|

Recommended Operating Conditions

Power Supply Voltage (V_{TT}) ..... -2.0V±5 %
Power Supply Voltage (V_{EE}) ..... -5.2V±5 %
Operating Temperature Range* (T) ..... (Commercial) 0° to 70°C, (Industrial) -40° to 85°C

** Lower limit of specification is ambient temperature and upper limit is case temperature.*

ESD Ratings

For performance considerations, minimum ESD protection is provided for the high speed input pins. Therefore, proper procedures should be used when handling these products. The VS8061/8062 are rated to the following ESD voltages based on the human body model:

1. All high speed input pins are rated at or above 500V.
2. All other pins are rated at or above 2000V.

The above ratings apply to both "F" and "QH" packages.

DC Characteristics

Table 1: ECL Inputs and Outputs

(Over recommended operating conditions with internal V_{REF}, V_{CC} = GND, Output load = 50 ohms to -2.0V)

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-1100	-	-700	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
V_{OL}	Output LOW voltage	V_{TT}	-	-1750	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
V_{IH}	Input HIGH voltage	-1040	-	-600	mV	Guaranteed HIGH signal for all inputs
V_{IL}	Input LOW voltage	V_{TT}	-	-1600	mV	Guaranteed LOW signal for all inputs
$\Delta VECL_{OUT}$	Output voltage swing	0.850	-	-	V	Output load 50 ohm to V_{TT}
$\Delta VECL_{IN}$	Input voltage swing	0.600	0.800	1.2	V	AC coupled

Note: Differential ECL output pins must be terminated identically.

Table 2: Power Dissipation

(Over recommended operating conditions, V_{CC}= GND, outputs open circuit)

Parameter	Description	VS8061 (Max)	VS8062 (Max)	Units
I_{EE}	Power supply current from V_{EE}	260	220	mA
I_{TT}	Power supply current from V_{TT}	260	230	mA
P_D	Power dissipation	2.0	1.7	W

Table 3: High Speed Input and Output Specifications

(Over recommended operating conditions, V_{CC} = GND, Output load = 50 ohm to -2.0V)

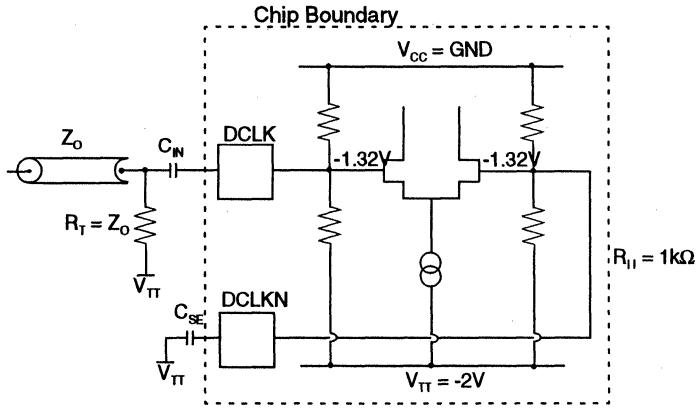
Parameter	Description	Min	Typ	Max	Units	Conditions
ΔV_{HSOUT}	Output voltage swing	0.7	0.9	-	V	Output load, 50 Ohm to -2.0V
ΔV_{HSIN}	Input voltage swing	0.6	0.7	1.2	V	AC coupled
T_r, T_f	Input voltage rise and fall time (high speed)	-	0.2	1.5	ns	same for all data rates; no worse than sine wave at max speed

Notes: 1) Built-in references generator, the high speed inputs are designed for AC coupling

2) If a high speed input is driven single-ended, a capacitor should be connected between the unused high speed or complement input and V_{TT} (see figures 7 and 8).

Coupling for Inputs

Figure 7: AC-Coupling for DCLK, DCLKN Inputs



C_{IN} TYP = 0.1µF

C_{SE} TYP = 0.1µF for single ended applications. (Capacitor values are selected for DCLK = 155 Mb/s.)

DCLK, DCLKN Inputs

Internal biasing will position the reference voltage of approximately -1.32V on both the true and complement inputs. This input can either be DC-coupled or AC-coupled; it can also be driven single-ended or differentially. Figure 7 shows the configuration for a single-ended, AC-coupling operation. In the case of direct coupling and single-ended input, it is recommended that a stable V_{REF} for ECL levels be used for the complementary input.

High Speed Clock and Serial Data Inputs

It is recommended that all high speed clock and serial data inputs (i.e. CLK/CLKN for the VS8061; DI/DIN and CLK/CLKN for the VS8062) be AC-coupled. Figure 8 shows the configuration for a single-ended AC-coupling operation.

In most situations these inputs will have high transition density and little DC offset. However, in cases where this does not hold, direct DC connection is possible. The following is to assist in this application.

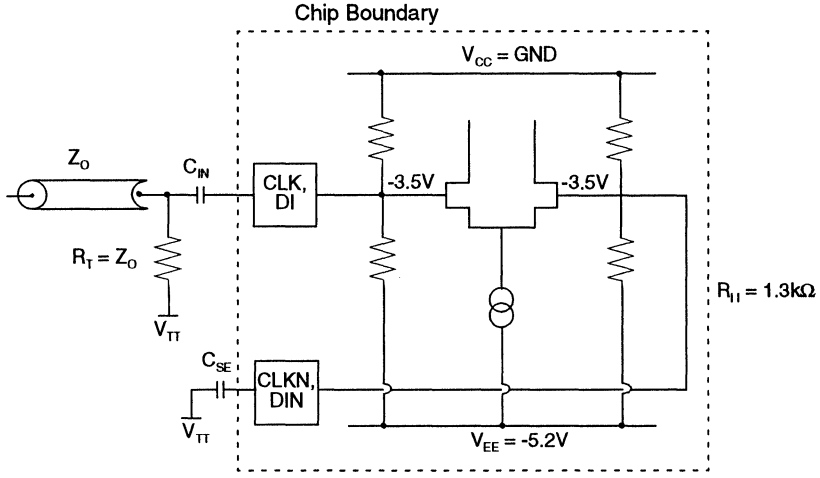
All serial data and clock inputs have the same circuit topology, as shown in figure 8. The reference voltage is created by a resistor divider as shown. If the input signal is driven differentially and DC-coupled to the part, the mid-point of the input signal swing should be centered about this reference voltage and not exceed the maximum allowable amplitude. For single-ended, DC-coupling operations, it is recommended that the user provides an external reference voltage which has better temperature and power supply noise rejection than the on-chip

resistor divider. The external reference should have a nominal value as indicated in the table and can be connected to either side of the differential gate.

Table 4: High Speed Clock and Serial Data Inputs

Product	*Input*	*Reference*	*Min (p-p)*	*Max (p-p)*
VS8061	DCLK, DCLKN	-1.32V	600mV	1.2V
VS8061, VS8062	CLK, CLKN	-3.5V	600mV	1.2V
VS8062	DI, DIN	-3.5V	600mV	1.2V

Figure 8: High Speed Clock and Serial Data Inputs



C_{IN} TYP = 100 pF

C_{SE} TYP = 100 pF for single ended applications. (Capacitor values are selected for DI = 2.5Gb/s.)

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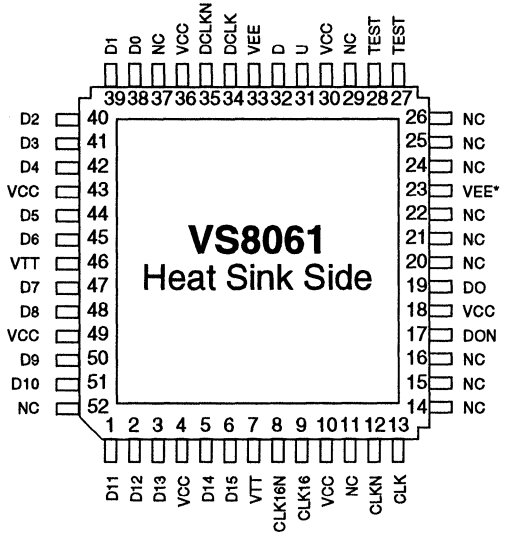
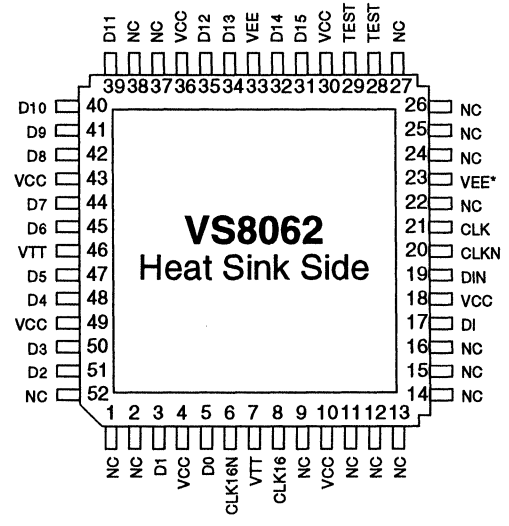
Figure 9: VS8061/8062 F (52-Pin LDCC) Pin Diagrams





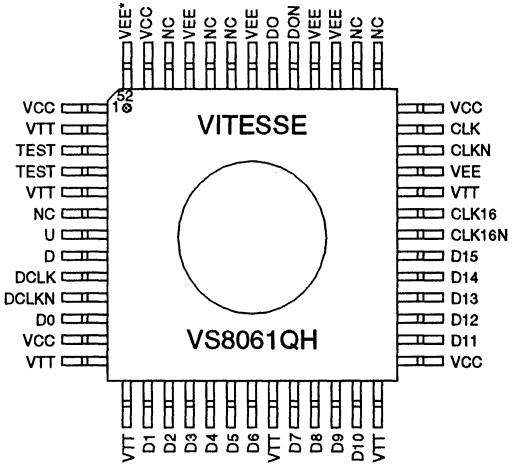
Heat Sink Up
Top View

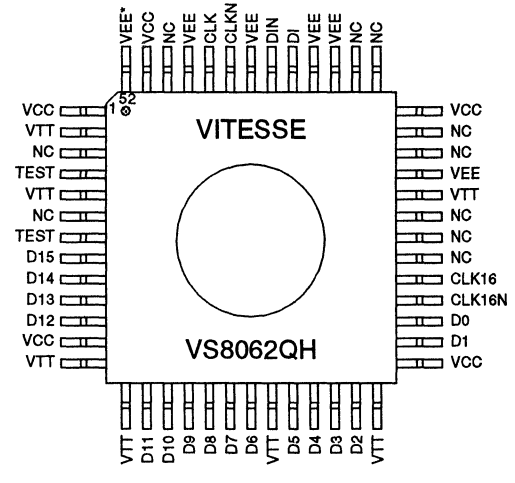
*Heat sink is electrically connected to pin 23 and should be biased to V_{EE}.

Data Sheet

2.5 Gbits/sec 16-Bit Multiplexer/ Demultiplexer Chipset

Figure 10: VS8061/8062 QH (52-Pin PQFP) Pin Diagrams





Heat Spreader Up
Top View

*Heat spreader is electrically connected to pin 52 and should be biased to V_{EE}.

Table 5: VS8061 Pin Description

Pin # For QH	Pin # For F	Name	I/O	Level	Description
38	13	CLK	I	HS	High speed clock true[1]
37	12	CLKN	I	HS	High speed clock complement [1]
9	34	DCLK	I	ECL	Data clock true[1]
10	35	DCLKN	I	ECL	Data Clock complement[1]
34	9	CLK16	O	ECL	Clock divide-by-16 true
33	8	CLK16N	O	ECL	Clock divide-by-16 complement
11, 15-20, 22-25, 28-32	1-3,5,6,38-42,44,45,47,48,50,51	D[0:15]	I	ECL	Parallel data inputs
45	19	DO	O	HS	Serial data output true
44	17	DON	O	HS	Serial data output complement
7	31	U	O	ECL	Phase detector output - up frequency
8	32	D	O	ECL	Phase detector output - down frequency
1,12,27, 39,51	4,10,18,30, 36,43,49	V_{CC}	-	-	Most positive supply
2,5,13,14,21, 26,35	7,46	V_{TT}	-	-	DCFL negative supply
36,42,43, 46, 49	33	V_{EE}	-	-	SCFL negative supply
6,40,41,47,48, 50	11,14-16,20-22,24-26,29,37,52	NC	-	-	Do not connect, leave open
3,4	27,28	Test	-	-	Test inputs. Used in factory for testing, connect to VTT through a resistor
52	23	V_{EE*}	-	-	Heat sink bias, connect to V_{EE}

[1] *Can be used single-ended.*

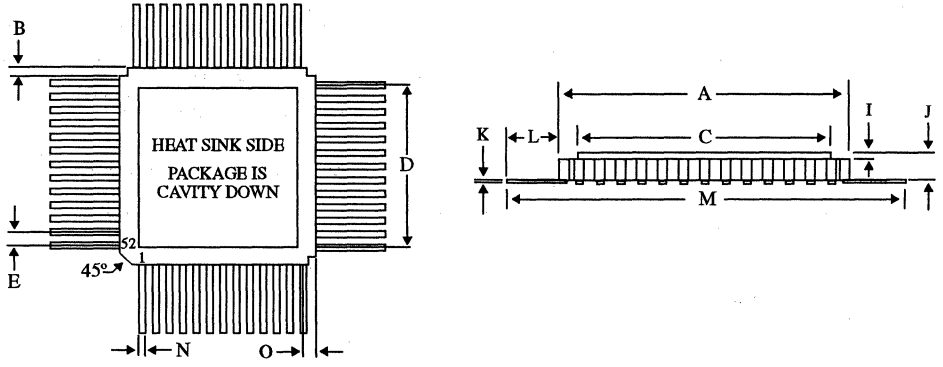
Table 6: VS8062 Pin Description

Pin # For QH	*Pin # For F*	*Name*	*I/O*	*Level*	*Description*
48	21	CLK	I	HS	High speed clock true [1]
47	20	CLKN	I	HS	High speed clock complement [1]
44	17	DI	I	HS	Serial data true [1]
45	19	DIN	I	HS	Serial data complement [1]
31	8	CLK16	O	ECL	Parallel data clock (high speed clock divide-by-16) true
30	6	CLK16N	O	ECL	Parallel data clock (high speed clock divide-by-16) complement
8-11,15-20, 22-25,28,29	3,5,31,32,34, 35,39-42, 44,45,47,48, 50,51	D[0:15]	O	ECL	Parallel data outputs
1,12,27, 39,51	4,10,18,30, 36,43,49	V_{CC}	-	-	Most positive supply
2,5,13,14,21, 26,35	7,46	V_{TT}	-	-	DCFL negative supply
36,42,43, 46,49	33	V_{EE}	-	-	SCFL negative supply
3,6,32-34,37, 38,40,41,50	1,2,9,11-16,22,24-27,37,38,52	NC	-	-	Do not connect, leave open
4,7	28,29	Test	-	-	Test inputs. Used in factory for testing, connect to VTT through a resistor
52	23	V_{EE*}	-	-	Heat sink bias, connect to V_{EE}

[1] *Can be used single-ended.*

Package Information

52-Pin Ceramic LDCC (F) Package



Item	mm (Min/Max)	in (Min/Max)	Item	mm (Min/Max)	in (Min/Max)
A	18.54/19.56	0.730/0.770	I	0.41/0.61	0.016/0.024
B	1.02/1.52	0.040/0.060	J	2.03/2.79	0.080/0.110
C*	15.49/16.51	0.610/0.650	K*	0.09/0.24	0.003/0.009
D*	15.24 TYP	0.600 TYP	L	4.57/5.34	0.180/0.210
E	1.27 TYP	0.050 TYP	M	27.69/30.22	1.090/1.190
			N	0.36/0.56	0.014/0.022
			O	1.75/1.90	0.069/0.075

**At package body.*
Notes: 1) Drawings not to scale
2) Packages: Ceramic (alumina); Heat Sinks: Copper Tungsten; Leads: Alloy 42 with gold plating.

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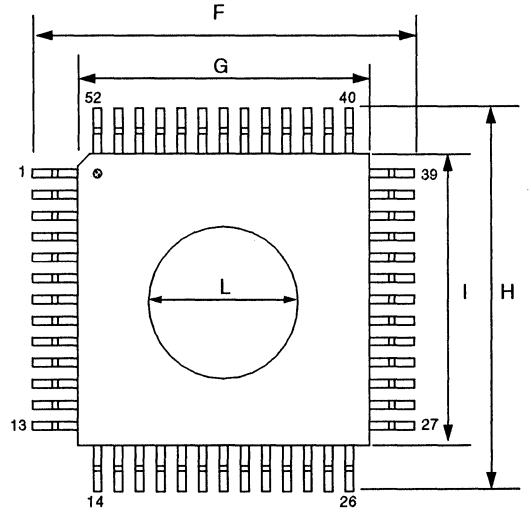
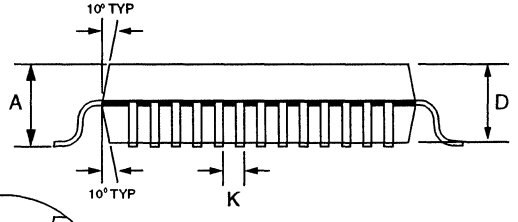
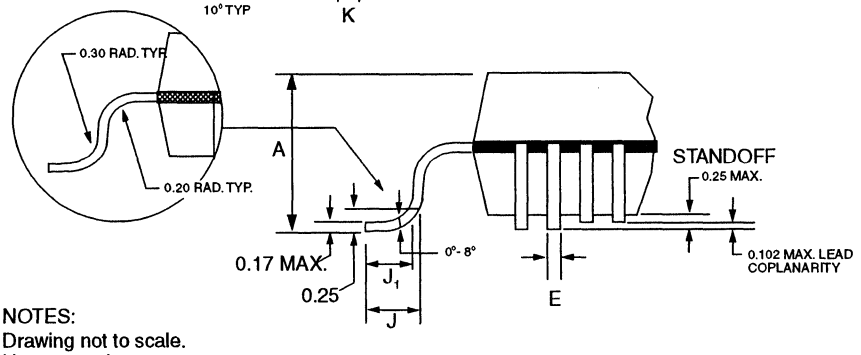
2.5 Gbits/sec 16-Bit Multiplexer/ Demultiplexer Chipset

52 Pin PQFP (QH) Package



Item	*mm*	*Tol.*
A	2.35	MAX
D	2.00	+.10 / -.05
E	0.35	±.05
F	17.20	±.25
G	14.00	±.10
H	17.20	±.25
I	14.00	±.10
J	0.88	+.15 / -.10
J1	0.80	+.15 / -.10
K	1.00	BASIC
L	5.84	±.50 DIA.





NOTES:
Drawing not to scale.
Heat spreader up.
All units in mm unless otherwise noted.

Thermal Considerations

The VS8061 and VS8062 are available in ceramic LDCC and thermally enhanced plastic quad flatpacks. These packages have been enhanced to improve thermal dissipation through low thermal resistance paths from the die to the exposed surface of the heat spreader. The thermal resistance of the two packages is shown in the following table

Table 7: Thermal Resistance

Symbol	*Description*	*F Pack*	*QH Pack*	*Units*
θ_{jc}	Thermal resistance from junction to case.	1.3	2.1	°C/W
θ_{ca}	Thermal resistance from case to ambient still air including conduction through the leads.	18.5	30.0	°C/W

Thermal Resistance with Airflow

Shown in the table below is the thermal resistance with airflow. This thermal resistance value reflects all the thermal paths including through the leads in an environment where the leads are exposed. The temperature difference between the ambient airflow temperature and the case temperature should be the worst case power of the device multiplied by the thermal resistance.

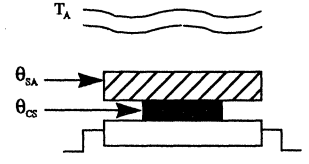
Table 8: Thermal Resistance with Airflow

Airflow	*θ_{ca} for F Pack (case to ambient)*	*θ_{ca} for QH Pack*	*Units*
100 lfpm	15.9	24	°C/W
200 lfpm	14.9	21	°C/W
300 lfpm	14.2	19	°C/W
500 lfpm	13.3	15	°C/W

Thermal Resistance with Heat Sink

The determination of appropriate heat sink to use is as shown below, using the VS8061 in QH package as an example.

Figure 11: VS8061 in QH Package



The worst case temperature rise from case to ambient is given by the equation:

$$\Delta T = P_{(MAX)}(\theta_{SA} + \theta_{CS})$$

where:

θ_{SA} Theta sink to ambient
θ_{CS} Theta case to sink
$T_{A(MAX)}$ Air temperature, user supplied (typically 55° C)
$T_{C(MAX)}$ Case temperature (85°C for Industrial range)
$\Delta TT_C - T_A$
$P_{(MAX)}$ Power (2.0 W for VS8061)

$$\therefore P = \frac{\Delta T}{\Sigma\theta} = \frac{T_C - T_A}{\theta_{SA} + \theta_{CS}}$$

$$\theta_{SA} = \frac{\Delta T}{P} - \theta_{CS}$$

If T_A = 55° C and θ_{CS} (user supplied) is typically 0.6° C/W,

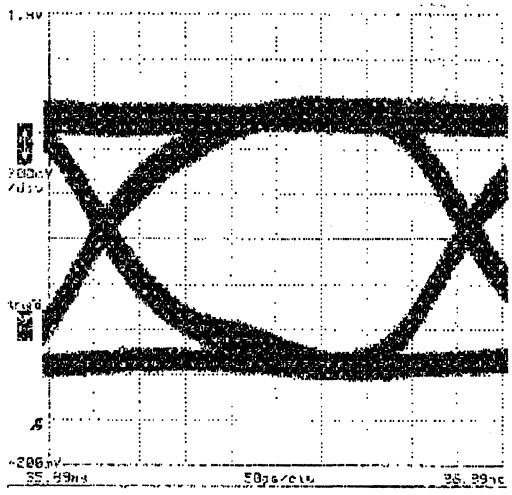
$$\theta_{SA} = \frac{(85 - 55)°C}{2W} - 0.6°C/W$$

$$\theta_{SA} = 14.4°C/W$$

Therefore, to maintain the proper case and junction temperature, a heat sink with a θ_{SA} of 14.4° C/W or less must be selected at the appropriate air flow.

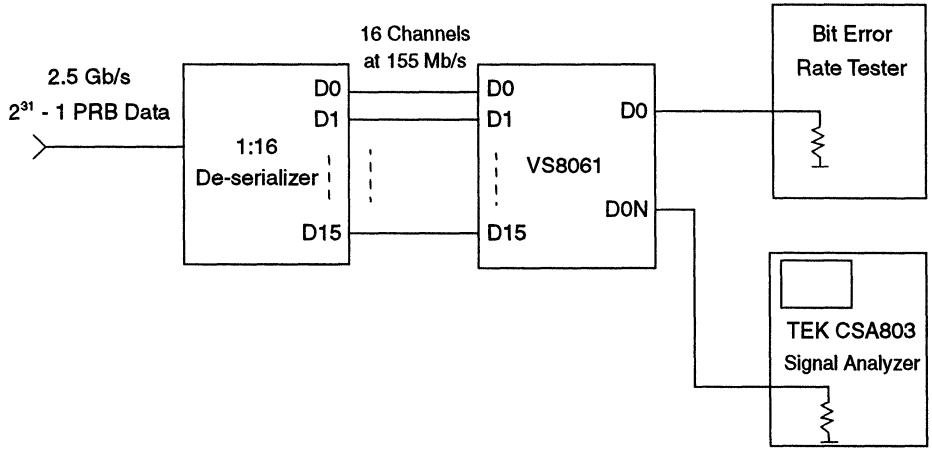
Note: the heat spreader is tied to V_{EE} in both the VS8061 and VS8062.

Figure 12: Data Eye From Serial Output of VS8061 in QH Package (D0/D0N)



Amplitude: 200 mV/div
Time Scale: 50 ps/div
Data Rate: 2.5 Gb/s

Figure 13: Measurement Setup



Data Sheet

2.5 Gbits/sec 16-Bit Multiplexer/ Demultiplexer Chipset

Ordering Information

The order number for this product is formed by a combination of the device number, package type, and the operating temperature range.

VS80XX **FC**

Device Type
VS8061 - 2.5 Gb/s 16-bit Multiplexer
VS8062 - 2.5 Gb/s 16-bit Demultiplexer

Package and Temperature
FC: 52 Pin Ceramic Leaded Chip Carrier (LDCC), 0° C ambient to +70° C case
FI: 52 Pin Ceramic Leaded Chip Carrier (LDCC), -40° C ambient to +85° C case
QH: 52 Pin Plastic Quad Flat Pack (PQFP), 0° C ambient to +85° C case

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Warning

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2.5 Gbits/sec 16-Bit Multiplexer/ Demultiplexer Chipset

Data Sheet

Advanced Product Information

STM-16/STS-48 16:1 Multiplexer with Integrated Clock Generation

Features

- 16:1 2.488 Gb/s Multiplexer
- Integrated PLL for Clock Generation - No External Components
- 16-bit Wide, Single-ended, ECL 100K Compatible Parallel Data Interface
- 155.52 MHz Reference Clock Frequency
- Differential High Speed Data Output
- Power Dissipation: 2.8 W(max)
- Standard ECL Power Supplies: V_{EE} = -5.2V V_{TT} = -2.0V
- Commercial (0° to 85° C) Temperature Range
- Available In 52-pin Plastic Quad Flat Pack

Functional Description

The VSC8063 is a high speed multiplexer designed for STM-16/STS-48 data rates at low power dissipation. For ease of system design, it uses industry standard, -5.2V and -2V, power supplies and has ECL-compatible I/O for parallel data interfaces. The VSC8063 provides an integrated solution for SDH/SONET transmission and instrumentation systems.

The VSC8063 consists of a 16:1 multiplexer circuit and a clock multiplier unit. The 16:1 multiplexer accepts 16 parallel single-ended ECL compatible inputs (D0..D15) at data rates of 155.52Mb/s then bitwise serializes the data word onto a 2.488Gb/s serial output (DO/DON). The internal timing of the VSC8063 is referenced to the negative going edge of the 155.52 MHz clock true input (REFCLK). A divided-by-16 clock output is also provided (CLK16/CLK16N). The setup and hold time of the parallel inputs (D0..D15) are specified with respect to the falling edge of CLK16, so that CLK16/CLK16N can be used to clock the data source of D0..D15.

VSC8063 Block Diagram

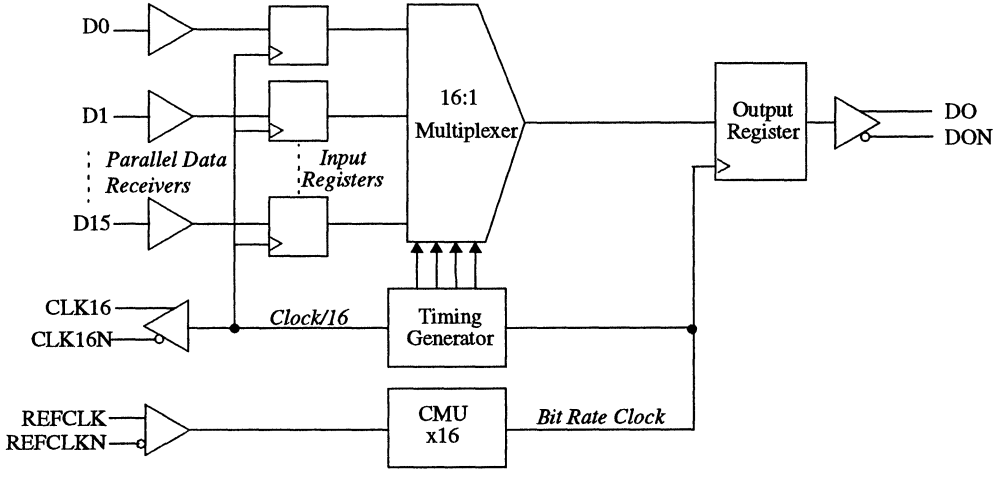

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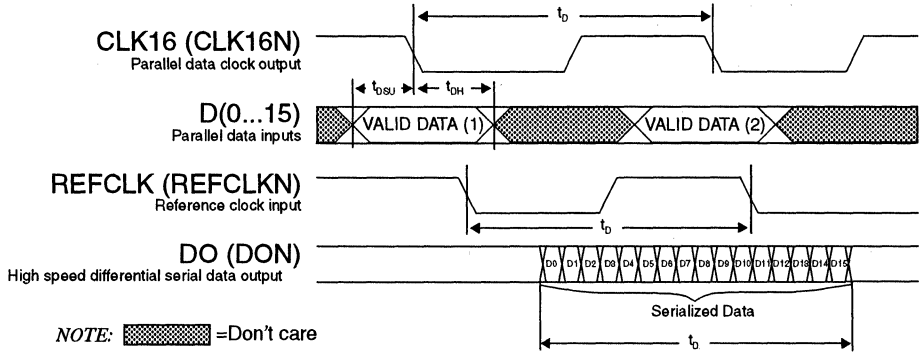
Table 1: VSC8063 Multiplexer AC Characteristics *(Over recommended operating range)*

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
t_D	CLK16, DCLK period		6.4	-	ns
t_{DSU}	Parallel data set-up time (wrt CLK16 falling edge)	1.5	-	-	ns
t_{DH}	Data hold time (wrt CLK16 falling edge)	0.5	-	-	ns
t_{DC}	CLK16 duty cycle	45	-	55	%
t_r, t_f	REFCLK (REFCLKN) rise and fall times (10%-90%)	-	-	1.5	ns
t_r, t_f	D(0..15) rise and fall times (10%-90%)	-	-	2.0	ns
t_r, t_f	CLK16 (CLK16N) rise and fall times (10%-90%)	-	0.5	1	ns
t_r, t_f	DO (DON) rise and fall times (20%-80%)	-	150	165	ps

Figure 1: VSC8063 Multiplexer Waveforms



Advanced Product Information

STM-16/STS-48 16:1 Multiplexer with Integrated Clock Generation

Absolute Maximum Ratings[1]

Power Supply Voltage (V_{TT}) ..... -3.0V to 0.5V
Power Supply Voltage (V_{EE}) ..... VTT + 0.7V to -7.0V
Input Voltage Applied (V_{ECLIN}) ..... -2.5V to 0.5V
Output Current, I_{OUT} (DC, output HI) ..... -50 mA
Case Temperature Under Bias (T_C) ..... -55° to 125°C
Storage Temperature (T_{STG}) ..... -65° to 150°C

Notes: (1) Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

(2) V_{TT} must be applied before the magnitude of any input signal voltage ($|V_{IN}|$, $|V_{HSIN}|$) can be greater than $|V_{TT}$ - 0.5V|

Recommended Operating Conditions

Power Supply Voltage (V_{TT}) ..... -2.0V±5 %
Power Supply Voltage (V_{EE}) ..... -5.2V±5 %
Operating Temperature Range* (T) ..... (Commercial) 0° to 85°C

** Lower limit of specification is ambient temperature and upper limit is case temperature.*

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DC Characteristics

Table 2: ECL Inputs and Outputs

(Over recommended operating conditions with internal V_{REF}, V_{CC} = GND, Output load = 50 ohms to -2.0V)

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-1100	-	-700	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
V_{OL}	Output LOW voltage	V_{TT}	-	-1750	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
V_{IH}	Input HIGH voltage	-1040	-	-600	mV	Guaranteed HIGH signal for all inputs
V_{IL}	Input LOW voltage	V_{TT}	-	-1600	mV	Guaranteed LOW signal for all inputs
$\Delta VECL_{OUT}$	Output voltage swing	0.850	-	-	V	Output load 50 ohm to V_{TT}
$\Delta VECL_{IN}$	Input voltage swing	0.600	0.800	1.2	V	AC coupled

Note: Differential ECL output pins must be terminated identically.

Table 3: Power Dissipation

(Over recommended operating conditions, V_{CC}= GND, outputs open circuit)

Parameter	Description	Typ	Max	Units
I_{EE}	Power supply current from V_{EE}	370	450	mA
I_{TT}	Power supply current from V_{TT}	140	170	mA
P_D	Power dissipation	2.3	2.8	W

Table 4: High Speed Output Specifications

(Over recommended operating conditions, V_{CC} = GND, Output load = 50 ohm to -2.0V)

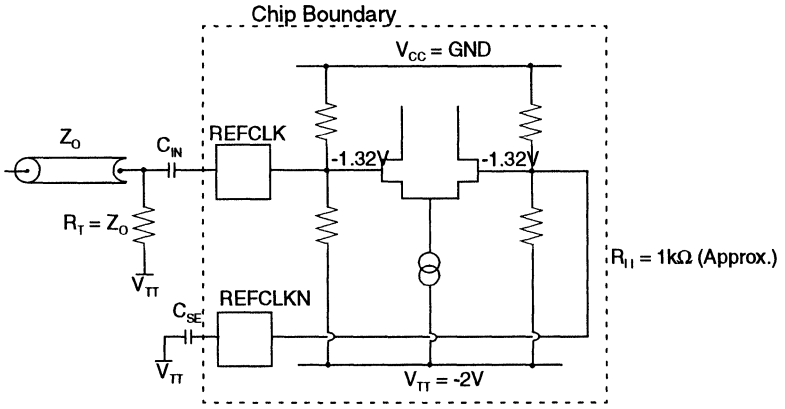
Parameter	Description	Min	Typ	Max	Units	Conditions
ΔV_{HSOUT}	Output voltage swing	0.7	0.9	-	V	Output load, 50 Ohm to -2.0V

Table 5: Clock Multiplier Unit Performance

Name	Description	Min	Typ	Max	Units
RC_d	Reference clock duty cycle	45		55	%
OC_d	CLK16 duty cycle	45		55	%
RCf	Reference clock frequency		155.52		MHz
Δf_{RC}	Reference clock frequency range	-30		+30	ppm
t_{jitter}	H.S. output jitter (12 KHz to 20 MHz)			0.01	UI_{RMS}

Coupling for Inputs

Figure 2: AC-Coupling for REFCLK, REFCLKN Inputs



C_{IN} TYP = 0.1µF

C_{SE} TYP = 0.1µF for single ended applications. (Capacitor values are selected for REFCLK = 155.52 MHz)

DCLK, DCLKN Inputs

Internal biasing will position the reference voltage of approximately -1.32V on both the true and complement inputs. This input can either be DC-coupled or AC-coupled; it can also be driven single-ended or differentially. Figure 3 shows the configuration for single-ended, AC-coupling operation. In the case of direct coupling and single-ended input, it is recommended that a stable V_{REF} for ECL levels be used for the complementary input.

Figure 3: VSC8063QH (52-Pin PQFP) Pin Diagrams

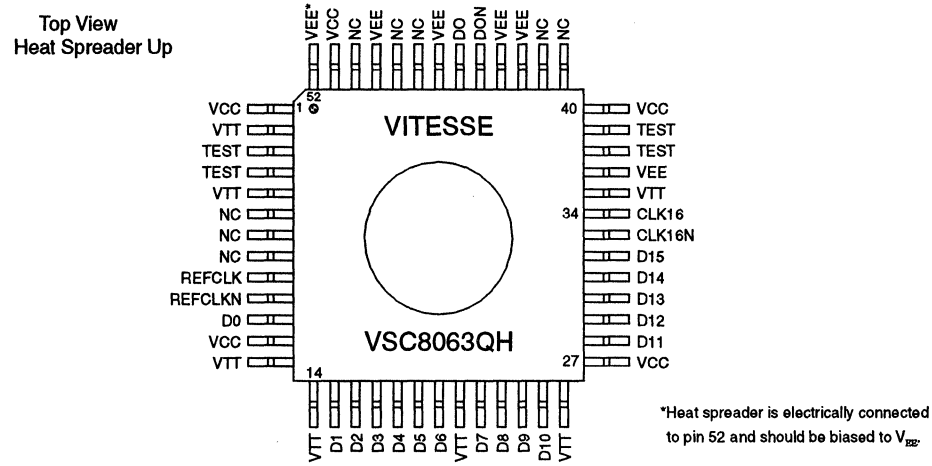


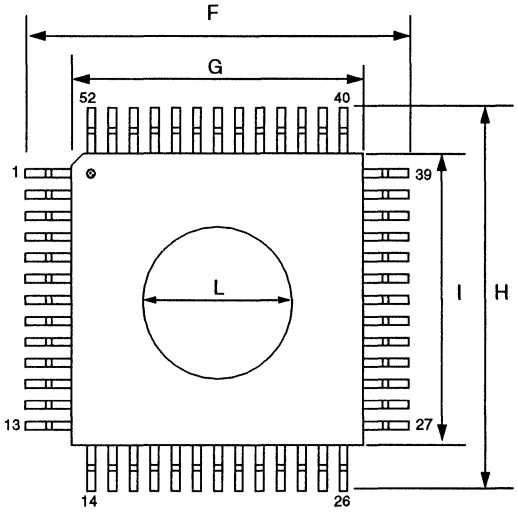
Table 6: VSC8063 Pin Description

Pin # For QH	*Name*	*I/O*	*Level*	*Description*
9	REFCLK	I	ECL	Reference clock true[1]
10	REFCLKN	I	ECL	Reference clock complement[1]
34	CLK16	O	ECL	Clock divide-by-16 true
33	CLK16N	O	ECL	Clock divide-by-16 complement
11, 15-20, 22-25, 28-32	D[0:15]	I	ECL	Parallel data inputs
45	DO	O	HS	Serial data output true
44	DON	O	HS	Serial data output complement
1,12,27, 39,51	V_{CC}	-	-	Most positive supply
2,5,13,14,21, 26,35	V_{TT}	-	-	DCFL negative supply
36,42,43, 46, 49	V_{EE}	-	-	SCFL negative supply
6,7,8,40,41, 47,48,50	NC	-	-	Do not connect, leave open
3,4	Test	I	-	Test inputs. Used in factory for testing, connect to VTT through a 1KΩ resistor
52	V_{EE*}	-	-	Heat sink bias, connect to V_{EE}
37,38	Test	O	-	Test outputs. Leave open.

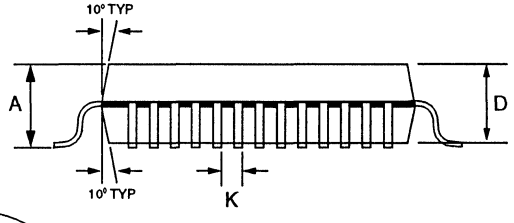
[1] *Can be used single-ended.*

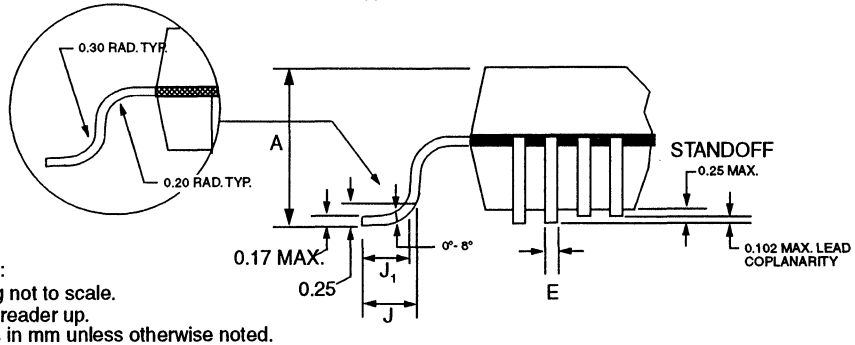
Package Information

52 Pin PQFP (QH) Package Drawings



Item	*mm*	*Tol.*
A	2.35	MAX
D	2.00	+.10 / -.05
E	0.35	±.05
F	17.20	±.25
G	14.00	±.10
H	17.20	±.25
I	14.00	±.10
J	0.88	+.15 / -.10
J1	0.80	+.15 / -.10
K	1.00	BASIC
L	5.84	±.50 DIA.





NOTES:
Drawing not to scale.
Heat spreader up.
All units in mm unless otherwise noted.

Thermal Considerations

The VSC8063 is available in a thermally enhanced plastic quad flatpack. This package has been enhanced to improve thermal dissipation through a low thermal resistance path from the die to the exposed surface of the heat spreader. The thermal resistance is shown in the following table:

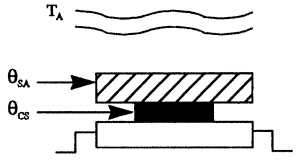
Table 7: Thermal Resistance

Symbol	Description	QH Pack	Units
θ_{jc}	Thermal resistance from junction to case.	2.1	°C/W
θ_{ca}	Thermal resistance from case to ambient still air including conduction through the leads.	35	°C/W
$\theta_{ca\text{-}100}$	Thermal resistance from case to ambient with 100 Linear Feet per Minute of airflow	29	°C/W
$\theta_{ca\text{-}200}$	Thermal resistance from case to ambient with 200 Linear Feet per Minute of airflow	26	°C/W
$\theta_{ca\text{-}400}$	Thermal resistance from case to ambient with 400 Linear Feet per Minute of airflow	22	°C/W
$\theta_{ca\text{-}600}$	Thermal resistance from case to ambient with 600 Linear Feet per Minute of airflow	20	°C/W

Thermal Resistance with Heat Sink

The determination of appropriate heat sink to use is as shown below, using the VSC8063 in QH package as an example.

Figure 4: VSC8063 In QH Package



The worst case temperature rise from case to ambient is given by the equation:

$$\Delta T = P_{(MAX)}(\theta_{SA} + \theta_{CS})$$

where:

θ_{SA} Theta sink to ambient
θ_{CS} Theta case to sink
$T_{A(MAX)}$ Air temperature, user supplied (typically 55° C)
$T_{C(MAX)}$ Case temperature (85°C)
$\Delta TT_C - T_A$
$P_{(MAX)}$ Power (2.8 W for VSC8063)

$$\therefore P = \frac{\Delta T}{\Sigma\theta} = \frac{T_C - T_A}{\theta_{SA} + \theta_{CS}}$$

$$\theta_{SA} = \frac{\Delta T}{P} - \theta_{CS}$$

If $T_A = 55°$ C and θ_{CS} (user supplied) is typically 0.6° C/W,

$$\theta_{SA} = \frac{(85 - 55)°C}{2.8W} - 0.6°C/W$$

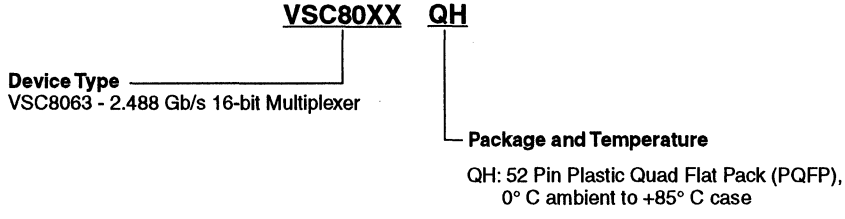
$$\theta_{SA} = 10.1°C/W$$

Therefore, to maintain the proper case and junction temperature, a heat sink with a θ_{SA} of 10.1° C/W or less must be selected at the appropriate air flow.

Note: the heat spreader is tied to V_{EE} in the VSC8063.

Ordering Information

The order number for this product is formed by a combination of the device number, package type, and the operating temperature range.



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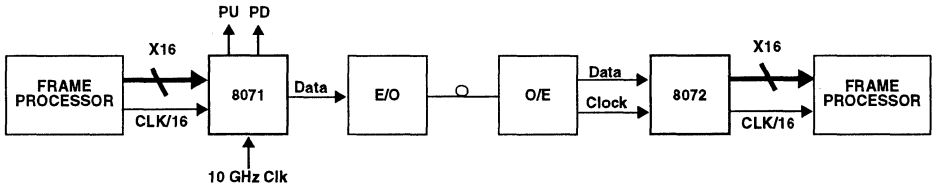
Advanced Product Information

10 Gbits/sec 16-Bit Mux/Demux for STS-192 and STM-64 Applications

Features

- Performs 16:1, 1:16 Mux/Demux Between 10 Gb/s High Speed Signal and 16 622 Mb/sec Low Speed Signals.
- Industry Standard -2.0V and -5.2V Power Supplies
- 50Ω Output Drive Capability and Impedance Matched Outputs
- Internal Input Terminations
- High Performance Module
- VSC8071 is a 16:1 10 Gb/s Multiplexer with an Integrated Phase-frequency Detector
- VSC8072 is a 1:16 10 Gb/s Demultiplexer

Typical System Block Diagram



General Description

The Vitesse 10 Gb/s multiplexer/demultiplexer chipset is intended to perform serialization and de-serialization between 622 Mb/s and 10 Gb/s rate bit streams. The devices are packaged in a custom multilayer connectorized module to provide an environment compatible with 10 GHz clock rates.

VSC8071 Functional Description

The VSC8071 10Gb/s multiplexer integrates a 16:1 multiplexer with synchronous timing control together with a phase detector. The phase detector can be used with an external loop filter and VCO to generate the bit rate clock.

The ECL compatible parallel data inputs (**D0...D15**) and parallel data rate clocks (**CLK16I/CLK16IN**) are provided with on chip 50 ohm terminations to V_{TT}. The bit rate clock (**CLKI**) input is internally terminated with a 50 ohm termination to V_{CC}. The serial data outputs (**DO, DON**) are back terminated with on-chip 100 ohm resistors. ECL compatible divided clock (**CLK16O/CLK16ON**) is provided and should be externally terminated with 50 ohm resistors to V_{TT}.

VSC8072 Functional Description

The VSC8072 10Gb/s demultiplexer integrates a 1:16 demultiplexer with synchronous timing control.

Serial data inputs (**DI/DIN**) and bit rate clock input (**CLKI**) are internally terminated with 50 ohm termination to V_{CC}. The deserialized data outputs (**Q0...Q15**) and divided clock (**CLK16O/CLK16ON**) are ECL compatible outputs and should be terminated in 50 ohms to V_{TT}.

Figure 5: VSC8071 Functional Block Diagram

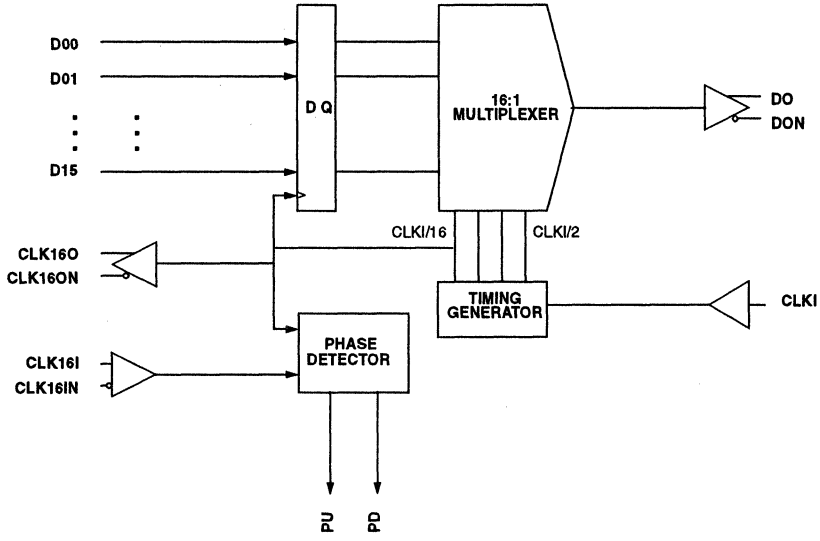
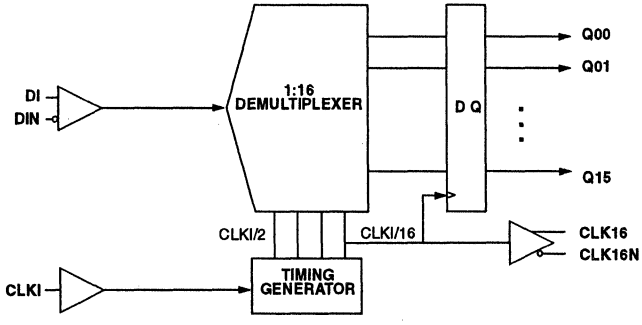


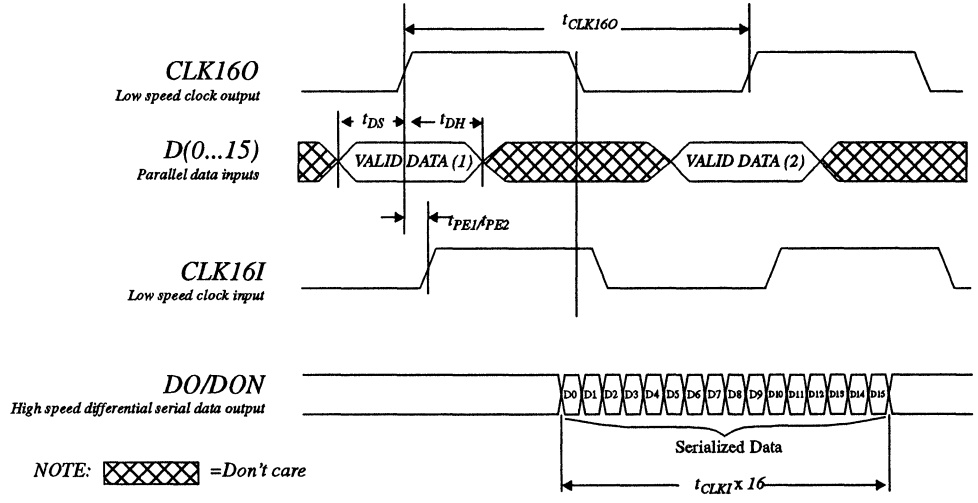
Figure 6: VSC8072 Functional Block Diagram



VSC8071 AC Characteristics *(Over recommended operating conditions)*

Parameters	Description	Min	Typ	Max	Units	Conditions
t_{DOR}, t_{DOF}	Serial data rise and fall time		35		pS	See figure 5.
t_{CLK16R}, t_{CLK16F}	CLK16O rise and fall times	-	200	300	pS	See figure 5.
t_{DS}	Data setup to CLK16O	TBD			pS	—
t_{DH}	Data hold from CLK16O	TBD			pS	—
t_{PE1}	CLK16I to CLK16O delay		TBD		pS	Single ended CLK16I, PU/PD = zero on-chip phase error
t_{PE2}	CLK16I to CLK16O delay		TBD		pS	differentially driven CLK16I, PU/PD = zero on-chip phase error
t_{CLKI}	CLKI period		100		pS	—
t_{CLK16I}	CLK16I period		1.6		nS	—

Figure 7: VSC8071 AC Timing Waveforms



Telecom/ATM

VSC8072 AC Characteristics *(Over recommended operating conditions)*

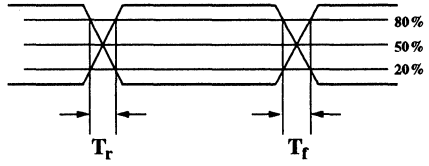
Parameters	*Description*	*Min.*	*Typ.*	*Max.*	*Units*	*Conditions*
t_{CLK16R}, t_{CLK16F}	CLK16 rise and fall times.		200	300	pS	See figure 5.
t_{QR}, t_{QF}	Parallel data out rise and fall time.		300		pS	See figure 5.
$Ø_m$	Phase margin		180		deg	at $(2^{23}-1)$ PRBS
t_{QS}	Output data valid time before CLK16.	TBD			pS	—
t_{QH}	Output data valid time after CLK16.	TBD			pS	—
t_{CLK}	CLK period.		100		pS	—

Figure 8: VSC8072 AC Timing Waveforms

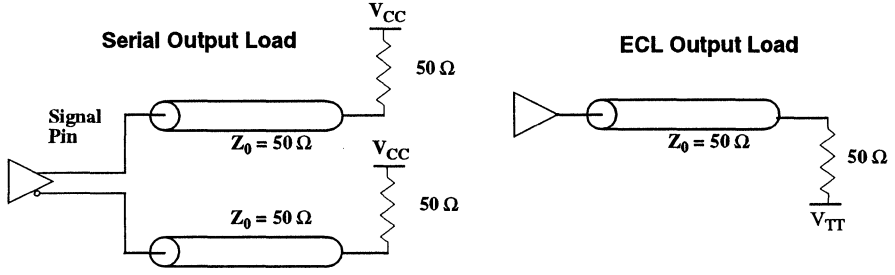
TBD

Figure 9: Parametric Measurement Information

Output Rise and Fall Time



Parametric Test Load Circuit



DC Characteristics *(Over recommended operating conditions)*

Table 2: ECL Inputs/Outputs.

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-1100	—	-700	mV	50Ω to V_{TT} Load
V_{OL}	Output LOW voltage	V_{TT}	—	-1750	mV	50Ω to V_{TT} Load
V_{IH}	Input HIGH voltage	-1100	—	-700	mV	
V_{IL}	Input LOW voltage	V_{TT}	—	-1540	mV	
ΔV_{IN}	Input Swing	400			mV	—
I_{IH}	Input HIGH current	—	—	32	mA	V_{IN} = -700mV, V_{TT} = -2.1 V
I_{IL}	Input LOW current			9	mA	V_{IN} = -1750mV, V_{TT} = -2.1 V

Table 3: High-Speed Outputs (VSC8071)

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-130	-100	-70	mV	External 50Ω to V_{CC}
V_{OL}	Output LOW voltage	-1100	-900	-750	mV	External 50Ω to V_{CC}
I_{OL}	Output Low Current			23	mA	—
I_{OH}	Output High Current			3	mA	—

Table 4: High-Speed Data Inputs (VSC8072)

Parameters	Description	Min	Typ	Max	Units	Conditions
ΔV_{IN}	Amplitude		1.0	2.0	V	
V_{IN}	Input Voltage	-2.0	-0.5	1.0	V	

Note: 1) Reference voltage in a single ended application must be ± 40mV from the mean input swing given ΔV_{IN} = 750 mV, and ± 100mV from the mean input swing given ΔV_{IN} = 1V.

Table 5: High-Speed Clock Inputs

Parameters	Description	Min	Typ	Max	Units	Conditions
ΔV_{IN}	Input Swing - single ended		0.75		V	—
V_{INDC}	DC Value of CLKI	-1.8		+1.8	V	

Table 6: Power Dissipation

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
I_{EE}	Supply Current - VSC8071	—	850		mA	$V_{EE} = V_{EE}$ min, apply only to IEE max
I_{EE}	Supply Current - VSC8072	—	650		mA	
I_{TT}	Termination Current - VSC8071	—		570	mA	$V_{TT} = V_{TT}$ min, ECL Inputs High apply only to ITT max
I_{TT}	Termination Current - VSC8072	—		50	mA	
P_D	Power Dissipation - VSC8071	—	5		W	$V_{EE} = V_{EE}$ min, $V_{TT} = V_{TT}$ min, ECL Inputs High apply only to PD max
P_D	Power Dissipation - VSC8072	—	4		W	

Absolute Maximum Ratings (1)

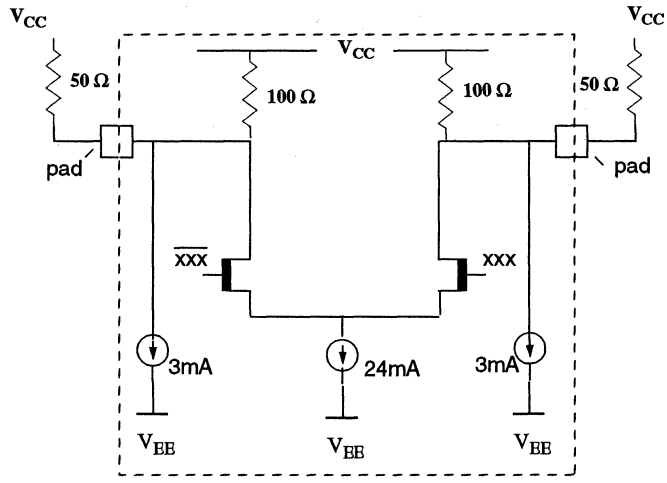
ECL Power Supply Voltage, (V_{EE}) ..... -7.0 V to +0.7 V
V_{TT} - Termination Voltage (ECL Inputs) ..... -2.5 V to +0.5 V
V_{TT} - Termination Voltage (CLKI) ..... -2.5 V to +0.5 V
DC Input Voltage (Low-speed inputs) ..... V_{TT} - 2.5 V to +0.5 V
DC Input Voltage, (CLKI) ..... V_C - 2.0 V to V_C + 2.0 V
DC Input Voltage, (DI) ..... -2.5 V to +0.5 V
Case Temperature Under Bias ..... -55° to +125 °C
Storage Temperature ..... -65 °C to +150 °C

Recommended Operating Conditions

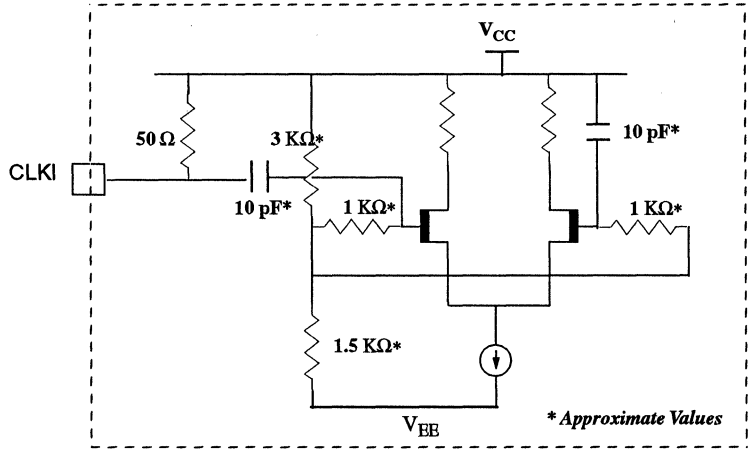
Power Supply Voltage, (V_{EE}) ..... -5.2 V ±5%
Termination Supply Voltage, (V_{TT}) ..... -2.0 V ±5%
Operating Temperature Range, (T) (2) ..... 0 °C to + 70 °C

Notes:
(1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.
(2) Lower limit is ambient temperature and upper limit is case temperature.
(3) CAUTION: Do not apply V_{TT} prior to V_{EE}

Figure 10: IO Structures

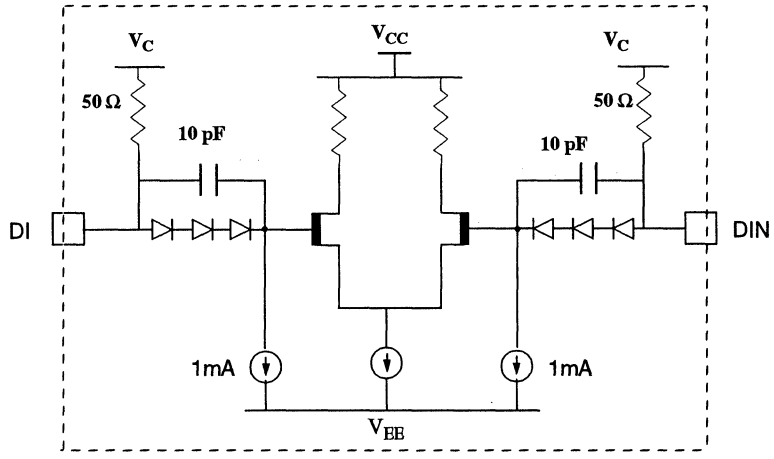


MUX High-Speed Output Buffer

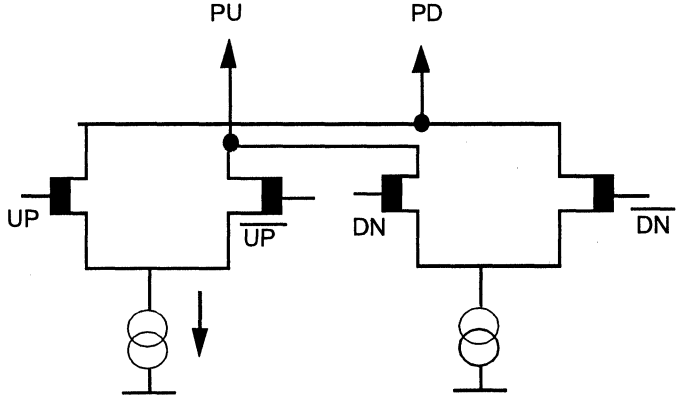


High-Speed Clock Input Buffer

Figure 11: IO Structures Cont.



DMUX High-Speed Data Input Buffer



MUX Phase-Detector Output Circuit

Table 7: VSC8071 Pin Description

Name	*Description*
D00:15	INPUT -ECL Parallel data presented to this port is clocked into the device. The timing of this data is relative to the CLK16O output.
CLKI	INPUT - HIGH SPEED CLOCK Bit rate input clock. This clock is terminated in 50 Ohms to V_C, and is AC coupled on-chip.
V_C	POWER SUPPLY (Common mode termination voltage for CLKI input) (Typically grounded)
CLK16I, CLK16IN	INPUT- DIFFERENTIAL ECL Parallel data rate clock.
DO, DON,	OUTPUT - DIFFERENTIAL HIGH SPEED Serial data output stream. DO and DON should be terminated with 50 Ohms to ground at the load.
CLK16O, CLK16ON	OUTPUT - DIFFERENTIAL ECL This is the bit rate clock divided by 16.
PU, PD	OUTPUT - ANALOG Phase detector outputs.
V_{CC}	GROUND
V_{EE}	POWER SUPPLY (-5.2 V NOM.)
V_{TT}	POWER SUPPLY (-2.0 V NOM.) Termination supply for the single ended ECL inputs.
Vbb	ECL Reference Voltage (typ. -1.32V)

Table 8: VSC8072 Pin Description

Name	*Description*
DI, DIN	INPUT - HIGH SPEED DIFFERENTIAL (HS) Serial data input stream. These inputs are internally terminated. If a single ended signal is used the other input should be capacitively de-coupled to V_{CC}.
CLKI	INPUT - HIGH SPEED CLOCK (HS) Bit rate clock input.
V_C	POWER SUPPLY (Termination voltage for CLKI input) (Typically grounded)
Q00:15	OUTPUT - ECL De-serialized data outputs. The outputs are updated at 1/16 of the bit rate.
CLK16, CLK16N	OUTPUT - DIFFERENTIAL ECL This is the bit rate clock divided by 16.
V_{CC}	GROUND
V_{EE}	POWER SUPPLY (-5.2 V NOM.)
V_D	POWER SUPPLY (Common mode termination voltage for DI,DIN inputs) (Typically grounded)

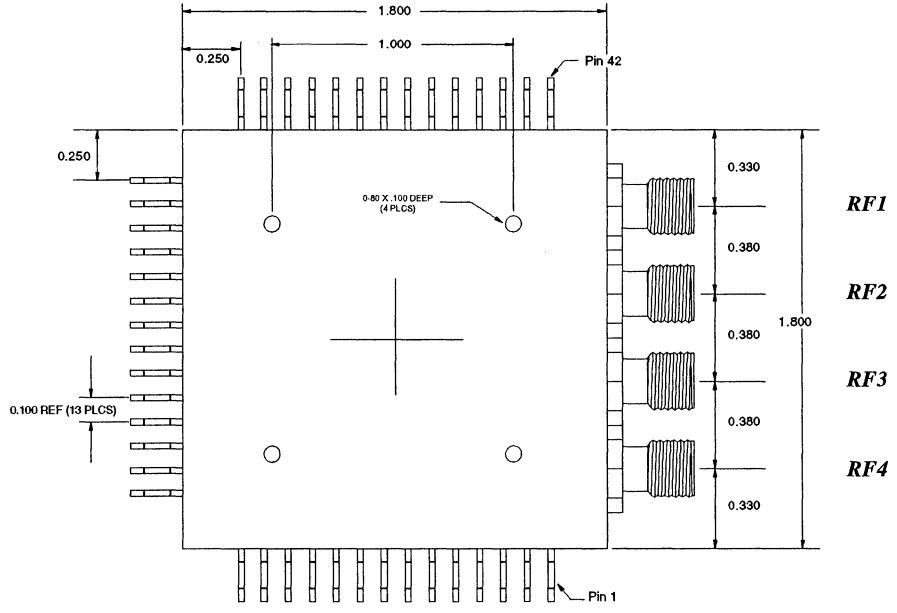
Advanced Product Information

10 Gbits/sec 16-Bit Mux/Demux
for STS-192 and STM-64 Applications

Package Information

VSC8071/8072 Module

Heat Sink Side



Module Side View

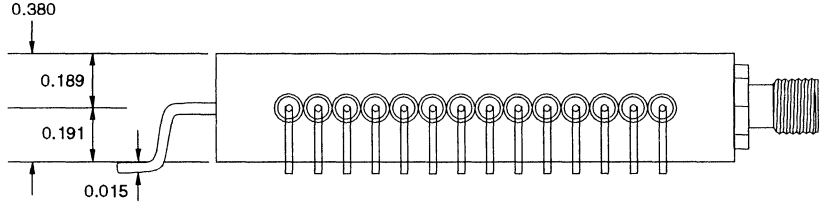
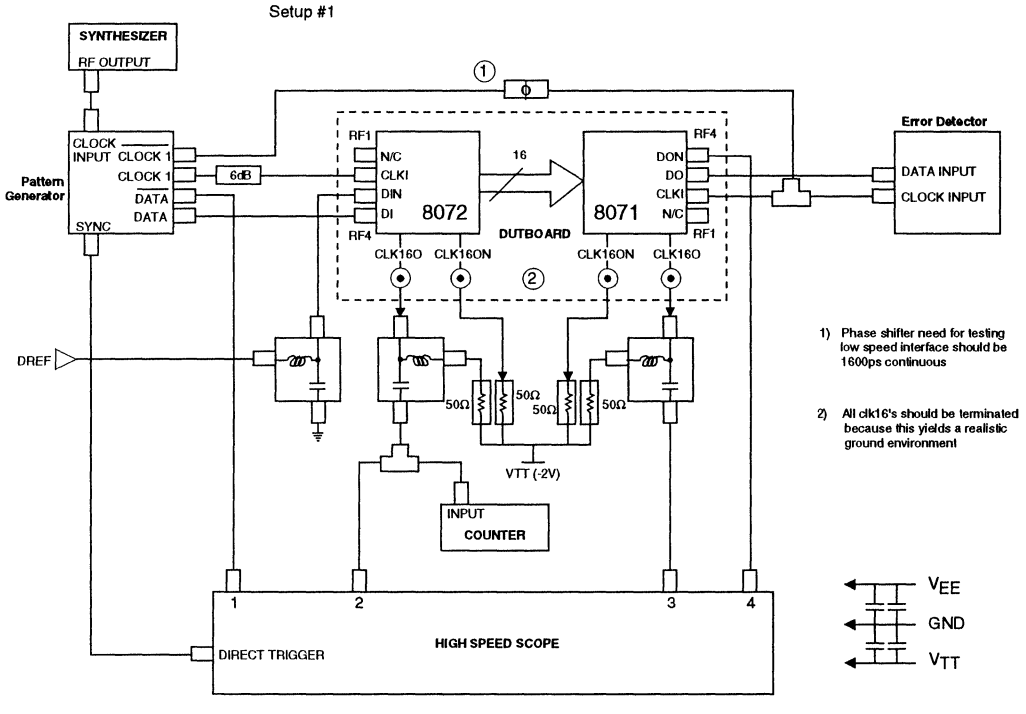


Table 9: Package Pin Table

PIN #	*VSC8071*	*VSC8072*	*PIN #*	*VSC8071*	*VSC8072*	*PIN #*	*VSC8071*	*VSC8072*
1	Gnd	Gnd	17	D10	Q05	33	D00	Q15
2	Vc	Vc	18	D09	Q06	34	Vee	Vee
3	Vd	Vd	19	D08	Q07	35	Clk16i	NC
4	Gnd	Gnd	20	Gnd	Gnd	36	Vtt	Vcca
5	Vbb	NC	21	Vtt	Vcca	37	Clk16in	NC
6	Clk16o	Clk16on	22	Vee	Vee	38	Pd	Pd
7	Vtt	Vcca	23	Gnd	Gnd	39	Pu	Pu
8	Clk16on	Clk16	24	D07	Q08	40	Vc01*	Vc01*
9	Vee	Vee	25	D06	Q09	41	Vc02*	Vc02*
10	D15	Q00	26	D05	Q10	42	Gnd	Gnd
11	D14	Q01	27	D04	Q11			
12	D13	Q02	28	Gnd	Gnd			
13	D12	Q03	29	Vee	Vee	RF1	NC	NC
14	Vee	Vee	30	D03	Q12	RF2	CLKI	CLKI
15	Gnd	Gnd	31	D02	Q13	RF3	DO	DIN
16	D11	Q04	32	D01	Q14	RF4	DON	DI

Note
(1) * Not Currently Implemented

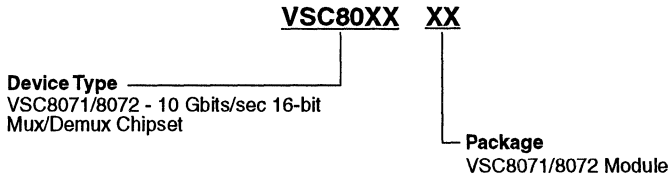
Figure 12: Setup #1 Typical Test Configuration



TYPICAL TEST CONFIGURATION

Ordering Information

The order number for this product is formed by a combination of the device number, and package type.



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Preliminary Data Sheet

155.52 Mb/s Clock and Data Recovery Units

Features

- Recovers Clock and Data at STS-3 (155.52 Mb/s) Data Rate.
- No External Components Required.
- Available in One-channel (VSC8101) or Eight-channel (VSC8102) Versions.
- Recovers Data from NRZ or NRZI Data Streams.
- No Output Clock Drift in Absence of Data Transitions Once Lock is Acquired.
- ECL or Psuedo ECL (PECL) Differential Inputs and Outputs.
- Maximum Power Dissipation: VSC8101: 400mW, VSC8102: 3W.
- Single 2V Power Supply
- Available in 28PLCC (VSC8101) and 100PQFP (VSC8102)

Functional Description

The VSC8101 and VSC8102 are clock and data recovery units for STS-3 (155.52 Mb/s) applications. They implement the complete clock and data recovery functions and require no external components. The one-channel device, VSC8101, accepts serial data in NRZ or NRZI format and re-times the data using a sampling clock extracted from the input data stream. The recovered clock (RCLK+/-) and re-timed data (RDAT+/-) are presented at the serial output ports, aligned such that the falling edge of the recovered clock (RCLK+) coincides with the center of the data eye (see figure 4). The VSC8102 is an octal version of the VSC8101. A single reference clock input (REFCK+/-) at the STS-3 data rate (155.52MHz) is required for either device. The data and reference clock inputs, and the recovered data and clock outputs are differential ECL levels referenced to the V_{CC} supply. Only one supply, +2V or -2V, is required for operation.

Both the VSC8101 and VSC8102 employ a digital clock extraction technique, and do not contain a conventional PLL. As a result, the spectrum of the jitter in the recovered clock and data is non-Gaussian. Peak-to-peak jitter of RCLK+/- is ± 400 ps or less. The data input rate to the devices is required to be within ± 30 ppm from the reference clock frequency. The devices have data input jitter accommodation up to 3.2ns, half the data period. The VSC8101and VSC8102 also provide an input which control the loop bandwidth of the clock extraction function.

Tracking Frequency Bandwidth Control

The tracking of the recovered clock and data to the frequency variation of the input data stream can be adjusted in the VSC8101 and VSC8102. In particular, the FILTER0 input controls the degree to which the internal clock can track the input data frequency. The effect is equivalent to controlling the loop bandwidth of a conventional PLL-based clock recovery system. Equivalent bandwidths of 150 KHz and 10 KHz can be selected. The FILTER0 input truth data is shown in the AC Characteristic Table.

Jitter Tolerance

The VSC8101 and VSC8102 are designed to meet the BellcoreGR-253-CORE, section 5.6.2.2.2 Jitter Tolerance specification.

Figure 1: Jitter Tolerance Mask for STS-3

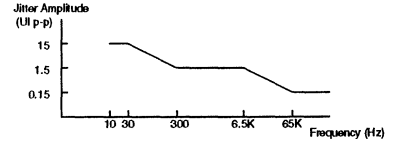


Figure 2: VSC8101 Block Diagram

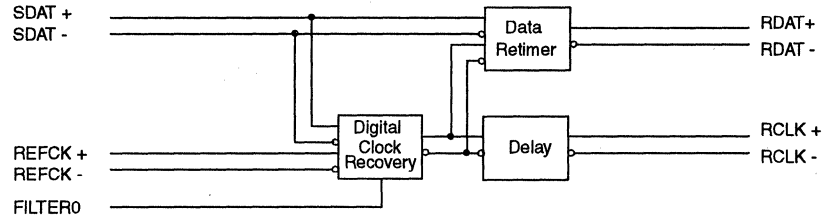
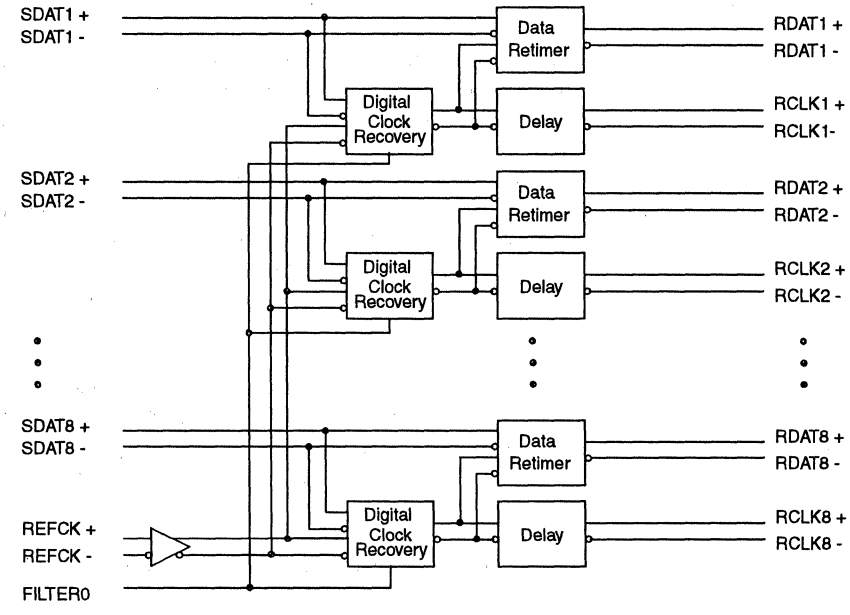


Figure 3: VSC8102 Block Diagram



Preliminary Data Sheet

155.52 Mb/s Clock and Data Recovery Units

VSC8101/8102 AC Characteristics *(Over recommended operating range*

Parameter	Description	Min	Typ	Max	Units
t_{CLK}	REFCK+/- Input Clock period[1]	—	6.43	—	ns
t_{DCYC}	SDAT +/- Input data period	t_{CLK} - 30 ppm	—	t_{CLK} + 30 ppm	
Δf_{DC}	SDAT+/- Input Rate Difference with respect to REFCK+/-	-30	—	+30	ppm
t_{CDC}	REFCK+/- Duty Cycle	40	—	60	%
t_{DH}	Recovered Data hold time from falling edge of Recovered Clock[2]	2.5	—	3.9	ns
t_{DS}	Recovered Data setup time to falling edge of Recovered Clock[2]	2.5	—	3.9	ns
t_{RCH}	RCLK+/- Recovered Clock Output High Pulse Width	2.6	—	—	ns
t_{RCL}	RCLK+/- Recovered Clock Output Low Pulse Width	2.6	—	—	ns
t_{RCYC}	RCLK+/- Recovered Clock Period	6.0	—	6.8	ns
t_{DJA}	SDAT+/- Input Jitter Accommodation (DC to 20 MHz) Peak-to-peak	—	—	3.2	ns
t_{LA}	Lock Acquisition Time [3]	—	—	5.0	µs
f_{BW}	Loop Bandwidth: a) at FILTER0 = Lo b) at FILTER0 = Hi	—	—	150 10	KHz
t_{RCJ}	RCLK+/- Recovered Clock Jitter	-400		400	ps
t_{PD}	Propagation Delay from SDATA+/- Input to RDAT+/- Output	—	—	TBD	ps
t_{Cr}, t_{Cf}	REFCK+/- Input rise and fall time, 20% to 80%	—	—	1.2	ns
t_{SDr}, t_{SDf}	SDATA+/- Input rise and fall time, 20% to 80%	—	—	1.2	ns
t_{RCr}, t_{RCf}	RCLK+/- Recovered Clock Output rise and fall time, 20% to 80%	300	—	800	ps
t_{RDr}, t_{RDf}	RDAT+/- Recovered Data Output rise and fall time, 20% to 80%	300	—	800	ps

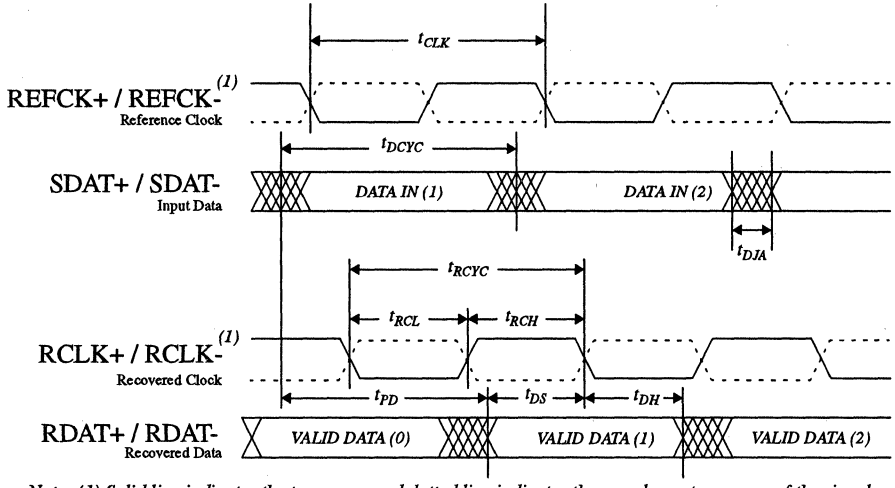
Notes: (1) The part is designed to operate at 155.52 MHz. A reference clock with frequency variation of +/- 50 ppm or better is recommended. Consult the factory for applications other than this frequency.

(2) With minimum 50% Input Data Eye opening at 155.52 Mb/s.

(3) With a jitter-free data input and minimum transition density of 50%.

Telecom/ATM

Figure 4: VSC8101/8102 AC Timing Waveform



Note: (1) Solid line indicates the true sense and dotted line indicates the complementary sense of the signal.

Absolute Maximum Ratings (1)

Power Supply Voltage (V_{CC} -V_{TT}) ..... -0.5V to +3.0V
Input Voltage (V_{IN}) ..... V_{CC} -2.5V to V_{CC} + 0.5V
Output Current, I_{OUT} (DC, Output HI) ..... -50mA
Case Temperature Under Bias, T_C ..... -55° to +125°C
Storage Temperature (T_{STG}) ..... -65°C to +135°C

Recommended Operating Conditions

The VSC8101 and VSC8102 can be powered by:
a) connecting V_{CC} to +2V and V_{TT} to GND, or
b) connecting V_{CC} to GND and V_{TT} to -2V.

Power Supply Voltage (V_{CC} -V_{TT}) ..... 2.0V ± 5%
Operating Temperature Range(2) ..... 0° to +70°C

Notes:
(1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing pe manent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.
(2) Lower limit is ambient temperature and upper limit is case temperature.

Preliminary Data Sheet

155.52 Mb/s Clock and Data Recovery Units

VSC8101/8102 DC Characteristics *(Over recommended operating conditions)*

Table 1: Inputs and Outputs

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{IH}	Input HIGH voltage	V_{CC} - 1150	—	V_{CC} - 600	mV	Guaranteed HIGH signal for all inputs
V_{IL}	Input LOW voltage	V_{TT}	—	V_{CC} - 1500	mV	Guaranteed LOW signal for all inputs
V_{OH}	Output HIGH voltage	V_{CC} - 1020	—	V_{CC} - 700	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min). Outputs terminated identically into V_{TT} with 50 ohms.
V_{OL}	Output LOW voltage	V_{TT}	—	V_{CC} - 1620	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min). Outputs terminated identically into V_{TT} with 50 ohms.
ΔV_I	Input voltage swing for REFCK+/- and SDAT+/-	450	—	—	mV	(1) For AC-Coupling: input swing at the pin. (2) For DC-Coupling: input swing referenced to the common mode voltage;
V_{OCM}	Output common mode voltage for RDAT+/- and RCLK+/-	.5 + V_{TT}	—	.8 + V_{TT}		Differential Outputs terminated identically into V_{TT} with 50 ohms.
ΔV_O	Output voltage swing for RDAT+/- and RCLK+/-	600	—	—	mV	Differential Outputs terminated identically into V_{TT} with 50 ohms.

Table 2: Power Dissipation

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
P_D	Power dissipation (VSC8101)	—	—	400	mW	Outputs open, $V_{CC} = 2.1V$
P_D	Power dissipation (VSC8102)	—	—	3.0	W	same as above
I_{CC}	Supply current (VSC8101)	—	—	190	mA	same as above
I_{CC}	Supply current (VSC8102)	—	—	1430	mA	same as above

Generation of 2V Supply for the VSC8101/VSC8102

In a ECL system, -2V will be one of the standard supplies and the VSC8101/VSC8102 can be powered with GND and -2V. However, for typical TTL systems, 2V is generally not available. In these applications, the 2V supply can be generated easily from a 5V or 3.3V supply. There are several manufacturers who supply complete single-chip linear regulators. Examples are:

Table 3: Linear Regulators and Suppliers

Device	*Regulator Recommended*	*Maximum Supply Current*	*Manufacturer's Information*
VSC8101	REG1117	800mA	Burr Brown, 800-548-6132
VSC8102	LT1086	1.5A	Linear Tech, 408-432-1900

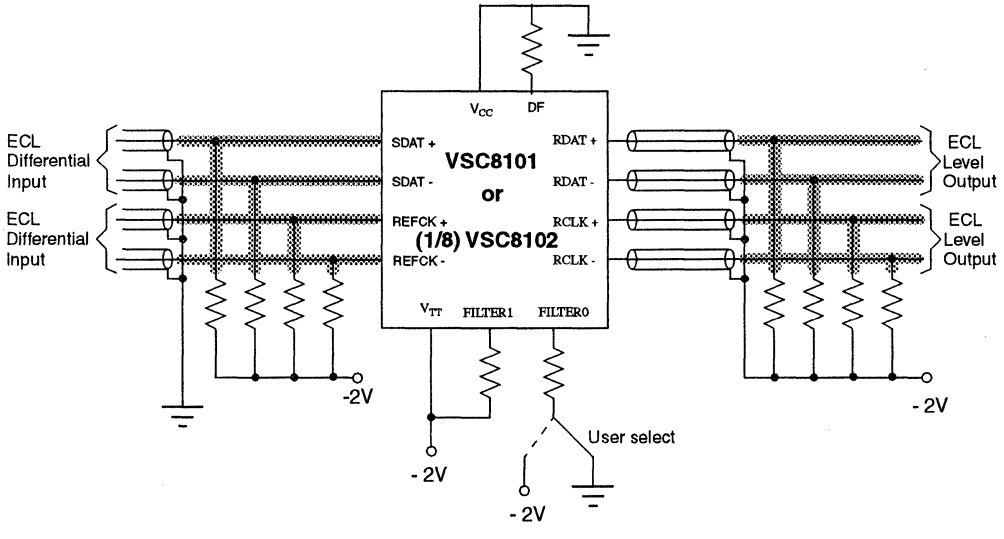
Note: (1) Complete data sheets for these regulators can be obtained from the manufacturers.

Preliminary Data Sheet

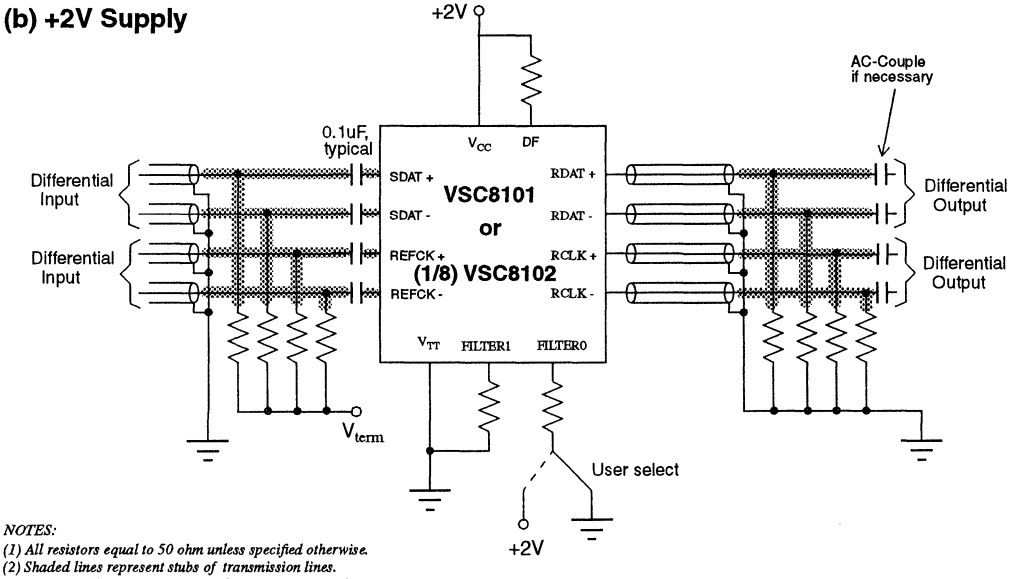
155.52 Mb/s Clock and Data Recovery Units

Figure 5: Typical Applications

(a) -2V Supply



(b) +2V Supply



NOTES:
(1) All resistors equal to 50 ohm unless specified otherwise.
(2) Shaded lines represent stubs of transmission lines. They should have the corresponding traces on board be as short as possible to minimize reflection.

Table 4: VSC8101 Pin Description

Signal Name	*Pin*	*Level*	*Description*
REFCK+	5	ECL	Reference Clock input true
REFCK-	6	ECL	Reference Clock input complement
SDAT+	9	ECL	Data input true
SDAT-	10	ECL	Data input complement
RCLK+	25	ECL	Recovered Clock true
RCLK-	23	ECL	Recovered Clock complement
RDAT+	21	ECL	Recovered Data true
RDAT-	19	ECL	Recovered Data complement
FILTER0	16	V_{CC}/V_{TT}	Selects the Loop Bandwidth: (1) FILTER0 = LO, Bandwidth = 150 KHz (2) FILTER0 = HI, Bandwidth = 10 KHz
FILTER1	17	V_{TT}	For normal operation, connect to V_{TT} thru 50 ohm resistor
DF	14	V_{CC}	For normal operation, connect to V_{CC} thru 50 ohm resistor
NC	1-3,7,11,13, 15,27,28		Do not connect, leave open
VCC	8,20,22,24		Positive supply, V_{CC}
VTT	4,12,18,26		Negative supply, V_{TT}

Figure 6: VSC8101 Pin Diagram

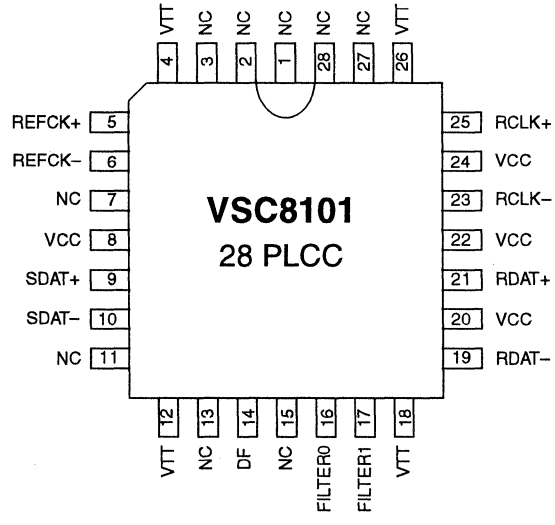
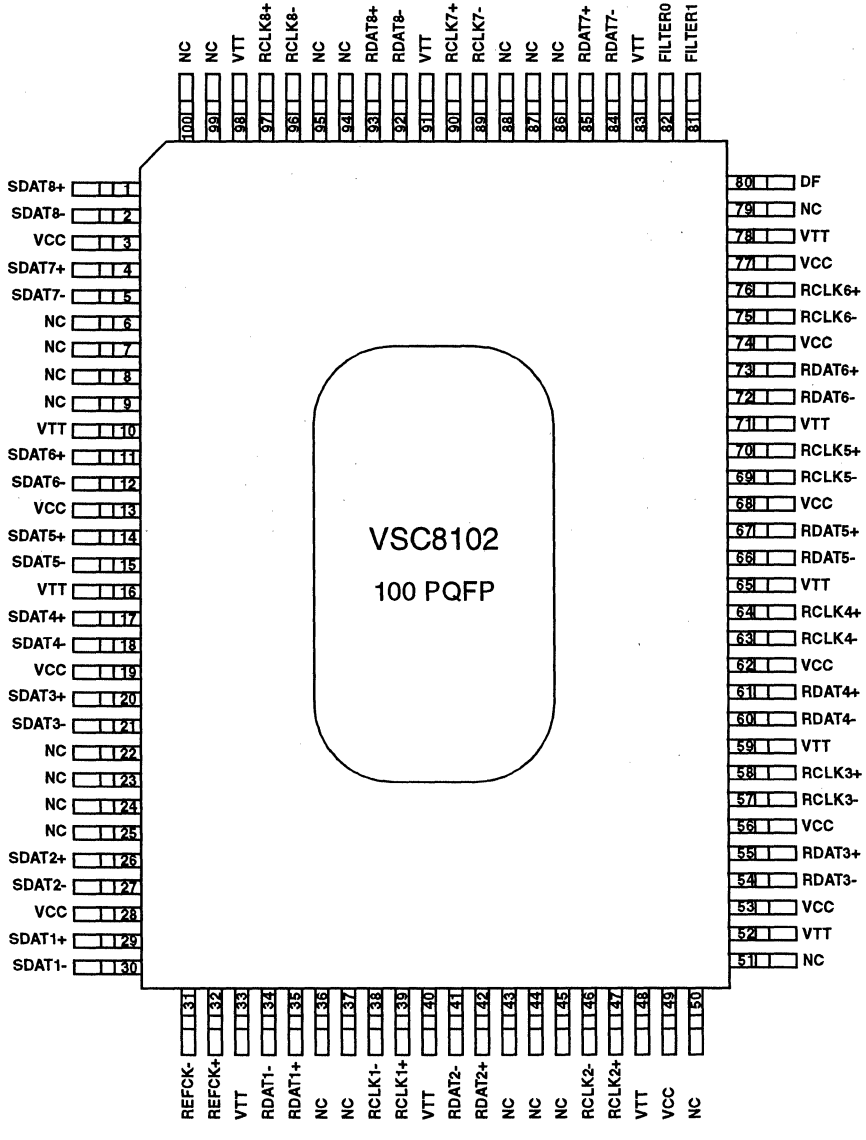


Table 5: VSC8102 Pin Description

Signal Name	*Pin*	*Level*	*Description*
REFCK+	32	ECL	Reference Clock Input True
REFCK-	31	ECL	Reference Clock input complement
SDAT+	29,26,20,17, 14,11,4,1	ECL	Data input true
SDAT-	30,27,21,18, 15,12,5,2	ECL	Data input complement
RCLK+	39,47,58,64, 70,76,90,97	ECL	Recovered Clock true
RCLK-	38,46,57,63, 69,75,89,96	ECL	Recovered Clock complement
RDAT+	35,42,55,61, 67,73,85,93	ECL	Recovered Data true
RDAT-	34,41,54,60, 66,72,84,92	ECL	Recovered Data complement
FILTER0	82	V_{CC}/V_{TT}	Selects the Loop Bandwidth: (1) FILTER0 = LO, Bandwidth = 150 KHz (2) FILTER0 = HI, Bandwidth = 10 KHz
FILTER1	81	V_{TT}	For normal operation, connect to V_{TT} thru 50 ohm resistor
DF	80	V_{CC}	For normal operation, connect to V_{CC} thru 50 ohm resistor
NC	6-9,22-25,36,37,43-45,50,51,79, 86-88,94,95, 99,100		Do not connect, leave open
VCC	3,13,19,28,49,53,56, 62,68, 74,77		Positive supply, V_{CC}
VTT	10,16,33,40, 48,52,59,65, 71,78,83,91, 98		Negative supply, V_{TT}

Figure 7: VSC8102 Pin Diagram



DRAWING IS HEAT SINK UP

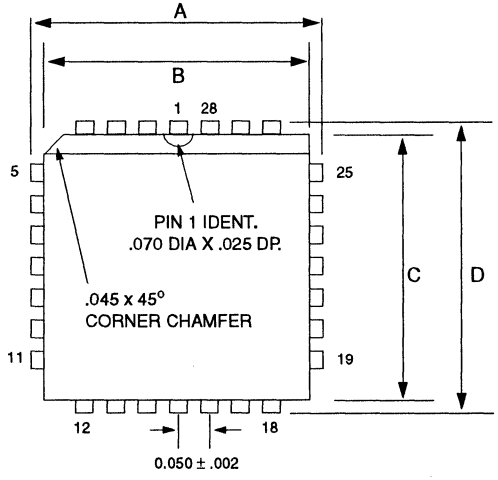
Preliminary Data Sheet

155.52 Mb/s Clock and Data Recovery Units

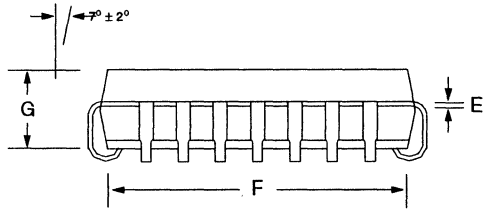
Package Information

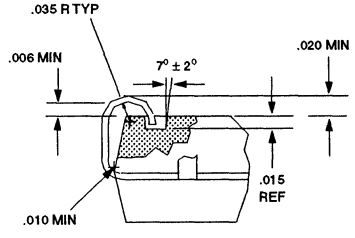
The VSC8101 is packaged in a 28-pin Plastic Leaded Chip Carrier (PLCC), 0.454 x 0.454 in.^{2} body size. The VSC8102 is packaged in a 100-pin Plastic Quad Flat Pack (PQFP), 20 x 14 mm^2 body size).

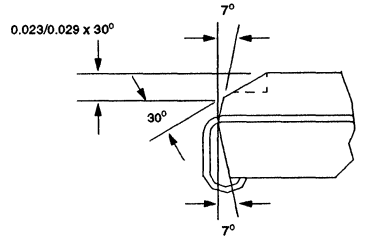
Figure 8: VSC8101 Package Drawings (28PLCC-JEDEC)



Item	inch	Tol.
A	.490	± .005
B	.454	± .002
C	.454	± .002
D	.490	± .005
E	.010	± .0003
F	.420	±.010
G	.152	± .002

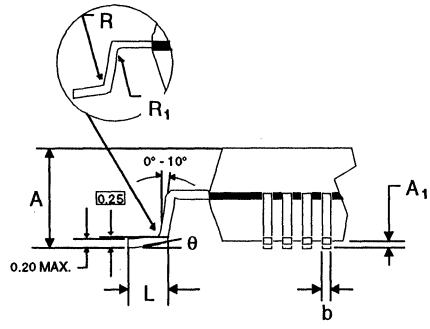




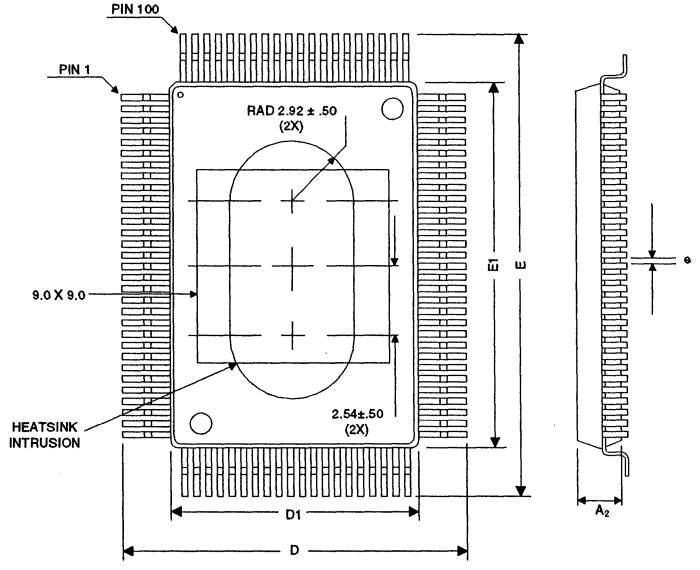


NOTES:
(1) Drawings not to scale.
(2) All units in inch unless otherwise noted.

Figure 9: VSC8102 Package Drawings (100PQFP)



Dims.	mm	Tolerance
A	3.40	MAX
A1	0.60	MAX
A2	2.7	±.10
D	17.20	±.40
D1	14.00	±.10
E	23.20	±.40
E1	20.00	±.10
L	0.80	±.2
e	0.65	NOM
b	0.30	±.10
θ	0-10°	
R	.25	NOM
R1	.2	NOM



NOTES:

(1) Drawings not to scale.
(2) Two styles of exposed heat spreaders may be used; square or oval.
(3) All units in millimeters

Thermal Characteristics of the VSC8101 and VSC8102 Packages

VSC8101

The VSC8101 is packaged in a 28PLCC, with an internal heat spreader for improved heat dissipation. With natural convection, the Case to Air Thermal Resistance (θ_{CA})is estimated to be 65°C/W.

VSC8102

The VSC8102 is packaged in a thermally enhanced 100PQFP with an embedded heat spreader. The heat spreader surface area is shown in figure 9. With natural convection, the Case to Air Thermal Resistance (θ_{CA})is estimated to be 27.5°C/W. The Air Flow versus Thermal Resistance relationship is shown in the following table:

Table 6: θ_{CA} Versus Air Velocity for the VSC8102 Package

Air Velocity (LFPM)	*Case to Air Thermal Resistance (°C/W)*
0	27.5
100	23.1
200	19.8
400	17.6
600	16

Ordering Information

The order numbers for this product family are:

Part Number	Device Type
VSC8101JA:	1-Channel Clock and Data Recovery Unit in 28 Pin PLCC
VSC8102QB:	8-Channel Clock and Data Recovery Unit in 100 Pin PQFP

Notice

This document contains information about a product during its preproduction phase of development. The information in this document is based on test results and initial product characterization. Characteristic data and other specifications are subject to change without notice. Therefore the reader is cautioned to confirm that this datasheet is current prior to design or order placement.

Warning

Vitesse Semiconductor Corporation products are not intended for use in life support appliances, devices or systems. Use of a Vitesse product in such applications without written consent is prohibited.

Data Sheet

ATM/SONET/SDH 155/622 Mb/s Transceiver
Mux/Demux with Integrated Clock Generation

Features

- Operates at Either STS-3/STM-1 (155.52 Mb/s) or STS-12/STM-4 (622.08 Mb/s) Data Rates
- Compatible with Industry ATM UNI Devices
- On Chip Clock Generation of the 155.52 Mhz or 622.08 Mhz High Speed Clock
- Reference Clock Frequencies Selectable for 19.44, 38.88, 51.84 and 77.76 Mhz
- 8 bit Parallel TTL Interface
- Integrated PLL for Clock Generation - No External Components
- SONET/SDH Frame Recovery
- Provides Equipment and Facilities Loopback
- Low Power - 1.98 Watts Maximum
- Dual Supply Operation- +2, +5 Volts
- 100 PQFP Package

General Description

The VSC8110 is an ATM/SONET/SDH compatible transceiver integrating high speed clock generation with 8 bit serial-to-parallel and parallel-to-serial data conversion. The high speed clock is generated using an on-chip PLL which is selectable for 155.52 or 622.08 Mhz operation. The part can be used with 19.44, 38.88, 51.84 or 77.76 Mhz external reference clocks. The demultiplexer contains SONET/SDH frame detection and recovery. In addition, the device provides both facility and equipment loopback modes. The part is packaged in a 100PQFP with integrated heat spreader for optimum thermal performance and reduced cost. The VSC8110 provides an integrated solution for ATM physical layers and SONET/SDH systems applications.

Functional Description

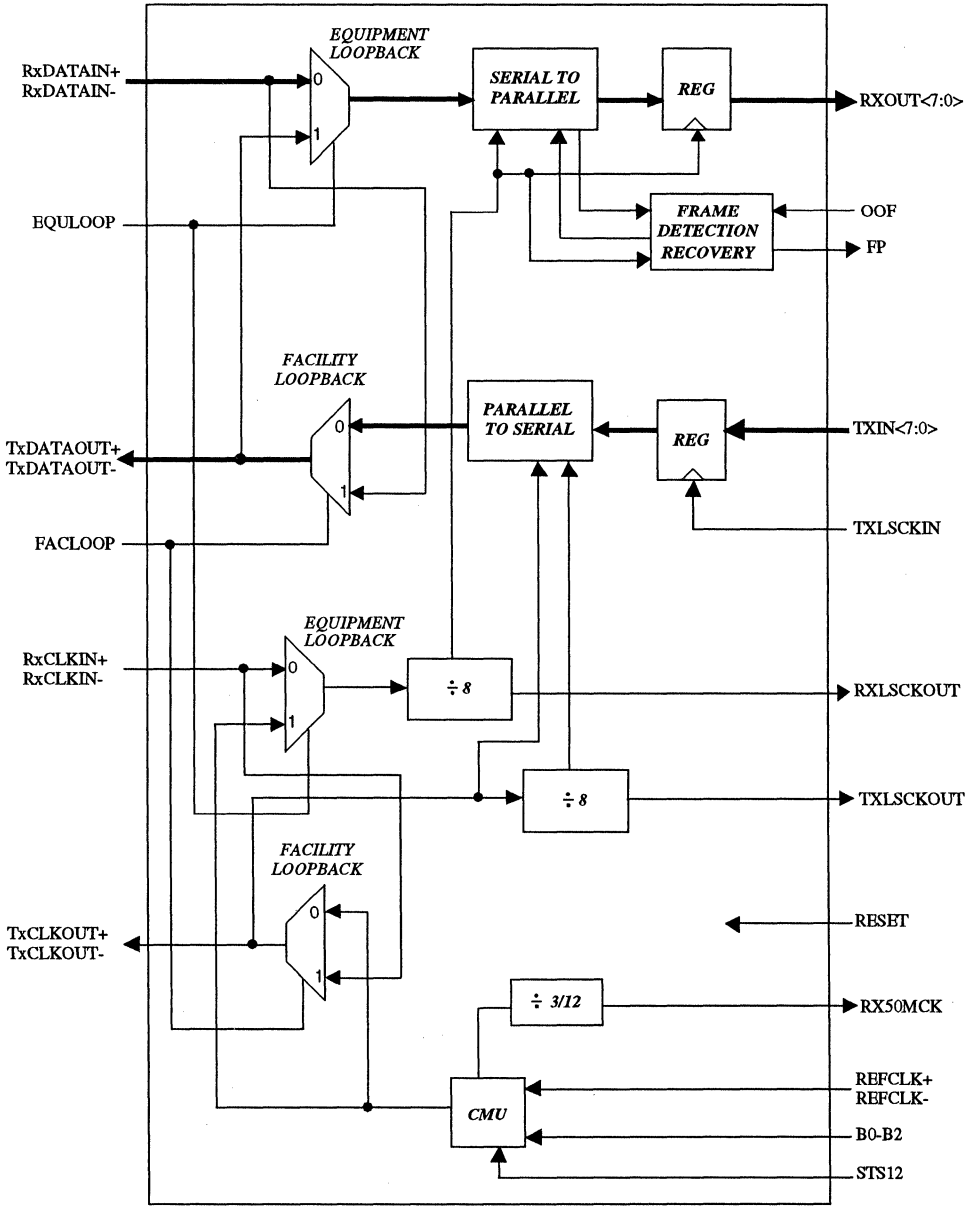
The VSC8110 is designed to provide a SONET/SDH compliant interface between the high speed optical networks and the lower speed User Network Interface devices such as the PM5355 S/UNI-622. The VSC8110 converts 8 bit parallel data at 77.76Mhz or 19.44Mhz to a serial bit stream at 622.08Mb/s or 155.52Mb/s respectively. The transmit section provides a Facility Loopback function which loops the received high speed data and clock directly to the transmit outputs. A clock multiplier unit is integrated into the transmit circuit to generate the high speed clock for the serial output data stream from input reference frequencies of 19.44, 38.88, 51.84 or 77.76 Mhz. The block diagram on page 2 shows the major functional blocks associated with the VSC8110.

The receive circuit provides the serial-to-parallel conversion, converting 155Mb/s or 622Mb/s to an 8 bit parallel output at 19.44Mhz or 77.76Mhz respectively. The receive section provides an Equipment Loopback function which will loop the high speed transmit data and clock back through the demultiplexer to the 8 bit parallel outputs.

Transmit Circuit

Byte-wide data is presented to TXIN<7:0> and is clocked into the part on the rising edge of TXLSCKIN; refer to Figure 1. The data is serialized (MSB leading) and presented at the TxOUT+/- pins. The Clock Multiplier Unit (CMU) generates the high speed clock required for serialization and transmission. The high speed clock accompanying the transmitted data appears on the TxCLKOUT+/- pins. The reference clock is selectable using the control lines BO-B2; refer to Table 13. The data rate (155Mb/s or 622Mb/s) is selected using the STS12 control pin; refer to Table 13. The Facility Loopback mode is set by FACLOOP and is active high. A 51.84Mhz continuous clock (RX50MCK) is provided as a general board-level clock to drive other circuits such as the UTOPIA interface on the UNI devices.

VSC8110 Block Diagram



Receive Circuit

155Mb/s or 622Mb/s serial data and 155Mhz or 622Mhz clock are input to RxIN+/- and RxCLKIN+/- pins respectively; refer to Figure 1. This data is converted to byte-wide parallel data and presented on RXOUT<7:0> pins; refer to Figure 4. The received high speed clock is divided by 8 and presented on the RXLSCKOUT pin.

The receive circuit includes frame detection and recovery. The frame circuitry detects the SONET/SDH frame, aligns the received serial data on byte boundaries, and initiates a frame pulse on FP coincident with the byte aligned data. The frame recovery is initiated when OOF is held high which must occur at least 4 byte clock cycles before the A1A2 boundary. OOF is a level-sensitive signal, and the VSC8110 will continually perform frame detection and recovery as long as this pin is held high even if 1 or more frames has been detected. Frame detection and recovery occurs when a series of three A1 bytes followed by three A2 bytes has been detected. The parallel output data on RXOUT<7:0> will be byte aligned starting on the third A2 byte. When a frame is detected, a pulse is generated on FP. The pulse FP is synchronized with the byte-aligned third A2 byte on RXOUT<7:0>. The FP pulse is one byte clock period long. The frame detector sends an FP pulse only if OOF is high or if a frame was detected while OOF was being pulled low.

Facility Loopback

The Facility Loopback function is controlled by the FACLOOP signal. When the FACLOOP signal is set high, the Facility Loopback mode is activated and the high speed serial receive data (RxDATAIN) is presented at the high speed transmit output (TxDATAOUT). In addition, the high speed receive clock input (RxCLKIN) is selected and presented at the high speed transmit clock output (TxCLKOUT). In Facility Loopback mode the high speed receive data (RxDATAIN) is also converted to parallel data and presented at the low speed receive data output pins (RXOUT<7:0>). The receive clock (RxCLKIN) is also divided down and presented at the low speed clock output (RXLSCKOUT). The Facility and Equipment Loopbacks are not designed to be enabled at the same time.

Equipment Loopback

The Equipment Loopback function is controlled by the EQULOOP signal. When the EQULOOP signal is set high, the Equipment Loopback mode is activated and the high speed transmit data generated from the parallel to serial conversion of the low speed data (TXIN<0:7>) is selected and converted back to parallel data on the receiver circuit side and presented at the low speed parallel outputs (RXOUT<7:0>). The internally generated 155Mhz/622Mhz clock is used to generate the low speed receive clock output (RXLSCKOUT), (Note that the clock presented at RXLSCKOUT can be changed to present the clock applied to the EXTCLKP/N pins if the EXTVCO control pin is set active high. In this mode EXTCLK is also presented at the TXCLKOUT and TXLSCKOUT pins.) In Equipment Loopback mode the transmit data (TXIN<7:0>) is serialized and presented at the high speed output (TxDATAOUT) along with the high speed transmit clock (TxCLKOUT) which is generated by the on board clock multiplier unit. The facility and Equipment Loopbacks are not designed to be enabled at the same time.

AC Timing Characteristics

Figure 1: Receive Data and Clock Block Diagram

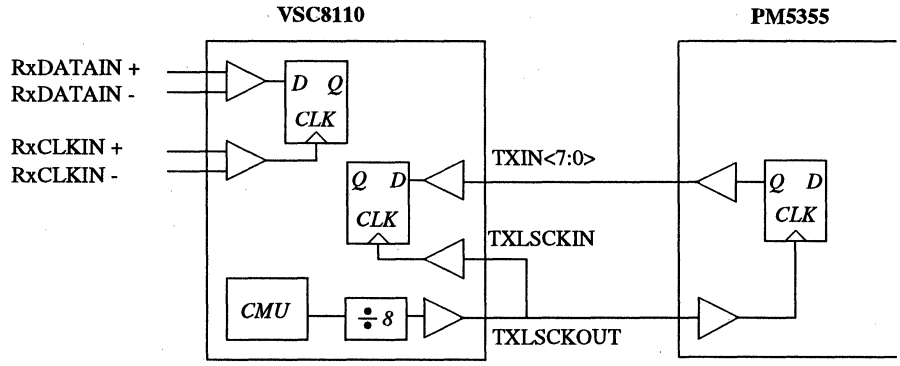


Figure 2: Receive High Speed Data Input Timing Diagram

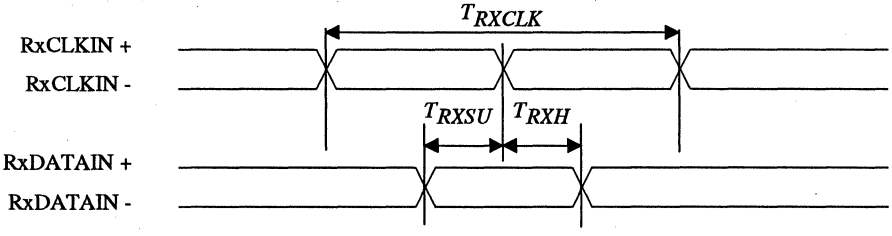


Table 1: Receive High Speed Data Input Timing Table *(STS-12 Operation)*

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{RXCLK}	Receive clock period	-	1.608	-	ns
T_{RXSU}	Serial data setup time with respect to RxCLKIN	500	-	-	ps
T_{RXH}	Serial data hold time with respect to RxCLKIN	500	-	-	ps

Table 2: Receive High Speed Data Input Timing Table *(STS-3 Operation)*

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{RXCLK}	Receive clock period	-	6.43	-	ns
T_{RXSU}	Serial data setup time with respect to RxCLKIN	1.5	-	-	ns
T_{RXH}	Serial data hold time with respect to RxCLKIN	1.5	-	-	ns

Figure 3: Transmit Data Input Timing Diagram

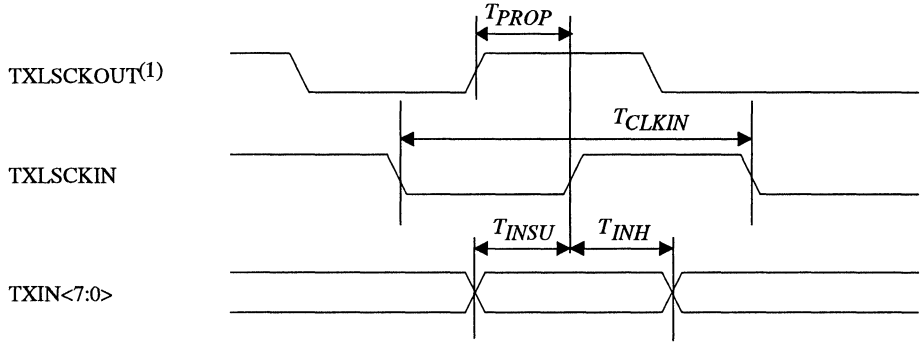


Table 3: Transmit Data Input Timing Table *(STS-12 Operation)*

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{CLKIN}	Transmit data input byte clock period	-	12.86	-	ns
T_{INSU}	Transmit data setup time with respect to TXLSCKIN	1.0	-	-	ns
T_{INH}	Transmit data hold time with respect to TXLSCKIN	1.0	-	-	ns
T_{PROP}	Maximum allowable propagation delay for connecting TXLSCKOUT to TXLSCKIN	-	-	3	ns

Note: Duty cycle for TXLSCKOUT is 50% +/- 5% worse case

Table 4: Transmit Data Input Timing Table *(STS-3 Operation)*

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{CLKIN}	Transmit data input byte clock period	-	51.44	-	ns
T_{INSU}	Transmit data setup time with respect to TXLSCKIN	1.0	-	-	ns
T_{INH}	Transmit data hold time with respect to TXLSCKIN	1.0	-	-	ns
T_{PROP}	Maximum allowable propagation delay for connecting TXLSCKOUT to TXLSCKIN	-	-	3	ns

Figure 4: Data and Clock Transmit Block Diagram

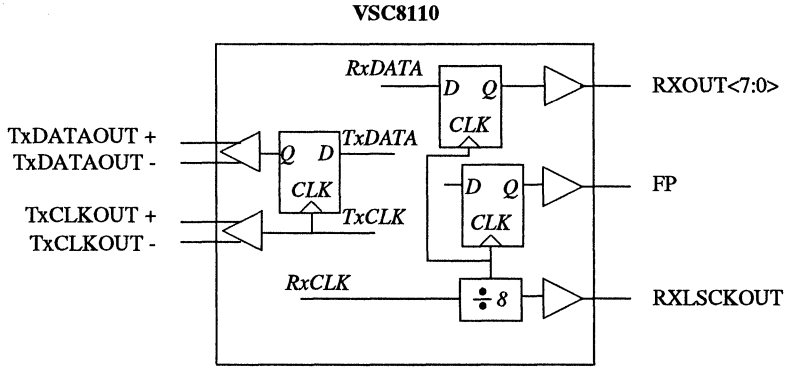


Figure 5: Receive Data Output Timing Diagram

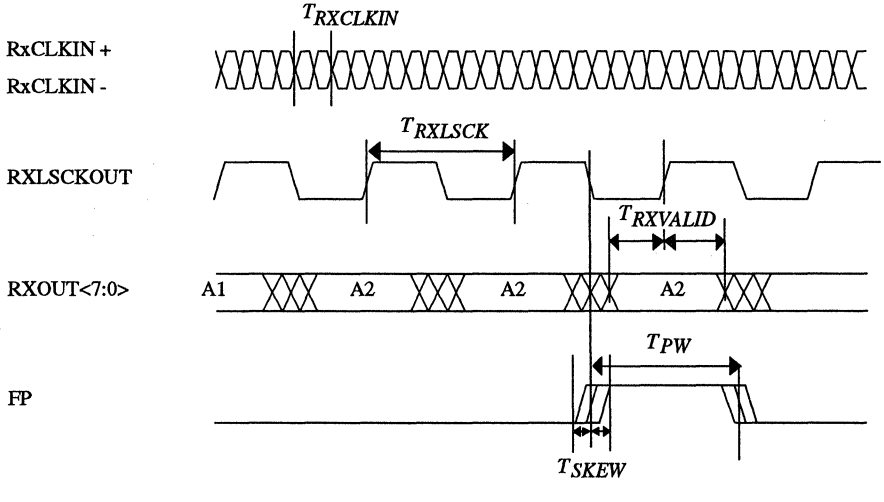


Table 5: Receive Data Output Timing Table *(STS-12 Operation)*

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
$T_{RXCLKIN}$	Receive clock period	-	1.608	-	ns
T_{RXLSCK}	Receive data output byte clock period	-	12.86	-	ns
T_{SKEW}	Range in which the rising edge of FP will appear in relation to the falling edge of RXLSCKOUT	-	-	+/-1.5	ns
$T_{RXVALID}$	Time data on RXOUT<7:0> is valid before and after the rising edge of RXLSCKOUT	4.9	-	-	ns
T_{PW}	Pulse width of frame detection pulse FP	-	12.86	-	ns

Table 6: Receive Data Output Timing Table *(STS-3 Operation)*

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
$T_{RXCLKIN}$	Receive clock period	-	6.43	-	ns
$T_{RXLSCKT}$	Receive data output byte clock period	-	51.44	-	ns
T_{SKEW}	Range in which the rising edge of FP will appear in relation to the falling edge of RXLSCKOUT	-	-	+/-1.5	ns
$T_{RXVALID}$	Time data on RXOUT<7:0> is valid before and after the rising edge of RXLSCKOUT	24	-	-	ns
T_{PW}	Pulse width of frame detection pulse FP	-	51.44	-	ns

Figure 6: Transmit High Speed Data Timing Diagram

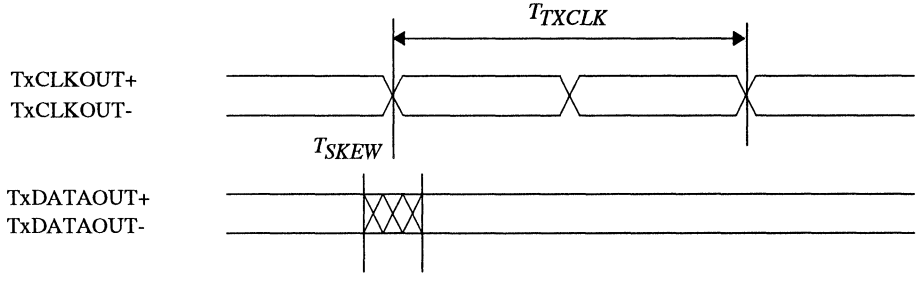


Table 7: Transmit High Speed Data Timing Table *(STS-12 Operation)*

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{TXCLK}	Transmit clock period	-	1.608	-	ns
T_{SKEW}	Skew between the falling edge of TxCLKOUT and valid data on TxDATAOUT	-	-	+/-200	ps

Table 8: Transmit High Speed Data Timing Table *(STS-3 Operation)*

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{TXCLK}	Transmit clock period	-	6.43	-	ns
T_{SKEW}	Skew between the falling edge of TxCLKOUT and valid data on TxDATAOUT	-	-	+/-200	ps

Data Latency

The VSC8110 contains several operating modes, each of which exercise different logic paths through the part. Table 9 bounds the data latency through each path with an associated clock signal.

Table 9: Data Latency

Circuit Mode	*Description*	*Clock Reference*	*Range of Clock cycles STS-12*	*Range of Clock cycles STS-3*
Transmit	Data TXIN<7:0> to MSB at TxDATAOUT	TxCLKOUT	2-11	2-11
Receive	MSB at RxDATAIN to data on RXOUT<7:0>	RxCLKIN	18-25	15-22
Equipment Loopback	Byte data TXIN<7:0> to byte data on RXOUT<7:0>	TxCLKOUT	19-33	17-31
Facilities Loopback	MSB at RxDATAIN to MSB at TxDATAOUT	RxCLKIN	10	10

Absolute Maximum Ratings[1]

Power Supply Voltage (V_{MM}) Potential to GND ..... -0.5V to +2.5V
Power Supply Voltage (V_{TTL}) Potential to GND ..... -0.5V to +5.5V
TTL Input Voltage Applied ..... -0.5V to V_{TTL} + 1.0V
VECL Input Voltage Applied ..... -0.5V to V_{MM} + 1.0V
Output Current (I_{OUT}) 50mA
Case Temperature Under Bias (T_C) ..... -55° to + 125°C
Storage Temperature (T_{STG}) ..... -65° to + 150°C

Note: Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Recommended Operating Conditions

Power Supply Voltage (V_{MM}) ..... +2.0V±5 %
Power Supply Voltage (V_{TTL}) ..... +5.0V±5 %
Commercial Operating Temperature Range* (T) ..... 0° to 70°C

** Lower limit of specification is ambient temperature and upper limit is case temperature.*

ESD Ratings

Proper ESD procedures should be used when handling this product. The VSC8110 is rated to the following ESD voltages based on the human body model:

1. All pins are rated at or above 1500V.

DC Characteristics

Table 10: VECL Inputs and Outputs

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	V_{MM}-1020	-	V_{MM}-850	mV	50 ohm to gnd
V_{OL}	Output LOW voltage	V_{MM}-2000	-	V_{MM}-1620	mV	50 ohm to gnd
V_{IH}	Input HIGH voltage	V_{MM}-1100	-	V_{MM}-700	mV	Guaranteed HIGH signal for all inputs
V^{IL}	Input LOW voltage	V_{MM}-2000	-	V_{MM}-1540	mV	Guaranteed LOW signal for all inputs
I_{IH}	Input HIGH current	-	-	200	uA	V_{IN}=V_{IH} (max)
I_{IL}	Input LOW current	-50	-	-	uA	V_{IN}=V_{IL} (min)
V_{DIFF}	Input Voltage Differential	200	-	-	mV	
V_{CM}	Common Mode Voltage	V_{MM}-1.5	-	V_{MM}-0.5	V	

Note: Differential VECL output pins must be terminated identically.

Table 11: TTL Inputs and Outputs

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	2.4	-	-	mV	V_{IN} = V_{IH} (max) or V_{IL} (min) I_{OH}=-2.4mA
V_{OL}	Output LOW voltage	0	-	0.5	mV	V_{IN} = V_{IH} (max) or V_{IL} (min) I_{OL}=8mA
V_{IH}	Input HIGH voltage	2.0	-	V_{TTL}+1.0	mV	Guaranteed HIGH signal for all inputs
V_{IL}	Input LOW voltage	0	-	0.8	mV	Guaranteed LOW signal for all inputs
I_{IH}	Input HIGH current	-	-	50	uA	V_{IN}=V_{IH} (max)
I_{IL}	Input LOW current	-500	-	-	uA	V_{IN}=V_{IL} (min)
I_{OZH}	3-State Output OFF current HIGH	-	-	200	uA	V_{OUT}=2.4V
I_{OZL}	3-State Output OFF current LOW	-200	-	-	uA	V_{OUT}=0.5V

Power Dissipation

Table 12: Power Supply Currents

Parameter	Description	(Max)	Units
I_{MM}	Power supply current from V_{MM}	430	mA
I_{TTL}	Power supply current from V_{TTL}	218	mA
P_D	Power dissipation	1.98	W

Note: Specified with outputs open circuit. The combined maximum currents (I_{MM}, I_{TTL}) for any part will not exceed 1.98 Watts.

Clock Multiplier Unit

Table 13: Reference Frequency Selection and Output Frequency Control

STS12	B2	B1	B0	Reference Frequency [MHz]	Output Frequency [MHz]
1	1	1	0	19.44	622.08
1	0	1	0	38.88	622.08
1	0	0	1	51.84	622.08
1	0	0	0	77.76	622.08
0	1	1	0	19.44	155.52
0	0	1	0	38.88	155.52
0	0	0	1	51.84	155.52
0	0	0	0	77.76	155.52

Table 14: Clock Multiplier Unit Performance

Name	Description	Min	Typ	Max	Units
RCd	Reference clock duty cycle	40		60	%
RCj	Reference clock jitter (RMS)			5	ps
OCd	Output clock duty cycle	40		60	%
OCj	Output clock jitter (RMS) @ 77.76 MHz ref			8	ps
OCj	Output clock jitter (RMS) @ 51.84 MHz ref			10	ps
OCj	Output clock jitter (RMS) @ 38.88 MHz ref			13	ps
OCj	Output clock jitter (RMS) @ 19.44 MHz ref			15	ps
OCfmin	Minimum output frequency			620	MHz
OCfmax	Maximum output frequency			624	MHz

Note: Jitter specification is defined utilizing a 12KHz - 5MHz LP-HP single pole filter.

Package Pin Description

Table 15: Pin Definitions

Signal	Pin	I/O	Level	Pin Description
FACLOOP	1	I	TTL	Facility loopback, active high
VMM	2		+2V	+2 volt supply
_VSCTE	3	I	TTL	Test pin enable. Tie low for system operation
RESET	4	I	TTL	Resets frame detection, dividers, controls, and tristates TTL outputs; active high
EXTVCO	5	I	TTL	Test mode control; tie low for system operation
B0	6	I	TTL	Reference clock select, refer to table 13
B1	7	I	TTL	Reference clock select, refer to table 13
B2	8	I	TTL	Reference clock select, refer to table 13
VMM	9		+2V	+2 volt supply
TxDATAOUT+	10	O	VECL	Transmit output, high speed differential data +
TxDATAOUT-	11	O	VECL	Transmit output, high speed differential data -
VCC	12		GND	Ground
TxCLKOUT+	13	O	VECL	Transmit high speed clock differential output+
TxCLKOUT-	14	O	VECL	Transmit high speed clock differential output-
VMM	15		+2V	+2 volt supply
EXTCLKP	16	I	VECL	External clock input+, test mode only; tie to V_{MM} for system operation
EXTCLKN	17	I	VECL	External clock input-, test mode only; tie to ground for system operation
VCC	18		GND	Ground
RxCLKIN+	19	I	VECL	Receive high speed differential clock input+
RxCLKIN-	20	I	VECL	Receive high speed differential clock input-
VMM	21		+2V	+2 volt supply
OOF	22	I	TTL	Out Of Frame; Frame detection initiated with high level
NC	23			No connection
RxDATAIN+	24	I	VECL	Receive high speed differential data input+
RxDATAIN-	25	I	VECL	Receive high speed differential data input-
NC	26			No connection
NC	27			No connection
VMM	28		+2V	+2 volt supply
NC	29			No connection

Signal	Pin	I/O	Level	Pin Description
_VSCIPNC	30	I	TTL	Test mode input. Tie low for system operation
VTTL	31		+5.0V	+5 volt supply
_VSCOPNC	32	O	VECL	Test mode output
RX50MCK	33	O	TTL	Constant 51.84Mhz reference clock output, derived from the Clock Multiplier Unit
VCC	34		GND	Ground
RXOUT0	35	O	TTL	Receive output data bit0
RXOUT1	36	O	TTL	Receive output data bit1
VCC	37		GND	Ground
RXOUT2	38	O	TTL	Receive output data bit2
RXOUT3	39	O	TTL	Receive output data bit3
VCC	40		GND	Ground
RXOUT4	41	O	TTL	Receive output data bit4
RXOUT5	42	O	TTL	Receive output data bit5
VCC	43		GND	Ground
RXOUT6	44	O	TTL	Receive output data bit6
RXOUT7	45	O	TTL	Receive output data bit7
VCC	46		GND	Ground
RXLSCKOUT	47	O	TTL	Receive byte clock output
FP	48	O	TTL	Frame detection pulse
VTTL	49		+5.0V	+5 volt supply
NC	50			No connection
NC	51			No connection
NC	52			No connection
NC	53			No connection
VMM	54		+2V	+2 volt supply
VCC	55		GND	Ground
REFCLK+	56	I	VECL	Differential reference clock input+, refer to table 13
REFCLK-	57	I	VECL	Differential reference clock input-, refer to table 13
VTTL	58		+5.0V	+5 volt supply (CMU)
VCC	59		GND	Ground (CMU)
VCC	60		GND	Ground (CMU)
NC	61			No connection
NC	62			No connection

Signal	Pin	I/O	Level	Pin Description
NC	63			No connection
NC	64			No connection
NC	65			No connection
NC	66			No connection
VTTL	67		+5.0V	+5 volt supply (CMU)
VTTL	68		+5.0V	+5 volt supply (CMU)
VTTL	69		+5.0V	+5 volt supply (CMU)
VCC	70		GND	Ground (CMU)
VCC	71		GND	Ground (CMU)
VCC	72		GND	Ground (CMU)
NC	73			No connection
NC	74			No connection
VCC	75		GND	Ground
VMM	76		+2V	+2 volt supply
NC	77			No connection
NC	78			No connection
NC	79			No connection
NC	80			No connection
VTTL	81		+5.0V	+5 volt supply
TXLSCKOUT	82	O	TTL	Transmit byte clock out
TXLSCKIN	83	I	TTL	Transmit byte clock in
VCC	84		GND	Ground
TXIN7	85	I	TTL	Transmit input data bit7
TXIN6	86	I	TTL	Transmit input data bit6
VCC	87		GND	Ground
TXIN5	88	I	TTL	Transmit input data bit5
TXIN4	89	I	TTL	Transmit input data bit4
NC	90			No connection
TXIN3	91	I	TTL	Transmit input data bit3
TXIN2	92	I	TTL	Transmit input data bit2
VCC	93		GND	Ground
TXIN1	94	I	TTL	Transmit input data bit1
TXIN0	95	I	TTL	Transmit input data bit0
NC	96			No connection

Signal	Pin	I/O	Level	Pin Description
STS12	97	I	TTL	155Mb/s or 622Mb/s mode select, refer to table 13
PLLM	98	O	VECL	PLL test output, leave unconnected in system operation
VTTL	99		+5.0V	+5 volt supply
EQULOOP	100	I	TTL	Equipment loopback, active high

The VSC8110 is manufactured in a 100PQFP package which is supplied by two different vendors. The critical dimensions in the drawing represent the superset of dimensions for both packages. The significant difference between the two packages is in the shape and size of the heatspreader which needs to be considered when attaching a heatsink.

Package Thermal Characteristics

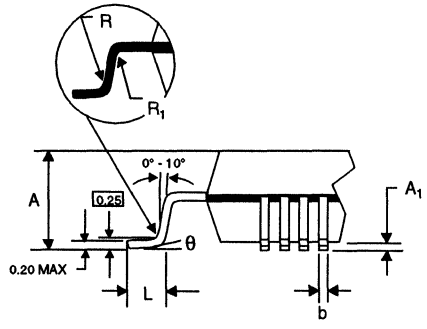
The VSC8110 is packaged in a thermally enhanced 100PQFP with an embedded heat sink. The heat sink surface configurations are shown in the package drawings. With natural convection, the case to air thermal resistance is estimated to be 27.5°C/W. The air flow versus thermal resistance relationship is shown in table 16.

Table 16: Theta Case to Ambient versus Air Velocity

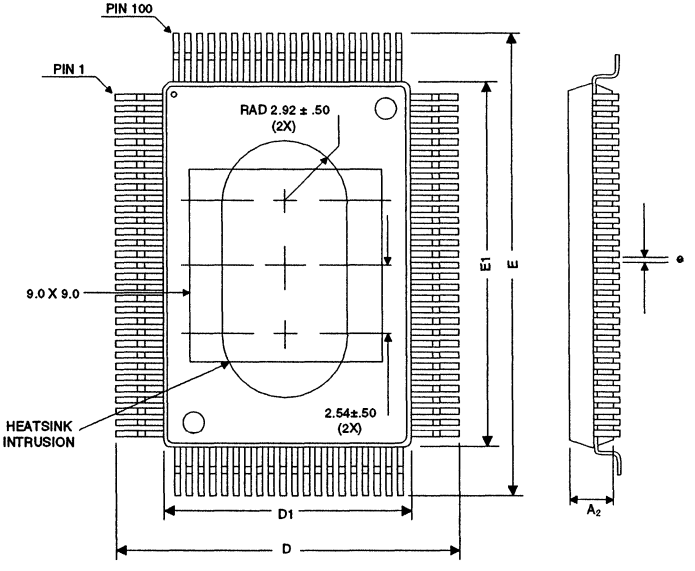
Air Velocity (LFPM)	Case to air thermal resistance °C/W
0	27.5
100	23.1
200	19.8
400	17.6
600	16

Package Information

100 PQFP Package Drawings



Dims.	mm	Tolerance
A	3.40	MAX
A1	0.60	MAX
A2	2.7	±.10
D	17.20	±.40
D1	14.00	±.10
E	23.20	±.40
E1	20.00	±.10
L	0.80	±.2
e	0.65	NOM
b	0.30	±.10
θ	0-10°	
R	.25	NOM
R1	.2	NOM



NOTES:
(1) Drawings not to scale.
(2) Two styles of exposed heat spreaders may be used; square or oval.
(3) All units in millimeters

Data Sheet

ATM/SONET/SDH 155/622 Mb/s Transceiver
Mux/Demux with Integrated Clock Generation

Ordering Information

The order numbers for this product are:

Part Number	Device Type
VSC8110QB:	155Mb/s-622Mb/s Mux/Dmux with CMU in 100 Pin PQFP Commercial temperature, 0°C ambient to 70° case
VSC8110QB1:	155Mb/s-622Mb/s Mux/Dmux with CMU in 100 Pin PQFP Extended temperature, 0°C ambient to 110° case
VSC8110QB2:	155Mb/s-622Mb/s Mux/Dmux with CMU in 100 Pin PQFP Industrial temperature, -40°C ambient to 85°C case

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Warning

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Application Notes

2 Volt Supply Generation From 5 Volts

The 2 volt supply can be generated from the 5 volt supply using a linear regulator. There are many manufacturers who supply linear regulators. Refer to Table 17 for examples.

Table 17: Recommended 2 Volt Voltage Regulator

Recommended Regulator	*Maximum Supply Current*	*Manufacturer's Information*
REG1117	800mA	Burr Brown 800-548-6132
LT117A	800mA	Linear Technology

Interconnecting the Byte Clocks (TXLSCKOUT and TXLSCKIN)

The byte clock (TXLSCKOUT and TXLSCKIN) on the VSC8110 has been brought off-chip to allow as much flexibility in system-level clocking schemes as possible. Since the byte clock (TXLSCKOUT) clocks both the VSC8110 and the UNI devices, it is important to pay close attention to the routing of this signal. The UNI device in general is a CMOS part which can have very wide spreads in timing (1-11ns clock in to parallel data out for the PM5355), which utilizes most of the 12.86ns period (at 78Mhz), leaving little for the trace delays and set-up times required to interconnect the 2 devices. The recommended way of routing this clock when used in a 622Mhz mode is to daisy chain it to the UNI device pin and then route it back to the VSC8110 along with the byte data. This eliminates the 1-way trace delay that would otherwise be encountered between the data and clock and thus leaves 1.86ns for the VSC8110 setup time and for variations in trace delays and rise times between clock and data. The trace delay must be kept under 2ns (allowing an additional 1ns for variations in rise times and skews) to ensure proper muxing of parallel input data into the VSC8110; reference Table 3 and 4.

AC Coupling and Terminating High-speed I/Os

The high speed signals on the VSC8110 (RxDATAIN, RxCLKIN, TxDATAOUT, TxCLKOUT) use VECL levels which are essentially ECL levels shifted positive by 2 volts. The VECL I/Os are referenced to the V_{MM} supply and are terminated to ground. Since most optics modules use either ECL or PECL levels, the high speed ports need to be ac coupled to overcome the difference in dc levels. In addition, the inputs must be dc biased to hold the inputs at their threshold value with no signal applied. The dc biasing and 50 ohm termination requirements can easily be integrated together using a thevenin equivalent circuit as shown in Figure 8. The figure shows the appropriate termination values when interfacing PECL to VECL and VECL to PECL. This network provides the equivalent 50 ohm termination for the high speed I/Os and also provides the required dc biasing for both the drivers and receivers. Table 18 contains recommended values for each of the components.

Layout of the 622 Signals

The routing of the 622 signals should be done using good high speed design practices. This would include using controlled impedance lines and keeping the distance between components to an absolute minimum. In addition, stubs should be kept at a minimum as well as any routing discontinuities. This will help minimize reflections and ringing on the high speed lines and insure the maximum eye opening. In addition the output pull

down resistor should be placed as close to the VSC8110 pin as possible while the AC-coupling capacitor and the biasing resistors should be placed as close as possible to the optics input pin. The same is true on the receive circuit side. Using small outline components and minimum pad sizes also helps in reducing discontinuities.

Ground Planes

The ground plane for the components used in the 622 interface should be continuous and not sectioned in an attempt to provide isolation to various components. Sectioning of the ground planes tends to interfere with the ground return currents on the signal lines as well as in general, the smaller the ground planes the less effective they are in reducing ground bounce noise and the more difficult to decouple etc. Sectioning of the positive supplies can provide some isolation benefits.

Reference Clock Generation

It has been noted that additional jitter may be generated on the reference clock if a TTL Oscillator is level shifted using a TTL to ECL converter. The best recommendation is to use an ECL oscillator which can be AC-coupled straight into the REF CLOCK inputs on the VSC8110

Figure 7: AC Coupled High Speed I/O

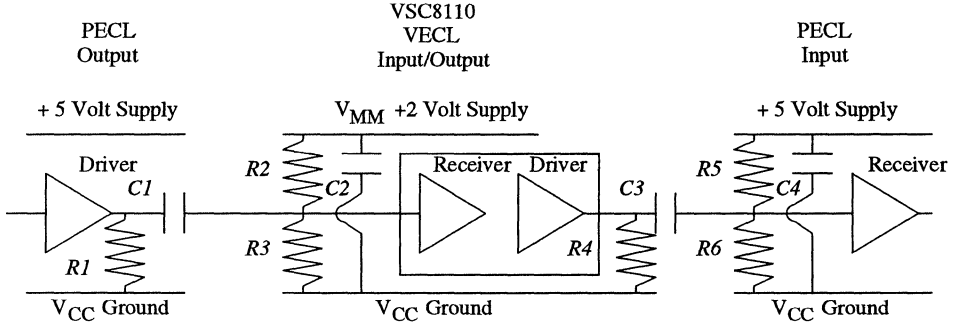


Table 18: AC Coupling Component Values

Component	*Value*	*Tolerance*
R1	270 ohms	1%
R2	147 ohms	1%
R3	76 ohms	1%
R4	50 - 100 ohms	1%
R5	68 ohms	1%
R6	190 ohms	1%
C1, C2, C3, C4	.01uf High Frequency	

Preliminary Data Sheet

ATM/SONET/SDH 622 Mb/s Transceiver
Evaluation Board Operating Description

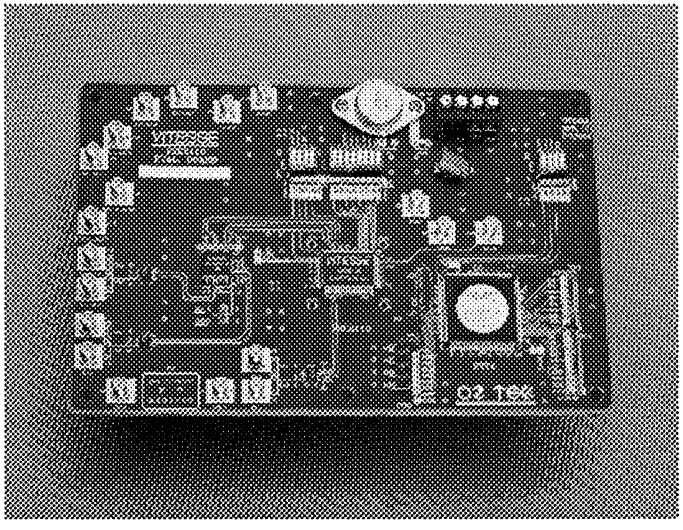
Features

- 622Mb/s at Speed Functional Operation
- Includes the PMC 5312 STTX Device for Interoperability Testing
- Completely Self Contained for Self Test Operations
- Flexibility to Evaluate the VSC8110 in All Modes Of Operation
- Mode Control Switches Included for Both the VSC8110 and PMC5312 Devices
- SMA Connections Included for High Speed Bench Characterization
- Allows Signals to be AC or Direct Coupled to the VSC8110
- ECL Buffered Interfaces are Included as an Option for High Speed Signals
- On-board Mux to Simulate Loss of Signal
- Socketed Board Option Available for the VSC8110 Device

General Description

The VSC8110 Evaluation Board provides users the ability to completely evaluate the VSC8110 device. The board contains both the VSC8110 and PMC's PM5312 devices allowing users to verify interoperability between the parts. The board is self contained and includes a self test mode between the PM5312 and the VSC8110 requiring only an external +5 volt supply. In addition, there are multiple SMA connections (both direct and AC coupled) to the high speed serial ports which allow connecting the VSC8110 to optical components for interoperability testing or to characterization equipment for jitter and waveform evaluations. LEDs are included which indicate functional status including loss of frame.

VSC8110 Evaluation Board



VSC8110 Evaluation Board Operation

Functional Description

The capability of the board can be divided into two areas. The first enables the evaluation of the VSC8110 device characteristics including output jitter, waveform integrity and basic functionality. The second allows interoperability testing with the PMC5312 as well as external optical interfaces. The board is designed to be as flexible as possible allowing direct coupled, AC coupled, single ended or differential signals and buffered high speed connections to the VSC8110. The board utilizes standard SMA connectors for all the high speed ports as well as the reference clock inputs. The board is self contained allowing for a closed loop test between the VSC8110 and the PMC5312 device. All the required passive components are included for the translation from ECL or PECL to the VSC8110 high speed I/Os. The only requirements are:

1. Connect a 5 volt supply;
2. Connect the high speed transmit outputs back to the receiver inputs;
3. Provide a reference crystal oscillator module (socket provided) at 19.44, 38.88, 51.84 or 77.76Mhz or external clock reference source to the VSC8110.

General Operation

Power Supplies

Operation of the board requires a 5 volt power supply connected to both +5 volt connectors on the power block along with a ground connection. The 5 volt supply is split to allow DC isolation of the VSC8110 from the other board components to allow measuring the supply currents. A 2 volt regulator is included on the board and no external 2 volt supply is required, however an external 2 volt connection is available on the power block as an option.

To enable the use of the mode switches (SW1, SW2, SW3) shorting connectors must be applied to all locations on CTR1, CTR2 and CTR6 pins.

Device Operation

Evaluation of the VSC8110 device can be performed by applying a reference clock to the reference clock input SMA connectors (J11 and J12) or by inserting a reference oscillator into the socket provided on the board and connecting it's output (J2, J4) to the reference clock inputs using SMA cables. The control pins (SW1 and SW2) must be set appropriately for the reference clock frequency and for the operation mode of the part; i.e. 622Mb/s or 155Mb/s along with the loopback modes. Note that the PMC5312 is not designed to work in a 155Mb/s mode and therefore a closed loop test at 155Mb/s is not possible on this evaluation board. With the exception of B0-B2 (B0, B1 and B2 set the reference frequency), most of the mode control switches should be set in the off position making them inactive. All of the controls on the VSC8110 are active high. This will insure the part is not in loopback mode or in reset mode and places the part in 622Mb/s mode. U4 is a differential receiver and is provided to insure clean edges are applied to the VSC8110 reference clock inputs. The input to this device and to the VSC8110 are AC coupled with a Thevenin equivalent 50 ohm termination on the input side of each device. In addition T4A and T4B are used to tie either input to VBB in the Motorola device if a single ended reference clock signal is applied.

Upon applying a reference clock to the part, the transmit data and clock outputs can be examined with or without applying data to the receive inputs. The high speed differential clock and data outputs go directly to the SMA connections J9 and J10, and J5 and J6 respectively. Note that these outputs are referenced to the +2 volt supply.

Multiple SMA connections are provided for the high speed receive clock and data inputs. The standard configuration for the board is to apply clock and data signals at the J13, J17, J15 and J14 inputs respectively. In this configuration the input signals are AC coupled onto the board with a Thevenin equivalent 50 ohm termination and the inputs are buffered by the Motorola receiver circuits, U3 and U5. T1A, T1B, T3A and T3B are provided for single-ended signals, connecting one side of each input to the VBB reference on the Motorola part. The U2 device is a Mux and is provided to allow a simulated loss of signal using the buffered inputs. This is accomplished by the connection at T2.

J7, J18, J16 and J8 SMAs are provided as alternative inputs into the VSC8110. This is controlled by the connections at T5, T6, T7 and T8. These connections allow the receive clock and data to be connected directly to the VSC8110 using J8, J18 and J16 and J8 respectively. There is a Thevenin equivalent 50 ohm termination on these lines. At this same connection point it is possible to insert a capacitor for AC coupling into the inputs. Again note the input buffers on the VSC8110 are referenced to +2 volts.

Connector T10 provides a convenient point to examine the 50Mhz free running output clock produced by the VSC8110.

SMA connections J3, J1 and J19 are used to exercise various test modes within the VSC8110 and not intended to be used by the customer.

Interoperability Testing

The VSC8110 parallel output bus and input bus are directly connected to the PMC5312 device. Test points are provided for each signal line via connectors CTR8 and CTR7 which can used to connect a high impedance scope probe.

Status signals from the PMC5312 are accessible via CTR5. The control signals LOF, LAIS, LOS and FERF are connected to LEDs providing a visual indication of these signals.

The data output bus on the PMC5312 is tied directly back to the input bus. This allows serial data received by the VSC8110 high speed inputs to be looped completely through the PMC5312 and fed back through the VSC8110 to the high speed transmit outputs, allowing for a closed loop evaluation using a SONET or BERT tester. This allows complete functional and at speed verification of the VSC8110 and PMC5312 to insure interoperability between the two components.

Key control lines for the PMC5312 can be set using SW3. By resetting the RSTB line the PMC5312 will reset itself and thus force a re-framing sequence to occur. This can be used to verify that the VSC8110 and 5312 are correctly working together and that the frame detection and byte alignment circuits are functioning and can repeatedly and correctly perform frame alignment.

T9 is a connector used to connect the low speed byte clock generated by the VSC8110 to the PMC5312. This clock is used by the PMC5312 to clock the data out and into the VSC8110. This connection should have a shorting bar on it to insure operation of the PMC5312.

Self Test Operation

A closed loop functional at speed test can be run on the board requiring only a 5 volt supply and a reference clock. This self test operation requires the use of SMA cables to connect the high speed transmit clock and data to the high speed receive clock and data. Note the differential clock signal needs to be inverted when connecting it to the receive side of the board. This is accomplished by connecting J5 to J14, J6 to J15 for the data, J13 to J9 and J17 to J10 for the clock. The reference clock is applied to the J12 and J11 inputs. The B0-B2 switches must be set for the correct reference frequency. The remaining switches should be set to the off position to disable the other modes of operation. When power is applied, random data will continuously loop through the VSC8110 and PMC5312 devices. A visual indication of operation can be obtained by removing the data cables while the devices are running. This will cause a LOF signal to be generated by the PMC5312 and the LOF LED will light. Replacing the cable will allow the devices to re-frame and the LED LOF indicator will turn off. Another test is to use the RSTB switch to reset the PMC5312 which will force the PMC5312 to request a re-frame from the VSC8110. This can be performed multiple times to demonstrate that the re-framing sequence consistently occurs. The LED will flicker each time, but will go off once the device has re-framed.

Preliminary Data Sheet

ATM/SONET/SDH 155/622 Mb/s Transceiver
Mux/Demux with Integrated Clock Generation

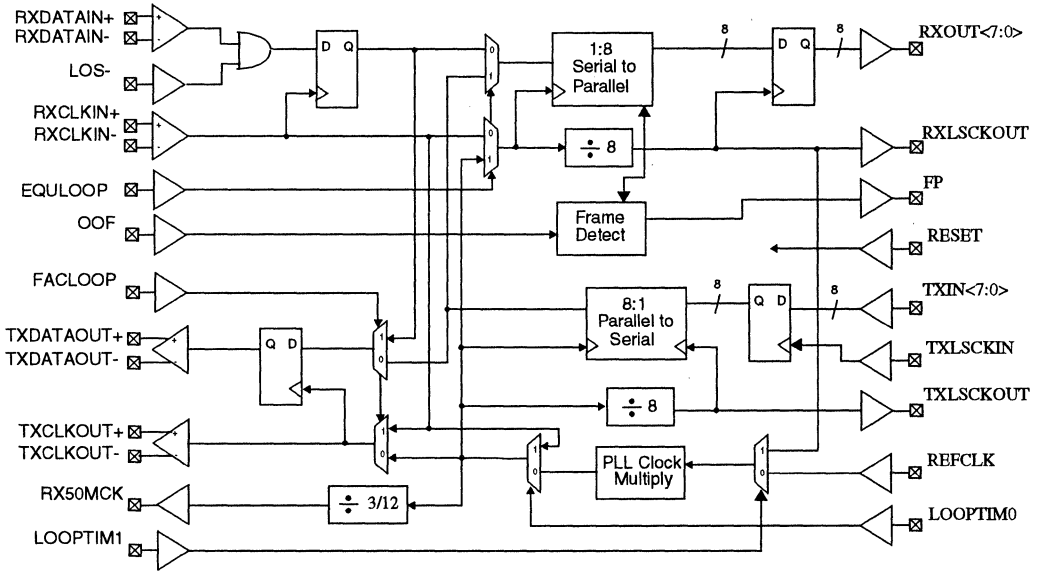
Features

- Operates at Either STS-3/STM-1 (155.52 Mb/s) or STS-12/STM-4 (622.08 Mb/s) Data Rates
- Compatible with Industry ATM UNI Devices
- On Chip Clock Generation of the 155.52 Mhz or 622.08 Mhz High Speed Clock
- 8 Bit Parallel TTL Interface
- SONET/SDH Frame Recovery
- Loss of Signal (LOS) Control
- Provides Equipment, Facilities and Split Loop-back Modes as well as Loop Timing Mode
- Meets or Exceeds Bellcore, ITU and ANSI Specifications for Jitter Performance
- Single 3.3V Supply Voltage
- Low Power - 1.2 Watts Maximum
- 100 PQFP Package

General Description

The VSC8111 is an ATM/SONET/SDH compatible transceiver integrating high speed clock generation and clock recovery 8 bit serial-to-parallel and parallel-to-serial data conversion. The high speed clock is generated using an on-chip PLL which is selectable for 155.52 or 622.08 Mhz operation. The demultiplexer contains SONET/SDH frame detection and recovery. In addition, the device provides both facility and equipment loop-back modes. The part is packaged in a 100PQFP with integrated heat spreader for optimum thermal performance and reduced cost. The VSC8111 provides an integrated solution for ATM physical layers and SONET/SDH systems applications.

VSC8111 Block Diagram



Functional Description

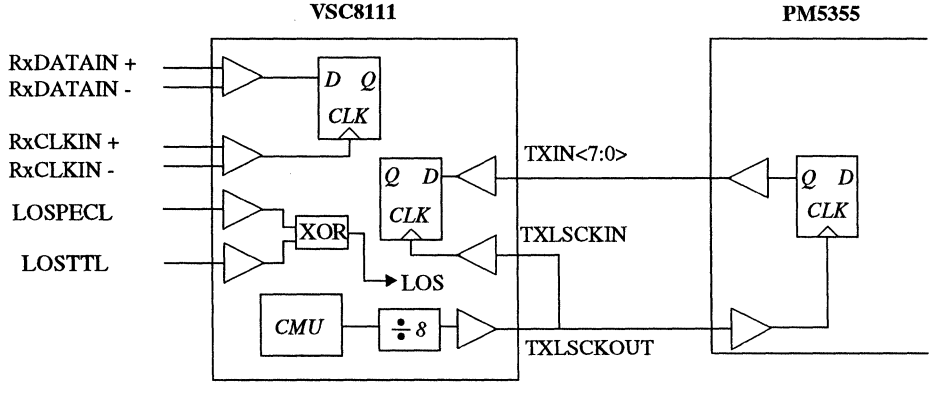
The VSC8111 is designed to provide a SONET/SDH compliant interface between the high speed optical networks and the lower speed User Network Interface devices such as the PM5355 S/UNI-622. The VSC8111 converts 8 bit parallel data at 77.76Mhz or 19.44Mhz to a serial bit stream at 622.08Mb/s or 155.52Mb/s respectively. The transmit section provides a Facility Loopback function which loops the received high speed data and clock directly to the transmit outputs. A Clock Multiplier Unit (CMU) is integrated into the transmit circuit to generate the high speed clock for the serial output data stream from input reference frequencies of 19.44, 38.88, 51.84 or 77.76 Mhz. The CMU can be bypassed with the receive clock in loop timing mode thus synchronizing the entire part to a single clock (RXCLKIN). The block diagram on page 1 shows the major functional blocks associated with the VSC8111.

The receive circuit provides the serial-to-parallel conversion, converting 155Mb/s or 622Mb/s to an 8 bit parallel output at 19.44Mhz or 77.76Mhz respectively. The receive section provides an Equipment Loopback function which will loop the high speed transmit data and clock back through the demultiplexer to the 8 bit parallel outputs.

Transmit Circuit

Byte-wide data is presented to TXIN<7:0> and is clocked into the part on the rising edge of TXLSCKIN (refer to Figure 1). The data is then serialized (MSB leading) and presented at the TxOUT+/- pins. The serial output stream is synchronized to the CMU generated clock which is a phase aligned and frequency scaled version of the input reference clock. External control inputs B0-B2 and STS12 select the multiply ratio of the CMU and either STS-3 (155Mb/s) or STS-12 (622Mb/s) transmission (see table 12). A divide-by-8 version of the CMU clock (TXLSCKOUT) should be used to synchronize the transmit interface of the UNI device to the transmit receive registers on the VSC8111 (Figure 1)

Figure 1: Receive Data and Clock Block Diagram



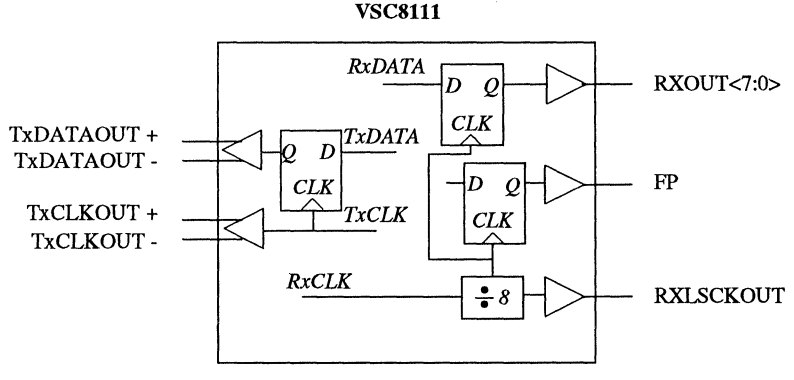
Receive Circuit

High speed Non-Return to Zero (NRZ) serial data at 155Mb/s or 622Mb/s and corresponding clock are received by the RXDATAIN and RXCLKIN inputs respectively. This data is converted to byte-wide parallel data and presented on RXOUT<7:0> pins (Figure 2). A divide-by-8 version of the received high-speed clock (RXLSCKOUT) should be used to synchronize the byte-serial RXOUT<7:0> data with the receive portion of the UNI device.

The VSC8111 supports Loss of Signal (LOS) detection by providing two control inputs; LOSPECL (PECL) and LOSTTL (TTL). Two LOS inputs are provided to simplify interfacing to the chip by providing both PECL and TTL level receivers. The PECL and TTL receive data is XOR'd to generate the internal LOS control. Thus, the active level of the LOS input can be controlled by connecting the unused LOS input to either power or ground. For example, the CDX2622 optics module from Hewlett-Packard signals loss of optical power by asserting their PECL LOS output low. To accommodate this signal, the VSC8111 part should have LOSPECL connected to the CDX2622 and the LOSTTL input should be tied to VDD (3.3V). Upon detecting LOS, the VSC8111 forces the receive data low which is an indication for any downstream equipment that an optical interface failure has occurred.

The receive circuit also includes frame detection and recovery circuitry which detects the SONET/SDH frame, aligns the received serial data on byte boundaries, and initiates a frame pulse on FP coincident with the byte aligned data. The frame recovery is initiated when OOF is held high which must occur at least 4 byte clock cycles before the A1A2 boundary. The OOF input control is a level-sensitive signal, and the VSC8111 will continually perform frame detection and recovery as long as this pin is held high even if 1 or more frames has been detected. Frame detection and recovery occurs when a series of three A1 bytes followed by three A2 bytes has been detected. The parallel output data on RXOUT<7:0> will be byte aligned starting on the third A2 byte. When a frame is detected, a single byte clock period long pulse is generated on FP which is synchronized with the byte-aligned third A2 byte on RXOUT<7:0>. The frame detector sends an FP pulse only if OOF is high or if a frame was detected while OOF was being pulled low.

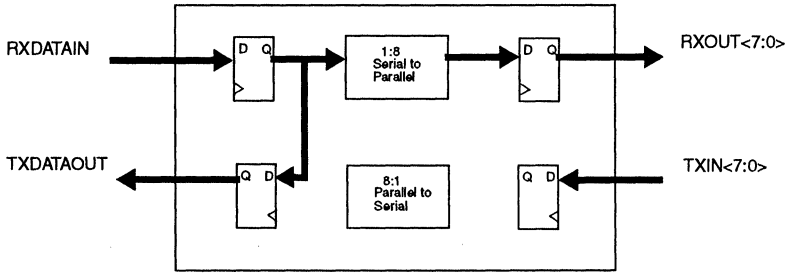
Figure 2: Data and Clock Transmit Block Diagram



Facility Loopback

The Facility Loopback function is controlled by the FACLOOP signal. When the FACLOOP signal is set high, the Facility Loopback mode is activated and the high speed serial receive data (RxDATAIN) is presented at the high speed transmit output (TxDATAOUT). In addition, the high speed receive clock input (RxCLKIN) is selected and presented at the high speed transmit clock output (TxCLKOUT). In Facility Loopback mode the high speed receive data (RxDATAIN) is also converted to parallel data and presented at the low speed receive data output pins (RXOUT<7:0>). The receive clock (RxCLKIN) is also divided down and presented at the low speed clock output (RXLSCKOUT).

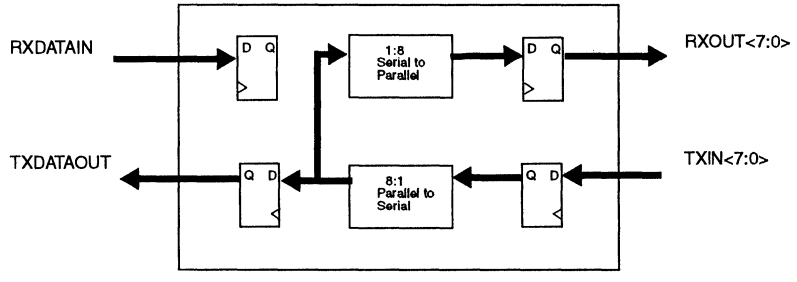
Figure 3: Facility Loopback Data Path



Equipment Loopback

The Equipment Loopback function is controlled by the EQULOOP signal. When the EQULOOP signal is set high, the Equipment Loopback mode is activated and the high speed transmit data generated from the parallel to serial conversion of the low speed data (TXIN<7:0>) is selected and converted back to parallel data on the receiver circuit side and presented at the low speed parallel outputs (RXOUT<7:0>). The internally generated 155Mhz/622Mhz clock is used to generate the low speed receive clock output (RXLSCKOUT). In Equipment Loopback mode the transmit data (TXIN<7:0>) is serialized and presented at the high speed output (TxDATAOUT) along with the high speed transmit clock (TxCLKOUT) which is generated by the on board clock multiplier unit.

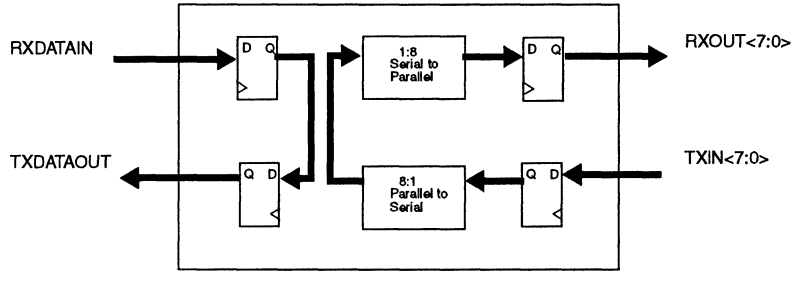
Figure 4: Equipment Loopback Data Path



Split Loopback

Equipment and facility loopback modes can be enabled simultaneously. In this case, high-speed serial data received (RXDATAIN) is mux'd through to the high-speed serial outputs (TXDATAOUT) and the low-speed transmit byte serial stream (TXIN) is mux'd into the low-speed byte serial receive output stream (RXOUT)

Figure 5: Split Loopback Datapath



Loop Timing

Two loop timing modes are supported by the VSC8111. Loop timing mode bypassing the PLL is enabled by asserting the LOOPTIM0 input high. In this mode, the CMU is bypassed with the receive clock (RXCLKIN). In this way, the entire part can be synchronously clocked from a single, external source.

Loop timing mode NOT bypassing the PLL is enabled by asserting the LOOPTIM1 input high. This control pin selects the divide-by-8 version of the receive clock as the reference input to the CMU.

Clock Synthesis

The VSC8111 uses an integrated phase-locked loop (PLL) for clock synthesis of the 622Mb/s transmit data stream. The PLL is comprised of a phase-frequency detector (PFD), an integrating operation amplifier and a voltage controlled oscillator (VCO) configured in classic feedback system. The PFD compares the selected divided down version of the 622MHz VCO (select pins B0-B2 select divide-by ratios of 8, 12, 16 and 32, see

Table 13) and the reference clock. The integrator provides a transfer function between input phase error and output voltage control. The VCO portion of the PLL is a voltage controlled ring-oscillator with a center frequency of 622MHz.

The reactive elements of the integrator are located off-chip and are connected to the feedback loop of the amplifier through the C1P, C2P, C1N and C2N pins. The configuration of these external surface mounted capacitors is shown in Figure 6. Table 1 shows the recommended external capacitor values for the configurable reference frequencies.

Good analog design practices should be applied to the board design for these external components. It is important that well matched capacitors are used and that tightly controlled analog ground and power planes are provided for the PLL portion of the circuitry. The dedicated PLL power (VDDANA) and ground (VSSANA) pins need to have quiet supply planes to minimize jitter generation within the clock synthesis unit.

Figure 6: External Integrator Capacitor

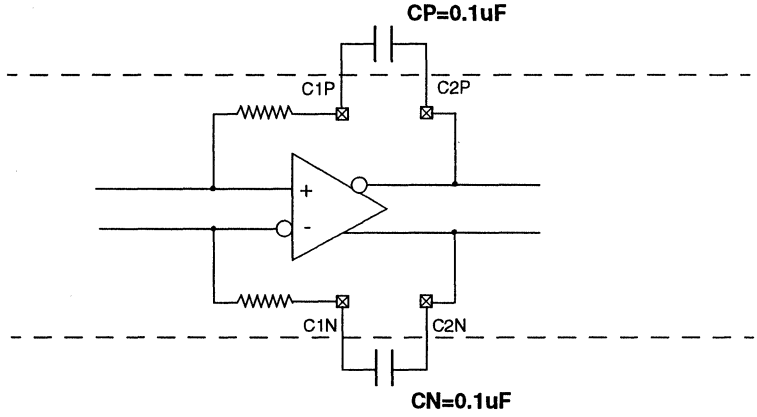


Table 1: Recommended External Capacitor Values

Reference Frequency [MHz]	*Divide Ratio*	*CP (uF)*	*CN (uF)*
19.44	32	0.1	0.1
38.88	16	0.1	0.1
51.84	12	0.1	0.1
77.76	8	0.1	0.1

AC Timing Characteristics

Figure 7: Receive High Speed Data Input Timing Diagram

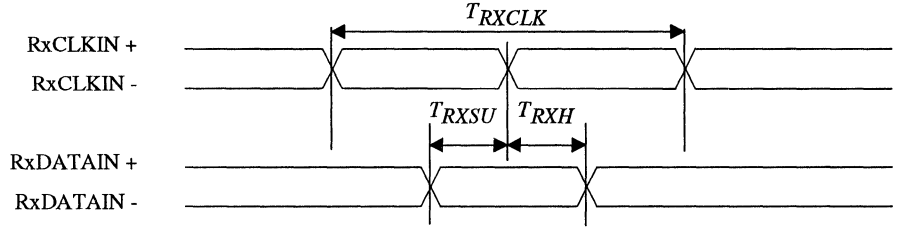


Table 2: Receive High Speed Data Input Timing Table *(STS-12 Operation)*

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{RXCLK}	Receive clock period	-	1.608	-	ns
T_{RXSU}	Serial data setup time with respect to RxCLKIN	500	-	-	ps
T_{RXH}	Serial data hold time with respect to RxCLKIN	500	-	-	ps

Table 3: Receive High Speed Data Input Timing Table *(STS-3 Operation)*

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{RXCLK}	Receive clock period	-	6.43	-	ns
T_{RXSU}	Serial data setup time with respect to RxCLKIN	1.5	-	-	ns
T_{RXH}	Serial data hold time with respect to RxCLKIN	1.5	-	-	ns

Figure 8: Transmit Data Input Timing Diagram

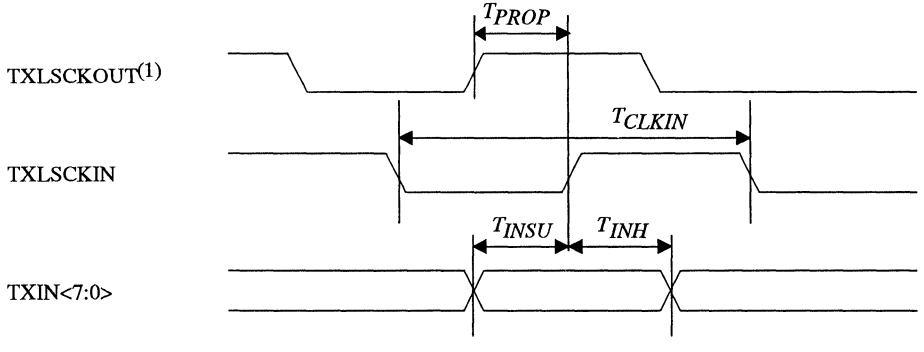


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Table 4: Transmit Data Input Timing Table *(STS-12 Operation)*

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{CLKIN}	Transmit data input byte clock period	-	12.86	-	ns
T_{INSU}	Transmit data setup time with respect to TXLSCKIN	1.0	-	-	ns
T_{INH}	Transmit data hold time with respect to TXLSCKIN	1.0	-	-	ns
T_{PROP}	Maximum allowable propagation delay for connecting TXLSCKOUT to TXLSCKIN	-	-	3	ns

Note: Duty cycle for TXLSCKOUT is 50% +/- 5% worse case

Table 5: Transmit Data Input Timing Table *(STS-3 Operation)*

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{CLKIN}	Transmit data input byte clock period	-	51.44	-	ns
T_{INSU}	Transmit data setup time with respect to TXLSCKIN	1.0	-	-	ns
T_{INH}	Transmit data hold time with respect to TXLSCKIN	1.0	-	-	ns
T_{PROP}	Maximum allowable propagation delay for connecting TXLSCKOUT to TXLSCKIN	-	-	3	ns

Figure 9: Receive Data Output Timing Diagram

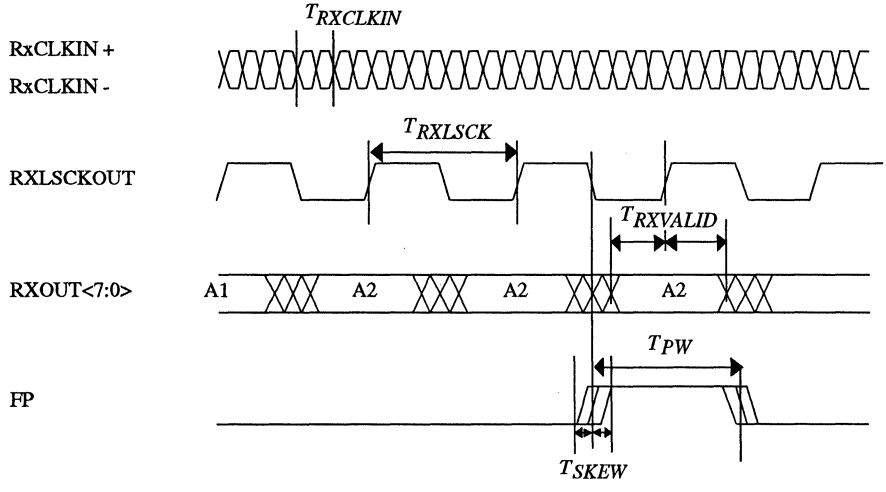


Table 6: Receive Data Output Timing Table *(STS-12 Operation)*

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
$T_{RXCLKIN}$	Receive clock period	-	1.608	-	ns
T_{RXLSCK}	Receive data output byte clock period	-	12.86	-	ns
T_{SKEW}	Range in which the rising edge of FP will appear in relation to the falling edge of RXLSCKOUT	-	-	+/-1.5	ns
$T_{RXVALID}$	Time data on RXOUT<7:0> is valid before and after the rising edge of RXLSCKOUT	4.9	-	-	ns
T_{PW}	Pulse width of frame detection pulse FP	-	12.86	-	ns

Table 7: Receive Data Output Timing Table *(STS-3 Operation)*

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
$T_{RXCLKIN}$	Receive clock period	-	6.43	-	ns
$T_{RXLSCKT}$	Receive data output byte clock period	-	51.44	-	ns
T_{SKEW}	Range in which the rising edge of FP will appear in relation to the falling edge of RXLSCKOUT	-	-	+/-1.5	ns
$T_{RXVALID}$	Time data on RXOUT<7:0> is valid before and after the rising edge of RXLSCKOUT	24	-	-	ns
T_{PW}	Pulse width of frame detection pulse FP	-	51.44	-	ns

Figure 10: Transmit High Speed Data Timing Diagram

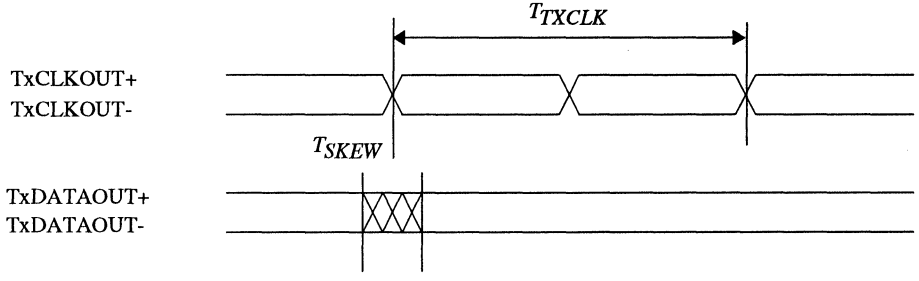


Table 8: Transmit High Speed Data Timing Table *(STS-12 Operation)*

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{TXCLK}	Transmit clock period	-	1.608	-	ns
T_{SKEW}	Skew between the falling edge of TxCLKOUT and valid data on TxDATAOUT	-	-	+/-200	ps

Table 9: Transmit High Speed Data Timing Table *(STS-3 Operation)*

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{TXCLK}	Transmit clock period	-	6.43	-	ns
T_{SKEW}	Skew between the falling edge of TxCLKOUT and valid data on TxDATAOUT	-	-	+/-200	ps

Data Latency

The VSC8111 contains several operating modes, each of which exercise different logic paths through the part. Table 10 bounds the data latency through each path with an associated clock signal.

Table 10: Data Latency

Circuit Mode	*Description*	*Clock Reference*	*Range of Clock cycles STS-12*	*Range of Clock cycles STS-3*
Transmit	Data TXIN<7:0> to MSB at TxDATAOUT	TxCLKOUT	2-11	2-11
Receive	MSB at RxDATAIN to data on RXOUT<7:0>	RxCLKIN	18-25	15-22
Equipment Loopback	Byte data TXIN<7:0> to byte data on RXOUT<7:0>	TxCLKOUT	19-33	17-31
Facilities Loopback	MSB at RxDATAIN to MSB at TxDATAOUT	RxCLKIN	10	10

Preliminary Data Sheet

ATM/SONET/SDH 155/622 Mb/s Transceiver
Mux/Demux with Integrated Clock Generation

Absolute Maximum Ratings[1]

Power Supply Voltage (V_{DD}) Potential to GND ..... -0.5V to +4V
DC Input Voltage (PECL inputs) ..... -0.5V to V_{DD} +0.5V
DC Input Voltage (TTL inputs) ..... -0.5V to 5.5V
DC Output Voltage (TTL Outputs) ..... -0.5V to V_{DD} + 0.5V
Output Current (TTL Outputs) ..... +/-50mA
Output Current (PECL Outputs) ..... +/-50mA
Case Temperature Under Bias ..... -55° to +125°C
Storage Temperature ..... -65°C to +150°C
Maximum Input ESD (Human Body Model) ..... 1500 V

Note: Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Recommended Operating Conditions

Power Supply Voltage (V_{DD}) ..... +3.3V±5 %
Commercial Operating Temperature Range* (T) ..... 0° to 70°C

** Lower limit of specification is ambient temperature and upper limit is case temperature.*

DC Characteristics

Table 11: PECL and TTL Inputs and Outputs

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage (TTL)	2.4	—	—	V	I_{OH} = -1.0 mA
V_{OL}	Output LOW voltage (TTL)	—	—	0.5	V	I_{OL} = +1.0 mA
ΔV_{OUT75}	Serial Output voltage swing (TX+/TX-)	600	—	1300	mV	75Ω to V_{DD} – 2.0 V
ΔV_{OUT50}	Serial Output voltage swing (TX+/TX-)	TBD	—	TBD	mV	50Ω to V_{DD} – 2.0 V
ΔV_{IN}	Serial Input voltage swing (RX+/RX-)	200	—	1600	mV	
V_{IH}	Input HIGH voltage (TTL)	2.0	—	5.5	V	
V_{IL}	Input LOW voltage (TTL)	0	—	0.8	V	—
I_{IH}	Input HIGH current (TTL)	—	50	500	µA	2.0V< V_{IN} < 5.5V, Typical@2.4V
I_{IL}	Input LOW current (TTL)	—	—	-500	µA	-0.5V < V_{IN} < 0.8V

Power Dissipation

Table 12: Power Supply Currents

Parameter	*Description*	*(Max)*	*Units*
I_{DD}	Power supply current from V_{DD}	TBD	mA
P_D	Power dissipation	TBD	W

Clock Multiplier Unit

Table 13: Reference Frequency Selection and Output Frequency Control

STS12	*B2*	*B1*	*B0*	*Reference Frequency [MHz]*	*Output Frequency [MHz]*
1	1	1	0	19.44	622.08
1	0	1	0	38.88	622.08
1	0	0	1	51.84	622.08
1	0	0	0	77.76	622.08
0	1	1	0	19.44	155.52
0	0	1	0	38.88	155.52
0	0	0	1	51.84	155.52
0	0	0	0	77.76	155.52

Table 14: Clock Multiplier Unit Performance

Name	*Description*	*Min*	*Typ*	*Max*	*Units*
RCd	Reference clock duty cycle	40		60	%
RCj	Reference clock jitter (RMS)			5	ps
OCd	Output clock duty cycle	40		60	%
OCj	Output clock jitter (RMS) @ 77.76 MHz ref			TBD	ps
OCj	Output clock jitter (RMS) @ 51.84 MHz ref			TBD	ps
OCj	Output clock jitter (RMS) @ 38.88 MHz ref			TBD	ps
OCj	Output clock jitter (RMS) @ 19.44 MHz ref			TBD	ps
OCfmin	Minimum output frequency			620	MHz
OCfmax	Maximum output frequency			624	MHz

Note: Jitter specification is defined utilizing a 12KHz - 5MHz LP-HP single pole filter.

Package Pin Description

Table 15: Pin Definitions

Signal	Pin	I/O	Level	Pin Description
FACLOOP	1	I	TTL	Facility loopback, active high
VDDD	2		+3.3V	Digital Logic Power Supply
_VSCTE	3	I	TTL	Test pin enable. Tie low for system operation
RESET	4	I	TTL	Resets frame detection, dividers, controls, and tristates TTL outputs; active high
LOOPTIM0	5	I	TTL	Enable loop timing operation; active HIGH
B0	6	I	TTL	Reference clock select, refer to table 12
B1	7	I	TTL	Reference clock select, refer to table 12
B2	8	I	TTL	Reference clock select, refer to table 12
VDDP	9		+3.3V	PECL I/O Power Supply
TXDATAOUT+	10	O	PECL	Transmit output, high speed differential data +
TXDATAOUT-	11	O	PECL	Transmit output, high speed differential data -
VSSD	12		GND	Digital Logic Ground
TxCLKOUT+	13	O	PECL	Transmit high speed clock differential output+
TxCLKOUT-	14	O	PECL	Transmit high speed clock differential output-
VDDP	15		+3.3V	PECL I/O Power Supply
LOSPECL	16	I	PECL	PECL Loss Of Signal control
N/C	17			No Connection
VSSD	18		GND	Digital Logic Ground
RxCLKIN+	19	I	PECL	Receive high speed differential clock input+
RxCLKIN-	20	I	PECL	Receive high speed differential clock input-
VDDD	21		+3.3V	Digital Logic Power Supply
OOF	22	I	TTL	Out Of Frame; Frame detection initiated with high level
LOSTTL	23	I	TTL	TTL Loss Of Signal control
RXDATAIN+	24	I	PECL	Receive high speed differential data input+
RXDATAIN-	25	I	PECL	Receive high speed differential data input-
NC	26			No connection
NC	27			No connection
VDDD	28		+3.3V	Digital Logic Power Supply
NC	29			No connection
_VSCIPNC	30	I	TTL	Test mode input. Tie low for system operation

Preliminary Data Sheet

ATM/SONET/SDH 155/622 Mb/s Transceiver
Mux/Demux with Integrated Clock Generation

Signal	Pin	I/O	Level	Pin Description
VDDT	31		+3.3V	TTL Output Power Supply
_VSCOPNC	32	O	PECL	Test mode output
RX50MCK	33	O	TTL	Constant 51.84Mhz reference clock output, derived from the Clock Multiplier Unit
VSST	34		GND	Ground
RXOUT0	35	O	TTL	Receive output data bit0
RXOUT1	36	O	TTL	Receive output data bit1
VSST	37		GND	TTL Output Ground
RXOUT2	38	O	TTL	Receive output data bit2
RXOUT3	39	O	TTL	Receive output data bit3
VSST	40		GND	TTL Output Ground
RXOUT4	41	O	TTL	Receive output data bit4
RXOUT5	42	O	TTL	Receive output data bit5
VSST	43		GND	TTL Output Ground
RXOUT6	44	O	TTL	Receive output data bit6
RXOUT7	45	O	TTL	Receive output data bit7
VSST	46		GND	TTL Output Ground
RXLSCKOUT	47	O	TTL	Receive byte clock output
FP	48	O	TTL	Frame detection pulse
VDDT	49		+3.3V	TTL Output Power Supply
N/C	50			No Connection
N/C	51			No Connection
N/C	52			No Connection
N/C	53			No Connection
VDDD	54		+3.3V	Digital Logic Power Supply
VSSD	55		GND	Digital Logic Ground
REFCLK	56	I	TTL	Reference clock input, refer to table 13
LOOPTIM1	57	I	TTL	Enable loop timing operation; active HIGH
VDDT	58		+3.3V	+3.3 volt supply (CMU)
VSSANA	59		GND	Analog Ground (CMU)
VSSANA	60		GND	Analog Ground (CMU)
N/C	61			No connection
N/C	62			No connection

Signal	Pin	I/O	Level	Pin Description
N/C	63			No connection
N/C	64			No connection
N/C	65			No connection
N/C	66			No connection
VDDANA	67		+3.3V	Analog Power Supply (CMU)
VDDANA	68		+3.3V	Analog Power Supply (CMU)
VDDANA	69		+3.3V	Analog Power Supply (CMU)
VSSANA	70		GND	Analog Ground (CMU)
VSSANA	71		GND	Analog Ground (CMU)
VSSD	72		GND	Digital Logic Ground
N/C	73			No connection
N/C	74			No connection
VSSD	75		GND	Digital Logic Ground
VDDD	76		+3.3V	Digital Logic Power Supply
C1P	77		Analog	CMU external capacitor pin 1 positive terminal
C2P	78		Analog	CMU external capacitor pin 2 positive terminal
C1N	79		Analog	CMU external capacitor pin 1 negative terminal
C2N	80		Analog	CMU external capacitor pin 2 negative terminal
VDDT	81		+3.3V	TTL Output Power Supply
TXLSCKOUT	82	O	TTL	Transmit byte clock out
TXLSCKIN	83	I	TTL	Transmit byte clock in
VSST	84		GND	TTL Output Ground
TXIN7	85	I	TTL	Transmit input data bit7
TXIN6	86	I	TTL	Transmit input data bit6
VSSD	87		GND	Digital Logic Ground
TXIN5	88	I	TTL	Transmit input data bit5
TXIN4	89	I	TTL	Transmit input data bit4
N/C	90			No connection
TXIN3	91	I	TTL	Transmit input data bit3
TXIN2	92	I	TTL	Transmit input data bit2
VSSD	93		GND	Digital Logic Ground
TXIN1	94	I	TTL	Transmit input data bit1
TXIN0	95	I	TTL	Transmit input data bit0

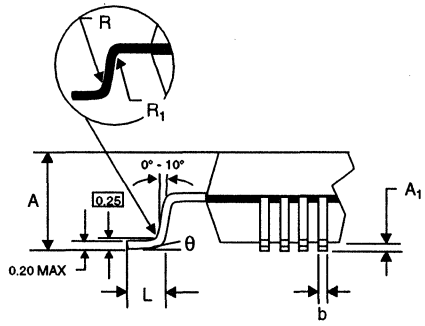
Preliminary Data Sheet

ATM/SONET/SDH 155/622 Mb/s Transceiver
Mux/Demux with Integrated Clock Generation

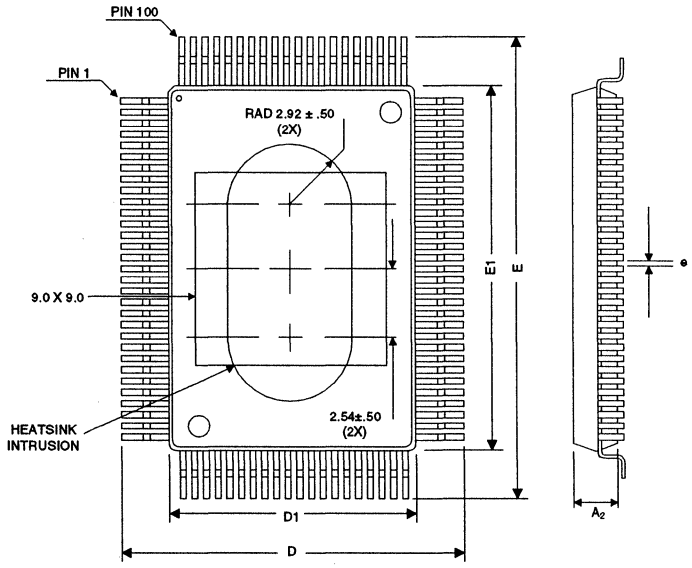
Signal	Pin	I/O	Level	Pin Description
N/C	96			No connection
STS12	97	I	TTL	155Mb/s or 622Mb/s mode select, refer to table 13
PLLM	98	O	PECL	PLL test output, leave unconnected in system operation
VDDT	99		+3.3V	TTL Output Power Supply
EQULOOP	100	I	TTL	Equipment loopback, active high

Package Information

100 PQFP Package Drawings



Dims.	mm	Tolerance
A	3.40	MAX
A1	0.60	MAX
A2	2.7	±.10
D	17.20	±.40
D1	14.00	±.10
E	23.20	±.40
E1	20.00	±.10
L	0.80	±.2
e	0.65	NOM
b	0.30	±.10
θ	0-10°	
R	.25	NOM
R1	.2	NOM



NOTES:
(1) Drawings not to scale.
(2) Two styles of exposed heat spreaders may be used; square or oval.
(3) All units in millimeters

The VSC8111 is manufactured in a 100PQFP package which is supplied by two different vendors. The critical dimensions in the drawing represent the superset of dimensions for both packages. The significant difference between the two packages is in the shape and size of the heatspreader which needs to be considered when attaching a heatsink.

Package Thermal Characteristics

The VSC8111 is packaged in a thermally enhanced 100PQFP with an embedded heat sink. The heat sink surface configurations are shown in the package drawings. With natural convection, the case to air thermal resistance is estimated to be 27.5°C/W. The air flow versus thermal resistance relationship is shown in Table 16.

Table 16: Theta Case to Ambient versus Air Velocity

Air Velocity (LFPM)	*Case to air thermal resistance °C/W*
0	27.5
100	23.1
200	19.8
400	17.6
600	16

ATM/SONET/SDH 155/622 Mb/s Transceiver
Mux/Demux with Integrated Clock Generation

Preliminary Data Sheet

Ordering Information

The order number for this product are:

Part Number	Device Type
VSC8111QB:	155Mb/s-622Mb/s Mux/Dmux with CMU in 100 Pin PQFP Commercial temperature, 0°C ambient to 70° case
VSC8111QB1	155Mb/s-622Mb/s Mux/Dmux with CMU in 100Pin PQFP 0° ambient to 110° case

Notice

This document contains information on products that are in the preproduction phase of development. The information contained in this document is based on test results and initial product characterization. Characteristic data and other specifications are subject to change without notice. Therefore, the reader is cautioned to confirm that this datasheet is current prior to placing orders.

Warning

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Application Notes

Interconnecting the Byte Clocks (TXLSCKOUT and TXLSCKIN)

The byte clock (TXLSCKOUT and TXLSCKIN) on the VSC8111 has been brought off-chip to allow as much flexibility in system-level clocking schemes as possible. Since the byte clock (TXLSCKOUT) clocks both the VSC8111 and the UNI devices, it is important to pay close attention to the routing of this signal. The UNI device in general is a CMOS part which can have very wide spreads in timing (1-11ns clock in to parallel data out for the PM5355), which utilizes most of the 12.86ns period (at 78Mhz), leaving little for the trace delays and set-up times required to interconnect the 2 devices. The recommended way of routing this clock when used in a 622Mhz mode is to daisy chain it to the UNI device pin and then route it back to the VSC8111 along with the byte data. This eliminates the 1-way trace delay that would otherwise be encountered between the data and clock and thus leaves 1.86ns for the VSC8111 setup time and for variations in trace delays and rise times between clock and data. The trace delay must be kept under 2ns (allowing an additional 1ns for variations in rise times and skews) to ensure proper muxing of parallel input data into the VSC8111; reference Table 4and 5.

AC Coupling and Terminating High-speed I/Os

The high speed signals on the VSC8111 (RXDATAIN, RXCLKIN, TXDATAOUT, TXCLKOUT) use 3.3V PECL levels which are essentially ECL levels shifted positive by 3.3 volts. The PECL I/Os are referenced to the V_{DD} supply and are terminated to ground. Since most optics modules use either ECL or 5.0V PECL levels, the high speed ports need to be ac coupled to overcome the difference in dc levels.

The PECL receiver inputs of the VSC8111 are internally biased at VDD/2. Therefore, AC-coupling to the VSC8111 inputs is accomplished by providing the pull-down resistor for the open-source PECL output and an AC-coupling capacitor used to eliminate the DC component of the output signal. This capacitor allows the PECL receivers of the VSC8111 to self-bias via its internal resistor divider network (see Figure 12). The PECL output drivers are capable of sourcing current but not sinking it. To establish a LOW output level, a pull-down resistor, traditionally connected to VDD-2.0V, is needed when the output FET is turned off. Since VDD-2.0V is usually not present in the system, the resistor should be terminated to ground for convenience. The VSC8111 output drivers should be AC-coupled to the 5.0V PECL inputs of the optics module. Appropriate biasing techniques for setting the DC-level of these inputs should be employed.

The dc biasing and 50 ohm termination requirements can easily be integrated together using a thevenin equivalent circuit as shown in Figure 11. The figure shows the appropriate termination values when interfacing 3.3V PECL to 5.0V PECL. This network provides the equivalent 50 ohm termination for the high speed I/Os and also provides the required dc biasing for the receivers of the optics module. Table 17 contains recommended values for each of the components.

The TTL inputs of the VSC8111 are 3.3V TTL which can accept 5.0V TTL levels within a giving set of tolerances (see Table 11). These input structures shown in Figure 12 use a current limiter to avoid overdriving the input FETs.

Layout of the 622 Signals

The routing of the 622 signals should be done using good high speed design practices. This would include using controlled impedance lines and keeping the distance between components to an absolute minimum. In addition, stubs should be kept at a minimum as well as any routing discontinuities. This will help minimize reflections and ringing on the high speed lines and insure the maximum eye opening. In addition the output pull down resistor should be placed as close to the VSC8111 pin as possible while the AC-coupling capacitor and the biasing resistors should be placed as close as possible to the optics input pin. The same is true on the receive circuit side. Using small outline components and minimum pad sizes also helps in reducing discontinuities.

Ground Planes

The ground plane for the components used in the 622 interface should be continuous and not sectioned in an attempt to provide isolation to various components. Sectioning of the ground planes tends to interfere with the ground return currents on the signal lines as well as in general, the smaller the ground planes the less effective they are in reducing ground bounce noise and the more difficult to decouple etc. Sectioning of the positive supplies can provide some isolation benefits.

Figure 11: AC Coupled High Speed I/O

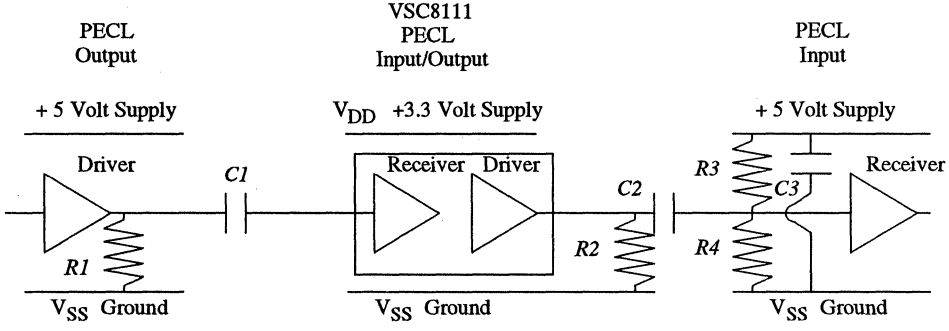
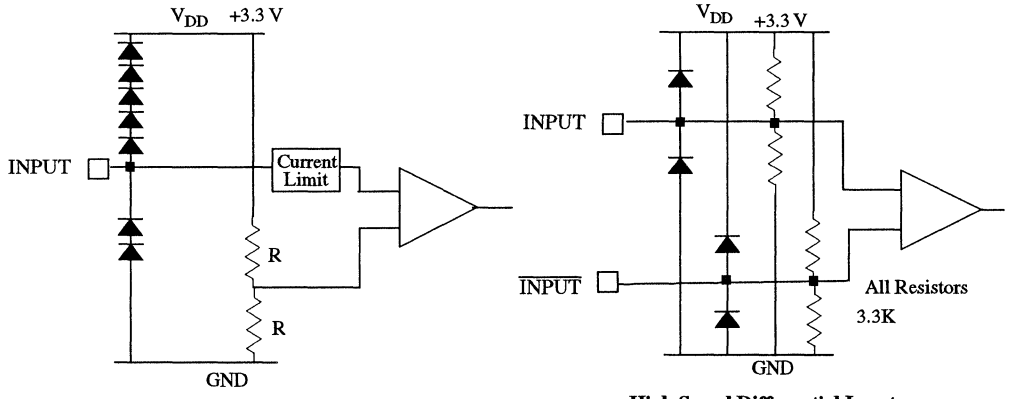


Table 17: AC Coupling Component Values

Component	*Value*	*Tolerance*
R1	182 ohms	1%
R2	182 ohms	1%
R3	68 ohms	1%
R4	190 ohms	1%
C1, C2, C3	.01uf High Frequency	

Figure 12: Input Structures



REFCLK and TTL Inputs

High Speed Differential Input
(RXDATAIN+/RXDATAIN-)
(RXCLKIN+/RXCLKIN-)

Advanced Product Information

SONET/SDH 622 Mb/s 4-bit Mux Demux with Integrated Clock Generation

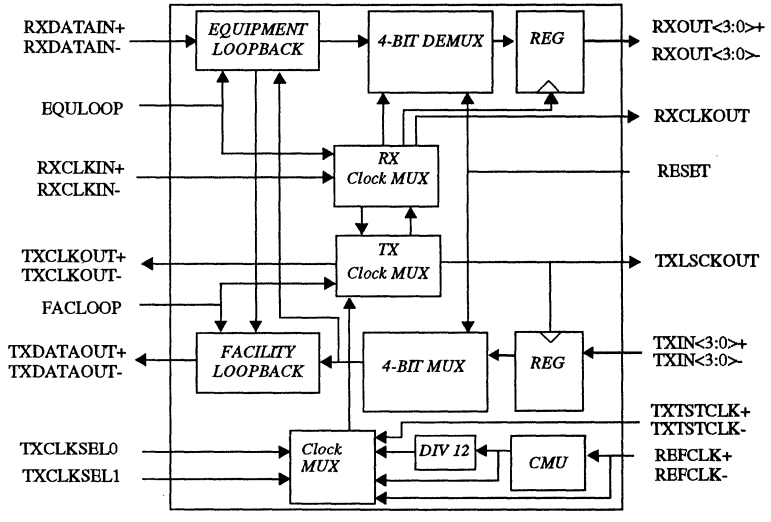
Features

- Operates as a Bit-serial STS-3/STM-1 to STS-12/STM-4 Mux/Dmux
- On Chip Clock Generation of the 622.08 Mhz High Speed Clock, 155.52 Mhz Reference Clock
- Fully Differential VECL Clock and Data I/O
- Integrated PLL for Clock Generation - No External Components
- Provides Equipment and Facilities Loopback
- Low Power - 1.5 Watts Maximum
- Dual Supply Operation- +2, +5 Volts
- 100 PQFP Package
- Extended Temperature Range - 0 °C - 110 °C case

General Description

The VSC8112 is a SONET/SDH rate compatible 4-bit STS-3/STM-1 to STS-12/STM-4 Mux/Dmux with integrated high speed clock generation. The high speed clock is generated using an on-chip PLL with a 155.52 Mhz reference clock. To facilitate testing, the part has a test clock input which can be used in place of the internally generated 622 Mhz clock. In addition, the device provides both facility and equipment loopback modes. The part is packaged in a 100PQFP with integrated heat spreader for optimum thermal performance and reduced cost. Given the worst case maximum power consumption of 1.5 Watts, extended temperature range of +110 °C case, and no air flow, a corresponding +70 °C ambient temperature can be achieved without a heat sink.

VSC8112 Block Diagram



Functional Description

The VSC8112 converts 4 parallel bits at 155.52Mhz to a serial bit stream at 622.08Mb/s. The transmit section provides a Facility Loopback function which loops the received high speed data and clock directly to the transmit outputs. A clock multiplier unit is integrated into the transmit circuit to generate the high speed clock for the serial output data stream from an input reference frequency of 155.52Mhz. The block diagram on page 1 shows the major functional blocks associated with the VSC8112.

The receive circuit provides the demux function, converting a 622Mb/s serial bit stream to a 4 bit parallel output at 155.52Mhz. The receive section provides an Equipment Loopback function which will loop the high speed transmit data and clock back through the demultiplexer to the 4 bit parallel outputs.

Transmit Circuit

Half-byte-wide data is presented to TXIN<3:0> and is clocked into the part on the rising edge of TXLSCKOUT. The data is serialized (MSB leading) and presented at the TXOUT+/- pins. The Clock Multiplier Unit (CMU) generates the high speed clock required for serialization and transmission. The high speed clock accompanying the transmitted data appears on the TXCLKOUT+/- pins. Two select lines, TXCLKSEL0 and TXCLKSEL1, control the selection of the TXCLKOUT clock. One can chose from the PLL output (622.02Mhz), the PLL output divided by 12 (51.84Mhz), a test clock input (TXTSTCLKIN) or the reference clock, which is 155.52Mhz. Please refer to table 9 for the definition of these 2 select lines. The Facility Loopback mode is set by FACLOOP and is active low.

Receive Circuit

622Mb/s serial data and 622Mhz clock are input to RXIN+/- and RXCLKIN+/- pins respectively. This data is converted to half-byte-wide parallel data and presented on the RXOUT<3:0> pins. The received high speed clock is divided by 4 and presented on the RXCLKOUT pin. The Equipment Loopback mode is set by EQULOOP and is active low.

AC Timing Characteristics

Figure 1: Receive High Speed Data Input Timing Diagram

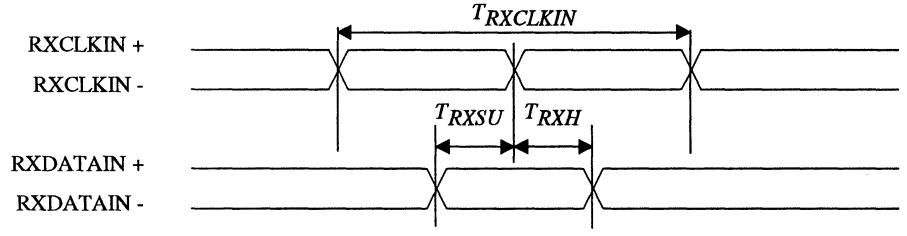


Table 1: Receive High Speed Data Input Timing Table

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
$T_{RXCLKIN}$	Receive clock period	-	1.608	-	ns
T_{RXSU}	Serial data setup time with respect to RXCLKIN	300	-	-	ps
T_{RXH}	Serial data hold time with respect to RXCLKIN	600	-	-	ps

Figure 2: Transmit Data Input Timing Diagram

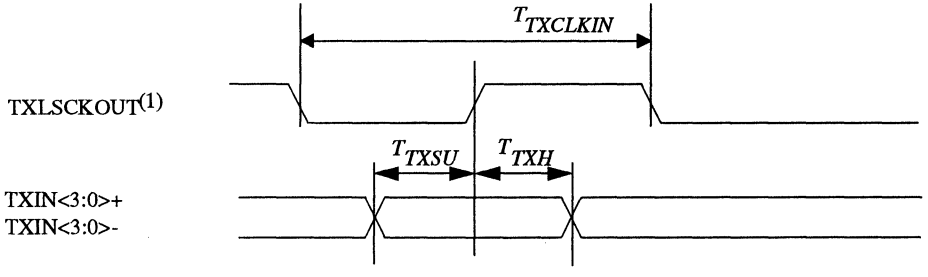


Table 2: Transmit Data Input Timing Table

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
$T_{TXCLKIN}$	Transmit data input byte clock period	-	12.86	-	ns
T_{TXSU}	Transmit data setup time with respect to TXLSCKOUT	2150	-	-	ps
T_{TXH}	Transmit data hold time with respect to TXLSCKOUT	-750	-	-	ps

Note: Duty cycle for TXLSCKOUT is 50% +/- 5% worse case

Figure 3: Receive Data Output Timing Diagram

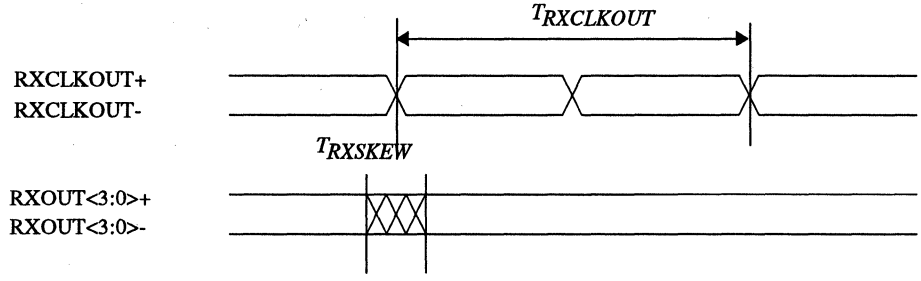


Table 3: Receive Data Output Timing Table

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
$T_{RXCLKOUT}$	Receive clock period	-	1.608	-	ns
T_{RXSKEW}	Skew between the falling edge of RXCLKOUT and valid data on RXOUT<3:0>	-	-	TBD	ps

Figure 4: Transmit Data Output Timing Diagram

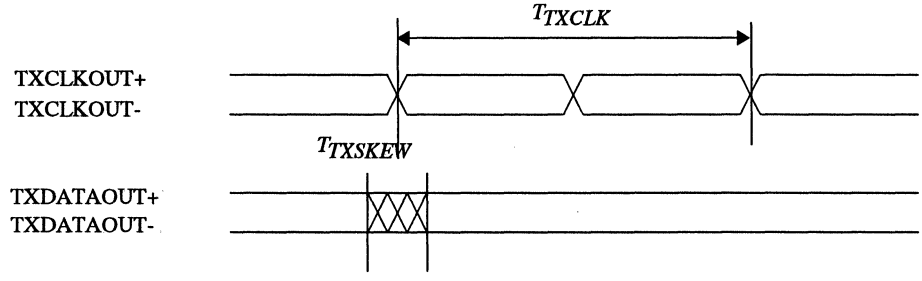


Table 4: Transmit Data Output Timing Table

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{TXCLK}	Transmit clock period	-	1.608	-	ns
T_{TXSKEW}	Skew between the falling edge of TXCLKOUT and valid data on TXDATAOUT	-	-	TBD	ps

DC Characteristics

Table 5: VECL Inputs and Outputs

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	V_{MM}-1020	-	V_{MM}-850	mV	50 ohm to gnd
V_{OL}	Output LOW voltage	V_{MM}-2000	-	V_{MM}-1620	mV	50 ohm to gnd
V_{IH}	Input HIGH voltage	V_{MM}-1100	-	V_{MM}-700	mV	Guaranteed HIGH signal for all inputs
V_{IL}	Input LOW voltage	V_{MM}-2000	-	V_{MM}-1540	mV	Guaranteed LOW signal for all inputs
I_{IH}	Input HIGH current	-	-	200	uA	$V_{IN}=V_{IH}$ (max)
I_{IL}	Input LOW current	-50	-	-	uA	$V_{IN}=V_{IL}$ (min)
V_{DIFF}	Input Voltage Differential	200	-	-	mV	
V_{CM}	Common Mode Voltage	V_{MM}-1.5	-	V_{MM}-0.5	V	

Note: Differential VECL output pins must be terminated identically.

Table 6: TTL Inputs and Outputs

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	2.4	-	-	mV	$V_{IN}=V_{IH}$ (max) or V_{IL} (min) I_{OH}=-2.4mA
V_{OL}	Output LOW voltage	0	-	0.5	mV	$V_{IN}=V_{IH}$ (max) or V_{IL} (min) I_{OL}=8mA
V_{IH}	Input HIGH voltage	2.0	-	V_{TTL}+1.0	mV	Guaranteed HIGH signal for all inputs
V_{IL}	Input LOW voltage	0	-	0.8	mV	Guaranteed LOW signal for all inputs
I_{IH}	Input HIGH current	-	-	50	uA	$V_{IN}=V_{IH}$ (max)
I_{IL}	Input LOW current	-500	-	-	uA	$V_{IN}=V_{IL}$ (min)
I_{OZH}	3-State Output OFF current HIGH	-	-	200	uA	V_{OUT}=2.4V
I_{OZL}	3-State Output OFF current LOW	-200	-	-	uA	V_{OUT}=0.5V

Power Dissipation

Table 7: Power Supply Currents

Parameter	Description	(Max)	Units
I_{MM}	Power supply current from V_{MM}	286	mA
I_{TTL}	Power supply current from V_{TTL}	170	mA
P_D	Power dissipation	1.50	W

Note: Specified with outputs open circuit. The combined maximum currents (I_{MM}, I_{TTL}) for any part will not exceed 1.50 Watts.

Clock Multiplier Unit

Table 8: TX Clock Selection

TXCLKSEL0	TXCLKSEL1	TXCLKOUT Frequency [MHz]	TXLSCKOUT Frequency [MHz]
0	0	622.08	155.52
0	1	TXTSTCLK	TXTSTCLK/4
1	0	REFCLK	REFCLK/4
1	1	51.84	12.96

Table 9: Clock Multiplier Unit Performance

Name	Description	Min	Typ	Max	Units
RCd	Reference clock duty cycle	40		60	%
RCj	Reference clock jitter (RMS)			5	ps
OCd	Output clock duty cycle	40		60	%
OCj	Output clock jitter (RMS) @ 155.52 MHz ref			10	ps
OCfmin	Minimum output frequency			620	MHz
OCfmax	Maximum output frequency			624	MHz

Note: Jitter specification is defined utilizing a 12KHz - 5MHz LP-HP single pole filter.

Data Latency

The VSC8112 contains several operating modes, each of which exercise different logic paths through the part. Table 5 bounds the data latency through each path with an associated clock signal.

Table 10: Data Latency

Circuit Mode	*Description*	*Clock Reference*	*Range of Clock cycles*
Transmit	Data TXIN<3:0> to MSB at TXDATAOUT	TXCLKOUT	TBD
Receive	MSB at RXDATAIN to data on RXOUT<3:0>	RXCLKIN	TBD
Equipment Loopback	Byte data TXIN<3:0> to byte data on RXOUT<3:0>	TXCLKOUT	TBD
Facilities Loopback	MSB at RXDATAIN to MSB at TXDATAOUT	RXCLKIN	TBD

Absolute Maximum Ratings[1]

Power Supply Voltage (V_{MM}) Potential to GND ..... -0.5V to +2.5V
Power Supply Voltage (V_{TTL}) Potential to GND ..... -0.5V to +5.5V
TTL Input Voltage Applied ..... -0.5V to V_{TTL} + 1.0V
VECL Input Voltage Applied ..... -0.5V to V_{MM} + 1.0V
Output Current (I_{OUT}) 50mA
Case Temperature Under Bias (T_C) ..... -55° to + 125°C
Storage Temperature (T_{STG}) ..... -65° to + 150°C

Note: Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Recommended Operating Conditions

Power Supply Voltage (V_{MM}) ..... +2.0V±5 %
Power Supply Voltage (V_{TTL}) ..... +5.0V±5 %
Extended Operating Temperature Range* (T) ..... 0° to 110°C

** Lower limit of specification is ambient temperature and upper limit is case temperature.*

ESD Ratings

Proper ESD procedures should be used when handling this product. The VSC8112 is rated to the following ESD voltages based on the human body model:

1. All pins are rated at or above 1500V.

Package Pin Description

Table 11: Pin Definitions

Signal	Pin	I/O	Level	Pin Description
NC	1			No connection
VMM	2		+2.0V	+2 volt supply
_VSCTE	3	I	TTL	Test pin enable. Tie low for system operation
RESET	4	I	TTL	Resets 1:4 Mux and 4:1 Dmux, and tristates TTL outputs; active high
NC	5			No connection
NC	6			No connection
NC	7			No connection
NC	8			No connection
VMM	9		+2.0V	+2 volt supply
TXDATAOUT+	10	O	VECL	Transmit output, high speed differential data +
TXDATAOUT-	11	O	VECL	Transmit output, high speed differential data -
VCC	12		GND	Ground
TXCLKOUT+	13	O	VECL	Transmit high speed clock differential output+
TXCLKOUT-	14	O	VECL	Transmit high speed clock differential output-
VMM	15		+2.0V	+2 volt supply
NC	16			No connection
NC	17			No connection
VCC	18		GND	Ground
RXDATAIN+	19	I	VECL	Receive high speed differential data input+
RXDATAIN-	20	I	VECL	Receive high speed differential data input-
VMM	21		+2.0V	+2 volt supply
NC	22			No connection
NC	23			No connection
RXCLKIN+	24	I	VECL	Receive high speed differential clock input+
RXCLKIN-	25	I	VECL	Receive high speed differential clock input-
NC	26			No connection
NC	27			No connection
VMM	28		+2.0V	+2 volt supply
NC	29			No connection
_VSCIPNC	30	I	TTL	Test mode input. Tie low for system operation
VTTL	31		+5.0V	+5 volt supply
_VSCOPNC	32	O	VECL	Test mode output

Signal	Pin	I/O	Level	Pin Description
NC	33			No connection
VMM	34		+2.0V	Ground
RXOUT0+	35	O	VECL	Receive output data bit0+
RXOUT0-	36	O	VECL	Receive output data bit0-
VCC	37		GND	Ground
RXOUT1+	38	O	VECL	Receive output data bit1+
RXOUT1-	39	O	VECL	Receive output data bit1-
VMM	40		+2.0V	+2 volt supply
RXOUT2+	41	O	VECL	Receive output data bit2+
RXOUT2-	42	O	VECL	Receive output data bit2-
VCC	43		GND	Ground
RXOUT3+	44	O	VECL	Receive output data bit3+
RXOUT3-	45	O	VECL	Receive output data bit3-
VMM	46		+2.0V	+2 volt supply
RXCLKOUT+	47	O	VECL	Receive output clock+
RXCLKOUT-	48	O	VECL	Receive output clock-
VTTL	49		+5.0V	+5 volt supply
NC	50			No connection
NC	51			No connection
NC	52			No connection
NC	53			No connection
VMM	54		+2V	+2 volt supply
VCC	55		GND	Ground
REFCLK+	56	I	VECL	Differential 155.52 Mhz reference clock input+
REFCLK-	57	I	VECL	Differential 155.52 Mhz reference clock input-
VTTL	58		+5.0V	+5 volt supply
VCC	59		GND	Ground
VCC	60		GND	Ground
NC	61			No connection
NC	62			No connection
NC	63			No connection
NC	64			No connection
NC	65			No connection
NC	66			No connection

Signal	Pin	I/O	Level	Pin Description
VTTL	67		+5.0V	+5 volt supply
VTTL	68		+5.0V	+5 volt supply
VTTL	69		+5.0V	+5 volt supply
VCC	70		GND	Ground
VCC	71		GND	Ground
VCC	72		GND	Ground
TXTSTCLK+	73	I	VECL	Test clock input+
TXTSTCLK-	74	I	VECL	Test clock input-
VCC	75		GND	Ground
VMM	76		+2.0V	+2 volt supply
NC	77			No connection
NC	78			No connection
TXCLKSEL0	79	I	TTL	Test clock select line 0
TXCLKSEL1	80	I	TTL	Test clock select line 1
VTTL	81		+5.0V	+5 volt supply
TXLSCKOUT+	82	O	VECL	Transmit half-byte clock out+
TXLSCKOUT-	83	O	VECL	Transmit half-byte clock out-
VMM	84		+2.0V	+2 volt supply
FACLOOP	85	I	TTL	Facility loopback, active low
EQULOOP	86	I	TTL	Equipment loopback, active low
VCC	87		GND	Ground
TXIN3+	88	I	VECL	Transmit input data bit3+
TXIN3-	89	I	VECL	Transmit input data bit3-
VMM	90		+2.0V	+2 volt supply
TXIN2+	91	I	VECL	Transmit input data bit2+
TXIN2-	92	I	VECL	Transmit input data bit2-
VCC	93		GND	Ground
TXIN1+	94	I	VECL	Transmit input data bit1+
TXIN1-	95	I	VECL	Transmit input data bit1-
VMM	96		+2.0V	+2 volt supply
TXIN0+	97	I	VECL	Transmit input data bit0+
TXIN0-	98	I	VECL	Transmit input data bit0-
VTTL	99		+5.0V	+5 volt supply
NC	100			No connection

The VSC8112 is manufactured in a 100PQFP package which is supplied by two different vendors. The critical dimensions in the drawing represent the superset of dimensions for both packages. The significant difference between the two packages is in the shape and size of the heatspreader which needs to be considered when attaching a heatsink.

Package Thermal Characteristics

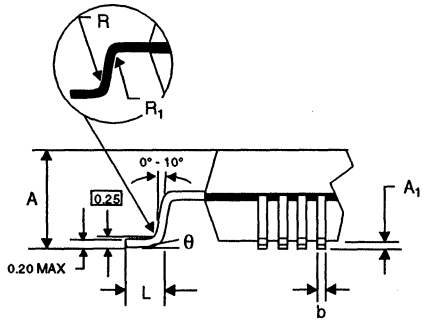
The VSC8112 is packaged in a thermally enhanced 100PQFP with an embedded heat sink. The heat sink surface configurations are shown in the package drawings. The air flow versus thermal resistance relationship is shown in table 12. With natural convection, the case to air thermal resistance is estimated to be 27.5°C/W. Therefore, at 70°C ambient with no air flow, no heat sink is required because of the extended operating temperature range of 0°C to 110°C.

Table 12: Theta Case to Ambient versus Air Velocity

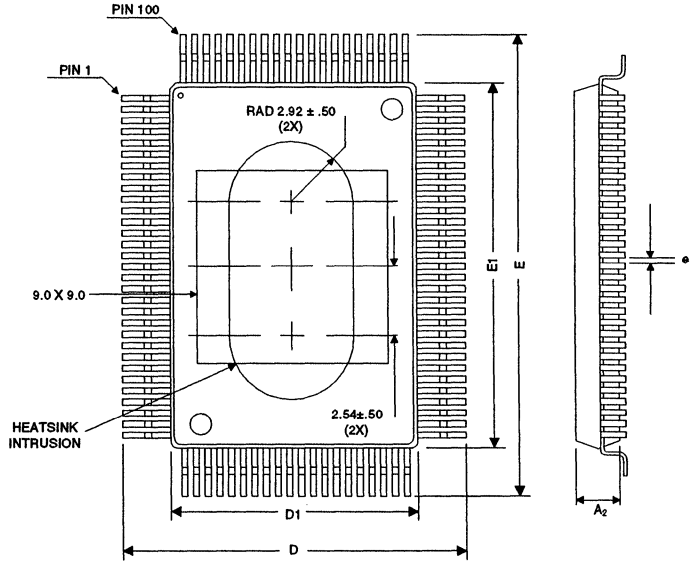
Air Velocity (LFPM)	*Case to air thermal resistance °C/W*
0	27.5
100	23.1
200	19.8
400	17.6
600	16

Package Information

100 PQFP Package Drawings



Dims.	mm	Tolerance
A	3.40	MAX
A1	0.60	MAX
A2	2.7	±.10
D	17.20	±.40
D1	14.00	±.10
E	23.20	±.40
E1	20.00	±.10
L	0.80	±.2
e	0.65	NOM
b	0.30	±.10
θ	0-10°	
R	.25	NOM
R1	.2	NOM



NOTES:
(1) Drawings not to scale.
(2) Two styles of exposed heat spreaders may be used; square or oval.
(3) All units in millimeters

Advanced Product Information

SONET/SDH 622 Mb/s 4-bit Mux Demux with Integrated Clock Generation

Ordering Information

The order number for this product are:

Part Number	Device Type
VSC8112QB1:	622Mb/s 4-bit Mux/Dmux with CMU in 100 Pin PQFP Extended temperature

Notice

This document contains information about a new product during its fabrication or early sampling phase of development. The information in this document is based on design targets, simulation results or early prototype test results. Characteristic data and other specifications are subject to change without notice. Therefore the reader is cautioned to confirm that this datasheet is current prior to design or order placement.

Warning

Vitesse Semiconductor Corporation's product are not intended for use in life support appliances, devices or systems. Use of a Vitesse product in such applications without the written consent is prohibited.

Application Notes

2 Volt Supply Generation From 5 Volts

The 2 volt supply can be generated from the 5 volt supply using a linear regulator. There are many manufacturers who supply linear regulators. Refer to Table 13 for examples.

Table 13: Recommended 2 Volt Voltage Regulator

Recommended Regulator	*Maximum Supply Current*	*Manufacturer's Information*
REG1117	800mA	Burr Brown 800-548-6132
LT117A	800mA	Linear Technology

AC Coupling and Terminating VECL Differential I/Os

All the clock and data signals on the VSC8112 use VECL levels which are essentially ECL levels shifted positive by 2 volts. The VECL I/Os are referenced to the V_{MM} supply and are terminated to ground. Since most optics modules use either ECL or PECL levels, the high speed ports need to be ac coupled to overcome the difference in dc levels. In addition, the inputs must be dc biased to hold the inputs at their threshold value with no signal applied. The dc biasing and 50 ohm termination requirements can easily be integrated together using a thevenin equivalent circuit as shown in Figure 5. The figure shows the appropriate termination values when interfacing PECL to VECL and VECL to PECL. This network provides the equivalent 50 ohm termination for the high speed I/Os and also provides the required dc biasing for both the drivers and receivers. Table 14 contains recommended values for each of the components.

Figure 5: AC Coupled High Speed I/O

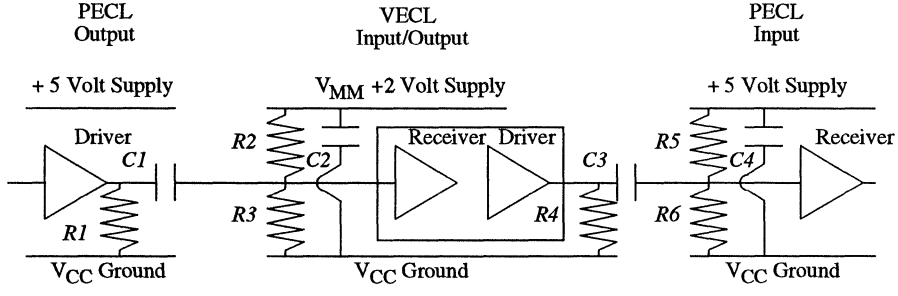


Table 14: AC Coupling Component Values

Component	*Value*	*Tolerance*
R1	270 ohms	1%
R2	147 ohms	1%
R3	76 ohms	1%
R4	50 - 100 ohms	1%
R5	68 ohms	1%
R6	190 ohms	1%
C1, C2, C3, C4	.01uf High Frequency	

Data Sheet

200 Mb/s 64 x 64 Crosspoint Switch

Features

- 200 Mb/s Operation
- Duty-cycle Distortion: ≤ 10%
- Clocked or Flow-through Operation
- ECL 100K Compatible I/O
- ≤ 1500 ps Output to Output Skew (clocked mode)
- 25Ω Output Drive
- Power Dissipation: 9.4 Watts (Typ.)
- Single Power Supply: -2 V ± 5%
- Commercial (0° to +70° C) or Industrial (-40° to +85° C) Temperature Ranges
- Full Diagnostic Monitors
- Cascadable for Larger System Requirements
- Package: 344-pin Ceramic LDCC

General Description

The VSC864A-2 is a 64 x 64 crosspoint switch intended for high speed (up to 200 Mb/s) digital data communications applications. This product has 64 data inputs and 64 data outputs. Any input can be multiplexed to any, some, or all outputs. High speed digital data up to 200 Mb/s can be switched with less than 20% pulse width distortion. In broadcast mode, any two outputs will exhibit less than 1500 ps of skew. All interfaces are fully compatible with ECL F100K logic levels. The VSC864A-2 requires only a single -2 V power supply.

A separate Q bus is provided to allow observation of individual internal multiplexer address latches. Since the VSC864A-2 outputs are capable of driving 25Ω double-terminated buses with cutoff drivers, the device can be cascaded to form larger crosspoint switches. The VSC864A-2 Crosspoint Switch can be operated in either flow-through or synchronous mode by use of internal input and output data registers. In flow-through mode the data propagation delay is less than 5.8 ns.

The individual address registers in the VSC864A-2 are double buffered. A local strobe signal is used to load an individual address for each output pin. A global strobe is used to simultaneously activate all 64 destination addresses.

This product is ideal for high speed digital applications including data distribution for telecommunications, computer network and multiprocessor switching, and test equipment. In a telecommunications SONET application, for example, the VSC864A-2 can be used as an STS-3 protection switch, or in the fabric of a large switching system.

The VSC864A-2 is packaged in a 344 pin ceramic LDCC package and typically dissipates less than 10 W. This product is fabricated using Vitesse's simple, high yielding, E/D GaAs MESFET process which achieves high speed coupled with low power dissipation.

Functional Description

The VSC864A-2 may be used to connect any one of 64 inputs to any combination of 64 output channels, according to a user defined bit pattern stored in each channel's control latch.

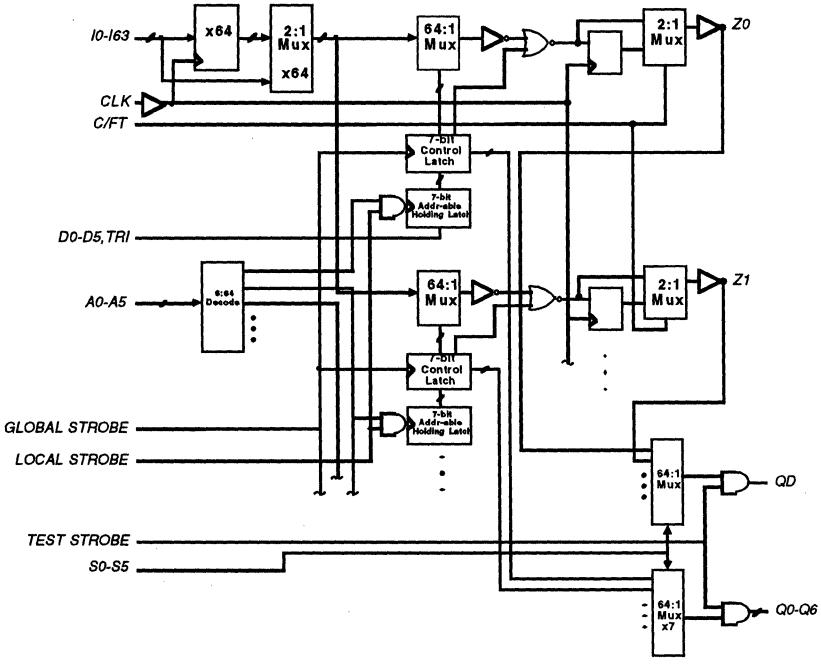
During normal operation, signals flow from inputs (I0 - I63) to output channels (Z0 - Z63) through sixty-four, 64:1 multiplexers. The traffic pattern is controllable by data previously stored in sixty-four 7-bit control registers with each register corresponding to an output channel. The first 6 least significant bits in each control register are reserved for designating the MUX input which will be connected to its corresponding output, the most significant bit is used to tri-state this output if desired. The 6 LSBs are a binary numerical representation of the input channel selected (i.e.., 000000 corresponds to I0, 000001 corresponds to I1, etc.).

The Write mode is used to alter any one or all signal paths. During Write mode, inputs A0 - A5 select which output channel's control register will be altered (also by a binary numerical representation). Inputs D0- D5 describe the new input signal to be selected for that channel. When a high pulse is applied to LOCAL STROBE, D0- D5 and the TRI bit is transferred into a holding latch. After some or all control registers are programmed, a high pulse is applied to GLOBAL STROBE to transfer the information from the holding latch into all the control registers. In this way the entire crosspoint switch can be reconfigured simultaneously.

The Read mode is a diagnostic feature used to examine the data stored in any one control register and its corresponding 64:1 multiplexer output. The control register to be examined is selected by inputs S0- S5 (by a binary numerical representation). When a high pulse is applied to the TEST STROBE, the contents of the selected control register will be displayed at the Q0- Q6 outputs and the corresponding 64:1 mux output will appear at the QD output. When TEST STROBE is "low" the Q bus has all low outputs (which is equivalent to being tri-stated).

The VSC864A-2 can be configured to run in either synchronous clocked mode or asynchronous flow-through mode. This feature is controlled by the C/FT input. When C/FT is high, the chip is in clocked mode and will require an input clock at its CK pin. In this mode all input and output data is registered. When C/FT is low the chip is in flow-through mode and will ignore the CK input. In clocked mode, the outputs on the monitor bus (Q0- Q6, and QD), and input data (I0 - I63) are registered by the master clock (CK).

Figure 1: Block Diagram



Data Sheet

200 Mb/s 64 x 64 Crosspoint Switch

Absolute Maximum Ratings (1)

Power Supply Voltage (ECL), VTT potential to GND ..... -3.0V to +0.5V
Input Voltage Applied, VE CLIN ..... -2.5V to +0.5V
Output Current, IOUT,(DC, output HI) ..... 100 mA
Case Temperature Under Bias, TC. ..... -55° to +125°C
Storage Temperature (ambient), TSTG. ..... -65°C to +150°C

Recommended Operating Conditions

ECL Supply Voltage, VTT. ..... -2.0V ± 0.1V
Commercial Operating Temperature Range, T(2). ..... 0° to 70°C
Industrial Operating Temperature Range, T(2). ..... -40° to 85°C

NOTES: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extendedperiods may affect device reliability.
(2) Lower limit of specification is ambient temperature and upper limit is case temperature.

AC Characteristics *(Over recommended operating conditions V_{CC} = V_{CCA} = GND Output load 25Ω to V_{TT})*

Table 1: Flow-Through Mode.

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
PW	Minimum data valid time	5	—	—	ns	≤ 20% Duty Cycle Distortion; 50% input
t_{DR}	Propagation delay (rising)	2800	—	5800	ps	—
t_{DF}	Propagation delay (falling)	2800	—	5800	ps	—
—	Duty cycle distortion	—	10	20	%	at 200 Mb/s(1)
skew	Output to output skew	—	—	2500	ps	On a given part broadcast mode
BER	Bit Error Rate	—	—	10^{-13}	—	Note (2)

(1) Duty cycle distortion = duty cycle out - duty cycle in / duty cycle in x 100%
(2) Based on limited measurement time, not device performance limitations

Table 2: Clocked Mode.

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
f_{MAX}	Maximum clock rate	—	—	200	MHz	—
t_{ISU}	Input data set-up time	50	—	—	ps	—
t_{IH}	Input data hold time	2000	—	—	ps	—
t_{CZR}	Clock to output delay (rising)	2000	—	3500	ps	—
t_{CZF}	Clock to output delay (falling)	2000	—	3500	ps	—
skew	Output to output skew	—	—	1500	ps	On a given part, broadcast mode

Table 3: Write Mode.

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
t_{RECON}	Reconfiguration time	650	1300	—	ns	—
t_{ALSSU}	A but to LOCAL STROBE set-up time	300	—	—	ps	—
t_{ALSH}	a bus to LOCAL STROBE hold time	0	-	—	ps	—
t_{DLSSU}	D bus to LOCAL STROBE set-up time	400	—	—	ps	—
t_{DLSH}	D bus to LOCAL STROBE hold time	2	—	—	ns	—
t_{GLSU}	GLOBAL STROBE to LOCAL STROBE set-up time	5	—	—	ns	—
t_{GS},t_{LS}	GLOBAL STROBE and LOCAL STROBE pulse widths	5	—	—	ns	Recommended local strobe frequency = 50MHz
t_{LSL}	LOCAL STROBE low time	5	—	—	ns	—
t_{TS}	TEST STROBE pulse width	6.5	—	—	ns	—
t_{GLH}	GLOBAL STROBE to LOCAL STROBE hold time	0	—	—	ps	—

Parameters	Description	Min	Typ	Max	Units	Conditions
t_{GSZ}	GLOBAL STROBE to valid output (flow-through mode)	2.7	—	5.6	ns	—
t_{CGSU}	CLK to GLOBAL STROBE set-up time (clocked mode)	200	—	—	ps	Data being clocked in at this time is invalid
t_{GCL}	GLOBAL STROBE to CLK hold time (clocked mode)	3.5	—	—	ns	Data being clocked in at this time is invalid
t_{TSQ}	TEST STROBE to valid Q output	—	—	7.1	ns	—
t_{TSBQ}	S bus to valid output	—	—	7.1	ns	—
t_{TSQT}	TEST STROBE to tri-state condition on Q	—	—	6.5	ns	—

AC Timing Waveforms

Figure 2: Flow-through Mode

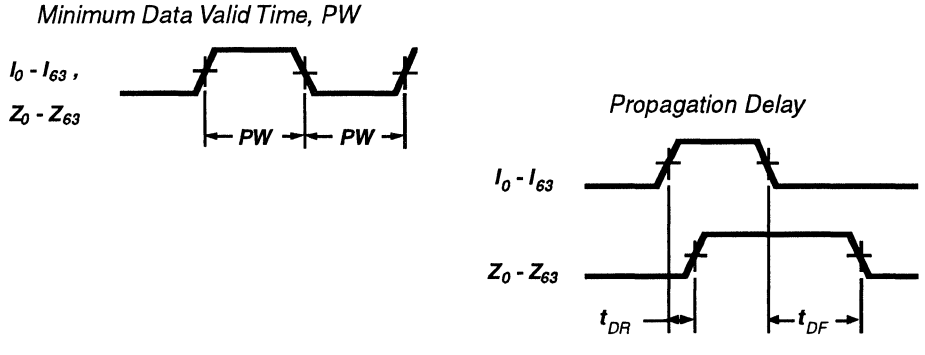
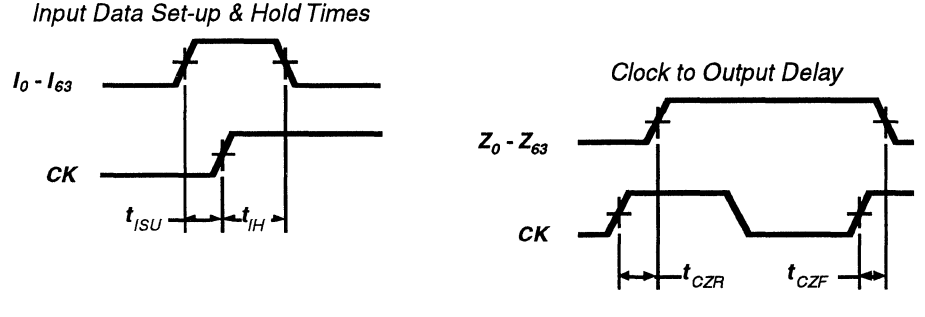


Figure 3: Clocked Mode



Telecom/ATM

Figure 4: Write Mode

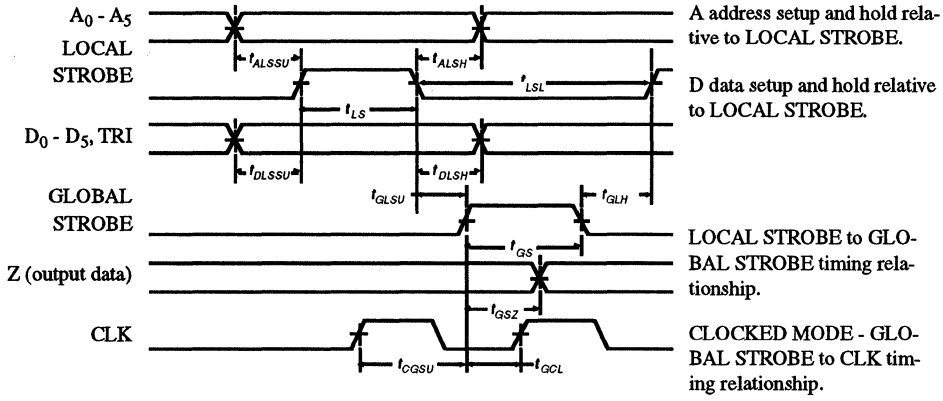


Figure 5: Read Mode

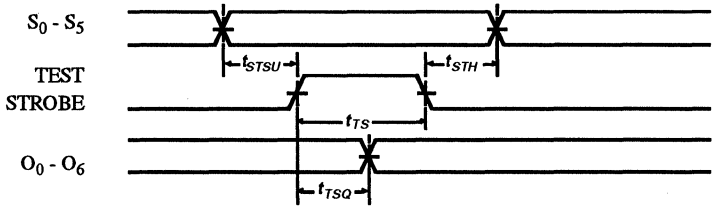


Figure 6: Block Diagram of Internal Write Mode Circuits

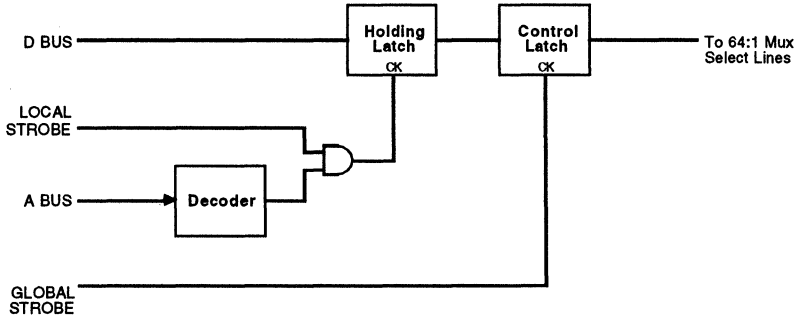


Table 4: Pin Description

Pin #	*Name*	*I/O*	*Description*
12-16, 20-30, 35-45, 49-53,184-188, 192- 202, 207-217, 221-225	I_0 - I_{63}	I	The 64 ECL signal inputs.
11	TRI	1	ECL input containing Tristate data to be loaded into a 64:1 Mux holding latch. (Tristate = HIGH) Combined with a control register's destination address. Used to tristate the corresponding output.
5-10	D_0 - D_5	I	ECL inputs containing the destination address to be loaded into the 64:1 Mux holding latch.
178-183	A_0 - A_5	I	ECL inputs containing the address of the 64:1 Mux holding/ control latch to be programmed.
177	LOCAL STROBE	I	Active HIGH, ECL input used to load the D0-D5 and TRI data into the 64:1 Mux holding latch.
34	GLOBAL STROBE	I	Active HIGH, ECL input used to load destination addresses to all 64:1 S Mux control latches simultaneously from the data contained in their corresponding holding latches.
54-59	S_0 - S_5	I	ECL inputs containing the address of the control latch to be observed at the QD output when the TEST STROBE is HIGH.
60	TEST STROBE	I	Active HIGH, ECL input used to enable Test Mode and observation of a selected 64:1 Mux control latch's destination address.
206	C/FT	I	ECL input used to enable Clocked or Flow-through Mode (Clocked = HIGH/Flow-Thru = LOW).
203	CK	I	ECL clock input for Clocked Mode.
68, 71, 73, 78, 80, 83, 85, 88, 92,95,97,100,102,107,109,112, 126, 129, 131, 136,138, 141,143, 148, 150, 153, 155,158, 162, 165, 167, 170, 240, 243, 245, 250, 252, 255, 257, 260, 264, 267, 269, 272, 274, 279, 281, 284, 298, 301, 303, 308, 310, 313, 315, 320, 322, 325, 327, 330, 334, 337, 339, 342	Z_0 - Z_{63}	O	The 64 ECL signal outputs.
296	QD	O	ECL output used to observe the output of a selected 64:1 Mux in Test Mode.
114,117,121,124,286,289,293	Q_0 - Q_6	O	ECL outputs containing the selected 64:1 Mux control register's destination address and TRI bit in Test Mode

Pin #	Name	I/O	Description
3, 17, 32, 47, 61, 76, 90, 104, 118,132, 146, 160, 175, 189, 204, 219, 233, 248, 262,276, 290, 304, 318, 332	VCC		ØV ground connection for internal logic.
2, 63, 69, 74, 81, 86, 93, 98, 103, 110, 115, 122, 127, 134, 139, 144, 151, 156, 163, 168, 174, 235, 241, 246, 253, 258, 265, 270, 275, 282, 287, 294, 299, 306, 311, 316, 323, 328, 335, 340	VCCA		ØV 'dirty' ground connection for outputs.
4, 18, 33, 48, 62, 77, 91, 105,119, 133, 147, 161, 176, 190,205, 220, 234, 249, 263, 277,305, 319, 333	VTT		-2V supply connection.
291	VSUB		-2V supply connection to substrate (most negative supply).
1, 19, 31, 46, 64-67, 70, 72, 75, 79, 82, 84, 87, 89, 94, 96, 99, 101, 106, 108, 111, 113, 116, 120, 123, 125, 128, 130, 135, 137, 140, 142, 145, 149, 152, 154, 157, 159, 164, 166, 169,171-173, 191, 218, 226-232, 236-239, 242, 244, 247, 251, 254, 256, 259, 261, 266, 268, 271, 273, 278, 280, 283, 285, 288, 292, 295, 297, 300, 302, 307, 309, 312, 314, 317, 321, 324, 326, 329, 331, 336, 338, 341, 343, 344	N/C		No Connection. These pins are not internally connected.

Data Sheet

200 Mb/s 64 x 64 Crosspoint Switch

Table 5: Pin Identification

Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #
I_0	12	I_{22}	26	I_{44}	41	D_2	7	Z_6	85	Z_{28}	162	Z_{50}	303
I_1	225	I_{23}	211	I_{45}	196	D_3	8	Z_7	88	Z_{29}	165	Z_{51}	308
I_2	13	I_{24}	27	I_{43}	42	D_4	9	Z_8	92	Z_{30}	167	Z_{52}	310
I_3	224	I_{25}	210	I_{43}	195	D_5	10	Z_9	95	Z_{31}	170	Z_{53}	313
I_4	14	I_{26}	28	I_{43}	43	A_0	183	Z_{10}	97	Z_{32}	240	Z_{54}	315
I_5	223	I_{27}	209	I_{43}	194	A_1	182	Z_{11}	100	Z_{33}	243	Z_{55}	320
I_6	15	I_{28}	29	I_{43}	44	A_2	181	Z_{12}	102	Z_{34}	245	Z_{56}	322
I_7	222	I_{29}	208	I_{43}	193	A_3	180	Z_{13}	107	Z_{35}	250	Z_{57}	325
I_8	16	I_{30}	30	I_{43}	45	A_4	179	Z_{14}	109	Z_{36}	252	Z_{58}	327
I_9	221	I_{31}	207	I_{43}	192	A_5	178	Z_{15}	112	Z_{37}	255	Z_{59}	330
I_{10}	20	I_{32}	35	I_{43}	49	S_0	54	Z_{16}	126	Z_{38}	257	Z_{601}	334
I_{11}	217	I_{33}	202	I_{43}	188	S_1	55	Z_{17}	129	Z_{39}	260	Z_{61}	337
I_{12}	21	I_{34}	36	I_{43}	50	S_2	56	Z_{18}	131	Z_{40}	264	Z_{62}	339
I_{13}	216	I_{35}	201	I_{43}	187	S_3	57	Z_{19}	136	Z_{41}	267	Z_{63}	342
I_{14}	22	I_{36}	37	I_{43}	51	S_4	58	Z_{20}	138	Z_{42}	269	Q_0	114
I_{15}	215	I_{37}	200	I_{43}	186	S_5	59	Z_{21}	141	Z_{43}	272	Q_1	117
I_{16}	23	I_{38}	38	I_{43}	52	Z_0	68	Z_{22}	143	Z_{44}	274	Q_2	121
I_{17}	214	I_{39}	199	I_{43}	185	Z_1	71	Z_{23}	148	Z_{45}	279	Q_3	124
I_{18}	24	I_{40}	39	I_{43}	53	Z_2	73	Z_{24}	150	Z_{46}	281	Q_4	286
I_{19}	213	I_{41}	198	I_{43}	184	Z_3	78	Z_{25}	153	Z_{47}	284	Q_5	289
I_{20}	25	I_{42}	40	D_0	5	Z_4	80	Z_{26}	155	Z_{48}	298	Q_6	293
I_{21}	212	I_{43}	197	D_1	6	Z_5	83	Z_{27}	158	Z_{49}	301		

Package Information

Figure 7: 344 Pin Ceramic LDCC Package

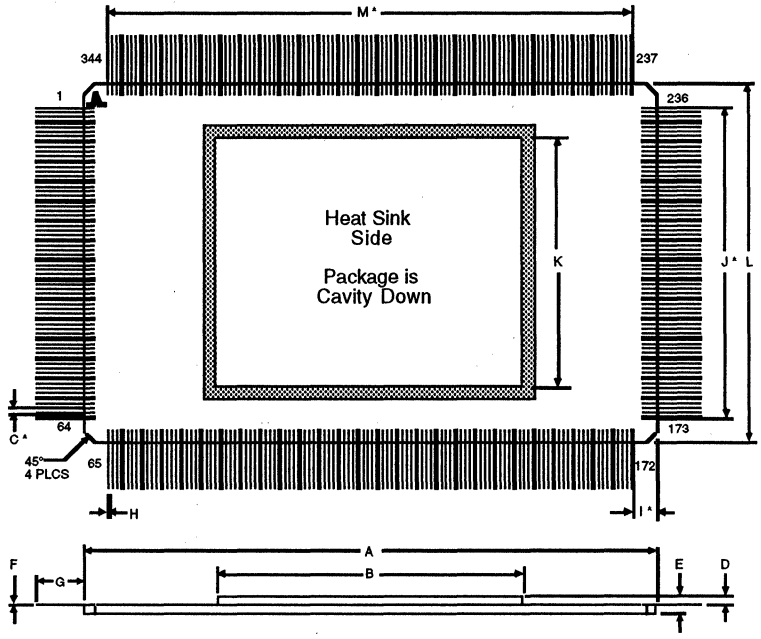


Table 6: 344 Pin Ceramic LDCC Tolerance Table

Item	*mm (Min/Max)*	*In (Min/Max)*	*Item*	*mm (Min/Max)*	*In (Min/Max)*
A	58.93/59.94	2.320/2.340	H	0.15/0.25	0.006/0.010
B	34.54 TYP	1.36 TYP	I*	REF 2.54 TYP	REF 0.100 TYP
C*	0.51 TYP	0.020 TYP	J*	32.00 TYP	1.26 TYP
D	0.38/0.63	0.015/0.025	K	39.46 TYP	1.08 TYP
E	2.16/2.92	0.085/0.115	L	36.57/37.59	1.440/1.480
F	0.09/0.216	0.0004/0.008	M*	54.36 TYP	2.140 TYP
G	5.08/7.62	0.200/0.300	—	—	—

**At package body*

NOTES: 1) Drawing not to scale.
2) Packages: Ceramic (alumina); Heat sinks: Copper-tungsten; Leads: Alloy 42 with gold plating

Expandability

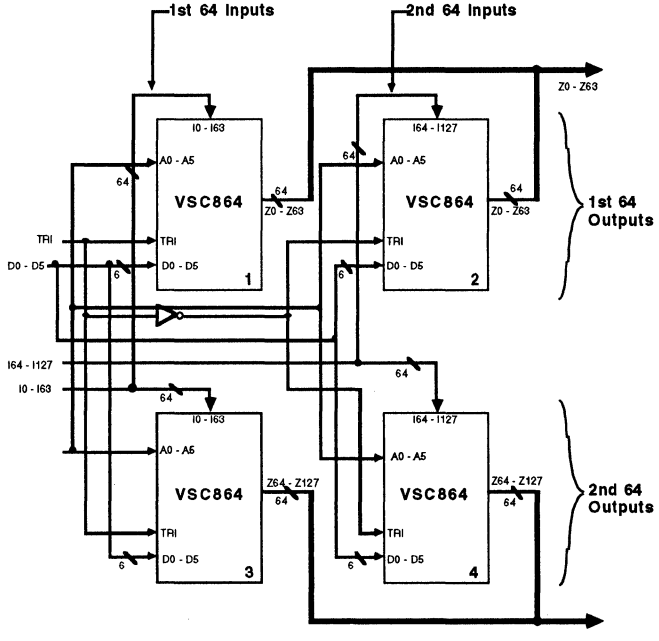
The VSC864A-2 can be expanded to larger crosspoint switches by configuring it so that any input can be multiplexed to any output. The figure below is an example of a 128 x 128 crosspoint switch. The top two VSC864A-2s (1&2) correspond to the first 64 outputs and the bottom two VSC864A-2s (3&4) correspond to the last 64 outputs. The VSC864A-2s on the left (1&3) correspond to the first 64 inputs, and the two VSC864A-2s on the right (2&4) correspond to the last inputs. All like outputs are then joined to form a 128 bit Z output bus. The ability of the VSC864A-2 to tri-state its outputs will prevent contention on the Z bus.

The TRI input is configured such that when it is active on the left hand chips (which are responsible for routing the first 64 inputs) it is inactive on the two right hand chips (which are responsible for routing the last 64 inputs). The TRI input thus functions as the MSB of a 7-bit channel address word (A-bus plus TRI). Chips can share A-bus information. The destination (D) bus can be shared among the four chips with the local strobe for each device being used to select which output address gets reconfigured.

The layout and placement of the VSC864A-2 is such that inputs are on the top and bottom of the chip and outputs are to the right and left. In this way a PC board design for a large crosspoint is facilitated.

In the read mode tri-stateability on the Q-bus can be controlled with the TEST STROBE input. A "low" level on this input will tri-state its corresponding Q-bus. In this way the Q-bus from all chips can be wire-OR'ed. Individual TEST STROBE signals to each chip, however, are required.

Figure 8: 128 X 128 Crosspoint Switch Diagram



Ordering Information

The part number for this product is formed by a combination of the device number and the package style:

VSC864A-2xx

Device Type:

VSC864A-2: 64X64 Crosspoint Switch

Package Type

F: 344-pin Leaded Chip Carrier (LDCC)

Notice

Vitesse Semiconductor Corporation reserves the right to make changes in its products, specifications or other information at any time without prior notice. Therefore the reader is cautioned to confirm that this datasheet is current prior to placing any orders. The company assumes no responsibility for any circuitry described other than circuitry entirely embodied in a Vitesse product.

Warning

Vitesse Semiconductor Corporation's product are not intended for use in life support appliances, devices or systems. Use of a Vitesse product in such applications without the written consent is prohibited.

Package Outlines

Introduction

This section contains outline drawings for all Vitesse Communications product packages. Table 1 lists each product, along with it's corresponding package and page number. Package outlines are also provided in the data sheets located in the telecommunications and datacommunications sections of this data book.

Table 1: Vitesse Communications Product Packages

Product	Package	Page #	Product	Package	Page #
VSC7105	44 pin PQFP	521	VS8022	52 pin LDCC	522
VSC7106	44 pin PQFP	521	VSC8023	192 TBGA	527
VSC7107	184 pin PQFP	526	VSC8024	192 TBGA	527
VSC7115	52 pin PQFP	523	VS8061	52 pin LDCC	522
VSC7116	52 pin PQFP	523		52 pin PQFP	523
VSC7117	208 pin PQFP	528	VS8062	52 pin LDCC	522
VSC7120	52 pin PQFP	523		52 pin PQFP	523
VSC7121	44 pin PQFP	521	VSC8063	52 pin PQFP	523
VSC7125	64 pin PQFP, 10 mm	524	VSC8071	Module	534
VSC7125	64 pin PQFP, 14 mm	524	VSC8072	Module	534
VSC7201A	269 pin TBGA	529	VSC8101	28 PLCC	520
VSC7203	301 pin TBGA	530	VSC8102	100 pin PQFP	525
VSC7802/7805, VSC7810	5.6 mm, TO-46 Ball Lens	532, 533	VSC8110	100 pin PQFP	525
VS8004	28 pin LDCC	519	VSC8111	100 pin PQFP	525
VS8005	28 pin LDCC	519	VSC8112	100 pin PQFP	525
VS8021	52 pin LDCC	522	VSC864A-2	344 pin LDCC	531

Trim and Form Equipment

Fancort Industries offers a variety of trim and form presses, ranging from smaller, economical, hand operated arbor presses, to more sophisticated trim and form presses for use in volume production and automated systems. Depending on the application, Fancort Industries will be able to recommend the most appropriate solution. Table 2 contains a list of all packages supported with Fancort lead trim and form equipment. For further information, contact Fancort Industries at 201/575-0610.

Table 2: Fancort Forming Tools for Vitesse Standard Packages

Pin Count	Type	Notes	Fancort Part #
28 LDCC	Quad	Square .050 pitch	VF-1A/4
52 LDCC	Quad	Square .050 pitch	VF-1A/4
344 LDCC	Quad	Rectangular .020 pitch	VF-1A/4L

Note: Trim and form equipment may be available for additional Vitesse packages.

Package Outlines

Corfin Industries, Inc., utilizing Fancort Industries equipment, is the approved Vitesse vendor for trimming, forming and tinning. The following are brief descriptions of Corfin's SMT tooling and services for processing your Vitesse quadpacks. The level should be determined by taking into account your production requirements and specifications.

Level 1

Corfin will form your components to specification using your universal systems, and if necessary, supply adjustable matrix trays for shipping the parts to you.

Level 2

Fancort's universal tooling is designed for high mix and low production, R&D, training and repair. They process one side of the component at a time, and give you the flexibility to produce almost any footprint on packages up to 2.5" X 2.5". A larger model is available for packages up to 4" X 4".

P/N V-F-1B/1-P	Fixed Foot
P/N V-F-1B/3A-P	Adjustable Foot

Level 3

Fancort's dedicated tooling with manual standoff control is designed for moderate production, and can be used in our hand or air press. These tools process all sides of the component at one time, and have a built-in micrometer for varying the standoff height. These tools hold the tightest, and most consistent tolerances.

P/N V-F-1A/4	28 pins to 256 pins
P/N V-F-1A/4L	344 pins
P/N 3300	Hand Press
P/N 5000-1	Air Press

Note: One dedicated die is necessary for each new pin count.

Level 4

Fancort's Electronic Floating Anvil tooling is designed for production runs of very expensive parts, and where automatic standoff control is required. These tools will automatically control the finished standoff to within +/-.002" regardless of lead exit point and ceramic thickness. These tools automatically hold the tightest and most consistent tolerances.

P/N V-F-1F/4	28 pins to 256 pins
P/N V-F-1F/4L	344 pins
P/N 5000-1	Special Air Press

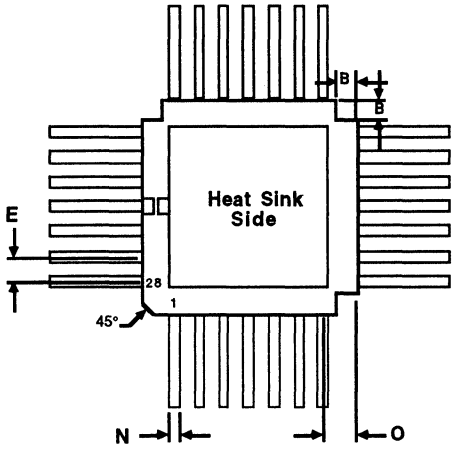
Note: One dedicated die is necessary for each new pin count.

Level 5

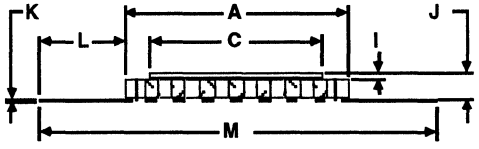
Corfin utilizes an electronic floating anvil press enabling customers to purchase a Level 4 tool for use in their integrated system. All you purchase is a dedicated Floating Anvil tool P/N F-1F series.

Package Outlines

Figure 1: 28 Pin Ceramic LDCC Package Dimensions



28-Pin Leaded
Ceramic Package (LDCC)

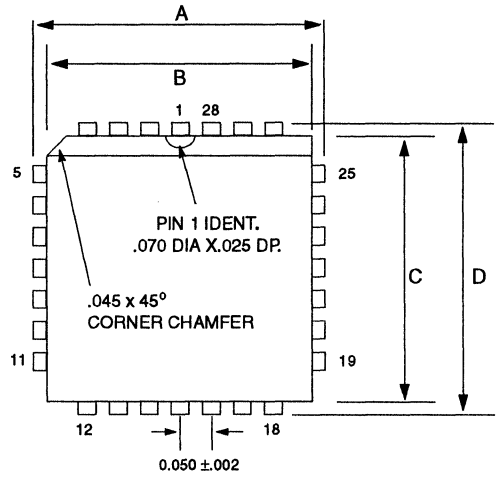


NOTES:
Drawing not to scale.
Package: Ceramic (alumina);
Heat sink: Copper-tungsten;
Leads: Alloy 42 with gold plating.

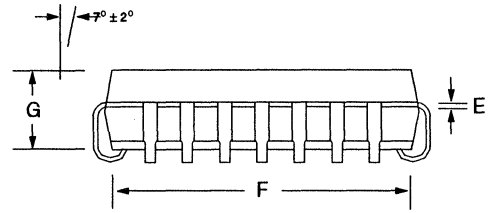
Item	mm (Min/Max)	in (Min/Max)	Item	mm (Min/Max)	in (Min/Max)
A	11.176/11.682	0.440/0.460	K	0.102/0.203	0.004/0.008
B	1.016/1.524	0.040/0.060	L	5.842/6.858	0.230/0.270
C	8.128/8.636	0.33 TYP	M	22.860/25.398	0.900/1.000
E	1.143/1.397	0.050 TYP	N	0.356/0.559	0.014/0.022
I	0.406/0.610	0.016/0.024	O	1.525/2.287	0.075 TYP
J	1.829/2.235	.072/.088	—	—	—

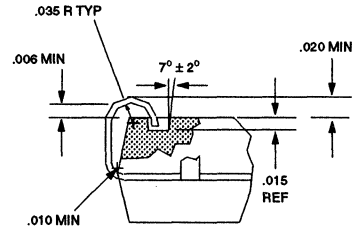
Package Outlines

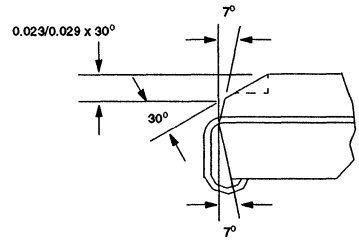
Figure 2: 28 PLCC Package Dimensions (JEDEC Format)



Item	*inch*	*Tol.*
A	.490	±.005
B	.454	±.002
C	.454	±.002
D	.490	±.005
E	.010	±.0003
F	.420	±.010
G	.152	±.002



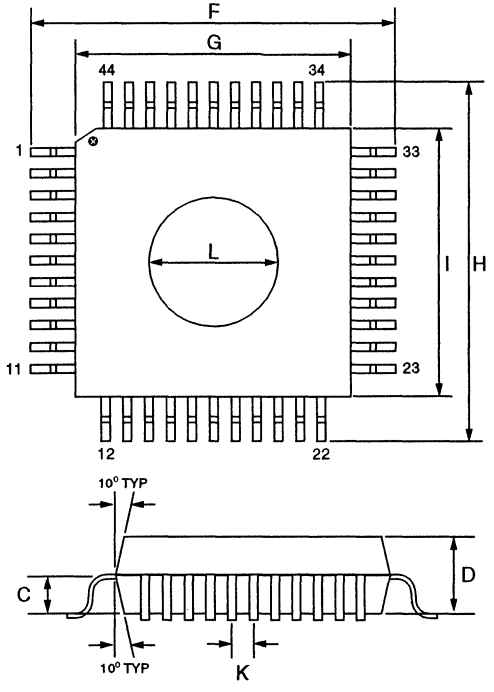




NOTES:
(1) Drawings not to scale.
(2) All units in inch unless otherwise noted.

Package Outlines

Figure 3: 44 Pin PQFP Package Dimensions



Item	*mm*	*Tol.*
A	2.35	MAX
D	2.00	+.10 / -.05
E	0.35	±.05
F	17.20	±.25
G	14.00	±.10
H	17.20	±.25
I	14.00	±.10
J	0.88	+.15 / -.10
J1	0.80	+.15 / -.10
K	1.00	BASIC
L	6.86	±.50 DIA.

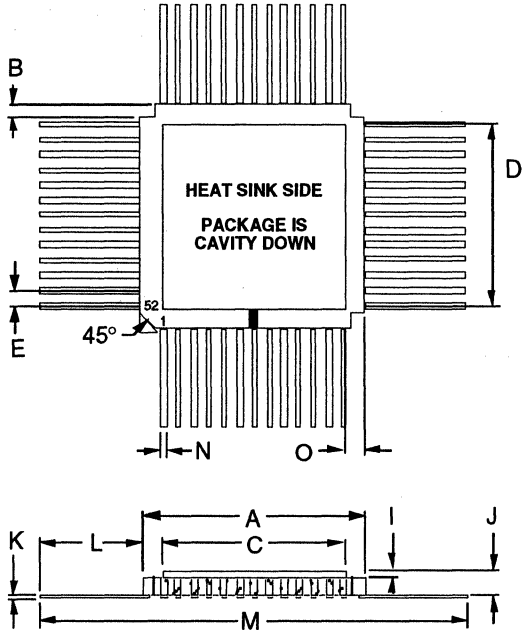
The heat spreader is tied to V_{SS}

NOTES:
Drawing not to scale.
Heat spreader up.
All units in mm unless otherwise noted.

Package Outlines

Figure 4: 52 Pin LDCC Package Dimensions

52-Pin Leaded
Ceramic Package (LDCC)



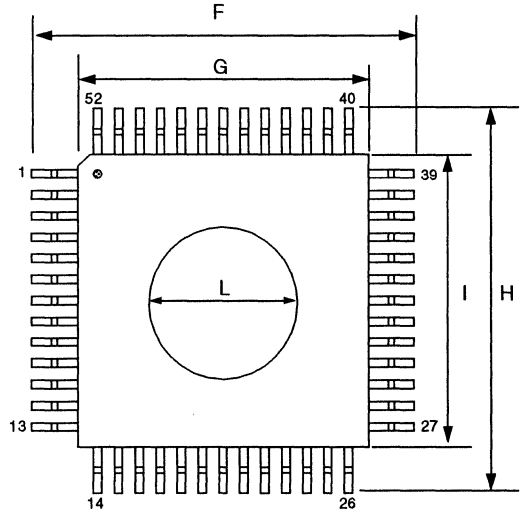
NOTES:
Drawing not to scale.
Packages: Ceramic (alumina);
Heat sink: Copper-tungsten;
Leads: Alloy 42 with gold plating.

Item	*mm (Min/Max)*	*in (Min/Max)*	*Item*	*mm (Min/Max)*	*in (Min/Max)*
A	18.54/19. 56	0.730/0.770	I	0.41/0.61	0.016/0.024
B	1.02/1.52	0.040/0.060	J	2.03/2.79	0.080/0.110
C*	15.49/16.51	0.610/0.650	K*	0.09/0.24	0.003/0.009
D*	15.24 TYP	0.600 TYP	L	4.57/5.34	0.180/0.210
E	1.27 TYP	0.050 TYP	M	27.69/30.22	1.090/1.190
F	0.76/1.02	0.030/0.040	N	0.36/0.56	0.014/0.022
G	16.94 TYP	0.667 TYP	O	1.75/1.90	0.069/0.075
H	1.91/2.41	0.075/0.095	—	—	—

**At package body.*

Package Outlines

Figure 5: 52 Pin PQFP Package Dimensions

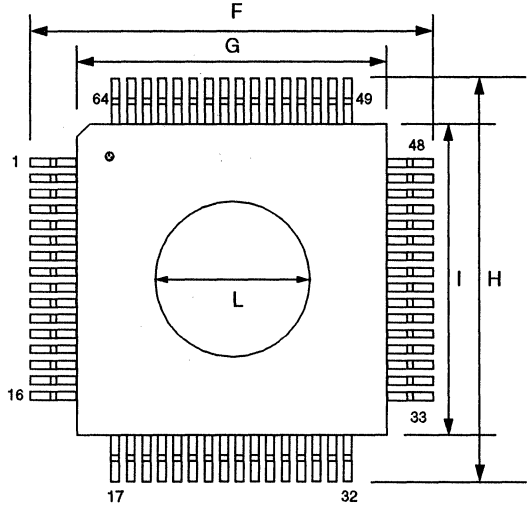


Item	mm	Tol.
A	2.45	MAX
D	2.00	+0.10/-.05
E	0.30	±.05
F	13.20	±.25
G	10.00	±.10
H	13.20	±.25
I	10.00	±.10
J	0.88	+.15 / -.10
K	0.65	BASIC
L	3.56	±.50 DIA.

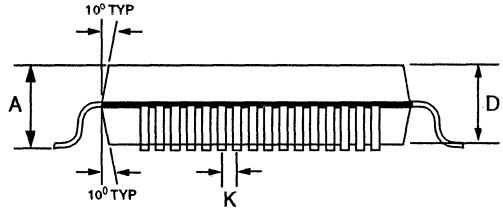
NOTES:
Drawing not to scale.
Heat spreader up.
All units in mm unless otherwise noted.
Heat spreader is connected to V_{ss}.

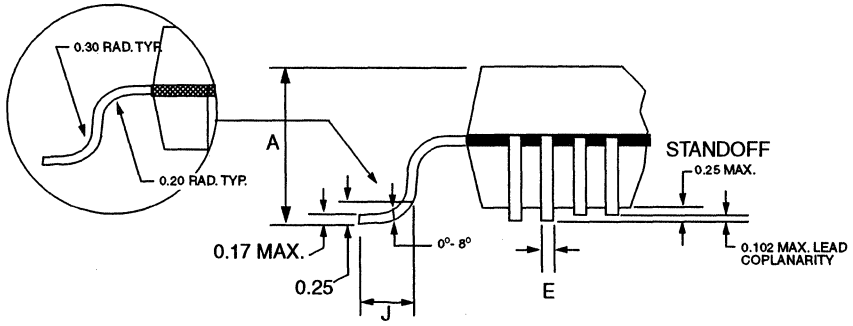
Package Outlines

Figure 6: 64 Pin PQFP Package Dimensions



Item	10 mm	14 mm	Tol.
A	2.45	2.45	MAX
D	2.00	2.00	+0.10
E	0.30	0.35	±.05
F	13.20	17.20	±.25
G	10.00	14.00	±.10
H	13.20	17.20	±.25
I	10.00	14.00	±.10
J1	TBD	TBD	TBD
J	0.88	0.80	±.15
K	0.50	0.80	BASIC
L	3.56	N/A	±.50 DIA.

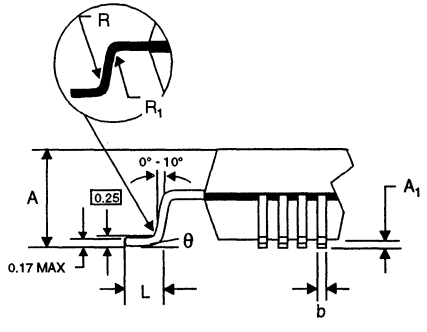




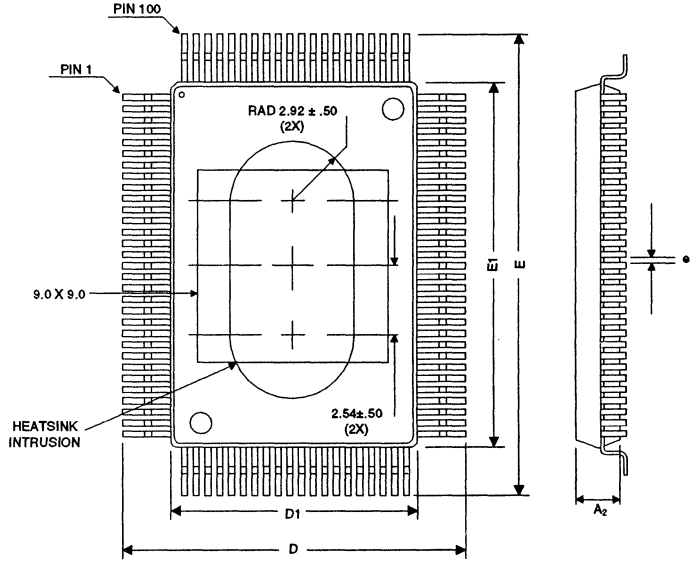
NOTES:
Drawing not to scale.
Heat spreader up on 10mm package only.
All units in mm unless otherwise noted.
Heat spreader is not electrically connected.

Package Outlines

Figure 7: 100 Pin PQFP Package Dimensions



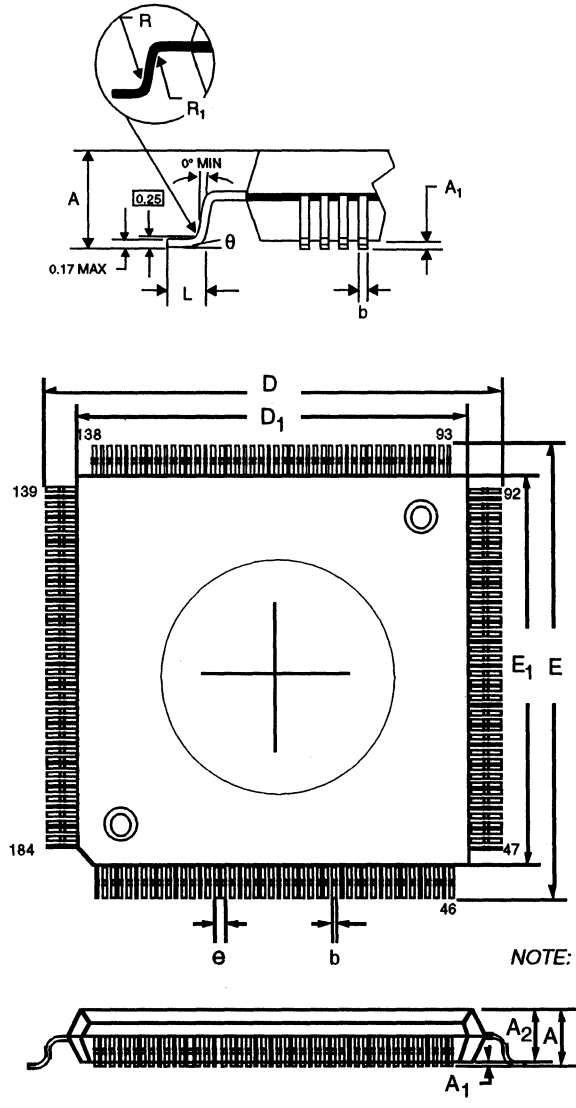
Dims.	mm	Tolerance
A	2.35	MAX
A1	0.25	MAX
A2	2.00	±.10
D	17.20	±.40
D1	14.00	±.10
E	23.20	±.40
E1	20.00	±.10
L	0.80	±.2
e	0.65	NOM
b	0.30	±.10
θ	0-7°	
R	.30	RAD TYP
R1	.2	NOM



NOTES:
(1) Drawings not to scale.
(2) Two styles of exposed heat spreaders may be used; square or oval.
(3) All units in millimeters

Package Outlines

Figure 8: 184 Pin PQFP Package Dimension

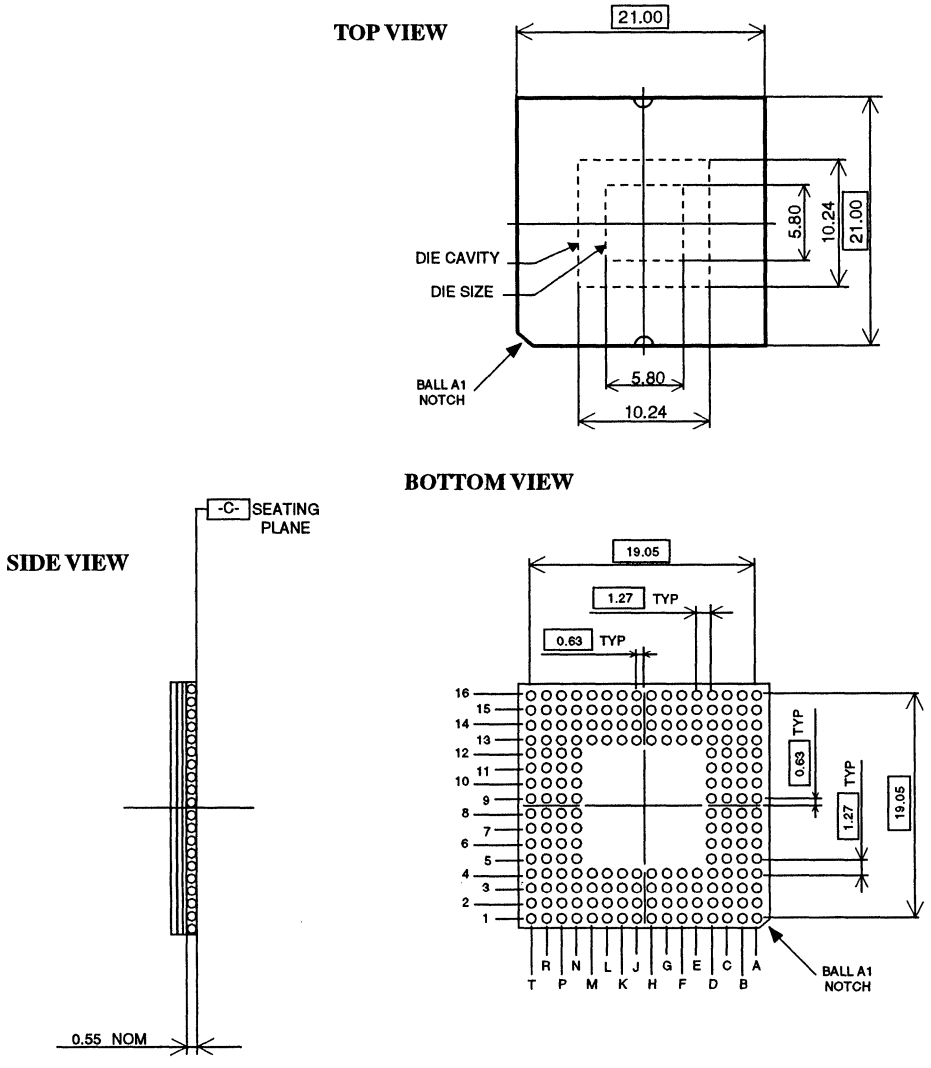


Dims.	mm	Tolerance
A	4.07	MAX
A1	0.25	MIN
A2	3.49	±.10
D	31.20	±.25
D1	28.00	±.10
E	31.20	±.25
E1	28.00	±.10
L	0.88	+.15/-.10
e	0.50	BASIC
b	0.22	±.05
θ	0-7°	
R	.30	TYP
R1	.20	TYP

NOTE: Drawing not to scale.

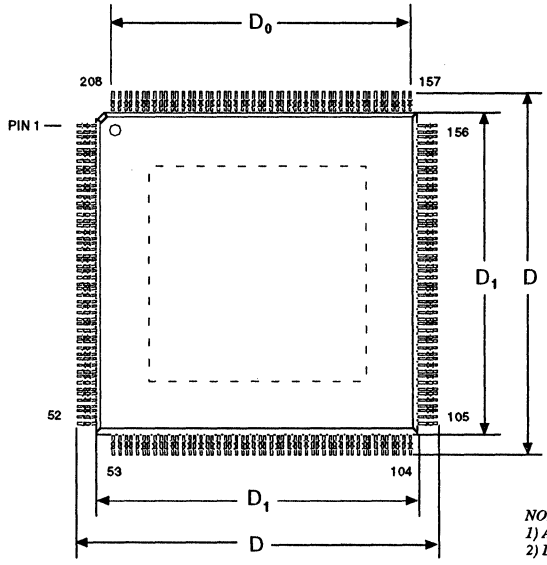
Package Outlines

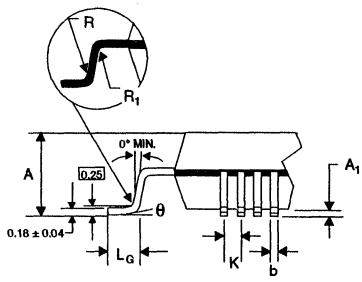
Figure 9: 192 Pin TBGA Package Dimensions *(in millimeters)*



Package Outlines

Figure 10: 208 Pin PQFP Package Dimensions



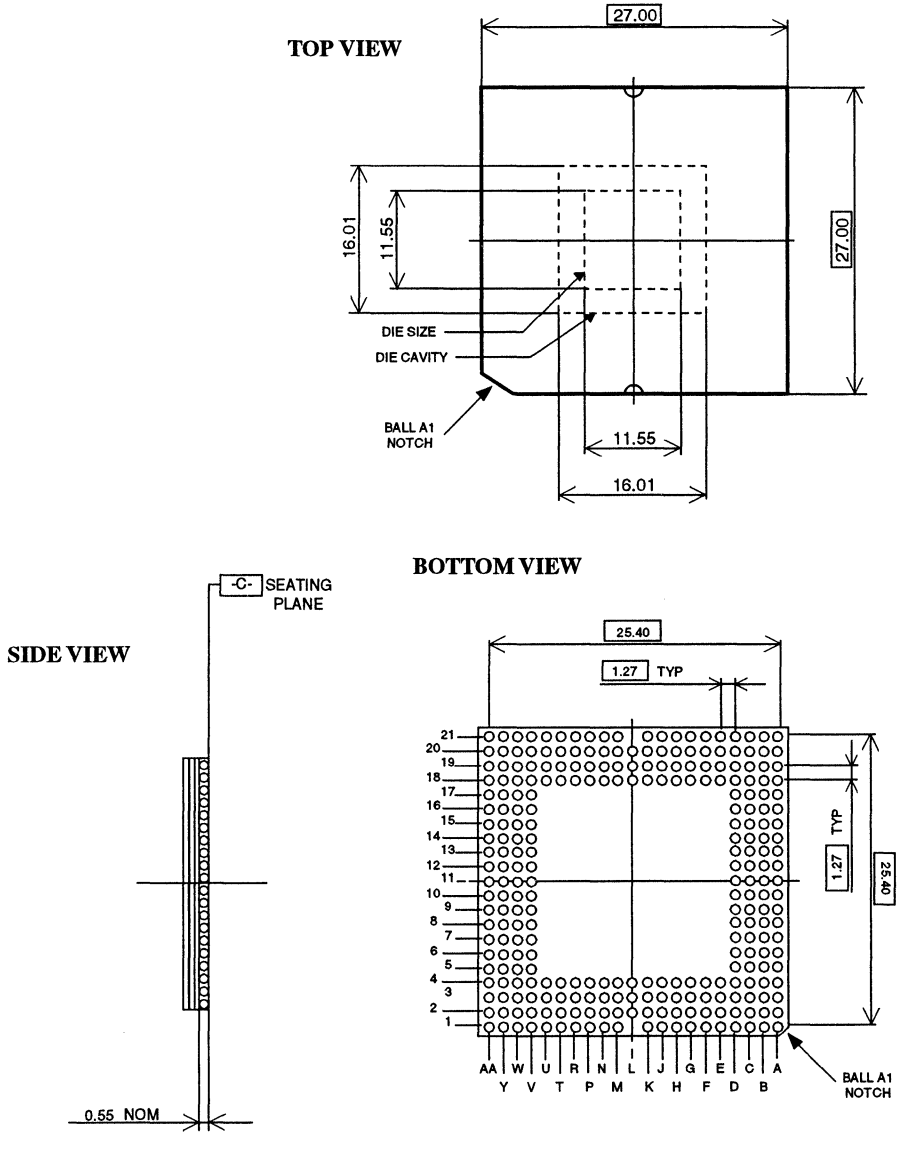


NOTES:
1) All dimensions in millimeters.
2) Dimensions shown are nominal with tolerances as indicated.

Dimensions	*mm*	*Tolerance*
A	4.10	MAX
A1	0.25	MIN
A2	3.40	± 0.20
D	30.60	
D0	25.5	REF
D1	28.00	± 0.10
b	0.22	± 0.08
K	0.50	NOM
LG	0.60	± 0.16
θ	0-10°	
R	.25	NOM
R1	.2	NOM

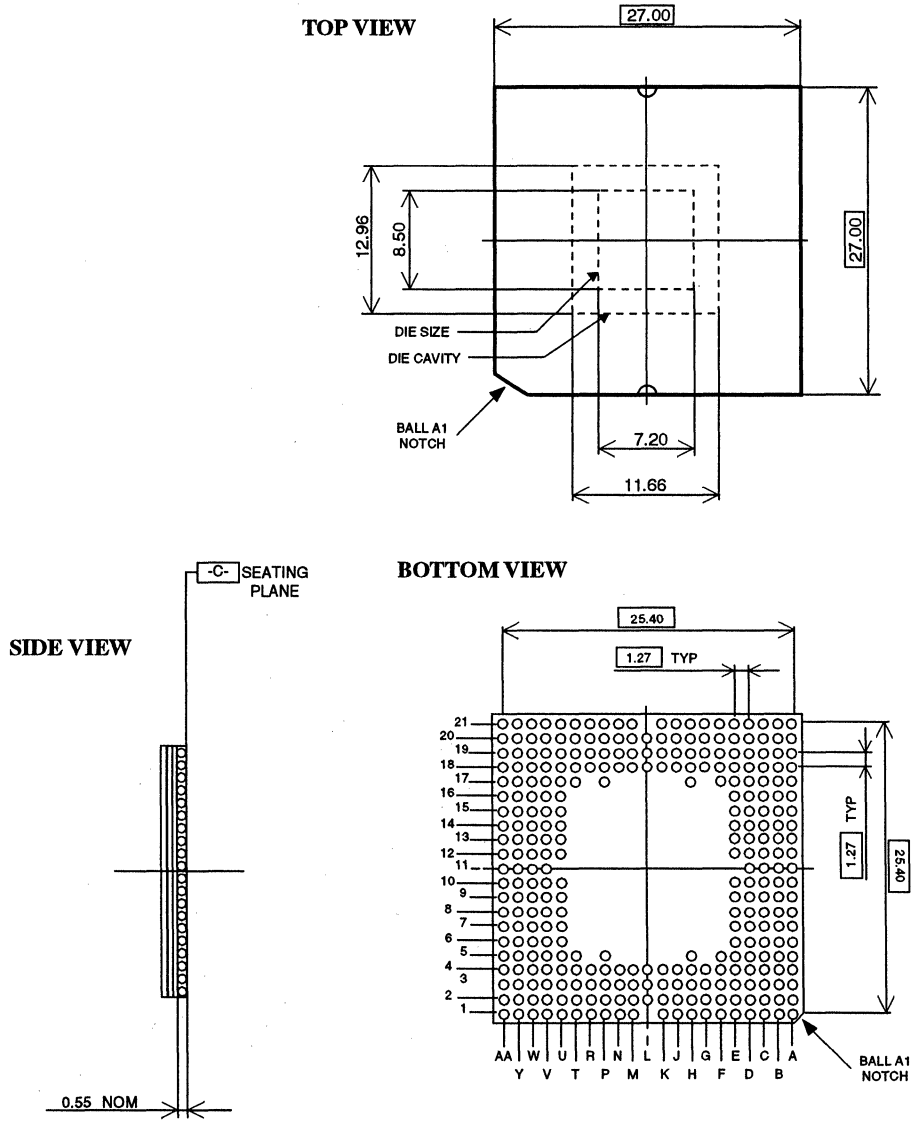
Package Outlines

Figure 11: 269 Pin TBGA Package Dimensions *(in millimeters)*



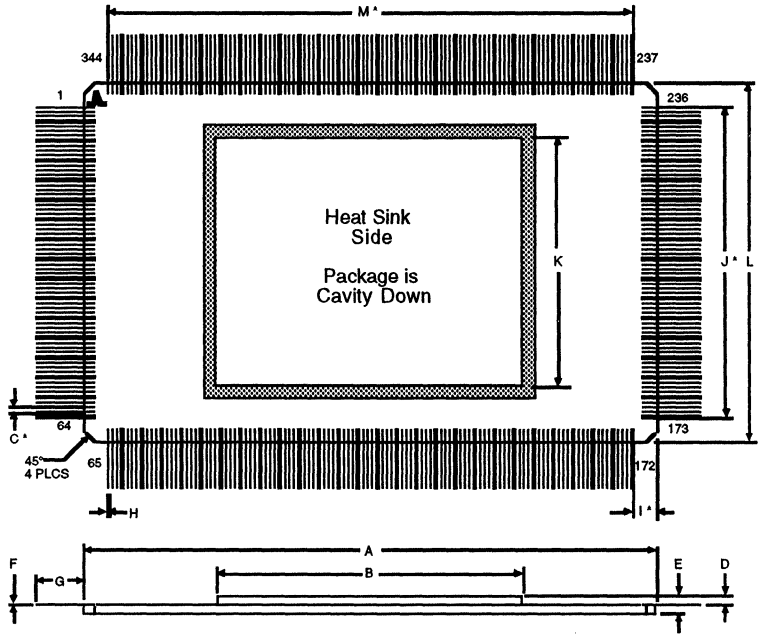
Package Outlines

Figure 12: 301 Pin TBGA Package Dimensions *(in millimeters)*



Package Outlines

Figure 13: 344 Pin Ceramic LDCC Package Dimensions



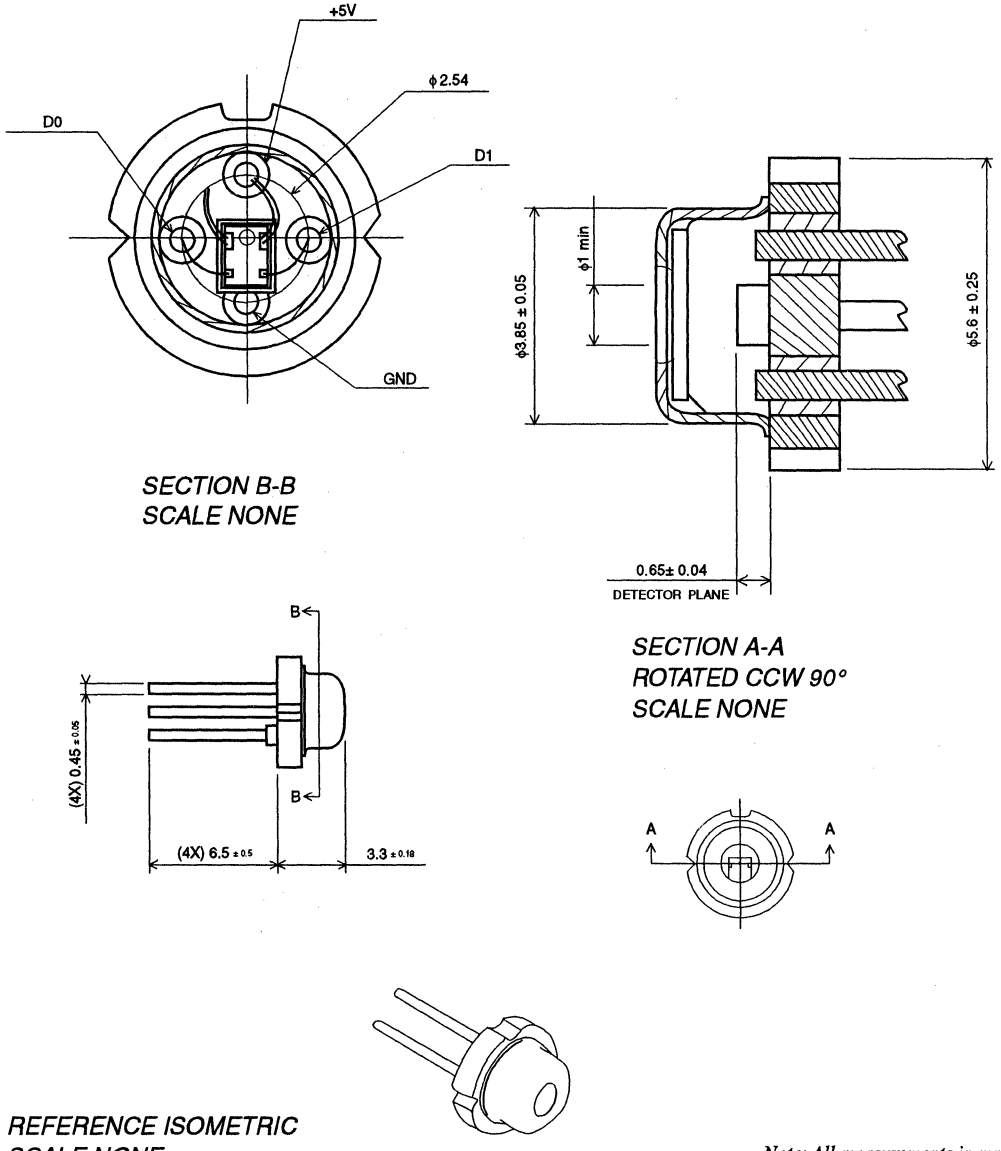
Item	mm (Min/Max)	In (Min/Max)	Item	mm (Min/Max)	In (Min/Max)
A	58.93/59.44	2.320/2.340	H	0.15/0.25	0.006/0.010
B	34.54 TYP	1.36 TYP	I*	REF 2.54 TYP	REF 0.100 TYP
C*	0.51 TYP	0.020 TYP	J*	32.00 TYP	1.26 TYP
D	0.38/0.63	0.015/0.025	K	39.46 TYP	1.08 TYP
E	2.16/2.92	0.085/0.115	L	36.57/37.59	1.440/1.480
F	0.09/0.216	0.0004/0.008	M*	54.36 TYP	2.140 TYP
G	5.08/7.62	0.200/0.300	—	—	—

**At package body*

NOTES: 1) Drawing not to scale.
2) Packages: Ceramic (alumina); Heat sinks: Copper-tungsten; Leads: Alloy 42 with gold plating

Package Outlines

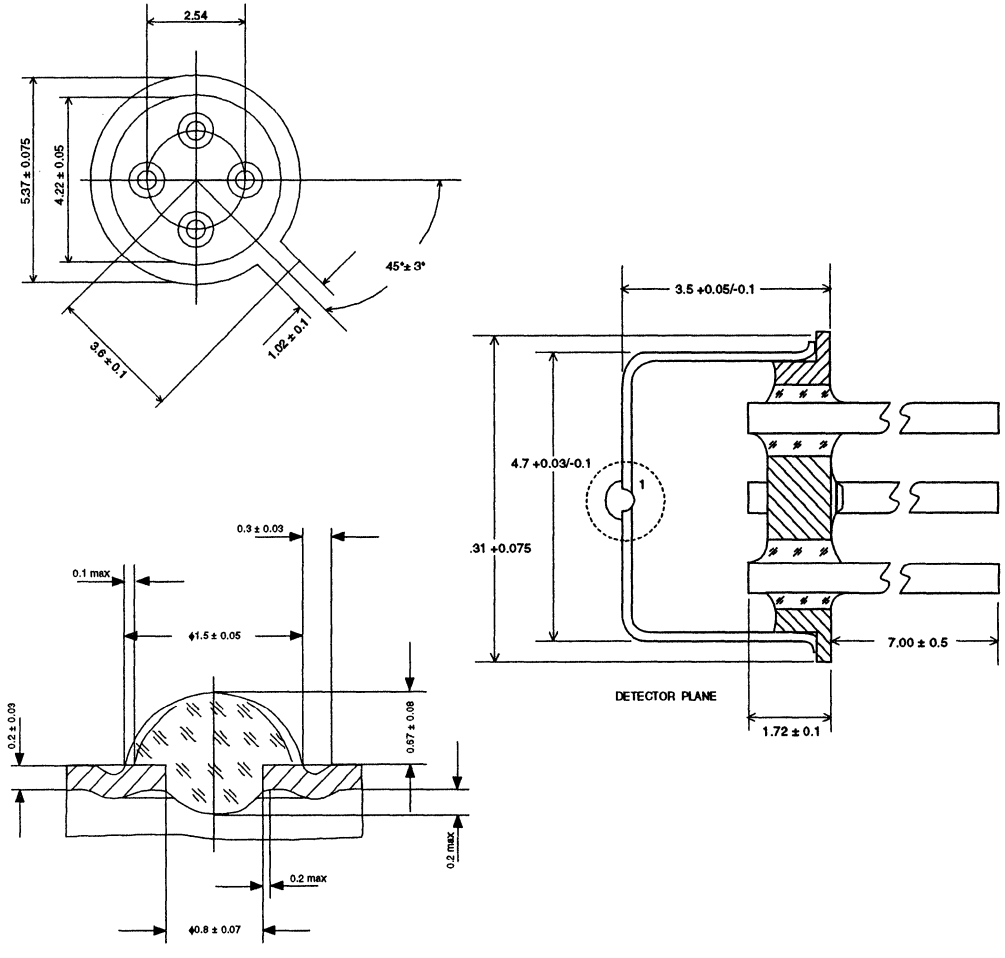
Figure 14: Mechanical Package Specifications *(5.6 mm Package)*



Note: All measurements in mm

Package Outlines

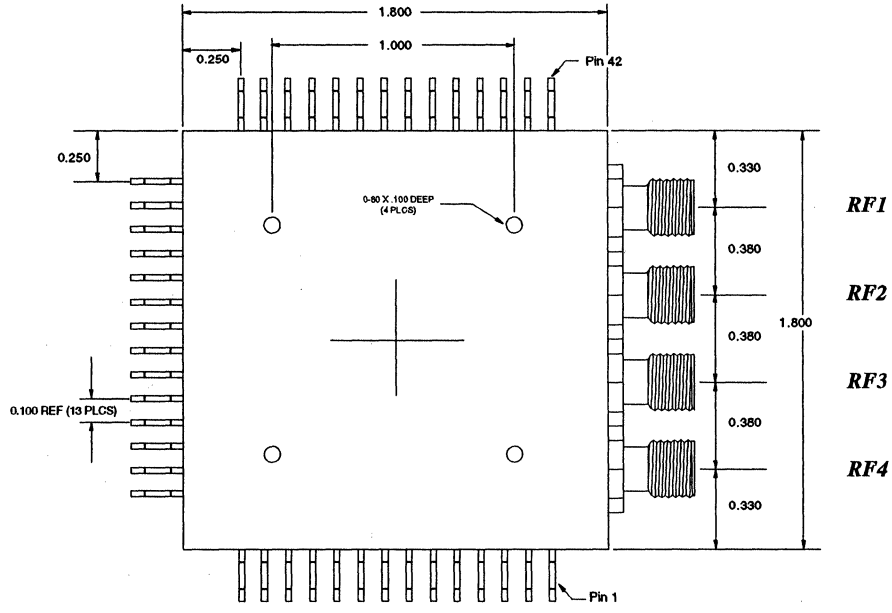
Figure 15: Mechanical Package Specifications (TO-46 *Ball Lens Package)*



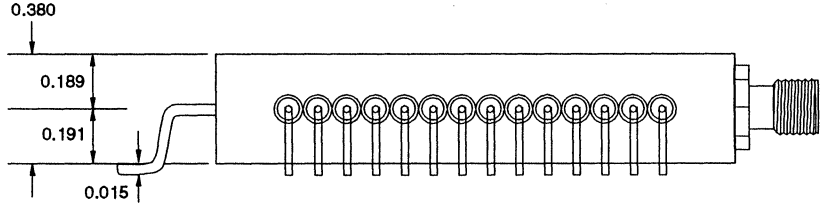
Package Outlines

Figure 16: VSC8071/8072 Module

Heat Sink Side



Module Side View

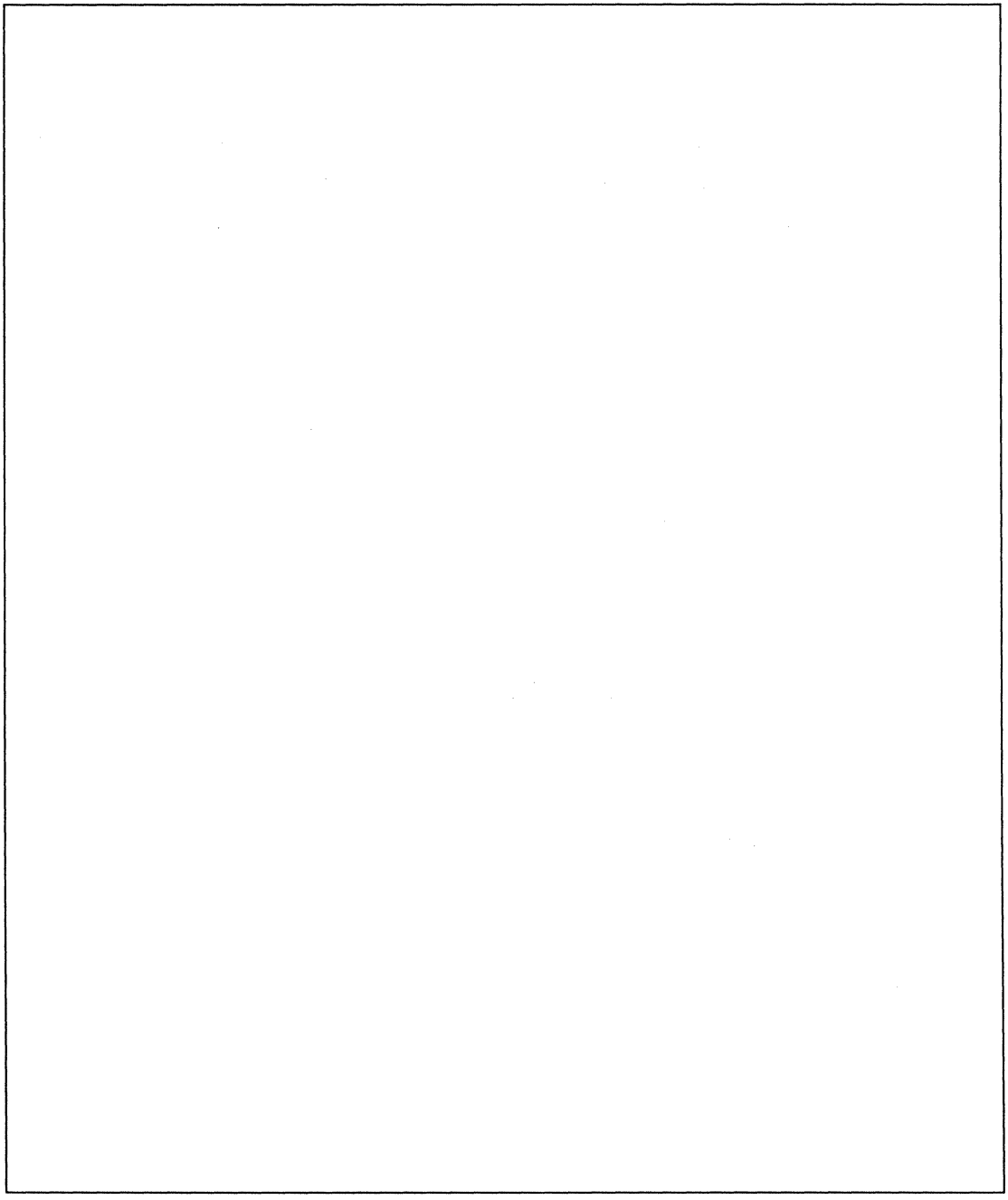


Product Summary

Product Family	Description	Features
GLX Family	Manufactured using latest generation H-GaAs IV technology to achieve lowest power solution. Ideal for cost sensitive applications in communications, ATE/instrumentation, and computers. Masterslice architecture accommodates embedded megacells.	• 25,000-250,000 Gates (raw) • Sea-of-Gates Architecture • Embedded SRAM, Register Files, PLL and Verniers • ECL, PECL, TTL, GTL, and HSTL Signal Levels • 0.5µ H-GaAs IV MESFET Process • Can Operate from Single 3.3V Power Supply • Full Speed and Half Power Macrocells • Power Management Slashes Power in Low Frequency Blocks • 2-Input NOR Delay (Typical): 37 ps (Unloaded) @ 0.1 mW of Power
FX Family	Highest integration and performance capable of 800 MHz in a sea of gates architecture. Ideal for applications requiring very high speed, low power digital logic at high levels of integration. Masterslice architecture makes FX ideal for applications requiring embedded megacells.	• 20,000-350,000 Gates (raw) • Sea-of-Gates Architecture • Embedded SRAM, Register Files, PLL and Verniers • ECL, PECL, and TTL • MIL-STD-883 Screening Available • 0.6µ H-GaAs III MESFET Process • 2-Input NOR Delay (Typical): 37 ps (Unloaded) @ 0.2 mW of Power
Viper Family	Low cost performance arrays. Ideal for 75 MHz to 700 MHz commercial applications.	• 7,000-20,000 Usable Gates • Sea-of-Gates Architecture • Industry Standard Plastic Packaging • ECL, PECL, and TTL Signal Levels • 2-Input NOR Delay (Typical): 44 ps (Unloaded) @ 0.2 mW of Power
SCFX Family	High performance SCFL/DCFL combination arrays optimized for high speed designs up to 3.0 GHz. Ideal for semi-custom telecommunications and data communications applications.	• 5,000-18,500 Usable Gates • Sea-of-Gates Architecture • Embedded SRAM, Register Files and PLLs • ECL, PECL, TTL, CML, and LVDS • 0.6µ H-GaAs III MESFET Process • DCFL 2-Input NOR Delay (Typical): 37 ps
Fury Family*	Balanced speed and power for performance better than ECL solutions at a fraction of the power. Ideal for low power, performance logic applications. Highest I/O to gate ratio.	Fury Family*

**Not Recommended for New Designs*

Product Summary



Vitesse ASIC Design Kit

Vitesse ASIC designs are supported on Mentor, Synopsys, Cadence, and Viewlogic platforms. Cadence includes support for Concept and Composer Schematic Capture. LASAR is the Sun/HP-based "Golden Simulator" supplied with every Vitesse design kit to verify the functional and AC performance of the design by accounting for on-chip timing variations. Macrocell libraries for the MOTIVE™ timing verifier from Quad Design are also available. The Vitesse Design Kit allows a designer to perform schematic capture, functional simulation, front-annotated timing simulation, electrical rule checks, and back-annotated simulation after place and route. To facilitate floorplanning and block pre-placement, Vitesse has developed an interactive graphical pre-placement tool, VSCDP, that runs in the X Windows™ environment. Cadence place and route tools are used for physical implementation at Vitesse.

CAE/EDA Tools

Vendor	*Tool*	*Function*
Mentor	Design Architect	Schematic Capture
	Quicksim II	Gate Level Simulation
Cadence	Composer	Schematic Capture
	Concept	Schematic Capture
	Verilog-XL	Gate Level & Behavioral Simulation
	Gate Ensemble	Place & Route
ViewLogic	ViewDraw	Schematic Capture
	ViewSim	Gate Level Simulation
	ViewTime (Motive)	Timing Verification
Synopsys	Design Compiler	Logic Synthesis
Teradyne	LASAR	Gate Level and Fault Grading Simulation
QUAD Design	Motive	Static Timing Verification

Application Specific Integrated Circuits

GLX, FX, VIPER, SCFX, FURY Gate Arrays

Because our customers have varying needs and different levels of gate array design experience, Vitesse offers several implementation options. These options range from a completely customer designed chip to a turn-key implementation based on mutually agreed upon specifications. In all cases, Vitesse implementation engineers are assigned to answer questions and track the progress of the design from start to finish. In addition, the following steps are normally performed by Vitesse engineers for all designs:

- Placement and routing of the design
- Net-length extraction
- Fan-out and metal delay calculation
- Final design rule checking and layout versus schematic verification

Through experience with many gate array designs, Vitesse has created a design automation framework and a well-defined flow for smooth implementation of customer designs. The flowchart at left summarizes the typical gate array project flow and breaks down the tasks as they are typically delegated to the customer or to Vitesse.

ASIC Design Training Course

Design classes are provided to help the customer understand the design methodology and tools utilized in the gate array design process. These classes are recommended for all customers planning to implement a design in a Vitesse gate array. Training can be provided at the Vitesse facility or at the customer's site.

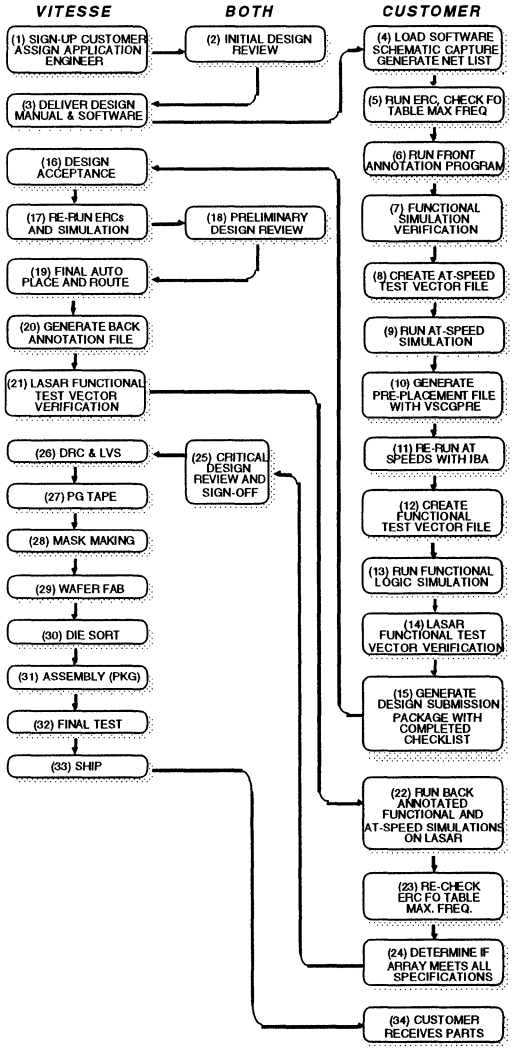
This introduction to semicustom digital high performance VLSI design prepares designers to implement circuits using high speed enhancement/depletion mode gallium arsenide technology. The intensive three-day course covers all phases of gate array design, including the design methodologies and tools specific to the design of VLSI semicustom GaAs ICs. After completing the course, the attendee will be able to design high performance circuits with minimum consultation. In addition, a complete overview of related topics which impact circuit design, including wafer fabrication, test, assembly, and packaging will be presented.

Schedule of Course Dates:

- Monday - Wednesday, August 12-14, 1996
- Monday - Wednesday, November 4-6, 1996
- Monday - Wednesday, February 3-5, 1997
- Monday - Wednesday, May 5-7, 1997
- Monday - Wednesday, August 4-6, 1997
- Monday - Wednesday, November 3-5, 1997

Implementing Vitesse Gate Arrays

Figure 1: Gate Array Project Flow



Application Specific Integrated Circuits

GLX, FX, VIPER, SCFX, FURY Gate Arrays

GLX, FX, SCFX Masterslice Arrays

Application Specific Integrated Circuits

Features

- Combines the Power of Megacells with the FX, SCFX or GLX Macrocell Library
- 20,000-350,000 Raw Gates, Channeless Architecture
- Sea-of-Gates Architecture and Four Layer Metal for High Density
- Embedded Megacells Including:RAM, Register Files, Verniers, Counters, and PLLs
- Data Sheets Available for all Megacells
- RAM Compiler to Create Optimized RAM
- ECL, PECL, and TTL Signal Levels
- Optional Fixed Clock Distribution Scheme to Minimize Clock Skew
- Commercial & Industrial Temperature Ranges

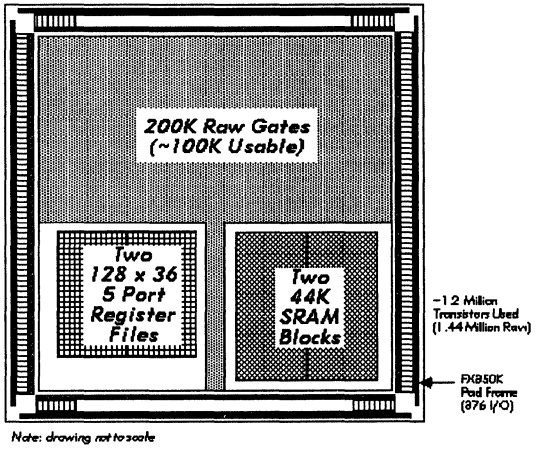
Description

FX, SCFX, and GLX gate arrays are available in Masterslice format with embedded full-custom megacells. Masterslice arrays combine the power of megacells with the flexibility of the FX, SCFX or GLX macrocell library. Depending upon the size of the megacell and the product, Masterslice arrays may incorporate in excess of 300,000 raw gates. As with all standard arrays, these products combine >1 GHz performance with integration levels comparable to BiCMOS gate arrays.

The masterslice approach provides simple integration of custom megafunctions onto the array, allowing the user to solve application specific requirements that cannot be effectively implemented in the sea-of-gates logic.

Typical megacells include RAM, register file, and custom data path blocks. In addition, Vitesse has developed megacells specifically designed to solve difficult timing problems in applications such as telecommunication, data communication, and ATE/instrumentation. These cells include PLLs, timing verniers, and very high-speed counters.

Masterslice Array



Note: drawing not to scale

ASICs

GLX Family Gate Arrays

Application Specific Integrated Circuits

Features

- Five Array Sizes: 15K, 40K, 80K, 120K and 220K Raw Gates
- Low-Power H-GaAs IV, 0.4µ, 4-Layer Metal, Technology
- Operates from either a single +3.3V Power Supply or Reduced Supply Voltages to Conserve Power
- Industry Standard Plastic Molded Packages
- Low-Power Macros Available
- Standard TTL, LVTTL, ECL, LVPECL, GTL, HSTL and LVDS I/O Compatibility
- Compatible With Standard TTL or ECL System Power Supplies
- Superior Speed/Power Performance:
- - Typical gate delay: 130 ps @110µW *(unbuffered 2-in NOR, F.O. = 2,0.13 mm wire)*
  - Typical gate delay: 140 ps @ 330µW *buffered 2-in NOR, F.O. = 2,0.5 mm wire)*

Description

The GLX series is a family of high performance, low power gate arrays based on the fourth generation, 0.4µ, 4-layer metal, HGaAs-IV process. GLX utilizes a sea-of-gates architecture and can be powered from 2.0V or 3.3V power supplies. The family consists of five members ranging from 15,000 raw gates to 220,000 raw gates with a utilization factor of up to 70%. GLX delivers both the lowest power per gate and the lowest price per gate of any high performance ASIC product family. All GLX macrocells are available in either full speed (110µW per gate) or half power (65µW per gate) versions. Power dissipation is independent of operating frequency. By combining the cost benefits of a high yielding process, reduced die sizes, and low cost thermally enhanced plastic packaging, GLX provides a low cost solution for applications requiring performance beyond the capabilities of CMOS.

Array Specific Features

Array Name	# of Internal Gates		# of Input Cells	# of I/O Cells	Total Signal Pins	Package Options
	Usable Gates	D Flip-Flops				
GLX15K	10K	1.0K	35	52	87	128 PQFP
GLX40K	26K	2.6K	35	76	111	160 PQFP
GLX80K	48K	4.8K	31	104	135	208 PQFP
GLX120K	72K	7.2K	31	120	151	240 PQFP
GLX220K	110K	11.0K	31	156	187	XXX BGA

FX Family Gate Arrays

Application Specific Integrated Circuits

Features

- 10,000-350,000 Raw Gates, Channeless Architecture
- Sea-of-Gates Architecture and Four Layer Metal for High Density
- 0.6µ H-GaAs III MESFET Process
- Multiple Buffering Options for Optimal Speed-Power Solution
- Optional Fixed Clock Distribution Scheme to Minimize Clock Skew
- MIL-STD-883 Screening Available
- Commercial, Industrial, Extended and Military Temperature Ranges
- ECL, PECL, and TTL Signal
- Array Performance
  - Typical gate delay: 97 ps @ 0.19 mW *(unbuffered 2-in NOR, F.O. = 1, 0.17 mm wire)*
  - Typical gate delay: 95 ps @ 0.59 mW *(buffered 2-in NOR, F.O. = 3, 0.51 mm wire)*

Description

The FX family consists of 8 products ranging from 10,000 to 350,000 raw gates. These arrays combine >1 GHz performance with integration levels comparable to BiCMOS gate arrays.

The FX family is manufactured in the production proven H-GaAs III process, and incorporates a channeless architecture allowing the first layer of metal to be routed over unused cells. This architecture eliminates the need for pre-defined channels, allowing much greater density and flexibility in design, resulting in superior performance.

Because power dissipation is frequency-independent in H-GaAs technology, FX arrays have power dissipation levels comparable to or lower than similar density BiCMOS arrays at frequencies above 50 MHz. Custom master-slices are also available to incorporate functions such as SRAMs and multiport register files into FX arrays.

FX arrays are ideal for mainframe computers, workstations, communications equipment and other systems requiring very high speed, low power digital logic at high levels of integration.

Array Specific Features

Array Name	# of Internal Gates			# of Input Cells	# of I/O Cells	Total Signal Pins	Package Options
	Total Raw Gates	Usable Gates	D Flip-Flops				
VGFX10K	10K	7K	790	7	24	31	52 PQFP
				31	40	71	100 PQFP
				13	24	37	52 LDCC
VGFX20K	20K	10K	1K	39	52	91	132 PGA, 132 LDCC, 144PQFP
VGFX40K	42K	21K	2.1K	40	99	139	195 PGA
	38K	19K	1.9K	36	99	135	208 PQFP
VGFX100K	100K	50K	5K	73	100	173	211 PGA
				91	100	191	256 LDCC
VGFX150K	188K	75K	8K	99	156	255	344 LDCC
VGFX200K	220K	110K	11K	83	172	255	415 PPGA
VGFX350K	350K	175K	17.5K	107	218	325	557 PPGA
VGFX350KE	350K	175K	17.5K	127	250	377	557 PPGA

VIPER Family Gate Arrays

Application Specific Integrated Circuits

Features

- 7,000-13,000 Usable Gates, Channeless Array Architecture
- Industry Standard Plastic Packaging
- Superior Speed/Power Performance and Cost Comparable to BiCMOS
- Production-Proven H-GaAs III Enhancement/ Depletion MESFET Process
- ECL, PECL, TTL, or Mixed Inputs/Outputs
- Array Performance
  - Typical gate delay: 118 ps @ 0.19 mW *(unbuffered 2-in NOR, F.O.= 1, 0.17 mm wire)*
  - Typical gate delay: 116 ps @ 0.59 mW *(buffered 2-in NOR, F.O.= 3, 0.51 mm wire)*
- Robust Clock Distribution Scheme for Minimized Clock Skew
- Multiple Buffering Options for Optimal Speed/ Power Solution

Description

The VIPER family of gate arrays provides the best cost-per-function solution for system applications between 50 and 700 MHz. By combining the high performance of H-GaAs technology with the low cost of molded-plastic packages, VIPER delivers two to three times the performance of BiCMOS at comparable cost. This allows the designer to implement much simpler architectures to achieve performance targets. As with all Vitesse ASIC products, VIPER arrays are compatible with industry-standard TTL, ECL, and pseudo-ECL (PECL) signal levels, and utilize standard power supplies.

The VIPER family is manufactured in the production proven H-GaAs III process, and incorporates a channeless architecture allowing the first layer of metal to be routed over unused cells. This architecture eliminates the need for pre-defined channels, allowing much greater density and flexibility in design, resulting in superior performance.

VIPER arrays are ideal for applications at 50 MHz or higher. The performance advantage of VIPER over BiCMOS enables system designers to consider simpler architectural alternatives, such as serializing data streams and eliminating pipeline stages.

Array Specific Features

Array Name	# of Internal Gates		# of Input Cells	# of I/O Cells	Total Signal Pins	Package Options
	Usable Gates	D Flip-Flops				
VGLC10K	7K	700	7	24	31	52 PQFP (1)
	7K	700	31	40	71	100 PQFP (2)
VGLC12K	10K	1K	39	52	91	144 PQFP (3)
VGLC15K	13K	1.3K	36	99	135	208 PQFP (3)

(1) EIAJ footpring, 14 x 14 mm body size, thermally enhanced package.
(2) EIAJ footprint, 14 x 20 mm body size, thermally enhanced package.
(3) EIAJ footprint, 28 x 28 mm body size, thermally enhanced package.

SCFX Family Gate Arrays

Application Specific Integrated Circuits

Features

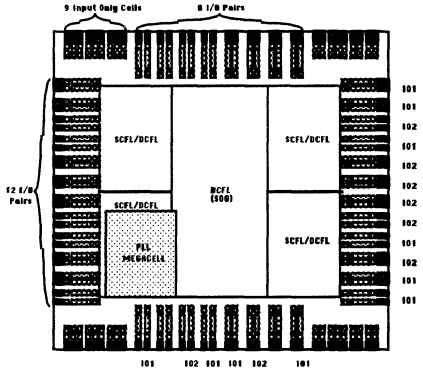
- Tailored Specifically for High Performance Telecommunications and Data Communications Applications. 2.5 GHz Performance.
- Ideal for Serialization/Deserialization
- 5,000-18,500 Usable Gates
- Combination of High Speed SCFL and Low Power DCFL Cells
- Flexible Allocation of SCFL Resources
- Embedded SRAM, Register Files and PLLs
- 0.6µ H-GaAs III MESFET Process
- Phase-Locked Loop Megacells Available:
  - 155/622 MHz SONET STS-3/STS-12
  - 1.0625 GHz Full Speed Fibre Channel
- DCFL 2-Input NOR Delay (Typical): 37 ps (Unloaded) @ 0.2 mW of Power
- DCFL D Flip Flop Toggle Rate: >1.6 GHz
- SCFL D Flip Flop Toggle Rate: >5.0 GHz
- TTL, ECL, PECL, VECL, CML, SCFL, and LVDS Signal Levels
- Low Cost Industry Standard Plastic Molded Packages and TBGAs

Description

The SCFX family of gate arrays provides solutions for high speed designs ranging from 50 MHz to 2.5 GHz. SCFX arrays offer a unique capability by combining very high speed SCFL logic with low power DCFL logic, for an optimum speed-power solution.

SCFX arrays are compatible with industry-standard TTL, ECL, and pseudo-ECL (PECL) signal levels, and utilize standard power supplies.

SCFX arrays are available as masterslice arrays with embedded megacells such as RAMs, Register Files, and Phase-Locked-Loops, making SCFX ideally suited to telecommunications, data communications, signal processing, instrumentation, and clocking applications.



Array Specific Features

Array Name	# Of Internal Gates			# Of Signals			Package Options
	Raw DCFL in Center	Usable DCFL per quadrant	Usable SCFL PER quadrant	# of Input Cells	# of I/O Cells	Total Signal Pins	
SCFX 10K	2600	876	34	3	24	27	52 PQFP
				27	40	67	100 PQFP
SCFX 40K	15748	2286	99	35	80	115	184PQFP 192TBGA

FURY Family Gate Arrays

Application Specific Integrated Circuits

Features

- Up To 30, 500 Equivalent Gates, Channeled Architecture
- MIL-STD-883C, Level B Screening and Qualification Available
- ECL and TTL Signal Levels
- Commercial, Industrial, and Military Temperature Ranges
- Array Performance
  - D Flip-flop Toggle Rates: >1 GHz
  - Typical Gate Delay: 144 Ps @ 1.1 mW *(2-input NOR, F.O. = 3, 1.5 mm wire)*
  - ECL Inputs/Outputs at 650 MHz
  - TTL Inputs/Outputs at 100 MHz
- Multiple Buffering Options for Macrocells

Description

The FURY family of gate arrays consists of five products ranging from 3,500 to 30,500 equivalent gates. These ASICs are ideally suited for systems which require high density, state-of-the-art performance while maintaining low power dissipation. These arrays interface with TTL and ECL technologies without additional system requirements. The FURY family offers speed performance equal to or better than leading edge ECL gate arrays, while dissipating only 1/3 to 1/4 of the power. This can add up to substantial cost savings in overall cooling requirements.

The FURY family of gate arrays can be used in such applications as computers, communications, test, and general instrumentation. This family of high performance semi-custom products is ideally suited for systems requiring very high speed, low power digital logic at high levels of integration.

Array Specific Features

Array Name	# of Internal Gates			# of Input Cells		# of Output Only Cells	Total Signal Pins	Package Options
	Total Raw Gates	Usable Gates	D Flip-Flops	TTL, ECL	Hi-Drive			
VSC3K	3.5K	3.5K	290	40	4	52	92	52 LDCC, 132 LDCC, 132 PGA
VSC5K	6.4K	6.4K	520	52	4	68	120	149 PGA, 164 LDCC
VSC10K	13.4K	13.4K	1.1K	74	8	100	174	211 PGA
				96	8	100	196	256 LDCC
VSC15K	16.9K	16.9K	1.4K	74	8	100	174	211 PGA
				96	8	100	196	256 LDCC
VSC30K	30.5K	30.5K	2.5K	100	8	156	256	344 LDCC

Not Recommended for New Design

Application Note 1

Printed Circuit Board Considerations

Introduction

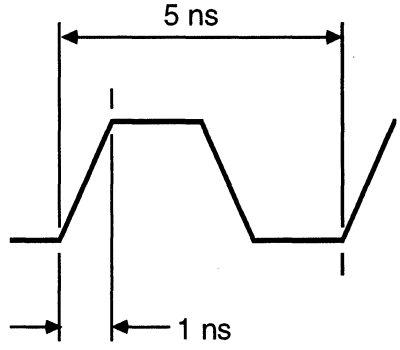
Several important considerations must be taken into account when high speed GaAs (or ECL) ICs are interconnected on printed circuit boards. Chief among them is the need to properly terminate signal trace interconnections and the maintenance of low impedance ground and power supply connections.

This application note reviews some of the popular design techniques which are utilized to insure the integrity of high frequency signals on a printed circuit board. While these techniques have been used in ECL systems for some time, they may not be familiar to designers accustomed to CMOS circuits.

In general, signal traces on circuit boards should be treated as transmission lines if the propagation delay of the trace is more than one-tenth of the rise time of the signal. In the event that the propagation delay of the trace is short with respect to the rise time of the signal, any reflections caused by unterminated transmission lines are masked during the relatively slow transition and are not seen as overshoot or ringing.

Because most CMOS circuits have a high ratio of signal rise time to trace propagation delay, several inches of unterminated signal trace can be used without signal distortion. Since edge speeds in GaAs components are faster, the trace lengths must be considered as transmission lines and must be terminated properly to retain signal integrity.

Figure 1: 200 MHz Signal



Why Are Properly Terminated Transmission Lines Needed?

Rapidly changing signals require fast edge rates. A 200 MHz 50% duty cycle clock signal, for example, has a total period of 5ns. This period must accommodate a rise time, a fall time and some pulse width duration. As seen in Figure 1, this signal can result in rise and fall times of approximately 1ns because of the desire to maintain the pulse signal integrity. Since GaAs circuits are designed to support signal rates beyond 200 MHz, both ECL compatible and'native' GaAs compatible output drivers are designed for sub-nanosecond rise and fall times.

Such fast rise and fall time signals require that board signal traces are terminated transmission lines. Anytime that the propagation delay of a signal trace is longer than one-tenth the rise or fall time of the signal, an unterminated trace will result in voltage reflections which can cause degradations in the signal integrity.

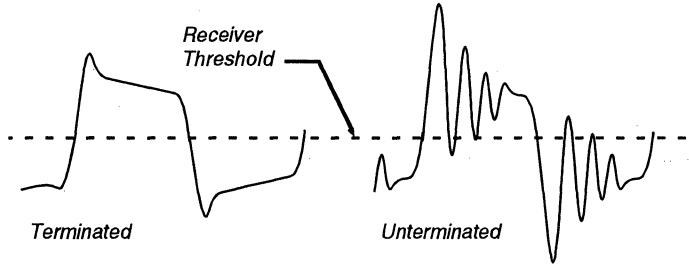
Figure 2 shows the difference in signals observed in terminated and unterminated environments. As seen, unterminated signal lines can result in substantial overshoot and ringing which are caused by voltage reflections.

Printed Circuit
Board Considerations

Application Note 1

These voltage reflections can cause a ringing signal which can be interpreted as several faster signals by the receiver. Terminated transmission lines eliminate voltage reflections and therefore produce clean waveforms. Generally, signals with sub-nanosecond rise and fall times must be terminated if the signal trace length is longer than 0.5 in. This is because the propagation velocity of a typical signal trace is approximately 2ns/ft.

Figure 2: Signals at Terminated and Unterminated Signal Traces



Transmission Line Theory

Transmission line theory is important to an understanding of the methods used to terminate GaAs signal lines. Figure 3 shows a signal trace with typical loads at both ends. Usually, the signal trace delay is long when compared with the signal rise or fall time and reflections will appear at their full amplitude. The output voltage swing at point A, (V_A), is given by:

$$V_A = (V_{int})\left[\frac{Z_O}{R_O + Z_O}\right]$$

where V_{int} is the internal voltage swing, R_O is the chip output impedance and Z_O is the line impedance.

Since R_O is small compared to the line impedance, the output swing is nearly the same as the internal transition. The internal swing is approximately 1.4 V and the typical output swing is 1.3 V. The signal propagates down the line and is seen at point B some time, T_{pd}, later. The voltage reflection coefficient at the load end of the line, rc, is a function of the line characteristic impedance and the load impedance and is given by:

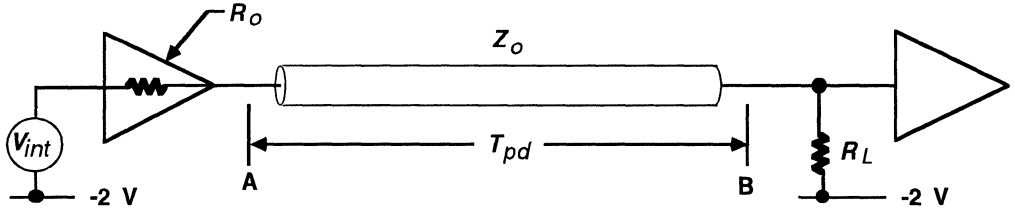
$$rc = \frac{(R_L - Z_O)}{(R_L + Z_O)}$$

where R_L is the termination load resistance and Z_O is the line impedance (both in ohms). If $R_L = Z_O$, there is no reflection. For any value of R_L close to Z_O, the reflection is small.

Application Note 1

Printed Circuit Board Considerations

Figure 3: Parallel Terminated Line Model



Practical Transmission Lines

The key to maintaining signal integrity in practical high frequency digital systems is the utilization of properly terminated, controlled impedance transmission lines. Controlled impedance transmission lines can be realized in several ways. For signal transmission over long distances, coaxial cables or twisted pairs are popular. Some common types of coaxial cable have characteristic impedances of 50, 75, 93 or 125 ohms. Twisted pairs can be made from AWG 24-28 hook-up wire twisted about 30 turns per foot. Such twisted pairs have a characteristic impedance of about 110 ohms.

For signal transmission within a circuit board, Striplines and Microstrip lines are usually used. A Microstrip line is shown in Figure 4. It is constructed with a strip conductor for the signal line separated from a ground plane by a dielectric. The signal line is made by etching away the unwanted copper using photoresist techniques. If the thickness, width of the line, and the distance from the ground plane are controlled, the line will exhibit a predictable characteristic impedance that can be controlled to within 5%. The characteristic impedance, Z_O, of a Microstrip Line can be approximated by:

$$Z_O = \frac{87}{\sqrt{e_r + 1.41}} \ln\left[\frac{5.98h}{0.8w + t}\right]$$

where e_r is the relative dielectric constant of the board material (which is typically 5 for FR-4 fiber-glass epoxy boards), and w, h and t are the dimensions indicated in Figure 4 in inches.

Figure 4: Microstrip

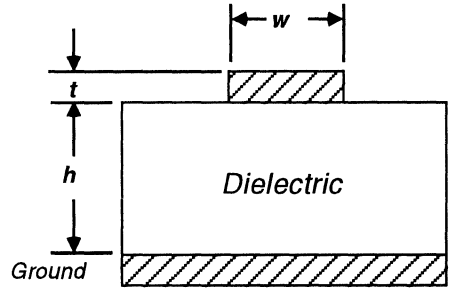
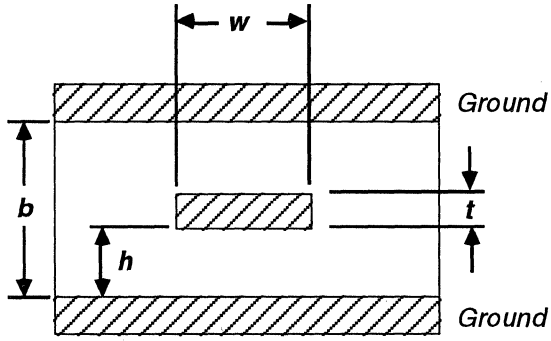


Figure 5: Stripline



The propagation delay of the line may be approximated by:

$$T_{pd} = 1.017\sqrt{0.475\,\varepsilon_r + 0.67}\ ns/ft$$

Note that the propagation delay of the line is dependent only on the dielectric constant and is not a function of line width or spacing. For FR-4 fiber-glass epoxy boards, the propagation delay of the Microstrip line is approximately 1.8 ns/ft.

A Stripline is shown in Figure 5. It consists of a copper ribbon centered in a dielectric medium between two conducting planes. If the thickness and width of the line, the dielectric constant medium, and the distance between the ground planes are all controlled, the line will exhibit a characteristic impedance that can be held constant within 5%. The characteristic impedance of a Strip Line is given by:

$$Z_O = \frac{60}{\sqrt{\varepsilon_r}} \ln\left[\frac{4b}{0.67\pi w\,(0.8 + t/w)}\right]$$

where ε_r is the relative dielectric constant of the medium and b, t, and w are the dimensions shown in Figure 3. This equation proves accurate for:

$$\frac{w}{(b - t)} < 0.35 \text{ and } \frac{t}{b} < 0.25$$

and the propagation delay of the line is:

$$t_{pd} = 1.017\sqrt{\varepsilon_r}\ ns/ft$$

For FR-4 fiber-glass epoxy, the propagation delay of the Stripline is about 2.27 ns/ft. Note that in both Striplines and Microstrip, the propagation delay is not a function of the width or spacing.

Application Note 1

Printed Circuit Board Considerations

Parallel Terminated Lines

Parallel terminated lines such as the one shown in Figure 3 are used for fastest circuit performance. Standard output drivers on Vitesse's GaAs products can drive 50 ohm lines. ASIC products also allow for up to 25 ohm drive capability. In each case the term "line" refers to a signal transmission line, terminated at the receiving end through a resistor of the characteristic line impedance to -2 Volts. With parallel terminated lines, the line termination supplies the output pull-down current for the open source-follower output FET. Thus, no other pull-down resistor is required at the output of the driving gate.

Power Distribution

Power distribution is an important factor in system design. The loss of noise margin dueto reduced power supply voltage or noise on the power supply lines means a reduction in the circuit tolerance to crosstalk and ringing. Points to consider for overall system operation include total circuit and termination power, voltage drops on the power busses, and noise induced on the power distribution lines by the circuits and by external sources.

Vitesse GaAs circuits are designed to interface with each other over a power supply voltage range of ± 5% from the nominal -2 Volts without a loss of noise margin. However, if two chips are at different supply voltages or on the same power supply with a voltage offset between them, there will be a predictable loss of noise margin.

The main causes of V_{TT} power supply offsets between circuits are:

- Inadequate power busses to handle the necessary current
- Separate supplies with common positive terminals at slightly different potentials
- Separate positive grounded supplies with an inadequate number of interconnection ground bus bars

Power supply requirements for Vitesse GaAs circuits must take into account the fact that a 50 ohm ECL compatible output sources about 22 mA in a logic HIGH state and no current in a logic LOW state. The 22 mA differential between the two states can produce a significant power supply current fluctuation. Such an effect should be considered when specifying the power supply.

Current fluctuations are by no means insurmountable. Brief current changes are smoothed by bypass capacitors at the power supplies. Also, the typical 50% distribution of output logic levels (e.g., HIGH and LOW states) tends to minimize current changes.

High frequency noise and ripple from the power supply should be avoided. These effects produce differences in voltage levels among sections of a system and lead to loss of noise margin. As a rule of thumb, noise can be considered "high frequency" whenever the mean wave length of the noise (in units of time) is not more than 2 times greater than the propagation delay of the longest power line. For implementations which use GaAs ICs, it is recommended that high frequency power supply noise be held to under 25 mV of total signal variation.

When multiple power supplies are used, the positive terminals should be connected together with a large bus and the output voltages maintained as equal as possible. It is desirable to keep the power supply levels within 25 mV of one another.

To achieve the requirements imposed by GaAs circuits on power supply distribution, printed circuit boards with large ground and power planes are commonly used. Power supply bypass capacitors are used on the circuit boards to handle the current transients required by the outputs.

Printed Circuit Board Considerations

Application Note 1

Typically, a 1 to 10 microfarad capacitor is placed on the board at the power supply inputs and a 0.1 to 0.01 microfarad capacitor is connected between ground and -2 V on every VTT package pin. RF type capacitors are recommended because of their low inductance.

Application Note 2

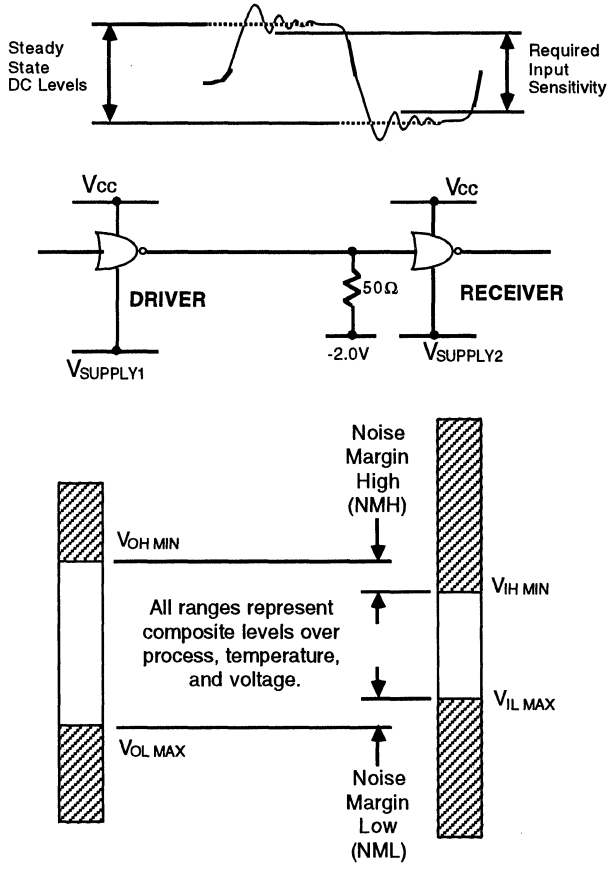
Interfacing GaAs Products to ECL/TTL I/O

Introduction

Vitesse GaAs products are designed to interface to external circuits with standard ECL and TTL signal levels. In some cases, however, slight differences exist between the signal levels produced by these compatible parts and actual silicon ECL or TTL components.

Although Vitesse components use GaAs DCFL circuitry internally, the I/O is designed to interface directly with industry standard ECL and TTL levels. In addition, the FURY Series of gate arrays, the VCB50K Standard Cells and the VS12G476 4K SRAM can send and receive signals at Vitesse's own internal GaAs levels, thus allowing one device to "talk" directly to another device with no translation delays. Figure 1 shows the model used to specify system noise margins.

Figure 1: Noise Margin Model



Interfacing GaAs Products to ECL/TTL I/O

Application Note 2

ECL I/O

Industry standard ECL I/O signal levels are based on voltage levels that result naturally from the characteristics of bipolar logic families. In order to interface with standard ECL logic, Vitesse components use buffered level translators at the input and output pads. The input translator consists of a differential current switch which drives a level shifter. The reference voltage for the differential pair can be provided in one of three ways:

1. Internal Reference

This option uses the internal reference on the chip. No additional pins are required. Noise margins for this scheme are shown in Table 1.

2. External Band-Gap Diode

This option is shown in Figure 2 and involves the use of an LM185 diode in conjunction with a gate array or standard cell product. The user must connect the LM185 to the external reference pin on the GaAs device. Use of the external diode reference provides improved input noise margins (see Table 2) over a wider VTT range of -2.0V ± 10%.

Figure 2: External Band-Gap Diode Reference

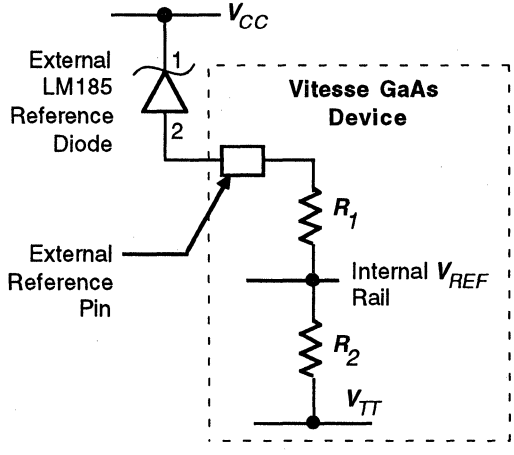


Table 1: ECL Noise Margins Using the Internal Reference

Noise Margin	*ECL Device Driving Vitesse Device*		*Vitesse Device Driving ECL Device*	
	ECL 100K	*ECL 10KH*	*ECL 100K*	*ECL 10KH*
HIGH	75 mV	80 mV	145 mV	150 mV
LOW	80 mV	60 mV	145 mV	140 mV

Application Note 2

Interfacing GaAs Products to ECL/TTL I/O

Table 2: ECL Noise Margins Using an External Diode Reference

Noise Margin	ECL Device Driving Vitesse Device		Vitesse Device Driving ECL Device	
	ECL 100K	ECL 10KH	ECL 100K	ECL 10KH
HIGH	100 mV	105 mV	145 mV	150 mV
LOW	110 mV	90 mV	145 mV	140 mV

Table 3: ECL Noise Margins Using a Full External Reference

Noise Margin	ECL Device Driving Vitesse Device		Vitesse Device Driving ECL Device	
	ECL 100K	ECL 10KH	ECL 100K	ECL 10KH
HIGH	140 mV	145 mV	145 mV	150 mV
LOW	145 mV	125 mV	145 mV	140 mV

Notes: (1)Worst case noise margins over nominal conditions.
(2)Source for ECL 100K DC Characteristics: Fairchild F100K DC Family Specifications.
(3)Source for ECL 10KH DC Characteristics: Motorola MECL10KH DC Family Specifications.

3. Full External Reference

The user may provide an external reference voltage of -1.32V ± 25 mV to the external reference pin. (See table 3 for noise margins.) AN-8 discusses the creation of an external reference using the LM185.

Different but equally important issues arise when interfacing Vitesse components' output (or any "non-bipolar" ECL output) with a silicon bi-polar ECL circuit input. Figures 3 & 4 illustrate this situation. In Figure 3, an ECL input is the base of an NPN bipolar transistor whose collector is connected to VCC (0 Volts). In order not to degrade the switching characteristics of this input, it is essential that this input transistor be kept out of saturation, which means that the base collector diode must not become forward biased. This condition is assured when driving this input with a bipolar ECL output, since the emitter follower output cannot go more positive than one diode drop below VCC.

The situation is different when the output emitter follower is replaced with a FET such as in Figure 4. Vitesse's ECL output driver incorporates clamp circuitry to ensure that the output high level does not go more positive than -700mV.

One major difference between Vitesse ECL compatible outputs and silicon ECL outputs is that Vitesse outputs are "cutoff" drivers which have an output low voltage equal to the VTT supply. In this way, a logic low is also a high impedance state and several outputs can be bussed together.

Figure 3: Bipolar ECL Outputs Driving an ECL Input

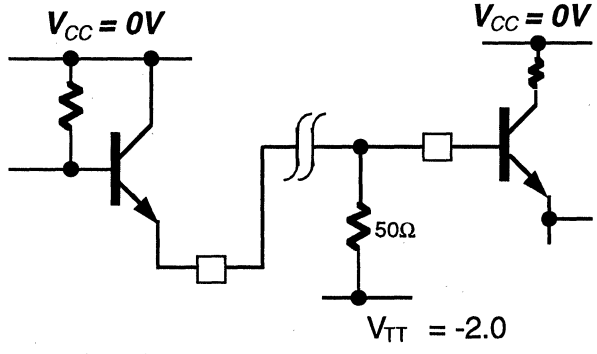
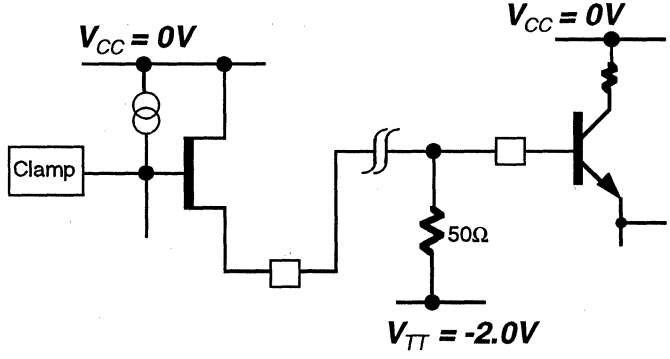


Figure 4: GaAs ECL Outputs Driving an ECL Input



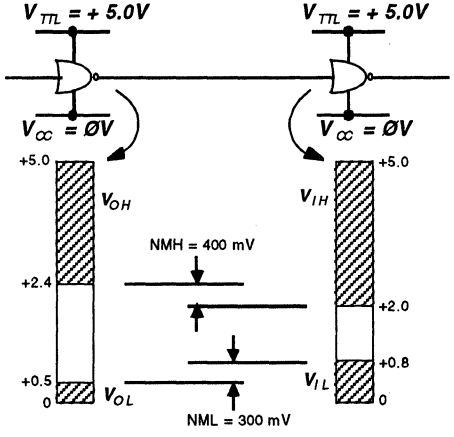
Application Note 2

Interfacing GaAs Products to ECL/TTL I/O

TTL I/O

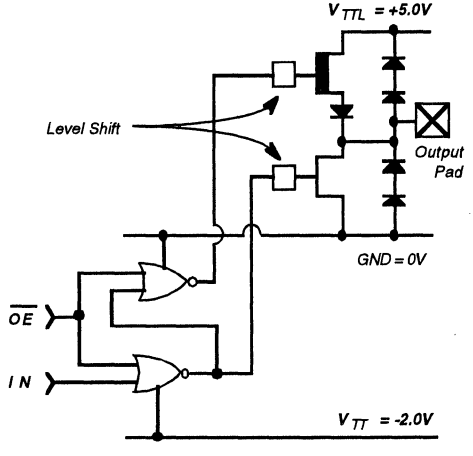
Vitesse ASICs support TTL inputs and outputs in addition to ECL I/O. The standard minimum input swing specification at a TTL input is ≥1.2 V (0.8 - 2.0 V) compared to 310 mV for ECL. Figure 5 shows the guaranteed worst case TTL I/O levels in Vitesse components. The TTL inputs source a worst case current of -500 µA.

Figure 5: Worst Case TTL I/O Levels for Vitesse Products



TTL compatible outputs impose certain constraints on the user. Figure 6 is a schematic representation of the TTL output buffer with tri-state capability.

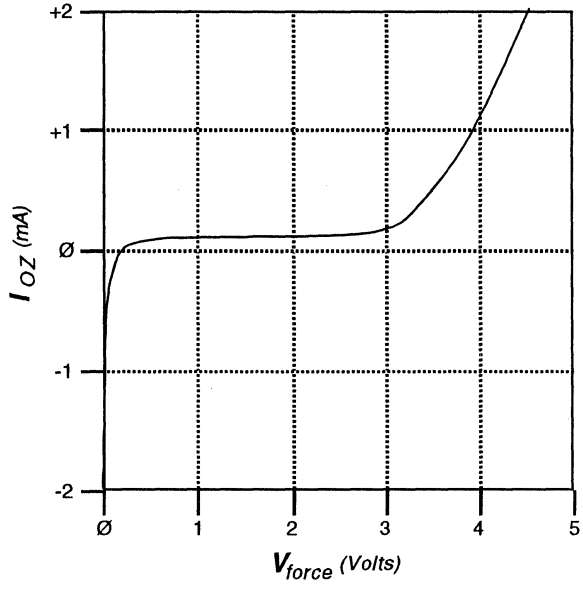
Figure 6: TTL Output Buffer Schematic



One difference between the Vitesse TTL totem-pole output and typical silicon TTL is that the high level (VOH) typically goes higher in the Vitesse output. The high level can be one diode drop below VTTL (+5.0 V), whereas in standard TTL, the output generally does not exceed 3.8 Volts. The low level (VOL) is similar to standard TTL (≥ 0.4 Volts) with the rated sinking current (8 mA).

The TTL output tri-state current voltage characteristics are also different from typical silicon bipolar devices. Figure 7 shows the TTL output tri-state I-V curve. Note that the tri-state leakage current, IOZ, shows a sharp increase near 3.5 Volts. This voltage is low, but well beyond the TTL valid high level of 2.4 Volts.

Figure 7: TTL Output Tri-State I-V Curve



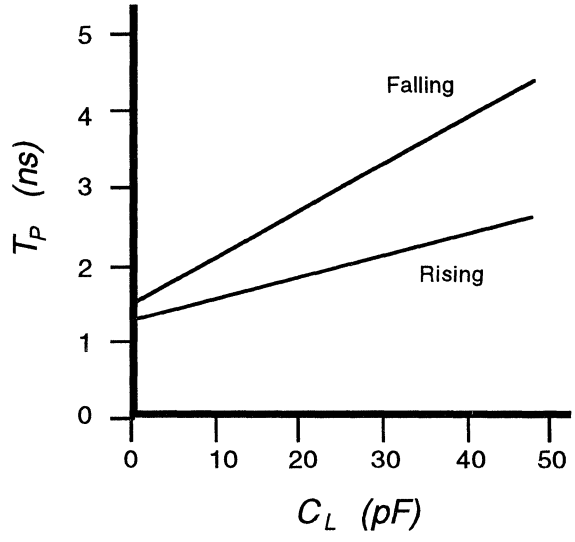
In a typical system application, there may be many TTL outputs from the Vitesse component bussed together with either CMOS or TTL open collector outputs. The output high level on the bus equilibriates at an operating point (Q point) consistent with the I-V characteristics shown in Figure 7 and the current sourcing capability of the driving device.

The output edge rates in the Vitesse TTL outputs are intrinsically fast (see Figure 8). With 30 pF capacitive load, the edge rates are about 3 ns. Handling very fast edge rates on TTL circuit boards is difficult due to the severe ringing that fast edges produce. To control the ringing on the circuit board, it is helpful to buffer the TTL outputs with a silicon bus interface chip such as the 74244.

Application Note 2

Interfacing GaAs Products to ECL/TTL I/O

Figure 8: Capacitive Loading Effect on Vitesse TTL Output Buffers



DC Specifications

The following tables (4-8) taken from the FURY Series Gate Array Design Manual are representative of all of Vitesse's GaAs devices. Tables 4, 5 and 6 give DC specifications for the ECL I/O cells using the internal reference, an external diode reference, or a full external reference, respectively. DC specifications for TTL I/Os are in Table 7. Following the tables are specified Recommended Operating Conditions and Absolute Maximum Ratings.

Table 4: DC Characteristics for ECL I/O Cells Using Internal Reference

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
V_{OH}	Output HIGH voltage	-1020	700	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
V_{OL}	Output LOW voltage	-2000	-1620	mV	
V_{IH}	Input HIGH voltage	-1100	-700	mV	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	-2000	-1540	mV	Guaranteed LOW for all inputs

Notes: (1) Over recommended operating conditions, $V_{CC} = V_{CCA}$ = GND, Output Load = 50Ω to V_{TT}

Table 5: DC Characteristics for ECL I/O Cells Using External Diode Reference

Parameters	Description	Min	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-1025	700	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
V_{OL}	Output LOW voltage	-2000	-1620	mV	
V_{IH}	Input HIGH voltage	-1125	-700	mV	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	-2000	-1510	mV	Guaranteed LOW for all inputs

Notes: (1) Over recommended operating conditions, $V_{CC} = V_{CCA}$ = GND, Output Load = 50Ω to V_{TT}

Table 6: DC Characteristics for ECL I/O Cells Using Full External Reference

Parameters	Description	Min	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-1025	700	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
V_{OL}	Output LOW voltage	-2000	-1620	mV	
V_{IH}	Input HIGH voltage	-1165	-700	mV	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	-2000	-1475	mV	Guaranteed LOW for all inputs

Notes: (1) Over recommended operating conditions, $V_{CC} = V_{CCA}$ = GND, Output Load = 50Ω to V_{TT}
External Reference = 1.32V± 0.025V.

Table 7: TTL Inputs/Outputs *(Over recommended operating conditions, TTLGND = GND)*

Parameters	Description	Min	Max	Units	Conditions
V_{OH}	Output HIGH voltage	2.4	V_{TTL}	V	I_{OH} = -2.4 mA
V_{OL}	Output LOW voltage	0	0.5	V	I_{OL} = 8 mA
V_{IH}	Input HIGH voltage	2.0	V_{TTL}	V	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	0	0.8	V	Guaranteed LOW for all inputs
I_{IH}	Input HIGH current	—	50	µA	$V_{IN} = V_{TTL}$
I_{IL}	Input LOW current	-500	—	µA	V_{IN} = 0.5V
I_{OZH}	3-State Output OFF Current HIGH	—	100	µA	V_{OUT} = 2.4V
I_{OZL}	3-State Output OFF Current LOW	-100	—	µA	V_{OUT} = 0.5V
I_{OH}	Open collector output leakage current	—	100	µA	V_{OUT} = 2.4V

Application Note 2

Interfacing GaAs Products to ECL/TTL I/O

Absolute Maximum Ratings [1]

Potential Pin to Ground, (V_{TT}) ..... -2.5V to +0.5V
Potential Pin to Ground, (V_{TTL}) ..... +6.0V to -0.5V
ECL Input Voltage Applied (2), ($V_{IN\ ECL}$) ..... +0.5V to VTT
TTL Input Voltage Applied (2), ($V_{IN\ TTL}$) ..... -0.5V to VTTL
ECL or TTL Output Current, I_{OUT} , (DC, output HIGH) ..... 50 mA
Case Temperature Under Bias, (T_C) ..... -55° to +125°C
Storage Temperature(3), (T_{STG}) ..... -65° to +150°C

NOTES: 1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.
2) VIT ,VITL must be applied before any input signal voltage and VECLIN input must be greater than VIT - 0.5V.
3) Lower limit of specification is ambient temperature and upper limit is case temperature.

Recommended Operating Conditions

ECL Supply Voltage (VCC), (VTT) ..... -2.0V ± 5%
TTL Supply Voltage, (VTTL) ..... +5.0V to +5%
Operating Temperature (2), (T)(Commercial) 0° to 70°C, (Industrial) -40° to +85°C, (Military) -55° to +125° C

NOTES: 1) When using internal ECL 100K reference level.
2) Lower limit of specification is ambient temperature and upper limit is case temperature.

Interfacing GaAs Products to ECL/TTL I/O

Application Note 2

Application Note 4

Generation of a -2 Volt Supply From a +5 Volt Supply

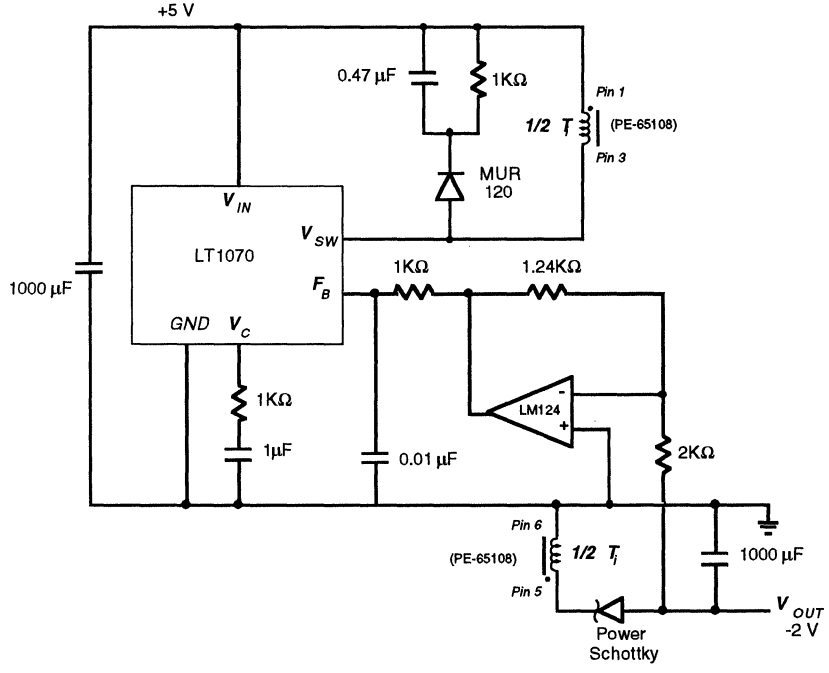
Description

Some Vitesse ASIC products need both -2V and +5V power supplies. This application note describes a method of generating a -2V supply from a +5V supply. It is possible to generate the -2V supply from a standard +5V supply, commonly found in TTL systems, by using a switching regulator IC such as the LT1070 from Linear Technology Corp. (Milpitas, CA).

The LT1070 is a monolithic high power switching regulator which can be configured with the aid of a few external components to create a positive input - negative output Flyback Converter. The schematic below depicts a Flyback Converter configuration capable of +5V to -2V conversion. In addition to the LT1070, the circuit includes a standard LM124 op-amp from National Semiconductor Corp. (Santa Clara, CA) and a PE-65108 Transformer from Pulse Engineering (San Diego, CA). Such a circuit is capable of delivering up to 4 Amps of continuous current at -2 Volts and has line regulation of 0.05%/V.

Additional information on the LT1070 and the Output Flyback Converter configuration can be obtained from Linear Technology Corp. (408/432-1900) in their Application Note # 19.

Figure 1: Flyback Converter Configuration



Generation of a -2 Volt Supply
From a +5 Volt Supply

Application Note 4

Application Note 6

Metastable Behavior of GaAs DCFL Registers

Introduction

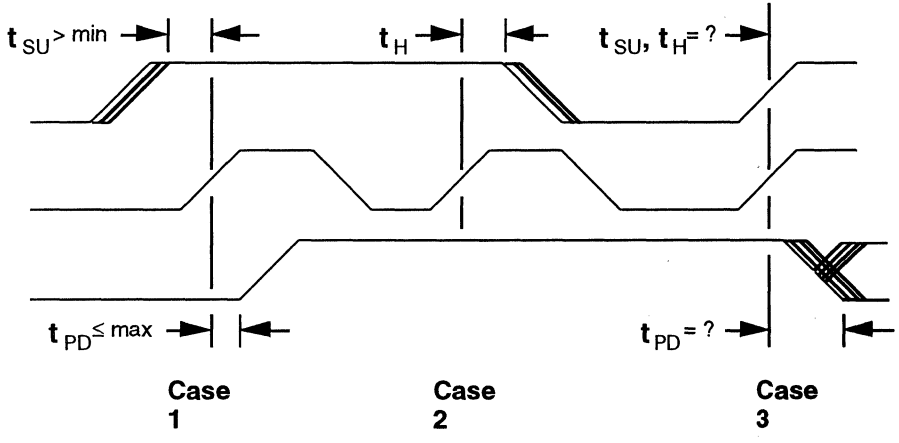
This application note describes the fundamentals of metastability as well as a method of characterizing metastable behavior. The results of the characterization are applied to a general failure rate formula to predict the reliability of data synchronizers implemented using GaAs DCFL registers.

Metastability Theory

In any system where a single flip-flop (or latch) is used to resolve the timing conflicts between two asynchronous digital circuits, this flip-flop is subject to marginal triggering behavior.[1] In recent years, this general phenomenon has been given the name "metastability". The theory and characterization of metastable behavior is of particular concern in determining the reliability (failure rate) of synchronizer circuits.

A metastable condition can occur when the setup and hold specifications of a register are violated. In Figure 1, Case 1 shows a transition of the asynchronous data which satisfies the setup time requirements of the synchronizing register. A logic "1" is therefore transferred to the register output. Case 2 in Figure 1 shows data which is stable for a sufficient period of time to satisfy the hold time requirements of the register. In Case 3, however, the asynchronous data and the clock transition concurrently, thus causing the output of the register to be indeterminate (neither a logic "1" or a logic "0") for a period of time. The amount of time required for the register output to transition from this indeterminate state to a valid logic state is commonly referred to as the "walk-out" time. The actual window of time where an indeterminate condition can occur is normally much smaller than the specified setup and hold time window for a given flip-flop.

Figure 1: Data and Clock Relationship for Bi-Stable Elements

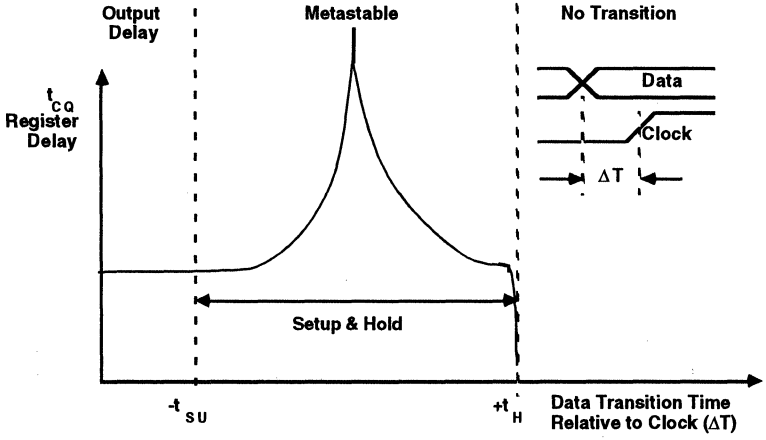


Metastable behavior can also be perceived in terms of its effect on flip-flop delay.[2] As seen in Figure 2, the flip-flop has a normal propagation delay, t_{CQ}, when the setup time specification is met. As the data input transition moves closer to the clock transition, however, the delay of the flip-flop increases - reaching its maximum value when the clock and data transitions occur simultaneously. As the data input transition moves past the hold time, no output transition occurs.

Metastable Behavior of GaAs DCFL Registers

Application Note 6

Figure 2: Metastable Delay



Perhaps the most important concept in understanding metastable behavior is that the walk-out time is always a probabilistic phenomenon. A "maximum" walkout time for a given register does not exist. Rather, for a certain flip-flop there exists a relationship between a given walk-out time and the probability that this walk-out time will occur. Empirical studies have shown that the mean time between events where the synchronizer flip-flop is still unresolved at time t_w, MTBF(t_w), is: [2,3]

$$MTBF(t_w) = \frac{exp(t_w/K2)}{(K1)(f_{CLK})(f_{DATA})} \quad (1)$$

for $t_w > h$

where:

t_w is the time the flip-flop has been allowed to resolve after the clock transition.
K1, *K2*, and *h* are parameters associated with a particular register and are functions of the circuit design and construction.

The total walk-out or indeterminate time can be viewed as two time periods: the amount of time taken for random noise to "push" the output just outside of the metastable state (T_M), and the recovery time (T_R) from time T_M until a valid logic state is achieved.

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Metastable Behavior of GaAs DCFL Registers

Metastability Characterization

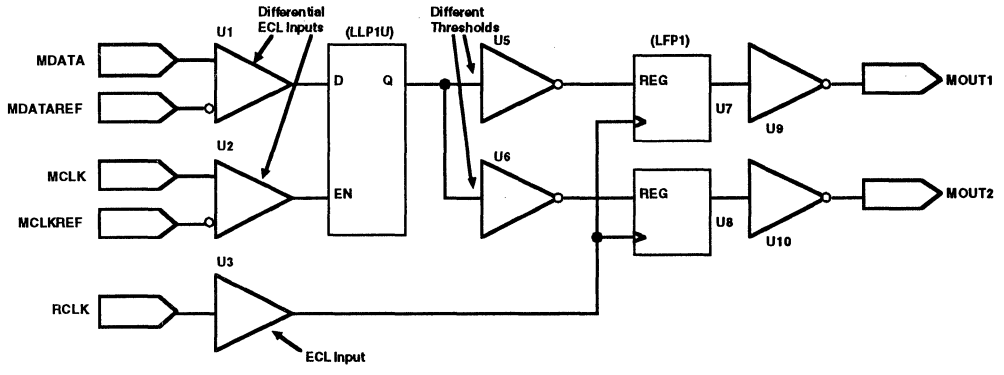
Metastable behavior can be observed using many different methods. Analog circuit simulators such as SPICE cannot accurately characterize metastable behavior in a bistable element unless an accurate noise model is incorporated into the simulation. Given the random and often complex origins of noise in actual circuits, accurate noise models are quite difficult to create. Metastable behavior can also be observed in the lab using fine resolution delay lines to vary the relationship between clock and data until an indeterminate condition is observed using a triggered oscilloscope. Because metastability is a probabilistic phenomenon, however, it is impossible to obtain the *K1*, *K2*, and *h* constants for a given register using either of the above methods.

The most direct and accurate method of characterizing the metastable behavior of a flip-flop is to construct a synchronizer using that flip-flop and gather statistical data on that flip-flop's failure rate as a function of the settling time allowed. This characterization method readily yields the *K1*, *K2*, and *h* constants necessary to predict synchronizer failure rates. To shorten the duration of the tests, random data transitions can be confined to a small window of time surrounding the active clock transition.

Test Setup

In order to characterize the metastable properties of GaAs DCFL registers, a synchronizer circuit was implemented on a FURY VSC10K gate array. The circuit schematic is shown in Figure 3. In order to simplify the testing, a latch (LLP1U) was used rather than a flip-flop. The LLP1U is an unbuffered DCFL latch. The clock and data signals are brought onto the chip through differential ECL compatible inputs. The clock (enable) signal was inverted to cause the circuit to latch on a positive clock, again to simplify the test. The output of the latch drives two DCFL inverters, U5 and U6. A difference in switching thresholds between the two inverters is created by using twice the standard D-mode FET width on inverter U5 and twice the E-mode FET width on inverter U6. This threshold window is approximately 130 mV in magnitude centered around the nominal inverter threshold. When the output of the latch is in the indeterminate region, therefore, the output of U5 will be high and the output of U6 will be low. The outputs of U5 and U6 are registered using flip-flops U7 and U8 and are driven off-chip through ECL outputs U9 and U10.

Figure 3: Metastability Circuit Schematic



Metastable Behavior of GaAs DCFL Registers

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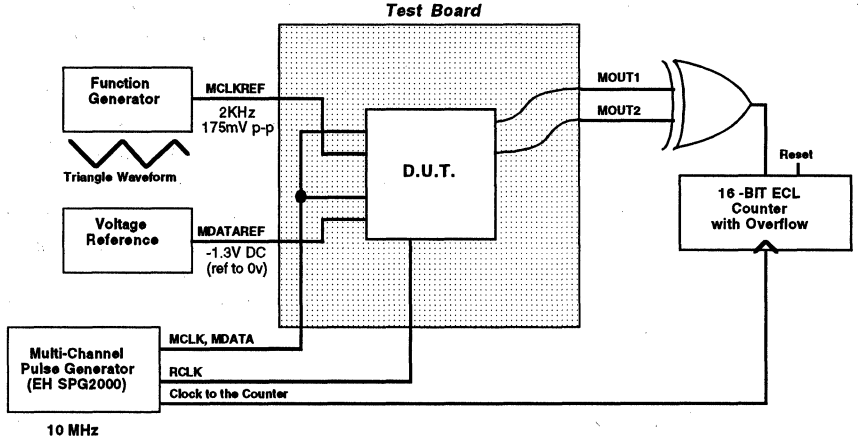
Figure 4: Metastability Bench Setup



The bench setup shown in Figure 4 was used to conduct the metastability testing. An EH SPG2000 4-channel pulse generator was used to provide the "raw" clock and data signals (MCLK and MDATA) to the latch as well as the RCLK signal to registers U7 and U8. In order to accurately control the relationship between the clock and data signals to the latch, the ECL differential input buffers, U1 and U2), were used as verniers. The MDATAREF signal was set to a fixed voltage to adjust the clock and data signals so that metastable events per unit time were maximized. A triangle waveform was driven onto the MCLKREF pin in order to sweep the latch back and forth through its entire window of metastability. The size of the actual window was determined empirically to be about 15 ps. However, a 350 ps sweep window was chosen (by adjusting the amplitude of the triangle waveform) to ensure that the entire period where metastable events occurred was covered even if the MDATAREF input voltage drifted. Because the slew rate of the MCLK/MDATA signal was set to 0.5 V/ns, a peak-to-peak voltage of 175 mV was used for The register output signals, MOUT1 and MOUT2, drive an off-chip exclusive-OR which in turn drives a 16-bit ECL counter with over-flow. For a given test the walkout time, tw, is controlled by setting the delay between the MCLK and RCLK signals. The time between trials (each trial being a latching edge on MCLK) is set by varying the internal period on the SPG2000 pulse generator. For all of the tests summarized in this document, a period of 100 ns was used which corresponds to a clock rate of 10 MHz. For each part, errors were counted over a specific period of time for various values of walkout time.

All of the testing was performed at room temperature with no air flow applied to the part. A case temperature of 52 ± 2°C was measured for these conditions. A nominal supply voltage of -2.0 Volts was applied to the device under test. Prior to the actual MTBF testing, the output of the latch was observed directly using a sampling oscilloscope to ensure that metastable conditions could be induced by the test setup.

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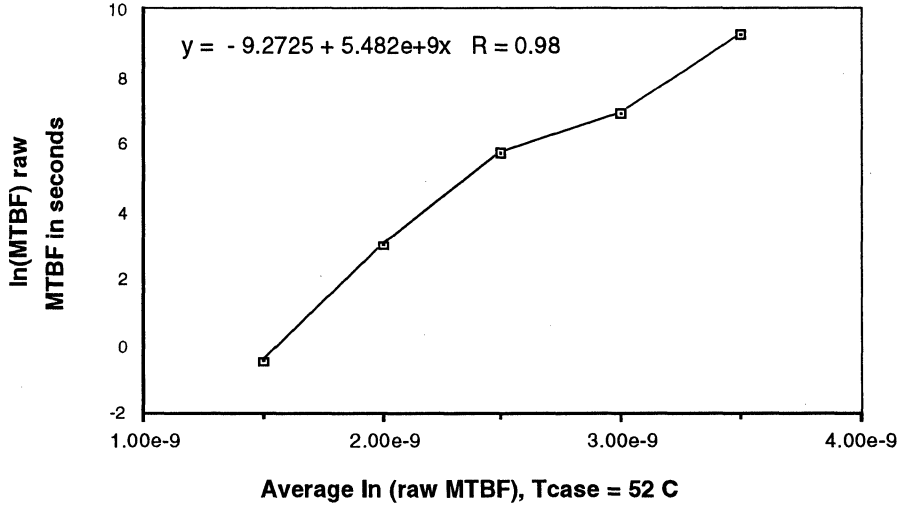
Metastable Behavior of GaAs DCFL Registers

Test Results

Figure 5 shows ln(MTBF raw) versus the walkout time. This data is an average of testing done on two devices and is considered to be typical. For both parts, the data taken fit the theoretical model described in equation (1). The value of the experimental constant, *h*, which represents the minimum value of t_w for which equation (1) holds, was not determined but appears to be less than 1 ns. Further testing is required to establish the worst case MTBF for a given walkout time. Vitesse recommends guardbanding the settling time allowed by at least 1 ns to meet the typical MTBF values specified.

Figure 5: ln(raw MTBF) as a Function of Walkout Time



The values for *K1* and *K2* are derived from the experimental data using the following relationships:

$$K1 = exp(-ln((f_{CLK})(f_{DATA})) - b) \quad (2)$$

$$K2 = 1/m \quad (3)$$

where:

f_{CLK} = clock frequency to the latch (10 MHz)
f_{DATA} = effective data frequency (1.43 GHz)
m,b = the slope and y-intercept of the linear fit of ln(MTBF) vs. t_w

The effective data rate of 1.43 GHz is achieved by limiting data transitions to the 350 ps sweep window around the clock. Because only a single rising edge occurs in this window, however, the effective data period is twice the sweep window. Using the slope and y-intercept from Figure 5, the values of *K1* and *K2* are:

K1 = 7.44E-13/sec

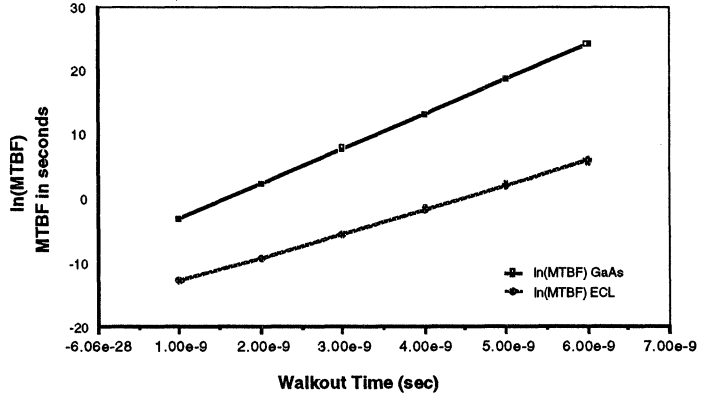
K2 = 1.82E-10 (dimensionless)

Figure 6 charts the MTBF as a function of walkout time for a data frequency of 100 MHz and a clock frequency of 75 MHz. Data is given for both a GaAs DCFL circuit and a typical ECL register. Table 1 shows the typical MTBF for various combinations of f_{CLK}, f_{DATA}, and t_w. The user should note that these MTBF values are for a single flip-flop. In order to calculate the MTBF for a dual-stage synchronizer, the MTBF of the first stage must be calculated first. This MTBF then becomes the data rate for the next stage when calculating the cumulative MTBF of the two registers in series.

Synchronizer Applications

Knowledge of the metastable behavior of registers in a given technology is crucial to the design of synchronizers. The VMEbus, for example, is an entirely asynchronous bus.[2] Because no timing is specified for bus arbitration signals, decision points such as the bus arbiter, the bus-grant daisy chain, and the interrupt-acknowledge daisy chain must contain synchronizers to resolve timing conflicts. Given that the system clock rate is a known value and the frequency of events to be synchronized can be estimated for the system, the MTBF for the synchronizer can be established based on the MTBF equation for that register. For example, a dual register synchronizer clocked at 100 MHz synchronizing data at 50 MHz will exhibit a mean time between failures of approximately 90 million years, allowing 1 ns for setup time and 1 ns for guardband. If the MTBF for a given amount of settling time is tolerable, a single DCFL register can be used to synchronize random events. For a single register, 100 MHz clock, and 50 MHz data, allowing an additional 5 ns of delay yields a typical MTBF of about 7 years.

Figure 6: MTBF vs. Walkout Time for GaAs and ECL



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Metastable Behavior of GaAs DCFL Registers

Conclusions

Compared with previously published results, initial testing indicates that GaAs DCFL registers are superior to ECL registers in terms of the mean time between failure due to metastable conditions. This result is likely attributable to the fast intrinsic delays of DCFL gates as well as the shorter feedback path inherent in DCFL latches. Past studies show that the trend is for the value of *K2* to be lower for newer and faster technologies.[2] Further testing will allow the variations in metastable behavior with respect to process to be determined. Testing over temperature and voltage variations is also scheduled although past research indicates that variations in *K1* and *K2* due to temperature and voltage are minimal compared to variations due to process.[2]

Table 1: MTBF as a Function of F_{DATA}, F_{CLK} and Walkout Time

f_data (Hz)	*f_clk (Hz)*	*t_walk (seconds)*	*MTBF Expressed In:*			
			Seconds	*Hours*	*Days*	*Years*
1.00E+07	2.00E+07	4.00E-08	1.15E+93	3.18E+89	1.33E+88	3.64E+85
2.50E+07	5.00E+07	1.80E-08	7.69E+39	2.14E+36	8.99E+35	2.44E+32
5.00E+07	1.00E+08	8.00E-09	2.99E+15	8.31E+11	3.46E+10	9.48E+07
1.00E+08	2.00E+08	4.50E-09	3.47E+06	9.65E+02	4.02E+01	1.10E.01
3.30E+07	6.60E+07	1.42E-08	3.04E+30	8.43E+26	3.51E+25	9.63E+22

References

1. Chaney, Thomas J., "Measured Flip-Flop Responses to Marginal Triggering", *IEEE Transactions on Computers*, Vol. C-32, No. 12, pp. 1207-1209, December 1983.

2. Beaston, John and R. Scott Tetrick "Designers Confront Metastability in Boards and Busses", *Computer Design*, pp 67-71, March 1, 1986.

3. Chaney, T.J. and F. U. Rosenberger, "Characterization and Scaling MOS flip-flop Performance in Synchronizer Applications", in Proc. Conf. *Very Large Scale Integration Architecture, Design, Fabrication*, California Instit. Technol., pp. 357-374, 22-24 Jan 1979.

Metastable Behavior of GaAs DCFL Registers

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Application Note 7

GaAs DCFL
ASIC Design

Introduction

For several years, Gallium Arsenide ICs have proven extremely useful in high-speed linear applications such as microwave amplifiers and fiber optic drivers. Within the past five years, however, improvements in processing technology coupled with the use of advanced design techniques have made the production of VLSI GaAs integrated circuits a reality. Vitesse Semiconductor Corporation has developed a tightly controlled GaAs enhancement/depletion mode (E/D) process. This process in conjunction with its direct-coupled FET logic (DCFL) design technique has enabled Vitesse to produce and ship ASIC circuits with complexities of over 100,000 gates. The performance of these circuits and the available ECL-compatible I/O structures allow GaAs DCFL ASICs to serve as a viable alternative to ECL gate arrays or standard cells at the system level. This application note describes the similarities and differences in structure and implementation of GaAs DCFL and Bipolar ECL/TTL ASIC devices.

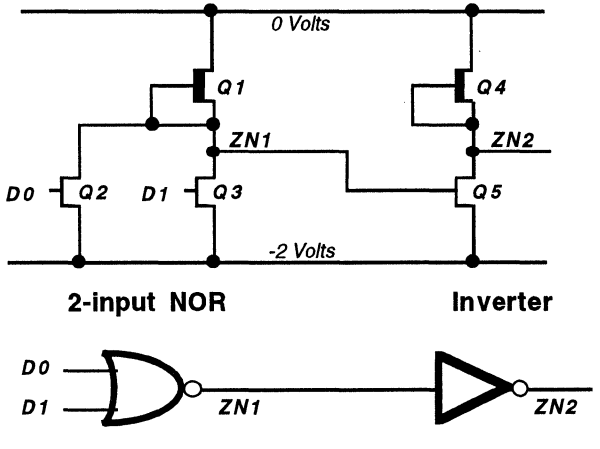
What is Direct-Coupled FET Logic?

Direct-coupled FET logic (DCFL) is a technique used to design logic structures from enhancement and depletion mode FETs. DCFL has been in use since the mid-1970's to build nMOS circuits and is widely recognized for its density and simplicity in the creation of large integrated circuits.

On paper, GaAs DCFL logic looks virtually identical to nMOS with the exception that nMOS uses MOSFETs while GaAs DCFL uses MESFETs. MOSFETs have an oxide insulated gate which prevents the flow of gate current, while MESFETs contain a Schottky barrier diode in the gate-source junction which allows the gate to source current supplied from the previous stage of logic. The gate diode also clamps the internal V_{OH} level to about -1.3 V, or one diode drop above V_{TT}.

Figure 1 shows a 2-input NOR driving an inverter. The depletion mode FETs (*Q1* & *Q4*) have their gates shorted to their drains and act like current sources. When both *D0* and *D1* are low, *Q2* and *Q3* are off, allowing *ZN1* to rise and turn on *Q5*. The current from *Q1* in this case will flow through the gate of *Q5*. If either *D0* or *D1* are pulled high, the *Q1* current is shunted through *Q2* and/or *Q3*, pulling *ZN1* low.

Figure 1: DCFL 2-input NOR and Inverter



GaAs DCFL
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DCFL Features

The key advantages of DCFL are circuit simplicity and the ability to switch very quickly using a small supply voltage. The 2-input NOR gate shown in Figure 1, uses only three transistors (resistors are not necessary). GaAs DCFL can operate reliably on a 1.1 V power supply, in contrast to bipolar ECL which requires either 4.5 or 5.2 V. Unlike ECL, no internal reference voltages are needed for GaAs DCFL circuits. All logic switches around the enhancement-mode FET threshold (about 250 mV above the source voltage, V_{TT}).

On the flip side, however, GaAs DCFL does not allow the use of series-gated structures, wire-ORs, or collector-dotting (all features of ECL). This is offset by the higher circuit density and corresponding shorter device interconnection lengths found in GaAs DCFL. Virtually all logic structures which have been created for Vitesse ASIC products are constructed from simple inverters or two to four input NOR gates. Figure 2 depicts a full adder macro implemented in GaAs DCFL. The logic portion of this macro is built from three 2-input NORs, five 3-input NORs, and one 4-input NOR. Vitesse incorporates a proprietary buffer on the outputs which effectively drive large capacitive loads with very little skew between the rising and falling edges. Table 1 is a comparison of the GaAs DCFL full adder macro with an equivalent version implemented in silicon bipolar ECL technology. Note that the GaAs DCFL version has a significantly shorter propagation delay, dissipates less than 30% of the power and uses only 70% of the space needed by its silicon counterpart.

Figure 2: Full Adder Implemented in GaAs DCFL

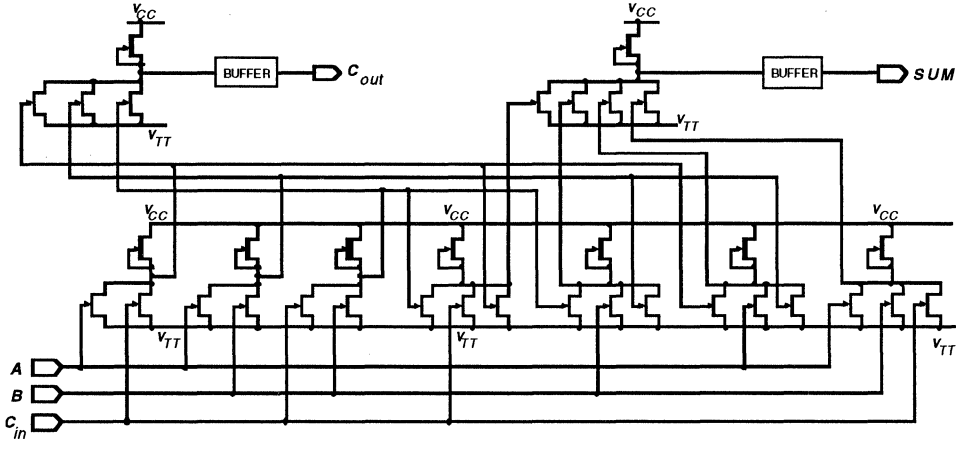

Table 1: GaAs DCFL vs. Silicon ECL: Full Adder Macro Comparison

Parameter	*GaAs DCFL*	*Silicon ECL*
A/B → SUM	560 ps	1125 ps
$C_{in} \rightarrow C_{out}$	340 ps	1338 ps
Power (typ)	2.6 mW	16.58 mW
Area	9144 μm^2	31750 μm^2

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GaAs DCFL
ASIC Design

Buffering Tradeoffs

Many ECL ASIC products allow for a tradeoff between speed and power. This is generally accomplished by allowing the designer to select different switch and emitter follower current values by paralleling resistors using the metal personalization. Generally, the resistors necessary for at least two different speed/power versions of many functions are included in the basic cell. In GaAs DCFL, however, the trade-offs involved in buffering are somewhat different. In Vitesse's FURY and FX Series' of gate arrays, internal macrocells can have unbuffered, 1x drive, or 2x drive outputs. The trade-offs involved with this choice of buffering involve speed, power, and density. Moreover, the speed/power versus density tradeoffs will vary depending on the complexity of the macro function. In general, the presence (or absence) of buffering affects the intrinsic delay of the macro very little. Buffering will increase the driving ability of the macro output in terms of both DC drive limitations and AC performance. On the other hand, buffering requires additional depletion and enhancement mode devices which could otherwise be used for logic and also consumes additional power. The more complex the macro function, the less the price paid for the buffer in terms of percentage area and power. Figures 3 and 4 depict the buffering tradeoffs for a 4-input NOR and a D flip flop in the FX Series macrocell library.

Figure 3: FX Macro Buffering Options for a 2-input NOR Gate

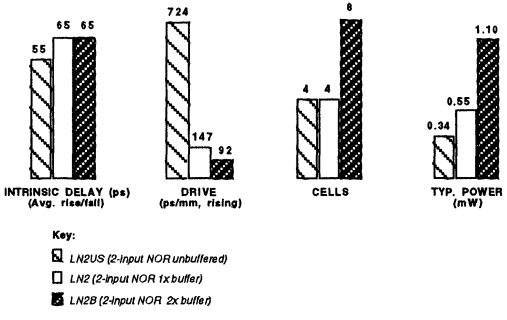
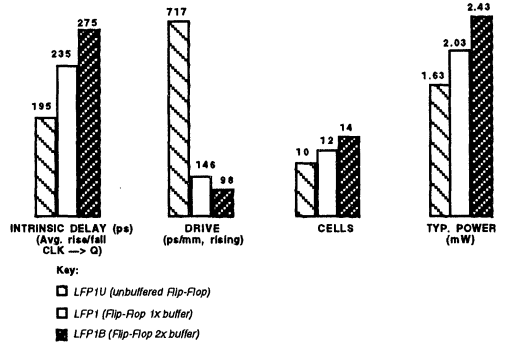


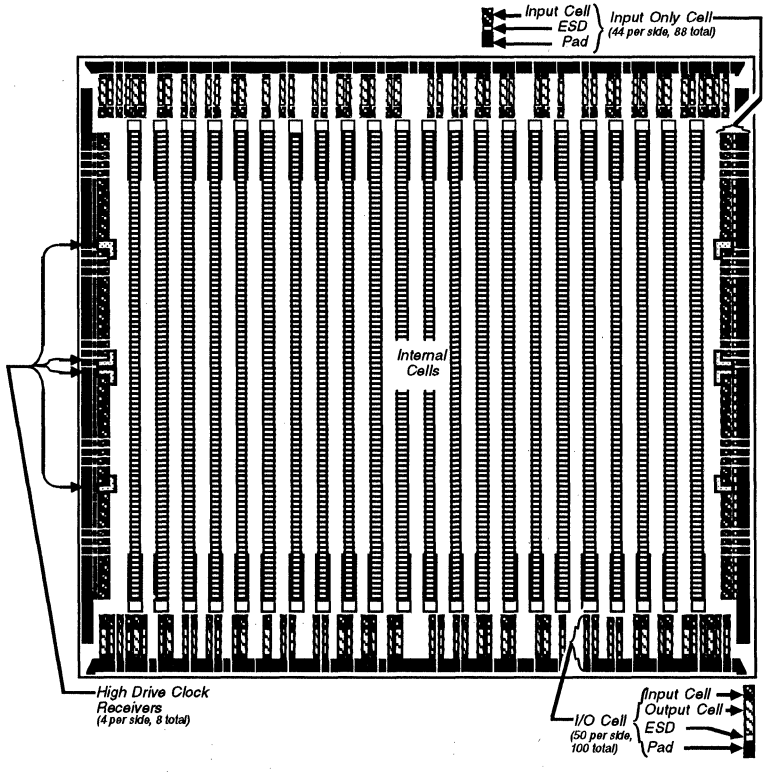
Figure 4: FX Macro Buffering Options for a D Flip-Flop



FURY Gate Array Architecture

Like most third generation ECL gate arrays, the Vitesse FURY Series of gate arrays employ a channeled architecture. Metal 1 is used to route within macrocells and in the vertical channels between macrocell columns reserved for routing. Metal 2 channels run horizontally over the entire core area. A third layer of metalization is used for fixed power and ground distribution in the macrocell columns. Figure 5 shows the layout of the FURY VSC15K array.

Figure 5: FURY VSC15K Array Architecture



The I/O ring contains 96 input-only buffers on the sides of the array and 100 input/output buffers on the top and bottom for a total of 196 I/O pads. A D-latch or buffer can be implemented in the input-only cells and a D-flip flop or a 2 or 3-input OR/NOR gate may be placed in the output cell structure. In addition, each FURY array contains a small number of high-drive input cells which are used for distributing large fanout signals, such as clocks, to local buffers in different areas of the core.

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Each cell column in the core is composed of a large number of "slices" (192 in the case of the VSC15K). A slice consists of four cells in a 2 by 2 configuration. A cell is equivalent to an unbuffered 2-input NOR (two enhancement-mode FETs and one depletion-mode FET). The minimum addressable unit (MAU) in a FURY array is two cells (six FETs). By contrast, the typical ECL gate array MAU contains 10 to 19 transistors and an equal number of resistors. The finer granularity of the FURY MAU minimizes the number of wasted transistors in a given macrocell implementation allowing for virtually 100% use of the core cells.

To the IC designer, a Vitesse GaAs DCFL gate array appears much the same as its present ECL counterpart. Both have internal and I/O macrocells and both generally use channeled architectures with two layers of user metal and one layer of power/ground metal.

FX Array Architecture

The FX Series offers the integration level of BiCMOS gate arrays with speed performance exceeding that of ECL devices. Implemented using Vitesse's proprietary H-GaAs III process, the FX family of gate arrays is the first to combine ultra high integration with leading edge performance.

The FX array family incorporates a channelless array architecture which allows metal routing on the first layer to be placed directly over unused cells. This approach avoids the need for pre-defined channels between columns of macros and therefore allows much greater density and flexibility than channelled gate array architectures. Due to an advanced four layer metal process, typical maximum array utilizations range from 50% to 67% of the total available gates.

Capable of operating at well over 500 MHz, the FX Series arrays have been designed to provide the best speed - power performance of any gate array technology. The speed of leading edge ECL technology is achieved at a fraction of ECL's power. In addition, because of the frequency independent power consumption of H-GaAs technology, power dissipation levels comparable to, or lower than, similar density BiCMOS arrays can be achieved at frequencies above 50 MHz (see Vitesse Application Note 10, "Power Dissipation: BiCMOS vs. GaAs"). This power savings can add up to substantial cost savings to users in terms of overall cooling requirements.

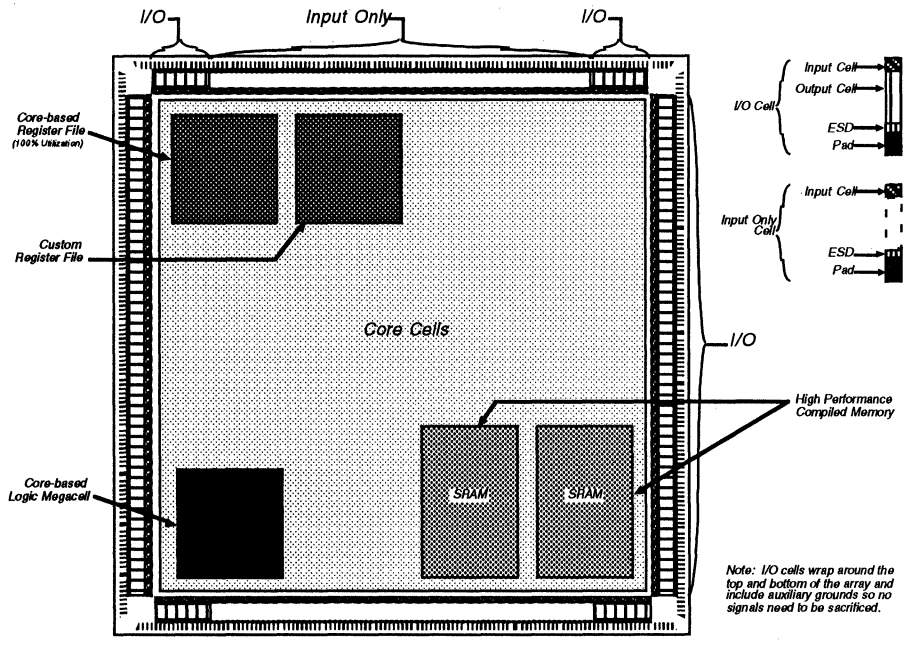
The FX Family includes support for the creation of custom masterslices. Functions such as SRAMs, multiport register files, and others can be merged with FX arrays resulting in unique architectures and optimum performance.

As with all of Vitesse's ASIC products, the FX arrays interface with TTL and ECL devices directly. The FX array family uses standard power supplies and is supported on the ASIC industry's most popular CAE platforms for schematic capture, behavioral modeling and logic synthesis.

The FX arrays contain three cell types: internal logic cells, input only cells and input/output (I/O) cells. All input only and input/output cells contain undedicated logic which the user may personalize. There is enough configurable logic in these cells to implement moderately complex functions such as mux'es and flip flops, allowing the arrays to conform to the JTAG boundary scan standard.

FX arrays can be designed to implement full custom megacells such as SRAM and pre-defined core based megacells such as register files. In addition, a proprietary compiler is available to customers wishing to incorporate custom RAM configurations in their designs. A depiction of a VGFX350K with megacells incorporated is shown in Figure 6.

Figure 6: FX Array Architecture



RAM/ROM Megacells

As with ECL standard cell architectures, the FX gate arrays allow for the inclusion of custom, hand-packed "megacell" blocks. Unlike newer ECL standard cell technologies which use BiCMOS for the implementation of dense RAM, the FX arrays use the same GaAs E/D process and design rules for RAM and ROM blocks that are used for standard DCFL logic.

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GaAs DCFL ASIC Design

System Considerations

At the system level (i.e., looking at a packaged part as a black box), Vitesse GaAs ASICs are virtually identical to ECL ASICs. ECL I/O buffers as well as TTL buffers are supported on all FURY and FX ASIC products. In implementing a board design which includes a Vitesse ASIC, however, the designer should be aware of ECL I/O differences and power supply requirements.

ECL I/O

Vitesse ASICs support ECL 100K input and output levels. Unlike standard ECL 100K, however, the GaAs V_{OL} min is always equal to V_{TT} because the ECL outputs are cutoff in the low state. This is not a problem in digital applications, but may necessitate the use of a higher V_{TT} (approximately -1.7 Volts) when driving a DAC because of potential analog feed-through problems associated with the larger input swings. Also, the -2.0 Volt supply must be controlled to ±5% to ensure that adequate noise margins are maintained using the internal V_{BB} reference generator. If such regulation is not feasible, or if the design must receive 10KH levels (which vary with temperature), then an external V_{BB} reference should be supplied.

Power Supply Considerations

Nearly all Vitesse ASICs use -2V as the primary supply voltage. In fact, for an ECL-only interface, -2V is the only supply required. Although the power dissipated by GaAs DCFL circuits is relatively small, the -2V regulator must be capable of supplying a large amount of current (up to 4 Amps in the case of a fully utilized VSC15K gate array). When TTL interfaces are needed, a +5V is required. Some gate arrays can be configured to a +5V, +2V supply environment for TTL only operation.

Conclusion

Though the internal logic structures and raw materials used to construct GaAs DCFL ASICs are somewhat different from those used to build ECL ASICs, the two technologies are virtually identical at the system level. The density and performance of GaAs DCFL ASICs make them attractive alternatives to ECL ASICs in many systems. With the advent of the FX family, the system designer now has the flexibility to more fully reap the benefits of GaAs DCFL technology. The major advantage of GaAs DCFL technology is the ability to produce ASIC devices which offer better density and performance than ECL while dissipating only 1/4 to 1/5 of the power.

GaAs DCFL
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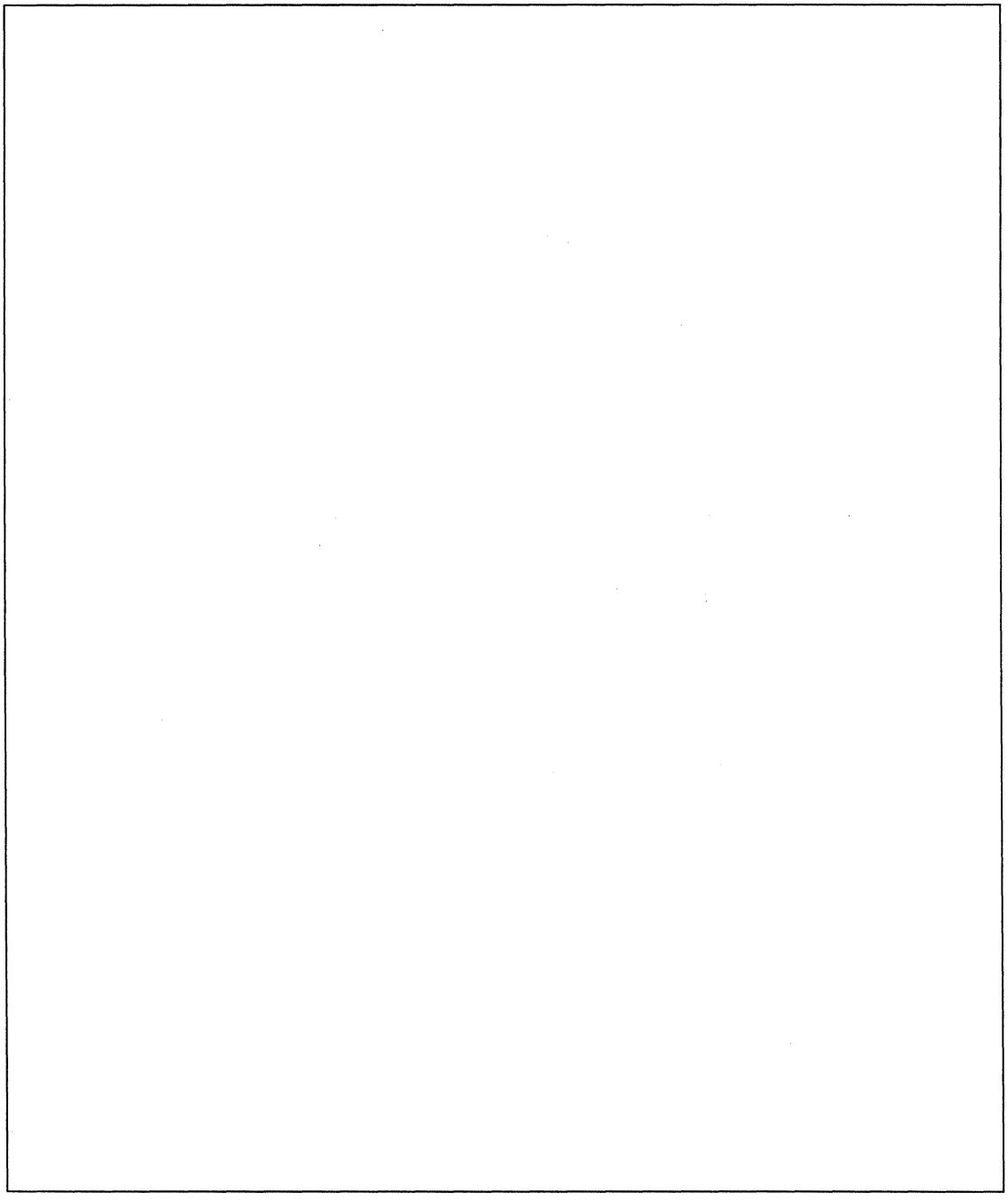


Application Note 8

Generating an External ECL Reference

Introduction

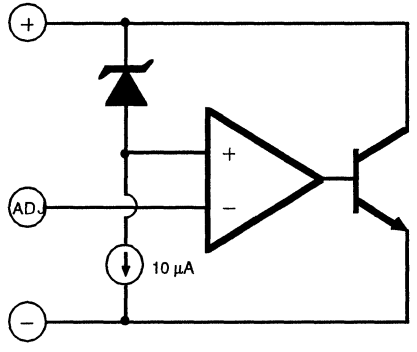
The use of multiple ECL (or ECL-compatible GaAs) ASIC devices on a circuit board may require the addition of an externally generated ECL input reference voltage (V_{BB}). Providing this reference ensures that the input receivers of the ECL devices will all switch at the same threshold voltage independent of power supply or temperature variations.

This application note describes a method for providing an external ECL input reference (-1.32 Volts) from a standard -2.0 Volt ECL supply using an adjustable micropower voltage reference and three resistors.

Reference Circuit Description

The reference circuit employs three resistors and an LM185, LM285, or LM385, which are 3-terminal adjustable band-gap voltage reference devices available from National Semiconductor Corporation. The LM185 is rated for operation over a -55°C to 125°C temperature range, while the LM285 is rated from -40°C to 85°C and the LM385, from 0°C to 70°C. A block diagram of the LM185/285/385 is shown in Figure 1. The circuit shown in Figure 2 is used to create the voltage reference.

Figure 1: Block Diagram of the LM185/285/385



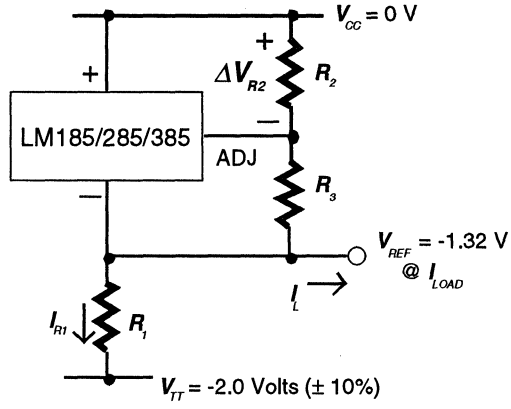
The reference circuit shown in Figure 2 uses V_{TT} and V_{CC} as external voltages to produce the reference voltage, V_{REF}. In order to create a reference which can be used with Vitesse ECL-compatible ASIC parts, the values for R_1, R_2, and R_3 must be chosen under the following operating conditions:

- Supply Voltage,(V_{TT}) -2.0 Volts (± 10 %)
- Current through LM185/285/385 from + to —, (I_D) 0.10 to 20 mA
- ADJ Current through LM185/285/385, (I_A) ≤ 10 nA (guaranteed by LM185/285/385 specs)
- Current to each Vitesse ECL compatible input cell from V_{REF}, (I_{Input}) ≤ 5 µA
- Potential between V_{CC} and ADJ, (ΔV_{R2}) 1.24 Volts (reference voltage produced by the LM385)

Generating an External ECL Reference

Application Note 8

Figure 2: ECL Reference Circuit



The values for R_2 and R_3 must satisfy the following condition:

$$V_{REF} = -1.24 \left(\frac{R_3}{R_2} + 1\right) \quad [1]$$

By equation [1], the following commonly available resistor values can be used for R_2 and R_3 to create a -1.32 Volt ± 10mV reference:

$$R_2 = 16\text{K}\,\Omega$$
$$R_3 = 1\text{K}\,\Omega$$

The stability of V_{REF} depends on the tolerances of these two resistors. If k is the maximum normalized value and p is the minimum normalized value of the resistors R_2 and R_3 expressed as decimals, then the variation in V_{REF} is given by the following equation:

$$\Delta V_{REF} = \frac{\frac{R_3}{R_2}\left(\frac{k}{p} - 1\right)}{\frac{R_3}{R_2} + 1} \quad [2]$$

Application Note 8

Generating an External ECL Reference

Assuming that the resistors have a 5% tolerance and substituting values into the equation, we can then solve the equation:

$$\Delta V_{REF} = \frac{\frac{1K\Omega}{16K\Omega}\left(\frac{1.05}{0.95} - 1\right)}{\frac{1K\Omega}{16K\Omega} + 1} \quad [3]$$

$$\Delta V_{REF} = 0.6\% \text{ or } \sim 8mV$$

Although use of 5% resistors gives a tight V_{REF}, it is advisable to use 1% metal film resistors instead of the commonly available 5% carbon composition resistors to minimize aging effects and to compensate for the tolerance on the 1.24 Volt band-gap reference voltage.

R_1 determines the no load regulator current. Assuming worst case power supply and 175µA total regulator current, then:

$$R_1 = \frac{1.8 - 1.32}{175\mu A} = 2.7\ k\Omega$$

Since the regulator can source up to 20mA, as many as 4000 Vitesse ECL inputs can be supported. Thus, a single regulator circuit, as shown in Figure 3, can be used on a circuit board to supply ECL input reference for many Vitesse IC's. A typical Vitesse compatible external VREF pad is shown in Figure 4. The exact number of IC's is dependent upon the number of ECL inputs per IC. The load current per input cell is ≤ 5µA, with an additional 100µA ESD diode leakage current per chip. For example, if 3 ASIC devices with 40 inputs each are serviced by the external V_{REF} circuit, then:

$$I_L = (3x40x5\mu A) + (3x100\mu A)$$
$$= 900\mu A$$

Generating an External ECL Reference

Application Note 8

Figure 3: Implementation of Reference Circuit

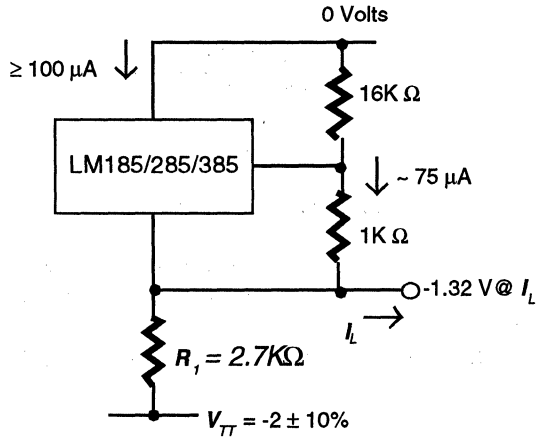
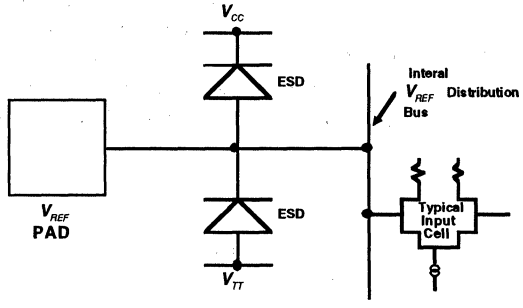


Figure 4: Typical Vitesse External V_{REF} Pad



Notes

1. In order to use this reference generation scheme, the Vitesse ASIC product (gate array or standard cell) must be specified with an external ECL reference.

2. Vitesse recommends the use of a 0.001 to 0.01 µF bypass capacitor at the reference input pin of each array. Refer to the design manual for the particular ASIC product for the location of the input reference pins.

3. Care must be taken to account for the effect of IR drop in the reference net on the PC board.

Application Note 10

Power Dissipation: BiCMOS vs GaAs

Introduction

CMOS and BiCMOS have traditionally been viewed as low power technologies. This reputation stems from the fact that unlike other technologies which have preceded them (TTL, ECL, NMOS, etc.) the power dissipated by a CMOS or a BiCMOS gate is dependent on the frequency of its operation. When CMOS or BiCMOS gates are not toggling they dissipate almost no power. As operational frequencies in the gates increase, however, the amount of power dissipated proportionately increases. At these higher frequencies, GaAs Direct Coupled FET Logic (DCFL), which is capable of faster gate delays, dissipates less power than BiCMOS.

This application note shows how power dissipation is calculated in both BiCMOS and DCFL GaAs and examines and compares power dissipation in the two technologies.

Power Calculations for BiCMOS

Little or no static power is dissipated in most practical topologies of BiCMOS gates because current is used exclusively to charge and discharge load capacitance. BiCMOS ASIC design manuals instruct the user to compute the internal cell power dissipation by multiplying a factor, whose units are microwatts/(gate-MHz), by the frequency of operation. This result is then multiplied by the total number of cells in a given design derated by an arbitrary fraction representing the number of gates switching. This latter derating factor ranges from 0.2 to 0.4 depending on the design at hand. The composite power is calculated using the following formula:

$$P_{internal} = F A_V G P_{gm} \qquad (1)$$

Where:

F = the highest frequency in MHz for gates in the design

A_V = average fraction of the gates which are switching at a given time

G = the total number of gates in the design

P_{gm} = the power per gate-MHz (typically between 20 and 40 microwatts/gate-MHz)

To obtain accurate results from a particular design, however, it would be a mistake to use the A_V estimation factor blindly. Not using any derating factor could also result in an incorrect estimate of the power dissipated in a sequential circuit. Between two successive registers in a sequential circuit there may be several levels of logic. As a result, the effective frequency seen by any one gate in the chain of gates between registers can be substantially lower than the clock frequency applied to the registers. For small designs it is practical to explicitly calculate the effective frequency of operation of each gate and obtain an accurate understanding of power dissipation.

As an example please refer to the benchmark circuit of Figure 1. Here several stages of logic are placed between two flip-flops. The maximum frequency seen by any gate other then the flip-flops is one half of the flip-flop frequency. This is due to the fact that the output of a flip-flop can only toggle at one-half its clock frequency. In addition, there is a statistical probability of 0.5 that the output of a given gate or flip-flop will remain at its previous logic state (assuming an equal number of ones and zeros in the incoming data stream) in which case no power is dissipated since a transition did not occur.

Power Dissipation:
BiCMOS vs GaAs

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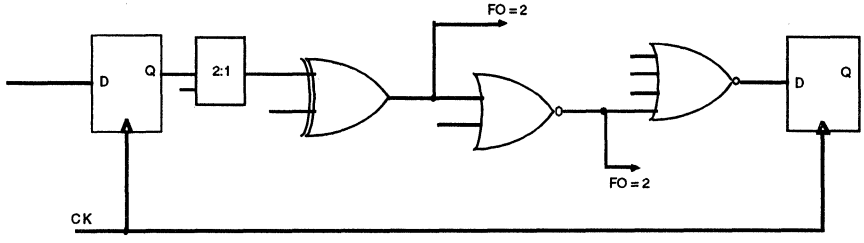
Figure 1: Benchmark Circuit.



Note: This circuit is analyzed in the ntext to compare its power dissipation vs. frequency when implemented in BiCMOS and GaAs.

We can split the problem into two; the power dissipated in the flip-flops and the power dissipated in the gates. For the flip-flops the power can be estimated by:

$$Power = F(0.5)GP_{gm} \qquad (2)$$

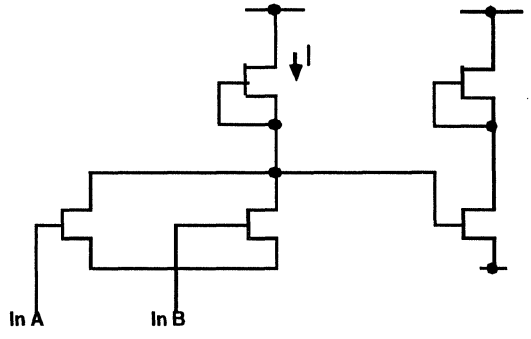
and for the gates in between:

$$Power = F(0.5)(0.5)GP_{gm} \qquad (3)$$

Power Calculation for DCFL GaAs Circuits

Unlike CMOS or BiCMOS, DCFL GaAs circuits have a power dissipation which is independent of logic state or frequency of operation. The reason for this can be seen by examining Figure 2 which depicts a typical DCFL NOR gate driving an inverter. The DCFL structure is composed of a pull up depletion FET and one or more pull down enhancement FETs. The NOR operation is possible because when both pull down FETs are off (corresponding to a logic low at each input) the logic gate's output voltage rises to a valid logic high. However, when one or more pull down FETs are on (corresponding to a logic high at their input) the pull down FET sinks all of the pull up FET current while maintaining a very small Vds. As a result a valid logic low is created at the gate's output.

Figure 2: DCFL Logic



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Power Dissipation: BiCMOS vs GaAs

GaAs FETs, unlike silicon MOS devices, do not have an insulator between the gate and channel region. Instead they employ the depletion region of a schottky barrier junction to modulate drain to source current. This schottky diode will conduct current between the gate and source when forward biased.

In normal DCFL operation, a valid logic high voltage is determined by the forward biased voltage of the gate to source diode. As a result the load current, I, of a DCFL gate will be used to forward bias the gate to source diode of a subsequent logic gate.

In normal operation the current consumption of a DCFL logic gate is constant. Current is simply steered either into the pull down FET in a logic low condition or into the gate to source diode of a subsequent logic gate in a logic high condition. For high speed logic this situation is ideal because current, and subsequent voltage, "spiking" on power supply lines is eliminated.

Therefore, when calculating the power dissipation of a DCFL based chip, the power dissipation reported for an individual logic macro is valid for any frequency at which it can operate.

Benchmark Circuit

To get an idea of the range of speeds and power dissipations achievable in both BiCMOS and GaAs technology we turn our attention again to the benchmark circuit of Figure 2. Table 1 shows the delay for each macro in both BiCMOS and GaAs technology. For the BiCMOS portion of this analysis the NEC BiCMOS-5 design manual was used. The Vitesse FURY manual was used for the GaAs portion.

As seen from Table 1 the delays for both rising and falling output waveforms were calculated. Because NOR gates cause signal inversion the worst case delay through a network must be calculated by evaluating all realistic propagations through the cascade of gates taking signal inversions into account. The worst case path for each situation is designated by arrows in Table 1.

Table 1: Macro Delay

MACRO	DELAY (BiCMOS)		DELAY (GaAs)	
	Rising	Falling	Rising	Falling
F/F CLK» Q	2.75	2.59	0.59	0.36
2:1 MUX (Fo = 1)	1.93	2.10	0.61	0.28
2 input XOR (Fo = 3)	1.66	2.10	1.34	0.45
2 input NOR (Fo = 3)	1.26	0.50	1.15	0.56
4 input NOR (Fo = 1)	2.88	0.45	0.49	0.26
F/F Setup Time	0.25	0.25	0.14	0.14
Rising Delay	9.97 nS		3.73 nS	
Falling Delay	9.98 nS		3.20 nS	
Max Operating Freq.	100.2MHz		268.1 MHz	

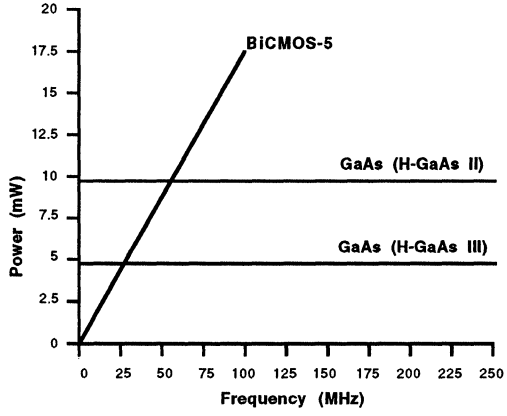
Power Dissipation:
BiCMOS vs GaAs

Application Note 10

Table 1 indicates that, for the benchmark circuit, the maximum frequency attainable in BiCMOS is 100.2 MHz. GaAs technology is capable of a 268.1 MHz frequency. The GaAs macros selected for this particular analysis are optimized for low power dissipation. As a result a factor of 2.7 improvement in speed is observed between GaAs and BiCMOS. A greater investment in power could yield speed improvement factors of between four and five.

Table 2 and the corresponding graph in Figure 3 (following page) depict the power dissipated by each technology as a function of frequency for the benchmark circuit. The power for the BiCMOS circuit was calculated using equations (2) and (3). The Pgm value NEC attributes to their BiCMOS-5 process is 0.038 mW/MHz.

Table 2: Macro Power



As seen in Figure 3, the crossover point between the linear BiCMOS power curve and the constant GaAs power curve occurs at about 60 MHz with the H-GaAs II process and at about 30 MHz with the H-GaAs III process. Since, for the circuit in question, BiCMOS is limited in frequency to about 100 MHz one can only speculate about the power it would dissipate if capable of higher frequencies. However, since the curve is linearly increasing it is safe to say that at frequencies above 150 MHz BiCMOS power dissipation is unreasonably high.

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Power Dissipation: BiCMOS vs GaAs

Figure 3: Power Dissipation vs. Frequency for Benchmark Circuit

BiCMOS

FUNCTION	BiCMOS-5 MACRO NAME	POWER DISSIPATION (mW)			
		25MHz	50MHz	80MHz	100MHz
Flip-Flop	F641	1.42	2.85	4.56	5.7
2:1 MUX	F571	0.47	0.95	1.52	1.9
2-Input XOR	F511	0.47	0.95	1.52	1.9
2-Input NOR	F202	0.24	0.475	0.76	0.95
4-Input NOR	F204	0.24	0.475	0.76	0.95
Flip-Flop	F641	1.42	2.85	4.56	5.1
		4.26	**8.55**	**13.68**	**17.1**

Source: NEC BiCMOS-5 Design Manual, Oct. '89
Vitesse FURY Design Manual, v. 3.0

GaAs

FUNCTION	FURY MACRO NAME	POWER (mW)	
		H-GaAs II	H-GaAs III
Flip-Flop	LFPIU	3.1	1.55
2:1 MUX	LMIU	1.3	0.65
2-Input XOR	LXIU	1.7	0.85
2-Input NOR	LN2U	0.33	0.16
4-Input NOR	LN4U	0.33	0.16
Flip-Flop	LFPIU	3.1	1.55
		9.86	**4.92**

Conclusion

BiCMOS, which has earned a reputation as a low power technology, earns that reputation at low frequencies only. Since its power dissipation increases linearly with frequency, GaAs technology actually dissipates less power at frequencies above 60-70 MHz. This capability coupled with the fact that GaAs technology is capable of speeds which range between a factor of 3 to 5 faster than BiCMOS positions GaAs as the dominant technology for any high speed digital application.

Power Dissipation:
BiCMOS vs GaAs

Application Note 10

Application Note 11

The Effects of Simultaneously Switching Outputs in GaAs Devices

Introduction

When one or more outputs of a semiconductor device switch, a change in voltage is effected on the driven signal lines. This change in voltage is in turn received by any inputs connected to those signal lines and interpreted as a change in logic state. Switching a group of outputs simultaneously, however, may cause undesirable effects on the operation of a circuit. These unwanted consequences are generally referred to as simultaneously switching output (SSO) effects. Features have been incorporated into the design of all Vitesse devices (die and packages) which minimize the deleterious effects of SSO's. These effects have been characterized by Vitesse using a test chip personalization of the FURY VSC10K gate array packaged in a multilayer ceramic 211 pin grid array.

The purpose of this application note, therefore, is to help the system designer minimize the probability of device or board level problems associated with SSO's. This will be accomplished by presenting the designer with some of the physics associated with output switching phenomena as well as some of the methods used to alleviate the effects of SSO's.

Statement of Problem

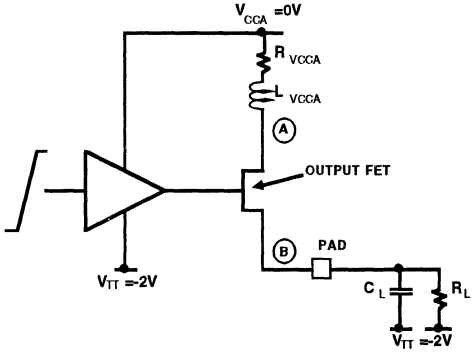
Simultaneously switching outputs can cause the following effects:

- Additional output delay
- Ground or power supply noise at the device
- Ground or power supply noise in the system
- Noise on adjacent signal pins which share supply or ground pins

Electrical Effects of Output Switching: A Basic Model

Figure 1 shows an ECL source-follower output driving a capacitive load and a 50Ω resistor. Figure 2 demonstrates the relationship between the drain voltage of the output FET (node A) and the source voltage of the output FET (node B) as a pulse is propagated through the ECL output. When the output switches from a logic low state to a logic high state, a substantial gate to source voltage is applied to the output FET causing its source-drain conductance to increase dramatically.

Figure 1: ECL SSO Model



The Effects of Simultaneously Switching Outputs in GaAs Devices

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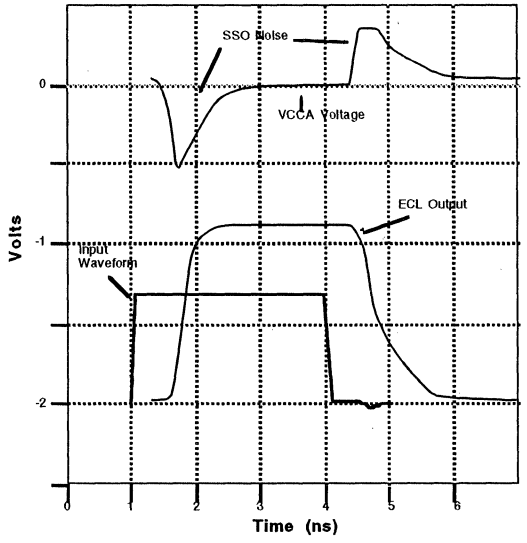
As the transient current is conducted through the device to charge the capacitive load, an instantaneous demand for current is placed on the VCCA (output ground) supply terminal of the output node A. If inductance is present in the VCCA supply path (as shown in Figure 1), the voltage at node A will drop until the inductor is energized and necessary current can be supplied to the output FET. A falling output edge conversely creates a positive transient voltage on the VCCA node. Increasing the inductance in the tends to impede the transient current flow and increase the size of the SSO noise pulses shown in Figure 2. At the system level, these effects are manifested as degradations in the pin-to-pin delay of a device. In addition, if sufficient noise is coupled from the VCCA pins to the logic elements in the device, the states of synchronous elements (registers or latches) in the core of the device may be altered causing the circuit to logically fail.

Figure 2: Power Supply Noise



ASIC Device and Package Features to Alleviate SSO Problems

All of Vitesse's high-performance packages are designed to minimize the electrical problems associated with simultaneously switching outputs. The power and ground pads on each device are fixed. These pads are bonded to separate planes in the multi-layer ceramic package. In order to isolate critical asynchronous inputs (such as clock and reset signals) from noise generated by output switching, outputs on Vitesse devices are confined to the top and bottom of the die (see Figure 4). Signals which are sensitive to noise can then be brought onto the device though input buffers on the left and right sides of the die. This not only isolates the inputs and outputs on the die itself but also minimizes mutual coupling (crosstalk) between output and input bond wires by placing them at 90° with respect to one another.

Application Note 11

The Effects of Simultaneously Switching Outputs in GaAs Devices

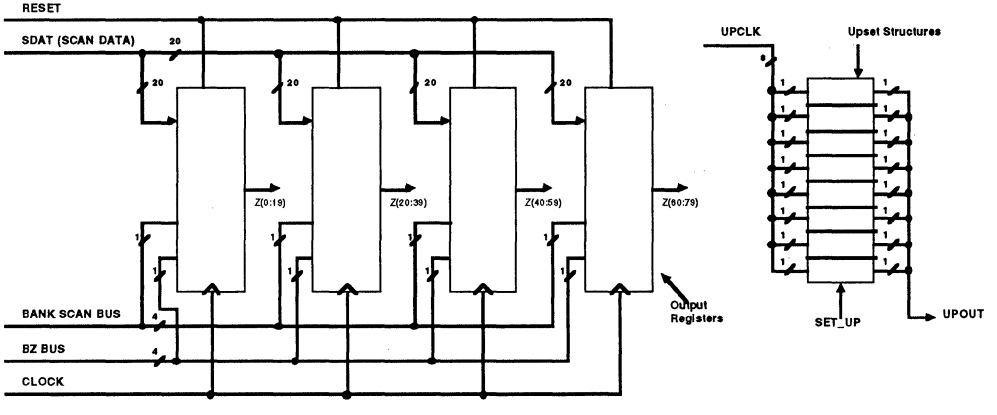
SSO Test Chip Description

Output Registers

In order to gain an empirical understanding of the effects of switching large groups of outputs on a large device, Vitesse has designed and produced a test chip specifically designed to examine these effects. The schematic of the test chip is shown in Figure 3. The SSO test chip, or SSOTC, is implemented using a Vitesse FURY VSC10K gate array in a 211 PGA package. The test circuitry consists of 80 shift registers grouped into four banks of 20 registers each. Each shift register contains four D flip-flops. The four Bank Scan signals allow data on the SDAT (scan data) bus to be clocked into the shift registers on a bank by bank basis. The input CLOCK serves as the system clock for both scanning and shifting operations. To reset all the registers at once, the RESET signal can be asserted. The BZ bus signals allow the user to force the outputs of given bank to logic low without resetting the registers in the bank. Using the scan inputs, patterns which switch anywhere from one up to 80 outputs can be scanned in and clocked to the Z outputs.

As with all FURY gate arrays, the power and ground pins are in fixed locations. In order to minimize the undesirable effects of simultaneous output switching, every four outputs typically share a ground, or VCCA, pad. The VCCA pads are in turn bonded to conductor planes in the 211 PGA package.

Figure 3: Benchmark Circuit



Upset Structures

In order to monitor the coupling of noise back into the SSO test chip, eight upset structures are interspersed around the periphery of the gate array as shown in Figure 4. Each upset structure consists of a D flip flop (FURY LFP3 macrocell) configured so that it will toggle on an active clock edge. The clock inputs of these structures (UPCLK bus) are driven by ECL input pins. The outputs of these structures are connected directly to ECL outputs (UPOUT bus). If the noise generated by the simultaneous output switching is sufficiently coupled to the upset structure input, the flip-flop will toggle, thus signifying an upset failure.

SSO Test Results

Characterization of SSO effects was performed on a Teradyne J953 VLSI tester. In order to execute a given test, all the shift registers are first reset and then logic highs are shifted into the registers whose outputs are to switch. The master clock is then used to shift the pattern to the outputs causing first a group of simultaneous rising edges and then a group of simultaneous falling edges.

Simultaneous Switching Delay

The effects of concurrent switching on output delay were measured by connecting both the CLK signal and one of the Z outputs, to a high speed oscilloscope while the test chip is in the Teradyne test fixture. The tester was then used to force various switching patterns on the part while the relative delay was monitored. During the initial testing, it was determined that most of the observed SSO delay was due to the device test fixture. The test fixture was re-worked to minimize the impedance to the VCCA pins. Subsequent testing showed a minimal delay degradation as increasing numbers of outputs sharing the same VCCA pin were switched. Analysis of the delay data showed the following typical delay per output switched:

$$T_{pd}(sso) = 15\ ps/SSO$$

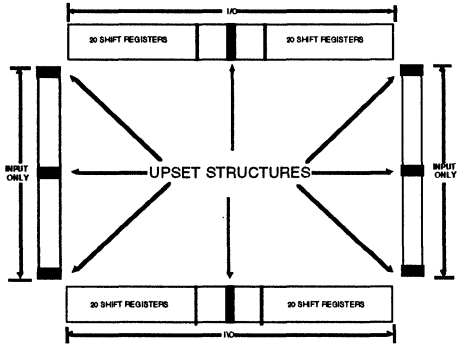
for ECL outputs which share a common VCCA pad.

A maximum total delay degradation of approximately 100 ps was observed when switching up to six ECL outputs sharing the same VCCA pad. Increasing the number of outputs switching beyond six, however, appeared to have a negligible effect on the output delay.

Simultaneous Switching Noise

A second phase of testing was performed to characterize the coupling of SSO noise to input pins. For these tests, various combinations of the Z outputs were switched and the states of the upset structure outputs (UPOUT bus) were monitored. No upset structure failures were observed when switching up to 40 outputs simultaneously. Results for more than 40 outputs switching were inconclusive due to the noise inherent in the VLSI test environment.

Figure 4: SSO Test Chip Block Diagram



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The Effects of Simultaneously Switching Outputs in GaAs Devices

As previously noted, however, SSO noise in the device appeared to be primarily a localized effect. The design of the pad ring on the FURY 10K as well as the design of the 211 PGA itself appears to accommodate the switching of all 100 ECL outputs on the device simultaneously with no effect on internal logic states.

System Design Recommendations for Minimizing SSO Effects

To minimize the possibility of SSO related problems in a given system, precautions should be taken in the arrangement of the inputs and outputs on the ASIC as well as in the construction of the board on which the integrated circuit(s) will reside. The following guidelines summarize these precautions.

ASIC and Board Design Guidelines

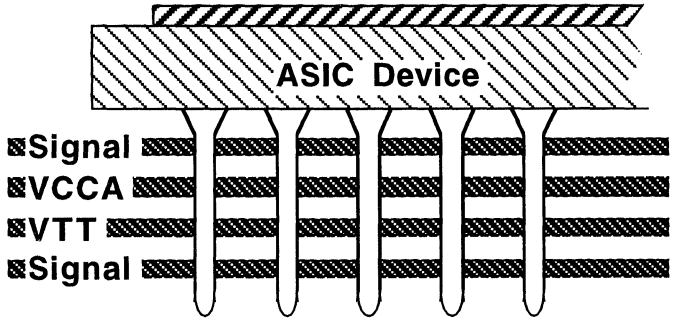
1. Place all clock, set, or reset signals on the ASIC at least six pads away from any output.
2. When designing a custom pad ring,a) a VCCA pad should be allotted for each set of four ECL or GaAs outputs, and b) two VCCA pads and a VTTL (+5 V) pad should be allotted for each set of eight TTL outputs.
3. A large power plane should be used on the PC for distribution of VCCA (Figure 5).
4. The peak switching current should be estimated for the worst case number of SSOs per device and adequate bypass capacitance should be added to satisfy the transient VCCA and VTTL current needs.

Bypass Capacitor Recommendations

Bypass capacitors must be used in high frequency (>100MHz) designs to filter out high frequency variations in the power supply voltages at the device power inputs and on the board. The following bypassing is recommended.

1. A 0.01μF high frequency capacitor should be placed between ground (VCCA) and each V_{TT} (-2Volt) pin as close to the V_{TT} pin as possible.
2. A 1 to 10 μF capacitor should be placed on the board at the power supply inputs to filter out variation in the power supply with longer time constants (e.g. power supply noise at the system clock frequency.)

Figure 5: Recommended Ground Distribution



The Effects of Simultaneously Switching Outputs in GaAs Devices

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Application Note 13

Calculating Path Delays in FX Gate Arrays

Introduction

The following information is provided to aid in estimating AC path delays in the FX Series of gate arrays. A delay equation is a first order approximation of the actual delay and is a convenient way to estimate delays with manual calculations. The simulation tools Vitesse provides in its software suite use a delay equation that is far more sophisticated. For this reason, simulation delays will not match perfectly with hand calculations using this model. For most preliminary investigations, however, the following delay equation is sufficient.

Delay Equation

The delay for each macro is expressed in terms of an equation which specifies the delay as a function of intrinsic delay, pin loading, metal length, pin drive, and derating based on a composite measure of process, temperature, and voltage. The standard form of the delay equation is shown below.

$$\text{DELAY} = \left[T_P + \frac{\Sigma N_I}{N_O} K_1 + \frac{ML}{N_O} K_2 \right] K^*$$

For output macros the following equation is used for the delay from A to PAD:

$$\text{DELAY (A to PAD)} = \left[T_P + k T_p \; K_1 (C_L) \right] K^*$$

For TTL output macros the following equation is used to determine the TRI to PAD delay:

$$\text{DELAY (TRI to PAD)} = \left[T_P \right] K^*$$

where:

T_P	=	The intrinsic delay of the macro for fan-out = 0, 0 mm of wire, and typical conditions (ps)
ΣN_I	=	Sum of the AC input loads being driven by the output (fan-out)
ML	=	Metal length being driven by the output (mm)
N_O	=	Drive capability of output (dimensionless)
K_1	=	Fan-out derating factor (ps/fan-out)
K_2	=	Metal load derating factor (ps/mm)
K^*	=	Composite derating factor (dimensionless)
C_L	=	Load capacitance (pF)
kT_P	=	Load dependent delay (ps/pF)

Calculating Path Delays in FX Gate Arrays

Application Note 13

The fan-out factor, K_1, and metal load factor, K_2, are parameters which have different values for low to high and high to low output signal transitions. They are used to convert the driven load drive strength ratios into time units. Their values are given in Table 1.

Table 1: Fan-Out (K_1) and Metal Load (K_2) Derating Factors

Factor	*Transition Low to High* $(T_{PLH})^1$	*Transition High to Low* $(T_{PHL})^2$	*Units*
K_1	14	23	ps/f.o.
K_2	86	86	ps/mm

Notes: 1) Applies to propagation delays with an output signal transition from low to high.
2) Applies to propagation delays with an output signal transition from high to low.

The composite derating factor, K*, given in Table 2, represents the extreme cases of process, temperature and voltage.

Table 2: K* Composite Performance Derating Factors

Factor	*Transition Low to High* $(T_{PLH})^1$		*Transition High to Low* $(T_{PHL})^2$	
	Min	*Max*	*Min*	*Max*
K*(Commercial)	0.30	1.01	0.30	1.04
K*(Industrial)	0.30	1.16	0.30	1.15

Notes: 1) Applies to propagation delays with an output signal transition from low to high.
2) Applies to propagation delays with an output signal transition from high to low.

The information required to estimate path delays is found in the macro library contained in the FX Series Gate Array Design Manual, version 2.0. Each data sheet in this library contains the macro name, functional description, cell utilization, the macro's icon as it appears on the workstation screen, a logical truth table, intrinsic delay, power dissipation, and loading factors.

The propagation delay (T_P) for every path through the macro is an intrinsic number based on a fan-out of 0, a wire load of 0 mm, and junction temperature of 25° C. They do not represent actual delay, but are used as the first entry in the delay equation. The loading factors give the fan-in load factor (AC and DC) for input pins (N_I) and the output drive (N_O)(AC and DC) which each of the macro outputs provide.

Application Note 13

Calculating Path Delays in FX Gate Arrays

Estimating Metal Lengths Before Place and Route

The following formula should be used to predict the metal interconnect length on a critical path net when estimating timing using hand calculations. This formula assumes that all macros have been hand placed to optimize metal interconnect lengths or have been grouped into sections smaller than a few thousand gates each prior to automatic placement.

$$\mathbf{ML} = (\mathbf{N}-1)0.17 \text{ mm}$$

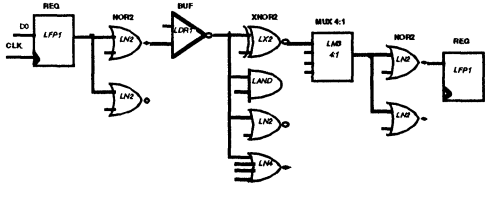
where:

ML = predicted metal interconnect length in mm
N = number of connections on the net

Figure 1: Sample Critical Path Calculation

Sample Critical Path Calculation

In the example at right, a critical path interconnect length of 0.17 mm of wire per driven input is assumed. To calculate the maximum clock frequency under worst case conditions through the path, the worst case delay must first be determined. A summary of this calculation is shown below.



Macro	Signal	$T_P + \frac{\Sigma N_I}{N_O} K_1 + \frac{ML}{N_O} K_2$	K*	Delay
REG	rise	180 + 52.7 + 24.8	1.01	260.1
	fall	290 + 42.3 + 16.6	1.04	362.9
NOR2	rise	80 + 26.3 + 24.8	1.01	132.4
	fall	50 + 17.4 + 13.7	1.04	84.3
BUF	rise	60 + 71.7 + 22.5	1.01	155.7
	fall	40 + 52.2 + 13.7	1.04	110.1
XNOR2	rise	340 + 8.8 + 24.8	1.01	377.3
	fall	310 + 7.4 + 17.4	1.04	348.2
MUX41	rise	210 + 59.8 + 28.1	1.01	300.9
	fall	270 + 44.4 + 17.4	1.04	345.1
NOR2	rise	80 + 26.3 + 24.8	1.01	132.4
	fall	50 + 17.4 + 13.7	1.04	84.3
REG t_{SU} (set-up)	rise	100 + — + —	1.01	104
	fall	100 + — + —	1.04	104

NOTE: Worst cast derated setup time is used irrespective of signal transition.

Possible Delay Paths:

1. T_{RISE}(REG1) + T_{FALL}(NOR2) + T_{RISE}(BUF) + T_{FALL}(XNOR2) + T_{FALL}(MUX41) + T_{RISE}(NOR2) + T_{SU}(REG)= 1429.8 ps
2. T_{FALL}(REG1) + T_{RISE}(NOR2) + T_{FALL}(BUF) + T_{RISE}(XNOR2) + T_{RISE}(MUX41) + T_{FALL}(NOR2) + T_{SU}(REG)= 1471.9 ps

Total Worst Case Path Delay:

1471.9 ps

Maximum Clock Rate:

1/1471.9 ps =679 MHz

Calculating Path Delays in FX Gate Arrays

Application Note 13

Macro Placement

In most designs a large block of logic will be partitioned into smaller sections called soft groups. Autoplacement will be improved by the specification of soft groups. The purpose of soft groups is to specify to the router those macros which should be placed in proximity to each other. In addition, you can specify timing assurance restrictions. These will also positively influence the correct placement of your design.

The most accurate method for estimating interconnect lengths is to have Gate Ensemble auto-place your design. Placement is about two times faster than place and route combined. The fully placed design can be annotated using a Vitesse-provided intermediate back annotation program called VSCIBA. In addition, a Vitesse-provided pre-placement tool (VSCGPRE) can be used to modify the placement obtained with autoplacement to iterate the placement.

A second option is to use the Intermediate Back Annotation (VSCIBA) program directly. This program will calculate the interconnect lengths based on the manhattan distance of all nets between placed macros. The placement is provided by the user in the form of the pre-placement file. If the design is fully placed and meets the desired timing using VSCIBA there is a very good chance that the first actual place and route will result in acceptable timing performance.

Further detailed discussion on timing driven placement can be found in the FX Series Gate Array Design Manual, version 2.0.

Estimating Metal Length for Automatic Place & Route

In rare instances a customer may wish to have his full design automatically place and routed. A statistical analysis of auto-routed FX personalizations has shown that the metal length per connection has a probabilistic distribution which varies with the size of the array. The following equation may be used to predict the interconnect length for a fully auto placed design based on the number of connections on a net. Note that the number of connections includes the output. For example, if a gate is driving one other gate, the number of connections, N, is equal to 2.

$$ML = (N + K)L$$

where:

ML = predicted metal length in mm
N = number of connections on the net
K = array constant (see table below)
L = length constant (0.25 mm for FX auto-placed macros)

Table 3: Array Routing Length Constants

Array	*K*	*Array*	*K*
FX20K	1	FX200K	4
FX40K	1	FX350K	7
FX100K	1		

Application Note 14

Working With The 344 Pin LDCC Package

Introduction

The 344 pin LDCC is a state-of-the-art leaded ceramic chip carrier used to package the VSC864 Crosspoint Switch and the VSC30K Gate Array. This surface mount package has many advantages, including high density and high pin count. These advantages are coupled with several important considerations for board designers. This application note lists hardware requirements and sources in addition to assembly guidelines using the socket and carrier.

1. Hardware Requirements

As board designers transition from prototypes to high volume production, needs will arise ranging from socketing to pick and place robotic equipment. The companies mentioned below provide sockets and carriers, lead trim equipment, and robotic place equipment. Similar equipment may also be available from other sources.

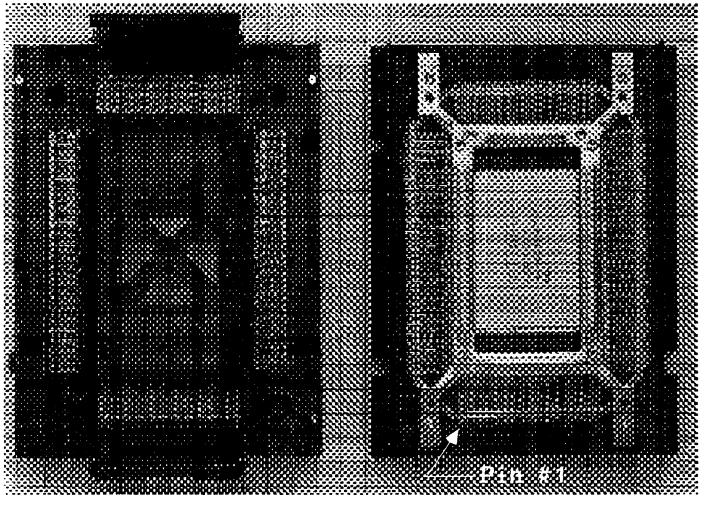
A. Sockets and Carriers

For prototyping at lower clock frequencies (up to 200 MHz) Vitesse has developed a socket that must be used with an accompanying carrier. The socket and carrier can be purchased from Vitesse. Part numbers and pricing are listed below:

Table 1: Pricing Table

Vitesse Part #	*Unit Price (Quantity 1-10)*
344 LDCC Socket	$395.00
344 LDCC Carrier	$40.00

Figure 1: 344 Socket and Carrier



Working With the
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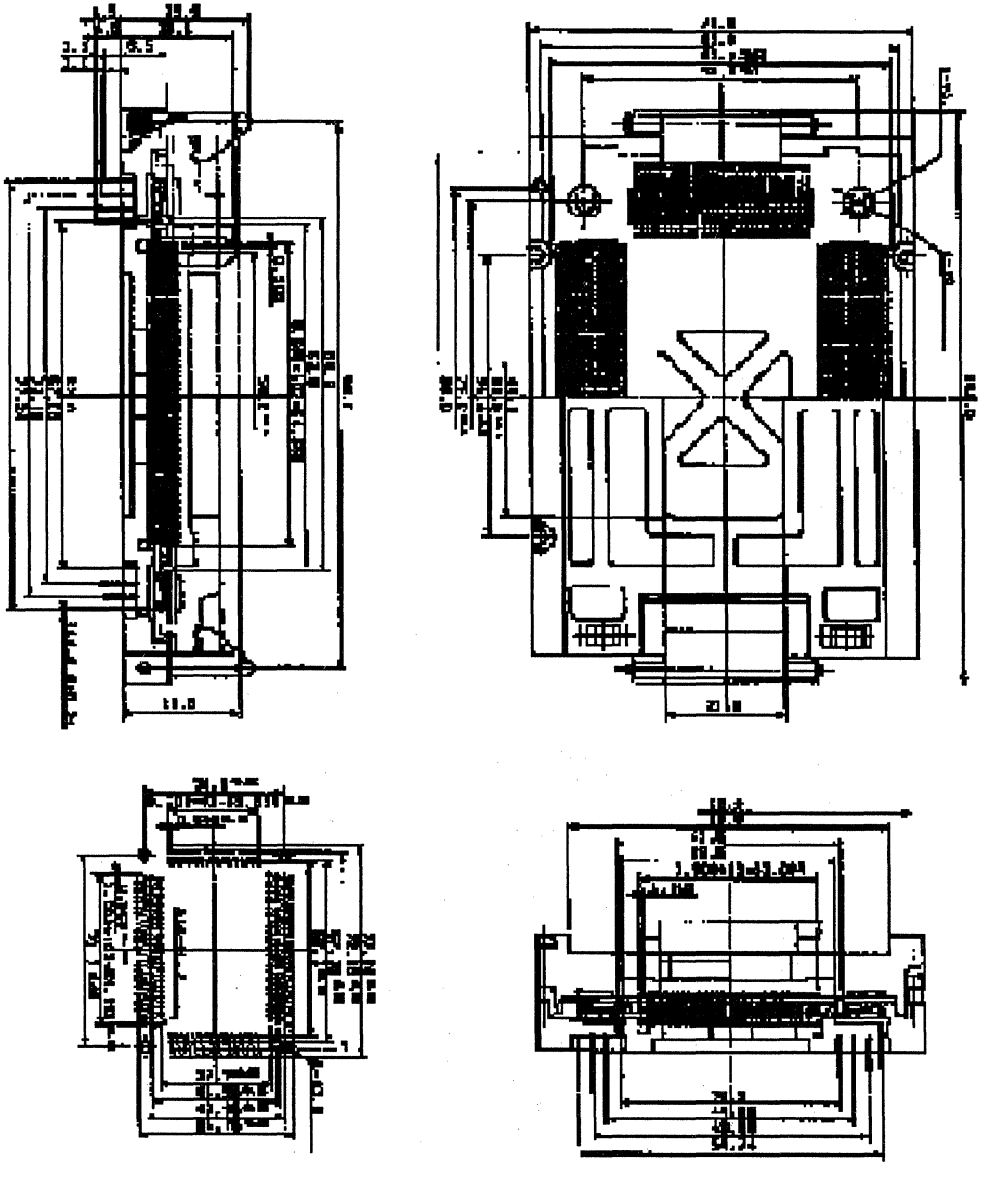
Figure 2: 344 Socket and Carrier Dimensions



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Working With The 344 Pin LDCC Package

When using the socket and carrier it is important to note that the heat spreader will now be facing down towards the PCB. This means that pin 1 is now at the upper right hand corner of the PCB rather than upper left. The pinout on the socket will also now run clockwise rather than counterclockwise.

When inserting the 344 LDCC into the carrier the " V" (indicating pin 1) should line up with the pointer (▲) on the carrier.

B. Lead Trim and Form Equipment

In order to reduce the PCB area which the 344 LDCC occupies, many customers will want to trim and form the leads. Fancort is a leading supplier of this equipment. Their address is listed below:

Fancort
31 Fairfield Place
West Caldwell, NJ 07006
(201) 575-0610

C. Robotic Placement Equipment

Automatic pick and place equipment for packages with 20 mil centers is available from the following sources:

Table 2: Vendor Table

Manufacturer	*Model*
Taltek 148-D Aero Camino Goleta, CA 93117 805/968-2127	FPS360 (Also does trim and form.)
Fuji (See your local sales rep for further information.)	IP series with 54 mm field of view

Working With the
344 Pin LDCC Package

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Procedures for Attachment to a Printed Circuit Board

The technique described below requires considerable expertise. Vitesse therefore recommends using a third party vendor (such as Tetratech or others) which has experience with fine pin pitch packages to perform the operation.

Tetratech
155 Granada Street, Suite Q
Camarillo, CA 93012
(805) 482-1792

The following steps should be taken when assembling on a "hybridized" PCB (printed circuit board integrated with through hole and surface mounted components). **Sequence of assembly is key**:

1.0 Insert all through hole components on the component side of the PCB EXCEPT those in close proximity with the fine pitch LDCC.

2.0 Epoxy ceramic chip capacitors to thesolder side of the PCB.

2.1 Epoxy should contact body of part only. It should not spread to the terminations.

2.2 Cure the epoxy according to the manufacturer's recommended curing schedule.

3.0 Wave solder the board so that the solder side of the board goes through the wave.

3.1 63% Sn / 37% Pb solder is preferable.

3.2 Use RMA flux.

3.3 The terminations of the ceramic capacitors will wet and affix in this process. The epoxy will hold them in place.

4.0 Clean the board in a commercial board cleaner thoroughly.

5.0 Now we are ready to place the LDCC [Note: The following procedure for LDCC placement applies to relatively low volume applications (fewer than 20 parts per day). Semi-automatic and automatic equipment and procedures are appropriate for higher volume applications. The associated variations and complexities of these procedures are not applicable to the present discussion.]

5.1 The surface and pads on which the LDCC is to be attached must be as flat as possible. Do not pre-tin the pads. Bare copper or plated pads are OK. The resulting meniscus shapes are not conducive to fine pitch attachment.

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Working With The 344 Pin LDCC Package

5.2 Apply a very thin layer of RMA flux over the pads.

5.3 If an appropriately fitted vacuum tweezer is not available, handle the part manually. Use finger cots and apply appropriate ESD safeguards.

5.4 Place the LDCC in its proper orientation under a magnifying lamp. Stronger magnification may be necessary depending upon the visual acuity of the operator.

5.5 Use .015 diameter RMA core, 63/37 solder to tack down corners of the LDCC diagonally. This procedure holds the component in place during the remaining soldering operation.

5.6 Use a fine tip soldering iron to solder each of the remaining LDCC leads. Use an Exacto blade or other fine instrument to carefully orient leads into exact position.

6.0 Hand solder the remaining through-hole and SMD components that are in close proximity to the LDCC.

7.0 Clean the board of the remaining RMA flux.

8.0 Inspect the soldered leads of the LDCC thor-oughly under 20-30x magnification for solder bridges or other anomalies.

Working With the
344 Pin LDCC Package

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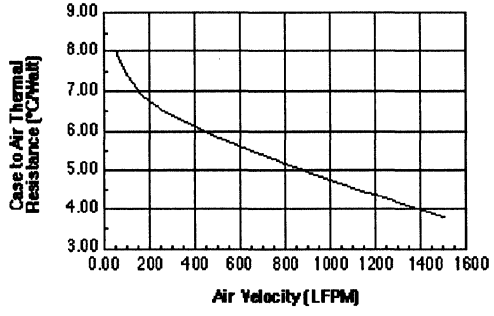
Package Thermal Properties

The 344 pin LDCC package has a set of thermal properties which have been characterized and are shown in the following table and figure. Using this information, the need for a heat sink and the proper air flow over the packages can be determined.

Figure 3: θca vs Air Velocity for the 344 LDCC



Note: All thermal data is shown at sea level

Table 3: θca vs Air Velocity for the 344 LDCC

Air Vel. (Ft./Min.)	*θca*	*Air Vel. (Ft./Min.)*	*θca*
Natural Convection	8.2	400	6.10
50	8.00	500	5.82
100	7.42	700	5.34
150	7.06	900	4.92
200	6.80	1200	4.34
300	6.40	1500	3.76

Trim And Form Equipment

Fancort Industries offers a trim and form press for the 344 LDCC (Fancort part # F-1A14L). For further information please contact Fancort at (201) 575- 0610

Conclusion

The 344 LDCC package offers a significant packing density advantage. It also offers some challenges for companies not accustomed to fine pitch packages. Many large companies including Convex Computers have chosen this package and have it running in volume production. It is our goal at Vitesse to help you through the challenges involved in acquiring this assembly capability.

Application Note 17

Implementing the Fixed Clock Tree in FX Gate Arrays

Introduction

This application note is intended as a guide for implementing fixed clock trees in FX Gate Arrays from Vitesse Semiconductor Corporation. The topics which are covered include:

- System Clock Design Issues
- Design Trade-offs: Fixed Clock Tree vs. Custom Clock Distribution
- Fixed Clock Tree Performance
- Logic Modeling and CAD Issues
- Custom Masterslice Fixed Clock Tree

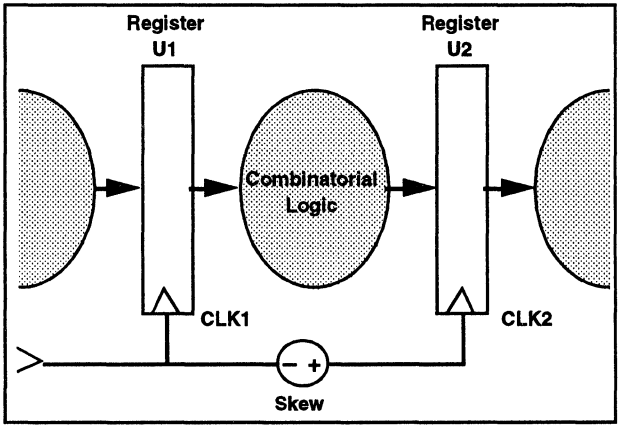
Background

The clock distribution hierarchy in a typical system includes the system level distribution, the board level distribution, and the chip level distribution. In this environment, clock skew, duty cycle, and edge rate can have significant impacts on system performance.

Clock skew is defined as the difference between the time that the critical clock edge arrives at a synchronous element relative to the time it arrives at another synchronous element. Clock skew can affect system performance by causing set-up and hold violations in registered elements.

In a typical sequential system using a pipeline approach as shown in Figure 1, registers are followed by combinatorial logic, followed by additional registers. If the clock skew is positive (the clock arrives at the first register before it arrives at the second), and the logic delay is small, hold violations can result at any system clock frequency. This is known as double clocking.

Figure 1: Typical Sequential System



Implementing the Fixed Clock Tree in FX Gate Arrays

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To avoid hold violations, the following equation must be met:

$$T_{CQ}(\text{min}) + T_D(\text{min}) + T_{RC}(\text{min}) - T_{HOLD}(\text{max}) > T_{SKEW}$$

Where:

T_{CQ}	Signal propagation delay from clock input to data output for register U1
T_D	Signal propagation delay due to combinatorial logic
T_{RC}	Signal propagation delay due to metal interconnect RC effects
T_{HOLD}	Data valid hold time requirement for register U2
T_{SKEW}	Maximum skew between clock signals CLK1 & CLK2

This issue becomes important in circuits such as shift registers or scan chains. If the clock skew is negative (the clock arrives at the second register before it arrives at the first), the logic delay must be decreased or the system clock period must be increased to satisfy setup times. To avoid setup violations, the following equation must be met:

$$T_{CQ}(\text{max}) + T_D(\text{max}) + T_{RC}(\text{max}) + T_{SET\text{-}UP}(\text{max}) + T_{SKEW} < t$$

Where:

$T_{SET\text{-}UP}$	Data valid set-up time requirement for register U2
t	Time for one period of the clock

Two categories of clock skew are defined for ASICs: on-chip skew and chip-to-chip skew. On-chip skew is determined by RC delay, loading variations, and transistor drive variations. This skew can be minimized with the fixed architectures described in Section III, "Clock Tree Architectures". Chip-to-chip skew is determined by board level clock loading and drive variations, and on-chip clock latency variations from die to die. Special clock drivers and board layout techniques can minimize board level clock skew, and clock delay variations from one chip to another can be minimized by using one or more of the following methods:

1) By using special board level clock driver chips with multiple outputs, clock edges can be adjusted to cancel the clock delay on the die.

2) Ceramic delay lines are included in series with each clock line to each chip on the board. Delay lines of various lengths can be added to the board to tailor the clock edge to each part.

3) A variable tap delay line (vernier) can be included on each chip. This delay line will add extra clock delay to faster parts for clock edge alignment with slower parts.

4) A Phase-Lock-Loop (PLL) can be included on each chip to lock the edge of the internal clock to a lightly loaded global reference clock edge.

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Implementing the Fixed Clock Tree in FX Gate Arrays

Items 1, 2, and 3 require a clock monitor output signal on each chip. Item 3 requires several input signals to adjust the clock edge. Item 4 requires a reference clock input signal.

The clock duty cycle can become distorted as the clock signal travels through several levels of buffering. Flip-flops have minimum clock pulse width specs that must be satisfied. In addition, latch based designs must maintain close to 50% duty cycle in order to achieve high clock frequencies.

Clock edge rate can affect both skew and pulse width. The input switching thresholds of clock buffers and flip-flops vary due to process, temperature, and power supply variations. This variation translates into clock skew. The amount of skew is defined by the following equation:

skew = (Vsw mismatch)/(edge rate V/ns)

For very slow edge rates, a small threshold mismatch can cause race conditions even within latches and flip-flops. Also, if slow edge rates keep the clock signal from reaching full voltage swing. Minimum pulse width violations can result. To avoid these violations, it is desirable to maintain edge rates that are less than 20% of the clock period and a maximum of 1 ns for high speed designs.

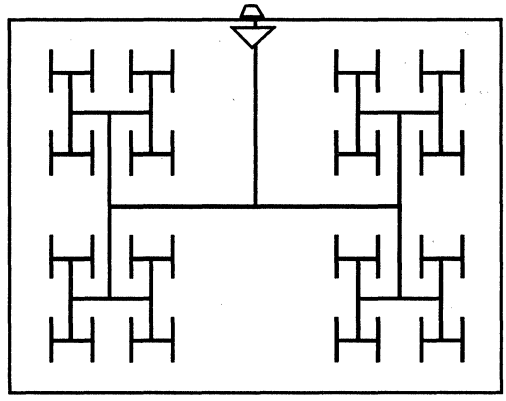
Clock Tree Architectures

Clock tree architecture and layout are key elements affecting skew and edge rate. When considering clock tree architectures, the main objectives are to minimize overall clock tree propagation delay while maintaining good edge rates (chip-to-chip skew), and to minimize differences in the clock tree branches (on-chip skew). Secondary objectives include minimizing the place-and-route blockages created by the clock tree and providing standard I/O interface levels (ECL, TTL).

The input capacitance on the clock input buffer must be minimized so that it does not represent a large capacitive stub to the PC board clock transmission line. Typical ASIC clock trees have to drive a total capacitance in the 100s of pF range. To drive this capacitance, current is typically amplified through several stages of buffers while maintaining minimum capacitance to the input pin. The goal is to minimize the number of buffer stages while maintaining good edge rates and low duty cycle distortion. Minimum and maximum clock tree delays can be established by multiplying the total clock tree delay by the composite ASIC derating factors. The difference between these delays is the device's contribution to chip-to-chip skew. Therefore, minimizing total clock tree delay will also minimize chip-to-chip clock skew.

On-chip skew can be minimized by carefully balancing the clock tree. The traditional approach is to use a hierarchy of 'H' patterns as shown in Figure 2. Typically, additional buffers are used at the four ends of the 'H'. This approach provides a very well balanced RC delay to any local driver on the die. It also minimizes RC delay by having several buffer stages along the RC path. However, the 'H' pattern approach also has several disadvantages including:

Figure 2: Clock Tree with Three Levels of 'H' Patterns



1) Several stages of clock buffers are typically used, increasing clock tree delay and chip-to-chip skew.

2) Local driver delay variations must be accounted for in the on-chip skew budget.

3) Local clock buffers are placed in the middle of the array, restricting the placement of large on-core mega-cells such as register files.

4) There are a limited number of local clock buffers at the end of the tree. Therefore, a significant portion of the clock tree will be routed with a place and route tool, adding to on-chip skew.

5) Depending on clock tree buffer placement, embedded memory blocks can cause unbalanced clock branches. Rebalancing the clock tree may require added buffer stages, leading to higher chip-to-chip skew.

The clock tree must also support I/O buffers and embedded memory blocks. Many designs use registered I/O synchronized to the core logic. In addition, pipelined memories have registered inputs and outputs. Both of these structures typically connect to the clock tree and must maintain the same clock skew specification as other registers in the design. In many cases, the clock tree must be tailored for these applications.

Skew can also be reduced by routing the clock on the thickest metal available. This will minimize RC delay. The RC product for a 1mm length of metal versus metal width is shown in Figure 3. In this example, widening the line greater than 5 microns has little effect on the RC delay, because the parallel plate capacitance becomes dominant above this width. Figure 3 clearly shows that Metal 2 and Metal 3 have much lower RC delay than Metal 1. The thicker metal in Metal 2 and Metal 3 reduces resistance but does not significantly affect capacitance. The thicker dielectrics surrounding these metals also contribute to their lower RC delay.

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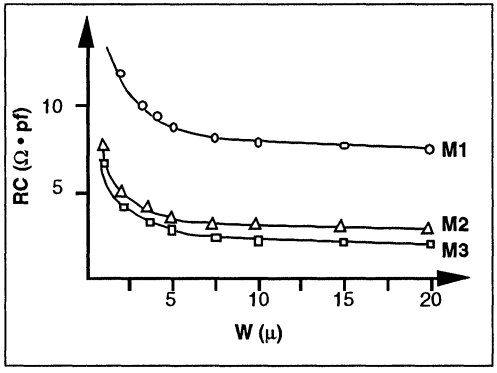
Implementing the Fixed Clock Tree in FX Gate Arrays

Figure 3: RC Product for 1mm Wire vs. Wire Width (Approx for H-GaAs III)



Vitesse Clock Trees

Vitesse has designed fixed clock trees for the FX gate array family to minimize most of the problems associated with the 'H' clock trees described above. Figure 4 shows the basic architecture and layout of this fixed clock tree. An input receiver at the top of the array drives a single large 'H' pattern through a very large buffer. Across the top and bottom of the array, local drivers feed local clock lines over every utilized column. In the corners, additional local drivers connect to local vertical and horizontal clock lines near the I/O buffers serving any registered I/O requirements. All clock routing is done in vertical Metal 3 and horizontal Metal 2, conforming to the signal routing convention and minimizing place and route blockages. In addition, the thick Metal 2 and Metal 3 used in the clock tree minimizes RC delay as discussed above. Finally, all outputs from the local drivers are shorted together to minimize skew.

The single drawback of the fixed clock tree approach is that the RC paths to each local driver are not identical. However, this adds less than 100ps to the skew on the largest array. This minor disadvantage is far outweighed by its many features including:

1) Only two stages of clock buffers are used, minimizing total propagation delay.

2) Since the outputs of all the local buffers are shorted together, local driver variations are virtually eliminated.

3) The local clock drivers are located only on the top and bottom edges of the gate array core. On-core megacells such as register files can therefore be placed anywhere in the core area.

4) Each usable gate array column has a dedicated local clock driver and clock line. Flip-flops make connections to the local clock lines through short stubs of Metal 2. The small length variations in these Metal 2 stubs add no additional skew.

5) Embedded memory blocks can easily be added by subtracting only local clock lines. This maintains skew balance on the global 'H' clock bus.

Implementing the Fixed Clock Tree in FX Gate Arrays

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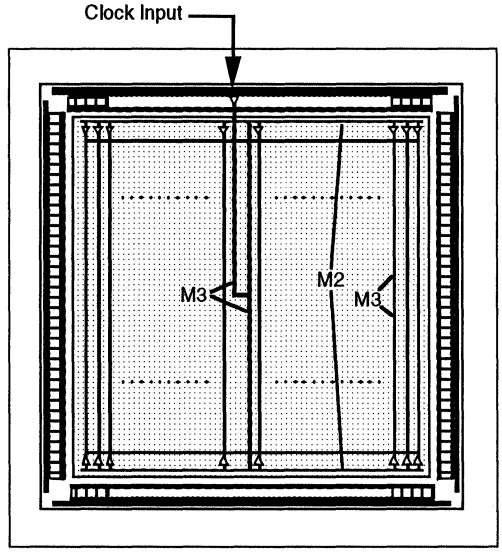
Figure 4: Vitesse Fixed Clock Tree



* Note: drawing not to scale

Vitesse offers two types of input buffers for the clock trees. The ECL buffer is a differential input that can be used on ECL only or mixed ECL/TTL FX gate arrays. If a high-speed clock is required on a TTL only array, this buffer can also be used, with its input levels referenced to V_{MM} (+2V) instead of ground. The second type of buffer is a TTL single-ended input for the TTL only FX arrays.

The I/O buffer and SRAM clock tree interfaces have been designed to add no additional skew to the overall clock tree. On the sides of the arrays, the local clock is routed with a vertical Metal 3 line over the core cells that exist inside the I/O buffer. On the top and bottom of the arrays, the local clock lines are routed in Metal 2 just outside the I/O core cells. To accommodate this, different registered I/O personalizations are used on the sides of the arrays than are used on the top and bottom.

The SRAM layouts contain a horizontal Metal 2 clock line that is part of the compiled SRAM layout. Several local clock buffers are connected in parallel to drive this line depending on the fan-out load.

Table 1 lists some of the key clock tree characteristics for the 5 gate arrays in the FX family. Skew and power dissipation specifications are all maximums. Keep in mind that the across die skew listed is a maximum value. This skew number must be derated along with the logic delays. Also, the numbers listed are for worst case points on the die. The skew will be much smaller (<50ps) for flip-flops in close proximity.

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Implementing the Fixed Clock Tree in FX Gate Arrays

Table 1: ECL Fixed Clock Tree Characteristics

Characteristic	*FX20K*	*FX40K*	*FX100K*	*FX200K*	*FX350K*
Max. Prop Delay (rise)	1200 ps	1540 ps	1610 ps	2020 ps	2460 ps
Across Die Skew	50 ps	70 ps	100 ps	150 ps	200 ps
Chip-Chip Skew	840 ps	1080 ps	1130 ps	1410 ps	1720 ps
Max Frequency[1]	650 MHz	600 MHz	550 MHz	450 MHz	350 MHz
Min Input Pulse	770 ps	830 ps	910 ps	1110 ps	1430 ps
Cells Required[2]	1198	1284	2544	4848	5200
Max. Flip-Flops	1120	1960	3840	7733	8320
Min Flip-Flops	56	92	192	387	416
Max. DC Power	202 mW	316 mW	617 mW	1145 mW	1224 mW

1) Assumes maximum flip-flip utilization.
2) Subtract from raw cell count.

Table 2: TTL Fixed Clock Tree Characteristics

CLK Tree Macro	*FX20KT*	*FX40KT*	*FX100KT*	*FX200KT*	*FX350KT*
Max. Prop Delay (rise)	2220 ps	2560 ps	2630 ps	3040 ps	3500 ps
Across Die Skew	50 ps	70 ps	100 ps	150 ps	200 ps
Chip-Chip Skew	1550 ps	1790 ps	1840 ps	2130 ps	2450 ps
Max Frequency[1]	150 MHz	150 MHz	150 MHz	150 MHz	150 MHz
Min Input Pulse	3000 ps	3000 ps	3000 ps	3000 ps	3000 ps
Cells Required[2]	1198	1284	2544	4848	5200
Max. Flip-Flops	1120	1960	3840	7733	8320
Min Flip-Flops	56	92	192	387	416
Max. DC Power	202 mW	316 mW	617 mW	1145 mW	1224 mW
Max. DC Power (TTL)	1.63 mW	1.63 mW	1.63 mW	1.63 mW	1.63 mW

1) Assumes maximum flip-flip utilization.
2) Subtract from raw cell count.

Implementing the Fixed Clock Tree in FX Gate Arrays

Application Note 17

CAD Interface

This section discusses the clock trees in relation to the Vitesse ASIC CAD flow. Each clock tree is offered as a macrocell in the FX macrocell library. One macrocell is listed for each particular FX array size and are named accordingly; CLK20K, CLK40K, CLK100K, CLK200K, or CLK350K for ECL level clocks and CLK20KT, CLK40KT, CLK100KT, CLK200KT, or CLK350KT for TTL level clocks. The array specific section of the FX Design Manual lists the specific pad numbers for which the fixed clock inputs are reserved.

In utilizing the fixed clock tree the user creates one global clock net and drives it with the special clock tree macrocell during schematic capture. Since the metal in the clock tree is fixed, the change in delay after back annotation is insignificant. Fan-out on the clock tree is automatically extracted from the netlist during netlist compilation so that the overall clocktree delay can be adjusted due to loading. The resulting ERC report will issue errors if the maximum or minimum fan-out is violated for the clock tree in the netlist.

The fixed clock tree input buffer is placed in a reserved position in the I/O pad ring and the subsequent branch buffers cannot be placed by the user. Placement is performed automatically and is therefore transparent to the user. As a result, the number of available cells in the gate array socket set is reduced when a fixed clock tree is chosen because the local clock drivers use 5 or 6 rows of core cells at the top and bottom of the gate array. These rows are automatically subtracted from the total available cells by the ERC when estimating gate array utilization. A Vitesse post-placement software routine has been developed that pre-routes the short Metal 2 stubs connecting the pre-placed flip-flops to the local clock lines. This routine also balances the loading across the array. Final timing simulations including on-chip skew are run on LASAR before CDR. Skew is included by using a fixed value, per a table, and adding it to each connection in the clock tree. This skew is the maximum specified for the global clock tree.

Custom Masterslices

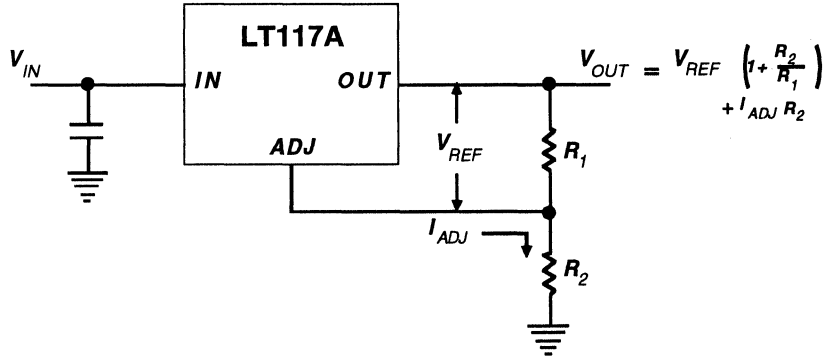
Custom masterslices require modifications to both the clock tree layout and the CAD software. First, local clock lines are removed in the locations of the embedded memory blocks. In some cases, more extensive modifications are required. Next, SPICE simulations are run on the new tree to determine skew and edge rate. Finally, the socket set and pre-routing software must be modified with the new clock tree information. Because of these steps, a masterslice with a fixed clock tree has a higher NRE charge than a masterslice without one.

Application Note 18

Generation of +2V or +3.3V Supplies from a +5V Supply

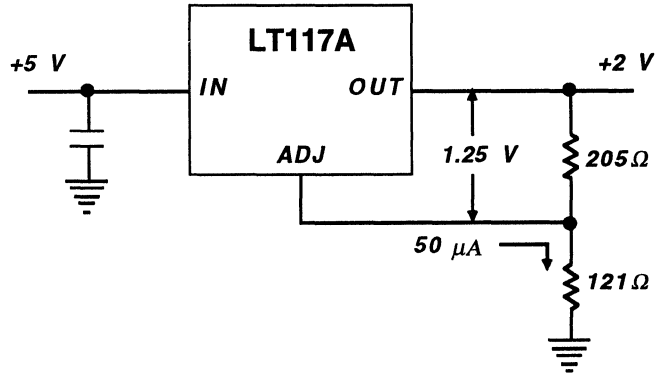
Some Vitesse products require both +2 and +5 Volt power supplies. In the event that a +2 V supply is not available in the system, a simple method exists to generate the +2 V from a +5 V supply. This method involves the use of a low cost voltage regulator. Voltage regulator ICs are offered by several vendors including National Semiconductor Corp., Linear Technology Inc., and Advanced Micro Devices.

Figure 1: Generating +2V or +3.3V with the LT117A



A voltage regulator IC, such as the LT117A made by Linear Technology, is a 3 terminal device. The LT117A develops a 1.25 V reference voltage between the ***OUT*** and the ***ADJ*** terminal (see Figure 1). By placing a resistor, R_1, between these two terminals, a constant current is caused to flow through R_1 and down through R_2 to set the overall output voltage. Normally this current is the specified minimum load current (approximately 5 mA). An additional current, called I_{ADJ}, flows from the ***ADJ*** terminal through R_2. This is a very small and constant current with a magnitude of approximately 50 µA.

Figure 2: Generating +2V from a +5V Supply



Generation of +2V or +3.3V Supplies from a +5V Supply

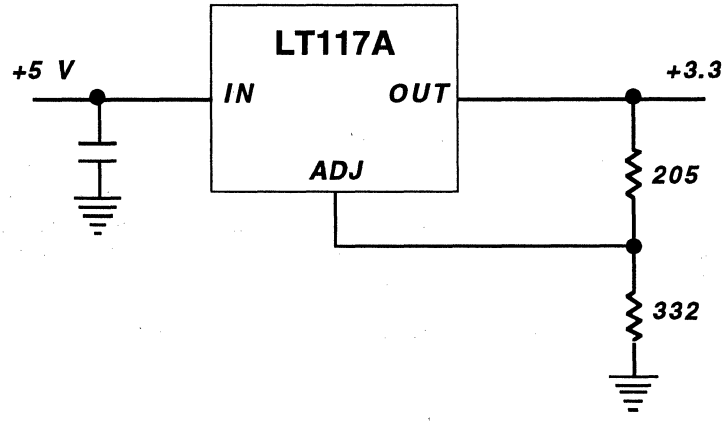
Application Note 18

It can be seen from the equation in Figure 1 that the accuracy of the output voltage is limited by the accuracy of V_{REF} and the tolerance of the R_1 and R_2 resistors. The LT117A has a very tight initial tolerance of V_{REF} which permits the use of relatively inexpensive 1% film resistors for R_1 and R_2 while setting an output voltage tolerance which is compatible with the ±5% need of Vitesse products. If voltage regulators with wider reference tolerance are used (such as industry standard LM117), a trim pot may be needed to set the exact value of the output voltage.

Figure 2 depicts the LT117A with the resistor values needed to generate the +2 V supply. The output current of the LT117A is limited to 1.5 Amps. For systems which use several chips, and regular larger currents regulation can be accomplished by devices such as the LT1038 (also from Linear Technology) which can handle an output current up to 10 Amps. The use of this larger regulator is identical to the LT117A.

Some Vitesse products, such as the VSC7105/7106 chipset, require a single +3.3V supply. Such a supply can be created from a +5V supply with the LT117A with the circuit shown in Figure 3.

Figure 3: Generating +3.3V from a +5V Supply



Application Note 18

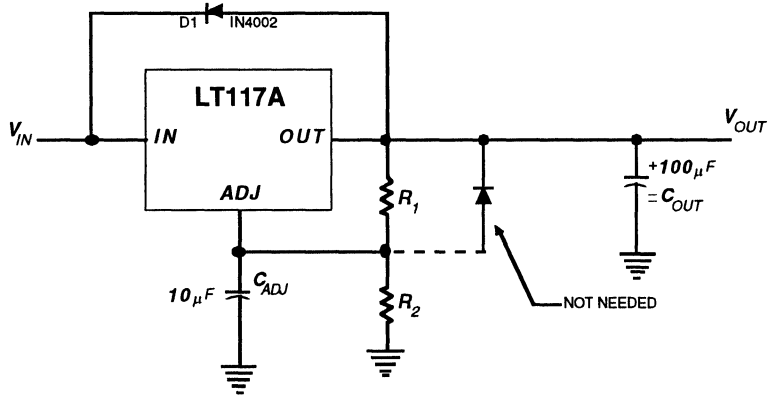
Generation of +2V or +3.3V Supplies from a +5V Supply

Protection Diodes

The LT117A does not require a protection diode from the adjustment terminal to the output as shown in Figure 2. Improved internal circuitry eliminates the need for this diode when the adjustment pin is bypassed with a capacitor to improve ripple rejection.

If a very large output capacitor is used, such as a 100µF shown in Figure 4, the regulator could be damaged or destroyed if the input is accidentally shorted to ground or crowbarred. This is due to the output capacitor discharging into the output terminal of the regulator. To prevent damage a diode D1 is recommended to safely discharge the capacitor.

Figure 4: Implementing Protection Diodes for a Larger C_{OUT}



Generation of +2V or +3.3V Supplies from a +5V Supply

Application Note 18

Application Note 20

Plastic Packaging Moisture Sensitivity Levels

Plastic packages are moisture sensitive. This may cause problems if not attended to properly. This application note describes suggested handling procedures for Vitesse products shipped in plastic packaging.

When the epoxy molding resin used in the plastic package molding process is left in the open, moisture in the air penetrates the package and diffuses internally throughout the package. When plastic packages are subsequently heated during the soldering process, this moisture vaporizes.

To minimize the effects of moisture absorbed in the package, these moisture-sensitive parts must be dry prior to being subjected to the high temperatures of second level assembly. A dry pack and handling procedure has been established to help ensure low moisture levels in the components prior to second level assembly. The dry pack procedure consists of a 24-hour bake at 125°C. After baking, the units are virtually dry. Within one hour of completion of the bake cycle, the units are sealed in moisture-barrier bags with a dessicant bag and a humidity indicator. These moisture-barrier shipping bags provide a shelf storage life of 12 months from the date of sealing, when stored at a temperature of ≤30°C and 60% relative humidity. After this time, the parts must be baked again for 24 hours at 125°C to ensure no moisture related problems during second level assembly.

Moisture absorption depends upon several factors including package size and thickness. This means that each package may have different moisture sensitivity. JEDEC has standardized moisture sensitivity levels with the proposed specification #A112. It specifies 6 levels of moisture sensitivity as well as the handling procedures to be followed at the customer site to protect the parts against moisture-related problems. These levels are summarized in the table below.

Table 1: Levels of Moisture Sensitivity

	Maximum Floor Life			*Packages*	
Level	*Temperature*	*Relative Humidity*	*Time*	*Body Size*	*Lead Counts*
1	≤30°C	90%	Unlimited		
2	≤30°C	60%	1 year		
3	≤30°C	60%	168 hours	14 x 14 x 2.0 mm	52L, 144L QFP
				28 x 28 x 3.5 mm	184L, 208L QFP
				14 x 20 x 2.7 mm	100L QFP
4	≤30°C	60%	72 hours	10 x 10 2.0 mm	52L QFP
5	≤30°C	60%	24 hours		
6	≤30°C	60%	6 hours		

Note: 1) Deduct 1 hour from the maximum floor life time to comprehend the time between bake and drypack prior to shipment to the customer.

Plastic Packaging Moisture Sensitivity Levels

Application Note 20

Handling of Devices at Customer Site

Moisture sensitive devices require specific care at the customer site where second level assembly is performed. The dry pack bags should be inspected prior to use. If the moisture-barrier bags have been opened at any time prior to the expiration date, or if upon opening, the humidity card reads greater than 30% relative humidity, the following precautions must be taken:

- If the humidity card reads greater than 30% relative humidity, the units must be rebaked for 24 hours at 125°C.
- If the expiration date on the dry pack bag has elapsed, the units will require a rebake for 24 hours at 125°C prior to second level assembly.
- The units must be rebaked for 24 hours at 125°C if the moisture-barrier bag has been opened for longer than specified in the previous table: **Levels of Moisture Sensitivity**.

As an example, consider the 28 mm x 28 mm x 3.5 mm, 208L thermally enhanced PQFP. According to the previoous table, this package is a level 3 package. Vitesse bakes the 208L QFP at 125°C for 24 hours, seals it in a dry pack bag within 1 hour of the completion of the bake cycle, and ships it to the customer. Because this package is a level 3 package, it has a maximum floor life of 168 hours. The customer receives the part, opens the bag after confirming that the dry pack expiration date has not passed, and verifies that the humidity indicator reads ≤30% relative humidity. Since one hour is consumed between bake and dry pack, the customer must assemble the 208L QFP within 167 hours of opening the dry pack bag. During this period, the parts should be stored in a controlled environment as indicated in the table.

Vitesse currently ships in high temperature trays that can withstand the 125°C bake temperature. If low temperature trays are used, a low-temperature bake must be used. This has not been specified by Vitesse although other sources have verified that baking at 40°C for 192 hours achieves a moisture level below the critical level necessary time for second level assembly.

Application Note 22

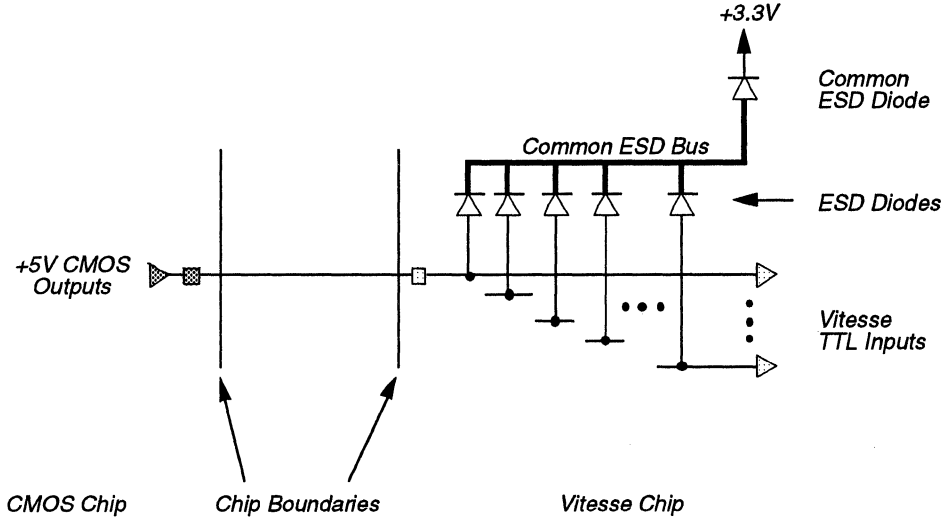
Interfacing Vitesse +3.3V TTL with +5V CMOS

Introduction

As the world transitions from purely 5V systems to 3V systems, there will be a number of systems incorporating both 3V and 5V logic. Driving 5V logic from 3V logic does not present a problem so long as the V_{IH} and V_{IL} limits are met. However, when driving 3V logic from 5V logic, an overdrive condition may occur. This application note discusses potential problems and suggests two interface techniques for driving a 3.3V Vitesse chip with a 5V CMOS chip.

The primary concern when driving a Vitesse TTL input from a +5V CMOS output is exceeding the electromigration limit of the common ESD Bus inside the Vitesse chip. When the signal exceeds V_{TIL}+1V (approximately 4.3V), the ESD diodes become forward biased, (see Figure 1). A number of TTL inputs will share a common ESD bus and if all of the TTL input ESD diodes are forward biased at the same time the current on the common ESD bus can become excessive. Exceeding the electromigration limit on the common ESD bus can cause reliability problems over a period of time. Therefore, Vitesse recommends either limiting the current into the ESD diodes or limiting the V_{OH} (max) seen at the TTL input pad.

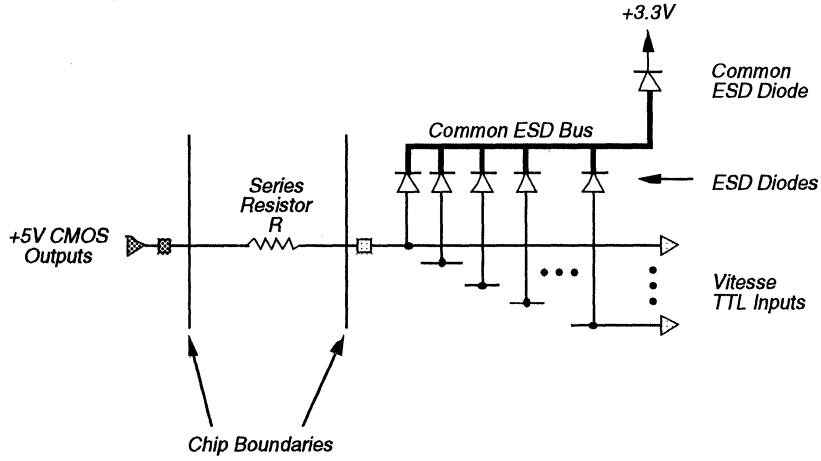
Figure 1: TTL Input ESD Structure



Solution #1, Series Resistor

One solution to the problem is the addition of a current limiting resistor in series with each TTL input, as shown in Figure 2. This will limit the amount of current that each input will contribute to the common ESD bus. The minimum size of the resistor is dependent on the number of TTL inputs sharing the common ESD bus.

Figure 2: Series Resistor



The equation for determining the minimum resistor size is as follows:

$$R_{MIN} = 50N_{IN},$$

Where:

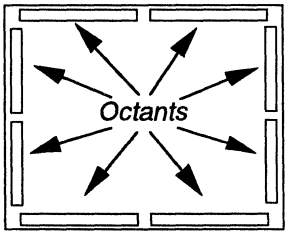
R_{MIN} = the minimum resistor size

N_{IN} = number of inputs from a common octant

The maximum allowed N_{IN} is 10.

The Maximum N_{IN} value will degrade V_{IL} noise margin by 250 mV. N_{IN} is determined by input location and is therefore design dependent. An octant is a group of I/O's that share a common ESD bus. As the name implies, there are 8 octants per chip, as shown in Figure 3.

Figure 3: Octants on a FX Vitesse Die



Power dissipated across a single resistor can be calculated using the following equation:

$$P = (V_{OH} - (V_{TTL}+1))^2 R,$$

Where:

V_{OH} = the CMOS output high voltage

The maximum frequency of an input signal will now depend on the ***RC*** time constant where ***R*** is R_{min} and ***C*** is the total capacitance of the package, pad and input buffer. The fewer CMOS driven inputs on a shared common ESD bus, the lower the resistance and the higher the frequency of operation. The maximum frequency can be approximated as follows:

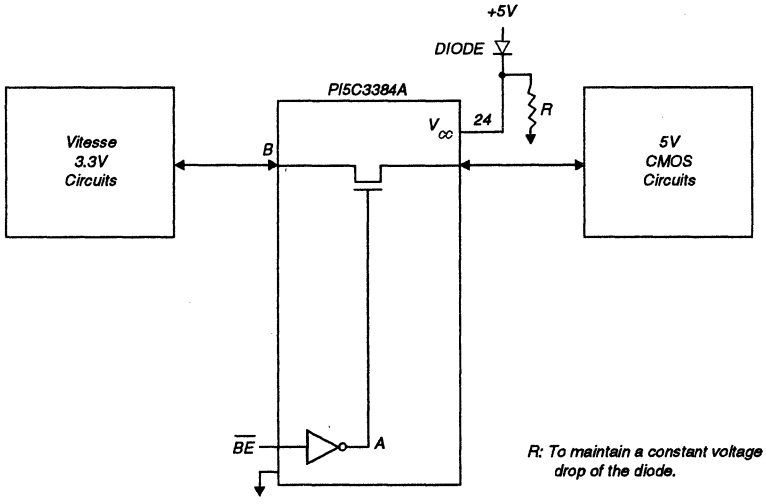
$$Max\ Freq = 1/(2\pi RC)$$

Note: This solution is not applicable to bidirectional TTL I/O's.

Solution #2 Bus Switch

A second recommended solution is to limit the V_{OH} (max) as seen at the TTL input as shown in Figure 4. This approach uses a 3384 chip, available from either Pericom or Quality Semiconductor, which is placed in series with the +5V CMOS output and the +3.3V Vitesse TTL input. This chip has a 10-bit interface, so 10 TTL inputs can be serviced by a single 3384 part. The part is available in a 24 pin DIP, surface mount SOIC or 1/4 size surface mount QSOP with a cost of $1 to $2 depending on quantity and package selection.

Figure 4: Bus Switch



Interfacing Vitesse +3.3V TTL with +5V CMOS

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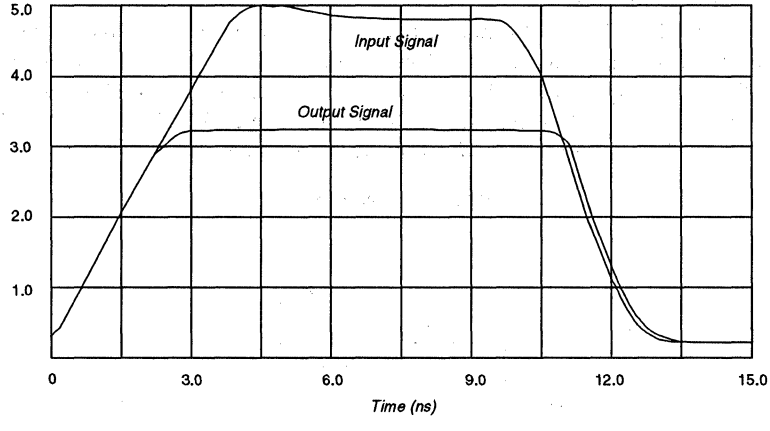
When this part is used to convert from 5V to 3V logic, it consumes almost no power. However, in addition to the 3384 part, this solution requires a diode and a resistor. The diode is required to drop the supply voltage from +5V to 4.2V. The resistor creates a constant voltage drop across the diode. This diode and resistor can be shared between a number of 3384 chips. As shown in the graph in Figure 5, the output signal is limited to 3.2V max which will not cause any problem to the 3.3V TTL circuit. For more information about this part, contact:

Pericom Semiconductor Corporation
2380 Bering Drive
San Jose, CA 95131
(408) 435-0800
FAX: 435-1100

Quality Semiconductor
851 Martin Avenue
Santa Clara, CA 95050
(408) 450-8000
FAX: 496-0773

Figure 5: Input and Output Signals of 3384 at V_{CC} = 4.2V



Conclusion

The current limiting resistor is simple and inexpensive, however this solution may limit the maximum frequency of the interface. The bus switch is a more elegant solution dissipating little power and able to handle frequencies over 100 MHz. However, the bus switch is more costly at $1 to $2 dollars per bus switch chip (which can service up to 10 inputs) and requires two extra components, a resistor and a diode.

Table 1: Bus Switch Power and Cost

	Series Resistor	*PI5C3384A*
Power[1]	~10 mW	~4 mW
Cost[1]	$0.05 - $0.10	$1.00 - $2.00

Note: 1) For 10 TTL Inputs

Application Note 24

Information Sources for Fibre Channel

The interest level in Fibre Channel has been running very high. This application note summarizes sources of information about Fibre Channel which can be readily accessed by the public. Fibre Channel is being developed by the ANSI X3T11 Technical Committee with Roger Cummings as the chairman. Formal distribution of Fibre Channel Specification is handled by Global Engineering. An industry trade association to promote Fibre Channel was formed called the Fibre Channel Association. Additionally, a substantial amount of information is available through internet. The listing below summarizes some of the more interesting locations for information.

ANSI X3T11	*Roger Cummings, Chairman* Storage Technology 2270 South 88th Street Louisville, CO 80028-0268 Ph: 303-673-6357 Fx: 303-673-8196 roger_cummings@stortek.com
ANSI Documents	*Global Engineering* Ph: 800-854-7179
Fibre Channel Association	*Jeff Silva, Chairman* Fibre Channel Association 12407 MoPac Expressway North 100-357 P.O. Box 9700 Austin, TX 78758 Ph: 512/301-2402
World Wide Web	http://www.amdahl.com/ext/CARP/FCA/FCA.html http://www.cern.ch/HSI/fcs/fca.htm http://www-atp.llnl.gov/atp/telecom.html
ANSI X3T11 Minutes	anonymous ftp
ftp_site	nsco.network.com
filename	X3T11/minutes/*date*min.txt or *date*min.ps
FC-AL Working Document	anonymous ftp
ftp_site	nsco.network.com
filename	FC/AL/fcal44p.listps

Information Sources for Fibre Channel

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FC-AL Direct Disk Attach Profile		anonymous ftp
	ftp_site	ftp.symbios.com
	filename	pub/standards/io/fc/profiles/prv_160.ps
FCSI Documents		anonymous ftp
	ftp_site	playground.sun.com
	directory	/pub/FCSI
		login: anonymous
		password: internet_sign-on
10-Bit Interface Specification		anonymous ftp
	ftp_site	fission.dt.wdc.com
	directory	/home/fissionC/ftp/pub/standards/10bit/frame
	directory	/home/fissionC/ftp/pub/standards/10bit/postscript

Application Note 25

Measuring Eye Diagrams on the VSC7105 Transmitter

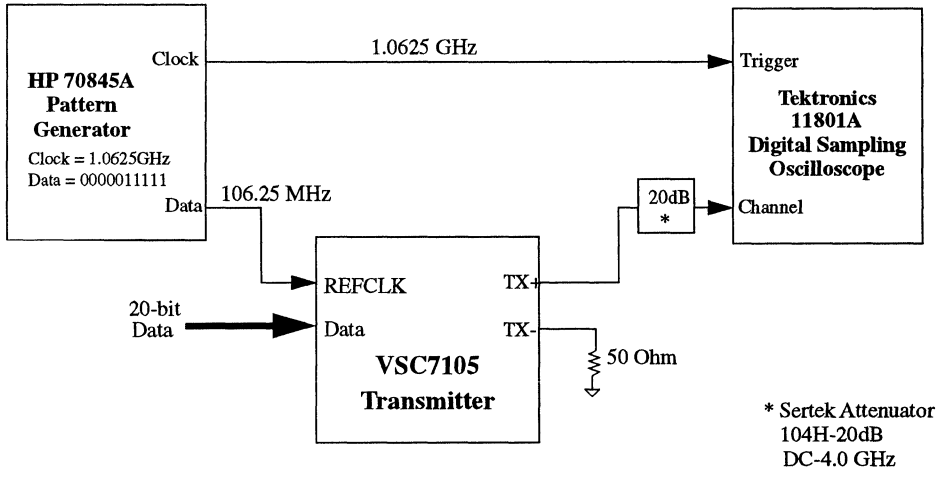
This Application Note describes how Vitesse Semiconductor measures the Data Eye on the VSC7105 full-speed Fibre Channel Transmitter. It includes details of how to generate the data, input data "Jitter", the output Data Eye and the Data Eye at the end of a 60', 50 ohm Coaxial cable.

A block diagram of the test setup is shown in Figure #1. In this measurement, an HP 70845A BERT Pattern Generator is used to generate an internal/external clock at 1.0625 GHz and a Data pattern of '0000011111' generates a 106.25 MHz output which is used as the REFCLK input to the VSC7105. The VSC7105 is on a Device Under Test board (DUT) which allows 20 bits of data to be selected through DIP switches which were set to an arbitrary pattern. The Digital Storage Oscilloscope is triggered with the 1.0625 GHz clock from the BERT and the Data Eye is using in relation to this clock.

The inputs to the VSC7105 are very clean. The Data Bus is static and the REFCLK from the BERT has only 5.2ps RMS / 40 ps peak-to-peak jitter when measured against the 1.0625 GHz clock (See Figure #2). The resultant data eye from the VSC7105 is shown in Figure #3. This was measured with a short 2' 50 ohm coaxial cable (RG-142U) and has jitter of only 21.5 ps RMS / 120 ps pk-pk. The rectangular box in these figures shows the sampling area for the histograms which are shown at the bottom of the scope trace. The data eye was also measured with a 60' coax cable between the VSC7105 DUT board and the attenuator input to the scope. The amplitude and jitter have increased due to the losses in the cable but a very acceptable signal is still available which shows 38.8 ps RMS / 244 ps pk-pk jitter.

The Fibre Channel FC-PH document calls for the use of a fourth-order, low-pass Bessel-Thompson filter when measuring Data Eyes but Vitesse has chosen not to use this filter since it would lower the measured jitter. Measuring Data Eye patterns is one of several methods used to determine how signal integrity varies with cable distance and quality. Additional testing is required to better understand these dependencies in order to determine maximum cable distances for Fibre Channel solutions.

Eye Diagram Test Setup



Measuring Eye Diagrams on the VSC7105 Transmitter

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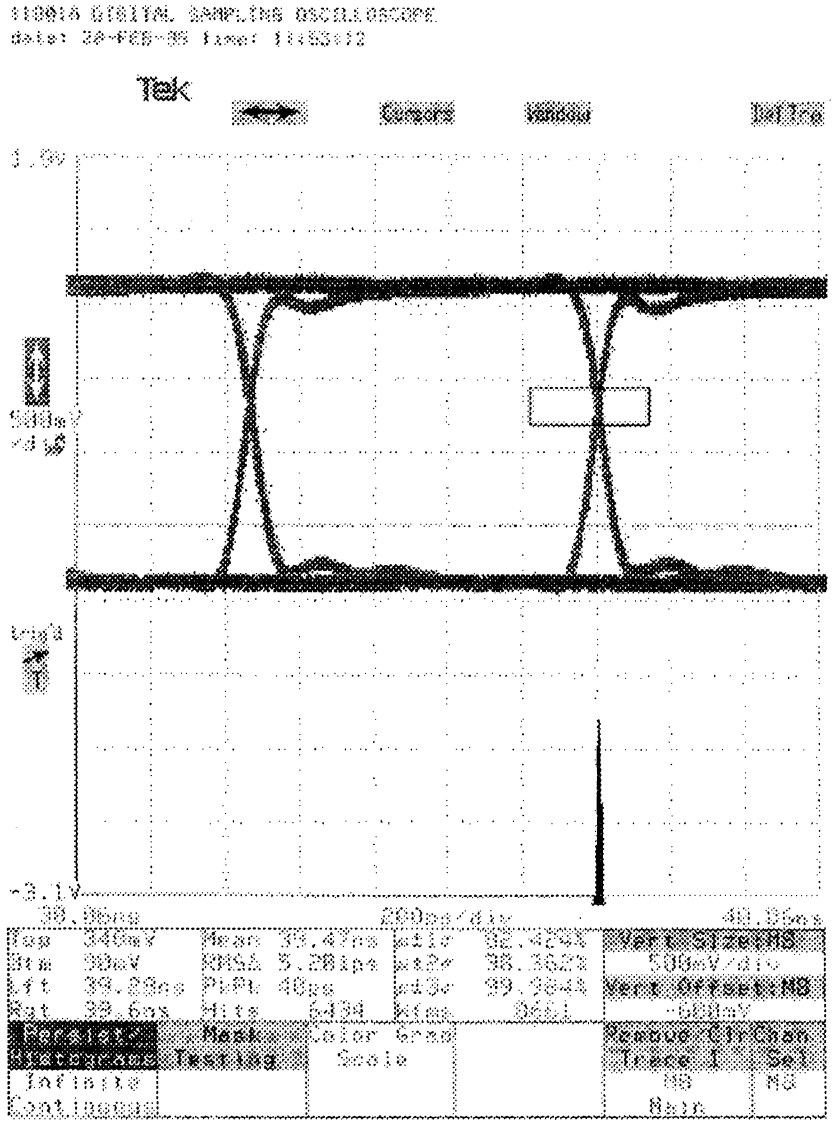
Figure 1: Data Eye of BERT Data



Application Note 25

Measuring Eye Diagrams on the VSC7105 Transmitter

Figure 2: VSC7105 Data Eye, 2' Coax Cable

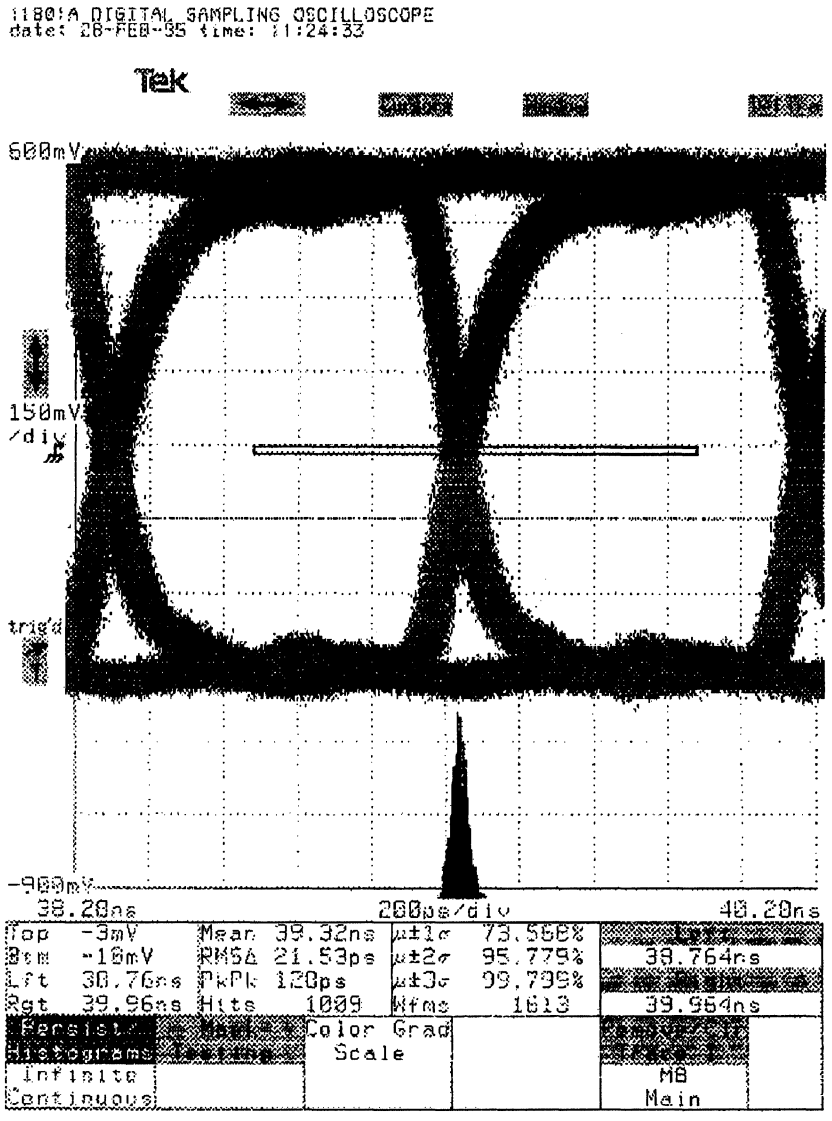
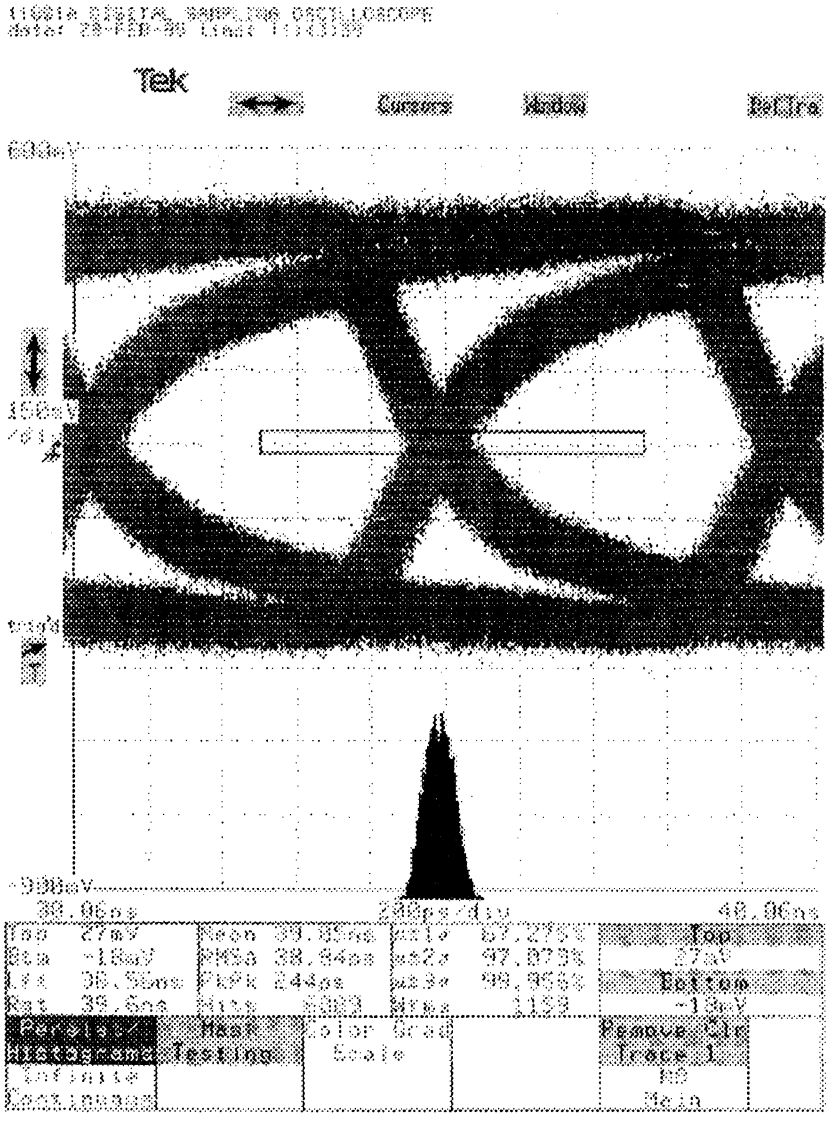


Figure 3: VSC7105 Data Eye, 60' Coax Cable



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