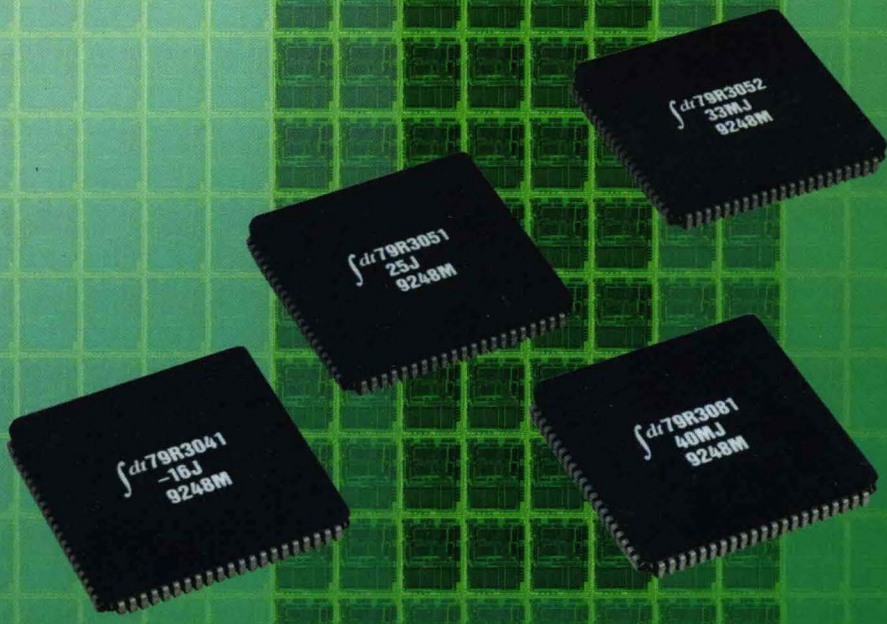
1992
1993

1992/93 DATA BOOK

RISC MICROPROCESSOR COMPONENTS & SUBSYSTEMS

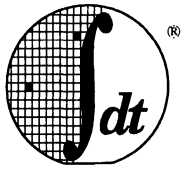
PROCESSORS, SUPPORT COMPONENTS, SOFTWARE, & BOARD-LEVEL PRODUCTS



Integrated Device Technology, Inc.

RISC MICROPROCESSOR COMPONENTS & SUBSYSTEMS
PROCESSORS, SUPPORT COMPONENTS, SOFTWARE, & BOARD-LEVEL PRODUCTS

Integrated Device Technology



Integrated Device Technology, Inc.

1992/93
RISC MICROPROCESSOR COMPONENTS & SUBSYSTEMS DATA BOOK

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CONTENTS OVERVIEW

For ease of use for our customers, Integrated Device Technology provides four separate data books: High-Performance Logic, Specialized Memories and Modules, RISC and RISC SubSystems, and Static RAM.

IDT's 1992/93 RISC Data Book is comprised of new and revised data sheets for the RISC and RISC Subsystem product lines. Also included is a current packaging section for the products included in this book.

The 1992 RISC Data Book's Table of Contents is a listing of the products contained in this data book only (in the past, we have also included products that appeared in other IDT data books). The numbering scheme for the book is consistent with the 1990–91 data books. The number at the bottom center of the page denotes the section number and the sequence of the data sheet within that section, (i.e., 5.5 would be the fifth data sheet in the fifth section). The number in the lower right-hand corner is the page number for that particular data sheet.

Integrated Device Technology, Inc. is a recognized leader in high-speed CMOS and BiCMOS technology and produces a broad line of products. This enables us to provide complete CMOS and BiCMOS solutions to designers of high-performance digital systems. Not only do our product lines include industry standard devices, they also feature products with faster speeds, lower power, and package and/or architectural benefits that allow designers to significantly improve system performance.

To find ordering information: Ordering Information for all products in this book appears in Section 1, along with the Package Marking Description, Product Selector Guide, and Ordering Information. Reference data on our Technology Capabilities, Quality Commitments, and Package Diagram Outlines is included in Sections 2, 3, and 4, respectively.

To find product data: Start with the Table of Contents, organized by product line (page 1.2), or with the Numeric Table of Contents (page 1.3). These indexes will direct you to the page on which the complete technical data sheet can be found. Data sheets may be of the following type:

ADVANCE INFORMATION—contain initial descriptions (subject to change) for products that are in development, including features, block diagrams, and target specifications.

PRELIMINARY—contain descriptions for products soon to be, or recently, released to production, including features, pinouts, and block diagrams. Timing data are based on simulation or initial characterization and are subject to change upon full characterization.

FINAL—contain minimum and maximum limits specified over the complete voltage supply and temperature range for full production devices.

New products, product performance enhancements, additional package types, and new product families are being introduced frequently. Please contact your local IDT sales representative to determine the latest device specifications, package types, and product availability.

ABOUT THE COVER

The cover shows IDT's family of RISController™ products, which includes the R3041™, R3051™, and R3081™. These R3000-derivative microprocessors are pin- and software-compatible, and have been designed to address specific price/performance targets for embedded applications. The background shows an R3081 wafer at approximately 1.2x magnification.

IDT also offers a variety of RISC-based board-level solutions, evaluation tools, and development support. IDT's success in the proliferation of application-optimized microprocessors is the result of blending the MIPS high-performance RISC architecture with our state-of-the-art process technology and wide-ranging system expertise.

LIFE SUPPORT POLICY

Integrated Device Technology's products are not authorized for use as critical components in life support devices or systems unless a specific written agreement pertaining to such intended use is executed between the manufacturer and an officer of IDT.

1. **Life support devices or systems are devices or systems which (a) are intended for surgical implant into the body or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.**
2. **A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.**

1992 RISC DATA BOOK
TABLE OF CONTENTS

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1992 RISC DATA BOOK (Continued)

RISC ASSEMBLIES

IDT SALES OFFICE, REPRESENTATIVE AND DISTRIBUTOR LOCATIONS

NUMERICAL TABLE OF CONTENTS

ORDERING INFORMATION

When ordering by TWX or Telex, the following format must be used:

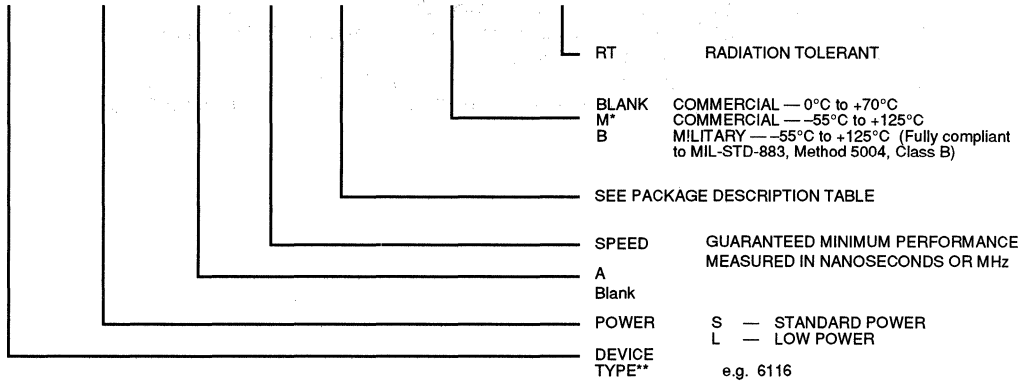
A. Complete Bill To.
B. Complete Ship To.
C. Purchase Order Number.
D. Certificate of Conformance. Y or N.
E. Customer Source Inspection. Y or N.
F. Government Source Inspection. Y or N
G. Government Contract Number and Rating.
H. Requested Routing.
I. IDT Part Number –
   Each item ordered must use the complete part number exactly as listed in the price book.
J. SCD Number — Specification Control Document (Internal Traveller).
K. Customer Part Number/Drawing Number/Revision Level –
   Specify whether part number is for reference only, mark only, or if extended processing to customer specification is required.
L. Customer General Specification Numbers/Other Referenced Drawing Numbers/Revision Levels.
M. Request Date With Exact Quantity.
N. Unit Price.
O. Special Instructions, Including Q.A. Clauses, Special Processing.

Federal Supply Code Number/Cage Number — 61772
Dun & Bradstreet Number — 03-814-2600
Federal Tax I.D. — 94-2669985
TLX# — 887766
FAX# — 408-727-3468

PART NUMBER DESCRIPTION

A = Alpha Character N = Numeric Character

IDT	XXXXX	A	X	999	A	A	A
	DEVICE TYPE	POWER	REVISION	SPEED	PACKAGE	PROCESS/ TEMPERATURE	SPECIAL PROCESS



PACKAGE DESCRIPTION TABLE

C	CERAMIC SIDEBRAZE	PF	PLASTIC FLATPACK
D	CERDIP	SO	PLASTIC SMALL OUTLINE IC
F	FLATPACK	TC	SIDEBRAZE THINDIP (300 MIL)
G	PIN GRID ARRAY	TP	PLASTIC THIN DUAL IN-LINE
J	PLASTIC LEADED CHIP CARRIER	QE	CERQUAD GULL WING
L	LEADLESS CHIP CARRIER	XE	CERPACK (F11 CONFIG. ONLY)
P	PLASTIC DIP	XL	FINE-PITCH LCC
Y	SOJ		

*Consult Factory
**For Logic, the "54" series (e.g. IDT54FCT138) — –55°C to +125°C
the "74" series (e.g. IDT74FCT138) — 0°C to +70°C

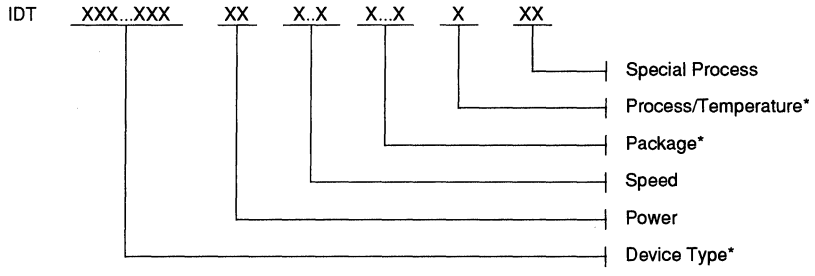
IDT PACKAGE MARKING DESCRIPTION

PART NUMBER DESCRIPTION

IDT's part number identifies the basic product, speed, power, package(s) available, operating temperature and processing grade. Each data sheet has a detailed description, using the part number, for ordering the proper product for the user's application. The part number is comprised of a series of alpha-numeric characters:

1. An "IDT" corporate identifier for Integrated Device Technology, Inc.
2. A basic device part number composed of alpha-numeric characters.
3. A device power identifier, composed of one or two alpha characters, is used to identify the power options. In most cases, the following alpha characters are used:
   "S" or "SA" is used for the standard power product.
   "L" or "LA" is used for lower power than the standard power product.
4. A device speed identifier, when applicable, is either alpha characters, such as "A" or "B", or numbers, such as 20 or 45. The speed units, depending on the product, are in nanoseconds or megahertz.
5. A package identifier, composed of one or two characters. The data sheet should be consulted to determine the packages available and the package identifiers for that particular product.
6. A temperature/process identifier. The product is available in either the commercial or military temperature range, processed to a commercial specification, or the product is available in the military temperature range with full compliance to MIL-STD-883. Many of IDT's products have burn-in included as part of the standard commercial process flow.
7. A special process identifier, composed of alpha characters, is used for products which require radiation enhancement (RE) or radiation tolerance (RT).

Example for Monolithic Devices:



* Field Identifier Applicable To All Products

2507 drw 01

ASSEMBLY LOCATION DESIGNATOR

IDT uses various locations for assembly. These are identified by an alpha character in the last letter of the date code marked on the package. Presently, the assembly location alpha character is as follows:

A = Anam, Korea
I = USA
P = Penang, Malaysia

MIL-STD-883C COMPLIANT DESIGNATOR

IDT ships military products which are compliant to the latest revision of MIL-STD-883C. Such products are identified by a "C" designation on the package. The location of this designator is specified by internal documentation at IDT.

Integrated Device Technology, Inc.

HIGH-SPEED CMOS MICROPROCESSOR FAMILY PRODUCT SELECTOR GUIDE

- Broadest range of high-performance to low-cost, code-compatible RISC processors: R3000A, R4000 CPUs, R3001, R3041, R3051/52, R3081 RISControllers™, R3010A FPA, R3500 RISCore™
- R4000—third-generation high-performance 64-bit CPU and FPA with on-chip cache
- R3001, R3041, R3051/52, and R3081 RISController Family—designed for lower cost embedded systems, all code-compatible with original R3000
- R3500 RISCore—combines CPU and FPA, pin- and SW-compatible with the R3000A
- Support chips designed for RISC systems: R3020 Write Buffer, 73720 Bus Exchanger, R3721 DRAM Controller
- Applications range from real-time control to multiprocessing systems
- Optimizing compilers for C, Pascal, FORTRAN, Ada, PL/1 and Cobol
- R3000, R3001, R3041, R3051/52, R3081, and R3500 are 100% code-compatible
- R3010A Floating Point Accelerator—conforms with IEEE 754 1985 Standard
- R3020 Write Buffer enhances CPU performance by allowing memory "write-through" during run cycles
- Low-cost Evaluation Boards available

Part Number	Description	Pkgs.	Avail.	Data Book Page
RISC CMOS MICROPROCESSORS				
IDT79R4000, 79R4000A	Very high-performance, highly integrated 64-bit CPU, fully binary compatible with the R3000A. Combines CPU, floating-point and 16KB of cache (32KB for R4000A) capable of over 50 VAX mips sustained performance	447PGA 179PGA	NOW	5.7
IDT79R3000A	RISC CPU Processor, 20–40MHz, on-chip Cache Control, Memory Management Unit, 64-Entry Translation Lookaside Buffer, Thirty-two 32-bit General Purpose Registers	144PGA 175PGA 172FP 160MQUAD	NOW	5.1
IDT79R3001	RISController, derivative of the R3000 designed for lower cost embedded systems. Achieves high performance with reduced memory parts count, lower overall system cost, and includes real-time features	144PGA 172FP	NOW	5.2
IDT79R3041	RISController, R3000A core, 4-deep read/write buffers, 2.5KB on-chip cache	84PLCC	1Q'93	5.4
IDT79R3051/52	RISControllers, 6kB or 10kB on-chip cache, R3000A CPU core, and 4-deep read/write buffers, low-cost 84-pin plastic packaging	84PLCC	NOW	5.5
IDT79R3081™	RISController, 20kB on-chip cache, R3000 CPU core, R3010A Floating Point Accelerator, 4-deep read/write buffers, pin-compatable with 3051/3052	84MQUAD 84PGA	NOW	5.6
IDT79R3500	RISCore integrates R3000A CPU and R3010A FPA using the R3000A pinout. Up to 32 VUPS sustained performance at 40MHz	161PGA	NOW	5.3
IDT79R3010A	RISC Floating-Point Accelerator, 20–40MHz	84PGA 84FP	NOW	6.1
RISC SUPPORT DEVICES				
IDT73720	16-Bit Tri-Port Bus Exchanger	68PLCC 80PQFP	NOW	6.5
IDT79R3721	DRAM Controller, Interfaces to R3051/52	84PLCC	NOW	6.4
IDT79R3020	RISC CPU Write Buffer	68PLCC	NOW	6.3
IDT79R3730	Integrated System Controller	208PQFP	1Q'93	6.6

Part Number	Description	Pkgs.	Avail.	Data Book Page
RISC DEVELOPMENT SYSTEMS				
IDT7RS503	R3000 NuBus™ add-in card for Macintosh® II, includes RISC/os™ and C Compiler, code development and debugging environment		NOW	7.11
RC3230	Magnum series desktop development host. Entry-level system for 15–20 users, rated at 17.8 SPECmarks with 25MHz R3000 CPU. 33MHz model now available.		NOW	
RC3240	Desk-side development host. For medium size projects, AT expansion slots, R3000-25 for 16SPECmarks performance		NOW	
RC3260	Pedestal development host. Higher-end multi-user.		NOW	
R3000 FAMILY EVALUATION TOOLS (See RISC SubSystems)				
IDT7RS382/383/385	R3000 Family Evaluation Boards		NOW	7.7
R3000 FAMILY MIPS SOFTWARE				
79SFOR-2n-RTU	FORTRAN RISCompiler™		NOW	
79SPAC-2n-RTU	Pascal RISCompiler		NOW	
79SANC-2n-RTU	ANSI C RISCompiler		NOW	
79S5053-n	AT&T C++ translator		NOW	
79SSPP-5-SRC1	SPP (System Programmer's Package) for R3000		NOW	
79SSPE-5-SRC1	SPP/e for embedded systems. Excludes simulation programs Cache 2000 and SABLE for R3000		NOW	
79SRWN-3n-RTU	RISCwindows™ operation environment		NOW	
79SRCM-2n-RTU	DECnet™ communication software		NOW	
79SSPP41BUI	SPP (System Programmer's Package) for R4000 Binary		NOW	
79SSPE41BUI	SPP/e for R4000 Binary		NOW	
79SSPS41BUI	Sable simulator for R4000 Binary		NOW	
79SSPC41BUI	Cache simulator for R4000 Binary		NOW	
79SSP55BUI	Sable Simulator for R3000 Binary		NOW	
79SSPC5BUI	Cache Simulator for R3000 Binary		NOW	

NOTE: All development systems (MacStation and MIPS) come standard with RISC/os (UNIX®) and C-Compiler software. Additional memory, disk peripherals, tape peripherals and interface options are available from IDT for MIPS development systems.

Integrated RISC Design Solutions

IDT is committed to providing complete integrated RISC solutions by combining expertise in silicon process technology with leadership products in development systems and software. Long an industry leader in producing the fastest static RAMs for cache memory and high-speed logic for memory interface, IDT offers:

- Dedicated RISC support chips
- MIPS compilers and cross-software for PC and Sun
- CPU and cache modules
- RISC evaluation and prototyping vehicles
- Monitors and debuggers
- Floating Point Library
- MIPS development hosts and
- Macintosh development system

The MacStation™ R3000 development board that is hosted in the Macintosh II (P/N IDT7RS503) comes complete with IDT/ux™ (UNIX operation system), the language compiler and software debugging tools. IDT complementary components and modules include:

Cache Memories

Part No.	Description	Frequency	Access Time
IDT71586	4k x 16 (w/Latch)	25MHz	25ns
IDT7164	8k x 8	33MHz	12ns
IDT7198	16k x 4	33MHz	12ns
IDT61298	64k x 4 (w/$\overline{OE}$)	33MHz	12ns
IDT6198	16k x 4	33MHz	12ns
IDT71B229	16k x 9 x 2	40MHz	12ns

Bus Interface Logic

IDT74FCT373A/C Octal Latch
IDT74FCT374A/C Octal Register
IDT74FCT240A/C Octal Buffer
IDT74FCT244A/C Octal Buffer
IDT29FCT520A/B Multilevel Pipeline Register
IDT49FCT804A Tri-Port Bus Multiplexer

Peripheral Components

73200 Read-write Buffer
73201 Read-write Buffer
73210 Read-write Buffer
73211 Read-write Buffer

Cache Modules

Standard Versions:

IDT7MB6139	Dual 64kB
IDT7MB6043	Dual 32kB
IDT7MB6044	Dual 16kB
IDT7MP6074	R4000 Secondary Cache Modules

Multiprocessing:

IDT7MB6049	Dual 64kB
IDT7MB6051	Dual 32kB
IDT7MB6061	Dual 64kB w/Resettable I-Cache
IDT7MB6064	Dual Resettable 16kB

Reduce Your Development Time with RISC SubSystems

FASTER SYSTEMS: FASTER DESIGN CYCLES

Using RISC technology, you can build systems that will run rings around an old 386 or 680x0 design. IDT's RISC SubSystems Division can help you get your design completed in record time. IDT has proven RISC design and manufacturing experience that you can rely on. Exploit our expertise by having IDT design and manufacture your board. Or integrate one of our pre-built, fully-tested modules into your design. IDT also offers a full range of development support including prototyping hardware, software tools, and the powerful MacStation 3 development system.

CUSTOM DESIGN AND MANUFACTURING

IDT has successfully designed and produced over thirty boards and modules based on the MIPS RISC architecture. We have become experts in quickly bringing quality products to market. The IDT advantage has five components: (1) extensive hardware design experience, (2) internal surface mount manufacturing capability, (3) complete suite of diagnostic tests, (4)experience in hardware/software integration, (5) a detailed understanding of component characteristics. Take advantage of this experience by allowing us to design and manufacture your board. Or work with us in a joint development program where we handle the CPU interface so you can concentrate on product differentiation.

MODULES

Our modules contain the RISC CPU, Floating Point Accelerator, and all the cache memory. Most include clock control, interrupt and initialization logic, and read and write buffers, as well. All the components are surface-mounted on small, plug-in PC boards, burned-in and tested at the rated speed. All the tricky timing, and high-speed design is done and tested for you. The modules can be plugged into motherboards containing main memory, I/O, and the rest of the system, all of which is relatively low speed and is easy to lay out using conventional design techniques.

PROTOTYPING PLATFORMS

To shorten your design time even more, we offer Prototyping Platforms for the modules. The Prototyping Platform contains main memory, serial I/O, a powerful debug monitor in EPROM, and a personality card that interfaces it directly to one of our modules. You can download your software onto the Prototyping Platform, and/or design additional hardware and plug it in.

MACSTATION 3—DEVELOPMENT SYSTEM

IDT offers a complete R3000 development system in a Macintosh II computer. Click an icon on your Mac and a new window opens under MultiFinder with the UNIX operating system in it. The UNIX code is actually running on a fast R3000 system board inside the Mac, and you can run all the MIPS and IDT development tools, including the C compiler and the System Programmers' Package. The MacStation 3 is available in 15mips and 25mips versions.

SOFTWARE

IDT's RISC SubSystems Division offers R3000 software that makes software development faster and easier. You can use our System Integration Manager to control prototypes, to debug software, and to manage I/O drivers. You can put our Monitor into your hardware to control the basic system startup. You can use the Kernel Integration Toolkit as a building block to quickly develop software. And our cross-software for PCs, MIPS and Sun work-stations makes efficient C-program compilation possible with readily available equipment.

Model	Description	Avail.	Data Book Page
R3000-BASED CPU MODULES AND PROTOTYPING HARDWARE			
IDT7RS109	64KB each of I- and D-cache. Supports Multiprocessor. On-board parity, clock, reset, interrupt control. Speeds up to 33MHz.	NOW	8.1
IDT7RS110	32KB each of I- and D-cache. Single-word Read and Write buffers. Small size ideal for embedded applications. Speeds up to 33MHz.	NOW	8.2
IDT7RS409	Prototyping Systems including a 33MHz 7RS109 module. Each prototyping system includes 1MB of static RAM, Counter/Timer, IDT/sim™ debug monitor in EPROM, serial and parallel I/O ports. Quick way to begin development of R3000 hardware and software.	NOW	
IDT7RS410	Prototyping Systems including a 33MHz 7RS110 module. Each prototyping system includes 1MB of static RAM, Counter/Timer, IDT/sim debug monitor in EPROM, serial and parallel I/O ports.	NOW	
EVALUATION BOARDS			
IDT79S385A	R3051 Family Evaluation Board. Complete, self-contained system requiring only a power supply and simple terminal to be operational. Contains R3052E CPU, 1MB of DRAM, IDT/sim monitor in EPROM, serial I/O ports, C compiler, R3081 sample. Supplied with all schematics and user's manual.	NOW	7.7
IDT79S389	R3051 Family Laser Printer Controller Reference Platform for PostScript Level 2 Software from Adobe.	NOW	7.5
SOFTWARE DEVELOPMENT SYSTEMS			
IDT7RS503	MacStation 3 Development System. Complete R3000 CPU on NuBus card that plugs into a Mac II. Runs IDT/ux™ (UNIX SVR3) in a window under MultiFinder. Available in 15mips and 25mips versions. Supplied with MIPS C/ compiler. Other MIPS software products are available for the MacStation 3.	NOW	7.11
R3000 HARDWARE AND SOFTWARE DEVELOPMENT TOOLS			
IDT7RS901	IDT/sim System Integration Manager. Powerful, flexible debug monitor for R3000-, R3001- and R305x-based systems. Includes trace, single-step, cache control, many more functions. Easily extensible. Includes support for source-level debug. Available in source code.	NOW	7.8
IDT7RS903	IDT/c. Multihost optimizing C compiler, available for operation on 386/486 machines (MS-DOS or UNIX), for MIPS or MacStation under RISC/os, and for Sun SparcStation. Generates efficient R3000 code. Includes floating point libraries for efficient operation without an FPU.	NOW	7.9
IDT7RS909	IDT/kit. Kernal Integration Toolkit. Consists of a set of modules ready to be linked with user-developed code to provide an operating system kernal for R3000-based embedded systems. Functions are provided for initializing systems, memory management, handling interrupts, servicing floating point exceptions and time support. Libraries are included for floating point emulation, transcendental math routines, and ANSI standard C functions. It also contains IDT's Micromonitor, a very simple monitor for initial debug of new hardware. The Micromonitor requires only that the CPU, RAM, and a serial port be operational. All code is supplied in source code (C and assembly), to allow easy access for any modifications needed to tailor the system to the specific application. Code is also supplied in standard archive library format (compiled with IDT/c and MIPS tool chains) for Big and Little Endian targets and for hardware floating point and software FP emulation.	NOW	7.10

IDT...LEADING THE CMOS FUTURE

A major revolution is taking place in the semiconductor industry today. A new technology is rapidly displacing older NMOS and bipolar technologies as the workhorse of the '80s and beyond. That technology is high-speed CMOS. Integrated Device Technology, a company totally predicated on and dedicated to implementing high-performance CMOS products, is on the leading edge of this dramatic change.

Beginning with the introduction of the industry's fastest CMOS 2K x 8 static RAM, IDT has grown into a company with multiple divisions producing a wide range of high-speed CMOS and BiCMOS circuits that are, in almost every case, the fastest available. These advanced products are produced with IDT's proprietary technology, a twin-well, dry-etched, stepper-aligned process utilizing progressively smaller dimensions.

From inception, IDT's product strategy has been to apply the advantages of its extremely fast CMOS technology to produce the integrated circuit elements required to implement high-performance digital systems. IDT's goal is to provide the circuits necessary to create systems which are far superior to previous generations in performance, reliability, cost, weight, and size. Many of the company's innovative product designs offer higher levels of integration, advanced architectures, higher density packaging and system enhancement features that are establishing tomorrow's industry standards. The company is committed to providing its customers with an ever-expanding series of these high-speed, lower-power IC solutions to system design needs.

IDT's commitment, however, extends beyond state-of-the-art technology and advanced products to providing the highest level of customer service and satisfaction in the industry. Manufacturing products to exacting quality standards that provide excellent, long-term reliability is given the same level of importance and priority as device performance. IDT is also dedicated to delivering these high-quality advanced products on time. The company would like to be known not only for its technological capabilities, but also for providing its customers with quick, responsive, and courteous service.

IDT's product families are available in both commercial and military grades. As a bonus, commercial customers obtain the benefits of military processing disciplines, established to meet or exceed the stringent criteria of the applicable military specifications.

IDT is a leading U.S. supplier of high-speed CMOS and BiCMOS circuits. The company's high-performance fast SRAM , FCT logic, high-density modules, FIFOs, multi-port memories, BiCMOS ECL I/O memories, RISC SubSystems, and the 32- and 64-bit RISC microprocessor families complement each other to provide high-speed CMOS and BiCMOS solutions for a wide range of applications and systems.

Dedicated to maintaining its leadership position as a state-of-the-art IC manufacturer, IDT will continue to focus on maintaining its technology edge as well as developing a broader range of innovative products. New products and speed enhancements are continuously being added to each of the existing product families, and additional product families are being introduced. Contact your IDT field representative or factory marketing engineer for information on the most current product offerings. If you're building state-of-the-art equipment, IDT wants to help you solve your design problems.

IDT MILITARY AND DESC-SMD PROGRAM

IDT is a leading supplier of military, high-speed CMOS circuits. The company's high-performance Static RAMs, FCT Logic Family, Complex Logic (CLP), FIFOs, Specialty Memories (SMP), ECL I/O BiCMOS Memories, 32-bit RISC Microprocessor, RISC Subsystems and high-density Subsystems Modules product lines complement each other to provide high-speed CMOS solutions to a wide range of military applications and systems. Most of these product lines offer Class B products which are fully compliant to the latest revision of MIL-STD-883, Paragraph 1.2.1. In addition, IDT offers Radiation Tolerant (RT), as well as Radiation Enhanced (RE), products.

IDT has an active program with the Defense Electronic Supply Center (DESC) to list all of IDT's military compliant devices on Standard Military Drawings (SMD). The SMD program allows standardization of militarized products and reduction of the proliferation of non-standard source control drawings. This program will go far toward reducing the need for each defense contractor to make separate specification control drawings for purchased parts. IDT plans to have SMDs for many of its product offerings. Presently, IDT has 88 devices which are listed or pending listing. The devices are from IDT's SRAM, FCT Logic family, Complex Logic (CLP), FIFOs and Specialty Memories (SMP) product families. IDT expects to add another 20 devices to the SMD program in the near future. Users should contact either IDT or DESC for current status of products in the SMD program.

SMD	
SRAM	**IDT**
84036	6116
5962-88740	6116LA
84132	6167
5962-86015	7187
5962-86859	6198/7198/7188
5962-86705	6168
5962-85525	7164
5962-88552	71256L
5962-88662	71256S
5962-88611	71682L
5962-88681	71258S
5962-88545	71258L
5962-89891	7198
5962-89892	6198
5962-89690	6116SA
5962-38294	7164
5962-89692	7188
5962-89712	71982
SMP	**IDT**
5962-86875	7130/7140
5962-87002	7132/7142
5962-88610	7133S/7143S
5962-88665	7133L/7143L
FIFO	**IDT**
5962-87531	7201LA
5962-86846	72404L
5962-88669	7203S
5962-89568	7204L
5962-89536	7202L
5962-89863	7201S
5962-89523	72403L
5962-89666	7200L
5962-89942	72103L
5962-89943	72104L
5962-89567	7203L
5962-90715	7204S

SMD	
LOGIC	**IDT**
5962-87630	54FCT244/A
5962-87629	54FCT245/A
5962-86862	54FCT299/A
5962-87644	54FCT373/A
5962-87628	54FCT374/A
5962-87627	54FCT377/A
5962-87654	54FCT138/A
5962-87655	54FCT240/A
5962-87656	54FCT273/A
5962-89533	54FCT861A/B
5962-89506	54FCT827A/B
5962-88575	54FCT841A/B
5962-88608	54FCT821A/B
5962-88543	54FCT521/A
5962-88640	54FCT161/A
5962-88639	54FCT573/A
5962-88656	54FCT823A/B
5962-88657	54FCT163/A
5962-88674	54FCT825A/B
5962-88661	54FCT863A/B
5962-88736	29FCT520A/B
5962-88775	54FCT646/A
5962-89508	54FCT139/A
5962-89665	54FCT824A/B
5962-88651	54FCT533/A
5962-88652	54FCT182/A
5962-88653	54FCT645A/B
5962-88654	54FCT640A/B
5962-88655	54FCT534/A
5962-89767	54FCT540/A
5962-89766	54FCT541/A
5962-89733	54FCT191/A
5962-89732	54FCT241/A
5962-89652	54FCT399/A
5962-89513	54FCT574/A
5962-89731	54FCT833A/B
5962-88675	54FCT845A/B
5962-89730	54FCT543/A

SMD	
CLP	**IDT**
5962-87708	39C10B & C
5962-88533	49C460A/B/C
5962-88613	39C60A
5962-88643	49C410
5962-86873	7216L
5962-87686	7217L
5962-88733	7210L
5962-89758	54FCT843A/B/C
5962-90669	54FCT193/A
5962-90901	29FCT52A/B/C

2509 tbl 01

RADIATION HARDENED TECHNOLOGY

IDT manufactures and supplies radiation hardened products for military/aerospace applications. Utilizing special processing and starting materials, IDT's radiation hardened devices survive in hostile radiation environments. In Total Dose, Dose Rate, and environments where single event upset is of concern, IDT products are designed to continue functioning without loss of performance. IDT can supply all its products on these processes. Total Dose radiation testing is performed in-house on an ARACOR X-Ray system. External facilities are utilized for device research on gamma cell, LINAC and other radiation equipment. IDT has an on-going research and development program for improving radiation handling capabilities (See "IDT Radiation Tolerant/Enhanced Products for Radiation Environments" in Section 3) of IDT products/processes.

IDT LEADING EDGE CMOS TECHNOLOGY

HIGH-PERFORMANCE CMOS

From IDT's beginnings in 1980, it has had a belief in and a commitment to CMOS. The company developed a high-performance version of CMOS that allows the design and manufacture of leading-edge components. It incorporates the best characteristics of traditional CMOS, including low power, high noise immunity and wide operating temperature range; it also achieves speed and output drive equal or superior to bipolar Schottky TTL. The last decade has seen development and production of four "generations" of IDT's CMOS technology with process improvements which have reduced IDT's electrical effective (Leff) gate lengths by more than 60 percent from 1.3 microns (millionths of a meter) in 1981 to 0.45 microns in 1990.

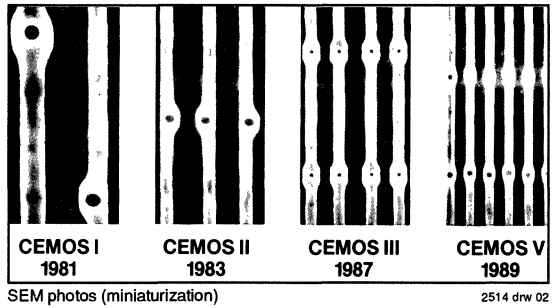
	CMOS I	CMOS II		CMOS III	CMOS V	CMOS VI
		A	C			
Calendar Year	**1981**	**1983**	**1985**	**1987**	**1989**	**1990**
Drawn Feature Size	2.5μ	1.7μ	1.3μ	1.2μ	1.0μ	0.8μ
Leff	1.3μ	1.1μ	0.9μ	0.8μ	0.6μ	0.45μ
Basic Proces Enhancements	Dual-well, Wet Etch, Projection Aligned	Dry Etch, Stepper	Shrink, Spacer	Silicide, BPSG, BiCMOS I	BiCMOS II	BiCMOS III

2514 drw 01

CMOS IV = CMOS III – scaled process optimized for high-speed logic.

Figure 1.

Continual advancement of CMOS technology allows IDT to implement progressively higher levels of integration and achieve increasingly faster speeds maintaining the company's established position as the leader in high-speed CMOS integrated circuits. In addition, the fundamental process technology has been extended to add bipolar elements to the CMOS platform. IDT's BiCMOS process combines the ultra-high speeds of bipolar devices with the lower power and cost of CMOS, allowing us to build even faster components than straight CMOS at a slightly higher cost.



SEM photos (miniaturization)

2514 drw 02

Figure 2. Fifteen-Hundred-Power Magnification Scanning Electron Microscope (SEM) Photos of the Five Generations of IDT's CMOS Technology

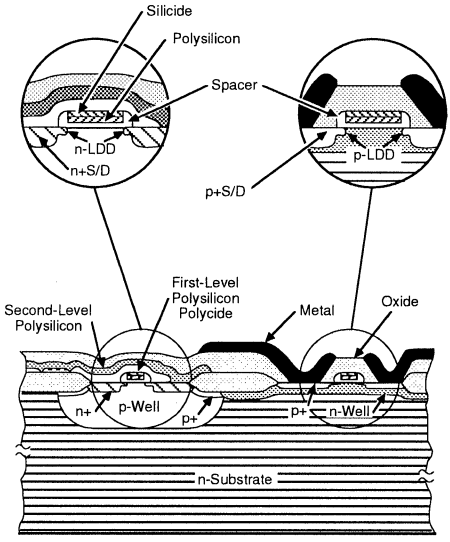


Figure 3. IDT CMOS Device Cross Section

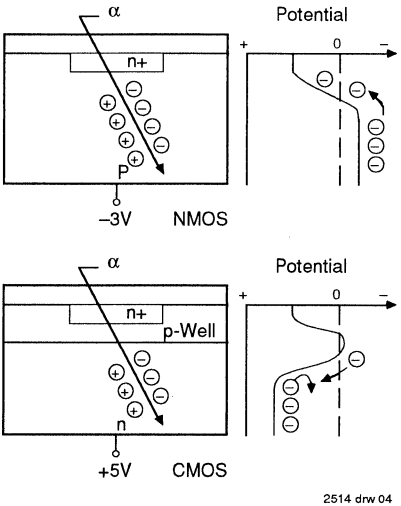


Figure 4. IDT CMOS Built-In High Alpha Particle Immunity

ALPHA PARTICLES

Random alpha particles can cause memory cells to temporarily lose their contents or suffer a "soft error." Traveling with high energy levels, alpha particles penetrate deep into an integrated chip. As they burrow into the silicon, they leave a trail of free electron-hole pairs in their wake.

The cause of alpha particles is well documented and understood in the industry. IDT has considered various techniques to protect the cells from this hazardous occurrence. These techniques include dual-well structures (Figures 3 and 4) and a polymeric compound for die coating. Presently, a polymeric compound is used in many of IDT's SRAMs; however, the specific techniques used may vary and change from one device generation to the next as the industry and IDT improve the alpha particle protection technology.

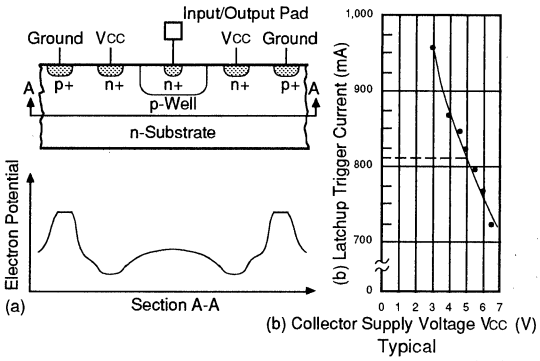


Figure 5. IDT CMOS Latchup Suppression

LATCHUP IMMUNITY

A combination of careful design layout, selective use of guard rings and proprietary techniques have resulted in virtual elimination of latchup problems often associated with older CMOS processes (Figure 5). The use of NPN and N-channel I/O devices eliminates hole injection latchup. Double guard ring structures are utilized on all input and output circuits to absorb injected electrons. These effectively cut off the current paths into the internal circuits to essentially isolate I/O circuits. Compared to older CMOS processes which exhibit latchup characteristics with trigger currents from 10-20mA, IDT products inhibit latchup at trigger currents substantially greater than this.

SURFACE MOUNT TECHNOLOGY AND IDT'S MODULE PRODUCTS

Requirements for circuit area reduction, utilizing the most efficient and compact component placement possible and the needs of production manufacturing for electronics assemblies are the driving forces behind the advancement of circuit-board assembly technologies. These needs are closely associated with the advances being made in surface mount devices (SMD) and surface mount technology (SMT) itself. Yet, there are two major issues with SMT in production manufacturing of electronic assemblies: high capital expenditures and complexity of testing.

The capital expenditure required to convert to efficient production using SMT is still too high for the majority of electronics companies, regardless of the 20–60% increase in the board densities which SMT can bring. Because of this high barrier to entry, we will continue to see a large market segment [large even compared to the exploding SMT market] using traditional through-hole packages (i.e. DIPs, PGAs, etc) and assembly techniques. How can these types of companies take advantage of SMD and SMT? Let someone else, such as IDT, do it for them by investing time and money in SMT and then in return offer through-hole products utilizing SMT processes. Products which fit this description are multi-chip modules, consisting of SMT assembled SMDs on a through-hole type substrate. Modules enable companies to enjoy SMT density advantages and traditional package options without the expensive startup costs required to do SMT in-house.

Although subcontracting this type of work to an assembly house is an alternative, there still is the other issue of testing, an area where many contract assembly operations fall short of IDT's capability and experience. Prerequisites for adequate module testing sophisticated high-performance parametric testers, customized test fixtures, and most importantly the experience to tests today's complex electronic devices. Companies can therefore take advantage of IDT's experience in testing and manufacturing high-performance CMOS multi-chip modules.

At IDT, SMD components are electrically tested, environmentally screened, and performance selected for each IDT module. All modules are 100% tested as if they are a separate functional component and are guaranteed to meet all specified parameters at the module output without the customer having to understand the modules' internal workings.

Other added benefits companies get by using IDT's CMOS module products are:

1) a wide variety of high-performance, through-hole products utilizing SMD packaged components,
2) fast speeds compared with NMOS based products,
3) low power consumption compared with bipolar technologies, and
4) low cost manufacturability compared with GaAs-based products.

IDT has recognized the problems of SMT and began offering CMOS modules as part of its standard product portfolio. IDT modules combine the advantages of:

1) the low power characteristics of IDT's CMOS and BiCMOS products,
2) the density advantages of first class SMD components including those from IDT's components divisions, and
3) experience in system level design, manufacturing, and testing with its own in-house SMT operation.

IDT currently has two divisions (Subsystems and RISC Subsystems) dedicated to the development of module products ranging from simple memory modules to complex VME sized application specific modules to full system-level CPU boards. These modules have surface mount devices assembled on both sides of either a multi-layer glass filled epoxy (FR-4) or a multi-layer co-fired ceramic substrate. Assembled modules come available in industry standard through-hole packages and other space-saving module packages. Industry proven vapor-phase or IR reflow techniques are used to solder the SMDs to the substrate during the assembly process. Because of our affiliation with IDT's experienced semiconductor manufacturing divisions, we thoroughly understand and therefore test all modules to the applicable datasheet specifications and customer requirements.

Thus, IDT is able to offer today's electronic design engineers a unique solution for their "need-more-for-less" problem.modules. These high speed, high performance products offer the density advantages of SMD and SMT, the added benefit of low power CMOS technology, and through-hole packaged electronics without the high cost of doing it in-house.

STATE-OF-THE-ART FACILITIES AND CAPABILITIES

Integrated Device Technology is headquartered in Santa Clara, California—the heart of "Silicon Valley." The company's operations are housed in six facilities totaling over 500,000 square feet. These facilities house all aspects of business from research and development to design, wafer fabrication, assembly, environmental screening, test, and administration. In-house capabilities include scanning electron microscope (SEM) evaluation, particle impact noise detection (PIND), plastic and hermetic packaging, military and commercial testing, burn-in, life test, and a full complement of environmental screening equipment.

The over-200,000-square-foot corporate headquarters campus is composed of three buildings. The largest facility on this site is a 100,000 square foot, two-building complex. The first building, a 60,000-square-foot facility, is dedicated to the Standard Logic and RISC Microprocessor product lines, as well as hermetic and plastic package assembly, logic products' test, burn-in, mark, QA, and a reliability/failure analysis lab.

IDT's Packaging and Assembly Process Development teams are located here. To keep pace with the development of new products and to enhance the IDT philosophy of "innovation," these teams have ultra-modern, integrated and correspondingly sophisticated equipment and environments at their disposal. All manufacturing is completed in dedicated clean room areas (Class 10K minimum), with all preseal operations accomplished under Class 100 laminar flow hoods.

Development of assembly materials, processes and equipment is accomplished under a fully operational production environment to ensure reliability and repeatable product. The Hermetic Manufacturing and Process Development team is currently producing custom products to the strict requirements of MIL-STD-883. The fully automated plastic facility is currently producing high volumes of USA-manufactured product, while developing state-of-the-art surface-mount technology patterned after MIL-STD-883.

The second building of the complex houses sales, marketing, finance, MIS, and Northwest Area Sales.

The RISC Subsystems Division is located across from the two-building complex in a 50,000-square-foot facility. Also located at this facility are Quality Assurance and wafer fabrication services. Administrative services, Human Resources, International Planning, Shipping and Receiving departments are also housed in this facility.

IDT's largest and newest facility, opened in 1990 in San Jose, California, is a multi-purpose 150,000-square-foot, ultra-modern technology development center. This facility houses a 25,000 square foot, combined Class 1 (a maximum of one particle-per-cubic-foot of 0.2 micron or larger), sub-half-micron R&D fabrication facility and a wafer fabrication area. This fab supports both production volumes of IDT products, including some next-generation SRAMs, and the R&D efforts of the technology development staff. Technology development efforts targeted for the center include advanced silicon processing and wafer fabrication techniques. A test area to support both production and research is located on-site. The building is also the home of the FIFO, ECL, and Subsystems product lines.

IDT's second largest facility is located in Salinas, California, about an hour south of Santa Clara. This 95,000-square-foot facility, located on 14 acres, houses the Static RAM Division and Specialty Memory product line. Constructed in 1985, this facility contains an ultra-modern 25,000-square-foot high-volume wafer fabrication area measured at Class 2-to-3 (a maximum of 2 to 3 particles-per-cubic-foot of 0.2 micron or larger) clean room conditions. Careful design and construction of this fabrication area created a clean room environment far beyond the 1985 average for U.S. fab areas. This made possible the production of large volumes of high-density submicron geometry, fast static RAMs. This facility also houses shipping areas for IDT's leadership family of CMOS and BiCMOS static RAMs. This site can expand to accommodate a 250,000-square-foot complex.

To extend our capabilities while maintaining strict control of our processes, IDT has an operational Assembly and Test facility located in Penang, Malaysia. This facility assembles product to U.S. standards, with all assemblies done under laminar flow conditions (Class 100) until the silicon is encased in its final packaging. All products in this facility are manufactured to the quality control requirements of MIL-STD-883.

All of IDT's facilities are aimed at increasing our manufacturing productivity to supply ever-larger volumes of high-performance, cost-effective, leadership CMOS products.

SUPERIOR QUALITY AND RELIABILITY

Maintaining the highest standards of quality in the industry on all products is the basis of Integrated Device Technology's manufacturing systems and procedures. From inception, quality and reliability are built into all of IDT's products. Quality is "designed in" at every stage of manufacturing – as opposed to being "tested-in" later – in order to ensure impeccable performance.

Dedicated commitment to fine workmanship, along with development of rigid controls throughout wafer fab, device assembly and electrical test, create inherently reliable products. Incoming materials are subjected to careful inspections. Quality monitors, or inspections, are performed throughout the manufacturing flow.

IDT military grade monolithic hermetic products are designed to meet or exceed the demanding Class B reliability levels of MIL-STD-883 and MIL-M-38510, as defined by Paragraph 1.2.1 of MIL-STD-883.

Product flow and test procedures for all monolithic hermetic military grade products are in accordance with the latest revision and notice of MIL-STD-883. State-of-the-art production techniques and computer-based test procedures are coupled with tight controls and inspections to ensure that products meet the requirements for 100% screening. Routine quality conformance lot testing is performed as defined in MIL-STD-883, Methods 5004 and 5005.

For IDT module products, screening of the fully assembled substrates is performed, in addition to the monolithic level screening, to assure package integrity and mechanical reliability. All modules receive 100% electrical tests (DC, functional and dynamic switching) to ensure compliance with the "subsystem" specifications.

By maintaining these high standards and rigid controls throughout every step of the manufacturing process, IDT ensures that commercial, industrial and military grade products consistently meet customer requirements for quality, reliability and performance.

SPECIAL PROGRAMS

Class S. IDT also has all manufacturing, screening and test capabilities in-house (except X-ray and some Group D tests) to perform complete Class S processing per MIL-STD-883 on all IDT products and has supplied Class S products on several programs.

Radiation Hardened. IDT has developed and supplied several levels of radiation hardened products for military/ aerospace applications to perform at various levels of dose rate, total dose, single event upset (SEU), upset and latchup. IDT products maintain nearly their same high-performance levels built to these special process requirements. The company has in-house radiation testing capability used both in process development and testing of deliverable product. IDT also has a separate group within the company dedicated to supplying products for radiation hardened applications and to continue research and development of process and products to further improve radiation hardening capabilities.

QSP–QUALITY, SERVICE AND PERFORMANCE

Quality from the beginning, is the foundation for IDT's commitment to supply consistently high-quality products to our customers. IDT's quality commitment is embodied in its all pervasive Continuous Quality Improvement (CQI) process. Everyone who influences the quality of the product–from the designer to the shipping clerk–is committed to constantly improving the quality of their actions.

IDT QUALITY PHILOSOPHY

"To make quantitative constant improvement in the quality of our actions that result in the supply of leadership products in conformance to the requirements of our customers."

IDT's ASSURANCE STRATEGY FOR CQI

Measurable standards are essential to the success of CQI. All the processes contributing to the final quality of the product need to be monitored, measured and improved upon through the use of statistical tools.

PRODUCT FLOW

DEVELOPMENT
|
FAB
|
ASSEMBLY
|
TEST
|
SHIP

Our customers receive the benefit of our optimized systems. Installed to enhance quality and reliability, these systems provide accurate and timely reporting on the effectiveness of manufacturing controls and the reliability and quality performance of IDT products and services.

SERVICE FLOW

ORDER ENTRY
|
PRODUCTION CONTROL
|
SHIPPING
|
CUSTOMER SUPPORT

These systems and controls concentrate on CQI by focusing on the following key elements:

Statistical Techniques
Using statistical techniques, including Statistical Process Control (SPC) to determine whether the product/ processes are under control.

Standardization
Implementing policies, procedures and measurement techniques that are common across different operational areas.

Documentation
Documenting and training in policies, procedures, measurement techniques and updating through characterization/ capability studies.

Productivity Improvement
Using constant improvement teams made up from employees at all levels of the organization.

Leadership
Focusing on quality as a key business parameter and strategic strength.

Total Employee Participation
Incorporating the CQI process into the IDT Corporate Culture.

Customer Service
Supporting the customer, as a partner, through performance review and pro-active problem solving.

People Excellence
Committing to growing, motivating and retaining people through training, goal setting, performance measurement and review.

PRODUCT FLOW

Product quality starts here. IDT has mechanisms and procedures in place that monitor and control the quality of our development activities. From the calibration of design capture libraries through process technology and product characterization that establish whether the performance, ratings and reliability criteria have been met. This includes failure analysis of parts that will improve the prototype product.

At the pre-production stage once again in-house qualification tests assure the quality and reliability of the product. All specifications and manufacturing flows are established and personnel trained before the product is placed into production.

Manufacturing
To accomplish CQI during the manufacturing stage, control items are determined for major manufacturing conditions. Data is gathered and statistical techniques are used to control specific manufacturing processes that affect the quality of the product.

In-process and final inspections are fed back to earlier processes to improve product quality. All product is burned-in (where applicable) before 100% inspection of electrical characteristics takes place.

Products which pass final inspection are then subject to Quality Assurance and Reliability Tests. This data is used to improve manufacturing processes and provide reliability predictions of field applications.

Inventory and Shipping

Controls in shipping focus on ensuring parts are identified and packaged correctly. Care is also taken to see that the correct paperwork is present and the product being shipped was processed correctly.

SERVICE FLOW

Quality not only applies to the product but to the quality-of-service we give our customers. Service is also constantly monitored for improvement.

Order Procedures

Checks are made at the order entry stage to ensure the correct processing of the Customer's product. After verification and data entry the Acknowledgements (sent to Customers) are again checked to ensure details are correct. As part of the CQI process, the results of these verifications are analyzed using statistical techniques and corrective actions are taken.

Production Control

Production Control (P.C.) is responsible for the flow and logistics of material as it moves through the manufacturing processes. The quality of the actions taken by P.C. greatly influences the quality of service the customer receives. Because many of our customers have implemented Just-in-Time (JIT) manufacturing practices, IDT as a supplier has adopted these same disciplines. As a result, employees receive extensive training and the performance level of key actions are kept under constant review. These key actions include:

Quotation response and accuracy.
Scheduling response and accuracy.
Response and accuracy of Expedites.
Inventory, management, and effectiveness.
On-time delivery.

Customer Support

IDT has a worldwide network of sales offices and Technical Development Centers. These provide local customer support on business transactions, and in addition, support customers on applications information, technical services, benchmarking of hardware solutions, and demonstration of various Development Workstations.

The key to CQI is the timely resolution of defects and implementation of the corrective actions. This is no more important than when product failures are found by a customer. When failures are found at the customer's incoming inspection, in the production line, or the field application, the Division Quality Assurance group is the focal point for the investigation of the cause of failure and implementation of the corrective action. IDT constantly improves the level of support we give our customers by monitoring the response time to customers who have detected a product failure. Providing the customer with an analysis of the failure, including corrective actions and the statistical analysis of defects, brings CQI full circle–full support of our customers and their designs with high-quality products.

SUMMARY

In 1990, IDT made the commitment to *"Leadership through Quality, Service, and Performance Products"*.

We believe by following this credo IDT and our customers will be successful in the coming decade. With the implementation of the CQI strategy within the company, we will satisfy our goal...

"Leadership through Quality, Service and Performance Products".

IDT QUALITY CONFORMANCE PROGRAM

A COMMITMENT TO QUALITY

Integrated Device Technology's monolithic assembly products are designed, manufactured and tested in accordance with the strict controls and procedures required by Military Standards. The documentation, design and manufacturing criteria of the Quality and Reliability Assurance Program were developed and are being maintained to the most current revisions of MIL-38510 as defined by paragraph 1.2.1 of MIL-STD-883 and MIL-STD-883 requirements.

Product flow and test procedures for all Class B *monolithic* hermetic Military Grade microcircuits are in full compliance with paragraph 1.2.1 of MIL-STD-883. State-of-the-art production techniques and computer-based test procedures are coupled with stringent controls and inspections to ensure that products meet the requirements for 100% screening and quality conformance tests as defined in MIL-STD-883, Methods 5004 and 5005.

Product flow and test procedures for all *plastic* and *commercial hermetic* products are in accordance with industry practices for producing highly reliable microcircuits to ensure that products meet the IDT requirements for 100% screening and quality conformance tests.

By maintaining these high standards and rigid controls throughout every step of the manufacturing process, IDT ensures that our products consistently meet customer requirements for quality, reliability and performance.

SUMMARY

Monolithic Hermetic Package Processing Flow(1)

Refer to the Monolithic Hermetic Package Processing Flow diagram. All test methods refer to MIL-STD-883 unless otherwise stated.

1. **Wafer Fabrication:** Humidity, temperature and particulate contamination levels are controlled and maintained according to criteria patterned after Federal Standard 209, Clean Room and Workstation Requirements. All critical workstations are maintained at Class 100 levels or better.

   Wafers from each wafer fabrication area are subjected to Scanning Electron Microscope analysis on a periodic basis.

2. **Die Visual Inspection:** Wafers are cut and separated and the individual die are 100% visually inspected to strict IDT-defined internal criteria.

3. **Die Shear Monitor:** To ensure die attach integrity, product samples are routinely subjected to a shear strength test per Method 2019.

4. **Wire Bond Monitor:** Product samples are routinely subjected to a strength test per Method 2011, Condition D, to ensure the integrity of the lead bond process.

5. **Pre-Cap Visual:** Before the completed package is sealed, 100% of the product is visually inspected to Method 2010, Condition B criteria.

6. **Environmental Conditioning:** 100% of the sealed product is subjected to environmental stress tests. These thermal and mechanical tests are designed to eliminate units with marginal seal, die attach or lead bond integrity.

7. **Hermetic Testing:** 100% of the hermetic packages are subjected to fine and gross leak seal tests to eliminate marginally sealed units or units whose seals may have become defective as a result of environmental conditioning tests.

8. **Pre-Burn-In Electrical Test:** Each product is 100% electrically tested at an ambient temperature of +25°C to IDT data sheet or the customer specification.

9. **Burn-In:** 100% of the Military Grade product is burned-in under dynamic electrical conditions to the time and temperature requirements of Method 1015, Condition D. Except for the time, Commercial Grade product is burned-in as applicable to the same conditions as Military Grade devices.

10. **Post-Burn-In Electrical:** After burn-in, 100% of the Class B Military Grade product is electrically tested to IDT data sheet or customer specifications over the –55°C to +125°C temperature range. Commercial Grade products are sample tested to the applicable temperature extremes.

11. **Mark:** All product is marked with product type and lot code identifiers. MIL-STD-883 compliant Military Grade products are identified with the required compliant code letter.

12. **Quality Conformance Tests:** Samples of the Military Grade product which have been processed to the 100% screening tests of Method 5004 are routinely subjected to the quality conformance requirements of Method 5005.

NOTE:

1. For quality requirements beyond Class B levels such as SEM analysis, X-Ray inspection, Particle Impact Noise Reduction (PIND) test, Class S screening or other customer specified screening flows, please contact your Integrated Device Technology sales representative.

SUMMARY

Monolithic Plastic Package Processing Flow

Refer to the Monolithic Plastic Package Processing Flow diagram. All test methods refer to MIL-STD-883 unless otherwise stated.

1. **Wafer Fabrication:** Humidity, temperature and particulate contamination levels are controlled and maintained according to criteria patterned after Federal Standard 209, Clean Room and Workstation Requirements. All critical workstations are maintained at Class 100 levels or better.

   Topside silicon nitride passivation is all applied to all wafers for better moisture barrier characteristics.

   Wafers from each wafer fabrication area are subjected to Scanning Electron Microscope analysis on a periodic basis.

2. **Die Visual Inspection:** Wafers are 100% visually inspected to strict IDT defined internal criteria.

3. **Die Push Test:** To ensure die attach integrity, product samples are routinely subjected to die push tests, patterned after MIL-STD-883, Method 2019.

4. **Wire Bond Monitor:** Product samples are routinely subjected to wire bond pull and ball shear tests to ensure the integrity of the wire bond process, patterned after MIL-STD-883, Method 2011, Condition D.

5. **Pre-Cap Visual:** Before encapsulation, all product lots are visually inspected (using LTPD 5 sampling plan) to criteria patterned after MIL-STD-883, Method 2010, Condition B.

6. **Post Mold Cure:** Plastic encapsulated devices are baked to ensure an optimum polymerization of the epoxy mold compound so as to enhance moisture resistance characteristics.

7. **Pre-Burn-In Electrical:** Each product is 100% electrically tested at an ambient temperature of +25°C to IDT data sheet or the customer specification.

8. **Burn-In:** Except for MSI Logic family devices where it may be obtained as an option, all Commercial Grade plastic package products are burned-in for 16 hours at +125°C minimum (or equivalent), utilizing the same burn-in conditions as the Military Grade product.

9. **Post-Burn-In Electrical:** After burn-in, 100% of the plastic product is electrically tested to IDT data sheet or customer specifications at the maximum temperature extreme. The minimum temperature extreme is tested periodically on an audit basis.

10. **Mark:** All product is marked with product type and lot code identifiers. Products are identified with the assembly and test locations.

11. **Quality Conformance Inspection:** Samples of the plastic product which have been processed to the 100% screening requirements are subjected to the Periodic Quality Conformance Inspection Program. Where indicated, the test methods are patterned after MIL-STD-883 criteria.

TABLE 1

This table defines the device class screening procedures for IDT's high reliability products in conformance with MIL-STD-883C.

Monolithic Hermetic Package Final Processing Flow

	CLASS-S		CLASS-B		CLASS-C [1]	
OPERATION	**TEST METHOD**	**RQMT**	**TEST METHOD**	**RQMT**	**TEST METHOD**	**RQMT**
BURN-IN	1015 Cond. D, 240 Hrs @ 125°C or equivalent	100%	1015 Cond. D, 160 Hrs. @ 125°C min or equivalent	100%	Per applicable device specification	100%
POST BURN-IN ELECTRICAL: Static (DC), Functional and Switching (AC)	Per applicable device specification +25, -55 and 125°C	100%	Per applicable device specification +25, -55 and 125°C	100%	Per applicable [2] device specification	100%
Group A ELECTRICAL: Static (DC), Functional and Switching (AC)	Per applicable device specification and 5005	Sample	Per applicable device specification and 5005	Sample	Per applicable [2] device specification	Sample
MARK/LEAD STRAIGHTENING	IDT Spec	100%	IDT Spec	100%	IDT Spec	100%
FINAL ELECTRICAL TEST	Per applicable device specification +25°C	100%	Per applicable device specification +25°C	100%	Per applicable device specification +25°C	100%
FINAL VISUAL/PACK	IDT Spec	100%	IDT Spec	100%	IDT Spec	100%
QUALITY CONFORMANCE INSPECTION	5005 Group B, C, D.	Sample	5005 Group B,C,D.	Sample	IDT Spec	Sample
QUALITY SHIPPING INSPECTION (Visual/Plant Clearance)	IDT Spec	100%	IDT Spec	100%	IDT Spec	100%

NOTES:
1. Class-C = IDT commercial spec. for hermetic and plastic packages
2. Typical 0°C, 70°C, Extended -55°C +125°C

RADIATION TOLERANT/ENHANCED/HARDENED PRODUCTS FOR RADIATION ENVIRONMENTS

INTRODUCTION

The need for high-performance CMOS integrated circuits in military and space systems is more critical today than ever before. The low power dissipation that is achieved using CMOS technology, along with the high complexity and density levels, makes CMOS the nearly ideal component for all types of applications.

Systems designed for military or space applications are intended for environments where high levels of radiation may be encountered. The implication of a device failure within a military or space system clearly is critical. IDT has made a significant contribution toward providing reliable radiation-tolerant systems by offering integrated circuits with enhanced radiation tolerance. Radiation environments, IDT process enhancements and device tolerance levels achieved are described below.

THE RADIATION ENVIRONMENT

There are four different types of radiation environments that are of concern to builders of military and space systems. These environments and their effects on the device operation, summarized in Figure 1, are as follows:

Total Dose Accumulation refers to the total amount of accumulated gamma rays experienced by the devices in the system, and is measured in RADS (SI) for radiation units experienced at the silicon level. The physical effect of gamma rays on semiconductor devices is to cause threshold shifts (Vt shifts) of both the active transistors as well as the parasitic field transistors. Threshold voltages decrease as total dose is accumulated; at some point, the device will begin to exhibit parametric failures as the input/output and supply currents increase. At higher radiation accumulation levels, functional failures occur. In memory circuits, however, functional failures due to memory cell failure often occur first.

Burst Radiation or Dose Rate refers to the amount of radiation, usually photons or electrons, experienced by the devices in the system due to a pulse event, and is measured in RADS (Si) per second. The effect of a high dose rate or burst of radiation on CMOS integrated circuits is to cause temporary upset of logic states and/or CMOS latch-up. Latch-up can cause permanent damage to the device.

Single Event Upset (SEU) is a transient logic state change caused by high-energy ions, such as energetic cosmic rays, striking the integrated circuits. As the ion passes through the silicon, charge is either created through ionization or direct nuclear collision. If collected by a circuit node, this excess charge can cause a change in logic state of the circuit. Dynamic nodes that are not actively held at a particular logic state (dynamic RAM cells for example) are the most susceptible. These upsets are transient, but can cause system failures known as "soft errors."

Neutron Irradiation will cause structural damage to the silicon lattice which may lead to device leakage and, ultimately, functional failure.

Radiation Category	Primary Particle	Source	Effect
Total Dose	Gamma	Space or Nuclear Event	Permanent
Dose Rate	Photons	Nuclear Event	Temporary Upset of Logic State or Latch-up
SEU	Cosmic Rays	Space	Temporary Upset of Logic State
Neutron	Neutrons	Nuclear Event	Device Leakage Due to Silicon Lattice Damage

2510 drw 01

Figure 1.

DEVICE ENHANCEMENTS

Of the four radiation environments above, IDT has taken considerable data on the first two, Total Dose Accumulation and Dose Rate. IDT has developed a process that significantly improves the radiation tolerance of its devices within these environments. Prevention of SEU failures is usually accomplished by system-level considerations, such as Error Detection and Correction (EDC) circuitry, since the occurrence of SEUs is not particularly dependent on process technology. Through IDT's customer contracts, SEU has been gathered on some devices. Little is yet known about the effects of neutron-induced damage. For more information on SEU testing, contact IDT's Radiation Hardened Product Group.

Enhancements to IDT's standard process are used to create radiation enhanced and tolerant processes. Field and gate oxides are "hardened" to make the device less susceptible to radiation damage by modifying the process architecture to allow lower temperature processing. Device implants and Vts adjustments allow more Vt margin. In addition to process changes, IDT's radiation enhanced process utilizes epitaxial substrate material. The use of epi substrate material provides a lower substrate resistance environment to create latch-up free CMOS structures.

RADIATION HARDNESS CATEGORIES

Radiation Enhanced (RE) or Radiation Tolerant ('RT) versions of IDT products follow IDT's military product data sheets whenever possible (consult factory). IDT's Total Dose Test plan exposes a sample of die on a wafer to a particular Total Dose level via ARACOR X-Ray radiation. This Total Dose Test plan qualifies each 'RE or 'RT wafer to a Total Dose level. Only wafers with sampled die that pass Total Dose level tests are assembled and used for orders (consult factory for more details on Total Dose sample testing). With regard to Total Dose testing, clarifications/exceptions to MIL-STD-883,

Methods 5005 and 1019 are required. Consult factory for more details.

The 'RE and 'RT process enhancements enable IDT to offer integrated circuits with varying grades of radiation tolerance or radiation "hardness".

- Radiation Enhanced process uses Epi wafers and is able to provide devices that can be Total Dose qualified to 10K RADs (Si) or greater by IDT's ARACOR X-Ray Total Dose sample die test plan (Total Dose levels require negotiation, consult factory for more details).
- Radiation Tolerant product uses standard wafer/process material that is qualified to 10K RADs (Si) Total Dose by IDT's ARACOR X-Ray Total Dose sample die test plan.

Integrated Device Technology can provide Radiation Tolerant/Enhanced versions of all product types (some speed grades may not be available as 'RE).

Please contact your IDT sales representative or factory marketing to determine availability and price of any IDT product processed in accordance with one of these levels of radiation hardness.

CONCLUSION

There has been widespread interest within the military and space community in IDT's CMOS product line for its radiation hardness levels, as well as its high-performance and low power dissipation. To serve this growing need for CMOS circuits that must operate in a radiation environment, IDT has created a separate group within the company to concentrate on supplying products for these applications.Continuing research and development of process and products, including the use of in-house radiation testing capability, will allow Integrated Device Technology to offer continuously increasing levels of radiation-tolerant solutions.

THERMAL PERFORMANCE CALCULATIONS FOR IDT'S PACKAGES

Since most of the electrical energy consumed by microelectronic devices eventually appears as heat, poor thermal performance of the device or lack of management of this thermal energy can cause a variety of deleterious effects. This device temperature increase can exhibit itself as one of the key variables in establishing device performance and long term reliability; on the other hand, effective dissipation of internally generated thermal energy can, if properly managed, reduce the deleterious effects and improve component reliability.

A few key benefits of IDT's enhanced CMOS process are: low power dissipation, high speed, increased levels of integration, wider operating temperature ranges and lower quiescent power dissipation. Because the reliability of an integrated circuit is largely dependent on the maximum temperature the device attains during operation, and as the junction stability declines with increases in junction temperature (T_J), it becomes increasingly important to maintain a low (T_J).

CMOS devices stabilize more quickly and at greatly lower temperature than bipolar devices under normal operation. The accelerated aging of an integrated circuit can be expressed as an exponential function of the junction temperature as:

$$t_A = t_o \exp \left[\frac{E_a}{k} \left(\frac{1}{T_o} - \frac{1}{T_J} \right) \right]$$

where

- t_A = lifetime at elevated junction (T_J) temperature
- t_o = normal lifetime at normal junction (T_o) temperature
- E_a = activation energy (ev)
- k = Boltzmann's constant (8.617×10^{-5}ev/k)

i.e. the lifetime of a device could be decreased by a factor of 2 for every 10°C increase temperature.

To minimize the deleterious effects associated with this potential increase, IDT has:

1. Optimized our proprietary low-power CMOS fabrication process to ensure the active junction temperature rise is minimal.
2. Selected only packaging materials that optimize heat dissipation, which encourages a cooler running device.
3. Physically designed all package components to enhance the inherent material properties and to take full advantage of heat transfer and radiation due to case geometries.
4. Tightly controlled the assembly procedures to meet or exceed the stringent criteria of MIL-STD-883 to ensure maximum heat transfer between die and packaging materials.

The following figures graphically illustrate the thermal values of IDT's current package families. Each envelope (shaded area) depicts a typical spread of values due to the influence of a number of factors which include: circuit size, package materials and package geometry. The following range of values are to be used as a comprehensive characterization of the major variables rather than single point of reference.

When calculating junction temperature (T_J), it is necessary to know the thermal resistance of the package (θ_{JA}) as measured in "degree celsius per watt". With the accompanying data, the following equation can be used to establish thermal performance, enhance device reliability and ultimately provide you, the user, with a continuing series of high-speed, low-power CMOS solutions to your system design needs.

$$\theta_{JA} = [T_J - T_A]/P$$
$$T_J = T_A + P[\theta_{JA}] = T_A + P[\theta_{JC} + \theta_{CA}]$$

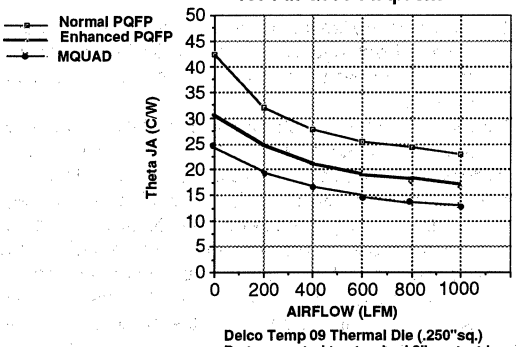
where

$$_{JJC} = \frac{T_J - T_C}{P} \qquad \theta_{CA} = \frac{T_C - T_A}{P}$$

- θ = Thermal resistance
- J = Junction
- P = Operational power of device (dissipated)
- T_A = Ambient temperature in degree celsius
- T_J = Temperature of the junction
- T_C = Temperature of case/package
- θ_{CA} = Case to Ambient, thermal resistance—usually a measure of the heat dissipation due to natural or forced convection, radiation and mounting techniques.
- θ_{JC} = Junction to Case, thermal resistance—usually measured with reference to the temperature at a specific point on the package (case) surface. (Dependent on the package material properties and package geometry.)
- θ_{JA} = Junction to Ambient, thermal resistance—usually measured with respect to the temperature of a specified volume of still air. (Dependent on θ_{JC} + θ_{JA} which includes the influence of area and environmental condition.)

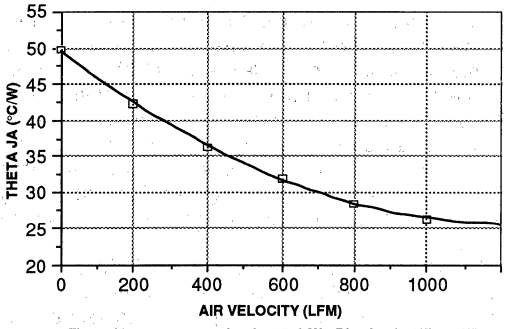
Ref. MIL-STD-883C, Method 1012.1
JEDEC ENG. Bulletin No. 20, January 1975
1986 Semi. Std., Vol. 4, Test Methods G30–86, G32–86.

Theta JA vs. Airflow
160 Pin Quad Flatpacks



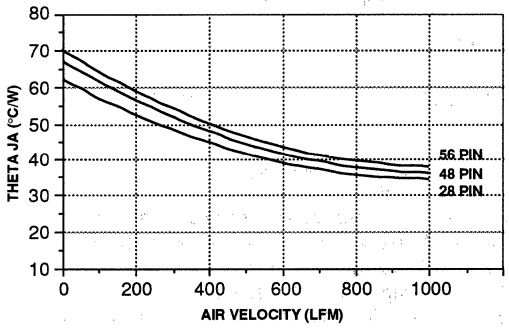
Delco Temp 09 Thermal Die (.250"sq.)
Parts mounted to standard 3" sq. test board.

THETA JA vs. AIR FLOW
32 pin J-bend SOIC

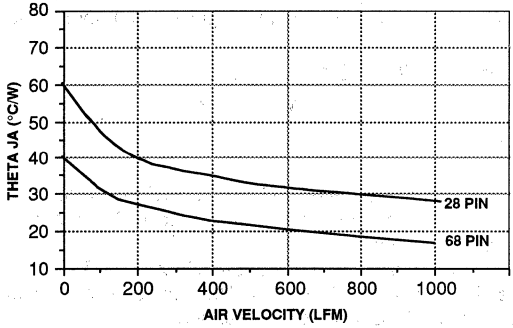


Theta JC was measured to be 17°C/W - Die size (.150"x.250")

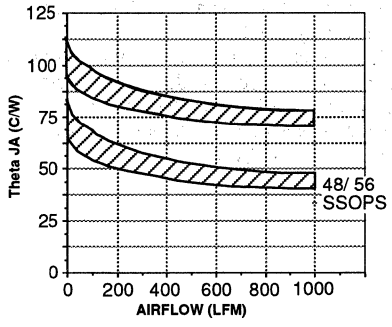
THETA JA vs. AIR FLOW
28/48/56 PIN CERPACKS



THETA JA vs. AIR FLOW
28/68 PIN FLATPACKS

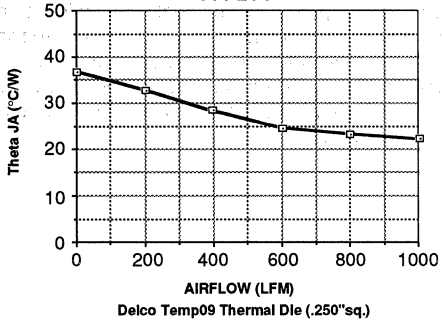


THETA JA vs. AIRFLOW
PLASTIC SSOP PACKAGES



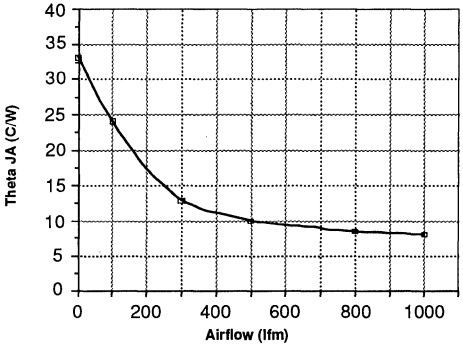
THETA JC : 20/24 PIN = 35-40 °C/W
48/56 PIN = 16-20 °C/W

THETA JA VS. AIRFLOW
84 PLCC



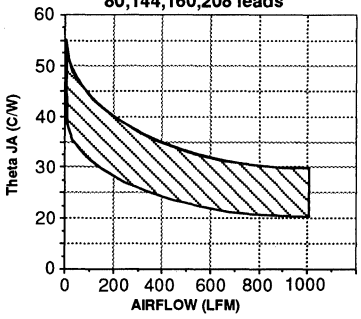
Delco Temp09 Thermal Die (.250"sq.)

Theta JA vs. Airflow
84 pin PGA - Cavity Down w/CuW heatsink



Measurements were done using Temp09 Delco Thermal Die (.250sq.)

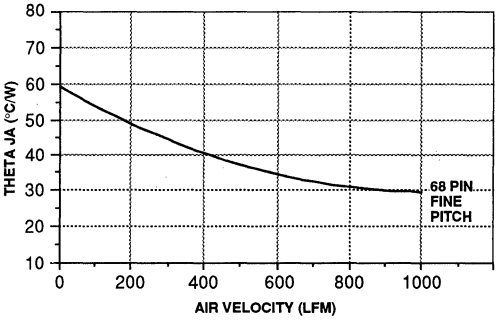
Theta JA vs. Airflow
Plastic Quad Flatpacks
80,144,160,208 leads



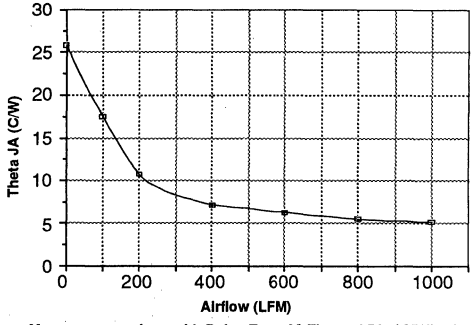
THETA JC : 15-25 °C/W

4

THETA JA vs. AIR FLOW
68 FINE PITCH FLATPACK

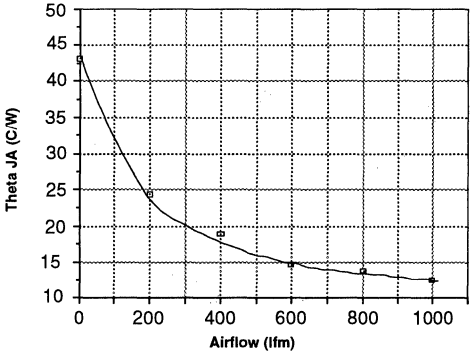


THETA JA vs. AIRFLOW
144 pin PGA - Cavity Down w/ CuW heatsink



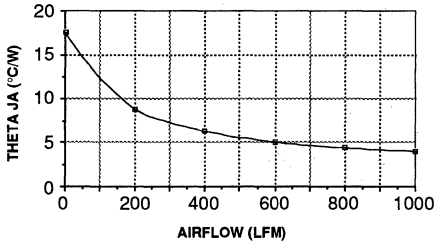
Measurements done with Delco Temp09 Thermal Die (.250"sq.)

Theta JA vs. AIRFLOW
68 pin PGA - Cavity UP



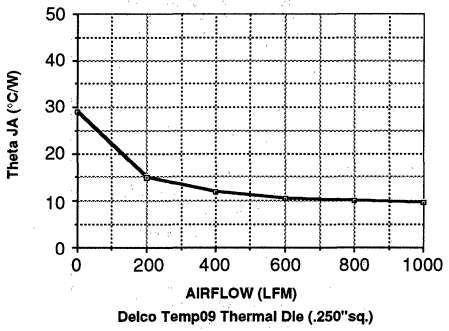
Measurements were done using Temp09 Delco Thermal Die (.250sq.)

THETA JA vs. AIRFLOW
179 PIN PGA - R4000 PACKAGE
INTEGRAL CuW HEATSINK - NO FIN ATTACHED



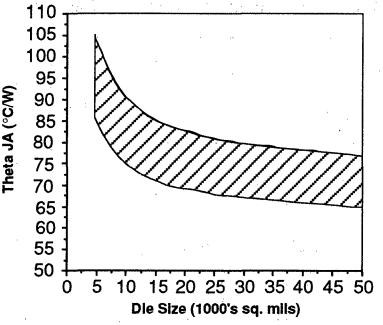
Delco Temp09 Thermal Die Array (.500"sq.)
applied power = 3W

GD 208 THETA JA VS. AIRFLOW

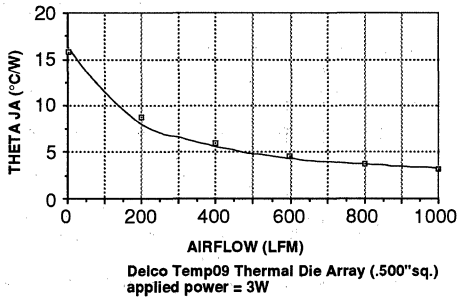


Delco Temp09 Thermal Die (.250"sq.)

Theta JA - Still Air 16-20 Lead Ceramic Dips

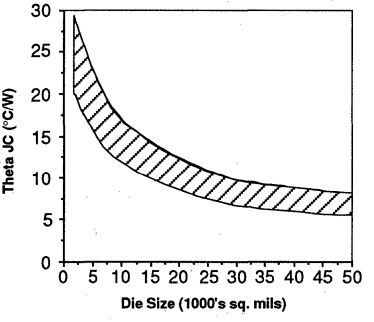


THETA JA vs. AIRFLOW
447 PIN PGA - R4000 PACKAGE
INTEGRAL CuW HEATSINK - NO FIN ATTACHED

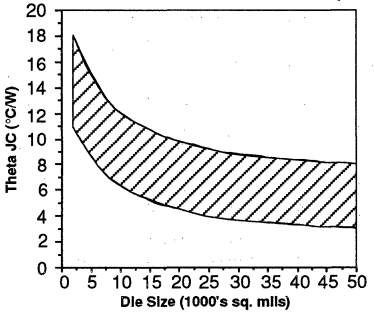


Delco Temp09 Thermal Die Array (.500"sq.)
applied power = 3W

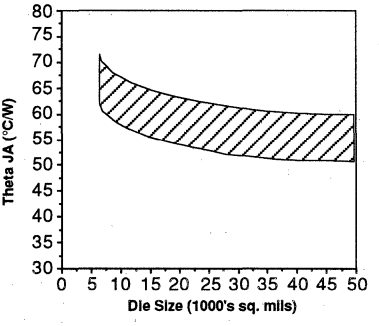
Theta JC 16-20 Lead Ceramic Dip



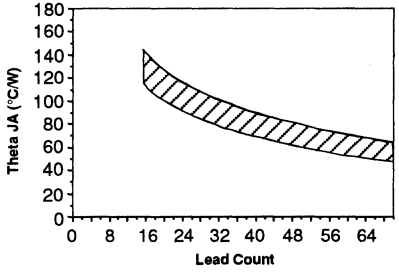
Theta JC 22-40 Lead Ceramic Dips



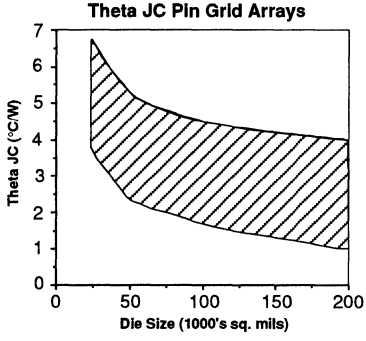
Theta JA - Still Air 22-40 Ceramic Dips



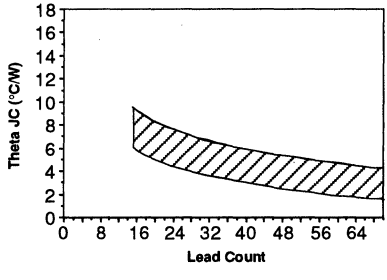
Theta JA Ceramic Flatpacks/Cerpacks



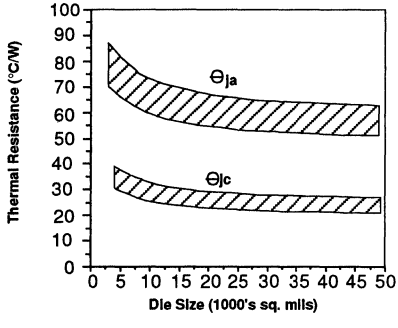
Theta JC Pin Grid Arrays



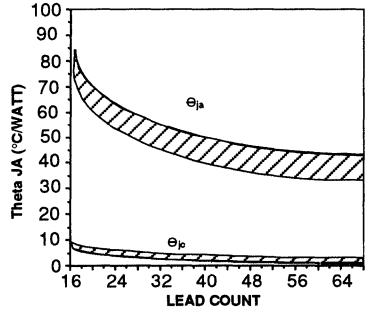
Theta JC Ceramic Flatpacks/Cerpacks



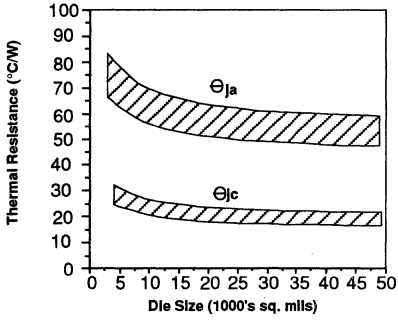
PLASTIC DIPS: 16,18 & 20 PINS



Thermal Resistance of Ceramic LCC's

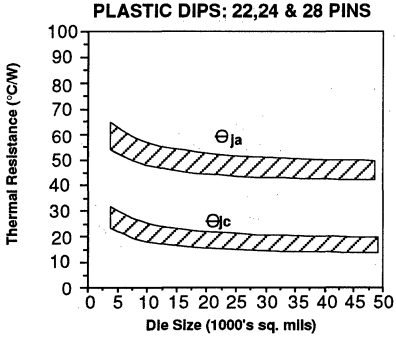


PLASTIC SOICS: 24,28 & 32 PINS

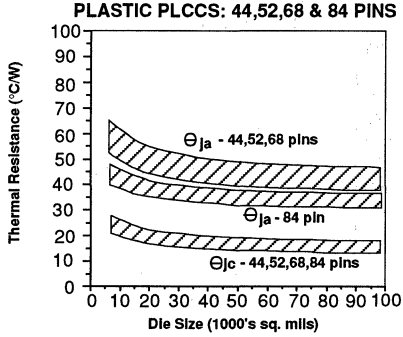


4

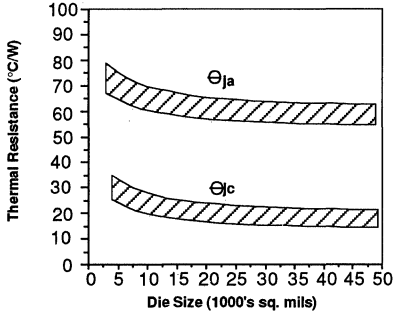
PLASTIC DIPS: 22,24 & 28 PINS



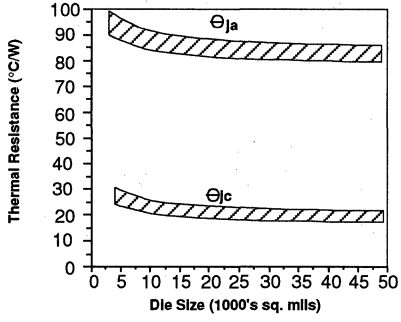
PLASTIC PLCCS: 44,52,68 & 84 PINS



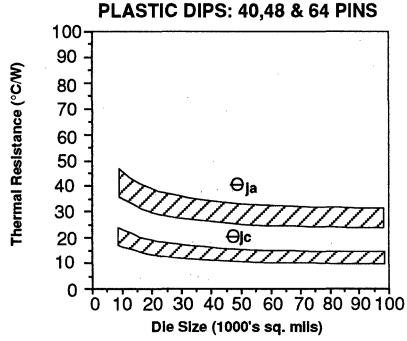
PLASTIC PLCCS: 28 & 32 PINS



PLASTIC SOICS: 16 & 20 PINS



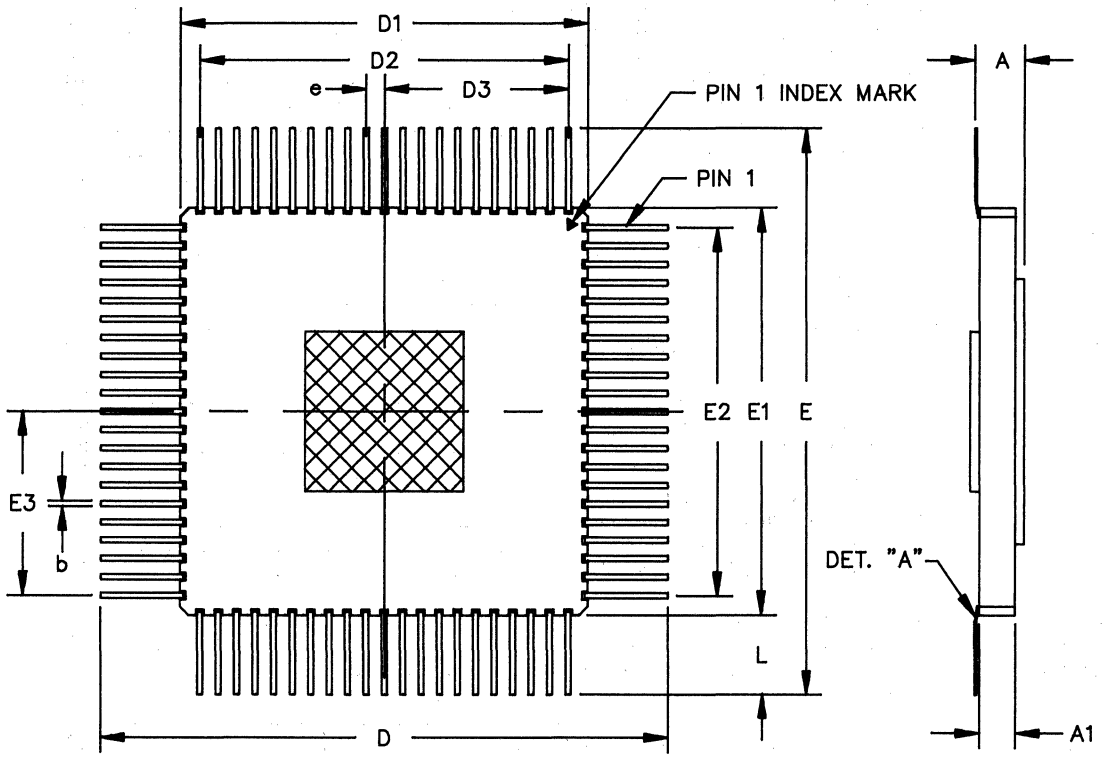
PLASTIC DIPS: 40,48 & 64 PINS



PACKAGE DIAGRAM OUTLINE INDEX

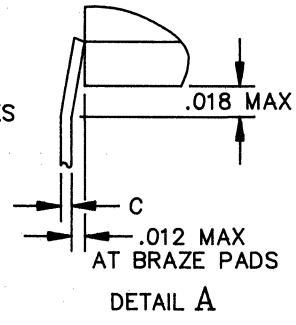
FLATPACKS

84 LEAD QUAD FLATPACK (CAVITY DOWN)



DWG #	F84-1	
# OF LDS (N)	84	
SYMBOL	MIN	MAX
A	–	.140
A1	–	.105
b	.014	.020
C	.007	.013
D/E	1.940	1.960
D1/E1	1.140	1.160
D2/E2	1.000 BSC	
D3/E3	.500 BSC	
e	.050 BSC	
L	.350	.450
ND/NE	21	

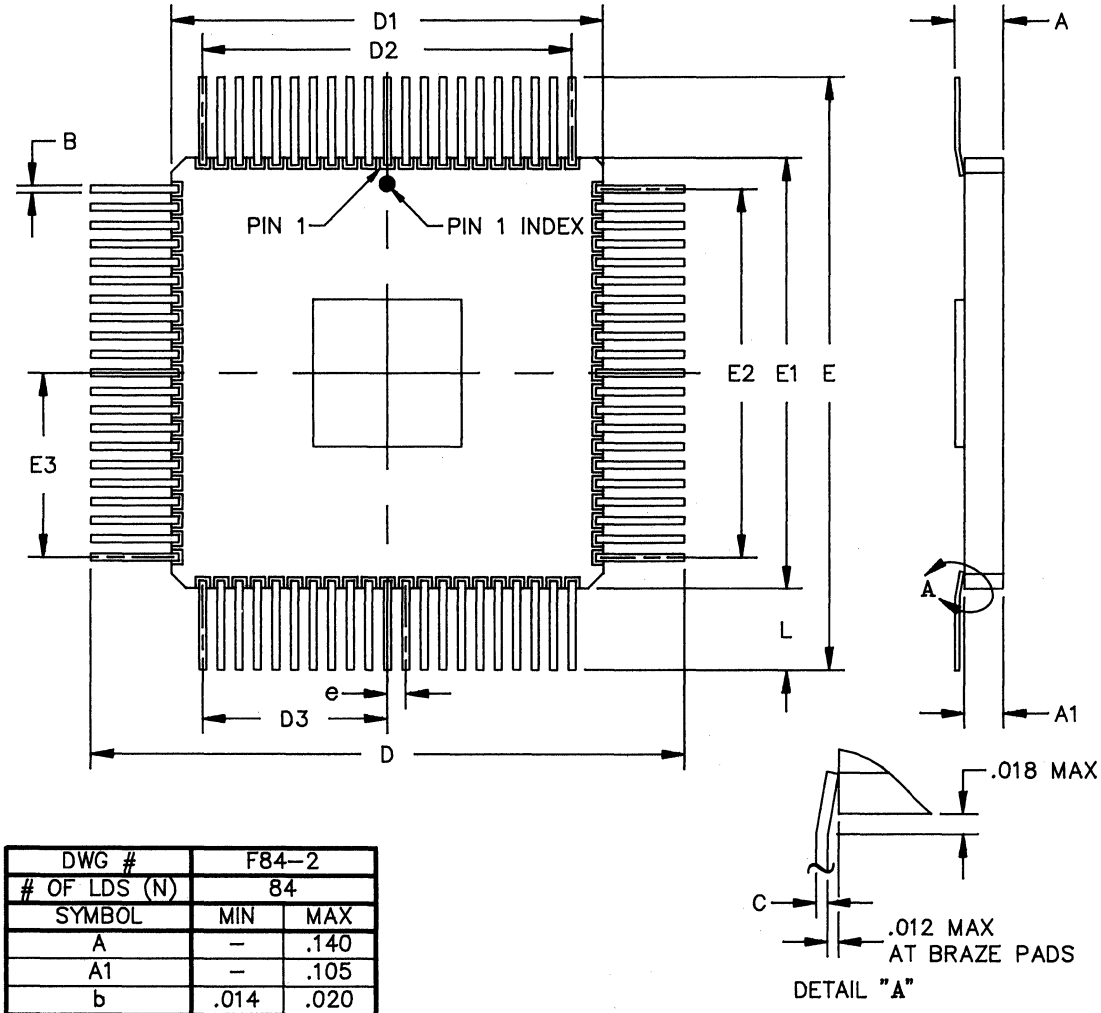
NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. CROSS HATCHED AREA INDICATES INTEGRAL METALLIC HEAT SINK.



DETAIL A

FLATPACKS (Continued)

84 LEAD QUAD FLATPACK (CAVITY UP)



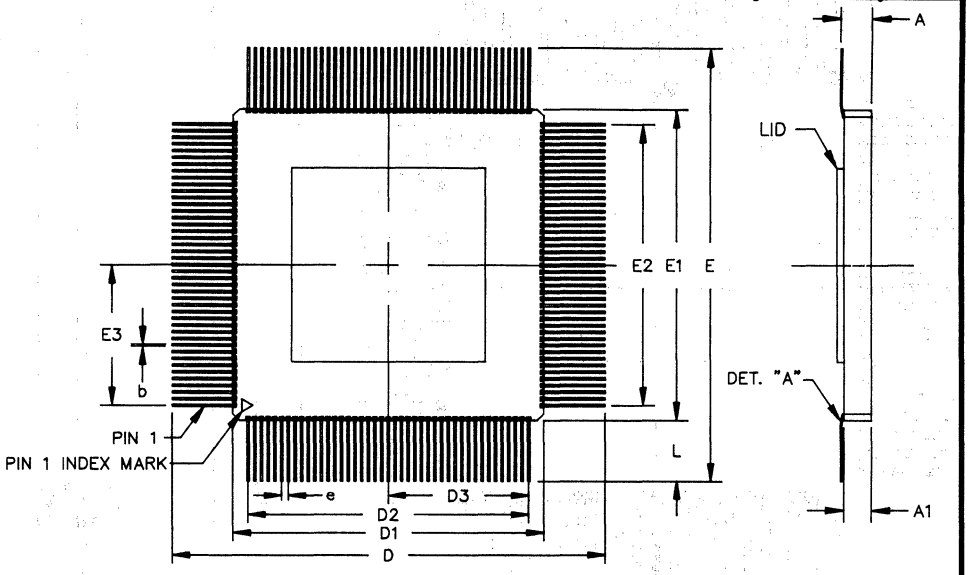
DWG #	F84-2	
# OF LDS (N)	84	
SYMBOL	MIN	MAX
A	–	.140
A1	–	.105
b	.014	.020
C	.007	.013
D/E	1.940	1.960
D1/E1	1.130	1.170
D2/E2	1.000 BSC	
D3/E3	.500 BSC	
e	.050 BSC	
L	.350	.450
ND/NE	21	

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

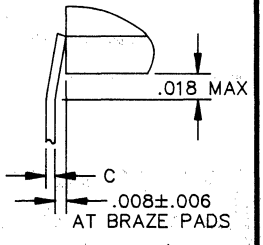
FLATPACKS (Continued)

172 LEAD QUAD FLATPACK (CAVITY UP – R3001)

REV	DCN	DESCRIPTION	DATE	APPROVED
00	23329	INITIAL RELEASE	11/2/92	



NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL DIMENSIONS ARE IN INCHES.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "N" REPRESENTS THE NUMBER OF LEADS.
4. PIN NUMBERING IS CLOCKWISE.



DETAIL A

SYMBOLS	MIN	MAX
A	–	.130
A1	–	.105
b	.006	.010
C	.004	.008
D/E	1.580	1.620
D1/E1	1.135	1.165
D2/E2	1.050 BSC	
D3/E3	.525 BSC	
e	.025 BSC	
L	.220	.230
N	172	
ND/NE	43	

JEDEC	IN PROGRESS
EXCEPTIONS	L = .250 MIN
MIL–M–38510	NOT LISTED
EXCEPTIONS	

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRAC DEC ANGLES
± – ± – ± –

APPROVALS	DATE
DRAWN dd	11/92
CHECKED	11/92

Integrated Device Technology, Inc.
3236 Scott Blvd., Santa Clara, CA 95051
(408) 727–6116 FAX: (408) 727–2328

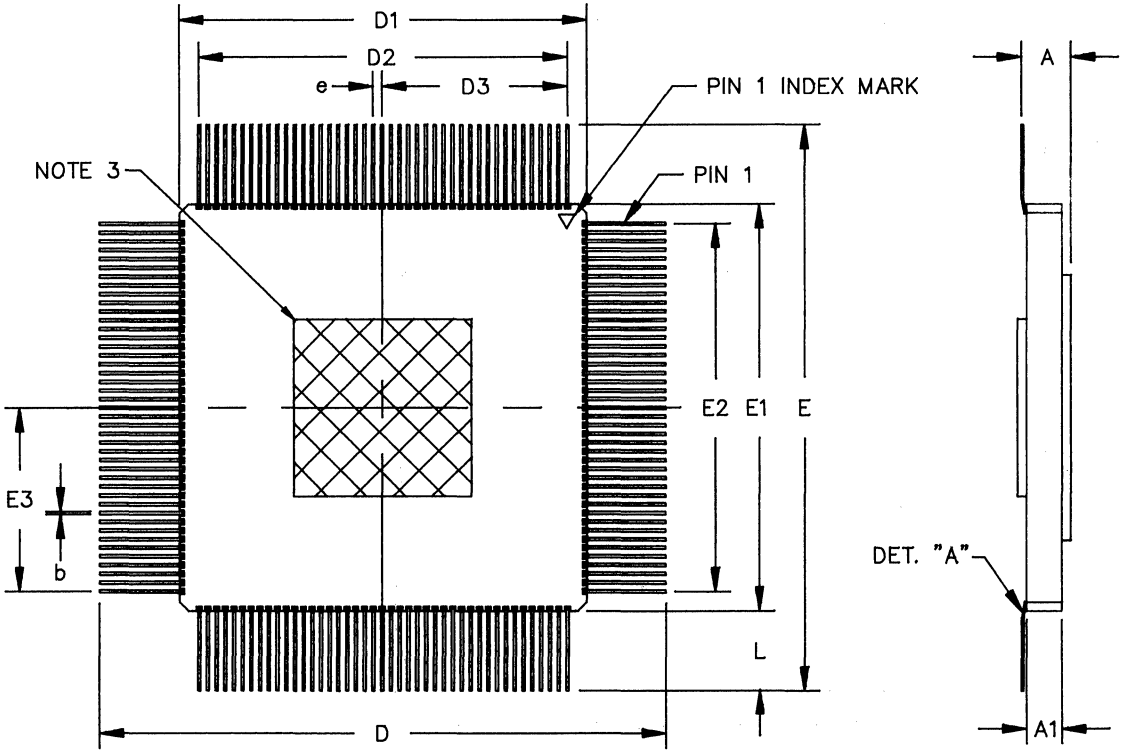
172 LD QUAD FLAT PACK
CAVITY UP – MARKETING DWG

SCALE	SIZE	DRAWING NO.	REV
N/A	A	PSC–2111	00

DO NOT SCALE DRAWING | SHEET 1 OF 1

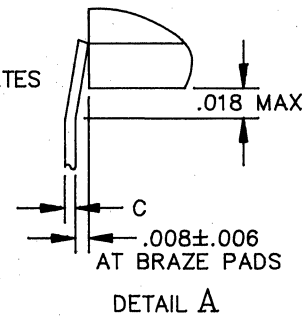
FLATPACKS (Continued)

172 LEAD QUAD FLATPACK (CAVITY DOWN – R3000A)



DWG #	F172-2	
# OF LDS (N)	172	
SYMBOL	MIN	MAX
A	–	.140
A1	–	.105
b	.006	.010
C	.004	.008
D/E	1.580	1.620
D1/E1	1.135	1.165
D2/E2	1.050 BSC	
D3/E3	.525 BSC	
e	.025 BSC	
L	.220	.230
ND/NE	43	

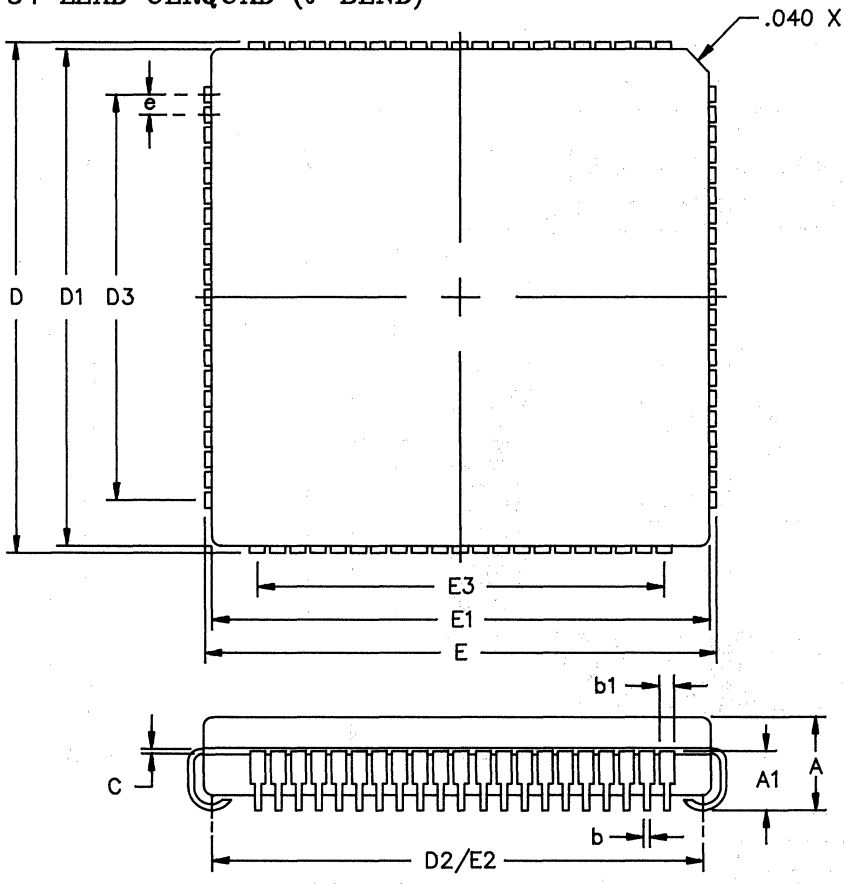
NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. CROSS HATCHED AREA INDICATES METALLIC HEAT SINK.



DETAIL A

CERQUADS

84 LEAD CERQUAD (J-BEND)

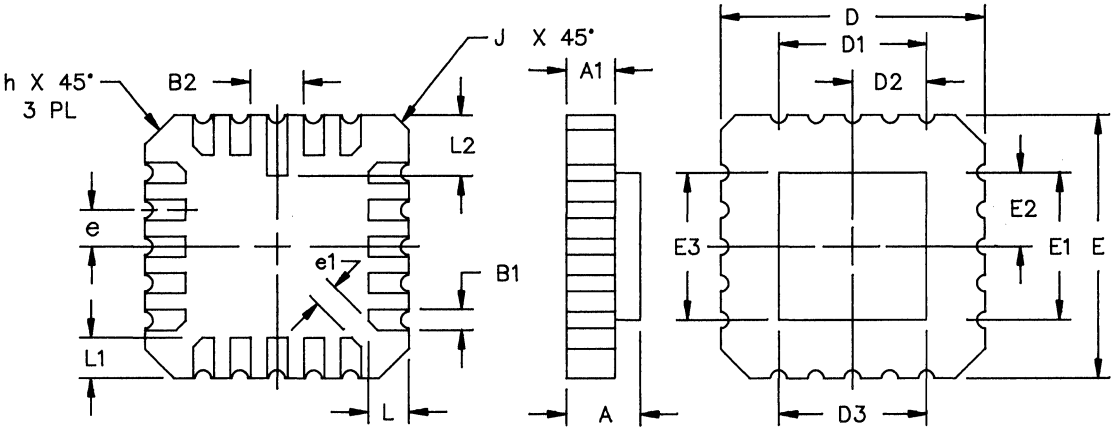


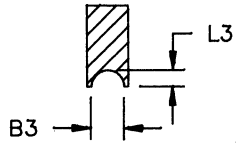
DWG #	CQ84-1	
# OF LDS (N)	84	
SYMBOL	MIN	MAX
A	.155	.200
A1	.090	.120
b1	.022	.032
b	.013	.023
C	.006	.013
D/E	1.170	1.190
D1/E1	1.138	1.162
D2/E2	1.100	.1.150
D3/.E3	1.000 BSC	
e	.050 BSC.	
ND/NE	21	

NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

LEADLESS CHIP CARRIERS





NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

20–48 LEAD LCC (SQUARE)

DWG #	L20–2		L28–1		L44–1		L48–1	
# OF LDS (N)	20		28		44		48	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.064	.100	.064	.100	.064	.120	.055	.120
A1	.054	.066	.050	.088	.054	.088	.045	.090
B1	.022	.028	.022	.028	.022	.028	.017	.023
B2	.072 REF		.072 REF		.072 REF		.072 REF	
B3	.006	.022	.006	.022	.006	.022	.006	.022
D/E	.342	.358	.442	.460	.640	.660	.554	.572
D1/E1	.200 BSC		.300 BSC		.500 BSC		.440 BSC	
D2/E2	.100 BSC		.150 BSC		.250 BSC		.220 BSC	
D3/E3	–	.358	–	.460	–	.560	.500	.535
e	.050 BSC		.050 BSC		.050 BSC		.040 BSC	
e1	.015	–	.015	–	.015	–	.015	–
h	.040 REF		.040 REF		.040 REF		.012 RADIUS	
J	.020 REF		.020 REF		.020 REF		.020 REF	
L	.045	.055	.045	.055	.045	.055	.033	.047
L1	.045	.055	.045	.055	.045	.055	.033	.047
L2	.077	.093	.077	.093	.077	.093	.077	.093
L3	.003	.015	.003	.015	.003	.015	.003	.015
ND/NE	5		7		11		12	

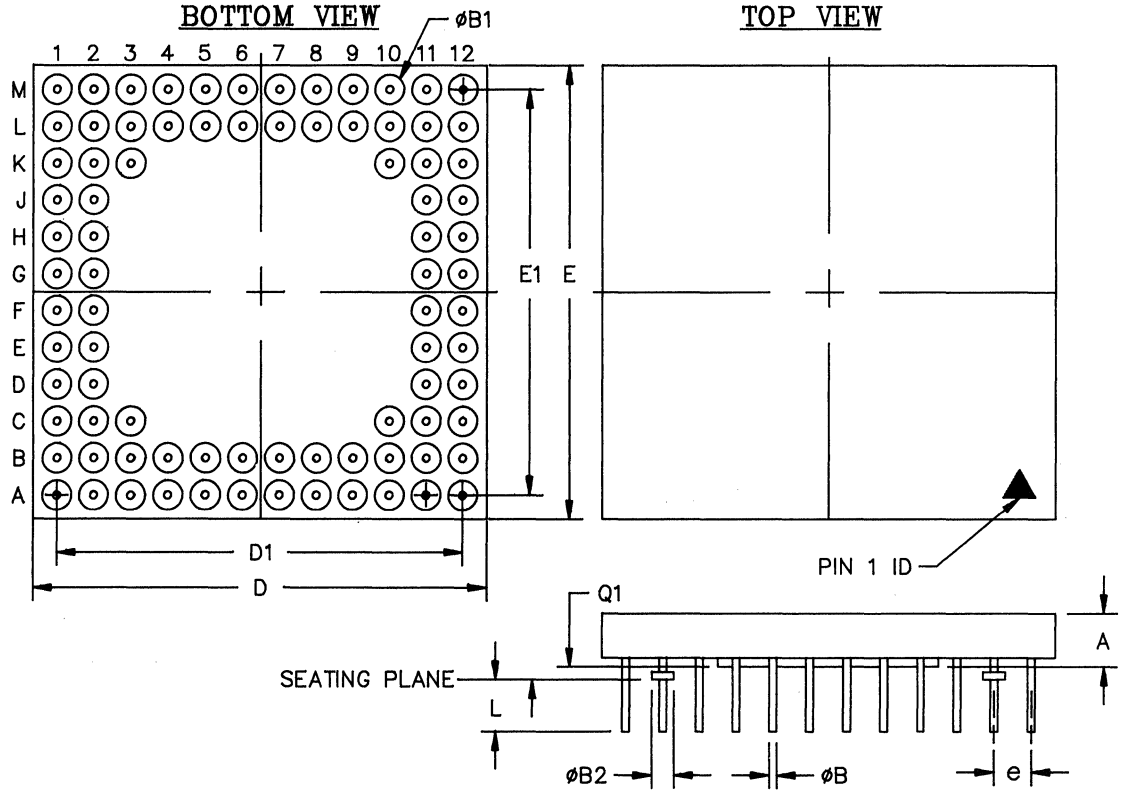
LEADLESS CHIP CARRIERS (Continued)

52–68 LEAD LCC (SQUARE)

DWG #	L52–1		L52–2		L68–2		L68–1	
# OF LDS (N)	52		52		68		68	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.061	.087	.082	.120	.082	.120	.065	.120
A1	.051	.077	.072	.088	.072	.088	.055	.075
B1	.022	.028	.022	.028	.022	.028	.008	.014
B2	.072 REF		.072 REF		.072 REF		.072 REF	
B3	.006	.022	.006	.022	.006	.022	.006	.022
D/E	.739	.761	.739	.761	.938	.962	.554	.566
D1/E1	.600 BSC		.600 BSC		.800 BSC		.400 BSC	
D2/E2	.300 BSC		.300 BSC		.400 BSC		.200 BSC	
D3/E3	–	.661	–	.661	–	.862	–	.535
e	.050 BSC		.050 BSC		.050 BSC		.025 BSC	
e1	.015	–	.015	–	.015	–	.015	–
h	.040 REF		.040 REF		.040 REF		.040 REF	
J	.020 REF		.020 REF		.020 REF		.020 REF	
L	.045	.055	.045	.055	.045	.055	.045	.055
L1	.045	.055	.045	.055	.045	.055	.045	.055
L2	.077	.093	.075	.093	.075	.095	.077	.093
L3	.003	.015	.003	.015	.003	.015	.003	.015
ND/NE	13		13		17		17	

PIN GRID ARRAYS

84 PIN PGA (CAVITY DOWN)

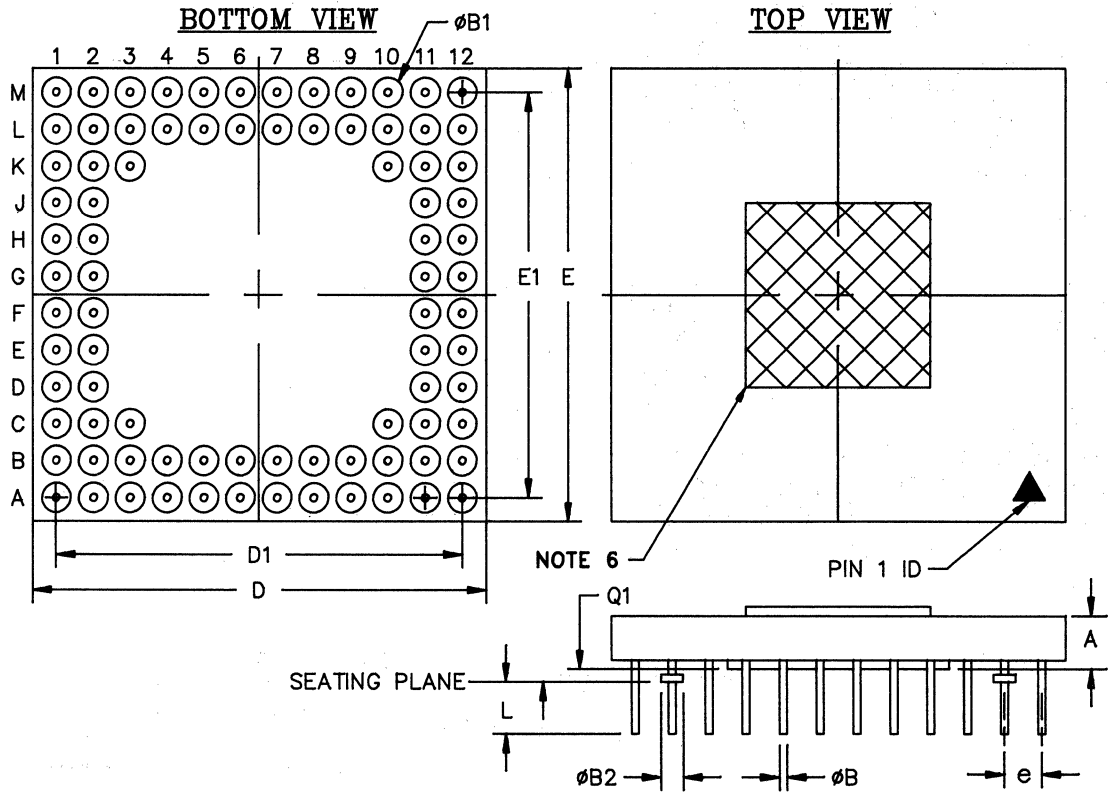


DWG #	G84–2	
# OF PINS (N)	84	
SYMBOL	MIN	MAX
A	.077	.145
øB	.016	.020
øB1	.060	.080
øB2	.040	.060
D/E	1.180	1.235
D1/E1	1.100 BSC	
e	.100 BSC	
L	.100	.120
M	12	
Q1	.025	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

84 PIN PGA (CAVITY DOWN – R3010A)

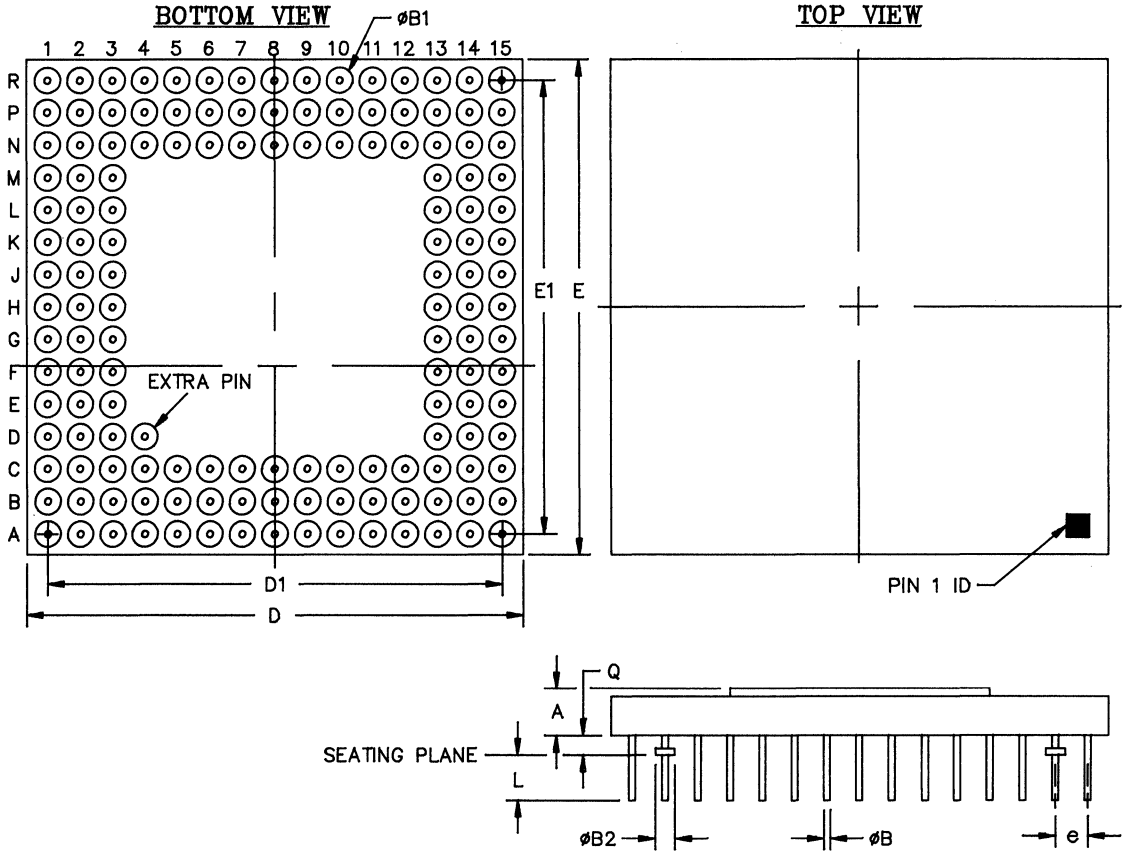


DWG #	G84–4	
# OF PINS (N)	84	
SYMBOL	MIN	MAX
A	.077	.145
øB	.016	.020
øB1	.060	.080
øB2	.040	.060
D/E	1.180	1.235
D1/E1	1.100 BSC	
e	.100 BSC	
L	.120	.140
M	12	
Q1	.025	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.
6. CROSS HATCHED AREA INDICATES INTEGRAL METALLIC HEAT SINK.

PIN GRID ARRAYS (Continued)

144 PIN PGA (CAVITY UP – R3001)

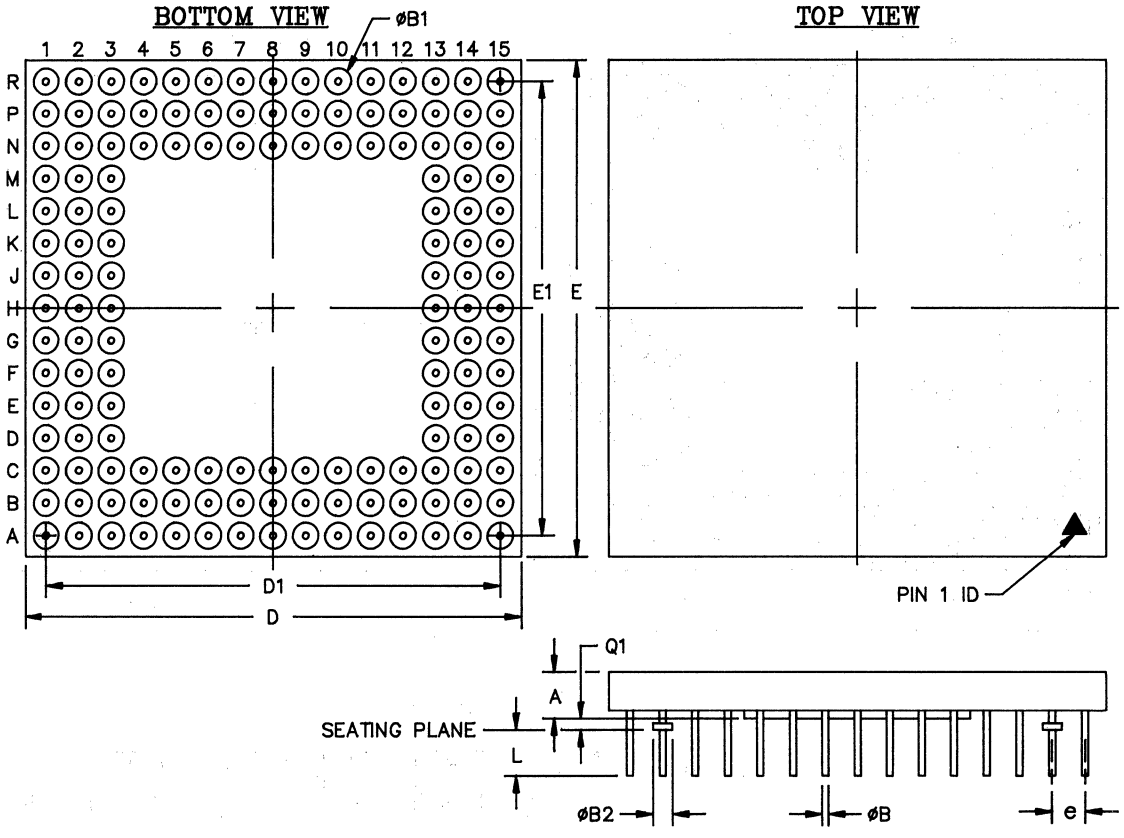


DWG #	G144-2	
# OF PINS (N)	145	
SYMBOL	MIN	MAX
A	.082	.125
ØB	.016	.020
ØB1	.060	.080
ØB2	.040	.060
D/E	1.559	1.590
D1/E1	1.400 BSC	
e	.100 BSC	
L	.120	.140
M	15	
Q	.040	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.
6. EXTRA PIN (D–4) ELECTRICALLY CONNECTED TO D–3.

PIN GRID ARRAYS (Continued)

144 PIN PGA (CAVITY DOWN)

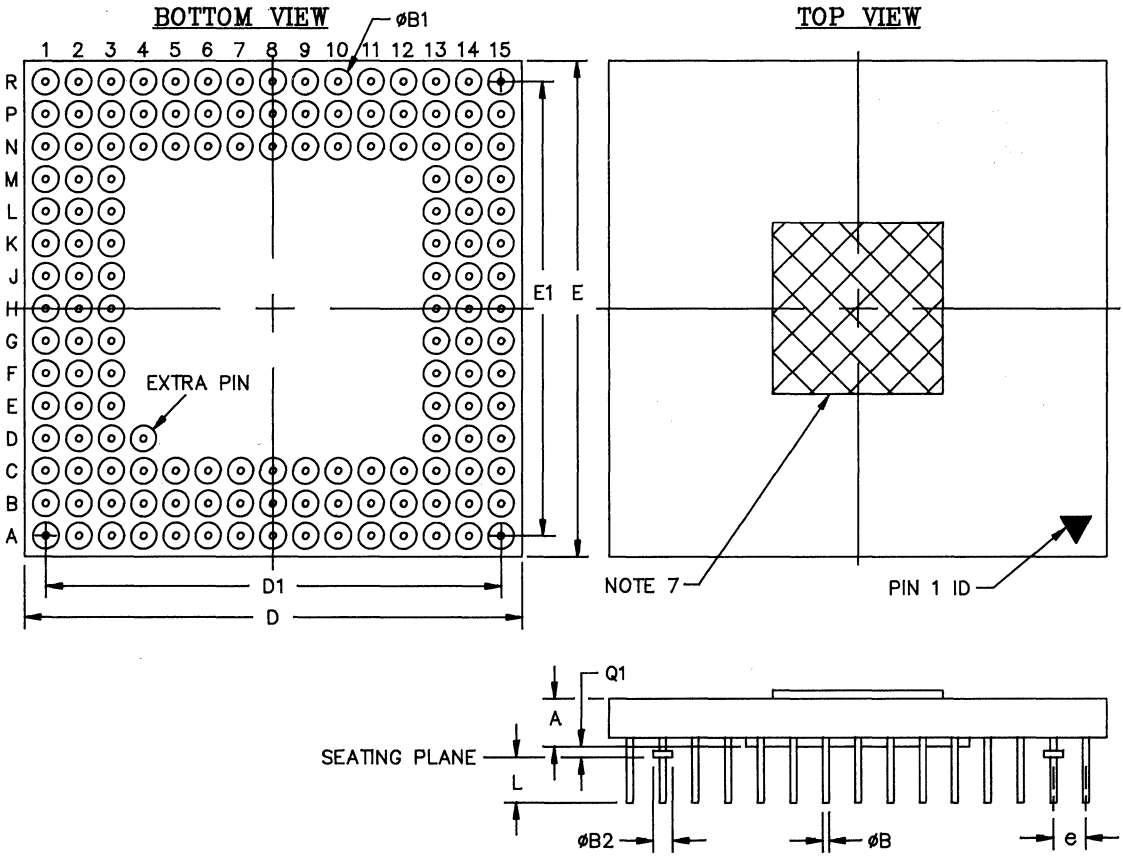


DWG #	G144-1	
# OF PINS (N)	144	
SYMBOL	MIN	MAX
A	.082	.100
ØB	.016	.020
ØB1	.060	.080
ØB2	.040	.060
D/E	1.559	1.590
D1/E1	1.400 BSC	
e	.100 BSC	
L	.120	.140
M	15	
Q1	.025	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

144 PIN PGA (CAVITY DOWN – R3000A)

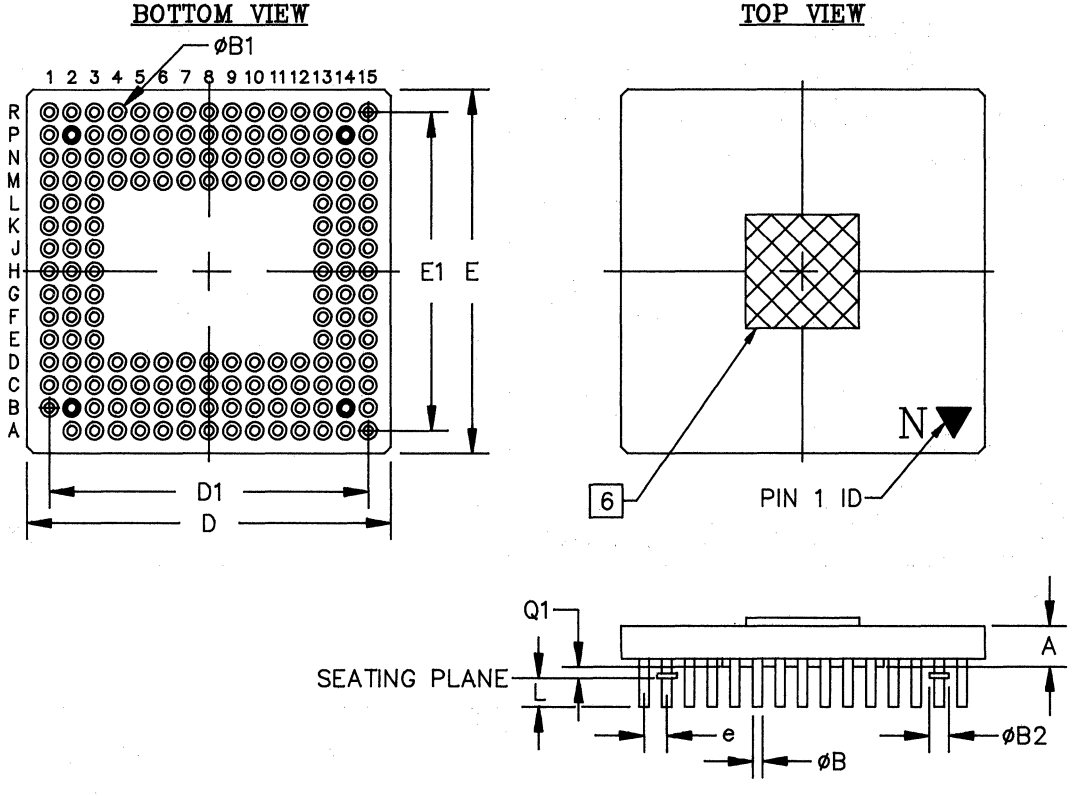


DWG #	G144–3	
# OF PINS (N)	145	
SYMBOL	MIN	MAX
A	.082	.130
ØB	.016	.020
ØB1	.060	.080
ØB2	.040	.060
D/E	1.559	1.590
D1/E1	1.400 BSC	
e	.100 BSC	
L	.120	.140
M	15	
Q1	.025	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.
6. EXTRA PIN (D–4) ELECTRICALLY CONNECTED TO D–3.
7. CROSS HATCHED AREA INDICATES INTEGRAL METALLIC HEAT SINK.

PIN GRID ARRAYS (Continued)

161 PIN PGA (CAVITY DOWN)



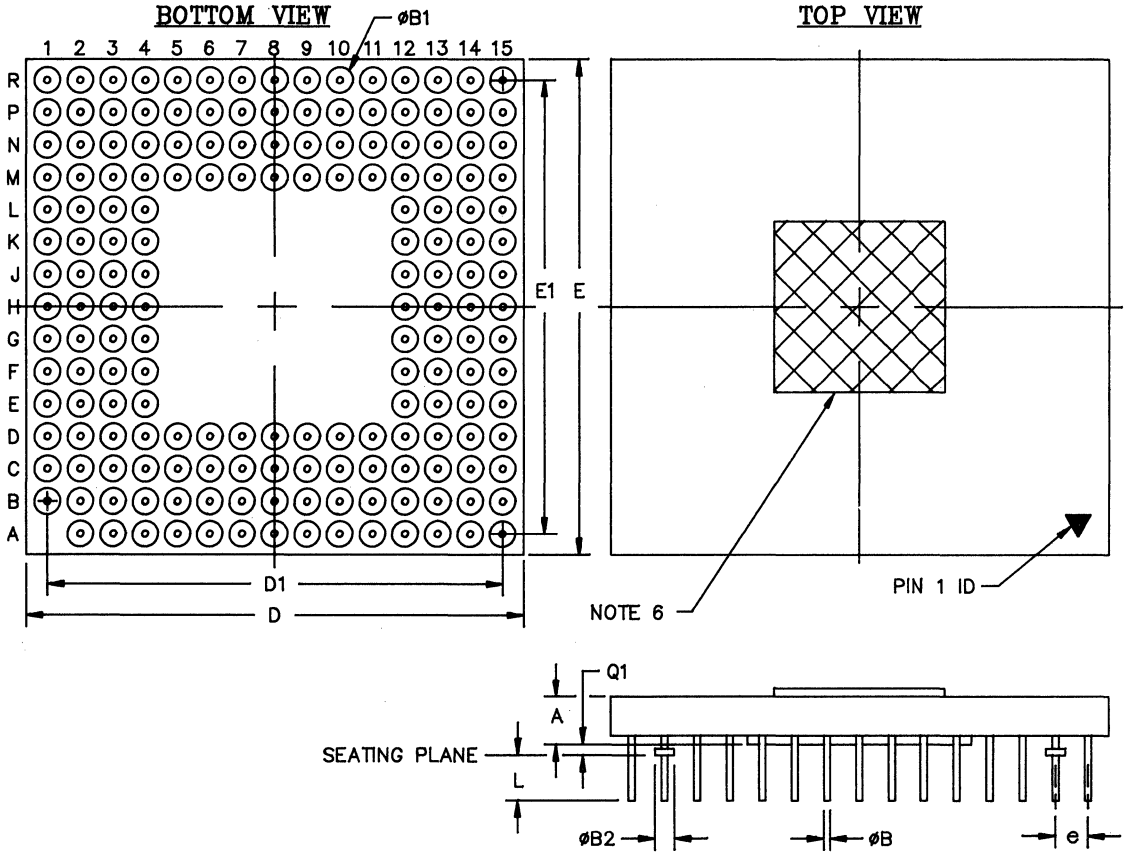
DWG #	G161-1	
# OF PINS (N)	161	
SYMBOL	MIN	MAX
A	.082	.145
øB	.016	.020
øB1	.060	.080
øB2	.040	.060
D/E	1.559	1.590
D1/E1	1.400 BSC	
e	.100 BSC	
L	.120	.140
M	15	
Q1	.025	.060

NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL DIMENSIONS ARE IN INCHES.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS.
5. CHAMFERRED CORNERS ARE IDT'S OPTION.

[6] CROSS HATCHED AREA INDICATES INTEGRAL METALLIC HEAT SINK..

PIN GRID ARRAYS (Continued)

175 PIN PGA (CAVITY DOWN – R3000A)

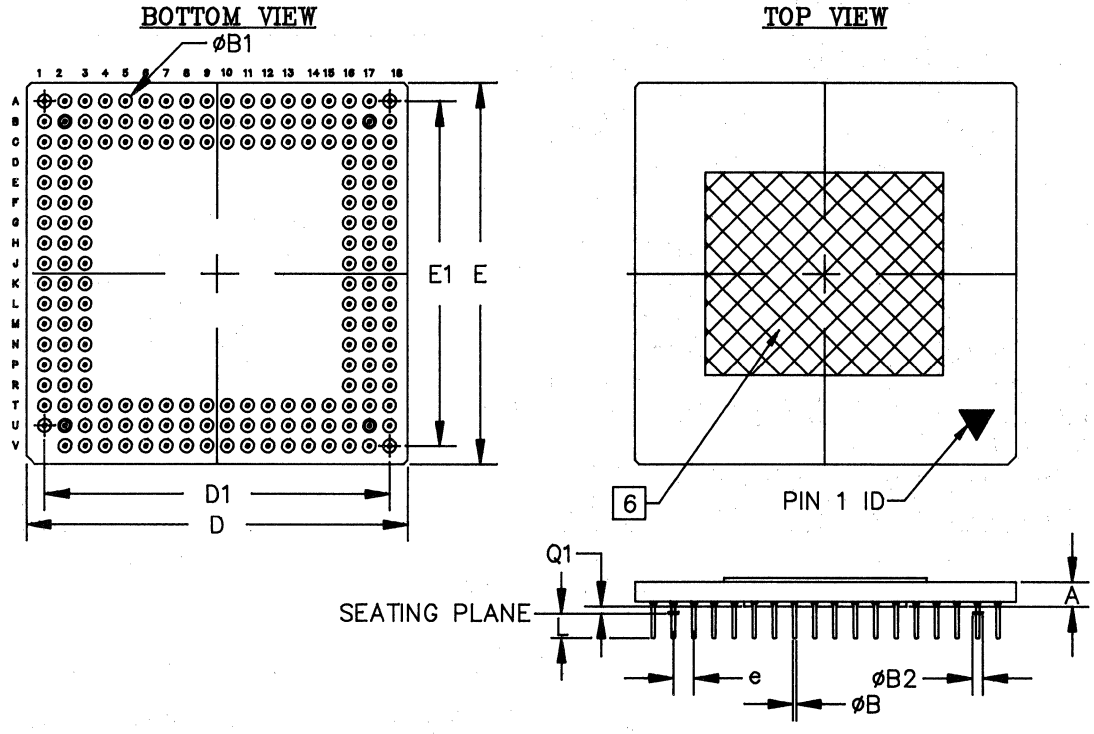


DWG #	G175–1	
# OF PINS (N)	175	
SYMBOL	MIN	MAX
A	.082	.145
ØB	.016	.020
ØB1	.060	.080
ØB2	.040	.060
D/E	1.559	1.590
D1/E1	1.400 BSC	
e	.100 BSC	
L	.120	.140
M	15	
Q1	.025	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.
6. CROSS HATCHED AREA INDICATES INTEGRAL METALLIC HEAT SINK.

PIN GRID ARRAYS (Continued)

179 PIN PGA (CAVITY DOWN)



DWG #	G179-1	
# OF PINS (N)	179	
SYMBOL	MIN	MAX
A	.082	.145
øB	.016	.020
øB1	.060	.080
øB2	.040	.060
D/E	1.840	1.880
D1/E1	1.700 BSC	
e	.100 BSC	
L	.120	.140
M	18	
Q1	.025	.060

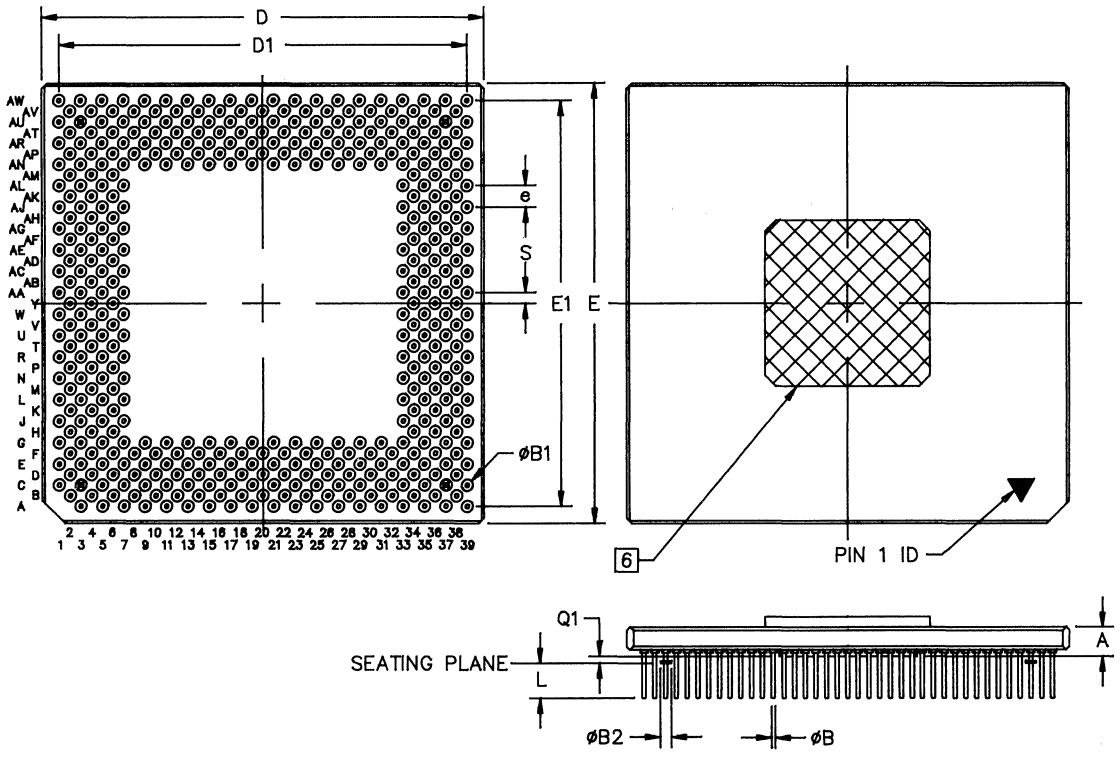
NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL DIMENSIONS ARE IN INCHES.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS.
5. CHAMFERRED CORNERS ARE IDT'S OPTION.
6. CROSS HATCHED AREA INDICATES INTEGRAL METALLIC HEAT SINK..

PIN GRID ARRAYS (Continued)

447 PIN PGA (CAVITY DOWN)

BOTTOM VIEW

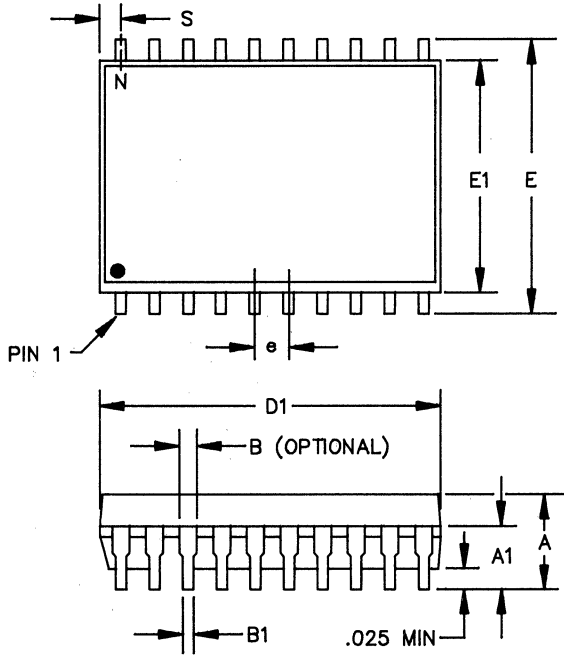
TOP VIEW



DWG #	G447-1	
# OF PINS (N)	447	
SYMBOL	MIN	MAX
A	.070	.145
øB	.016	.020
øB1	.050	.060
øB2	.045	.055
D/E	2.040	2.080
D1/E1	1.900 BSC	
e	.100 BSC	
L	.120	.140
M	39	
Q1	.025	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS.
5. CHAMFERRED CORNERS ARE IDT'S OPTION.
6. CROSS HATCHED AREA INDICATES INTEGRAL METALLIC HEAT SINK..

SMALL OUTLINE IC

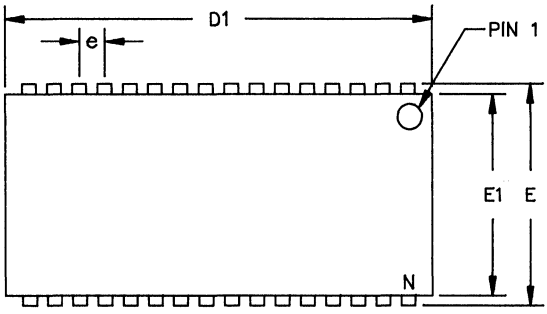


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D1 & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSION AND TO BE MEASURED FROM THE BOTTOM OF THE PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE

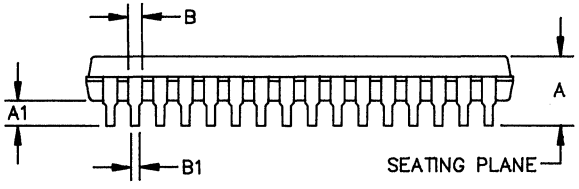
20–32 LEAD SMALL OUTLINE (J–BEND, 300 MIL)

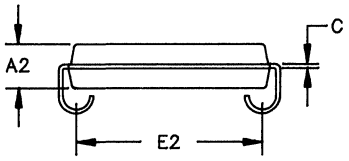
DWG #	SO20–1		SO24–4		SO24–8		SO28–5		SO32–2	
# OF LDS (N)	20		24		24		28		32	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.120	.140	.130	.148	.120	.140	.120	.140	.130	.148
A1	.078	.095	.082	.095	.078	.091	.078	.095	.082	.095
B	–	–	.026	.032	–	–	–	–	.026	.032
B1	.014	.020	.015	.020	.014	.019	.014	.020	.016	.020
C	.008	.013	.007	.011	.0091	.0125	.008	.013	.008	.013
D1	.500	.512	.620	.630	.602	.612	.700	.712	.820	.830
E	.335	.347	.335	.345	.335	.347	.335	.347	.330	.340
E1	.292	.300	.295	.305	.292	.299	.292	.300	.295	.305
E2	.262	.272	.260	.280	.262	.272	.262	.272	.260	.275
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
h	.010	.020	.010	.020	.010	.016	.012	.020	.012	.020
S	.023	.035	.032	.043	.032	.043	.023	.035	.032	.043

SMALL OUTLINE IC (Continued)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D1 & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSION AND TO BE MEASURED FROM THE BOTTOM OF THE PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.



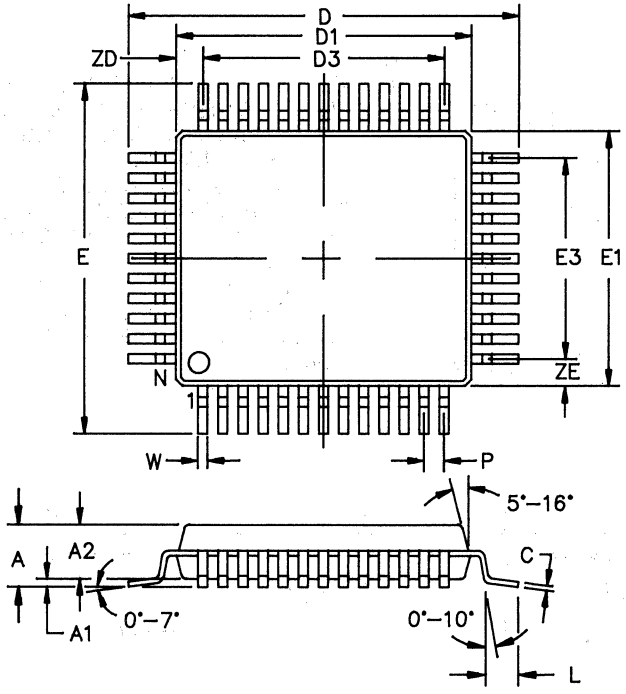


28–32 LEAD SMALL OUTLINE (J–BEND, 400 MIL)

DWG #	SO28–6		SO32–3	
# OF LDS (N)	28		32	
SYMBOLS	MIN	MAX	MIN	MAX
A	.131	.145	.131	.145
A1	.045	.055	.045	.055
A2	.086	.090	.086	.090
B	.026	.032	.026	.032
B1	.015	.020	.015	.020
C	.007	.0125	.007	.0125
D1	.720	.730	.820	.830
E	.435	.445	.435	.445
E1	.395	.405	.395	.405
E2	.360	.380	.360	.380
e	.050 BSC		.050 BSC	
S	.032	.043	.032	.043

PLASTIC QUAD FLATPACKS

80 & 100 LEAD RECTANGULAR PLASTIC QUAD FLATPACK (EIAJ)

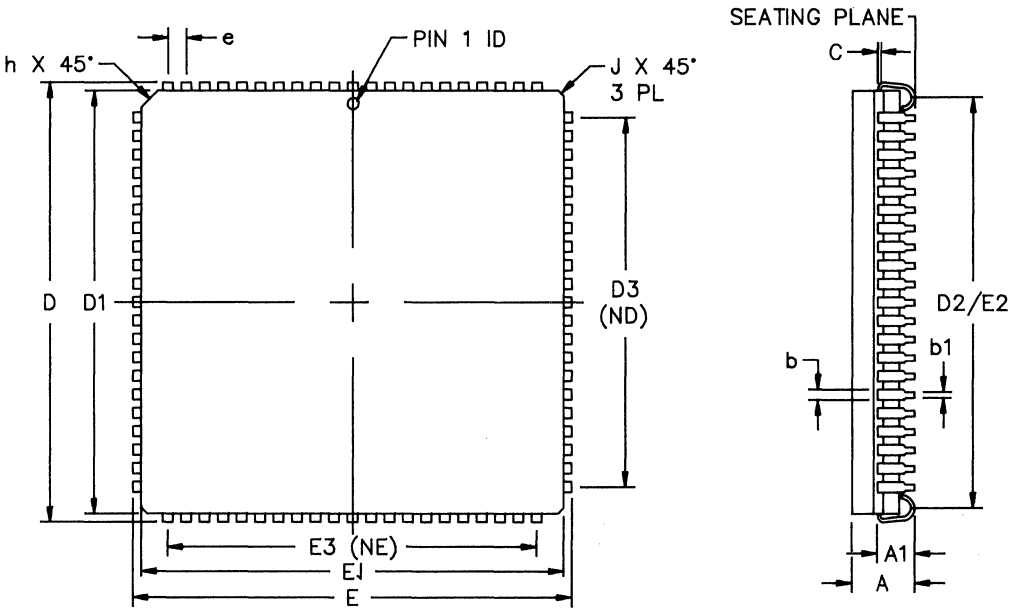


DWG #	PQ80–2		PQ100–2	
# OF LDS (N)	80		100	
SYMBOLS	MIN	MAX	MIN	MAX
A	2.80	3.40	2.80	3.40
A1	.25	–	.25	–
A2	2.54	3.05	2.54	3.05
C	.13	.20	.13	.20
D	23.65	24.15	23.65	24.15
D1	19.90	20.10	19.90	20.10
D3	18.40 REF		18.85 REF	
E	17.65	18.15	17.65	18.15
E1	13.90	14.10	13.90	14.10
E3	12.00 REF		12.35 REF	
L	.65	.95	.65	.95
ND/NE	16/24		20/30	
P	.80 BSC		.65 BSC	
W	.30	.45	.25	.40
ZD	.80		.575	
ZE	1.00		.825	

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D1 & E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .254 PER SIDE.
4. ND & NE REPRESENT NUMBERS OF LEADS IN D & E DIRECTIONS RESPECTIVELY.

MQUADS®

84 LEAD MQUAD (J–BEND, CAVITY DOWN)



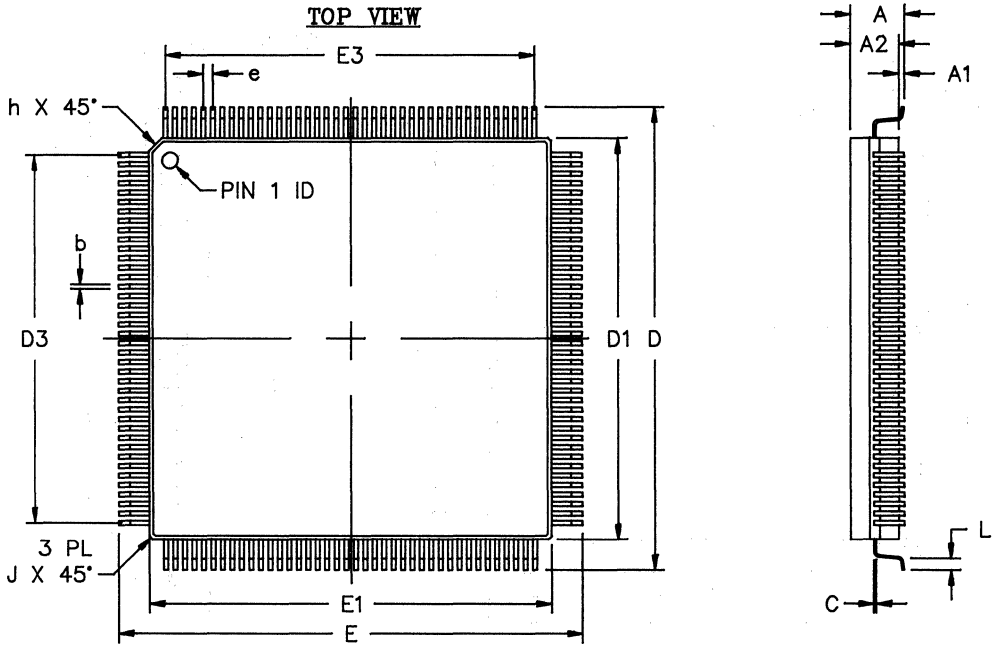
DWG #	M84–1	
# OF LDS (N)	84	
SYMBOL	MIN	MAX
A	.165	.180
A1	.094	.114
b	.026	.032
b1	.013	.021
C	.008	.012
D/E	1.185	1.195
D1/E1	1.140	1.150
D2/E2	1.090	1.130
D3/.E3	1.000 BSC	
e	.050 BSC	
h	.045 REF	
J	.015 REF	
ND/NE	21	

NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.
4. D1 & E1 SHOULD BE MEASURED FROM THE BOTTOM OF THE PACKAGE.
5. ND & NE REPRESENT NUMBER OF LEADS IN D & E DIRECTIONS RESPECTIVELY.

MQUADS ® (Continued)

160 LEAD MQUAD (CAVITY DOWN)



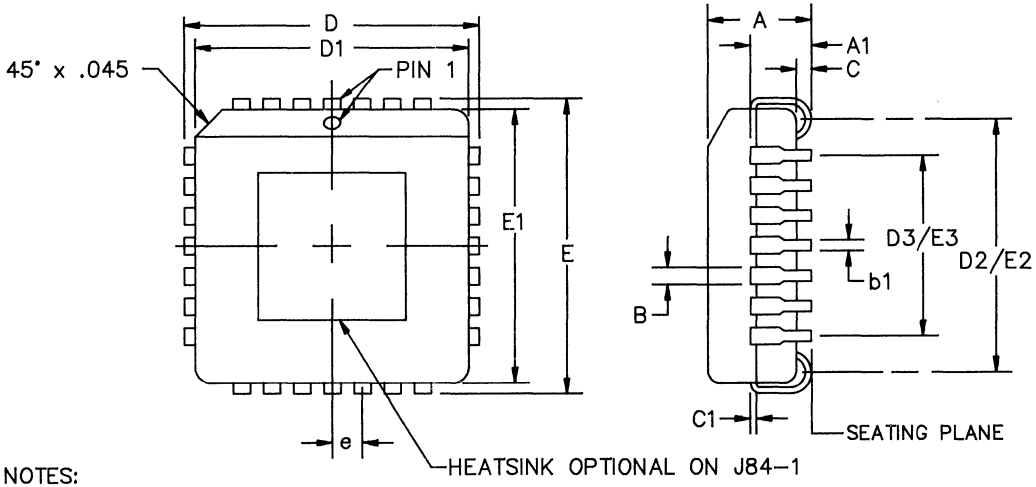
DWG #	M160-1	
# OF LDS (N)	160	
SYMBOL	MIN	MAX
A	3.50	3.86
A1	.25	.51
A2	3.17	3.43
b	.22	.35
C	.13	.20
D/E	31.70	32.10
D1/E1	27.56	27.72
D3/.E3	25.35 BSC	
e	.65 BSC	
h	.89 REF	
J	.20 REF	
L	.67	.93
ND/NE	40	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D1 & E1 SHOULD BE MEASURED FORM THE BOTTOM OF THE PACKAGE.
4. ND & NE REPRESENT NUMBER OF LEADS IN D & E DIRECTIONS RESPECTIVELY.

PLASTIC LEADED CHIP CARRIERS

20–84 LEAD PLCC (SQUARE)



NOTES:

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2. BSC – BASIC LEAD SPACING BETWEEN CENTERS
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.
5. ND & NE REPRESENT NUMBER OF LEADS IN D & E DIRECTIONS RESPECTIVELY.
6. D1 & E1 SHOULD BE MEASURED FROM THE BOTTOM OF THE PKG.

DWG #	J20–1		J28–1		J44–1		J52–1		J68–1		J84–1	
# OF LDS	20		28		44		52		68		84	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.165	.180	.165	.180	.165	.180	.165	.180	.165	.180	.165	.180
A1	.095	.115	.095	.115	.095	.115	.095	.115	.095	.115	.095	.115
B	.026	.032	.026	.032	.026	.032	.026	.032	.026	.032	.026	.032
b1	.013	.021	.013	.021	.013	.021	.013	.021	.013	.021	.013	.021
C	.020	.040	.020	.040	.020	.040	.020	.040	.020	.040	.020	.040
C1	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012
D	.385	.395	.485	.495	.685	.695	.785	.795	.985	.995	1.185	1.195
D1	.350	.356	.450	.456	.650	.656	.750	.756	.950	.956	1.150	1.156
D2/E2	.290	.330	.390	.430	.590	.630	.690	.730	.890	.930	1.090	1.130
D3/E3	.200 REF		.300 REF		.500 REF		.600 REF		.800 REF		1.000 REF	
E	.385	.395	.485	.495	.685	.695	.785	.795	.985	.995	1.185	1.195
E1	.350	.356	.450	.456	.650	.656	.750	.756	.950	.956	1.150	1.156
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
ND/NE	5		7		11		13		17		21	

IDT RISC PROCESSING COMPONENTS

THE COMPLETE RISC SOLUTION

Integrated Device Technology, Inc. is dedicated to providing complete RISC design solutions by combining expertise in silicon processes with leadership products in development systems and software. Long an industry leader in the fastest static RAMs and high-speed logic, IDT now offers RISC system building blocks comprised of components and board-level subsystems.

As a semiconductor partner with MIPS Computer Systems, IDT has established a leadership position in the RISC marketplace by supplying the fastest CPUs at 40MHz, pioneering RISC CPU Subsystem™ modules, and offering cost-effective development tools and software.

The MIPS architecture has become an industry standard and has been adopted by over 100 leading OEM manufacturers including DEC, Sony, Tandem, NEC, CDC, Adobe, Siemens, Nixdorf, Honeywell Bull and Silicon Graphics. The MIPS ISA (Instruction Set Architecture) has been selected by JIAWG as the 32-bit microprocessor standard for military avionics.

RISComponent™ FAMILY OVERVIEW

The R3000 Family consists of the R3000 RISC CPU, the R3001, R3041, R3051/52, and R3081 RISControllers™, the R3010A Floating-Point Accelerator, the R3500 RISCore™ and the R3020 Write Buffer. The R3000 processor is a derivative of the R2000A, the first commercially-available RISC processor introduced in 1985. The R3001 RISController and the R3051 family, including the R3041 and R3081, are versions of the processor tailored for embedded control and low-cost workstations. The R3500 integrates floating-point capability onto the R3000 pinout. The R4000 is the third generation of the MIPS RISC architecture that sets a new performance standard for the 1990s.

THE IDT79R3000 CPU

The R3000 processor consists of two tightly-coupled processors implemented on a single chip.

The first processor is a full 32-bit Harvard Architecture CPU consisting of 32 registers, an integer ALU, a single-cycle shifter, and a multiplier/divider. The second processor is a system control coprocessor containing a Translation Lookaside Buffer (TLB) and control registers to support a virtual memory space of 4GB and separate instruction and Data caches.

The R3000 CPU features:

- Full 32-bit operation
- Three instruction formats
- Efficient 5-stage pipeline
- On-chip cache control
- On-chip Memory Management Unit
- Multiprocessor capability

5

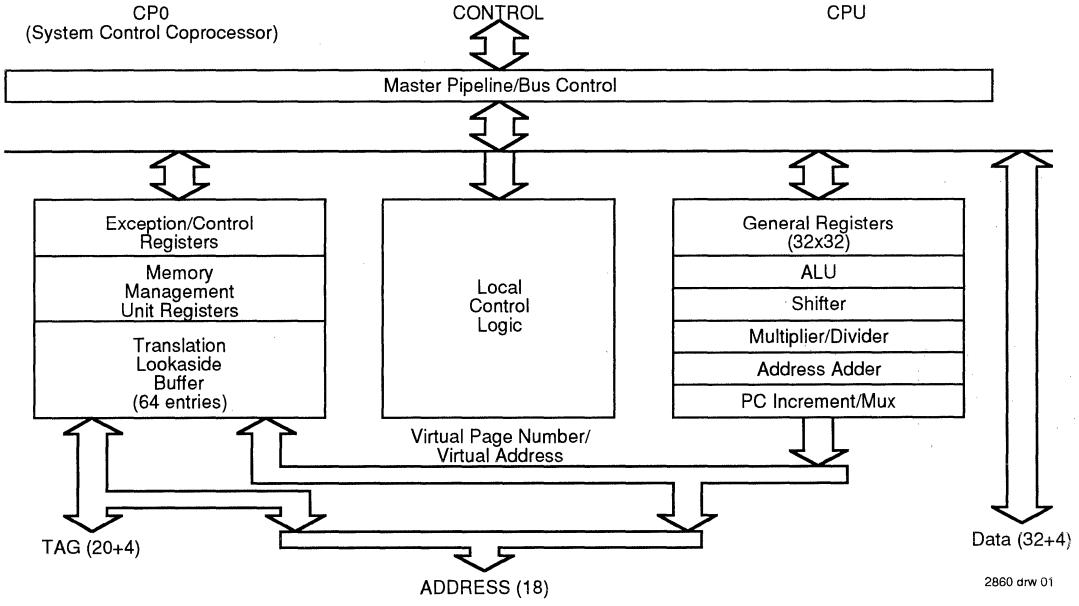

Figure 1. IDT79R3000 Processor

THE IDT79R3010A FLOATING-POINT ACCELERATOR

The R3010A Floating-Point Accelerator (FPA) supports full conformance with the IEEE 754 floating-point specification. It acts as a coprocessor to the R3000 CPU, providing a seamless integration of fixed and floating-point instructions. All floating-point operations are transparent to the programmer.

The R3010A FPA features:

- Full 64-bit operation
- Single-cycle load/store instructions
- Seamless interface to the R3000 or R3001 CPU
- Three operation units (add/subtract, multiply and divide) can operate in parallel
- Six-level pipeline

THE IDT79R3001 RISController™

The R3001 RISController optimizes the high-performance MIPS architecture for embedded control systems. Capable of 28 MIPS performance at 33MHz, the R3001 incorporates new features for real-time control. The controller extends the performance range of the current R3000 processor, saves valuable real estate for space-critical designs and lowers system memory costs.

The MIPS performance range is extended by the increase in the R3000 in the synchronous memory space from 512KB, maximum, to a full 32MB. This allows the system to perform with a guaranteed "cache" hit rate of 100%. The on-chip memory controller allows the designer to use standard SRAMs, DRAMs, or even VRAMs, representing a significant cost savings over other solutions. The processor supports predictable interrupt response times for real-time control applications, and system chip count is lowered by substantially reducing the number of devices needed to implement local memory.

THE R3051 FAMILY OF RISControllers™

The IDT79R3051 Family is a derivative of the R3000, featuring a high level of integration and targeted to high-performance but cost-sensitive embedded processing applications. The R3051 family is designed to bring the high-performance inherent in the MIPS RISC architecture into low-cost, simplified, power-sensitive applications.

Functional units were integrated onto the CPU core in order to reduce the total system cost rather than to increase the inherent performance of the integer engine. Thus, the R3051 family is able to offer 35 MIPS of integer performance at 40MHz without requiring external SRAM or caches.

The R3041 extends the range of price/performance achievable with the R3051 family, by dramatically lowering the cost of using the MIPS architecture. The R3041 has been designed to achieve minimal system and components cost, yet maintain the high performance inherent in the MIPS architecture. The R3041 also maintains pin and software compatibility with the R3051 and R3081.

The R3081 extends the capabilities of the R3051 family by integrating the additional resources into the same pinout. The R3081 thus extends the range of applications addressed by the R3051 family and allows designers to implement a single, base system and software set capable of accepting a wide variety of CPUs according to the price/performance goals of the end system.

THE R3500 RISCore™ CPU/FPA

The R3500 is a single chip that integrates the R3000A CPU and the R3010A FPA execution units using the R3000A packaging and pinout. This high-integration device is completely binary software, compatible with the R3000, R2000 CPUs and R3010A FPA to facilitate the migration path to higher performance and lower chip count systems that utilize both the CPU and the floating point units.

IDT has also made several enhancements to the R3000 architecture such as faster multiply and divide instructions and added a programmable tag bus width allowing reduced cache cost. The power consumption is lower by 33% when compared to the standard R3000 and R3010A.

THE IDT79R4000 CPU

The R4000 is the third generation of MIPS RISC technology and establishes a new performance standard for RISC processors for the 1990s. The R4000 extends the performance range served by the MIPS architecture and, thereby, provides a migration path to applications served by the R3000, R3001, and the R3051.

This third generation processor maintains full binary compatibility with applications executing on the R2000/R3000 and IDT's RISController family, while achieving substantially higher performance. The key to this performance is both the architecture/implementation of the processor and the high level of integration achieved in a single chip. The R4000 contains the RISC integer unit, floating-point unit, MMU, 8K of I- and D-cache, along with multiprocessing support such as direct control of optional secondary caches. To achieve performance levels capable of over 50 VAX MIPS sustained performance, the R4000 utilizes technology such as super-pipelining to exploit 2-level instruction parallelism with no issue restrictions. The R4000 presents a balanced architectural approach to achieve a wide range of price/performance goals.

TABLE OF CONTENTS

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Integrated Device Technology, Inc.

RISC CPU PROCESSOR

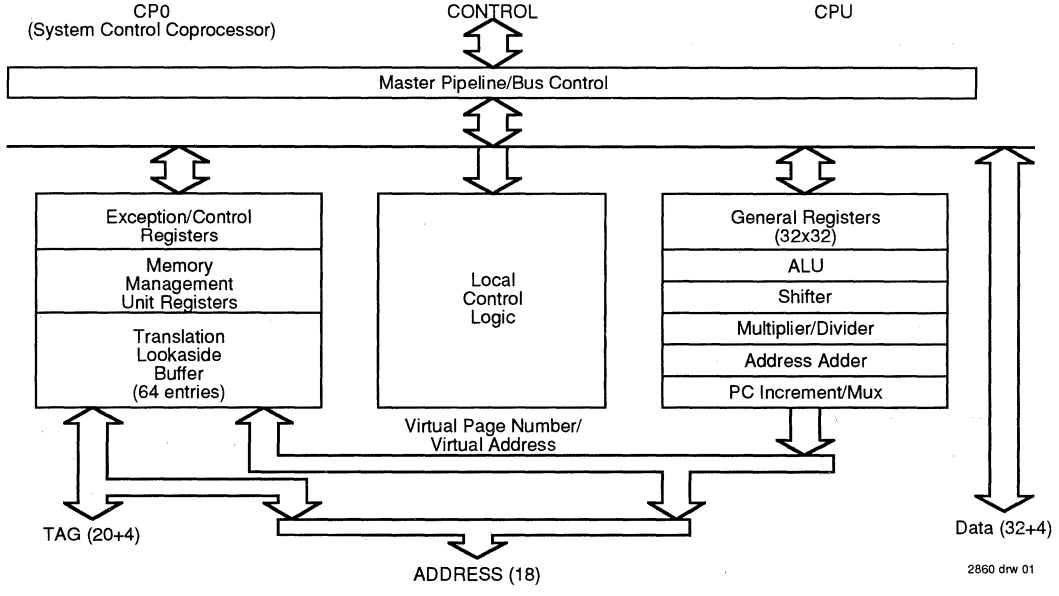
IDT79R3000A
IDT79R3000AE

FEATURES:

- Enhanced instruction set compatible version of the IDT79R2000, IDT79R3000 RISC CPUs.
- Upwardly pin-compatible with IDT79R3000 RISC CPU.
- IDT79R3000A "E" version relaxes system memory timing requirements in a high-speed systems.
- Full 32-bit Operation—Thirty-two 32-bit registers and all instructions and addresses are 32-bit.
- Efficient Pipelining—The CPU's 5-stage pipeline design assists in obtaining an execution rate approaching one instruction per cycle. Pipeline stalls and exceptions are handled precisely and efficiently.
- On-Chip Cache Control—The IDT79R3000A provides a high-bandwidth memory interface that handles separate external Instruction and Data Caches ranging in size from 4 to 256kB each. Both caches are accessed during a single CPU cycle. All cache control is on-chip.
- On-Chip Memory Management Unit—A fully-associative, 64-entry Translation Look-aside Buffer (TLB) provides fast address translation for virtual-to-physical memory mapping of the 4gB virtual address space.
- Dynamically able to switch between Big- and Little-Endian byte ordering conventions.
- Coprocessor Interface—The IDT79R3000A generates all addresses and handles memory interface control for up to three additional tightly coupled external processors.
- Optimizing Compilers are available for C, Fortran, Pascal, COBOL, Ada, PL/1, and C++.
- UNIX™ System V.4 and BSD 4.3 operating systems supported.
- High-speed CMOS technology.
- 16.7 through 40MHz clock rates yield up to 32VUPS sustained throughput.
- Supports independent multi-word block refill of both the instruction and data caches with variable block sizes.
- Supports concurrent refill and execution of instructions.
- Partial word stores executed as read-modify-write operations.
- 6 external interrupt inputs, 2 software interrupts, with single cycle latency to exception handler routine.
- Flexible multiprocessing support on chip with no impact on uniprocessor designs.

5

IDT79R3000A PROCESSOR BLOCK DIAGRAM



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UNIX is a Trademark of AT&T

DESCRIPTION

The IDT79R3000A RISC Microprocessor consists of two tightly-coupled processors integrated on a single chip. The first processor is a full 32-bit CPU based on RISC (Reduced Instruction Set Computer) principles to achieve a new standard of microprocessor performance. The second processor is a system control coprocessor, called CP0, containing a fully-associative 64-entry TLB (Translation Look-aside Buffer), MMU (Memory Management Unit) and control registers, supporting a 4gB virtual memory subsystem, and a Harvard Architecture Cache Controller achieving a bandwidth of 320mB/second using industry standard static RAMs.

This data sheet provides an overview of the features and architecture of the IDT79R3000A CPU, Revision 3.0. A more detailed description of the operation of the device is incorporated in the *IDT79R3000A Family Hardware User Manual*, and a more detailed architectural overview is provided in the *MIPS RISC Architecture* book, both available from IDT. Documentation providing details of the software and development environments supporting this processor are also available from IDT.

IDT79R3000A CPU Registers

The IDT79R3000A CPU provides 32 general-purpose 32-bit registers, a 32-bit Program Counter, and two 32-bit registers that hold the results of integer multiply and divide operations. Only two of the 32 general registers have a special purpose: register r0 is hard-wired to the value "0", which is a useful constant, and register r31 is used as the link register in jump-and-link instructions (return address for subroutine calls).

The CPU registers are shown in Figure 2. Note that there is no Program Status Word (PSW) register shown in this figure: the functions traditionally provided by a PSW register are instead provided in the Status and Cause registers incorporated within the System Control Coprocessor (CP0).

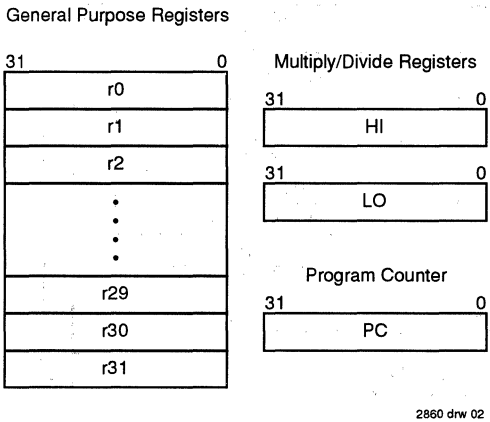


Figure 2. IDT79R3000A CPU Registers

Instruction Set Overview

All IDT79R3000A instructions are 32 bits long, and there are only three instruction formats. This approach simplifies instruction decoding, thus minimizing instruction execution time. The IDT79R3000A processor initiates a new instruction on every run cycle, and is able to complete an instruction on almost every clock cycle. The only exceptions are the Load instructions and Branch instructions, which each have a single cycle of latency associated with their execution. Note, however, that in the majority of cases the compilers are able to fill these latency cycles with useful instructions which do not require the result of the previous instruction. This effectively eliminates these latency effects.

The actual instruction set of the CPU was determined after extensive simulations to determine which instructions should be implemented in hardware, and which operations are best synthesized in software from other basic instructions. This methodology resulted in the IDT79R3000A having the highest performance of any available microprocessor.

The IDT79R3000A instruction set can be divided into the following groups:

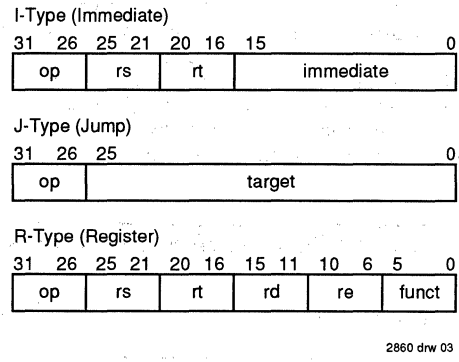


Figure 3. IDT79R3000A Instruction Formats

- **Load/Store** instructions move data between memory and general registers. They are all I-type instructions, since the only addressing mode supported is base register plus 16-bit, signed immediate offset.
  The Load instruction has a single cycle of latency, which means that the data being loaded is not available to the instruction immediately after the load instruction. The compiler will fill this delay slot with either an instruction which is not dependent on the loaded data, or with a NOP instruction. There is no latency associated with the store instruction.
  Loads and Stores can be performed on byte, half-word, word, or unaligned word data (32-bit data not aligned on a modulo-4 address). The CPU cache is constructed as a write-through cache.
- **Computational** instructions perform arithmetic, logical and shift operations on values in registers. They occur in both R-type (both operands and the result are registers) and I-type (one operand is a 16-bit immediate) formats.

Note that computational instructions are three operand instructions; that is, the result of the operation can be stored into a different register than either of the two operands. This means that operands need not be overwritten by arithmetic operations. This results in a more efficient use of the large register set.

- **Jump and Branch** instructions change the control flow of a program. Jumps are always to a paged absolute address formed by combining a 26-bit target with four bits of the Program counter (J-type format, for subroutine calls), or 32-bit register byte addresses (R-type, for returns and dispatches). Branches have 16-bit offsets relative to the program counter (I-type). Jump and Link instructions save a return address in Register 31. The IDT79R3000A instruction set features a number of branch conditions. Included is the ability to compare a register to zero and branch, and also the ability to branch based on a comparison between two registers. Thus, net performance is increased since software does not have to perform arithmetic instructions prior to the branch to set up the branch conditions.
- **Coprocessor** instructions perform operations in the coprocessors. Coprocessor Loads and Stores are I-type. Coprocessor computational instructions have coprocessor-dependent formats (see coprocessor manuals).
- **Coprocessor 0** instructions perform operations on the System Control Coprocessor (CP0) registers to manipulate the memory management and exception handling facilities of the processor.
- **Special** instructions perform a variety of tasks, including movement of data between special and general registers, system calls, and breakpoint. They are always R-type.

Table 1 lists the instruction set of the IDT79R3000A processor.

5

IDT79R3000A INSTRUCTION SUMMARY

OP	Description	OP	Description
	Load/Store Instructions		**Multiply/Divide Instructions**
LB	Load Byte	MULT	Multiply
LBU	Load Byte Unsigned	MULTU	Multiply Unsigned
LH	Load Halfword	DIV	Divide
LHU	Load Halfword Unsigned	DIVU	Divide Unsigned
LW	Load Word	MFHI	Move From HI
LWL	Load Word Left	MTHI	Move To HI
LWR	Load Word Right	MFLO	Move From LO
SB	Store Byte	MTLO	Move To LO
SH	Store Halfword		
SW	Store Word		**Jump and Branch Instructions**
SWL	Store Word Left	J	Jump
SWR	Store Word Right	JAL	Jump and Link
		JR	Jump to Register
	Arithmetic Instructions	JALR	Jump and Link Register
	(ALU Immediate)	BEQ	Branch on Equal
ADDI	Add Immediate	BNE	Branch on Not Equal
ADDIU	Add Immediate Unsigned	BLEZ	Branch on Less than or Equal to Zero
SLTI	Set on Less Than Immediate	BGTZ	Branch on Greater Than Zero
SLTIU	Set on Less Than Immediate Unsigned	BLTZ	Branch on Less Than Zero
		BGEZ	Branch on Greater than or Equal to Zero
ANDI	AND Immediate		
ORI	OR Immediate	BLTZAL	Branch on Less Than Zero and Link
XORI	Exclusive OR Immediate	BGEZAL	Branch on Greater than or Equal to Zero and Link
LUI	Load Upper Immediate		
			Special Instructions
	Arithmetic Instructions	SYSCALL	System Call
	(3-operand, register-type)	BREAK	Break
ADD	Add		
ADDU	Add Unsigned		**Coprocessor Instructions**
SUB	Subtract	LWCz	Load Word from Coprocessor
SUBU	Subtract Unsigned	SWCz	Store Word to Coprocessor
SLT	Set on Less Than	MTCz	Move To Coprocessor
		MFCz	Move From Coprocessor
SLTU	Set on Less Than Unsigned	CTCz	Move Control to Coprocessor
AND	AND	CFCz	Move Control From Coprocessor
OR	OR	COPz	Coprocessor Operation
XOR	Exclusive OR	BCzT	Branch on Coprocessor z True
NOR	NOR	BCzF	Branch on Coprocessor z False
	Shift Instructions		**System Control Coprocessor**
SLL	Shift Left Logical		**(CP0) Instructions**
SRL	Shift Right Logical	MTC0	Move To CP_0
SRA	Shift Right Arithmetic	MFC0	Move From CP_0
SLLV	Shift Left Logical Variable	TLBR	Read indexed TLB entry
SRLV	Shift Right Logical Variable	TLBWI	Write Indexed TLB entry
SRAV	Shift Right Arithmetic Variable	TLBWR	Write Random TLB entry
		TLBP	Probe TLB for matching entry
		RFE	Restore From Exception

2860 tbl 01

IDT79R3000A System Control Coprocessor (CP0)

The IDT79R3000A can operate with up to four tightly-coupled coprocessors (designated CP0 through CP3). The System Control Coprocessor (or CP0), is incorporated on the IDT79R3000 chip and supports the virtual memory system and exception handling functions of the IDT79R3000A. The virtual memory system is implemented using a Translation Look-aside Buffer and a group of programmable registers as shown in Figure 4.

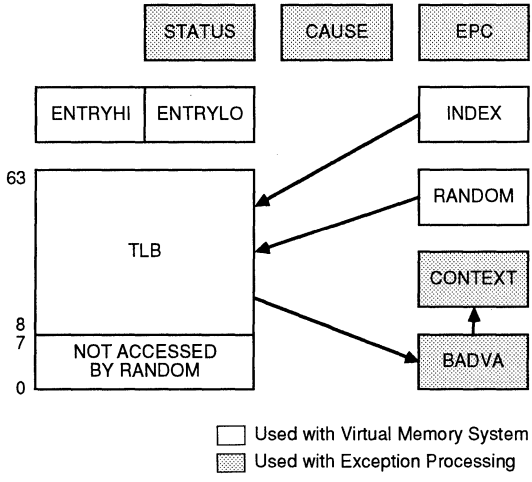
SYSTEM CONTROL COPROCESSOR (CP0) REGISTERS

The CP0 registers shown in Figure 4 are used to control the memory management and exception handling capabilities of the IDT79R3000A. Table 2 provides a brief description of each register.

SYSTEM CONTROL COPROCESSOR (CP0) REGISTERS

Register	Description
EntryHi	HIGH half of a TLB entry
EntryLo	LOW half of a TLB entry
Index	Programmable pointer into TLB array
Random	Pseudo-random pointer into TLB array
Status	Mode, interrupt enables, and diagnostic status info
Cause	Indicates nature of last exception
EPC	Exception Program Counter
Context	Pointer into kernel's virtual Page Table Entry array
BadVA	Most recent bad virtual address
PRId	Processor revision identification (Read only)

2860 tbl 02



2860 drw 04

Figure 4. The System Coprocessor Registers

Memory Management System

The IDT79R3000A has an addressing range of 4gB. However, since most IDT79R3000A systems implement a physical memory smaller than 4gB, the IDT79R3000A provides for the logical expansion of memory space by translating addresses composed in a large virtual address space into available physical memory address. The 4gB address space is divided into 2gB which can be accessed by both the users and the kernel, and 2gB for the kernel only.

The TLB (Translation Lookaside Buffer)

Virtual memory mapping is assisted by the Translation Lookaside Buffer (TLB). The on-chip TLB provides very fast virtual memory access and is well-matched to the requirements of multi-tasking operating systems. The fully-associative TLB contains 64 entries, each of which maps a 4kB page, with controls for read/write access, cacheability, and process identification. The TLB allows each user to access up to 2gB of virtual address space.

Figure 5 illustrates the format of each TLB entry. The Translation operation involves matching the current Process ID (PID) and upper 20 bits of the address against PID and VPN (Virtual Page Number) fields in the TLB. When both match (or the TLB entry is Global), the VPN is replaced with the PFN (Physical Frame Number) to form the physical address.

TLB misses are handled in software, with the entry to be replaced determined by as imple RANDOM function. The routine to process a TLB miss in the UNIX environment requires only 10-12 cycles, which compares favorably with many CPUs which perform the operation in hardware.

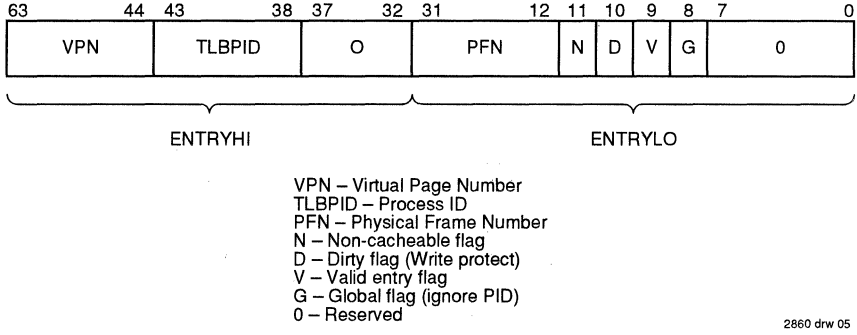


Figure 5. TLB Entry Format

IDT79R3000 Operating Modes

The IDT79R3000A has two operating modes: User mode and Kernel/mode. The IDT79R3000A normally operates in the User mode until an exception is detected forcing it into the Kernel mode. It remains in the Kernel mode until a Restore From Exception (RFE) instruction is executed. The manner in which memory addresses are translated or mapped depends on the operating mode of the IDT79R3000A (Figure 6) shows the MMU translation performed for each of the operating modes.

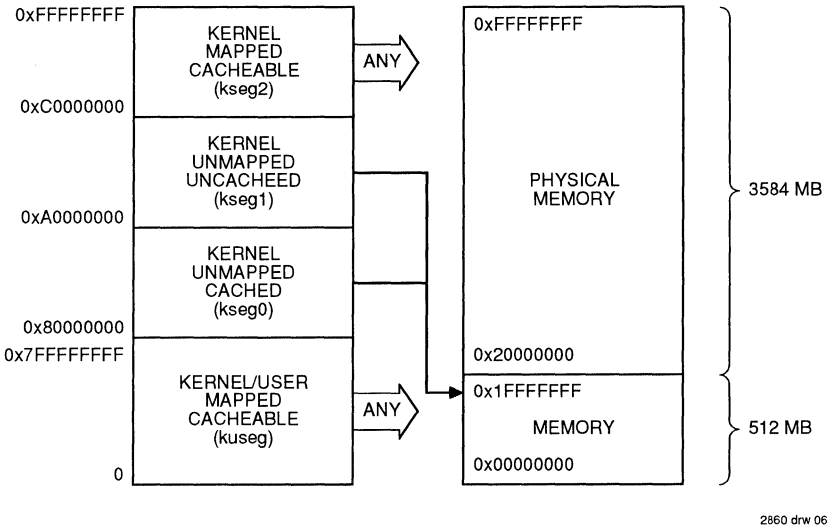


Figure 6. IDT79R3000A Virtual Address Mapping

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User Mode—in this mode, a single, uniform virtual address space (kuseg) of 2gB is available. Each virtual address is extended with a 6-bit process identifier field to form unique virtual addresses. All references to this segment are mapped through the TLB. Use of the cache for up to 64 processes is determined by bit settings for each page within the TLB entries.

Kernel Mode—four separate segments are defined in this mode:

- *kuseg*—when in the kernel mode, references to this segment are treated just like user mode references, thus streamlining kernel access to user data.
- *kseg0*—references to this 512mB segment use cache memory but are not mapped through the TLB. Instead, they always map to the first 0.5gB of physical address space.
- *kseg1*—references to this 512mB segment are not mapped through the TLB and do not use the cache. Instead, they are hard-mapped into the same 0.5gB segment of physical address space as kseg0.
- *kseg2*—references to this 1gB segment are always mapped through the TLB and use of the cache is determined by bit settings within the TLB entries.

IDT79R3000 Pipeline Architecture

The execution of a single IDT79R3000A instruction consists of five primary steps:

1) **IF** — Fetch the instruction (I-Cache).
2) **RD** — Read any required operands from CPU registers while decoding the instruction.
3) **ALU** — Perform the required operation on instruction operands.
4) **MEM**— Access memory (D-Cache).
5) **WB** — Write back results to register file.

Each of these steps requires approximately one CPU cycle, as shown in Figure 7 (parts of some operations overlap into another cycle while other operations require only 1/2 cycle).

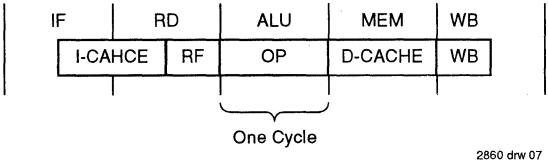


Figure 7. IDT79R3000A Instruction Pipeline

INSTRUCTION EXECUTION

The IDT79R3000A uses a 5-stage pipeline to achieve an instruction execution rate approaching one instruction per CPU cycle. Thus, execution of five instructions at a time are overlapped as shown in Figure 8.

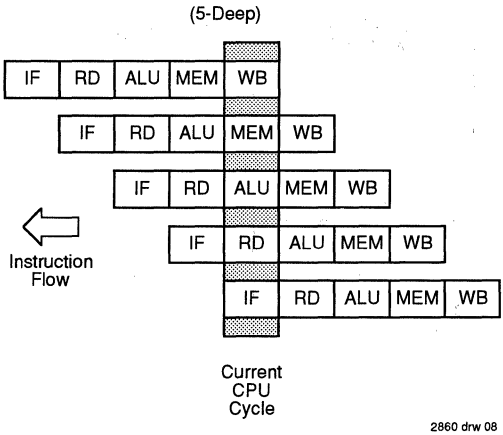


Figure 8. IDT79R3000A Execution Sequence

This pipeline operates efficiently because different CPU resources (address and data bus accesses, ALU operations, register accesses, and so on) are utilized on a non-interfering basis.

Memory System Hierarchy

The high performance capabilities of the IDT79R3000A processor demand system configurations incorporating techniques frequently employed in large, mainframe computers but seldom encountered in systems based on more traditional microprocessors.

A primary goal of systems employing RISC techniques is to minimize the average number of cycles each instruction requires for execution. In order to achieve this goal, RISC processors incorporate a number of RISC techniques, including a compact and uniform instruction set, a deep instruction pipeline (as described above), and utilization of optimizing compilers. Many of the advantages obtained from these techniques can, however, be negated by an inefficient memory system.

Figure 9 illustrates memory in a simple microprocessor system. In this system, the CPU outputs addresses to memory and reads instructions and data from memory or writes data to memory. The address space is completely undifferentiated: instructions, data, and I/O devices are all treated the same. In such a system, a primary limiting performance factor is memory bandwidth.

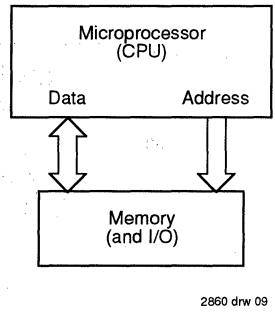


Figure 9. A Simple Microprocessor Memory System

Figure 10 illustrates a memory system that supports the significantly greater memory bandwidth required to take full advantage of the IDT79R3000A's performance capabilities. The key features of this system are:

- **External Cache Memory**—Local, high-speed memory (called cache memory) is used to hold instructions and data that is repetitively accessed by the CPU (for example, within a program loop) and thus reduces the number of references that must be made to the slower-speed main

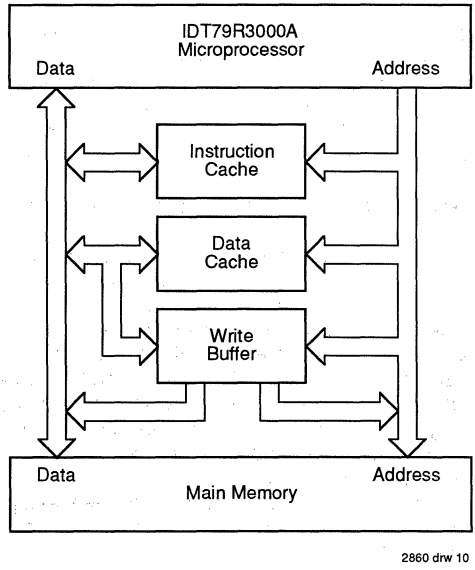


Figure 10. An IDT79R3000A System with a High-Performance Memory System

memory. Some microprocessors provide a limited amount of cache memory on the CPU chip itself. The external caches supported by the IDT79R3000A can be much larger; while a small cache can improve performance of some programs, significant improvements for a wide range of programs require large caches.

- **Separate Caches for data and Instructions**—Even with high-speed caches, memory speed can still be a limiting factor because of the fast cycle time of a high-performance microprocessor. The IDT79R3000A supports separate caches for instructions and data and alternates accesses of the two caches during each CPU cycle. Thus, the processor can obtain data and instructions at the cycle rate of the CPU using caches constructed with commercially available IDT static RAM devices.
  In order to maximize bandwidth in the cache while minimizing the requirement for SRAM access speed, the IDT79R3000A divides a single-processor clock cycle into two phases. During one phase, the address for the data cache access is presented while data previously addressed in the instruction cache is read; during the next phase, the data operation is completed while the instruction cache is being addressed. Thus, both caches are read in a single processor cycle using only one set of address and data pins.

- **Write Buffer**—in order to ensure data consistency, all data that is written to the data cache must also be written out to main memory. The cache write model used by the IDT79R3000A is that of a write-through cache; that is, all data written by the CPU is immediately written into the main memory. To relieve the CPU of this responsibility (and the inherent performance burden) the IDT79R3000A supports an interface to a write buffer. The IDT79R3020 Write Buffer captures data (and associated addresses) output by the CPU and ensures that the data is passed on to main memory.

IDT79R3000A Processor Subsystem Interfaces

Figure 11 illustrates the three subsystem interfaces provided by the IDT79R3000A processor:

- **Cache control** interface (on-chip) for separate data and instruction caches permits implementation of off-chip caches using standard IDT SRAM devices. The IDT79R3000A directly controls the cache memory with a minimum of external components. Both the instruction and data cache can vary from 0 to 256kB (64K entries). The IDT79R3000A also includes the TAG control logic which determines whether or not the entry read from the cache is the desired data. The IDT79R3000A cache controller implements a direct mapped cache for high net performance (bandwidth). It has the ability to refill multiple words when a cache miss occurs, thus reducing the effective miss rate to less than 2% for large caches. When a cache miss occurs, the IDT79R3000A can support refilling the cache in 1, 4, 8, 16, or 32-word blocks to minimize the effective penalty of having to access main memory. The IDT79R3000A also incorporates the ability to perform instruction streaming; while the cache is refilling, the processor can resume execution once the missed word is obtained from main memory. In this way, the processor can continue to execute concurrently with the cache block refill.
- **Memory controller** interface for system (main) memory. This interface also includes the logic and signals to allow operation with a write buffer to further improve memory bandwidth. In addition to the standard full word access, the memory controller supports the ability to write bytes and half-words by using partial word operations. The memory controller also supports the ability to retry memory accesses if, for example, the data returned from memory is invalid and a bus error needs to be signalled.
- **Coprocessor Interface**—The IDT79R3000A features a tightly coupled co-processor interface in which all coprocessors maintain synchronization with the main processor; reside on the same data bus as the main processor; and participate in bus transactions in an identical manner to the main processor. The IDT79R3000A generates all required cache and memory control signals, including cache and memory addresses for attached coprocessors. As a result, only the data bus and a few control signals need to be connected to a coprocessor.
  The interface supports three types of coprocessor instructions: loads/stores, coprocessor operations, and processor-coprocessor transfers. Note that coprocessor loads and stores occur directly between the coprocessor and memory, without requiring the data to go through the CPU. Synchronization between the CPU and external coprocessors is achieved using a Phased-Lock Loop interface to the coprocessor. The coprocessor physical interface also includes coprocessor condition signals (CpCond(n)), which are used in coprocessor branch instructions, and a coprocessor busy signal (CpBusy) which is used to stall the CPU if the coprocessor needs to hold off subsequent operations.

  Finally, a precise exception interface is defined between the CPU and coprocessors using the external interrupt inputs of the CPU. This allows a coprocessor exception, even if it was the result of a multi-cycle operation, to be traced to the precise coprocessor operation which caused it. This is an important feature for languages which can define specific error handlers for each task.
  The interface supports up to four separate coprocessors. Coprocessor 0 is defined to be the system control coprocessor, and resides on the same chip as the CPU unit. Coprocessor 1 is the Floating Point Accelerator, IDT79R3010A. Coprocessors 2 and 3 are available to support an interface to application specific functions.

5

MULTIPROCESSING SUPPORT

The IDT79R3000A supports multiprocessing applications in a simple but effective way. Multiprocessing applications require cache coherency across the multiple processors. The IDT79R3000A offers two signals to support cache coherency: the first, MPStall, stalls the processor within two cycles of being received and keeps it from accessing the cache. This allows an external agent to snoop into the processor data cache. The second signal, MPInvalidate, causes the processor to write data on the data cache bus which indicates the externally addressed cache entry is invalid. Thus, a subsequent access to that location would result in a cache miss, and the data would be obtained from main memory.

The two MP signals would be generated by a external logic which utilizes a secondary cache to perform bus snooping functions. The IDT79R3000A does not impose an architecture for this secondary cache, but rather is flexible enough to support a variety of application specific architecture stand still maintain cache coherency. Further, there is no impact on designs which do not require this feature. The IDT79R3000A has further improved on the microprocessor support found in the IDT79R3000, by allowing the use of cache RAMs with internal address latches in multiprocessor systems.

ADVANCED FEATURES

The IDT79R3000A offers a number of additional features such as the ability to swap the instruction and data caches, facilitating diagnostics and cache flushing. Another feature isolates the caches, which forces cache hits to occur regardless of the contents of the tag fields. The IDT79R3000A allows the processor to execute user tasks of the opposite byte ordering (endianness) of the operating system, and further allows parity checking to be disabled. More details on these features can be found in the IDT79R3000A Family Hardware User's Manual.

Further features of the IDT79R3000A are configured during the last four cycles prior to the negation of the RESET input. These functions include the ability to select cache sizes and cache refill block sizes; the ability to utilize the multiprocessor interface; whether or not instruction streaming is enabled; whether byte ordering follows "Big-Endian" or "Little-Endian" protocols, etc. Table 3 shows the configuration options selected at Reset. These are further discussed in the *Hardware User's Manual.*

BACKWARD COMPATIBILITY WITH IDT79R2000

The IDT79R3000A can be used in sockets designed for the IDT79R3000. The pin-out of the IDT79R3000A has been selected to ensure this compatibility, with new functions mapped onto previously unused pins. The instruction set is compatible with that of the IDT79R2000 at the binary level. As a result, code written for the older processor can be executed. New features can be selectively disabled.

In most IDT79R3000 applications, the IDT79R3000A can be placed in the socket with no modification to initialization settings. Further application assistance on this topic is available from IDT.

PACKAGE THERMAL SPECIFICATIONS

The IDT79R3000A utilizes special packaging techniques to improve both the thermal and electrical characteristics of the microprocessor.

In order to improve the electrical characteristics of the device, the package is constructed using multiple signal planes, including individual power planes and ground planes to reduce noise associated with high-frequency TTL parts. In addition, the 175-pin PGA package utilizes extra power and ground pins to reduce the inductance from the internal power planes to the power planes of the PC Board.

In order to improve the electrical characteristics of the microprocessor, the device is housed using cavity down packaging. In addition, these packages incorporate a copper-tungsten thermal slug designed to efficiently transfer heat from the die to the case of the package, and thus effectively lower the thermal resistance of the package. The use of an additional external heat sink affixed to the package thermal slug further decreases the effective thermal resistance of the package.

The case temperature may be measured in any environment to determine whether the device is within the specified operating range. The case temperature should be measured at the center of the top surface opposite the package cavity (the package cavity is the side where the package lid is mounted).

The equivalent allowable ambient temperature, T_A, can be calculated using the thermal resistance from case to ambient (0ca) for the given package. The following equation relates ambient and case temperature:

$$T_A = T_c - P*\varnothing ca$$

where P is the maximum power consumption, calculated by using the maximum Icc from the DC Electrical Characteristics section.

Typical values for Øca at various airflows are shown in table 4 for various CPU packages.

R3000A PACKAGE CHARACTERISTICS

	Airflow - (ft/min)					
0	200	400	600	800	1000	
Øca (175-PGA, 144-PGA)	21	7	3	2	1	0.5
Øca (172 Quad Flatpack)	23	9	4	3	2.5	1.5

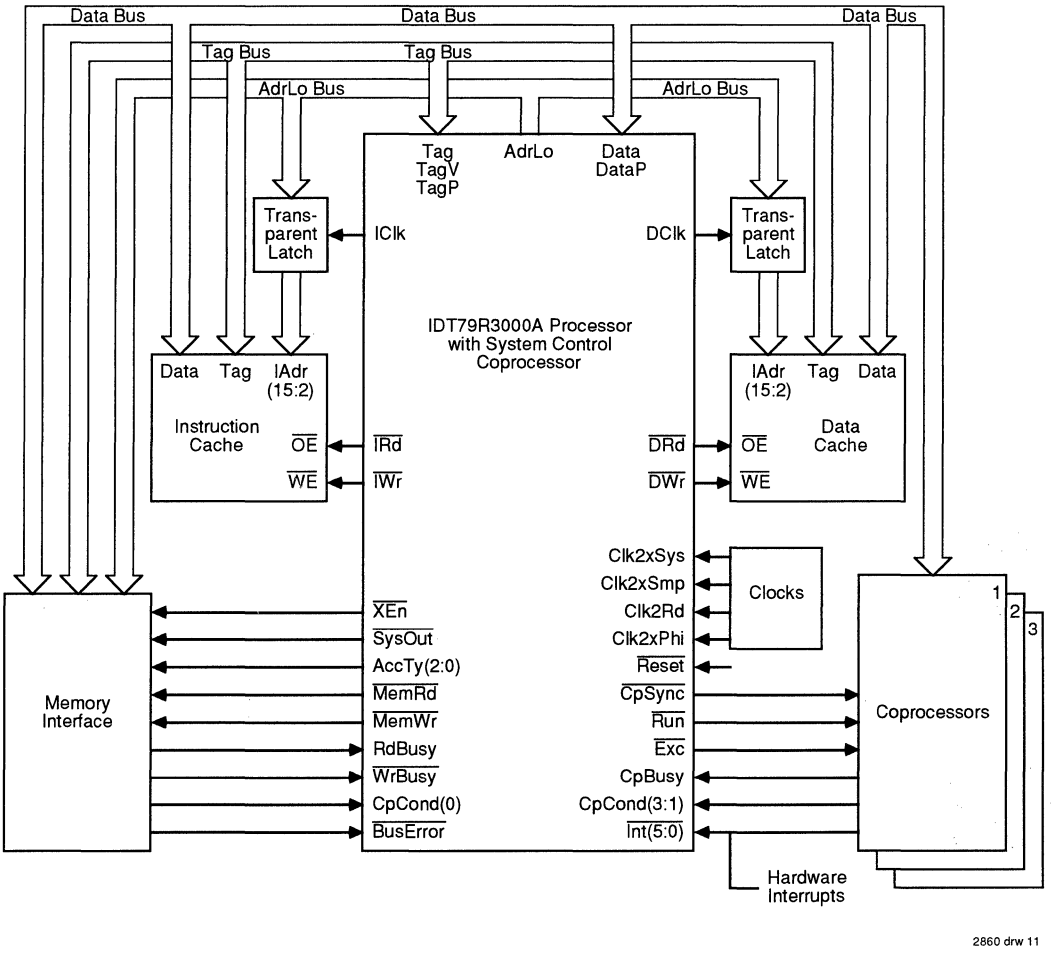
2860 tbl 03

R3000A MODE SELECTABLE FEATURES

Input	W Cycle	X Cycle	Y Cycle	Z Cycle
Int0	DBlkSize0	DBlkSize1	Extend Cache	Big Endian
Int1	IBlkSize0	IBlkSize1	MPAdrDisable	TriState
Int2	DispPar/RevEnd	IStream	IgnoreParity	NoCache
Int3	Reserved(1)	StorePartial	MultiProcessor	BusDriveOn
Int4	PhaseDelayOn(2)	PhaseDelayOn(2)	PhaseDelayOn(2)	PhaseDelayOn(2)
Int5	R3000 Mode(2)	R3000 Mode(2)	R3000 Mode(2)	R3000 Mode(2)

2860 tbl 04

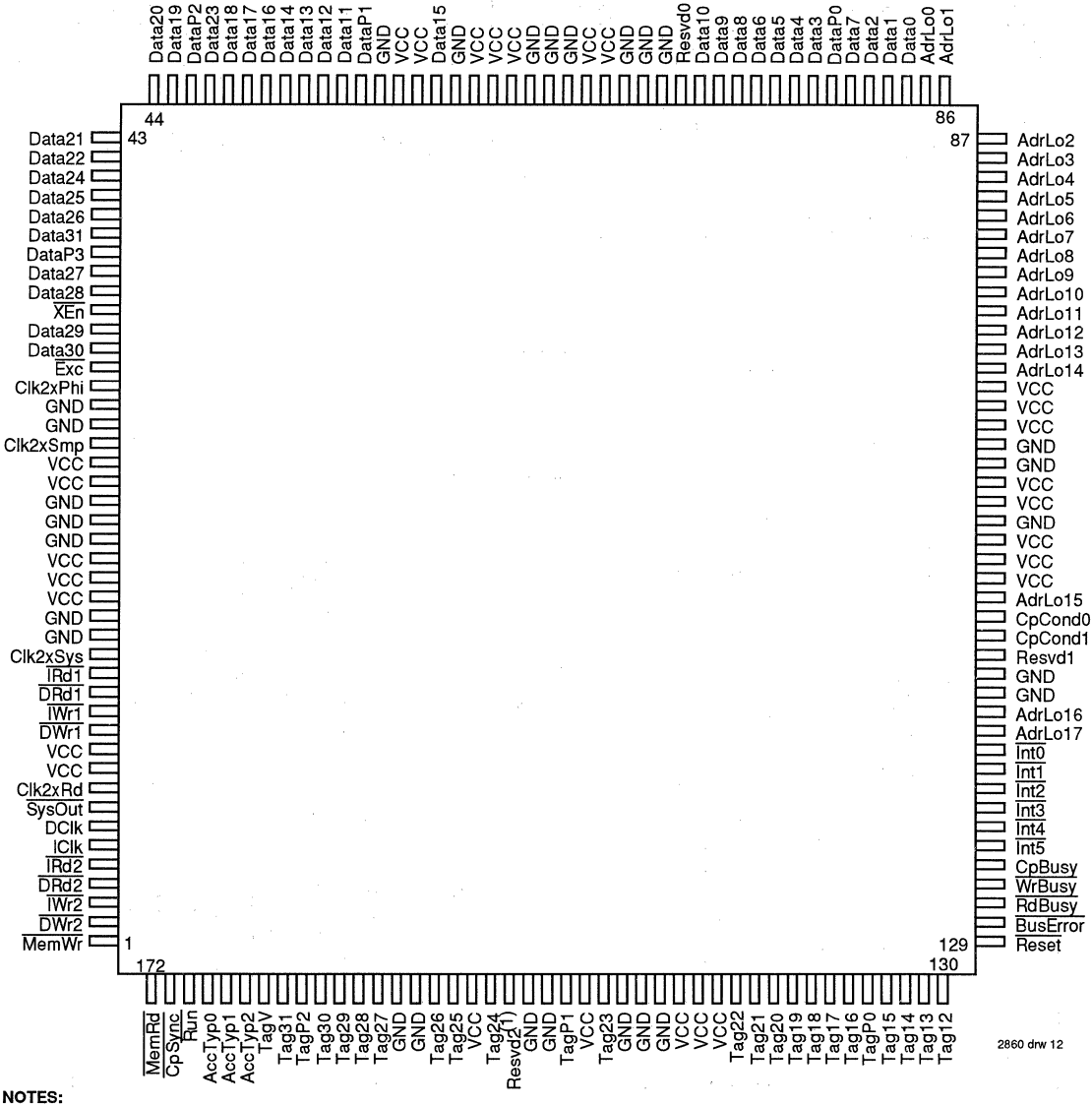
NOTES:
1. Reserved entries must be driven high.
2. These values must be driven stable throughout the enfire RESET period.



2860 drw 11

Figure 11. IDT79R3000A Subsystem Interfaces Example; 64 KB Caches

PIN CONFIGURATION



NOTES:

1. Reserved pins must not be connected.
2. AdrLo 16 and 17 are multifunction pins which are controlled by mode select programming on interrupt pins at reset time
   AdrLo 16: MP Invalidate, CpCond (2).
   AdrLo 17: MP Stall, CpCond (3).

172-Pin Flatpack (Top View)

PIN CONFIGURATION

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	(No Pin)	AdrLo 6	AdrLo 10	AdrLo 11	VCC	AdrLo 14	AdrLo 15	CpCond 0	AdrLo 16	AdrLo 17	$\overline{\text{Int(2)}}$	$\overline{\text{Int(5)}}$	Wr Busy	$\overline{\text{Reset}}$	VCC
B	AdrLo 3	$\overline{\text{DRd2}}$	AdrLo 7	AdrLo 9	AdrLo 12	$\overline{\text{IRd2}}$	AdrLo 13	CpCond 1	$\overline{\text{Int(1)}}$	$\overline{\text{Int(3)}}$	Cp Busy	$\overline{\text{Bus Error}}$	DWr2	Tag12	Tag15
C	AdrLo 0	AdrLo 4	VCC	AdrLo 5	AdrLo 8	GND	GND	VCC	$\overline{\text{Int(0)}}$	$\overline{\text{Int(4)}}$	Rd Busy	GND	Tag13	TagP0	Tag18
D	Data 1	AdrLo 2	GND	GND	VCC	GND	VCC	GND	VCC	GND	VCC	GND	Tag14	Tag17	Tag19
E	DataP 0	Data 0	AdrLo 1	VCC								VCC	Tag16	Tag20	VCC
F	VCC	Data 7	Data 2	GND								GND	GND	Tag21	Tag23
G	Data 4	Data 3	GND	VCC								VCC	GND	Tag22	TagP1
H	Data 6	Data 5	Data 8	GND								GND	VCC	Tag25	Tag24
J	Data 10	DataP 1	Data 9	VCC								VCC	Tag28	Tag29	Tag26
K	Data 15	Data 11	GND	GND								GND	GND	TagP2	Tag27
L	VCC	Data 12	Data 17	VCC								VCC	Acc Typ2	Tag31	Tag30
M	Data 13	Data 16	DataP 2	GND	VCC	GND	VCC	GND	VCC	GND	VCC	GND	GND	Acc Typ1	VCC
N	Data 14	Data 18	Data 19	GND	Data 24	DataP 3	VCC	VCC	GND	GND	$\overline{\text{DRd1}}$	$\overline{\text{Mem Wr}}$	$\overline{\text{Mem Rd}}$	$\overline{\text{Run}}$	TagV
P	Data 23	Data 20	$\overline{\text{IWr2}}$	Data 22	Data 26	Data 27	$\overline{\text{XEn}}$	Data 30	Clk2x Sys	Clk2x Rd	DClk	$\overline{\text{IRd1}}$	$\overline{\text{IWr1}}$	$\overline{\text{Cp Sync}}$	Acc Typ0
Q	VCC	Data 21	Data 25	Data 31	Data 28	GND	Data 29	$\overline{\text{Excep-tion}}$	Clk2x Phi	Clk2x Smp	$\overline{\text{SysOut}}$	VCC	IClk	$\overline{\text{DWr1}}$	VCC

2860 drw 13

NOTE:
1. AdrLo 16 and 17 are multifunction pins which are controlled by mode select programming on interrupt pins at reset time
   AdrLo 16: MP Invalidate, CpCond (2).
   AdrLo 17: MP Stall, CpCond (3).

175-Pin PGA (Top View)

5

PIN CONFIGURATION

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	VCC	AdrLo 6	AdrLo 10	AdrLo 11	VCC	AdrLo 14	AdrLo 15	CpCond 0	AdrLo 16	AdrLo 17	$\overline{\text{Int(2)}}$	$\overline{\text{Int(5)}}$	Wr Busy	$\overline{\text{Reset}}$	VCC
B	AdrLo 3	$\overline{\text{DRd2}}$	AdrLo 7	AdrLo 9	AdrLo 12	$\overline{\text{IRd2}}$	AdrLo 13	CpCond 1	$\overline{\text{Int(1)}}$	$\overline{\text{Int(3)}}$	Cp Busy	$\overline{\text{Bus Error}}$	$\overline{\text{DWr2}}$	Tag12	Tag15
C	AdrLo 0	AdrLo 4	VCC	AdrLo 5	AdrLo 8	GND	GND	VCC	$\overline{\text{Int(0)}}$	$\overline{\text{Int(4)}}$	Rd Busy	GND	Tag13	TagP0	Tag18
D	Data 1	AdrLo 2	GND	GND									Tag14	Tag17	Tag19
E	DataP 0	Data 0	AdrLo 1										Tag16	Tag20	VCC
F	VCC	Data 7	Data 2										GND	Tag21	Tag23
G	Data 4	Data 3	GND										GND	Tag22	TagP1
H	Data 6	Data 5	Data 8										VCC	Tag25	Tag24
J	Data 10	DataP 1	Data 9										Tag28	Tag29	Tag26
K	Data 15	Data 11	GND										GND	TagP2	Tag27
L	VCC	Data 12	Data 17										Acc Typ2	Tag31	Tag30
M	Data 13	Data 16	DataP 2										GND	Acc Typ1	VCC
N	Data 14	Data 18	Data 19	GND	Data 24	DataP 3	VCC	VCC	GND	GND	$\overline{\text{DRd1}}$	$\overline{\text{Mem Wr}}$	$\overline{\text{Mem Rd}}$	$\overline{\text{Run}}$	TagV
P	Data 23	Data 20	$\overline{\text{IWr2}}$	Data 22	Data 26	Data 27	$\overline{\text{XEn}}$	Data 30	Clk2x Sys	Clk2x Rd	DClk	$\overline{\text{IRd1}}$	$\overline{\text{IWr1}}$	$\overline{\text{Cp Sync}}$	Acc Typ0
Q	VCC	Data 21	Data 25	Data 31	Data 28	GND	Data 29	$\overline{\text{Excep-tion}}$	Clk2x Phi	Clk2x Smp	$\overline{\text{SysOut}}$	VCC	IClk	$\overline{\text{DWr1}}$	VCC

NOTE:

1. AdrLo 16 and 17 are multifunction pins which are controlled by mode select programming on interrupt pins at reset time.
   AdrLo 16: MP Invalidate, CpCond (2).
   AdrLo 17: MP Stall, CpCond (3).

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144-Pin PGA (Top View)

PIN DESCRIPTIONS

Pin Name	I/O	Description
Data (0-31)	I/O	A 32-bit bus used for all instruction and data transmission among the processor, caches, memory interface, and coprocessors.
DataP (0-3)	I/O	A 4-bit bus containing even parity over the data bus.
Tag (12-31)	I/O	A 20-bit bus used for transferring cache tags and high addresses between the processor, caches, and memory interface.
TagV	I/O	The tag validity indicator.
Tag P (0-2)	I/O	A 3-bit bus containing even parity over the concatenation of TagV and Tag.
AdrLo (0-17)	O	An 18-bit bus containing byte addresses used for transferring low addresses from the processor to the caches and memory interface. (AdrLo 16: CpCond (2), AdrLo 17: CpCond (3) set by reset initialization).
$\overline{\text{IRd1}}$	O	Read enable for the instruction cache.
$\overline{\text{IWr1}}$	O	Write enable for the instructon cache.
$\overline{\text{IRd2}}$	O	An identical copy of $\overline{\text{IRd1}}$ used to split the load.
$\overline{\text{IWr2}}$	O	An identical copy of $\overline{\text{IWr1}}$ used to split the load.
IClk	O	The instruction cache address latch clock. This clock runs continuously.
$\overline{\text{DRd1}}$	O	The read enable for the data cache.
$\overline{\text{DWr1}}$	O	The write enable for the data cache.
$\overline{\text{DRd2}}$	O	An identical copy of $\overline{\text{DRd1}}$ used to split the load.
$\overline{\text{DWr2}}$	O	An identical copy of $\overline{\text{DWr1}}$ used to split the load.
DClk	O	The data cache address latch clock. This clock runs continuously.
$\overline{\text{XEn}}$	O	The read enable for the Read Buffer.
AccTyp(0-2)	O	A 3-bit bus used to indicate the size of data being transferred on the data bus, whether or not a data transfer is occurring, and the purpose of the transfer.
$\overline{\text{MemWr}}$	O	Signals the occurrence of a main memory write.
$\overline{\text{MemRd}}$	O	Signals the occurrence of a main memory read.
$\overline{\text{BusError}}$	I	Signals the occurrence of a bus error during a main memory read or write.
$\overline{\text{Run}}$	O	Indicates whether the processor is in the run or stall state.
$\overline{\text{Exception}}$	O	Indicates that the instruction about to commit state should be aborted and other exception related information.
$\overline{\text{SysOut}}$	O	A reflection of the internal processor clock used to generate the system clock.
$\overline{\text{CpSync}}$	O	A clock which is identical to $\overline{\text{SysOut}}$ and used by coprocessors for timing synchronization with the CPU.
RdBusy	I	The main memory read stall termination signal. In most system designs RdBusy is normally asserted and is deasserted only to indicate the successful completion of a memory read. RdBusy is sampled by the processor only during memory read stalls.
$\overline{\text{WrBusy}}$	I	The main memory write stall initiation/termination signal.
CpBusy	I	The coprocessor busy stall initiation/termination signal.
CpCond (0-1)	I	A 2-bit bus used to transfer conditional branch status from the coprocessors to the main processor.
CpCond (2-3)	I	Conditional branch status from coprocessors to the processor. Function is provided on AdrLo 16/17 pins and is selected at reset time.
MPStall	I	Multiprocessing Stall. Signals to the processor that it should stall accesses to the caches in a multiprocessing environment. This is physically the same pin as CpCond3; its use is determined at RESET initialization.
MPInvalidate	I	Multiprocessing Invalidate. Signals to the processor that it should issue invalidate data on the cache data bus. The address to be invalidated is externally provided. This is the same pin as CpCond2; its use is determined at RESET initialization.
$\overline{\text{Int}}$ (0-5)	I	A 6-bit bus used by the memory interface and coprocessors to signal maskable interrupts to the processor. At reset time, mode select values are read in.

2860 tbl 05

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PIN DESCRIPTIONS (Continued)

Pin Name	I/O	Description
Clk2xSys	I	The master double frequency input clock used for generating $\overline{SysOut}$.
Clk2xSmp	I	A double frequency clock input used to determine the sample point for data coming into the processor and coprocessors.
Clk2xRd	I	A double frequency clock input used to determine the enable time of the cache RAMs.
Clk2xPhi	I	A double frequency clock input used to determine the position of the internal phases, phase1 and phase2.
$\overline{Reset}$	I	Synchronous initialization input used to force execution starting from the reset memory address. $\overline{Reset}$ must be deasseted synchronously but asserted asynchronously. The deassertion of $\overline{Reset}$ must be synchronized by the leading edge of $\overline{SysOut}$.

2860 tbl 06

ABSOLUTE MAXIMUM RATINGS(1, 3)

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A, T_C	Operating Temperature	0 to +70(4) (Ambient) 0 to +90(5) (Case)	°C
T_{BIAS}	Case Temperature Under Bias	–55 to +125(4) 0 to +90(5)	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{IN}	Input Voltage	–0.5 to +7.0	V

2860 tbl 07

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN} minimum = –3.0V for pulse width less than 15ns. V_{IN} should not exceed V_{CC} +0.5 Volts.
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.
4. 16-33 MHz only.
5. 37-40 MHz only.

AC TEST CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{IH}	Input HIGH Voltage	3.0	—	V
V_{IL}	Input LOW Voltage	—	0.4	V
V_{IHS}	Input HIGH Voltage	3.5	—	V
V_{ILS}	Input LOW Voltage	—	0.4	V

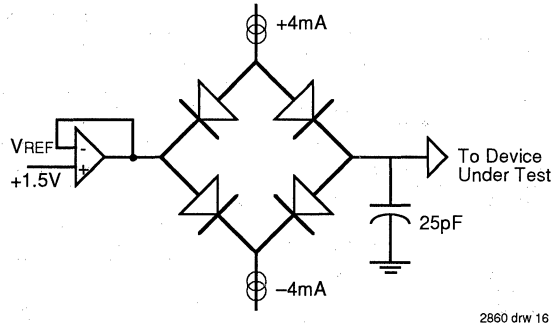
2860 tbl 08

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Commercial 16-33 MHz	0°C to +70°C (Ambient)	0V	5.0 ±5%
Commercial 40 MHz	0°C to +90°C (Case)	0V	5.0 ±5%

2860 tbl 09

OUTPUT LOADING FOR AC TESTING



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DC ELECTRICAL CHARACTERISTICS
COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to +70°C, V_{CC} = +5.0V ±5%)

Symbol	Parameter	Test Conditions	79R3000A				79R3000AE				Unit
			16.67MHz		20.0MHz		25.0MHz		33.33MHz		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = -4mA	3.5	—	3.5	—	3.5	—	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	—	0.4	—	0.4	—	0.4	—	0.4	V
V_{OHC}	Output HIGH Voltage(7)	V_{CC} = Min., I_{OH} = -4mA	4.0	—	4.0	—	4.0	—	4.0	—	V
V_{OHT}	Output HIGH Voltage(4,6)	V_{CC} = Min., I_{OH} = -8mA	2.4	—	2.4	—	2.4	—	2.4	—	V
V_{OLT}	Output LOW Voltage(4,6)	V_{CC} = Min., I_{OL} = 8mA	—	0.8	—	0.8	—	0.8	—	0.8	V
V_{IH}	Input HIGH Voltage(5)		2.0	—	2.0	—	2.0	—	2.0	—	V
V_{IL}	Input LOW Voltage(1)		—	0.8	—	0.8	—	0.8	—	0.8	V
V_{IHS}	Input HIGH Voltage(2,5)		3.0	—	3.0	—	3.0	—	3.0	—	V
V_{ILS}	Input LOW Voltage(1,2)		—	0.4	—	0.4	—	0.4	—	0.4	V
C_{IN}	Input Capacitance(6)		—	10	—	10	—	10	—	10	pF
C_{OUT}	Output Capacitance(6)		—	10	—	10	—	10	—	10	pF
I_{CC}	Operating Current	V_{CC} = 5V, T_A = 70°C	—	450	—	550	—	650	—	750	mA
I_{IH}	Input HIGH Leakage(3)	V_{IH} = VCC	—	100	—	100	—	100	—	100	µA
I_{IL}	Input LOW Leakage(3)	V_{IL} = GND	–100	—	–100	—	–100	—	–100	—	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = VCC, V_{OL} = GND	–100	100	–100	100	–100	100	–100	100	µA

2860 tbl 10

NOTES:

1. V_{IL} Min. = –3.0V for pulse width less than 15ns. V_{IL} should not fall below –0.5 Volts for larger periods.
2. V_{IHS} and V_{ILS} apply to Clk2xSys, Clk2xSmp, Clk2xRd, Clk2xPhi, CpBusy, and $\overline{\text{Reset}}$.
3. These parameters do not apply to the clock inputs.
4. V_{OHT} and V_{OLT} apply to the bidirectional data and tag busses only. Note that V_{IH} and V_{IL} also apply to these signals. V_{OHT} and V_{OLT} are provided to give the designer further information about these specific signals.
5. V_{IH} should not be held above V_{CC} + 0.5 volts.
6. Guaranteed by design.
7. V_{OHC} applies to $\overline{\text{RUN}}$ and $\overline{\text{Exception}}$.

5

DC ELECTRICAL CHARACTERISTICS
COMMERCIAL TEMPERATURE RANGE (T_C = 0°C to +90°C, V_{CC} = +5.0V ±5%)

Symbol	Parameter	Test Conditions	79R3000AE 40.0MHz Min.	79R3000AE 40.0MHz Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = -4mA	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	—	0.4	V
V_{OHC}	Output HIGH Voltage(7)	V_{CC} = Min., I_{OH} = –4mA	4.0	—	V
V_{OHT}	Output HIGH Voltage(4,6)	V_{CC} = Min., I_{OH} =–8mA	2.4	—	V
V_{OLT}	Output LOW Voltage(4,6)	V_{CC} = Min., I_{OL} = 8mA	—	0.8	V
V_{IH}	Input HIGH Voltage(5)		2.0	—	V
V_{IL}	Input LOW Voltage(1)		—	0.8	V
V_{IHS}	Input HIGH Voltage(2,5)		3.0	—	V
V_{ILS}	Input LOW Voltage(1,2)		—	0.4	V
C_{IN}	Input Capacitance(6)		—	10	pF
C_{OUT}	Output Capacitance(6)		—	10	pF
I_{CC}	Operating Current	V_{CC} = 5V, T_A = 70°C	—	850	mA
I_{IH}	Input HIGH Leakage(3)	V_{IH} = VCC	—	100	µA
I_{IL}	Input LOW Leakage(3)	V_{IL} = GND	–100	—	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = VCC, V_{OL} = GND	–100	100	µA

2860 tbl 12

NOTES:

1. V_{IL} Min. = –3.0V for pulse width less than 15ns. V_{IL} should not fall below –0.5 Volts for larger periods.
2. V_{IHS} and V_{ILS} apply to Clk2xSys, Clk2xSmp, Clk2xRd, Clk2xPhi, CpBusy, and $\overline{\text{Reset}}$.
3. These parameters do not apply to the clock inputs.
4. V_{OHT} and V_{OLT} apply to the bidirectional data and tag busses only. Note that V_{IH} and V_{IL} also apply to these signals. V_{OHT} and V_{OLT} are provided to give the designer further information about these specific signals.
5. V_{IH} should not be held above V_{CC} + 0.5 volts.
6. Guaranteed by design.
7. V_{OHC} applies to $\overline{\text{RUN}}$ and $\overline{\text{Exception}}$.

AC ELECTRICAL CHARACTERISTICS(1,2,3)

COMMERCIAL TEMPERATURE RANGE (TA = 0°C to +70°C, VCC = +5.0V ±5%)

Symbol	Parameter	Test Conditions	79R3000A 16.67MHz Min.	79R3000A 16.67MHz Max.	79R3000A 20.0MHz Min.	79R3000A 20.0MHz Max.	79R3000AE 25.0MHz Min.	79R3000AE 25.0MHz Max.	79R3000AE 33.33MHz Min.	79R3000AE 33.33MHz Max.	Unit
Clock											
TCkHigh	Input Clock HIGH(2)	Note 7	12.5	—	10	—	8.0	—	6.0	—	ns
TCkLow	Input Clock LOW(2)	Note 7	12.5	—	10	—	8.0	—	6.0	—	ns
TCkP	Input Clock Period(2)		30	500	25	500	20	500	15	500	ns
	Clk2xSys to Clk2XSmp(6)		0	tcyc/4	0	tcyc/4	0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xRd(6)		0	tcyc/4	0	tcyc/4	0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xPhi(6)		9.0	tcyc/4	7.0	tcyc/4	5.0	tcyc/4	3.5	tcyc/4	ns
Run Operation											
TDEn	Data Enable(3)		—	–2.0	—	–2.0	—	–1.5	—	–1.5	ns
TDDis	Data Disable(3)		—	–1.0	—	–1.0	—	–0.5	—	–0.5	ns
TDVal	Data Valid	Load= 25pF	—	3.0	—	3.0	—	2.0	—	2.0	ns
TWrDly	Write Delay	Load= 25pF	—	5.0	—	4.0	—	3.0	—	2.0	ns
TDS	Data Set-up		9.0	—	8.0	—	6.0	—	4.5	—	ns
TDH	Data Hold(3)		–2.5	—	–2.5	—	–2.5	—	–2.5	—	ns
TCBS	CpBusy Set-up		13	—	11	—	9.0	—	7.0	—	ns
TCBH	CpBusy Hold		–2.5	—	–2.5	—	–2.5	—	–2.5	—	ns
TAcTy	Access Type (1:0)	Load= 25pF	—	7.0	—	6.0	—	5.0	—	3.5	ns
TAT2	Access Type 2	Load= 25pF	—	17	—	14	—	12	—	8.5	ns
TMWr	Memory Write	Load= 25pF	—	27	—	23	—	18	—	9.5	ns
TExc	Exception	Load= 25pF	—	7.0	—	7.0	—	5.0	—	3.5	ns
TAval	Address Valid	Load= 25pF	—	2.0	—	2.0	—	1.5	—	1.0	ns
TIntS	$\overline{\text{Int(n)}}$ Set-up		9.0	—	8.0	—	6.0	—	4.5	—	ns
TIntH	$\overline{\text{Int(n)}}$ Hold		–2.5	—	–2.5	—	–2.5	—	–2.5	—	ns
Stall Operation											
TSAVal	Address Valid	Load= 25pF	—	30	—	23	—	20	—	15	ns
TSAcTy	Access Type	Load= 25pF	—	27	—	23	—	18	—	13.5	ns
TMRdi	Memory Read Initiate	Load= 25pF	1.0	27	1.0	23	1.0	18	1.0	13.5	ns
TMRdt	Memory Read Terminate	Load= 25pF	—	27	—	23	—	18	—	10	ns
TStl	Run Terminate	Load= 25pF	3.0	17	3.0	15	3.0	10	2.0	7.5	ns
TRun	Run Initiate	Load= 25pF	—	7.0	—	6.0	—	4.0	—	3.0	ns
TSMWr	Memory Write	Load= 25pF	3.0	27	3.0	23	3.0	18	2.0	9.5	ns
TSExc	Exception Valid	Load= 25pF	—	15	—	13	—	10	—	7.5	ns
Reset Initialization											
TRST	Reset Pulse Width		6.0	—	6.0	—	6.0	—	6.0	—	Tcyc
TrstPLL	Reset timing, Phase-lock on(4,5)		3000	—	3000	—	3000	—	3000	—	Tcyc
Trstcp	Reset timing, Phase-lock off(4,5)		128	—	128	—	128	—	128	—	Tcyc
Capacitive Load Deration											
CLD	Load Derate(6)		0.5	2.0	0.5	1.0	0.5	1.0	0	1.0	ns/25pF

2860 tbl 13

NOTES:

1. All timings are referenced to 1.5V.
2. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. These parameters apply when the IDT79R3010 Floating Point Coprocessor is connected to the CPU. With phase lock on, $\overline{\text{Reset}}$ must be asserted for the longer of 3000 clock cycles or 200 microseconds.
5. Tcyc is one CPU clock cycle (two cycles of a 2x clock).
6. With the exception of the $\overline{\text{Run}}$ signal, no two signals on a given device will derate for a given load by a difference greater than 15%.
7. Clock transition time < 2.5ns for 33.33MHz; clock transition time < 5ns for other speeds.

5

AC ELECTRICAL CHARACTERISTICS(1,2,3)

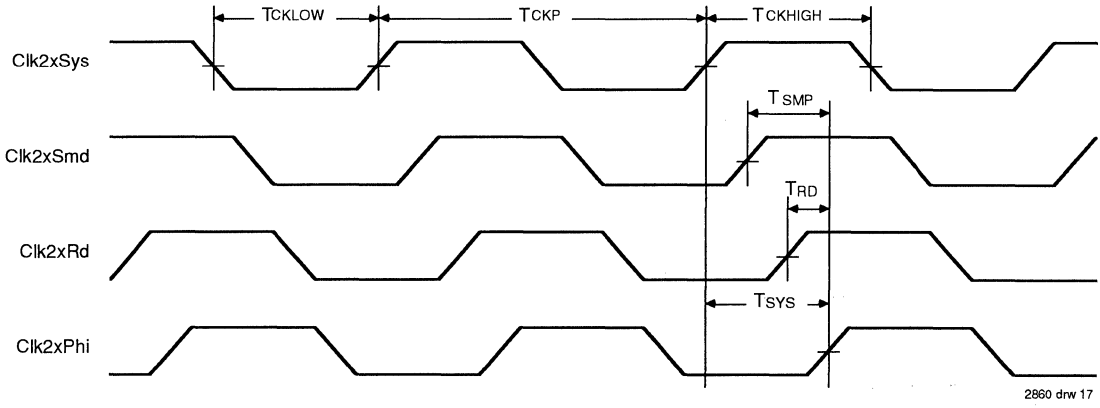
COMMERCIAL TEMPERATURE RANGE (Tc = 0°C to +90°C, Vcc = +5.0V ±5%)

Symbol	Parameter	Test Conditions	79R3000AE 40.0MHz Min.	79R3000AE 40.0MHz Max.	Unit
Clock					
TCkHigh	Input Clock High(2)	Note 7	5.0	—	ns
TCkLow	Input Clock Low(2)	Note 7	5.0	—	ns
TCkP	Input Clock Period(2)		12.5	500	ns
	Clk2xSys to Clk2XSmp(6)		0	tcyc/4	ns
	Clk2xSmp to Clk2xRd(6)		0	tcyc/4	ns
	Clk2xSmp to Clk2xPhi(6)		3.0	tcyc/4	ns
Run Operation					
	TDEn	Data Enable(3)	—	–1.5	ns
TDDis	Data Disable(3)		—	–0.5	ns
TDVal	Data Valid	Load= 25pF	—	1.5	ns
TWrDly	Write Delay	Load= 25pF	—	2.0	ns
TDS	Data Set-up		4.0	—	ns
TDH	Data Hold(3)		–2.5	—	ns
TCBS	CpBusy Set-up		6.0	—	ns
TCBH	CpBusy Hold		–2.5	—	ns
TAcTy	Access Type (1:0)	Load= 25pF	—	3.0	ns
TAT2	Access Type 2	Load= 25pF	—	7.5	ns
TMWr	Memory Write	Load= 25pF	—	9.0	ns
TExc	Exception	Load= 25pF	—	3.0	ns
TAval	Address Valid	Load= 25pF	—	0.5	ns
TIntS	$\overline{\text{Int(n)}}$ Set-up		4.0	—	ns
TIntH	$\overline{\text{Int(n)}}$ Hold		–2.5	—	ns
Stall Operation					
TSAVal	Address Valid	Load= 25pF	—	12.5	ns
TSAcTy	Access Type	Load= 25pF	—	9.0	ns
TMRdi	Memory Read Initiate	Load= 25pF	—	9.0	ns
TMRdt	Memory Read Terminate	Load= 25pF	—	9.0	ns
TStl	Run Terminate	Load= 25pF	2.0	6.0	ns
TRun	Run Initiate	Load= 25pF	—	3.0	ns
TSMWr	Memory Write	Load= 25pF	2.0	9.0	ns
TSExc	Exception Valid	Load= 25pF	—	6.0	ns
Reset Initialization					
TRST	Reset Pulse Width		6.0	—	Tcyc
TrstPLL	Reset timing, Phase-lock on(4,5)		3000	—	Tcyc
Trstcp	Reset timing, Phase-lock off(4,5)		128	—	Tcyc
Capacitive Load Deration					
CLD	Load Derate(6)		0	1.0	ns/25pF

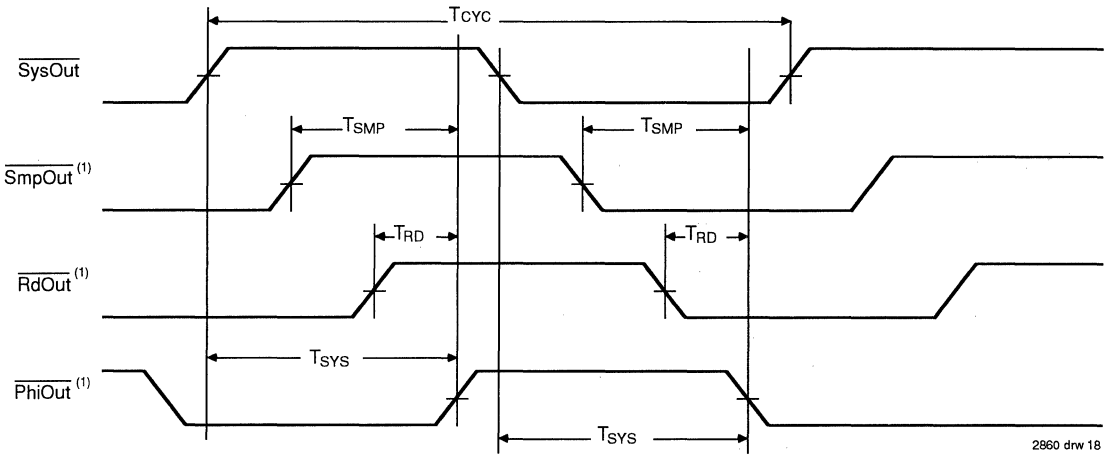
2860 tbl 15

NOTES:
1. All timings are referenced to 1.5V.
2. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. These parameters apply when the IDT79R3010 Floating Point Coprocessor is connected to the CPU. With phase lock on, $\overline{\text{Reset}}$ must be asserted for the longer of 3000 clock cycles or 200 microseconds.
5. Tcyc is one CPU clock cycle (two cycles of a 2x clock).
6. With the exception of the $\overline{\text{Run}}$ signal, no two signals on a given device will derate for a given load by a difference greater than 15%.
7. Clock transition time < 2.5ns.

INPUT CLOCK TIMING



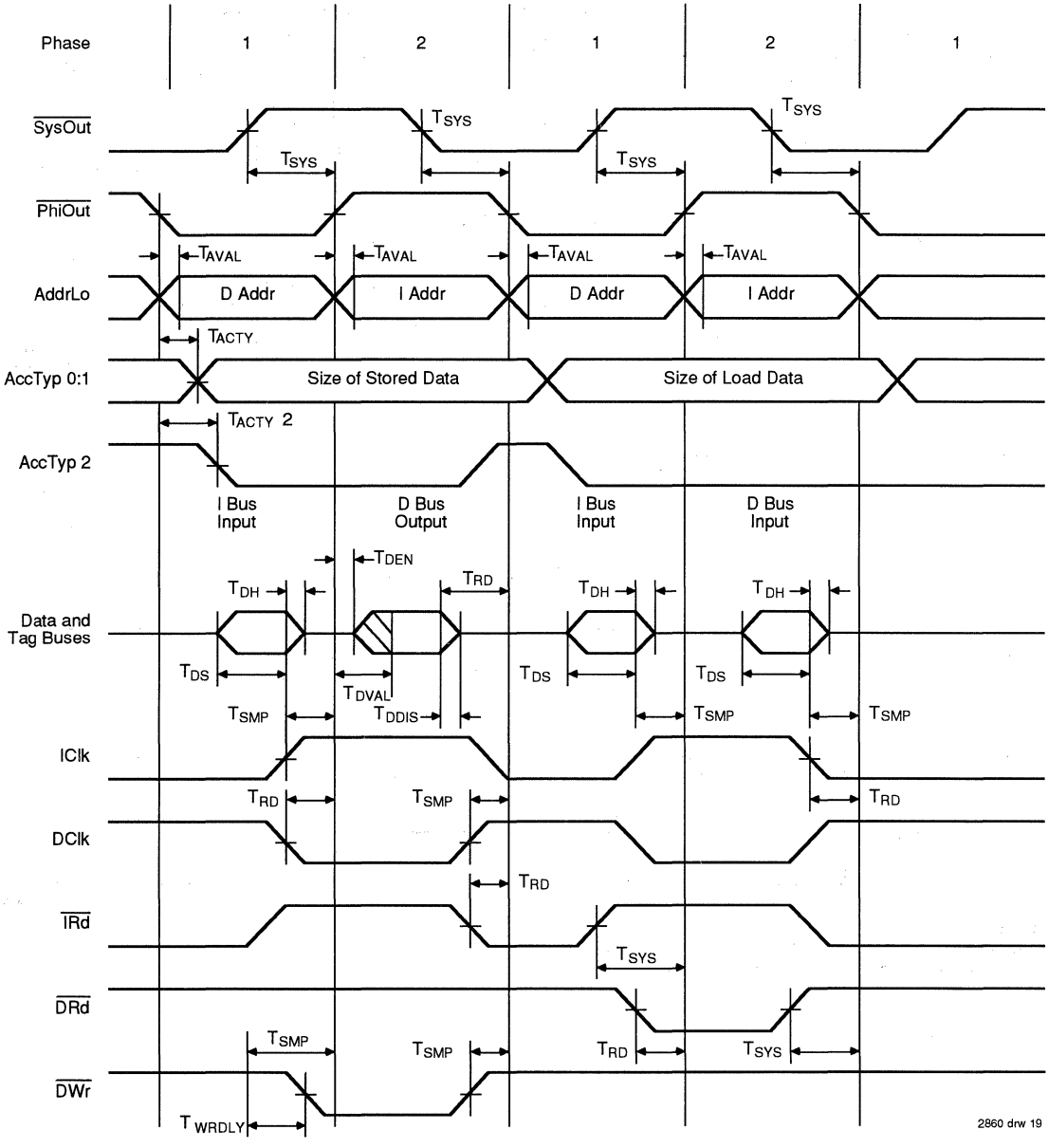
PROCESSOR REFERENCE CLOCK TIMING



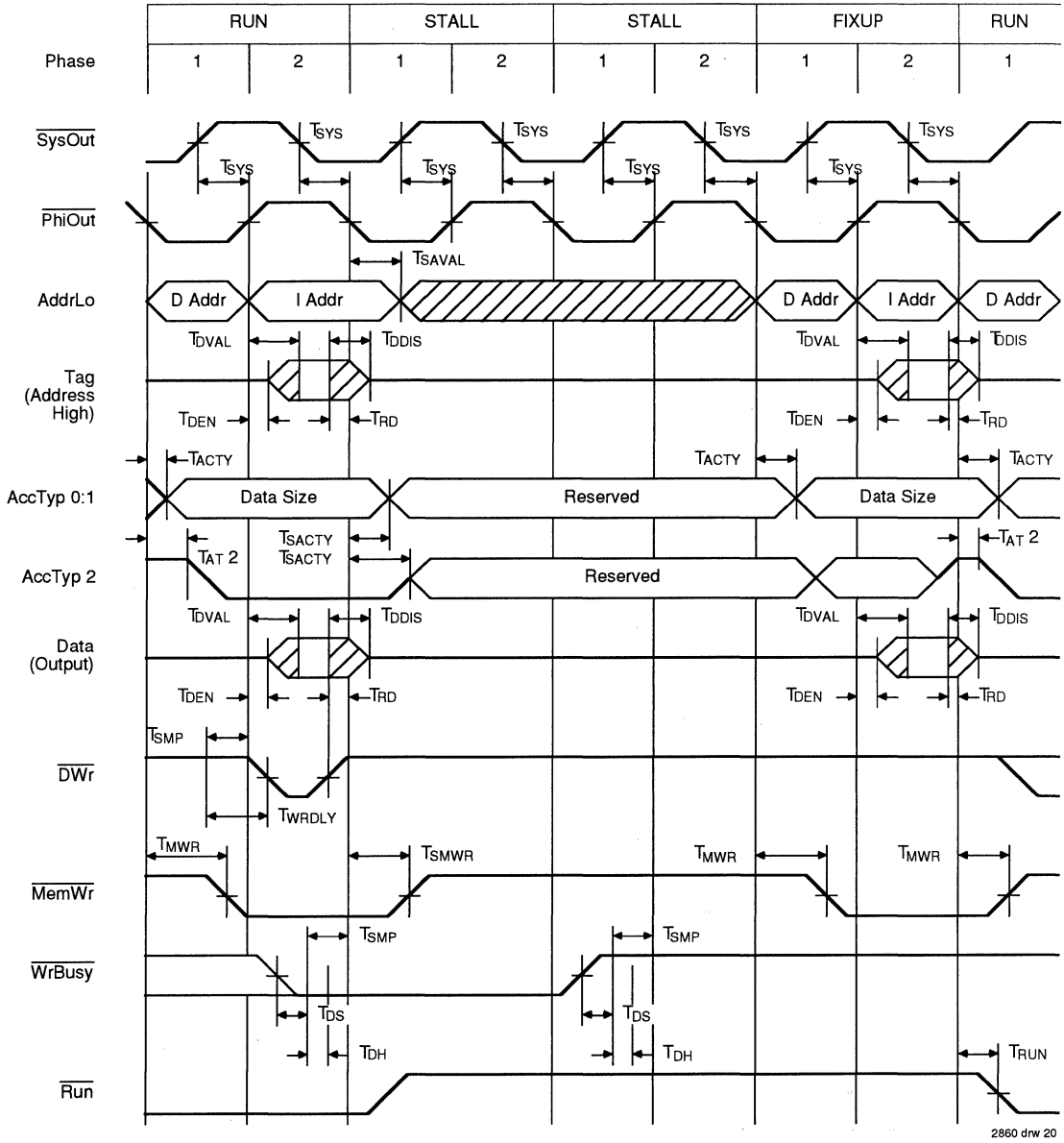
NOTE:
1. These signals are not actually output from the processor. They are drawn to provide a reference for other timing diagrams.

5

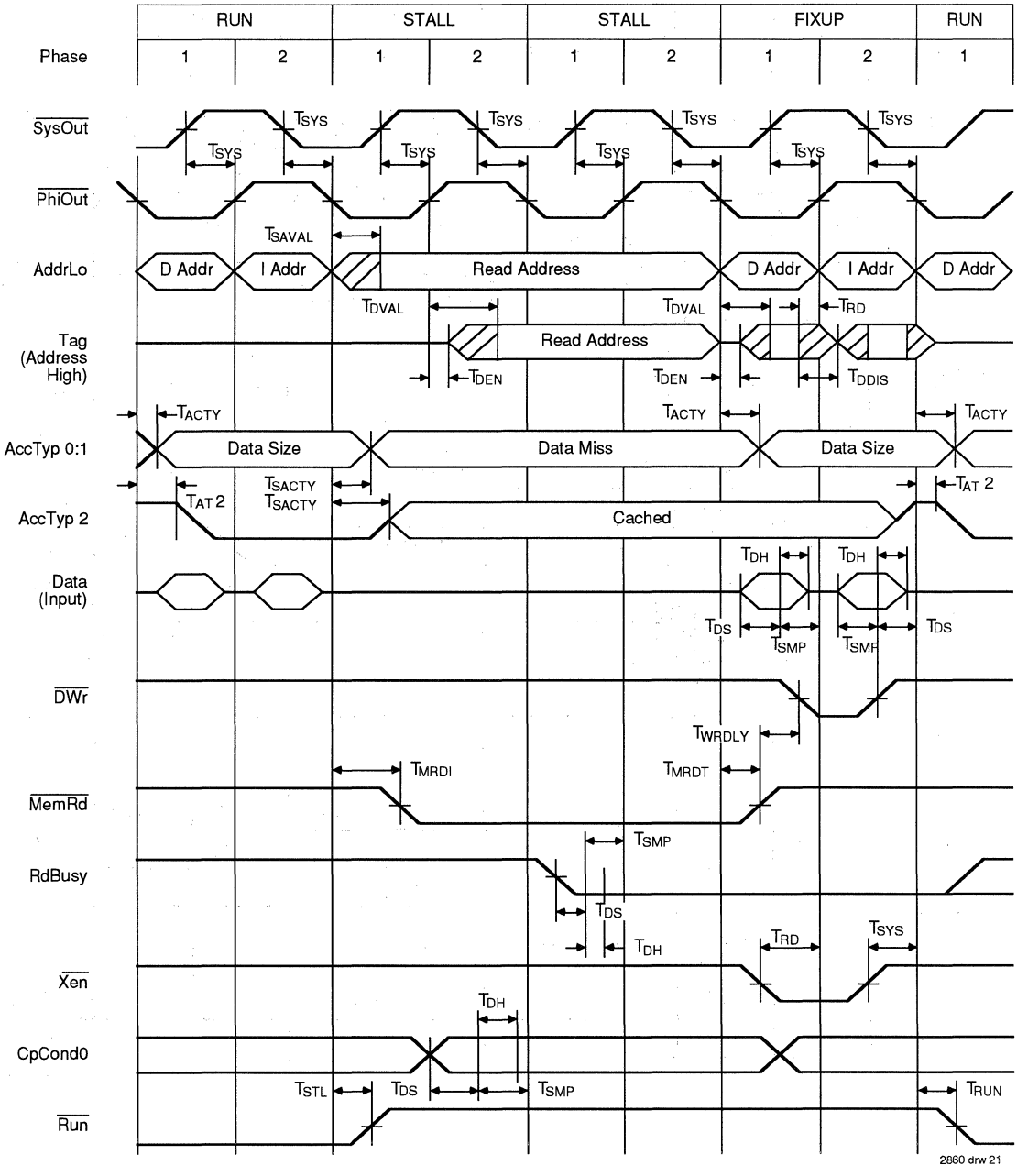
SYNCHRONOUS MEMORY (CACHE) TIMING



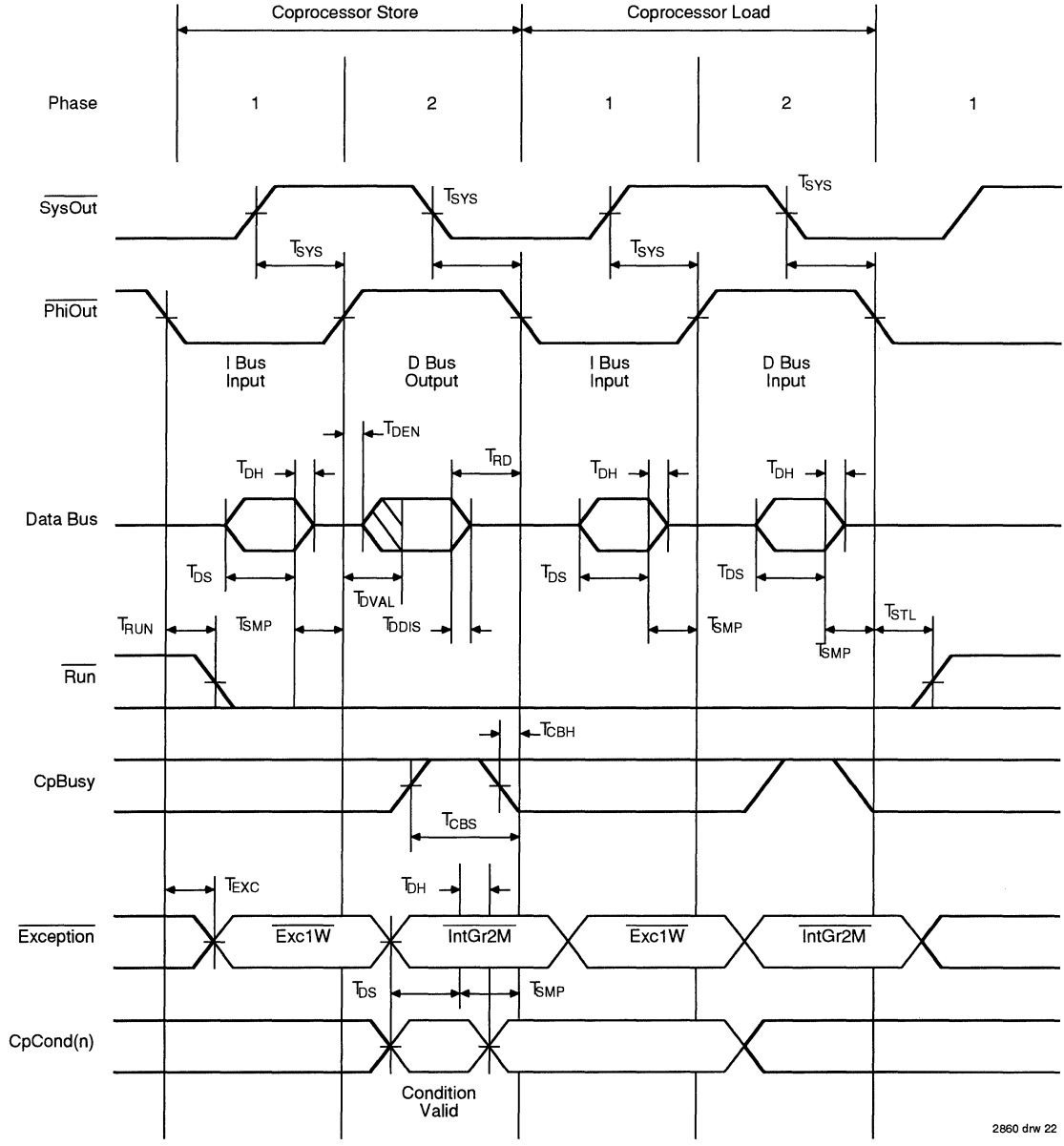
MEMORY WRITE TIMING



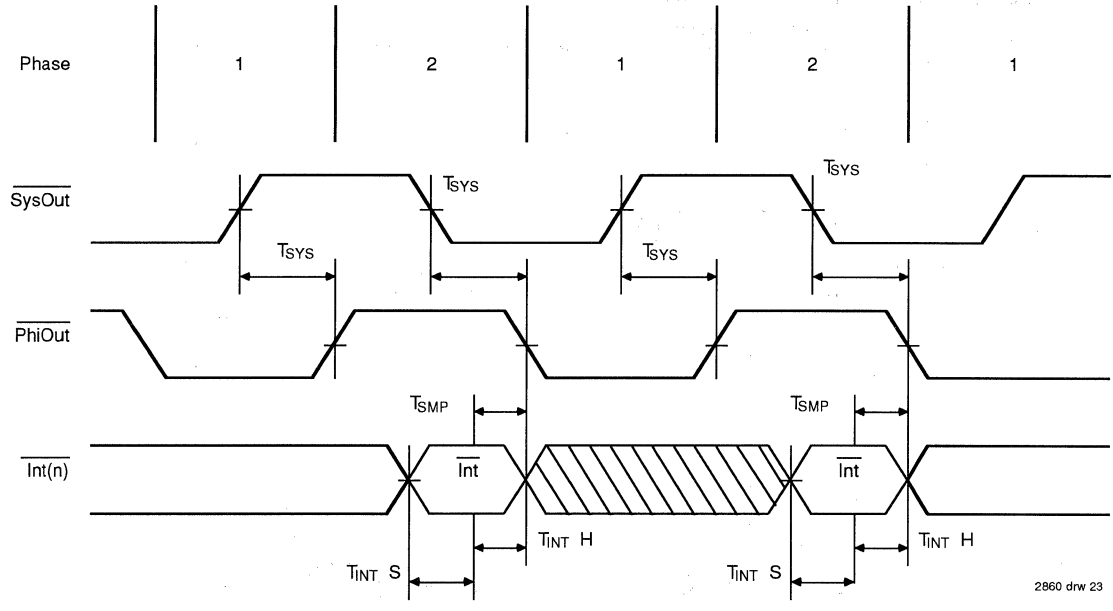
MEMORY READ TIMING



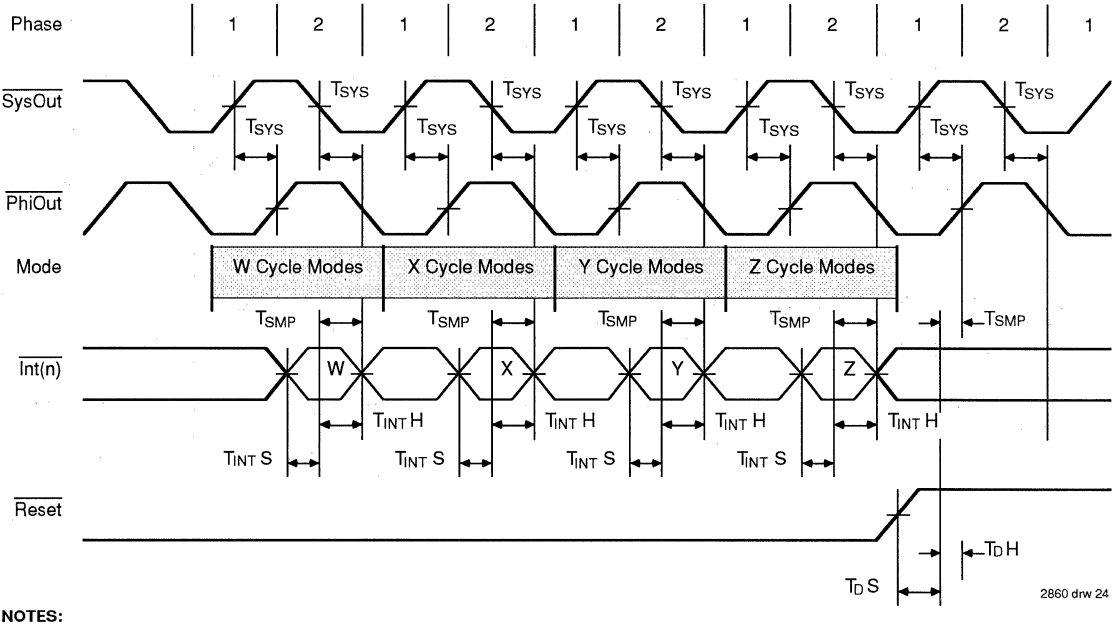
COPROCESSOR LOAD/STORE TIMING



INTERRUPT TIMING



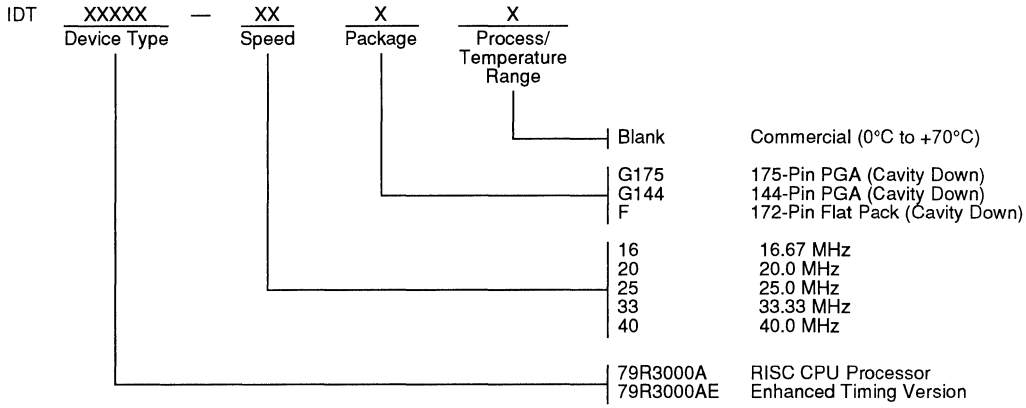
MODE VECTOR INITIALIZATION



NOTES:

1. Reset must be negated synchronously; however, it should be asserted asynchronously. Designs must not rely on the proper functioning of $\overline{\text{SysOut}}$ prior to the assertion of $\overline{\text{Reset}}$.
2. If $\overline{\text{Phase-Lock On}}$ or $\overline{\text{R3000 Mode}}$ are asserted as mode select options, they should be asserted throughout the $\overline{\text{Reset}}$ period, to insure that the slowest coprocessor in the system has sufficient time to lock to the CPU clocks.
3. $\overline{\text{Reset}}$ is actually sampled in both Phase 1 and Phase 2. To insure proper initialization, it must be negated relative to the end of Phase 1.

ORDERING INFORMATION



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VALID COMBINATIONS

IDT	79R3000A - 16, 20	All Packages
	79R3000AE - 25, 33, 40	All Packages

5

Integrated Device Technology, Inc.

RISController™ CPU FOR HIGH-PERFORMANCE EMBEDDED SYSTEMS

IDT79R3001

FEATURES:

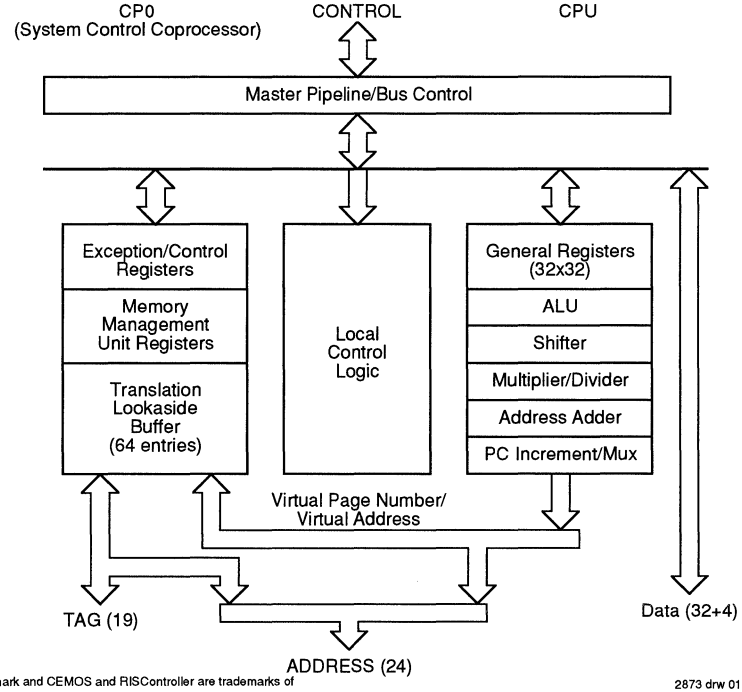
- Enhanced Instruction Set compatible version of IDT79R3000 RISC CPU
- Achieves high-performance with reduced parts count and lower overall system cost
- Flexible on-chip cache controller supports various cache, main memory sizes
- Supports optional data parity with parity error output signal
- Works with IDT79R3010A RISC Floating-Point Coprocessor
- DMA interface support
- Large synchronous memory space for real-time systems
- Full 32-bit operations — 32-bit registers, 32-bit address and data interface
- On-chip memory management unit with 64 fully-associative TLB entries maps 4GB virtual address space
- High-speed interrupt response (6 interrupt input pins) with precise exception capability
- High-speed CMOS technology results in speeds from 12.5 to 40MHz
- Supports caches from 8kB to 16MB
- Independent block refill sizes for the instruction and data caches
- Concurrent cache refill and execution
- Works on 8-, 16- and 32-bit data
- Supports unaligned 32-bit data
- Optimizing compilers for C, Ada, Pascal, Fortran, others
- RTOS support for C or Ada environments

DESCRIPTION:

The IDT79R3001 brings the high-performance inherent in the IDT79R3000 RISC Microprocessor to lower cost systems. It does this while maintaining full (both User and Kernel) software compatibility with both the IDT79R2000A and IDT79R3000 RISC Microprocessors.

The IDT79R3001 achieves lower system cost by reducing the number of components required to construct a synchronous memory (or cache) external to the processor and by simplifying the asynchronous memory interface. By removing the requirement for parity and allowing the system designer to select the cache organization which best suits the system,

FUNCTIONAL BLOCK DIAGRAM



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overall parts count is dramatically reduced while maintaining high performance.

The IDT79R3001 RISC Microprocessor extends the ability of the IDT79R3000 family to support embedded and cost sensitive applications. Its level of integration and flexibility allows high-performance systems to be constructed at reasonable cost in a straightforward manner, without forcing the system designer to support features not required in his application.

The IDT79R3001 consists of two tightly coupled processors integrated on a single chip. The first processor is a full 32-bit CPU based on RISC principles to achieve a new standard of performance in microprocessor based systems. The second processor is a system control co-processor, called CP0, containing a fully associative 64-entry TLB (Translation Lookaside Buffer), MMU (Memory Management Unit), and control registers, supporting a 4GB virtual memory subsystem and a Harvard Architecture Synchronous Memory/Cache controller which achieves ultra-high bandwidth using industry standard SRAM devices.

This data sheet provides an overview of the features and architecture of the IDT79R3001 CPU. A more detailed description of the operation and timing of this device is incorporated in the *IDT79R3001 Hardware User's Guide*, and a detailed architectural overview is provided in the *MIPS RISC Architecture* book, both available from IDT. Further literature describing the hardware, software, and development tools for the IDT79R3001 is also available from IDT.

HARDWARE OVERVIEW

The IDT79R3001 is a high-performance RISC microprocessor incorporating a fast execution engine and sophisticated yet flexible memory interface designed to support the processor bandwidth requirements at minimal system cost.

Execution Engine

The IDT79R3001 contains the same basic execution engine as the ultra-high performance IDT79R3000 and thus achieves over 28 MIPS performance at 33MHz.

The key to the performance of the processor is the instruction pipeline, illustrated in Figure 2. The execution of a single IDT79R3001 instruction consists of five primary steps, some of which may be broken down further into smaller subsets.

The five primary stages of the pipeline, each of which require approximately one CPU cycle, are:

IF Instruction Fetch, when the processor fetches the instruction from the Instruction Synchronous Memory.

RD Read required operands from on-chip register file while decoding the instruction.

ALU Perform the required operation on instruction operands.

MEM Access data memory (load or store).

WB Write results back to register file.

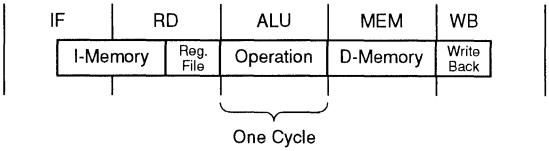

Figure 2. IDT79R3001 Five-Stage Pipeline

Thus, the CPU achieves an average execution rate approaching one instruction per CPU cycle, since the execution of five instructions at a time are overlapped within the processor (Figure 3). Optimizing compiler technology fully comprehends the interaction of software with the various pipeline resources, and serves to both eliminate any potential pipeline conflicts which might arise and to maximize instruction throughput.

The IDT79R3001 Memory Interfaces

The key to achieving the inherent performance of the IDT79R3001 is to design a memory subsystem capable of providing a new instruction to the processor on almost every clock cycle.

Like the IDT79R3000, the IDT79R3001 supports a hierarchical view of the memory subsystem. However, the IDT79R3001 allows the system designer to make more tradeoffs in the partitioning and architecture of the various levels in order to more completely meet the needs of certain types of applications.

The IDT79R3001 supports two classifications of external memory: synchronous and asynchronous. The Harvard-Architecture (separate instruction and data memories) synchronous memory allows the processor to achieve the highest levels of performance. The processor is able to obtain both an instruction and data word from the synchronous memory on every clock cycle, resulting in high instruction and data throughput.

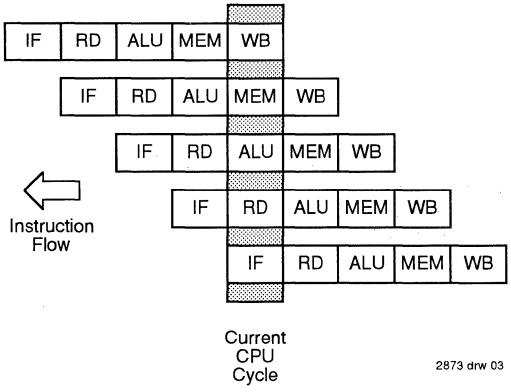

Figure 3. Instruction Execution in IDT79R3001 Pipeline

The asynchronous memory space contains larger, slower memory devices such as EPROM, main memory DRAMs, and peripheral devices. Multiple clock cycles are required for data movement in the asynchronous memory.

Many systems implement a memory hierarchy between these two memory spaces, whereby the synchronous memory space is used as processor caches and the asynchronous memory space is used for main memory. The IDT79R3001 integrates a flexible Direct-Mapped Cache Controller On-Chip, eliminating external cache control logic and minimizing cache management overhead. If the synchronous memory space is used for processor caches, then cache "misses" will cause the processor to automatically process an asynchronous memory transfer to refill the cache.

The key to achieving the system cost and performance goals of an IDT79R3001-based system is to partition the memory system to the needs of the application.

Synchronous Memory System

As with any high-performance processor, the IDT79R3001 requires high-bandwidth to achieve high-performance. Thus, it is important that the majority of its execution occur in the synchronous memory space. In applications which require substantial amounts of main memory, this memory space will be implemented as instruction and data caches.

The synchronous memory is designed to be able to supply both an instruction and data word to the processor on each clock cycle. When the synchronous memory spaces are used as caches, then they are used to hold instruction and data that is repetitively accessed by the CPU (for example, within a program loop). This reduces the number of slower asynchronous memory cycles and thus achieves higher performance.

Some microprocessors incorporate small amounts of cache on-chip, which has a very small and unpredictable effect on the execution of large programs. The IDT79R3001 supports

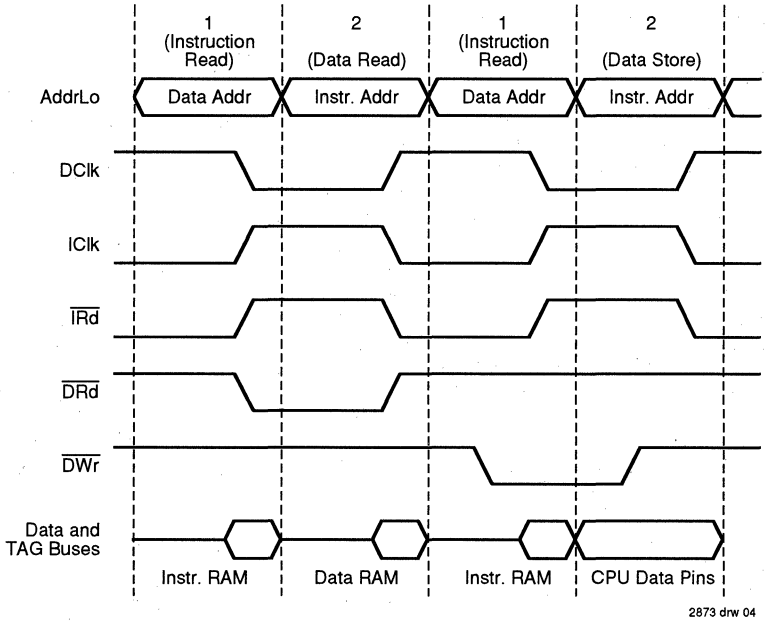

Figure 4. Synchronous Memory Control Timing

caches of from 8kB in size up through 16MB, thus bringing substantial performance improvements to very large programs and also allowing real-time system designers to design cache-based systems to support deterministic requirements.

The IDT79R3001 directly controls the synchronous memory interface (whether it is being used as caches or not) with a minimum of external components. The IDT79R3001 includes all control signals and cache TAG control logic (for a direct mapped cache) for the synchronous memory interfaces. Parity over the data portion of each synchronous memory can be optionally selected at RESET time for applications which desire to make this cost trade-off.

The synchronous interface works by dividing the basic CPU cycles into two phases. During one phase, a cache address is presented by the processor and captured by external latches (the latch control signals are directly generated by the CPU). During the next phase, the address for the other memory space is generated and captured while the data movement operation or the first cache is completed. The processor directly generates the SRAM Output Enable and Write Enable signals and the address latch enable signals, requiring no external decoding. This is illustrated in Figure 4.

Further, the IDT79R3001 supports the ability to refill multiple words into the cache from main memory when a cache-

miss occurs, further reducing system cost and increasing performance in cache-based systems. The IDT79R3001 can obtain 1, 4, 8, 16, or 32 words from main memory when processing a cache-miss, thus amortizing the cache-miss penalty over a large amount of data.

The IDT79R3001 also performs instruction streaming, which is the simultaneous execution of incoming instructions while the cache is being refilled.

The actual width of the tag bus, and whether or not parity over the data parts of each synchronous memory is included, is determined according to how the device is initialized. The IDT79R3001 can accommodate a TAG bus width of 0-19 bits, compatible with a variety of cache sizes and cacheable main memory choices. The IDT79R3001 allows the system designer to scale the synchronous memory system exactly according to the system needs, thus eliminating extra memory and logic devices and achieving substantial cost savings with no loss of performance.

Thus, the synchronous memory interface of the IDT79R3001 allows for high-bandwidth memory systems to be implemented with a minimum of control logic. This is desirable, since RISC performance tends to be a function of memory bandwidth. By simplifying the design of the synchronous memory system (illustrated in Figure 5), it is easier for the system designer to achieve high performance with minimum chip count and without requiring ultra-fast or specialty components.

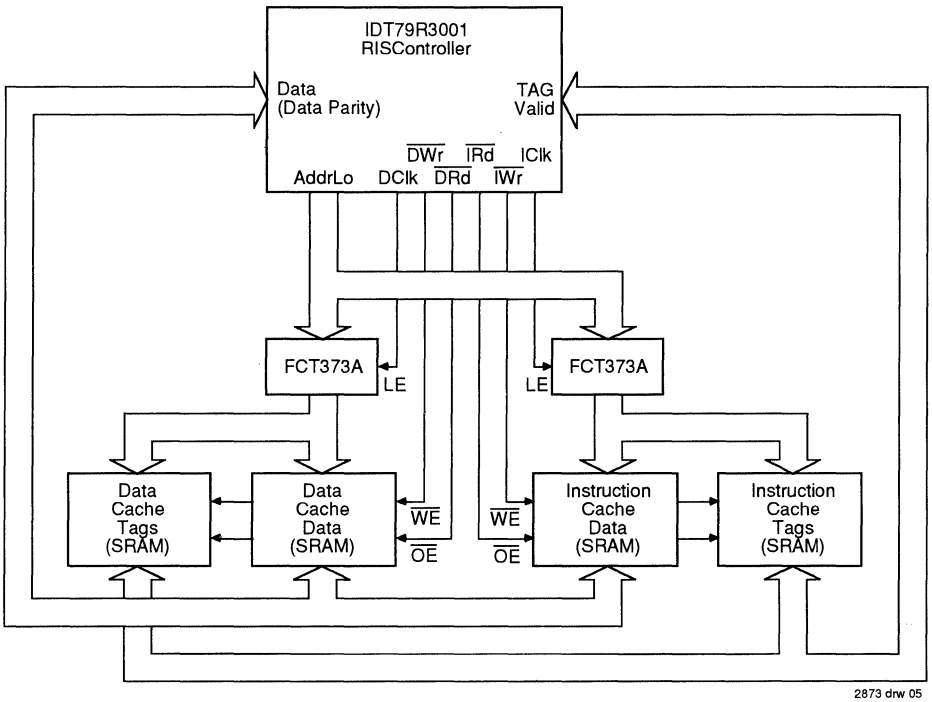

Figure 5. IDT79R3001 Synchronous Interface

The TAG Bus

The TAG bus of the IDT79R3001 has been designed to allow the system designer to implement the exact cache configuration that is right for the system. For larger caches, low-order TAG bits do not need to be supplied for the TAG comparison. Additionally, the number of high-order TAG bits supplied is determined by the system designer, according to the amount of cacheable main memory the system supports. Since most embedded systems would tend to implement caches of 16kB and greater, and cacheable memory spaces of 32MB or smaller, significant cost and area reductions are achieved by configuring a smaller TAG bus.

The system configures the on-chip TAG comparator at RESET Initialization time. If a TAG bit is not to be included in the synchronous memory TAG bit compare, a pull-down resistor of 4kΩ is connected to the appropriate IDT79R3001 TAG pin. If a TAG bit is to be included, no resistor is required (the IDT79R3001 pulls floating inputs to Vcc during RESET by a small pull-up, which is disabled when RESET is negated).

If a TAG bit is excluded from the cycle-by-cycle comparison, it is still driven out with the appropriate address value during write cycles or asynchronous memory reads. Thus, the system designer still has the full 4GB of address space available for address decoding, without requiring the synchronous memory to be able to cache all such addresses.

Figure 6 illustrates a reduced system, which implements 16kB of Instruction and 16kB of data cache, and 512MB of cacheable address space, using just 6 IDT71586 4kx16 Latched CacheRAM™ components and 4 pull-down resistors.

Note that in systems which do not implement the synchronous memory space as cache, then pull-down resistors would be added to all TAG pins. The Valid Pin still needs to be supplied on each cycle, thus allowing various memory schemes to be implemented (such as static column DRAM). However, the IDT79R3001 can be initialized to not assert the Valid pin as an output during Write cycles, simplifying the design of logic to drive the signal.

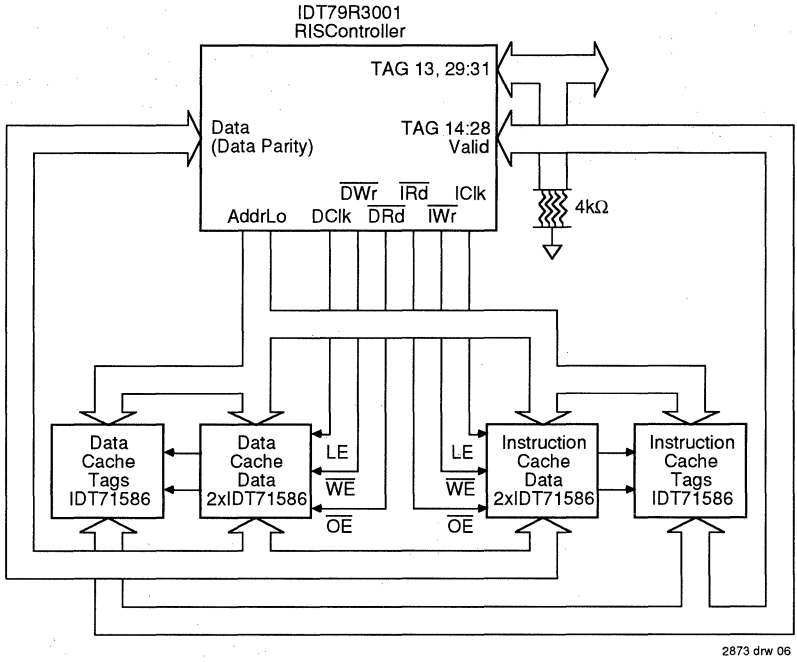

Figure 6. Small Footprint Cache for IDT79R3001

Cache Update

When the on-chip TAG comparator indicates that the item read from the cache was not the desired item, a cache-miss is processed. A main memory (asynchronous) transfer is automatically processed.

The IDT79R3001 desires to update the cache using a burst refill of multiple adjacent words from main memory. The processor is "stalled" until the first word of the block is available. The processor is then released, and the block of words is brought into the cache at the rate of one word per CPU clock cycle.

Note that if the cache-miss was in the instruction cache, the processor is capable of simultaneously executing the incoming instruction stream as the cache is updated, thus effectively making the cache update transparent to the system and increasing performance.

Write Cycles

The IDT79R3001 utilizes a write through cache. That is, data written by the processor is both written to the cache and main memory simultaneously. Thus, main memory always has a current copy of all data.

Typically, latching devices are used between the cache subsystem and the slower main memory. These Write Buffers capture the data simultaneous with the cache update, allowing the processor to continue to the next cycle without actually waiting for the main memory transfer to complete. The IDT79R3001 generates parity over the data field on write cycles, which can be propagated into both the synchronous and asynchronous memory spaces.

When the processor writes less than a 32-bit quantity (a "partial" word), the processor can perform a "read-modify-write" of the cache. That is, the processor will read the 32-bit word containing the partial address(es) to be updated from the cache. If a "hit" occurs, then the new data will be merged with the old and the new 32-bit value will be written both to the cache and to main memory. If a cache "miss" occurs, then only the partial data is written to main memory and the cache is unchanged. Partial word capability is selected as a RESET option.

THE ASYNCHRONOUS MEMORY INTERFACE

The IDT79R3001 also supports an asynchronous memory interface, which supports the use of slower memory devices such as slow DRAM or EPROM and also supports the use of peripherals and other "non-cacheable" devices.

In general, if a cache-miss (or parity error, if enabled) occurs, the processor will automatically use the asynchronous memory interface to retrieve the desired data, and will update the cache accordingly.

Additionally, software can force the use of the asynchronous memory space through the use of the on-chip MMU. When the processor seeks either instructions or data within a certain address range (kseg1), the processor knows that this data is uncacheable and will perform an asynchronous memory transfer. Additionally, within cacheable memory, TLB entries can be used to make certain pages as "uncacheable". When an address of an "uncacheable" page is used, the processor will automatically use the asynchronous memory space.

The asynchronous memory space uses the same data bus as the synchronous memory space. This facilitates the automatic updating of cache memory when the asynchronous memory is accessed due to cache-miss activity or memory writes. The asynchronous address bus is composed from the synchronous memory AddrLo bus, and the TAG bus. External logic devices (such as IDT74FCT374A registers) are used to capture AddrLo and TAG values for the asynchronous transfer address. Note that systems which exclude individual TAG bits from comparison (to reduce cache width) still have all TAGs available as outputs.

The data path between the processor and the asynchronous memory space is managed according to the needs of the application. Write Buffer FIFO devices, such as the IDT79R3020, are used to capture address and data during store cycles. These devices are used to capture the data in one-cycle, and allow the processor to continue to execute from the synchronous memory while the slower asynchronous memory actual retires the write.

The read path is also constructed according to the needs of the system. If block refill is used, then the read path is highly dependent on the design of the main memory system. Pipeline devices such as IDT74FCT540A, or simple latches such as IDT74FCT374, may be used.

A simple asynchronous memory interface is shown in Figure 7. In this system, main memory is assumed to be fast enough to support the block refill requirements of the system, thus simplifying the read path. In fact, both the read and write data paths are actually managed through a single set of IDT29FCT52A bidirectional latching transceivers.

During write cycles (which are typically captured by Write Buffers), the processor asserts $\overline{\text{MemWr}}$ to indicate that a write cycle is in progress. The memory system negates WrBusy to indicate that the processor is done with the write cycle.

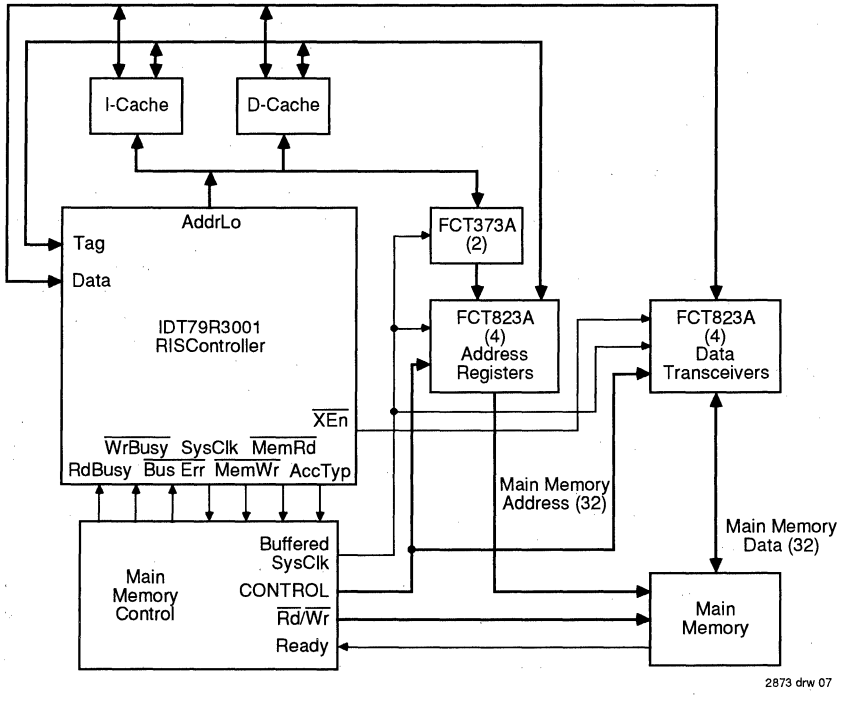

Figure 7. IDT79R3001 Asynchronous Interface

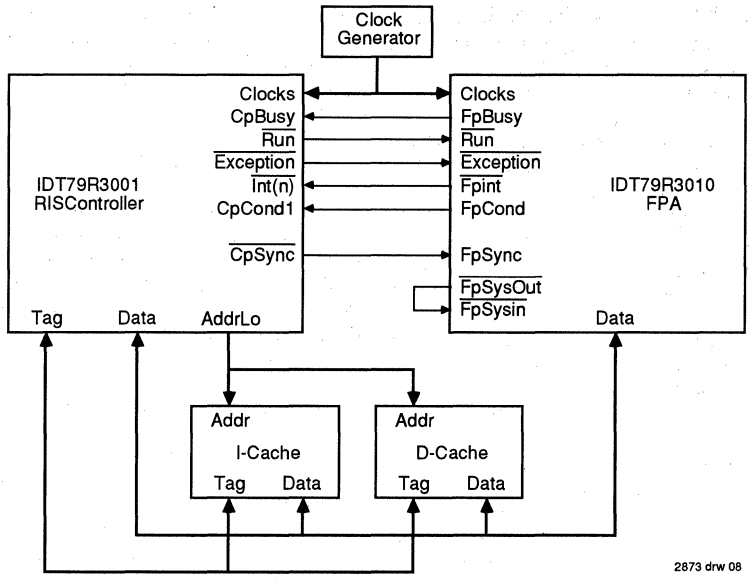

Figure 8. IDT79R3001 Interface to IDT79R3010 Floating Point Co-Processor

During read cycles, the processor will assert $\overline{\text{MemRd}}$ to indicate that a main memory read is in progress. The memory system will hold RdBusy active until the desired data is available. The processor will activate the $\overline{\text{XEn}}$ signal to allow data to be passed from the main memory to the processor databus. If the cache is to be updated with the new data, then the processor will assert the appropriate cache write signal to allow the cache RAMs to capture the incoming databus.

The AccTyp bus is used to indicate the size of the data transfer (8-, 16-, 24-, or 32-bits), and for main memory reads, whether or not the data is "cacheable". This simplifies the main memory address decoding, since the AccTyp indicates whether the main memory needs to perform a burst read of multiple words.

Co-Processor Interface

The IDT79R3001 implements a co-processor interface, which allows the use of the IDT79R3010 high-performance RISC Floating Point Accelerator without requiring the use of external interface components.

The co-processor interface has been designed to make system co-processors appear to the programmer as if they were on-chip extensions of the core execution engine. Thus, the IDT79R3010 FPA works as a true co-processor, rather than as a peripheral which must be programmed.

In the IDT79R3001 co-processor model, the CPU is responsible for controlling all data cycles. The co-processor keeps in synchronization with the CPU (including the pipeline stages), and uses a Phase-Locked Loop to keep synchronized with the processor bus traffic. The co-processor then "snoops" the data bus, watching for co-processor instructions. It also knows when data cycles on the bus are intended for it (either as a target in co-processor load operations, or as a source for co-processor restore operations), and performs the data portion of the operation when appropriate. Thus, co-processors effectively load and store directly with memory, without requiring operands to go through the CPU first. This achieves the highest levels of performance (note that the co-processor interface also supports move, whereby data can be moved directly between the CPU and any co-processor).

Figure 8 illustrates the use of the IDT79R3010 in a IDT79R3001 system. The co-processor interface manages synchronization between the parts, and is used to communicate status from the co-processor to the CPU. CpBusy, or Co-processor Busy, stalls the CPU until the busy co-processor resource (requested by a co-processor instruction) is free, and CpCond, or Co-processor Condition, is used to report status on co-processor test instructions. CpSync, is used to help the co-processor stay "locked" to the CPU, so that the co-processor knows when data is on the bus to be sampled on load operations, or when to place data on the bus for store operations.

Note that the co-processor sits on the same data bus as the CPU, but has no connection to the address bus. The CPU is responsible for performing all memory addressing, including the determination of "cache hit", write-buffer full cycles, and any processing that might be required for cache misses.

INTERRUPTS

The IDT79R3001 features 6 separate interrupt input pins. Interrupts are not vectored, but rather cause the general exception vector address to be the next execution address.

These pins are not encoded internally; external logic can choose to implement these interrupt lines as either 6 or 64 interrupt sources; software would then perform the appropriate decoding to get to the specific interrupt handler.

Interrupts are recognized in the ALU stage of the on-chip pipeline. Instructions less advanced in the pipeline are "flushed" and will be restarted when the return from exception occurs (an on-chip register contains the address of the instruction which was excepted). Instructions further advanced in the pipeline are allowed to continue. Unlike other RISC processors, the IDT79R3001 does not require the programmer to save and restore pipeline status to allow normal execution to be resumed. Depending on the application and exception, at most software would need to save/restore the on-chip data registers, status register, Exception PC and exception "cause" register.

Note that the co-processor model includes "precise exceptions." That is, an exception is signaled to the exact instruction which generated the exceptional condition. No further state commitments are made by the IDT79R3001 and, thus, the exact context at the time of the exception is known to the programmer. This is true even for multi-cycle operations, such as those of the FPA.

DMA INTERFACE

The IDT79R3001 features a simple DMA interface which allows an external master to gain control of the synchronous memory space. Note that it is not necessary to include logic on the CPU to arbitrate for the asynchronous memory space; the read/write buffer interface is where such arbitration logic belongs and it is left to the system designer to implement the type of asynchronous memory structure that best fits the application.

When an external master "owns" the synchronous bus, the CPU will tri-state the following pins and buses:

- **AddrLo:** The synchronous memory direct address bus.
- **Data & Tag:** The synchronous memory RAM data lines.
- **Cache Control:** $\overline{IRd}$, $\overline{IWr}$, IClk, $\overline{DRd}$, $\overline{DWr}$ and DClk. This allows the external master to use the existing control lines to control the synchronous memory.
- **XEn:** The read buffer transceiver enable, which will allow the external master to use the read/write buffer path for DMA.
- **Valid:** This enables the DMA interface to be used for multi-processing applications.

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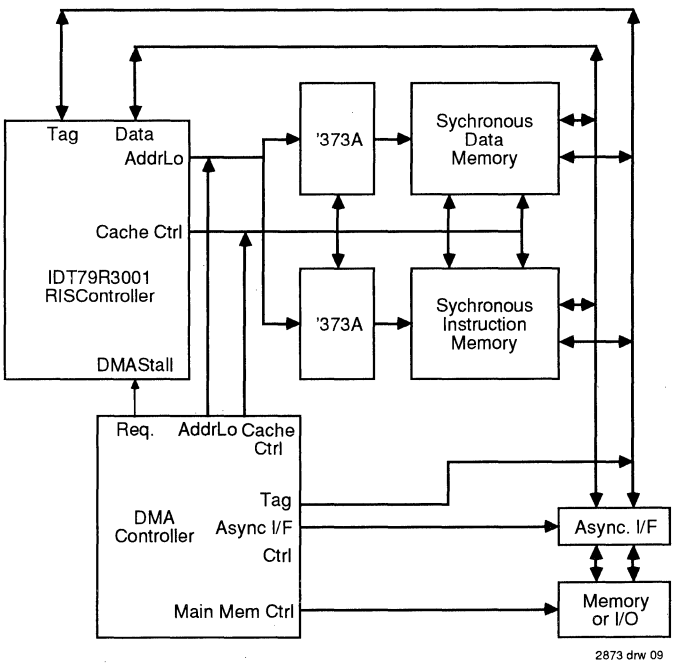

Figure 9. IDT79R3001 DMA Interface

MODE SELECTABLE FEATURES FOR THE IDT79R3001

Input	W Cycle	X Cycle	Y Cycle	Z Cycle
$\overline{Int0}$	Reserved	Reserved	Reserved	Reserved
$\overline{Int1}$	Reserved	Reserved	Reserved	Reserved
$\overline{Int2}$	$\overline{DBlkSize0}$	$\overline{DBlkSize1}$	$\overline{Parity\ On}$	Valid Output
$\overline{Int3}$	$\overline{IBlkSize0}$	$\overline{IBlkSize1}$	StorePartial	ControlLow
$\overline{Int4}$	$\overline{PllOn}$	$\overline{PllOn}$	$\overline{PllOn}$	$\overline{PllOn}$
$\overline{Int5}$	Reserved	BigEndian	$\overline{TriState}$	Reserved

NOTE:
1. Reserved signals must be "HIGH" during these cycles.

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The DMA interface consists of a single input signal, DMAStall, which causes the processor to stall and to tri-state the above named lines. The external master is guaranteed mastership of the bus within a very short number of cycles, depending on the exact external bus activity of the CPU when the DMA was requested. The DMA master negates the DMAStall signal when the DMA operation is completed to allow the CPU to resume processing. Consult the *IDT79R3001 Hardware User's Guide* for more details.

Figure 9 illustrates the system connection of an external DMA master to a IDT79R3001 system.

ADVANCED FEATURES

The IDT79R3001 contains special features which provide added flexibility across a number of applications, as well as allow for system diagnostic support.

In support of diagnostics, the IDT79R3001 allows for cache "swapping" (interchange of which memory bank is for instruction and which is for data), which is useful in system initialization, cache flushing, and diagnostics. Additionally, the caches can be "isolated" from main memory, which forces cache "hits" to occur regardless of the tag comparison, and which is useful in determining that the synchronous memory space RAMs are functional.

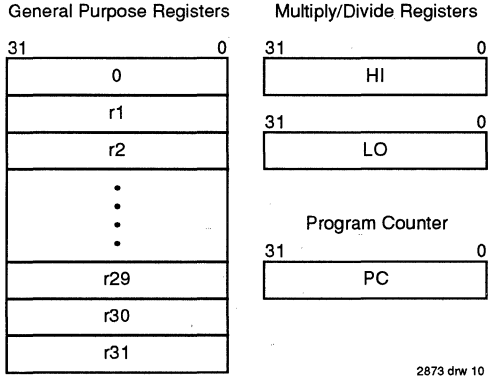

Figure 10. IDT79R3001 Registers

An additional feature is the ability to enable parity checking over the data field of each synchronous memory. If parity is enabled, the processor will check the parity when a synchronous access occurs; if a parity error is detected, it is signaled to the external world on the $\overline{Parity\ Error}$ signal and a cache-miss cycle is processed. the $\overline{Parity\ Error}$ signal will remain low until the parity error flag in the CP0 status register is cleared by software.

A number of other system selectable features are selected at reset time. The input reset "vectors" are sampled on the interrupt input lines during the last four cycles of the reset period. The input vectors are listed in Table 1. These selections include the ability to select the block refill sizes for each of the instruction and data memories, whether Big Endian or Little Endian order is to be used, whether to use data parity, and whether or not to accommodate a Phase-Locked Loop for a co-processor. The initialization of the CPU and meaning of each input vector is more fully explained in the *IDT79R3001 Hardware User's Guide*.

PROCESSOR ARCHITECTURE

The IDT79R3001 is a full implementation of the IDT79R2000A/IDT79R3000 Instruction Set Architecture (the MIPS-I ISA). This architecture is discussed in great detail in *MIPS RISC Architecture*, available from IDT.

IDT79R3001 CPU Registers

The IDT79R3001 CPU provides 32 general purpose (orthogonal) 32-bit registers, a 32-bit Program Counter and two 32-bit registers used to hold the results of the CPU integer multiply and divide operations.

Two of the 32 general registers have special purposes designed to increase processor performance: register r0 is hardwired to the value "0", a useful constant; and register r31 is used as the link register in jump-and-link instructions (the return address for subroutine calls). Otherwise, there is no requirement that a particular register be used as a stack or frame pointer, etc., although there is a register convention as part of the "mips ABI" (Applications Binary Interface standard) which the compiler suite uses.

The CPU registers are illustrated in Figure 10. Note that there is no Program Status Word register shown in this figure. The functions traditionally provided by a PSW register are instead provided in the Status and Cause Registers incorporated within the on-chip System Control Co-Processor (CP0). The instruction set does not use condition codes.

Instruction Set Overview

All IDT79R3001 instructions are 32 bits long and there are only three instruction formats (see Figure 11). This approach simplifies decoding, thus minimizing instruction execution time. The IDT79R3001 processor initiates a new instruction on every RUN cycle, and is able to complete an instruction on almost every clock cycle. The only exceptions are the LOAD instructions and BRANCH instructions, which each have a single cycle of latency associated with their execution (that is, the instruction immediately after the branch is always executed regardless of the branch condition; similarly, the data loaded by a LOAD instruction is not available to the subsequent instruction). However, in the majority of cases the compilers (and even the MIPS assembler) are able to reorder instructions to fill these latency cycles with useful instructions which do not require the results of the previous instruction (in the worst case, a NOP instruction is inserted). This effectively eliminates these latency effects and does not require the applications programmer to be aware of the pipeline structure.

The actual instruction set of the CPU was determined after extensive simulations to determine which instructions should be implemented in hardware and which operations are best synthesized in software from other basic operations. This methodology has resulted in the highest performance processor available.

The IDT79R3001 instruction set can be divided into the following groups:

- **Load/Store Instructions** move data between memory and the general registers. These are all "I-Type" instructions. The only addressing mode supported is base register plus signed, immediate 16-bit offset. This effectively allows three addressing modes: register plus offset, register (using zero offset), and immediate (using r0,the zero register).

  The Load instruction has a single cycle of latency, as described above. That is, the instruction immediately after the load instruction cannot rely on the new data; however, the assembler and compilers automatically handle this, reordering code to insure that no conflicts occur. Note that the store operation has no latency in its effect.

  Loads and stores can be performed on byte, half-word, word, or unaligned word data (32-bit data not aligned on a modulo-4 address).
- **Computational Instructions** perform arithmetic, logical, and shift operations on values in registers. They occur in both "R-Type" (both operands and the result are general registers), and "I-Type" (one operand is a 16-bit immediate value) formats.

  Note that computational instructions are three operand instructions: that is, the result register can be different from both source registers. This means that operands need not be overwritten by arithmetic operations. This results in a more efficient use of the register set, and further increases performance.

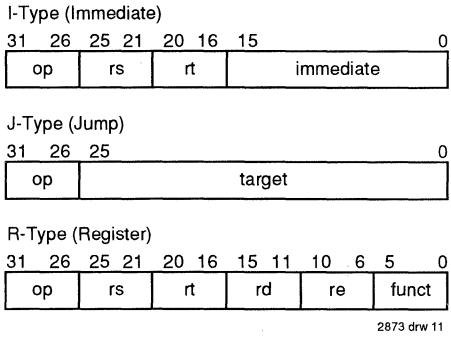

Figure 11. IDT79R3001 Instruction Formats

- **Jump and Branch Instructions** change the flow of control of a program. Jumps are always to a paged absolute address formed by combining a 26-bit target with four bits of the Program Counter ("J-Type" format for subroutine calls), or 32-bit register byte addresses ("R-Type," for Returns and dispatches). Branches have 16-bit offsets relative to the program counter ("I-Type").

  Jump and Link instructions save a return address in Register 31. The IDT79R3001 instruction set features numerous branch conditions. Included is the ability to branch based on a comparison of two registers, or on the comparison of a register to zero. Thus, net performance is increased since the processor does not have to precede the branch instruction with arithmetic operations.
- **Co-processor Instructions** perform operations in the co-processors (such as the IDT79R3010 FPA). Co-processor Loads and Stores are "I- Type;" computational instructions have co-processor dependent formats.
- **Co-processor 0 Instructions** perform operations on the System Control Co-processor (CP0) registers to manipulate the memory management and exception handling facilities of the on-chip co-processor.
- **Special Instructions** perform a variety of tasks, including movement of data between general and special registers, system calls, and breakpoint operations. These are always "R-Type."

IDT79R3001 System Control Co-processor (CP0)

The IDT79R3001 can operate with up to four tightly coupled co-processors, designated CP0-CP3. CP0 is included on-chip as co-processor 0, the System Control co-processor. CP0 is responsible for supporting both the virtual memory system and the exception handling functions of the IDT79R3001.

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IDT79R3001 INSTRUCTION SUMMARY

OP	Description	OP	Description
	Load/Store Instructions		**Multiply/Divide Instructions**
LB	Load Byte	MULT	Multiply
LBU	Load Byte Unsigned	MULTU	Multiply Unsigned
LH	Load Halfword	DIV	Divide
LHU	Load Halfword Unsigned	DIVU	Divide Unsigned
LW	Load Word	MFHI	Move From HI
LWL	Load Word Left	MTHI	Move To HI
LWR	Load Word Right	MFLO	Move From LO
SB	Store Byte	MTLO	Move To LO
SH	Store Halfword		
SW	Store Word		**Jump and Branch Instructions**
SWL	Store Word Left	J	Jump
SWR	Store Word Right	JAL	Jump and Link
		JR	Jump to Register
	Arithmetic Instructions	JALR	Jump and Link Register
	(ALU Immediate)	BEQ	Branch on Equal
ADDI	Add Immediate	BNE	Branch on Not Equal
ADDIU	Add Immediate Unsigned	BLEZ	Branch on Less than or Equal to Zero
SLTI	Set on Less Than Immediate	BGTZ	Branch on Greater Than Zero
SLTIU	Set on Less Than Immediate Unsigned	BLTZ	Branch on Less Than Zero
		BGEZ	Branch on Greater than or Equal to Zero
ANDI	AND Immediate		
ORI	OR Immediate	BLTZAL	Branch on Less Than Zero and Link
XORI	Exclusive OR Immediate	BGEZAL	Branch on Greater than or Equal to Zero and Link
LUI	Load Upper Immediate		
			Special Instructions
	Arithmetic Instructions	SYSCALL	System Call
	(3-operand, register-type)	BREAK	Break
ADD	Add		
ADDU	Add Unsigned		**Coprocessor Instructions**
SUB	Subtract	LWCz	Load Word from Coprocessor
SUBU	Subtract Unsigned	SWCz	Store Word to Coprocessor
SLT	Set on Less Than	MTCz	Move To Coprocessor
		MFCz	Move From Coprocessor
SLTU	Set on Less Than Unsigned	CTCz	Move Control to Coprocessor
AND	AND	CFCz	Move Control From Coprocessor
OR	OR	COPz	Coprocessor Operation
XOR	Exclusive OR	BCzT	Branch on Coprocessor z True
NOR	NOR	BCzF	Branch on Coprocessor z False
	Shift Instructions		**System Control Coprocessor**
SLL	Shift Left Logical		**(CP0) Instructions**
SRL	Shift Right Logical	MTC0	Move To CP0
SRA	Shift Right Arithmetic	MFC0	Move From CP0
SLLV	Shift Left Logical Variable	TLBR	Read indexed TLB entry
SRLV	Shift Right Logical Variable	TLBWI	Write Indexed TLB entry
SRAV	Shift Right Arithmetic Variable	TLBWR	Write Random TLB entry
		TLBP	Probe TLB for matching entry
		RFE	Restore From Exception

2873 tbl 02

CP0 Registers

As a co-processor, CP0 has a number of registers which it uses to perform its control functions. These include 64 fully associative Translation Lookaside Buffers (TLBs), used to manage the virtual memory space; registers to manage the TLB set; and the exception handling registers. Figure 12 illustrates the register set of the System Control Co-processor. Table 3 provides a brief explanation of the function of each of these registers. A more detailed explanation of the use of each of these registers is included in the *MIPS RISC Architecture* manual.

Memory Management System

The IDT79R3001 supports a virtual memory system, so that each task in a given application can be unaware of the addressing needs of other tasks. This is also useful in systems with limited physical memory; the IDT79R3001 provides for the logical expansion of memory by translating addresses composed in a large virtual space into available physical memory addresses.

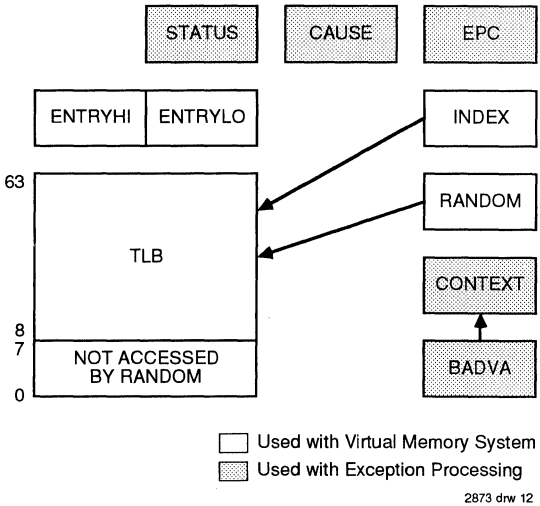

Figure 12. The System Control Co-processor (CP0) Registers

CP0 REGISTERS

Register	Description
EntryHi	High half of a TLB entry
EntryLo	Low half of a TLB entry
Index	Programmable pointer into TLB array
Random	Pseudo-random pointer into TLB array
Status	Mode, interrupt enables and diagnostic status information
Cause	Indicates nature of last exception
EPC	Exception Program Counter—contains address of instruction which detected the exception
Context	Pointer into kernel's virtual Page Table Entry array
BadVA	Most recent bad virtual address
PrID	Processor revision identification (Read only)

2873 tbl 03

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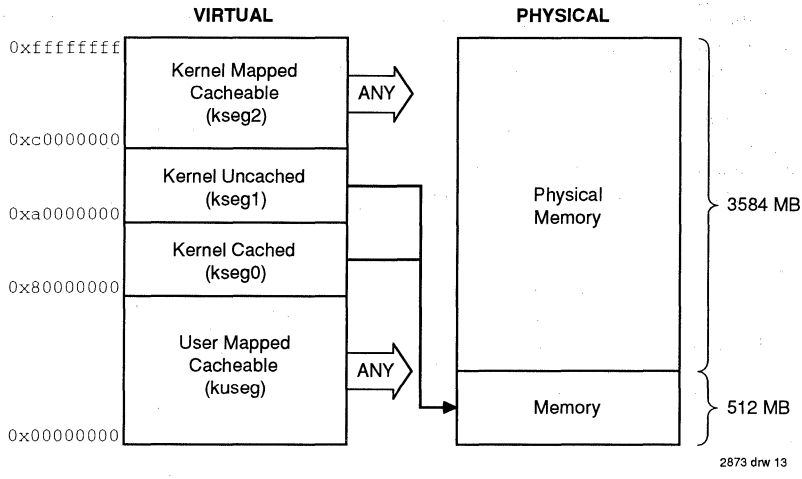
MMU ADDRESS TRANSLATION



IDT79R3001 Operating Modes

The IDT79R3001 has two operating modes: User Mode and Kernel Mode. The IDT79R3001 normally operates in the User Mode until an exception is detected, forcing it into the Kernel Mode. The processor remains in Kernel Mode until the exceptions are handled and the processor executes an RFE (Return from Exception) instruction, which will restore it to User Mode. Kernel Mode allows software to alter machine state information such as that contained in the CP0 registers; that is, if in User Mode an access is attempted to Co-processor 0 and the Kernel has not enabled the User to access the co-processor, an exception will occur. Similarly, if a User task attempts to use a Kernel virtual address, an exception will occur. Thus, system resources are protected from User tasks.

The manner in which memory addresses are translated (mapped) depends on the operating mode of the IDT79R3001 and on the virtual address desired. Figure 13 illustrates the virtual address mapping performed by the IDT79R3001:

User Mode — in this mode, a single, uniform virtual address space (kuseg) of 2GB is available to each user task (tasks are further identified by a 6-bit process identifier field in order to form unique virtual addresses). All references to this segment are mapped using the TLB, which utilizes both the virtual address and the Process ID field to perform the virtual-to-physical mapping (note that this allows the cache to be shared by up to 64 User processes at a time without requiring time consuming Cache or TLB flushing).

Kernel Mode—Four separate segments are accessible through this mode:

- **kuseg**—When in the Kernel Mode, references to this segment are treated just like User Mode references, thus streamlining Kernel accesses to User memory.
- **kseg0**—References to this 512MB segment may use the cache memory, but are not translated by the TLB. Instead, these addresses map directly to the first 512MB of the physical address space. Note that many dedicated embedded applications will utilize this address space and kseg1 only, rather than any of the TLB mapped segments.
- **kseg1**—References to this 512MB segment are not mapped through the TLB. Additionally, this memory is viewed as uncacheable, which means that references through this segment will always use the asynchronous memory interface. As with kseg0, references through this segment are hard-mapped to the first 512MB of physical memory. When

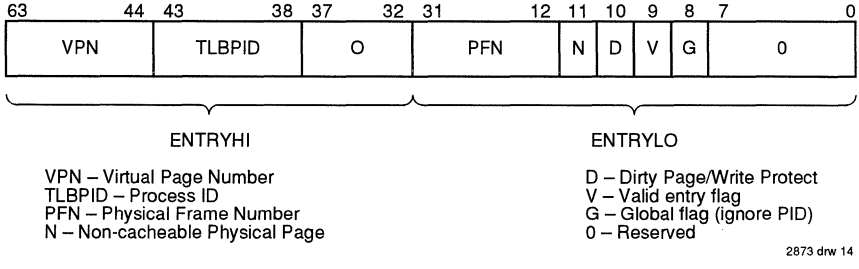


Figure 14. TLB Entry Format

the processor boots, the reset vector is contained in this segment, so that the processor does not require either the cache or the TLB to be valid at RESET time.

- **kseg2**—References to this 1GB segment are always mapped through the TLB. As with kuseg, the ability of memory pages to be cached is determined by a bit setting in the TLB entry for that page.

The Translation Lookaside Buffer (TLB)

The translation of virtual addresses in either kuseg or kseg2 (mapped segments) is performed by the on-chip Translation Lookaside Buffer array. This array consists of 64 fully-associative (content addressable) memory elements. Each entry maps a 4kB virtual page to a 4kB physical page. Each TLB entry contains other information about the virtual address it maps (such as which User process it maps) and also about the physical address (such as whether it is cacheable or writeable).

Figure 14 illustrates the format of each TLB entry. The translation operation is illustrated in Figure 15. The upper portion of the desired virtual address is compared against the VPN field of each TLB entry. Additionally, the current process ID (contained in the TLBHI register) is matched against the PID field of the TLB entry (if the TLB entry is marked as Global, the PID comparison is ignored). If a match occurs, and the TLB entry is marked as Valid, then the translation is completed by replacing the VPN of the virtual address with the corresponding PFN (Physical Frame Number).

Note that the use of the TLB does not incur an execution penalty, since the execution engine pipeline includes stages to cover for the time required to make the TLB search and translation.

TLB misses occur when no successful match occurs. These events are handled in software. The CP0 registers give the software enough information to obtain the appropriate TLB entry at speeds which exceed those achieved by many CPUs which use hardware TLB replacement (10-12 cycles under UNIX).

When a TLB miss occurs, the address of the instruction which was executing is stored in the EPC register, and the BadVA register contains the address which was being translated. The Context register uses the BadVA value to generate a direct pointer to the kernel Page Table Entry for the desired virtual address. The Random register suggests the TLB entry to be replaced by the new entry. Note that the lower eight TLB entries are not pointed to by Random; the kernel software can thus insure that it is constantly mapped, and deterministic response is guaranteed.

BACKWARD COMPATIBILITY WITH IDT79R2000A AND 79R3000 PROCESSORS

The IDT79R3001 can execute the same binary software (either kernel or user) that is executed by either the IDT79R2000A or IDT79R3000. At the system level, some hardware re-design is necessary to achieve the cost savings inherent in the IDT79R3001 hardware interface.

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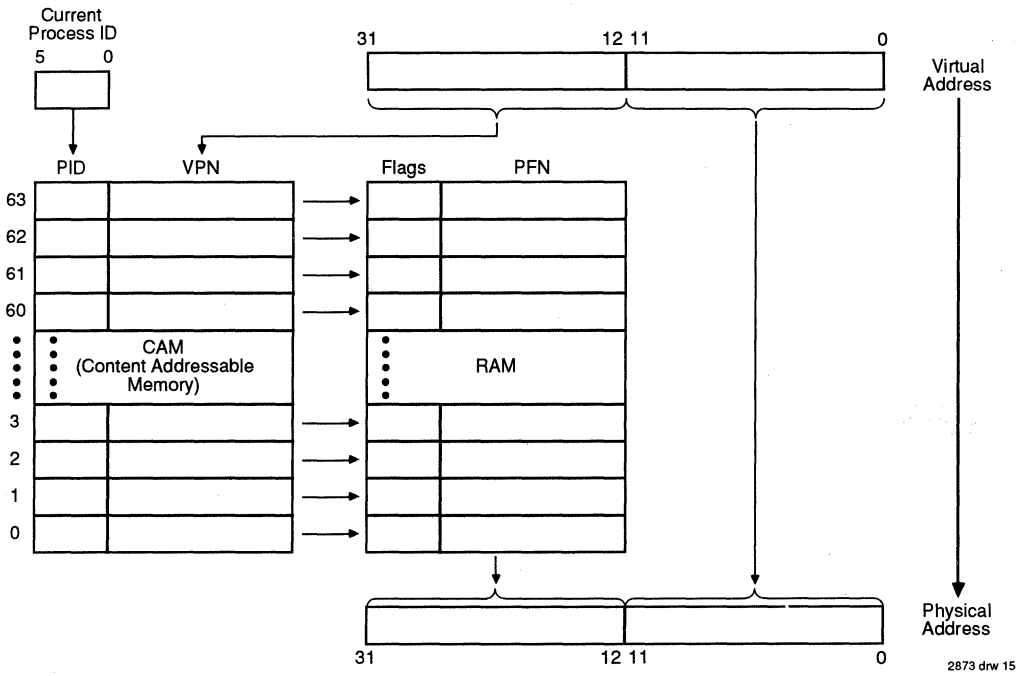


Figure 15. Virtual to Physical TLB Translation

PIN DESCRIPTIONS

Pin Name	I/O	Description
Memory Interface		
Data (0:31)	I/O	A 32-bit bus used for all instruction and data transmission among the processor, synchronous memory space, asynchronous memory space and co-processors.
DataP (0:3)	I/O	A 4-bit bus containing even parity over the data bus. If parity checking is enabled, a parity error will cause the $\overline{PErr}$ signal to be asserted and a cache-miss to occur. Regardless of whether parity checking is enabled, the processor will always generate parity on writes.
Tag (13:31)	I/O	A 19-bit bus used for transferring cache tags and high-order address bits between the processor, caches and asynchronous memory spaces.
AddrLo (0:23)	O	A 24-bit bus containing low-order byte addresses for both the synchronous (cache) and asynchronous memory spaces.
Synchronous Memory Control		
$\overline{IRd}$	O	The output enable for the instruction cache. The polarity of this signal is selectable.
$\overline{IWr}$	O	The write enable for the instruction cache. The polarity of this signal is selectable.
IClk	O	The instruction cache address latch clock. The clock runs continuously.
$\overline{DRd}$	O	The output enable for the data cache. The polarity of this signal is selectable.
$\overline{DWr}$	O	The write enable for the data cache. The polarity of this signal is selectable.
DClk	O	The data cache address latch clock. The clock runs continuously.
Valid	I/O	A high on this signal indicates that the Tags just read from the cache are valid. When a cache update occurs, the processor will generate the appropriate Valid bit.
$\overline{PErr}$	O	If parity checking is enabled, this signal is an active low output of the internal CP0 parity error status bit. It is driven low when a parity error is detected and remains low until software clears the parity error flag in the status register. This pin is physically the same pin as AccTyp2. Its function is selected during device reset.
Asynchronous Memory Interface		
$\overline{XEn}$	O	The transceiver enable for the read buffer.
AccTyp (0:2)	O	A 3-bit bus used to indicate the size of data being transferred on the asynchronous memory bus, whether or not a data transfer is occurring and the purpose of the transfer. If parity checking is enabled, AccTyp2 becomes the $\overline{PErr}$ signal.
$\overline{MemWr}$	O	Signals the occurrence of an asynchronous memory write cycle.
$\overline{MemRd}$	O	Signals the occurrence of an asynchronous memory read cycle.
$\overline{BusError}$	I	Signals the occurrence of a bus error during an asynchronous memory transfer cycle.
$\overline{Run}$	O	Indicates whether the processor is in a RUN or STALL state.
$\overline{Exception}$	O	Indicates the instruction about to commit processor state should be aborted and other exception related information.
$\overline{SysOut}$	O	A clock derived from the internal processor clock used to generate the system clock.
RdBusy	I	The asynchronous memory read stall termination signal. In most system designs, RdBusy is normally asserted and is deasserted only to indicate the successful completion of the memory read. RdBusy is sampled by the processor only during memory read stalls.
$\overline{WrBusy}$	I	The asynchronous memory write stall initiation/termination signal. $\overline{WrBusy}$ is only sampled during write operation.
Co-Processor Interface		
$\overline{CpSync}$	O	A clock which is identical to $\overline{SysOut}$ and used by co-processors for timing synchronization with the CPU.
CPBusy	I	The co-processor busy stall initiation/termination signal.
CpCond (0:3)	I	A 4-bit bus used to transfer conditional branch status from the co-processors to the CPU. CpCond(0) is used to control whether or not a cache burst refill occurs; the other signals are used as input port pins for co-processor branch instructions.
Processor Control Signals		
DMAStall	I	DMA Stall. Signals to the processor that it should stall accesses to the synchronous memories and tri-state the synchronous memory interface.
$\overline{Int}$ (0:5)	I	A 6-bit bus used to signal maskable interrupts to the CPU. A reset time, mode values are sampled from this bus to initialize the processor. During normal operation, these signals are not latched by the processor and must remain asserted until the processor acknowledges the interrupt (through software) to the interrupt source.
Clk2xSys	I	The master double frequency input clock, used to generate $\overline{SysOut}$.
Clk2xSmp/Rd	I	A double frequency clock input used to determine the sample point for data coming into the CPU and co-processors and used to determine the enable time of the synchronous memory RAMs.
Clk2xPhi	I	A double frequency clock input used to determine the position of the two internal phases.
$\overline{Reset}$	I	Initialization input used to force execution starting from the reset memory address. $\overline{Reset}$ should be asserted asynchronously but must be negated synchronously with the leading edge of $\overline{SysOut}$.

ABSOLUTE MAXIMUM RATINGS[1, 3]

Symbol	Rating	Commercial	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TA, TC	Operating Temperature	0 to +70[4] (Ambient) 0 to +90[5] (Case)	°C
TBIAS	Case Temperature Under Bias	–55 to +125[4] 0 to +90[5]	°C
TSTG	Storage Temperature	–55 to +125	°C
IIN	Input Voltage	–0.5 to +7.0	V

2873 tbl 05

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN} minimum = –3.0V for pulse width less than 15ns. V_{IN} should not exceed V_{CC} +0.5 Volts.
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.
4. 16-25 MHz only.
5. 40 MHz only.

AC TEST CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
VIH	Input HIGH Voltage	3.0	—	V
VIL	Input LOW Voltage	—	0.4	V
VIHS	Input HIGH Voltage	3.5	—	V
VILS	Input LOW Voltage	—	0.4	V

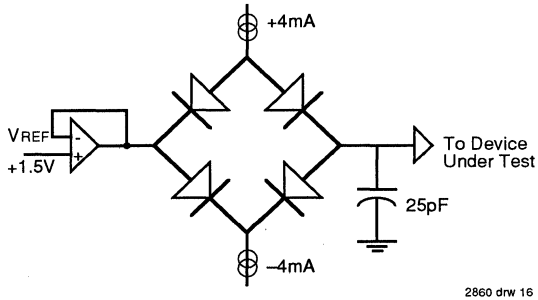
2873 tbl 06

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Commercial 16-33 MHz	0°C to +70°C (Ambient)	0V	5.0 ±5%
Commercial 40 MHz	0°C to +90°C (Case)	0V	5.0 ±5%

2873 tbl 07

OUTPUT LOADING FOR AC TESTING



2860 drw 16

Signal	CL
IRd, IWr, DRd, DWr	50pf
All Others	25pf

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DC ELECTRICAL CHARACTERISTICS
COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to +70°C, V_{CC} = +5.0V ±5%)

Symbol	Parameter	Test Conditions	16.67MHz		20.0MHz		25.0MHz		33.33MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4mA	3.5	—	3.5	—	3.5	—	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	—	0.4	—	0.4	—	0.4	—	0.4	V
V_{OHT}	Output HIGH Voltage(4,7)	V_{CC} = Min., I_{OH} = –8mA	2.4	—	2.4	—	2.4	—	2.4	—	V
V_{OHC}	Output HIGH Voltage(8)	V_{CC} = Min., I_{OH} =–4mA	4.0	—	4.0	—	4.0	—	4.0	—	V
V_{OLT}	Output LOW Voltage(4,7)	V_{CC} = Min., I_{OL} = 8mA	—	0.8	—	0.8	—	0.8	—	0.8	V
V_{IH}	Input HIGH Voltage(5)		2.0	—	2.0	—	2.0	—	2.0	—	V
V_{IL}	Input LOW Voltage		—	0.8	—	0.8	—	0.8	—	0.8	V
V_{IHS}	Input HIGH Voltage(2,5)		3.0	—	3.0	—	3.0	—	3.0	—	V
V_{ILS}	Input LOW Voltage(1,2)		—	0.4	—	0.4	—	0.4	—	0.4	V
I_{RESET}	Input HIGH Current(6)		10	100	10	100	10	100	10	100	µA
C_{IN}	Input Capacitance(7)		—	10	—	10	—	10	—	10	pF
C_{OUT}	Output Capacitance(7)		—	10	—	10	—	10	—	10	pF
I_{CC}	Operating Current	V_{CC} = Max.	—	575	—	650	—	750	—	800	mA
I_{IH}	Input HIGH Leakage(3)	V_{IH} = V_{CC}	—	100	—	100	—	100	—	100	µA
I_{IL}	Input LOW Leakage(3)	V_{IL} = GND	–100	—	–100	—	–100	—	–100	—	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	–100	100	–100	100	–100	100	–100	100	µA

2873 tbl 08

NOTES:
1. V_{IL} Min. = –3.0V for pulse width less than 15ns. VIL should not fall below –0.5V for larger periods.
2. V_{IHS} and V_{ILS} apply to Clk2xSys, Clk2xSmp/Rd, Clk2xPhi, CpBusy, and Reset.
3. These parameters do not apply to the clock inputs.
4. V_{OHT} and V_{OLT} apply to the bidirectional data and tag buses only. Note that V_{IH} and V_{IL} also apply to these signals. V_{OHT} and V_{OLT} are supplies as additional information to help the system designer understand the relationship between current drive and output voltage on these pins..
5. V_{IH} should not be held above V_{CC} + 0.5 volts.
6. The IDT79R3001 contains an internal pull-up/current source on the TAG pins to facilitate initialization. This current source is disconnected when Reset is inactive.
7. Guaranteed by design.
8. V_{OHC} applies to RUN and Exception.

DC ELECTRICAL CHARACTERISTICS
COMMERCIAL TEMPERATURE RANGE (T_C = 0°C to +90°C, V_{CC} = +5.0V ±5%)

Symbol	Parameter	Test Conditions	40.0MHz		Unit
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = -4mA	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	—	0.4	V
V_{OHC}	Output HIGH Voltage(7)	V_{CC} = Min., I_{OH} = -4mA	4.0	—	V
V_{OHT}	Output HIGH Voltage(4,6)	V_{CC} = Min., I_{OH} = -8mA	2.4	—	V
V_{OLT}	Output LOW Voltage(4,6)	V_{CC} = Min., I_{OL} = 8mA	—	0.8	V
V_{IH}	Input HIGH Voltage(5)		2.0	—	V
V_{IL}	Input LOW Voltage(1)		—	0.8	V
V_{IHS}	Input HIGH Voltage(2,5)		3.0	—	V
V_{ILS}	Input LOW Voltage(1,2)		—	–0.4	V
I_{RESET}	Input HIGH Current(6)		10	100	µA
C_{IN}	Input Capacitance(6)		—	10	pF
C_{OUT}	Output Capacitance(6)		—	10	pF
I_{CC}	Operating Current	V_{CC} = 5V, T_A = 70°C	—	850	mA
I_{IH}	Input HIGH Leakage(3)	V_{IH} = VCC	—	100	µA
I_{IL}	Input LOW Leakage(3)	V_{IL} = GND	–100	—	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = VCC, V_{OL} = GND	–100	100	µA

2873 tbl 09

NOTES:

1. V_{IL} Min. = –3.0V for pulse width less than 15ns. V_{IL} should not fall below –0.5 Volts for larger periods.
2. V_{IHS} and V_{ILS} apply to Clk2xSys, Clk2xSmp, Clk2xRd, Clk2xPhi, CpBusy, and $\overline{\text{Reset}}$.
3. These parameters do not apply to the clock inputs.
4. V_{OHT} and V_{OLT} apply to the bidirectional data and tag buses only. Note that V_{IH} and V_{IL} also apply to these signals. V_{OHT} and V_{OLT} are provided to give the designer further information about these specific signals.
5. V_{IH} should not be held above V_{CC} + 0.5 volts.
6. Guaranteed by design.
7. V_{OHC} applies to $\overline{\text{RUN}}$ and $\overline{\text{Exception}}$.

5

AC ELECTRICAL CHARACTERISTICS(1,4)

COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to +70°C, V_{CC} = +5.0V ±5%)

Symbol	Parameter	Test Conditions	16.67MHz		20.0MHz		25.0MHz		33.33MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clock											
TCkHigh	Input Clock HIGH(2)	Note 7	12.5	—	10	—	8.0	—	6.0	—	ns
TCkLow	Input Clock LOW(2)	Note 7	12.5	—	10	—	8.0	—	6.0	—	ns
TCkP	Input Clock Period(2)		30	500	25	500	20	500	15	500	ns
	Clk2xSys to Clk2xSmp/Rd(5)		0	Tcyc/4	0	Tcyc/4	0.0	Tcyc/4	0	Tcyc/4	ns
	Clk2xSmp/Rd to Clk2xPhi(5)		9.0	Tcyc/4	7.0	Tcyc/4	5.0	Tcyc/4	3.5	Tcyc/4	ns
Run Operation											
TDEn	Data Enable(3)		—	–2.0	—	–2.0	—	–1.5	—	–1.5	ns
TDDis	Data Disable(3)		—	–1.0	—	–1.0	—	–0.5	—	–0.5	ns
TDVal	Data Valid	Load= 25pF	—	3.0	—	3.0	—	2.0	—	2.0	ns
TWrDly	Write Delay	Load= 25pF	—	5.0	—	4.0	—	3.0	—	2.0	ns
TDS	Data Set-up		9.0	—	8.0	—	6.0	—	4.5	—	ns
TDH	Data Hold		–2.5	—	–2.5	—	–2.5	—	–2.5	—	ns
TCBS	CpBusy Set-up		13	—	11	—	9.0	—	7.0	—	ns
TCBH	CpBusy Hold		–2.5	—	–2.5	—	–2.5	—	–2.5	—	ns
TAcTy	Access Type (1:0)	Load= 25pF	—	7.0	—	6.0	—	5.0	—	3.5	ns
TAT2	Access Type2	Load= 25pF	17	—	14	—	12	—	—	8.5	ns
TMWr	Memory Write	Load= 25pF	1.0	27	1.0	23	1.0	18	—	9.5	ns
TExc	Exception	Load= 25pF	—	7.0	—	7.0	—	5.0	—	3.5	ns
TAval	Address Valid	Load= 25pF	—	2.0	—	2.0	—	1.5	—	1.0	ns
TInts	$\overline{\text{Int(n)}}$ Set-up		9.0	—	8.0	—	6.0	—	4.5	—	ns
TWTH	$\overline{\text{Int(n)}}$ Hold		–2.5	—	–2.5	—	–2.5	—	–2.5	—	ns
Stall Operation											
TSAVal	Address Valid	Load= 25pF	—	30	—	23	—	20	—	15	ns
TSAcTy	Access Type	Load= 25pF	—	27	—	23	—	18	—	13.5	ns
TMRdi	Memory Read Initiate	Load= 25pF	1.0	27	1.0	23	1.0	18	1.0	13.5	ns
TMRdT	Memory Read Terminate	Load= 25pF	1.0	2.0	1.0	23	1.0	5.0	1.0	13.5	ns
TStl	Run Terminate	Load= 25pF	3.0	17	3.0	15	3.0	10	2.0	7.5	ns
TRun	Run Initiate	Load= 25pF	—	7.0	—	6.0	—	4.0	—	3.0	ns
TSMWr	Memory Write	Load= 25pF	3.0	27	3.0	23	3.0	18	2.0	9.5	ns
TSEc	Exception Valid	Load= 25pF	—	15	—	13	—	10	—	7.5	ns
TDMADis	DMA Drive On	Load= 25pF	3.0	15	3.0	15	3.0	15	3.0	15	ns
TDMAEn	DMA Drive Off	Load= 25pF	—	10	—	10	—	10	—	10	ns
Reset Initialization											
TRST	Reset Pulse Width		6.0	—	6.0	—	6.0	—	6.0	—	Tcyc
TRSTTAG	Reset Pulse Width, Pull-downs on Tag		140	—	140	—	140	—	140	—	µs
Capacitive Load Deration											
CLD	Load Derate(6)		0.5	1.0	0.5	1.0	0.5	1.0	0.5	1.0	ns/25pF

2873 tbl 11

NOTES:
1. All timings are referenced to 1.5V.
2. The clock parameters apply to all three 2xClocks: Clk2xSys, Clk2xSmp/Rd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. These parameters are illustrated in detail in the *IDT79R3001 Hardware Interface Guide.*
5. T_{cyc} is one CPU clock cycle (2 cycles of a 2x clock).
6. With the exception of $\overline{\text{Run}}$, no two signals on a given device will derate for a given load by a difference greater than 15%.
7. Transition time <2.5ns for 33MHz; <5ns for lower speeds.

AC ELECTRICAL CHARACTERISTICS[1,4]
COMMERCIAL TEMPERATURE RANGE (Tc = 0°C to +90°C, Vcc = +5.0V ±5%)

Symbol	Parameter	Test Conditions	40.0MHz		Unit
			Min.	Max.	
Clock					
TckHigh	Input Clock HIGH[2]	Transition < 2.5ns	5.0	—	ns
TckLow	Input Clock LOW[2]	Transition < 2.5ns	5.0	—	ns
TckP	Input Clock Period[2]		12.5	500	ns
	Clk2xSys to Clk2xSmp/Rd[5]		0	Tcyc/4	ns
	Clk2xSmp/Rd to Clk2xPhi[5]		3.0	Tcyc/4	ns
Run Operation					
TDEn	Data Enable[3]		—	–1.5	ns
TDDis	Data Disable[3]		—	–0.5	ns
TDVal	Data Valid	Load= 25pF	—	1.5	ns
TWrDly	Write Delay	Load= 25pF	—	2.0	ns
TDS	Data Set-up		4.0	—	ns
TDH	Data Hold		–2.5	—	ns
TCBS	CpBusy Set-up		6.0	—	ns
TCBH	CpBusy Hold		–2.5	—	ns
TAcTy	Access Type (1:0)	Load= 25pF	—	3.0	ns
TAT2	Access Type2	Load= 25pF	—	7.5	ns
TMWr	Memory Write	Load= 25pF	—	9.0	ns
TExc	Exception	Load= 25pF	—	3.0	ns
Stall Operation					
TSAVal	Address Valid	Load= 25pF	—	12.5	ns
TSAcTy	Access Type	Load= 25pF	—	9.0	ns
TMRdi	Memory Read Initiate	Load= 25pF	—	9.0	ns
TMRdT	Memory Read Terminate	Load= 25pF	—	9.0	ns
TStl	Run Terminate	Load= 25pF	2.0	6.0	ns
TRun	Run Initiate	Load= 25pF	—	3.0	ns
TSMWr	Memory Write	Load= 25pF	2.0	9.0	ns
TSExc	Exception Valid	Load= 25pF	—	6.0	ns
TDMADis	DMA Drive On	Load= 25pF	3.0	15	ns
TDMAEn	DMA Drive Off	Load= 25pF	—	10	ns
Reset Initialization					
TRST	Reset Pulse Width		—	—	Tcyc
TRSTTAG	Reset Pulse Width, Pull-downs on Tag		—	—	µs
Capacitive Load Deration					
CLD	Load Derate[6]		—	—	ns/25pF

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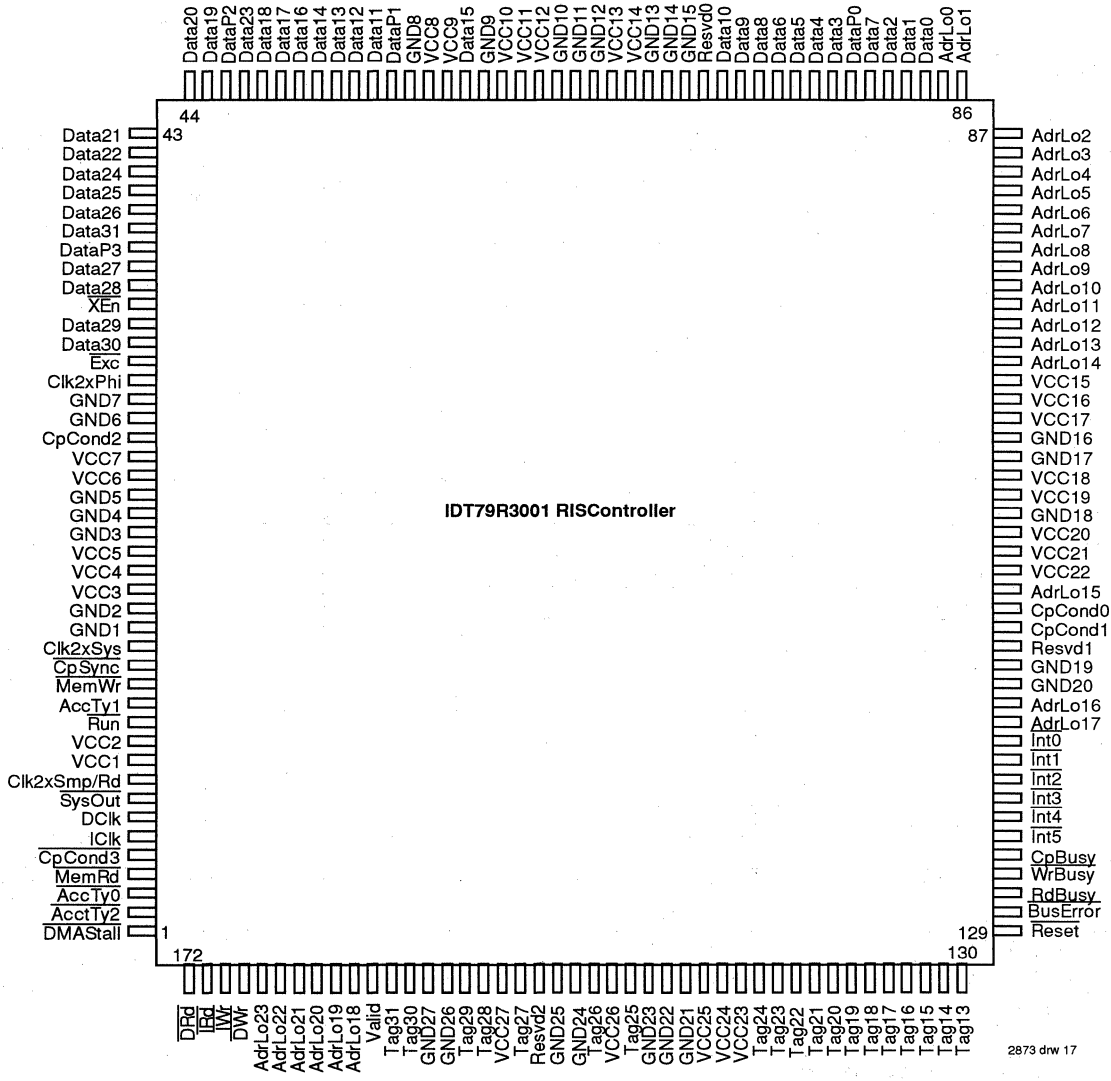
NOTES:
1. All timings are referenced to 1.5V.
2. The clock parameters apply to all three 2xClocks: Clk2xSys, Clk2xSmp/Rd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. These parameters are illustrated in detail in the *IDT79R3001 Hardware Interface Guide.*
5. Tcyc is one CPU clock cycle (2 cycles of a 2x clock).
6. With the exception of $\overline{\text{Run}}$, no two signals on a given device will derate for a given load by a difference greater than 15%.

5

PIN CONFIGURATIONS

172-Pin Ceramic Flatpack (Cavity Side View)



NOTE:
1. AccTyp2 is redefined to be $\overline{\text{Parity Error}}$ if the parity enable option is selected at device initialization.

PIN CONFIGURATIONS (Continued)

144-Pin PGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	VCC14	AdrLo 6	AdrLo 10	AdrLo 11	VCC12	AdrLo 14	AdrLo 15	CpCond 0	AdrLo 16	AdrLo 17	$\overline{\text{Int(2)}}$	$\overline{\text{Int(5)}}$	$\overline{\text{Wr}}$ Busy	$\overline{\text{Reset}}$	VCC10
B	AdrLo 3	$\overline{\text{Mem}}$ $\overline{\text{Wr}}$	AdrLo 7	AdrLo 9	AdrLo 12	$\overline{\text{Cp}}$ $\overline{\text{Sync}}$	AdrLo 13	CpCond 1	$\overline{\text{Int(1)}}$	$\overline{\text{Int(3)}}$	Cp Busy	$\overline{\text{Bus}}$ $\overline{\text{Error}}$	$\overline{\text{Run}}$	Tag13	Tag16
C	AdrLo 0	AdrLo 4	VCC13	AdrLo 5	AdrLo 8	GND13	GND12	VCC11	$\overline{\text{Int(0)}}$	$\overline{\text{Int(4)}}$	Rd Busy	GND	Tag14	Tag17	Tag20
D	Data 1	AdrLo 2	GND0										Tag15	Tag19	Tag21
E	DataP 0	Data 0	AdrLo 1										Tag18	Tag22	VCC9
F	VCC0	Data 7	Data 2										GND10	Tag23	Tag25
G	Data 4	Data 3	GND1										GND9	Tag24	Tag26
H	Data 6	Data 5	Data 8					**IDT79R3001 RISController**					VCC8	Tag28	Tag27
J	Data 10	DataP 1	Data 9										Tag31	Valid	Tag29
K	Data 15	Data 11	GND2										GND8	AdrLo 19	Tag30
L	VCC1	Data 12	Data 17										AdrLo 22	AdrLo 20	AdrLo 18
M	Data 13	Data 16	DataP 2										GND7	AdrLo 23	VCC7
N	Data 14	Data 18	Data 19	GND3	Data 24	DataP 3	VCC3	VCC4	GND5	GND6	$\overline{\text{Mem}}$ $\overline{\text{Rd}}$	DMA Stall	$\overline{\text{DRd}}$	$\overline{\text{IWr}}$	AdrLo 21
P	Data 23	Data 20	AccTy1	Data 22	Data 26	Data 27	$\overline{\text{XEn}}$	Data 30	Clk2x Sys	Clk2x Smp/Rd	$\overline{\text{DClk}}$	Cp Cond3	AccTy0	$\overline{\text{IRd}}$	$\overline{\text{DWr}}$
Q	VCC2	Data 21	Data 25	Data 31	Data 28	GND4	Data 29	$\overline{\text{Excep-}}$ $\overline{\text{tion}}$	Clk2x Phi	Cp Cond2	$\overline{\text{SysOut}}$	VCC5	IClk	AccTy2	VCC6

NOTE:
1. AccTyp2 is redefined to be $\overline{\text{Parity Error}}$ if the parity enable option is selected at device initialization.

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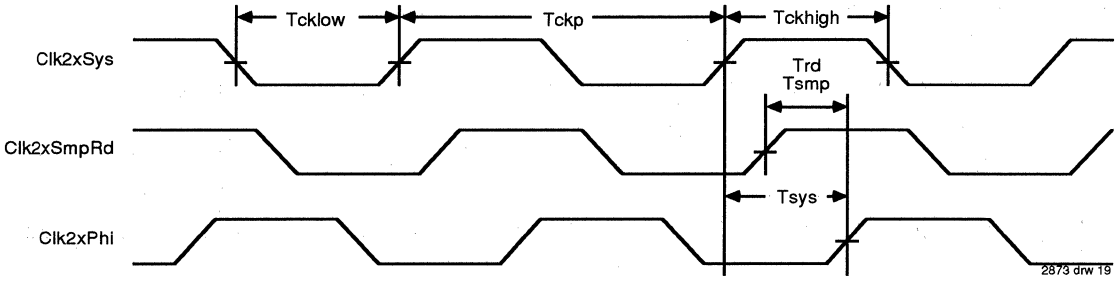

Figure 16. Input Clock Timing

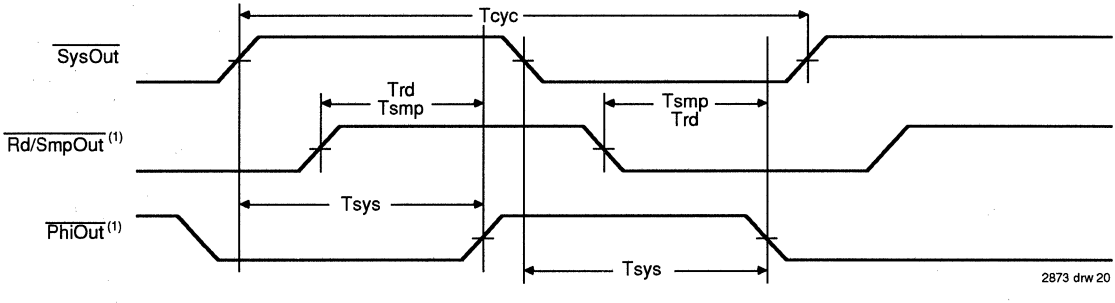

Figure 17. Processor Reference Clock Timing

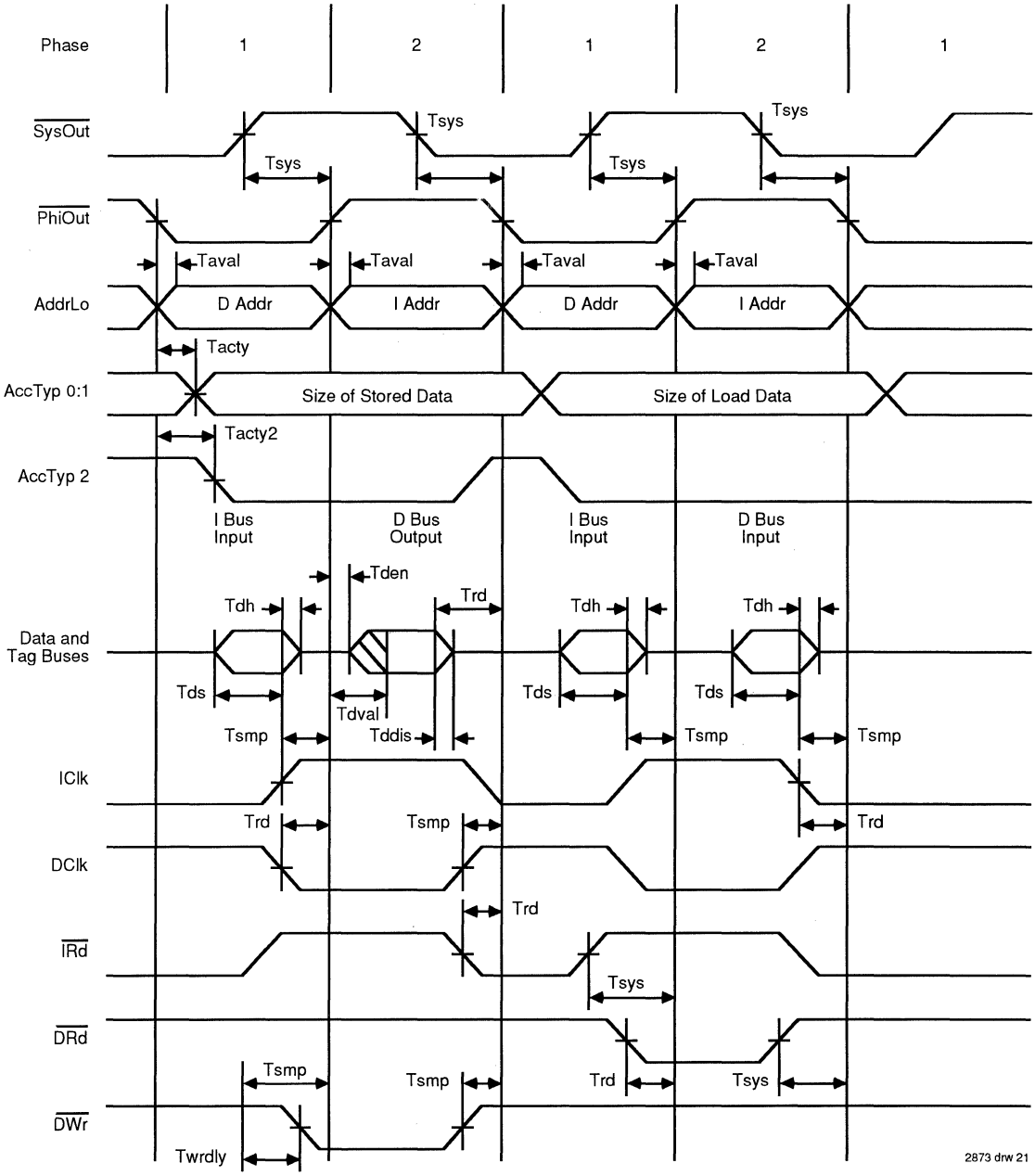

Figure 18. Synchronous Memory (Cache) Timing

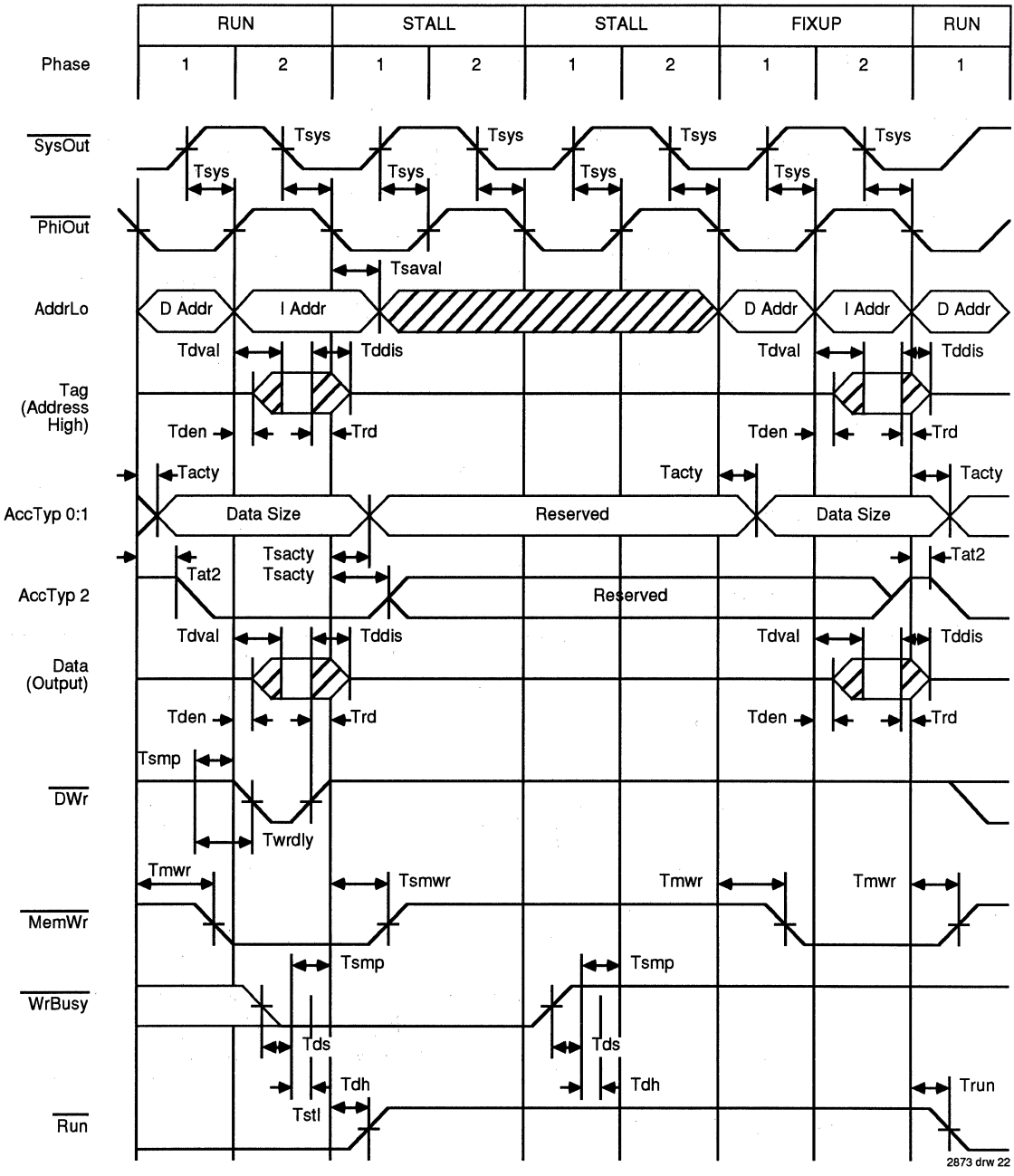

Figure 19. Memory Write Timing

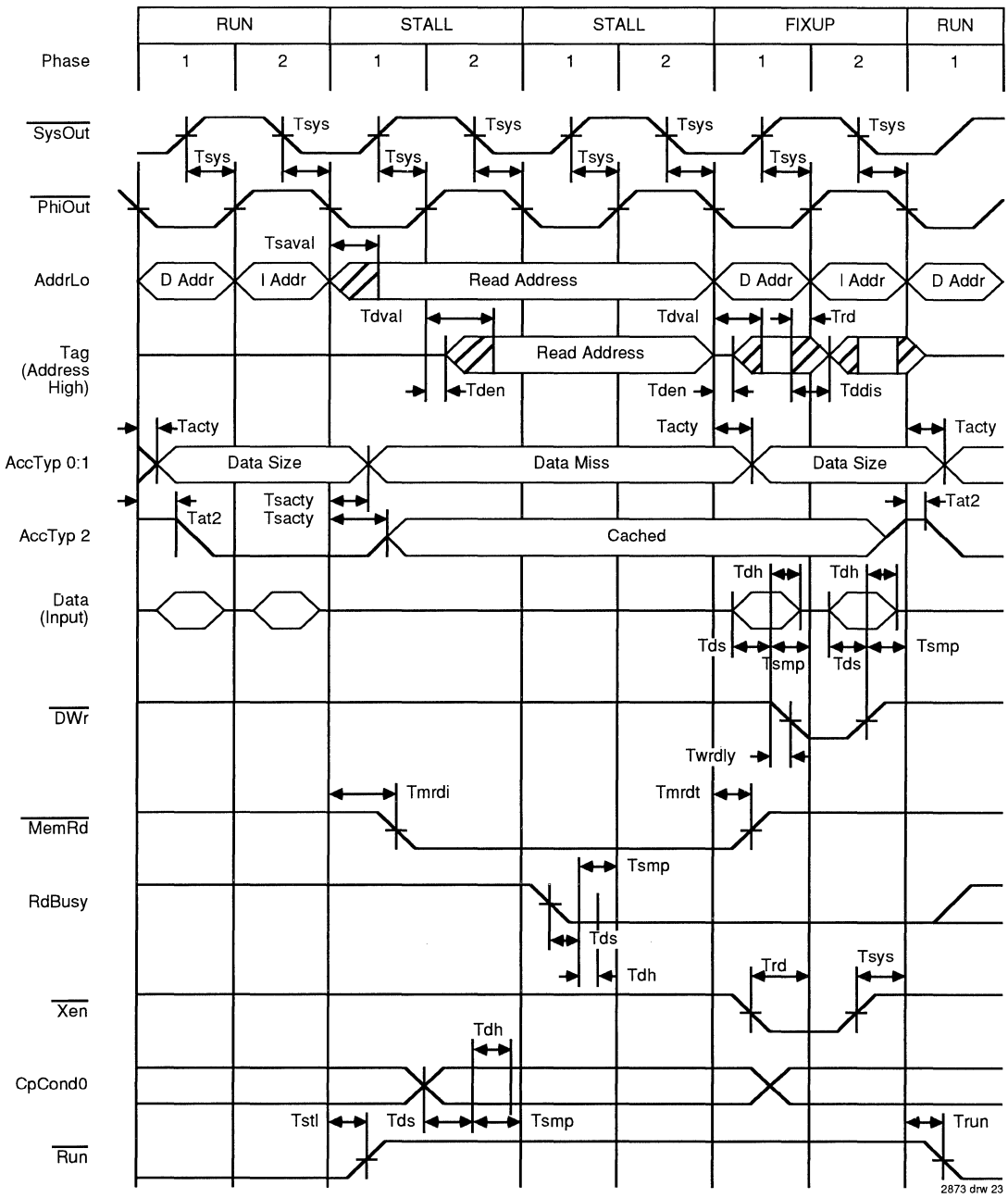

Figure 20. Memory Read Timing

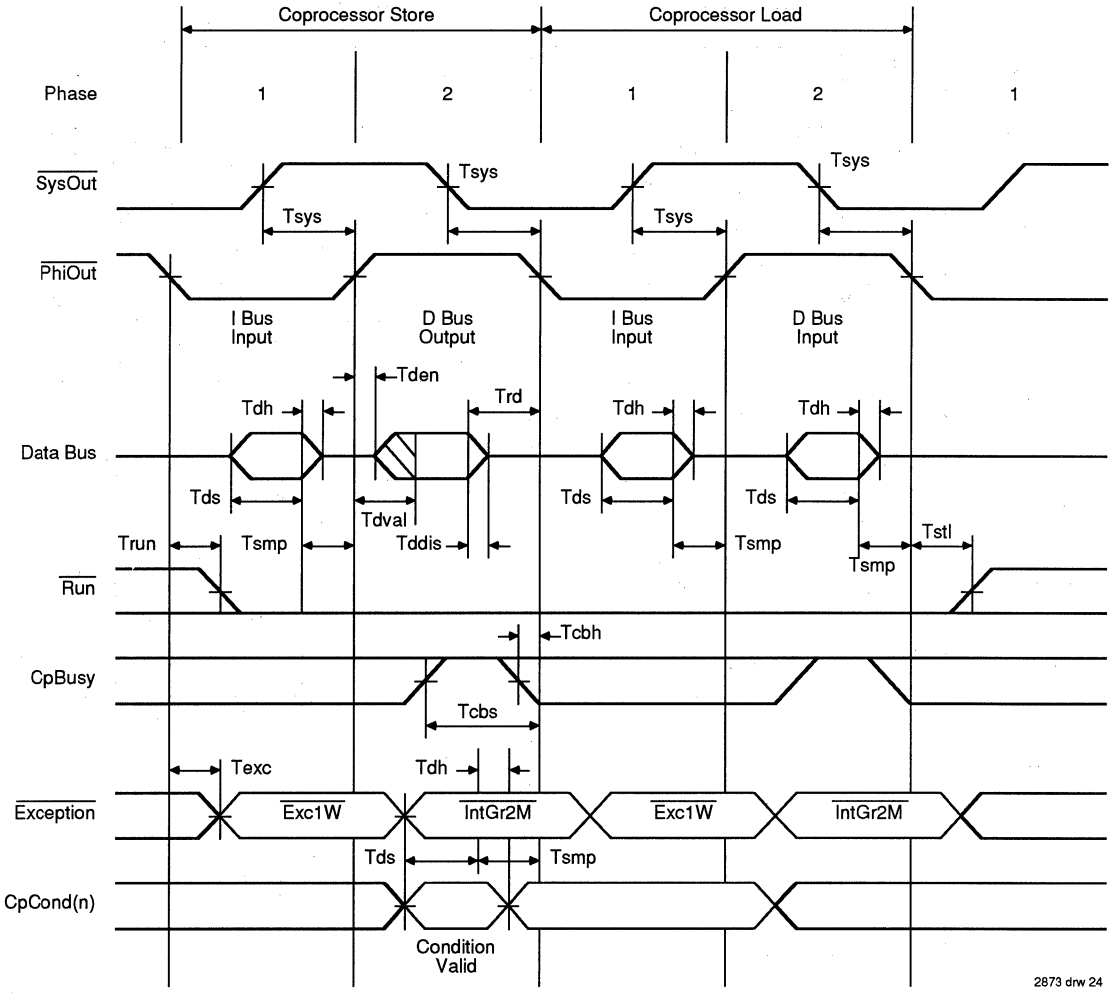

Figure 21. Co-Processor Load/Store Timing

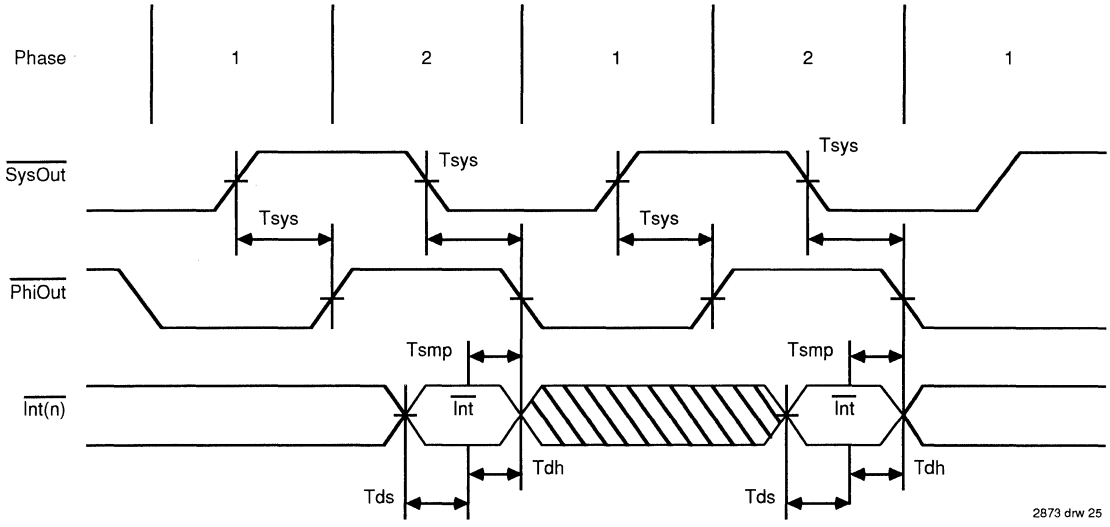

Figure 22. Interrupt Timing

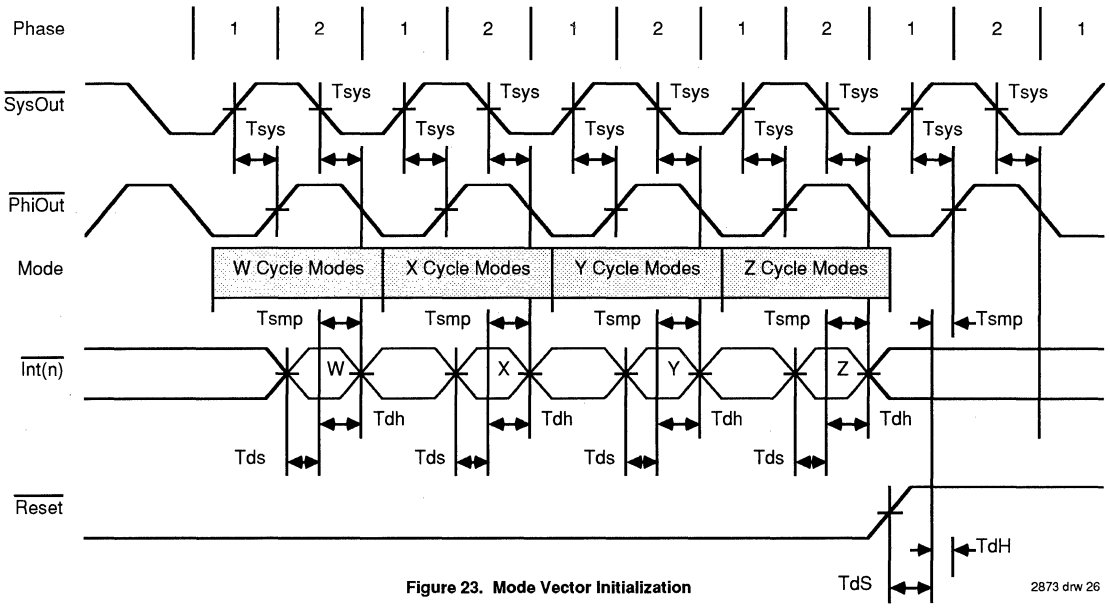

Figure 23. Mode Vector Initialization

NOTES:
1. Reset must be negated synchronously; however, it can be asserted asynchronously. Designs must not rely on the proper functioning of $\overline{\text{SysOut}}$ prior to the assertion of $\overline{\text{Reset}}$.
2. If $\overline{\text{Phase-Lock On}}$ or is asserted as mode select options, they should be asserted throughout the $\overline{\text{Reset}}$ period, to insure that the slowest coprocessor in the system has sufficient time to lock to the CPU clocks.
3. $\overline{\text{Reset}}$ is actually sampled in both Phase 1 and Phase 2. To insure proper initialization, it must be negated relative to the end of Phase 1.

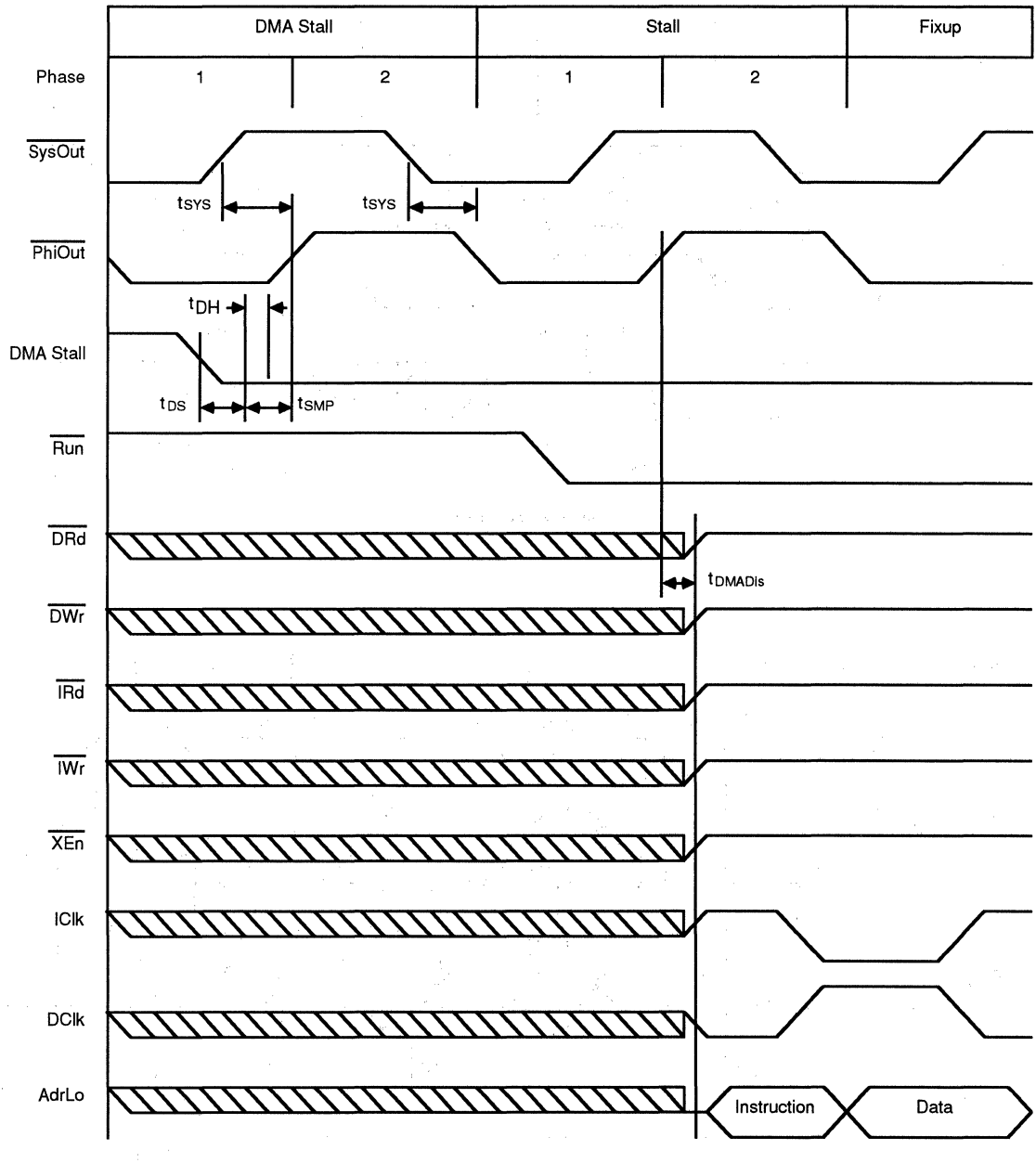

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Figure 24. Entering DMA Stall

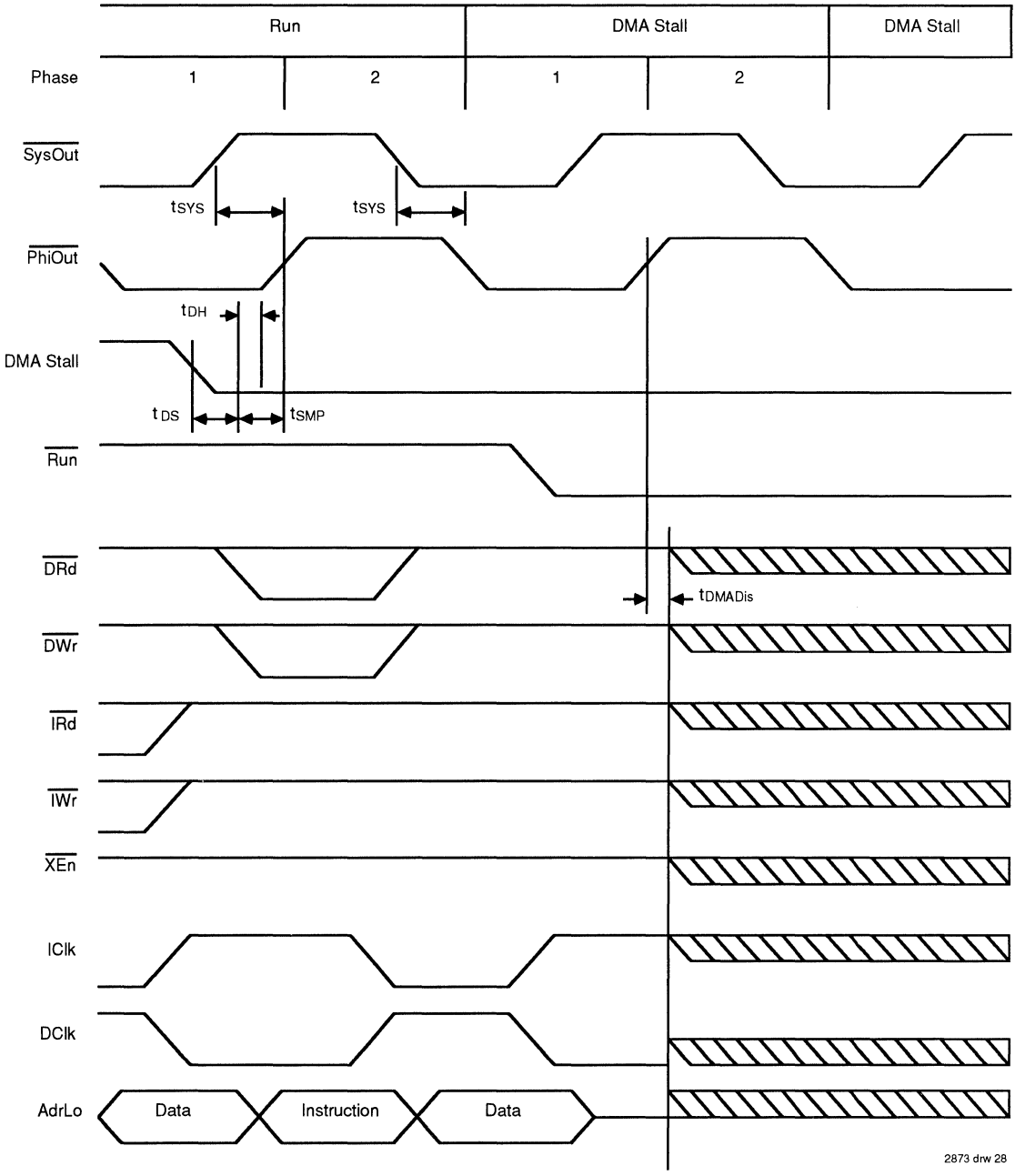

Figure 25. Completing DMA Stall

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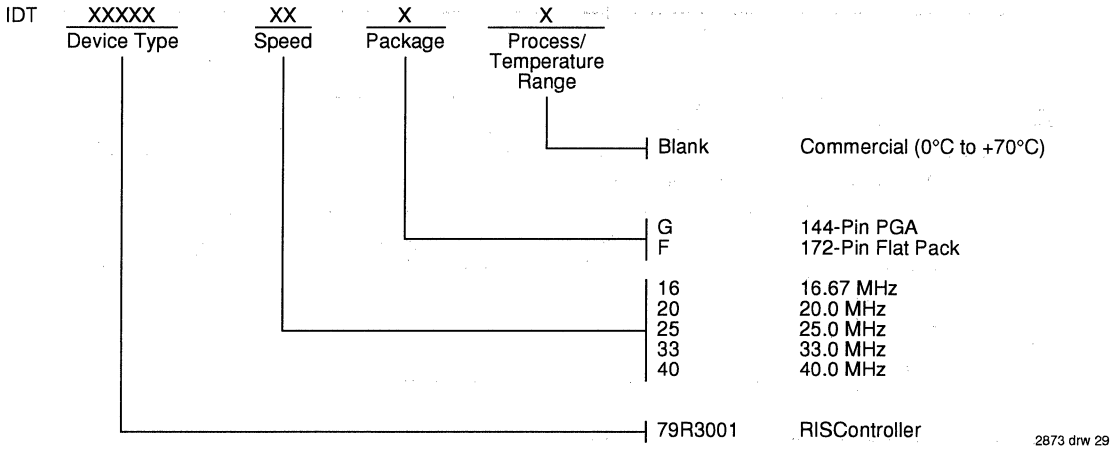
ORDERING INFORMATION



VALID COMBINATIONS

IDT	79R3001- 16,20,25,33	All Packages
	79R3001- 40	G

Integrated Device Technology, Inc.

RISC CPU PROCESSOR
RISCore™

IDT79R3500

FEATURES:

- Efficient Pipelining—The CPU's 5-stage pipeline design assists in obtaining an execution rate approaching one instruction per cycle. Pipeline stalls and exceptions are handled precisely and efficiently.
- On-Chip Cache Control—The IDT79R3500 provides a high-bandwidth memory interface that handles separate external Instruction and Data Caches ranging in size from 4 to 256kBs each. Both caches are accessed during a single CPU cycle. All cache control is on-chip.
- On-Chip Memory Management Unit—A fully-associative, 64-entry Translation Lookaside Buffer (TLB) provides fast address translation for virtual-to-physical memory mapping of the 4GB virtual address space.
- Dynamically able to switch between Big- and Little- Endian byte ordering conventions.
- Optimizing Compilers are available for C, FORTRAN, Pascal, COBOL, Ada, PL/1 and C++.
- 20 through 40MHz clock rates yield up to 32VUPS sustained throughput.
- Supports independent multi-word block refill of both the instruction and data caches with variable block sizes.
- Supports concurrent refill and execution of instructions.
- Partial word stores executed as read-modify-write.
- 6 external interrupt inputs, 2 software interrupts, with single cycle latency to exception handler routine.
- Flexible multiprocessing support on chip with no impact on uniprocessor designs.
- A single chip integrating the R3000 CPU and R3010 FPA execution units, using the R3000A pinout.
- Software compatible with R3000, R2000 CPUs and R3010, R2010 FPAs.
- TLB disable feature allowing a simple memory model for Embedded Applications.
- Programmable Tag bus width allowing reduced cost cache.
- Hardware Support of Single- and Double-Precision Floating Point Operations that include Add, Subtract, Multiply, Divide, Comparisons, and Conversions.
- Sustained Floating Point Performance of 11 MFlops single precision LINPACK and 7.3MFLOPS double precision
- Supports Full Conformance With IEEE 754-1985 Floating Point Specification
- 64-bit FP operation using sixteen 64-bit data registers
- Military product compliant to MIL-STD 833, class B

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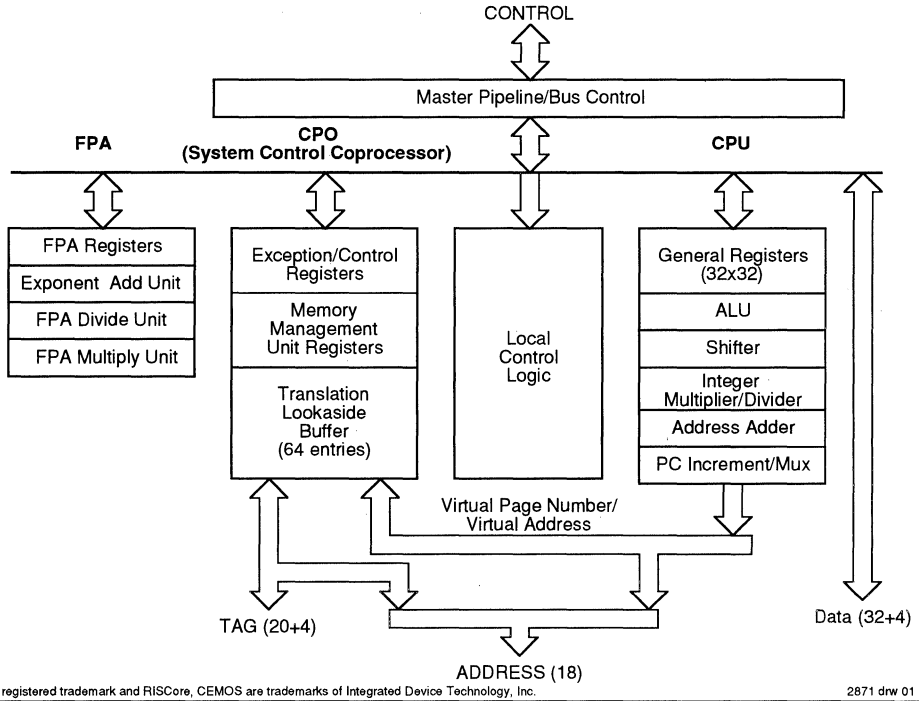
IDT79R3500 PROCESSOR



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DESCRIPTION:

The IDT79R3500 RISC Microprocessor consists of three tightly-coupled processors integrated on a single chip. The first processor is a full 32-bit CPU based on RISC (Reduced Instruction Set Computer) principles to achieve a new standard of microprocessor performance. The second processor is a system control coprocessor, called CP0, containing a fully-associative 64-entry TLB (Translation Lookaside Buffer), MMU (Memory Management Unit) and control registers, supporting a 4GB virtual memory subsystem, and a Harvard Architecture Cache Controller achieving a bandwidth of 320MBs/second using industry standard static RAMs. The third processor is the Floating Point Accelerator which performs arithmetic operations on values in floating-point representations. This processor fully conforms to the requirements of ANSI/IEEE Standard 754-1985, "IEEE Standard for Binary Floating-Point Arithmetic." In addition, the architecture fully supports the standard's recommendations.

The programmer model of this device will be the same as the programmer model of a system which uses a discrete IDT79R3000 with the IDT79R3010: 32 integer registers, 16 floating point registers; co-processor 0 registers; floating point status and control register; RISC integer ALU; Integer Multiply and Divide ALU; Floating Point Add/Subtract, Multiply, and Divide ALUs. The device pipeline will be the same as for the IDT79R3000, as will the co-processor 0 functionality. No new instructions have been introduced. Pin compatibility extends to AC and DC characteristics, software execution and initialization mode vector selection.

This data sheet provides an overview of the features and architecture of the IDT79R3500 CPU, Revision 3.0. A more detailed description of the operation of the device is incorporated in the *R3500 Family Hardware User Manual*, and a more detailed architectural overview is provided in the *MIPS RISC Architecture* book, both available from IDT. Documentation providing details of the software and development environments supporting this processor are also available from IDT.

IDT79R3500 CPU Registers

The IDT79R3500 CPU provides 32 general purpose 32-bit registers, a 32-bit Program Counter, and two 32-bit registers that hold the results of integer multiply and divide operations. Only two of the 32 general registers have a special purpose: register r0 is hardwired to the value "0", which is a useful constant, and register r31 is used as the link register in jump-and-link instructions (return address for subroutine calls).

The CPU registers are shown in Figure 2. Note that there is no Program Status Word (PSW) register shown in this figure: the functions traditionally provided by a PSW register are instead provided in the Status and Cause registers incorporated within the System Control Coprocessor (CP0).

FPA REGISTERS

The IDT79R3010A FPA provides 32 general purpose 32-bit registers, a Control/Status register, and a Revision Identification register.

Floating-point coprocessor operations reference three types of registers:

- Floating-Point Control Registers (FCR)
- Floating-Point General Registers (FGR)
- Floating-Point Registers (FPR)

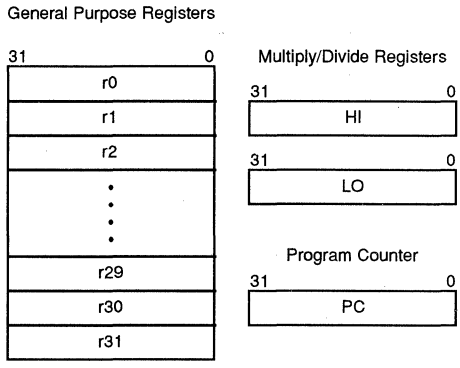

Figure 2. IDT79R3500 CPU Registers

Floating-Point General Registers (FGR)

There are 32 Floating-Point General Registers (FGR) on the FPA. They represent directly-addressable 32-bit registers, and can be accessed by Load, Store, or Move Operations.

Floating-Point Registers (FPR)

The 32 FGRs described in the preceding paragraph are also used to form sixteen 64-bit Floating-Point Registers (FPR). Pairs of general registers (FGRs), for example FGR0 and FGR1 (Figure 3) are physically combined to form a single 64-bit FPR. The FPRs hold a value in either single- or double-precision floating-point format. Double-precision format FPRs are formed from two adjacent FGRs.

Floating-Point Control Registers (FCR)

There are 2 Floating-Point Control Registers (FCR) on the FPA. They can be accessed only by Move operations and include the following:

- Control/Status register, used to control and monitor exceptions, operating modes, and rounding modes;
- Revision register, containing revision information about the FPA.

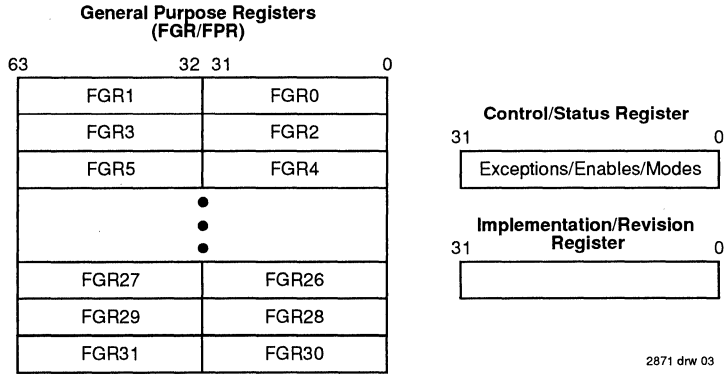

Figure 3. FPA Registers

Instruction Set Overview

All IDT79R3500 instructions are 32 bits long, and there are only three instruction formats. This approach simplifies instruction decoding, thus minimizing instruction execution time. The IDT79R3500 processor initiates a new instruction on every run cycle, and is able to complete an instruction on almost every clock cycle. The only exceptions are the Load instructions and Branch instructions, which each have a single cycle of latency associated with their execution. Note, however, that in the majority of cases the compilers are able to fill these latency cycles with useful instructions which do not require the result of the previous instruction. This effectively eliminates these latency effects.

The actual instruction set of the CPU was determined after extensive simulations to determine which instructions should be implemented in hardware, and which operations are best synthesized in software from other basic instructions. This methodology resulted in the IDT79R3500 having the highest performance of any available microprocessor.

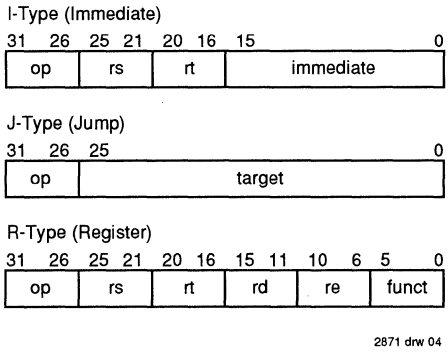

Figure 4. IDT79R3500 Instruction Formats

The IDT79R3500 instruction set can be divided into the following groups:

- **Load/Store** instructions move data between memory and general registers. They are all I-type instructions, since the only addressing mode supported is base register plus 16-bit, signed immediate offset.
  The Load instruction has a single cycle of latency, which means that the data being loaded is not available to the instruction immediately after the load instruction. The compiler will fill this delay slot with either an instruction which is not dependent on the loaded data, or with a NOP instruction. There is no latency associated with the store instruction.
  Loads and Stores can be performed on byte, half-word, word, or unaligned word data (32-bit data not aligned on a modulo-4 address). The CPU cache is constructed as a write-through cache.
- **Computational** instructions perform arithmetic, logical and shift operations on values in registers. They occur in both R-type (both operands and the result are registers) and I-type (one operand is a 16-bit immediate) formats. FP computational instructions perform arithmetic operations on floating point values in the FPA registers. Note that computational instructions are three operand instructions; that is, the result of the operation can be stored into a different register than either of the two operands. This means that operands need not be overwritten by arithmetic operations. This results in a more efficient use of the large register set.
- **Conversion** instructions perform conversion operations on the floating point values in the FPA registers.
- **Compare** intructions perform comparisons of the contents of FPA registers and set a condition bit based on the results. The result of the compare operations is tied directly to Cp Cond (1) for software testing.
- **Jump and Branch** instructions change the control flow of a program. Jumps are always to a paged absolute address formed by combining a 26-bit target with four bits of the Program counter (J-type format, for subroutine calls), or 32-bit register byte addresses (R-type, for returns and

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OP	Description	OP	Description
	Load/Store Instructions		
LB	Load Byte		**Shift Instructions (Cont.)**
LBU	Load Byte Unsigned	SRA	Shift Right Arithmetic
LH	Load Halfword	SLLV	Shift Left Logical Variable
LHU	Load Halfword Unsigned	SRLV	Shift Right Logical Variable
LW	Load Word	SRAV	Shift Right Arithmetic Variable
LWL	Load Word Left		
LWR	Load Word Right		**FPA Conversion Instructions**
SB	Store Byte	CVT.S.fmt	Floating point Convert to Single FP
SH	Store Halfword	CVT.D.fmt	Floating point Convert to Double FP
SW	Store Word	CVT.W.fmt	Floating point Convert to fixed point
SWL	Store Word Left		
SWR	Store Word Right		**Multiply/Divide Instructions**
		MULT	Multiply
	FPA Load/Store/Move Instructions	MULTU	Multiply Unsigned
LWC1	Load Word to FPA	DIV	Divide
SWC1	Store Word from FPA	DIVU	Divide Unsigned
MTC1	Move Word to FPA	MFHI	Move From HI
MFC1	Move Word from FPA	MTHI	Move To HI
CTC1	Move Control word to FPA	MFLO	Move From LO
CFC1	Move Control word from FPA	MTLO	Move To LO
	Arithmetic Instructions		**Jump and Branch Instructions**
	(ALU Immediate)	J	Jump
ADDI	Add Immediate	JAL	Jump and Link
ADDIU	Add Immediate Unsigned	JR	Jump to Register
SLTI	Set on Less Than Immediate	JALR	Jump and Link Register
SLTIU	Set on Less Than Immediate Unsigned	BEQ	Branch on Equal
		BNE	Branch on Not Equal
ANDI	AND Immediate	BLEZ	Branch on Less than or Equal to Zero
ORI	OR Immediate	BGTZ	Branch on Greater Than Zero
XORI	Exclusive OR Immediate	BLTZ	Branch on Less Than Zero
LUI	Load Upper Immediate	BGEZ	Branch on Greater than or Equal to Zero
	Arithmetic Instructions	BLTZAL	Branch on Less Than Zero and Link
	(3-operand, register-type)	BGEZAL	Branch on Greater than or Equal to Zero and Link
ADD	Add		
ADDU	Add Unsigned		
SUB	Subtract		**Special Instructions**
SUBU	Subtract Unsigned	SYSCALL	System Call
SLT	Set on Less Than	BREAK	Break
SLTU	Set on Less Than Unsigned		
AND	AND		**Coprocessor Instructions**
OR	OR	LWCZ	Load Word from Coprocessor
XOR	Exclusive OR	SWCZ	Store Word to Coprocessor
NOR	NOR	MTCZ	Move To Coprocessor
		MFCZ	Move From Coprocessor
	FPA Computational Instructions	CTCZ	Move Control to Coprocessor
ADD.fmt	Floating point Add	CFCZ	Move Control From Coprocessor
SUB.fmt	Floating point Subtract	COPZ	Coprocessor Operation
MUL.fmt	Floating point Multiply	BCZT	Branch on Coprocessor z True
DIV.fmt	Floating point Divide	BCZF	Branch on Coprocessor z False
ABS.fmt	Floating-point Absolute value		
MOV.fmt	Floating point Move		**System Control Coprocessor**
NEG.fmt	Floating point Negate		**(CP0) Instructions**
		MTC0	Move To CP0
	FPA Compare Instructions	MFC0	Move From CP0
C.cond.fmt	Floating-point Compare	TLBR	Read indexed TLB entry
		TLBWI	Write Indexed TLB entry
	Shift Instructions	TLBWR	Write Random TLB entry
SLL	Shift Left Logical	TLBP	Probe TLB for matching entry
SRL	Shift Right Logical	RFE	Restore From Exception

IDT79R3500 Instruction Summary

2871 tbl 01

dispatches). Branches have 16-bit offsets relative to the program counter (I-type). Jump and Link instructions save a return address in Register 31. The R3500 instruction set features a number of branch conditions. Included is the ability to compare a register to zero and branch, and also the ability to branch based on a comparison between two registers. Thus, net performance is increased since software does not have to perform arithmetic instructions prior to the branch to set up the branch conditions.

- **Coprocessor** instructions perform operations in the coprocessors. Coprocessor Loads and Stores are I-type.
- **Coprocessor 0** instructions perform operations on the System Control Coprocessor (CP0) registers to manipulate the memory management and exception handling facilities of the processor.
- **Special** instructions perform a variety of tasks, including movement of data between special and general registers, system calls, and breakpoint. They are always R-type.

Table 1 lists the instruction set of the IDT79R3500 processor.

IDT79R3500 System Control Coprocessor (CP0)

The IDT79R3500 can operate with up to four tightly-coupled coprocessors (designated CP0 through CP3). The System Control Coprocessor (or CP0), is incorporated on the IDT79R3500 chip and supports the virtual memory system and exception handling functions of the IDT79R3500. The virtual memory system is implemented using a Translation Lookaside Buffer and a group of programmable registers as shown in Figure 5.

System Control Coprocessor (CP0) Registers

The CP0 registers shown in Figure 5 are used to control the memory management and exception handling capabilities of the IDT79R3500. Table 2 provides a brief description of each register.

SYSTEM CONTROL COPROCESSOR (CP0) INSTRUCTIONS

Register	Description
EntryHi	High half of a TLB entry
EntryLo	Low half of a TLB entry
Index	Programmable pointer into TLB array
Random	Pseudo-random pointer into TLB array
Status	Mode, interrupt enables, and diagnostic status info
Cause	Indicates nature of last exception
EPC	Exception Program Counter
Context	Pointer into kernel's virtual Page Table Entry array
BadVA	Most recent bad virtual address
PRId	Processor revision identification (Read only)

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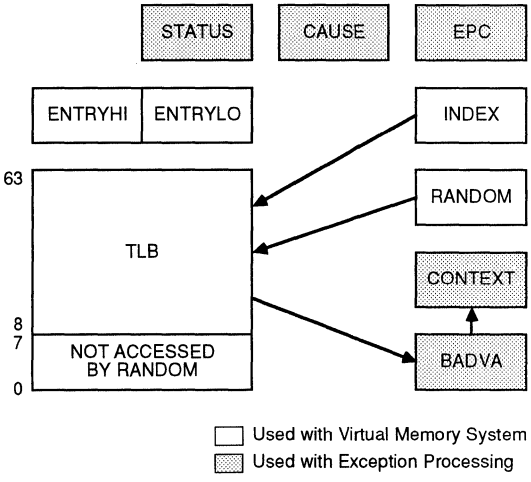

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Figure 5. The System Coprocessor Registers

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Memory Management System

The IDT79R3500 has an addressing range of 4GB. However, since most IDT79R3500 systems implement a physical memory smaller than 4GBs, the IDT79R3500 provides for the logical expansion of memory space by translating addresses composed in a large virtual address space into available physical memory address. Two TLB modes are supported. When the TLB is used, the 4GB address space is divided into 2GBs which can be accessed by both the users and the kernel, and 2GBs for the kernel only. Virtual addresses within the kernel/user segment are translated to physical addresses on a 4kB page basis. This mode is typical of UNIX and other sophisticated operating systems. When the TLB is disabled, mapping is locked as 2GBs as kernel/user, and 1.5GBs as kernel only. This mode requires no TLB manipulation, provides large linear address space, and is typical for embedded applications.

TLB (Translation Lookaside Buffer)

Virtual memory mapping is assisted by the Translation Lookaside Buffer (TLB). The on-chip TLB provides very fast virtual memory access and is well-matched to the requirements of multi-tasking operating systems. The fully-associative TLB contains 64 entries, each of which maps a 4kB page, with controls for read/write access, cacheability, and process identification. The TLB allows each user to access up to 2GBs of virtual address space.

Figure 6 illustrates the format of each TLB entry. The Translation operation involves matching the current Process ID (PID) and upper 20 bits of the address against PID and VPN (Virtual Page Number) fields in the TLB. When both match (or the TLB entry is Global), the VPN is replaced with the PFN (Physical Frame Number) to form the physical address.

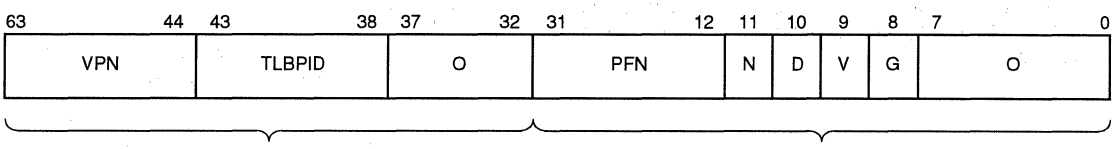
TLB misses are handled in software, with the entry to be replaced determined by as imple RANDOM function. The routine to process a TLB miss in the UNIX environment requires only 10-12 cycles, which compares favorably with many CPUs which perform the operation in hardware.

TLB Disabled Operation

Many embedded systems do not like the complexity or uncertainty associated with the on-chip TLB. However, many systems still desire the ability to implement a kernel/user mode. Therefore, to implement a hierachical task model, the TLB must be used. The R3500 gives the system designer one more option, allowing the TLB to be disabled and performing a fixed mapping of virtual to physical addresses, while maintaining separation of kernel and user resources.

The user may elect to disable the TLB through the reset sectors. In this case, the mapping shown in Figure 8. is used, and device power consumption is reduced. Note tha "cached" segments means that there is no mechanism to exclude addresses in these regions from the cache.

This mapping means that applications designed to run in kseg0 and kseg1 (to avoid the TLB) can use the R3500, disable the TLB to reduce power, and not have to change software to take advantage of this new feature.



VPN – Virtual Page Number
TLBPID – Process ID
PFN – Physical Frame Number
N – Non-cacheable flag
D – Dirty flag (Write protect)
V – Valid entry flag
G – Global flag (ignore PID)
O – Reserved

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Figure 6. TLB Entry Format

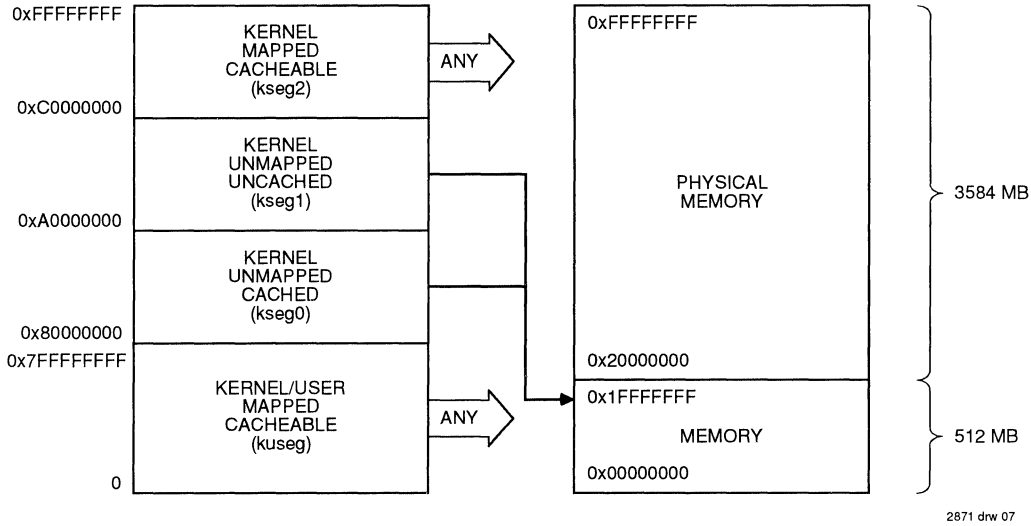
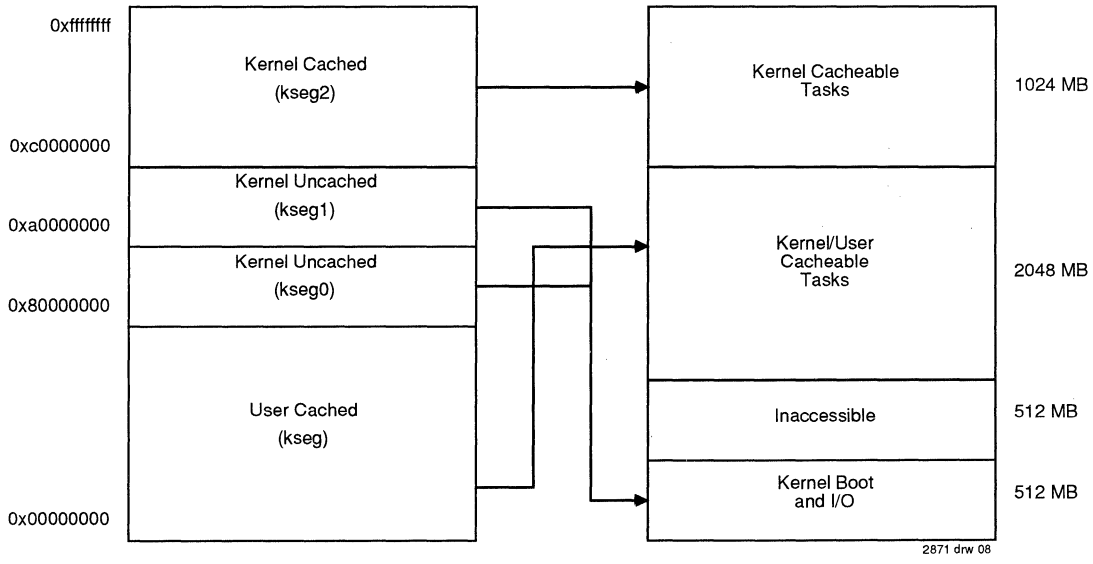


Figure 7. IDT79R3500 Virtual Address Mapping

MNU Address Translation
Virtual –> Physical
(TBL Disabled)



NOTE: This model is consistent with the mapping available in the IDT79R3051 family. The identical mapping provides software compatibility to the lower cost CPUs.

Figure 8. TLB Disabled Mapping

Operating Modes

The IDT79R3500 has two operating modes: User mode and Kernel mode. The IDT79R3500 normally operates in the User mode until an exception is detected forcing it into the Kernel mode. It remains in the Kernel mode until a Restore From Exception (RFE) instruction is executed. The manner in which memory addresses are translated or mapped depends on the operating mode of the IDT79R3500. Figure 7 shows the MMU translation performed for each of the operating modes.

User Mode—in this mode, a single, uniform virtual address space (kuseg) of 2GB is available. When the TLB is used, each virtual address is extended with a 6-bit process identifier field to form unique virtual addresses. All references to this segment are mapped through the TLB. Use of the cache for up to 64 processes is determined by bit settings for each page within the TLB entries. If the TLB is not used, these addresses are translated to begin at 1GB of the physical address space.

Kernel Mode—four separate segments are defined in this mode:

- *kuseg*—when in the kernel mode, references to this segment are treated just like user mode references, thus streamlining kernel access to user data.
- *kseg0*—references to this 512MB segment use cache memory but are not mapped through the TLB. Instead, they always map to the first 0.5GB of physical address space.
- *kseg1*—references to this 512MB segment are not mapped through the TLB and do not use the cache. Instead, they are hard-mapped into the same 0.5GB segment of physical address space as kseg0.
- *kseg2*—when the TLB is not used, references to this 1GB segment directly addresses the upper 1GB of physical address space. These addresses are defined to be kernel mode which are cacheable. When the TLB is used, references to this 1GB segment are always mapped through the TLB and use of the cache is determined by bit settings within the TLB entry.

FPA COPROCESSOR OPERATION (CP1)

The FPA continually monitors the processor instruction stream. If an instruction does not apply to the coprocessor, it is ignored; if an instruction does apply to the coprocessor, the FPA executes that instruction and transfers necessary result and exception data synchronously to the main processor.

The FPA performs three types of operations:

- Loads and Stores;
- Moves;
- Two- and three-register floating-point operations.

Load, Store, and Move Operation

Load, Store, and Move operations data between memory or the integer registers and the FPA registers. These operations perform no format conversions and cause no floating-point exceptions. Load, Store, and Move operations reference a single 32-bit word of either the Floating-Point General Registers (FGR) or the Floating-Point Control Registers (FCR).

Floating-Point Operations

The FPA supports the following single- and double-precision format floating-point operations:

- Add
- Subtract
- Multiply
- Divide
- Absolute Value
- Move
- Negate
- Compare

In addition, the FPA supports conversions between single- and double-precision floating-point formats and fixed-point formats.

The FPA incorporates separate Add/Subtract, Multiply, and Divide units, each capable of independent and concurrent operation. Thus, to achieve very high performance, floating point divides can be overlapped with floating point multiplies and floating point additions. These floating point operations occur independently of the actions of the CPU, allowing further overlap of integer and floating point operations. Figure 9 illustrates an example of the types of overlap permissible.

Exceptions

The FPA supports all five IEEE standard exceptions:

- Invalid Operation
- Inexact Operation
- Division by Zero
- Overflow
- Underflow

The FPA also suppoerts the optional, Unimplemented Operation exception that allows unimplemented instructions to trap to software emulation routines.

The FPA provides precise exception capability to the CPU; that is, the execution of a floating point operation which generates an exception causes that exception to occur at the CPU instruction which caused the operation. This precise exception capability is a requirement in applications and languages which provide a mechanism for local software exception handlers within software modules.

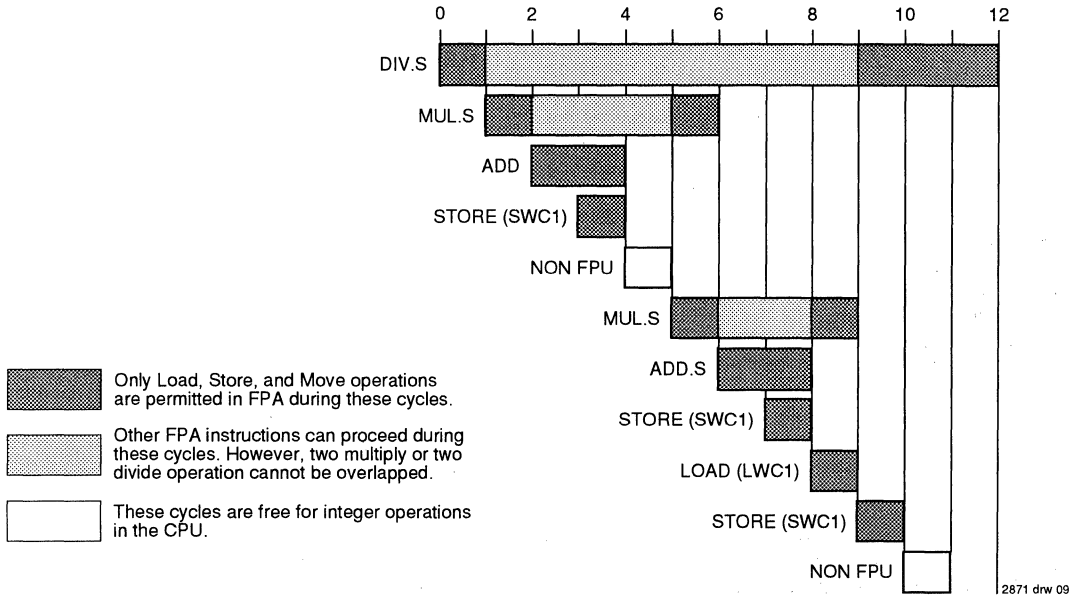


Figure 9. Examples of Overlapping Floating Point Operation

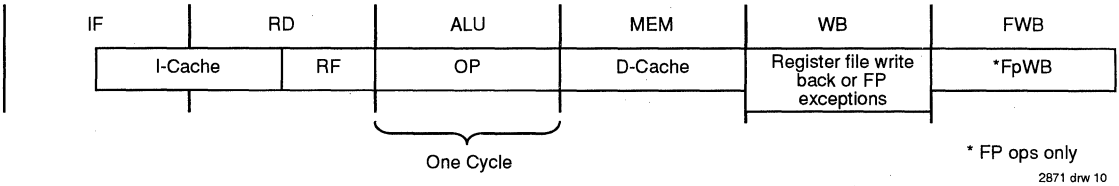


Figure 10. Instruction Execution

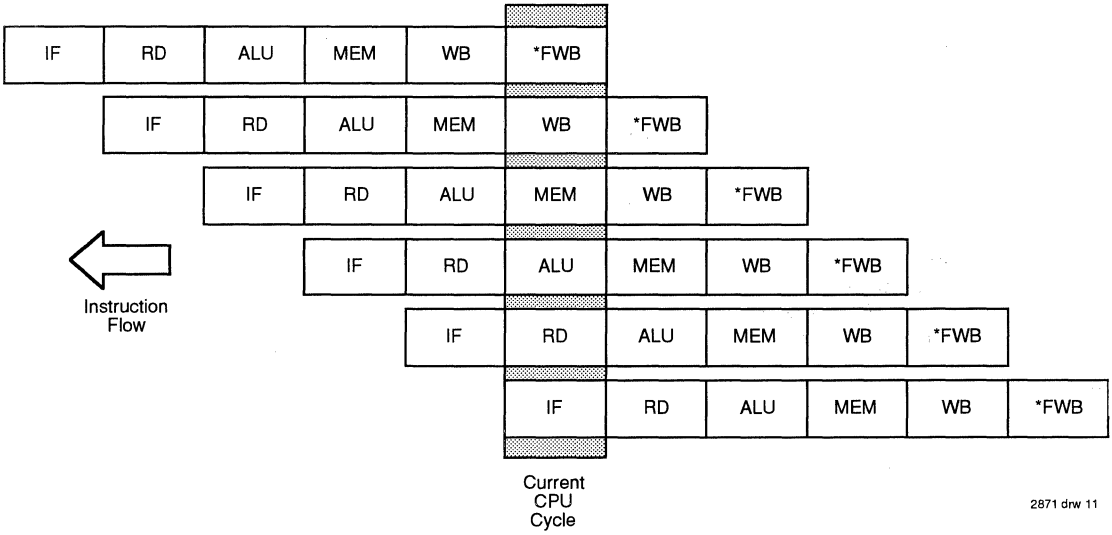


Figure 11. IDT79R3500 Execution Sequence

IDT79R3500 PIPELINE ARCHITECTURE

The execution of a single IDT79R3500 integer instruction consists of five pipe stages while floating point instruction takes six pipe stages. They are:

1) IF—Instruction fetch. The processor calculates the instruction address required to read from the I cache.
2) RD—The instruction is present on the data bus during phase one of this pipe stage. Instruction decode occurs during phase two. Operands are read from the registers if required.
3) ALU—Perform the required operation on instruction operands. If this is a FPA instruction, instruction execution commences.
4) MEM—Access memory. If the instruction is a load or store, the data is presented or captured during phase 2 of this pipe stage.
5) WB—Write integer results back into register file. In FPA cycles this pipe stage is used for exceptions.
6) FWB—The FPA uses this stage to write back ALU results to its register file.

Each of these steps requires approximately one FPA cycle as shown in Figure 10. (parts of some operations spill over into another cycle while other operations require only 1/2 cycle.)

The CPU uses a five stage pipeline while while the FPA uses a 6 stage to achieve an instruction execution rate approaching one instruction per cycle. Thus, execution of six instructions at a time are overlapped as shown in Figure 11.

This pipeline operates efficiently because different CPU resources (address and data bus accesses, ALU operations, register accesses, and so on) are utilized on a non-interfering basis.

MEMORY SYSTEM HIERARCHY

The high performance capabilities of the IDT79R3500 processor demand system configurations incorporating techniques frequently employed in large, mainframe computers but seldom encountered in systems based on more traditional microprocessors.

A primary goal of systems employing RISC techniques is to minimize the average number of cycles each instruction requires for execution. Techniques to reduce cycles-per-instruction include a compact and uniform instruction set, a deep instruction pipeline (as described above), and utilization of optimizing compilers. Many of the advantages obtained from these techniques can, however, be negated by an inefficient memory system.

Figure 12 illustrates memory in a simple microprocessor system. In this system, the CPU outputs addresses to memory and reads instructions and data from memory or writes data to memory. The address space is completely undifferentiated: instructions, data, and I/O devices are all treated the same. In such a system, a primary limiting performance factor is memory bandwidth.

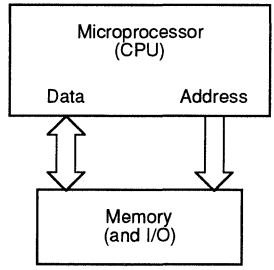


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Figure 12. A Simple Microprocessor Memory System

Figure 13 illustrates a memory system that supports the significantly greater memory bandwidth required to take full advantage of the IDT79R3500's performance capabilities. The key features of this system are:

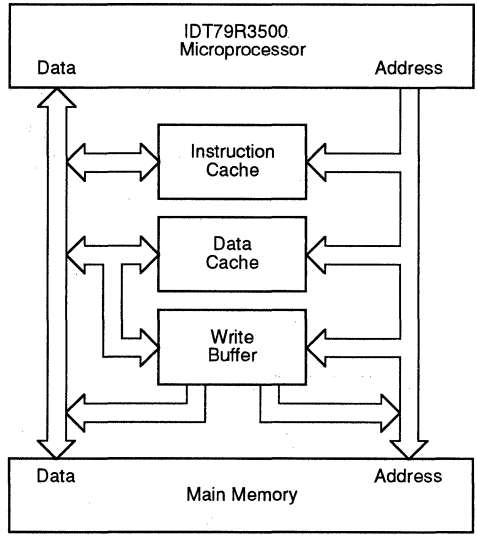

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Figure 13. An IDT79R3500 System with a High-Performance Memory System

- **External Cache Memory**—Local, high-speed memory (called cache memory) is used to hold instructions and data that is repetitively accessed by the CPU (for example, within a program loop) and thus reduces the number of references that must be made to the slower-speed main memory. Some microprocessors provide a limited amount of cache memory on the CPU chip itself. The external caches supported by the IDT79R3500 can be much larger; while a small cache can improve performance of some programs, significant improvements for a wide range of programs require large caches.
- **Separate Caches for data and Instructions**—Even with high-speed caches, memory speed can still be a limiting factor because of the fast cycle time of a high-performance microprocessor. The IDT79R3500 supports separate caches for instructions and data and alternates accesses of the two caches during each CPU cycle. Thus, the processor can obtain data and instructions at the cycle rate of the CPU using caches constructed with commercially available IDT static RAM devices.

  In order to maximize bandwidth in the cache while minimizing the requirement for SRAM access speed, the IDT79RR3500 divides a single-processor clock cycle into two phases. During one phase, the address for the data cache access is presented while data previously addressed in the instruction cache is read; during the next phase, the data operation is completed while the instruction cache is being addressed. Thus, both caches are read in a single processor cycle using only one set of address and data pins.
- **Write Buffer**—in order to ensure data consistency, all data that is written to the data cache must also be written out to main memory. The cache write model used by the IDT79R3500 is that of a write-through cache; that is, all data written by the CPU is immediately written into the main memory. To relieve the CPU of this responsibility (and the inherent performance burden) the IDT79R3500 supports an interface to a write buffer. The IDT79R3020 Write Buffer captures data (and associated addresses) output by the CPU and ensures that the data is passed on to main memory.

IDT79R3500 Processor Subsystem Interfaces

Figure 14 illustrates the three subsystem interfaces provided by the IDT79R3500 processor:

- **Cache control** interface (on-chip) for separate data and instruction caches permits implementation of off-chip caches using standard IDT SRAM devices. The IDT79R3500 directly controls the cache memory with a minimum of external components. Both the instruction and data cache can vary from 0 to 256kB (64K entries). The IDT79R3500 also includes the TAG control logic which determines whether or not the entry read from the cache is the desired data. The IDT79RR3500 implements an advanced feature that allows certain tag comparisons to be eliminated, which in turn reduces the number of cache SRAMs required. The Int(5) reset mode vector contains two bits which sets the tag comparison options. Table 3 illustrates the tag disable encoding. The first row in the table implements the standard IDT79R3000A operating mode where all the tag and tag parity are used. The second row eliminates the upper 4 tag bits, eliminating normally required SRAMs and limiting main memory addressing to 128mB. The third row elimnates the lower 4 tag bits, which requires the cache to be at least 64kB each. The fourth row eliminates the upper 4 and lower 4 tag bits, requiring at least 16K cache entries, and limits main memory addressing to 128mB. In all cases, the IDT79R3500 continues to check tag parity which are selected as driven from the cache. The IDT79R3500 cache controller implements a direct mapped cache for high net performance (bandwidth). It has the ability to refill multiple words when a cache miss occurs, thus reducing the effective miss rate to less than 2% for large caches. When a cache miss occurs, the IDT79R3500 can support refilling the cache in 1, 4, 8, 16, or 32 word blocks to minimize the effective penalty of having to access main memory. The IDT79R3500 also incorporates the ability to perform instruction streaming; while the cache is refilling, the processor can resume execution once the missed word is obtained from main memory. In this way, the processor can continue to execute concurrently with the cache block refill.
- **Memory controller** interface for system (main) memory. This interface also includes the logic and signals to allow operation with a write buffer to further improve memory bandwidth. In addition to the standard full word access, the memory controller supports the ability to write bytes and half-words by using partial word operations. The memory controller also supports the ability to retry memory accesses if, for example, the data returned from memory is invalid and a bus error needs to be signalled.
- **Coprocessor Interface**—The IDT79R3500 features a set of on board tightly coupled coprocessors. Coprocessor 0 is defined to be the system control coprocessor and Coprocessor 1 is the Floating Point Accelerator. They have direct access to the internal data bus which allows them direct load and store of data in the same fashion as accessing the CPU registers. This relieves the typical bottleneck of having to load data into the CPU register set and then passing that data off to the co-processors.

  In applications where the FPA was off chip, as in using the IDT79R3010A, several control pins were used for communications with the CPU and a Phase Lock Loop was located on the IDT79R3010A to synchronize the two together. As they are now integrated into a single chip, these are no longer needed. The FpCond output, which is used in coprocessor branch instructions, is now internally tied to the CpCond(1) input of the CPU leaving the external CpCond(1) pin available for another function. This signal is selectable to either output the FpBusy or the FpInt. Cp

5

Cond(1) output selection is determined at reset time according to the value read on Int(4). Table 4 illustrates the options that allow the FpInt to be routed to either the CpCond(1) output, or one of the internal Int pins. If it is internally routed, that interrupt is dedicated and that input will no longer affect the IDT79R3500. The selection of using CpCond(1) allows some external Logic to be added to the path, which might be required in some applications. Another method for Fpint handling is also accommodated. A mode pin, previously Vcc can be programmed to route the FPU interrupt to a dedicated Fpint output that was previously a GND. If the mode pin is sampled at reset as a 0, the dedicated Fpint indicates the FPU interrupt - if a 1, then the routing of Table 4 applies.

The internal CPBusy input, which is used to stall the CPU if the coprocessor needs to hold off subsequent operations, has two sources-FPBusy and the external CpBusy pin which are logically ORed together. Further, Run and Exception of both the FPA and CPU are internally tied and brought out with the external CPBusy input to accommodate off chip coprocessor 2 and 3. This external interface is available to support application specific functions.

Tag Mode 1	Tag Mode 0	Check Which TAGs	Ignore Which Tags
0	0	Tag (31:12)	None
0	1	Tag (27:12)	Tag (31:28)
1	0	Tag (31:16)	Tag (15:12)
1	1	Tag (27:16)	Tag (31:28;15:12)

2871 tbl 03

Table 3. Tag Disable Encoding

W Cycle	X Cycle	Y Cycle	Z Cycle	Action
X	X	X	"HIGH"	FPint driven onto CpCond(1)
"LOW"	"LOW"	"LOW"	"LOW"	Use Int(3) for Fpint
"LOW"	"LOW"	"HIGH"	"LOW"	Use Int(1) for Fpint
"LOW"	"HIGH"	"LOW"	"LOW"	Use Int(2) for Fpint
"LOW"	"HIGH"	"HIGH"	"LOW"	Use Int(0) for Fpint
'HIGH"	"LOW"	"LOW"	"LOW"	Use Int(4) for Fpint
'HIGH"	"LOW"	"HIGH"	"LOW"	Use Int(5) for Fpint
'HIGH"	"HIGH"	"LOW"	"LOW"	Reserved, Undefined
'HIGH"	"HIGH"	"HIGH"	"LOW"	Reserved, Undefined

2871 tbl 04

Table 4. Int(4) Encoding for Fpint

MULTIPROCESSING SUPPORT

The IDT79R3500 supports multiprocessing applications in a simple but effective way. Multiprocessing applications require cache coherency across the multiple processors. The IDT79R3500 offers two signals to support cache coherency: the first, MPStall, stalls the processor within two cycles of being received and keeps it from accessing the cache. This allows an external agent to snoop into the processor data cache. The second signal, MPInvalidate, causes the processor to write data on the data cache bus which indicates the externally addressed cache entry is invalid. Thus, a subsequent access to that location would result in a cache miss, and the data would be obtained from main memory.

The two MP signals would be generated by a external logic which utilizes a secondary cache to perform bus snooping functions. The IDT79R3500 does not impose an architecture for this secondary cache, but rather is flexible enough to support a variety of application specific architectures and still maintain cache coherency. Further, there is no impact on designs which do not require this feature. The IDT79R3500 further allows the use of cache RAMs with internal address latches in multiprocessor systems.

ADVANCED FEATURES

The IDT79R3500 offers a number of additional features such as the ability to swap the instruction and data caches, facilitating diagnostics and cache flushing. Another feature isolates the, caches, which forces cache hits to occur regardless of the contents of the tag fields. The IDT79R3500 allows the processor to execute user tasks of the opposite byte ordering (endianness) of the operating system, has a programmable Tag width bus, and further allows certain parity checking to be disabled. More details on these features can be found in the *IDT79R3000A Family Hardware User's Manual.*

Further features of the IDT79R3500 are configured during the last four cycles prior to the negation of the RESET input. These functions include the ability to select cache sizes and cache refill block sizes; the ability to utilize the multiprocessor interface; whether or not instruction streaming is enabled; whether byte ordering follows "Big-Endian" or "Little-Endian" protocols, etc. Additionally, the IDT79R3500 mode must be

true to enable any of the new features that the X,Y, and Z cycles define. Table 6 shows the configuration options selected at Reset. These are further discussed in the *IDT79R3000A Family Hardware User's Manual.*

BACKWARD COMPATIBILITY

The primary goal of the IDT79R3500 is the ability to replace the IDT79R3000A and IDT79R3010A with a single chip solution. The pinout of the IDT79R3500 has been selected to ensure this compatibility, with new functions mapped onto previously used pins. The instruction set is compatible with that of the R2000 at the binary level. As a result, code written for the older processor can be executed.

In most IDT79R3000A applications, the IDT79R3500 can be placed in the socket with no modification to initialization settings. Additionally, the IDT79R3500 can be used in systems that did not include the IDT79R3010 in the original design. Further application assistance on these topics are available from IDT.

PACKAGE THERMAL SPECIFICATIONS

The IDT79R3500 utilizes special packaging techniques to improve both the thermal and electrical characteristics of the microprocessor.

In order to improve the electrical characteristics of the device, the package is constructed using multiple signal planes, including individual power planes and ground planes to reduce noise associated with high-frequency TTL parts. In addition, the 161-pin PGA package utilizes extra power and ground pins to reduce the inductance from the internal power planes to the power planes of the PC Board.

In order to improve the thermal characteristics of the microprocessor, the device is housed using cavity down packaging. In addition, these packages incorporate a copper-tungsten thermal slug designed to efficiently transfer heat from the die to the case of the package, and thus effectively lower the thermal resistance of the package. The use of an additional external heat sink affixed to the package thermal slug further decreases the effective thermal resistance of the package.

The case temperature may be measured in any environment to determine whether the device is within the specified operating range. The case temperature should be measured at the center of the top surface opposite the package cavity (the package cavity is the side where the package lid is mounted).

The equivalent allowable ambient temperature, T_A, can be calculated using the thermal resistance from case to ambient ($\varnothing ca$) for the given package. The following equation relates ambient and case temperature:

$$T_A = T_C - P * \varnothing ca$$

where P is the maximum power consumption, calculated by using the maximum Icc from the DC Electrical Characteristics section.

Typical values for $\varnothing ca$ at various airflows are shown in Table 5 for the various CPU packages.

	Airflow - (ft/min)					
	0	200	400	600	800	1000
$\varnothing ca$ (161-PGA)	21	7	3	2	1	0.5
$\varnothing ca$ (160 MQUAD)	17	11	9	8	7	6.5

2871 tbl 05

Table 5. R3500 Package Characteristics

Input	W Cycle	X Cycle	Y Cycle	Z Cycle
$\overline{Int0}$	$\overline{DBlkSize0}$	$\overline{DBlkSize1}$	Extend Cache	$\overline{Big\ Endian}$
$\overline{Int1}$	$\overline{IBlkSize0}$	$\overline{IBlkSize1}$	$\overline{MPAdrDisable}$	$\overline{TriState}$
$\overline{Int2}$	$\overline{DispPar/RevEnd}$	IStream	$\overline{IgnoreParity}$	$\overline{NoCache}$
$\overline{Int3}$	Reserved(1)	StorePartial	MultiProcessor	BusDriveOn
$\overline{Int4}$	FPINT decode	FPINT decode	FPINT decode	FPINT onto CpCond
$\overline{Int5}$	7R3500 mode	TLB disable	Tag Mode 1	Tag Mode 0

2871 tbl 06

NOTES:
1. Reserved entries must be driven high.
2. These values must be driven stable throughout the enfire RESET period.

Table 6. R3500 Mode Selectable Features

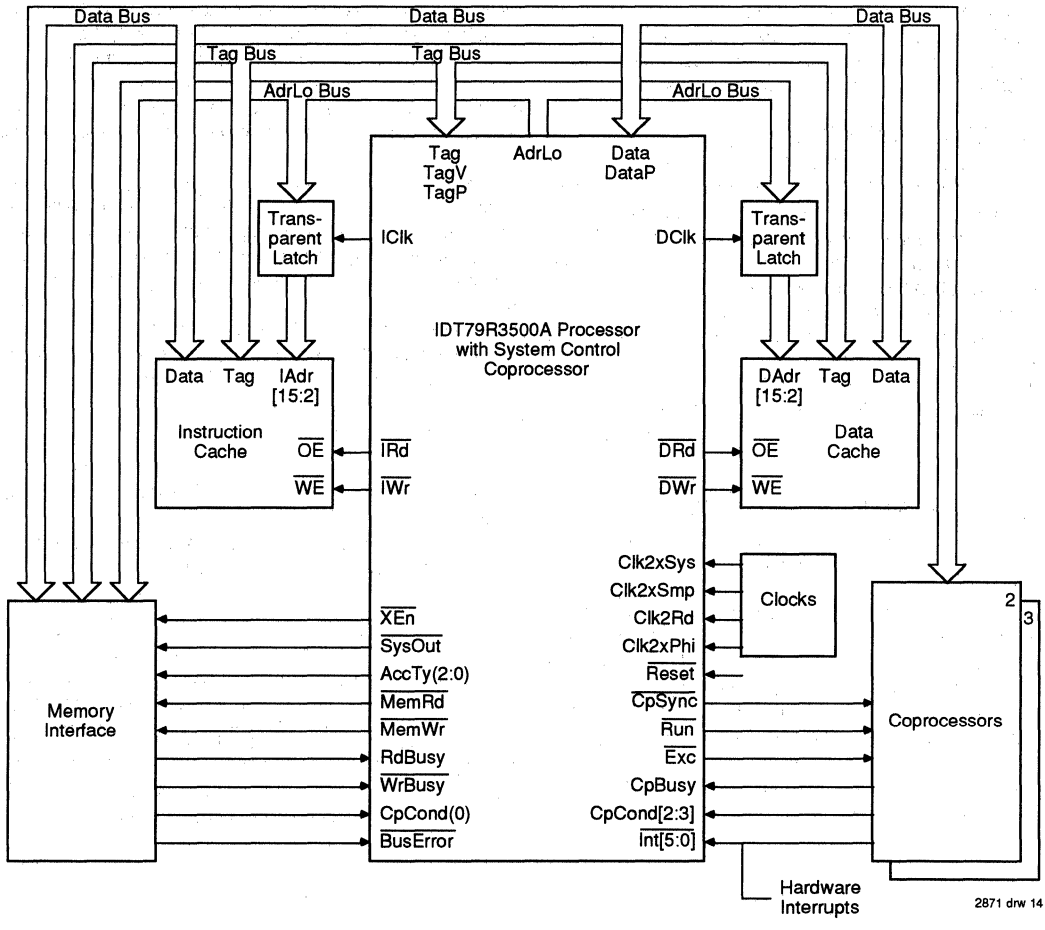

Figure 14. IDT79R3500 Subsystem Interfaces Example; 64 KB Caches

PIN CONFIGURATION

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	(No Pin)	AdrLo 6	AdrLo 10	AdrLo 11	VCC	AdrLo 14	AdrLo 15	CpCond 0	AdrLo 16	AdrLo 17	$\overline{\text{Int(2)}}$	$\overline{\text{Int(5)}}$	Wr Busy	$\overline{\text{Reset}}$	VCC
B	AdrLo 3	$\overline{\text{DRd2}}$	AdrLo 7	AdrLo 9	AdrLo 12	$\overline{\text{IRd2}}$	AdrLo 13	CpCond 1	$\overline{\text{Int(1)}}$	$\overline{\text{Int(3)}}$	Cp Busy	$\overline{\text{Bus Error}}$	$\overline{\text{DWr2}}$	Tag12	Tag15
C	AdrLo 0	AdrLo 4	Mode	AdrLo 5	AdrLo 8	GND	GND	VCC	$\overline{\text{Int(0)}}$	$\overline{\text{Int(4)}}$	Rd Busy	GND	Tag13	TagP0	Tag18
D	Data 1	AdrLo 2	$\overline{\text{FpInt}}$	GND	VCC	GND	VCC	GND	VCC	GND	VCC	GND	Tag14	Tag17	Tag19
E	DataP 0	Data 0	AdrLo 1										Tag16	Tag20	VCC
F	VCC	Data 7	Data 2										GND	Tag21	Tag23
G	Data 4	Data 3	GND										GND	Tag22	TagP1
H	Data 6	Data 5	Data 8										VCC	Tag25	Tag24
J	Data 10	DataP 1	Data 9										Tag28	Tag29	Tag26
K	Data 15	Data 11	GND										GND	TagP2	Tag27
L	VCC	Data 12	Data 17										Acc Typ2	Tag31	Tag30
M	Data 13	Data 16	DataP 2	GND	VCC	GND	VCC	GND	VCC	GND	VCC	GND	GND	Acc Typ1	VCC
N	Data 14	Data 18	Data 19	GND	Data 24	DataP 3	VCC	VCC	GND	GND	$\overline{\text{DRd1}}$	$\overline{\text{Mem Wr}}$	$\overline{\text{Mem Rd}}$	$\overline{\text{Run}}$	TagV
P	Data 23	Data 20	$\overline{\text{IWr2}}$	Data 22	Data 26	Data 27	$\overline{\text{XEn}}$	Data 30	Clk2x Sys	Clk2x Rd	DClk	$\overline{\text{IRd1}}$	$\overline{\text{IWr1}}$	$\overline{\text{Cp Sync}}$	Acc Typ0
Q	VCC	Data 21	Data 25	Data 31	Data 28	GND	Data 29	$\overline{\text{Excep-tion}}$	Clk2x Phi	Clk2x Smp	$\overline{\text{SysOut}}$	VCC	IClk	$\overline{\text{DWr1}}$	VCC

2871 drw 16

NOTE:

1. AdrLo 16 and 17 are multifunction pins which are controlled by mode select programming on interrupt pins at reset time
   AdrLo 16: MP Invalidate, CpCond (2).
   AdrLo 17: MP Stall, CpCond (3).
2. This package is pin-compatible with the 175-pin PGA for the R3000A.

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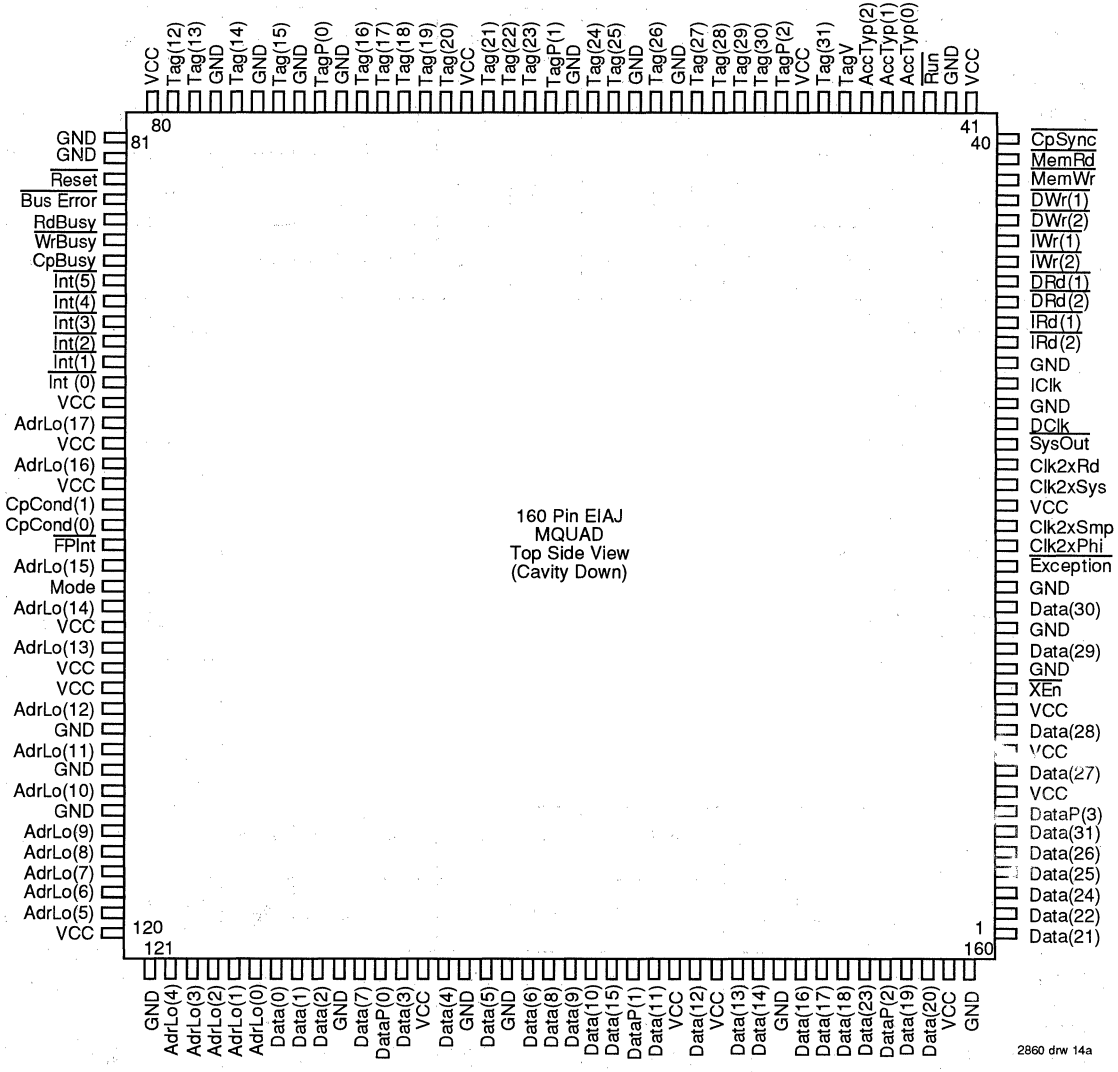
PIN CONFIGURATION



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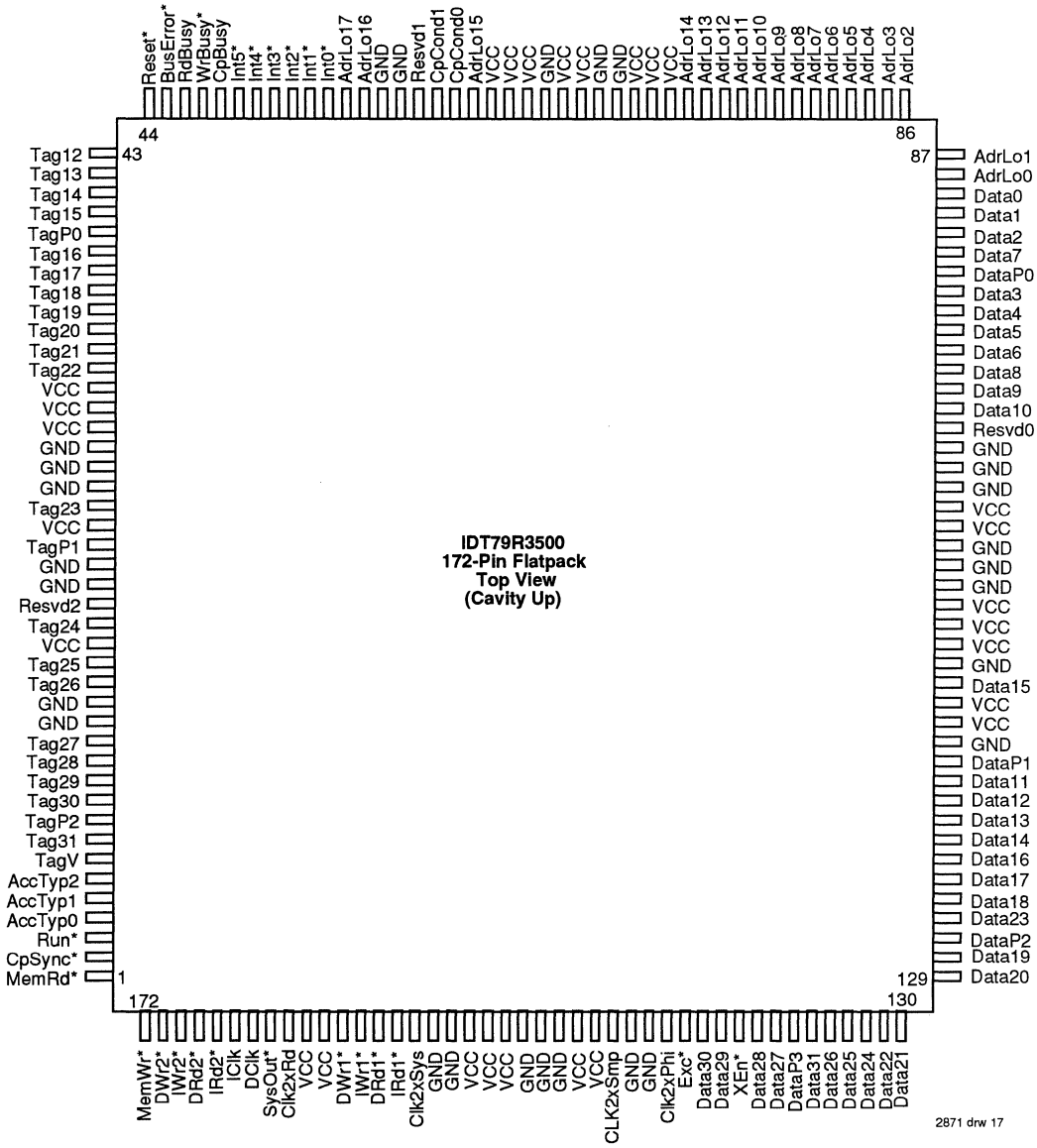
PIN CONFIGURATION



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PIN DESCRIPTIONS

Pin Name	I/O	Description
Data (0-31)	I/O	A 32-bit bus used for all instruction and data transmission among the processor, caches, memory interface, and coprocessors.
DataP (0-3)	I/O	A 4-bit bus containing even parity over the data bus.
Tag (12-31)	I/O	A 20-bit bus used for transferring cache tags and high addresses between the processor, caches, and memory interface.
TagV	I/O	The tag validity indicator.
Tag P (0-2)	I/O	A 3-bit bus containing even parity over the concatenation of TagV and Tag.
AdrLo (0-17)	O	An 18-bit bus containing byte addresses used for transferring low addresses from the processor to the caches and memory interface. (AdrLo 16: CpCond (2), AdrLo 17: CpCond (3) set by reset initialization).
$\overline{\text{IRd1}}$	O	Read enable for the instruction cache.
$\overline{\text{IWr1}}$	O	Write enable for the instructon cache.
$\overline{\text{IRd2}}$	O	An identical copy of $\overline{\text{IRd1}}$ used to split the load.
$\overline{\text{IWr2}}$	O	An identical copy of $\overline{\text{IWr1}}$ used to split the load.
IClk	O	The instruction cache address latch clock. This clock runs continuously.
$\overline{\text{DRd1}}$	O	The read enable for the data cache.
$\overline{\text{DWr1}}$	O	The write enable for the data cache.
$\overline{\text{DRd2}}$	O	An identical copy of $\overline{\text{DRd1}}$ used to split the load.
$\overline{\text{DWr2}}$	O	An identical copy of $\overline{\text{DWr1}}$ used to split the load.
DClk	O	The data cache address latch clock. This clock runs continuously.
$\overline{\text{XEn}}$	O	The read enable for the Read Buffer.
AccTyp(0-2)	O	A 3-bit bus used to indicate the size of data being transferred on the data bus, whether or not a data transfer is occurring, and the purpose of the transfer.
$\overline{\text{MemWr}}$	O	Signals the occurrence of a main memory write.
$\overline{\text{MemRd}}$	O	Signals the occurrence of a main memory read.
$\overline{\text{BusError}}$	I	Signals the occurrence of a bus error during a main memory read or write.
$\overline{\text{Run}}$	O	Indicates whether the processor is in the RUN or STALL state. In the discrete design, the R3000 $\overline{\text{Run}}$ output is tied directly to the R3010 $\overline{\text{Run}}$ input. In theIDT79 R3500, this is done internally, but the $\overline{\text{Run}}$ signal is also brought out for application specific coprocessors.
$\overline{\text{Exception}}$	O	Indicates that the instruction that is about to commit to a state change should be aborted; also indicates other exception related information. In the discrete design, the R3000 $\overline{\text{Exception}}$ output is tied to the IDT79R3010 $\overline{\text{Exception}}$ input. In the IDT79R3500 this is done internally, but the $\overline{\text{Exception}}$ signal is also brought out for application specific coprocessors.
$\overline{\text{CpSync}}$	O	A clock which is identical to $\overline{\text{SysOut}}$ and used by external coprocessors for timing synchronization with the IDT79R3500. In the discrete design, $\overline{\text{CpSync}}$ output from the IDT79R3000 is tied to the IDT79R3010 $\overline{\text{FPSync}}$ input. In the IDT79R3500, this is done internally, but the $\overline{\text{CpSync}}$ signal is also brought out for application specific coprocessors.
RdBusy	I	The main memory read stall termination signal. In most system designs RdBusy is normally asserted and is deasserted only to indicate the successful completion of a memory read. RdBusy is sampled by the processor only during memory read stalls.
$\overline{\text{WrBusy}}$	I	The main memory write stall initiation/termination signal.
$\overline{\text{CpBusy}}$	I	Input used to indicate that the requested coprocessor resource is unavailable, or used to preserve the precise exception model. In the descrete design, $\overline{\text{CpBusy}}$ is driven directly by the R3010 $\overline{\text{FpBusy}}$ output. In the IDT79R3500 the $\overline{\text{CpBusy}}$ input of the CPU is the logical OR of both the internal FPA $\overline{\text{FpBusy}}$ and the external $\overline{\text{CpBusy}}$ pin. This input is provided for external application specific coprocessors. An internal pull down resistor is provided if this input is left open.
CpCond(1)	O	Signal used by the branch on Coprocessor 1 true/false instruction. In discrete systems using a IDT79R3010 FPA, this is normally tied to the FpCond output. In the IDT79R3500, the internal $\overline{\text{FpCond}}$ is directly tied to the internal CpCond(1) input leaving this pin available for other functions. This pin defaults to output the FpBusy internal signal or, (via the Reset vectors), output the FPInt—in the latter case, external hardware must route this signal to the appropriate Int pin.
CpCond (0,2-3)	I	Conditional branch status from coprocessors to the processor. Function is provided on AdrLo 16/17 pins and is selected at reset time.
MPStall	I	Multiprocessing Stall. Signals to the processor that it should stall accesses to the caches in a multiprocessing environment. This is physically the same pin as CpCond3; its use is determined at RESET initialization.
MPInvalidate	I	Multiprocessing Invalidate. Signals to the processor that it should issue invalidate data on the cache data bus. The address to be invalidated is externally provided. This is the same pin as CpCond2; its use is determined at RESET initialization.
$\overline{\text{Int (0-5)}}$	I	A 6-bit bus used by the memory interface and coprocessors to signal maskable interrupts to the IDT79R3500. This bus is also used at reset time to select among the mode-selectable features of the IDT79R3500. The FPA $\overline{\text{FPInt}}$ output signal is typically connected to one of these interrupt lines; the choice is programmable through the reset vectors with the default being Int(3).

PIN DESCRIPTIONS (Continued)

Pin Name	I/O	Description
Clk2xSys	I	The master double frequency input clock used for generating $\overline{SysOut}$.
Clk2xSmp	I	A double frequency clock input used to determine the sample point for data coming into the processor and coprocessors.
Clk2xRd	I	A double frequency clock input used to determine the enable time of the cache RAMs.
Clk2xPhi	I	A double frequency clock input used to determine the position of the internal phases, phase1 and phase2.
$\overline{Reset}$	I	Synchronous initialization input used to force execution starting from the reset memory address. $\overline{Reset}$ must be deasseted synchronously but asserted asynchronously. The deassertion of $\overline{Reset}$ must be synchronized by the leading edge of $\overline{SysOut}$.
Mode	I	If the mode input is sampled as a '1' at the rising edge of reset, the connection between FpInt and the CPU interrrupt bus will be established via the interrept reset vector. Vcc should be used to establish this option. If mode is sampled as a 0 at the rising edge of reset, the FpInt will be an output, and must be externally connected back to a CPU interrupt input pin. Ground should be used to select this option.
$\overline{FPINT}$	O	If the mode pin is sampled as a 0 at the rising edge of reset, this signal will be the FPInt output from the FPA core of the IDT79R3500, and must be externally connected back to a CPU interrupt pin. If the mode pin is sampled as a 1 at the rising edge of reset, this pin should be grounded.

2871 tbl 07

ABSOLUTE MAXIMUM RATINGS(1, 3)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A, T_C	Operating Temperature	0 to +70(4) (Ambient) 0 to +90(5) (Case)	–55 to +125 (Case)	°C
T_{BIAS}	Case Temperature Under Bias	–55 to +125(4) 0 to +90(5)	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +155	°C
I_{IN}	Input Voltage	–0.5 to +7.0	–0.5 to +7.0	V

2871 tbl 08

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN} minimum = –3.0V for pulse width less than 15ns. V_{IN} should not exceed V_{CC} +0.5 Volts.
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.
4. 16-33 MHz only.
5. 37-40 MHz only.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military 20-25 MHZ	–55°C to +125°C (Case)	0V	5.0 ±10%
Commercial 20-33 MHz	0°C to +70°C (Ambient)	0V	5.0 ±5%
Commercial 40 MHz	0°C to +90°C (Case)	0V	5.0 ±5%

2871 tbl 10

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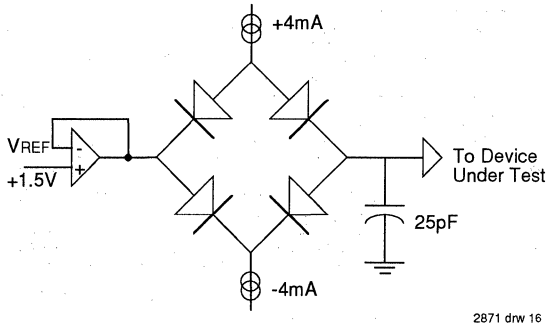
AC TEST CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{IH}	Input HIGH Voltage	3.0	—	V
V_{IL}	Input LOW Voltage	—	0.4	V
V_{IHS}	Input HIGH Voltage	3.5	—	V
V_{ILS}	Input LOW Voltage	—	0.4	V

2871 tbl 09

OUTPUT LOADING FOR AC TESTING



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DC ELECTRICAL CHARACTERISTICS
COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to +70°C, V_{CC} = +5.0V ±5%)

			79R3500						
			20.0MHz		25.0MHz		33.33MHz		
Symbol	Parameter	Test Conditions	Min.	Max.	Min.	Max.	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4mA	3.5	—	3.5	—	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	—	0.4	—	0.4	—	0.4	V
V_{OHC}	Output HIGH Voltage(7)	V_{CC} = Min., I_{OH} = –4mA	4.0	—	4.0	—	4.0	—	V
V_{OHT}	Output HIGH Voltage(4,6)	V_{CC} = Min., I_{OH} = –8mA	2.4	—	2.4	—	2.4	—	V
V_{OLT}	Output LOW Voltage(4,6)	V_{CC} = Min., I_{OL} = 8mA	—	0.8	—	0.8	—	0.8	V
V_{IH}	Input HIGH Voltage(5)		2.0	—	2.0	—	2.0	—	V
V_{IL}	Input LOW Voltage(1)		—	0.8	—	0.8	—	0.8	V
V_{IHS}	Input HIGH Voltage(2,5)		3.0	—	3.0	—	3.0	—	V
V_{ILS}	Input LOW Voltage(1,2)		—	0.4	—	0.4	—	0.4	V
C_{IN}	Input Capacitance(6)		—	10	—	10	—	10	pF
C_{OUT}	Output Capacitance(6)		—	10	—	10	—	10	pF
I_{CC}	Operating Current	V_{CC} = 5V, T_A = 70°C	—	550	—	650	—	750	mA
I_{IH}	Input HIGH Leakage(3)	V_{IH} = VCC	—	100	—	100	—	100	µA
I_{IL}	Input LOW Leakage(3)	V_{IL} = GND	–100	—	–100	—	–100	—	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = VCC, V_{OL} = GND	–100	100	–100	100	–100	100	µA

2871 tbl 11

NOTES:

1. V_{IL} Min. = –3.0V for pulse width less than 15ns. V_{IL} should not fall below –0.5 Volts for larger periods.
2. V_{IHS} and V_{ILS} apply to Clk2xSys, Clk2xSmp, Clk2xRd, Clk2xPhi, CpBusy, and $\overline{\text{Reset}}$.
3. These parameters do not apply to the clock inputs.
4. V_{OHT} and V_{OLT} apply to the bidirectional data and tag busses only. Note that V_{IH} and V_{IL} also apply to these signals. V_{OHT} and V_{OLT} are provided to give the designer further information about these specific signals.
5. V_{IH} should not be held above V_{CC} + 0.5 volts.
6. Guaranteed by design.
7. V_{OHC} applies to $\overline{\text{RUN}}$ and $\overline{\text{Exception}}$.

DC ELECTRICAL CHARACTERISTICS
MILITARY TEMPERATURE RANGE (TC = -55°C to +125°C, VCC = +5.0V ±10%)

Symbol	Parameter	Test Conditions	79R3500				Unit
			20.0MHz		25.0MHz		
			Min.	Max.	Min.	Max.	
VOH	Output HIGH Voltage	VCC = Min., IOH = –4mA	3.5	—	3.5	—	V
VOL	Output LOW Voltage	VCC = Min., IOL = 4mA	—	0.4	—	0.4	V
VOHC	Output HIGH Voltage(7)	VCC = Min., IOH = –4mA	4.0	—	4.0	—	V
VOHT	Output HIGH Voltage(4,6)	VCC = Min., IOH = –8mA	2.4	—	2.4	—	V
VOLT	Output LOW Voltage(4,6)	VCC = Min., IOL = 8mA	—	0.8	—	0.8	V
VIH	Input HIGH Voltage(5)		2.0	—	2.0	—	V
VIL	Input LOW Voltage(1)		—	0.8	—	0.8	V
VIHS	Input HIGH Voltage(2,5)		3.0	—	3.0	—	V
VILS	Input LOW Voltage(1,2)		—	0.4	—	0.4	V
CIN	Input Capacitance(6)		—	10	—	10	pF
COUT	Output Capacitance(6)		—	10	—	10	pF
ICC	Operating Current	VCC = 5V, TA = 70°C	—	800	—	875	mA
IIH	Input HIGH Leakage(3)	VIH = VCC	—	100	—	100	µA
IIL	Input LOW Leakage(3)	VIL = GND	–100	—	–100	—	µA
IOZ	Output Tri-state Leakage	VOH = VCC, VOL = GND	–100	100	–100	100	µA

2871 tbl 12

NOTES:

1. VIL Min. = –3.0V for pulse width less than 15ns. VIL should not fall below –0.5 Volts for larger periods.
2. VIHS and VILS apply to Clk2xSys, Clk2xSmp, Clk2xRd, Clk2xPhi, CpBusy, and $\overline{\text{Reset}}$.
3. These parameters do not apply to the clock inputs.
4. VOHT and VOLT apply to the bidirectional data and tag busses only. Note that VIH and VIL also apply to these signals. VOHT and VOLT are provided to give the designer further information about these specific signals.
5. VIH should not be held above VCC + 0.5 volts.
6. Tested only initially, and after design changes which may affect capacitance.
7. VOHC applies to $\overline{\text{RUN}}$ and $\overline{\text{Exception}}$.

5

DC ELECTRICAL CHARACTERISTICS
COMMERCIAL TEMPERATURE RANGE (T_C = 0°C to +90°C, V_{CC} = +5.0V ±5%)

Symbol	Parameter	Test Conditions	79R3500 40.0MHz Min.	79R3500 40.0MHz Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4mA	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	—	0.4	V
V_{OHC}	Output HIGH Voltage(7)	V_{CC} = Min., I_{OH} = –4mA	4.0	—	V
V_{OHT}	Output HIGH Voltage(4,6)	V_{CC} = Min., I_{OH} = –8mA	2.4	—	V
V_{OLT}	Output LOW Voltage(4,6)	V_{CC} = Min., I_{OL} = 8mA	—	0.8	V
V_{IH}	Input HIGH Voltage(5)		2.0	—	V
V_{IL}	Input LOW Voltage(1)		—	0.8	V
V_{IHS}	Input HIGH Voltage(2,5)		3.0	—	V
V_{ILS}	Input LOW Voltage(1,2)		—	0.4	V
C_{IN}	Input Capacitance(6)		—	10	pF
C_{OUT}	Output Capacitance(6)		—	10	pF
I_{CC}	Operating Current	V_{CC} = 5V, T_A = 70°C	—	850	mA
I_{IH}	Input HIGH Leakage(3)	V_{IH} = VCC	—	100	µA
I_{IL}	Input LOW Leakage(3)	V_{IL} = GND	–100	—	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = VCC, V_{OL} = GND	–100	100	µA

2871 tbl 13

NOTES:

1. V_{IL} Min. = –3.0V for pulse width less than 15ns. V_{IL} should not fall below –0.5 Volts for larger periods.
2. V_{IHS} and V_{ILS} apply to Clk2xSys, Clk2xSmp, Clk2xRd, Clk2xPhi, CpBusy, and $\overline{\text{Reset}}$.
3. These parameters do not apply to the clock inputs.
4. V_{OHT} and V_{OLT} apply to the bidirectional data and tag busses only. Note that V_{IH} and V_{IL} also apply to these signals. V_{OHT} and V_{OLT} are provided to give the designer further information about these specific signals.
5. V_{IH} should not be held above V_{CC} + 0.5 volts.
6. Guaranteed by design.
7. V_{OHC} applies to $\overline{\text{RUN}}$ and $\overline{\text{Exception}}$.

AC ELECTRICAL CHARACTERISTICS(1,2,3)
COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to +70°C, V_{CC} = +5.0V ±5%)

Symbol	Parameter	Test Conditions	79R3500						Unit
			20.0MHz		25.0MHz		33.33MHz		
			Min.	Max.	Min.	Max.	Min.	Max.	
Clock									
TCkHigh	Input Clock HIGH(2)	Note 6	10	—	8.0	—	6.0	—	ns
TCkLow	Input Clock LOW(2)	Note 6	10	—	8.0	—	6.0	—	ns
TCkP	Input Clock Period(2)		25	500	20	500	15	500	ns
	Clk2xSys to Clk2xSmp(5)		0	tcyc/4	0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xRd(5)		0	tcyc/4	0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xPhi(5)		7.0	tcyc/4	5.0	tcyc/4	3.5	tcyc/4	ns
Run Operation									
TDEn	Data Enable(3)		—	–2.0	—	–1.5	—	–1.5	ns
TDDis	Data Disable(3)		—	–1.0	—	–0.5	—	–0.5	ns
TDVal	Data Valid	Load= 25pF	—	3.0	—	2.0	—	2.0	ns
TWrDly	Write Delay	Load= 25pF	—	4.0	—	3.0	—	2.0	ns
TDS	Data Set-up		8.0	—	6.0	—	4.5	—	ns
TDH	Data Hold(3)		–2.5	—	–2.5	—	–2.5	—	ns
TCBS	CpBusy Set-up		11	—	9.0	—	7.0	—	ns
TCBH	CpBusy Hold		–2.5	—	–2.5	—	–2.5	—	ns
TAcTy	Access Type (1:0)	Load= 25pF	—	6.0	—	5.0	—	3.5	ns
TAT2	Access Type (2)	Load= 25pF	—	14	—	12	—	8.5	ns
TMWr	Memory Write	Load= 25pF	—	23	—	18	—	9.5	ns
TExc	Exception	Load= 25pF	—	7.0	—	5.0	—	3.5	ns
TAval	Address Valid	Load= 25pF	—	2.0	—	1.5	—	1.0	ns
TIntS	$\overline{\text{Int(n)}}$ Set-up		8.0	—	6.0	—	4.5	—	ns
TIntH	$\overline{\text{Int(n)}}$ Hold		–2.5	—	–2.5	—	–2.5	—	ns
TFpbusy			—	13	—	10	—	7.0	ns
Tfpint			—	35	—	25	—	18	
Stall Operation									
TSAVal	Address Valid	Load= 25pF	—	23	—	20	—	15	ns
TSAcTy	Access Type	Load= 25pF	—	23	—	18	—	13.5	ns
TMRdi	Memory Read Initiate	Load= 25pF	1.0	23	1.0	18	1.0	13.5	ns
TMRdt	Memory Read Terminate	Load= 25pF	—	23	—	18	—	10	ns
TStl	Run Terminate	Load= 25pF	3.0	15	3.0	10	2.0	7.5	ns
TRun	Run Initiate	Load= 25pF	—	6.0	—	4.0	—	3.0	ns
TSMWr	Memory Write	Load= 25pF	3.0	23	3.0	18	2.0	9.5	ns
TSExc	Exception Valid	Load= 25pF	—	13	—	10	—	7.5	ns
Reset Initialization									
TRST	Reset Pulse Width		6.0	—	6.0	—	6.0	—	Tcyc
TprwOn	Power on (4)		3000	—	3000	—	3000	—	Tcyc
Capacitive Load Deration									
CLD	Load Derate(5)		0.5	1.0	0.5	1.0	0	1.0	ns/25pF

NOTES:

2871 tbl 14

1. All timings are referenced to 1.5V.
2. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. T_{cyc} is one CPU clock cycle (two cycles of a 2x clock).
5. With the exception of the $\overline{\text{Run}}$ signal, no two signals on a given device will derate for a given load by a difference greater than 15%.
6. Clock transition time < 2.5ns for 33.33MHz; clock transition time < 5ns for other speeds.

5

AC ELECTRICAL CHARACTERISTICS(1,2,3)

MILITARY TEMPERATURE RANGE (Tc = -55°C to +125°C, Vcc = +5.0V ±10%)

Symbol	Parameter	Test Conditions	79R3500				Unit
			20.0MHz		25.0MHz		
			Min.	Max.	Min.	Max.	
Clock							
TckHigh	Input Clock HIGH(2)	Note 6	10	—	8.0	—	ns
TckLow	Input Clock LOW(2)	Note 6	10	—	8.0	—	ns
TckP	Input Clock Period(2)		25	500	20	500	ns
	Clk2xSys to Clk2xSmp(5)		0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xRd(5)		0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xPhi(5)		7.0	tcyc/4	5.0	tcyc/4	ns
Run Operation							
TDEn	Data Enable(3)		—	–2.0	—	–1.5	ns
TDDis	Data Disable(3)		—	–1.0	—	–0.5	ns
TDVal	Data Valid	Load= 25pF	—	3.0	—	3.0	ns
TWrDly	Write Delay	Load= 25pF	—	4.0	—	3.0	ns
TDS	Data Set-up		7.0	—	6.0	—	ns
TDH	Data Hold(3)		–1.5	—	–1.5	—	ns
TCBS	CpBusy Set-up		11	—	9.0	—	ns
TCBH	CpBusy Hold		–1.5	—	–1.5	—	ns
TAcTy	Access Type (1:0)	Load= 25pF	—	6.0	—	5.0	ns
TAT2	Access Type (2)	Load= 25pF	—	14	—	12	ns
TMWr	Memory Write	Load= 25pF	—	23	—	18	ns
TExc	Exception	Load= 25pF	—	7.0	—	5.0	ns
TAval	Address Valid	Load= 25pF	—	2.5	—	2.0	ns
TIntS	$\overline{\text{Int(n)}}$ Set-up		7.0	—	6.0	—	ns
TIntH	$\overline{\text{Int(n)}}$ Hold		–1.5	—	–1.5	—	ns
Stall Operation							
TSAVal	Address Valid	Load= 25pF	—	23	—	20	ns
TSAcTy	Access Type	Load= 25pF	—	23	—	18	ns
TMRdi	Memory Read Initiate	Load= 25pF	1.0	23	—	18	ns
TMRdt	Memory Read Terminate	Load= 25pF	—	23	—	18	ns
TStl	Run Terminate	Load= 25pF	0.0	15	0.0	10	ns
TRun	Run Initiate	Load= 25pF	—	6.0	—	4.0	ns
TSMWr	Memory Write	Load= 25pF	0.0	23	0.0	18	ns
TSExc	Exception Valid	Load= 25pF	—	13	—	10	ns
Reset Initialization							
TRST	Reset Pulse Width		6.0	—	6.0	—	Tcyc
TpwrOn	Power On (4)		3000	—	3000	—	Tcyc
Capacitive Load Deration							
CLD	Load Derate(5)		0.5	1.0	0.5	1.0	ns/25pF

2871 tbl 15

NOTES:

1. All timings are referenced to 1.5V.
2. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. Tcyc is one CPU clock cycle (two cycles of a 2x clock).
5. With the exception of the $\overline{\text{Run}}$ signal, no two signals on a given device will derate for a given load by a difference greater than 15%.
6. Clock transition time < 2.5ns for 33.33MHz; clock transition time < 5ns for other speeds.

AC ELECTRICAL CHARACTERISTICS(1,2,3)
COMMERCIAL TEMPERATURE RANGE (Tc = 0°C to +90°C, Vcc = +5.0V ±5%)

Symbol	Parameter	Test Conditions	79R3500 40.0MHz Min.	79R3500 40.0MHz Max.	Unit
Clock					
TCkHigh	Input Clock HIGH(2)	Note 6	5.0	—	ns
TCkLow	Input Clock LOW(2)	Note 6	5.0	—	ns
TCkP	Input Clock Period(2)		12.5	500	ns
	Clk2xSys to Clk2xSmp(5)		0	tcyc/4	ns
	Clk2xSmp to Clk2xRd(5)		0	tcyc/4	ns
	Clk2xSmp to Clk2xPhi(5)		3.0	tcyc/4	ns
Run Operation					
	TDEn	Data Enable(3)	—	–1.5	ns
TDDIs	Data Disable(3)		—	–0.5	ns
TDVal	Data Valid	Load= 25pF	—	1.5	ns
TWrDly	Write Delay	Load= 25pF	—	2.0	ns
TDS	Data Set-up		4.0	—	ns
TDH	Data Hold(3)		–2.5	—	ns
TCBS	CpBusy Set-up		6.0	—	ns
TCBH	CpBusy Hold		–2.5	—	ns
TAcTy	Access Type (1:0)	Load= 25pF	—	3.0	ns
TAT2	Access Type (2)	Load= 25pF	—	7.5	ns
TMWr	Memory Write	Load= 25pF	—	9.0	ns
TExc	Exception	Load= 25pF	—	3.0	ns
TAval	Address Valid	Load= 25pF	—	0.5	ns
TIntS	$\overline{\text{Int(n)}}$ Set-up		4.0	—	ns
TIntH	$\overline{\text{Int(n)}}$ Hold		–2.5	—	ns
Tfpbusy			—	6.0	ns
Tfpint			—	17	ns
Stall Operation					
TSAVal	Address Valid	Load= 25pF	—	12.5	ns
TSAcTy	Access Type	Load= 25pF	—	9.0	ns
TMRdi	Memory Read Initiate	Load= 25pF	—	9.0	ns
TMRdt	Memory Read Terminate	Load= 25pF	—	9.0	ns
TStl	Run Terminate	Load= 25pF	2.0	6.0	ns
TRun	Run Initiate	Load= 25pF	—	3.0	ns
TSMWr	Memory Write	Load= 25pF	2.0	9.0	ns
TSExc	Exception Valid	Load= 25pF	—	6.0	ns
Reset Initialization					
TRST	Reset Pulse Width		6.0	—	Tcyc
TpwrOn	Power On(4)		3000	—	Tcyc
Capacitive Load Deration					
CLD	Load Derate(5)		0	1.0	ns/25pF

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NOTES:
1. All timings are referenced to 1.5V.
2. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. Tcyc is one CPU clock cycle (two cycles of a 2x clock).
5. With the exception of the $\overline{\text{Run}}$ signal, no two signals on a given device will derate for a given load by a difference greater than 15%.
6. Clock transition time < 2.5ns.

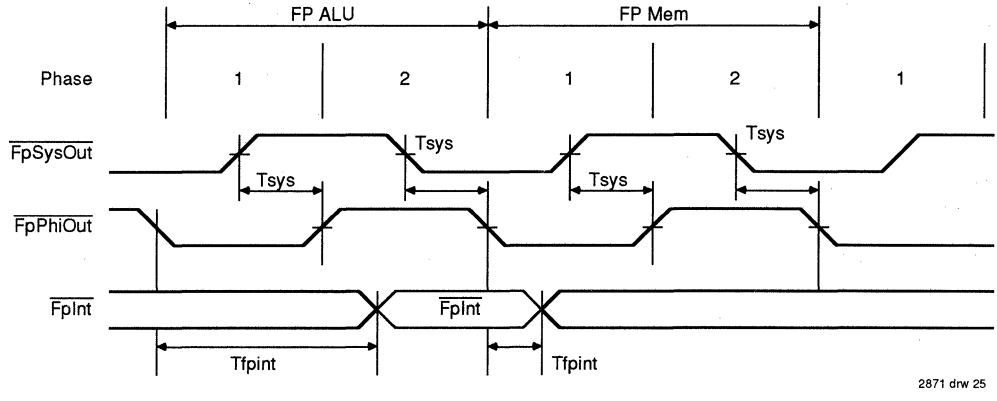

Figure 13. Floating Point Interrupt

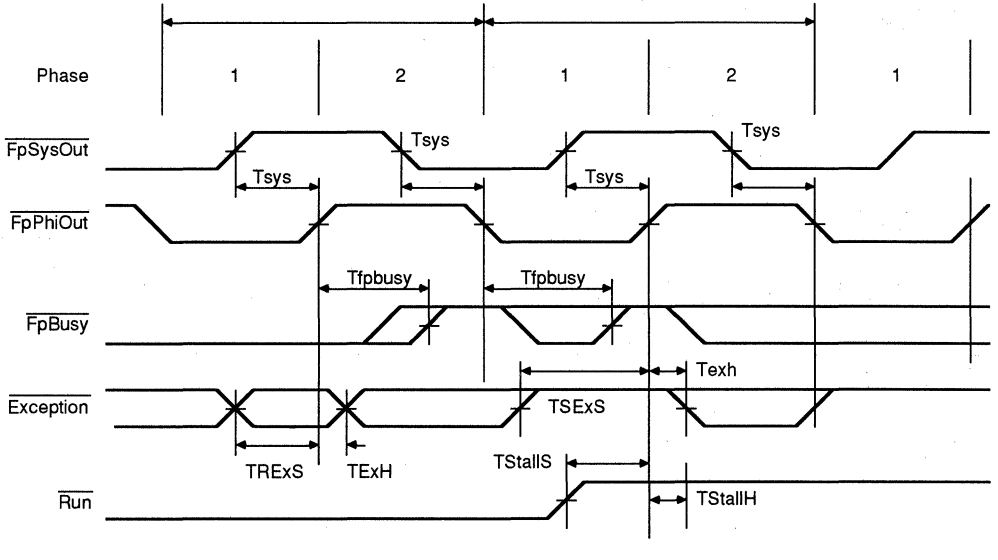

Figure 14. Floating Point Busy

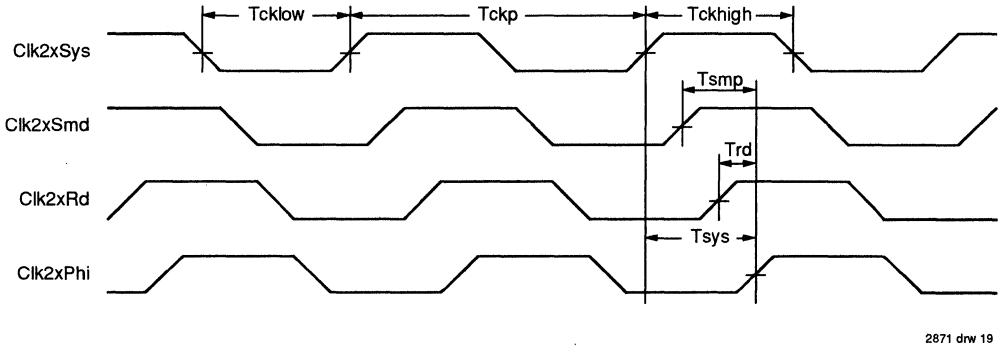

Figure 15. Input Clock Timing

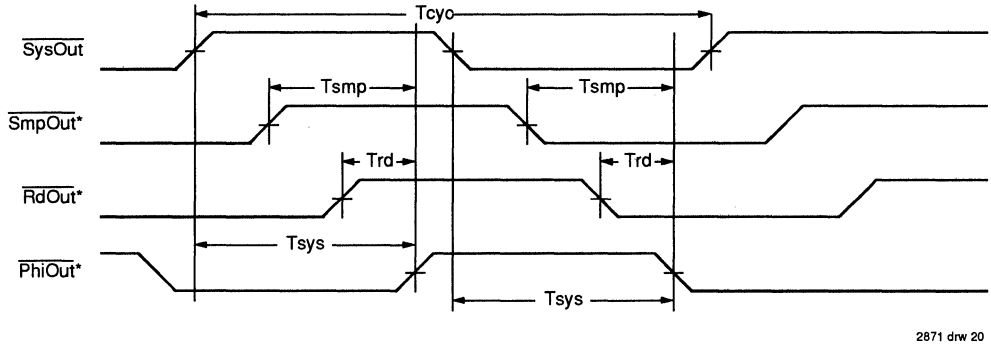

Figure 16. Processor Reference Clock Timing

* These signals are not actually output from the processor.
They are drawn to provide a reference for other timing diagrams.

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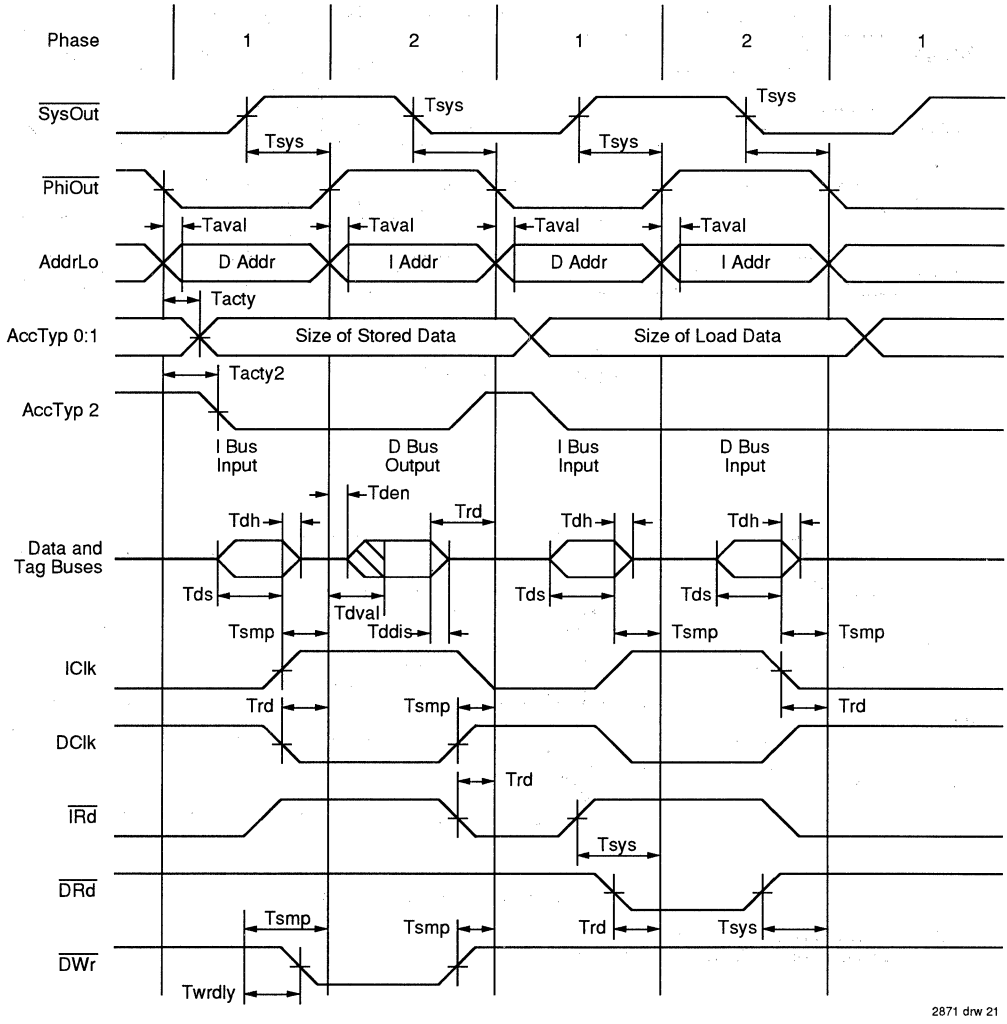

Figure 17. Synchronous Memory (Cache) Timing

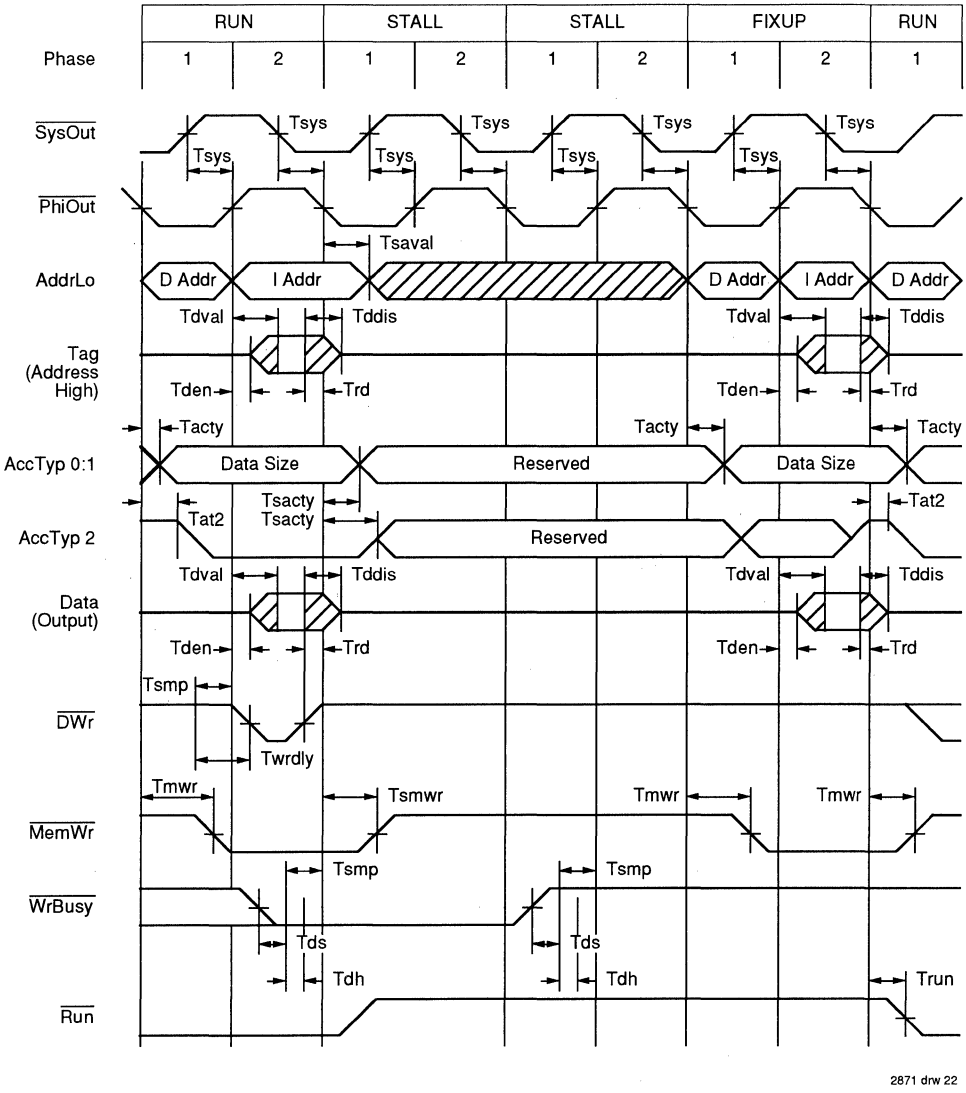

Figure 18. Memory Write Timing

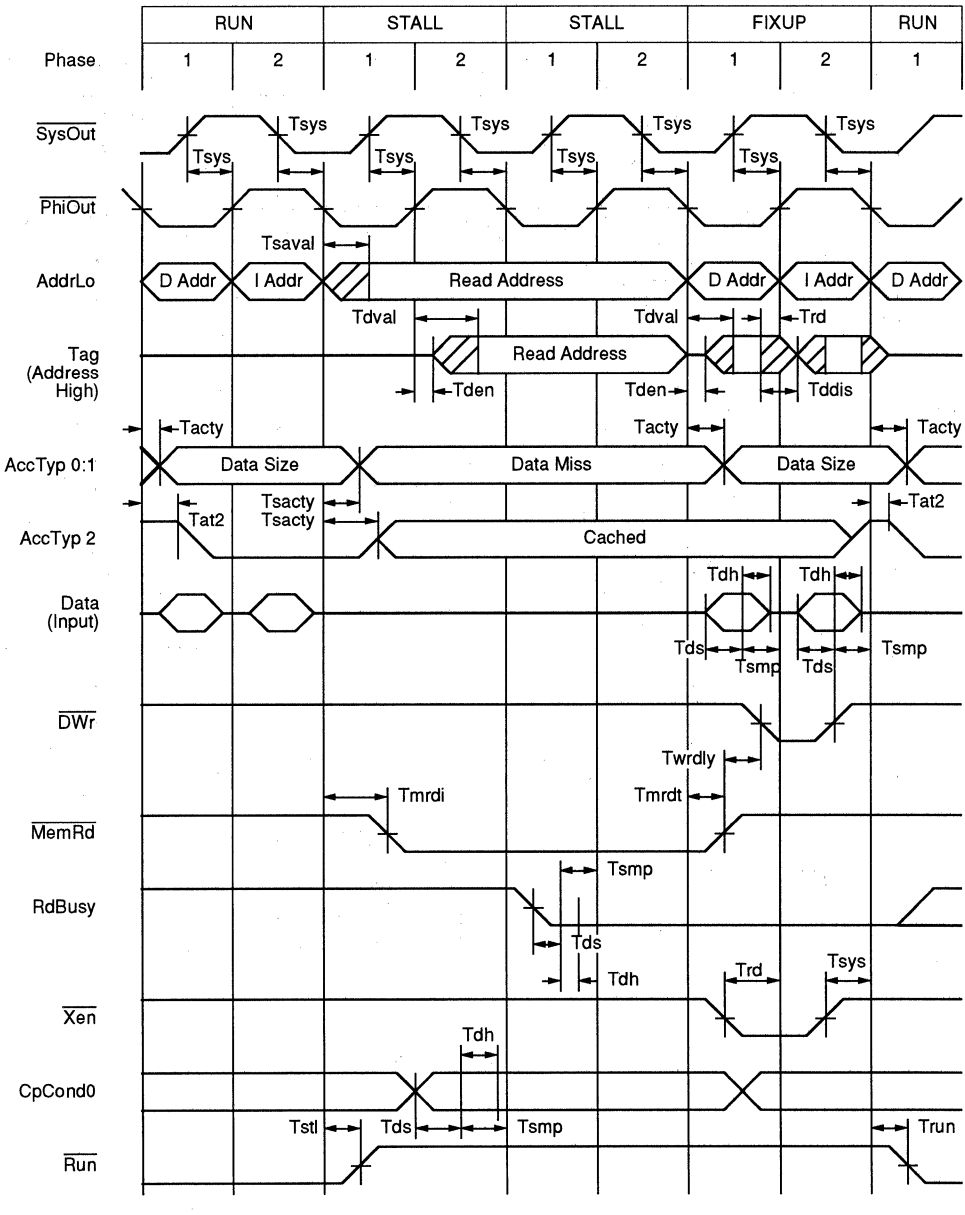

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Figure 19. Memory Read Timing

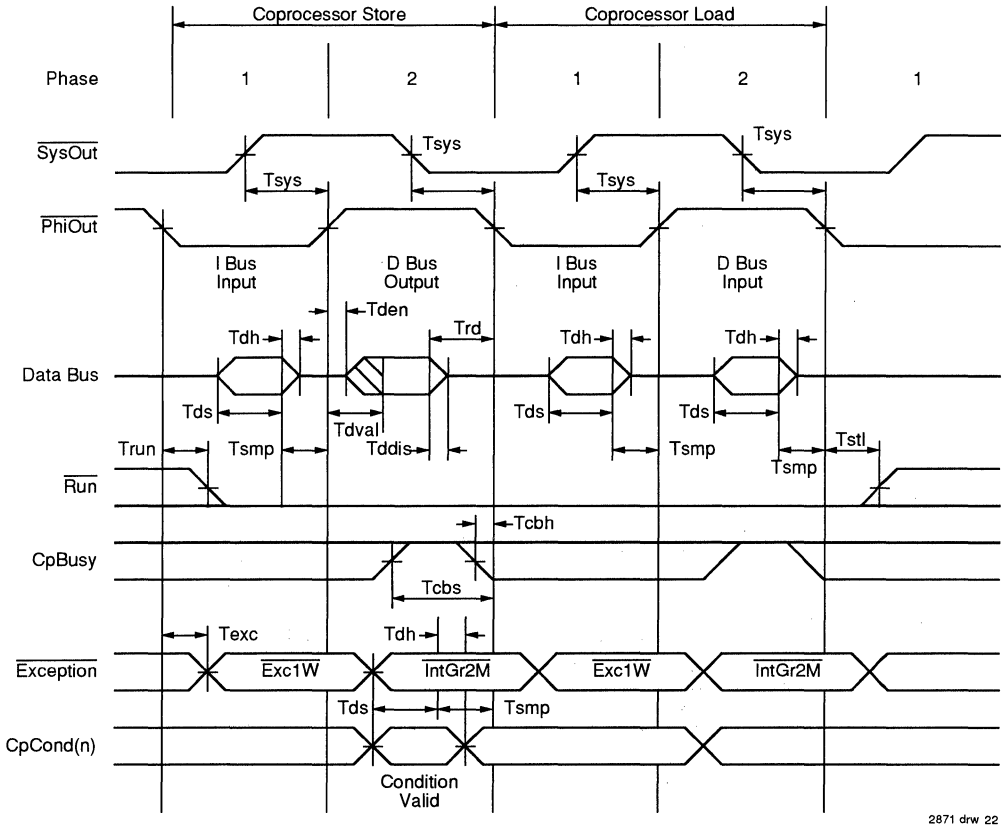

Figure 20. Coprocessor Load/Store Timing

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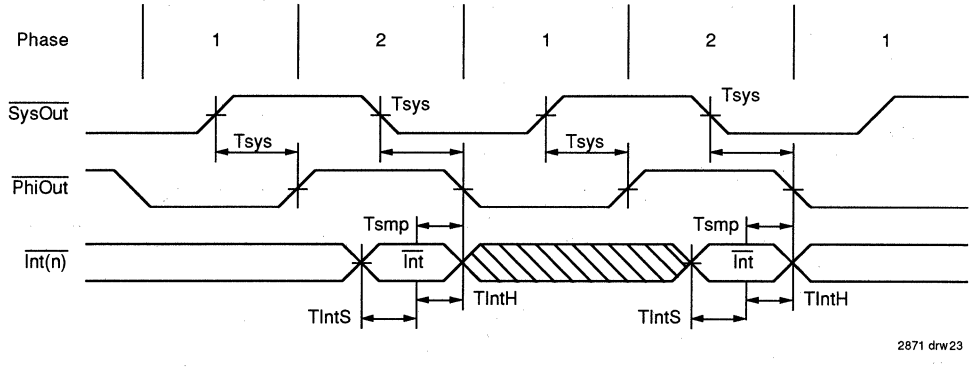


Figure 21. Interrupt Timing

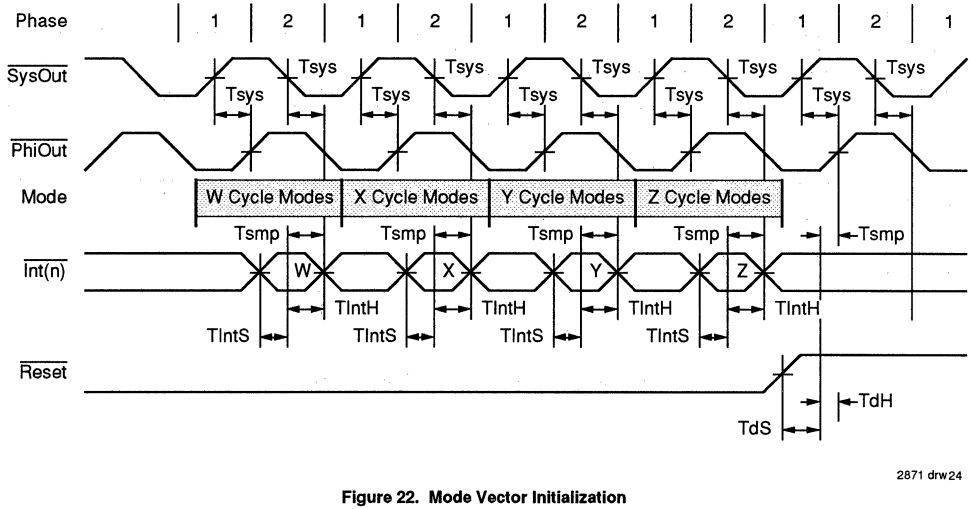
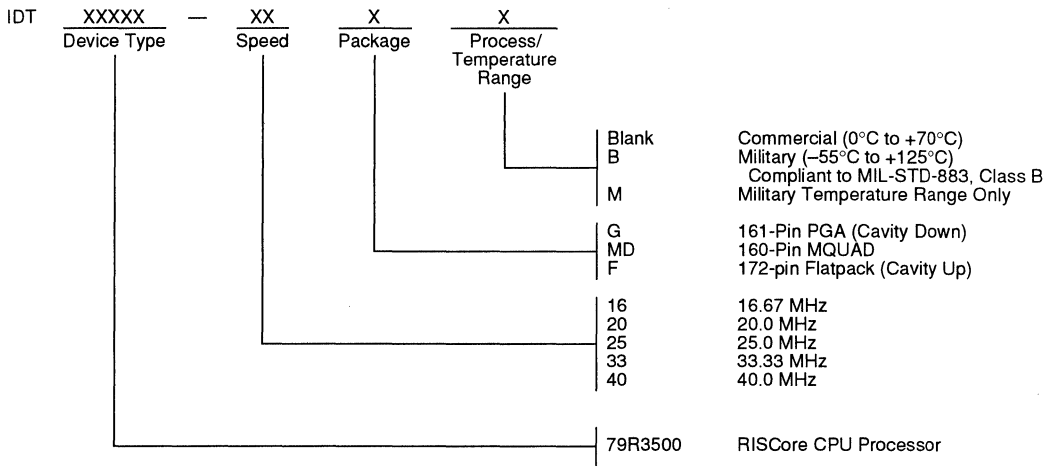


Figure 22. Mode Vector Initialization

NOTES:
1. Reset must be negated synchronously; however, it should be asserted asynchronously. Designs must not rely on the proper functioning of SysOut prior to the assertion of Reset.
2. Reset is actually sampled in both Phase 1 and Phase 2. To insure proper initialization, it must be negated relative to the end of Phase 1.

ORDERING INFORMATION



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VALID COMBINATIONS

IDT	79R3500 - 20,25,33,40	G, MD
	79R3500 - 20,25,-B,M	G, F

5

Integrated Device Technology, Inc.

IDT79R3041™ INTEGRATED RISController™ FOR LOW-COST SYSTEMS

ADVANCE INFORMATION
IDT79R3041

FEATURES:

- Instruction set compatible with IDT79R3000A and R3051™ Family RISC CPUs
- High level of integration minimizes system cost
  - — RISC CPU
  - — Multiply/divide unit
  - — Instruction Cache
  - — Data Cache
  - — Programmable bus interface
  - — Programmable port width support
- On-chip instruction and data caches
  - — 2kB of Instruction Cache
  - — 512B of Data Cache
- Flexible bus interface allows simple, low cost designs
  - — Superset pin-compatible with R3051
  - — Adds programmable port width interface (8-, 16-, and 32-bit memory sub-regions)
  - — Adds programmable bus interface timing support (Extended address hold, Bus turn around time, Read/write masks)
- Single, double-frequency clock input
- 16 and 20MHz operation
- 14 MIPS at 20MHz
- Low cost 84-pin PLCC packaging
- On-chip 4-deep write buffer eliminates memory write stalls
- On-chip 4-word read buffer supports burst or simple block reads
- On-chip DMA arbiter
- On-chip 24-bit timer
- Boot from 8-bit, 16-bit, or 32-bit wide boot PROMs
- Pin- and software-compatible family includes R3041™, R3051™, R3052™, and R3081™
- Complete software support
  - — Optimizing compilers
  - — Real-time operating systems
  - — Monitors/debuggers
  - — Floating Point Software
  - — Page Description Languages

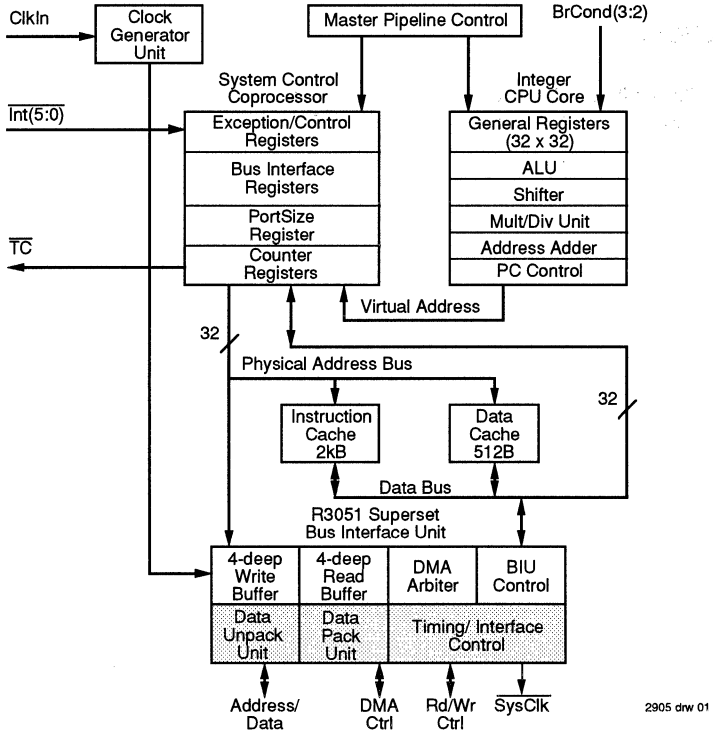


Figure 1. R3041 Block Diagram

INTRODUCTION

The IDT R3051 family is a series of high-performance 32-bit microprocessors featuring a high-level of integration, and targeted to high-performance but cost sensitive embedded processing applications. The R3051 family is designed to bring the high-performance inherent in the MIPS RISC architecture into low-cost, simplified, power sensitive applications.

Thus, functional units have been integrated onto the CPU core in order to reduce the total system cost, rather than to increase the inherent performance of the integer engine. Nevertheless, the R3051 family is able to offer 35 MIPS of integer performance at 40 MHz without requiring external SRAM or caches.

Further, the R3051 family brings dramatic power reduction to these embedded applications, allowing the use of low-cost packaging. Thus, the R3051 family allows customer applications to bring maximum performance at minimum cost.

The R3041 extends the range of price/performance achievable with the R3051 family, by dramatically lowering the cost of using the MIPS architecture. The R3041 has been designed to achieve minimal system and components cost, yet maintain the high-performance inherent in the MIPS architecture. The R3041 also maintains pin and software compatibility with the R3051 and R3081.

The R3051 family offers a variety of price/performance features in a pin-compatible, software compatible family. Table 1 provides an overview of the current members of the R3051 family. Note that the R3051, R3052, and R3081 are also available in pin-compatible versions that include a full-function memory management unit, including 64-entry TLB. The R3051/2 and R3081 are described in separate manuals and data sheets.

Figure 1 shows a block level representation of the functional units within the R3041. The R3041 can be viewed as the embodiment of a discrete solution built around the R3000A. By integrating this functionality on a single chip, dramatic cost and power reductions are achieved.

An overview of these blocks is presented here, followed with detailed information on each block.

Device Name	Instruction Cache	Data Cache	Floating Point	Bus Options
R3051	4kB	2kB	Software Emulation	Mux'ed A/D
R3052	8kB	2kB	Software Emulation	Mux'ed A/D
R3081	16kB or 8kB	4kB or 8kB	On-chip Hardware	1/2 frequency bus option
R3041	2kB	512B	Software Emulation	8-, 16-, and 32-bit port widths support Programmable timing support

2905 tbl 01

Table 1. Pin compatible R3051 Family

CPU Core

The CPU core is a full 32-bit RISC integer execution engine, capable of sustaining close to single cycle execution rate. The CPU core contains a five stage pipeline, and 32 orthogonal 32-bit registers. The R3051 family implements the MIPS-I ISA. In fact, the execution engine of the R3041 is the same as the execution engine of the R3000A. Thus, the R3041 is binary compatible with those CPU engines, as well as compatible with other members of the R3051 family.

The execution engine of the R3051 family uses a five-stage pipeline to achieve close to single cycle execution. A new instruction can be started in every clock cycle; the execution engine actually processes five instructions concurrently (in various pipeline stages). Figure 2 shows the concurrency achieved by the R3051 family pipeline.

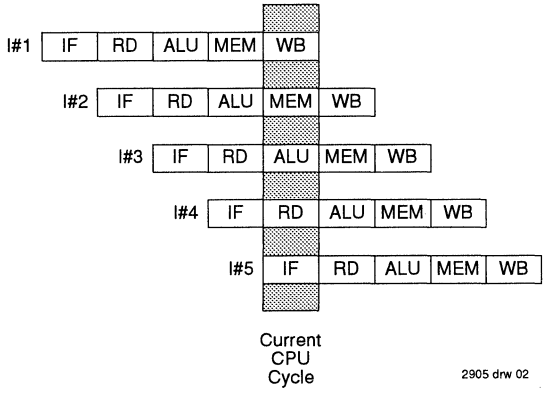


Figure 2. R3051 Family 5-Stage Pipeline

System Control Co-Processor

The R3041 also integrates on-chip a System Control Co-processor, CP0. CP0 manages the exception handling capability of the R3041, the virtual to physical address mapping of the R3041, and the programmable bus interface capabilities of the R3041. These topics are discussed in subsequent sections.

The R3041 does not include the optional TLB found in other members of the R3051 family, but instead performs the same virtual to physical address mapping of the base versions of the R3051 family. These devices still support distinct kernel and user mode operation, but do not require page management software or an on-chip TLB, leading to a simpler software model and a lower-cost processor.

The memory mapping used by these devices is illustrated in figure 3. Note that the reserved address spaces shown are for compatibility with future family members; in the current family members, references to these addresses are translated in the same fashion as their respective segments, with no traps or exceptions taken.

When using the base versions of the architecture, the system designer can implement a distinction between the user tasks and the kernel tasks, without having to execute page management software. This distinction can take the form of physical memory protection, accomplished by address decoding, or in other forms. In systems which do not wish to implement memory protection, and wish to have the kernel and user tasks operate out of a single unified memory space, upper address lines can be ignored by the address decoder, and thus all references will be seen in the lower gigabyte of the physical address space.

The R3041 adds additional resources into the on-chip CP0. These resources are detailed in the R3041 User's Manual. They allow kernel software to directly control activity of the processor internal resources and bus interface, and include:

- **Cache Configuration Register.** This register controls the data cache miss refill algorithm used, and also controls some of the debug features of the R3041.
- **Bus Control Register.** This register controls the behavior of various bus interface signals.
- **Count and Compare Registers.** Together, these registers implement a programmable 24-bit timer, which can be used for DRAM refresh or as a general purpose timer.
- **PortSize Control Register.** This register allows the kernel to indicate the port width of reads and writes to various sub-regions of the physical address space. Thus, the R3041 can interface directly with 8-, 16-, and 32-bit memory ports, including a mix of sizes, for both instruction and data references, without requiring external logic.

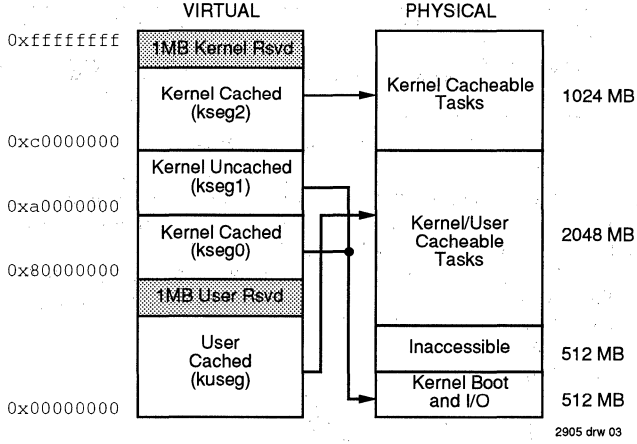


Figure 3. Virtual to Physical Mapping of Base Architecture Versions

Clock Generation Unit

The R3041 is driven from a single input clock, capable of operating in a range of 40%-60% duty cycle. On-chip, the clock generator unit is responsible for managing the interaction of the CPU core, caches, and bus interface. The clock generator unit replaces the external delay line required in R3000A based applications.

Instruction Cache

The R3041 integrates 2kB of on-chip Instruction Cache, organized with a line size of 16 bytes (four 32-bit entries). This relatively large cache substantially contributes to the performance inherent in the R3041, and allows systems based on the R3041 to achieve high-performance even from low-cost memory systems. The cache is implemented as a direct mapped cache, and is capable of caching instructions from anywhere within the 4GB physical address space. The cache is implemented using physical addresses and physical tags (rather than virtual addresses or tags), and thus does not require flushing on context switch.

Data Cache

The R3041 incorporates an on-chip data cache of 512B, organized as a line size of 4 bytes (one word). This relatively large data cache contributes substantially to the performance inherent in the R3051 family. As with the instruction cache, the data cache is implemented as a direct mapped physical address cache. The cache is capable of mapping any word within the 4GB physical address space.

The data cache is implemented as a write through cache, to insure that main memory is always consistent with the internal cache. In order to minimize processor stalls due to data write operations, the bus interface unit incorporates a 4-deep write buffer which captures address and data at the processor execution rate, allowing it to be retired to main memory at a much slower rate without impacting system performance.

Bus Interface Unit

The R3051 family uses its large internal caches to provide the majority of the bandwidth requirements of the execution engine, and thus can utilize a simple bus interface connected to slow memory devices.

The R3051 family bus interface utilizes a 32-bit address and data bus multiplexed onto a single set of pins. The bus interface unit also provides an ALE (Address Latch Enable) output signal to de-multiplex the A/D bus, and simple handshake signals to process CPU read and write requests. In addition to the read and write interface, the R3041 incorporates a DMA arbiter, to allow an external master to control the external bus.

The R3041 augments the basic R3051 bus interface capability by adding the ability to directly interface with varying memory port widths, for instructions or data. Thus, the R3041 can be used in a system with an 8-bit boot PROM, 16-bit font cartridges, and 32-bit page buffer, transparently to software, and without requiring external data packing, rotation, and unpacking.

In addition, the R3041 incorporates the ability to change some of the interface timing of the bus. These features can be used to eliminate external data buffers, and take advantage of lower speed (lower cost) interface components.

One of the bus interface options is the Extended Address Hold mode which adds 1/2 clock of extra address hold time from ALE falling. This allows easier interfacing to FPGAs and ASICs.

The R3041 incorporates a 4-deep write buffer to decouple the speed of the execution engine from the speed of the memory system. The write buffers capture and FIFO processor address and data information in store operations, and present it to the bus interface as write transactions at the rate the memory system can accommodate. During main memory writes, the R3041 can break a large datum (e.g. 32-bit word) into a series of smaller transactions (e.g. bytes), according to the width of the memory port being written. This operation is transparent to the software which initiated the store, insuring that the same software can run in true 32-bit memory systems.

The R3051 family read interface performs both single word reads and quad word reads. Single word reads work with a simple handshake, and quad word reads can either utilize the simple handshake (in lower performance, simple systems) or utilize a tighter timing mode when the memory system can burst data at the processor clock rate. Thus, the system designer can choose to utilize page or nibble mode DRAMs (and possibly use interleaving, if desired, in high-performance systems), or use simpler techniques to reduce complexity.

In order to accommodate slower quad word reads, the R3051 family incorporates a 4-deep read buffer FIFO, so that the external interface can queue up data within the processor before releasing it to perform a burst fill of the internal caches.

In addition, the R3041 can perform on-chip data packing when performing large datum reads (e.g., quad words) from narrower memory systems (e.g., 16-bits). Once again, this operation is transparent to the actual software, simplifying migration of software to higher performance (true 32-bit) systems, and simplifying field upgrades to wider memory. Since this capability works for either instruction or data reads, using 8-, 16-, or 32-bit boot PROMs is easily supported by the R3041.

SYSTEM USAGE

The IDT R3051 family has been specifically designed to easily connect to low-cost memory systems. Typical low-cost memory systems utilize slow EPROMs, DRAMs, and application specific peripherals.

Figure 4 shows some of the flexibility inherent in the R3041. In this example system, which is typical of a laser printer, a 32-bit PROM interface is used due to the size of the PDL interpreter. An embedded system can use an 8-bit boot PROM instead. A 16-bit font cartridge interface is provided for add- in cards and a 16-bit page buffer is used for low cost. In this system, a field or manufacturing upgrade to a 32-bit page buffer is supported by the boot software and DRAM controller. Such a system features a very low entry price, with a range of field upgrade options including the ability to upgrade to a more powerful member of the R3051 family.

The IDT R3051 family has been specifically designed to easily connect to low-cost memory systems. Typical low-cost memory systems utilize slow EPROMs, DRAMs, and application specific peripherals. Embedded systems may typically substitute static RAMs for the DRAMs.

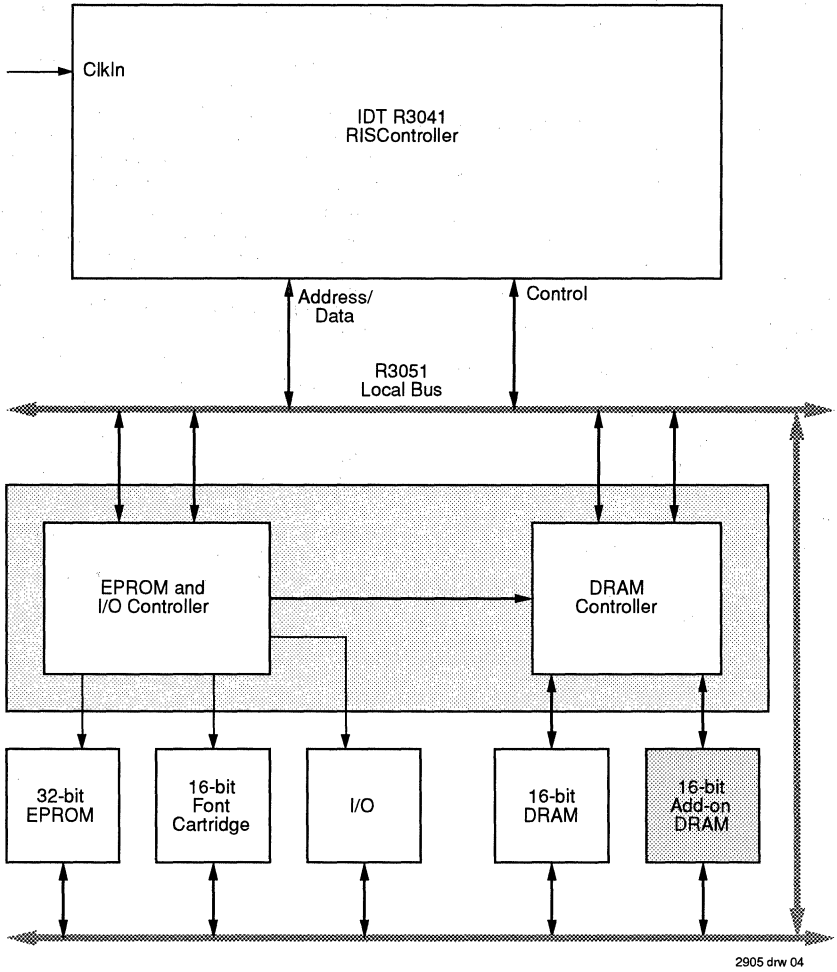


Figure 4. Typical R3041-Based Application

DEVELOPMENT SUPPORT

The IDT R3051 family is supported by a rich set of development tools, ranging from system simulation tools through PROM monitor and debug support, applications software and utility libraries, logic analysis tools, and sub-system modules.

Figure 5 is an overview of the system development process typically used when developing R3041 applications. The R3051 family is supported in all phases of project development. These tools allow timely, parallel development of hardware and software for R3051 family based applications, and include tools such as:

- A program, Cache-3041, which allows the performance of an R3041 based system to be modeled and understood without requiring actual hardware.
- Sable, an instruction set simulator.
- Optimizing compilers from MIPS Technology, the acknowledged leader in optimizing compiler technology.
- Cross development tools, available in a variety of development environments.
- The high-performance IDT floating point emulation library software.
- The IDT Evaluation Board, which includes RAM, EPROM, I/O, and the IDT PROM Monitor.
- The IDT Laser Printer System board, which directly drives a low-cost print engine, and runs Microsoft TrueImage™ Page Description Language on top of PeerlessPage™ Advanced Printer Controller BIOS.
- Adobe PostScript™ Page Description Language running on the IDT R3051 family.
- The IDT/sim PROM Monitor, which implements a full PROM monitor (diagnostics, remote debug support, peek/poke, etc.).
- IDT/kit (Kernel Integration Toolkit), providing library support and a frame work for the system run time environment.

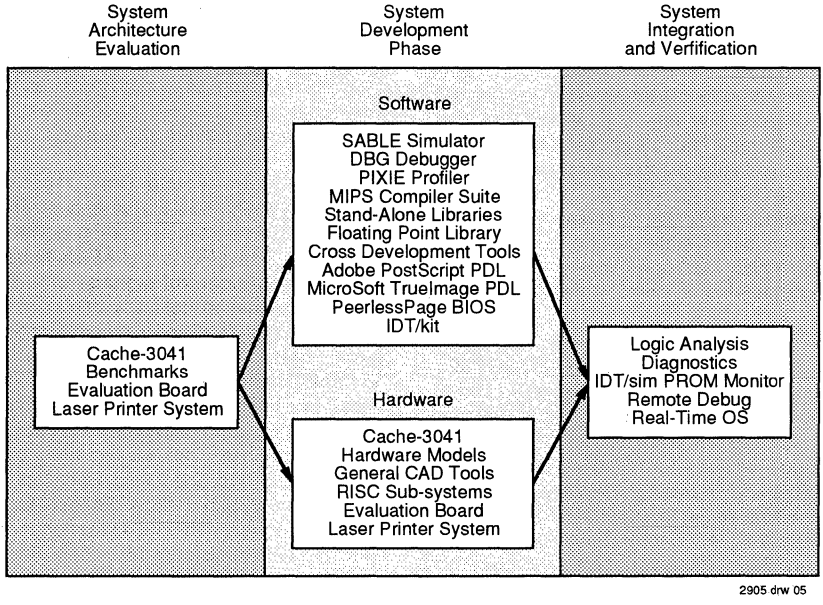


Figure 5. R3041 Development Environment

PERFORMANCE OVERVIEW

The R3051 family achieves a very high-level of performance. This performance is based on:

- **An efficient execution engine.** The CPU performs ALU operations and store operations in a single cycle, and has an effective load time of 1.3 cycles, and branch execution rate of 1.5 cycles (based on the ability of the compilers to avoid software interlocks). Thus, the R3041 achieves over 16 MIPS performance when operating out of cache.
- **Large on-chip caches.** The R3051 family contains caches which are substantially larger than those on the majority of embedded microprocessors. These large caches minimize the number of bus transactions required, and allow the R3051 family to achieve actual sustained performance very close to its peak execution rate, even with low cost memory systems.
- **Autonomous multiply and divide operations.** The R3051 family features an on-chip integer multiplier/divide unit which is separate from the other ALU. This allows the R3041 to perform multiply or divide operations in parallel with other integer operations, using a single multiply or divide instruction rather than using "step" operations.
- **Integrated write buffer.** The R3041 features a four deep write buffer, which captures store target addresses and data at the processor execution rate and retires it to main memory at the slower main memory access rate. Use of on-chip write buffers eliminates the need for the processor to stall when performing store operations.
- **Burst read support.** The R3041 enables the system designer to utilize page mode, static column, or nibble mode RAMs when performing read operations to minimize the main memory read penalty and increase the effective cache hit rates.

The performance differences among the various R3051 family members depends on the application software and the design of the memory system. Different family members feature different cache sizes, and the R3081 features a hardware floating point accelerator. Since all these devices can be used in a pin and software compatible fashion, the system designer has maximum freedom in trading between performance and cost. The memory simulation tools (e.g. Cache-3041) allows the system designers to analyze and understand the performance differences among these devices in their application.

SELECTABLE FEATURES

The R3051 family allows the system designer to configure some aspects of operation.

Some of these configuration options are under the software control of the kernel, and are contained in the System Control Co-Processor registers. Others are established via mode inputs sampled at the negating edge of device reset.

Selectable features include:

- **BigEndian vs. LittleEndian operation**: The part can be configured to operate with either byte ordering convention, and in fact may also be dynamically switched between the two conventions. This facilitates the porting of applications from other processor architectures, and also permits inter-communication between various types of processors and databases.
- **Data cache refill of one or four words**: The memory system must be capable of performing 4 word transfers to satisfy instruction cache misses and 1 word transfers to satisfy uncached references. The data cache refill size option allows the system designers to choose between one and four word refill on data cache misses, depending on the performance each option brings to their application.
- **Bus Turn Around Speed**: The R3041 allows the kernel to increase the amount of time between bus transactions when changes in bus direction occur (e.g. the end of reads). This allows transceivers and buffers to be eliminated from the system.
- **Extended Address Hold Time**: The R3041 allows the system designer to increase the amount of hold time available for address latching, thus allowing slower speed (low cost) address latches, FPGAs and ASICs to be used.
- **Programmable control signals**: The R3041 allows the system designer to optimally configure various memory control signals to simplify external logic, thus reducing system cost.
- **Variable Memory Port Widths**: The R3041 allows the kernel to partition the physical memory space into various sub-regions, and to individually indicate the port width of these sub-regions. Thus, the bus interface unit can perform data packing and unpacking when communicating with narrow memory sub-regions. For example, these features, can be used to allow the R3041 to interface with narrow boot PROMS, or to implement 16-bit only memory systems.

THERMAL CONSIDERATIONS

The R3051 family utilizes special packaging techniques to improve the thermal properties of high-speed processors. Thus, all versions of the R3051 family are packaged in cavity down packaging.

The lowest cost members of the family use a standard cavity down, injection molded PLCC package (the "J" package). This package is used for all speeds of the R3041 family.

Higher speed and higher performance members of the R3051 family utilize more advanced packaging techniques to dissipate power while remaining both low-cost and pin- and socket- compatible with the PLCC package. Thus, these members of the R3051 family are available in the MQUAD package (the "MJ" package), which is an all aluminum package with the die attached to a normal copper lead-frame mounted to the aluminum casing. The MQUAD package is pin and form compatible with the PLCC package. Thus, designers can choose to utilize this package without changing their PCB.

The members of the R3051 family are guaranteed in a case temperature range of 0°C to +95°C. The type of package, speed (power) of the device, and airflow conditions, affect the equivalent ambient conditions which meet this specification.

The equivalent allowable ambient temperature, T_A, can be calculated using the thermal resistance from case to ambient ($\emptyset_{CA}$) of the given package. The following equation relates ambient and case temperature:

$$T_A = T_C - P * \emptyset_{CA}$$

where P is the maximum power consumption at hot temperature, calculated by using the maximum Icc specification for the device.

Typical values for $\emptyset_{CA}$ at various airflows are shown in Table 2 for the PLCC package.

	Airflow (ft/min)					
ØCA	**0**	**200**	**400**	**600**	**800**	**1000**
"J" Package	29	26	21	18	16	15

2905 tbl 02

Table 2. Thermal Resistance ($\emptyset_{CA}$) at Various Airflows

5

PIN DESCRIPTION

PIN NAME	I/O	DESCRIPTION
A/D(31:0)	I/O	**Address/Data:** A 32-bit time multiplexed bus which indicates the desired address for a bus transaction in one phase, and which is used to transmit data between the CPU and external memory resources during the rest of the transfer. Bus transactions on this bus are logically separated into two phases: during the first phase, information about the transfer is presented to the memory system to be captured using the ALE output. This information consists of: **Address(31:4)**: The high-order address for the transfer is presented on A/D(31:4). **$\overline{\text{BE(3:0)}}$**: These strobes indicate which bytes of the 32-bit bus will be involved in the transfer, and are presented on A/D(3:0). $\overline{\text{BE(3)}}$ indicates that A/D(31:24) will be used, and $\overline{\text{BE(0)}}$ corresponds to A/D(7:0). These strobes are only valid for accesses to 32-bit wide memory ports. Note that $\overline{\text{BE(3:0)}}$ can be held in-active during reads by setting the appropriate bit of CP0; thus, these signals could be directly used as Write Enable strobes. During the second phase, these signals are the data bus for the transaction. **Data(31:0):** During write cycles, the bus contains the data to be stored and is driven from the internal write buffer. On read cycles, the bus receives the data from the external resource, in either a single data transaction or in a burst of four words, and places it into the on-chip read buffer. The byte lanes used during the transfer are a function of the datum size, the memory port width, and the system byte-ordering.
Addr(3:0)	O	**Low Address (3:0)** A 4-bit bus which indicates which word/halfword/byte is currently expected by the processor. For 32-bit port widths, only Addr(3:2) is valid during the transfer; for 16-bit port widths, only Addr(3:1) are valid; for 8-bit port widths, all of Addr(3:0) are valid. These address lines always contain the address of the current datum to be transferred. In writes and single datum reads, the addresses initially output the specific target address, and will increment if the size of the datum is wider than the target memory port. For quad word reads, these outputs function as a counter starting at '0000', and incrementing according to the width of the memory port. The R3041 Addr(1:0) output pins are designated as the Rsvd(1:0) pins in the R3051 and R3081.
Diag	O	**Diagnostic Pin.** This output indicates whether the current bus read transaction is due to an on-chip cache miss and whether the read is an instruction or data, and is time multiplexed as described below: **Cached:** During the phase in which the A/D bus presents address information, this pin is an active high output which indicates whether or not the current read is a result of a cache miss. The value of this pin at this time other than in read cycles is undefined. **I/$\overline{\text{D}}$:** A high at this time indicates an instruction reference, and a low indicates a data reference. The value of this pin at this time other than in read cycles is undefined. The R3041 Diag output pin is designated as Diag(1) in the R3051 and R3081.
ALE	O	**Address Latch Enable:** Used to indicate that the A/D bus contains valid address information for the bus transaction. This signal is used by external logic to capture the address for the transfer, typically using transparent latches.
$\overline{\text{DataEn}}$	O	**Data Enable:** This signal indicates that the A/D bus is no longer being driven by the processor during read cycles, and thus the external memory system may enable the drivers of the memory system onto this bus without having a bus conflict occur. During write cycles, or when no bus transaction is occurring, this signal is negated, thus disabling the external memory drivers.

2905 tbl 03

PIN DESCRIPTION (Continued):

PIN NAME	I/O	DESCRIPTION
Burst/ WrNear	O	**Burst Transfer/Write Near:** On read transactions, the Burst signal indicates that the current bus read is requesting a block of four contiguous words from memory. This signal is asserted only in read cycles due to cache misses; it is asserted for all I-Cache miss read cycles, and for D-Cache miss read cycles if selected in the CP0 Cache Config Register. On write transactions, the WrNear output tells the external memory system that the bus interface unit is performing back-to-back write transactions to an address within the same 256 byte page as the prior write transaction. This signal is useful in memory systems which employ page mode or static column DRAMs, and allows nearby writes to be retired quickly.
Rd	O	**Read:** An output which indicates that the current bus transaction is a read.
Wr	O	**Write:** An output which indicates that the current bus transaction is a write.
Ack	I	**Acknowledge:** An input which indicates to the device that the memory system has sufficiently processed the bus transaction. On write transactions, this signal indicates that the CPU may either progress to the next data item (for mini-burst writes of wide datums to narrow memories), or terminate the write cycle. On read transactions, this signal indicates that the memory system has sufficiently processed the read, and that the processor core may begin processing the data from this read transfer.
RdCEn	I	**Read Buffer Clock Enable:** An input which indicates to the device that the memory system has placed valid data on the A/D bus, and that the processor may move the data into the on-chip Read Buffer.
SysClk	O	**System Reference Clock:** An output from the CPU which reflects the timing of the internal processor "Sys" clock. This clock is used to control state transitions in the read buffer, write buffer, memory controller, and bus interface unit.
BusReq	I	**DMA Arbiter Bus Request:** An input to the device which requests that the CPU tri-state its bus interface signals so that they may be driven by an external master. The negation of this input relinquishes mastership back to the CPU.
BusGnt	O	**DMA Arbiter Bus Grant.** An output from the CPU used to acknowledge that a BusReq has been detected, and that the bus is relinquished to the external master. The R3041 adds an additional DMA protocol, under the control of CP0. If the DMA Protocol is enabled, the R3041 can request that the external master relinquish bus mastership back to the processor by negating the BusGnt output early, and waiting for the BusReq input to be negated.
SBrCond(3)/ IOStrobe	I/O	**Branch Condition Port/IO Strobe:** The use of this signal depends on the setting of various bits of the CP0 Bus Control register. If BrCond mode is selected, this input is logically connected to CpCond(3), and can be used by the branch on co-processor condition instructions as an input port. The SBrCond(3) input has special internal logic to synchronize the input, and thus may be driven by asynchronous agents. If this pin is selected to function as IOStrobe, it may be asserted as an output on reads, writes, or both, as programmed into CP0. This strobe asserts in the second clock cycle of a transfer, and thus can be used to strobe various control signals from the bus interface.
SBrCond(2)/ ExtDataEn	I/O	**Branch Condition Port/Extended Data Enable:** The use of this signal depends on the settings in the CP0 Bus Control register. If BrCond mode is selected, this input is logically connected to CpCond(2), and can be used by the branch on co-processor condition instructions as an input port. The SBrCond(2) input has special internal logic to synchronize the input, and thus may be driven by asynchronous agents. If this pin is selected to function as Extended Data Enable, it may be asserted as an output on reads, writes, or both, as programmed into CP0. This strobe can be used as an extended data enable strobe, in that it is held asserted for one-half clock cycle after the negation of Rd or Wr. This signal may typically be used as a write enable control line for transceivers, as a write line for I/O, or as an address mux select for DRAMs.
MemStrobe	O	**Memory Strobe:** This active low output pulses low for each data read or written, as configured in the CP0 Bus Control register. Thus, it can be used as a read strobe, write strobe, or both, for SRAM type memories or for I/O devices. In the R3051 and R3081, this pin is designated as the BrCond(0) input.

2905 tbl 04

5

PIN DESCRIPTION (Continued):

PIN NAME	I/O	DESCRIPTION
$\overline{BE16(1:0)}$	O	**Byte Enable Strobes for 16-bit Memory Port:** These active low outputs are the byte lane strobes for accesses to 16-bit wide memory ports; they are not necessarily valid for 8- or 32-bit wide ports. If $\overline{BE16(1)}$ is asserted, then the most significant byte (either D(31:24) or D(15:8), depending on system endianness) is going to be used in this transfer. If $\overline{BE16(0)}$ is asserted, the least significant byte (D(23:16) or D(7:0)) will be used. $\overline{BE16(1:0)}$ can be held inactive (masked) during read transfers, according to the programming of the CP0 Bus Control register. In the R3051 and R3081, these pins are designated as Rsvd(3:2).
$\overline{Last}$	O	**Last Datum in Mini-Burst:** This active low output indicates that this is the last datum transfer in a given transaction. It is asserted after the next to last $\overline{RdCEn}$ (reads) or $\overline{Ack}$ (writes), and is negated when $\overline{Rd}$ or $\overline{Wr}$ is negated. The $\overline{Last}$ output pin is designated in the R3051 and R3081 as the Diag(0) output pin.
$\overline{TC}$	O	**Terminal Count:** This is an active low output from the processor which indicates that the on-chip timer has reached its terminal count. It will remain low for either 1.5 clock cycles, or until software resets the timer, depending on the mode selected in the CP0 Bus Control register. Thus, the on-chip timer can function either as a free running timer for system functions such as DRAM refresh, or can operate as a software controlled time-slice timer, or real-time clock. The $\overline{TC}$ output pin is designated in the R3051 as the BrCond(1) input, and in the R3081 as the Run output.
$\overline{BusError}$	I	**Bus Error:** Input to the bus interface unit to terminate a bus transaction due to an external bus error. This signal is only sampled during read and write operations. If the bus transaction is a read operation, then the CPU will take a bus error exception.
$\overline{Int}(5:3)$ $\overline{SInt}(2:0)$	I	**Processor Interrupt:** During normal operation, these signals are logically the same as the $\overline{Int}(5:0)$ signals of the R3000. During processor reset, these signals perform mode initialization of the CPU, but in a different (simpler) fashion than the interrupt signals of the R3000. There are two types of interrupt inputs: the $\overline{SInt}$ inputs are internally synchronized by the processor, and may be driven by an asynchronous external agent. The direct interrupt inputs are not internally synchronized, and thus must be externally synchronized to the CPU. The direct interrupt inputs have one cycle lower latency than the synchronized interrupts.
ClkIn	I	**Master Clock Input:** This is a double frequency input used to control the timing of the CPU.
$\overline{Reset}$	I	**Master Processor Reset:** This signal initializes the CPU. Reset initialization mode selection is performed during the last cycle of $\overline{Reset}$.
$\overline{TriState}$	I	**Tri-State:** This input to the R3041 requests that the R3041 tri-state all of its outputs. In addition to those outputs tri-stated during DMA, tri-state will cause $\overline{SysClk}$, $\overline{TC}$, and $\overline{BusGnt}$ to tri-state. This signal is intended for use during board testing and emulation during debug and board manufacture. In the R3051 and R3081, this input pin is designated as Rsvd(4).

2905 tbl 05

ABSOLUTE MAXIMUM RATINGS(1, 3)

Symbol	Rating	Commercial	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TC	Operating Case Temperature	0 to +95	°C
TBIAS	TemperatureUnder Bias	–55 to +125	°C
TSTG	Storage Temperature	–55 to +125	°C
VIN	Input Voltage –0.5 to +7.0	V	

2905 tbl 06

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VIN minimum = –3.0V for pulse width less than 15ns. VIN should not exceed VCC +0.5 Volts.
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

AC TEST CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
VIH	Input HIGH Voltage	3.0	—	V
VIL	Input LOW Voltage	—	0.4	V
VIHS	Input HIGH Voltage	3.5	—	V
VILS	Input LOW Voltage	—	0.4	V

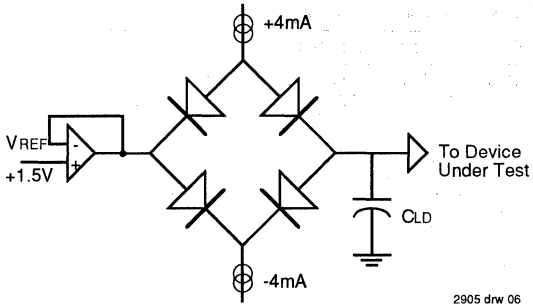
2905 tbl 08

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Commercial	0°C to +95°C (Case)	0V	5.0 ±5%

2905 tbl 07

OUTPUT LOADING FOR AC TESTING



2905 drw 06

Signal	Cld
All Signals	25 pF

2905 tbl 09

5

DC ELECTRICAL CHARACTERISTICS— (T_C = 0°C to +95°C, V_{CC} = +5.0V ±5%)

Symbol	Parameter	Test Conditions	16.67 MHz		20 MHz		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4mA	3.5	—	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	—	0.4	—	0.4	V
V_{IH}	Input HIGH Voltage(3)	—	2.0	—	2.0	—	V
V_{IL}	Input LOW Voltage(1)	—	—	0.8	—	0.8	V
V_{IHS}	Input HIGH Voltage(2,3)	—	3.0	—	3.0	—	V
V_{ILS}	Input LOW Voltage(1,2)	—	—	0.4	—	0.4	V
C_{IN}	Input Capacitance(4)	—	—	10	—	10	pF
C_{OUT}	Output Capacitance(4)	—	—	10	—	10	pF
I_{CC}	Operating Current	V_{CC} = 5V, T_A = 70°C	—	350	—	400	mA
I_{IH}	Input HIGH Leakage	V_{IH} = VCC	—	100	—	100	µA
I_{IL}	Input LOW Leakage	V_{IL} = GND	–100	—	–100	—	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	–100	100	–100	100	µA

2905 tbl 10

NOTES:
1. V_{IL} Min. = –3.0V for pulse width less than 15ns. V_{IL} should not fall below –0.5 volts for larger periods.
2. V_{IHS} and V_{ILS} apply to Clk2xIn and $\overline{\text{Reset}}$.
3. V_{IH} should not be held above V_{CC} + 0.5 volts.
4. Guaranteed by design.

AC ELECTRICAL CHARACTERISTICS [1, 2, 3] — (T_C = 0°C to +95°C, V_{CC} = +5.0V ±5%)

Symbol	Signals	Description	16.67 MHz		20 MHz		Unit
			Min.	Max.	Min.	Max.	
t1	$\overline{\text{BusReq}}$, $\overline{\text{Ack}}$, $\overline{\text{BusError}}$, $\overline{\text{RdCEn}}$	Set-up to $\overline{\text{SysClk}}$ rising	8	—	7	—	ns
t1a	A/D	Set-up to $\overline{\text{SysClk}}$ falling	9	—	8	—	ns
t2	$\overline{\text{BusReq}}$, $\overline{\text{Ack}}$, $\overline{\text{BusError}}$, $\overline{\text{RdCEn}}$	Hold from $\overline{\text{SysClk}}$ rising	2	—	2	—	ns
t2a	A/D	Hold from $\overline{\text{SysClk}}$ falling	1	—	1	—	ns
t3	A/D, Addr, Diag, ALE, $\overline{\text{Wr}}$ $\overline{\text{Burst/WrNear}}$, $\overline{\text{Rd}}$, $\overline{\text{DataEn}}$	Tri-state from $\overline{\text{SysClk}}$ rising	—	10	—	10	ns
t4	A/D, Addr, Diag, ALE, $\overline{\text{Wr}}$ $\overline{\text{Burst/WrNear}}$, $\overline{\text{Rd}}$, $\overline{\text{DataEn}}$	Driven from $\overline{\text{SysClk}}$ falling	—	10	—	10	ns
t5	$\overline{\text{BusGnt}}$	Asserted from $\overline{\text{SysClk}}$ rising	—	9	—	8	ns
t6	$\overline{\text{BusGnt}}$	Negated from $\overline{\text{SysClk}}$ falling	—	9	—	8	ns
t7	$\overline{\text{Wr}}$, $\overline{\text{Rd}}$, $\overline{\text{Burst/WrNear}}$, $\overline{\text{Last}}$, $\overline{\text{TC}}$	Valid from $\overline{\text{SysClk}}$ rising	—	6	—	5	ns
t7a	A/D	Valid from $\overline{\text{SysClk}}$ rising	—	11	—	9	ns
t8	ALE	Asserted from $\overline{\text{SysClk}}$ rising	—	5	—	4	ns
t9	ALE	Negated from $\overline{\text{SysClk}}$ falling	—	5	—	4	ns
t10	A/D	Hold from ALE negated	2	—	2	—	ns
t11	$\overline{\text{DataEn}}$	Asserted from $\overline{\text{SysClk}}$	—	16	—	15	ns
t12	$\overline{\text{DataEn}}$	Asserted from A/D tri-state[4]	0	—	0	—	ns
t14	A/D	Driven from $\overline{\text{SysClk}}$ rising[4]	0	—	0	—	ns
t15	$\overline{\text{Wr}}$, $\overline{\text{Rd}}$, $\overline{\text{DataEn}}$, $\overline{\text{Burst/WrNear}}$, $\overline{\text{Last}}$, $\overline{\text{TC}}$	Negated from $\overline{\text{SysClk}}$ falling	—	8	—	7	ns
t16	Addr(3:2), $\overline{\text{BE}}$ 16(1:0)	Valid from $\overline{\text{SysClk}}$	—	7	—	6	ns
t17	Diag	Valid from $\overline{\text{SysClk}}$	—	9	—	8	ns
t18	A/D	Tri-state from $\overline{\text{SysClk}}$	—	10	—	10	ns
t19	A/D	$\overline{\text{SysClk}}$ to data out	—	13	—	12	ns
t20	ClkIn	Pulse Width High	12	—	10	—	ns
t21	ClkIn	Pulse Width Low	12	—	10	—	ns
t22	ClkIn	Clock Period	30	250	25	250	ns
t23	$\overline{\text{Reset}}$	Pulse Width from Vcc valid	200	—	200	—	µs
t24	$\overline{\text{Reset}}$	Minimum Pulse Width	32	—	32	—	tsys
t25	$\overline{\text{Reset}}$	Set-up to $\overline{\text{SysClk}}$ falling	7	—	6	—	ns
t26	$\overline{\text{Int}}$	Mode set-up to $\overline{\text{Reset}}$ rising	7	—	6	—	ns
t27	$\overline{\text{Int}}$	Mode hold from $\overline{\text{Reset}}$ rising	2.5	—	2.5	—	ns
t28	$\overline{\text{SInt}}$, SBrCond	Set-up to $\overline{\text{SysClk}}$ falling	7	—	6	—	ns
t29	$\overline{\text{SInt}}$, SBrCond	Hold from $\overline{\text{SysClk}}$ falling	4	—	3	—	ns
t30	$\overline{\text{Int}}$, BrCond	Set-up to $\overline{\text{SysClk}}$ falling	7	—	6	—	ns
t31	$\overline{\text{Int}}$, BrCond	Hold from $\overline{\text{SysClk}}$ falling	4	—	3	—	ns
tsys	$\overline{\text{SysClk}}$	Pulse Width	2*t22	2*t22	2*t22	2*t22	ns
t32	$\overline{\text{SysClk}}$	Clock High Time	t22 - 2	t22 + 2	t22 - 2	t22 + 2	ns
t33	$\overline{\text{SysClk}}$	Clock Low Time	t22 - 2	t22 + 2	t22 - 2	t22 + 2	ns

2905 tbl 11

5

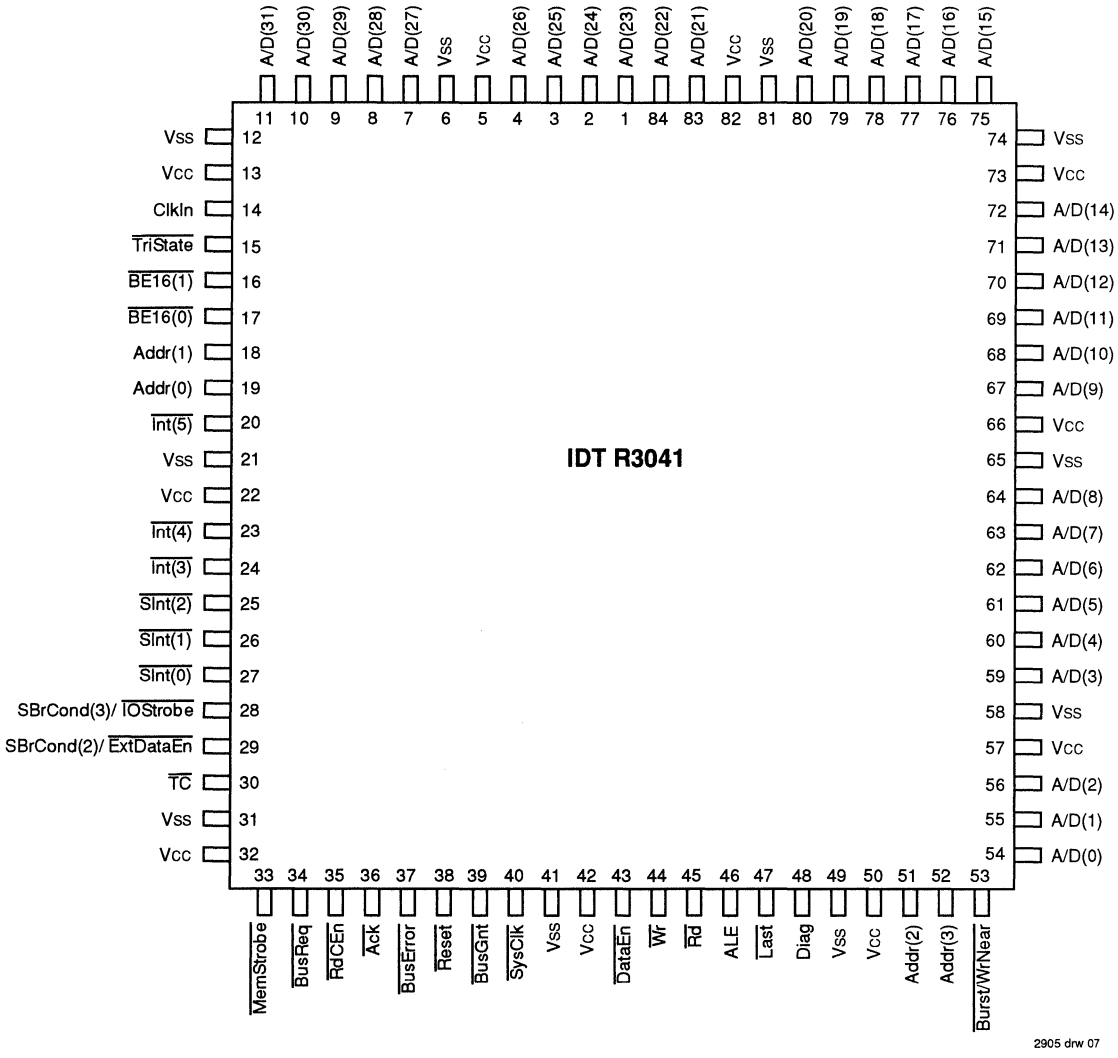
AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Symbol	Signals	Description	16.67 MHz		20 MHz		Unit
			Min.	Max.	Min.	Max.	
t45	$\overline{\text{ExtDataEn}}$	Tri-state from $\overline{\text{SysClk}}$ rising	—	10	—	10	ns
t46	$\overline{\text{ExtDataEn}}$	Driven from $\overline{\text{SysClk}}$ falling	—	10	—	10	ns
t47	$\overline{\text{IOStrobe}}$	Valid from $\overline{\text{SysClk}}$ falling	—	9	—	8	ns
t48	$\overline{\text{ExtDataEn}}$, $\overline{\text{DataEn}}$	Asserted from $\overline{\text{SysClk}}$ rising	—	13	—	12	ns
t49	$\overline{\text{ExtDataEn}}$	Negated from $\overline{\text{SysClk}}$ rising	—	8	—	7	ns
t50	$\overline{\text{MemStrobe}}$	Asserted from $\overline{\text{SysClk}}$ rising	—	18	—	15	ns
t51	$\overline{\text{MemStrobe}}$	Negated from $\overline{\text{SysClk}}$ falling	—	18	—	15	ns
t52	$\overline{\text{MemStrobe}}$	Asserted from Addr(3:0) valid[4]	0	—	0	—	ns
tderate	All outputs	Timing deration for loading over 25pf[4, 5]	—	0.5	—	0.5	ns/ 25pF

2905 tbl 12

NOTES:
1. All timings referenced to 1.5 Volts, with a rise and fall time of less than 2.5ns.
2. All outputs tested with 25 pF loading.
3. The AC values listed here reference timing diagrams contained in the R3041 Hardware User's Manual.
4. Guaranteed by design.
5. This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25 pF over the specified test load condition.
6. Timings t34 - t44 are reserved for other R3051 family members.

PIN CONFIGURATIONS



2905 drw 07

84-Pin PLCC/
Top View

5

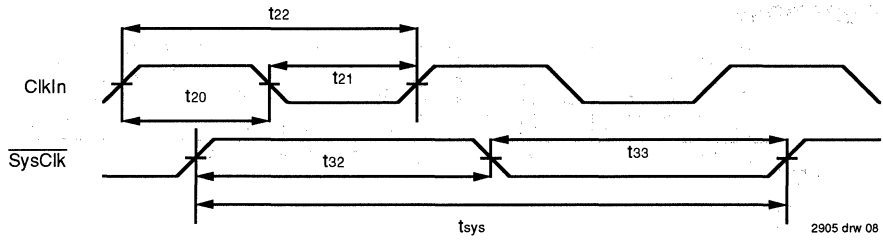


Figure 8. R3051 Family Clocking

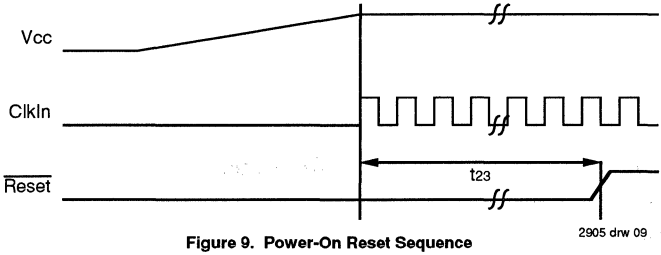


Figure 9. Power-On Reset Sequence

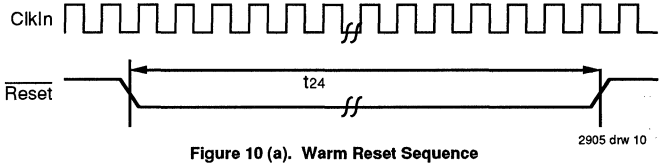


Figure 10 (a). Warm Reset Sequence

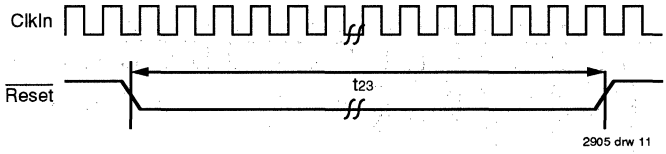


Figure 10 (b). Warm Reset Sequence (Internal Pull-Ups Used)

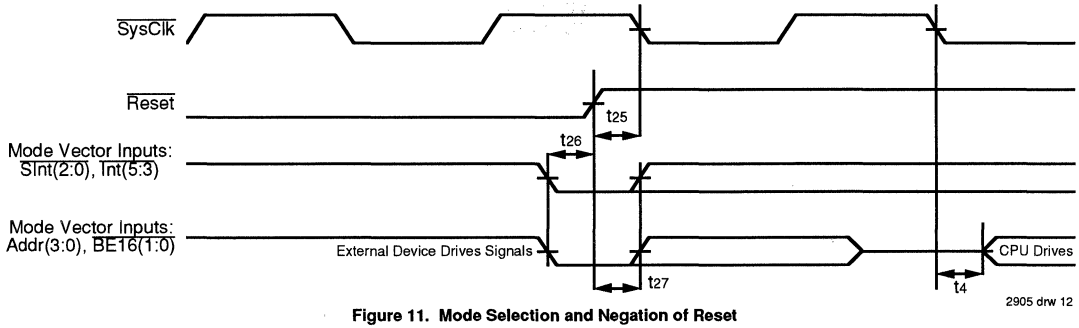


Figure 11. Mode Selection and Negation of Reset

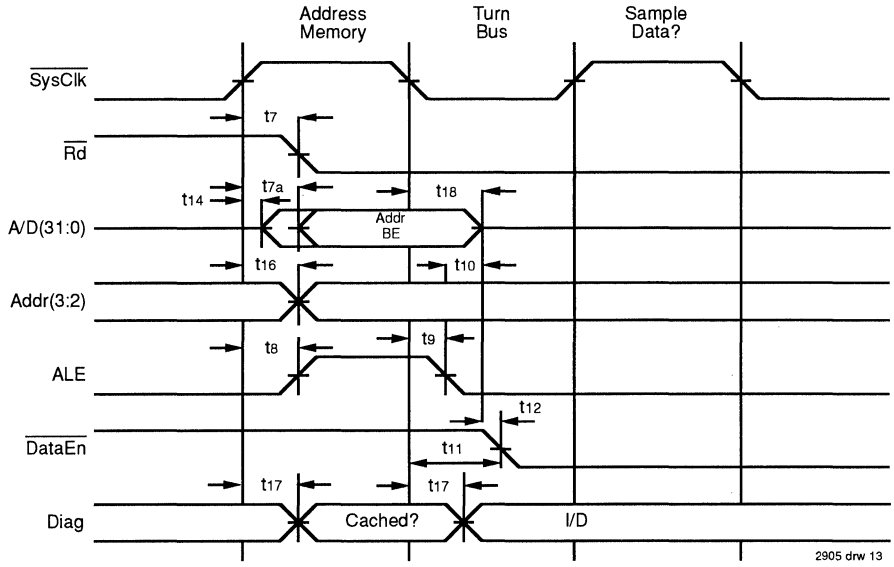


Figure 12(a). Timing with Non-Extended Address Hold Option

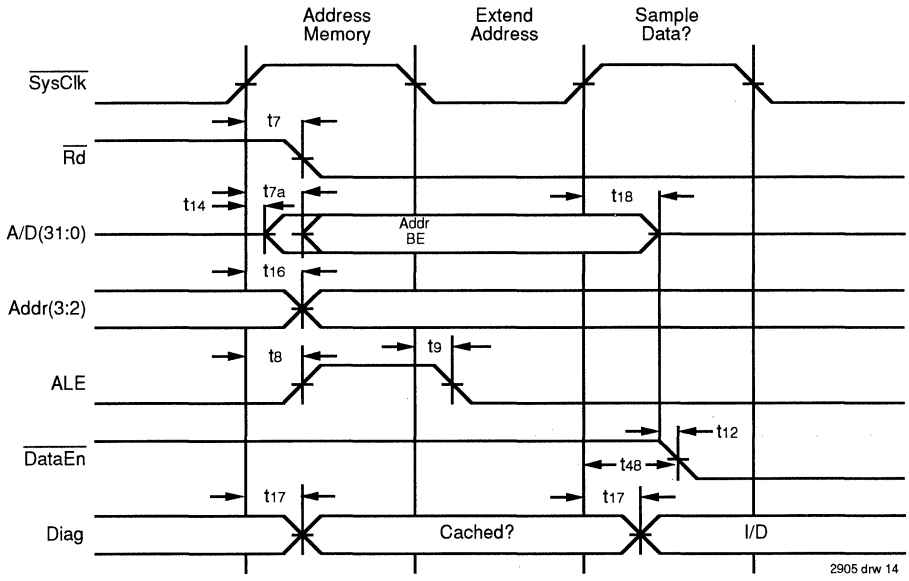


Figure 12(b). Timing with Extended Address Hold Option

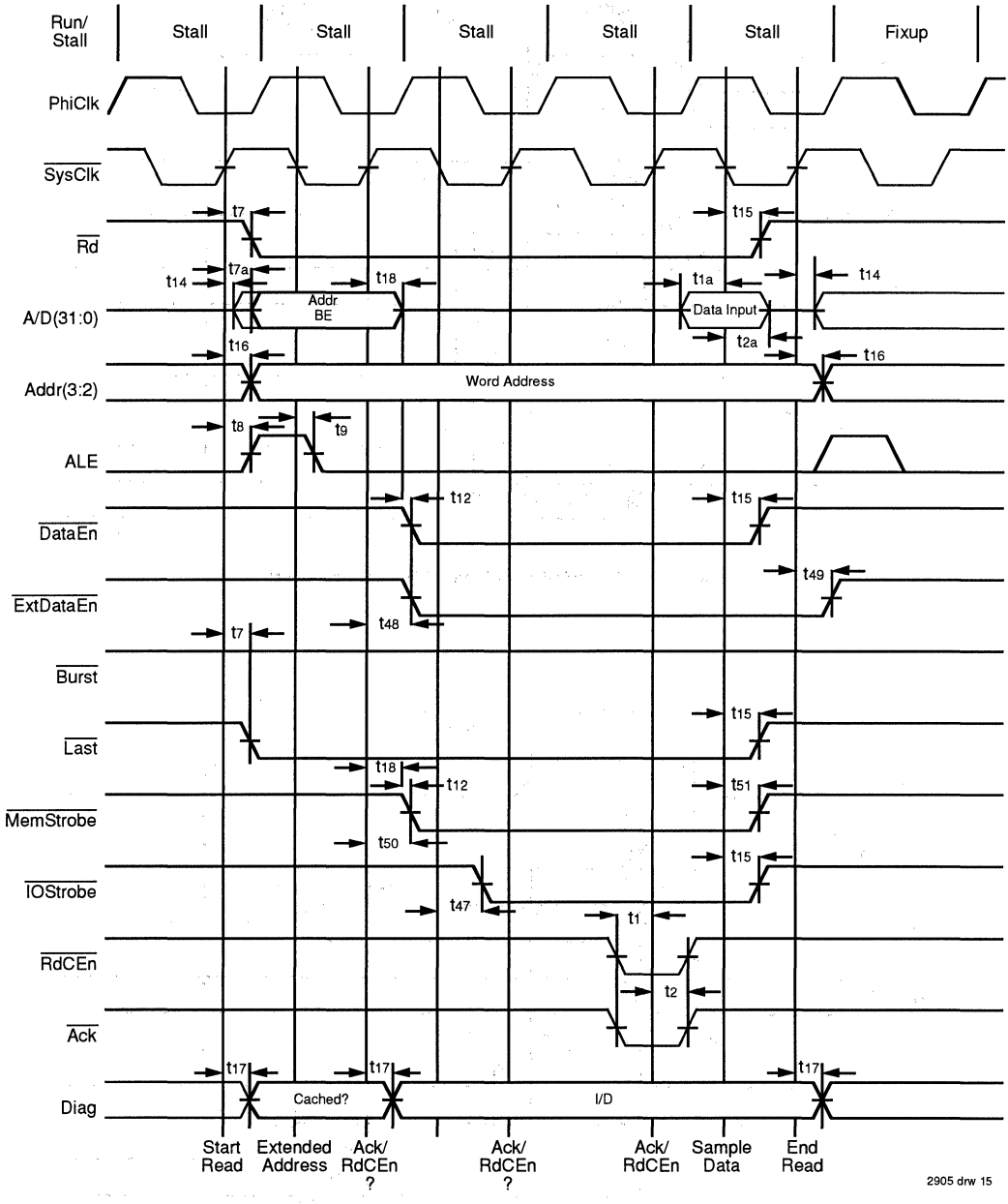


Figure 13. Single Datum Read

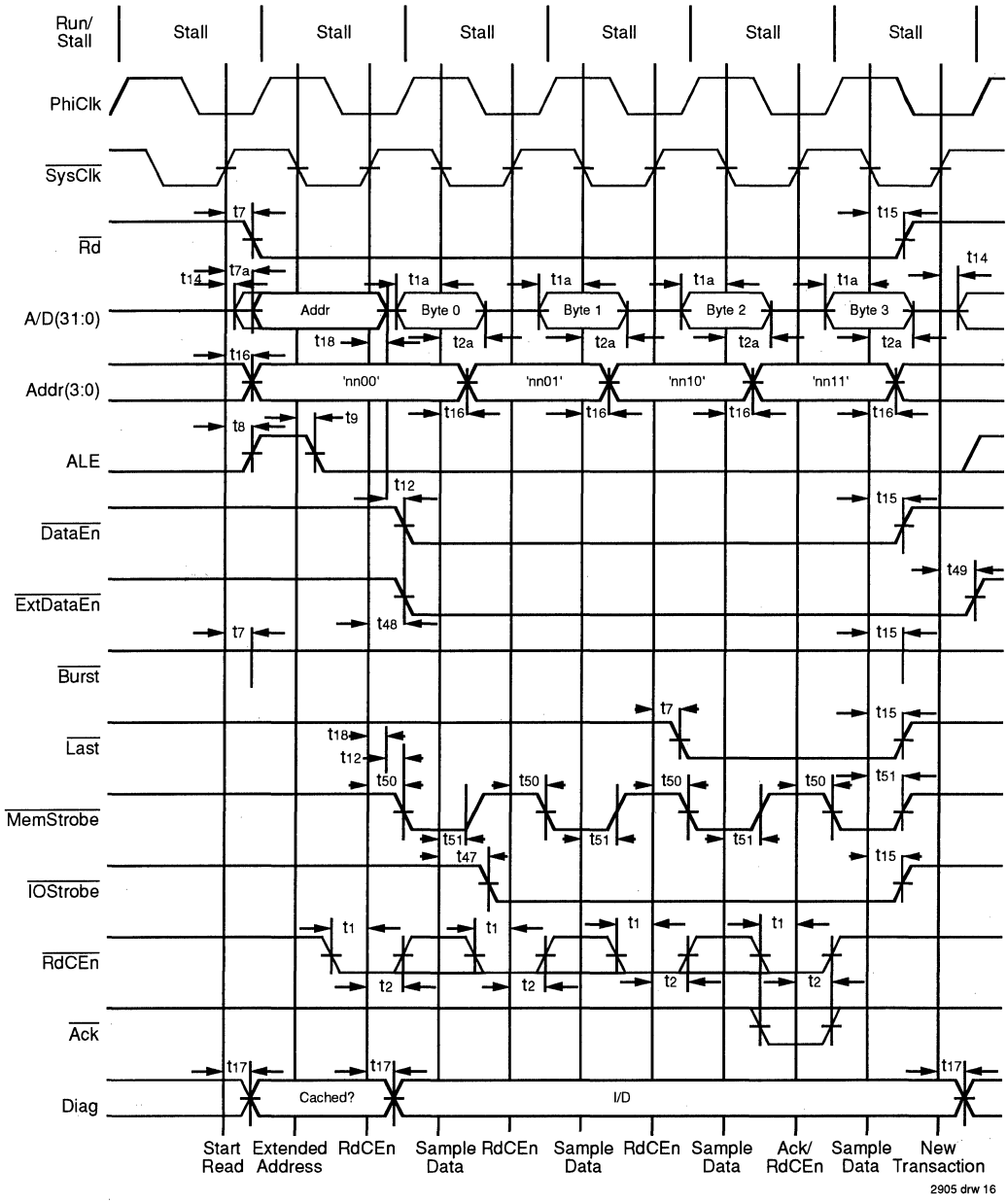


Figure 14. Mini-burst read of 32-bit datum from 8-bit wide memory port

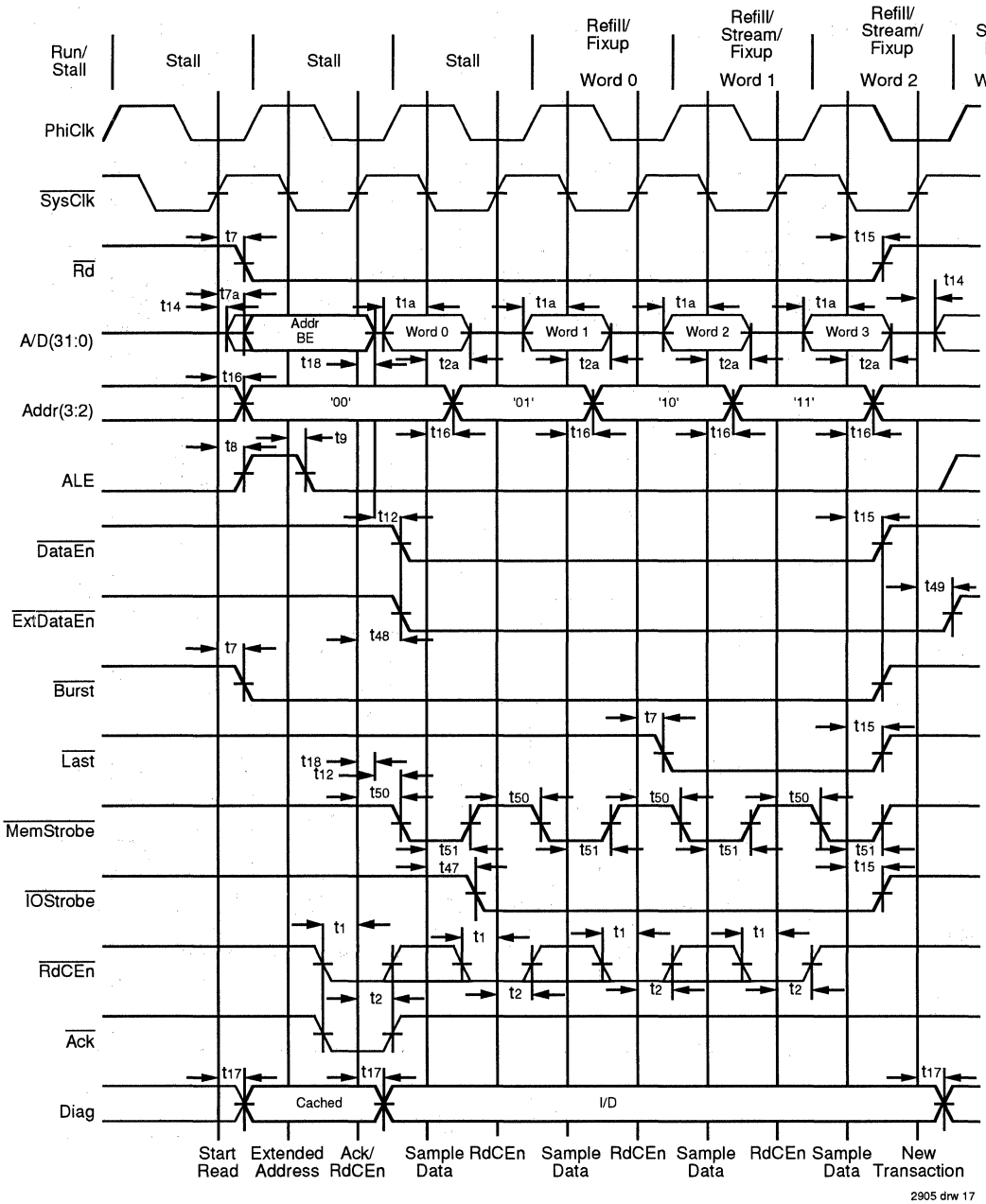


Figure 15. R3041 Quad Word Read

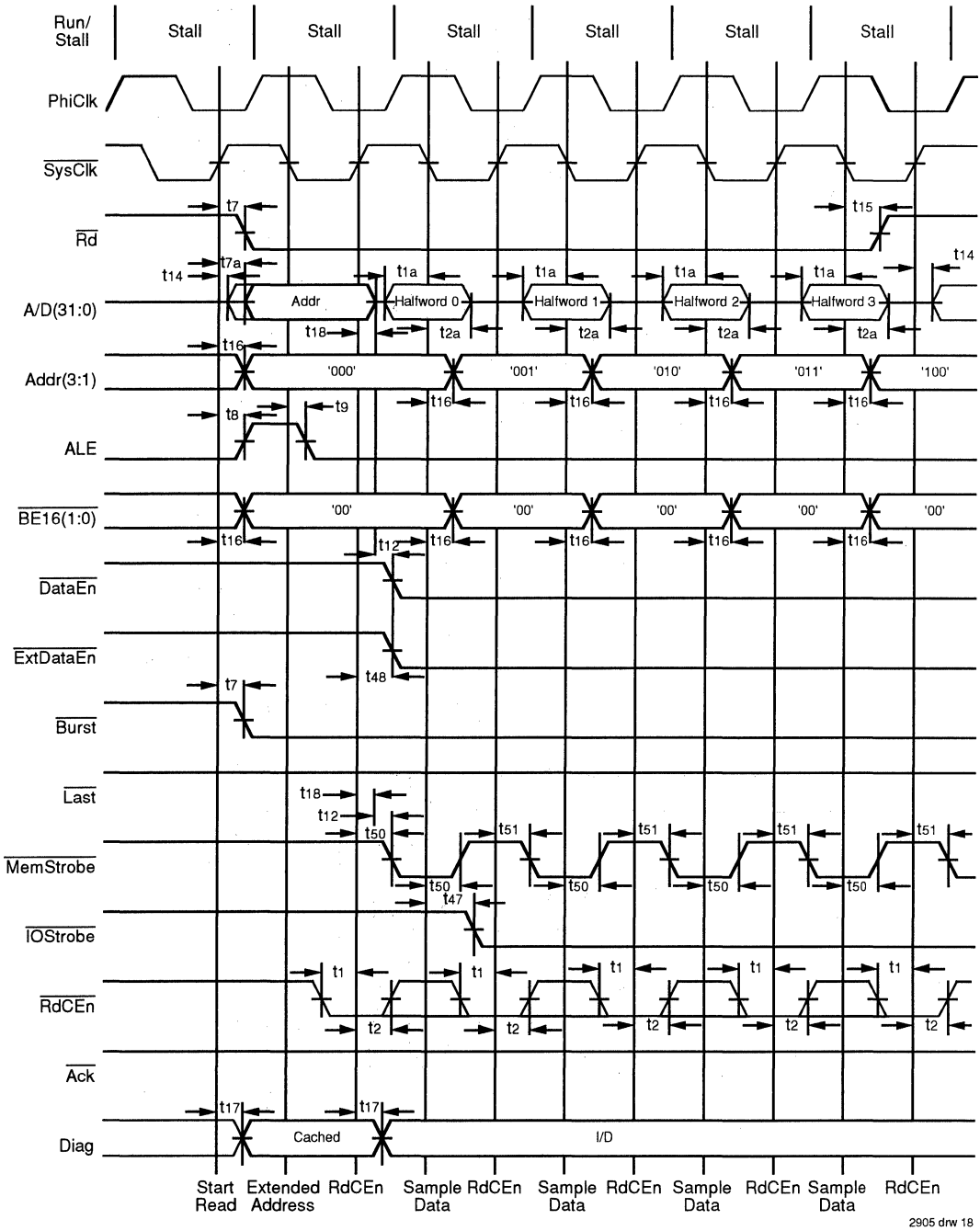


Figure 16 (a). Quad Word Read to 16-bit wide Memory Port

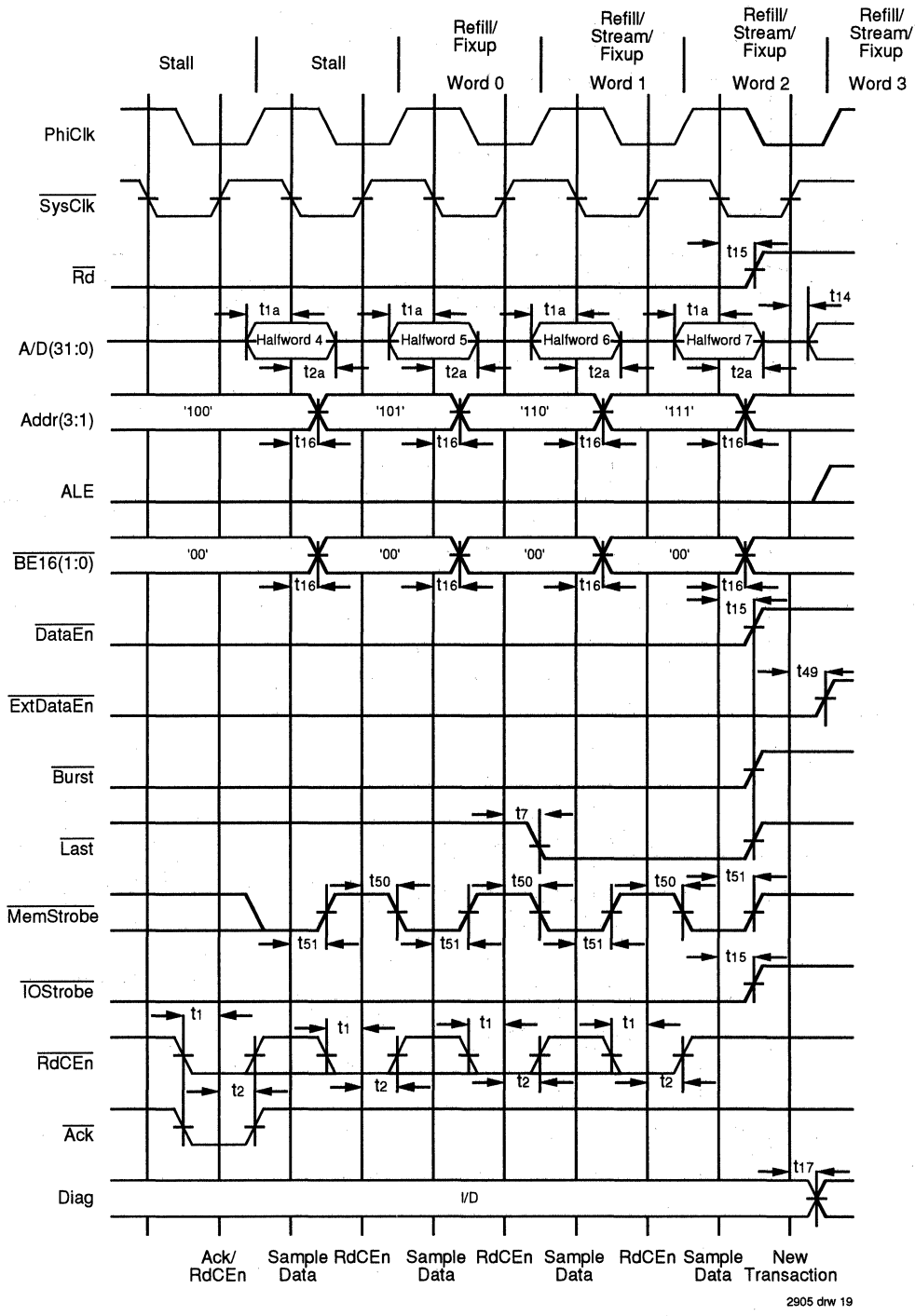


Figure 16 (b). End of Quad Word read from 16-bit Wide Memory Port

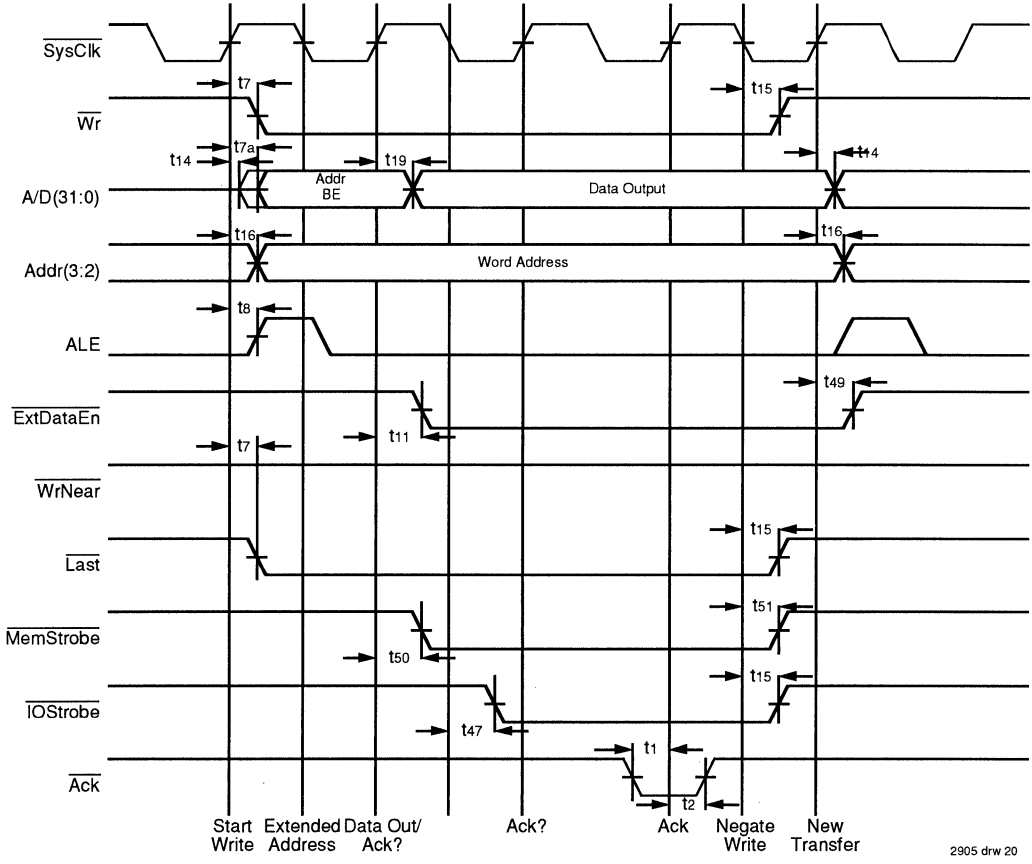


Figure 17. Basic Write to 32-bit Memory Port

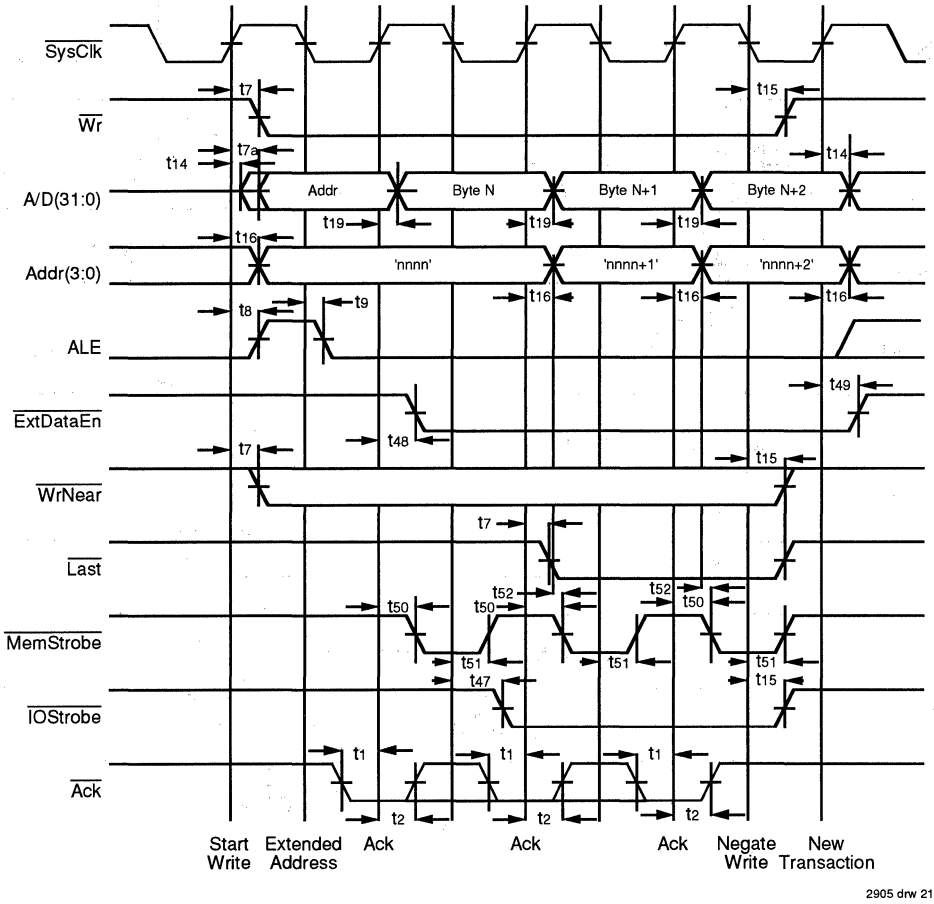


Figure 18. Tri-Byte Mini-burst Write to 8-bit Port

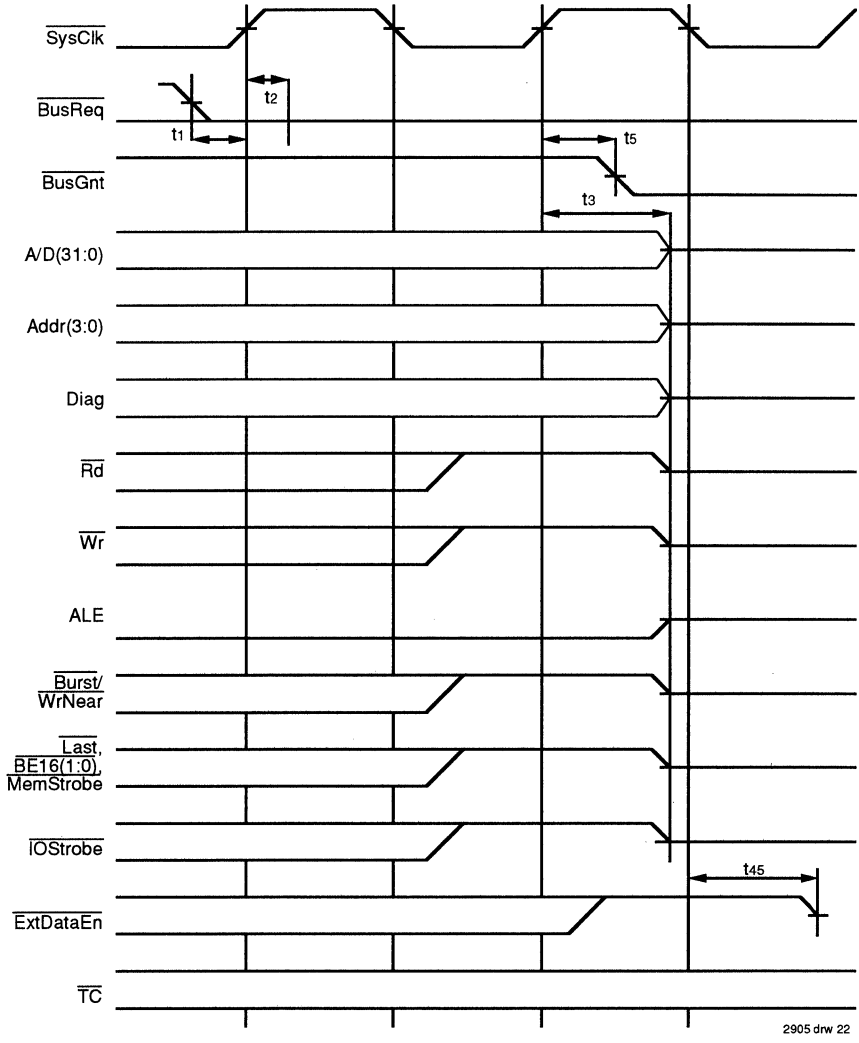


Figure 19. Request and Relinquish of R3041 Bus to External Master

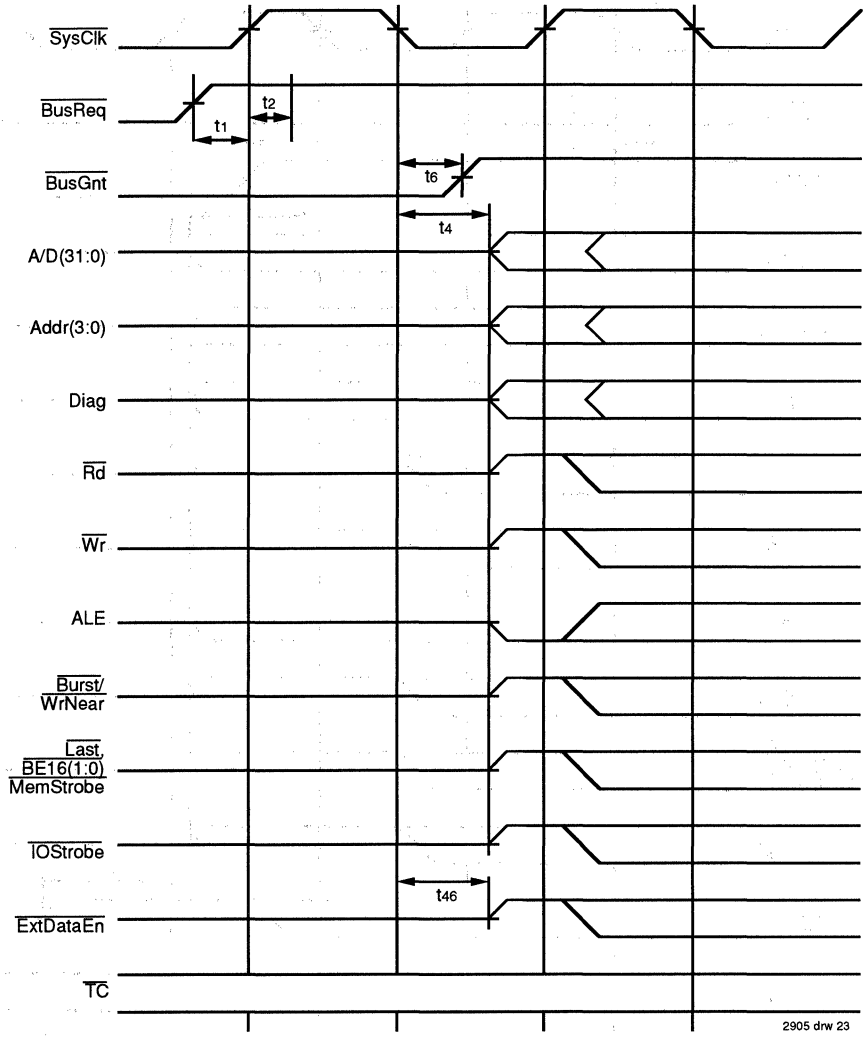


Figure 20. R3041 Regaining Bus Mastership

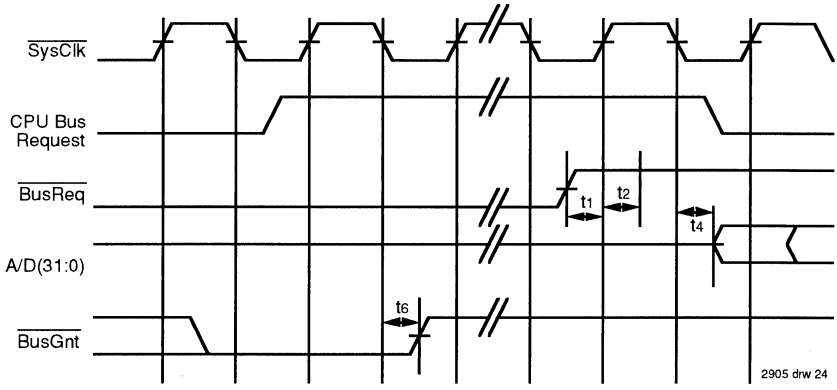


Figure 21. R3041 DMA Pulse Protocol

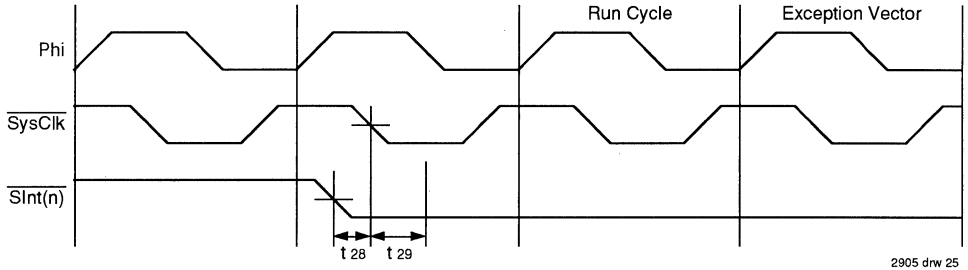


Figure 22. Synchronized Interrupt Input Timing

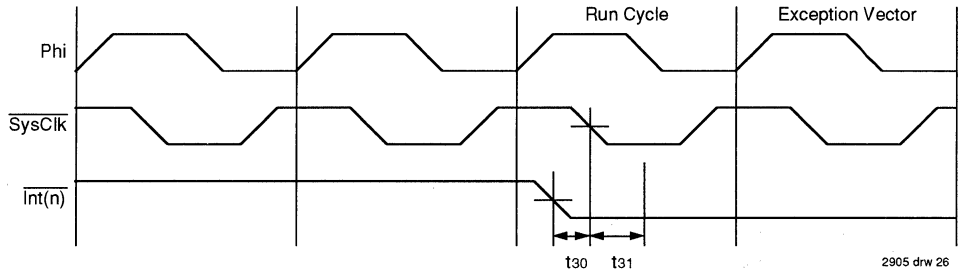


Figure 23. Direct Interrupt Input Timing

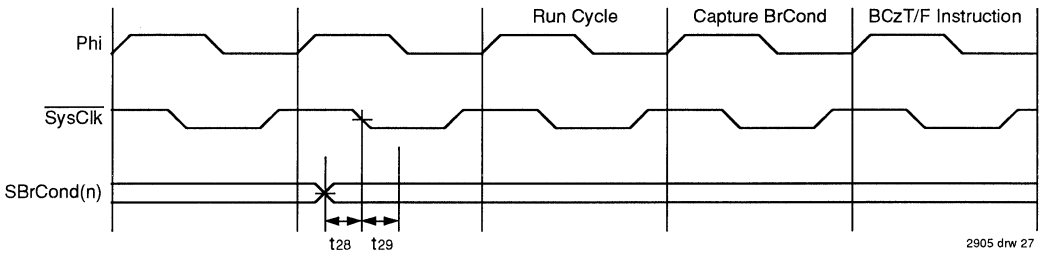


Figure 24. Synchronized Branch Condition Input Timing

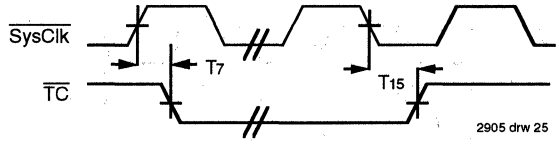
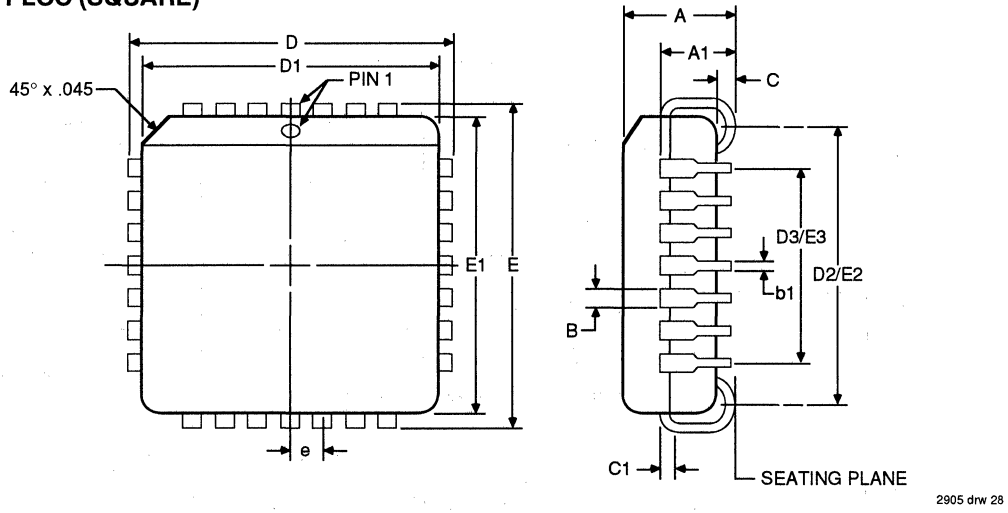


Figure 25. TC Output

84 LEAD PLCC (SQUARE)

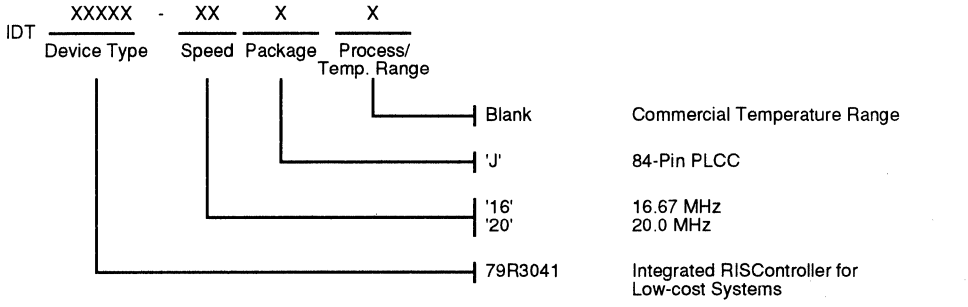


DWG #	J84-1	
# of Leads	84	
Symbol	Min.	Max.
A	165	.180
A1	.095	.115
B	.026	.032
b1	.013	.021
C	.020	.040
C1	.008	.012
D	1.185	1.195
D1	1.150	1.156
D2/E2	1.090	1.130
D3/E3	1.000 REF	
E	1.185	1.195
E1	1.150	1.156
e	.050 BSC	
ND/NE	21	

2905 tbl 13

NOTES:
1. All dimensions are in inches, unless otherwise noted.
2. BSC—Basic lead Spacing between Centers.
3. D & E do not include mold flash or protutions.
4. Formed leads shall be planar with respect to one another and within .004" at the seating plane.
5. ND & NE represent the number of leads in the D & E directions respectively.
6. D1 & E1 should be measured from the bottom of the package.
7. PLCC is pin & form compatible with MQUAD; the MQUAD package is used in other R3051 family members.

ORDERING INFORMATION



VALID COMBINATIONS

IDT 79R3041 - 16, 20J PLCC Package, Commercial Temperature Range

5

Integrated Device Technology, Inc.

IDT79R3051/79R3052 INTEGRATED RISControllers™

IDT79R3051™, 79R3051E
IDT79R3052™, 79R3052E

FEATURES:

- Instruction set compatible with IDT79R3000A and IDT79R3001 MIPS RISC CPUs
- High level of integration minimizes system cost, power consumption
  - IDT79R3000A /IDT79R3001 RISC Integer CPU
  - R3051 features 4kB of Instruction Cache
  - R3052 features 8kB of Instruction Cache
  - All devices feature 2kB of Data Cache
  - "E" Versions (Extended Architecture) feature full function Memory Management Unit, including 64-entry Translation Lookaside Buffer (TLB)
  - 4-deep write buffer eliminates memory write stalls
  - 4-deep read buffer supports burst refill from slow memory devices
  - On-chip DMA arbiter
  - Bus Interface minimizes design complexity
- Single clock input with 40%-60% duty cycle
- Direct interface to R3720/21/22 RISChipset™
- 35 MIPS, over 64,000 Dhrystones at 40MHz
- Low cost 84-pin PLCC packaging that's pin/package compatible with thermally-enhanced 84-pin MQUAD.
- Flexible bus interface allows simple, low cost designs
- 20, 25, 33, and 40MHz operation
- Complete software support
  - Optimizing compilers
  - Real-time operating systems
  - Monitors/debuggers
  - Floating Point Software
  - Page Description Languages

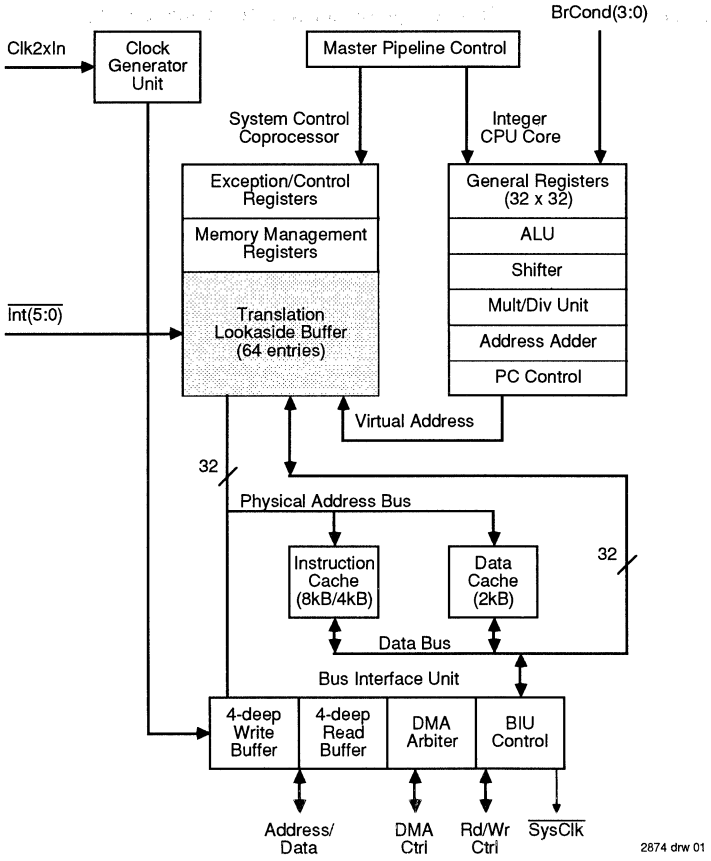


Figure 1. R3051 Family Block Diagram

INTRODUCTION

The IDT IDT79R3051 family is a series of high-performance 32-bit microprocessors featuring a high level of integration, and targeted to high-performance but cost sensitive embedded processing applications. The IDT79R3051 family is designed to bring the high-performance inherent in the MIPS RISC architecture into low-cost, simplified, power sensitive applications.

Functional units were integrated onto the CPU core in order to reduce the total system cost, without significantly degrading system performance. Thus, the IDT79R3051 family is able to offer 35 MIPS of integer performance at 40MHz without requiring external SRAM or caches.

Further, the IDT79R3051 family brings dramatic power reduction to these embedded applications, allowing the use of low-cost packaging for devices up to 25 MHz. The IDT79R3051 family allows customer applications to bring maximum performance at minimum cost.

Figure 1 shows a block level representation of the functional units within the IDT79R3051 family. The IDT79R3051 family could be viewed as the embodiment of a discrete solution built around the IDT79R3000A or IDT79R3001. However, by integrating this functionality on a single chip, dramatic cost and power reductions are achieved.

Currently, there are four members of the IDT79R3051 family family. All devices are pin and software compatible: the differences lie in the amount of instruction cache, and in the memory management capabilities of the processor:

- The IDT79R3052"E" incorporates 8kB of Instruction Cache, and features a full function memory management unit (MMU) including a 64-entry fully-associative Translation Lookaside Buffer (TLB). This is the same memory management unit incorporated in the IDT79R3000A and IDT79R3001.
- The IDT79R3052 also incorporates 8kB of Instruction Cache. However, the memory management unit is a much simpler subset of the capabilities of the enhanced versions of the architecture, and in fact does not use a TLB.
- The IDT79R3051"E" incorporates 4kB of Instruction Cache. Additionally, this device features the same full function MMU (including TLB file) as the IDT79R3052"E", and IDT79R3000A.
- The IDT79R3051 incorporates 4kB of Instruction Cache, and uses the simpler memory management model of the IDT79R3052.

An overview of the functional blocks incorporated in these devices follows.

CPU Core

The CPU core is a full 32-bit RISC integer execution engine, capable of sustaining close to single cycle execution rate. The CPU core contains a five stage pipeline, and 32 orthogonal 32-bit registers. The IDT79R3051 family implements the MIPS ISA. In fact, the execution engine of the IDT79R3051 family is the same as the execution engine of the IDT79R3000A (and IDT79R3001). Thus, the IDT79R3051 family is binary compatible with those CPU engines.

The execution engine of the IDT79R3051 family uses a five-stage pipeline to achieve close to single cycle execution. A new instruction can be started in every clock cycle; the execution engine actually processes five instructions concurrently (in various pipeline stages). Figure 2 shows the concurrency achieved by the IDT79R3051 family pipeline.

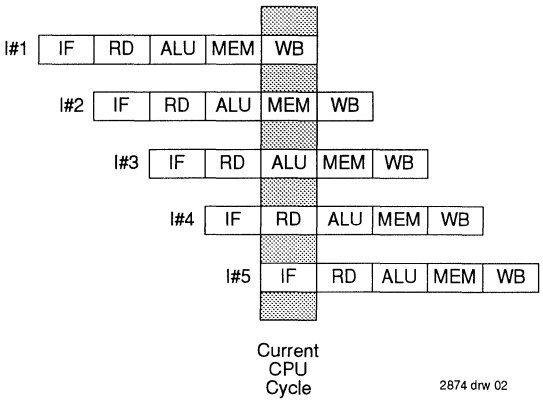


Figure 2. R3051 Family 5-Stage Pipeline

5

System Control Co-Processor

The R3051 family also integrates on-chip the System Control Co-processor, CP0. CP0 manages both the exception handling capability of the IDT79R3051 family, as well as the virtual to physical mapping of the IDT79R3051 family.

There are two versions of the IDT79R3051 family architecture: the Extended Architecture Versions (the IDT79R3051E and IDT79R3052E) contain a fully associative 64-entry TLB which maps 4kB virtual pages into the physical address space. The virtual to physical mapping thus includes kernel segments which are hard mapped to physical addresses, and kernel and user segments which are mapped on a page basis by the TLB into anywhere within the 4gB physical address space. In this TLB, 8 page translations can be "locked" by the kernel to insure deterministic response in real-time applications. These versions thus use the same MMU structure as that found in the IDT79R3000A and IDT79R3001. Figure 3 shows the virtual to physical address mapping found in the Extended Architecture versions of the processor family.

The Extended Architecture devices allow the system designer to implement kernel software to dynamically manage User task utilization of memory resources, and also allow the Kernel to effectively "protect" certain resources from user tasks. These capabilities are important in a number of embedded applications, from process control (where resource protection may be extremely important) to X-Window display systems (where virtual memory management is extremely important), and can also be used to simplify system debugging.

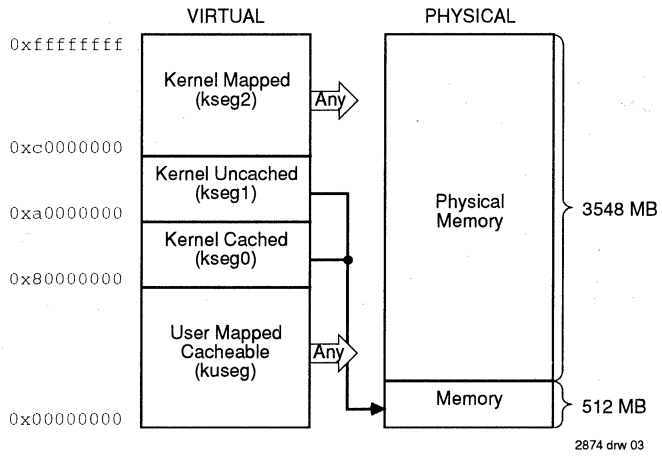


Figure 3. Virtual to Physical Mapping of Extended Architecture Versions

The base versions of the architecture (the IDT79R3051 and IDT79R3052) remove the TLB and institute a fixed address mapping for the various segments of the virtual address space. The base processors support distinct kernel and user mode operation without requiring page management software, leading to a simpler software model. The memory mapping used by these devices is illustrated in Figure 4. Note that the reserved address spaces shown are for compatibility with future family members; in the current family members, references to these addresses are translated in the same fashion as their respective segments, with no traps or exceptions taken.

When using the base versions of the architecture, the system designer can implement a distinction between the user tasks and the kernel tasks, without having to execute page management software. This distinction can take the form of physical memory protection, accomplished by address decoding, or in other forms. In systems which do not wish to implement memory protection, and wish to have the kernel and user tasks operate out of a single unified memory space, upper address lines can be ignored by the address decoder, and thus all references will be seen in the lower gigabyte of the physical address space.

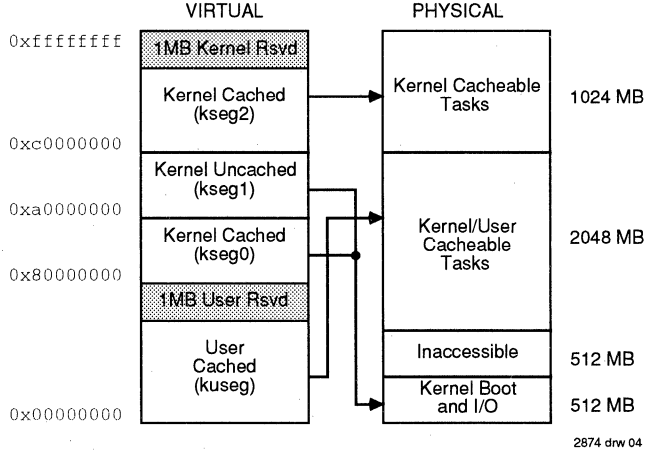


Figure 4. Virtual to Physical Mapping of Base Architecture Versions

Clock Generation Unit

The IDT79R3051 family is driven from a single input clock, capable of operating in a range of 40%-60% duty cycle. On-chip, the clock generator unit is responsible for managing the interaction of the CPU core, caches, and bus interface. The clock generator unit replaces the external delay line required in IDT79R3000A and IDT79R3001 based applications.

Instruction Cache

The current family includes two different instruction cache sizes: the IDT79R3051 family (the IDT79R3051 and IDT79R3051E) feature 4kB of instruction cache, and the IDT79R3052 and IDT79R3052E each incorporate 8kB of Instruction Cache. For all four devices, the instruction cache is organized as a line size of 16 bytes (four words). This relatively large cache achieves a hit rate well in excess of 95% in most applications, and substantially contributes to the performance inherent in the IDT79R3051 family. The cache is implemented as a direct mapped cache, and is capable of caching instructions from anywhere within the 4gB physical address space. The cache is implemented using physical addresses (rather than virtual addresses), and thus does not require flushing on context switch.

Data Cache

All four devices incorporate an on-chip data cache of 2kB, organized as a line size of 4 bytes (one word). This relatively large data cache achieves hit rates well in excess of 90% in most applications, and contributes substantially to the performance inherent in the IDT79R3051 family. As with the instruction cache, the data cache is implemented as a direct mapped physical address cache. The cache is capable of mapping any word within the 4gB physical address space.

The data cache is implemented as a write through cache, to insure that main memory is always consistent with the internal cache. In order to minimize processor stalls due to data write operations, the bus interface unit incorporates a 4-deep write buffer which captures address and data at the processor execution rate, allowing it to be retired to main memory at a much slower rate without impacting system performance.

Bus Interface Unit

The IDT79R3051 family uses its large internal caches to provide the majority of the bandwidth requirements of the execution engine, and thus can utilize a simple bus interface connected to slow memory devices.

The IDT79R3051 family bus interface utilizes a 32-bit address and data bus multiplexed onto a single set of pins. The bus interface unit also provides an ALE signal to demultiplex the A/D bus, and simple handshake signals to process processor read and write requests. In addition to the read and write interface, the IDT79R3051 family incorporates a DMA arbiter, to allow an external master to control the external bus.

The IDT79R3051 family incorporates a 4-deep write buffer to decouple the speed of the execution engine from the speed of the memory system. The write buffers capture and FIFO processor address and data information in store operations, and presents it to the bus interface as write transactions at the rate the memory system can accommodate.

The IDT79R3051/52 read interface performs both single word reads and quad word reads. Single word reads work with a simple handshake, and quad word reads can either utilize the simple handshake (in lower performance, simple systems) or utilize a tighter timing mode when the memory system can burst data at the processor clock rate. Thus, the system designer can choose to utilize page or nibble mode DRAMs (and possibly use interleaving), if desired, in high-performance systems, or use simpler techniques to reduce complexity.

In order to accommodate slower quad word reads, the IDT79R3051 family incorporates a 4-deep read buffer FIFO, so that the external interface can queue up data within the processor before releasing it to perform a burst fill of the internal caches. Depending on the cost vs. performance tradeoffs appropriate to a given application, the system design engineer could include true burst support from the DRAM to provide for high-performance cache miss processing, or utilize the read buffer to process quad word reads from slower memory systems.

SYSTEM USAGE

The IDT79R3051 family has been specifically designed to easily connect to low-cost memory systems. Typical low-cost memory systems utilize slow EPROMs, DRAMs, and application specific peripherals. These systems may also typically contain large, slow static RAMs, although the IDT79R3051 family has been designed to not specifically require the use of external SRAMs.

Figure 5 shows a typical system block diagram. Transparent latches are used to de-multiplex the IDT79R3051/52 address and data busses from the A/D bus. The data paths between the memory system elements and the R3051 family A/D bus is managed by simple octal devices. A small set of simple PALs can be used to control the various data path elements, and to control the handshake between the memory devices and the CPU.

Alternately, the memory interface can be constructed using the IDT79R3051 family RISChipset, which includes DRAM control, data path control for interleaved memories, and other general memory and system interface control functions. These devices are described in separate data sheets. Figure 6 illustrates a simple system constructed using the R3051 RISChipset.

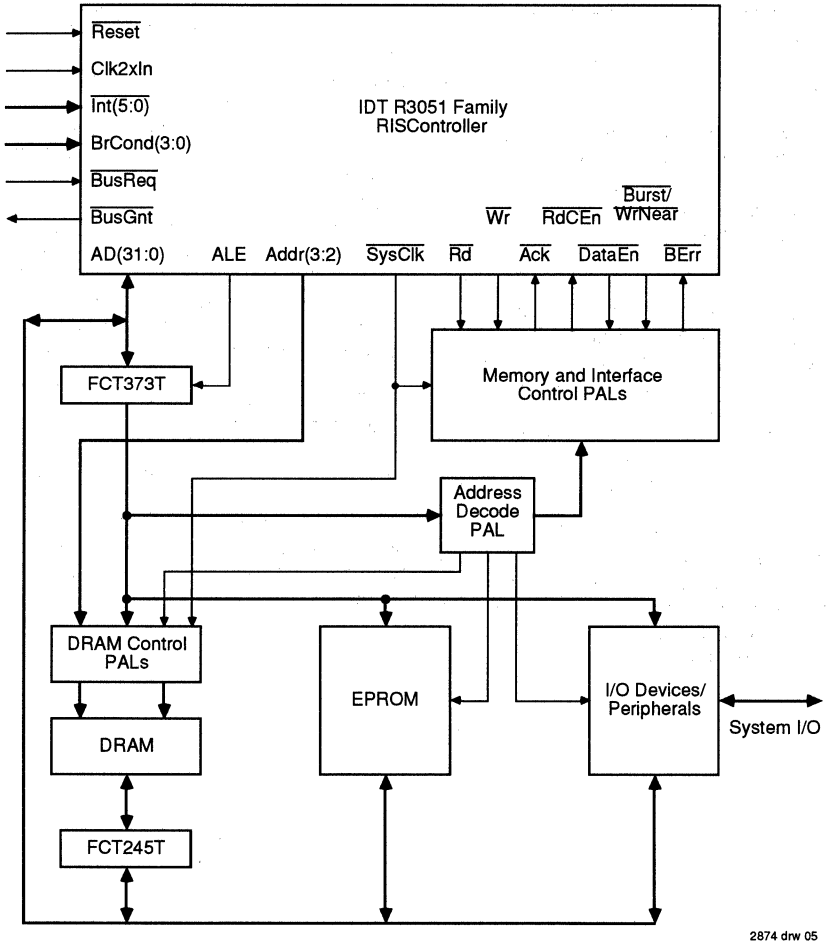


Figure 5. Typical R3051 Family Based System

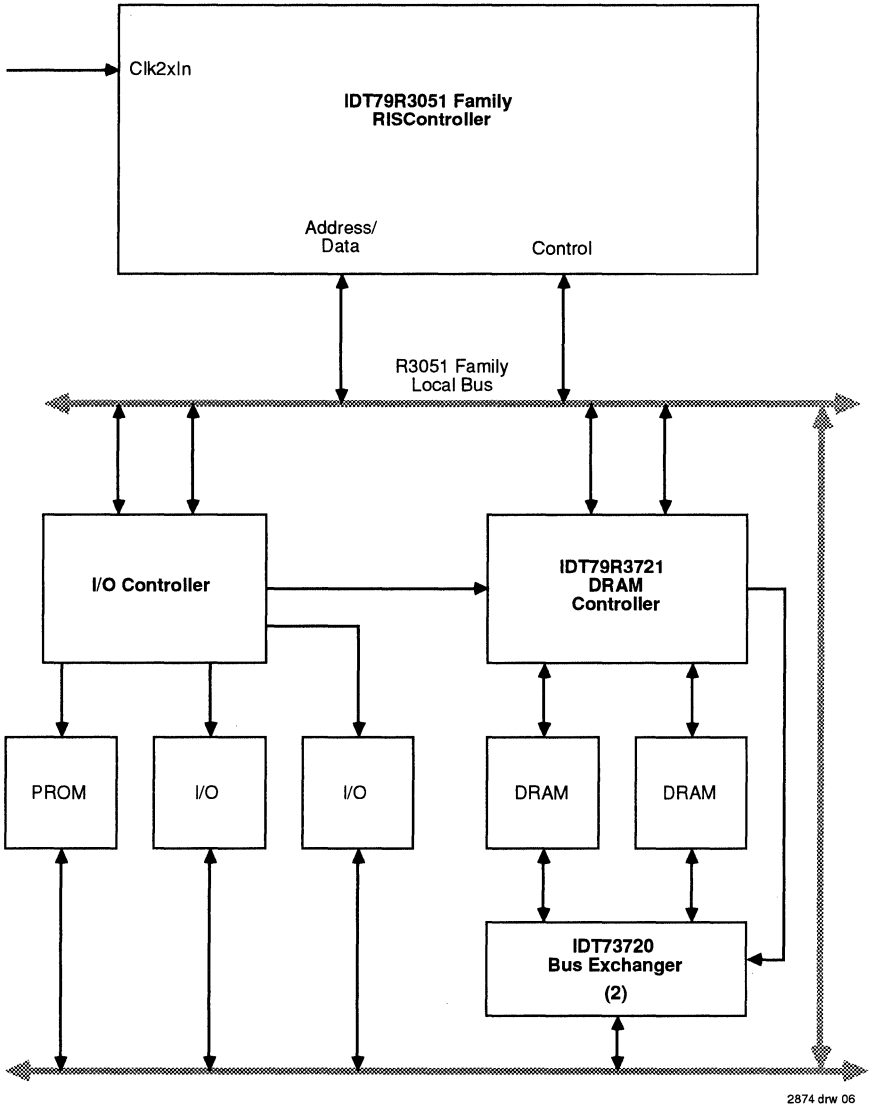


Figure 6. R3051 Family Chip Set Based System

DEVELOPMENT SUPPORT

The IDT79R3051 family is supported by a rich set of development tools, ranging from system simulation tools through prom monitor support, logic analysis tools, and subsystem modules.

Figure 7 is an overview of the system development process typically used when developing IDT79R3051 family-based applications. The IDT79R3051 family is supported by powerful tools through all phases of project development. These tools allow timely, parallel development of hardware and software for IDT79R3051/52 based applications, and include tools such as:

- A program, Cache-3051, which allows the performance of an IDT79R3051 family based system to be modeled and understood without requiring actual hardware.
- Sable, an instruction set simulator.
- Optimizing compilers from MIPS, the acknowledged leader in optimizing compiler technology.
- IDT Cross development tools, available in a variety of development environments.
- The high-performance IDT floating point library software, which has been integrated into the compiler toolchain to allow software floating point to replace hardware floating point without modifying the original source code.
- The IDT Evaluation Board, which includes RAM, EPROM, I/O, and the IDT Prom Monitor.
- The IDT Laser Printer System board, which directly drives a low-cost print engine, and runs Microsoft TrueImage™ Page Description Language on top of PeerlessPage™ Advanced Printer Controller BIOS.
- Adobe PostScript™ Page Description Language, ported to the R3000 instruction set, runs on the IDT79R3051 family.
- The IDT Prom Monitor, which implements a full prom monitor (diagnostics, remote debug support, peek/poke, etc.).
- An In-Circuit Emulator, developed and sold by Embedded Performance, Inc.

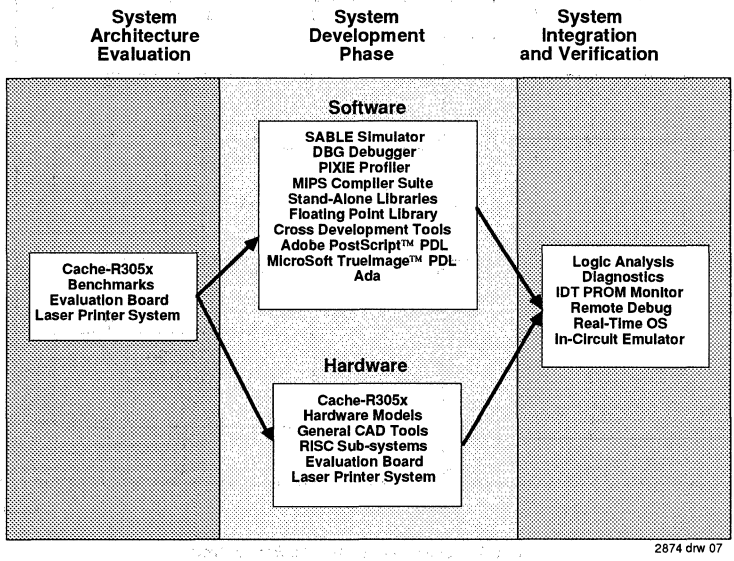


Figure 7. R3051 Family Development Toolchain

PERFORMANCE OVERVIEW

The IDT79R3051 family achieves a very high-level of performance. This performance is based on:

- **An efficient execution engine.** The CPU performs ALU operations and store operations at a single cycle rate, and has an effective load time of 1.3 cycles, and branch execution rate of 1.5 cycles (based on the ability of the compilers to avoid software interlocks). Thus, the execution engine achieves over 35 MIPS performance when operating out of cache.
- **Large on-chip caches.** The IDT79R3051 family contains caches which are substantially larger than those on the majority of today's embedded microprocessors. These large caches minimize the number of bus transactions required, and allow the R3051 family to achieve actual sustained performance very close to its peak execution rate.
- **Autonomous multiply and divide operations.** The IDT79R3051 family features an on-chip integer multiplier/divide unit which is separate from the other ALU. This allows the IDT79R3051 family to perform multiply or divide operations in parallel with other integer operations, using a single multiply or divide instruction rather than "step" operations.
- **Integrated write buffer.** The IDT79R3051 family features a four deep write buffer, which captures store target addresses and data at the processor execution rate and retires it to main memory at the slower main memory access rate. Use of on-chip write buffers eliminates the need for the processor to stall when performing store operations.
- **Burst read support.** The IDT79R3051 family enables the system designer to utilize page mode or nibble mode RAMs when performing read operations to minimize the main memory read penalty and increase the effective cache hit rates.

These techniques combine to allow the processor to achieve 35 MIPS integer performance, and over 64,000 dhrystones at 40MHz without the use of external caches or zero wait-state memory devices.

SELECTABLE FEATURES

The IDT79R3051 family allows the system designer to configure some aspects of operation. These aspects are established when the device is reset, and include:

- **Big Endian vs. Little Endian operation:** The part can be configured to operate with either byte ordering convention, and in fact may also be dynamically switched between the two conventions. This facilitates the porting of applications from other processor architectures, and also permits intercommunications between various types of processors and databases.
- **Data cache refill of one or four words:** The memory system must be capable of performing 4 word transfers to satisfy cache misses. This option allows the system designer to choose between one and four word refill on data cache misses, depending on the performance each option brings to his application.

THERMAL CONSIDERATIONS

The IDT79R3051 family utilizes special packaging techniques to improve the thermal properties of high-speed processors. Thus, all versions of the IDT79R3051 family are packaged in cavity down packaging.

The lowest cost members of the family use a standard cavity down, injection molded PLCC package (the "J" package). This package, coupled with the power reduction techniques employed in the design of the IDT79R3051 family, allows operation at speeds to 25MHz. However, at higher speeds, additional thermal care must be taken.

Thus, the IDT79R3051 family is also available in the MQUAD package (the "MJ" package), which is an all aluminum package with the die attached to a normal copper leadframe mounted to the aluminum casing. The MQUAD allows for a more efficient thermal transfer between the die and the case of the part due to the heat spreading effect of the aluminum. The aluminum offers less internal resistance from one end of the package to the other, reducing the temperature gradient across the package and therefore presenting a greater area for convection and conduction to the PCB for a given temperature. Even nominal amounts of airflow will dramatically reduce the junction temperature of the die, resulting in cooler operation. The MQUAD package is available at all frequencies, and is pin and form compatible with the PLCC package. Thus, designers can choose to utilize this package without changing their PCB.

Finally, the IDT79R3051 family is also available in a cavity down PGA with integral thermal slug. As with the MQUAD package, this package is highly thermally efficient, and is appropriate for use in more extreme temperature conditions, such as military applications.

The members of the IDT79R3051 family are guaranteed in a case temperature range of 0°C to +95°C. The type of package, speed (power) of the device, and airflow conditions, affect the equivalent ambient conditions which meet this specification.

The equivalent allowable ambient temperature, T_A, can be calculated using the thermal resistance from case to ambient ($Ø_{CA}$) of the given package. The following equation relates ambient and case temperature:

$$T_A = T_C - P * Ø_{CA}$$

where P is the maximum power consumption at hot temperature, calculated by using the maximum Icc specification for the device.

Typical values for $Ø_{CA}$ at various airflows are shown in Table 1 for the various packages.

	Airflow (ft/min)					
ØCA	**0**	**200**	**400**	**600**	**800**	**1000**
"J" Package	29	26	21	18	16	15
"MJ" Package*	22	14	12	11	9	8
PGA Package	29	15	9	7	6	5

2874 tbl 01

Table 1. Thermal Resistance ($Ø_{CA}$) at Various Airflows (*estimated: final values tbd)

PIN DESCRIPTION

PIN NAME	I/O	DESCRIPTION
A/D(31:0)	I/O	**Address/Data:** A 32-bit time multiplexed bus which indicates the desired address for a bus transaction in one phase, and which is used to transmit data between the CPU and external memory resources during the rest of the transfer. Bus transactions on this bus are logically separated into two phases: during the first phase, information about the transfer is presented to the memory system to be captured using the ALE output. This information consists of: **Address(31:4)**: The high-order address for the transfer is presented on A/D(31:4). **$\overline{BE}$(3:0)**: These strobes indicate which bytes of the 32-bit bus will be involved in the transfer, and are presented on A/D(3:0). During write cycles, the bus contains the data to be stored and is driven from the internal write buffer. On read cycles, the bus receives the data from the external resource, in either a single data transaction or in a burst of four words, and places it into the on-chip read buffer.
Addr(3:2)	O	**Low Address (3:2)** A 2-bit bus which indicates which word is currently expected by the processor. Specifically, this two bit bus presents either the address bits for the single word to be transferred (writes or single datum reads) or functions as a two bit counter starting at '00' for burst read operations.
Diag(1)	O	**Diagnostic Pin 1.** This output indicates whether the current bus read transaction is due to an on-chip cache miss, and also presents part of the miss address. The value output on this pin is time multiplexed: **Cached:** During the phase in which the A/D bus presents address information, this pin is an active high output which indicates whether the current read is a result of a cache miss. The value of this pin at this time in other than read cycles is undefined. **Miss Address (3):** During the remainder of the read operation, this output presents address bit (3) of the address the processor was attempting to reference when the cache miss occurred. Regardless of whether a cache miss is being processed, this pin reports the transfer address during this time.
Diag(0)	O	**Diagnostic Pin 0.** This output distinguishes cache misses due to instruction references from those due to data references, and presents the remaining bit of the miss address. The value output on this pin is also time multiplexed: **I/$\overline{D}$:** If the "Cached" Pin indicates a cache miss, then a high on this pin at this time indicates an instruction reference, and a low indicates a data reference. If the read is not due to a cache miss but rather an uncached reference, then this pin is undefined during this phase. **Miss Address (2):** During the remainder of the read operation, this output presents address bit (2) of the address the processor was attempting to reference when the cache miss occurred. Regardless of whether a cache miss is being processed, this pin reports the transfer address during this time.
ALE	O	**Address Latch Enable:** Used to indicate that the A/D bus contains valid address information for the bus transaction. This signal is used by external logic to capture the address for the transfer, typically using transparent latches.
$\overline{DataEn}$	O	**External Data Enable:** This signal indicates that the A/D bus is no longer being driven by the processor during read cycles, and thus the external memory system may enable the drivers of the memory system onto this bus without having a bus conflict occur. During write cycles, or when no bus transaction is occurring, this signal is negated, thus disabling the external memory drivers.

2874 tbl 02

PIN DESCRIPTION (Continued):

PIN NAME	I/O	DESCRIPTION
Burst/ WrNear	O	**Burst Transfer/Write Near:** On read transactions, the Burst signal indicates that the current bus read is requesting a block of four contiguous words from memory. This signal is asserted only in read cycles due to cache misses; it is asserted for all I-Cache miss read cycles, and for D-Cache miss read cycles if selected at device reset time. On write transactions, the WrNear output tells the external memory system that the bus interface unit is performing back-to-back write transactions to an address within the same 256 word page as the prior write transaction. This signal is useful in memory systems which employ page mode or static column DRAMs, and allows near writes to be retired quickly.
Rd	O	**Read:** An output which indicates that the current bus transaction is a read.
Wr	O	**Write:** An output which indicates that the current bus transaction is a write.
Ack	I	**Acknowledge:** An input which indicates to the device that the memory system has sufficiently processed the bus transaction, and that the CPU may either terminate the write cycle or process the read data from this read transfer.
RdCEn	I	**Read Buffer Clock Enable:** An input which indicates to the device that the memory system has placed valid data on the A/D bus, and that the processor may move the data into the on-chip Read Buffer.
SysClk	O	**System Reference Clock:** An output from the CPU which reflects the timing of the internal processor "Sys" clock. This clock is used to control state transitions in the read buffer, write buffer, memory controller, and bus interface unit.
BusReq	I	**DMA Arbiter Bus Request:** An input to the device which requests that the CPU tri-state its bus interface signals so that they may be driven by an external master.
BusGnt	O	**DMA Arbiter Bus Grant.** An output from the CPU used to acknowledge that a BusReq has been detected, and that the bus is relinquished to the external master.
SBrCond(3:2) BrCond(1:0)	I	**Branch Condition Port:** These external signals are internally connected to the CPU signals CpCond(3:0). These signals can be used by the branch on co-processor condition instructions as input ports. There are two types of Branch Condition inputs: the SBrCond inputs have special internal logic to synchronize the inputs, and thus may be driven by asynchronous agents. The direct Branch Condition inputs must be driven synchronously.
BErr	I	**Bus Error:** Input to the bus interface unit to terminate a bus transaction due to an external bus error. This signal is only sampled during read and write operations. If the bus transaction is a read operation, then the CPU will take a bus error exception.
Int(5:3) SInt(2:0)	I	**Processor Interrupt:** During normal operation, these signals are logically the same as the Int(5:0) signals of the R3000. During processor reset, these signals perform mode initialization of the CPU, but in a different (simpler) fashion than the interrupt signals of the R3000. There are two types of interrupt inputs: the SInt inputs are internally synchronized by the processor, and may be driven by an asynchronous external agent. The direct interrupt inputs are not internally synchronized, and thus must be externally synchronized to the CPU. The direct interrupt inputs have one cycle lower latency than the synchronized interrupts.
Clk2xIn	I	**Master Clock Input:** This is a double frequency input used to control the timing of the CPU.
Reset	I	**Master Processor Reset:** This signal initializes the CPU. Mode selection is performed during the last cycle of Reset.
Rsvd(4:0)	I/O	**Reserved:** These five signal pins are reserved for testing and for future revisions of this device. Users must not connect these pins.

2874 tbl 03

5

ABSOLUTE MAXIMUM RATINGS(1, 3)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_C	Operating Case Temperature	0 to +95	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +155	°C
V_{IN}	Input Voltage	–0.5 to +7.0	–0.5 to +7.0	V

2874 tbl 04

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN} minimum = –3.0V for pulse width less than 15ns. V_{IN} should not exceed V_{CC} +0.5V.
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

AC TEST CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{IH}	Input HIGH Voltage	3.0	—	V
V_{IL}	Input LOW Voltage	—	0.4	V
V_{IHS}	Input HIGH Voltage	3.5	—	V
V_{ILS}	Input LOW Voltage	—	0.4	V

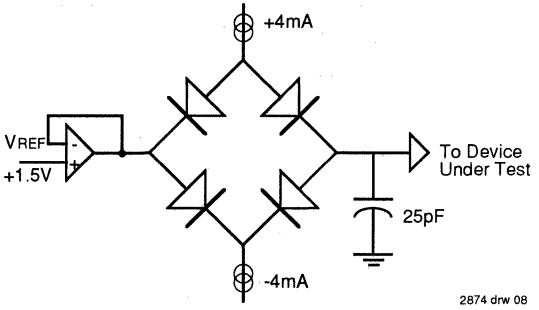
2874 tbl 05

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	–55°C to +125°C (Case)	0V	5.0 ±10%
Commercial	0°C to +95°C (Case)	0V	5.0 ±5%

2874 tbl 06

OUTPUT LOADING FOR AC TESTING



2874 drw 08

DC ELECTRICAL CHARACTERISTICS (T_C = 0°C to +95°C, V_{CC} = +5.0V ±5%)

Symbol	Parameter	Test Conditions	20MHz		25MHz		33.33MHz		40MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4mA	3.5	—	3.5	—	3.5	—	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	—	0.4	—	0.4	—	0.4	—	0.4	V
V_{IH}	Input HIGH Voltage(3)	—	2.0	—	2.0	—	2.0	—	2.0	—	V
V_{IL}	Input LOW Voltage(1)	—	—	0.8	—	0.8	—	0.8	—	0.8	V
V_{IHS}	Input HIGH Voltage(2,3)	—	3.0	—	3.0	—	3.0	—	3.0	—	V
V_{ILS}	Input LOW Voltage(1,2)	—	—	0.4	—	0.4	—	0.4	—	0.4	V
C_{IN}	Input Capacitance(4)	—	—	10	—	10	—	10	—	10	pF
C_{OUT}	Output Capacitance(4)	—	—	10	—	10	—	10	—	10	pF
I_{CC}	Operating Current	V_{CC} = 5V, T_A = 25°C	—	400	—	450	—	600	—	700	mA
I_{IH}	Input HIGH Leakage	V_{IH} = VCC	—	100	—	100	—	100	—	100	µA
I_{IL}	Input LOW Leakage	V_{IL} = GND	–100	—	–100	—	–100	—	–100	—	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	–100	100	–100	100	–100	100	–100	100	µA

2874 tbl 07

NOTES:

1. V_{IL} Min. = –3.0V for pulse width less than 15ns. V_{IL} should not fall below –0.5V for larger periods.
2. V_{IHS} and V_{ILS} apply to Clk2xIn and $\overline{\text{Reset}}$.
3. V_{IH} should not be held above V_{CC} + 0.5V.
4. Guaranteed by design.

5

AC ELECTRICAL CHARACTERISTICS [1, 2, 3] (Tc = 0°C to +95°C, Vcc = +5.0V ±5%)

Symbol	Signals	Description	20MHz		25MHz		33.33MHz		40MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t1	$\overline{\text{BusReq}}$, $\overline{\text{Ack}}$, $\overline{\text{BusError}}$, $\overline{\text{RdCEn}}$,	Set-up to $\overline{\text{SysClk}}$ rising	6	—	5	—	4	—	3	—	ns
t1a	A/D	Set-up to $\overline{\text{SysClk}}$ falling	7	—	6	—	5	—	4.5	—	ns
t2	$\overline{\text{BusReq}}$, $\overline{\text{Ack}}$, $\overline{\text{BusError}}$, $\overline{\text{RdCEn}}$,	Hold from $\overline{\text{SysClk}}$ rising	4	—	4	—	3	—	3	—	ns
t2a	A/D	Hold from $\overline{\text{SysClk}}$ falling	2	—	2	—	1	—	1	—	
t3	A/D, Addr, Diag, ALE, $\overline{\text{Wr}}$ $\overline{\text{Burst/WrNear}}$, $\overline{\text{Rd}}$, $\overline{\text{DataEn}}$	Tri-state from $\overline{\text{SysClk}}$ rising	—	10	—	10	—	10	—	10	ns
t4	A/D, Addr, Diag, ALE, $\overline{\text{Wr}}$ $\overline{\text{Burst/WrNear}}$, $\overline{\text{Rd}}$, $\overline{\text{DataEn}}$	Driven from $\overline{\text{SysClk}}$ falling	—	10	—	10	—	10	—	10	ns
t5	$\overline{\text{BusGnt}}$	Asserted from $\overline{\text{SysClk}}$ rising	—	8	—	7	—	6	—	5	ns
t6	$\overline{\text{BusGnt}}$	Negated from $\overline{\text{SysClk}}$ falling	—	8	—	7	—	6	—	5	ns
t7	$\overline{\text{Wr}}$, $\overline{\text{Rd}}$, $\overline{\text{Burst/WrNear}}$, A/D	Valid from $\overline{\text{SysClk}}$ rising	—	5	—	5	—	4	—	3.5	ns
t8	ALE	Asserted from $\overline{\text{SysClk}}$ rising	—	4	—	4	—	3	—	3	ns
t9	ALE	Negated from $\overline{\text{SysClk}}$ falling	—	4	—	4	—	3	—	3	ns
t10	A/D	Hold from ALE negated	2	—	2	—	1.5	—	1.5	—	ns
t11	$\overline{\text{DataEn}}$	Asserted from $\overline{\text{SysClk}}$ falling	—	15	—	15	—	13	—	12	ns
t12	$\overline{\text{DataEn}}$	Asserted from A/D tri-state[4]	0	—	0	—	0	—	0	—	ns
t14	A/D	Driven from $\overline{\text{SysClk}}$ rising[4]	0	—	0	—	0	—	0	—	ns
t15	$\overline{\text{Wr}}$, $\overline{\text{Rd}}$, $\overline{\text{DataEn}}$, $\overline{\text{Burst/WrNear}}$	Negated from $\overline{\text{SysClk}}$ falling	—	7	—	6	—	5	—	4	ns
t16	Addr(3:2)	Valid from $\overline{\text{SysClk}}$	—	6	—	6	—	5	—	4.5	ns
t17	Diag	Valid from $\overline{\text{SysClk}}$	—	12	—	11	—	10	—	9	ns
t18	A/D	Tri-state from $\overline{\text{SysClk}}$ falling	—	10	—	10	—	9	—	8	ns
t19	A/D	$\overline{\text{SysClk}}$ falling to data out	—	12	—	11	—	10	—	9	ns
t20	Clk2xIn	Pulse Width High	10	—	8	—	6.5	—	5.6	—	ns
t21	Clk2xIn	Pulse Width Low	10	—	8	—	6.5	—	5.6	—	ns
t22	Clk2xIn	Clock Period	25	250	20	250	15	250	12.5	250	ns
t23	$\overline{\text{Reset}}$	Pulse Width from Vcc valid	200	—	200	—	200	—	200	—	µs
t24	$\overline{\text{Reset}}$	Minimum Pulse Width	32	—	32	—	32	—	32	—	tsys
t25	$\overline{\text{Reset}}$	Set-up to $\overline{\text{SysClk}}$ falling	6	—	5	—	4	—	3	—	ns
t26	$\overline{\text{Int}}$	Mode set-up to $\overline{\text{Reset}}$ rising	6	—	5	—	4	—	3	—	ns
t27	$\overline{\text{Int}}$	Mode hold from $\overline{\text{Reset}}$ rising	2.5	—	2.5	—	2.5	—	2.5	—	ns
t28	$\overline{\text{SInt}}$, SBrCond	Set-up to $\overline{\text{SysClk}}$ falling	6	—	5	—	4	—	3	—	ns
t29	$\overline{\text{SInt}}$, SBrCond	Hold from $\overline{\text{SysClk}}$ falling	3	—	3	—	2	—	2	—	ns
t30	$\overline{\text{Int}}$, BrCond	Set-up to $\overline{\text{SysClk}}$ falling	6	—	5	—	4	—	3	—	ns
t31	$\overline{\text{Int}}$, BrCond	Hold from $\overline{\text{SysClk}}$ falling	3	—	3	—	2	—	2	—	ns
tsys	$\overline{\text{SysClk}}$	Pulse Width	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	
t32	$\overline{\text{SysClk}}$	Clock High Time	t22 – 2	t22 + 2	t22 – 2	t22 + 2	t22 – 1	t22 + 1	t22 – 1	t22 + 1	ns
t33	$\overline{\text{SysClk}}$	Clock Low Time	t22 – 2	t22 + 2	t22 – 2	t22 + 2	t22 – 1	t22 + 1	t22 – 1	t22 + 1	ns
tderate	All outputs	Timing deration for loading over 25pf[4, 5]	—	0.5	—	0.5	—	0.5	—	0.5	ns/ 25pF

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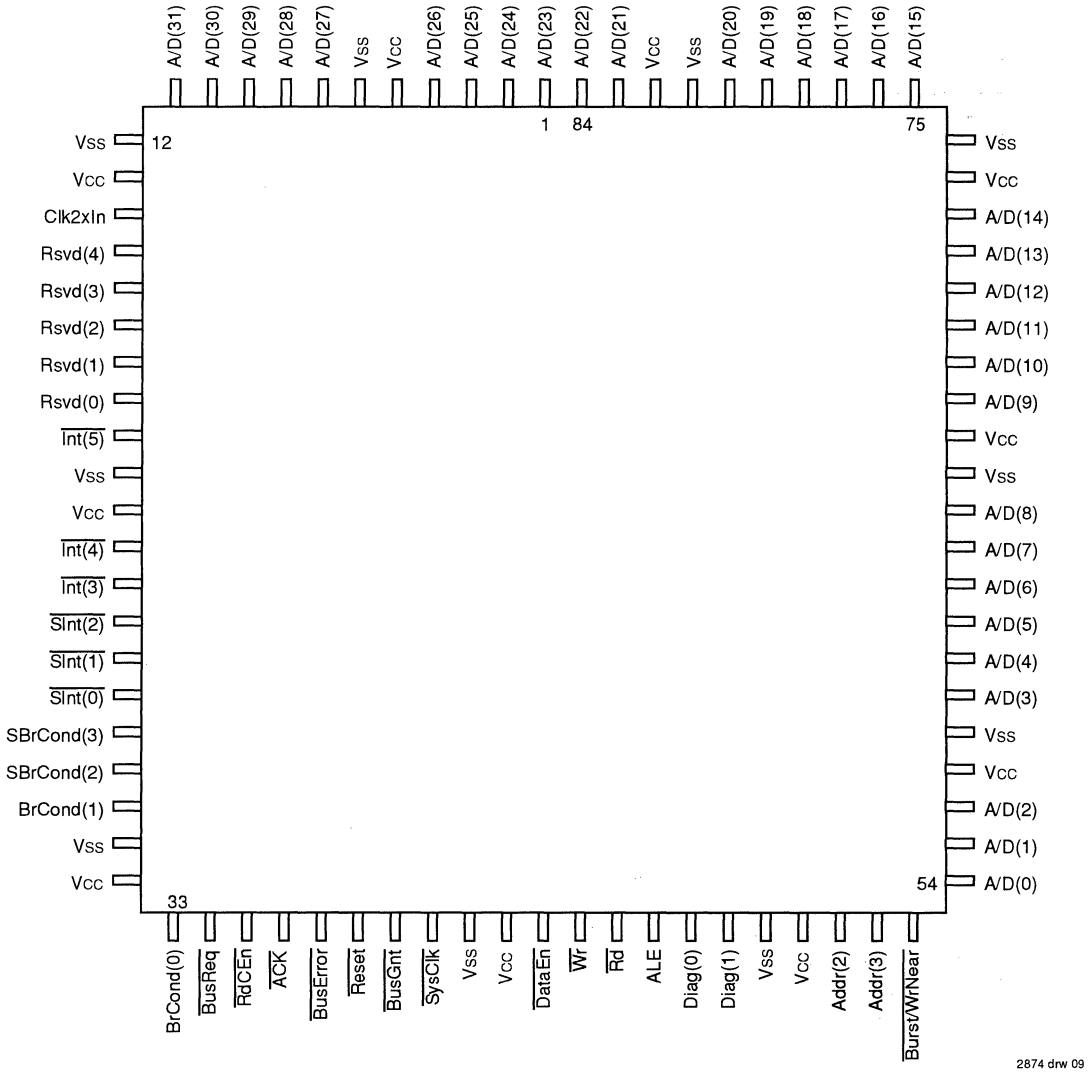
NOTES:

1. All timings referenced to 1.5V, with a rise and fall time of less than 2.5ns.
2. All outputs tested with 25pF loading.
3. The AC values listed here reference timing diagrams contained in the R3051 Family Hardware User's Manual.
4. Guaranteed by design.
5. This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25pF over the specified test load condition.

PIN CONFIGURATIONS



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84-Pin PLCC/MQUAD
Top View

NOTE:
Reserved Pins must not be connected.

PIN CONFIGURATIONS (CONTINUED)

	1	2	3	4	5	6	7	8	9	10	11	12
M	Vss	Clk2xIn	Rsvd (4)	Rsvd (2)	Rsvd (0)	Vss	$\overline{\text{Int}}$ (4)	$\overline{\text{Int}}$ (3)	$\overline{\text{SInt}}$ (1)	S BrCond (3)	S BrCond (2)	BrCond (0)
L	A/D (28)	A/D (30)	Vcc	Rsvd (3)	Rsvd (1)	$\overline{\text{Int}}$ (5)	Vcc	$\overline{\text{SInt}}$ (2)	$\overline{\text{SInt}}$ (0)	BrCond (1)	Vss	$\overline{\text{RdCEn}}$
K	A/D (27)	A/D (29)	A/D (31)							Vcc	$\overline{\text{BusReq}}$	$\overline{\text{ACK}}$
J	Vcc	Vss									$\overline{\text{Bus Error}}$	$\overline{\text{Reset}}$
H	A/D (25)	A/D (26)									$\overline{\text{BusGnt}}$	$\overline{\text{SysClk}}$
G	A/D (23)	A/D (24)									Vcc	Vss
F	A/D (21)	A/D (22)									$\overline{\text{Wr}}$	$\overline{\text{DataEn}}$
E	Vcc	Vss									ALE	$\overline{\text{Rd}}$
D	A/D (20)	A/D (19)									Diag (1)	Diag (0)
C	A/D (18)	A/D (16)	Vss							$\overline{\text{Burst/ WrNear}}$	Addr (2)	Vss
B	A/D (17)	Vcc	A/D (14)	A/D (11)	A/D (9)	A/D (8)	A/D (6)	A/D (4)	Vss	A/D (1)	Addr (3)	Vcc
A	A/D (15)	A/D (13)	A/D (12)	A/D (10)	Vcc	Vss	A/D (7)	A/D (5)	A/D (3)	Vcc	A/D (2)	A/D (0)

R3051
84-Pin Ceramic Pin Grid Array
(Cavity Down)

Bottom View

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84-Pin PGA with Integral Thermal Slug
BottomView

NOTE:
Reserved Pins must not be connected.

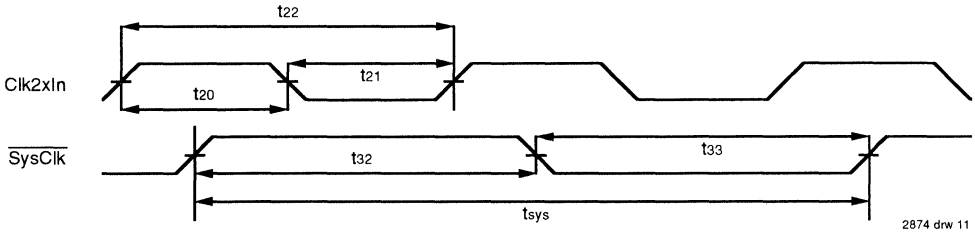


Figure 8. R3051 Family Clocking

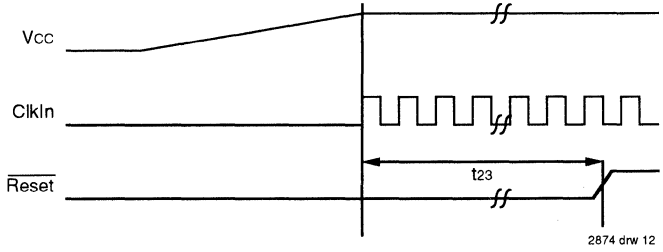


Figure 9. Power-On Reset Sequence

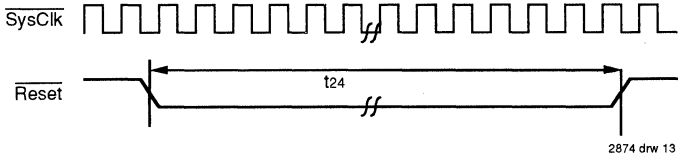


Figure 10. Warm Reset Sequence

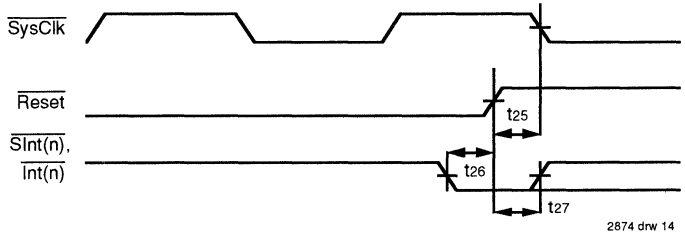


Figure 11. Mode Selection and Negation of Reset

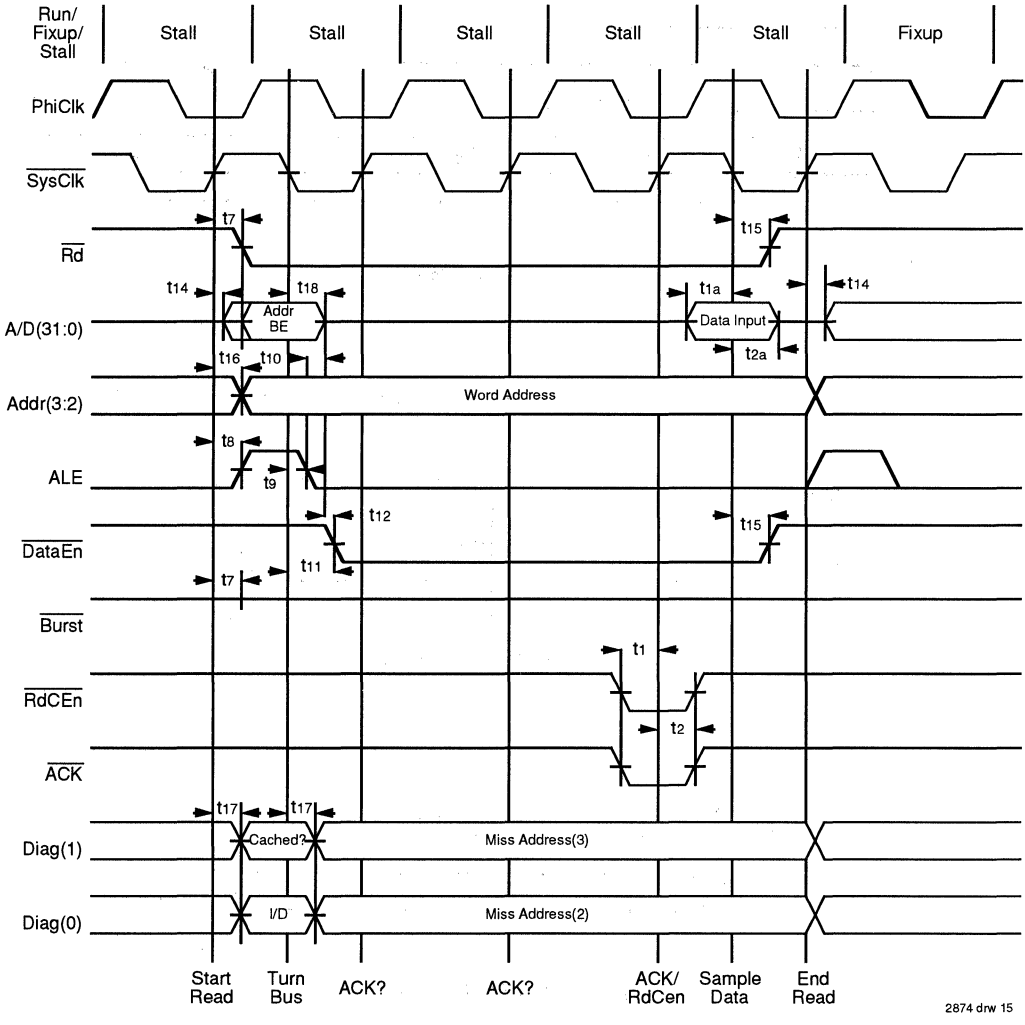


Figure 12. Single Datum Read in R3051 Family

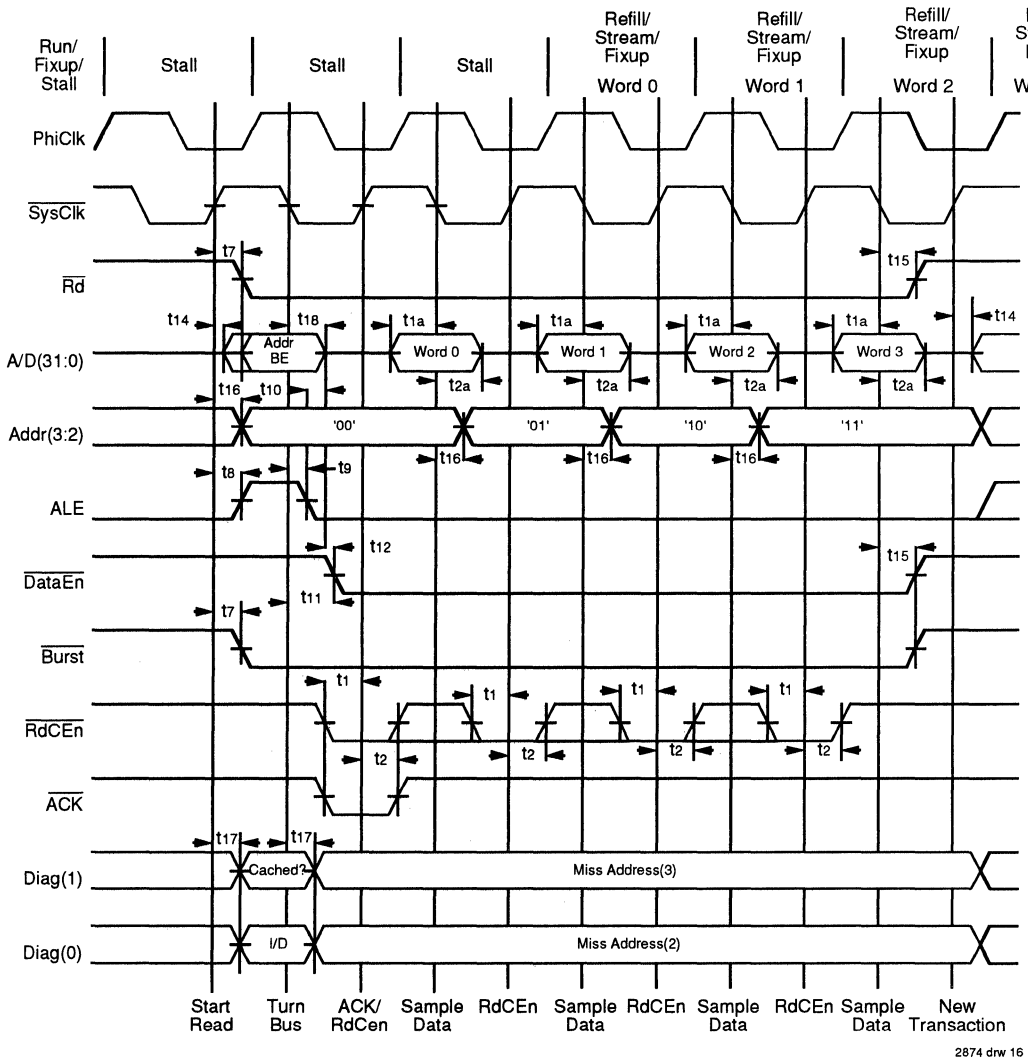


Figure 13. R3051 Family Burst Read

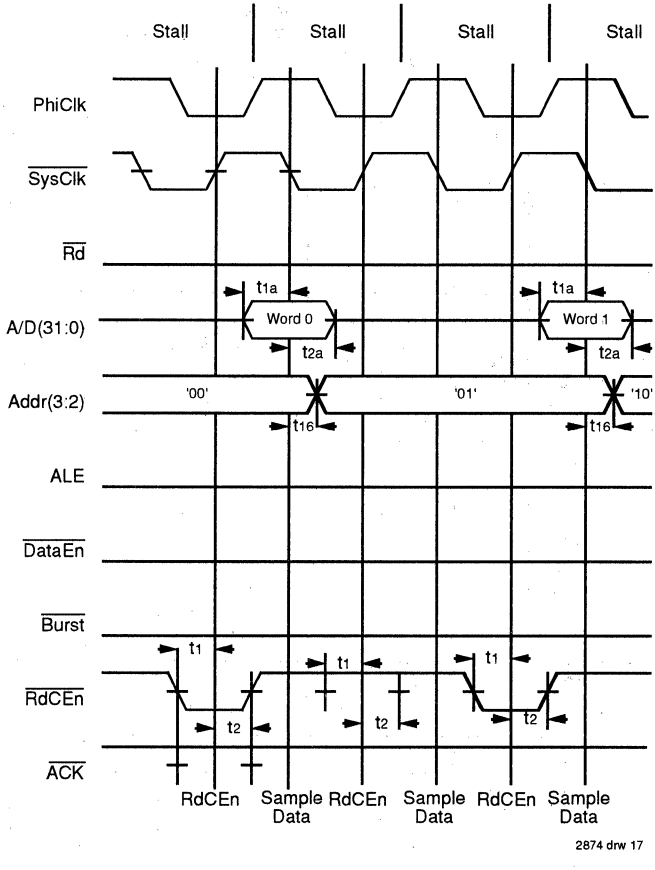


Figure 14 (a). Start of Throttled Quad Read

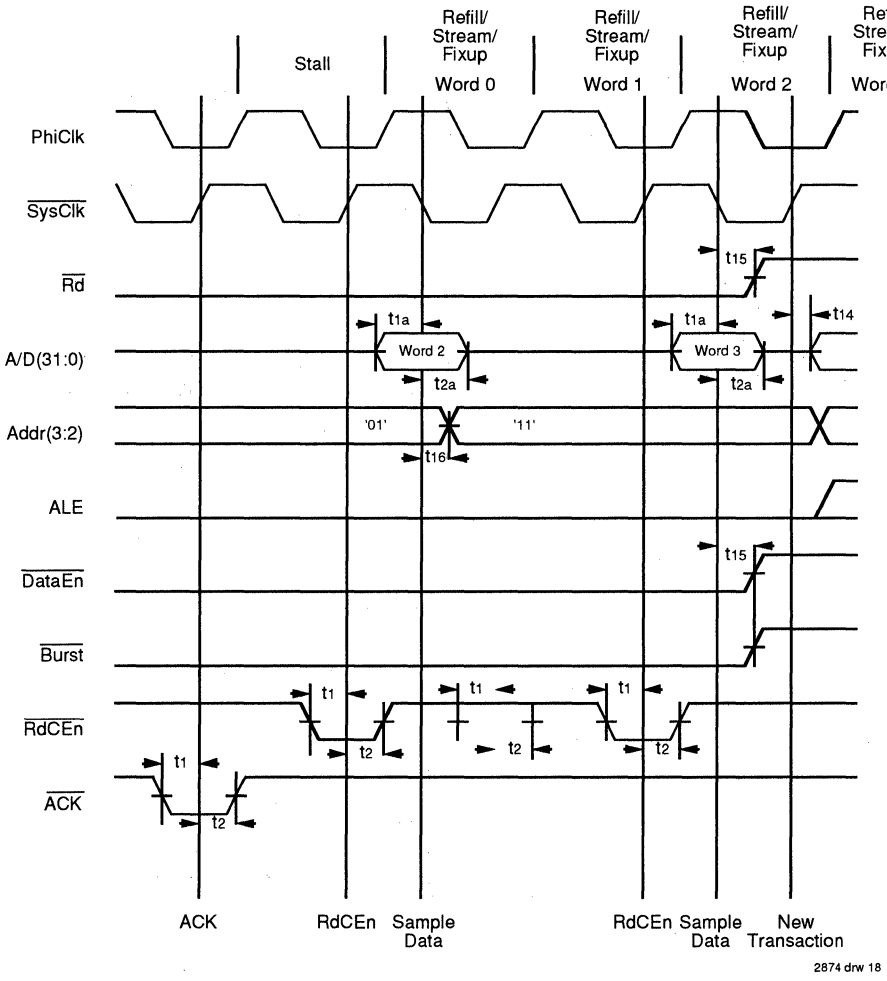


Figure 14 (b). End of Throttled Quad Read

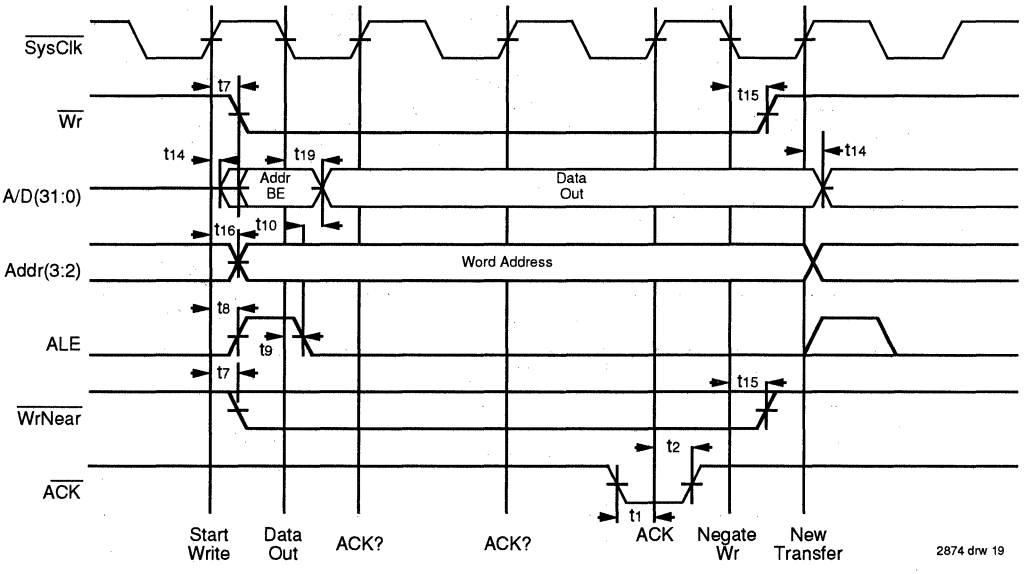


Figure 15. R3051 Family Write Cycle

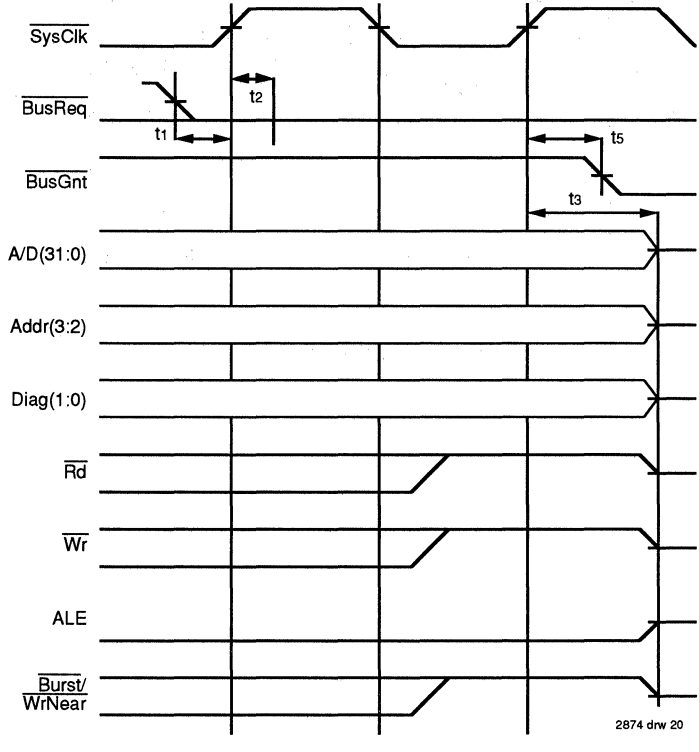


Figure 16. Request and Relinquish of R3051 Family Bus to External Master

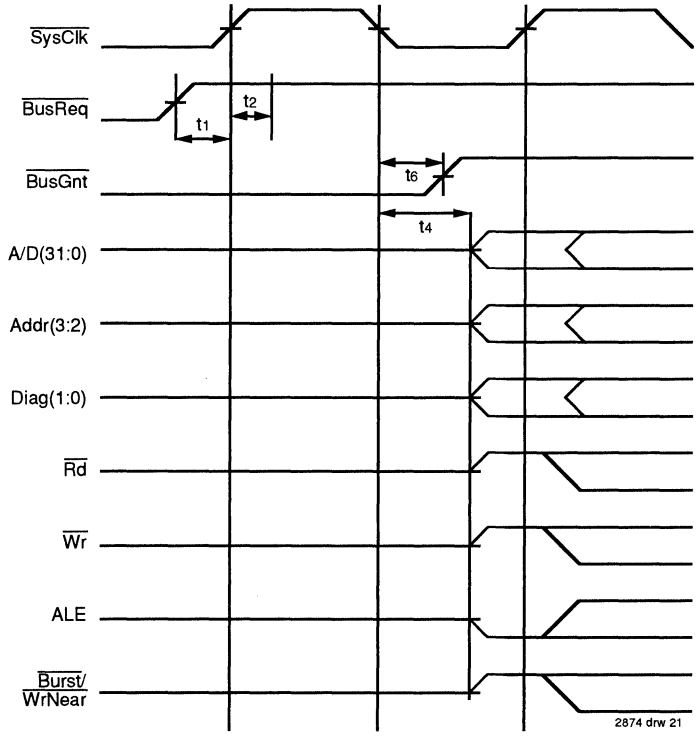


Figure 17. R3051 Family Regaining Bus Mastership

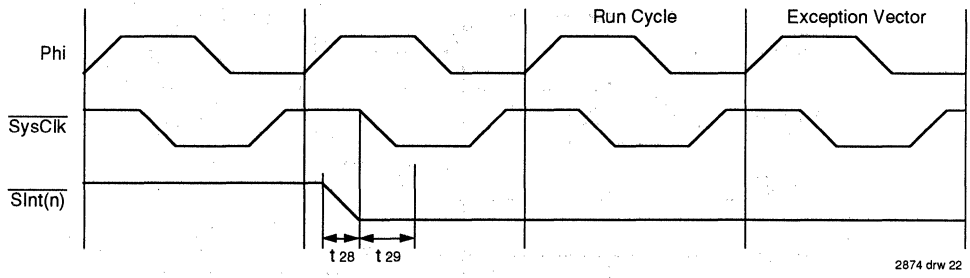


Figure 18. Synchronized Interrupt Input Timing

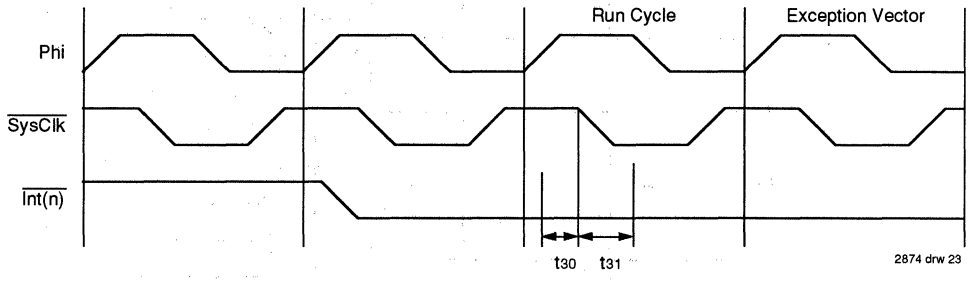


Figure 19. Direct Interrupt Input Timing

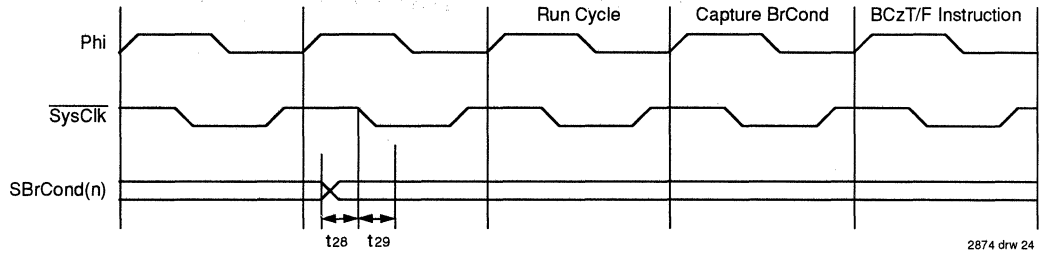


Figure 20. Synchronized Branch Condition Input Timing

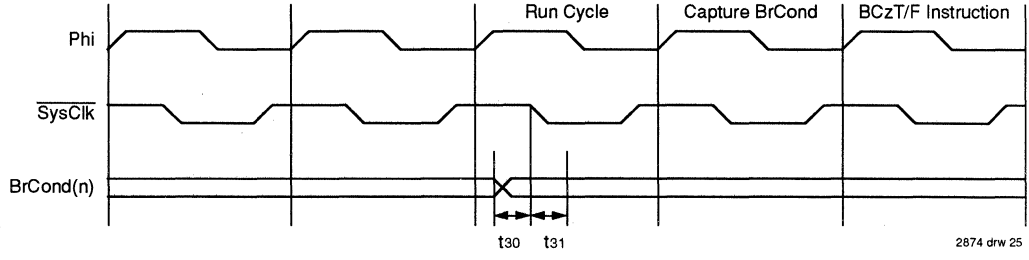
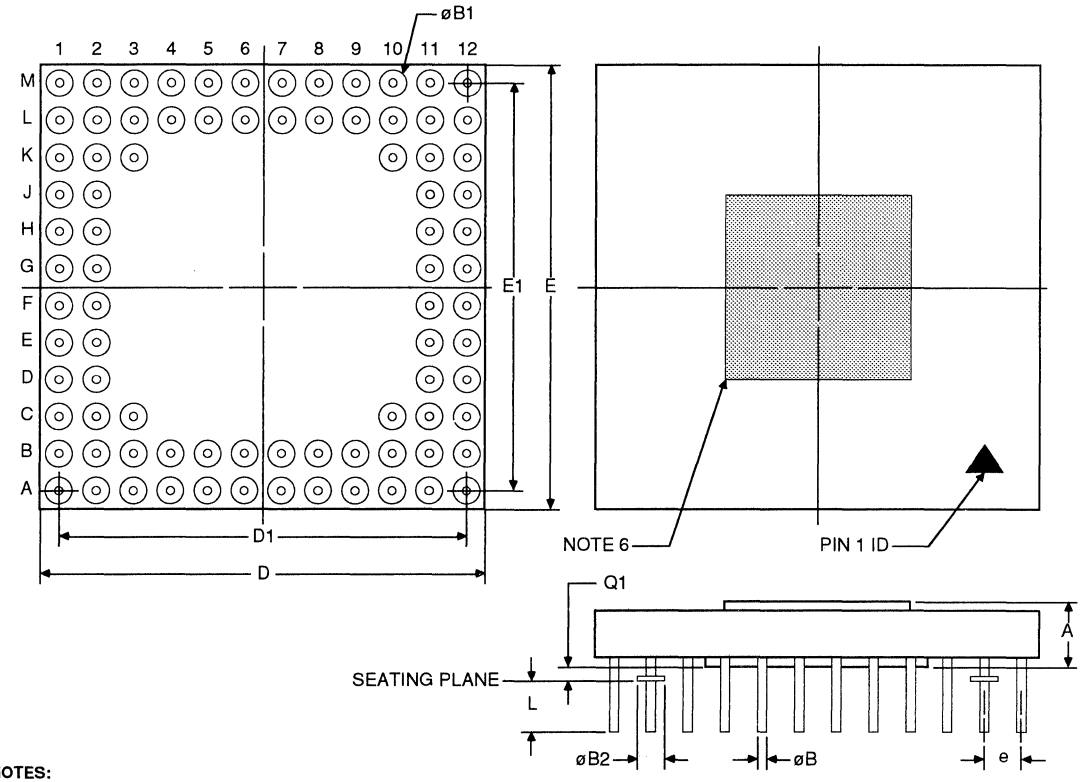


Figure 21. Direct Branch Condition Input Timing

84-PIN PGA (CAVITY DOWN)



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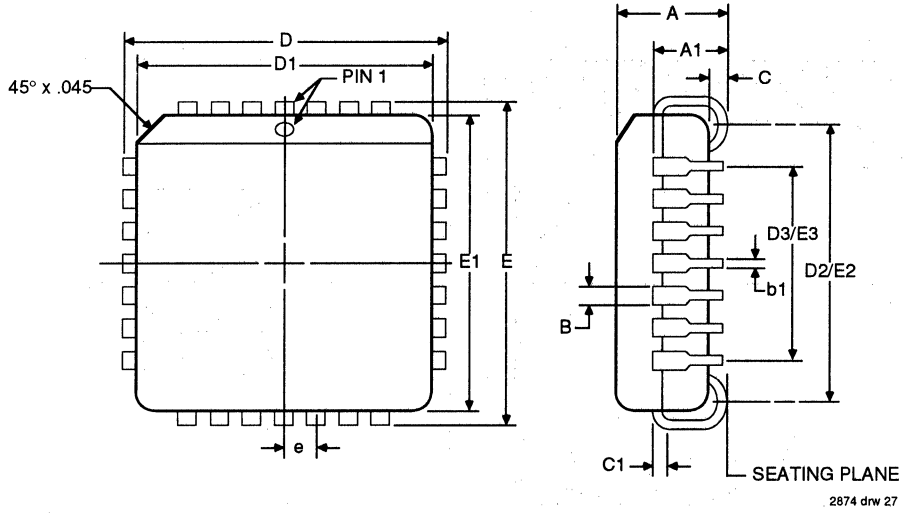
NOTES:
1. All dimensions are in inches, unless otherwise noted.
2. BSC—Basic lead Spacing between Centers
3. Symbol "M" represents the PGA matrix size.
4. Symbol "N" represents the number of pins.
5. Chamfered corners are IDT's option.
6. Shaded area indicates integral metallic heat sink.

Drawing #	G84-4	
Symbol	**Min**	**Max**
A	.077	.145
øB	.016	.020
øB1	.060	.080
øB2	.040	.060
D/E	1.180	1.235
D1/E1	1.100 BSC	
e	.100 BSC	
L	.120	.140
M	12	
N	84	
Q1	.025	.060

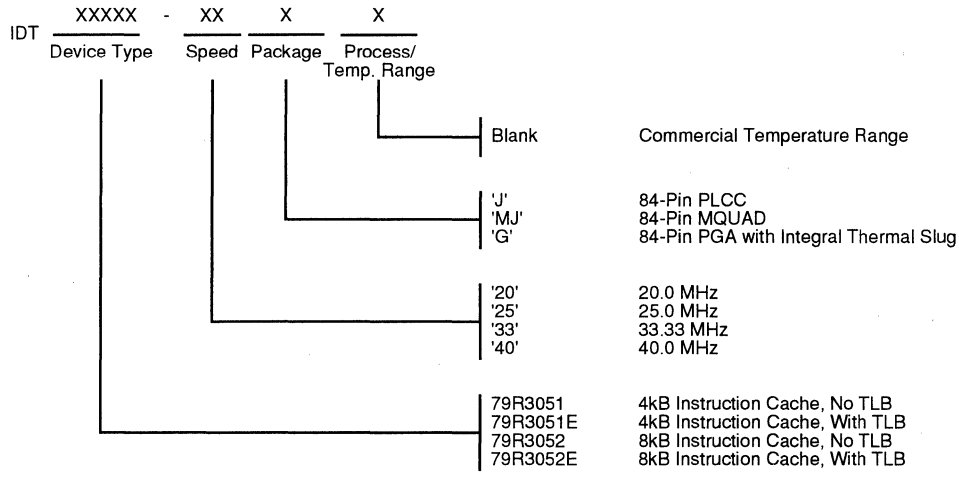
84 LEAD PLCC/MQUAD[7] (SQUARE)



NOTES:
1. All dimensions are in inches, unless otherwise noted.
2. BSC—Basic lead Spacing between Centers.
3. D & E do not include mold flash or protutions.
4. Formed leads shall be planar with respect to one another and within .004" at the seating plane.
5. ND & NE represent the number of leads in the D & E directions respectively.
6. D1 & E1 should be measured from the bottom of the package.
7. MQUAD is pin & form compatible with PLCC.

DWG #	J84-1		MJ84-1	
# of Leads	84		84	
Symbol	Min.	Max.	Min.	Max.
A	165	.180	165	.180
A1	.095	.115	.094	.114
B	.026	.032	.026	.032
b1	.013	.021	.013	.021
C	.020	.040	.020	.040
C1	.008	.012	.008	.012
D	1.185	1.195	1.185	1.195
D1	1.150	1.156	1.140	1.150
D2/E2	1.090	1.130	1.090	1.130
D3/E3	1.000 REF		1.000 REF	
E	1.185	1.195	1.185	1.195
E1	1.150	1.156	1.140	1.150
e	.050 BSC		.050 BSC	
ND/NE	21		21	

ORDERING INFORMATION



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VALID COMBINATIONS

IDT	79R3051 - 20, 25	All packages
	79R3051E - 20, 25	All packages
	79R3052 - 20, 25	All packages
	79R3052E - 20, 25	All packages
	79R3051 - 33, 40	PGA, MJ Packages Only
	79R3051E - 33, 40	PGA, MJ Packages Only
	79R3052 - 33, 40	PGA, MJ Packages Only
	79R3052E - 33, 40	PGA, MJ Packages Only

Integrated Device Technology, Inc.

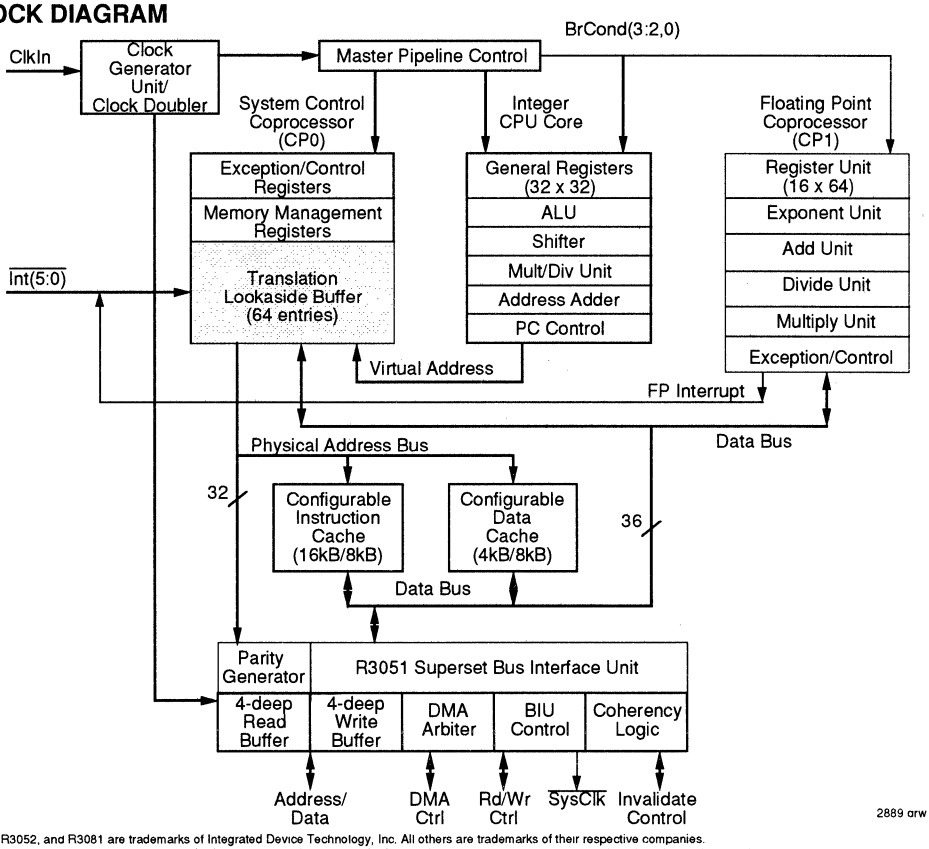
IDT79R3081 RISController™

IDT 79R3081™, 79R3081E IDT 79R3081L, 79R3081LE

FEATURES

- Instruction set compatible with IDT79R3000A, R3051, and R3500 RISC CPUs
- High level of integration minimizes system cost
  - — R3000A Compatible CPU
  - — R3010A Compatible Floating Point Accelerator
  - — Optional R3000A compatible MMU
  - — Large Instruction Cache
  - — Large Data Cache
  - — Read/Write Buffers
- 35 VUPS at 40MHz
  - — 64,000 Dhrystones
  - — 11 MFlops
- Flexible bus interface allows simple, low cost designs
- Optional 1x or 2x clock input
- 20 through 40MHz operation
- "L" version operates at 3.3V
- Large on-chip caches with user configurability
  - — 16kB Instruction Cache, 4kB Data Cache
  - — Dynamically configurable to 8kB Instruction Cache, 8kB Data Cache
  - — Parity protection over data and tag fields
- Low cost 84-pin packaging
- Superset pin- and software-compatible with R3051
- Multiplexed bus interface with support for low-cost, low-speed memory systems with a high-speed CPU
- On-chip 4-deep write buffer eliminates memory write stalls
- On-chip 4-deep read buffer supports burst or simple block reads
- On-chip DMA arbiter
- Hardware-based Cache Coherency Support
- Programmable power reduction mode
- Bus Interface can operate at half-processor frequency

R3081 BLOCK DIAGRAM



INTRODUCTION

The IDT R3051 family is a series of high-performance 32-bit microprocessors featuring a high-level of integration, and targeted to high-performance but cost sensitive processing applications. The R3051 family is designed to bring the high-performance inherent in the MIPS RISC architecture into low-cost, simplified, power sensitive applications.

Thus, functional units have been integrated onto the CPU core in order to reduce the total system cost, rather than to increase the inherent performance of the integer engine. Nevertheless, the R3051 family is able to offer 35 VUPS performance at 40MHz without requiring external SRAM or caches.

The R3081 extends the capabilities of the R3051 family, by integrating additional resources into the same pin-out. The R3081 thus extends the range of applications addressed by the R3051 family, and allows designers to implement a single, base system and software set capable of accepting a wide variety of CPUs, according to the price/performance goals of the end system.

In addition to the embedded applications served by the R3051 family, the R3081 allows low-cost, entry level computer systems to be constructed. These systems will offer many times the performance of traditional PC systems, yet cost approximately the same. The R3081 is able to run any standard R3000A operation system, including ACE UNIX. Thus, the R3081 can be used to build a low-cost ARC compliant system, further widening the range of performance solutions of the ACE Initiative.

An overview of this device, and quantitative electrical parameters and mechanical data, is found in this data sheet; consult the *"R3081 Family Hardware User's Guide"* for a complete description of this processor.

DEVICE OVERVIEW

As part of the R3051 family, the R3081 extends the offering of a wide range of functionality in a compatible interface. The R3051 family allows the system designer to implement a single base system, and utilize interface-compatible processors of various complexity to achieve the price-performance goals of the particular end system.

Differences among the various family members pertain to the on-chip resources of the processor. Current family members include:

- The R3052E, which incorporates an 8kB instruction cache, a 2kB data cache, and full function memory management unit (MMU) including 64-entry fully associative Translation Lookaside Buffer (TLB).
- The R3052, which also incorporates an 8kB instruction cache and 2kB data cache, but does not include the TLB, and instead uses a simpler virtual to physical address mapping.
- The R3051E, which incorporates 4kB of instruction cache and 2kB of data cache, along with the full function MMU/TLB of the R3000A.
- The R3051, which incorporates 4kB of instruction cache and 2kB of data cache, but omits the TLB, and instead uses a simpler virtual to physical address mapping.
- The R3081E, which incorporates a 16kB instruction cache, a 4kB data cache, and full function memory management unit (MMU) including 64-entry fully associative Translation Lookaside Buffer (TLB). The cache on the R3081E is user configurable to an 8kB Instruction Cache and 8kB Data Cache.
- The R3081, which incorporates a 16kB instruction cache, a 4kB data cache, but uses the simpler memory mapping of the R3051/52, and thus omits the TLB. The cache on the R3081 is user configurable to an 8kB Instruction Cache and 8kB Data Cache.

Figure 1 shows a block level representation of the functional units within the R3081E. The R3081E could be viewed as the embodiment of a discrete solution built around the R3000A and R3010A. However, by integrating this functionality on a single chip, dramatic cost and power reductions are achieved.

CPU Core

The CPU core is a full 32-bit RISC integer execution engine, capable of sustaining close to single cycle execution. The CPU core contains a five stage pipeline, and 32 orthogonal 32-bit registers. The R3081 uses the same basic integer execution core as the entire R3051 family, which is the R3000A implementation of the MIPS instruction set. Thus, the R3081 family is binary compatible with the R3051, R3052, R3000A, R3001, and R3500 CPUs. In addition, the R4000 represents an upwardly software compatible migration path to still higher levels of performance.

The execution engine in the R3081 uses a five-stage pipeline to achieve near single-cycle instruction execution rates. A new instruction can be initiated in each clock cycle; the execution engine actually processes five instructions concurrently (in various pipeline stages). Figure 2 shows the concurrency achieved in the R3081 execution pipeline.

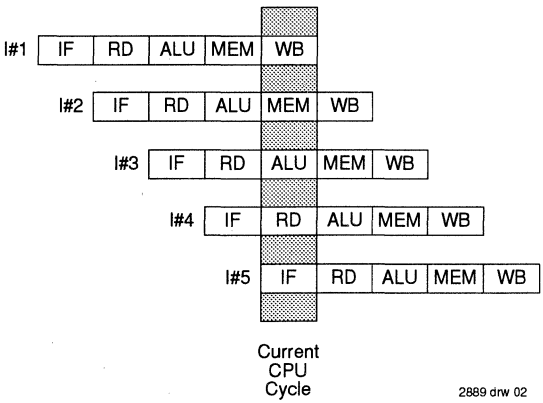


Figure 2. R3081 5-Stage Pipeline

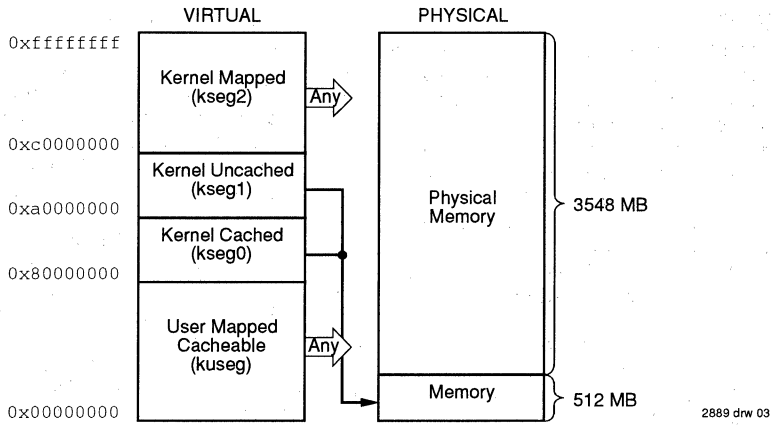


Figure 3. Virtual to Physical Mapping of Extended Architecture Versions

System Control Co-Processor

The R3081 family also integrates on-chip the System Control Co-processor, CP0. CP0 manages both the exception handling capability of the R3081, as well as the virtual to physical address mapping.

As with the R3051 and R3052, the R3081 offers two versions of memory management and virtual to physical address mapping: the extended architecture versions, the R3051E, R3052E, and R3081E, incorporate the same MMU as the R3000A. These versions contain a fully associative 64-entry TLB which maps 4kB virtual pages into the physical address space. The virtual to physical mapping thus includes kernel segments which are hard-mapped to physical addresses, and kernel and user segments which are mapped page by page by the TLB into anywhere in the 4GB physical address space. In this TLB, 8 pages can be "locked" by the kernel to insure deterministic response in real-time applications. Figure 3 illustrates the virtual to physical mapping found in the R3081E.

The Extended architecture versions of the R3051 family (the R3051E, R3052E, and R3081E) allow the system designer to implement kernel software which dynamically manages User task utilization of system resources, and also allows the Kernel to protect certain resources from User tasks. These capabilities are important in general computing applications such as ARC computers, and are also important in a variety of embedded applications, from process control (where protection may be important) to X-Window display systems (where virtual memory management can be used). The MMU can also be used to simplify system debug.

R3051 family base versions (the R3051, R3052, and R3081) remove the TLB and institute a fixed address mapping for the various segments of the virtual address space. These devices still support distinct kernel and user mode operation, but do not require page management software, leading to a simpler software model. The memory mapping used by these devices is shown in Figure 4. Note that the reserved spaces are for compatiblity with future family members, which may

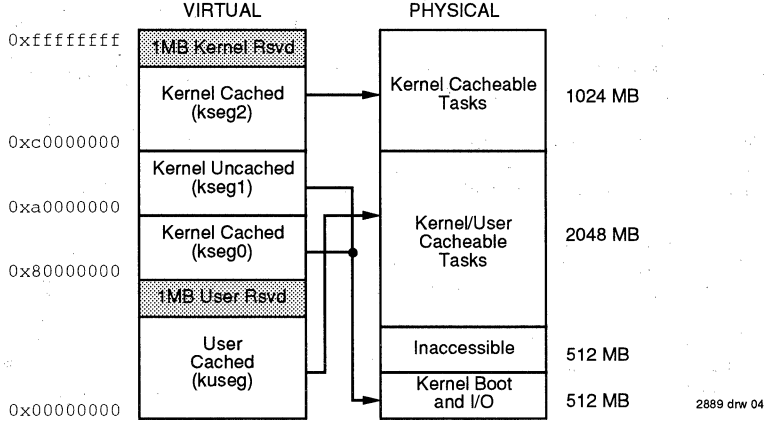


Figure 4. Virtual to Physical Mapping of Base Architecture Versions

map on-chip resources to these addresses. References to these addresses in the R3081 will be translated in the same fashion as the rest of their respective segments, with no traps or exceptions signalled.

When using the base versions of the architecture, the system designer can implement a distinction between the user tasks and the kernel tasks, without having to implement page management software. This distinction can be implemented by decoding the output physical address. In systems which do not need memory protection, and wish to have the kernel and user tasks operate out of the same memory space, high-order address lines can be ignored by the address decoder, and thus all references will be seen in the lower gigabyte of the physical address space.

Floating Point Co-Processor

The R3081 also integrates an R3010A compatible floating point accelerator on-chip. The FPA is a high performance co-processor (co-processor 1 to the CPU) providing separate add, multiply, and divide functional units for single and double precision floating point arithmetic. The floating point accelerator features low latency operations, and autonomous functional units which allow differing types of floating point operations to function concurrently with integer operations. The R3010A appears to the software programmer as a simple extension of the integer execution unit, with 16 dedicated 64-bit floating point registers (software references these as 32 32-bit registers when performing loads or stores). Figure 5 illustrates the functional block diagram of the on-chip FPA.

Clock Generator Unit

The R3081 is driven from a single input clock which can be either at the processor rated speed, or at twice that speed. On-chip, the clock generator unit is responsible for managing the interaction of the CPU core, caches, and bus interface. The R3081 includes an on-chip clock doubler to provide higher frequency signals to the internal execution core; if 1x clock mode is selected, the clock doubler will internally convert it to a double frequency clock. The 2x clock mode is provided for compatiblity with the R3051. The clock generator unit replaces the external delay line required in R3000A based applications.

Instruction Cache

The R3081 implements a 16kB Instruction Cache. The system may choose to repartition the on-chip caches, so that the instruction cache is reduced to 8kB but the data cache is increased to 8kB. The instruction cache is organized with a line size of 16 bytes (four entries). This large cache achieves hit rates in excess of 98% in most applications, and substantially contributes to the performance inherent in the R3081. The cache is implemented as a direct mapped cache, and is capable of caching instructions from anywhere within the 4GB physical address space. The cache is implemented using physical addresses (rather than virtual addresses), and thus does not require flushing on context switch.

The instruction cache is parity protected over the instruction word and tag fields. Parity is generated by the read buffer during cache refill; during cache references, the parity is checked, and in the case of a parity error, a cache miss is processed.

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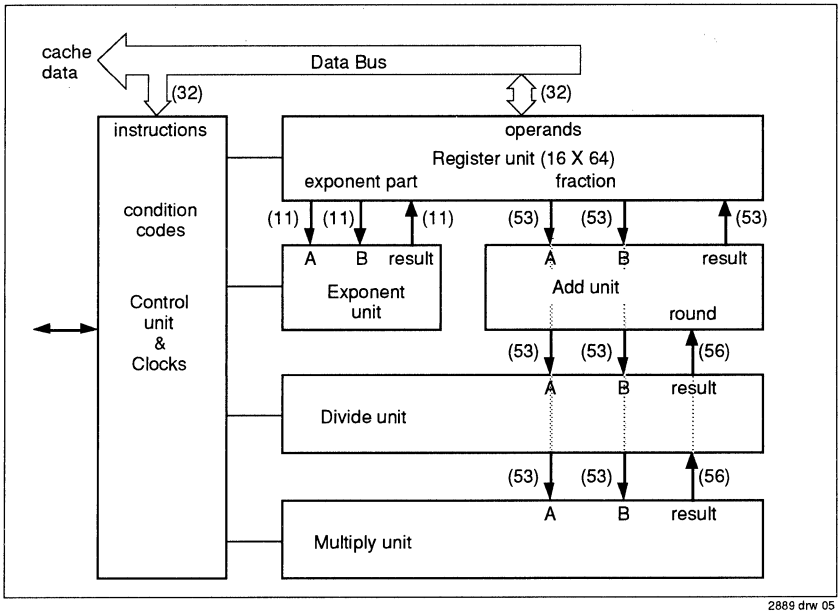

Figure 5. FPA Functional Block Diagram

Data Cache

The R3081 incorporates an on-chip data cache of 4kB, organized as a line size of 4 bytes (one word). The R3081 allows the system to reconfigure the on-chip cache from the default 16kB I-Cache/4kB D-Cache to 8kB of Instruction and 8kB of Data caches.

The relatively large data cache achieves hit rates in excess of 95% in most applications, and contributes substantially to the performance inherent in the R3081. As with the instruction cache, the data cache is implemented as a direct mapped physical address cache. The cache is capable of mapping any word within the 4GB physical address space.

The data cache is implemented as a write-through cache, to insure that main memory is always consistent with the internal cache. In order to minimize processor stalls due to data write operations, the bus interface unit incorporates a 4-deep write buffer which captures address and data at the processor execution rate, allowing it to be retired to main memory at a much slower rate without impacting system performance. Further, support has been provided to allow hardware based data cache coherency in a multi-master environment, such as one utilizing DMA from I/O to memory.

The data cache is parity protected over the data and tag fields. Parity is generated by the read buffer during cache refill; during cache references, the parity is checked, and in the case of a parity error, a cache miss is processed.

Bus Interface Unit

The R3081 uses its large internal caches to provide the majority of the bandwidth requirements of the execution engine, and thus can utilize a simple bus interface connected to slower memory devices. Alternately, a high-performance, low cost secondary cache can be implemented, allowing the processor to increase performance in systems where bus bandwidth is a performance limitation.

As part of the R3051 family, the R3081 bus interface utilizes a 32-bit address and data bus multiplexed onto a single set of pins. The bus interface unit also provides an ALE (Address Latch Enable) output signal to de-multiplex the A/D bus, and simple handshake signals to process CPU read and write requests. In addition to the read and write interface, the R3051 family incorporates a DMA arbiter, to allow an external master to control the external bus.

The R3081 also supports hardware based cache coherency during DMA writes. The R3081 can invalidate a specified line of data cache, or in fact can perform burst invalidations during burst DMA writes.

The R3081 incorporates a 4-deep write buffer to decouple the speed of the execution engine from the speed of the memory system. The write buffers capture and FIFO processor address and data information in store operations, and present it to the bus interface as write transactions at the rate the memory system can accommodate.

The R3081 read interface performs both single datum reads and quad word reads. Single reads work with a simple handshake, and quad word reads can either utilize the simple handshake (in lower performance, simple systems) or utilize a tighter timing mode when the memory system can burst data at the processor clock rate. Thus, the system designer can choose to utilize page or nibble mode DRAMs (and possibly use interleaving, if desired, in high-performance systems), or use simpler techniques to reduce complexity.

In order to accommodate slower quad word reads, the R3081 incorporates a 4-deep read buffer FIFO, so that the external interface can queue up data within the processor before releasing it to perform a burst fill of the internal caches.

The R3081 is R3051 superset compatible in its bus interface. Specifically, the R3081 has additional support to simplify the design of very high frequency systems. This support includes the ability to run the bus interface at one-half the processor execution rate, as well as the ability to slow the transitions between reads and writes to provide extra buffer disable time for the memory interface. However, it is still possible to design a system which, with no modification to the PC Board or software, can accept either an R3051, R3052, or R3081.

SYSTEM USAGE

The IDT R3051 family has been specifically designed to allow a wide variety of memory systems. Low-cost systems can use slow speed memories and simple controllers, while other designers may choose to incorporate higher frequencies, faster memories, and techniques such as DMA to achieve maximum performance. The R3081 includes specific support for high perfromance systems, including signals necessary to implement external secondary caches, and the ability to perform hardware based cache coherency in multi-master systems.

Figure 6 shows a typical system implementation. Transparent latches are used to de-multiplex the R3081 address and data busses from the A/D bus. The data paths between the memory system elements and the A/D bus is managed by simple octal devices. A small set of simple PALs is used to control the various data path elements, and to control the handshake between the memory devices and the CPU. IDT has implemented the R3720/21 support chip set specifically tailored to R3051 family systems. This chip set directly interfaces the processor to DRAM, simplifying design and eliminating discrete logic chips and PAL devices.

Depending on the cost vs. performance tradeoffs appropriate to a given application, the system design engineer could include true burst support from the DRAM to provide for high-performance cache miss processing, or utilize a simpler, lower performance memory system to reduce cost and simplify the design. Similarly, the system designer could choose to implement techniques such as external secondary cache, or DMA, to further improve system performance.

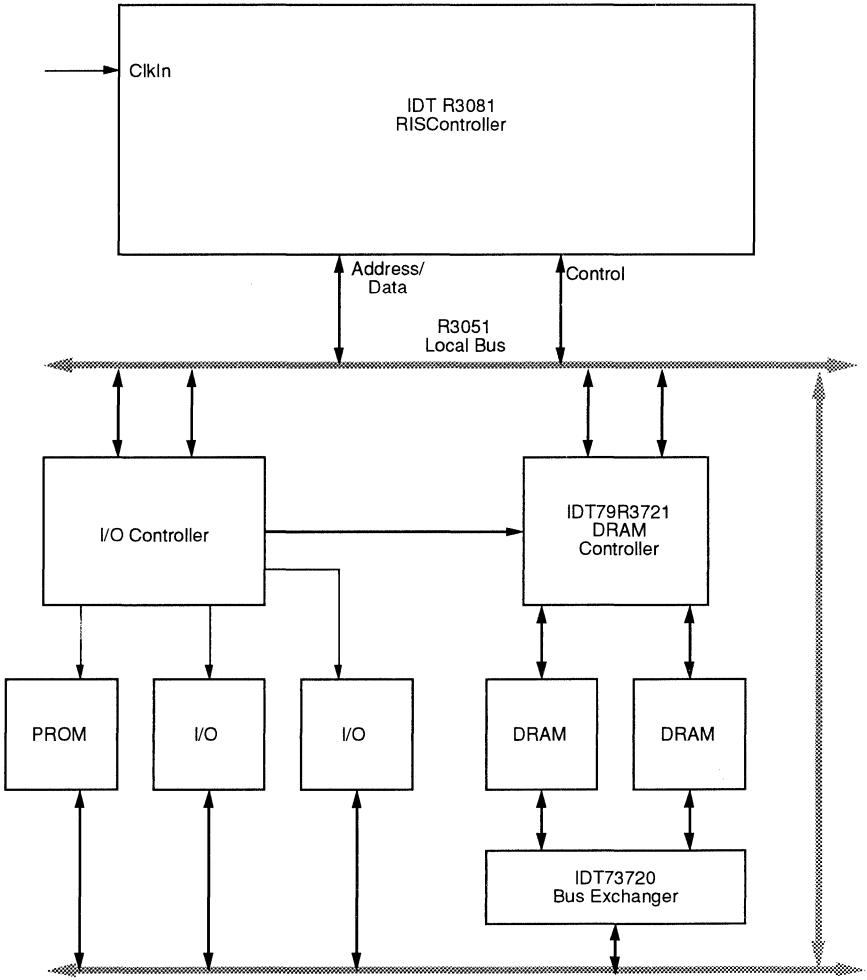

Figure 6. R3081 RISChipset Based System

2889 drw 06

DEVELOPMENT SUPPORT

The IDT R3051 family is supported by a rich set of development tools, ranging from system simulation tools through PROM monitor and debug support, applications software and utility libraries, logic analysis tools, sub-system modules, and shrink wrap operating systems. The R3081, which is pin and software compatible with the R3051, can directly utilize these existing tools to reduce time to market.

Figure 7 is an overview of the system development process typically used when developing R3051 family applications. The R3051 family is supported in all phases of project development. These tools allow timely, parallel development of hardware and software for R3051 family applications, and include tools such as:

- A program, Cache-R3051, which allows the performance of an R3051 family system to be modeled and understood without requiring actual hardware.
- Sable, an instruction set simulator.
- Optimizing compilers from MIPS, the acknowledged leader in optimizing compiler technology.
- Cross development tools, available in a variety of development environments.
- The high-performance IDT floating point library software, including transcendental functions and IEEE compliant exception handlers.
- The IDT Evaluation Board, which includes RAM, EPROM, I/O, and the IDT PROM Monitor.
- The IDT Laser Printer System board, which directly drives a low-cost print engine, and runs Microsoft TrueImage™ Page Description Language on top of PeerlessPage™ Advanced Printer Controller BIOS.
- Adobe PostScript™ Page Description Language, ported to the R3000 instruction set, runs on the IDT R3051 family.
- IDT/sim, which implements a full prom monitor (diagnostics, remote debug support, peek/poke, etc.).
- IDT/sae, which implements a run-time support package for R3051 family systems.
- ACE UNIX operating system; bringing ACE compatibility.

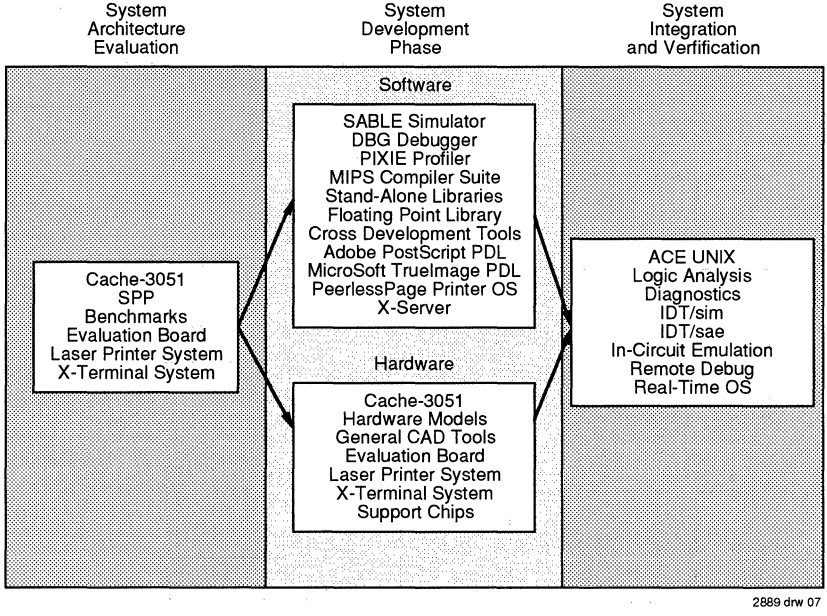

Figure 7. R3051 Family Development Toolchain

PERFORMANCE OVERVIEW

The R3081 achieves a very high-level of performance. This performance is based on:

- An efficient execution engine. The CPU performs ALU operations and store operations in a single cycle, and has an effective load time of 1.3 cycles, and branch execution rate of 1.5 cycles (based on the ability of the compilers to avoid software interlocks). Thus, the execution engine achieves over 35 VUPS performance when operating out of cache.
- A full featured floating point accelerator/co-processor. The R3081 incorporates an R3010A compatible floating point accelerator on-chip, with independent ALUs for floating point add, multiply, and divide. The floating point unit is fully hardware interlocked, and features overlapped operation and precise exceptions. The FPA allows floating point adds, multiplies, and divides to occur concurrently with each other, as well as concurrently with integer operations.
- Large on-chip caches. The R3051 family contains caches which are substantially larger than those on the majority of today's microprocessors. These large caches minimize the number of bus transactions required, and allow the R3051 family to achieve actual sustained performance very close to its peak execution rate. The R3081 doubles the cache available on the R3052, making it a suitable enging for many general purpose computing applications, such as ARC compliant systems.
- Autonomous multiply and divide operations. The R3051 family features an on-chip integer multiplier/divide unit which is separate from the other ALU. This allows the CPU to perform multiply or divide operations in parallel with other integer operations, using a single multiply or divide instruction rather than "step" operations.
- Integrated write buffer. The R3081 features a four deep write buffer, which captures store target addresses and data at the processor execution rate and retires it to main memory at the slower main memory access rate. Use of on-chip write buffers eliminates the need for the processor to stall when performing store operations.
- Burst read support. The R3051 family enables the system designer to utilize page mode or nibble mode RAMs when performing read operations to minimize the main memory read penalty and increase the effective cache hit rates.

These techniques combine to allow the processor to achieve over 35 VUPS integer performance, 11MFlops of Linpack performance, and 64,000 dhrystones without the use of external caches or zero wait-state memory devices.

The performance differences between the various family members depends on the application software and the design of the memory system. The impact of the various cache sizes, and the hardware floating point, can be accurately modeled using Cache-3051. Since the R3051, R3052, and R3081 are all pin and software compatible, the system designer has maximum freedom in trading between performance and cost. A system can be designed, and later the appropriate CPU inserted into the board, depending on the desired system performance.

SELECTABLE FEATURES

The R3081 allows the system designer to configure certain aspects of operation. Some of these options are established when the device is reset, while others are enabled via the Config registers:

- BigEndian vs. LittleEndian Byte Ordering. The part can be configured to operate with either byte ordering. ACE/ARC systems typically use Little Endian byte ordering. However, various embedded applications, written originally for a Big Endian processor such as the MC680x0, are easier to port to a Big Endian system.
- Data Cache Refill of one or four words. The memory system must be capable of performing four word refills of instruction cache misses. The R3081 allows the system designer to enable D-Cache refill of one or four words dynamically. Thus, specialized algorithms can choose one refill size, while the rest of the system can operate with the other.
- Half-frequency bus mode. The processor can be configured such that the external bus interface is at one-half the frequency of the processor core. This simplifies system design; however, the large on-chip caches mitigate the performance impact of using a slower system bus clock.
- Slow bus turn-around. The R3081 allows the system designer to space processor operations, so that more time is allowed for transitions between memory and the processor on the multiplexed address/data bus.
- Configurable cache. The R3081 allows the system designer to use software to select either a 16kB Instruction Cache/ 4kB Data Cache organization, or an 8kB Instruction/8kB Data Cache organization.
- Cache Coherent Interface. The R3081 has an optional hardware based cache coherency interface intended to support multi-master systems such as those utilizing DMA between memory and I/O.
- Optional 1x or 2x clock input. The R3081 can be driven with an R3051 compatible 2x clock input, or a lower frequency 1x clock input.

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THERMAL CONSIDERATIONS

The R3081 utilizes special packaging techniques to improve the thermal properties of high-speed processors. Thus, the R3081 is packaged using cavity down packaging, with an embedded thermal slug to improve thermal transfer to the suurrounding air.

The R3081 utilizes the 84-pin MQUAD package (the "MJ" package), which is an all aluminum package with the die attached to a normal copper lead-frame mounted to the aluminum casing. The MQUAD package allows for an efficient thermal transfer between the die and the case due to the heat spreading effect of the aluminum. The aluminum offers less internal resistance from one end of the package to the other, reducing the temperature gradient across the package and therefore presenting a greater area for convection and conduction to the PCB for a given temperature. Even nominal amounts of airflow will dramatically reduce the junction temperature of the die, resulting in cooler operation. The MQUAD package is available at all frequencies, and is pin and form compatible with the PLCC used for the R3051. Thus, designers can inter-change R3081's and R3051's in a particular design, without changing their PC Board.

Finally, the R3081 is also available in a cavity-down PGA with exposed thermal slug. As with the MQUAD package, this package is extremely thermal efficient, and is appropriate in extreme temperature conditions, such as military systems.

The R3081 is guaranteed in a case temperature range of 0°C to +85°C. The type of package, speed (power) of the device, and airflow conditions, affect the equivalent ambient temperature conditions which will meet this specification.

The equivalent allowable ambient temperature, T_A, can be calculated using the thermal resistance from case to ambient ($Ø_{CA}$) of the given package. The following equation relates ambient and case temperatures:

$$T_A = T_C - P * Ø_{CA}$$

where P is the maximum power consumption at hot temperature, calculated by using the maximum Icc specification for the device.

Typical values for $Ø_{CA}$ at various airflows are shown in Table 1.

Note that the R3081 allows the operational frequency to be turned down during idle periods to reduce power consumption. This operation is described in the *R3081 Hardware User's Guide*. Reducing the operation frequency dramatically reduces power consumption.

	ØCA					
Airflow (ft/min)	**0**	**200**	**400**	**600**	**800**	**1000**
"MJ" Package*	22	14	12	11	9	8
PGA Package	29	15	9	7	6	5

2889 tbl 01

Table 1. Thermal Resistance ($Ø_{CA}$) at Various Airflows (*estimated: final values tbd)

PIN DESCRIPTION

PIN NAME	I/O	DESCRIPTION
A/D(31:0)	I/O	**Address/Data:** A 32-bit time multiplexed bus which indicates the desired address for a bus transaction in one phase, and which is used to transmit data between the CPU and external memory resources during the rest of the transfer. Bus transactions on this bus are logically separated into two phases: during the first phase, information about the transfer is presented to the memory system to be captured using the ALE output. This information consists of: **Address(31:4)**: The high-order address for the transfer is presented on A/D(31:4). **$\overline{BE}$(3:0)**: These strobes indicate which bytes of the 32-bit bus will be involved in the transfer, and are presented on A/D(3:0). During write cycles, the bus contains the data to be stored and is driven from the internal write buffer. On read cycles, the bus receives the data from the external resource, in either a single data transaction or in a burst of four words, and places it into the on-chip read buffer. During cache coherency operations, the R3081 monitors the A/D bus at the start of a DMA write to capture the write target address for potential data cache invalidates.
Addr(3:2)	O	**Low Address (3:2)** A 2-bit bus which indicates which word is currently expected by the processor. Specifically, this two bit bus presents either the address bits for the single word to be transferred (writes or single datum reads) or functions as a two bit counter starting at '00' for burst read operations. During cache coherency operations, the R3081 monitors the Addr bus at the start of a DMA write to capture the write target address for potential data cache invalidates.
Diag(1)	O	**Diagnostic Pin 1.** This output indicates whether the current bus read transaction is due to an on-chip cache miss, and also presents part of the miss address. The value output on this pin is time multiplexed: **Cached:** During the phase in which the A/D bus presents address information, this pin is an active high output which indicates whether the current read is a result of a cache miss. **Miss Address (3):** During the remainder of the read operation, this output presents address bit (3) of the address the processor was attempting to reference when the cache miss occurred. Regardless of whether a cache miss is being processed, this pin reports the transfer address during this time. On write cycles, this output signals whether the data being written as retained in the on-chip data cache. The value of this pin is time multiplexed during writes: **Cached:** During the address phase of write transactions, this signal is an active high output which indicates that the store data was retained in the on-chip data cache. **Reserved:** The value of this pin during the data phase of writes is reserved.
Diag(0)	O	**Diagnostic Pin 0.** This output distinguishes cache misses due to instruction references from those due to data references, and presents the remaining bit of the miss address. The value output on this pin is also time multiplexed: **I/$\overline{D}$:** If the "Cached" Pin indicates a cache miss, then a high on this pin at this time indicates an instruction reference, and a low indicates a data reference. If the read is not due to a cache miss but rather an uncached reference, then this pin is undefined during this phase. **Miss Address (2):** During the remainder of the read operation, this output presents address bit (2) of the address the processor was attempting to reference when the cache miss occurred. Regardless of whether a cache miss is being processed, this pin reports the transfer address during this time. During write cycles, the value of this pin during both the address and data phases is reserved.

2889 tbl 02

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PIN DESCRIPTION (Continued):

PIN NAME	I/O	DESCRIPTION
ALE	I/O	**Address Latch Enable:** Used to indicate that the A/D bus contains valid address information for the bus transaction. This signal is used by external logic to capture the address for the transfer, typically using transparent latches. During cache coherency operations, the R3081 monitors ALE at the start of a DMA write, to capture the write target address for potential data cache invalidates.
$\overline{Rd}$	O	**Read:** An output which indicates that the current bus transaction is a read.
$\overline{Wr}$	I/O	**Write:** An output which indicates that the current bus transaction is a write. During coherent DMA, this input indicates that the current transfer is a write.
$\overline{DataEn}$	O	**External Data Enable:** This signal indicates that the A/D bus is no longer being driven by the processor during read cycles, and thus the external memory system may enable the drivers of the memory system onto this bus without having a bus conflict occur. During write cycles, or when no bus transaction is occurring, this signal is negated, thus disabling the external memory drivers
$\overline{Burst}$/ $\overline{WrNear}$	O	**Burst Transfer/Write Near:** On read transactions, the $\overline{Burst}$ signal indicates that the current bus read is requesting a block of four contiguous words from memory. This signal is asserted only in read cycles due to cache misses; it is asserted for all I-Cache miss read cycles, and for D-Cache miss read cycles if quad word refill is currently selected. On write transactions, the $\overline{WrNear}$ output tells the external memory system that the bus interface unit is performing back-to-back write transactions to an address within the same 512 word page as the prior write transaction. This signal is useful in memory systems which employ page mode or static column DRAMs, and allows near writes to be retired quickly.
$\overline{Ack}$	I	**Acknowledge:** An input which indicates to the device that the memory system has sufficiently processed the bus transaction, and that the CPU may either terminate the write cycle or process the read data from this read transfer. During Coherent DMA, this input indicates that the current write transfer is completed, and that the internal invalidation address counter should be incremented.
$\overline{RdCEn}$	I	**Read Buffer Clock Enable:** An input which indicates to the device that the memory system has placed valid data on the A/D bus, and that the processor may move the data into the on-chip Read Buffer.
$\overline{SysClk}$	O	**System Reference Clock:** An output from the CPU which reflects the timing of the internal processor "Sys" clock. This clock is used to control state transitions in the read buffer, write buffer, memory controller, and bus interface unit. This clock will either be at the same frequency as the CPU execution rate clock, or at one-half that frequency, as selected during reset.
$\overline{BusReq}$	I	**DMA Arbiter Bus Request:** An input to the device which requests that the CPU tri-state its bus interface signals so that they may be driven by an external master.
$\overline{BusGnt}$	O	**DMA Arbiter Bus Grant.** An output from the CPU used to acknowledge that a $\overline{BusReq}$ has been detected, and that the bus is relinquished to the external master.
$\overline{IvdReq}$	I	**Invalidate Request.** An input provided by an external DMA controller to request that the CPU invalidate the Data Cache line corresponding to the current DMA write target address. This signal is the same pin as Diag(0)
$\overline{CohReq}$	I	**Coherent DMA Request.** An input used by the external DMA controller to indicate that the requested DMA operations could involve hardware cache coherency. This signal is the Rsvd(0) of the R3051.
SBrCond(3:2) BrCond(0)	I	**Branch Condition Port:** These external signals are internally connected to the CPU signals CpCond(3:0). These signals can be used by the branch on co-processor condition instructions as input ports. There are two types of Branch Condition inputs: the SBrCond inputs have special internal logic to synchronize the inputs, and thus may be driven by asynchronous agents. The direct Branch Condition inputs must be driven synchronously. Note that BrCond(1) is used by the internal FPA, and thus is not available on an external pin.
$\overline{BusError}$	I	**Bus Error:** Input to the bus interface unit to terminate a bus transaction due to an external bus error. This signal is only sampled during read and write operations. If the bus transaction is a read operation, then the CPU will take a bus error exception.

2889 tbl 03

PIN DESCRIPTION (Continued):

PIN NAME	I/O	DESCRIPTION
$\overline{Int}$(5:3) $\overline{SInt}$(2:0)	I	**Processor Interrupt:** During normal operation, these signals are logically the same as the $\overline{Int}$(5:0) signals of the R3000. During processor reset, these signals perform mode initialization of the CPU, but in a different (simpler) fashion than the interrupt signals of the R3000. There are two types of interrupt inputs: the $\overline{SInt}$ inputs are internally synchronized by the processor, and may be driven by an asynchronous external agent. The direct interrupt inputs are not internally synchronized, and thus must be externally synchronized to the CPU. The direct interrupt inputs have one cycle lower latency than the synchronized interrupts. Note that the interrupt used by the on-chip FPA will not be monitored externally.
ClkIn	I	**Master Clock Input:** This input clock can be provided at the execution frequency of the CPU (1x clock mode) or at twice that frequency (2x clock mode), as selected at reset..
$\overline{Reset}$	I	**Master Processor Reset:** This signal initializes the CPU. Mode selection is performed during the last cycle of $\overline{Reset}$.
Rsvd(4:1)	I/O	**Reserved:** These four signal pins are reserved for testing and for future revisions of this device. Users must not connect these pins. Note that Rsvd(0) of the R3051 is now used for the $\overline{CohReq}$ input pin.

2889 tbl 04

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ABSOLUTE MAXIMUM RATINGS(1, 3)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TC	Operating Case Temperature	0 to +85	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +155	°C
VIN	Input Voltage	–0.5 to +7.0	–0.5 to +7.0	V

2889 tbl 05

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VIN minimum = –3.0V for pulse width less than 15ns.
   VIN should not exceed VCC +0.5V.
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

AC TEST CONDITIONS—3081

Symbol	Parameter	Min.	Max.	Unit
VIH	Input HIGH Voltage	3.0	—	V
VIL	Input LOW Voltage	—	0.4	V
VIHS	Input HIGH Voltage	3.5	—	V
VILS	Input LOW Voltage	—	0.4	V

2889 tbl 06

AC TEST CONDITIONS—3081L

Symbol	Parameter	Min.	Max.	Unit
VIH	Input HIGH Voltage	3.0	—	V
VIL	Input LOW Voltage	—	0.4	V
VIHS	Input HIGH Voltage	3.5	—	V
VILS	Input LOW Voltage	—	0.4	V

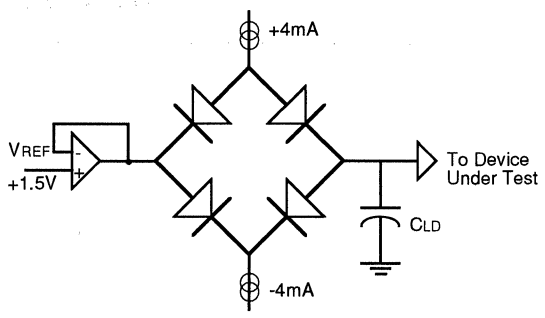
2889 tbl 06

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	VCC
Military	–55°C to +125°C (Case)	0V	5.0 ±10%
Commercial	0°C to +85°C (Case)	0V	5.0 ±5%
Commercial	0°C to +85°C (Case)	0V	3.3 ±5%

2889 tbl 07

OUTPUT LOADING FOR AC TESTING



2889 drw 08

Signal	CLD
$\overline{\text{SysClk}}$	50 pf
All Others	25 pf

2889 tbl 08

DC ELECTRICAL CHARACTERISTICS 3081— (T_C = 0°C to +85°C, V_{CC} = +5.0V ±5%)

Symbol	Parameter	Test Conditions	20MHz		25MHz		33.33MHz		40MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = -4mA	3.5	—	3.5	—	3.5	—	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	—	0.4	—	0.4	—	0.4	—	0.4	V
V_{IH}	Input HIGH Voltage(3)	—	2.0	—	2.0	—	2.0	—	2.0	—	V
V_{IL}	Input LOW Voltage(1)	—	—	0.8	—	0.8	—	0.8	—	0.8	V
V_{IHS}	Input HIGH Voltage(2,3)	—	3.0	—	3.0	—	3.0	—	3.0	—	V
V_{ILS}	Input LOW Voltage(1,2)	—	—	0.4	—	0.4	—	0.4	—	0.4	V
C_{IN}	Input Capacitance(4)	—	—	10	—	10	—	10	—	10	pF
C_{OUT}	Output Capacitance(4)	—	—	10	—	10	—	10	—	10	pF
I_{CC}	Operating Current	V_{CC} = 5V, T_A = 25°C	—	850	—	950	—	1050	—	1200	mA
I_{IH}	Input HIGH Leakage	V_{IH} = VCC	—	100	—	100	—	100	—	100	µA
I_{IL}	Input LOW Leakage	V_{IL} = GND	–100	—	–100	—	–100	—	–100	—	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	–100	100	–100	100	–100	100	–100	100	µA

NOTES: 2889 tbl 09

1. V_{IL} Min. = –3.0V for pulse width less than 15ns. V_{IL} should not fall below -0.5V for larger periods.
2. V_{IHS} and V_{ILS} apply to ClkIn and $\overline{Reset}$.
3. V_{IH} should not be held above V_{CC} + 0.5V.
4. Guaranteed by design.

DC ELECTRICAL CHARACTERISTICS 3081L— (T_C = 0°C to +85°C, V_{CC} = +3.3V ±0.3V)

Symbol	Parameter	Test Conditions	20MHz		25MHz		33.33MHz		40MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	—	2.4	—	2.4	—	2.4	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	—	0.4	—	0.4	—	0.4	—	0.4	V
V_{IH}	Input HIGH Voltage(3)	—	2.0	—	2.0	—	2.0	—	2.0	—	V
V_{IL}	Input LOW Voltage(1)	—	—	0.8	—	0.8	—	0.8	—	0.8	V
V_{IHS}	Input HIGH Voltage(2,3)	—	2.8	—	2.8	—	2.8	—	2.8	—	V
V_{ILS}	Input LOW Voltage(1,2)	—	—	0.4	—	0.4	—	0.4	—	0.4	V
C_{IN}	Input Capacitance(4)	—	—	10	—	10	—	10	—	10	pF
C_{OUT}	Output Capacitance(4)	—	—	10	—	10	—	10	—	10	pF
I_{CC}	Operating Current	V_{CC} = 3.3V, T_A = 25°C	—	500	—	550	—	650	—	750	mA
I_{IH}	Input HIGH Leakage	V_{IH} = VCC	—	100	—	100	—	100	—	100	µA
I_{IL}	Input LOW Leakage	V_{IL} = GND	–100	—	–100	—	–100	—	–100	—	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	–100	100	–100	100	–100	100	–100	100	µA

NOTES: 2889 tbl 09

1. V_{IL} Min. = –3.0V for pulse width less than 15ns. V_{IL} should not fall below -0.5V for larger periods.
2. V_{IHS} and V_{ILS} apply to ClkIn and $\overline{Reset}$.
3. V_{IH} should not be held above V_{CC} + 0.5V.
4. Guaranteed by design.

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AC ELECTRICAL CHARACTERISTICS 3081 (1, 2) — (Tc = 0°C to +85°C, Vcc = +5.0V ±5%)

Symbol	Signals	Description	20MHz		25MHz		33.33MHz		40MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t1	BusReq, Ack, BusError, RdCEn, CohReq	Set-up to SysClk rising	6	—	5	—	4	—	3	—	ns
t1a	A/D	Set-up to SysClk falling	7	—	6	—	5	—	4.5	—	ns
t2	BusReq, Ack, BusError, RdCEn, CohReq	Hold from SysClk rising	4	—	4	—	3	—	3	—	ns
t2a	A/D	Hold from SysClk falling	2	—	2	—	1	—	1	—	
t3	A/D, Addr, Diag, ALE, Wr Burst/WrNear, Rd, DataEn	Tri-state from SysClk rising	—	10	—	10	—	10	—	10	ns
t4	A/D, Addr, Diag, ALE, Wr Burst/WrNear, Rd, DataEn	Driven from SysClk falling	—	10	—	10	—	10	—	10	ns
t5	BusGnt	Asserted from SysClk rising	—	8	—	7	—	6	—	5	ns
t6	BusGnt	Negated from SysClk falling	—	8	—	7	—	6	—	5	ns
t7	Wr, Rd, Burst/WrNear, A/D	Valid from SysClk rising	—	5	—	5	—	4	—	3.5	ns
t8	ALE	Asserted from SysClk rising	—	4	—	4	—	3	—	3	ns
t9	ALE	Negated from SysClk falling	—	4	—	4	—	3	—	3	ns
t10	A/D	Hold from ALE negated	2	—	2	—	1.5	—	1.5	—	ns
t11	DataEn	Asserted from SysClk falling	—	15	—	15	—	13	—	12	ns
t12	DataEn	Asserted from A/D tri-state(3)	0	—	0	—	0	—	0	—	ns
t14	A/D	Driven from SysClk rising(3)	0	—	0	—	0	—	0	—	ns
t15	Wr, Rd, DataEn, Burst/WrNear	Negated from SysClk falling	—	7	—	6	—	5	—	4	ns
t16	Addr(3:2)	Valid from SysClk	—	6	—	6	—	5	—	4.5	ns
t17	Diag	Valid from SysClk	—	12	—	11	—	10	—	9	ns
t18	A/D	Tri-state from SysClk falling	—	10	—	10	—	9	—	8	ns
t19	A/D	SysClk falling to data out	—	12	—	11	—	10	—	9	ns
t20	ClkIn (2x clock mode)	Pulse Width High	10	—	8	—	6.5	—	5.6	—	ns
t21	ClkIn (2x clock mode)	Pulse Width Low	10	—	8	—	6.5	—	5.6	—	ns
t22	ClkIn (2x clock mode)	Clock Period	25	250	20	250	15	250	12.5	250	ns
t23	Reset	Pulse Width from Vcc valid	200	—	200	—	200	—	200	—	µs
t24	Reset	Minimum Pulse Width	32	—	32	—	32	—	32	—	tsys
t25	Reset	Set-up to SysClk falling	6	—	5	—	4	—	3	—	ns
t26	Int	Mode set-up to Reset rising	10	—	9	—	8	—	7	—	ns
t27	Int	Mode hold from Reset rising	0	—	0	—	0	—	0	—	ns
t28	SInt, SBrCond	Set-up to SysClk falling	6	—	5	—	4	—	3	—	ns
t29	SInt, SBrCond	Hold from SysClk falling	3	—	3	—	2	—	2	—	ns
t30	Int, BrCond	Set-up to SysClk falling	6	—	5	—	4	—	3	—	ns
t31	Int, BrCond	Hold from SysClk falling	3	—	3	—	2	—	2	—	ns
tsys	SysClk (full frequency mode)	Pulse Width(5)	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	
t32	SysClk (full frequency mode)	Clock High Time(5)	t22-2	t22+2	t22-2	t22+2	t22-1	t22+1	t22-1	t22+1	ns

2889 tbl 10

NOTES:

1. All timings referenced to 1.5V.
2. The AC values listed here reference timing diagrams contained in the *R3081 Family Hardware User's Manual.*
3. Guaranteed by design.
4. This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25pF over the specified test load condition.
5. In 1x clock mode, t22 is replaced by t44/2.

AC ELECTRICAL CHARACTERISTICS 3081 (continued)[1, 2] — (T_C = 0°C to +85°C, V_{CC} = +5.0V ±5%)

Symbol	Signals	Description	20MHz		25MHz		33.33MHz		40MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t33	$\overline{SysClk}$ (full frequency mode)	Clock Low Time[5]	t22-2	t22+2	t22-2	t22+2	t22-1	t22+1	t22-1	t22+1	ns
tsys/2	$\overline{SysClk}$ (half frequency mode)	Pulse Width[5]	4*t22	4*t22	4*t22	4*t22	4*t22	4*t22	4*t22	4*t22	
t34	$\overline{SysClk}$ (half frequency mode)	Clock High Time[5]	2*t22-2	2*t22+2	2*t22-2	2*t22+2	2*t22-1	2*t22+1	2*t22-1	2*t22+1	ns
t35	$\overline{SysClk}$ (half frequency mode)	Clock Low Time[5]	2*t22-2	2*t22+2	2*t22-2	2*t22+2	2*t22-1	2*t22+1	2*t22-1	2*t22+1	ns
t36	ALE	Set-up to $\overline{SysClk}$ falling	9	—	8	—	7	—	6	—	ns
t37	ALE	Hold from $\overline{SysClk}$ falling	2	—	2	—	1	—	1	—	ns
t38	A/D	Set-up to ALE falling	10	—	9	—	8	—	8	—	ns
t39	A/D	Hold from ALE falling	2	—	2	—	1	—	1	—	ns
t40	$\overline{Wr}$	Set-up to $\overline{SysClk}$ rising	10	—	9	—	8	—	7	—	ns
t41	$\overline{Wr}$	Hold from $\overline{SysClk}$ rising	3	—	3	—	3	—	3	—	ns
t42	ClkIn (1x clock mode)	Pulse Width High	20	—	16	—	13	—	11	—	ns
t43	ClkIn (1x clock mode)	Pulse Width Low	20	—	16	—	13	—	11	—	ns
t44	ClkIn (1x clock mode)	Clock Period	50	50	40	50	30	50	25	50	ns
tderate	All outputs	Timing deration for loading over C_{LD}[3, 4]	—	0.5	—	0.5	—	0.5	—	0.5	ns/ 25pF

2889 tbl 11

NOTES:
1. All timings referenced to 1.5V.
2. The AC values listed here reference timing diagrams contained in the *R3081 Family Hardware User's Manual.*
3. Guaranteed by design.
4. This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25pF over the specified test load condition.
5. In 1x clock mode, t22 is replaced by t44/2.

5

AC ELECTRICAL CHARACTERISTICS 3081L [1, 2] — (Tc = 0°C to +85°C, Vcc = +3.3V ±5%)

Symbol	Signals	Description	20MHz		25MHz		33.33MHz		40MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t1	BusReq, Ack, BusError, RdCEn, CohReq	Set-up to SysClk rising	6	—	5	—	4	—	3	—	ns
t1a	A/D	Set-up to SysClk falling	7	—	6	—	5	—	4.5	—	ns
t2	BusReq, Ack, BusError, RdCEn, CohReq	Hold from SysClk rising	4	—	4	—	3	—	3	—	ns
t2a	A/D	Hold from SysClk falling	2	—	2	—	1	—	1	—	
t3	A/D, Addr, Diag, ALE, Wr Burst/WrNear, Rd, DataEn	Tri-state from SysClk rising	—	10	—	10	—	10	—	10	ns
t4	A/D, Addr, Diag, ALE, Wr Burst/WrNear, Rd, DataEn	Driven from SysClk falling	—	10	—	10	—	10	—	10	ns
t5	BusGnt	Asserted from SysClk rising	—	8	—	7	—	6	—	5	ns
t6	BusGnt	Negated from SysClk falling	—	8	—	7	—	6	—	5	ns
t7	Wr, Rd, Burst/WrNear, A/D	Valid from SysClk rising	—	5	—	5	—	4	—	3.5	ns
t8	ALE	Asserted from SysClk rising	—	4	—	4	—	3	—	3	ns
t9	ALE	Negated from SysClk falling	—	4	—	4	—	3	—	3	ns
t10	A/D	Hold from ALE negated	2	—	2	—	1.5	—	1.5	—	ns
t11	DataEn	Asserted from SysClk falling	—	15	—	15	—	13	—	12	ns
t12	DataEn	Asserted from A/D tri-state[3]	0	—	0	—	0	—	0	—	ns
t14	A/D	Driven from SysClk rising[3]	0	—	0	—	0	—	0	—	ns
t15	Wr, Rd, DataEn, Burst/WrNear	Negated from SysClk falling	—	7	—	6	—	5	—	4	ns
t16	Addr(3:2)	Valid from SysClk	—	6	—	6	—	5	—	4.5	ns
t17	Diag	Valid from SysClk	—	12	—	11	—	10	—	9	ns
t18	A/D	Tri-state from SysClk falling	—	10	—	10	—	9	—	8	ns
t19	A/D	SysClk falling to data out	—	12	—	11	—	10	—	9	ns
t20	ClkIn (2x clock mode)	Pulse Width High	10	—	8	—	6.5	—	5.5	—	ns
t21	ClkIn (2x clock mode)	Pulse Width Low	10	—	8	—	6.5	—	5.5	—	ns
t22	ClkIn (2x clock mode)	Clock Period	25	250	20	250	15	250	12.5	250	ns
t23	Reset	Pulse Width from Vcc valid	200	—	200	—	200	—	200	—	µs
t24	Reset	Minimum Pulse Width	32	—	32	—	32	—	32	—	tsys
t25	Reset	Set-up to SysClk falling	6	—	5	—	4	—	3	—	ns
t26	Int	Mode set-up to Reset rising	10	—	9	—	8	—	7	—	ns
t27	Int	Mode hold from Reset rising	0	—	0	—	0	—	0	—	ns
t28	SInt, SBrCond	Set-up to SysClk falling	6	—	5	—	4	—	3	—	ns
t29	SInt, SBrCond	Hold from SysClk falling	3	—	3	—	2	—	2	—	ns
t30	Int, BrCond	Set-up to SysClk falling	6	—	5	—	4	—	3	—	ns
t31	Int, BrCond	Hold from SysClk falling	3	—	3	—	2	—	2	—	ns
tsys	SysClk (full frequency mode)	Pulse Width[5]	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	
t32	SysClk (full frequency mode)	Clock High Time[5]	t22-2	t22+2	t22-2	t22+2	t22-1	t22+1	t22-1	t22+1	ns

2889 tbl 10

NOTES:
1. All timings referenced to 1.5V.
2. The AC values listed here reference timing diagrams contained in the *R3081 Family Hardware User's Manual.*
3. Guaranteed by design.
4. This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25pF over the specified test load condition.
5. In 1x clock mode, t22 is replaced by t44/2.

AC ELECTRICAL CHARACTERISTICS 3081L (continued)[1, 2] — (Tc = 0°C to +85°C, Vcc = +3.3V ±5%)

Symbol	Signals	Description	20MHz		25MHz		33.33MHz		40MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t33	$\overline{SysClk}$ (full frequency mode)	Clock Low Time[5]	t22-2	t22+2	t22-2	t22+2	t22-1	t22+1	t22-1	t22+1	ns
tsys/2	$\overline{SysClk}$ (half frequency mode)	Pulse Width[5]	4*t22	4*t22	4*t22	4*t22	4*t22	4*t22	4*t22	4*t22	
t34	$\overline{SysClk}$ (half frequency mode)	Clock High Time[5]	2*t22-2	2*t22+2	2*t22-2	2*t22+2	2*t22-1	2*t22+1	2*t22-1	2*t22+1	ns
t35	$\overline{SysClk}$ (half frequency mode)	Clock Low Time[5]	2*t22-2	2*t22+2	2*t22-2	2*t22+2	2*t22-1	2*t22+1	2*t22-1	2*t22+1	ns
t36	ALE	Set-up to $\overline{SysClk}$ falling	9	—	8	—	7	—	6	—	ns
t37	ALE	Hold from $\overline{SysClk}$ falling	2	—	2	—	1	—	1	—	ns
t38	A/D	Set-up to ALE falling	10	—	9	—	8	—	8	—	ns
t39	A/D	Hold from ALE falling	2	—	2	—	1	—	1	—	ns
t40	$\overline{Wr}$	Set-up to $\overline{SysClk}$ rising	10	—	9	—	8	—	7	—	ns
t41	$\overline{Wr}$	Hold from $\overline{SysClk}$ rising	3	—	3	—	3	—	3	—	ns
t42	ClkIn (1x clock mode)	Pulse Width High	20	—	16	—	13	—	11	—	ns
t43	ClkIn (1x clock mode)	Pulse Width Low	20	—	16	—	13	—	11	—	ns
t44	ClkIn (1x clock mode)	Clock Period	50	50	40	50	30	50	25	50	ns
tderate	All outputs	Timing deration for loading over C_{LD}[3, 4]	—	0.5	—	0.5	—	0.5	—	0.5	ns/ 25pF

2889 tbl 11

NOTES:
1. All timings referenced to 1.5V.
2. The AC values listed here reference timing diagrams contained in the *R3081 Family Hardware User's Manual.*
3. Guaranteed by design.
4. This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25pF over the specified test load condition.
5. In 1x clock mode, t22 is replaced by t44/2.

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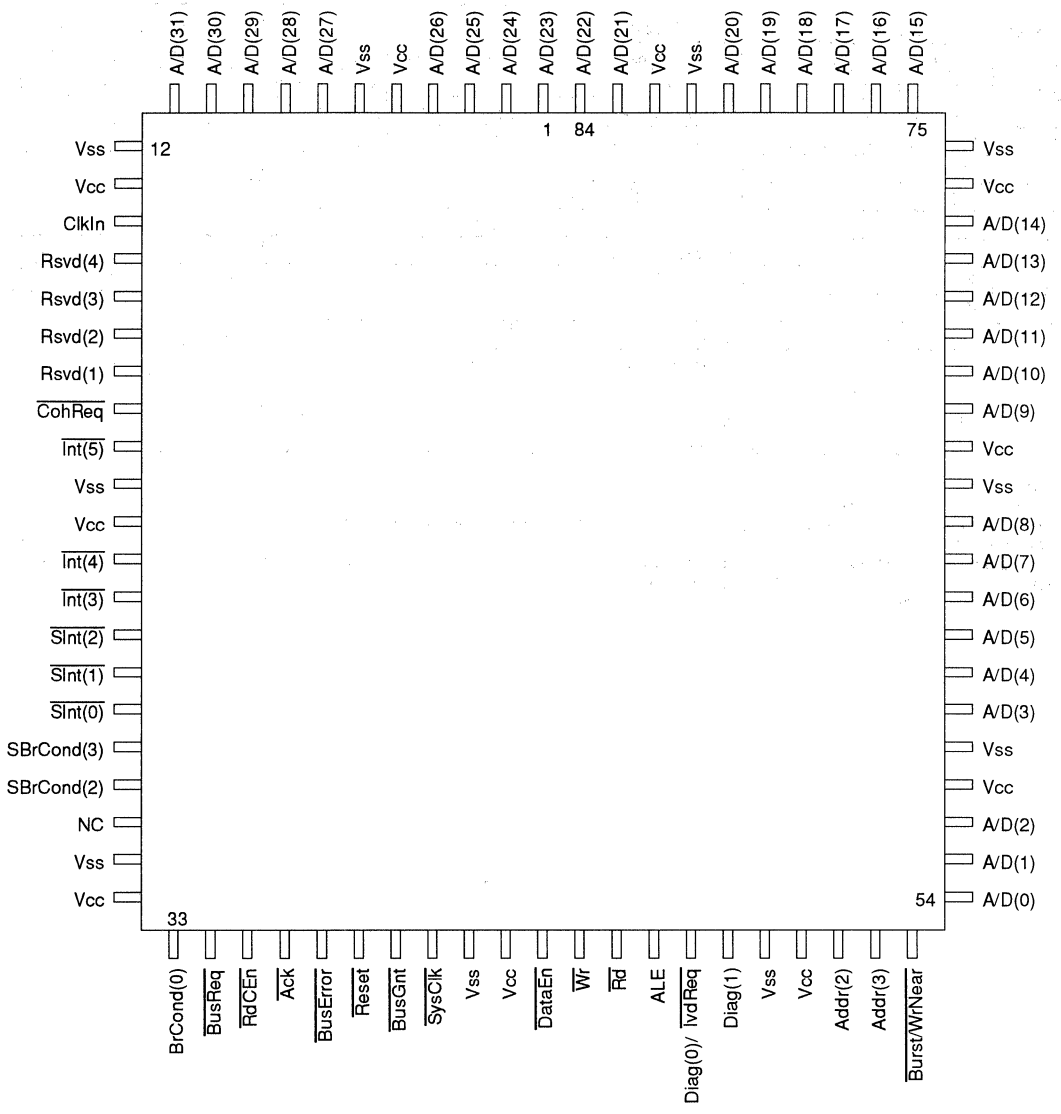
PIN CONFIGURATIONS



84-Pin MQUAD
Top View

NOTE:
Reserved Pins must not be connected.

PIN CONFIGURATIONS (CONTINUED)

	1	2	3	4	5	6	7	8	9	10	11	12
M	Vss	ClkIn	Rsvd (4)	Rsvd (2)	$\overline{\text{CohReq}}$	Vss	$\overline{\text{Int}}$ (4)	$\overline{\text{Int}}$ (3)	$\overline{\text{SInt}}$ (1)	S BrCond (3)	S BrCond (2)	BrCond (0)
L	A/D (28)	A/D (30)	Vcc	Rsvd (3)	Rsvd (1)	$\overline{\text{Int}}$ (5)	Vcc	$\overline{\text{SInt}}$ (2)	$\overline{\text{SInt}}$ (0)	NC	Vss	$\overline{\text{RdCEn}}$
K	A/D (27)	A/D (29)	A/D (31)							Vcc	$\overline{\text{BusReq}}$	$\overline{\text{Ack}}$
J	Vcc	Vss									$\overline{\text{Bus Error}}$	$\overline{\text{Reset}}$
H	A/D (25)	A/D (26)									$\overline{\text{BusGnt}}$	$\overline{\text{SysClk}}$
G	A/D (23)	A/D (24)									Vcc	Vss
F	A/D (21)	A/D (22)									$\overline{\text{Wr}}$	$\overline{\text{DataEn}}$
E	Vcc	Vss									ALE	$\overline{\text{Rd}}$
D	A/D (20)	A/D (19)									Diag (1)	Diag (0)/ $\overline{\text{IvdReq}}$
C	A/D (18)	A/D (16)	Vss							$\overline{\text{Burst/ WrNear}}$	Addr (2)	Vss
B	A/D (17)	Vcc	A/D (14)	A/D (11)	A/D (9)	A/D (8)	A/D (6)	A/D (4)	Vss	A/D (1)	Addr (3)	Vcc
A	A/D (15)	A/D (13)	A/D (12)	A/D (10)	Vcc	Vss	A/D (7)	A/D (5)	A/D (3)	Vcc	A/D (2)	A/D (0)

R3081
84-Pin Ceramic Pin Grid Array
(Cavity Down)

Bottom View

2889 drw 10

84-Pin PGA with Integral Thermal Slug

BottomView

NOTE
Reserved Pins must not be connected.

5

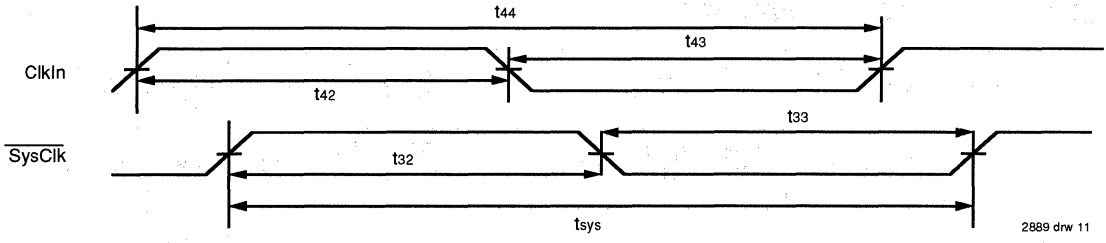


Figure 8 (a). R3081 Clocking (1x clock input mode, full frequency bus)

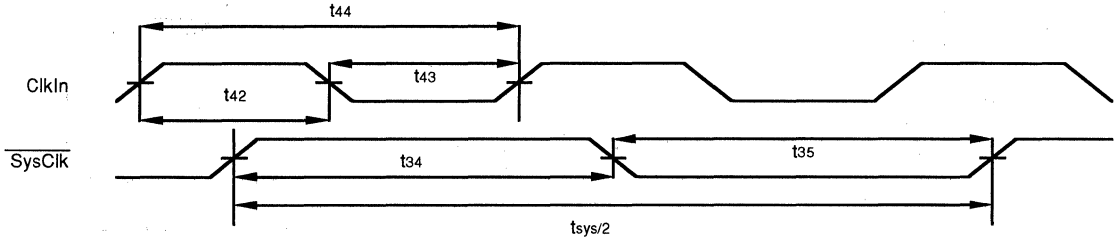


Figure 8 (b). R3081Clocking (1x clock input mode, half-frequency bus)

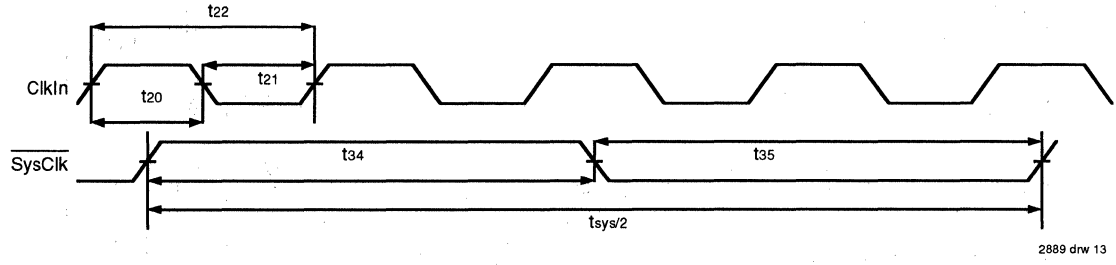


Figure 8 (c). R3081 Clocking (2x clock input mode, half-frequency bus)

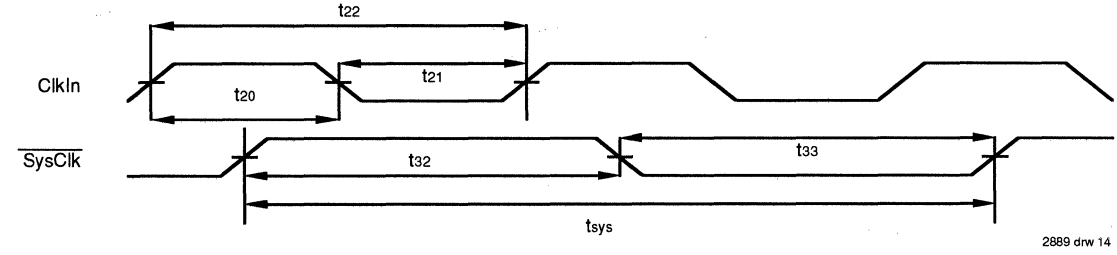


Figure 8 (d). R3081 Clocking (2x clock input mode, full-frequency bus)

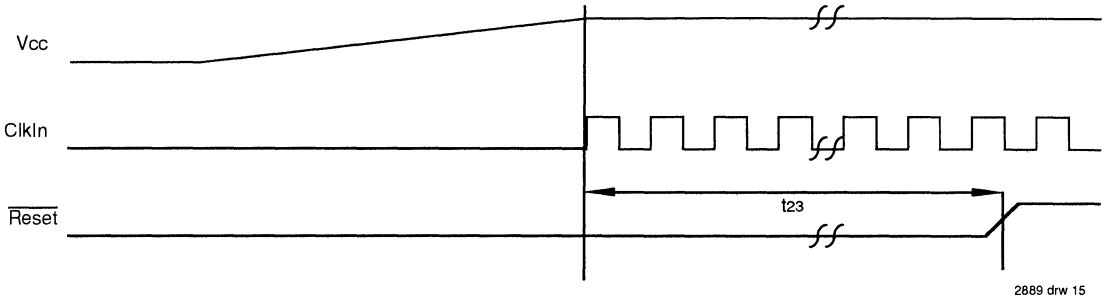


Figure 9. Power-On Reset Sequence

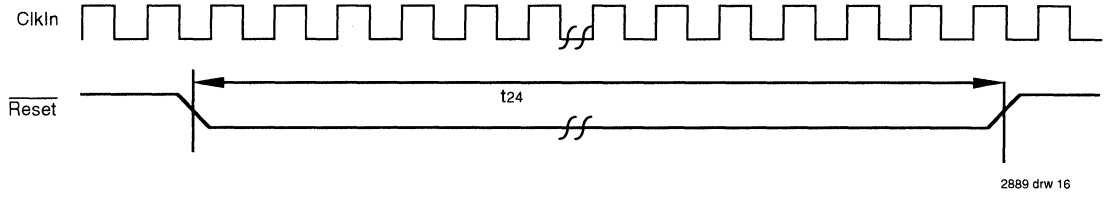


Figure 10. Warm Reset Sequence

5

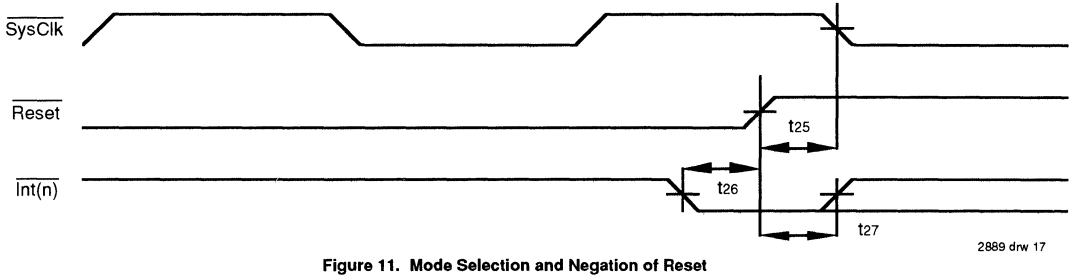


Figure 11. Mode Selection and Negation of Reset

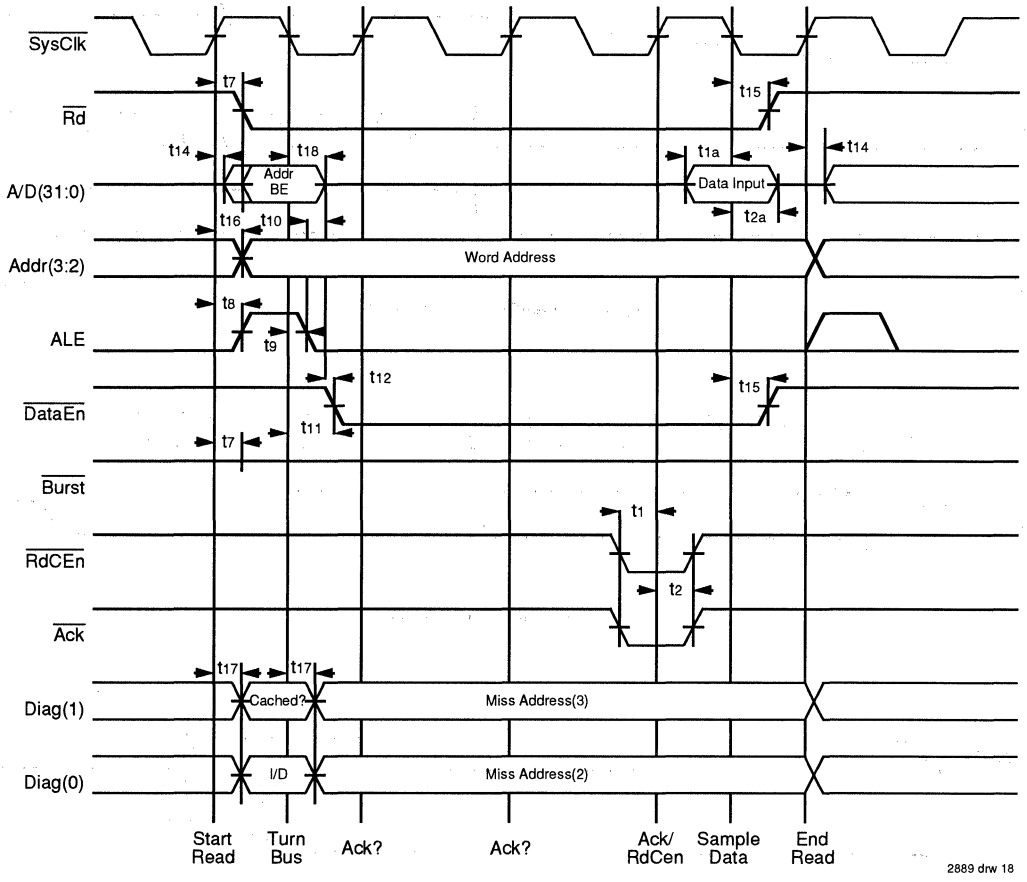


Figure 12. Single Datum Read in R3081

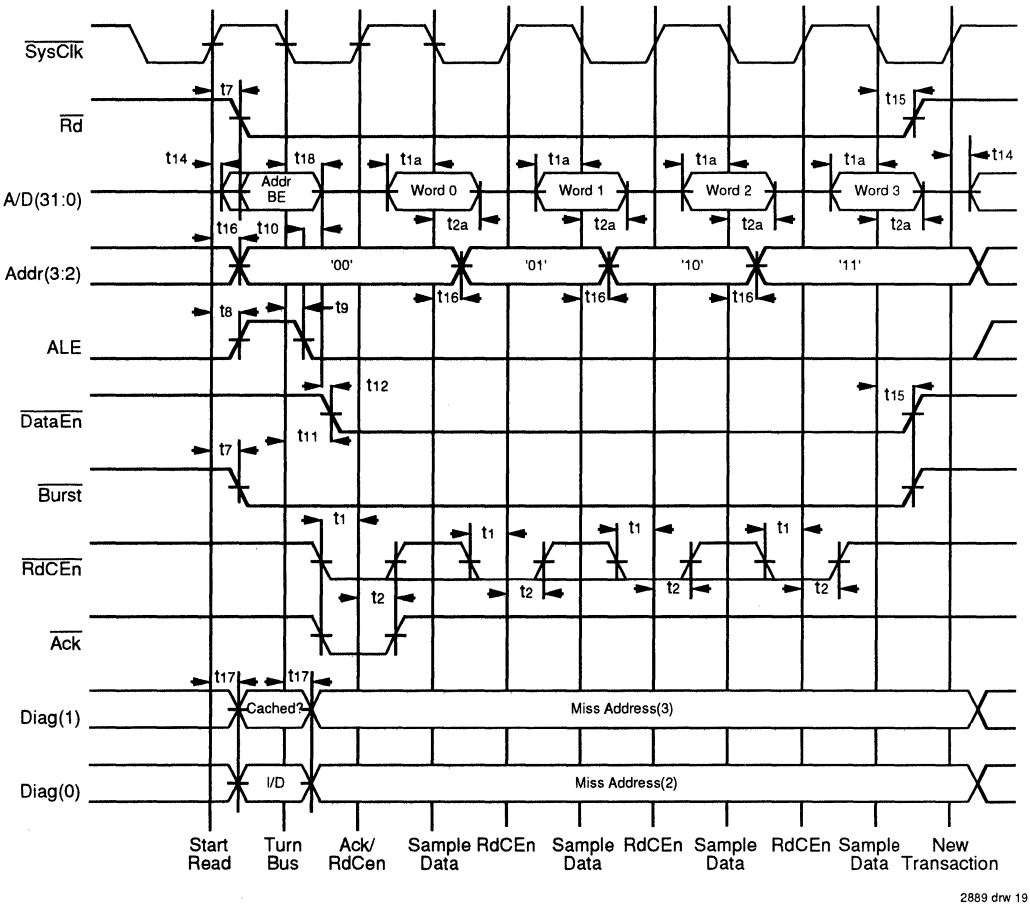


Figure 13. R3081 Burst Read

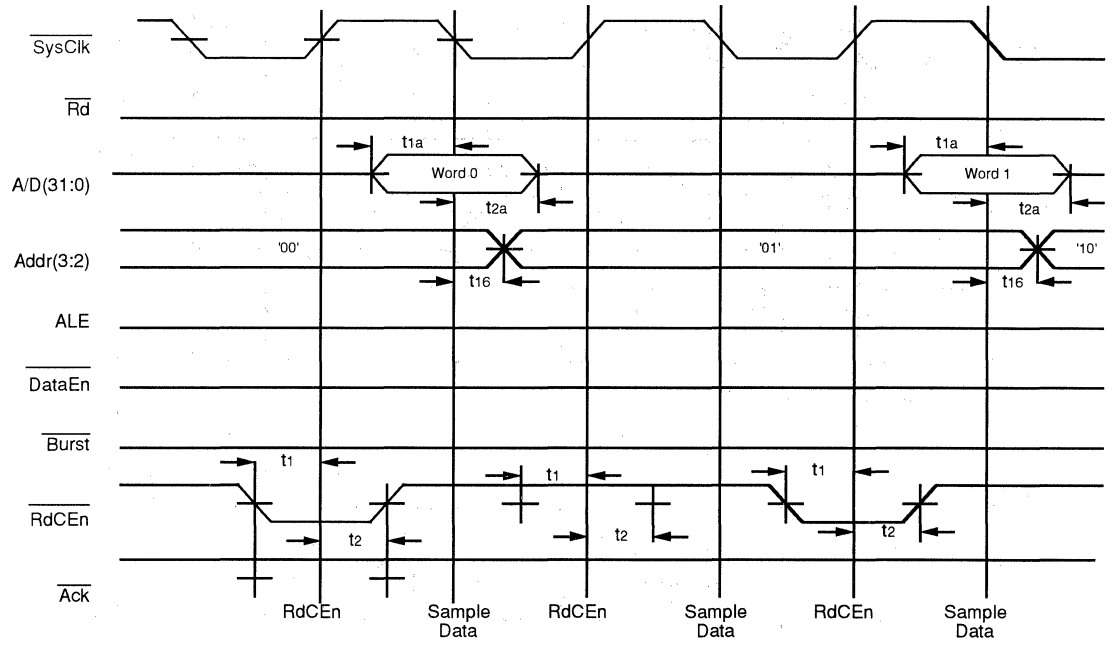


Figure 14 (a). Start of Throttled Quad Read

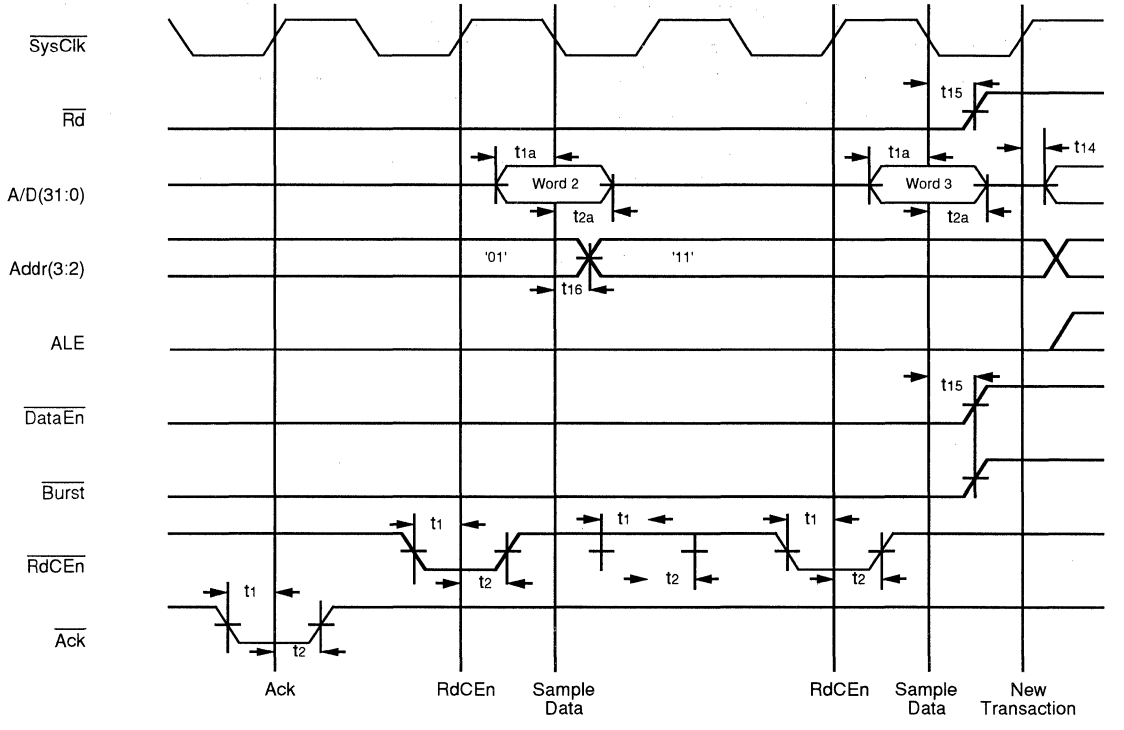


Figure 14 (b). End of Throttled Quad Read

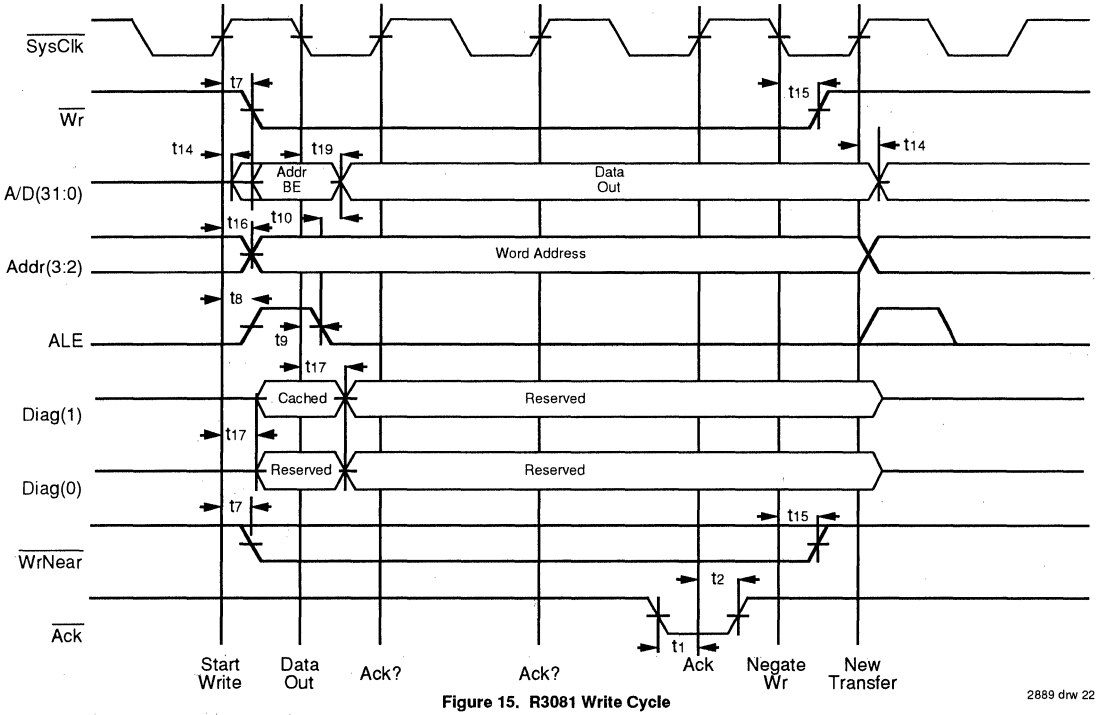


Figure 15. R3081 Write Cycle

2889 drw 22

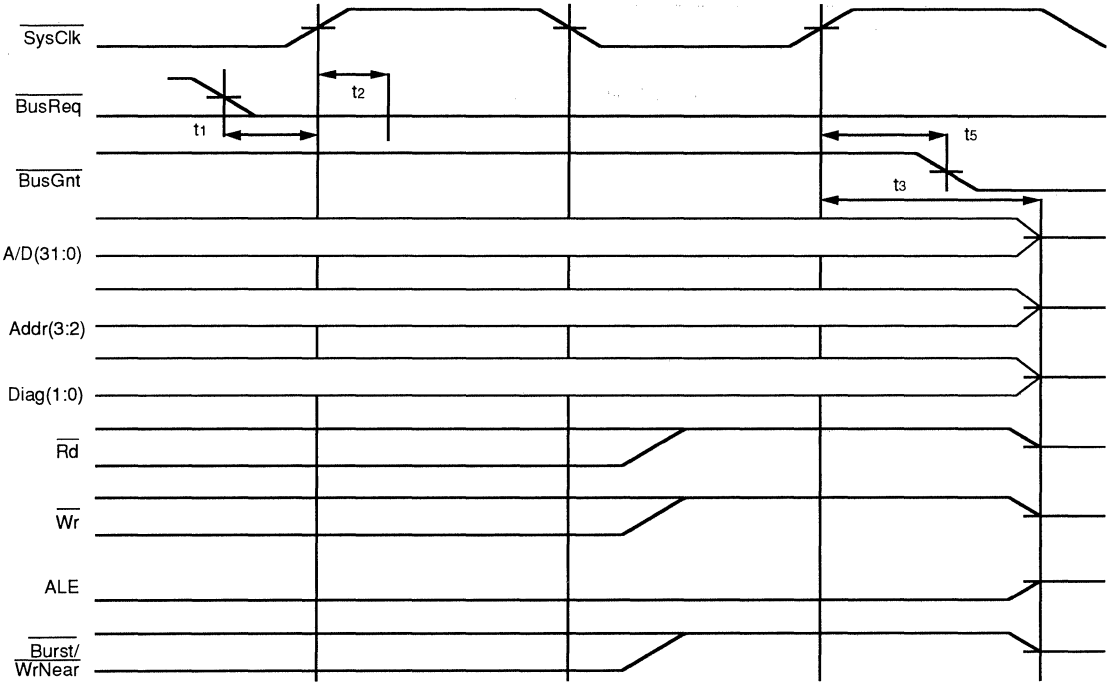


Figure 16. Request and Relinquish of R3081 Bus to External Master

2889 drw 23

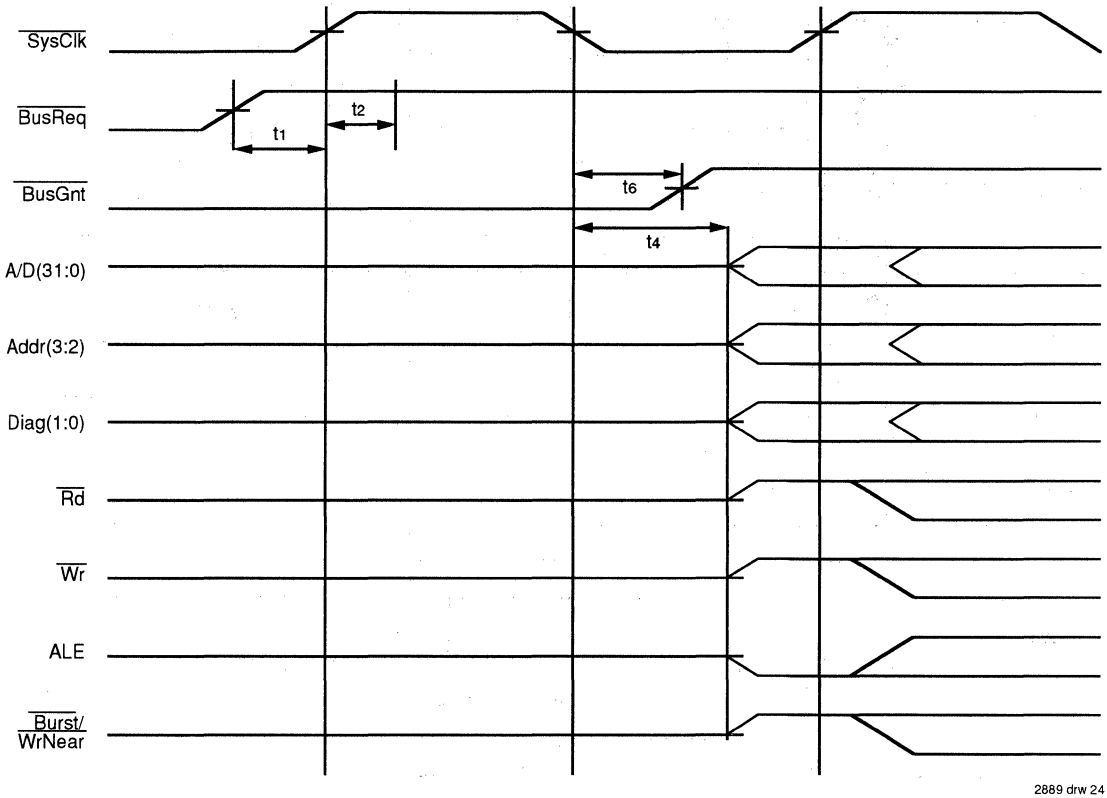


Figure 17. R3081 Regaining Bus Mastership

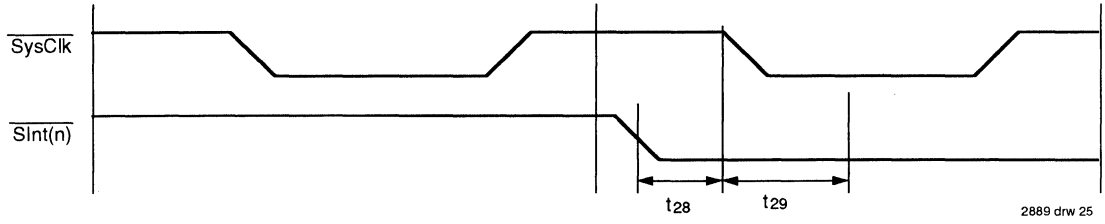


Figure 18. Synchronized Interrupt Input Timing

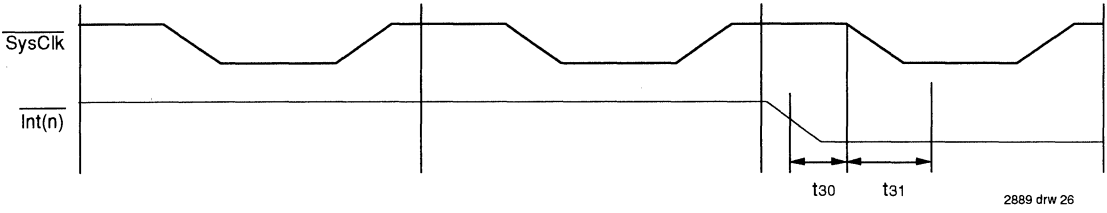


Figure 19. Direct Interrupt Input Timing

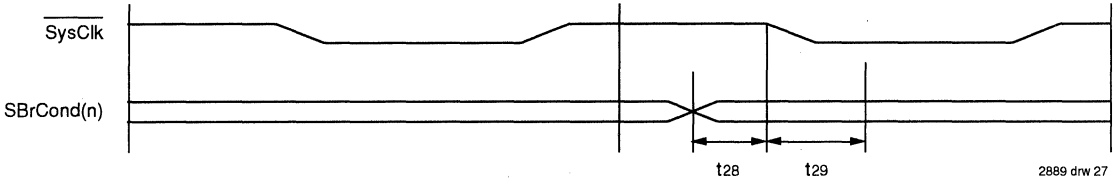


Figure 20. Synchronized Branch Condition Input Timing

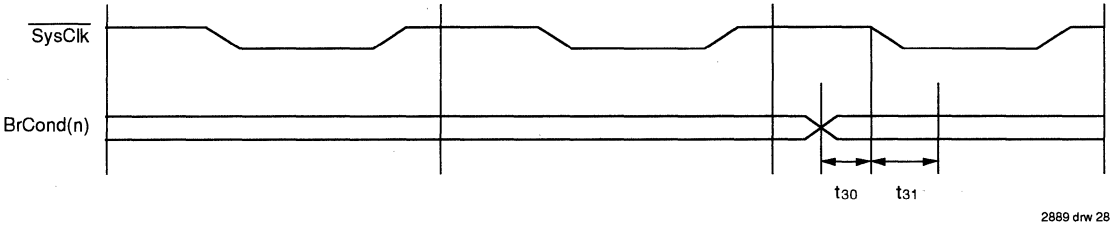


Figure 21. Direct Branch Condition Input Timing

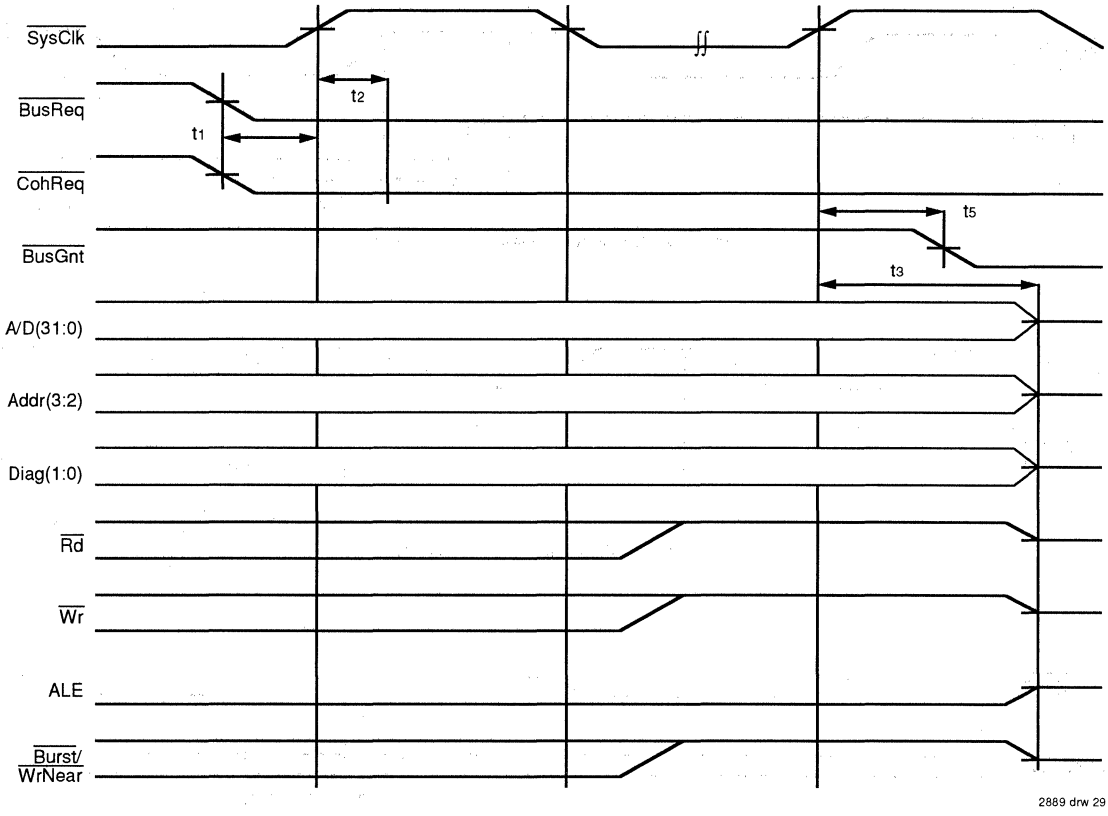


Figure 22. Coherent DMA Request

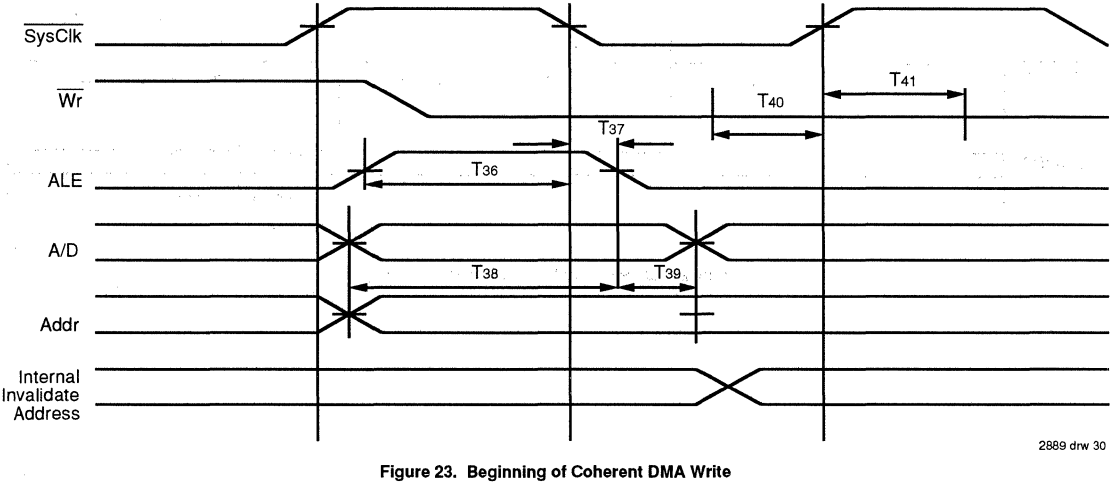


Figure 23. Beginning of Coherent DMA Write

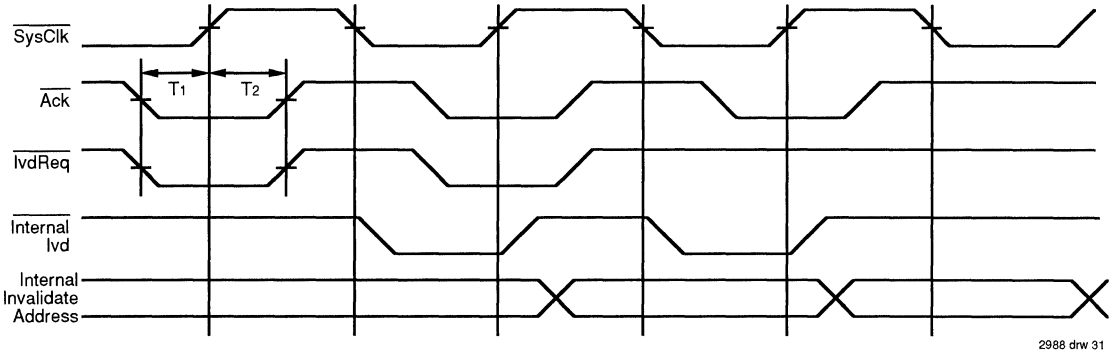


Figure 24. Cache Word Invalidation

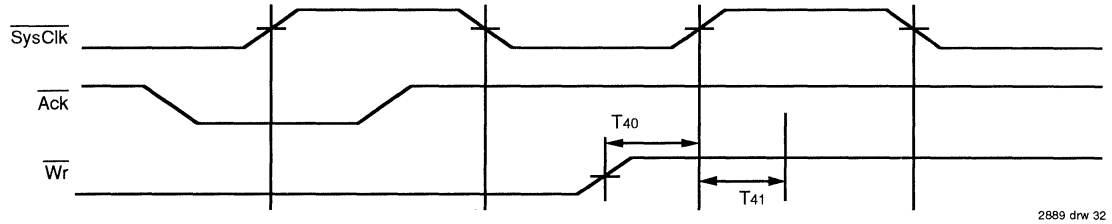


Figure 25. End of Coherent Write

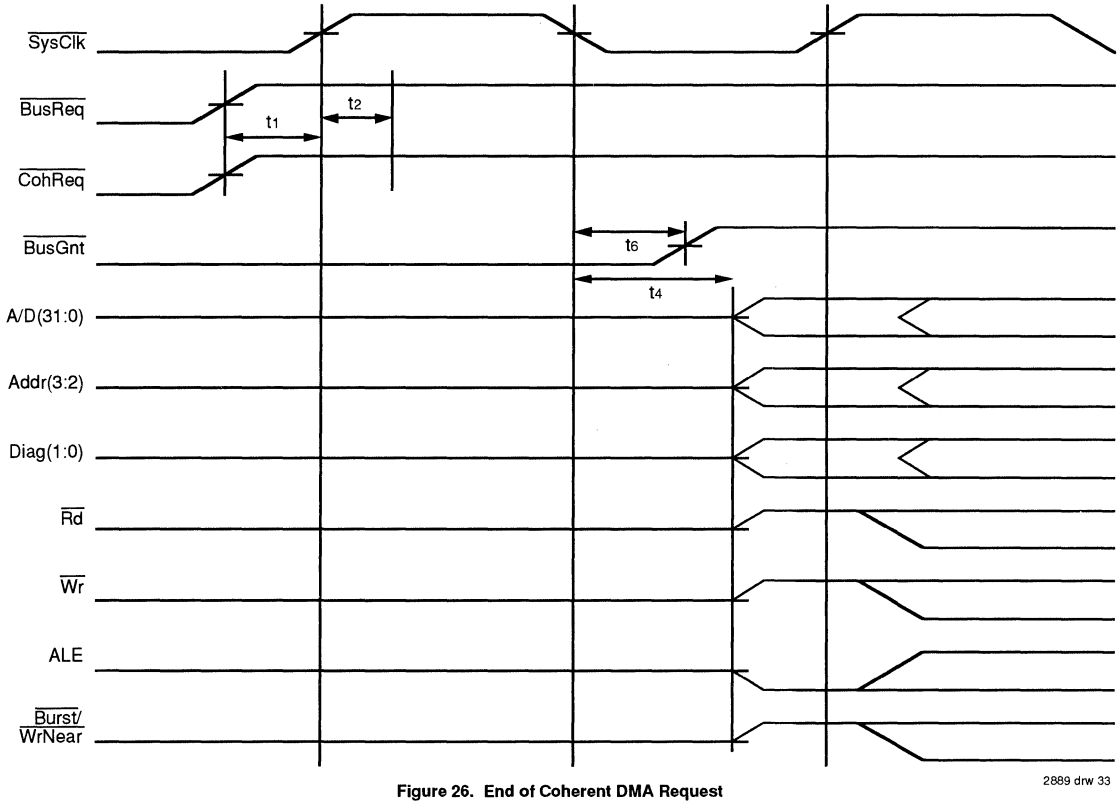


Figure 26. End of Coherent DMA Request

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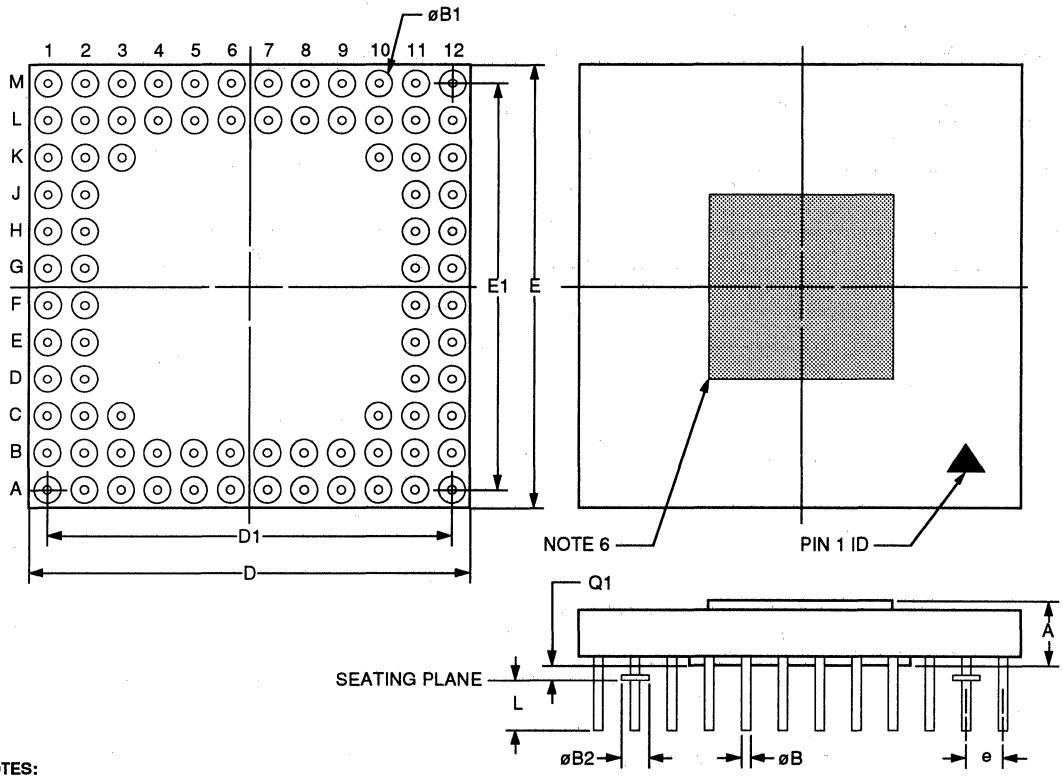
84-PIN PGA (CAVITY DOWN)



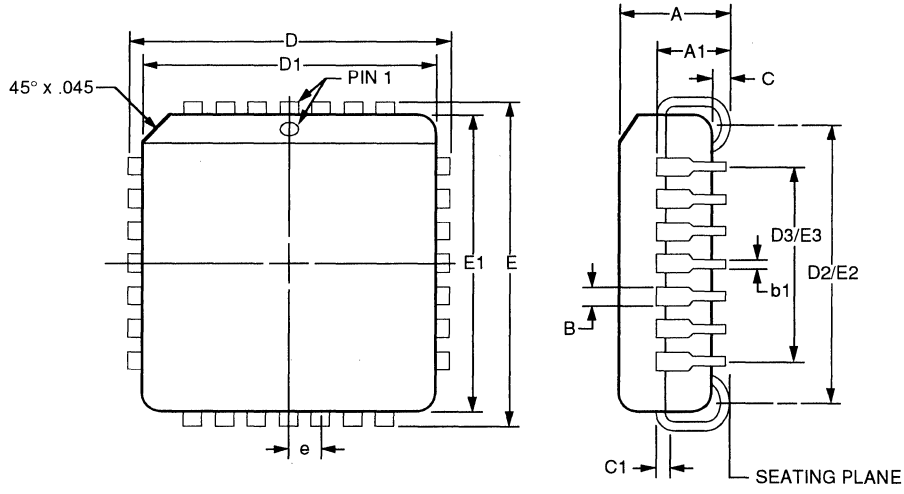
2889 drw 34

NOTES:
1. All dimensions are in inches, unless otherwise noted.
2. BSC—Basic lead Spacing between Centers
3. Symbol "M" represents the PGA matrix size.
4. Symbol "N" represents the number of pins.
5. Chamfered corners are IDT's option.
6. Shaded area indicates integral metallic heat sink.

Drawing #	G84-4	
Symbol	**Min**	**Max**
A	.077	.145
øB	.016	.020
øB1	.060	.080
øB2	.040	.060
D/E	1.180	1.235
D1/E1	1.100 BSC	
e	.100 BSC	
L	.120	.140
M	12	
N	84	
Q1	.025	.060

2889 tbl 12

84 LEAD MQUAD[7]



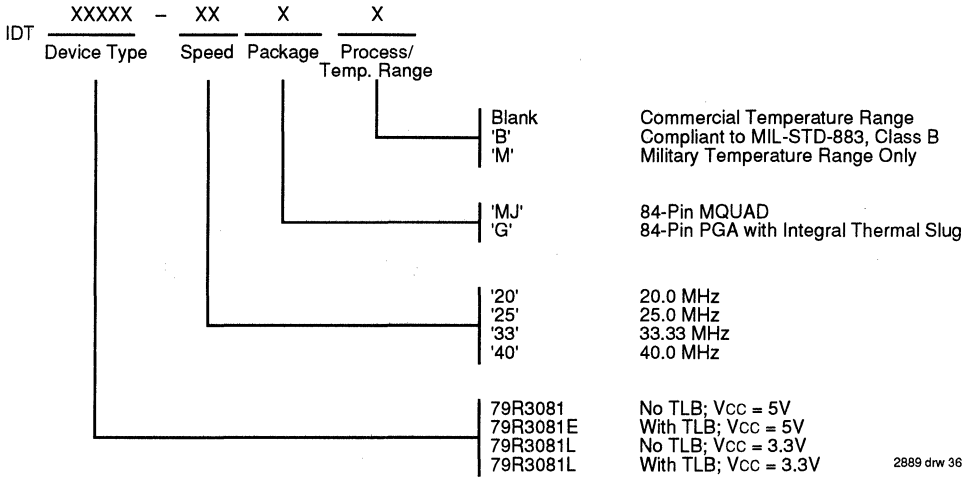
2889 drw 35

NOTES:
1. All dimensions are in inches, unless otherwise noted.
2. BSC—Basic lead Spacing between Centers.
3. D & E do not include mold flash or protutions.
4. Formed leads shall be planar with respect to one another and within .004" at the seating plane.
5. ND & NE represent the number of leads in the D & E directions respectively.
6. D1 & E1 should be measured from the bottom of the package.
7. 84-pin MQUAD is pin & form compatible with 84-pin PLCC of R3051/2

DWG #	MJ84-1	
# of Leads	84	
Symbol	Min.	Max.
A	165	.180
A1	.094	.114
B	.026	.032
b1	.013	.021
C	.020	.040
C1	.008	.012
D	1.185	1.195
D1	1.140	1.150
D2/E2	1.090	1.130
D3/E3	1.000 REF	
E	1.185	1.195
E1	1.140	1.150
e	.050 BSC	
ND/NE	21	

2889 tbl 13

ORDERING INFORMATION



VALID COMBINATIONS

IDT	79R3081 – 20, 25, 33, 40	All packages
	79R3081E – 20, 25, 33, 40	All packages
	79R3081L – 20, 25, 33, 40	All packages
	79R3081LE – 20, 25, 33, 40	All packages
	79R3081M, B – 20, 25	PGA Package Only
	79R3081EM, B – 20, 25	PGA Package Only

Integrated Device Technology, Inc.

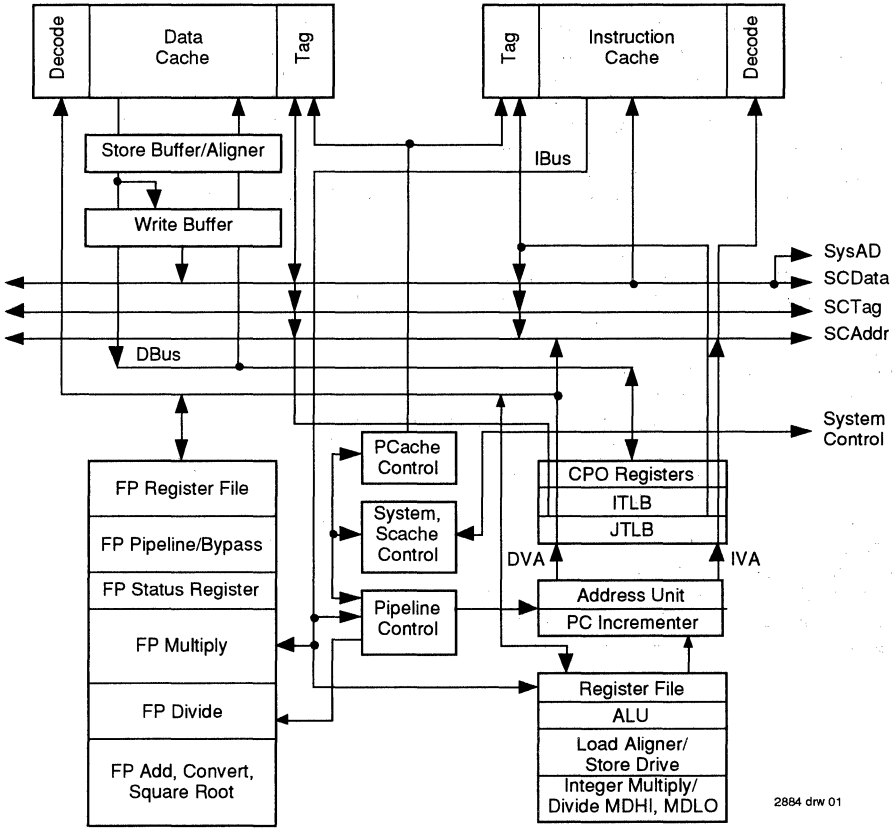
THIRD GENERATION 64-BIT SUPER-PIPELINED RISC MICROPROCESSOR

IDT79R4000, IDT79R4400 PRELIMINARY

FEATURES:

- True 64-bit microprocessor
  - — 64-bit integer operations
  - — 64-bit floating-point operations
  - — 64-bit registers
  - — 64-bit virtual address space
- High-performance microprocessor
  - — Super-pipelined architecture supports 150MIPS at 75MHz
  - — No issue restrictions for dual instruction issue
  - — Over 80 VUPs performance at 75MHz clock frequency
- High level of integration
  - — 64-bit integer CPU
  - — 64-bit floating-point accelerator
  - — 8KB instruction cache; 8KB data cache (R4000)
  - — 16KB instruction; 16KB data cache (R4400)
  - — Flexible MMU with large TLB
- Standard operating system support includes:
  - — Microsoft Windows NT
  - — UNISOFT UNIX System V.4
- Fully software compatible with R3000A 32-bit RISC Processor Family
- 50, 67 and 75MHz clock frequencies
- 64GB physical address space
- Processor family for a wide variety of applications
  - — Desktop workstations
  - — Deskside or departmental servers
  - — High-performance embedded applications
  - — Tightly coupled multi-processing systems
  - — Fault tolerant systems

BLOCK DIAGRAM



5

DESCRIPTION:

The IDT79R4000 family supports a wide variety of processor based applications, from 32-bit ARC compliant desktop systems through high-performance, 64-bit OLTP systems manipulating large data bases in a multi-processor based system. The IDT79R4000/R4400 family offers a broad range of price-performance options for high-performance systems, allowing the system architect unprecedented degrees of freedom in making price-performance tradeoffs.

The IDT R4000 family provides complete upward application-software compatibility with the IDT79R3000 family of microprocessors, including the IDT79R3000A and the IDT RISController™ family (the IDT79R3001 and IDT79R3051 family). Microsoft Windows NT and UNISOFT UNIX V.4 operating systems insure the availability of thousands of applications programs, geared to provide a complete solution to a large number of processing needs. An array of development tools facilitates the rapid development of R4000-based systems, enabling a wide variety of customers to take advantage of the MIPS Open Architecture philosophy.

The R4000 family achieves a unique balance between high-integer and high-floating-point performance. The key to this balance is the super-pipelined architecture of the processor, which brings performance gains to both integer and floating-point intensive programs without requiring re-compilation to take advantage of the architectural advancement. The super-pipeline architecture is well-balanced in the R4000 family; the high-performance execution engine is assured of a rapid and continual supply of instructions and data through the use of large on-chip caches, and a high-performance on-chip TLB. The result is consistently high-performance: over 80 VUPS at 75MHz over a wide variety of realistic applications programs.

The R4000 family also provides a compatible, timely, and necessary evolution path from 32-bit to true, 64-bit computing. The original design objectives of the R4000 clearly mandated this evolution path; the result is a true 64-bit processor fully compatible with 32-bit operating systems and applications.

The 64-bit computing and addressing capability of the R4000 enables a wide variety of capabilities previously limited by a smaller address space. For example, the large address space allows operating systems with extensive file mapping; direct access to large files can occur without explicit I/O calls. Applications such as large CAD databases, multi-media, and high-quality image storage and retrieval all directly benefit from the enlarged address space.

This data sheet provides an overview of the features and architecture of the IDT79R4000 CPU family. A more detailed description of the processor is available in the *"R4000 User's Manual"*, available from IDT. Further information on development support, applications notes, and complementary products are also available from your local IDT sales representative.

This data sheet describes both the R4000 and the R4400. The primary difference between the two devices is the amount of on-chip primary cache: the R4000 contains 8kB each of primary instruction and data cache, while the R4400 doubles this to 16kB each of cache. Throughout this data sheet, the term "R4000" will be used to describe characteristics common to both the R4000 and the R4400 devices.

IDT79R4000 FAMILY MEMBERS

The IDT79R4000 processor is available in three different configurations: the IDT79R4000MC and IDT79R4000SC, which include a 128-bit wide secondary cache bus; and the IDT79R4000PC, with no secondary cache interface. Additionally, the R4000PC and R4000SC are available with two different on-chip cache configurations: the R4000, with 8KB each of instruction and data cache; and the R4400, which doubles on-chip cache to 16KB each of instruction and cache.

PC CONFIGURATION

The IDT79R4000PC and 79R4400PC are available in a 179-pin Pin Grid Array (PGA). This configuration does not support secondary cache or cache coherency, and is ideal for applications such as high-performance embedded control and low-cost desktop systems, where the on-chip caches provide enough performance and where cost, power, and board space must be kept to a minimum. By eliminating a secondary cache, a system can be designed with fewer parts and lower power consumption.

SC CONFIGURATION

The IDT79R4000SC and 79R4400SC are available in a 447-pin Pin Grid Array (PGA). This processor supports a secondary cache interface and is ideal in systems where high performance is desired. This component supports a 128kB to 4mB secondary cache made from standard SRAMs. This flexibility allows system designers to make price/performance tradeoffs in cache subsystem designs.

MC CONFIGURATION

The IDT79R4400MC is also available in the 447-pin Pin Grid Array (PGA). This processor supports a secondary cache and configurable multiprocessor cache coherency protocols. Like the "SC" configuration, this processor also supports a 128kB to 4mB secondary cache made from standard SRAMs. The IDT79R4400MC is well suited for a range of designs from high performance desktop systems to fault tolerant multiprocessor servers.

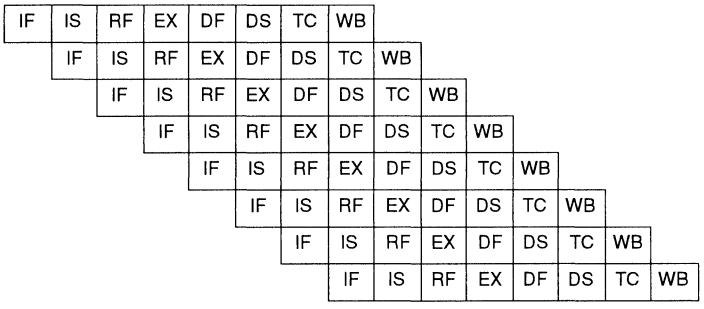
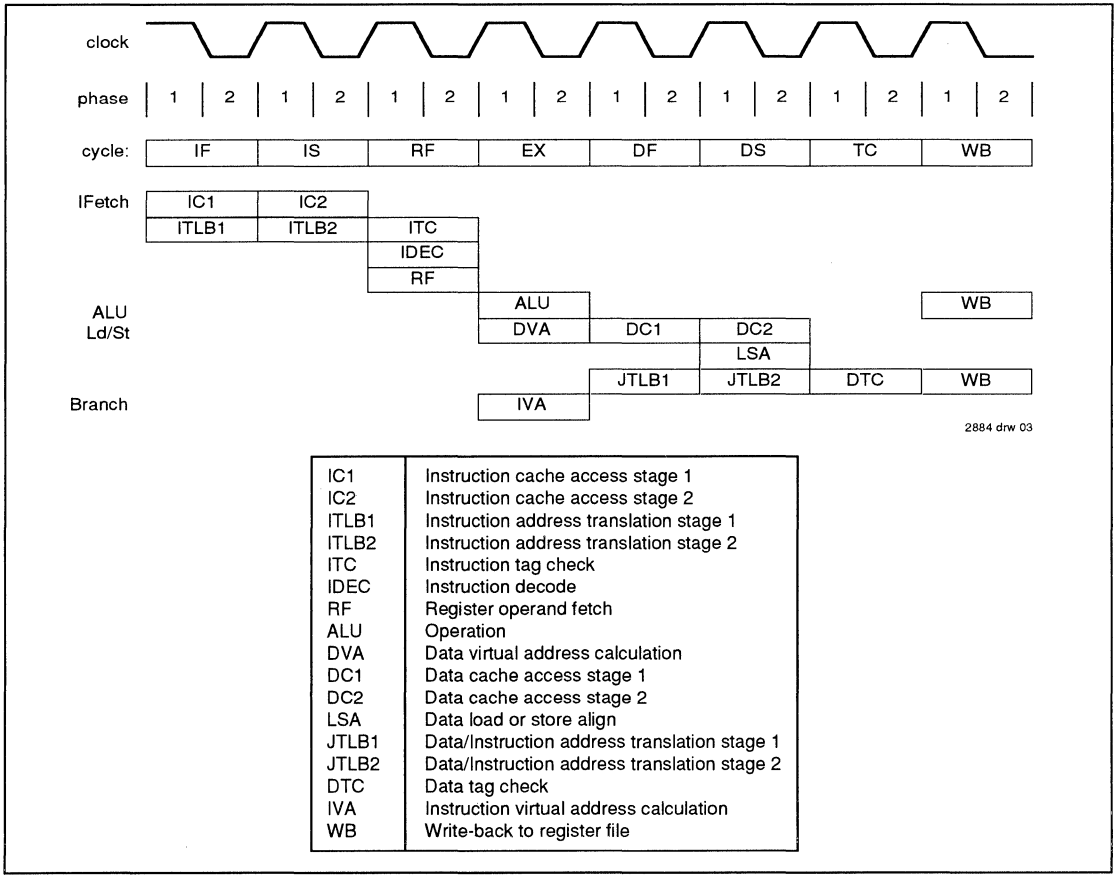


Figure 1. R4000 Family 8-Stage Super-Pipeline



IC1	Instruction cache access stage 1
IC2	Instruction cache access stage 2
ITLB1	Instruction address translation stage 1
ITLB2	Instruction address translation stage 2
ITC	Instruction tag check
IDEC	Instruction decode
RF	Register operand fetch
ALU	Operation
DVA	Data virtual address calculation
DC1	Data cache access stage 1
DC2	Data cache access stage 2
LSA	Data load or store align
JTLB1	Data/Instruction address translation stage 1
JTLB2	Data/Instruction address translation stage 2
DTC	Data tag check
IVA	Instruction virtual address calculation
WB	Write-back to register file

Figure 2. Pipeline Activities

5

HARDWARE OVERVIEW

The IDT R4000 family brings a high-level of integration designed for high-performance computing. The key elements of the IDT R4000 are briefly described below. A more detailed description of each of these subsystems is available in other literature.

Superpipelined Implementation

In order to achieve the high-performance desired for today's applications and user's interfaces, the R4000 exploits instruction level parallelism using a super-pipelined micro-architecture.

The R4000 uses an 8-stage superpipeline which places no issue restrictions on instruction issue. Thus, any two instructions can be issued each master clock cycle under normal circumstances, leading to 150MIPS performance at 75MHz. One key advantage of this architecture is that all existing applications can gain from the architectural advancement represented by the R4000, without requiring re-compilation to re-order the software.

In order to support dual instruction issue, the internal pipeline of the R4000 operates at twice the external clock frequency. Instruction execution stages such as cache accesses are pipelined (thus the chip itself is super-pipelined) to eliminate bottlenecks associated with long-latency functional units. Other stages, such as the ALU stage, completely process one operation per pipeline clock cycle, allowing the results of one operation to be immediately used by the instruction which follows, with no pipeline interlocks.

High clock frequency results from careful construction of the various resources of the processor: pipelining cache accesses, shortening register access times, implementing virtually indexed primary caches, and allowing the latency of functional units to span multiple pipeline stages.

After extensive simulation of many methods of exploiting instruction level parallelism, superpipelining was chosen because it improves integer performance commensurate with floating-point performance. Thus, the R4000 provides performance benefits both to technical computing applications, and also to a wide variety of commercial applications as well. In today's technology, super-pipelining results in less complex logic, faster cycle times, quicker design cycles, and lower cost. The pipeline of the IDT79R4000 is illustrated in Figure 1.

THE R4000 PIPELINE

The R4000 processor has an eight-stage execution pipeline. That is, each instruction takes eight Pclock (Pipeline clocks, at twice the frequency of the input clock) cycles to execute, but a new instruction is started on each Pclock cycle. Another way of viewing the process is that at any point in time, eight separate instructions are being executed at once. Figure 1 shows the R4000 pipeline in both views: a horizontal slice shows the execution process of individual instructions, and a vertical slice shows the processing of eight instructions at once.

Each box shown in the diagram corresponds to a part of the execution process.

Figure 2 illustrates the activities occuring within each pipestage as a function of the instruction type. First, in the IF stage, an instruction address is selected by the program counter logic and the first half of the both the instruction cache fetch (IC1) and the instruction virtual to physical address translation (ITLB1) is performed. The instruction address translation is done through a two entry subset of the main or *joint* translation lookaside buffer (JTLB) called the ITLB. In the IS stage, the second half of both the instruction cache fetch (IC2) and instruction translation (ITLB2) is done.

During the RF stage, three activities occur in parallel. The instruction decoder (IDEC) decodes the instruction and checks for interlock conditions. Meanwhile, the instruction tag check (ITC) is performed between the instruction cache tag and the page frame number (PFN) from the ITLB's translation. In parallel with both of the above, the operands are fetched from the register file (RF).

In the EX stage, if the instruction is a register-to-register operation, the arithmetic or logical operation is performed (ALU). If the instruction is a load/store, a data virtual address is calculated (DVA). If the instruction is a branch, a virtual branch target address is calculated (IVA).

For load/stores, the DF stage is used to do the first half of both the data cache fetch (DC1) and the data virtual to

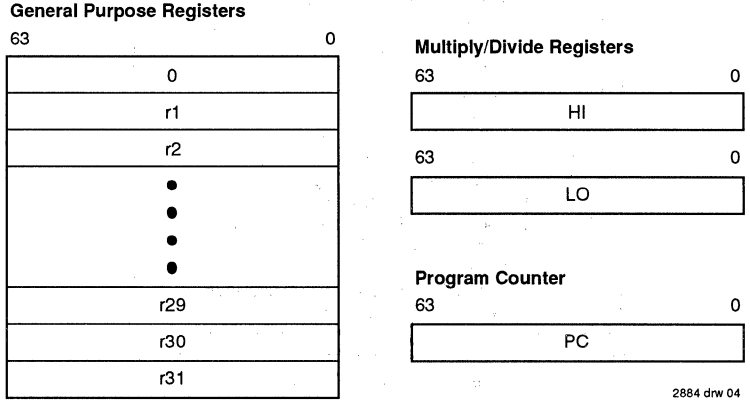


Figure 3. CPU Registers

physical address translation (JTLB1). Similarly, the DS stage does the second half of both the data fetch (DC2) and the data translation (JTLB2) as well as the load align or store align (LSA), as appropriate. If the instruction is a branch, the JTLB is used during DF and DS to translate the branch address and refill the ITLB if necessary.

The TC stage is used to perform the tag check for load/stores. During the WB stage the instruction result is written to the register file.

Smooth pipeline flow is interrupted when cache accesses miss, data dependencies are detected, or when exceptions occur. Interruptions that are handled by hardware, such as cache misses, are referred to as *interlocks,* while those that are handled using software are *exceptions.* Collectively, the cases of all interlock and exception conditions are referred to as *faults.*

Interlocks come in two varieties. Those interlocks which are resolved by simply stopping the pipeline are referred to as *stalls,* while those which require part of the pipeline to advance while holding up another part are *slips.*

At each cycle, exception and interlock conditions are checked for all active instructions. The conditions can be referred back to particular instructions, as each exception or interlock condition corresponds to a particular pipeline stage.

When an exception condition occurs, the relevant instruction and all that follow it in the pipeline are cancelled. Accordingly, any stall conditions and any later exception conditions that are referenced to the same instruction are inhibited; there is no value in servicing stalls for a cancelled instruction. A new instruction stream is begun, starting execution at a predefined exception vector. System control coprocessor registers are loaded with information that will identify the type of exception and any necessary auxiliary information, such as the virtual address at which translation exceptions occur.

When a stall condition is detected, all eight instructions, each in a different stage of the pipeline, are frozen at once. Often, the stall condition is only detected after parts of the pipeline have advanced using incorrect data; this occurrence is referred to as *pipeline overrun.* When in the stalled state, parts of the pipeline that are immune to overrun are frozen and the remainder is permitted to continue clocking. Just before resuming execution, the pipeline overrun is reversed by inserting corrected information into the pipeline.

When a slip condition is detected, the pipeline stages which must advance in order to resolve the dependency continue to be retired while the dependent stages are held until the necessary data is available.

Another class of interlocks exists which, since they originate external to the processor, are not referenced to a particular pipeline stage. These interlocks are referred to as *external* stalls and are unaffected by the occurrence of exceptions.

Integer Execution Engine

The R4000 implements the extended MIPS Instruction Set architecture, and thus is fully upwards compatible with appli-

5

CP0 & the TLB

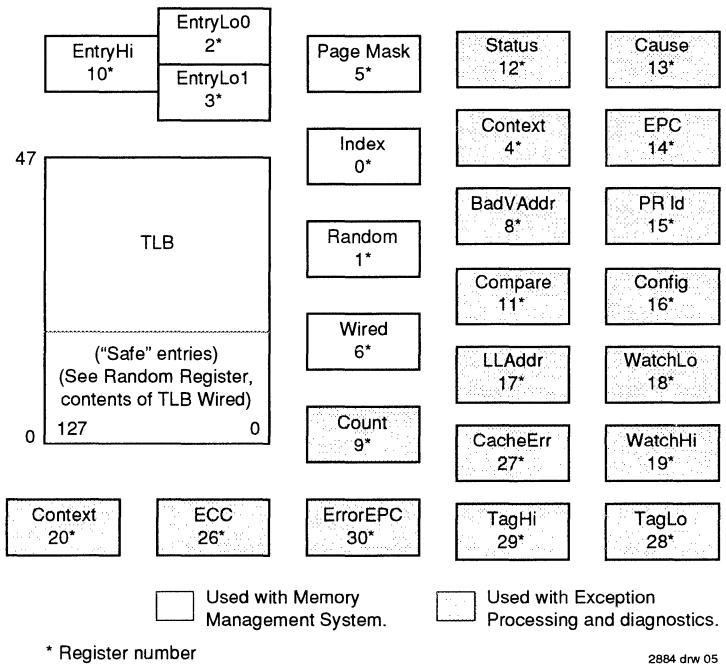


Figure 4. The R4000 CP0 Registers

cations running on the earlier generation parts. The R4000 includes additions to the instruction set, targeted at improving performance and capability while maintaining binary compatibility with earlier processors. The extensions result in better code density, greater multi-processing support, improved performance for commonly used code sequences in operating system kernels, and faster execution of floating-point intensive applications. All resource dependencies are made transparent to the programmer, insuring transportability amongst implementations of the MIPS instruction set architecture.

In addition to the instruction extensions detailed above, new instructions have been defined to take advantage of the 64-bit architecture of the processor. When operating as a 32-bit processor, the R4000 will take an exception on these new instructions.

The MIPS integer unit implements a load/store architecture with single cycle ALU operations (logical, shift, add, sub) and autonomous multiply/divide unit. The programmer model for the R4000 includes the register set illustrated in Figure 3. The register resources include: 32 general purpose orthogonal integer registers, the HI/LO result registers for the intger multiply/divide unit, and the program counter. In addition, the on-chip floating-point co-processor adds 32 floating-point registers, and a floating-point control/status register.

System Control Co-processor (CP0)

The system control co-processor in the MIPS architecture is responsible for the virtual memory sub-system, the exception control system, and the diagnostics capability of the processor. In the MIPS architecture, the system control co-processor (and thus the kernel software) is implementation dependent. The R4000 CP0 is a superset extension of the MMU found in the R3000A.

The Memory management unit controls the virtual memory system page mapping. It consists of an instruction translation buffer (the ITLB), a Joint TLB (the JTLB), and co-processor registers used for the virtual memory mapping sub-system.

System Control Co-Processor Registers

The R4000 incorporates all system control co-processor (CP0) registers on-chip. These registers provide the path through which the virtual memory system's page mapping is examined and changed, the operating modes (kernel vs. user mode, interrupts enabled or disabled, cache features) controlled, and these registers control exception handling. In addition, the R4000 includes registers to implement a real-time cycle counting facility, to address reference traps for debugging, to aid in cache diagnostic testing, and to assist in data error detection and correction.

Figure 4 illustrates the System Control Co-Processor.

Virtual to Physical Address Mapping

The R4000 provides three modes of virtual addressing:

- user mode
- kernel mode
- supervisor mode

This mechanism is available to system software to provide a secure environment for user processes. Bits in a status register determine which virtual addressing mode is used. In the user mode, the R4000 provides a single, uniform virtual address space of 2GB.

When operating in the kernel mode, four distinct virtual address spaces, totalling 4GB, are simultaneously available and are differentiated by the high-order bits of the virtual address.

The R4000 processors also support a supervisor mode in which the virtual address space is 2.5GB, divided into two regions based on the high-order bits of the virtual address. The three different modes of virtual addressing are shown in Figure 5. When the R4000 is configured as a 64-bit microprocessor, the virtual address space layout is a compatible extension of the 32-bit virtual address space layout.

Joint TLB

For fast virtual-to-physical address decoding, the R4000 uses a large, fully associative TLB which maps 96 Virtual pages to their corresponding physical addresses. The TLB is organized as 48 pairs of even-odd entries, and maps a virtual address and address space identifier into the large, 64gB physical address space.

Two mechanisms are provided to assist in controlling the amount of mapped space, and the replacement characteristics of various memory regions. First, the page size can be configured, on a per-entry basis, to map a page size of 4KB to 16MB (in multiples of 4). A CP0 register is loaded with the page size of a mapping, and that size is entered into the TLB when

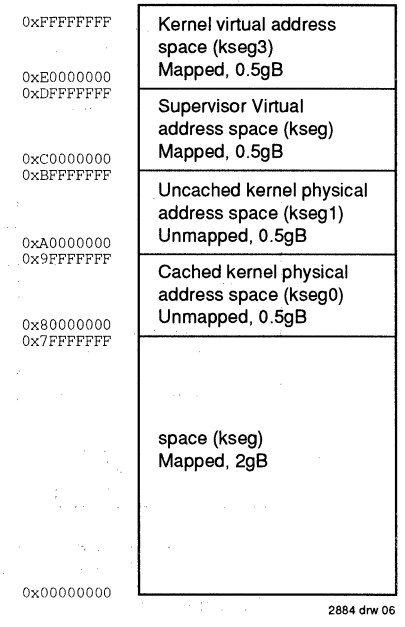


Figure 5. Kernel Mode Virtual Addressing (32-bit mode)

a new entry is written. Thus, operating systems can treat various regions of memory distinctly from applications programs and data files: for example, a typical frame buffer can be memory mapped using only one TLB entry.

The second mechanism controls the replacement algorithm when a TLB miss occurs. The R4000 uses a Random Replacement algorithm to select a TLB entry to be written with a new mapping; however, the processor provides a mechanism whereby a system specific number of mappings can be locked into the TLB, and thus avoid being randomly replaced. This facilitates the design of real-time systems, by allowing deterministic access to critical software.

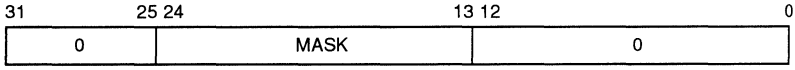
The joint TLB also contains information to control the cache coherency protocol for each page. Specifically, each page has attribute bits to determine whether the coherency algorithm is: uncached, noncoherent, sharable, exclusive, or update. The use of these attributes, coupled with state information in the processor caches, enables a wide variety of multi-processing strategies to be easily implemented.

Figure 6 shows the format of the TLB entry and registers used to control the TLB.

Instruction TLB

The R4000 also incorporates a 2-entry instruction TLB. Each entry maps a 4KB page. The instruction TLB improves performance by allowing instruction address translation to occur in parallel with data address translation. When a miss occurs on an instruction address translation, the ITLB is filled from the JTLB. The operation of the ITLB is invisible to the user.

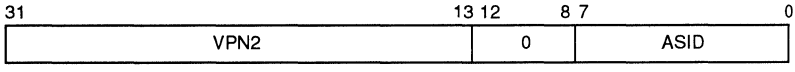
PageMask Register



MASK Page comparison mask

0 Reserved. Must be written as zero; returns zero when read.

EntryHi Register

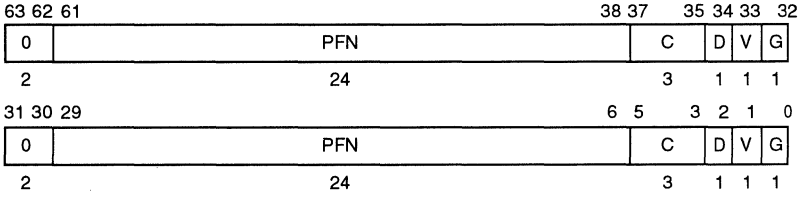


VPN2 Virtual Page Number divided by two (maps to two pages)

ASID Address Space ID field. An 8-bit field which lets multiple processes share the TLB while each process has a distinct mapping of otherwise identical virtual page numbers. This is the same ASID described at the beginning of this chapter.

0 Reserved. Must be written as zero; returns zero when read.

EntryLo0 & EntryLo1



PFN Page Frame Number. Upper bits of the physical address.

C Specifies the cache algorithm to be used.

D Dirty. If this bit is set, the page is marked as dirty and, therefore, writable. This bit is actually a write-protect bit that software can use to prevent alteration of data.

V Valid. If this bit is set, it indicates that the TLB entry is valid; otherwise, a TLBL or TLBS Miss occurs.

G Global. If this bit is set in both Lo0 and Lo1, then ignore the ASID.

0 Reserved. Must be written as zero; returns zero when read.

2844 drw 07

Figure 6. Fields of an R4000 TLB Entry

Register File

The R4000 has thirty-two general purpose registers. These registers are used for scalar integer operations and address calculation. The register file consists of two read ports and one write port, and uses bypassing to enable the reading and writing of the same regist•er twice per cycle as well as to minimize the operation latency in the pipeline.

ALU

The R4000 ALU consists of the integer adder and logic unit. The adder performs address calculations in addition to arithmetic operations, and the logic unit performs all shift operations. Each of these units is highly optimized and can perform an operation in a single superpipeline cycle.

Integer Multiplier/Divider

The R4000 integer multplier and divider units perform signed and unsigned multiply and divide operations and execute instructions in parallel with the ALU. The results of the operation are placed in the *MDHI* and *MDLO* registers. The values can then be transferred to the general purpose register file using the MFHI/MFLO instructions. The following table shows the number of processor internal cycles required between a 32-bit integer multiply or divide and a subsequent MFHI or MFLO operation, in order that no interlock or stall occurs.

Operation	Single Word	Double Word
MULT	10	20
DIV	69	133

2884 tbl 01

FLOATING-POINT UNIT

The R4000 incorporates an entire floating-point unit on chip, including a floating-point register file and execution unit. The floating-point unit forms a "seamless" interface with the integer unit, decoding and executing instructions in parallel with the integer unit.

Floating-point Co-Processor

The R4000 floating-point execution unit supports single and double precision arithmetic, as specified in the IEEE Standard 754. The execution unit is broken into separate multiply, divide, and add/convert/square root units, which allow for overlapped operations. The multiplier is pipelined, allowing a new multiply to begin every 4 cycles.

As in the IDT79R2010 and IDT79R3010, the R4000 maintains fully precise floating-point exceptions while allowing both overlapped and pipelined operations. Precise exceptions are extremely important in mission-critical environments, such as ADA, and highly desirable for debugging in any environment.

The floating-point unit's operation set includes floating-point add, subtract, multiply, divide, square root, conversion between fixed-point and floating-point format, conversion among floating-point formats, and floating-point compare. Thes operations comply with the IEEE Standard 754.

The following table gives the latencies of some of the floating-point instructions in internal processor cycles.

Operation	Single Precision	Double Precision
ADD	4	4
SUB	4	4
MUL	7	8
DIV	23	36
SQRT	54	112
CMP	3	3
FIX	4	4
ROUND	4	4
TRUNC	4	4
FLOAT	5	5
ABS	2	2
MOV	1	1
NEG	2	2
LWC1,LDC1	3	3
SWC1,SDC1	1	1

2884 tbl 02

Floating-Point General Register File

The floating-point register file is made up of sixteen 64-bit registers which can also be viewed as thirty-two 32-bit floating-point registers. The MIPS architecture supports a coprocessor load and store double so, when configured as 64-bit registers, the floating-point unit can take advantage of the 64-bit wide data cache and issue a co-processor load or store a doubleword instruction in every cycle.

Floating-Point Control Register File

The floating-point control registers contain a register for determining configuration and revision information for the coprocessor and control and status information. These are primarily involved with diagnostic software, exception handling, state saving and restoring, and control of rounding modes.

CACHE MEMORY

In order to keep the R4000's high-performance superpipeline full and operating efficiently, the R4000 incorporates on-chip instruction and data caches. Each cache has its own 64-bit data path that can be accessed twice a cycle, so the instruction and data caches can be accessed in parallel with full pipelining. Combining this feature with a pipelined, single master clock cycle access of each cache, the cache subsystem provides the integer and floating-point units with an aggregate bandwidth of 2GB per second at a system clock frequency of 75MHz.

Instruction Cache

The IDT79R4000 incorporates a direct-mapped on-chip instruction cache. This virtually indexed, physically tagged

cache is 8KB in size and is protected with byte parity. The R4400 doubles the on-chip instruction cache to 16KB.

Because the cache is virtually indexed, the virtual-to-physical address translation occurs in parallel with the cache access, thus further increasing performance by allowing these two operations to occur simultaneously. The tag holds a 24-bit physical address and valid bit, and is parity protected.

The instruction cache is 64-bits wide, and can be refilled or accessed twice per master clock cycle, although the current IDT79R4000 CPU fetches on 32-bit unit/master cycle for a peak instruction bandwidth of 400MB/sec. The line size can be configured as four or eight words to allow different applications to have a line size that delivers optimum performance.

Data Cache

For fast, single cycle data access, the IDT79R4000 includes an 8KB on-chip data cache. The R4400 doubles the on-chip instruction cache to 16KB.

The data cache is protected with byte parity and its tag is protected with a single parity bit. It is virtually indexed and physically tagged to allow simultaneous address translation and data cache access.

The Data Cache is direct mapped, and its line size can be configured as four or eight words. The write policy is writeback, which means that a Store to a cache line does not immediately cause memory to be updated. This increases system performance by reducing bus traffic and eliminating the bottleneck of waiting for each Store operation to finish before issuing a subsequent memory operation.

Associated with the Data Cache is the store buffer. When the R4000 executes a Store instruction, this 2-entry buffer gets written with the store data while the tag comparison is performed. If the tag matches, then the data gets written into the Data Cache in the next cycle that the Data Cache is not accessed. The store buffer allows the R4000 to execute two stores per master cycle and to perform back-to-back stores without penalty. Likewise, the R4000 can perform two loads or a load and store per master cycle without penalty, yielding 1.2GB/sec bandwidth without restrictions on instruction combinations.

When the Data Cache line does need to be written back to slower memory (either secondary cache or main memory), the processor writes the data to an internal write buffer which can hold a line (4 or 8 words) of data. By writing the data to the fast write buffer, the processor can continue executing instructions without having to wait until the write completes to the slower memory.

The IDT79R4000 caches are designed for easy and flexible integration in many types of multiprocessor systems. The Data Cache contains all the necessary state bits to allow the R4000 to maintain cache coherency across all R4000 processors in a system.

SECONDARY CACHE INTERFACE

The R4000/R4400SC and R4400MC support a secondary cache that can range in size from 128KBs to 4MBs. The cache can be configured as a unified cache or split into an instruction cache and a data cache, and it can be designed using industry standard SRAMs. The IDT R4000 provides all of the secondary cache control circuitry on chip, including ECC.

The secondary cache interface consists of a 128-bit data bus, a 25-bit tag bus, and 18-bit address bus, and SRAM control signals. The wide data bus improves performance by providing a high bandwidth data path to fill the primary caches. ECC check bits are added to both the data and tag buses to improve data integrity. All double-bit errors can be detected and all single bit-errors can be detected and all single bit-errors can be corrected on both buses.

The secondary cache access time is configurable, providing system designers with the flexibility to tailor the cache design to specific applications. The line size of the secondary cache is also configurable and can be 4, 8, 16, or 32 words. The line size of the primary cache must always be less than or equal to the line size of the secondary cache.

The secondary cache is physically tagged and physically indexed. The physical cache prevents problems that could arise due to virtual address aliasing. Also, a physical cache makes multiprocessing cache coherency protocols easier to implement. The R4400MC provides a set of cache states and a mechanism for manipulating the contents and state of the

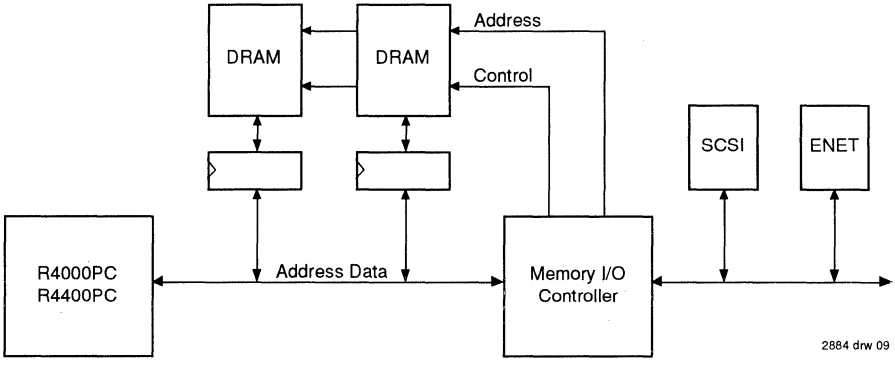


Figure 7. Typical Desktop System Block Diagram

cache, which are sufficient to implement a variety of cache coherency protocols, using either bus snooping or directory based schemes.

SYSTEM INTERFACE

The R4000 supports a 64-bit system interface that can be used to construct systems as simple as a uniprocessor with a direct DRAM interface and no secondary cache or as sopisticated as a fully cache coherent multiprocessor. The interface consists of a 64-bit Address/Data bus with 8 check bits and a 9-bit command bus protected with parity. In addition, there are 8 handshake signals. The interface has a simple timing specification and is capable of transferring data between the processor and memory at a peak rate of 600MB/sec at 75MHz.

Figure 7 shows a typical desktop system using the R4000PC. Similarly, a high-performance desktop workstation/server system can be built using the IDT79R4000SC and adding a secondary cache.

The system interface allows the processor to access external resources in order to satisfy cache misses and uncached operations. The IDT79R4000MC, in addition to handling simple memory and I/O transactions, supports a number of cache coherency transactions of sufficient generality to support a variety of cache coherent multiprocessing models. In particular, the interface is designed to support both bus snooping and directory based multiprocessor models and supports both write-update and write-invalidate coherency protocols.

Figure 8 shows a typical multiprocessor system using the IDT79R4000MC, an interface agent, and a secondary cache.

System Address/Data Bus

The 64-bit System Address Data (SysAD) bus is used to transfer addresses and data between the R4000 and the rest of the system. It is protected with an 8-bit check bus, SysADC. The check bits can be configured as either parity or ECC, for flexibility in interfacing to either parity or ECC memory systems.

The system interface is configurable to allow easier interfacing to memory and I/O systems of varying frequencies. The data rate and the bus frequency at which the R4000 transmits data to the system interface are programmable via boot time mode control bits. Also, the rate at which the processor receives data is fully controlled by the external device. Therefore, either a low cost interface requiring no write buffering or a fast, high performance interface can be designed to communicate with the R4000. Again, the system designer has the flexibility to make these price/perfomance tradeoffs.

System Command Bus

The R4000 interface has a 9-bit System Command (SysCmd) bus. The command bus indicates whether the SysAD bus carries an address or data. If the SysAD carries an address, then the SysCmd bus also indicates what type of transaction is to take place (for example, a read or write). If the SysAD carries data, then the SysCmd bus also gives information about the data (for example, this is the last data word transmitted, or the cache state of this line of data is clean exclusive). The SysCmd bus is bidirectional to support both processor requests and external requests to the R4000. Processor requests are initiated by the R4000 and responded to by an external device. External requests are issued by an external device and require the R4000 to respond.

The R4000 supports byte, halfword, tribyte, word, doubleword, and block transfers on the SysAD bus. In the case of a sub-doubleword transfer, the low-order 3 address bits gives the byte address of the transfer, and the SysCmd bus indicates the number of bytes being transferred.

Handshake Signals

There are eight handshake signals on the system interface. Two of these, $\overline{\text{RdRdy}}$ and $\overline{\text{WrRdy}}$ are used by an external device to indicate to the IDT79R4000 whether it can accept a new read or write transaction. The IDT79R4000 samples these signals before deasserting the address on read and write requests.

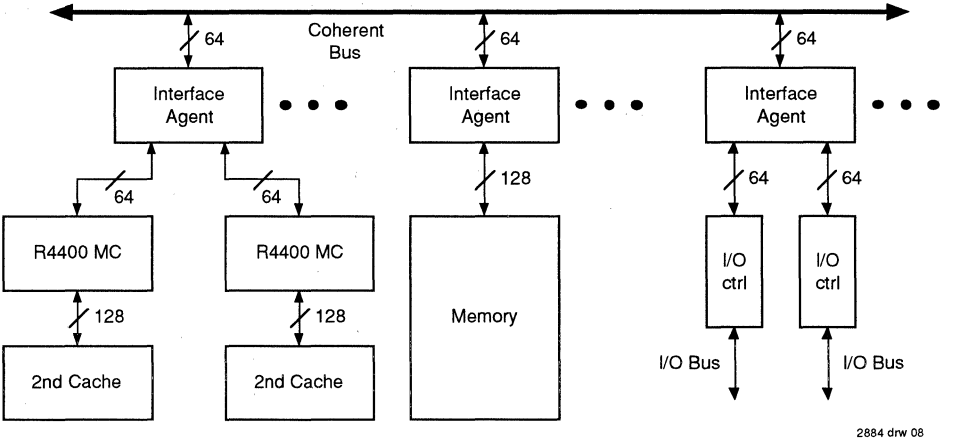


Figure 8. Multiprocessor System Using the R4400 MC

ExtRqst and Release are used to transfer control of the SysAD and SysCmd buses between the processor and an external device. When an external device needs to control the interface, it asserts ExtRqst. The IDT79R4000 responds by asserting Release to release the system interface to slave state.

ValidOut and ValidIn are used by the IDT79R4000 and the external device respectively to indicate that there is a valid command or data on the SysAD and SysCmd buses. The R4000 asserts ValidOut when it is driving these buses with a valid command or data, and the external device drives ValidIn when it has control of the buses and is driving a valid command or data.

Finally, there are two signals that are available on the MC version only and are used in multiprocessing systems. They are IvdAck and IvdErr, and they are driven by an external device to indicate the completion status of the current processor invalidate or update request.

R4000 Requests

The R4000 is capable of issuing requests to a memory and I/O subsystem. The system interface supports two modes of operation:

- Secondary Cache mode
- No Secondary Cache mode

No Secondary Cache Mode

The R4000 without a secondary cache requires a non-overlapping system interface. This means that only one processor request may be outstanding at a time and that the request must be serviced by an external device before the R4000 issues another request. The R4000PC can issue read and write requests to an external device, and an external device can issue read and write requests to the R4000.

Figure 9 shows a processor read request. The R4000 asserts ValidOut and simultaneously drives the address and read command on th SysAD and SysCmd buses. If the system interface has RdRdy asserted, then the processor tristates its drivers and releases the system interface to slave state by asserting Release. The external device can then begin sending the data to the IDT79R4000.

Secondary Cache Mode

The R4000 with a secondary cache operates in an overlapping bus transfer mode in which multiple system interface transactions may be issued in parallel. The processor may issue a combination of read request, an update or invalidate request, and a write request. For instance, when a dirty cache line needs to be replaced, the processor issues a read request immediately followed by a write request, without waiting for the read data to return. This has the advantage of "hiding" the write transaction between the read request and read response, thus increasing overall system performance. This mode of operation is not necessary or useful in R4000 systems without secondary cache since the processor contains a write buffer capable of accepting an entire primary cache line of data. Overlapping is a superset of non-overlapping systemoperation.

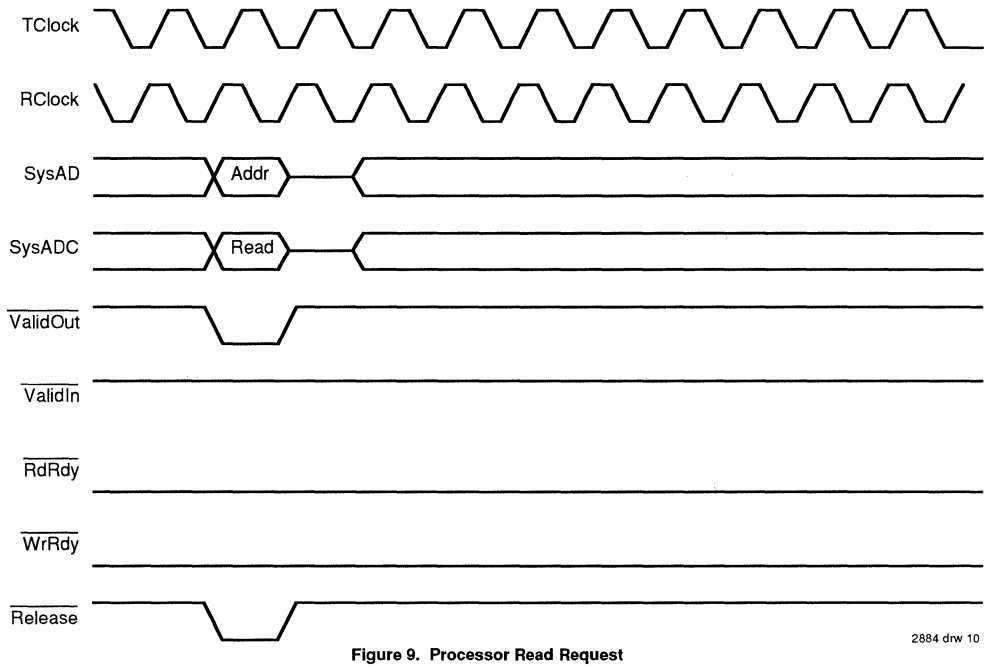


Figure 9. Processor Read Request

Figure 10 illustrates a processor request in overlap mode. This request is made up of a read, invalidate, and write request. Note that the protocol for the read, the invalidate, and the write are all similar to each other, with the exception that the processor also sends out valid data during the write request. In Figure 10 the processor write transaction not only occurs before the read response from the external device, but it also illustrates how an external device can hold off a write request through the deassertion of $\overline{\text{WrRdy}}$.

External Requests

The R4000 responds to requests issued by an external device. The requests can take several forms. An external device may need to supply data in response to an R4000 read request or it may need to gain control over the system interface bus to access other resources which may be on that bus. It also may issue cache coherency requests to the processor, such as a request for the R4000 to update, invalidate, or snoop upon its caches, or to supply a cache line of data. Additionally, an external device may need to write to the R4000 interrupt register.

The following is a list of the supported external requests:

- Read
- Write
- Invalidate
- Update
- Snoop
- Intervention
- Null

Figure 11 shows an example of an external snoop request. The process by which the external device issues the request is very similar to the way the R4000 issues a request. The external device first gains ownership of the system interface by asserting $\overline{\text{ExtRqst}}$ and waiting for the R4000 to assert $\overline{\text{Release}}$. The external device then sends in a valid command by asserting $\overline{\text{ValidIn}}$ and driving the SysCmd and SysAD buses with the snoop command and address. The R4000 responds to the request by asserting $\overline{\text{ValidOut}}$ and driving the SysCmd bus with the cache state of the snooped upon line.

CACHE COHERENCY CAPABILITY

With the IDT79R4400MC, cache coherence is maintained in hardware. The system control coprocessor permits the specification of different caching protocols on a per-page basis. A page may be:

- uncached
- cached but non-coherent
- cached and coherent exclusive (only one processor cache contains the data on loads and stores).
- cached and coherent exclusive on writes (write invalidate scheme-only one processor cache contains the data when that datum is written to).
- cached and coherent with updates on writes (write-update scheme).

Depending upon the amount and type of data sharing in an application, the operating system can choose the most appropriate caching strategy.

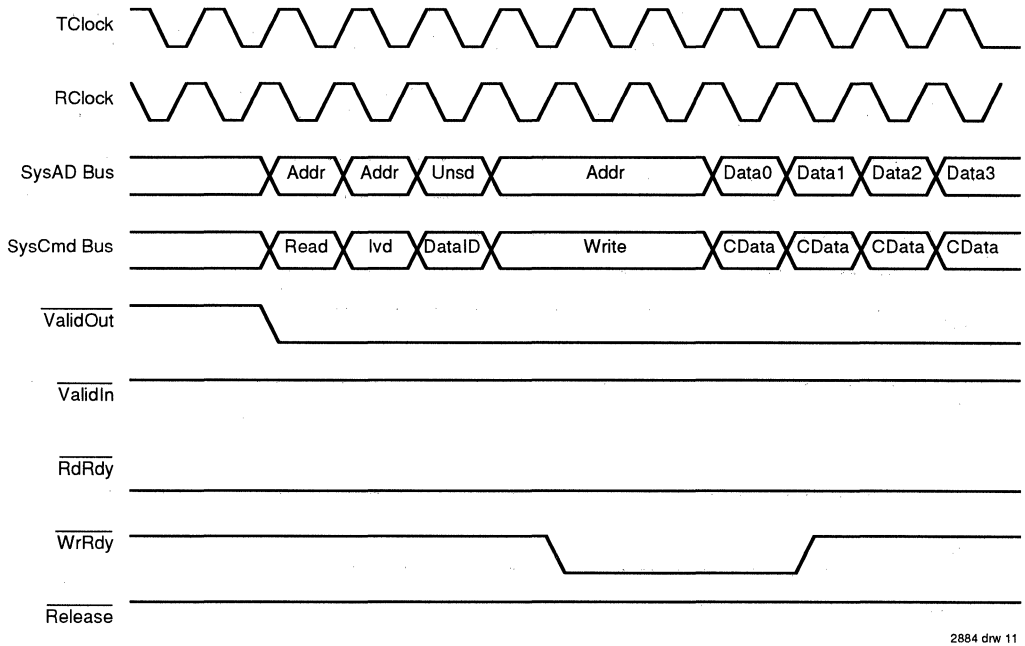


Figure 10. Processor Read, Invalidate, Write Request

Support for processor synchronization is provided by the Load Linked and Store Conditional instructions. The Load Linked and Store Conditional instructions:

1. Provide a simple mechanism for generating all of the common synchronization primitives including test-and-set, bit-level locks, semaphores, counters, sequencers, etc. with no additional hardware overhead.
2. Operate in such a fashion that bus traffic is only generated when the state of the cache line changes.
3. Need not lock a system bus—a very important feature for larger systems.

ADVANCED FEATURES

The R4000 supports a number of other capabilities in addition to the standard processor model described above. Many of these capabilities are selected by the system designer during the processor reset sequence, via the boot time mode control interface. Features are included to support fault tolerance, system test, or other system environments.

Boot Time Options

Fundamental operational modes for the processor are initialized by the boot-time mode control interface. The boot-time mode control interface is a serial interface operating at a very low frequency (Master clock divided by 256). The low frequency operation allows the initialization information to be kept in a low cost EPROM.

Immediately after the VCCOk Signal is asserted, the processor reads a serial bit stream of 256 bits to initialize all fundamental operational modes. After initialization is complete, the processor continues to drive the serial clock output, but no further initialization bits are read.

JTAG INTERFACE

The JTAG boundary scan mechanism provides a capability for testing the interconnect between the IDT79R4000 processor, the printed circuit board to which it is attached, and the other components on the board. In addition the JTAG boundary scan mechanism provides a rudimentary capability for low-speed logical testing of the secondary cache RAMs. The JTAG boundary scan mechanism does not provide any capability for testing the R4000 processor itself.

In accordance with the JTAG specification the R4000 processor contains a TAP controller, JTAG instruction register, JTAG boundary scan register, JTAG identification register, and JTAG bypass register. However, the R4000 JTAG implementation provides only the *external test* functionality of the boundary scan register.

FAULT TOLERANT SUPPORT

The R4000 has been designed to support varying models of fault tolerance. These modes include: master/checker operation and triple-modular redundancy. In addition to explicit fault-tolerant modes of operation, the design of internal processor operation is such to support processor synchronization; for example, both the TLB random replacement algorithm, and the on-chip timer, can be forced to known states via software. Thus, the IDT R4000 family can be used to build "non-stop" machines across a number of different system models.

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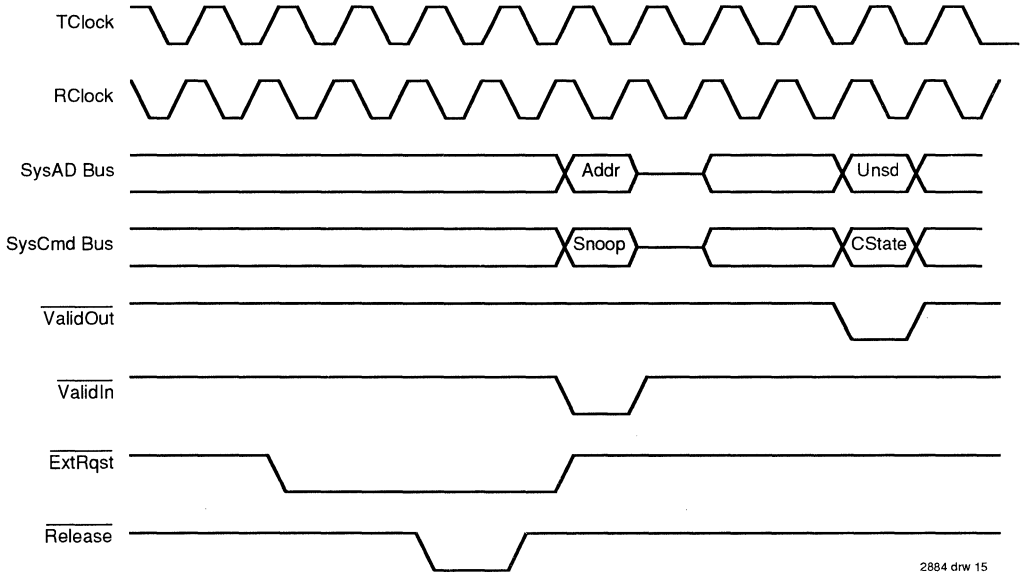

Figure 11. External Snoop Request

BOOT-TIME MODES

Serial Bit	Value	Mode Setting
0		**BlkOrder**: Block read response ordering.
	0	Sequential ordering.
	1	Sub-block ordering.
1		**EIBParMode:** System interface check bus checking.
	0	SECDED error checking and correcting mode.
	1	Byte parity.
2		**EndBit:** Byte ordering.
	0	Little Endian.
	1	Big Endian.
3		**DShMdDis:** Dirty shared mode, enables transition to dirty shared state on processor update successful.
	0	Dirty Shared Enabled.
	1	Dirty Shared Disabled.
4		**NoSCMode:** Specifies presence of secondary cache.
	0	Present.
	1	Not Present.
5:6		**SysPort:** System Interface port width (Bit 6 Most Significant).
	0	64 bits.
	1-3	Reserved(1)
7		**SC64BitMd:** Secondary cache interface port width.
	0	128 bits.
	1	Reserved(1)
8		**EISpltMd:** Secondary cache organization
	0	Unified
	1	Reserved(1)
9:10		**SCBlkSz:** Secondary cache line size (Bit 10 Most Significant).
	0	4 words.
	1	8 words.
	2	16 words.
	3	32 words.
11:14		**XmitDatPat:** System Interface Data Rate (Bit 14 Most Significant).
	0	D
	1	DDx
	2	DDxx
	3	DxDx
	4	DDxxx
	5	DDxxxx
	6	DxxDxx
	7	DDxxxxxx
	8	DxxxDxxx
	9-15	Reserved(1)
15:17		**SysCkRatio:** PClock to SClock divisor: frequency relationship between SClock, RClock, and TClock and PClock (Bit 17 MostSignificant).
	0	Divide by 2
	1	Divide by 3
	2	Divide by 4
	3-7	Reserved(1)
18	0	Reserved (Required value)
19		**TimIntDis:** Timer Interrupt enable allows timer interrupts, otherwise the interrupt used by the timer becomes a general-purpose interrupt.
	0	Enabled
	1	Disabled
20		**PotUpdDis:** Potential invalidate enable (allows potential invalidates to be issued. Otherwise only normal invalidates are issued).
	0	Enabled
	1	Disabled

2884 tbl 03

Serial Bit	Value	Mode Setting
21:24		**TWrSUp:** Secondary cache write deassertion delay, TWrSup in PCycles (Bit 24 Most Signifi cant).
	0-2	Undefined
	3-15	Mumber of PCLK cycles (Min 3; Max 15)
25:26		**TWr2Dly:** Secondary cache write assertion delay 2, TWrDly in PCycles (Bit 26 Most Signifi cant).
	0	Undefined
	1-3	Number of PCLK cycles (Min 1; Max 3)
27:28		**TWr1Dly:** Secondary cache write assertion delay 1, TWrDly in PCycles (Bit 28 Most Signifi cant).
	0	Undefined
	1-3	Number of PCLK cycles (Min 1; Max 3)
29		**TWrRc:** Secondary cache write recovery time, TWrRc in PCycles either 0 or 1 cycles.
	0	0 cycle
	1	1 cycle
30:32		**TDis:** Secondary cache disable time, TDis in PCycles (Bit 32 Most Significant).
	0	Undefined
	1	Number of PCLK cycles (Min 2; Max 7)
33:36		**TRd2Cyc:** Secondary cache read cycle time 2, TRdCyc2 in PCycles (Bit 36 Most Significant).
	0-2	Undefined
	3-15	Number of PCLK cycles (Min 3; Max 15)
37:40		**TRd2Cyc:** Secondary cache read cycle time 1, TRdCyc1 in PCycles, (Bit 40 Most Significant).
	0-3	Undefined
	4-15	Number of PCLK cycles (Min 4; Max 15)
41:45[2]	0	Reserved.
46		**Pkg179:** R4000 type.
	0	Large (447 pin). SC/MC
	1	Small (179). PC
47:49		**CycDivisor:** This mode determines the clock divisior for the reduced power mode. When the RP bit in the Status Register is set to one, the pipeline clock is divided by one of the following values (Bit 49 is Most Significant).
	0	Divide by 2
	1	Divide by 4
	2	Divide by 8
	3	Divide by 16
	4-7	Reserved[1]
50:52		**Drv0_50, Drv0_75, Drv1_00:** Drive the outputs in N x MasterClock period (Bit 52 Most Significant) .
	0-1	Drive at 0.5 x MasterClockperiod.
	2-3	Drive at 0.75 x MasterClock period.
	4-7	Drive at 1.0 x MasterClock period.
53:56		**InitP:** Initial values for the state bits that determine the pull-down di/dt and switching speed of the output buffers (Bit 53 Most Significant).
	0	Fastest pull-down rate.
	1-14	Intermediate pull-down rate.
	15	Slowest pull-down rate.
57:60		**InitN:** Initial values for the state bits that determine the pull-up di/dt and switching speed of the output buffers (Bit 57 Most Significant).
	0	Slowest pull-up rate.
	1-14	Intermediate pull-up rates.
	15	Fastest pull-up rate.
61		**EnbIDPLLR:** Enables the negative feedback loop that determines the di/dt and switching speed of the output buffers only during ColdReset.
	0	Disable di/dt control mechanism.
	1	Enable di/dt control mechanism.

2884 tbl 04

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Serial Bit	Value	Mode Setting
62		**EnbIDPLL:** Enables the negative feedback loop that determines the di/dt and switching speed of the output buffers during ColdReset and during normal operation.
	0	Disable di/dt control mechanism.
	1	Enable di/dt control mechanism.
63		**DsbIDPLL**: Enables PLLs that match MasterIn and produce RClock, TClock, SClock and the internal clocks.
	0	Enable PLLs.
	1	Disable PLLs.
64		**SRTristate:** Controls when output-only pins are trestated
	0	Only whe $\overline{\text{ColdReset}}$ is asserted.
	1	When $\overline{\text{Reset}}$ or $\overline{\text{ColdReset}}$ are asserted
65-255	0[2]	Reserved (must be scanned in as zeros).

2884 tbl 05

NOTES:
1. Selecting a Reserved value results in undefined processor behavior.
2. 0's must be presented for these reserved values.

PIN DESCRIPTION

The following is a list of interface, interrupt, and maintenance pins available on the different package configurations.

Pin Name	Type	Description
Secondary cache interface pins available *only* on the SC and MC configuration:		
SCAddr(17:1)	Output	Secondary cache address bus A 17-bit address bus for the secondary cache.
SCAddr0(W:Z)	Output	Secondary cache address lsb To minimize loading effect, there are 4 identical copies of this signal.
SCAPar(2:0)	Output	Secondary cache address parity bus A 3-bit bus that carries the parity of the SCAddr bus and the cache control lines $\overline{SCOE}$, $\overline{SCWR}$, $\overline{SCDCS}$ and $\overline{SCTCS}$.
SCData(127:0)	Input/Output	Secondary cache data bus A 128-bit bus used to read or write cache data from/to the secondary cache.
SCDChk(15:0)	Input/Output	Secondary cache data ECC bus A 16-bit bus that carries two 8-bit ECC fields that covers the 128 bits of the SCData from/to the secondary cache. SCDChk(15:8) corresponds to SCData(127:64) and SCDChk(7:0) corresponds to SCData(63:0).
$\overline{SCDCS}$	Output	Secondary cache data chip select Chip select enable signal for the secondary cache Ram associated with SCData and SCDChk.
$\overline{SCOE}$	Output	Secondary cache output enable Output enable for the secondary cache RAM.
SCTag(24:0)	Input/Output	Secondary cache tag bus A 25-bit bus used to read or write cache tags from/to the secondary cache.
SCTChk(6:0)	Input/Output	Secondary cache tag ECC bus A 7-bit bus that carries an ECC field covering the SCTag from/to the secondary cache.
$\overline{SCTCS}$	Output	Secondary cache tag chip select Chip select enable signal for the secondary cache tag RAM associated with SCTag and SCTChk.
$\overline{SCWr}$(W:Z)	Output	Secondary Cache write enable Write enable for the secondary cache RAM.
System interface pins available on all parts:		
$\overline{ExtRqst}$	Input	External request Signals that the system interface needs to submit an external request.
$\overline{Release}$	Output	Release interface Signals that the processor is releasing the system interface to slave state
$\overline{RdRdy}$	Input	Read Ready Signals that an external agent can now accept a processor read, invalidate, or update request in both secondary cache and no secondary cache mode or can accept a read followed by a write request in secondary cache mode.
SysAD(63:0)	Input/Output	System address/data bus A 64-bit address and data bus for communication between the processor and an external agent.
SysADC(7:0)	Input/Output	System address/data check bus An 8-bit bus containing check bits for the SysAD bus.
SysCmd(8:0)	Input/Output	System command/data identifier bus A 9-bit bus for command and data identifier transmission between the processor and an external agent.
SysCmdP	Input/Output	System command/data identifier bus parity A single, even-parity bit for the SysCmd bus.
$\overline{ValidIn}$	Input	Valid Input Signals that an external agent is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.

2884 tbl 06

Pin Name	Type	Description
$\overline{\text{ValidOut}}$	Output	Valid output Signals that the processor is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
$\overline{\text{WrRdy}}$	Input	Write Ready Signals that an external agent can now accept a processor write request in both non-overlap and overlap mode.
System interface pins available only on the MC configuration.		
$\overline{\text{IvdAck}}$	Input	Invalidate acknowledge Signals successful completion of a processor invalidate or update request.
$\overline{\text{IvdErr}}$	Input	Invalidate error Signals unsuccessful completion of a processor invalidate or update request.
Interrupt pins available only on the PC configuration:		
$\overline{\text{Int(5:1)}}$	Input	Interrupt Five of six general processor interrupts, bit-wise ORed with bits 5:1 of the interrupt register.
Interrupt pin available on all devices:		
$\overline{\text{Int(0)}}$	Input	Interrupt One of six general processor interrupts, bit-wise ORed with bit 0 of the interrupt register.
Non-maskable interrupt pin available on all devices:		
$\overline{\text{NMI}}$	Input	Non-maskable interrupt Non-maskable interrupt, ORed with bit 6 of the interrupt register.
Boot-time mode control interface pins available on all devices:		
ModeClock	Output	Boot mode clock Serial boot-mode data clock output at the system clock frequency divided by two hundred and fifty six.
ModeIn	Input	Boot mode data in Serial boot-mode data input.
JTAG interface pins available on all devices:		
JTDI	Input	JTAG data in JTAG serial data in.
JTCK	Input	JTAG clock input JTAG serial clock input.
JTDO	Output	JTAG data out JTAG serial data out.
JTMS	Input	JTAG command JTAG command signal, signals that the incoming serial data is command data.
Maintenance pins available on all devices:		
IOOut	Output	I/O output Output slew rate control feedback loop output. Must be connected to IOIn through a delay loop that models the IO path from the R4000 to an external agent.
IOIn	Input	I/O input Output slew rate control feedback loop input (see IOOut).
MasterClock	Input	Master clock Master clock input at the processor operating frequency.
MasterOut	Output	Master clock out Master clock output aligned with MasterClock.
RClock(1:0)	Output	Receive clocks Two identical receive clocks at the system interface frequency.
SyncOut	Output	Synchronization clock out Synchronization clock output. Must be connected to SyncIn through an interconnect that models the interconnect between MasterOut, TClock, RClock, and the external agent.

2884 tbl 07

Pin Name	Type	Description
SyncIn	Input	Synchronization clock in Synchronization clock input. See SyncOut.
TClock(1:0)	Output	Transmit clocks Two identical transmit clocks at the system interface frequency.
VCCOk	Input	VCC is OK When asserted, this signal indicates to the R4000 that the +5 volt power supply has been above 4.75 volts for more than 100 milliseconds and will remain stable. The assertion of VCCOk initiates the reading of the boot-time mode control serial stream.
$\overline{\text{ColdReset}}$	Input	Cold reset This signal must be asserted for a power on reset or a cold reset. The clocks SClock, TClock, and RClock begin to cycle and are synchronized with the de-assertion edge of $\overline{\text{ColdReset}}$. $\overline{\text{ColdReset}}$ must be de-asserted synchronously with MasterOut.
$\overline{\text{Reset}}$	Input	Reset This signal must be asserted for any reset sequence. It may be asserted synchronously or asynchronously for a cold reset, or synchronously to initiate a warm reset. $\overline{\text{Reset}}$ must be de-asserted synchronously with MasterOut.
$\overline{\text{Fault}}$	Output	Fault Mismatch output of boundary comparators.
VccP	Input	Quiet VCC for PLL Quiet Vcc for the internal phase locked loop.
VssP	Input	Quiet VSS for PLL Quiet Vss for the internal phase locked loop.
Maintenance pins available only on the SC and MC configurations:		
Status(7:0)	Status	Output An 8-bit bus that indicates the current operation status of the processor.

2884 tbl 08

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ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_C	Operating Temperature	0 to +85 (Case)	°C
T_{BIAS}	Case Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

2884 tbl 09

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN} minimum = -3.0V for pulse width less than 15ns. V_{IN} should not exceed Vcc +0.5 Volts.
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

RECOMMENDED OPERATION TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Commercial	0°C to +85°C (Case)	0V	5.0 ±5%

2884 tbl 10

DC ELECTRICAL CHARACTERISTICS—COMMERCIAL TEMPERATURE RANGE

(Vcc = 5.0V ± 5%; Tcase = 0°C to +85°C)

			50MHz		67MHz		75MHz		
Symbol	Parameter	Conditions	Min.	Max.	Min.	Max.	Min.	Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = –4mA	3.5	—	3.5	—	3.5	—	V
V_{OHC}	Output HIGH Voltage (MasterOut, TClock, RClock, SyncOut)(3)	I_{OH} = –4mA	4.0	—	4.0	—	4.0	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 4mA	—	0.4	—	0.4	—	0.4	V
V_{IH}	Input HIGH Voltage		2.0	Vcc + .5	2.0	Vcc + .5	2.0	Vcc + .5	V
V_{IL}	Input LOW Voltage(1,2)		–0.5(1)	0.8	–0.5(1)	0.8	–0.5(1)	0.8	V
V_{IHC}	Input HIGH Voltage (MasterClock, SyncIn)		0.8 Vcc	Vcc + .5	0.8 Vcc	Vcc + .5	0.8 Vcc	Vcc + .5	V
V_{ILC}	Input LOW Voltage (MasterClock, SyncIn)		–0.5(1)	0.2 Vcc	–0.5(1)	0.8 Vcc	–0.5(1)	0.8 Vcc	V
C_{In}	Input Capacitance		—	10	—	10	—	10	pF
C_{Out}	Output Capacitance		—	10	—	10	—	10	pF
I_{Leak}	Input Leakage		—	10	—	10	—	10	µA
I_{OLeak}	Input/Output Leakage		—	20	—	20	—	20	µA
I_{CC}	Operating Current	Vcc = 5.5V, Tc=0°C	—	3.0	—	4.0	—	TBD	A

2884 tbl 11

NOTES:
1. V_{IL} (min.) = -3.0V for pulse width less than 15ns.
2. Except for MasterClock input.
3. Applies to TClock, RClock, MasterOut, and ModeClock outputs.

AC ELECTRICAL CHARACTERISTICS—COMMERCIAL TEMPERATURE RANGE

(Vcc=5.0V ± 5%; Tcase = 0°C to +85°C) MasterClock and Clock Parameters[2]

Symbol	Parameter	Conditions	50MHz		67MHz		75MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
TMCkHigh	MasterClock High	[3]	4	—	3	—	3	—	ns
TMCkLow	MasterClock Low	[3]	4	—	3	—	3	—	ns
	MasterClock Freq[1]		25	50	25	67	25	75	MHz
TMCP	MasterClock Period		20	40	15	40	13.3	40	ns
TMCJitter	Clock Jitter (on RClock, TClock, MasterOut, SyncOut)		—	±500	—	±500	—	±500	ps
TMCRise	MasterClock Rise Time		—	5	—	4	—	3.5	ns
TMCFall	MasterClock Fall Time		—	5	—	4	—	3.5	ns
TModeCKP	ModeClock Period		—	256*TMCP	—	256*TMCP	—	256*TMCP	ns
TJTAGCKP	JTAG Clock Period		4*TMCP	—	4*TMCP	—	4*TMCP	—	ns

NOTES:

2884 tbl 12

1. Operation of the R4000 family is only guaranteed with the phase lock loop enabled.
2. Capacitive load for all output timings is 50pF. Deration is per CLD specification.
3. Transition ≤ 5ns for 50, 67MHz; transition ≤ 3.5ns for 75MHz.

SYSTEM INTERFACE PARAMETERS

Symbol	Parameter	Conditions	50MHz		67MHz		75MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
TDO[1,2,3]	Data Output	Max Slew Rate Modebits[53:56] = 0 Modebits[57:60] = 15	3.5	10	2	7	2	7	ns
		Min Slew Rate Modebits[53:56] = 15 Modebits[57:60] = 0	6	16	6	12	6	12	ns
TDS	Data Setup		5	—	5	—	3.5	—	ns
TDH	Data Hold		1.5	—	1.5	—	1	—	ns

NOTES:

2884 tbl 13a

1. When the dynamic output slew rate control Modebits [61] or [62] are enabled, the initial values for the pull-up and pull-down rates should be set to the slowest value, Modebits [53:56]=15, Modebits[57:60]=0.
2. Timings are measured from 1.5V of the clock to 1.5V of signal.
3. Capacitive load for all output timings is 50pF. Deration is per CLD specification.
4. Data Output, Data Setup and Data Hold apply to all logic signals driven out of or driven into the R4000 on the system interface. Secondary cache signals are specified separately.

BOOT MODE INTERFACE PARAMETERS

Symbol	Parameter	Conditions	50MHz		67MHz		75MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
TMDS	Mode Data Setup		3	—	3	—	3	—	MCLK cycles
TMDH	Mode Data Hold		0	—	0	—	0	—	MCLK cycles

2884 tbl 13b

SECONDARY CACHE INTERFACE PARAMETERS

Symbol	Parameter	Conditions	50MHz		67MHz		75MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
T_{SCO}[1,2,3]	PClock to Output	Max Slew Rate Modebits[53:56] = 0 Modebits[57:60] = 15	2	10	2	7	2	7	ns
		Min Slew Rate Modebits[53:56] = 15 Modebits[57:60] = 0	6	16	6	12	6	12	ns
T_{SCDS}	Data Setup		5	—	5	—	3.5	—	ns
T_{SCDH}	Data Hold		2	—	1.5	—	1	—	ns
T_{Rd1Cyc}[4]	Cycle length of 4 word Rd		4	15	4	15	4	15	Pcycles
T_{Dis}[4]	Cycles between Rd & Wr		2	7	2	7	2	7	Pcycles
T_{Rd2Cyc}[4]	Cycle length of 8 word Rd		3	15	3	15	3	15	Pcycles
T_{Wr1Dly}[4]	Cycles bet. Addr & $\overline{SCWr}$		1	3	1	3	1	3	Pcycles
T_{WrRc}[4]	Cycles bet. deassertion of $\overline{SCWr}$ to start of next cycle		0	1	0	1	0	1	Pcycles
T_{WrSUp}[4]	Cycles from second doubleword to $\overline{SCWr}$		2	15	2	15	3	15	Pcycles
T_{Wr2Dly}[4]	Cycles between1st & 2nd word in 8-word write		1	3	1	3	1	3	Pcycles

2884 tbl 14

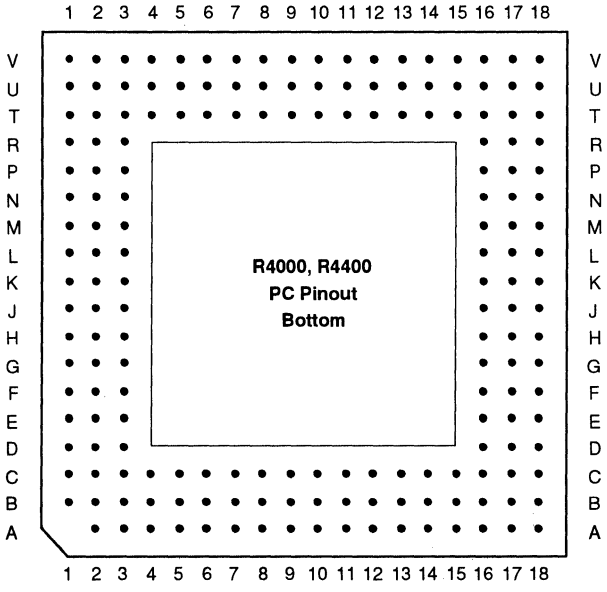
NOTES:
1. When the dynamic output slew rate control Mode bits [61] or [62] are enabled, the initial values for the pull-up and pull-down rates should be set to the slowest value, Modebits [53:56]=15, Modebits[57:60]=0.
2. Timings are measured from 1.5V of the Pclock to 1.5V of signal.
3. Capacitive load for all output timings is 50pF. Deration is per CLD specification.
4. Number of cycles is configured through the boot time mode control.

CAPACITIVE LOAD DERATION

Symbol	Parameter	50MHz		67MHz		75MHz		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
CLD	Load Derate	—	2	—	2	—	2	ns/25pF

2884 tbl 15

PHYSICAL SPECIFICATIONS



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IDT79R4000/4400 PC PACKAGE PINOUT

R4000 Function	PC Pkg Pin	R4000 Function	PC Pkg Pin	R4000 Function	PC Pkg Pin
ColdReset	T14	SysAD29	T16	VssP	K16
ExtRqst	U2	SysAD30	R17	Vcc	A2
Fault	B16	SysAD31	M16	Vcc	A4
Reserved (NC)	U10	SysAD32	H2	Vcc	A9
Vcc	T9	SysAD33	G3	Vcc	A11
IOIn	T13	SysAD34	F3	Vcc	A13
IOOut	U12	SysAD35	D2	Vcc	A16
Int0	N2	SysAD36	C3	Vcc	B18
Int1	L3	SysAD37	B3	Vcc	C1
Int2	K3	SysAD38	C6	Vcc	D18
Int3	J3	SysAD39	C7	Vcc	F1
Int4	H3	SysAD40	C10	Vcc	G18
Int5	F2	SysAD41	C11	Vcc	H1
JTCK	H17	SysAD42	B13	Vcc	J18
JTDI	G16	SysAD43	A15	Vcc	K1
JTDO	F16	SysAD44	C15	Vcc	L18
JTMS	E16	SysAD45	B17	Vcc	M1
MasterClock	J17	SysAD46	E17	Vcc	N18
MasterOut	P17	SysAD47	F17	Vcc	R1
ModeClock	B4	SysAD48	L2	Vcc	T18
ModeIn	U4	SysAD49	M3	Vcc	U1
NMI	U7	SysAD50	N3	Vcc	V3
PLLCap0	****	SysAD51	R2	Vcc	V6
PLLCap1	****	SysAD52	T3	Vcc	V8
RClock0	T17	SysAD53	U3	Vcc	V10
RClock1	R16	SysAD54	T6	Vcc	V12
RdRdy	T5	SysAD55	T7	Vcc	V14
Release	V5	SysAD56	T10	Vcc	V17
Reset	U16	SysAD57	T11	Vss	A3
SyncIn	J16	SysAD58	U13	Vss	A6
SyncOut	P16	SysAD59	V15	Vss	A8
SysAD0	J2	SysAD60	T15	Vss	A10
SysAD1	G2	SysAD61	U17	Vss	A12
SysAD2	E1	SysAD62	N16	Vss	A14
SysAD3	E3	SysAD63	N17	Vss	A17
SysAD4	C2	SysADC0	C8	Vss	A18
SysAD5	C4	SysADC1	G17	Vss	B1
SysAD6	B5	SysADC2	T8	Vss	C18
SysAD7	B6	SysADC3	L16	Vss	D1
SysAD8	B9	SysADC4	B8	Vss	F18
SysAD9	B11	SysADC5	H16	Vss	G1
SysAD10	C12	SysADC6	U8	Vss	H18
SysAD11	B14	SysADC7	L17	Vss	J1
SysAD12	B15	SysCmd0	E2	Vss	K18
SysAD13	C16	SysCmd1	D3	Vss	L1
SysAD14	D17	SysCmd2	B2	Vss	M18
SysAD15	E18	SysCmd3	A5	Vss	N1
SysAD16	K2	SysCmd4	B7	Vss	P18
SysAD17	M2	SysCmd5	C9	Vss	R18
SysAD18	P1	SysCmd6	B10	Vss	T1
SysAD19	P3	SysCmd7	B12	Vss	U18
SysAD20	T2	SysCmd8	C13	Vss	V1
SysAD21	T4	SysCmdP	C14	Vss	V2
SysAD22	U5	TClock0	C17	Vss	V4
SysAD23	U6	TClock1	D16	Vss	V7
SysAD24	U9	VCCOk	M17	Vss	V9
SysAD25	U11	ValidIn	P2	Vss	V11
SysAD26	T12	ValidOut	R3	Vss	V13
SysAD27	U14	WrRdy	C5	Vss	V16
SysAD28	U15	VccP	K17	Vss	V18

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PHYSICAL SPECIFICATIONS

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IDT79R4000/R4400 MC/SC PACKAGE PINOUT

R4000 Function	SC/MC Pkg Pin	R4000 Function	SC/MC Pkg Pin	R4000 Function	SC/MC Pkg Pin
$\overline{\text{ColdReset}}$	AW37	SCDChk9	N37	SCData53	AR13
$\overline{\text{ExtRqst}}$	AV2	SCDChk10	AU17	SCData54	AR15
$\overline{\text{Fault}}$	C39	SCDChk11	AG37	SCData55	AT18
Reserved (NC)	AV24	SCDChk12	E19	SCData56	AU23
IOIn	AV32	SCDChk13	R35	SCData57	AT26
IOOut	AV28	SCDChk14	AR19	SCData58	AR27
$\overline{\text{Int0}}$	AL1	SCDChk15	AE35	SCData59	AN29
$\overline{\text{IvdAck}}$[1]	AA35	SCData0	R3	SCData60	AP32
$\overline{\text{IvdErr}}$[1]	AA39	SCData1	R7	SCData61	AN35
JTCK	U39	SCData2	L5	SCData62	AJ35
JTDI	N39	SCData3	F8	SCData63	AE33
JTDO	J39	SCData4	C9	SCData64	V4
JTMS	G37	SCData5	F12	SCData65	R5
MasterClock	AA37	SCData6	G15	SCData66	N5
MasterOut	AJ39	SCData7	E17	SCData67	E5
ModeClock	B8	SCData8	G21	SCData68	G9
ModeIn	AV8	SCData9	C25	SCData69	E11
NMI	AV16	SCData10	G25	SCData70	G13
PLLCap0	****	SCData11	E29	SCData71	D14
PLLCap1	****	SCData12	G31	SCData72	C21
RClock0	AM34	SCData13	C35	SCData73	D22
RClock1	AL33	SCData14	K36	SCData74	E25
$\overline{\text{RdRdy}}$	AW7	SCData15	N35	SCData75	G27
$\overline{\text{Release}}$	AV12	SCData16	AE3	SCData76	C31
$\overline{\text{Reset}}$	AU39	SCData17	AG5	SCData77	F32
Reserved (NC)	Y2	SCData18	AK4	SCData78	J35
SCAPar0	U5	SCData19	AN9	SCData79	M34
SCAPar1	U1	SCData20	AU9	SCData80	AC7
SCAPar2	P4	SCData21	AN13	SCData81	AE5
SCAddr1	AL5	SCData22	AT14	SCData82	AG7
SCAddr2	AG1	SCData23	AR17	SCData83	AR5
SCAddr3	AE7	SCData24	AT22	SCData84	AR9
SCAddr4	AC1	SCData25	AU25	SCData85	AR11
SCAddr5	AC5	SCData26	AN27	SCData86	AN15
SCAddr6	AC3	SCData27	AR29	SCData87	AP16
SCAddr7	AA1	SCData28	AN31	SCData88	AU21
SCAddr8	AB4	SCData29	AR35	SCData89	AN23
SCAddr9	AA5	SCData30	AK36	SCData90	AR25
SCAddr10	AA7	SCData31	AG35	SCData91	AP28
SCAddr11	AA3	SCData32	T6	SCData92	AU31
SCAddr12	W3	SCData33	L3	SCData93	AR33
SCAddr13	Y6	SCData34	L7	SCData94	AL35
SCAddr14	W5	SCData35	E7	SCData95	AH34
SCAddr15	W7	SCData36	G11	SCData96	U7
SCAddr16	W1	SCData37	E13	SCData97	N3
SCAddr17	U3	SCData38	E15	SCData98	N7
SCAddr0W	AN7	SCData39	G17	SCData99	C5
SCAddr0X	AN5	SCData40	C23	SCData100	E9
SCAddr0Y	AM6	SCData41	F24	SCData101	C11
SCAddr0Z	AL7	SCData42	E27	SCData102	C13
$\overline{\text{SCDCS}}$	M6	SCData43	D30	SCData103	F16
SCDChk0	G19	SCData44	C33	SCData104	E21
SCDChk1	T34	SCData45	E35	SCData105	G23
SCDChk2	AP20	SCData46	L35	SCData106	C27
SCDChk3	AD34	SCData47	R33	SCData107	F28
SCDChk4	C19	SCData48	AF4	SCData108	E31
SCDChk5	R37	SCData49	AJ3	SCData109	G33
SCDChk6	AU19	SCData50	AJ7	SCData110	J37
SCDChk7	AE37	SCData51	AP8	SCData111	N33
SCDChk8	C17	SCData52	AT10	SCData112	AD6

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IDT79R4000/R4400 MC/SC PACKAGE PINOUT (continued)

R4000 Function	SC/MC Pkg Pin	R4000 Function	SC/MC Pkg Pin	R4000 Function	SC/MC Pkg Pin
SCData113	AG3	Status7	AC33	SysAD57	AW27
SCData114	AJ5	SyncIn	W39	SysAD58	AW31
SCData115	AU5	SyncOut	AN39	SysAd59	AW35
SCData116	AN11	SysAD0	T2	SysAD60	AU37
SCData117	AU11	SysAD1	M2	SysAD61	AR39
SCData118	AU13	SysAD2	J3	SysAD62	AL39
SCData119	AN17	SysAD3	G3	SysAD63	AG39
SCData120	AR21	SysAD4	C1	SysADC0	A17
SCData121	AP24	SysAD5	A3	SysADC1	R39
SCData122	AU27	SysAD6	A9	SysADC2	AW17
SCData123	AT30	SysAD7	A13	SysADC3	AD38
SCData124	AU33	SysAD8	A21	SysADC4	A19
SCData125	AN33	SysAD9	A25	SysADC5	T38
SCData126	AL37	SysAD10	A29	SysADC6	AW19
SCData127	AG33	SysAD11	A33	SysADC7	AC39
$\overline{SCOE}$	N1	SysAd12	B38	SysCmd0	G1
$\overline{SCTCS}$	J1	SysAD13	E37	SysCmd1	E3
SCTChk0	AN21	SysAD14	G39	SysCmd2	B2
SCTChk1	AN19	SysAD15	L39	SysCmd3	B12
SCTChk2	AU15	SysAD16	AD2	SysCmd4	B16
SCTChk3	AP12	SysAD17	AH2	SysCmd5	B20
SCTChk4	AU7	SysAD18	AL3	SysCmd6	B24
SCTChk5	AR7	SysAD19	AN3	SysCmd7	B28
SCTChk6	AH6	SysAD20	AU1	SysCmd8	B32
SCTag0	K4	SysAD21	AW3	SysCmdP	A37
SCTag1	G7	SysAD22	AW9	TClock0	H34
SCTag2	C7	SysAD23	AW13	TClock1	J33
SCTag3	D10	SysAD24	AW21	VCCOk	AE39
SCTag4	C15	SysAD25	AW25	$\overline{ValidIn}$	AN1
SCTag5	D18	SysAD26	AW29	$\overline{ValidOut}$	AR3
SCTag6	F20	SysAD27	AW33	$\overline{WrRdy}$	A7
SCTag7	E23	SysAD28	AV38	VccSense	W33
SCTag8	D26	SysAD29	AR37	VssSense	U37
SCTag9	C29	SysAD30	AM38	VccP	AA33
SCTag10	G29	SysAD31	AH38	VssP	Y34
SCTag11	E33	SysAD32	R1	Vcc	A39
SCTag12	G35	SysAD33	L1	Vcc	B6
SCTag13	L33	SysAD34	H2	Vcc	B10
SCTag14	L37	SysAD35	E1	Vcc	B18
SCTag15	P36	SysAD36	C3	Vcc	B26
SCTag16	AF36	SysAD37	A5	Vcc	B34
SCTag17	AJ37	SysAD38	A11	Vcc	D4
SCTag18	AJ33	SysAd39	A15	Vcc	D8
SCTag19	AN37	SysAD40	A23	Vcc	D16
SCTag20	AU35	SysAD41	A27	Vcc	D24
SCTag21	AR31	SysAd42	A31	Vcc	D32
SCTag22	AU29	SysAD43	A35	Vcc	D36
SCTag23	AN25	SysAd44	C37	Vcc	F2
SCTag24	AR23	SysAD45	E39	Vcc	F14
$\overline{SCWrW}$	J5	SysAD46	H38	Vcc	F22
$\overline{SCWrX}$	J7	SysAD47	M38	Vcc	F30
$\overline{SCWrY}$	H6	SysAD48	AE1	Vcc	F38
$\overline{SCWrZ}$	G5	SysAD49	AJ1	Vcc	H4
Status0	U33	SysAD50	AM2	Vcc	H36
Status1	U35	SysAD51	AR1	Vcc	K6
Status2	V36	SysAD52	AU3	Vcc	K38
Status3	W35	SysAD53	AW5	Vcc	P2
Status4	W37	SysAD54	AW11	Vcc	P34
Status5	AC37	SysAD55	AW15	Vcc	T4
Status6	AC35	SysAD56	AW23		

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IDT79R4000/R4400 MC/SC PACKAGE PINOUT (continued)

R4000 Function	SC/MC Pkg Pin	R4000 Function	SC/MC Pkg Pin	R4000 Function	SC/MC Pkg Pin
Vcc	T36	Vcc	AV34	Vss	Y4
Vcc	V6	Vcc	AW1	Vss	Y36
Vcc	V38	Vcc	AW39	Vss	AB6
Vcc	Y38	Vss	B4	Vss	AB36
Vcc	AB2	Vss	B14	Vss	AB38
Vcc	AB34	Vss	B22	Vss	AF2
Vcc	AD4	Vss	B30	Vss	AF34
Vcc	AD36	Vss	B36	Vss	AH4
Vcc	AF6	Vss	D2	Vss	AH36
Vcc	AF38	Vss	D6	Vss	AK6
Vcc	AK2	Vss	D12	Vss	AK38
Vcc	AK34	Vss	D20	Vss	AP4
Vcc	AM4	Vss	D28	Vss	AP6
Vcc	AM36	Vss	D34	Vss	AP14
Vcc	AP2	Vss	D38	Vss	AP22
Vcc	AP10	Vss	F4	Vss	AP30
Vcc	AP18	Vss	F6	Vss	AP34
Vcc	AP26	Vss	F10	Vss	AP36
Vcc	AP38	Vss	F18	Vss	AT2
Vcc	AT4	Vss	F26	Vss	AT6
Vcc	AT8	Vss	F34	Vss	AT12
Vcc	AT16	Vss	F36	Vss	AT20
Vcc	AT24	Vss	K2	Vss	AT28
Vcc	AT32	Vss	K34	Vss	AT34
Vcc	AT36	Vss	M4	Vss	AT38
Vcc	AV6	Vss	M36	Vss	AV4
Vcc	AV14	Vss	P6	Vss	AV10
Vcc	AV20	Vss	P38	Vss	AV18
Vcc	AV22	Vss	V2	Vss	AV26
Vcc	AV30	Vss	V34	Vss	AV36

NOTE:
1. Available in IDT79R4400MC only. For IDT79R4000SC and R4400SC, these inputs must be pulled to Vcc.

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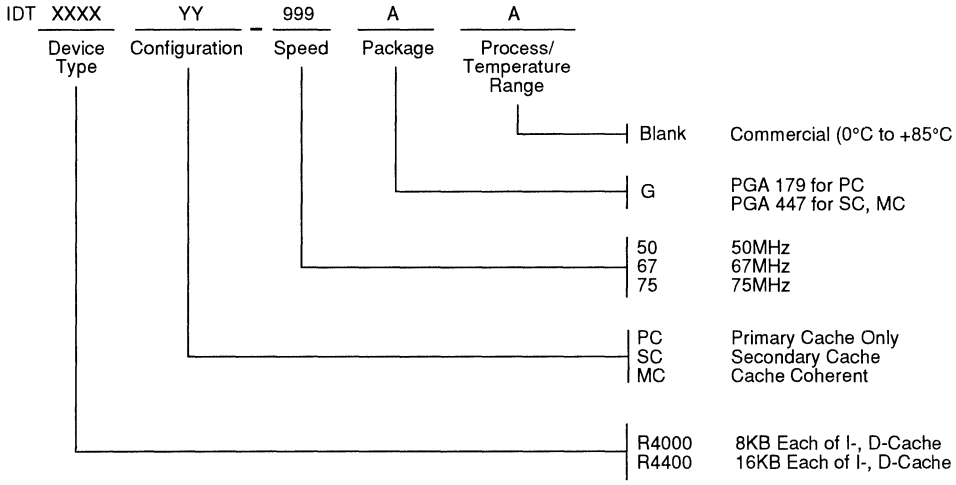
ORDERING INFORMATION



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VALID COMBINATIONS

R4000 PC — 50, 67	G
R4000 SC — 50, 67	G
R4400 PC — 50, 67, 75	G
R4400 SC — 50, 67, 75	G
R4400 MC — 50, 67, 75	G

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RISC SUPPORT COMPONENTS

A RISC microprocessor is an important, but not self-sufficient, element of a high-performance general or embedded computing system. Equally important is the memory system (both cache and main memory) and the I/O interface to the execution core.

To simplify the task of building these high-performance subsystems, IDT produces a wide variety of support chips and building block devices. These chips range from general purpose devices such as fast static RAM and high-performance logic (used with many processor families), to specialized devices used in only certain types of applications (such as the IDT LaserFIFO, used in laser printer systems) and devices designed to work with only a specific processor family.

Generic building block devices include SRAMs, with densities from 16KB to 1MB and access times as low as 7ns, as well as high-speed logic devices such as the FCT-T family.

Devices specifically developed for RISC systems include the 3720 Bus Exchanger and 3721 DRAM Controller. These components facilitate design of systems based upon the R3051/52 controller family. The DRAM and I/O controllers have direct bus interface to the 3051/52.

The R3020 Write Buffer enhances the performance of R3000 systems by allowing the processor to perform write operations at full clock speeds instead of resorting to time-consuming CPU stall cycles. The memory can then retire the data at a slower rate. The R32xx family of read/write buffers includes the memory read capability, enabling the use of slower main memory without impacting system performance.

The R3730 Integrated System Controller is a highly programmable controller for high-performance Raster Image Systems. It contains DMA, FIFOs and arbitration logic to provide bandwidth matching between CPU/memory bus and slower standard I/O peripherals.

By providing these system solutions as building blocks, IDT allows its customers the maximum flexibility in achieving their price/performance goals while minimizing time-to-market, real estate and complexity of the end system.

This section of the data book contains some selected devices which have either been specifically designed for particular RISC processors or found to be exceptionally useful in these high-performance systems.

TABLE OF CONTENTS

Integrated Device Technology, Inc.

RISC FLOATING POINT ACCELERATOR (FPA)

IDT79R3010A
IDT79R3010AE

FEATURES:

- Hardware Support of Single and Double-Precision Operations:
  - — Floating-Point Add
  - — Floating-Point Subtract
  - — Floating-Point Multiply
  - — Floating-Point Divide
  - — Floating-Point Comparisons
  - — Floating-Point Conversions
- Sustained performance:
  - — 11 MFLOPS single precision LINPACK
  - — 7.3 MFLOPS double precision LINPACK
- 16.7MHz through 40MHz operation
- Direct, high-speed interface with IDT79R3000A and IDT79R3001 Processor
- Supports Full Conformance With IEEE 754-1985 Floating-PointSpecification
- Full 64-bit operation using sixteen 64-bit data registers
- High-speed CMOS technology
- 32-bit status/control register providing access to all IEEE-Standard exception handling
- Load/store architecture allows data movement directly between FPA and memory or between CPU and FPA
- Overlapped operation of independent floating point ALUs

DESCRIPTION:

The IDT79R3010A Floating-Point Accelerator (FPA) operates in conjunction with the IDT79R3000A Processor and extends the IDT79R3000As instruction set to perform arithmetic operations on values in floating-point representations. The IDT79R3010A FPA, with associated system software, fully conforms to the requirements of ANSI/IEEE Standard 754-1985, "IEEE Standard for Binary Floating-Point Arithmetic." In addition, the architecture fully supports the standard's recomendations.

This data sheet provides an overview of the features and architecture of the 79R3010A FPA. A more detailed description of the operation of the device is incorporated in the *R3000A Family Hardware User's Manual*, available from IDT, and a more detailed architectural overview is provided in the *MIPS RISC Architecture* book, available from MIPS/SGI.

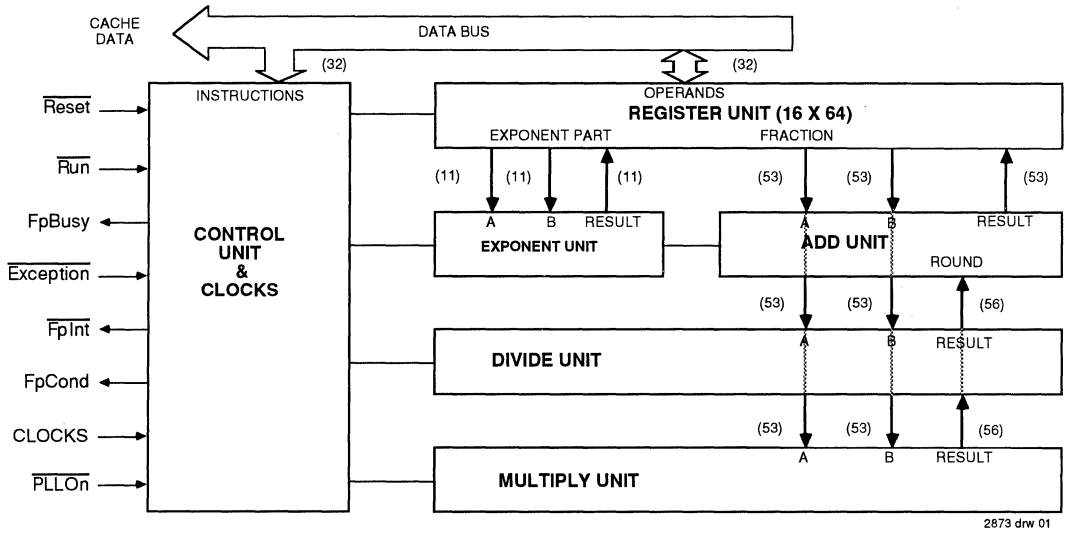

Figure 1. IDT79R3010A Functional Block Diagram

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IDT79R3010A FPA REGISTERS

The IDT79R3010A FPA provides 32 general purpose 32-bit registers, a Control/Status register, and a Revision Identification register. The tightly-coupled coprocessor interface causes the register resources of the FPA to appear to the systems programmers as an extension of the CPU internal registers. The FPA registers are shown in Figure 2.

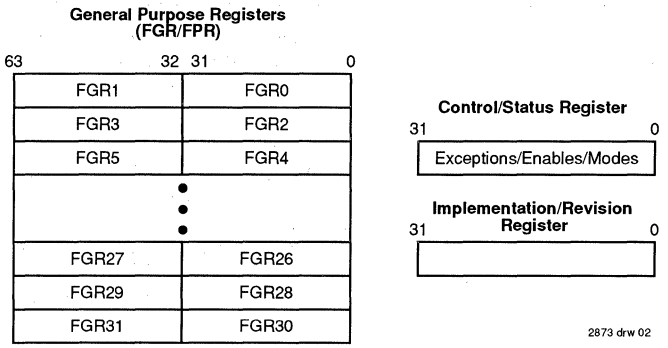

Figure 2. IDT79R3010A FPA Registers

Floating-point coprocessor operations reference three types of registers:

- Floating-Point Control Registers (FCR)
- Floating-Point General Registers (FGR)
- Floating-Point Registers (FPR)

Floating-Point General Registers (FGR)

There are 32 Floating-Point General Registers (FGR) on the FPA. They represent directly-addressable 32-bit registers, and can be accessed by Load, Store, or Move Operations.

Floating-Point Registers (FPR)

The 32 FGRs described in the preceding paragraph are also used to form sixteen 64-bit Floating-Point Registers (FPR). Pairs of general registers (FGRs), for example FGR0 and FGR1 (refer to Figure 2) are physically combined to form a single 64-bit FPR. The FPRs hold a value in either single- or double-precision floating-point format. Double-precision format FPRs are formed from two adjacent FGRs.

Floating-Point Control Registers (FCR)

There are 2 Floating-Point Control Registers (FCR) on the FPA. They can be accessed only by Move operations and include the following:

- Control/Status register, used to control and monitor exceptions, operating modes, and rounding modes;
- Revision register, containing revision information about the FPA.

COPROCESSOR OPERATION

The FPA continually monitors the IDT79R3000A processor instruction stream. If an instruction does not apply to the coprocessor, it is ignored; if an instruction does apply to the coprocessor, the FPA executes that instruction and transfers necessary result and exception data synchronously to the IDT79R3000A main processor.

The FPA performs three types of operations:

- Loads and Stores;
- Moves;
- Two- and three-register floating-point operations.

Load, Store, and Move Operations

Load, Store, and Move operations move data between memory or the IDT79R3000A Processor registers and the IDT79R3010A FPA registers. These operations perform no format conversions and cause no floating-point exceptions. Load, Store, and Move operations reference a single 32-bit word of either the Floating-Point General Registers (FGR) or the Floating-Point Control Registers (FCR).

Floating-Point Operations

The FPA supports the folowing single- and double-precision format floating-point operations:

- Add
- Subtract
- Multiply
- Divide
- Absolute Value
- Move
- Negate
- Compare

In addition, the FPA supports conversions between single- and double-precision floating-point formats and fixed-point formats.

The FPA incorporates separate Add/Subtract, Multiply, and Divide units, each capable of independent and concurrent operation. Thus, to achieve very high performance, floating point divides can be overlapped with floating point multiplies and floating point additions. These floating point operations occur independently of the actions of the CPU, allowing further overlap of integer and floating point operations. Figure 3 illustrates an example of the types of overlap permissible.

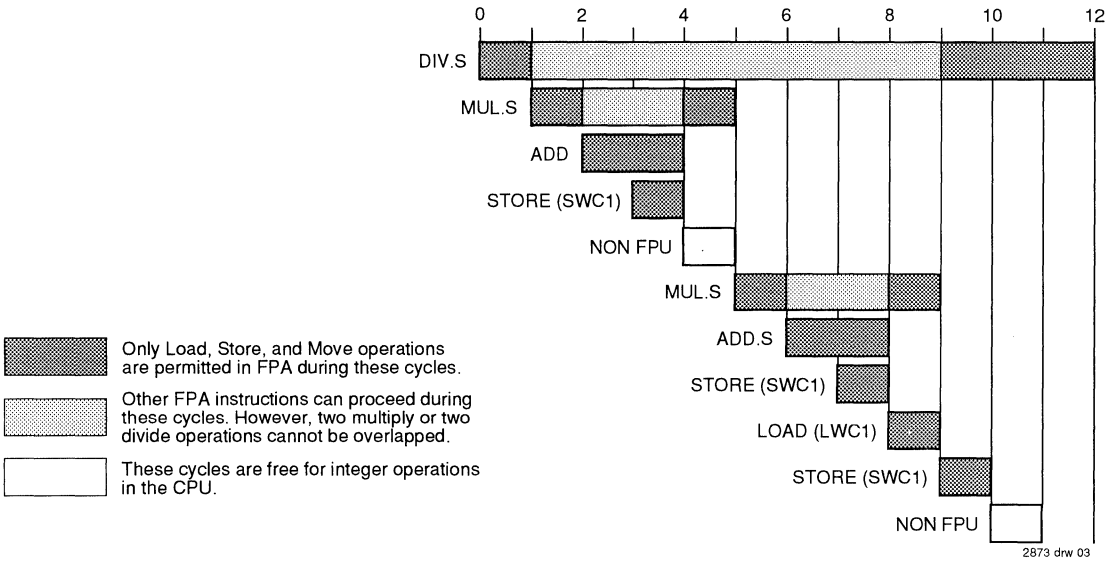

Figure 3. Examples of Overlapping Floating Point Operation

Exceptions

The IDT79R3010A FPA supports all five IEEE standard exceptions:

- Invalid Operation
- Inexact Operation
- Division by Zero
- Overflow
- Underflow

The FPA also supports the optional, Unimplemented Operation exception that allows unimplemented instructions to trap to software emulation routines.

The FPA provides precise exception capability to the CPU; that is, the execution of a floating point operation which generates an exception causes that exception to occur at the CPU instruction which caused the operation. This precise exception capability is a requirement in applications and languages which provide a mechanism for local software exception handlers within software modules.

INSTRUCTION SET OVERVIEW

All IDT79R3010A instructions are 32 bits long and they can be divided into the folowing groups:

- **Load/Store and Move** instructions move data between memory, the main processor and the FPA general registers.
- **Computational** instructions perform arithmetic operations on floating point values in the FPA registers.
- **Conversion** instructions perform conversion operations between the various data formats.
- **Compare** instructions perform comparisons of the contents of registers and set a condition bit based on the results. The result of the compare operation is output on the FpCond output of the FPA, which is typically used as CpCond1 on the CPU for use in coprocessor branch operations.

Table 1 lists the instruction set of the IDT79R3010A FPA.

OP	Description	OP	Description
	Load/Store/Move Instructions		**Computational Instructions**
LWC1	Load Word to FPA	**ADD.fmt**	Floating-point Add
SWC1	Store Word from FPA	**SUB.fmt**	Floating-point Subtract
MTC1	Move Word to FPA	**MUL. fmt**	Floating-point Multiply
MFC1	Move Word from FPA	**DIV.fmt**	Floating-point Divide
CTC1	Move Control word to FPA	**ABS.fmt**	Floating-point Absolute value
CFC1	Move Control word from FPA	**MOV.fmt**	Floating-point Move
		NEG.fmt	Floating-point Negate
	Conversion Instructions		**Compare Instructions**
CVT.S.fmt	Floating-point Convert to Single FP	**C.cond.fmt**	Floating-point Compare
CVT.D.fmt	Floating-point Convert to Double FP		
CVT.W.fmt	Floating-point Convert to fixed-point		

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Table 1. IDT79R3010A Instruction Summary

ID79R3010 PIPELINE ARCHITECTURE

The IDT79R3010A FPA provides an instruction pipeline that parallels that of the IDT79R3000A processor. The FPA, however, has a 6-stage pipeline instead of the 5-stage pipeline of the IDT79R3000: the additional FPA pipe stage is used to provide efficient coordination of exception responses between the FPA and main processor.

The execution of a single IDT79R3010A instruction consists of six primary steps:

1) **IF**—Instruction Fetch. The main processor calculates the insruction address required to read an instruction from the I-Cache. No action is required of the FPA during this pipe stage since the main processor is responsible for address generation.
2) **RD**—The instruction is present on the data bus during phase 1 of this pipe stage and the FPA decodes the instruction on the bus to determine if it is an instruction for the FPA.
3) **ALU**—If the instruction is an FPA instruction, instruction execution commences during this pipe stage.
4) **MEM**—If this is a coprocessor load or store instruction, the FPA presents or captures the data during phase 2 of this pipe stage.
5) **WB**—The FPA uses this pipe stage solely to deal with exceptions.
6) **FWB**—The FPA uses this stage to write back ALU results to its register file. This stage is the equivalent of the WB stage in the IDT79R3000A main processor.

Each of these steps requires approximately one FPA cycle as shown in Figure 3 (parts of some operations spill over into another cycle while other operations require only 1/2 cycle).

INSTRUCTION EXECUTION

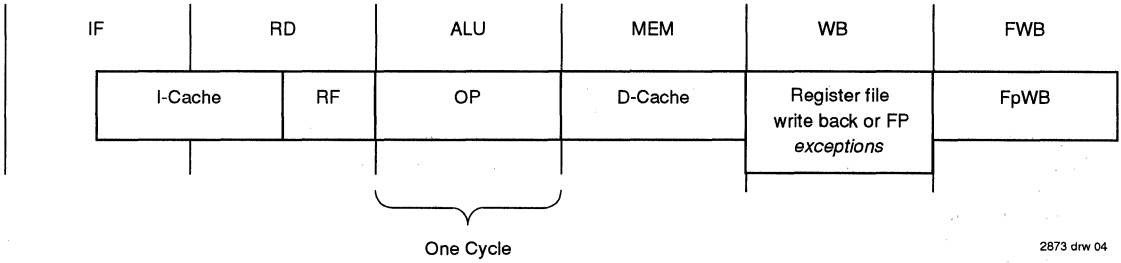


Figure 4. IDT79R3010A Instruction Summary

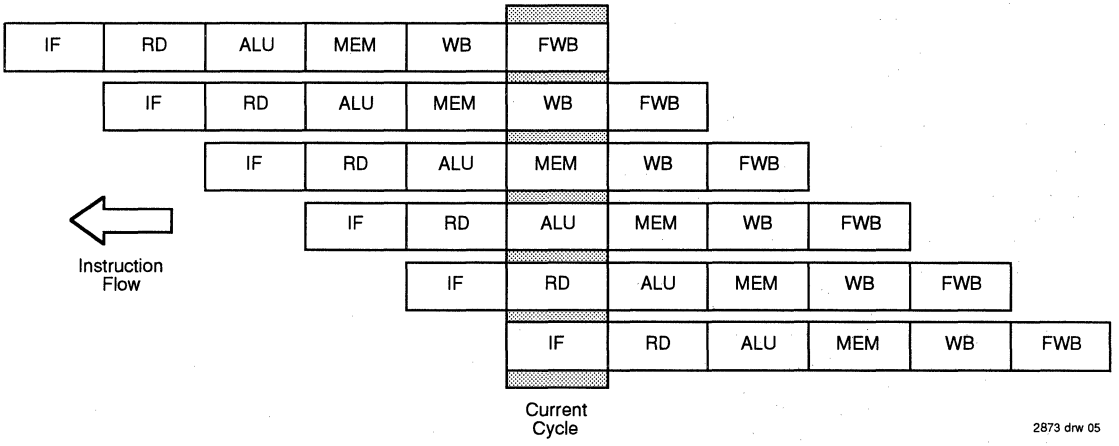


Figure 5. IDT79R3010A Instruction Pipeline

The IDT79R3010A uses a 6-stage pipeline to achieve an instruction execution rate approaching one instruction per FPA cycle. Thus, execution of six instructions at a time are overlapped as shown in Figure 5.

This pipeline operates efficiently because different FPA resources (address and data bus accesses, ALU operations, register accesses, and so on) are utilized on a non-interfering basis.

PACKAGE THERMAL SPECIFICATIONS

The IDT79R3010A utilizes special packaging techniques to improve both the thermal and electrical characteristics of the floating point accelerator.

In order to improve the electrical characteristics of the device, the package is constructed using multiple signal planes, including individual power planes and ground planes to reduce noise associated with high-frequency TTL parts.

In order to improve the thermal characteristics of the floating point accelerator, the device is housed using cavity down packaging for the flatpack and the PGA (the J-bend CerQuad is cavity up). In addition, these packages incorporate a copper-tungsten thermal slug designed to efficiently transfer heat from the die to the case of the package, and thus effectively lower the thermal resistance of the package. The use of an additional external heat sink affixed to the package thermal slug further decreases the effective thermal resistance of the package.

The case temperature may be measured in any environment to determine whether the device is within the specified operating range. The case temperature should be measured at the center of the top surface opposite the package cavity (the package cavity is the side where the package lid is mounted).

The equivalent allowable ambient temperature, T_A, can be calculated using the thermal resistance from case to ambient ($\varnothing ca$) for the given package. The following equation relates ambient and case temperature:

$$T_A = T_C - P * \varnothing ca$$

where P is the maximum power consumption, calculated by using the maximum Icc from the DC Electrical Characteristic section.

Typical values for $\varnothing ca$ at various airflows are shown in Table 2 for the various CPU packages.

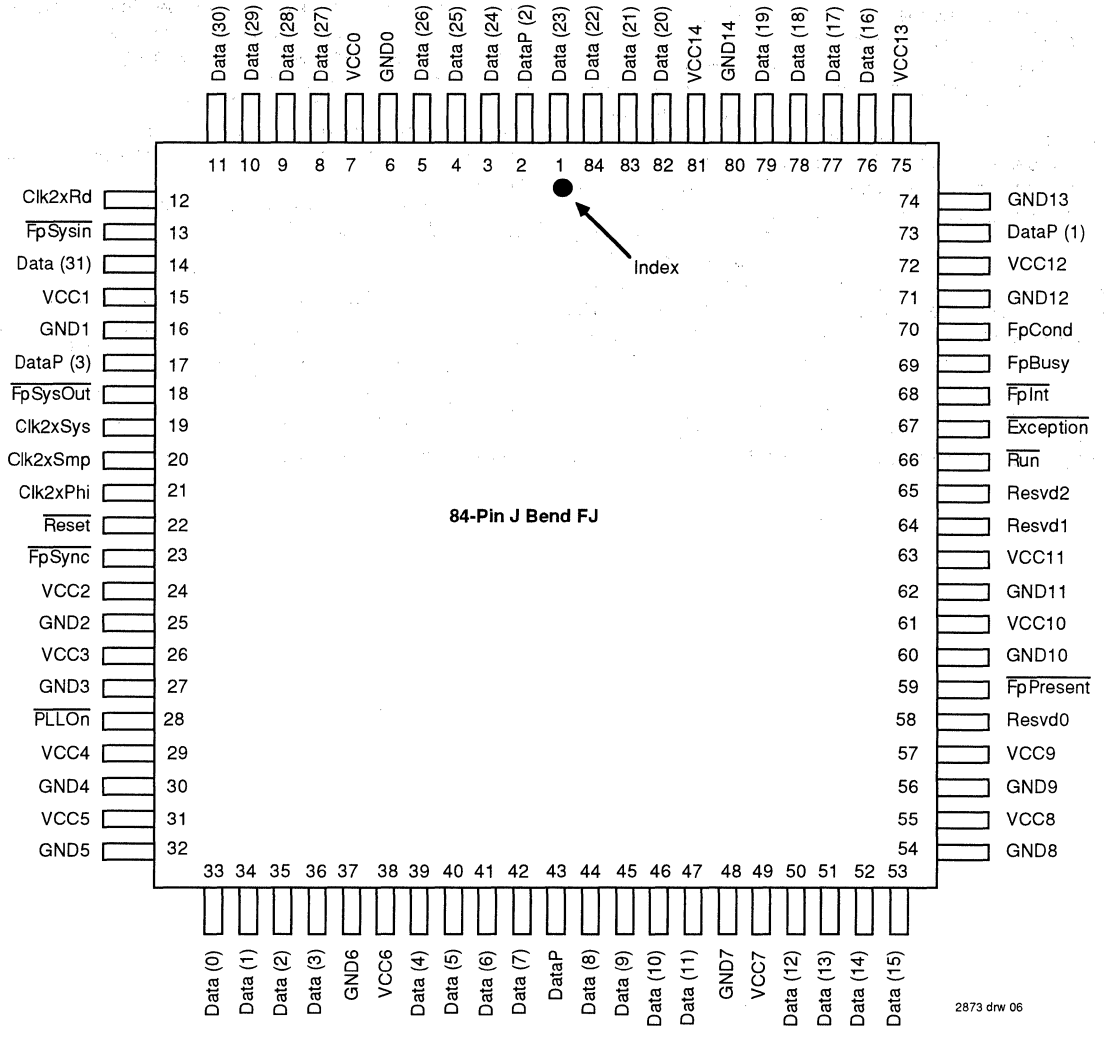
	Airflow - (ft/min)					
	0	200	400	600	800	1000
$\varnothing ca$ (84-PGA)	22	8	3	2	1.5	1.0
$\varnothing ca$ (84-Flatpack)	22	9	4	3	2	1.5
$\varnothing ca$ (84-CerQuad)	25	17	12	8	7	6

2873 tbl 02

Table 2. Thermal Resistance (Oca) at Various Airflows

6

PIN CONFIGURATION[1]
(Top View)



NOTE:
1. Reserved pins must not be connected.

PIN CONFIGURATION[1]
(Ceramic, Cavity Down) – BOTTOM VIEW

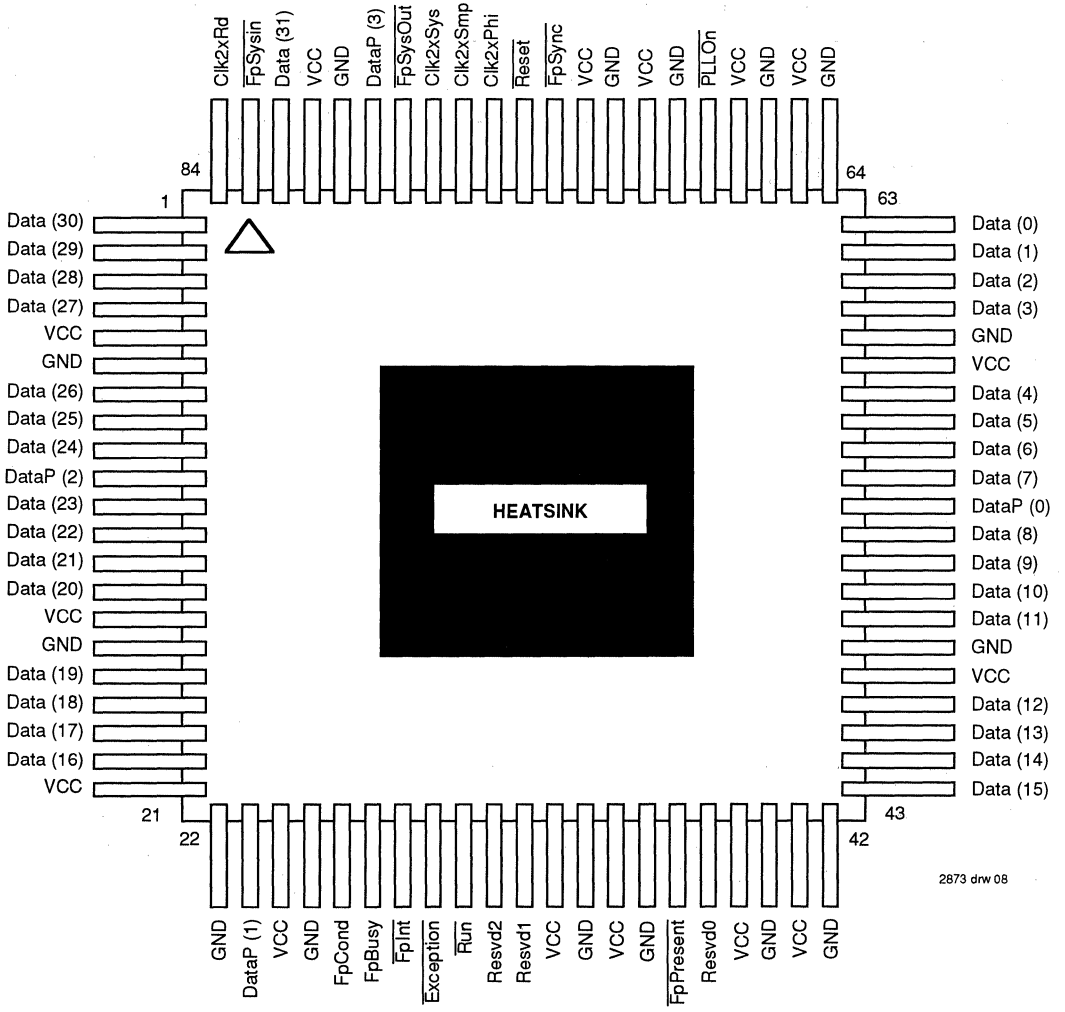
	1	2	3	4	5	6	7	8	9	10	11	12
M	Vss	Vcc	Data 17	DataP 1	Vss	FP Cond	$\overline{\text{FPInt}}$	Vss	$\overline{\text{Run}}$	Rsrvd 1	Vcc	Vss
L	Data 21	Data 20	Data 18	Data 16	Vcc	FPBusy	Except-tion	Vcc	Rsrvd 2	$\overline{\text{FP}}$ Present	Data 15	Data 14
K	Vss	Vcc	Data 19							Rsrvd 0	Vcc	Vss
J	Data 23	Data 22									Data 13	Data 12
H	Data 24	DataP 2									Data 11	Data 10
G	Data 26	Data 25				**84-Pin Ceramic Pin Grid Array**					Vcc	Vss
F	Vss	Vcc									Data 8	Data 9
E	Data 27	Data 28									Data 7	DataP 0
D	Data 29	Data 30									Data 5	Data 6
C	Vss	Vcc	Clk2x Rd							Data 2	Vcc	Vss
B	$\overline{\text{Fp}}$ SysIn	Data 31	DataP 3	Vcc	Clk2x Sys	Vcc	Clk2x Phi	Vcc	$\overline{\text{PllOn}}$	Data 1	Data 3	Data 4
A	Vss	Vcc	$\overline{\text{FpSys}}$ Out	Vss	Clk2x Smp	Vss	$\overline{\text{Reset}}$	Vss	$\overline{\text{FP}}$ Sync	Data 0	Vcc	Vss

2873 drw 07

NOTE:
1. Reserved pins must not be connected.

6

PIN CONFIGURATION[1]
84–L QUAD FLATPACK (CAVITY DOWN)
TOP VIEW



NOTE:
1. Reserved pins must not be connected.

PIN DESCRIPTIONS

Pin Name	I/O	Description
Data (0-31)	I/O	A multiplexed 32-bit bus used for instruction and data transfers on phase 1 and phase 2, respectively.
DataP (0-3)	O	A 4-bit bus containing even parity over the data bus. Parity is generated by the FPA on stores.
$\overline{\text{Run}}$	I	Input to the FPA which indicates whether the processor-coprocessor system is in the run or stall state.
$\overline{\text{Exception}}$	I	Input to the FPA which indicates exception related status information.
FpBusy	O	Signal to the CPU indicating a request for a coprocessor busy stall.
FpCond	O	Signal to the CPU indicating the result of the last comparision operation.
$\overline{\text{FpInt}}$	O	Signal to the CPU indicating that a floating-point exception has occured for the current FPA instruction.
$\overline{\text{Reset}}$	I	Synchronous initialization input used to distinguish the processor-FPA synchronization period from the execution period. $\overline{\text{Reset}}$ must be synchronized by the leading edge of $\overline{\text{SysOut}}$ from the CPU.
$\overline{\text{PllOn}}$	I	Input which during the reset period determines whether the phase lock mechanism is enabled and during the execution period determines the output timing model.
$\overline{\text{FpPresent}}$	O	Output which is pulled to ground through an impedance of approximately 0.5kΩ. By providing an external pullup on this line, an indication of the presence or absence of the FPA can be obtained.
Clk2xSys	I	A double frequency clock input used for generating $\overline{\text{FpSysOut}}$.
Clk2xSmp	I	A double frequency clock input used to determine the sample point for data coming in to the FPA.
Clk2xRd	I	A double frequency clock input used to determine the disable point for the data drivers.
Clk2xPhi	I	A double frequency clock input used to determine the position of the internal phases, phase 1 and phase 2.
$\overline{\text{FpSysOut}}$	O	Synchronization clock from the FPA.
$\overline{\text{FpSysIn}}$	I	Input used to receive the synchronization clock from the FPA.
$\overline{\text{FpSync}}$	I	Input used to receive the synchronization clock from the CPU.

2873 tbl 03

6

ABSOLUTE MAXIMUM RATINGS(1, 3)

Symbol	Rating	Commercial	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TA, TC	Operating Temperature	0 to +70(4) (Ambient) 0 to +90(5) (Case)	°C
TBIAS	Case Temperature Under Bias	–55 to +125(4) 0 to +90(5)	°C
TSTG	Storage Temperature	–55 to +125	°C
IIN	Input Voltage	–0.5 to +7.0	V

2873 tbl 04

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VIN minimum = –3.0V for pulse width less than 15ns. VIN should not exceed VCC +0.5 Volts.
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.
4. 16-33MHz only.
5. 40MHz only.

AC TEST CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
VIH	Input HIGH Voltage	3.0	—	V
VIL	Input LOW Voltage	—	0.4	V
VIHS	Input HIGH Voltage	3.5	—	V
VILS	Input LOW Voltage	—	0.4	V
VIHC	Input HIGH Voltage	4.0	—	V
VILC	Input LOW Voltage	—	0.4	V

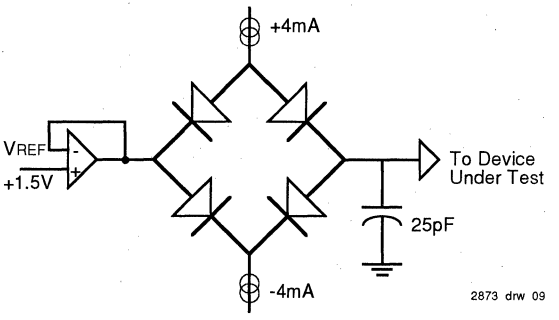
2873 tbl 05

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Commercial 16-33MHz	0°C to +70°C (Ambient)	0V	5.0 ±5%
Commercial 40MHz	0°C to +90°C (Case)	0V	5.0 ±5%

2873 tbl 06

OUTPUT LOADING FOR AC TESTING



2873 drw 09

DC ELECTRICAL CHARACTERISTICS FOR IDT79R3010A
COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to + 70°C, V_{CC} = + 5.0 V ± 5%)

Symbol	Parameter	Test Conditions	16.67 MHz		20.0 MHz		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –4mA	3.5	—	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OLFP}	Output LOW Voltage(5)	V_{CC} = Min, I_{OL} = 1.5mA	—	0.5	—	0.5	V
V_{IH}	Input HIGH Voltage(6)		2.0	—	2.0	—	V
V_{IL}	Input LOW Voltage(1)		—	0.8	—	0.8	V
V_{IHS}	Input HIGH Voltage(2,6)		3.0	—	3.0	—	V
V_{ILS}	Input LOW Voltage(1,2)		—	0.4	—	0.4	V
V_{IHC}	Input HIGH Voltage(4,6)		4.0	—	4.0	—	V
V_{ILC}	Input LOW Voltage(1,4)		—	0.4	—	0.4	V
C_{IN}	Input Capacitance(7)		—	10	—	10	pF
C_{OUT}	Output Capacitance(7)		—	10	—	10	pF
I_{CC}	Operating Current	V_{CC} = 5.0V, T_A = 70°C	—	525	—	600	mA
I_{IH}	Input HIGH Leakage(3)	V_{IH} = V_{CC}	—	100	—	100	µA
I_{IL}	Input LOW Leakage(3)	V_{IL} = GND	–100	—	–100	—	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	–100	100	–100	100	µA

2873 tbl 07

DC ELECTRICAL CHARACTERISTICS FOR IDT79R3010AE
COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to + 70°C, V_{CC} = + 5.0 V ± 5%)

Symbol	Parameter	Test Conditions	25.0 MHz		33.33 MHz		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –4mA	3.5	—	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OLFP}	Output LOW Voltage(5)	V_{CC} = Min, I_{OL} = 1.5mA	—	0.5	—	0.5	V
V_{IH}	Input HIGH Voltage(6)		2.0	—	2.0	—	V
V_{IL}	Input LOW Voltage(1)		—	0.8	—	0.8	V
V_{IHS}	Input HIGH Voltage(2,6)		3.0	—	3.0	—	V
V_{ILS}	Input LOW Voltage(1,2)		—	0.4	—	0.4	V
V_{IHC}	Input HIGH Voltage(4,6)		4.0	—	4.0	—	V
V_{ILC}	Input LOW Voltage(1,4)		—	0.4	—	0.4	V
C_{IN}	Input Capacitance(7)		—	10	—	10	pF
C_{OUT}	Output Capacitance(7)		—	10	—	10	pF
I_{CC}	Operating Current	V_{CC} = 5.0V, T_A = 70°C	—	650	—	700	mA
I_{IH}	Input HIGH Leakage(3)	V_{IH} = V_{CC}	—	100	—	100	µA
I_{IL}	Input LOW Leakage(3)	V_{IL} = GND	–100	—	–100	—	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	–100	100	–100	100	µA

2873 tbl 08

NOTES:

1. V_{IL} Min. = –3.0V for pulse width less than 15ns. V_{IL} should not fall below –0.5V for larger periods.
2. V_{IHS} and V_{ILS} apply to Clk2xSys, Clk2xSmp, Clk2xRd, Clk2xPhi, $\overline{\text{FpSysin}}$, $\overline{\text{FpSync}}$ and $\overline{\text{Reset}}$.
3. These parameters do not apply to the clock inputs.
4. V_{IHC} and V_{ILC} apply to $\overline{\text{Run}}$, $\overline{\text{PllOn}}$ and $\overline{\text{Exception}}$.
5. V_{OLFP} applies to the $\overline{\text{FPPresent}}$ pin only.
6. V_{IH} and V_{IHS} should not be held above V_{CC} + 0.5V.
7. Guaranteed by design.

6

DC ELECTRICAL CHARACTERISTICS FOR IDT79R3010AE
COMMERCIAL TEMPERATURE RANGE (T_C = 0°C to + 90°C, V_{CC} = + 5.0 V ± 5%)

Symbol	Parameter	Test Conditions	40 MHz		Unit
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –4mA	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 4mA	—	0.4	V
V_{OLFP}	Output LOW Voltage(5)	V_{CC} = Min, I_{OL} = 1.5mA	—	0.5	V
V_{IH}	Input HIGH Voltage(6)		2.0	—	V
V_{IL}	Input LOW Voltage(1)		—	0.8	V
V_{IHS}	Input HIGH Voltage(2,6)		3.0	—	V
V_{ILS}	Input LOW Voltage(1,2)		—	0.4	V
V_{IHC}	Input HIGH Voltage(4,6)		4.0	—	V
V_{ILC}	Input LOW Voltage(1,4)		—	0.4	V
C_{IN}	Input Capacitance(7)		—	10	pF
C_{OUT}	Output Capacitance(7)		—	10	pF
I_{CC}	Operating Current	V_{CC} = 5.0V, T_C = 90°C	—	750	mA
I_{IH}	Input HIGH Leakage(3)	V_{IH} = V_{CC}	—	100	µA
I_{IL}	Input LOW Leakage(3)	V_{IL} = GND	–100	—	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	–100	100	µA

2873 tbl 09

NOTES:

1. V_{IL} Min. = –3.0V for pulse width less than 15ns. V_{IL} should not fall below –0.5V for larger periods.
2. V_{IHS} and V_{ILS} apply to Clk2xSys, Clk2xSmp, Clk2xRd, Clk2xPhi, $\overline{\text{FpSysin}}$, $\overline{\text{FpSync}}$ and $\overline{\text{Reset}}$.
3. These parameters do not apply to the clock inputs.
4. V_{IHC} and V_{ILC} apply to $\overline{\text{Run}}$, $\overline{\text{PllOn}}$ and $\overline{\text{Exception}}$.
5. V_{OLFP} applies to the $\overline{\text{FPPresent}}$ pin only.
6. V_{IH} and V_{IHS} should not be held above V_{CC} + 0.5V.
7. Guaranteed by design.

AC ELECTRICAL CHARACTERISTICS FOR IDT79R3010A(1, 3)
COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to +70°C, V_{CC} = +5.0V ± 5%)

Symbol	Parameter	Test Conditions	16.67 MHz		20.0 MHz		Unit
			Min.	Max.	Min.	Max.	
Clock							
TCkHigh	Input Clock HIGH(2)	Note 7	12	—	10	—	ns
TCkLow	Input Clock LOW(2)	Note 7	12	—	10	—	ns
TCkP	Input Clock Period		30	1000	25	1000	ns
	Clk2xSys to Clk2xSmp(5)		0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xRd(5)		0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xPhi(5)		9.0	tcyc/4	7.0	tcyc/4	ns
Timing Paramters							
TDEn	Data Enable(3)		—	–2.0	—	–2.0	ns
TDDis	Data Disable(3)		—	–1.0	—	–1.0	ns
TDVal	Data Valid	Load= 25pF	—	3.0	—	3.0	ns
TRSDS	Reset Set-up		15	—	15	—	ns
TDS	Data Set-up		9.0	—	8.0	—	ns
TDH	Data Hold(3)		–2.5	—	–2.5	—	ns
TFpCond	Fp Condition		—	35	—	30	ns
TFpBusy	Fp Busy		—	15	—	13	ns
TFpInt	Fp Interrupt		—	40	—	35	ns
TFpMov	Fp Move To		—	35	—	30	ns
TRExS	Exception Set-up (Run Cycle)		14	—	12	—	ns
TSExS	Exception Set-up (Stall Cycle)		12	—	10	—	ns
TExH	Exception Hold		0	—	0	—	ns
TRunS	Run Set-up		17	—	15	—	ns
TRunH	Run Hold		–2.0	—	–2.0	—	ns
TStallS	Stall Set-up		10	—	10	—	ns
TStallH	Stall Hold		–2.0	—	–2.0	—	ns
Reset Initialization							
TrstPLL	Reset Timing, Phase-lock on(4, 5)		3000	—	3000	—	Tcyc
Trst	Reset Timing, Phase-lock off(5)		128	—	128	—	Tcyc
Capacitive Load Deration							
CLD	Load Derate(6)		0.5	2.0	0.5	1.0	ns/25pF

2873 tbl 12

NOTES:
1. All timings are referenced to 1.5V.
2. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. With $\overline{\text{PllOn}}$ asserted, $\overline{\text{Reset}}$ must be asserted for the longer of 3000 clock cycles or 200 microseconds.
5. T_{cyc} is one CPU clock cycle (two cycles of a 2x clock).
6. No two signals on a given device will derate for a given load by a difference greater than 15%.
7. Clock transition time < 5ns.

6

AC ELECTRICAL CHARACTERISTICS FOR IDT79R3010AE(1, 3)
COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to +70°C, V_{CC} = +5.0V ± 5%)

Symbol	Parameter	Test Conditions	25.0 MHz		33.33 MHz		Unit
			Min.	Max.	Min.	Max.	
Clock							
TCkHigh	Input Clock High(2)	Note 7	8.0	—	6.0	—	ns
TCkLow	Input Clock Low(2)	Note 7	8.0	—	6.0	—	ns
TCkP	Input Clock Period		20	1000	15	1000	ns
	Clk2xSys to Clk2XSmp(5)		0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xRd(5)		0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xPhi(5)		5.0	tcyc/4	3.5	tcyc/4	ns
Timing Paramters							
TDEn	Data Enable(3)		—	–1.5	—	–1.0	ns
TDDIs	Data Disable(3)		—	–0.5	—	–0.5	ns
TDVal	Data Valid	Load= 25pF	—	2.0	—	2.0	ns
TRSDS	Reset Set-up		10	—	10	—	ns
TDS	Data Set-up		6.0	—	4.5	—	ns
TDH	Data Hold(3)		–2.5	—	–2.5	—	ns
TFpCond	Fp Condition		—	25	—	17	ns
TFpBusy	Fp Busy		—	10	—	7.0	ns
TFpInt	Fp Interrupt		—	25	—	18	ns
TFpMov	Fp Move To		—	25	—	16	ns
TRExS	Exception Set-up (Run Cycle)		11	—	9.0	—	ns
TSExS	Exception Set-up (Stall Cycle)		8.0	—	6.5	—	ns
TExH	Exception Hold		0	—	0	—	ns
TRunS	Run Set-up		15	—	12.5	—	ns
TRunH	Run Hold		–2.0	—	–1.5	—	ns
TStallS	Stall Set-up		9.0	—	7.0	—	ns
TStallH	Stall Hold		–2.0	—	–2.0	—	ns
Reset Initialization							
TrstPLL	Reset Timing, Phase-lock on(4, 5)		3000	—	3000	—	Tcyc
Trst	Reset Timing, Phase-lock off(5)		128	—	128	—	Tcyc
Capacitive Load Deration							
CLD	Load Derate(6)		0.5	1.0	0.5	1.0	ns/25pF

2873 tbl 13

NOTES:
1. All timings are referenced to 1.5V.
2. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. With $\overline{\text{PllOn}}$ asserted, $\overline{\text{Reset}}$ must be asserted for the longer of 3000 clock cycles or 200 microseconds.
5. Tcyc is one CPU clock cycle (two cycles of a 2x clock).
6. No two signals on a given device will derate for a given load by a difference greater than 15%.
7. Clock transition time < 2.5ns for 33MHz; clock transition time < 5ns for all other speeds.

AC ELECTRICAL CHARACTERISTICS FOR IDT79R3010AE(1, 3)
COMMERCIAL TEMPERATURE RANGE (Tc = 0°C to +90°C, Vcc = +5.0V ± 5%)

Symbol	Parameter	Test Conditions	40.0 MHz		Unit
			Min.	Max.	
Clock					
TckHigh	Input Clock HIGH(2)	Note 7	5.5	—	ns
TckLow	Input Clock LOW(2)	Note 7	5.5	—	ns
TckP	Input Clock Period		12.5	1000	ns
	Clk2xSys to Clk2XSmp(5)		0	tcyc/4	ns
	Clk2xSmp to Clk2xRd(5)		0	tcyc/4	ns
	Clk2xSmp to Clk2xPhi(5)		3.0	tcyc/4	ns
Timing Paramters					
TDEn	Data Enable(3)		—	–1.0	ns
TDDis	Data Disable(3)		—	–0.5	ns
TDVal	Data Valid	Load= 25pF	—	2.0	ns
TRSDS	Reset Set-up		8.0	—	ns
TDS	Data Set-up		4.0	—	ns
TDH	Data Hold(3)		–2.5	—	ns
TFpCond	Fp Condition		—	16	ns
TFpBusy	Fp Busy		—	6.0	ns
TFpInt	Fp Interrupt		—	17	ns
TFpMov	Fp Move To		—	16	ns
TRExS	Exception Set-up (Run Cycle)		8.5	—	ns
TSExS	Exception Set-up (Stall Cycle)		5.5	—	ns
TExH	Exception Hold		0	—	ns
TRunS	Run Set-up		9.0	—	ns
TRunH	Run Hold		–1.5	—	ns
TStallS	Stall Set-up		6.0	—	ns
TStallH	Stall Hold		–2.0	—	ns
Reset Initialization					
TrstPLL	Reset Timing, Phase-lock on(4, 5)		3000	—	Tcyc
Trst	Reset Timing, Phase-lock off(5)		128	—	Tcyc
Capacitive Load Deration					
CLD	Load Derate(6)		0.5	1.0	ns/25pF

2873 tbl 14

NOTES:
1. All timings are referenced to 1.5V.
2. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. With $\overline{\text{PllOn}}$ asserted, $\overline{\text{Reset}}$ must be asserted for the longer of 3000 clock cycles or 200 microseconds.
5. Tcyc is one CPU clock cycle (two cycles of a 2x clock).
6. No two signals on a given device will derate for a given load by a difference greater than 15%.
7. Clock transition time < 2.5ns.

6

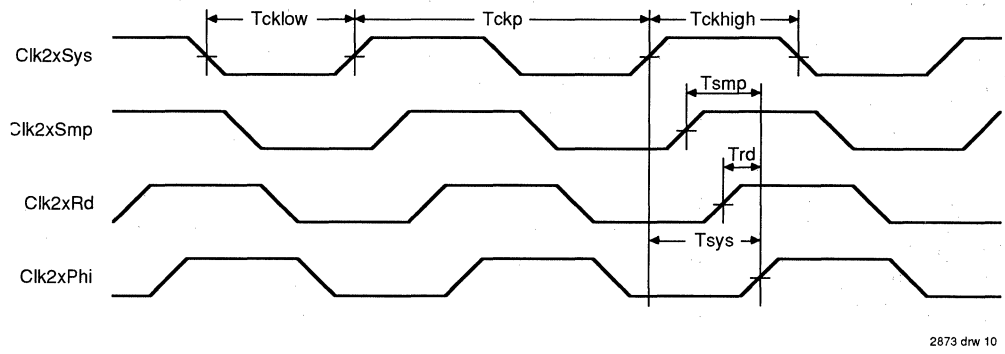


Figure 6. Input "2x" Clock Timing

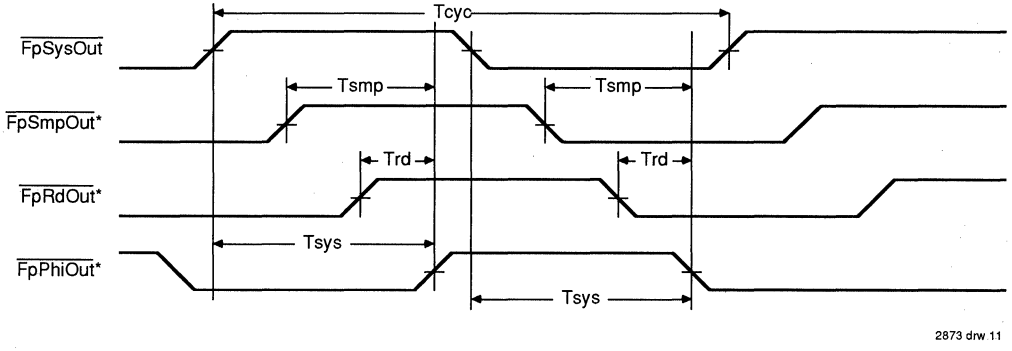


Figure 7. Processor Reference Clock

* These signals are not actually output from the floating point processor.
They are drawn to provide a reference for other timing diagrams.

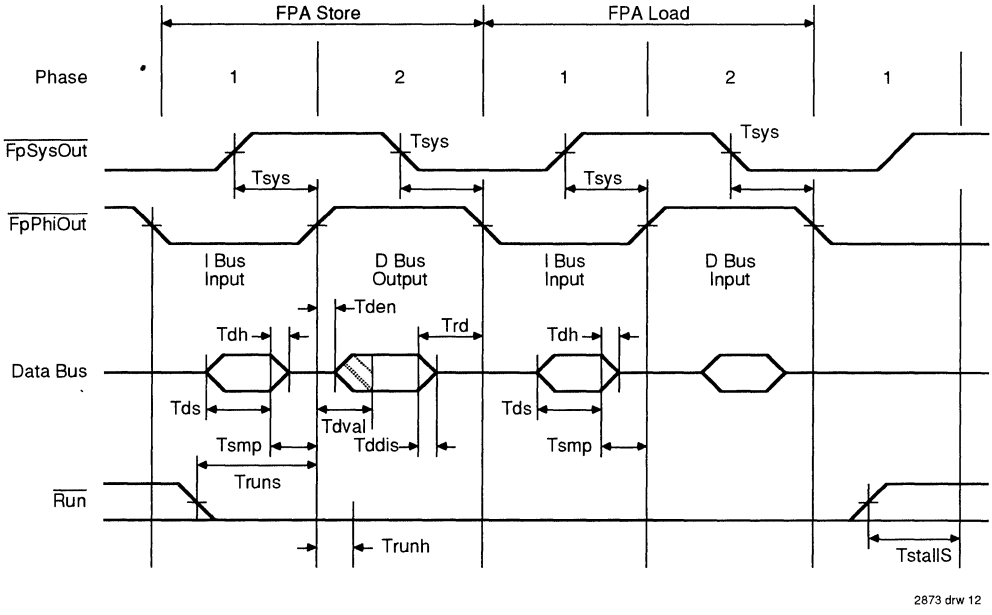


Figure 8. Floating Point Load/Store Timing

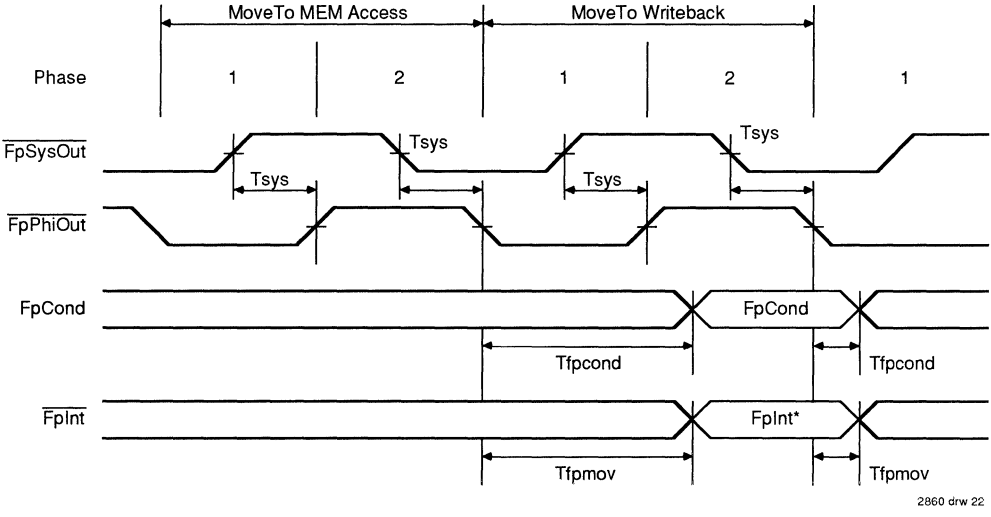


Figure 9. Move to FPC Status Timing

6

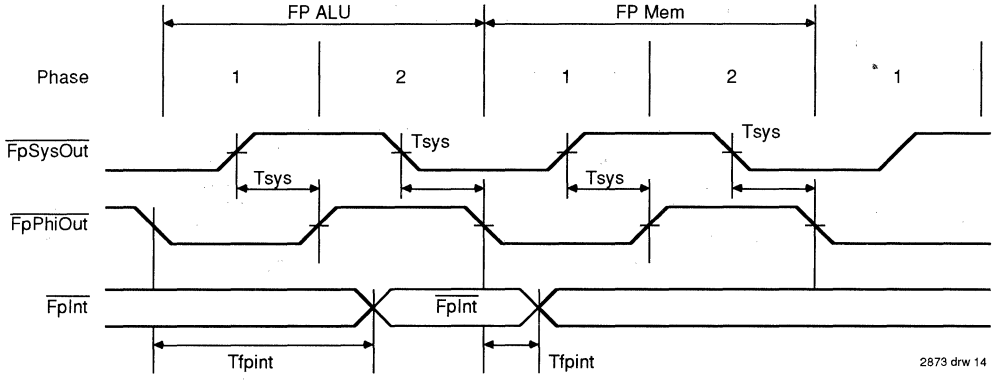


Figure 10. Floating Point Interrupt Timing

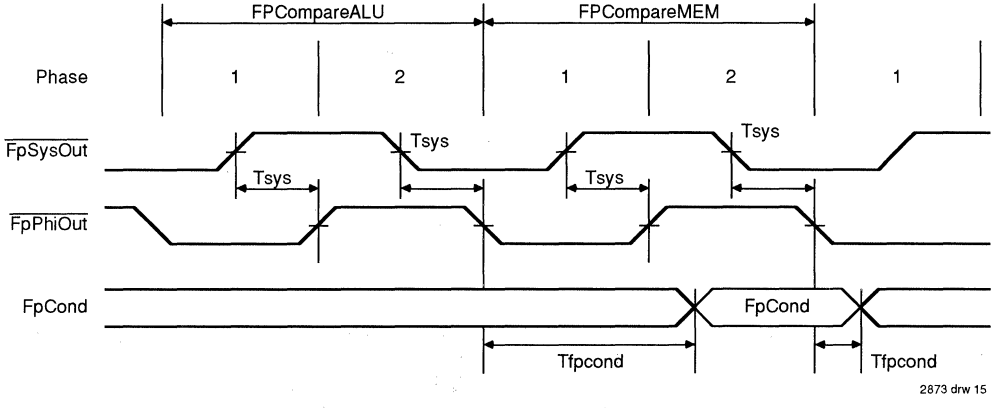


Figure 11. Floating Point Condition Timing

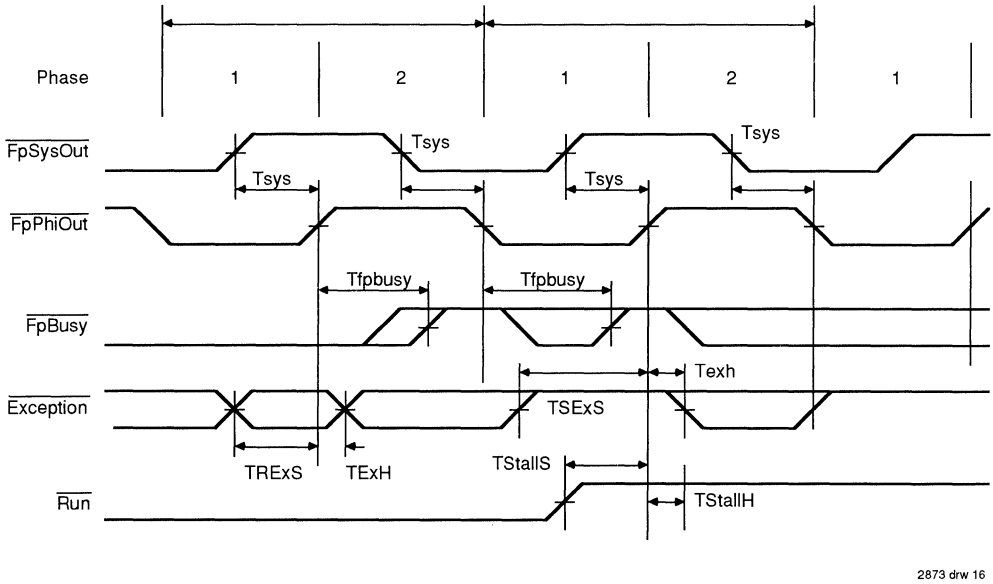


Figure 12. Floating Point Busy, Exception Timing

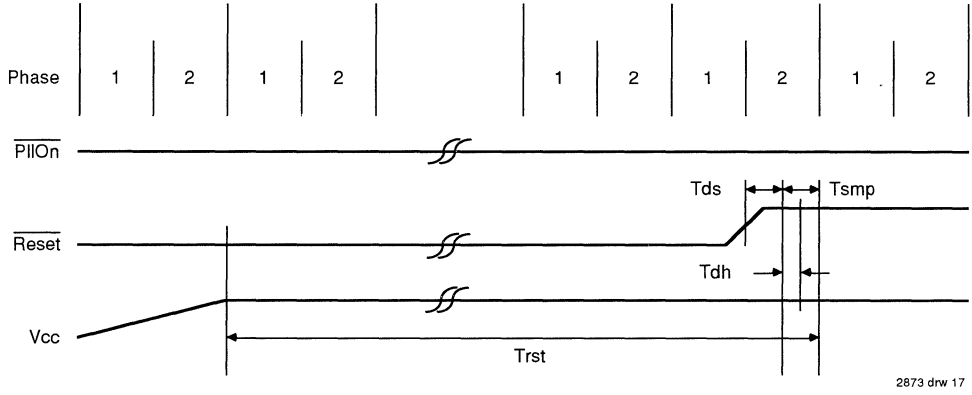
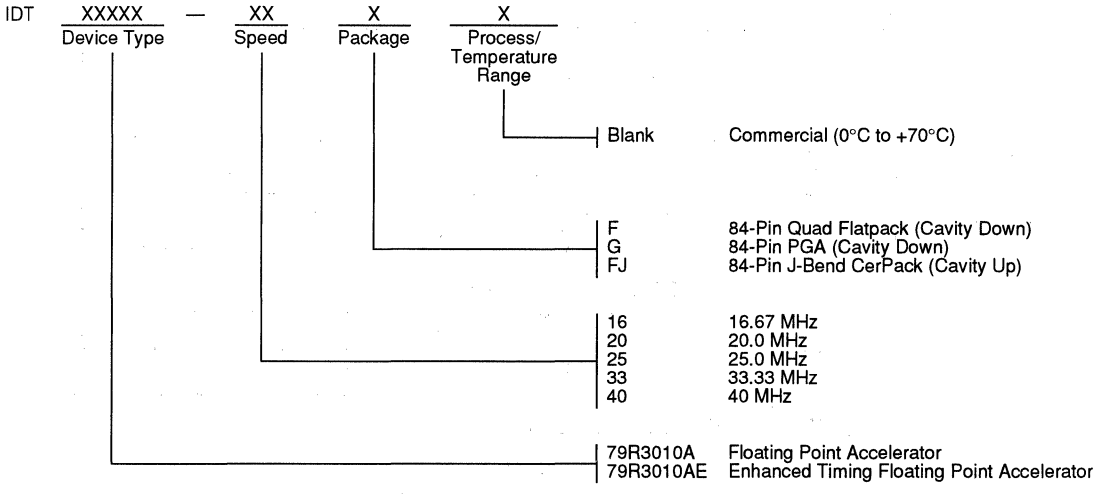


Figure 13. Power-On Reset Timing

ORDERING INFORMATION



2873 drw 18

VALID COMBINATIONS

IDT	79R3010A - 16, 20	All packages
	79R3010AE - 25, 33, 40	G

Integrated Device Technology, Inc.

BiCameral™ CacheRAM™ 288K (16K x 9 x 2) FOR RISC CACHES

PRELIMINARY
IDT71B229S

FEATURES:

- Supports the R3000 and R3001 to 40MHz
- BiCameral organization:
  - — Split instruction/data cache support
  - — No bank-switching timing contention
- Single address bus
- Single data bus
- Separate write enable and output enable for each bank
- Standard read and write control interface
- Internal address latches
- 32-pin 300mil SOJ package

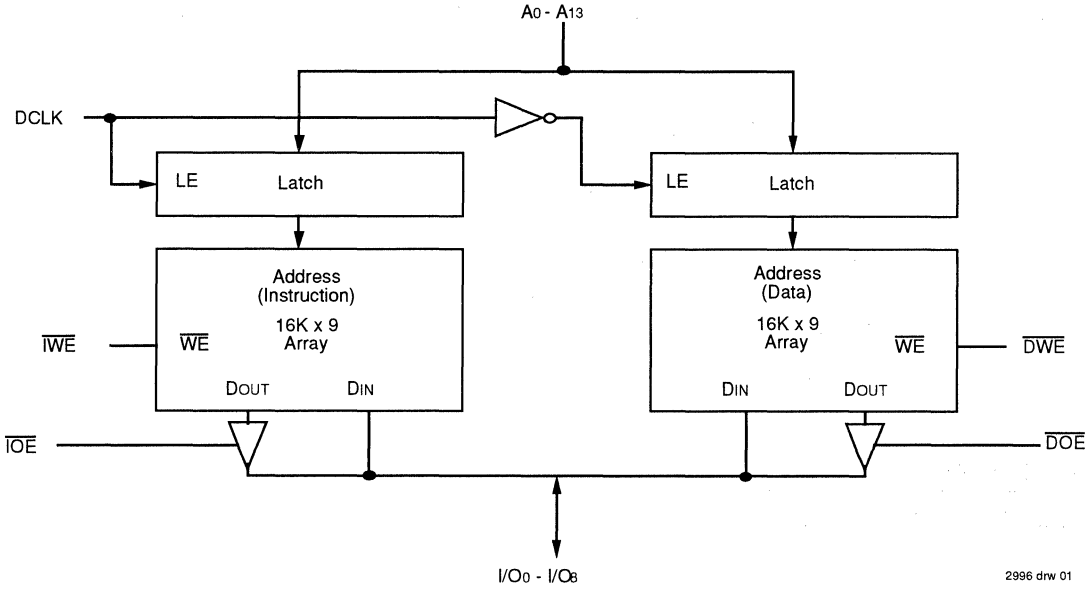
DESCRIPTION:

The IDT71B229 is a BiCameral CacheRAM specifically designed to support the split instruction and data caches of the IDT79R3000 microprocessor. A complete 128KB cache for the R3000 or the R3500 can be built with only six to seven IDT71B229s (depending on the main memory size supported by the system), while an R3001 cache can be built with five to six parts. CPU clock frequencies up to 40MHz are supported. The small 300mil package allows a 128KB cache to fit in a circuit board area of approximately two square inches.

Internal address latches eliminate the need for external latches. The BiCameral (two bank) organization reduces the number of devices required to support the R3000's split-cache architecture and eliminates contention problems encountered when one RAM bank is being enabled while the other is being disabled. All timing parameters have been optimized to support the complete range of R3000 clock speeds, simplifying R3000 cache design.

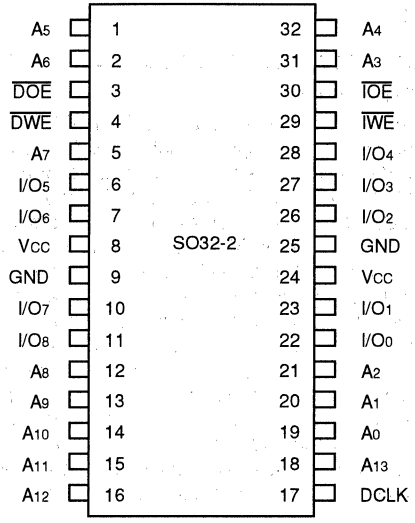
The IDT71B229 provides dense caches in low board space while consuming minimum power.

FUNCTIONAL BLOCK DIAGRAM



6

PIN CONFIGURATIONS



2996 drw 02

TRUTH TABLE 1

$\overline{IOE}$	$\overline{IWE}$	$\overline{DOE}$	$\overline{DWE}$	I/O(0:8)	Function
H	H	L	H	Out, D Bank	Read D Bank data
H	H	H	L	High-Z	Write data to D Bank
L	H	H	H	Out, I Bank	Read I Bank data
H	L	H	H	High-Z	Write data to I Bank
H	H	H	H	High-Z	No Activity
L	L	X	X	High-Z	Not Allowed
L	X	L	X	High-Z	Not Allowed
L	X	X	L	High-Z	Not Allowed
X	L	L	X	High-Z	Not Allowed
X	L	X	L	High-Z	Not Allowed
X	X	L	L	High-Z	Not Allowed

2996 tbl 01

TRUTH TABLE 2(1)

DCLK	I Address Latch	D Address Latch
L	Transparent	Latched
H	Latched	Transparent

2996 tbl 02

NOTE:
1. L = LOW, H = HIGH, X = Don't Care, = Unrelated, High-Z = High-Impedance

PIN DESCRIPTION

Name	Description
DCLK	DCLK, when HIGH, allows the address inputs to flow through the D bank's address latch. Conversely, the address in the I bank's latch is held during a HIGH input on DCLK. Taking DCLK LOW freezes data in the D bank's address latch and allows addresses to flow through the I bank's address latch.
$\overline{IOE}$	I Output Enable enables the data outputs from the I bank onto the data input/output pins. $\overline{IOE}$ must not be asserted simultanteously with the $\overline{DOE}$, $\overline{DWE}$ or $\overline{IWE}$ pins.
$\overline{DOE}$	This is an input which enables the data outputs from the D bank onto the data input/output pins. $\overline{DOE}$ must not be asserted simultanteously with the $\overline{IOE}$, $\overline{IWE}$ or $\overline{DWE}$ pins.
$\overline{IWE}$	I Write Enable, when LOW, gates data from the input/output pins into the RAM at the I bank address indicated by the output of the I bank address latch. Neither $\overline{DOE}$ nor $\overline{IOE}$ should be enabled during a write operation.
$\overline{DWE}$	D Write Enable is an input which is taken LOW to gate data from the input/output pins onto the RAM at the address being output from the D bank address latch. Neither $\overline{DOE}$ or $\overline{IOE}$ should be asserted during a write operation.
Addr(0:13)	The fourteen address inputs are used to access any of the 16,384 locations in either the D or I bank. When an address latch is in the transparent state, these pins are routed directly to that latch's RAM bank. Taking the latch into its latched state causes that RAM bank to ignore subsequent changes on the address input pins.
I/O0:8	The input/output bus comprises nine signals whose functions are determined by the state of the $\overline{IOE}$, $\overline{IWE}$, $\overline{DOE}$ and $\overline{DWE}$ pins. During Output Enables, data is output upon these pins from the selected RAM bank from an address pointed to by the outputs of that bank's address latch. When either Write Enable is asserted, data can be written from these pins into the selected bank's RAM at the address being output by that bank's address latch. When $\overline{IOE}$, $\overline{IWE}$, $\overline{DOE}$ and $\overline{DWE}$ are all inactive, the input/output pins are floated in a high-impedance state.

2996 tbl 03

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE: 2996 tbl 04
1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input HIGH Voltage	2.2	—	V_{CC}+0.5	V
V_{IL}	Input LOW Voltage	–0.5[1]	—	0.8	V

NOTE: 2996 tbl 05
1. V_{IL} (min.) = –3.0V for pulse width less than 20ns.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0(2)	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTES: 2996 tbl 06
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC}+0.5V.

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DC ELECTRICAL CHARACTERISTICS(1, 2)

(V_{CC} = 5.0V ± 5%)

Symbol	Parameter	71B229S12 Com'l.	71B229S16 Com'l.	71B229S22 Com'l.	71B229S28 Com'l	Unit
I_{CC1}	Operating Power Supply Current Outputs Open, V_{CC} = Max., f = 0	190	180	170	160	mA
I_{CC2}	Dynamic Operating Current Outputs Open, V_{CC} = Max., f = f_{MAX}	250	230	200	190	mA

NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX}=1/t_{CYC} with address bits cycling at maximum frequency. f = 0 means no inputs change.

2996 tbl 07

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMERATURE AND SUPPLY VOLTAGE (V_{CC} = 5.0V ± 5%)

Symbol	Parameter	Test Condition	IDT71B229S Min.	IDT71B229S Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

2996 tbl 08

ACCESS TIME AND CLOCK FREQUENCY EQUIVALENTS

R3000/1 Clock Frequency	71B229 Access Time
40 MHz	12 ns
33 MHz	16 ns
25 MHz	22 ns
20 MHz	28 ns

2996 tbl 09

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5V ± 5%

2996 tbl 10

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1A, 1B, 1C

2996 tbl 11

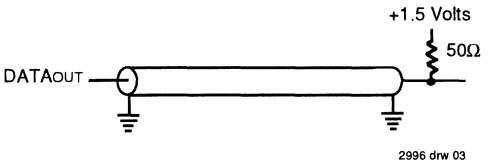


Figure 1A. AC Test Load

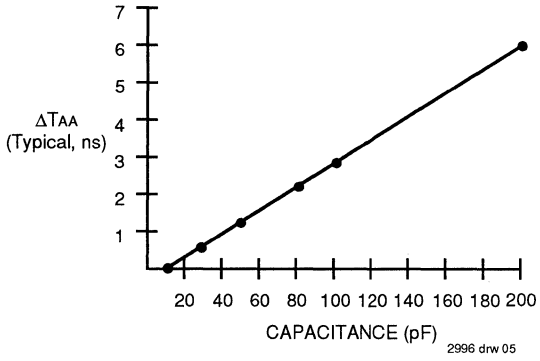
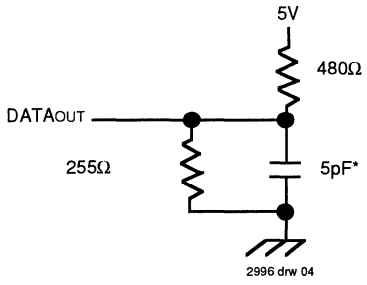


Figure 1C. Lumped Capacitive Load, Typical Derating Curve



*Includes scope and jig.

Figure 1B. AC Test Load (for tOLZ & tOHZ)

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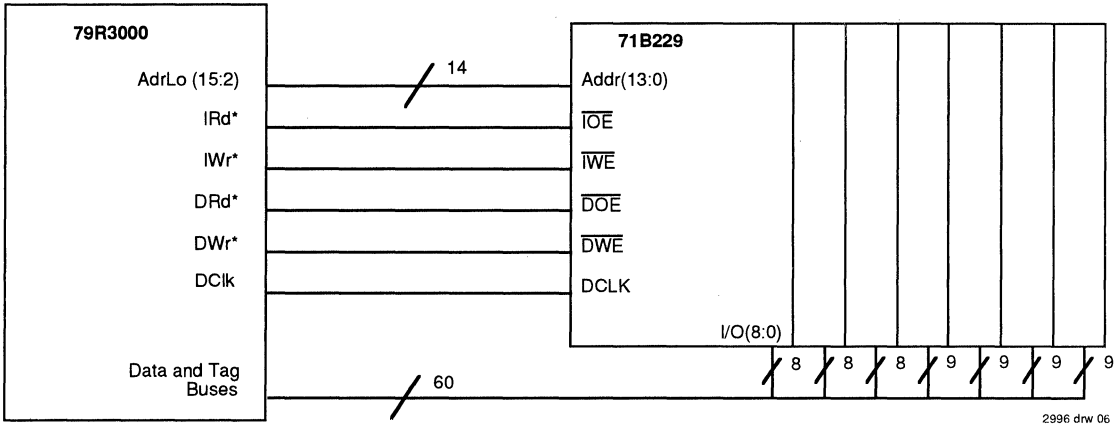


NOTE:
1. Loading of the IRd, IWr, DRd and DWr signals should be split evenly between the pair of R3000 pins dedicated to each of these functions.

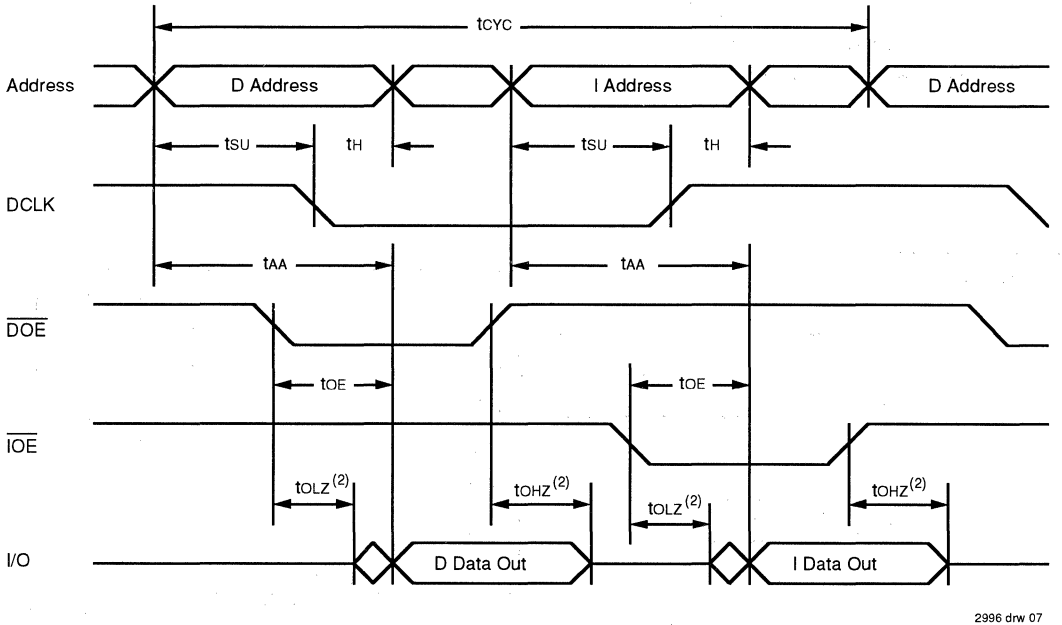
Figure 2. Example of Cache Memory System Block Diagram

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 5%, All Temperature Ranges)

Symbol	Parameter	71B229S12		71B229S16		71B229S22		71B229S28		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
tCYC	Read Cycle Time(1)	25	—	30	—	40	—	50	—	ns
tSU	Address Setup Time	6	—	8	—	11	—	14	—	ns
tH	Address Hold Time	3	—	3	—	4	—	6	—	ns
tAA	Address Access Time	—	12	—	16	—	22	—	28	ns
tOE	Output Enable Time	—	5	—	7	—	10	—	13	ns
tOLZ(2)	Output Enable to Output in Low-Z	2	—	2	—	2	—	2	—	ns
tOHZ(2)	Output Disable to Output in High-Z	2	5	2	6	2	8	2	10	ns

NOTES:
2996 tbl 12
1. One cycle includes both a D bank read or write and an I bank read or write.
2. This parameter is guaranteed with the AC test load, Figure 1B,due to device characterization, but is not production tested.

TIMING WAVEFORM OF READ CYCLES(1)



2996 drw 07

NOTES:
1. $\overline{DWE}$ and $\overline{IWE}$ must be high during read cycles.
2. The transition is measured ±200mV from steady state with load in Figure 1B.

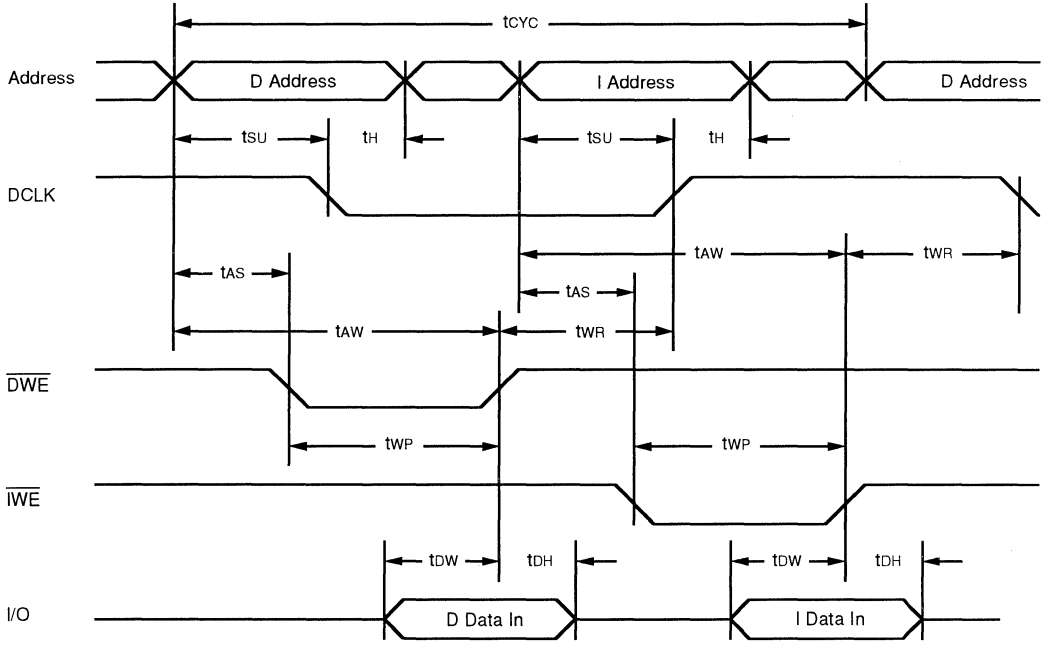
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 5%, All Temperature Ranges)

Symbol	Parameter	71B229S12		71B229S16		71B229S22		71B229S28		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle										
tCYC	Write Cycle Time(1)	25	—	30	—	40	—	50	—	ns
tSU	Address Setup Time	6	—	8	—	11	—	14	—	ns
tH	Address Hold Time	3	—	3	—	4	—	6	—	ns
tAW	Address to End-of-Write	18	—	20	—	22	—	28	—	ns
tAS	Address to Start-of-Write	5	—	5	—	5	—	5	—	ns
tWR	Write Recovery Time	–1	—	–1	—	–1	—	–1	—	ns
tWP	Write Pulse Width	10	—	13	—	16	—	20	—	ns
tDW	Data to Write Time Overlap	5.5	—	7	—	9	—	11	—	ns
tDH	Data Hold from Write Time	2	—	2	—	2	—	2	—	ns

NOTE:
1. One cycle includes both a D bank read or write and an I bank read or write.

2996 tbl 13

TIMING WAVEFORM OF WRITE CYCLES(1, 2)

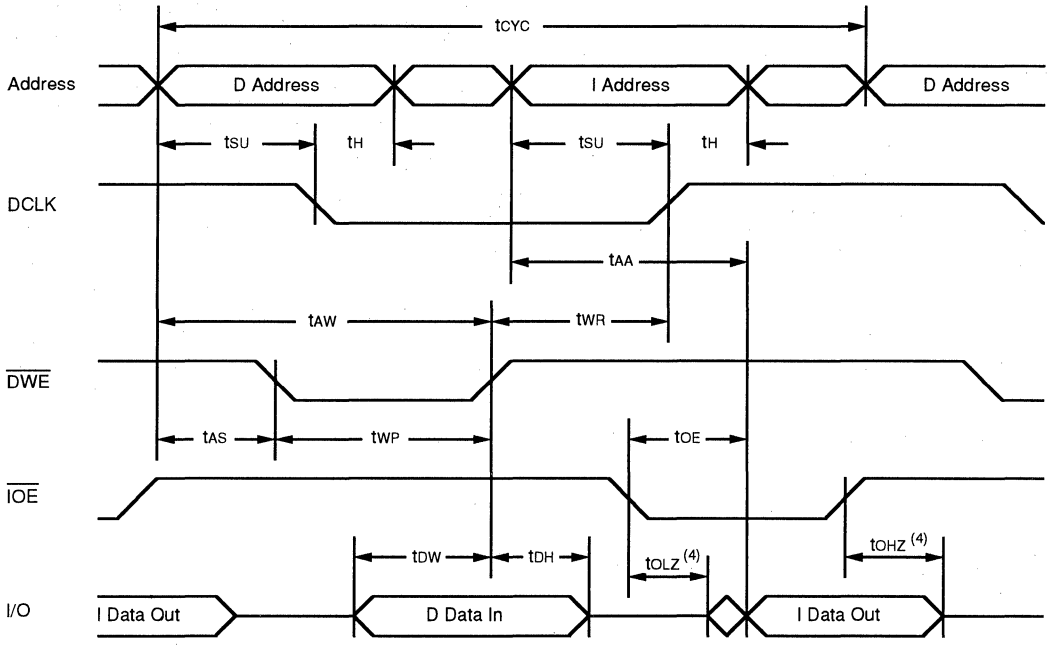


NOTES:
1. $\overline{DOE}$ and $\overline{IOE}$ are high during write cycles.
2. $\overline{DWE}$ must be high or DCLK must be low during all address transitions. Likewise, $\overline{IWE}$ or DCLK must be high during all address transitions.

2996 drw 08

6

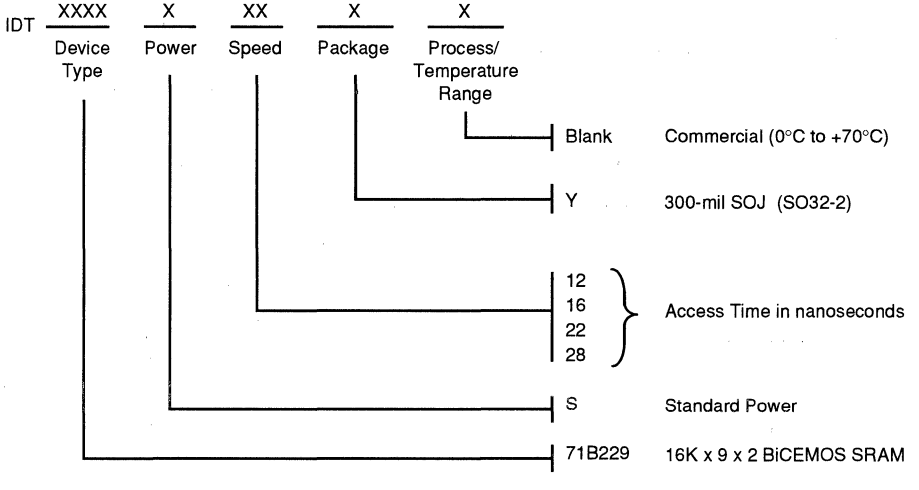
TIMING WAVEFORM OF MIXED READ AND WRITE CYCLES(1, 2, 3)



2996 drw 09

NOTES:
1. $\overline{DOE}$ and $\overline{IOE}$ are high during write cycles.
2. $\overline{DWE}$ must be high or DCLK must be low during all address transitions. Likewise, $\overline{IWE}$ or DCLK must be high during all address transitions.
3. $\overline{DWE}$ and $\overline{IWE}$ must be high during read cycles.
4. The transition is measured ±200mV from steady state with load in figure 1B.

ORDERING INFORMATION



2996 drw 10

Integrated Device Technology, Inc.

RISC CPU WRITE BUFFER

IDT79R3020

FEATURES:

- Temporary storage buffers to enhance the performance of the IDT79R3000 RISC CPU processor
- Allows for write operations by the RISC CPU processor during Run cycles
- Each Write Buffer has four locations to handle an 8-bit address slice and a 9-bit data slice (including a parity bit)
- High-speed CMOS technology
- Pin, functionally and software compatible with the MIPS Computer Systems R2020 Write Buffer
- Speeds from 16.7 to 40MHz
- Also works with Intel i486™ for Writeback secondary cache

DESCRIPTION:

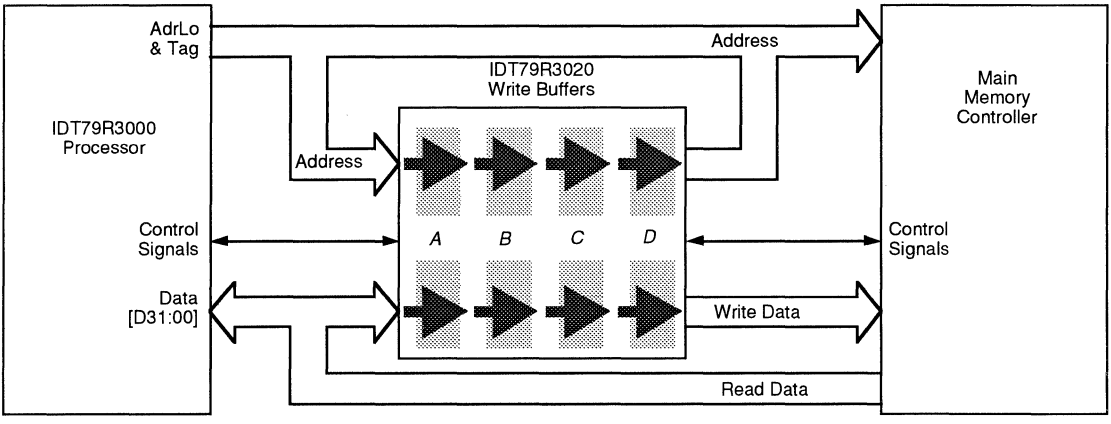
The IDT79R3020 Write Buffer enhances the performance of IDT79R3000 systems by allowing the processor to perform write operations during Run cycles instead of resorting to time-consuming stall cycles. Each IDT79R3020 device handles an 8-bit slice of address, and a 9-bit slice of data (one parity bit per byte); thus, four IDT79R3020s provide 4-deep buffering of 32 bits of address and 36 bits of data and parity. Figure 1 illustrates the functional position of the Write Buffer in an IDT79R3000 system.

Whenever the processor performs a write operation, the Write Buffer captures the output data and its address (including the access type bits). The Write Buffer can hold up to four data-address sets while it waits to pass the data on to main memory. Transfers from the processor to the write buffers occur synchronously at the cycle rate of the processor and the write buffer signals the processor if it is unable to accept data. The write buffer also provides a set of handshake signals to communicate with a main memory controller and coordinate the transfer of write data to main memory.

The sections that follow describe these IDT79R3020 Write Buffer interfaces:

- the processor-Write Buffer interface
- the Write Buffer-main memory interface
- a miscellaneous, Write Buffer-board control interface.

WRITE BUFFER



5002 drw 01

Figure 1. The IDT79R3020 Write Buffer in an IDT79R3000 System

WRITE BUFFER - IDT79R3000 PROCESSOR INTERFACE

Figure 2 shows the signals comprising the Write Buffer interface to the IDT79R3000 (all descriptions assume that four IDT79R3020 Write Buffers are used to implement a 32-bit, buffered interface). The AdrLo bus and Tag bus bits from the processor are both connected to the Write Buffer to form a 32-bit physical address that is captured by the buffers. Thirty-two bits of data, four bits of parity, and two access type bits are also captured by the Write Buffer. The paragraphs that follow describe the Write Buffer-processor interface signals and the timing of processor-to-Write Buffer data transfers.

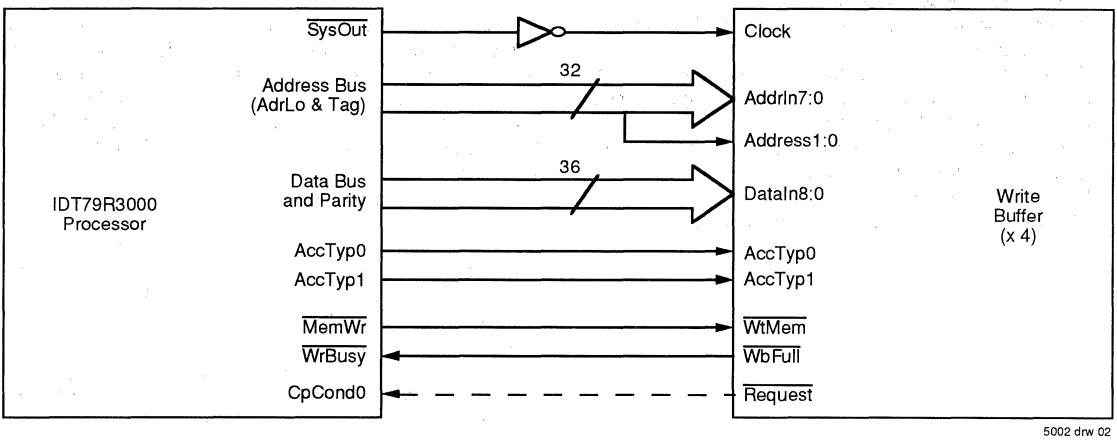


Figure 2. Write Buffer — IDT79R3000 Processor Interface

Write Buffer-Processor Interface Signals

Clock

An inverted version of the R3000s SysOut signal from the R3000 processor that synchronizes data transfers. The Write Buffer uses the trailing edge of *Clock* to latch the contents of the AdrLo bus and uses the leading *Clock* edge to latch the contents of the Data and Tag buses.

DataIn8:0

Nine input data lines from the IDT79R3000 processor's Data bus (eight bits of data and one bit of parity).

AddrIn7:0

Eight input address lines from the IDT79R3000 processor. The address lines are taken from the AdrLo and Tag buses.

Address1:0

The two least significant address bits from the IDT79R3000 processor. These two address bits must be connected to all four Write Buffers and are used in conjunction with the access type *(AccTyp1:0)* signals, the *Position1:0* signals, and the *BigEndian* signal to determine which byte(s) in a word are being written into a particular Write Buffer.

AccTypIn1:0

The access type signals from the IDT79R3000 processor specifying the size of a data access: word, tri-byte, half-word, or byte.

WtMem

This input is connected to the MemWr signal from the IDT79R3000 processor that is asserted whenever the processor is performing a store (write) operation.

Request

The primary purpose of this signal is to request access to memory and is described later when the Write Buffer-Main Memory Interface is discussed. The Request signal can also be connected to the CpCond0 input of the IDT79R3000 and can then be tested by software to determine if there is any data in the Write Buffer. Since Request is deasserted if there is no data in the Write Buffer, software can determine if a previous write operation (for example, to an I/O device) has been completed before initiating a read or read status operation from that device.

WbFull

The Write Buffer asserts this signal to the IDT79R3000s WrBusy input whenever it cannot accept any more data; that is, when the current write will fill the buffer or the buffer has all address-data pairs occupied. The IDT79R3000 processor performs a write-busy stall if it needs to store data while the WbFull/WrBusy signal is asserted.

Data & Address Connections

Figure 3 illustrates how four Write Buffers are connected to the address and data outputs of the IDT79R3000 processor.

Address Inputs

Each Write Buffer device has eight address inputs (AdrIn7:0). The four low-order bits (AdrIn3:0) are clocked into the device on the trailing edge of the Clock signal and are taken from the IDT79R3000s AdrLo bus. The four high-order bits (AdrIn7:4) are clocked into the device on the rising edge of the Clock signal and are taken from the IDT79R3000s Tag bus.

Each device also has separate inputs (Address1, Address0) for the two low-order bits from the AdrLo bus. These bits must be input to each device since they comprise the byte pointer. Note in Figure 3 that the two low-order AdrIn inputs (AdrIn1:0) to Write Buffer device 0 are connected to ground since the Address1, Address0 inputs already supply these bits to the device.

Data Inputs

Each Write Buffer device has nine data inputs that are clocked into the device on the leading edge of the Clock signal and are taken from the IDT79R3000s Data bus. In Figure 3, each device captures eight bits of data and one bit of parity. Also note that the data bits assigned to each device correspond to the address bits connected to the device. This arrangement is required since data selection is dependent on a combination of the AccType signals and the two low order address bits. The arrangement also simplifies system utilization of the "Read Error Address" feature described later.

The *Position1* and *Position0* signals shown in Figure 3 specify the nibble position within a halfword that each write buffer device comprises.

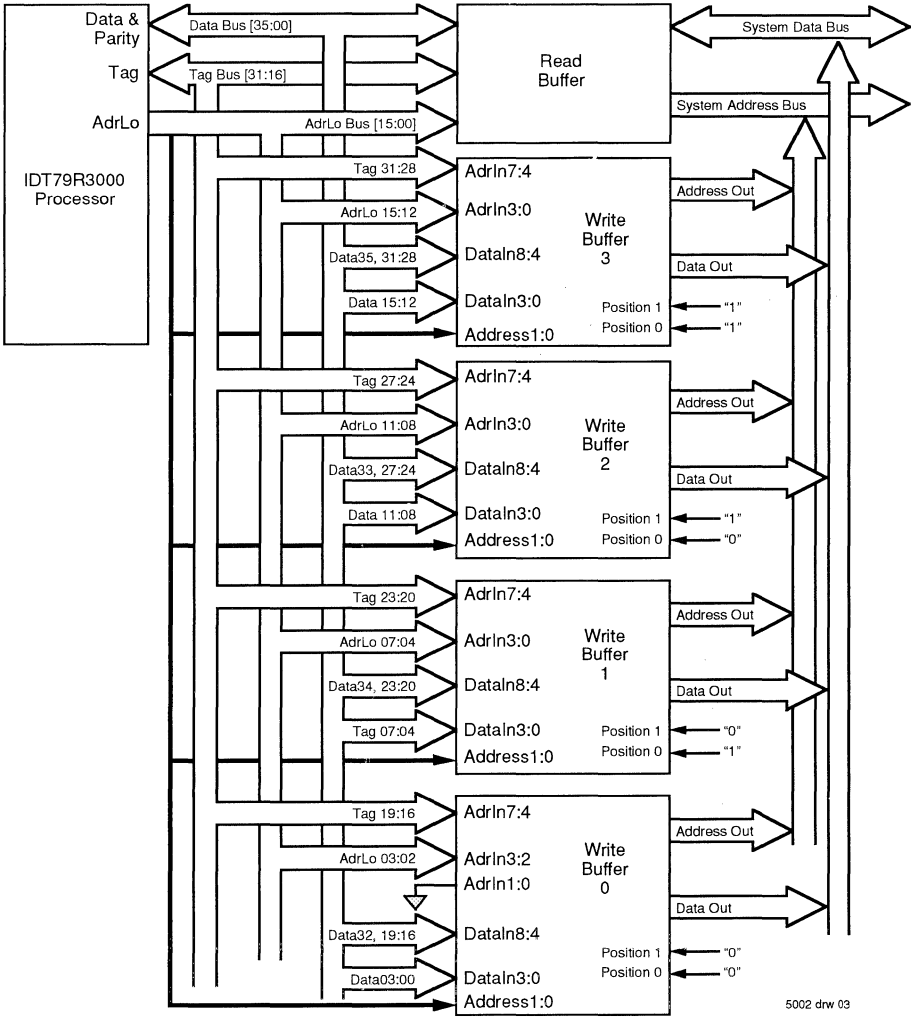


Figure 3. Write Buffer Data and Address Line Connections

Write Buffer - Processor Timing

Transfers between the processor and the Write Buffers occur synchronously: the Clock signal from the processor is input to the Write Buffers and used to clock the address and data information into the Write Buffers' latches. Figure 4 illustrates the timing for the processor-Write Buffer interface.

When the $\overline{\text{WrtMem}}$ signal is asserted, the low-order address bits, and the Address 1:0 inputs, are latched on the trailing edge of the Clock signal (1). The rising edge of Clock (2) is used to latch the high-order address bits, the access type inputs and the contents of the data bus.

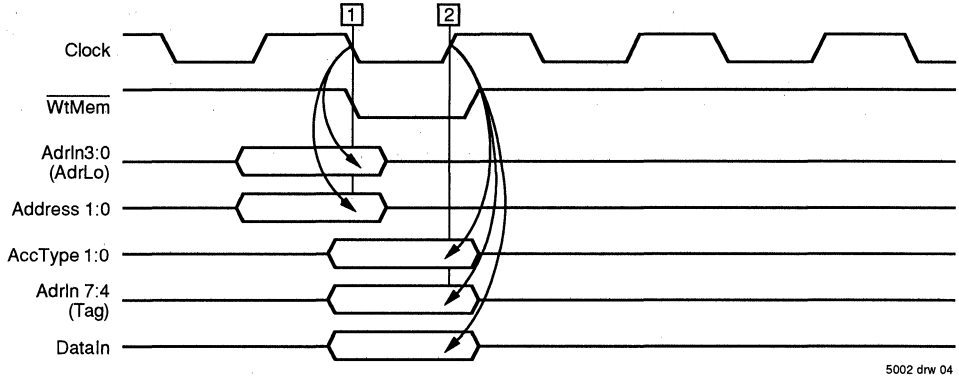


Figure 4. Processor — Write Buffer Interface Timing

WRITE BUFFER - MAIN MEMORY INTERFACE

Figure 5 shows the signals comprising the Write Buffer interface to main memory. This interface is essentially decoupled from the Write Buffer-processor interface: although some synchronization of the memory interface signals and the Clock signal is required, the handshaking signals in this interface have no direct connection to the operation of the Write Buffer-processor interface.

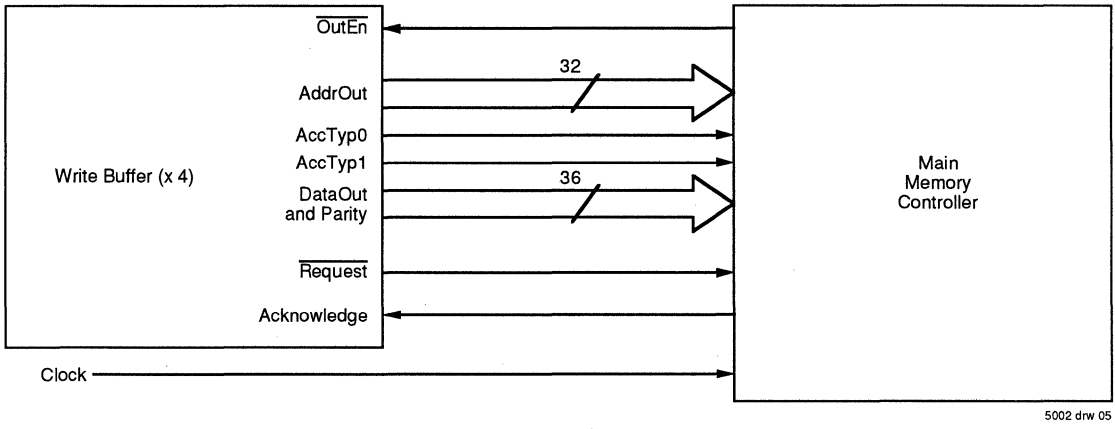


Figure 5. Write Buffer — Main Memory Interface

Write Buffer - Main Memory Interface Signals

Each Write Buffer provides the following signals that comprise the interface to a main memory controller:

AddrOut 7:0

Eight address line output from each Write Buffer.

DataOut 8:0

Nine data lines from each Write Buffer (eight bits of data and one bit of parity).

AccTypOut 1:0

The access type signals from the Write Buffer specifying the size of a data access: word, tri-byte, half-word, or byte.

$\overline{\text{OutEn}}$

The memory controller asserts this write input to enable the tri-state outputs of the IDT79R3020 address data signals, and AccTyp Out.

$\overline{\text{Request}}$

The Write Buffer asserts this signal to inform the main memory system that it has data to be written to memory.

Acknowledge

The main memory system asserts this signal when it has captured the data presented by the Write Buffer on the DataOut lines.

Write Buffer - Main Memory Interface Timing

Figure 6 illustrates the timing for the transfer of data from the Write Buffer to the main memory system. The sequence illustrated in this figure is as follows:

1. When the Write Buffer has a data-address pair for transfer to the memory system, it asserts the $\overline{\text{Request}}$ signal.
2. When memory system is ready to handle the Write Buffer data, it asserts the $\overline{\text{OutEn}}$ signal to enable the Write Buffers' address and data outputs onto the system buses.
3. When memory system no longer requires the Write Buffer address and data outputs, it asserts the Acknowledge signal.
   The Write Buffer responds to this signal by discarding the address-data pair that was just output.
4. The memory system can deassert the $\overline{\text{OutEn}}$ signal to return the Write Buffers' address and data outputs to their tri-state condition.
5. Since the $\overline{\text{Request}}$ signal remains asserted, the memory system asserts the $\overline{\text{OutEn}}$ signal again to enable the next address-data pair onto the system buses.
6. When memory system has accepted the second address-data pair, it again asserts the Acknowledge signal. If the Write Buffer is now empty, it responds to this signal by deasserting the $\overline{\text{Request}}$ signal.

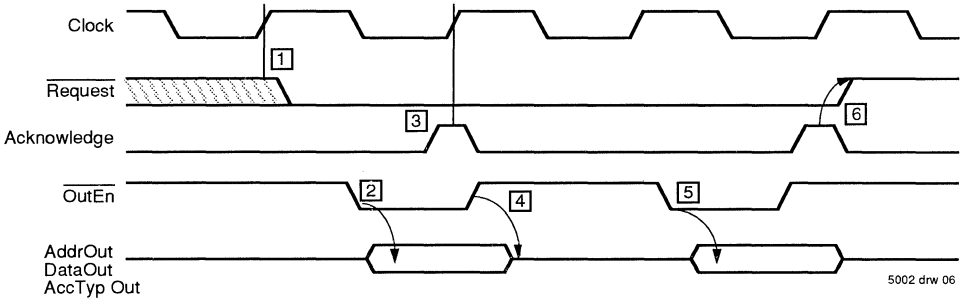


Figure 6. Write Buffer — Main Memory Interface Timing

Note that the buffer's interface to main memory is not completely asynchronous: assertion of the $\overline{\text{Request}}$ signal by the Write Buffer is synchronized with the rising edge of Clock, and the Acknowledge signal input by main memory has a minimum set up and hold time in relation to the Clock signal.

MISCELLANEOUS WRITE BUFFER - BOARD LOGIC INTERFACE

The Write Buffers support several functions that utilize signals that do not fit neatly into the descriptions of either the processor or main memory interfaces. These functions and signals typically involve miscellaneous logic on a CPU board and include the following:

- byte gathering
- configuration connections (Big Endian, Position 1:0)
- address matching logic
- error address latch logic

The sections that follow describe each of these categories.

Byte Gathering

The Write Buffers perform byte (half-word, tri-byte and word) gathering to decrease the number of write transfers to same location; that is, sequential writes to the same WORD address have their data combined into the same address-data pair buffer.

Byte gathering is prohibited in the address-data pair that is currently available to the memory controller. Thus, the first write into an empty Write Buffer will not have subsequent writes gathered into it because it is currently available for output to memory. Writes to the same location (byte) may be overwritten in the Write Buffer if the gathering is not prohibited by the preceding rule.

The Write Buffers present address-data pairs to the main memory controller in the sequence in which they were received from the processor except in the case of gathered data, where bytes or half words can be collected and written to main memory in a single write operation. If the address-data pair buffer is scheduled to be output, then gathering is inhibited and the buffer contents are presented to the main memory controller. Subsequent writes are then placed in another buffer. No reliance should be placed in any aspect of gathering (except that it only involves sequential writes to the same word address) as it is not readily deterministic. Non-sequential writes to the same word address are not gathered.

Note that gathering can require that two main memory controller references be used to empty a single Write Buffer entry. For example, this can occur if Bytes 0 and 3 of a word are sequentially written. Where order in writing is important, such as in I/O controllers, software should avoid sequential accesses to the same word. In cases where write-read access ordering is important but reading of the write location is not desired, such as during I/O, then a write followed by a write to a dummy location followed by a read of the dummy location will insure the first write has occurred before continuing. Alternatively, the Request signal can be tested to determine that the Write Buffer is empty.

Configuration Logic Connections

Because of their byte gathering capability, each buffer device internally maintains a record of each valid byte in an address/data pair. To do this, each device must have a way of determining which data bits within a word it is handling. The following signals determine how the write buffers handle data that is written to the devices:

- **Position 1, Position 0** - these signals (in conjunction with Big Endian) determine how each Write Buffer decodes the Address 1/0 and AccType 1/0 to determine if it should store the data inputs. Refer to Figure 3 for an illustration of how data bits are assigned to Write Buffer devices based on their *position*.
- Big Endian - When asserted, byte 0 is the leftmost, most significant byte (big-endian): when deasserted, byte 0 is the rightmost, least-significant byte (little-endian).
- **Address 1, Address 0** - these signals (taken from the AdrLo bus) must be connected to all buffer devices since they determine which byte within a word is being accessed.
- **AccType 1, AccType 0** - these inputs signals specify the data size of a write operation as shown in Table 1.

Table 1 shows how these signals operate to specify how bytes are saved within the Write Buffers.

Access Type 1 0	Address 1 0	Bytes Accessed: 31 Big–Endian 0	Bytes Accessed: 31 Little–Endian 0
1 1 (word)	0 0	0 1 2 3	3 2 1 0
1 0 (triple-byte)	0 0	0 1 2	2 1 0
	0 1	1 2 3	3 2 1
0 1 (halfword)	0 0	0 1	1 0
	1 0	2 3	3 2
0 0 (byte)	0 0	0	0
	0 1	1	1
	1 0	2	2
	1 1	3	3

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Table 1. Byte Specifications for Write Operations

The lower two address bits of the device in position zero (as determined by the two POSITION inputs) are inhibited; that is, they are not stored directly as they are output on the AdrLo bus. Instead, on output, the lower two address bits are generated from the indication of the positions of the valid data bytes as determined by above table.

MatchOut/Matchin Logic and Read Conflicts

Whenever the processor references main memory (either a write or a read reference), the Write Buffers compare the word address from the CPU with the word addresses stored in the buffers. If any word address matches, the buffers assert signals that can be used by the main memory controller to ensure that the Write Buffer is emptied before the read access with the conflicting address has been performed.

Figure 7 illustrates the Write Buffer signals involved in address comparison logic. Each write buffer provides four output signals (MatchOut A, B, C, and D) which correspond to the four buffer ranks (A, B, C, D) in each device as shown in Figure 1. These MatchOut signals can be externally NANDed as shown in Figure 7 to determine if the address being input matches those in any rank of the Write Buffer.

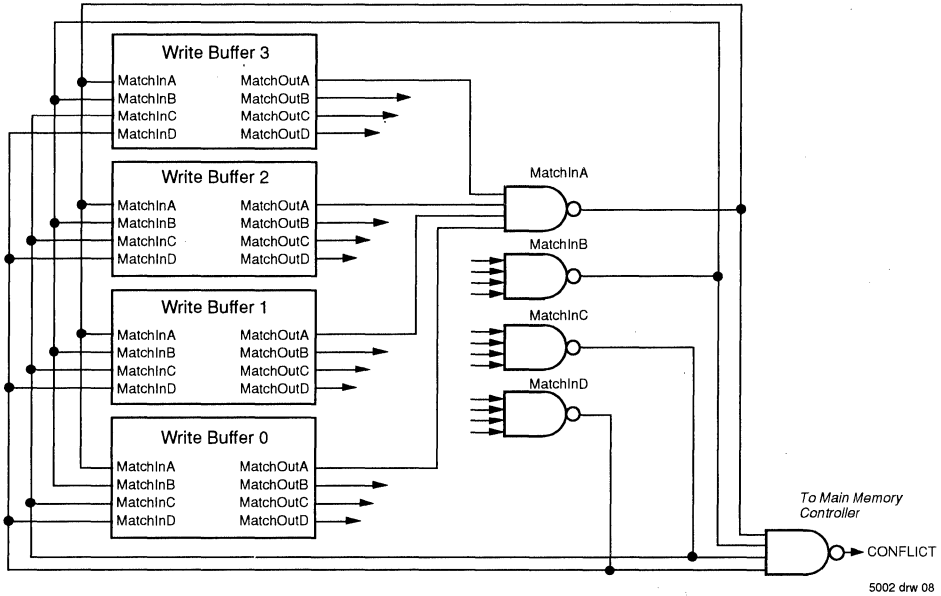

Figure 7. Write Buffer MatchOut/Matchin Logic

The outputs of the NAND gates are fed into Write Buffers via the MatchIn A, B, C, and D signals and are used within each device as part of the byte gathering logic. The NAND gate outputs can be NANDed together as shown in Figure 7 with the resultant signal used (in conjunction with the processor's $\overline{\text{MEMRD}}$ signal) to alert the main memory controller logic that there is a pending buffered write that conflicts with a just-issued read. The main memory controller can then delay the read access until the Request signal is deasserted indicating that the Write Buffer has been emptied.

Error Address Latch

The write buffer incorporates an internal latch that can be loaded with one of the buffered addresses and subsequently enabled out onto the data lines. This feature can be used by error handling routines to read an address back from the Write Buffer and analyze or recover from certain bus errors. Figure 8 shows the signals involved in operation of this latch.

When the LatchErrAddr signal is asserted, the address currently available to the address outputs of the Write Buffer is latched into the internal latch. This address can then be output on the DataOut lines by asserting the EnErrAdr signal so that the processor can read the address in as data. Refer to the AC specifications for timing parameters of the signals associated with the error address latch.

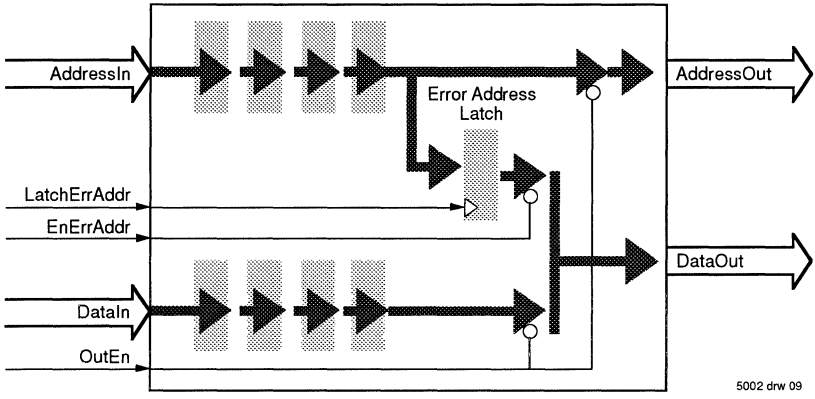

Figure 8. The Write Buffer Error Address Latch

ABSOLUTE MAXIMUM RATINGS(1, 3)

SYMBOL	RATING	COM.	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature(2)	–55 to +125	°C
V_{IN}	Input Voltage	–0.5 to +7.0	V

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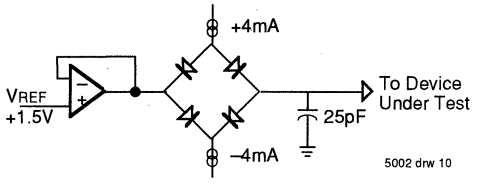
NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN} minimum = –3.0V for pulse width less than 15ns. V_{IN} should not exceed V_{CC} + 0.5V.
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	Vcc
Commercial	0°C to +70°C	0V	5.0 ± 5%

5002 tbl 02

OUTPUT LOADING FOR AC TESTING



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DC ELECTRICAL CHARACTERISTICS — COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to +70°C, V_{CC} = +5.0 V ± 5%)

SYMBOL	PARAMETER	TEST CONDITIONS	16.67MHz Min.	16.67MHz Max.	20.0MHz Min.	20.0MHz Max.	25.0MHz Min.	25.0MHz Max.	33.33MHz Min.	33.33MHz Max.	40MHz Min.	40MHz Max.	UNIT
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4mA	3.5	—	3.5	—	3.5	—	3.5	—	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	—	0.4	—	0.4	—	0.4	—	0.4	—	2.4	V
V_{IH}	Input HIGH Voltage(1)		2.4	—	2.4	—	2.4	—	2.4	—	2.4	—	V
V_{IL}	Input LOW Voltage(2)		—	0.8	—	0.8	—	0.8	=	0.8	—	0.8	V
C_{IN}	Input Capacitance(3)		10	—	10	—	10	—	10	—	10	—	pF
C_{OUT}	Output Capacitance(3)		10	—	10	—	10	—	10	—	10	—	pF
I_{CC}	Operating Current	V_{CC} = Max.	—	50	—	60	—	70	—	80	—	90	mA
I_{IH}	Input HIGH Leakage	V_{IH} = V_{CC}	—	10	—	10	—	10	—	10	—	10	µA
I_{IL}	Input LOW Leakage	V_{IL} = GND	–10	—	–10	—	–10	—	–10	—	–10	—	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	–40	40	–40	40	–40	40	–40	40	–40	40	µA

5002 tbl 03

NOTES:
1. V_{IH} should be held above V_{CC} + 0.5V.
2. V_{IL} Min. = –3.0V for pulse width less than 15ns. V_{IL} should not fall below –0.5V for longer periods.
3. Tested only initially, and after design changes which may affect capitance.

AC ELECTRICAL CHARACTERISTICS — COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to +70°C, V_{CC} = +5.0V ± 5%)

SYMBOL	PARAMETER	16.67MHz Min.	16.67MHz Max.	20.0MHz Min.	20.0MHz Max.	25.0MHz Min.	25.0MHz Max.	33.33MHz Min.	33.33MHz Max.	40MHz Min.	40MHz Max.	UNIT
t1	Addrin (3:0) to Clock falling setup	8	—	7	—	6	—	3	—	3	—	ns
t2	Addrin (3:0) from Clock falling hold	4	—	4	—	4	—	3	—	3	—	ns
t3	Address 1:0 to Clock falling setup	8	—	7	—	6	—	3	—	3	—	ns
t4	Address 1:0 from Clock falling hold	4	—	4	—	4	—	3	—	3	—	ns
t5	Access Type 1:0 to Clock rising setup	7	—	6	—	5	—	4	—	4	—	ns
t6	Access Type 1:0 from Clock rising hold	3	—	3	—	2	—	2	—	2	—	ns
t7	Addrin (7:4) to Clock rising setup	7	—	5	—	4	—	4	—	4	—	ns
t8	Addrin (7:4) from Clock rising hold	3	—	3	—	2	—	1	—	1	—	ns
t9	DataIn (8:0) to Clock rising setup	7	—	5	—	4	—	4	—	4	—	ns
t10	DataIn (8:0) from Clock rising hold	3	—	3	—	2	—	1	—	1	—	ns
t11	$\overline{\text{WrtMem}}$ to Clock rising setup	10	—	8	—	7	—	6	—	6	—	ns
t12	$\overline{\text{WrtMem}}$ from Clock rising hold	6	—	5	—	4	—	3	—	3	—	ns
t13	Request from Clock rising	—	32	—	30	—	22	—	16	—	16	ns
t14	Acknowledge to Clock rising setup	12	—	11	—	6	—	4	—	4	—	ns
t15	Acknowledge from Clock rising hold	7	—	6	—	5	—	3	—	3	—	ns
t16	LatchErrAdr to Acknowledge rising	5	—	5	—	5	—	3	—	3	—	ns
t17	$\overline{\text{WbFull}}$ active from Clock rising	—	21	—	19	—	17	—	9	—	9	ns
t18	$\overline{\text{WbFull}}$ inactive from Clock rising	—	21	—	19	—	11	—	9	—	9	ns
t19	OutEn to AddrOut (7:0), DataOut (8:0) valid	2	15	2	15	2	15	2	12	2	12	ns
t20	OutEn to AddrOut (7:0), DataOut (8:0) tri-state	2	15	2	15	2	15	2	12	2	12	ns
t21	MatchOut (ABCD) from Clock rising	—	24	—	22	—	20	—	15	—	12	ns
t22	MatchIn (ABCD) to Clock rising setup	10	—	9	—	8	—	5	—	5	—	ns
t23	MatchIn (ABCD) from Clock rising hold	3	—	3	—	3	—	3	—	3	—	ns
t24	$\overline{\text{EnErrAdr}}$ to Data (error latch) valid	2	15	2	15	2	15	2	15	2	15	ns
t25	$\overline{\text{EnErrAdr}}$ to Data (error latch) tri-state	2	15	2	15	2	15	2	15	2	15	ns
t26	Address/Data out from Clock rising	—	30	—	27	—	24	—	16	—	16	ns
t27	$\overline{\text{Reset}}$ to Clock rising, set-up	10	—	10	—	10	—	8	—	8	—	ns
t28	$\overline{\text{Reset}}$ from Clock rising, hold	3	—	2	—	1	—	1	—	1	—	ns
t29	Reset LOW pulse width	8	—	8	—	8	—	8	—	8	—	cycles
t30	$\overline{\text{WbFull}}$ HIGH from Clock rising (after $\overline{\text{Reset}}$)	—	22	—	21	—	20	—	11		11	ns
t31	$\overline{\text{Request}}$ HIGH from $\overline{\text{Reset}}$ LOW	—	20	—	19	—	18	—	16	—	16	ns
t32	Access TypOut 1:0 from $\overline{\text{Reset}}$ LOW $\overline{\text{OutEn}}$ Asserted	—	28	—	26	—	25	—	23	—	23	ns
t33	MatchOut (ABCD) LOW from $\overline{\text{Reset}}$ LOW	—	21	—	20	—	20	—	15	—	15	ns
t34	Address/Data out tri-state from $\overline{\text{Reset}}$ LOW (OutEn negated)	—	32	—	30	—	27	—	23	—	23	ns
t35	Access TypeOut from Clock rising	—	32	—	30	—	27	—	23	—	23	ns
tcyc	Clock Pulse Width	60	2000	50	2000	40	2000	30	2000	25	2000	ns
tckhigh	Clock HIGH Pulse Width	24	—	20	—	16	—	12	—	10	—	ns
tcklow	Clock LOW Pulse Width	24	—	20	—	16	—	12	—	10	—	ns

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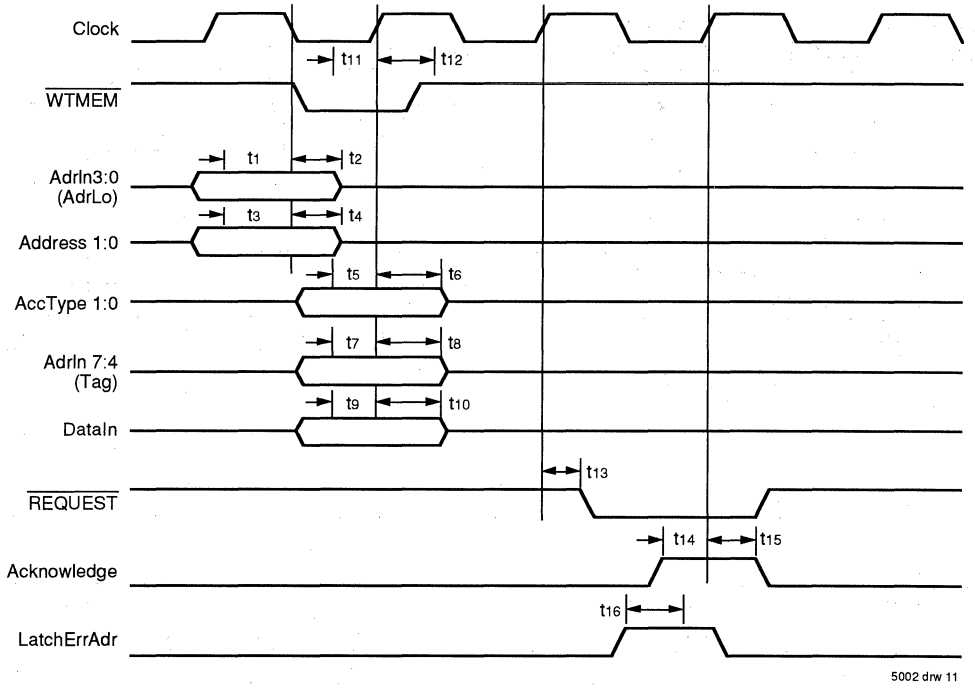

Figure 9. Write Buffer Timing Specifications

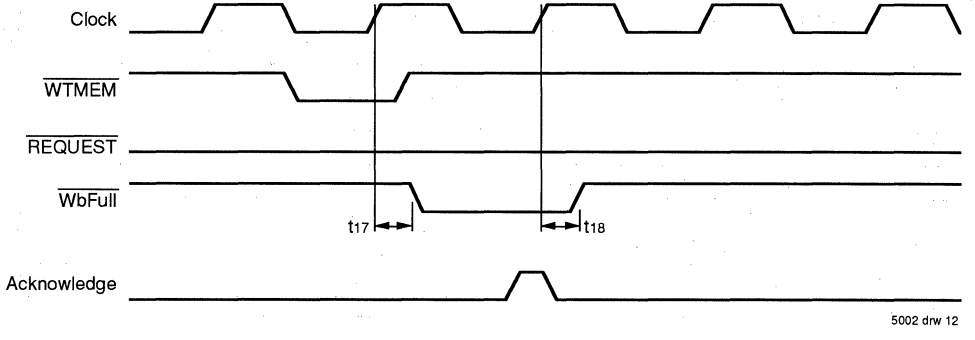

Figure 10. $\overline{\text{WBFULL}}$ Signal Timing Specificaions

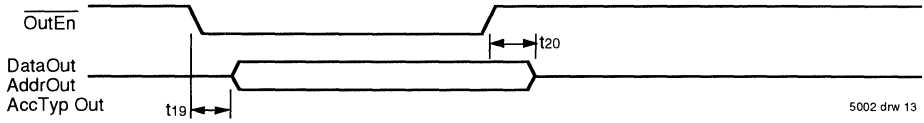

Figure 11. $\overline{\text{OUTEN}}$ Timing Specifications

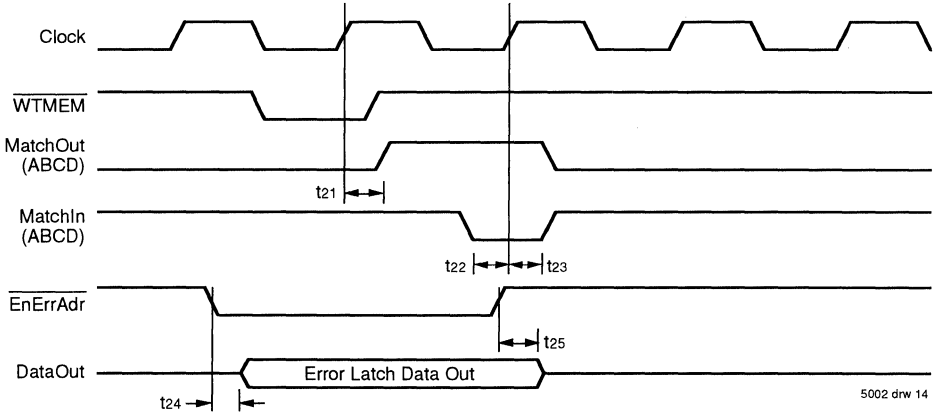

Figure 12. Match and Error Latch Timing Specifications

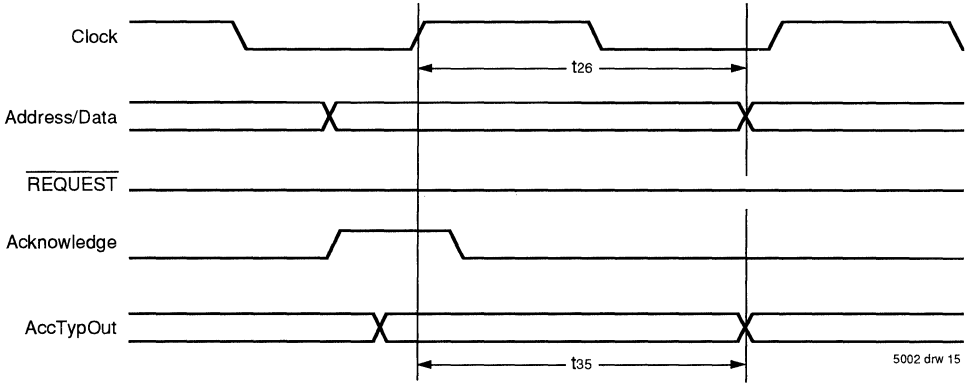

Figure 13. Address/Data Out, Access Type Out

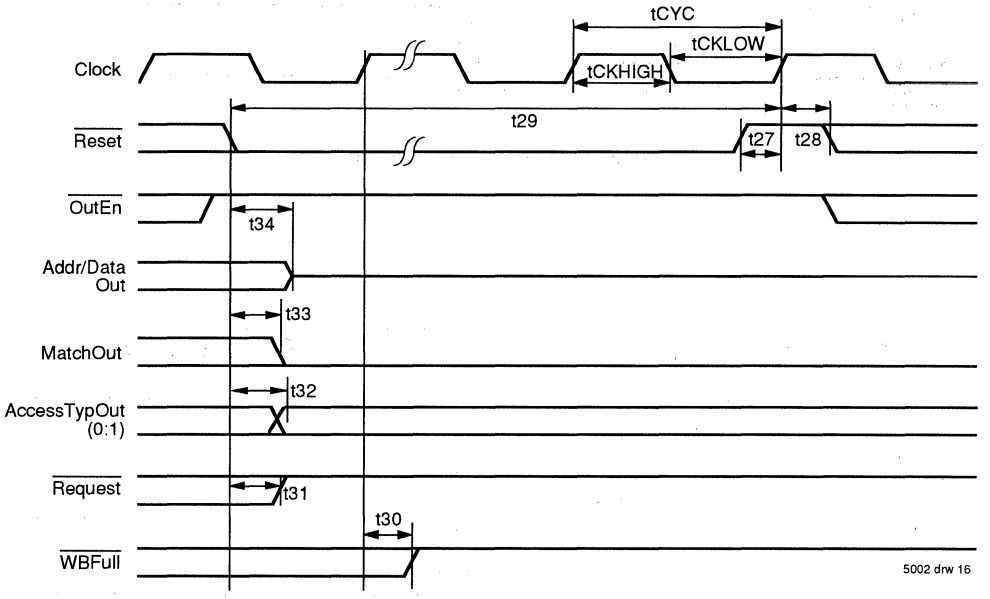

Figure 14. Reset Timing

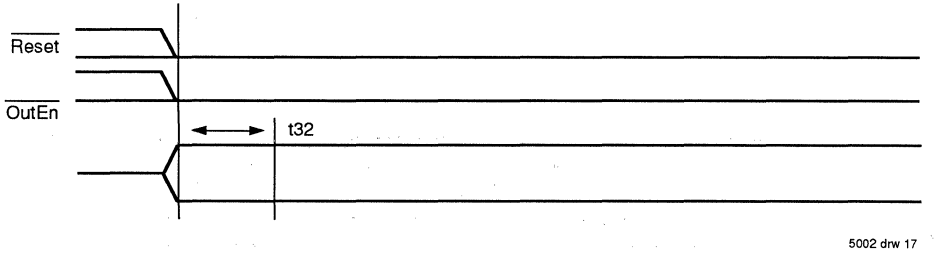

Figure 15. Reset Timing for Access Type Out

68-PIN CPGA FOR 3020
PIN GRID ARRAY (CERAMIC) – BOTTOM VIEW

	1	2	3	4	5	6	7	8	9	10	11
L		ACC-TYP0	AC-KNOW-LEDGE	ADD-RESS1	CLOCK	DATA-IN0	DATA-IN2	DATA-IN4	DATA-IN6	VCC2	
K	GND1	VCC1	ACC-TYPE1	ADD-RESS0	$\overline{\text{BIG-ENDIAN}}$	$\overline{\text{EN-ERROR-ADR}}$	DATA-IN1	DATA-IN3	DATA-IN5	GND2	DATA-IN7
J	ADDR-OUT5	ADDR-OUT4								DATA-IN8	ADDR-IN0
H	ADDR-OUT3	ADDR-OUT2								ADDR-IN1	ADDR-IN2
G	ADDR-OUT1	ADDR-OUT0								ADDR-IN3	ADDR-IN4
F	DATA-OUT8	DATA-OUT0								ADDR-IN5	ADDR-IN6
E	DATA-OUT1	DATA-OUT2								ADDR-IN7	LATCH-ERR-ADR
D	DATA-OUT3	ADDR-OUT6								MATCH-INA	MATCH-INB
C	ADDR-OUT7	ACC-TYPE OUT1								MATCH-INC	MATCH-IND
B	ACC-TYPE OUT0	GND0	DATA-OUT7	DATA-OUT4	$\overline{\text{RE-QUEST}}$	MATCH-OUTC	MATCH-OUTA	$\overline{\text{RESET}}$	POSI-TION0	VCC3	GND3
A		VCC0	DATA-OUT5	DATA-OUT6	$\overline{\text{WB-FULL}}$	MATCH-OUTD	MATCH-OUTB	$\overline{\text{WTMEM}}$	POSI-TION1	OUTEN	

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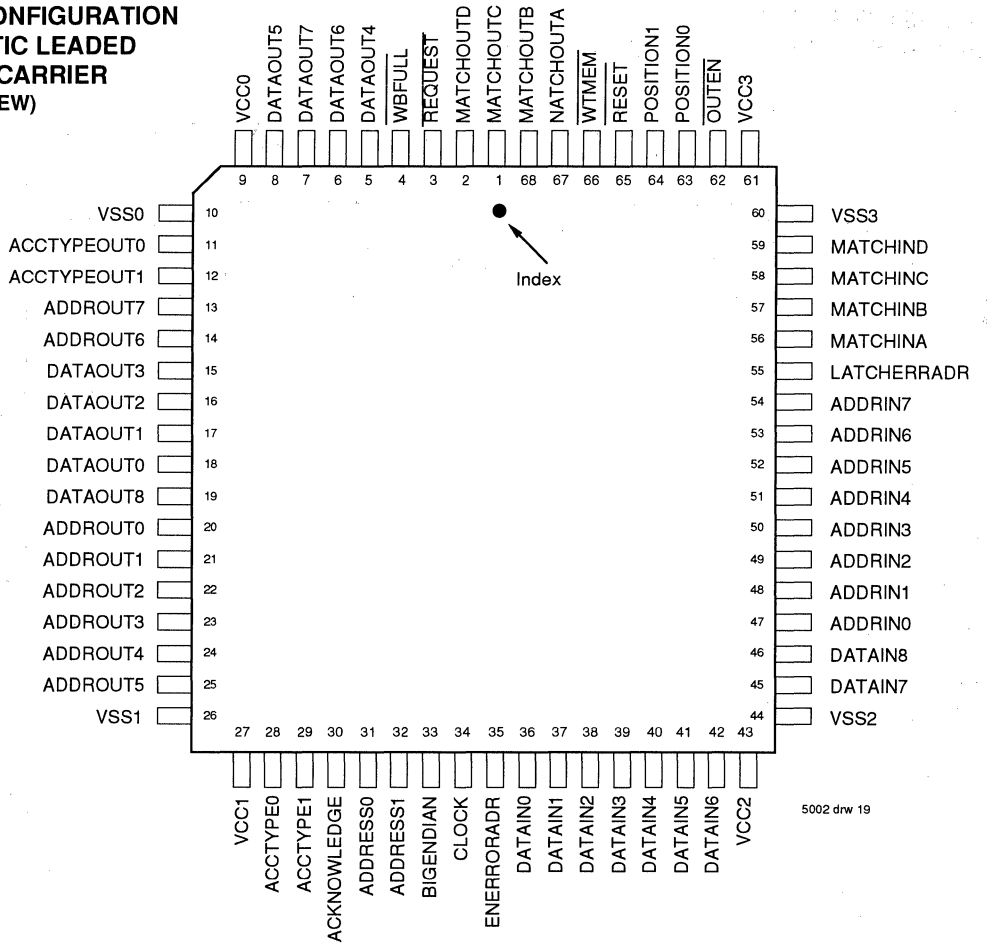
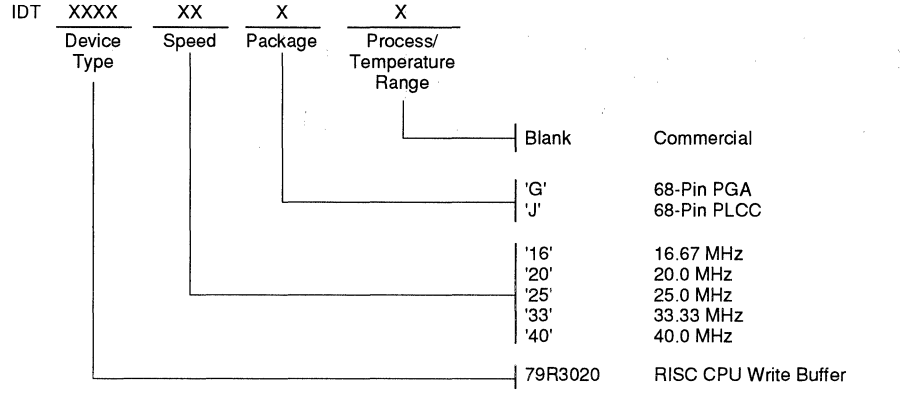
PIN CONFIGURATION
PLASTIC LEADED CHIP CARRIER
(TOP VIEW)



5002 drw 19

ORDERING INFORMATION



5002 drw 20

Integrated Device Technology, Inc.

DRAM CONTROLLER FOR THE R3051 FAMILY

PRELIMINARY
IDT79R3721

FEATURES

- Highly integrated DRAM Controller for R3051 Family Systems
  - — Direct control of DRAM data path transceivers
  - — Direct handshake with R3041/51/81
  - — Direct control of DRAMs, including address, $\overline{RAS}$, and $\overline{CAS}$
- Wide variety of DRAM subsystems supported
  - — 256K x 1 through 4MB x 4 DRAM devices
  - — 1 to 4 banks of DRAM
  - — non-interleaved or two-way interleaved
  - — DRAM access times of 100ns or faster
  - — Capability to drive up to 36 DRAMs directly
- Supports all bus transfers of the R3051 family
  - — Page mode reads and writes
  - — Quad word reads
  - — Normal read or write accesses
- 84-pin PLCC
- Supports page mode operation of DRAMs (either read or write) using on-chip page hit detector
- Automatic $\overline{CAS}$-before-$\overline{RAS}$ refresh with on-chip Refresh timer
- Supports various system address decoding schemes

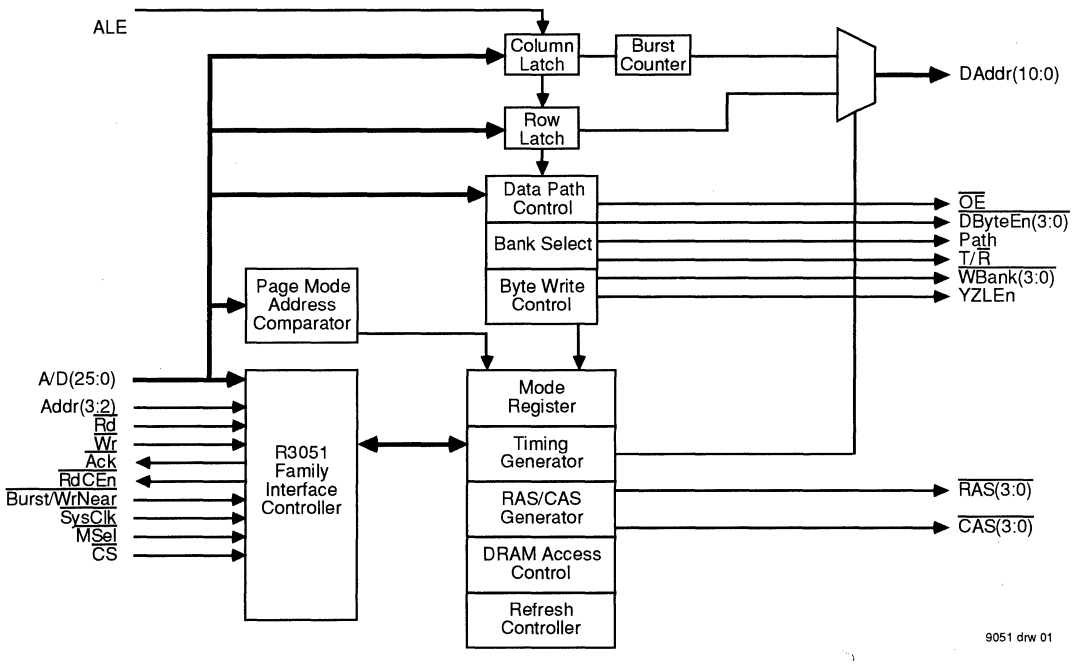


Figure 1. R3721 Block Diagram

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INTRODUCTION

The R3721 is a Dynamic RAM Memory Controller, designed to offer the same levels of system flexibility as the R3051 family.

The R3721 is responsible for translating between the R3051 family bus interface and the special control requirements of various DRAM based sub-systems. The R3721 performs all necessary handshaking and timing control. All that is required to implement a DRAM sub-system for the R3051 family is the R3721, DRAMs, an address decoder, and some transceivers for the data path.

The R3721 has been designed to enable systems to be implemented with field upgrade capabilities of their memory system. In order to upgrade to larger memory devices, or to increase the amount of memory, software merely needs to re-program the R3721 mode register at boot time. No complicated re-routing of address lines, nor modifications of the data path need to occur. Thus, as with the R3051 family, a single footprint and base design can offer a wide variety of end products, depending on the frequency of devices selected, the amount of memory installed, and the specific R3051 family CPU selected.

Figure 1 illustrates the block diagram of the R3721 DRAM controller.

The R3721 DRAM controller contains all of the functional elements necessary to support the bus transaction requirements of the R3051 family. The R3721 connects directly to the R3051 bus, and captures address and control information from the bus as the R3051, or a DMA controller, drives it. The R3721 begins its transaction once its memory space is selected by an external address decoder.

The R3721 will generate all of the DRAM control signal sequencing required:

- Row address set-up to $\overline{RAS}$ asserted.
- Row address hold from $\overline{RAS}$ asserted
- Column address set-up to $\overline{CAS}$ asserted
- $\overline{RAS}$ to $\overline{CAS}$ delay
- $\overline{CAS}$ to data valid (read)
- $\overline{WE}$ to $\overline{CAS}$ set-up (write)

In addition, the R3721 will manage the transceiver-based data path interface, to properly control the flow of data between the CPU bus and the DRAM devices. The R3721 can either control standard FCT245 type transceivers (non-interleaved memory systems), or use the high-performance 73720 Bus Exchanger (for interleaved memory systems). Figure 2 illustrates a typical system composed of the R3051, R3721 DRAM controller, and 73720 Bus Exchanger.

Finally, the R3721 will provide the proper acknowledgement back to the R3051, at the optimum time. That is, the R3721 will generate $\overline{Ack}$ and/or $\overline{RdCEn}$, according to the timing model for the DRAMs and the type of transfer requested.

This data sheet provides an overview on the R3721, and also includes specific electrical and mechanical information on the device. A detailed understanding of the R3721 and its uses can be obtained from the *R3721 Hardware User's Manual*, available from your local IDT sales representative.

R3721 PROCESSOR INTERFACE

The R3721 is designed to reside directly on the R3051 family A/D and control busses. To complete the system design, an external address decoder is required, and external data path chips such as the IDT73720 Bus Exchangers, or IDT74FCT245 bi-directional transceivers.

Regardless of size or organization of DRAM, the R3721 is always connected to particular bits of the R3051 A/D bus. The R3721 uses programmed values for the DRAM size and organization to internally multiplex R3051 address lines into the appropriate row and column addresses for the DRAM. Table 1 shows the internal multiplexing of addresses performed by the R3721. Table 2 shows the DRAM bank selection, and which $\overline{RAS}/\overline{CAS}$ control signals are output.

The R3721 monitors the processor ALE, $\overline{Rd}$, $\overline{Wr}$ and $\overline{Burst}/\overline{WrNear}$ control signals to determine the type of cycle in progress. The R3721 contains its own address latches, and alignes processor address outputs with DRAM Row and Column addresses.

If the external address decoder indicates that this transfer is intended for the DRAM sub-system, the R3721 performs the DRAM control interface. At the appropriate time, the DRAM controller will return the $\overline{RdCEn}/\overline{Ack}$ handshake back to the processor to indicate that the transaction is sufficiently completed.

The interface to $\overline{Ack}$ and $\overline{RdCEn}$ is performed using a tri-stateable output driver. This allows other tri-stateable sources to directly drive $\overline{Ack}$ and $\overline{RdCEn}$ without introducing combinatorial logic delays inherent in combining the acknowledgements from multiple memory subsystems.

DRAM Address	Interleaved	Non-Interleaved
Column(8:0)	A(11:3)	A(10:2)
Row(8:0)	A(20:12)	A(19:11)
Bank Sel(1:0)	A21A(21:20)	

Address assignment for 256k x 4 and 256k x 1 DRAMs 9051 tbl 01

DRAM Address	Interleaved	Non-Interleaved
Column(9:0)	A(12:3)	A(11:2)
Row(9:0)	A(22:13)	A(21:12)
Bank Sel(1:0)	A23A(23:22)	

Address assignment for 1M x 1 and 1M x 4 DRAMs 9051 tbl 02

DRAM Address	Interleaved	Non-Interleaved
Column(10:0)	A(13:3)	A(12:2)
Row(10:0)	A(24:14)	A(23:13)
Bank Sel(1:0)	A25A(25:24)	

Address assignment for 4Mx1 and 4Mx4 DRAMs 9051 tbl 03

Table 1. Processor to DRAM Address Multiplexing

Bank Sel(1:0)	Non-Interleaved	Interleaved
00	RAS(0)/CAS(3:0)	RAS(1:0)/CAS(3:0)
01	RAS(1)/CAS(3:0)	RAS(1:0)/CAS(3:0)
10	RAS(2)/CAS(3:0)	RAS(3:2)/CAS(3:0)
11	RAS(3)/CAS(3:0)	RAS(3:2)/CAS(3:0)

Table 2. Bank Selection in Multi-Bank System 9051 tbl 04

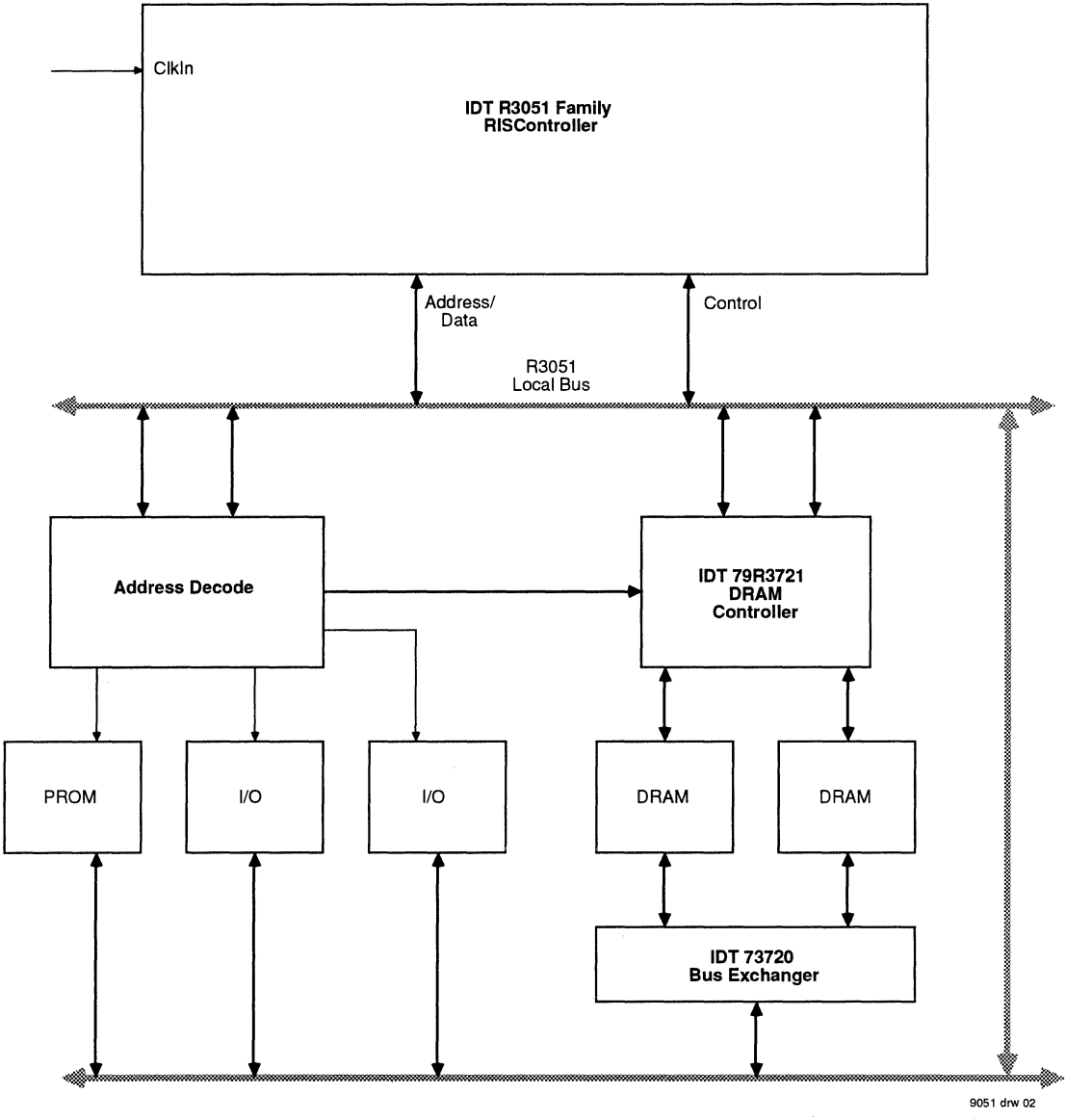

Figure 2. R3721 Used in R3051 System

R3721 DRAM INTERFACE

The R3721 has been designed to interface to a wide variety of DRAM subsystems. Various options include:

- Interleaved vs. Non-Interleaved

  Interleaved memory subsystems offer higher system performance by providing higher bandwidth to the processor during quad word refills. However, an interleaved memory system requires a larger "base" amount of memory (two 32-bit arrays minimum) and a wider data path (one for each array, time multiplexed onto a single CPU bus).

  The R3721 offers the system designer the flexibility to design either type of memory system. In fact, with proper planning, the system designer can offer a base model that does not perform memory interleaving, but allow field upgrades to perform interleaving (thus increasing both the memory and raw performance of the system).

- Various densities of DRAM

  The R3721 allows the system designer to use DRAM densities from 256k x 1 through 4M x 4. Thus, depending on the memory requirements of the application, the system designer can decide the appropriate memory subsystem for the application. In addition, the DRAM controller internally aligns the CPU address bus with the DRAM address lines; this allows a later field upgrade to increase the density of memory devices used without requiring jumpering of address lines. The R3721 performs internal multiplexing of address lines in order to support varying densities of DRAMs, without changing its interface to the processor bus.

- Single bank or multiple banks of memory

  The R3721 allows systems to be constructed with one to four banks (32-bit wide memory arrays) of memory (either interleaved or not). Obviously, it has been designed to allow various strategies of "field upgrades" in the DRAM memory sub-system.

  The R3721 utilizes a high-performance output drivers, and four sets of the $\overline{RAS}$ and $\overline{CAS}$ DRAM controls, to directly drive up to 36 DRAM devices. The R3721 uses a high-power output driver with built-in series resistance to avoid the noise problems typically associated with driving large capacitive loads.

  In addition to the capability to directly drive these large loads, the R3721 also allows the system designer to incorporate additional, external memory drivers if needed. The various timing options supported can be selected to accomodate the additional delay of buffer drivers in the DRAM subsystem.

  The R3721 takes care of the particular case of partial writes. $\overline{CAS}$(3:0) are used to provide selective enabling of those DRAMs being written; that is, only those byte lanes involved in the write will have their corresponding $\overline{CAS}$ signals asserted.

- Intelligent Control interface to take advantage of Page Mode DRAMs

  The R3721 state machine was designed after extensive simulation of R3051 program behavior. Optimizations around typical locality of reference are included in the state machine for the R3051.

  Figure 3 shows the basic state machine for the R3721. Note that it is optimized for series of page mode DRAM accesses.

  Specifically, page mode is used for:

  — Burst Refill.

  Page mode is used to obtain words within a quad word read. However, simulation has shown that the most likely next transfer is a single word write; thus, $\overline{RAS}$ and $\overline{CAS}$ are negated at the end of the burst refill to minimize the latency of subsequent operations due to $\overline{RAS}$ pre-charge.

  — Single Reads.

  After a single read, the DRAM controller will leave the DRAMs expecting a subsequent page mode access to the same page (either another read, a write, or a burst refill). The R3721 includes an on-chip page comparator which uses the DRAM density programmed into the device to determine whether or not a given access can take advantage of page mode.

  — Single Writes.

  After a single write, the DRAM controller will leave the DRAMs expecting a subsequent page mode access to the same page (either another write, a read, or a burst refill). The DRAM controller can use either $\overline{WrNear}$, or its internal page comparator, to detect opportunity for page mode accesses.

  Thus, the R3721 has truly been optimized to the operating environment of the R3051 based systems.

- Various speeds of DRAMs and Processors

  The R3721 has been designed to support a wide range of processor frequencies, across a wide range of DRAM speeds. The system designer can configure varying times for the DRAM control signals. Programmable DRAM control parameters include:

  — $\overline{RAS}$ to $\overline{CAS}$ Delay.

  This allows the system designer to control a number of critical timings, including row address hold time from $\overline{RAS}$ and the $\overline{RAS}$ to $\overline{CAS}$ delay requirements of the system.

  — $\overline{RAS}$ and $\overline{CAS}$ pulse widths.

  These parameters directly control the access time of the DRAM, and the resulting system performance.

  — $\overline{RAS}$ and $\overline{CAS}$ pre-charge times.

  These parameters allow the system designer to minimize the performance penalty of DRAM pre-charge, yet still insure proper system operation.

— Refresh period.
Depending on the system speed, the DRAM controller will establish the appropriate counter value to insure both proper refresh operation, and to insure that the maximum $\overline{RAS}$ low time of the DRAM is not violated. The R3721 uses a $\overline{CAS}$-before-$\overline{RAS}$ refresh protocol to perform DRAM refresh.
— Address decode time.
The DRAM controller can work in systems which can properly decode addresses within the first cycle of a transfer, for optimal performance. Alternately, the DRAM controller can work with slower systems, requiring an extra cycle to perform proper address decoding.

• Various data path options.
The R3721 directly controls the data path between the CPU and the DRAM sub-system. The R3721 can control either a set of IDT74FCT245s (for non-interleaved memory systems) or IDT73720s (for either multiple banked or interleaved memory configurations).

The R3721 allows this variety of options through the use of the on-chip MODE register.

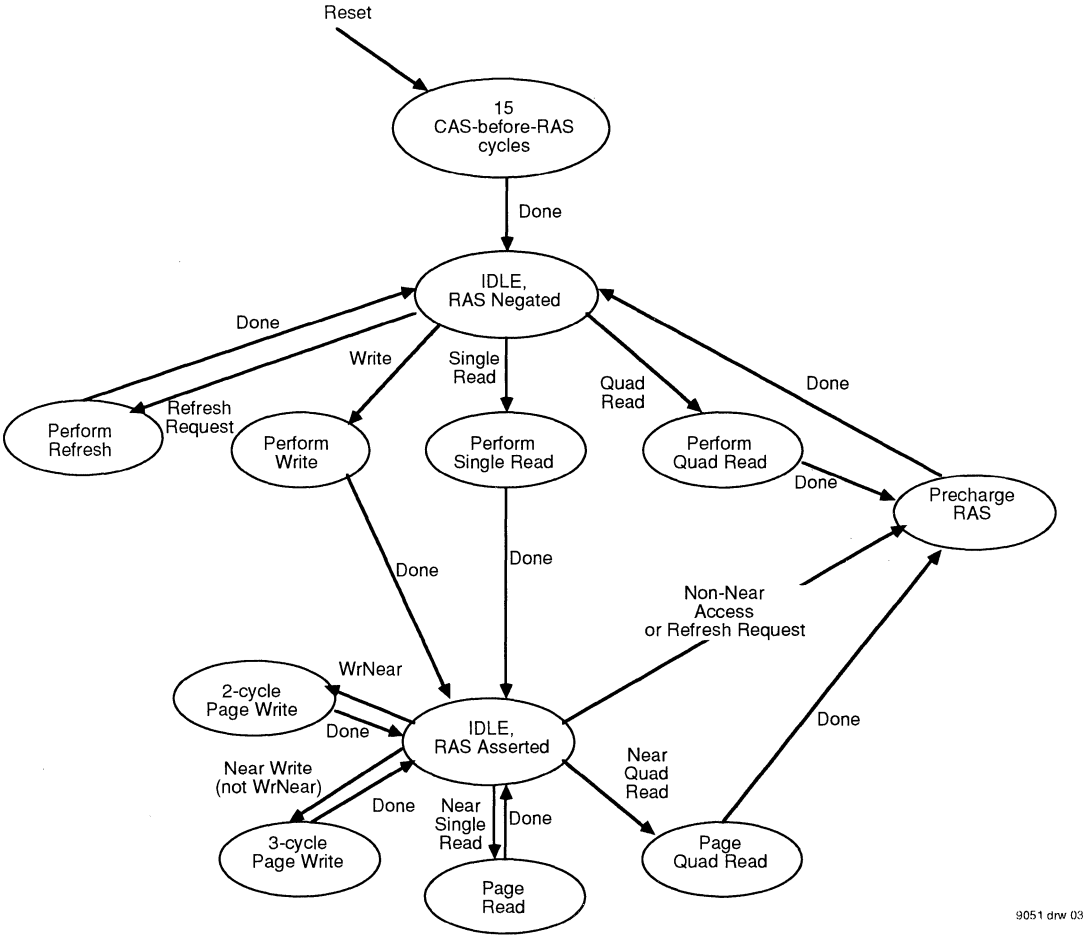

Figure 3. R3721 DRAM Control State Machine

THE MODE REGISTER

The mode register is a 16-bit write-only register used to configure the R3721 to adapt it to a variety of different applications. Figure 4 illustrates the mode register. The settings of the mode register influence the signals used to control the external DRAM banks as well as the signals involved in controlling the data path.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd	DCS	RF2	RF1	RF0	CP	Rsvd	C0	R2	R1	R0	RCD	WrNr	InIvd	DZ1	DZ0

9051 drw 04

Figure 4. R3721 Mode Register

PROGRAMMING THE MODE REGISTER

The mode register contains different fields that provide the R3721 with great flexibility in interfacing with a wide range of applications. Each field is used to control one aspect of the behavior of the R3721. All the fields get updated when writing to the mode register.

DRAM PAGE SIZE FIELD

Bits 0 and 1 of the mode register are used to inform the R3721 of the organization of the DRAMs used in the system as follows:

This allows the R3721 to control up to a maximum of 64 MBytes of memory in the "X1" configurations and up to a maximum of 16 Mbytes in the "X4" configurations.

Bit 1 DZ1	Bit 0 DZ0	DRAM Page Size
0	0	512 entries
0	1	1K entries
1	0	1K entries
1	1	2K entries

9051 tbl 05

EXTERNAL MEMORY CONFIGURATION

Bit 2 of the mode register are used to program the physical configuration of the external memory and the data path.

The R3721 always assumes that Bus Exchangers are used in the data path for the interleaved configuration. In the Non-Interleaved configurations, it is possible to connect either standard transceivers or Bus Exchangers.

Bit 2 InIvd	Memory Configuration
0	Non-Interleaved memory system
1	Interleaved memory system and Bus Exchangers are used in the data path.

9051 tbl 06

WRITE NEAR

The R3721 has the ability to use the R3051 $\overline{\text{WrNear}}$ output to provide fast page mode writes. The extra delay may be appropriate in certain memory configurations, as discussed in User's Manual.

Bit 3 WrNr	Use of $\overline{\text{WrNear}}$
0	Use of $\overline{\text{WrNear}}$ is enabled
1	Use of $\overline{\text{WrNear}}$ is disabled

9051 tbl 07

$\overline{\text{RAS}}$ TO $\overline{\text{CAS}}$ DELAY

Bit 4 of the mode register specifies the delay between the assertion of the appropriate $\overline{\text{RAS}}$ signal to the assertion of the related $\overline{\text{CAS}}$ signal. This delay can be programmed to be either one clock cycle or two clock cycles. Figure 5 illustrates the effect of the RCD bit .

The DRAM controller always transitions the DAddr bus from Row Address to Column Address one-half clock cycle before the assertion of $\overline{\text{CAS}}$.

Bit4 RCD	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay
0	One clock cycle delay from $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$
1	Two clock cycles delay from $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$

9051 tbl 08

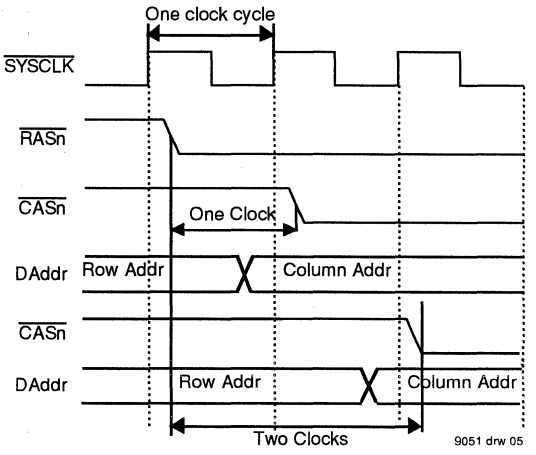

Figure 5. $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay

RAS TIMING

Bits 5, 6 and 7 of the mode register specify the width of the RAS pulse in clock cycles as well as the RAS pre-charge time. This field gives the system designer the freedom to choose from a wide range of DRAM speeds based on a performance/ cost criteria. Figure 6 illustrates the timings of the RAS signals.

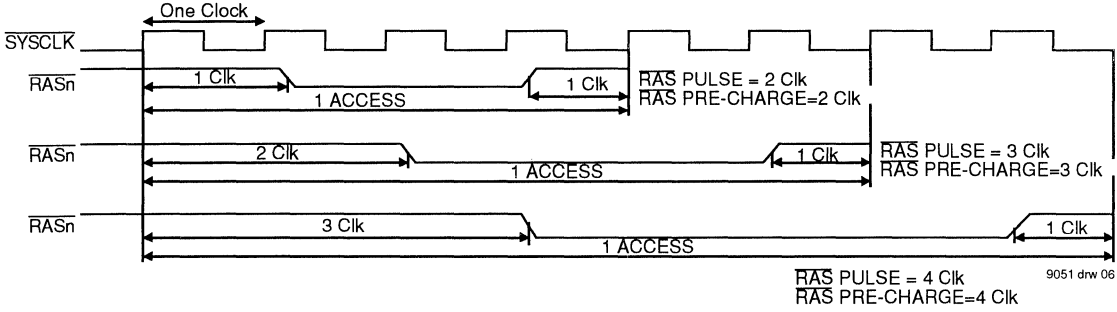

Figure 6. RAS Timing

Bit 7 R2	Bit 6 R1	Bit 5 R0	Pulse Width	Pre-charge
0	0	0	2 clocks	2 clocks
0	0	1	3 clocks	2 clocks
0	1	0	3 clocks	3 clocks
0	1	1	4 clocks	2 clocks
1	0	0	4 clocks	3 clocks
1	0	1	4 clocks	4 clocks
1	1	0	Reserved	
1	1	1	Reserved	

9051 tbl 09

CAS PULSE WIDTH

Bit 8 of the mode register specify the CAS pulse width in clock cycles. The CAS pulse width can be programmed to be 1.5 or 2.5 clock cycles. Figure 7 illustrates the timings of the CAS pulse width.

The CAS pulse width, along with the CAS precharge time, has the most dramatic impact on system performance. These parameters affect the performance of the various page mode accesses performed by the DRAM controller, and thus directly affect the timing of the RdCEn and Ack acknowledgement signals back to the processor.

C0	CAS Pulse Width
0	2.5 clock cycles
1	1.5 clock cycles

9051 tbl 10

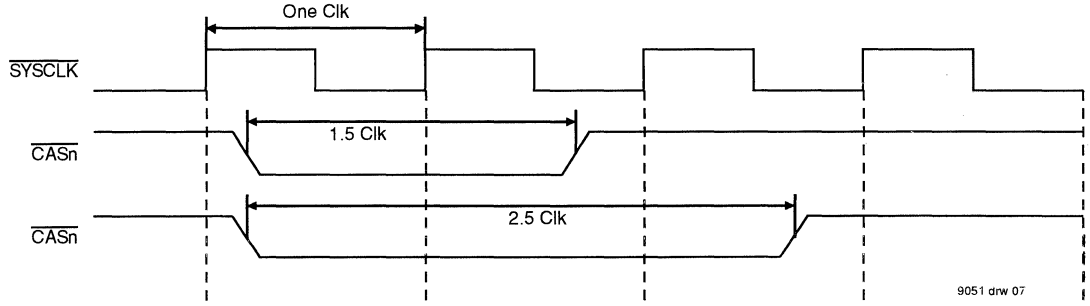

Figure 7. CAS Pulse Width

$\overline{CAS}$ PRE-CHARGE TIME

Bit 10 of the mode register specifies the $\overline{CAS}$ pre-charge time which could be programmed to be either 0.5 clock cycle or 1.5 clock cycles. Any combination between the $\overline{CAS}$ pulse width and the $\overline{CAS}$ pre-charge time is possible. Figure 8 illustrates the $\overline{CAS}$ pre-charge timing.

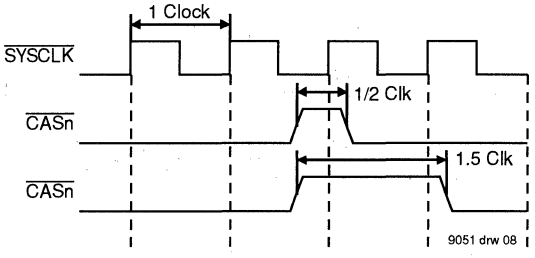

Figure 8. $\overline{CAS}$ Pre-charge Timing

Bit 10 CP	$\overline{CAS}$ Precharge Width
0	0.5 clock cycle
1	1.5 clock cycle

9051 tbl 11

REFRESH PERIOD

Bits 11, 12 and 13 of the mode register specify the frequency of the input clock to the R3721. The R3721 loads an internal refresh timer with the appropiate value to refresh the DRAMs according to the table below.

The value is appropriate to avoid violating the maximum $\overline{RAS}$ low time of 10µS specification for DRAMs. Using this value, the DRAM controller will insure $\overline{RAS}$ does not stay low too long, by performing a refresh cycle.

Bit 13 RF2	Bit 12 RF1	Bit 11 RF0	Timer Value	$\overline{SysClk}$ Freq.
0	0	0	23	4 MHz
0	0	1	63	8 MHz
0	1	0	103	12 MHz
0	1	1	143	16 MHz
1	0	0	176	20 MHz
1	0	1	226	25 MHz
1	1	0	307	33 MHz
1	1	1	374	40 MHz

9051 tbl 12

DELAYED CHIP-SELECT

Bit 14 of the mode register specifies when the R3721 will sample the Chip-Select and/or the Mode-Select input pins at the beginning of any access. The R3721 can be programmed to sample the Chip-Select on the first positive edge of the clock following the negation of ALE or on the first negative edge of the clock following the negation of ALE.

This bit allows the R3721 to perform optimally in either a high-performance (or low frequency) system capable of rapidly decoding addresses, or in systems using a slower, or synchronous approach to address decoding. The R3721 needs to also be explicitly aware of transfers which do not use its memory devices; for example, it can use these cycles to perform a DRAM refresh without performance loss in the system.

The DCS bit also affects the operation of the R3721 for page writes. If the DCS is cleared, the R3721 can perform page writes in a minimum of two clock cycles. If the DCS bit is set, the R3721 can perform page writes in a minimum of 3 clock cycles. Figure 9 illustrates the timings of the Chip-Select or the Mode-Select input pins.

Bit 14 DCS	Action
0	$\overline{CS}$ sampled on the positive edge of the clock 2 clock cycle page writes may be possible
1	$\overline{CS}$ sampled on the negative edge of the clock 2 clock cycle page writes not possible

9051 tbl 13

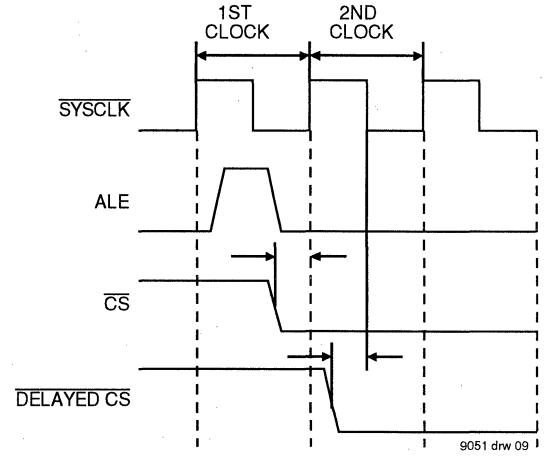

Figure 9. Delayed $\overline{CS}$ Settings

NOTE:
1. Rsvd bits must be written with "0".

DEFAULT SETTINGS

At power up, the mode register is loaded with default values which correspond to the following system:

- DRAM page size: 512 entries
- System configuration: Non-interleaved
- $\overline{\text{WrNear}}$ for fast writes enabled.
- 2 clock cycles delay from $\overline{\text{RAS}}$ assertion to $\overline{\text{CAS}}$ assertion
- 4 clock cycles for the $\overline{\text{RAS}}$ pulse width and the $\overline{\text{RAS}}$ pre-charge time
- 2.5 clock cycles for the $\overline{\text{CAS}}$ pulse width
- 1.5 clock cycle for the $\overline{\text{CAS}}$ pre-charge time
- 25 Mhz frequency of operation
- Delayed Chip-Select.

Figure 10 illustrates the settings of the mode register at power up.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd	DCS	RF2	RF1	RF0	CP	Rsvd	C0	R2	R1	R0	RCD	WrNr	Inlvd	DZ1	DZ0
x	1	1	0	1	1	x	0	1	0	1	1	0	0	0	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

9051 drw 10

Figure 10. MODE Register Default Values

NOTE:
1. Rsvd bits must be written as "0".

WRITING TO THE MODE REGISTER

The mode register is a 16-bit write only register that controls the internal operation of the R3721 DRAM controller. The different fields of the mode register control the behavior of various output control signals such as the $\overline{\text{RAS}}$ and the $\overline{\text{CAS}}$ signals. At power up, the mode register is initialized with the default settings illustrated in figure 10. To obtain maximum performance out of the R3721 DRAM Controller, the mode register needs to be programmed to fit the application at hand.

To access the internal mode register of the R3721, the external address decoder must assert both the $\overline{\text{CS}}$ line and the $\overline{\text{MSel}}$ lines. The assertion of the $\overline{\text{CS}}$ line is imporatnt to distinguish among multiple R3721s in a single system. The Internal mode register of the R3721 should be mapped in the uncachable I/O space of the R3051.

The R3051 can access the mode register by proceeding with a standard write operation to the I/O location occupied by the mode register. The R3721 detects the assertion of both the $\overline{\text{CS}}$ and the $\overline{\text{MSel}}$ lines and determines that the access is for the internal mode register. The data present on the R3051 data bus A/D(15:0) is written into the mode register, regardless of system byte ordering. The R3721 returns the $\overline{\text{ACK}}$ signal to the R3051 to terminate the write access to the mode register in 3 clock cycles. Thus, the write access to the mode register is always 3 clock cycles regardless of the configuration of the external memory system.

Note that it is recommended that writes to the mode register use '0' in the upper A/D bits (A/D(25:16)). This insures compatibility with possible future versions of the DRAM controller.

6

PIN DESCRIPTION

SIGNAL	I/O	DESCRIPTION
$\overline{\text{Reset}}$	I	**Reset**: An active low input used to reset the DRAM controller state machines. At the end of Reset, the R3721 loads the mode register with default values, and performs 15 $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycles to the DRAMs to initialize them.
A/D(25:0)	I	**Address/Data(25:0)**: These signals are connected directly with A/D(25:0) of the R3051 family CPU. The DRAM controller uses these inputs to obtain: $\overline{\text{BE}}$**(3:0)**: Individual data byte enables used in write operations. **Address(25:4)**: Address bits used to select amongst banks of DRAMs, and Row and Column addresses, according to tables 1 and 2. **Data(15:0)**: During Mode register write operations, during the data phase the A/D bus carries the values to be written into the mode register.
Addr(3:2)	I	**Low Order Address(3:2)**:These signals carry the word within quad word address currently expected by the processor. During single reads, or writes, these inputs carry the specified address. During quad word reads, the DRAM controller uses an internal counter to manage word within quad word addressing, and thus ignores these inputs.
ALE	I	**Address Latch Enable**: This signal is used to de-multiplex the A/D bus from address to data phase. The R3721 uses this signal to capture the current value of A/D(25:0) and Addr(3:2) during the address phase. The R3721 also uses this signal as the indication of the beginning of a memory transfer, and awaits its "Chip Select", according to the timing specified in the mode register.
$\overline{\text{Rd}}$	I	**Read**: Indicates that the current transfer is a read (single or burst).
$\overline{\text{Wr}}$	I	**Write**: Indicates that the current transfer is a write (near or not).
$\overline{\text{Burst}}$/ $\overline{\text{WrNear}}$	I	**Burst**: During reads, this signal functions as the "Burst" indicator. If burst is asserted during a read, the R3721 knows that a quad word read sequence is expected. **WrNear**: During writes, this signal functions as the "Write Near" indicator. If the DRAM controller is in the "IDLE, $\overline{\text{RAS}}$ asserted" state, it may use this signal to retire the write in two cycles.
$\overline{\text{SysClk}}$	I	**System Clock**: This is the master timing reference, and is a direct connection from the $\overline{\text{SysClk}}$ output of the R3051 family processor. All timing events are referenced to the $\overline{\text{SysClk}}$ input.
$\overline{\text{CS}}$	I	**DRAM Chip Select**: This input is provided by the external address decoder, and is used to indicate that this R3721 controls the DRAM responsible for retiring this transfer. The R3721 uses the programmed value in the Mode Register to determine when to sample this input.
$\overline{\text{MSel}}$	I	**Mode Register Select**: This input is provided by the external address decoder, and is used to indicate that this transfer targets the internal mode register of the R3721. To write to the mode register, both $\overline{\text{CS}}$ and $\overline{\text{MSel}}$ must be asserted by the external address decoder. The R3721 uses the programmed value in the Mode Register to determine when to sample this input.
$\overline{\text{RdCEn}}$	O	**Read Buffer Clock Enable**: This output to the R3051 processor indicates that the currently requested word will be available on its A/D bus at the next sampling clock edge (falling edge of $\overline{\text{SysClk}}$). This output is a tri-stateable output; it is only driven by the R3721 in transfers in which its $\overline{\text{CS}}$ input is asserted at the proper time. It is internally pulled up, so that no external pull-up resistor is required.

9051 tbl 14

SIGNAL	I/O	DESCRIPTION
$\overline{\text{Ack}}$	O	**Acknowledge**: This output to the R3051 family processor indicates that the R3721 has sufficiently processed the current transfer. On read operations, the processor uses this information to determine when to begin emptying the read buffer into the on-chip cache. The timing of this output during quad word reads is determined by the R3721 for optimal performance. The R3721 will release the processor to begin execution as early as possible in the transfer, but will insure that the fourth word of the quad read is available before the processor obtains it from the read buffer. Thus, the processor can simultaneously execute the incoming instruction stream even while the R3721 obtains the remaining words of the transfer. On write operations, the processor uses this to terminate the write operation. This output is a tri-stateable output; it is only driven by the R3721 in transfers in which its $\overline{\text{CS}}$ input is asserted at the proper time. It is internally pulled up, so that no external pull-up resistor is required.
DAddr(10:0)	O	**DRAM Address**: These outputs are typically connected directly to the DRAM multiplexed row/ column address inputs. Depending on the memory system organization and the organization of the DRAMs used, the R3721 will align the processor addresses with the DRAM addresses according to table 1. These outputs incorporate series resistors to eliminate overshoot and undershoot problems associated with large capacitive loads. In addition, high-drive capability has been incorporated in these outputs. Thus, the R3721 can directly drive large numbers of DRAMs or multiple SIMM modules.
$\overline{\text{RAS}}$(3:0)	O	**Row Address Strobe**: These outputs are directly connected with the $\overline{\text{RAS}}$ inputs of the DRAMs on a bank basis, according to table 2. The falling edge of this signal is used by the DRAM to capture the row address presented on DAdr(10:0). In order to directly drive multiple DRAM devices, these signals provide high drive, and incorporate series resistors. Each $\overline{\text{RAS}}$ signal may drivemultiple loads with no system performance degradation.
$\overline{\text{CAS}}$(3:0)	O	**Column Address Strobe**: These outputs are directly connected with the $\overline{\text{CAS}}$ inputs of the DRAMs on a byte basis, according to table 2. The R3051 processor may write partial word quantities, in which case the R3721 only enables those DRAMs in the byte lane being updated. $\overline{\text{CAS}}$(3) corresponds to $\overline{\text{BE}}$(3); $\overline{\text{CAS}}$(2) corresponds to $\overline{\text{BE}}$(2); etc. The falling edge of this signal is used by the DRAM to capture the column address presented on DAddr(10:0). In order to directly drive multiple DRAM devices, these signals provide high drive, and incorporate series resistors. However, the propagation delay of $\overline{\text{CAS}}$ is a system critical parameter; thus, no $\overline{\text{CAS}}$ signal should drive more than 8 loads.
$\overline{\text{WBank}}$(3:0)	O	**Bank Write Enable**:These outputs are used to individually control the write enables of various memory banks. In non-interleaved systems, all four outputs are asserted; $\overline{\text{RAS}}$ selects the specific bank to be written. In interleaved systems, they are enabled in pairs; that is, writes to an even bank cause $\overline{\text{WBank}}$(2) and $\overline{\text{WBank}}$(0) to be asserted, while writes to an odd bank cause $\overline{\text{WBank}}$(3) and $\overline{\text{WBank}}$(1) to be asserted. Again, only the specific bank being written will have its $\overline{\text{RAS}}$ asserted, and thus only that bank will be updated during the write. During refresh cycles, these outputs are negated. This avoids accessing the "test mode" built into modern 4MB DRAMs. In order to directly drive multiple DRAM devices, these signals provide high drive, and incorporate series resistors
$\overline{\text{OE}}$	O	**DRAM Output Enable**: This output is directly connected to the output enable of common I/O DRAMs. It is connected to all DRAMs under the control of the R3721.

9051 tbl 15

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SIGNAL	I/O	DESCRIPTION
$\overline{\text{DByteEn}}(3:0)$	O	**Data Path Byte Enable**: These outputs are four identical output enables for the transceivers in the DRAM data path. Even in the case of partial writes, all four enables will be asserted; $\overline{\text{CAS}}$ will control which devices actually get updated. In typical systems, $\overline{\text{DByteEn}}$ is connected on a byte lane basis to evenly distribute the load. For example, if the data path interfaces uses 74FCT245s, then the $\overline{\text{DByteEn}}$ is directly connected to the "$\overline{\text{OE}}$" input of the transceiver on that byte lane. If the data path uses IDT73720 Bus Exchangers, $\overline{\text{DByteEn}}(1:0)$ are connected to the Bus Exchanger on the lower half of the data bus (Data(15:0)), and $\overline{\text{DByteEn}}(2:0)$ are connected to the Bus Exchanger on the upper half of the data bus (Data(31:16)).
T/$\overline{\text{R}}$	O	**Transmit/Receive**: This signal indicates the direction of the data path, and is connected directly to the T/$\overline{\text{R}}$ input of the 74FCT245 or IDT73720. This output is HIGH during write cycles, and LOW during reads.
Path	O	**Path**: This signal is directly connected to the Path input of the IDT73720. It is used to specify the even or odd memory bank participating in the current transfer. A HIGH specifies an even bank, and a LOW specifies an odd bank.
YZLEn	O	**Data Path Latch Enable**: This signal is connected to the YLEn and the ZLEn inputs of the IDT73720 Bus Exchanger. It is used to capture the data provided by both banks of memory of an interleaved system, for later sequencing onto the processor A/D bus.

9051 tbl 16

ABSOLUTE MAXIMUM RATINGS(1, 3)

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_C, T_A	Operating Temperature	0 to +70 (Ambient)	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
V_{IN}	Input Voltage	–0.5 to +7.0	V

NOTES: 9051 tbl 17

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN} minimum = –3.0V for pulse width less than 15ns. V_{IN} should not exceed V_{CC} +0.5V.
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

AC TEST CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{IH}	Input HIGH Voltage	3.0	—	V
V_{IL}	Input LOW Voltage	—	0.4	V

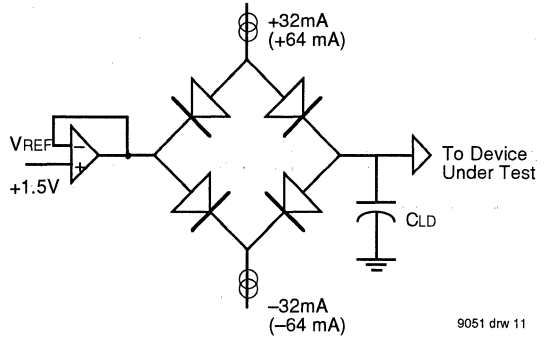
9051 tbl 18

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Commercial	0°C to +70°C (Ambient)	0V	5.0 ±5%

9051 tbl 19

OUTPUT LOADING FOR AC TESTING



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NOTE:
CLD is 25pF unless otherwise specified in the AC Electrical Characteristics Table.

DC ELECTRICAL CHARACTERISTICS— (T_A = 0°C to +70°C, V_{CC} = +5.0V ±5%)

Symbol	Parameter	Test Conditions	20MHz		25MHz		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH}[5]	2.4	—	2.4	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL}[5]	—	0.4	—	0.4	V
V_{IH}	Input HIGH Voltage[2]	—	2.0	—	2.0	—	V
V_{IL}	Input LOW Voltage[1]	—	—	0.8	—	0.8	V
C_{IN}	Input Capacitance[3]	—	—	10	—	10	pF
C_{OUT}	Output Capacitance[3]	—	—	10	—	10	pF
I_{CC}	Operating Current	V_{CC} = 5V, T_A = 70°C	—	175	—	200	mA
I_{IH}	Input HIGH Leakage	V_{IH} = VCC	—	10	—	10	µA
I_{IL}	Input LOW Leakage[4]	V_{IL} = GND	–10	—	–10	—	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	–10	10	–10	10	µA

NOTES:

9051 tbl 20

1. V_{IL} Min. = –3.0V for pulse width less than 15ns. V_{IL} should not fall below –0.5V for larger periods.
2. V_{IH} should not be held above V_{CC} + 0.5V.
3. Guaranteed by design.
4. Except for $\overline{Ack}$ and $\overline{RdCEn}$.
5. For DAddr: I_{OH} = –64mA, I_{OL} = +64mA, for all other signals: I_{OH} = –32mA, I_{OL} = +32mA.

AC ELECTRICAL CHARACTERISTICS [1, 2, 5] (T_A = 0°C to +70°C, V_{CC} = +5.0V ±5%)

Symbol	Description	Test Condition	20MHz		25MHz		Unit
			Min.	Max.	Min.	Max.	
t1	$\overline{SysClk}$ rising to $\overline{CAS}$ LOW	100pF	—	8	—	7	ns
t1a	$\overline{SysClk}$ falling to $\overline{CAS}$ HIGH	100pF	—	7.5	—	6.5	ns
t2	$\overline{SysClk}$ rising to $\overline{RAS}$ LOW	100pF	—	8	—	7	ns
t2a	$\overline{SysClk}$ rising to $\overline{RAS}$ HIGH	100pF	—	8	—	7	ns
t3	$\overline{SysClk}$ falling to DAddr valid	300pF	—	20	—	16.5	ns
t4	$\overline{SysClk}$ falling to $\overline{WBank}$ asserted	100pF	—	13	—	12	ns
t4a	$\overline{SysClk}$ rising to $\overline{WBank}$ asserted	100pF	—	13	—	12	ns
t5	$\overline{SysClk}$ rising to $\overline{WBank}$ negated	100pF	—	13	—	12	ns
t5a	$\overline{SysClk}$ falling to $\overline{WBank}$ negated	100pF	—	13	—	12	ns
t6	$\overline{SysClk}$ falling to Path valid	50pF	—	11	—	10	ns
t7	$\overline{SysClk}$ falling to $\overline{T/R}$ LOW	50pF	—	11	—	10	ns
t8	$\overline{SysClk}$ rising to $\overline{T/R}$ HIGH	50pF	—	11	—	10	ns
t9	$\overline{SysClk}$ rising to $\overline{Ack}$, $\overline{RdCEn}$ enabled	50pF	—	11	—	9	ns
t10	$\overline{SysClk}$ rising to $\overline{Ack}$, $\overline{RdCEn}$ disabled	50pF	—	11	—	9	ns
t11	$\overline{SysClk}$ falling to $\overline{Ack}$, $\overline{RdCEn}$ asserted	50pF	—	16	—	12.5	ns
t12	$\overline{SysClk}$ falling to Ack, $\overline{RdCEn}$ negated	50pF	—	16	—	12.5	ns
t13	$\overline{SysClk}$ falling to YZLEn valid	50pF	—	9	—	8	ns
t14	$\overline{SysClk}$ falling to $\overline{DByteEn}$ asserted	50pF	—	11	—	10	ns
t14a	$\overline{SysClk}$ rising to $\overline{DByteEn}$ asserted	50pF	—	13	—	11	ns
t15	$\overline{SysClk}$ falling to $\overline{DByteEn}$ negated	50pF	—	16	—	14	ns

9051 tbl 21

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AC ELECTRICAL CHARACTERISTICS (1, 2, 5) (T_A = 0°C to +70°C, V_{CC} = +5.0V ±5%)

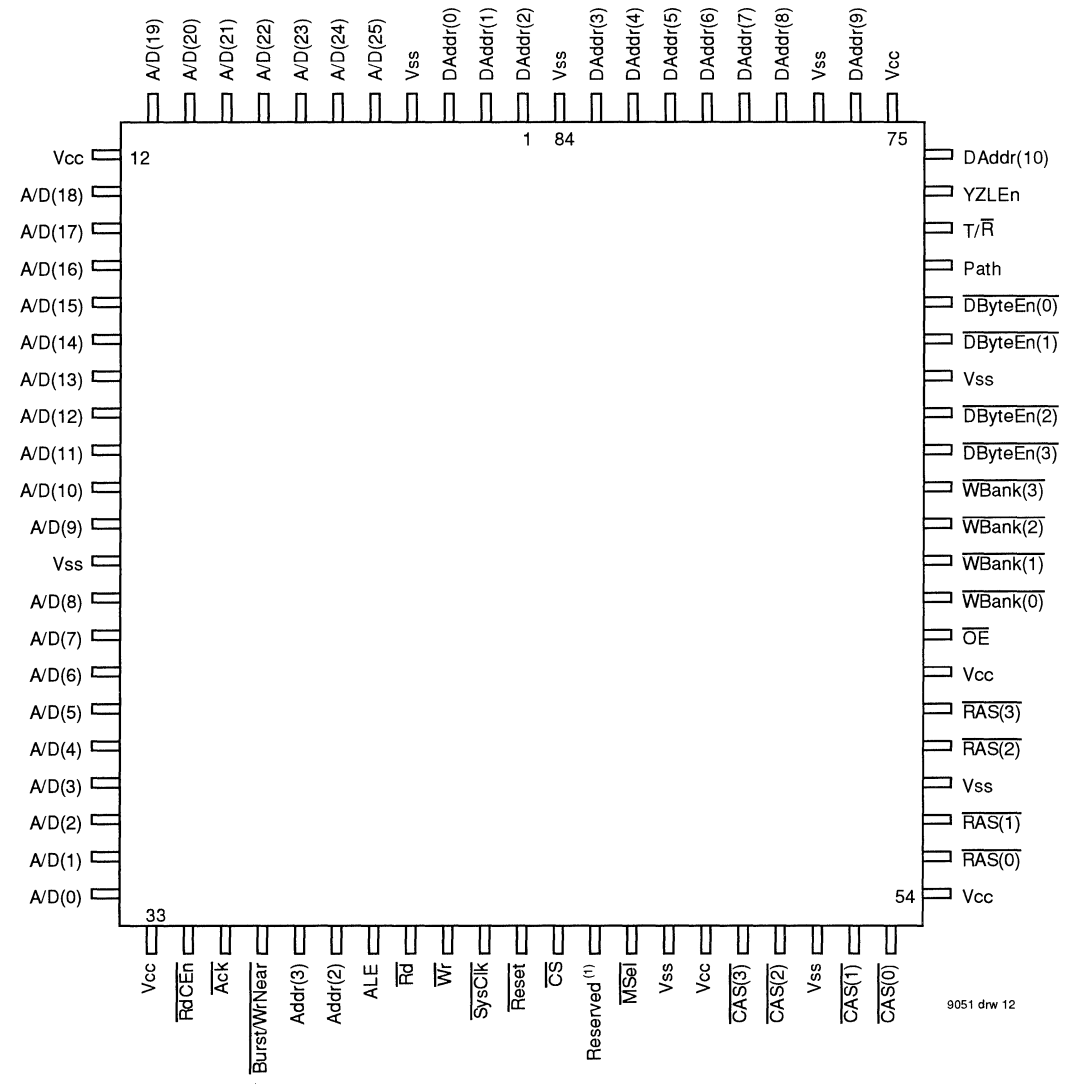
Symbol	Description	Test Condition	20MHz		25MHz		Unit
			Min.	Max.	Min.	Max.	
t15a	$\overline{SysClk}$ rising to $\overline{DByteEn}$ negated	50 pF	—	11	—	10	ns
t16	$\overline{SysClk}$ falling to $\overline{OE}$ asserted	300 pF	—	14	—	12	ns
t17	$\overline{SysClk}$ rising to $\overline{OE}$ negated	300 pF	—	14	—	12	ns
t18	$\overline{CS}$ & $\overline{MSel}$ setup to $\overline{SysClk}$ rising	50 pF	6	—	5	—	ns
t18a	$\overline{CS}$ & $\overline{MSel}$ setup to $\overline{SysClk}$ falling	50 pF	7	—	6	—	ns
t19	$\overline{CS}$ & $\overline{MSel}$ hold after $\overline{SysClk}$	50 pF	3	—	2.5	—	ns
t22	A/D hold after ALE falling	50 pF	2	—	2	—	ns
t22a	A/D setup to $\overline{SysClk}$ falling	—	6	—	6	—	ns
t23	Reset pulse width from Vcc valid	—	500	—	500	—	ns
t24	Reset minimum pulse width	—	100	—	100	—	ns
t25	$\overline{SysClk}$ pulse width	—	50	—	40	—	ns
t26	$\overline{SysClk}$ HIGH time	—	22	—	17	—	ns
t27	$\overline{SysClk}$ LOW time	—	22	—	17	—	ns
t28	$\overline{RAS}$ valid after CAS (refresh)(3)	—	1	—	1	—	cyc
t29	$\overline{CAS}$ hold after RAS (refresh)(3)	—	1.5	—	1.5	—	cyc
t30	Write to Mode register(3)	—	—	3	—	3	cyc
t31	ALE setup to $\overline{SysClk}$ falling	50pF	6	(t26-1)	5	(t26-1)	ns
t32	ALE hold after $\overline{SysClk}$ falling	50pF	0	(t27-3)	0	(t27-3)	ns
t34	A/D hold from $\overline{SysClk}$ falling	—	—	—	—	—	ns
t35	$\overline{Rd}$, $\overline{Wr}$, $\overline{Burst}$/$\overline{WrNear}$ setup to $\overline{SysClk}$ falling	50pF	6	—	5	—	ns
t37	Reset setup to $\overline{SysClk}$	50pF	5	—	5	—	ns
tderate	Timing deration for loading over C_{LD}(3, 4)	—	—	0.5	—	0.5	ns/ 25pF

NOTES:

9051 tbl 22

1. All timings referenced to 1.5V unless specified otherwise.
2. The AC values listed here reference timing diagrams contained in the *R3721 Hardware User's Manual* and this data sheet.
3. Guaranteed by design.
4. This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25pF over the specified test load condition, unless specified otherwise.
5. Test Conditions refer to the capacitive load and V_{OH} and V_{OL} level of outputs. Refer to the AC test conditions diagram for more information.

PIN CONFIGURATION



84-Pin PLCC
Top View

NOTE:
1. Reserved pin must be pulled high.

6

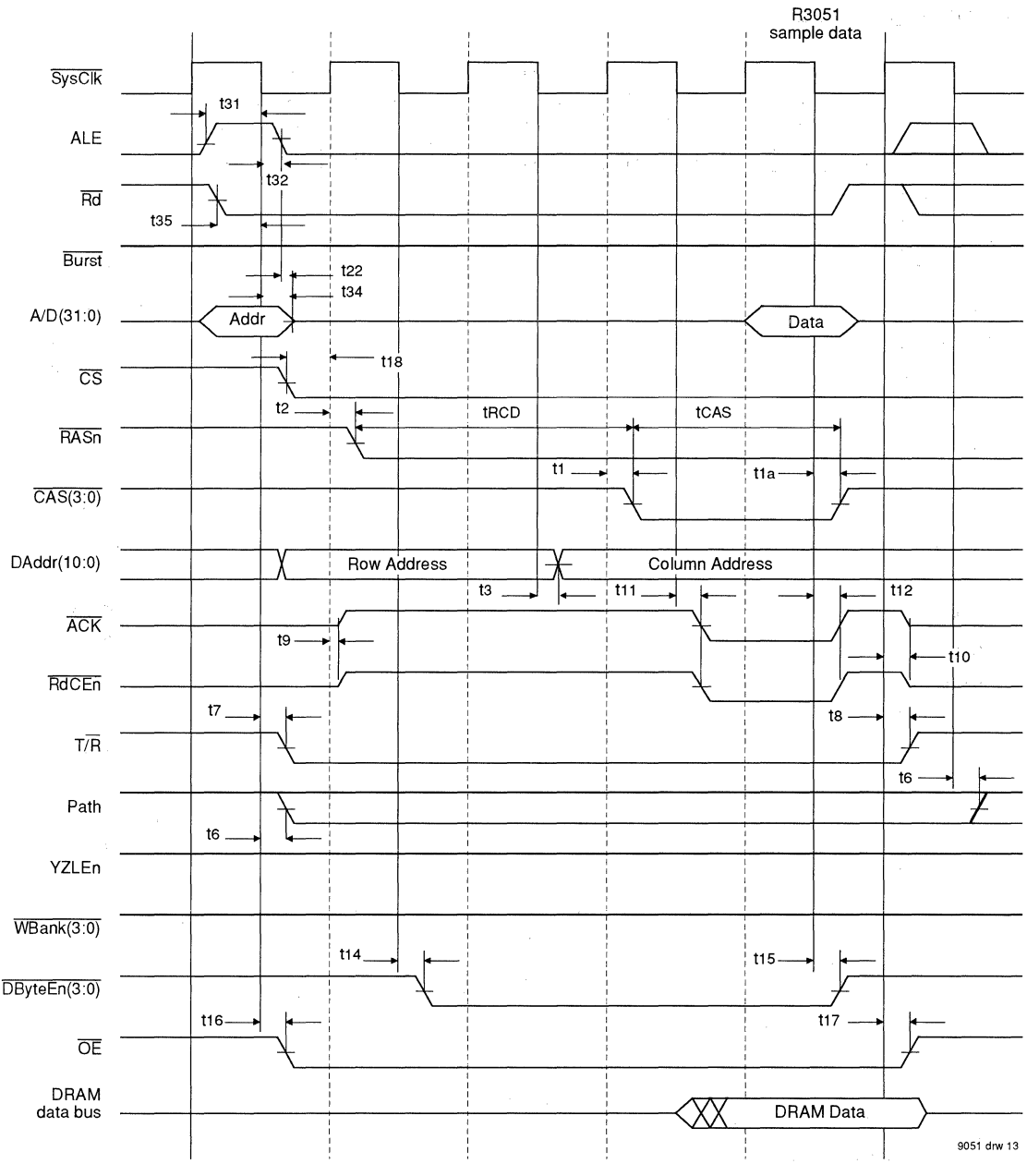


Figure 11. Single Read in Non-Interleaved Memory System

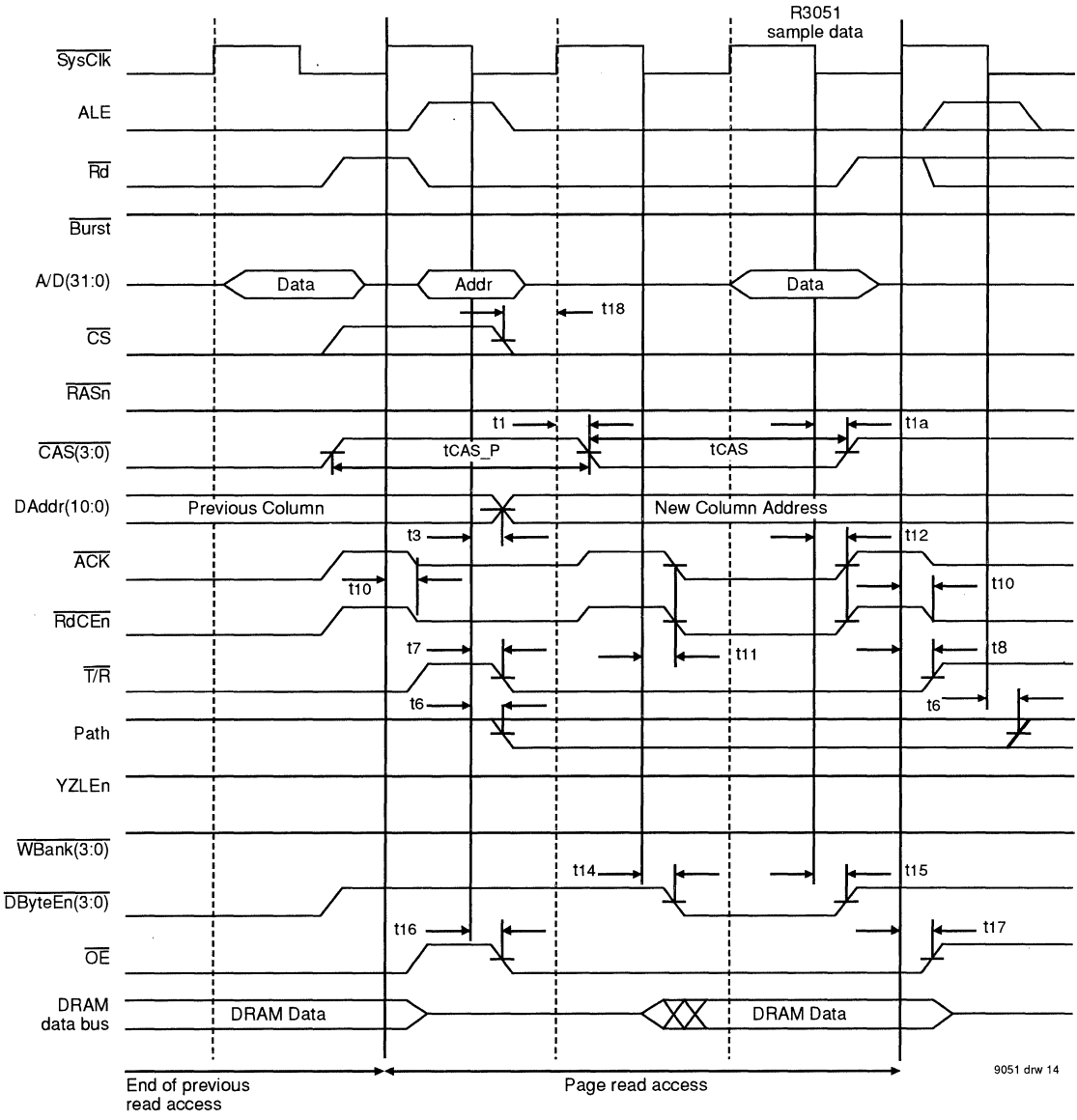


Figure 12. Page Mode Read in Non-Interleaved Memory System

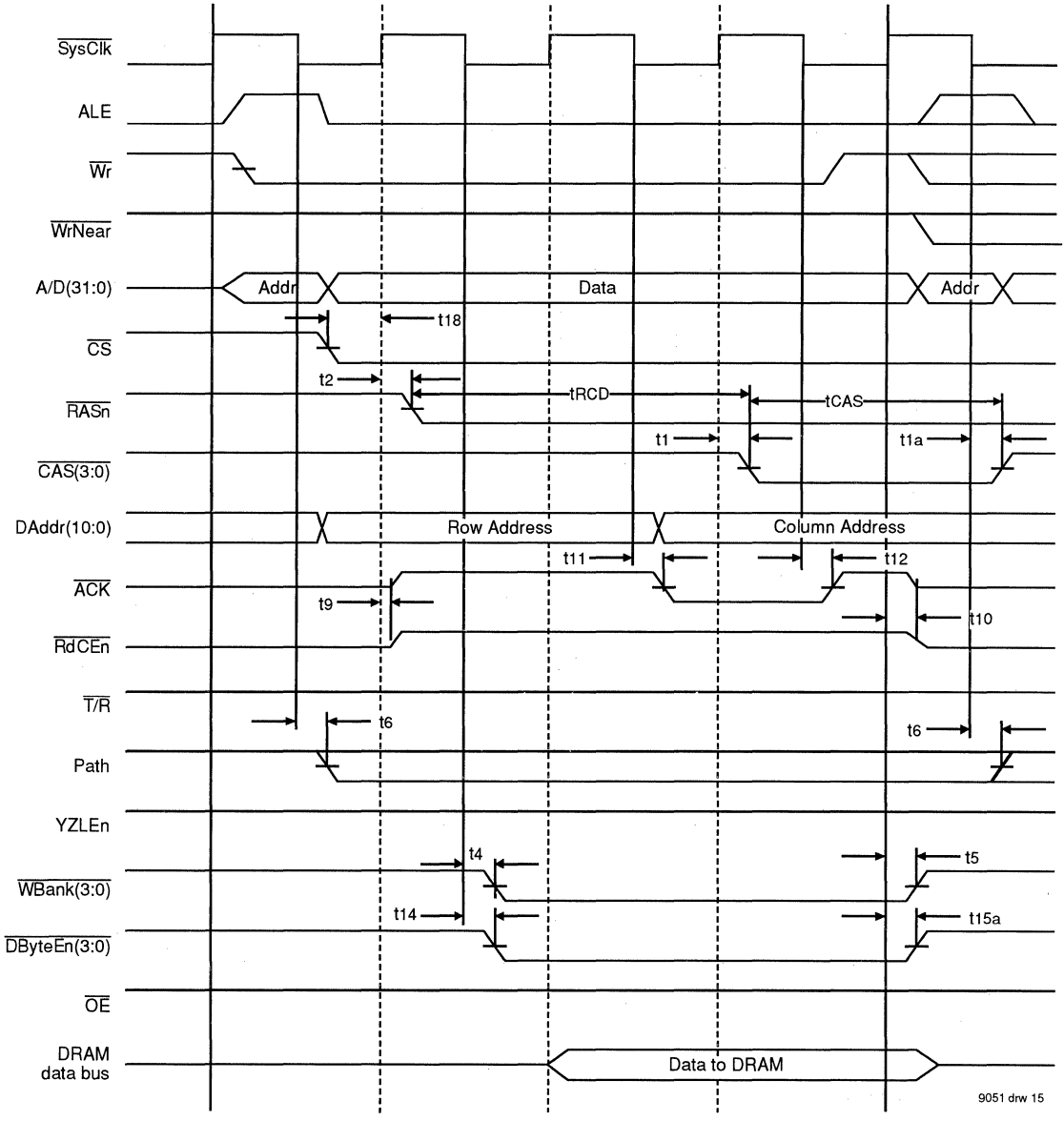


Figure 13. Single Write in Non-Interleaved Memory System

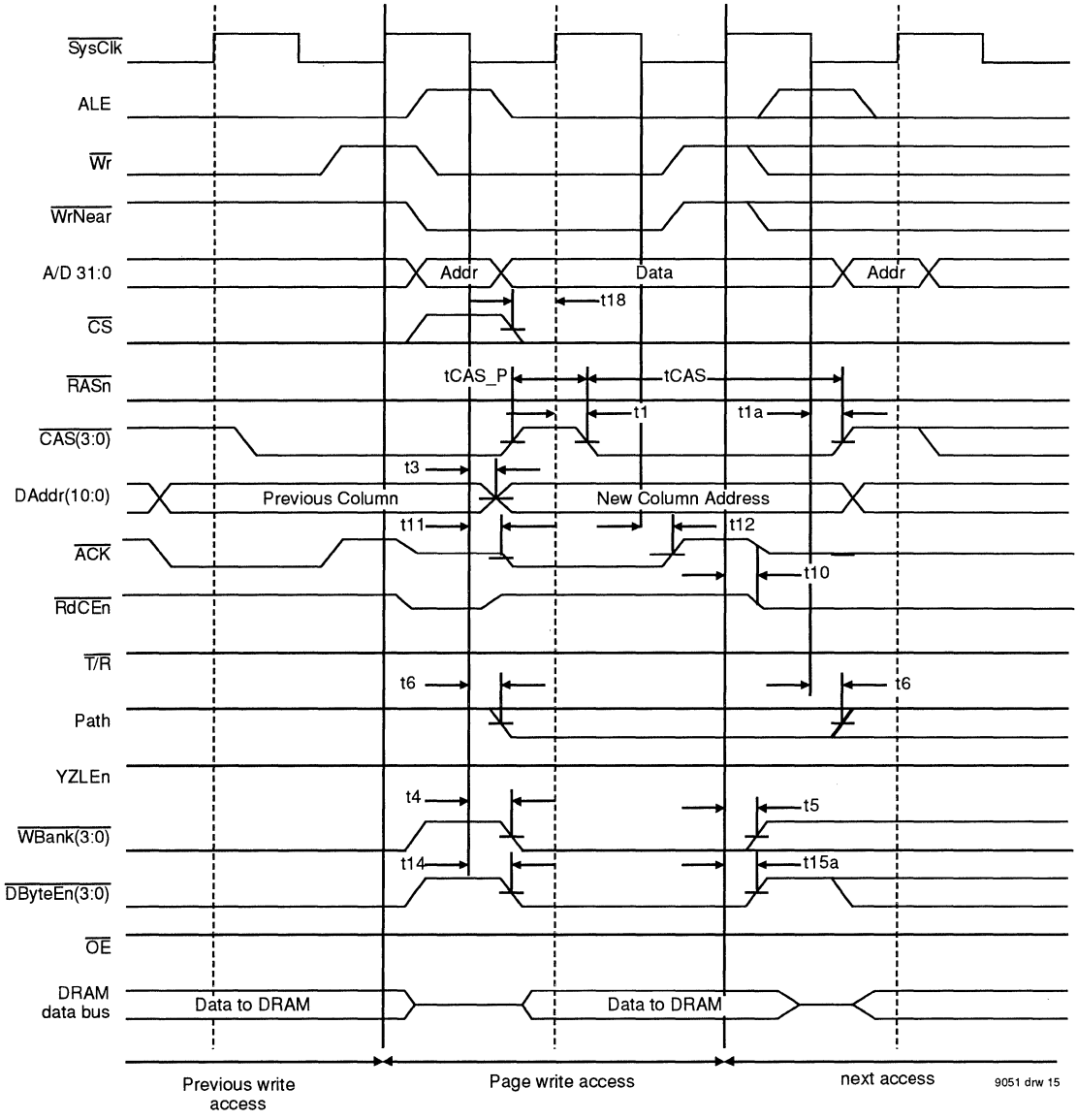


Figure 14. Page Mode Write in Non-Interleaved Memory System

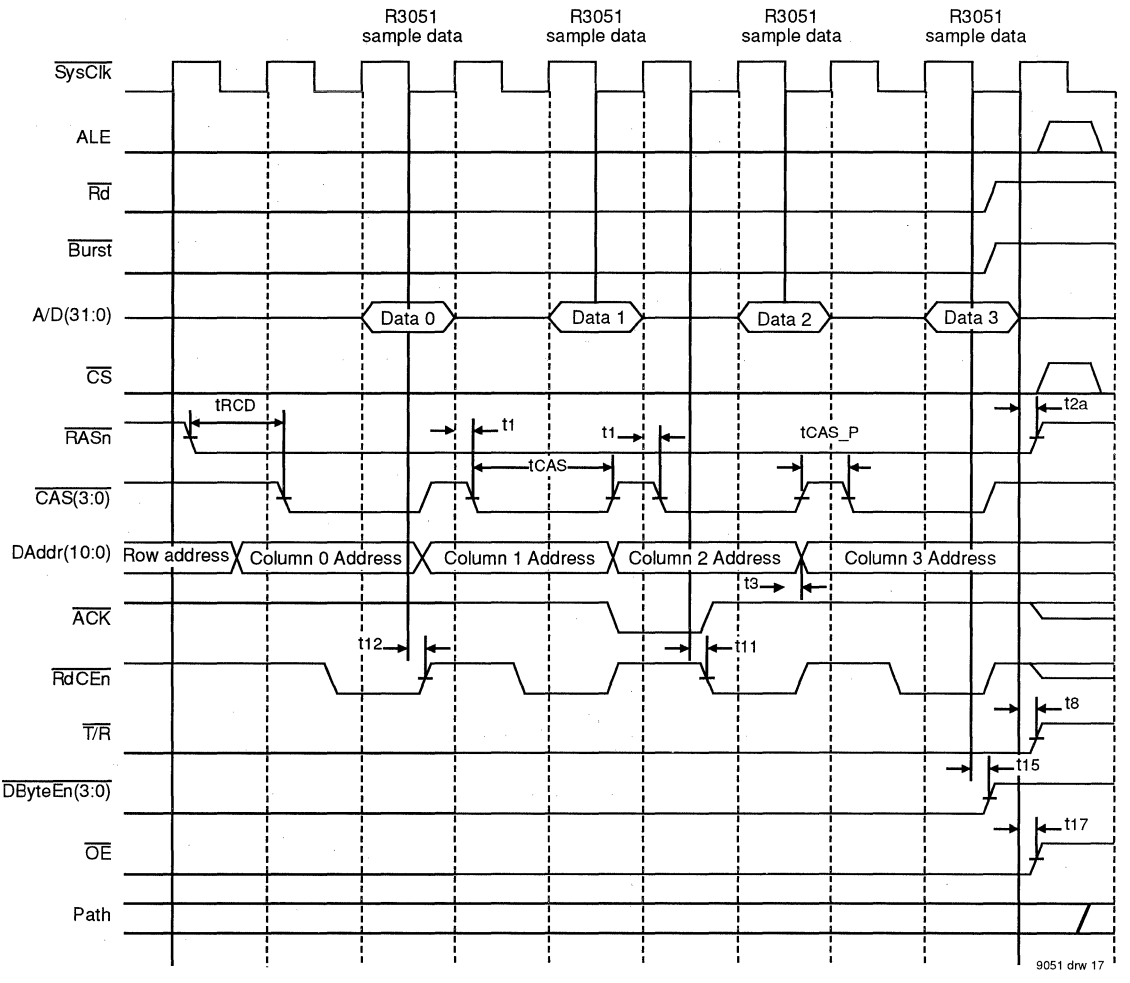


Figure 15. Quad Word Read in Non-Interleaved System

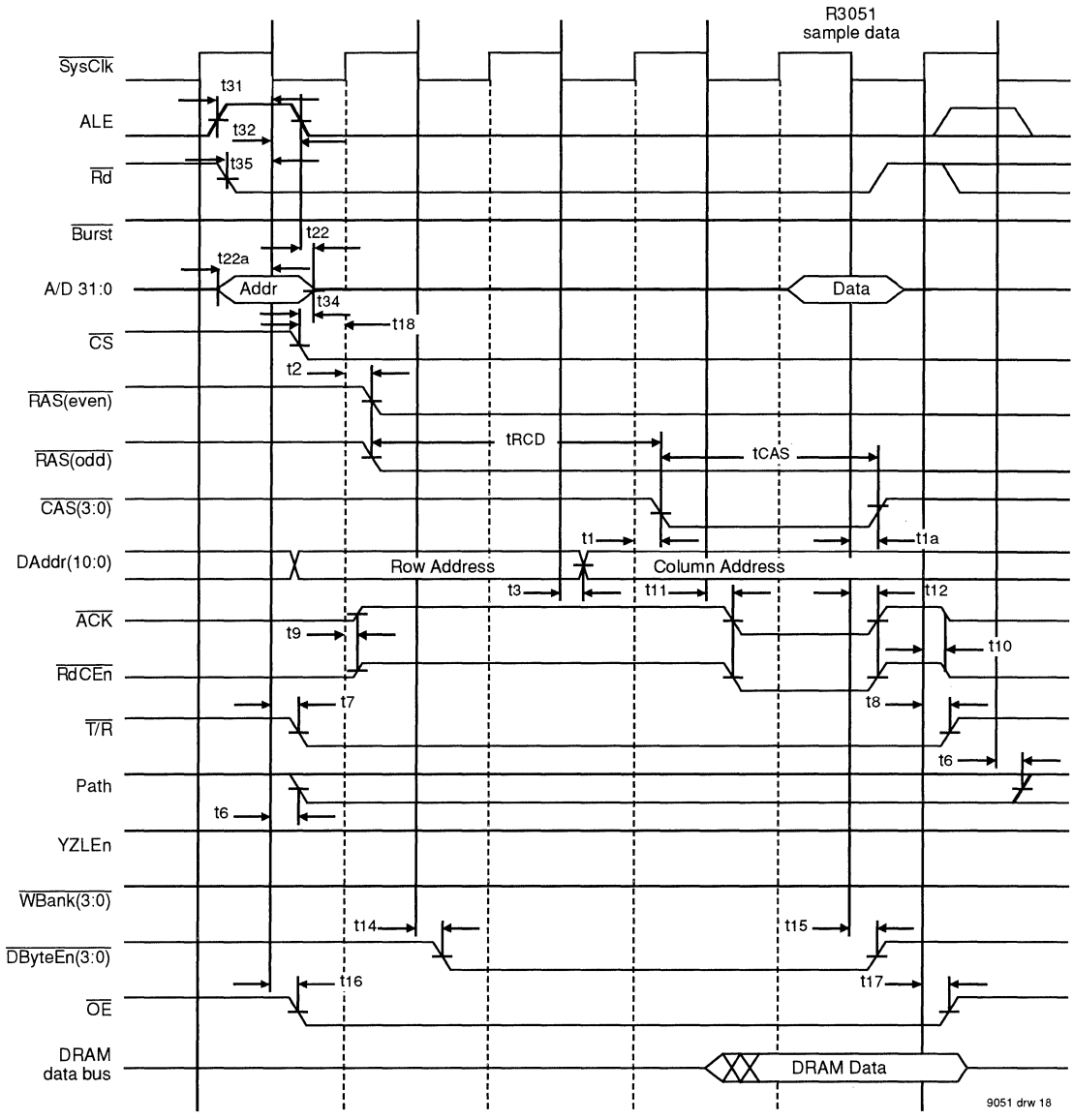


Figure 16. Single Read in Interleaved Memory

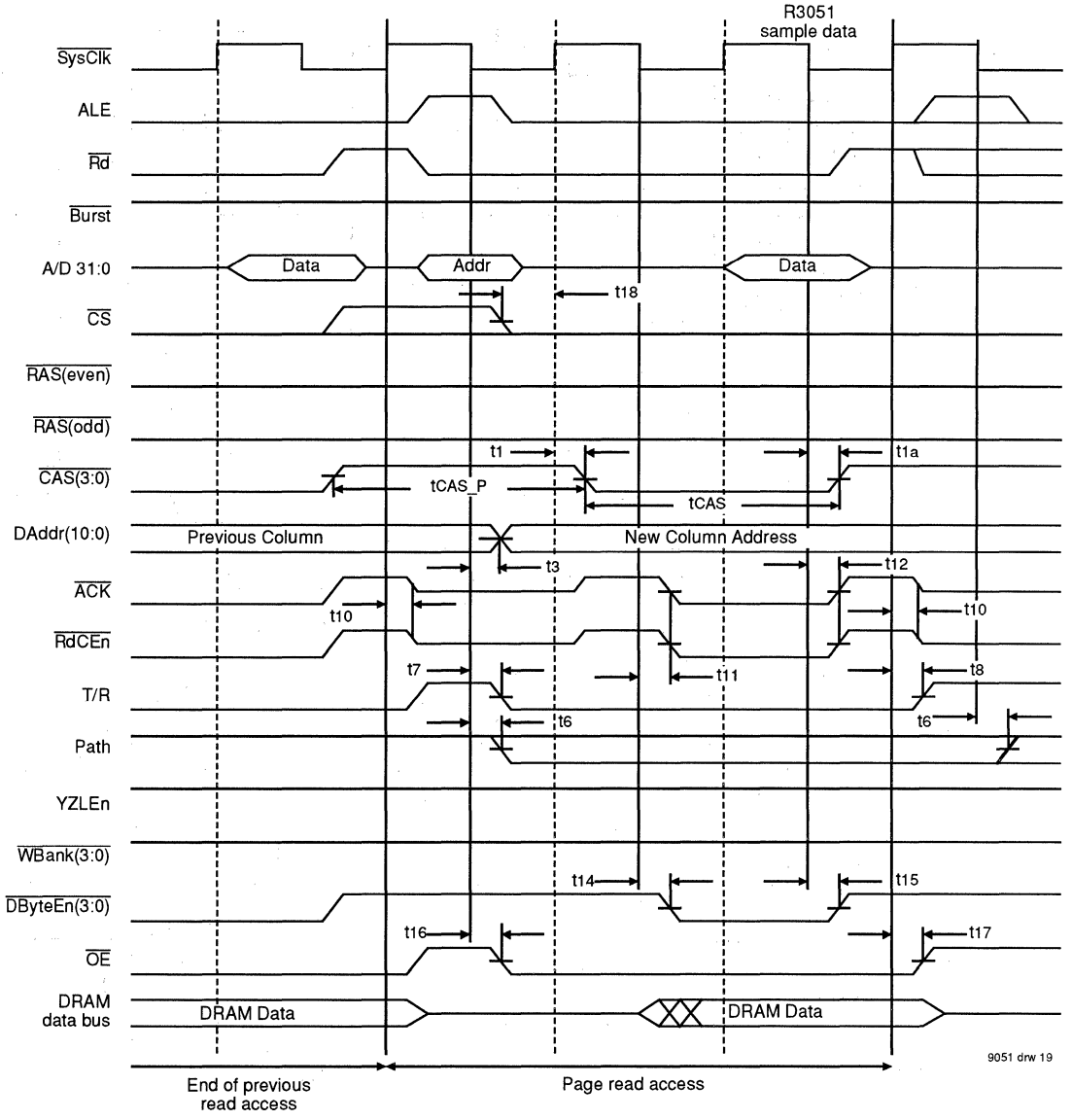


Figure 17. Page Mode Read of Interleaved Memory

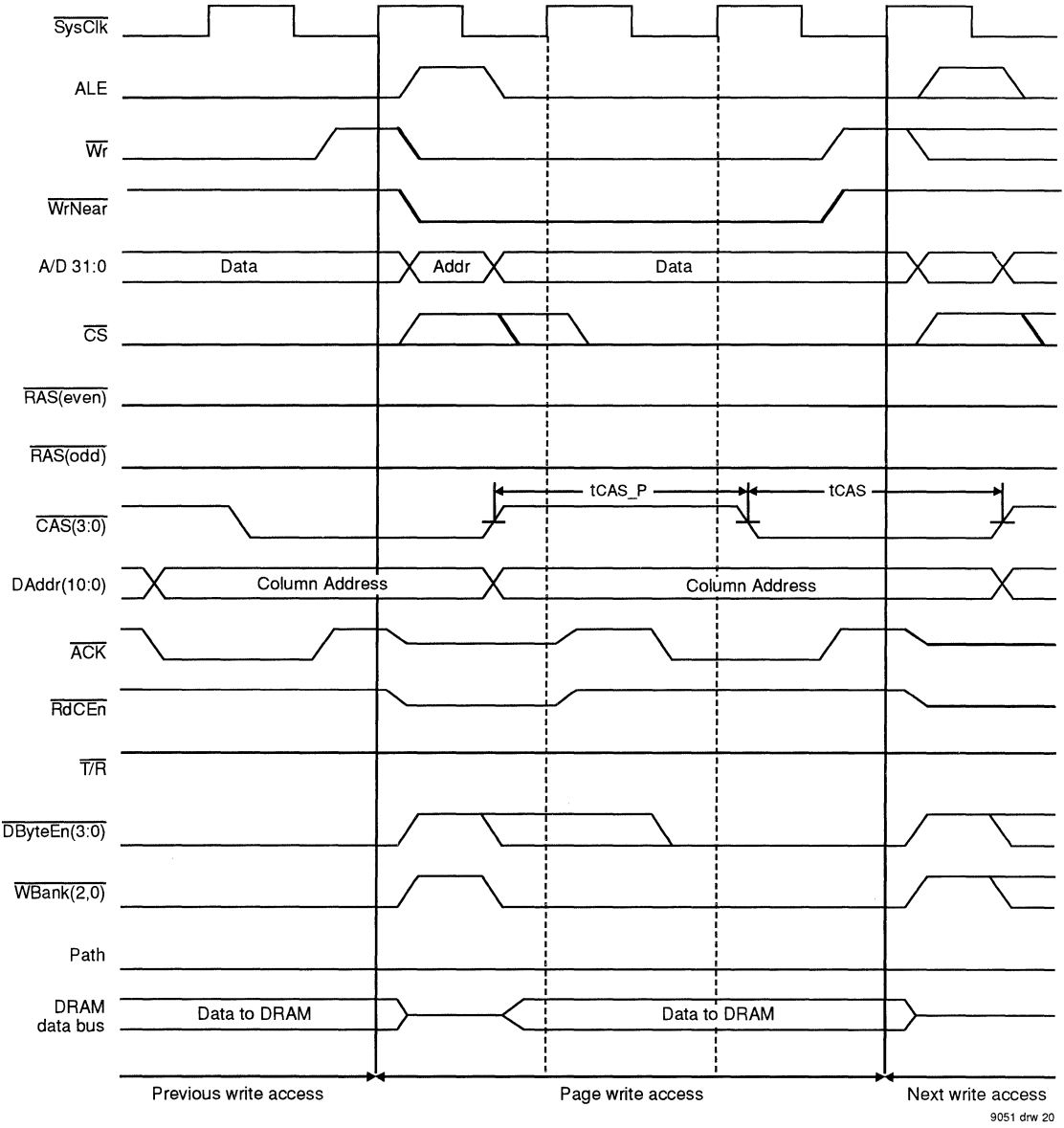


Figure 18. Page Mode Write to Interleaved Memory

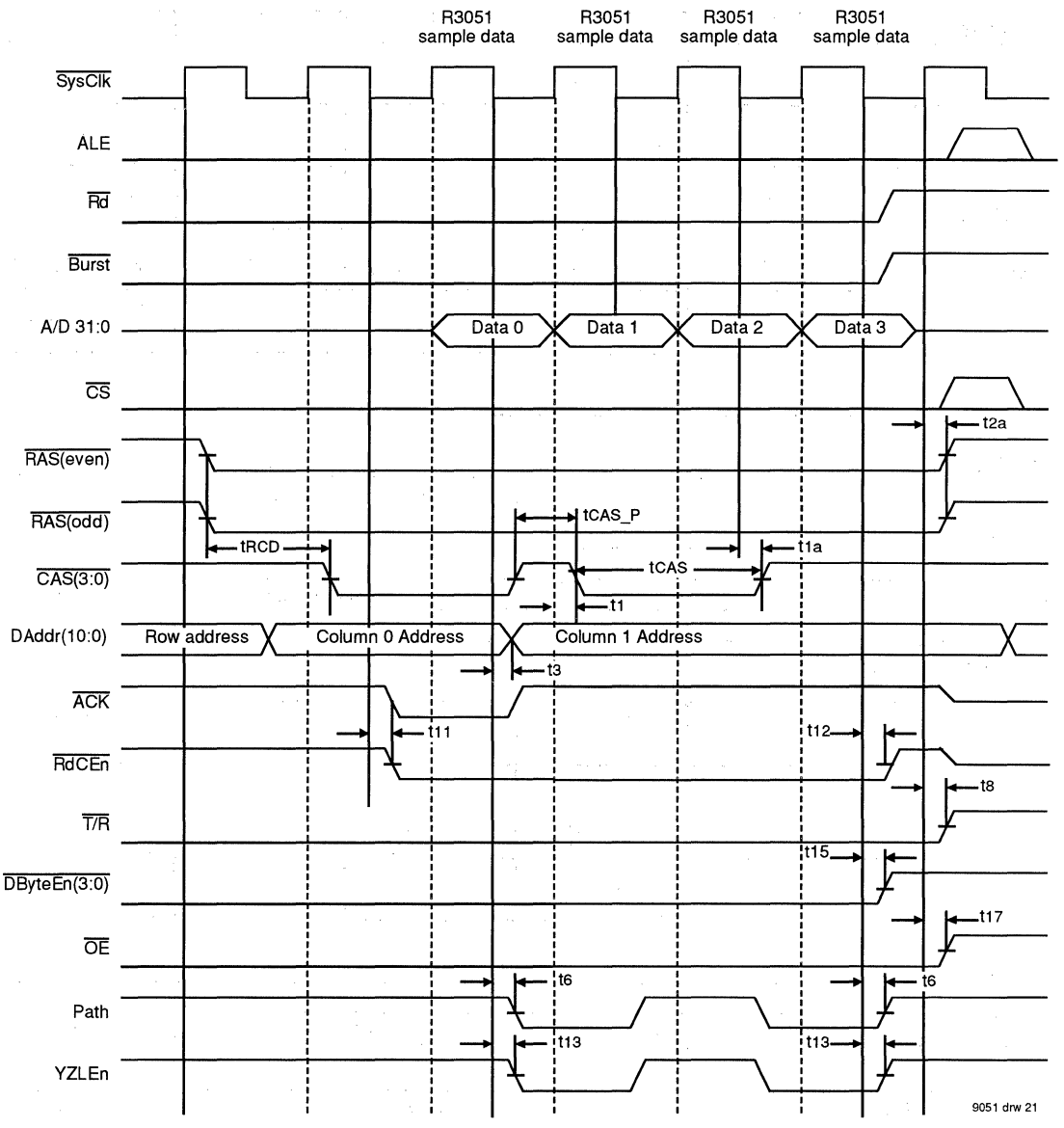


Figure 19. Quad Word Read from Interleaved Memory

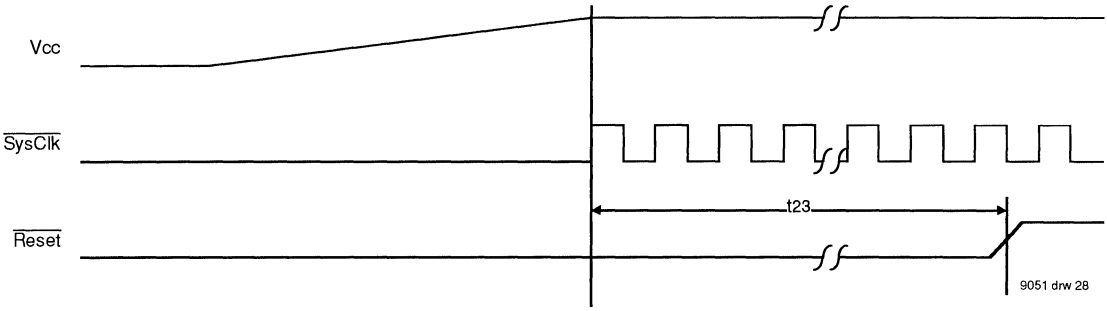


Figure 20. Power On Reset

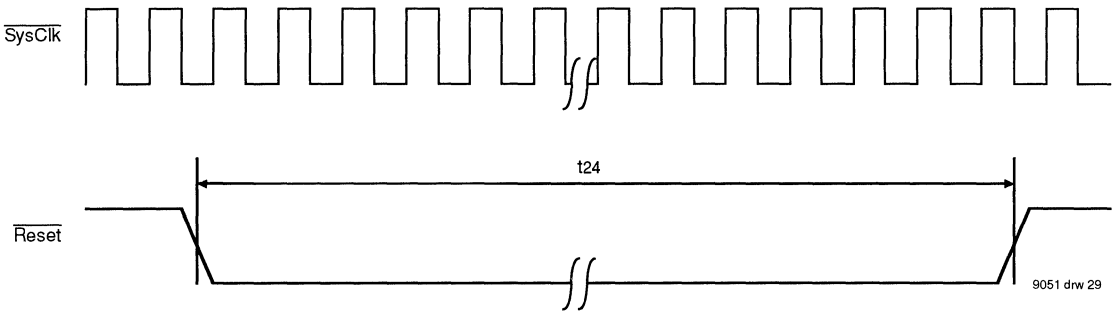


Figure 21. Warm Start Reset

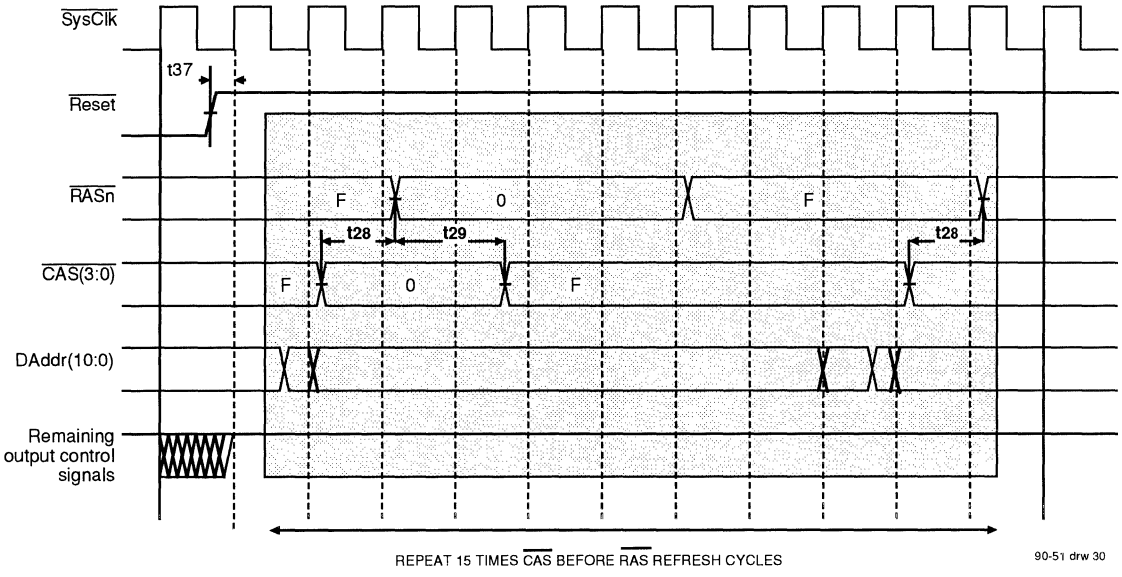


Figure 22. CAS-before-RAS Reset Sequence

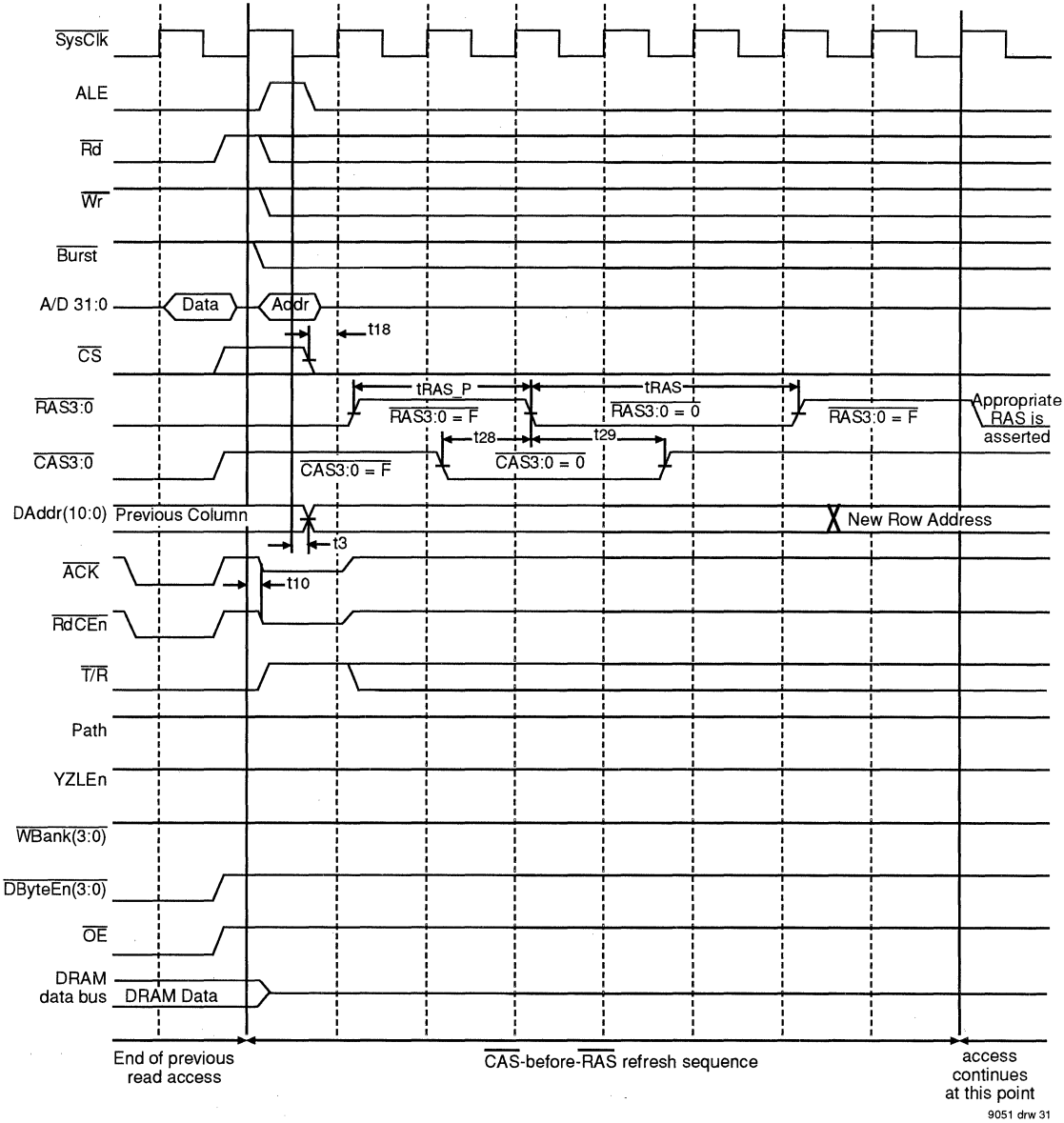


Figure 23. CAS-before-RAS DRAM Refresh

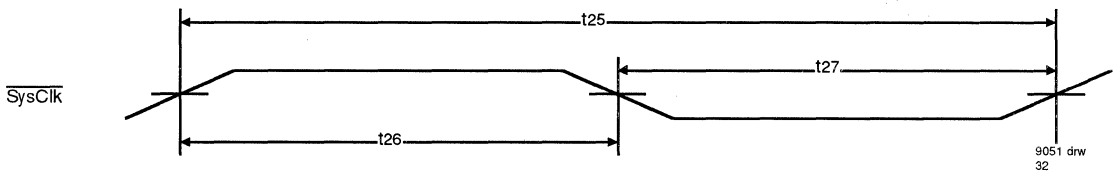
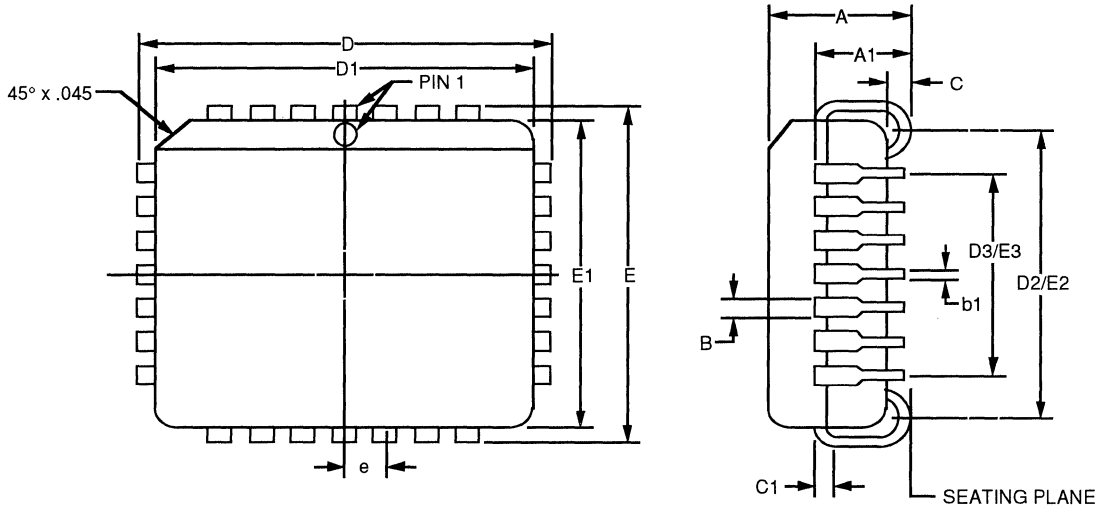


Figure 24. Input Clocking

84 LEAD PLCC (SQUARE)



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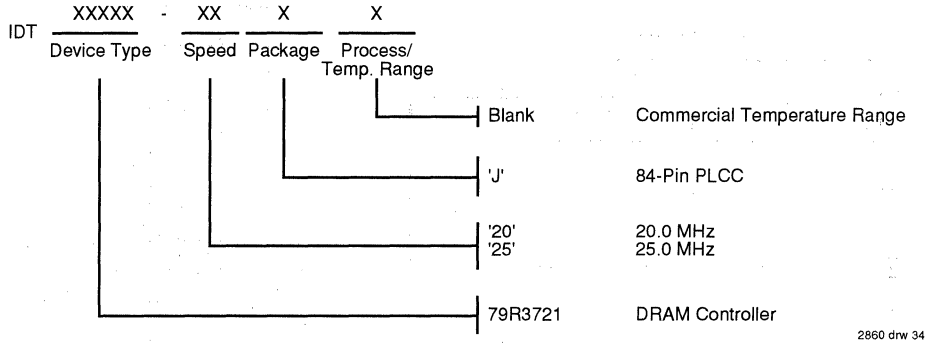
NOTES:
1. All dimensions are in inches, unless otherwise noted.
2. BSC—Basic lead Spacing between Centers.
3. D & E do not include mold flash or protutions.
4. Formed leads shall be planar with respect to one another and within .004" at the seating plane.
5. ND & NE represent the number of leads in the D & E directions respectively.
6. D1 & E1 should be measured from the bottom of the package.

DWG #	J84-1	
# of Leads	84	
Symbol	Min.	Max.
A	165	.180
A1	.095	.115
B	.026	.032
b1	.013	.021
C	.020	.040
CI	.008	.012
D	1.185	1.195
D1	1.150	1.156
D2/E2	1.090	1.130
D3/E3	1.000 REF	
E	1.185	1.195
E1	1.150	1.156
e	.050 BSC	
ND/NE	21	

9051 tbl 23

6

ORDERING INFORMATION



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Integrated Device Technology, Inc.

16-BIT TRI-PORT BUS EXCHANGER

IDT73720/A

FEATURES:

- High-speed 16-bit bus exchange for interbus communication in the following environments:
  - — Multi-way interleaving memory
  - — Multiplexed address and data busses
- Direct interface to R3051 family RISChipSet™
  - — R3051™ family of integrated RISController™ CPUs
  - — R3721 DRAM controller
- Data path for read and write operations
- Low noise 12mA TTL level outputs
- Bidirectional 3-bus architecture: X, Y, Z
  - — One CPU bus: X
  - — Two (interleaved or banked) memory busses: Y & Z
  - — Each bus can be independently latched
- Byte control on all three busses
- Source terminated outputs for low noise and undershoot control
- 68-pin PLCC and 80-pin PQFP package
- High-performance CMOS technology.

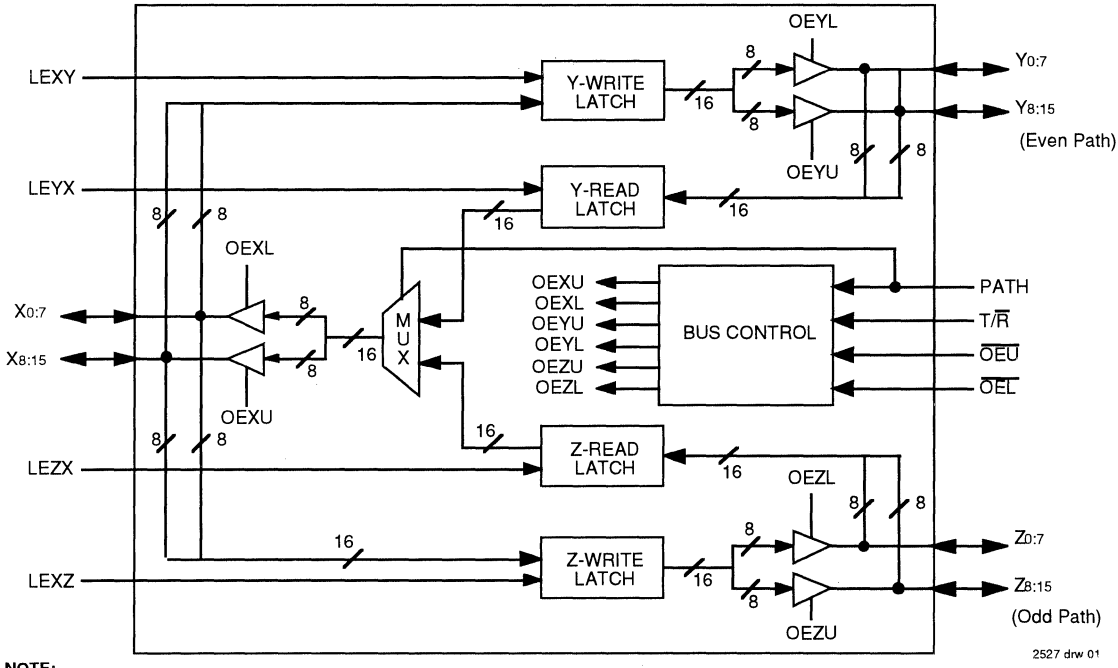
DESCRIPTION:

The IDT73720/A Bus Exchanger is a high-speed 16-bit bus exchange device intended for inter-bus communication in interleaved memory systems and high-performance multiplexed address and data busses.

The Bus Exchanger is responsible for interfacing between the CPU A/D bus (CPU address/data bus) and multiple memory data busses.

The 73720/A uses a three bus architecture (X, Y, Z), with control signals suitable for simple transfer between the CPU bus (X) and either memory bus (Y or Z). The Bus Exchanger features independent read and write latches for each memory bus, thus supporting a variety of memory strategies. All three ports support byte enable to independently enable upper and lower bytes.

FUNCTIONAL BLOCK DIAGRAM



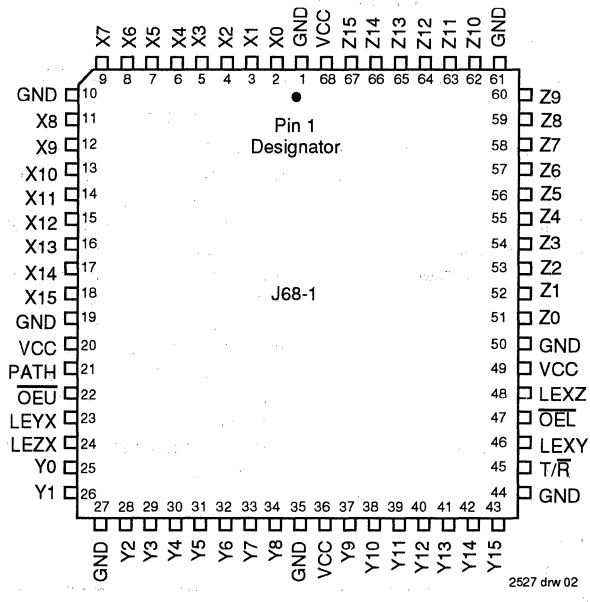
2527 drw 01

Figure 1. 73720 Block Diagram

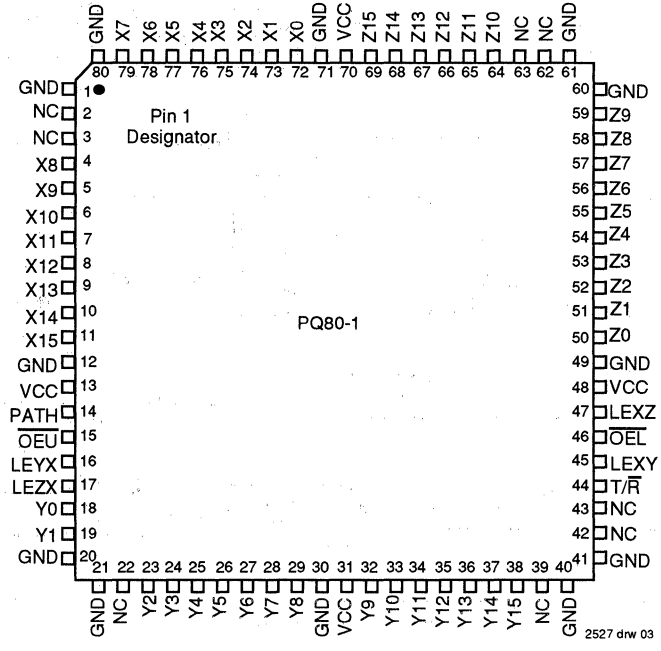
NOTE:

1. Logic equations for bus control:
   OEXU = T/$\overline{R}$* . $\overline{OEU}$*; OEXL = T/$\overline{R}$* . $\overline{OEL}$*; OEYU = T/$\overline{R}$. PATH . $\overline{OEU}$*
   OEYL = T/$\overline{R}$. PATH . $\overline{OEL}$*; OEZU = T/$\overline{R}$. PATH* . $\overline{OEU}$*; OEZL = T/$\overline{R}$. PATH* . $\overline{OEL}$*

PIN CONFIGURATIONS



PLCC
TOP VIEW



PQFP
TOP VIEW

PIN DESCRIPTION

Signal	I/O	Description
X(0:15)	I/O	Bidirectional Data Port X. Usually connected to the CPU's A/D (Address/Data) bus.
Y(0:15)	I/O	Bidirectional Data port Y. Connected to the even path or even bank of memory.
Z(0:15)	I/O	Bidirectional Data port Z. Connected to the odd path or odd bank of memory.
LEXY	I	Latch Enable input for Y-Write Latch. The Y-Write Latch is open when LEXY is HIGH. Data from the X-port (CPU) is latched on the HIGH-to-LOW transition of LEXY
LEXZ	I	Latch Enable input for Z-Write Latch. The Z-Write Latch is open when LEXZ is HIGH. Data from the X-port (CPU) is latched on the HIGH-to-LOW transition of LEXZ.
LEYX	I	Latch Enable input for the Y-Read Latch. The Y-Read Latch is open when LEYX is HIGH. Data from the even path Y is latched on the HIGH-to-LOW transition of LEYX.
LEZX	I	Latch Enable input for the Z-Read Latch. The Z-Read Latch is open when LEZX is HIGH. Data from the odd path Z is latched on the HIGH-to-LOW transition of LEZX
PATH	I	Even/Odd Path Selection. When HIGH, PATH enables data transfer between the X-Port and the Y-port (even path). When low, PATH enables data transfer between the X-Port and the Z-Port (odd path).
T/$\overline{R}$	I	Transmit/Receive Data. When HIGH, Port X is an input Port and either Port Y or Z is an output Port. When low, Port X is an output Port while Ports Y & Z are input Ports
$\overline{OEU}$	I	Output Enable for Upper byte. When LOW, the Upper byte of data is transfered to the port specified by PATH in the direction specified by T/$\overline{R}$.
$\overline{OEL}$	I	Output Enable for Lower byte. When LOW, the Lower byte of data is transfered to the port specified by PATH in the direction specified by T/$\overline{R}$.

2527 tbl 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +125	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2527 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE: 2527 tbl 04

1. This parameter is guaranteed by device characterization, but is not production tested.

TRUTH TABLE

Path	T/$\overline{R}$	$\overline{OEU}$	$\overline{OEL}$	Functionality
L	L	L	L	Z→X (16-bits)–Read Z(1)
L	H	L	L	X→Z (16 bits)–Write Z(1)
H	L	L	L	Y→X (16-bits)–Read Y(2)
H	H	L	L	X→Y (16 bits)–Write Y(2)
X	X	H	H	All output buffers are disabled
X	X	H	L	Transfer of lower 8 bits (0:7) as per PATH & T/$\overline{R}$
X	X	L	H	Transfer of upper 8 bits (8:15) as per PATH & T/$\overline{R}$

NOTES: 2527 tbl 01

1. For Z→X and X→Z transfers, Y-port output buffers are tristated.
2. For Y→X and X→Y transfers, Z-port output buffers are tristated.

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ARCHITECTURE OVERVIEW

The Bus Exchanger is used to service both read and write operations between the CPU and the dual memory busses. It includes independent data path elements for reads from and writes to each of the memory banks (Y and Z). Data flow control is managed by a simple set of control signals, analogous to a simple transceiver. In short, the Bus Exchanger allows bidirectional communication between ports X and Y and ports X and Z as illustrated in figure 1.

The data path elements for each port include:

Read Latch: Each of the memory ports Y and Z contains a transparent latch to capture the contents of the memory bus. Each latch features an independent latch enable.

Write Latch: Each memory port Y and Z contains an independent latch to capture data from the CPU bus during writes. Each memory port write latch features an independent latch enable, allowing write data to be directed to a specific memory port without disrupting the other memory port.

Data Flow Control Signals

T/$\overline{R}$ (Transmit/$\overline{\text{Receive}}$). This signal controls the direction of data transfer. A transmit is used for CPU writes, and a receive is used for read operations.

$\overline{OEU}$, $\overline{OEL}$ are the output enable control signals to select upper or lower bytes of all three ports.

Path: The path control signal is used to select between the even memory path Y and the odd memory path Z during read or write operations. Path selects the memory port to be connected to the CPU bus (X-port), and is independent of the latch enable signals. Thus, it is possible to transfer data from one memory port to the CPU bus (X) while capturing data from the other memory port.

MEMORY READ OPERATIONS

Latch Mode

In this mode the read operation consists of two stages. During the first stage, the data present at the memory port is captured by the read latch for that memory port. During a subsequent stage, data is brought from a selected memory port to the CPU A/D port X by using output enable control.

The read operation is selected by driving T/$\overline{R}$ low. The read is managed using the Path input to select the memory port (Y or Z); the LEYX/LEZX enable the data capture into the corresponding Read Latch.

In this way, memory interleaving can be performed. While data from one bank is output onto the CPU bus, data on the other bank is captured in the other memory port. In the next cycle, the Path input is changed, enabling the next data element onto the CPU bus, while the first bank is presented with a new data element.

Transparent Mode

The Bus Exchanger may be used as a data transceiver by leaving all latches open or transparent.

Memory Write Operations

Memory write operations also consist of two distinct stages. During one stage, the write data is captured into the selected memory port write latch. During a later stage, the memory is presented on the memory port bus

The write operation is selected by driving T/$\overline{R}$ high. Writes are thus performed using the Path input to select the memory port (Y or Z). The LEXY/LEXZ capture data in the corresponding Write Latch.

Note that it is possible to utilize the bus exchanger's write resources as an additional write buffer, if desired; the CPU A/D bus can be freed up once the data has been captured by the Bus Exchanger.

APPLICATIONS

Use as Part of the R3051 Family ChipSet

Figure 2 shows the use of the Bus Exchanger in a typical R3051 based system.

In write transactions, the R3051 drives data on the CPU bus. The latch enables are held open through the entire write; thus, the bus exchanger is used like a transceiver. The appropriate LEXY/LEXZ signal is derived from ALE (Logic low- indicating that the processor is driving data) and the low order address bit. The rising edge of $\overline{Wr}$ from the CPU, ends the write operation.

During read transactions, the memory system is responsible for generating the input control signals to cause data to be captured at the memory ports. The memory controller is also responsible for acknowledging back to the CPU that the data is available, and causing the appropriate path to be selected.

The R3721 DRAM controller for the R3051 family uses the transparent latches of the read ports. The R3721 directly controls the inputs of the bus exchanger, during both reads and writes. Consult the R3721 data sheet for more information on these control signals.

Use in a general 32-bit System

Figures 3 and 4 illustrate the use of the Bus Exchanger in a 32-bit microprocessor based system. Note the reduced pin count achieved with the Bus Exchanger.

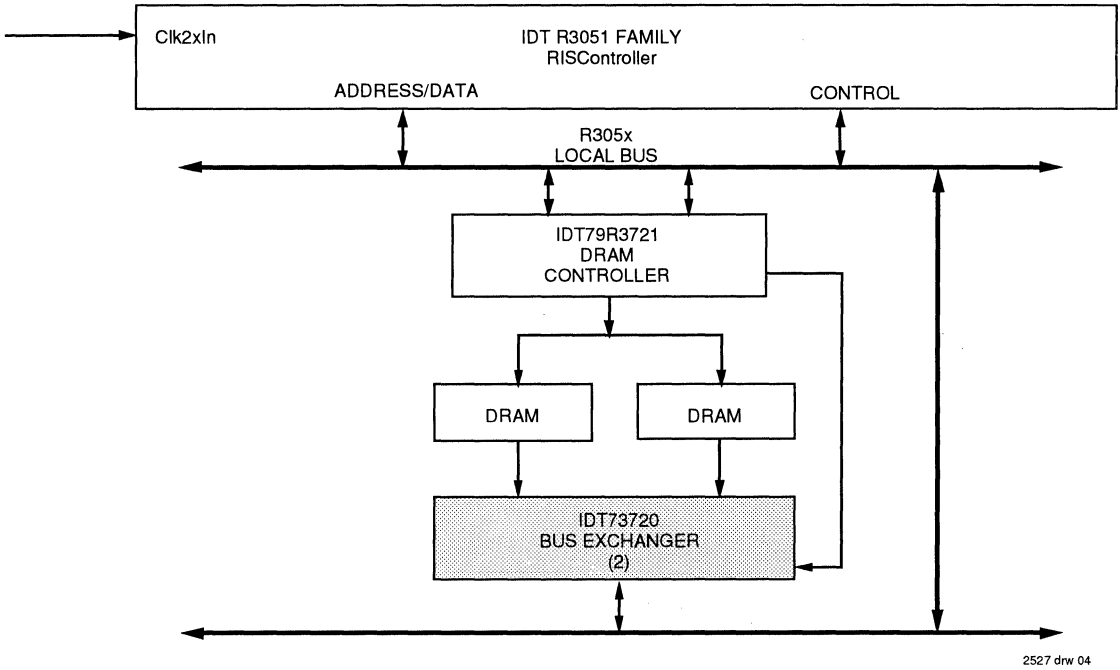


Figure 2. Bus Exchanger Used in R3051 Family System

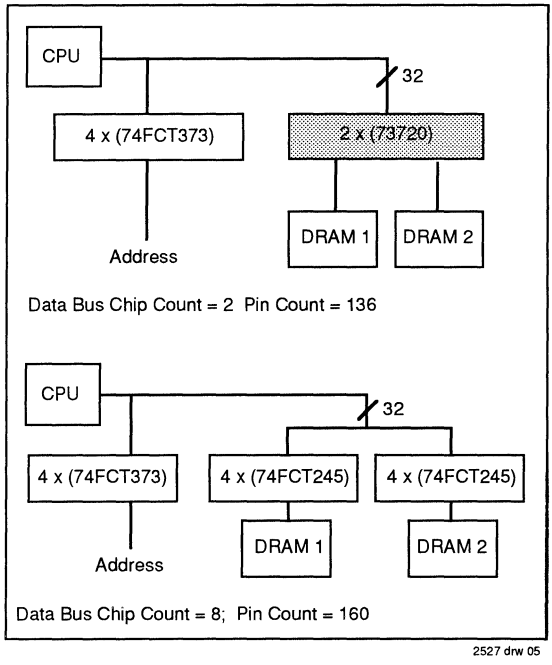


Figure 3. CPU System with Transparent Data Path (2-way Interleaving)

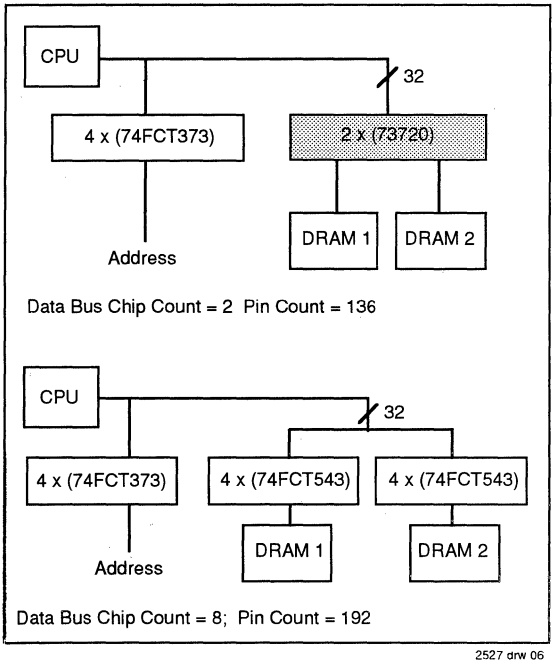


Figure 4. CPU System with Latched Data Path (2-way Interleaving)

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level			2.0	—	—	V
V_{IL}	Input LOW Level			—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IH} = 2.7V	Inputs only	—	—	5.0	µA
			I/O pins	—	—	5.0	
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IL} = 0.5V	Inputs only	—	—	–5.0	µA
			I/O pins	—	—	–5.0	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}[3]	Short Circuit Current	V_{CC} = Max., V_O = GND		–60.0	—	–200.0	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}, I_{OH} = –12mA		2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}, I_{OL} = 12mA		—	0.3	0.5	V
V_H	Input Hysteresis All inputs	V_{CC} = 5V		—	200.0	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = 3.4 V[4]		—	0.5	2.0	mA/ Input
I_{CCD}	Dynamic Power Supply Current[5]	V_{CC} = Max. V_{IN} = V_{CC} or GND Outputs Disabled $\overline{OE}$ = V_{CC} One Input Toggling 50 % Duty Cycle		—	0.25	0.5	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. V_{IN} = V_{CC} or GND Outputs Disabled 50 % Duty Cycle $\overline{OE}$ = V_{CC} fi = 10MHz One Bit Toggling		—	2.7	6.5	mA

NOTES: 2527 tbl 05

1. For conditions shown as Max. or Min., use appropriate V_{CC} value.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
5. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL HIGH Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs HIGH
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megaherz.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 5

2527 tbl 06

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = 0° to +70°C)

Symbol	Parameter		Test Conditions[1]	73720A		73720		Units
				Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	X to Y & X to Z Latches enabled		C_L = 50pF R_L = 500 Ohms	—	—	2.0	7.5	ns
t_{PLH} t_{PHL}	Y to X & Z to X Latches enabled			—	—	2.0	7.5	ns
t_{PLH} t_{PHL}	Latch Enable to Y & Z Port	LEXY to Y LEXZ to Z		—	—	2.0	8.5	ns
t_{PLH} t_{PHL}	Latch Enable to X	LEYX to X LEZX to X		—	—	2.0	8.5	ns
t_{PLH} t_{PHL}	Path to X Port Propagation Delay			—	—	2.0	8.5	ns
t_{HZ} t_{LZ}	Y & Z Port Disable Time ($T/\overline{R}$, PATH, $\overline{OEU}$, $\overline{OEL}$)[3]			—	—	2.0	9.5	ns
t_{ZH} t_{ZL}	Y & Z Port Enable Time ($T/\overline{R}$, PATH, $\overline{OEU}$, $\overline{OEL}$)[3]			—	—	2.0	10.5	ns
t_{HZ} t_{LZ}	X-Port DisableTime ($T/\overline{R}$, $\overline{OEU}$, $\overline{OEL}$)[3]			—	—	2.0	9.5	ns
t_{ZH} t_{ZL}	X-Port Enable Time ($T/\overline{R}$, $\overline{OEU}$, $\overline{OEL}$)[3]			—	—	2.0	10.5	ns
t_{SU}	Port to LE Set-up time			—	—	2.0	—	ns
t_H	Port to LE Hold time			—	—	1.5	—	ns

2527 tbl 07

NOTES:
1. All timings are referenced to 1.5 V.
2. This parameter is guaranteed by design, but not tested.
3. Bus turnaround times are guaranteed by design, but not tested. ($T/\overline{R}$ enable/disable times).

TEST CIRCUITS AND WAVEFORMS

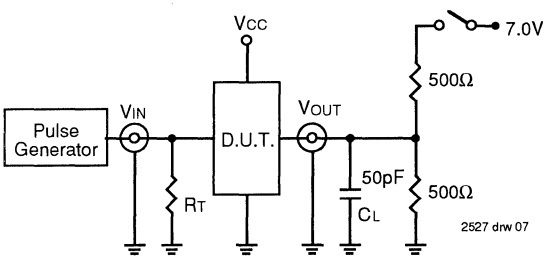


Figure 5. Test Circuit for all outputs

SWITCH POSITION

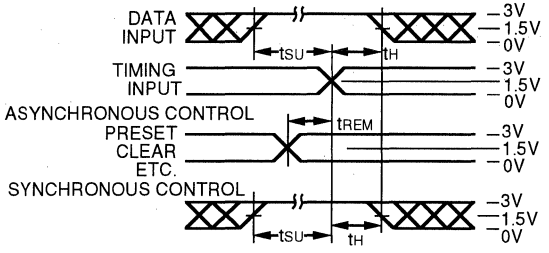
Test	Switch
Disable Low	Closed
Enable Low	
All Other Tests	Open

2527 tbl 08

DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

6

SET-UP, HOLD AND RELEASE TIMES



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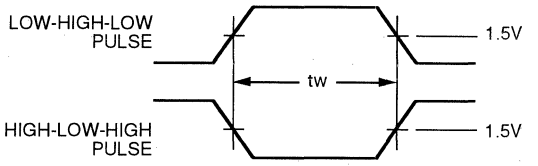
PULSE WIDTH



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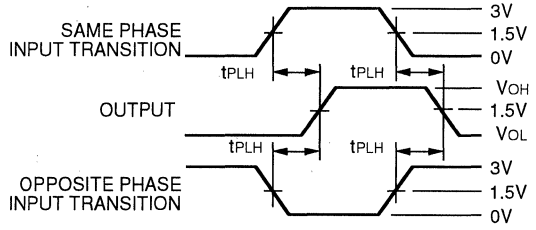
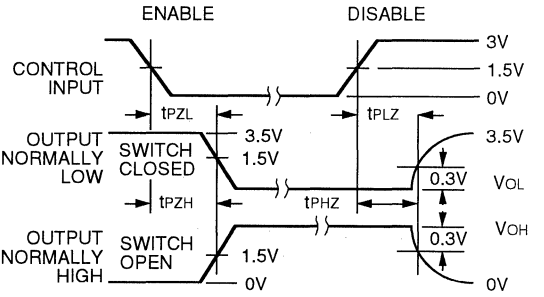
PROPAGATION DELAY



2527 drw 10

ENABLE AND DISABLE TIMES

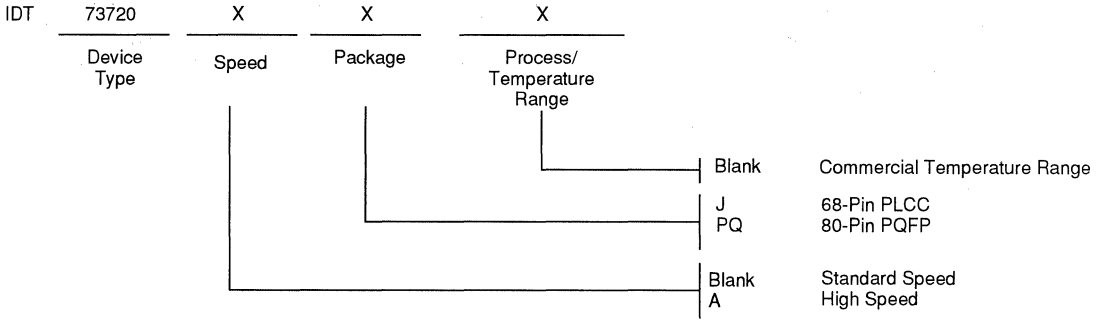


2527 drw 11

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; ZO ≤ 50Ω; tF ≤ 2.5ns; tR ≤ 2.5ns.

ORDERING INFORMATION



2527 drw 12

Integrated Device Technology, Inc.

RASTER IMAGE PROCESSOR
Integrated SystemController™ for IDT R3051 Family

ADVANCE INFORMATION
IDT79R3730

FEATURES:

- Integrated SystemController™ for IDT R3051 Family Raster Image Processors and Laser Printer Controllers
  - Direct interface to R3041, R3051, R3052 and R3081
  - Supports clock frequencies to 40MHz
- High-performance, programmable DRAM controller:
  - Flexible DRAM control for up to 128MB of two-way interleaved or non-interleaved DRAM (up to 8 banks)
  - Wide variety of memory configurations (e.g. different size DRAMs for base and SIMM extensions)
  - DMA channel for memory pattern fill/clear
  - DRAM parity generation/checking
- Programmable I/O ports support glue-less interface support low-cost peripherals
  - Burst DMA channels with chaining
  - On-chip 4-word x 32-bit FIFOs with data packing and unpacking
  - Master/slave peripheral interface
  - 8-bit and 16-bit I/O ports
- Coprocessor DMA interface for accelerator ASICs (e.g. Adobe's Type 1 font rasterizer and PixelBurst™ display list coprocessor)
- Programmable Interrupt Controller
- High-performance programmable video interface
  - 1, 2 or 4 serial video streams support high video bandwidth (bi-level or 4-bit color)
  - Video DMA channels with chaining
  - On-chip 8-word x 32-bit video FIFO
  - Programmable margin counters
  - Video bit rates to 160 megabits per second
  - Supports split stream video
  - Pel counter
- Controls for ROM memory system
  - Programmable controls for up to 24MB of interleaved or non-interleaved ROM/EPROM (up to 6 banks)
  - Burst ROM/EPROM support
  - Glue-less interface for 8-bit boot ROM or EEROM
- General purpose functions
  - Bus timeout counter
  - Rotate assist (0°, 90°, 180°, 270° and mirror) hardware
  - General purpose counter/timer
  - Bit programmable I/O port

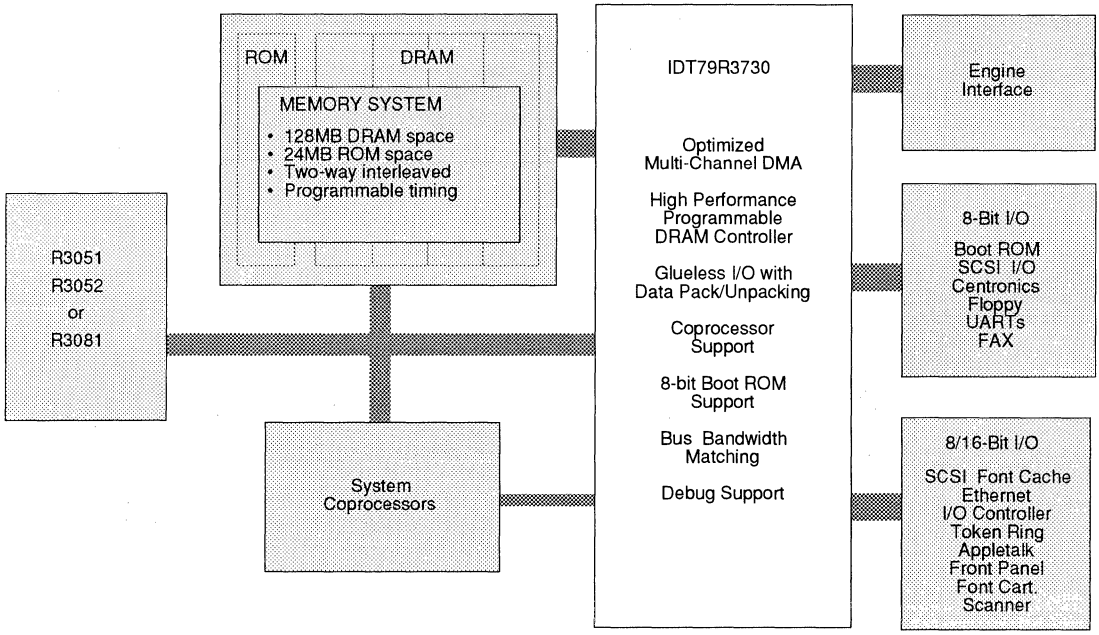


Figure 1. IDT79R3730 System Organization

2906 drw 01

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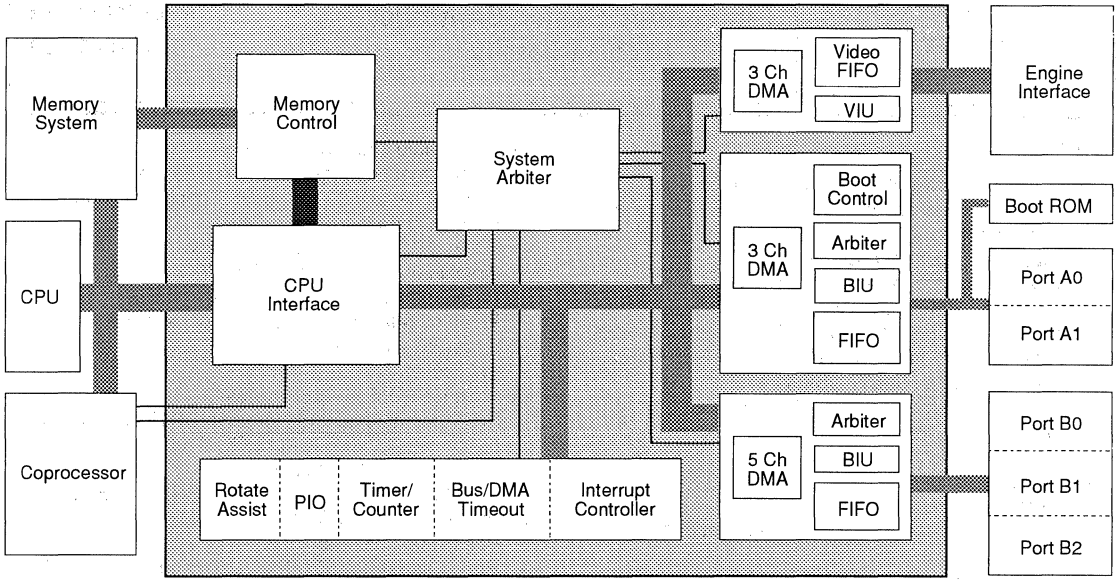
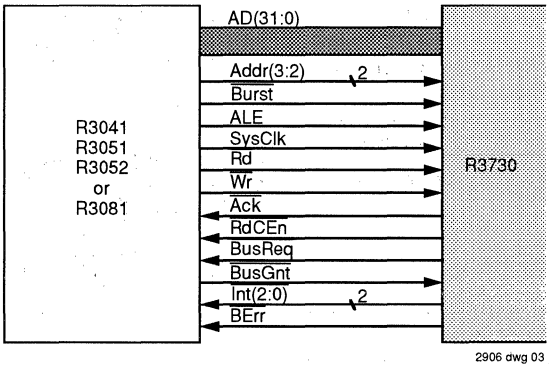


Figure 2. IDT79R3730 Block Diagram

2906 dwg 02

GENERAL DESCRIPTION

The IDT79R3730 SystemController™ is a highly integrated and highly programmable controller for high-performance Raster Image Systems. It contains sophisticated DMA, FIFOs and arbitration logic to provide bandwidth matching between the high-speed CPU/memory bus and slower standard I/O peripherals. The IDT79R3730 provides standard interfaces for the R3051 family of RISControllers™, a high-performance, flexible memory system controller, an optional coprocessor accelerator interface, controls for industry standard I/O peripherals, and a high-performance engine interface.



2906 dwg 03

Figure 3. CPU to IDT79R3730 Interface

The IDT79R3730 provides unique system flexibility by providing comprehensive programmability of the system interface functions and timing parameters. These include controls for memory configuration and device size, edge timing for DRAM and I/O peripheral control signals, and controls for the format and timing of engine interface signals. Each system interface is defined based on specific system goals for that interface. Standard IDT79R3730 feature selections assume that most printer OEMs want a low base unit price, with modular add-ons for memory, I/O and accelerators.

CPU INTERFACE

IDT79R3730 communicates with the CPU via a multiplexed address/data bus and control interface that is a pin-for-pin, glue-less match with the control signal and timing standards for IDT's R3051 RISController family, including R3041, R3051, R3052, and R3081.

A key *system* goal of IDT79R3730 is to integrate most general purpose logic to lower system cost, while preserving OEM flexibility for product differentiation through CPU and clock frequency choices, memory timing/tuning and addition of coprocessor accelerators.

A primary *performance* goal is to run the CPU bus at maximum utilization and frequency, with a minimum of stalls caused by memory system latencies or I/O device bandwidth limitations. IDT79R3730's on-chip FIFOs, arbitration logic and DMA capability allow I/O transfers to burst in and out of system memory at maximum memory system bandwidth. The CPU bus remains at minimum loading with only the CPU, IDT79R3730, an address latch, memory system buffers/transceivers and the system coprocessor (if used).

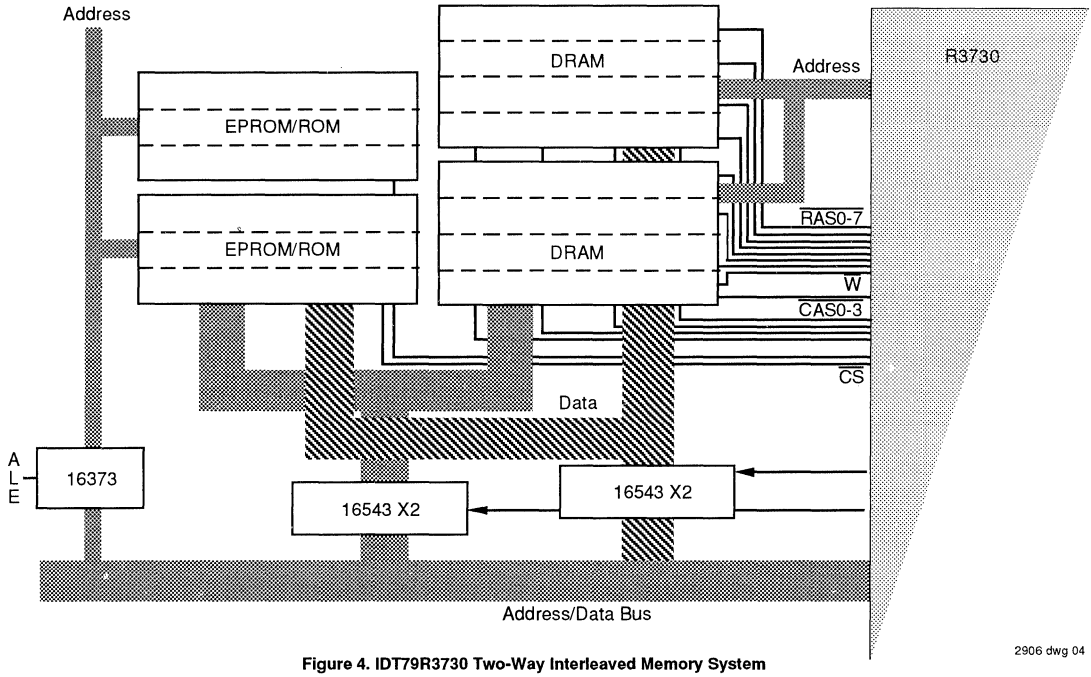


Figure 4. IDT79R3730 Two-Way Interleaved Memory System

MEMORY SYSTEM INTERFACE

The IDT79R3730 provides the controls for a wide range of DRAM and/or ROM based memory system configurations. Options range from DRAM-only systems where the interpreter and fonts are down-loaded from the host and run out of DRAM, to ROM based systems including interpreter and fonts, or systems including SCSI disc for font caching.

Controls are provided to support base-plus-extension memory organizations where the minimum DRAM configuration is installed in the board and optional memory is added by the end user (typically in SIMMs). The base and extension options can be configured with different size devices. There can be 1, 2 or 4 base memory banks, and 1 to 6 extension banks, up to a total of 8 banks of DRAM. Configuration Register controls are provided to allow the user to specify different device sizes in each area, and how much memory is addressable. The memory system can be all two-way interleaved or all non-interleaved.

The IDT79R3730 provides the $\overline{RAS}$, $\overline{CAS}$, chip select and enable controls for a wide variety of configurations. Since the target applications for IDT79R3730 typically have large amounts of memory, IDT79R3730 provides enable controls for external latches/transceivers. IDT79R3730 supports page mode accesses, early write cycles, and $\overline{CAS}$ before $\overline{RAS}$ refresh.

The IDT79R3730 Configuration Registers provide control for each of the various timing edges to allow precise memory system tuning to get the best performance at each cost point. This makes it possible to independently scale CPU performance over a wide frequency range to achieve the desired cost/performance balance. Timing resolutions down to one half the period of the CPU clock are selectable for memory system control timing via the Configuration Registers.

BOOT MEMORY CONTROL

The IDT79R3730 always starts up from a boot ROM. Therefore, IDT79R3730 provides a single 8-bit boot ROM control interface in conjunction with 8-bit data Port A. One of the IDT79R3730 Configuration Registers provides timing control for this interface. 4 MB of address space is supported. Timing from chip select to first data sampling and to next access is programmable to accommodate device timing.

PROGRAMMABLE ENGINE INTERFACE

The video data is transferred via DMA from system memory to the 8-deep by 32-bit wide video FIFO, and is then serialized for the video output(s). DMA chaining is supported for video transfers, and can be set for single line transfers, multiple line transfers, or full page transfers. The IDT79R3730 supports duplex printing.

The video interface provides one, two or four serial data streams, plus synchronization signals. Four video data streams provide lower clock rates for high-bandwidth bi-level, or 4-bit parallel output for grey scale or 4 or 8-bit continuous tone color.

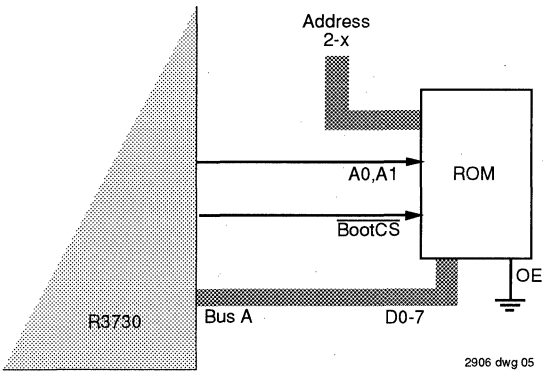


Figure 5. Boot ROM Connections

The IDT79R3730 engine interface includes VCLK, a video clock input from an external pixel clock oscillator, and SHCLK, a programmable mode shift clock output indicating when video data is valid. Inputs are also provided for LSync (line sync, or beam detect), an input from the engine indicating when to start a new scan line, and PSync (page sync), an input indicating the start of a new page.

Vertical and horizontal page margins are supported by programmable "skip counters" that allow specification of the number of vertical lines or horizontal dots to be skipped before starting to print.

A "pel" counter is provided to count the number of black dots printed. This provides a measure of toner usage.

The IDT79R3730 supports split stream video for LED page printers.

GLUE-LESS I/O CHANNELS

The IDT79R3730 supports the end-product strategy that the minimally configured product must be low-cost with modular addition of a wide range of point-to-point or network I/O options. The options must also be low-cost and as glue-less as possible, even though IDT79R3730 targets high-performance products. The IDT79R3730 provides the "intelligence" needed to obtain maximum bandwidth from low-cost standard I/O peripherals by incorporating DMA, FIFOs and packing/unpacking logic. Therefore, the I/O option strategy can take advantage of the lowest cost device options (e.g. 53C90 for SCSI, 85C30 for Appletalk, 82593 for Ethernet), rather than peripherals with higher cost because of their wide data buses or on-chip CPUs and DMA controllers.

Two independent I/O ports are provided. Port A provides channels A0 and A1 to support one or two 8-bit devices, and provides the data path for Boot ROM. Port B provides channels B0, B1 and B2 to support up to three 8 and/or 16-bit devices.

Channels A0 and B0 are associated with 16MB of address space, and are therefore, appropriate locations for font ROM (cartridge or board) addition. Ports A1, B1 and B2 are associated with 16KB of address space, and are appropriate choices for I/O peripherals.

Individual channels within I/O Ports A and B share Rd, Wr and data lines, but have individual chip select, and DMA request/acknowledge lines. Wait, Burst and the timing relationships between $\overline{Rd}/\overline{Wr}$ and $\overline{CS}/\overline{DACK}$ are programmable for each channel via the Configuration Registers. This allows customization of I/O channel control timing for each specific I/O device.

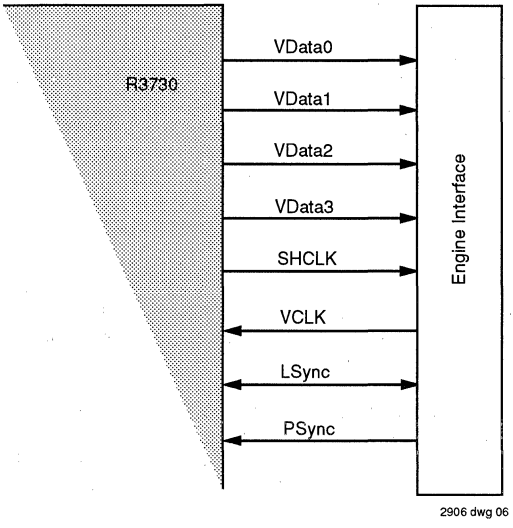


Figure 6. Engine Interface

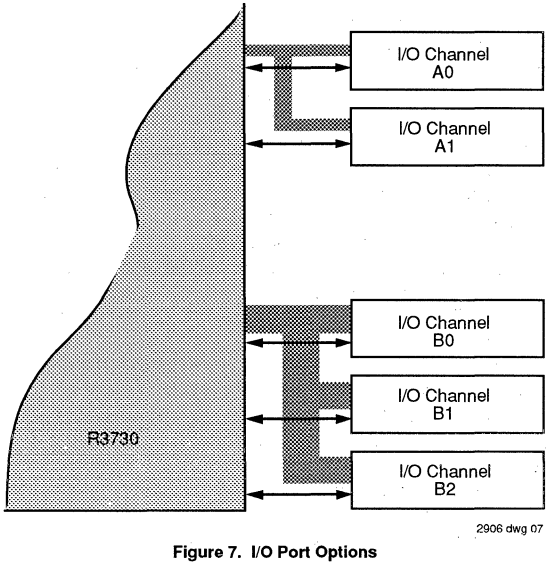


Figure 7. I/O Port Options

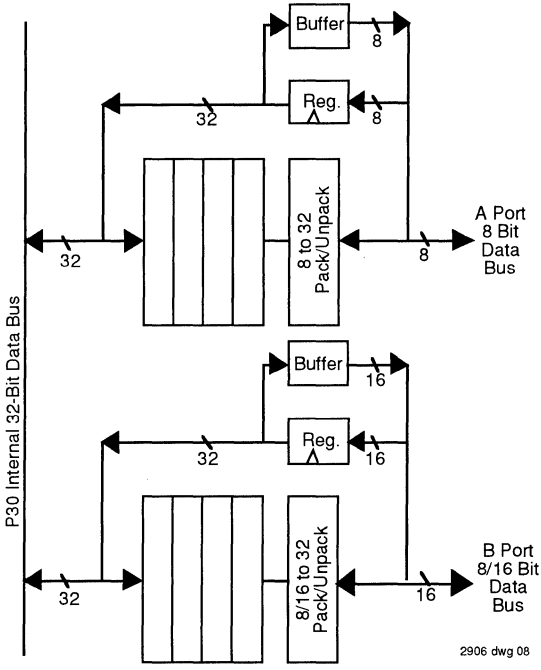


Figure 8. I/O Port Logic

Data bus A and B each have a four word deep, 32-bit wide, bi-directional FIFO, and the logic to pack and unpack bytes (and 16-bit half words for Port B) to 32-bit words (Figure 8).

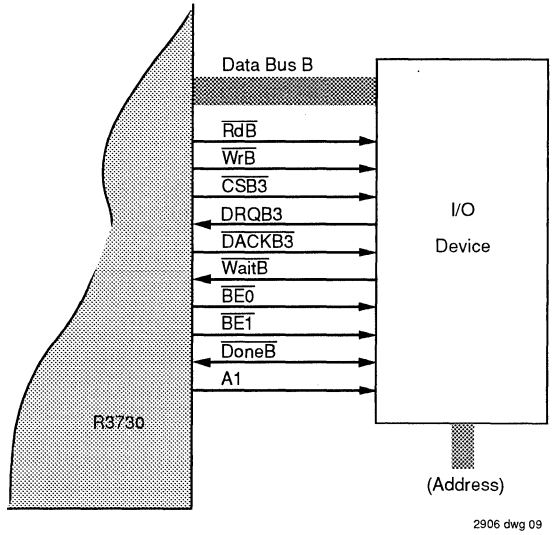


Figure 9. I/O Port B Controls

There are also bi-directional buffer/registers that bypass the FIFO, giving the CPU the capability to access different devices without ending DMA operation.

DMA BURST I/O

High speed I/O transfers, DRAM frame buffer Pattern Fill (clear), and video output data transfers are supported by eleven independent DMA channels. IDT79R3730 breaks all

6

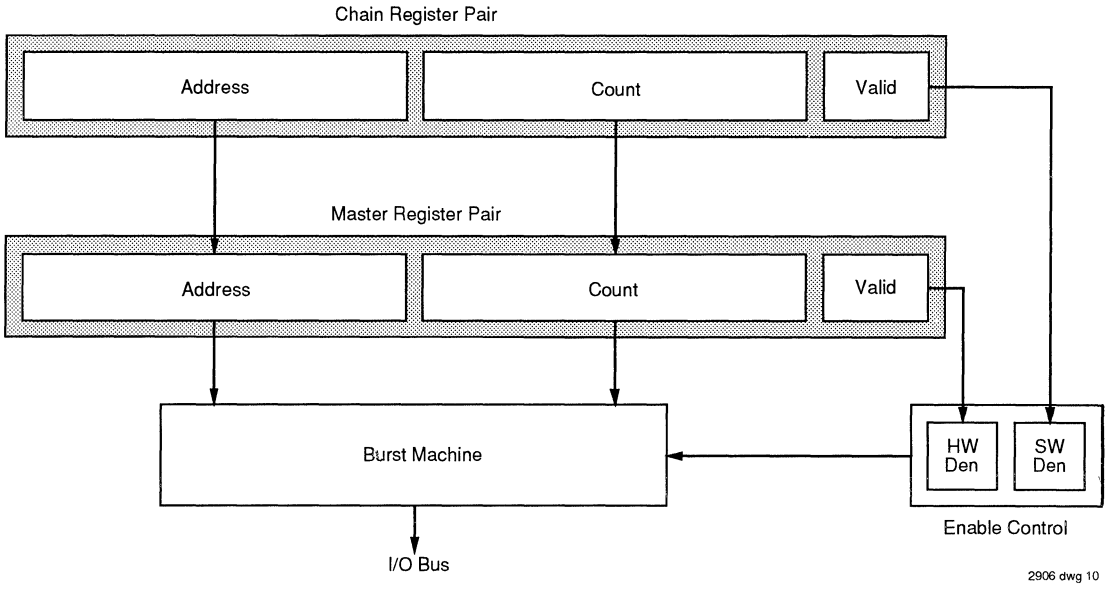


Figure 10. IDT79R3730 DMA Architecture

data transfer requests into burst transfers of 1—16 bytes. Channels A1, B2 and Pattern Fill have single Master channel register pairs. Channels A0, B0, B1 and video also have associated chaining register pairs. The data in the chaining register pair is automatically transferred to the master register pair when the master count reaches zero. The chaining register pair allows a "next" packet to immediately begin transfer without incurring the delay required to reprogram the master channel, an important feature in high-performance DMA implementations (e.g. saves memory for I/O by allowing use of smaller buffers).

Each register pair has an associated "valid" bit that indicates when the data in the count register is valid. An active-high Master valid bit indicates that the data associated with the Master address/count transfer has not completed transfer. An active-high Chain valid bit indicates that the data in the chain address/count register has not yet been transferred to the Master register pair.

Controls are provided to set a variety of priority scenarios. Channels can be assigned to different priority groups, be disabled or have round-robin priority. There are four independent DMA state machines: Port A, Port B, Video and DRAM.

COPROCESSOR SUPPORT

The IDT79R3730 provides a generic 32-bit multiplexed interface for various coprocessor configurations using a combination of CPU interface signals $\overline{Rd}$, $\overline{Wr}$ and ALE, plus coprocessor interface signals $\overline{DRQ}$, $\overline{DACK}$ and $\overline{DS}$. The coprocessor resides on the CPU's A/D bus. This provides a straighforward interface (one PAL plus data buffers) to support standard devices such as Adobe's Type 1 font rasterizer or PixelBurst display list coprocessor.

INTEGRATED INTERRUPT CONTROLLER

The IDT79R3730 contains an interrupt controller with multiple interrupt sources and programmable grouping into high or low-priority CPU interrupt inputs. There is a Configuration Register for masking individual interrupt sources, and an interrupt cause register.

TIMER/COUNTERS

A programmable 9-bit Timeout Counter and a general purpose programmable 27-bit Timer/Counter are included and incorporated into the interrupt structure.

The Timeout Counter can be used as a CPU timeout counter (counting from the start of a CPU active bus cycle to the assertion of $\overline{Ack}$), or as a DMA timeout counter (acounting from the assertion to the de-assertion of $\overline{BusGnt}$). On a CPU timeout, $\overline{BErr}$ is asserted for one cycle and an interupt is asserted. For a DMA timeout, DMA acknowledge ($\overline{Ack}$) and an interrupt will be asserted, and $\overline{BusReq}$ will be de-asserted.

The general purpose Timer/Counter can be programmed as either function. As a counter, counting will stop with the assertion of $\overline{TCnt}$ when terminal count is reached. As a timer, TCnt will be asserted and the programmed count value will be reloaded when terminal count is reached.

ROTATE ASSIST

The Rotate Assist logic performs 0°, 90°, 180° or 270° rotations and mirror rotations on a 16x16 bit array.

CONFIGURATION REGISTERS

The IDT79R3730 is configured at boot time by programming various fields in 49 internal Configuration Registers. The IDT79R3730 occupies 128KB of address space. The location of this space (the Base Address) is programmable via the Base Address register. This register's address is 1FFXXXXX.

The other registers are at the offset relative to the base address as shown in Table 1.

Offset	Register Name/Function
0000	**General Purpose Registers**
0000	R3730 base address register
0004	CPU interface
0008	CS and DRAM base address
000C	CS and External I/O base addresses
0010	Channel priority
0014	Pattern fill data
1000	**DRAM Control Configuration Registers**
1000	Size and $\overline{RAS}$ timing
1004	$\overline{CAS}$ and refresh timing
2000	**I/O Bus A Configuration Registers**
2000	Channel A0 and A1 interface timing
2004	Boot CS timing
3000	**I/O Bus B Configuration Registers**
3000	Channel B0 and B1 interface timing
3004	Channel B2 interface timing
4000	**DMA Configuration Registers**
4054	Channel A0 DMA address
4058	Channel A1 DMA address
405C	Channel B0 DMA address
4060	Channel B1 DMA address
4064	Channel B2 DMA address
4068	Channel A0 DMA chain address
406C	Channel B0 DMA chain address
4070	Channel B1 DMA chain address
4074	Channel A0 DMA count
4078	Channel A1 DMA count
407C	Channel B0 DMA count
4080	Channel B1 DMA count
4084	Channel B2 DMA count
4088	Channel A0 DMA chain count
408C	Channel B0 DMA chain count
4090	Channel B1 DMA chain count
40A0	Pattern fill address
40A4	Pattern fill count
5000	**Video Configuration Registers**
5000	Video interface
5004	Pel counter
5008	Margin widths
500C	Margin widths chain register
5010	Video buffer DMA address
5014	Video buffer DMA chain address
5018	Addressing mode and DMA count
501C	Addressing mode and DMA chain count
5020	Test mode left
5024	Test mode right
6000	**Rotate Assist Configuration Register**
7000	**System Configuration Registers**
7000	Parallel I/O mode register
7004	Parallel I/O
7008	Bus time out count
700C	General purpose timer/counter mode/count
7010	Interrupt cause register
7014	Interrupt mask register
7018	Interrupt priority register
701C	CS0, CS1 and CS2 timing and address space

Table 1. IDT79R3730 Register Address Offset

PIN DESCRIPTION

PIN NAME	I/O	DESCRIPTION
CPU Interface		
A/D(31:0)	I/O	**Address/Data:** These signals are connected directly with A/D(31:0) of the CPU. This is a 32-bit time multiplexed bus which indicates the desired address for a bus transaction in one phase, and which is used to transmit data between the CPU and system memory resources during the rest of the transfer. Transactions on this bus are logically separated into two phases: during the first address phase, information about the transfer is presented to the memory system to be captured using the ALE output. This information consists of: **Address(31:4)**: The high-order address for the transfer is presented on A/D(31:4). **$\overline{BE}$(3:0)**: These strobes indicate which bytes of the 32-bit bus will be involved in the transfer, and are presented on A/D(3:0). The use of the bus during the second data phase depends on the type of transfer. During CPU write cycles, the bus contains the data to be stored and is driven from the CPU's internal write buffer. On read cycles, the bus receives the data from the external resource, in either a single data transaction or in a burst of four words, and places it into the on-chip read buffer.
Addr(3:2)	I	**Low Address (3:2)** A 2-bit bus which indicates which word is currently expected by the processor. Specifically, this two bit bus presents either the address bits for the single word to be transferred (writes or single datum reads) or functions as a two bit counter starting at '00' for burst read operations.
ALE	I	**Address Latch Enable:** Used by the CPU to indicate that the A/D bus contains valid address information for the bus transaction. This signal is used by IDT79R3730 logic to capture the address for the transfer.
$\overline{Burst}$	I	**Burst Transfer:** On read transactions, the $\overline{Burst}$ signal indicates that the current bus read is requesting a block of four contiguous words from memory. This signal is used only in read cycles. This pin connects to the CPU's $\overline{Burst}$/WrNear
$\overline{Rd}$	I	**Read:** A CPU output which indicates that the current bus transaction is a read (single or burst).
$\overline{Wr}$	I	**Write:** A CPU output which indicates that the current bus transaction is a write.
$\overline{Ack}$	O	**Acknowledge:** An output to the CPU which indicates that the memory system has sufficiently processed the bus transaction, and that the CPU may either terminate the write cycle or process the read data from this read transfer.
$\overline{RdCEn}$	O	**Read Buffer Clock Enable:** A IDT79R3730 output which indicates to the CPU that the memory system has placed valid data on the A/D bus, and that the processor may move the data into its on-chip Read Buffer.
$\overline{SysClk}$	I	**System Reference Clock:** An input to IDT79R3730 from the CPU which reflects the timing of the processor bus interface. This clock is used as a timing reference for the system interface.
$\overline{BusReq}$	O	**DMA Arbiter Bus Request:** An output to the CPU which requests that the CPU tri-state its bus interface signals so that they may be driven by an external master.
$\overline{BusGnt}$	I	**DMA Arbiter Bus Grant.** An input to IDT79R3730 from the CPU used to acknowledge that a $\overline{BusReq}$ has been detected, and that the bus is relinquished to the external master.
$\overline{BErr}$	O	**Bus Error:** Output to the CPU bus interface unit to terminate a bus transaction due to an external bus error.
$\overline{Int}$(2:0)	O	**Processor Interrupt:** Interrupt outputs to the CPU from IDT79R3730, providing prioritized interrupt during normal operation and system configuration input during reset in conjunction with the Config(2:0) inputs.
$\overline{DataEn}$	I	**Data Enable:** This input from the CPU indicates that the A/D bus is no longer being driven by the CPU during read cycles, thereby allowing the IDT79R3730 to enable the memory system drivers onto the A/D bus without a bus conflict.

PIN NAME	I/O	DESCRIPTION
CPU Bus Interface		
$\overline{CS}$(2:0)	O	**General Purpose System Bus Chip Select:** Three Chip Select outputs associated with the 32-bit CPU high speed bus. The memory space associated with each chip select is programmable from 512KB to 4MB in non-interleaved mode, and 1MB to 8MB in interleaved mode.
IntA3	O	**Interleave A3:** This is an address output which is substituted for the latched address A3 from the A/D data bus when the ROM/EPROM memory is interleaved.
OEM/AD(Odd)	O D	**Buffer Control Output Enable:** Output Enable for the data path buffer from the memory system to the A/ bus for the odd bank in interleaved memory systems.
OEMAD(Even)	O D	**Buffer Control Output Enable:** Output Enable for the data path buffer from the memory system to the A/ bus for the even bank in interleaved memory systems.
$\overline{OEADM}$	O	**Buffer Control Output Enable:** Output Enable for the data path buffer from the A/D bus to the memory system data bus.
LEMAD	O	**Buffer Control Latch Enable:** Latch Enable for the data path from the memory system data bus to the A/D bus.
LEADM(Odd)	O	**Buffer Control Latch Enable:** Latch Enable for the data path from the A/D bus to the memory system for the odd bank in interleaved memory systems.
LEADM(Even)	O	**Buffer Control Latch Enable:** Latch Enable for the data path from the A/D bus to the memory system for the even bank in interleaved memory systems.
DRAM Interface		
DAddr(10:0)	O	**DRAM Address:** These outputs are typically connected to the DRAM multiplexed row/column address inputs. The relationship between CPU address and DRAM address is a function of DRAM size and organization.
$\overline{RAS}$(7:0)	O	**Row Address Strobe:** These outputs are directly connected to the $\overline{RAS}$ inputs of the DRAMs on a bank basis. The falling edge of $\overline{RAS}$ is used by the DRAMs to capture the row address presented on DAddr(10:0).
$\overline{CASOdd}$(3:0)	O	**Column Address Strobe:** These outputs are directly connected to the $\overline{CAS}$ inputs of the DRAMs on a byte basis. The falling edge of $\overline{CAS}$ is used by the DRAMs to capture the row address presented on DAddr(10:0). These signals are identical to $\overline{CASEven}$ in the non-interleaved mode.
$\overline{CASEven}$(3:0)	O	**Column Address Strobe:** These outputs are directly connected to the $\overline{CAS}$ inputs of the DRAMs on a byte basis. The falling edge of $\overline{CAS}$ is used by the DRAMs to capture the row address presented on DAddr(10:0). These signals are identical to $\overline{CASOdd}$ in the non-interleaved mode.
$\overline{W}$	O	**Write Enable:** This output is used by the DRAM memory system to determine if a memory access is a read or write cycle ($\overline{W}$ = LOW for a write cycle, $\overline{W}$ = HIGH for a read cycle).
Video Interface		
VCLK	I	**Video Clock Input:** An input clock from the print device running at the video dot rate.
SHCLK	O	**Shift Clock Output:** The programmable mode Shift Clock output from IDT79R3730 to the printer device indicating when Video Data output is valid.
VData(3:0)	O	**Video Data Outputs (serial):** Video Data output to the printer device, typically formatted through one bit stream from VData0, two data streams from VData0 and VData1, or four streams from all four outputs (to limit video frequency).
LSync	I/O	**Line Sync Input/Output:** Depending on the configuration of the printer/output device, LSync can be used as on output from the IDT79R3730 to the device to indicate that valid data is present. It can also be used as an input to IDT79R3730 to begin transfer of the next line of video.
PSync	I	**Page Sync Input:** This is an input to IDT79R3730 from the output device to begin transfer of the next page.

PIN NAME	I/O	DESCRIPTION
I/O Port A		
DataA(7:0)	I/O	**Port A Data Bus:** Bidirectional 8-bit data bus for Port A, for channels A0, A1, and Boot ROM during startup.
$\overline{\text{RdA}}$	O	**Port A Read:** An IDT79R3730 output which indicates that the current port A bus transaction is a read from the peripheral/channel selected.
$\overline{\text{WrA}}$	O	**Port A Write:** An IDT79R3730 output which indicates that the current port A bus transaction is a write to the peripheral/channel selected.
$\overline{\text{CSA}}$(1:0)	O	**Port A Chip Selects:** IDT79R3730 Chip Select outputs for channels A1 and A0.
DRQA(1:0)	I	**Port A DMA Request:** IDT79R3730 inputs for channels A1 and A0 requesting DMA service for the respective peripheral/channel.
$\overline{\text{DACKA}}$(1:0)	O	**Port A DMA Acknowledge:** IDT79R3730 outputs for channels A1 and A0 indicating that DMA service requested by a respective peripheral/channel is acknowledged and that bus access is granted.
$\overline{\text{WaitA}}$	I	**Port A Wait Request:** An input from a Port A device that indicates that a transfer cycle needs to be extended. An active Wait input will halt the state machine control for port A.
$\overline{\text{DoneA}}$	I/O	**Port A Done:** An open collector pin that goes low to indicate the end of a DMA cycle, or can be driven low to terminate the current DMA cycle for an A channel.
BootAddr(1:0)	O	**Boot Address (Port A):** These outputs supply the byte address in conjunction with the word address latched from the A/D bus for the a byte wide boot ROM/EPROM using the A port data bus.
$\overline{\text{BootCS}}$	O	**Port A Boot ROM Chip Select:** Chip Select for the Boot ROM device during startup.
I/O Port B		
DataB(15:0)	I/O	**Port B Data Bus:** Bidirectional 8/16-bit data bus for Port B channels B0, B1 and B2.
$\overline{\text{RdB}}$	O	**Port B Read:** A IDT79R3730 output which indicates that the current port B bus transaction is a read from the peripheral/channel selected.
$\overline{\text{WrB}}$	O	**Port B Write:** A IDT79R3730 output which indicates that the current port B bus transaction is a write from the peripheral/channel selected.
$\overline{\text{CSB}}$(2:0)	O	**Port B Chip Selects:** IDT79R3730 Chip Select outputs for channels B0, B1 and B2.
DRQB(2:0)	I	**Port B DMA Request:** IDT79R3730 inputs for channels B0, B1 and B2 requesting DMA service for the respective peripheral/channel.
$\overline{\text{DACKB}}$(2:0)	O	**Port B DMA Acknowledge:** IDT79R3730 outputs for channels B0, B1 and B2 indicating that DMA service requested by a respective peripheral/channel is acknowledged and that bus access is granted.
$\overline{\text{WaitB}}$	I	**Port B Wait Request:** An input from a Port B device that indicates that a transfer cycle needs to be extended. An active Wait input will halt the state machine control for port B.
$\overline{\text{DoneB}}$	I/O	**Port B:** An open collector pin that goes low to indicate the end of a DMA cycle, or can be driven low to terminate the current DMA cycle for a B channel.
$\overline{\text{BE}}$(1:0)	O	**Port B Byte Enables:** The Byte Enables indicate which byte is valid for 16-bit peripherals.
A1	O	**Port B Half-Word Select:** This output provides address A1 for 16-bit devices and indicates how 16-bit data input to Port B is interpreted on a half-word basis.

PIN NAME	I/O	DESCRIPTION
System Interface		
Config(0)	I	**Configuration Input 0:** Config(0) is an IDT79R3730 input wired high or low to set the Big/Little endian format during Reset for the A/D bus within IDT79R3730. During Reset, Config(0) also controls the state of Int0, which is connected to CPU Int0 to set the endian format of the CPU. After completion of the reset cycle, Int0 resumes its normal function as an asynchronous, maskable, interrupt input to the CPU.
Config(1)	I	**Configuration Input 1:** Config(1) is an IDT79R3730 input wired high or low to set the state of output Int1 during Reset, and therefore,the state of the CPU input Int1 is connected to. After completion of the reset cycle, Int1 resumes its normal function as an asynchronous maskable interrupt input to the CPU.
Config(2)	I	**Configuration Input 2:** Config(2) is an IDT79R3730 input used in conjunction with the Test input. During IDT79R3730 Reset, if Test is set low, Config(2) is a IDT79R3730 input wired to set the state of Int1. If Test is set high during IDT79R3730 Reset, a Config(2) high input will cause IDT79R3730 to be reset with all IDT79R3730 outputs three-stated for board testing. If Test is set high during IDT79R3730 Reset, a Config(2) low input will cause IDT79R3730 to be reset in a mode used only for factory test.
DRQ	I	**Coprocessor DMA Request:** An IDT79R3730 input to request DMA service for the coprocessor interface, using the A/D data bus.
DACK	O	**Coprocessor DMA Acknowledge:** An IDT79R3730 output indicating that DMA service for the coprocessor interface is acknowledged and that bus access is granted.
DS	I	**Data Strobe:** This input indicates to the IDT79R3730 when data on the A/D bus is valid.
PIO(11:0)	I/O	**Programmable I/O:** The PIO pins provide three general purpose functions: programmable bit-level I/O, maskable interrupt input, or parity generation/checking between the IDT79R3730 and DRAM. Each pin can be programmed to be an input or an output. Their function is set by programming individual bits/fields in the appropriate Confuguration Registers. PIO(11:0) are sub-divided into three 4-bit fields. Two Configuration Register bits determine if fields PIO(3:0) and PIO(7:4) are to function as I/O bits or as parity fields for DRAM. If they are to be used for parity, PIO(3:0) provides parity bits for the even bank (interleaved) and PIO(7:4) provides parity for the odd bank.
		If PIO bits are used as I/O, additional Confuguration Register bits determine if individual PIO bits are to be used for input or output. In the input mode, a low level input will be interpreted as a maskable interrupt, readable from the cause register.
Reset	I	**Reset IDT79R3730:** This input resets the IDT79R3730.
TCnt	O	**Terminal Count:** This output indicates that the timer/counter has decremented to zero.
Test	I	**Test Mode Input:** Used in conjunction with Config(2) to three-state IDT79R3730 outputs for board test. See Config(2) description.

Integrated Device Technology, Inc.

256KB/ 1MB/ 4MB IDT79R4000 SECONDARY CACHE MODULE BLOCK FAMILY

PRELIMINARY
IDT7MP6074
IDT7MP6084
IDT7MP6094

FEATURES:

- High-speed BiCMOS/CMOS secondary cache module block constructed to support the IDT79R4000 CPU
- Available as a pin compatible family to build 256KB (unified), 1MB (unified) and 4MB (unified or split) secondary caches
- Zero wait-state operation
- Four-word line size
- Operating frequencies to support 50MHz and 75MHz IDT79R4000
- Available as a set of four identical high-density 80-lead (gold-plated fingers) SIMMs (Single In-Line Memory Modules)
- Surface mounted plastic components on a multilayer epoxy laminate (FR-4) substrate
- Multiple ground pins and decoupling capacitors for maximum noise immunity
- TTL compatible I/Os
- Single 5V (±10%) power supply

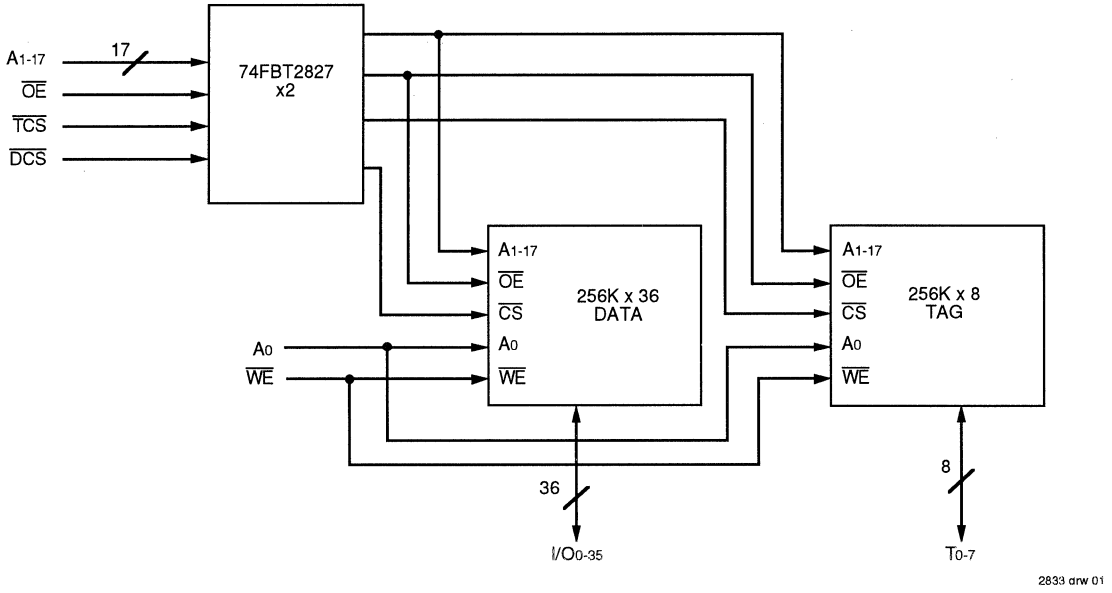
DESCRIPTION:

The IDT7MP6074 is a 256KB IDT79R4000 secondary cache module block constructed on a multilayer epoxy laminate substrate (FR-4), using eleven 16K x 4 SRAMs and two IDT74FBT2827 drivers. The IDT7MP6084 is a 1MB IDT79R4000 secondary cache module block using eleven 64K x 4 SRAMs, and the IDT7MP6094 is a 4MB IDT79R4000 secondary cache module block using eleven 256K x 4 static RAMs. The IDT74FBT2827 has internal 25W series resistors and BiCMOS I/Os resulting in the fastest propagation times with minimal overshoot and ringing. Four identical cache module blocks comprise a full secondary cache.

The IDT7MP6074/84/94 support use in an IDT79R4000-based system at speeds of 50MHz and 75MHz with zero wait-state operation. These modules support a four word line size. For other line sizes, please consult factory.

All inputs and outputs of the IDT7MP6074/84/94 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refresh for operation.

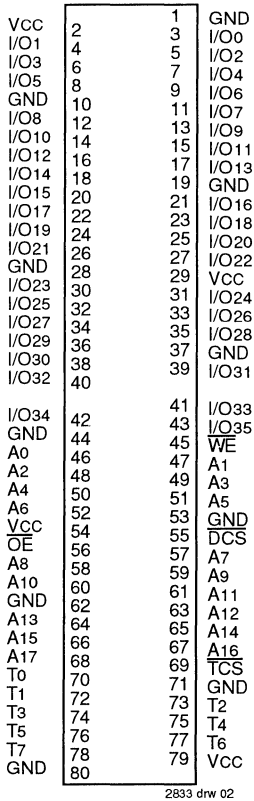
FUNCTIONAL BLOCK DIAGRAM



2833 drw 01

The IDT logo is a registered trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



2833 drw 02

SIMM
TOP VIEW

PIN NAMES

I/O_{0-35}	Data Inputs/Outputs
T_{0-7}	Tag Inputs/Outputs
A_{0-17}	Address Inputs
$\overline{DCS}$	Data Chip Select
$\overline{TCS}$	Tag Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
GND	Ground

2833 tbl 02

CAPACITANCE

Symbol	Parameter[1]	Conditions	Max.	Unit
$C_{IN(D)}$	Input Capacitance (Data)	V_{IN} = 0V	10	pF
$C_{IN(A)}$	Input Capacitance (A_{1-15}, $\overline{OE}$, $\overline{TCS}$, $\overline{DCS}$)	V_{IN} = 0V	10	pF
$C_{IN(B)}$	Input Capacitance (A_0, $\overline{WE}$)	V_{IN} = 0V	100	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	10	pF

NOTE: 2833 tbl 03
1. This parameter is guaranteed by design, but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 2833 tbl 04
1. VIL = –1.5V for pulse width less than 10ns.

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating[1]	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 2833 tbl 05
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5V ± 10%

2833 tbl 01

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI1}\|$	Input Leakage (except A_0, $\overline{WE}$)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LI2}\|$	Input Leakage (A_0, $\overline{WE}$)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	110	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
I_{CC}	Operating Current	$\overline{CS}$ = V_{IL}; V_{CC} = Max., Outputs Open	—	2200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4mA	2.4	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V

2833 tbl 06

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 - 4

2833 tbl 07

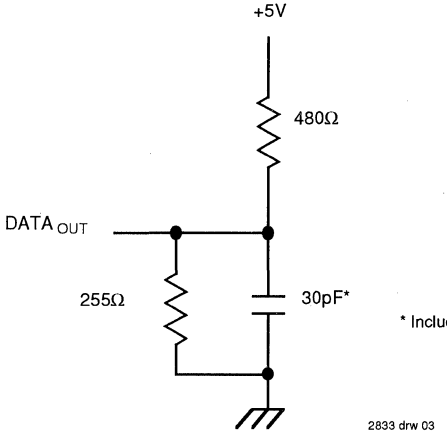


Figure 1. Output Load

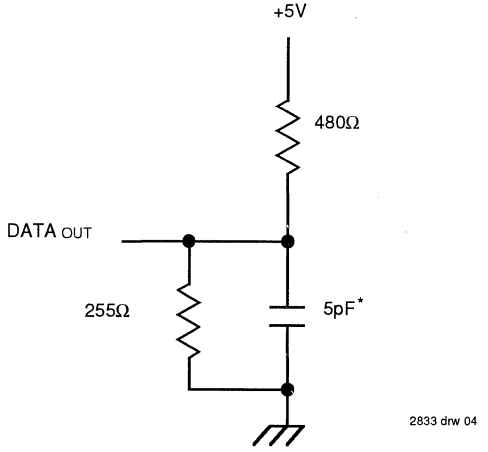


Figure 2. Output Load (for t_{OLZ} and t_{OHZ})

* Including scope and jig.

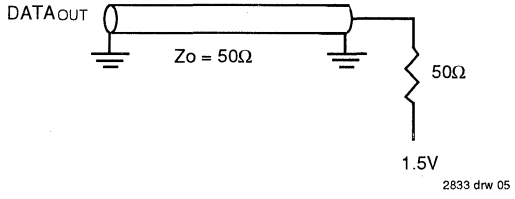


Figure 3. Alternate Output Load

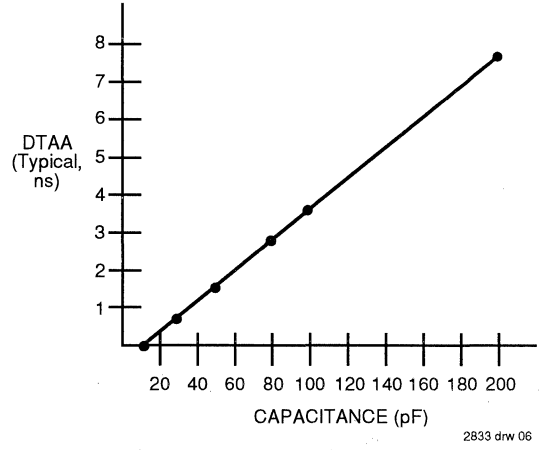


Figure 4. Alternate Lumped Capacitive Load, Typical Derating

AC ELECTRICAL CHARACTERISTICS

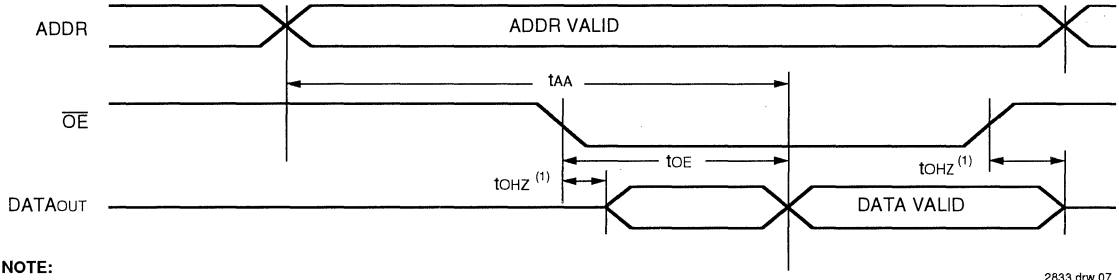
(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MP6074/6084/6094SxxM												Unit
		-12		-15		-17		-20		-25		-30		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE														
t_{AA}	Address Access Time	—	12	—	15	—	17	—	20	—	25	—	30	ns
t_{A0A}	A_0 Access Time	—	10	—	12	—	14	—	16	—	21	—	26	ns
t_{OE}	Output Enable to Output Valid	—	12	—	15	—	17	—	20	—	25	—	30	ns
t_{OHZ}(1)	Output Disable to Output in High-Z	—	10	—	12	—	13	—	15	—	17	—	20	ns
t_{OLZ}(1)	Output Enable to Output in Low-Z	2	—	2	—	2	—	2	—	2	—	2	—	ns
WRITE CYCLE														
t_{AW}	Address Valid to End-of-Write	12	—	15	—	17	—	20	—	25	—	30	—	ns
t_{A0W}	A_0 Valid to End-of-Write	10	—	12	—	14	—	16	—	21	—	26	—	ns
t_{WP}	Write Pulse Width	7	—	10	—	12	—	15	—	20	—	25	—	ns
t_{DW}	Data Valid to End-of-Write	7	—	10	—	12	—	15	—	20	—	25	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design but not tested.

2833 tbl 08

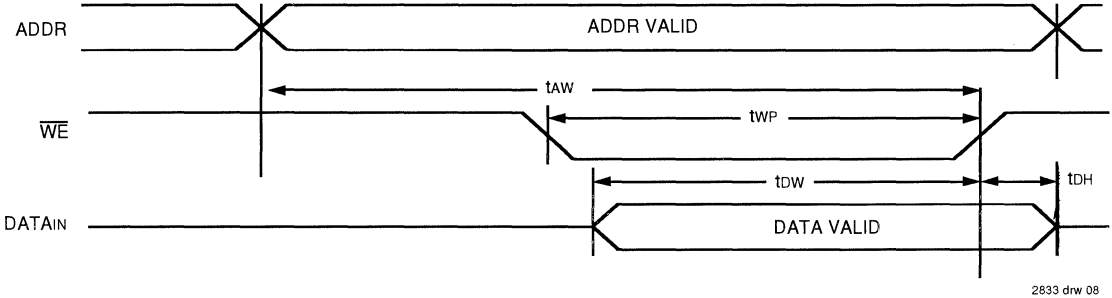
TIMING WAVEFORM OF READ CYCLE(1)



NOTE:
1. This parameter is guaranteed by design, but not tested.

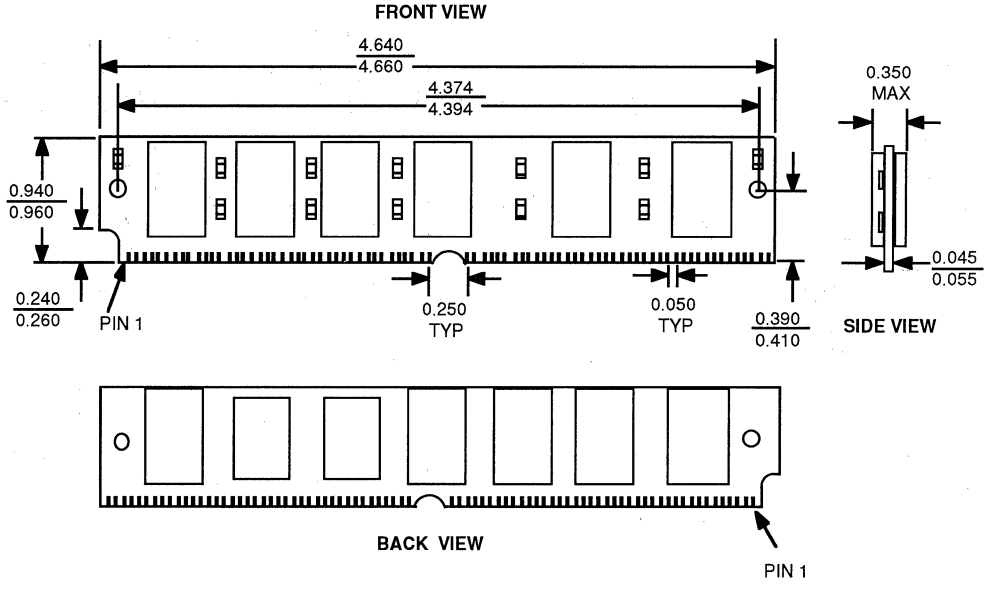
2833 drw 07

TIMING WAVEFORM OF WRITE CYCLE



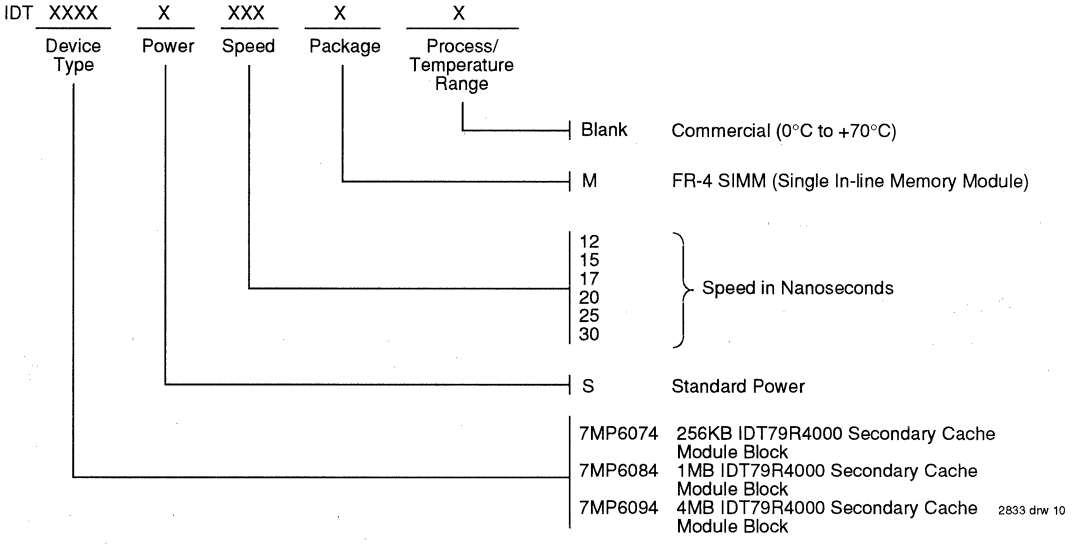
2833 drw 08

PACKAGE DIMENSIONS



2833 drw 09

ORDERING INFORMATION



2833 drw 10

Integrated Device Technology, Inc.

RISC DEVELOPMENT SUPPORT PRODUCTS

INTRODUCTION

For engineers developing software and hardware products around the IDT79R3000 Instruction Set Architecture (ISA), which includes the IDT79R3000, IDT79R3001, and IDT79R3051 family of RISControllers, IDT offers three software products, several prototyping and evaluation systems, and two versions of its MacStation bundled with IDT's software development tools. IDT is also an authorized reseller of MIPS workstations and software and has a close working relationship with many third parties who also provide support tools for this processor family. This catalog primarily focuses on products manufactured and sold directly by Integrated Device Technology.

SOFTWARE PRODUCTS

IDT/c—IDT's optimizing ANSI C-compiler. This compiler, which uses the Gnu C front end, includes full ANSI C compatibility and highly efficient floating point emulation libraries for IDT79R3051-based systems (without hardware floating point). A unique debug control scripting language makes it easy to locate hardware problems that occur only under rare conditions. IDT/c includes the compiler, optimizer, assembler, linker, librarian, C libraries, Floating Point Libraries, and symbolic debugger.

IDT/sim—IDT/sim is IDT's System Integration Manager, used to bring up new hardware and to support the symbolic debug in both the MIPS and IDT C compilers. IDT/sim is a ROMable debug kernal with extensive diagnostics built-in. It is supplied in EPROM on all IDT prototyping boards, and is available in source code for use with either the MIPS or IDT C Compilers.

IDT/kit—IDT/kit is our newest software development product: The Kernel Integration ToolKit. It contains source code and compiled versions of a complete set of routines for initializing systems, servicing interrupts, handling floating point exceptions, and so forth. Also included is source code for ANSI libraries, for the Floating Point Emulation Libraries and for transcendental functions.

PROTOTYPING SYSTEMS

Completely assembled and tested hardware systems are available for prototyping and initial software porting. All include a CPU, serial I/O, EPROM containing the IDT/sim monitor, and some amount of RAM. All have provision for simple addition of user-defined hardware. Units are available with the 3051/2 CPU, with the IDT79R3000 and IDT79R3010, and with high-performance CPU modules containing the IDT79R3000/R3010 and up to 256 KB each of I- and D- cache.

For laser printer controllers, the IDT79S389 Reference Platform provides a ready prototyping target for R3051 Family laser printer controllers using PostScript™ Level 2 software from Adobe.

MacStation DEVELOPER SYSTEMS

The MacStation Developer Systems include an IDT79R3000-based CPU card, a Macintosh II computer, a 19" monochrome monitor, the Apple extended keyboard, the complete Unix software package (MIPS RISC/os with NFS and X), and an external hard disk large enough for the Unix file systems. The Developer Systems include all three of the software tools listed above. IDT is an authorized Apple VAR for these systems.

CUSTOM DEVELOPMENT PROGRAMS

IDT can design and manufacture your R3000 based product for you. We manufacture very high performance CPU modules for a number of IDT79R3000 users, including Pyramid Technology and AT&T. These modules are designed according to your needs and are manufactured on 8 to 10 layer FR-4 boards using surface mount components on both sides of the board for the tightest possible layouts. We have built thousands of these modules at speeds of 33MHz and higher.

We have also designed and manufactured IDT79R3000 and IDT79R3051 board level products for lower performance, more cost-sensitive applications such as laser printers.

In addition to our extensive design and layout experience with IDT79R3000 based products, IDT has a great deal of experience in indentifying problems as new software is brought up on in new hardware. This skill helps us bring up new systems very quickly. In production test, we use software routines that have been developed over several years of volume manufacturing experience to ensure that products operate reliably under worst-case conditions.

THIRD PARTY DEVELOPMENT TOOLS

The increasing popularity of IDT's RISController family has resulted in a dramatic increase in the number of third party tools available. For information on these products, contact your local IDT sales representative.

- Real-Time Operating Systems from Lynx, Ready Systems, and Wind River
- Compilers from MIPS, Green Hills, and BSO Tasking
- VME Boards from CES, RISQ Modular Systems, Omnibyte, and Sanders Associates
- Device Simulation Models from LMSI, Zycad and HDL Systems
- Peripheral Support Circuits from V3 and National Semiconductor
- Page Description Language interpreters from Peerless and Adobe Systems
- In-Circuit Emulators from Embedded Performance, Inc.
- Logic Analyzer support from Hewlett-Packard, Fluke Instruments, and Tektronix

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Integrated Device Technology, Inc.

THIRD-PARTY DEVELOPMENT TOOLS AND APPLICATIONS SOFTWARE FOR IDT RISC PROCESSORS

OVERVIEW

The MIPS/IDT RISC Microprocessor family is supported by a wide variety of third-party development tools and applications software. Many of these tools are software products, useful across the entire line of processors; others of these are hardware development tools, appropriate for one or two members fo the family.

As the MIPS architecture is increasingly popular and successful, many new tools are constantly being announced. IDT encourages our customers to work closely with their local sales representative for a current list of third party support. This listing is intended to be reasonably current as of the data of this document.

Type	Vendor	Product Name	Phone
Logic Analyzer			
	Arium	ML4400	(714) 978-9531
			(800) 862-7486
	Biomation	CLAS4000	(800) 538-9320
			(408) 988-6800
	Hewlett Packard	Support thru Corelis For HP16500 / 1650	(310) 926-6727
	Fluke	PM3580	(800) 44-FLUKE
	Tektronix	DAS9200	(800) 426-2200
			(503) 627-7111
In-Circuit Emulator			
	Embedded Performance		(408) 980-8833
Simulation Models			
	Mentor Graphics	HML	(800) 547-7390
	VIEWlogic		(508) 480-0881
	HDL Systems	Verilog	(408) 432-3209
	Protocol	Model Bank	(201) 347-7900
Ada Development on Vax host			
	DDC I		(212) 696-3700
	Telesoft		(619) 457-2700
	Alsys		(617) 270-0030
	Verdix		(800) 289-8237
VME Board			
	RISQ Modular Systems		(415) 490-0732
	Lockheed Sanders, Inc.		(603) 885-6022
	Omnibyte		(708) 231-6880
	Heurikon		(608) 831-0900
	Aeon		(505) 828-9120
Real-time Operating Systems			
	JMI	C-EXECUTIVE™	(215) 628-0846
	Lynx OS	Lynx™	(408) 354-7770
	Wind River Sys.	VxWorks™	(415) 748-4100
	Accelerated Tech.	Nuecleus	(205) 661-5770
	Ready Systems	VRTX	(800) 228-1249

Type	Vendor	Product Name	Phone
Laser Printer Languages			
	Adobe Systems	Postscript™ PDL	(415) 961-4400
	Microsoft	TrueImage™	(206) 882-8080
	Peerless Group	PeerlessPage™ OS	(213) 536 0908
Compiler Products			
	BSO Tasking		(617) 320-9400
	Greenhills		(805) 965-6044
Support Peripherals			
	V3 Corporation	DRAM/DMA Controller	(416) 285-9188
	Chips & Technologies	RPC	(408) 434-0600
UNIX Support			
	UniSoft	SVR4	(510) 420-6400
FDDI Support			
	XLNT Designs Inc.	Plug-n-Play	(619) 487-9320

Integrated Device Technology, Inc.

IDT/MIPS DEVELOPMENT TOOLS: SYSTEMS AND SOFTWARE

PRODUCT OVERVIEW

FEATURES

- Based on Very High Performance MIPS® RISC Technology
- Binary compatibility across the complete line of MIPS RISComputers™, RISCstations™ and the IDT MacStation™ family
- Native Development Environment for MIPS ISA CPUs
- RISC/os™ MIPS SVID compliant UNIX® operating system with System V and BSD converged
- World class optimizing compilers including C, Pascal, ADA, PL/1, FORTRAN, COBOL
- Networking standards such as TCP/IP and NFS™ for connections to SUN, DEC, and other equipment
- X-Terminal support via RISCwindows™
- Source level symbolic debugging
- Supports a wide range of development tools
  - — System Programmer's Package
  - — IDT/c including floating point emulation
  - — IDT System Integration Manager
  - — System modeling tools for performance projections
- MIPS native host platforms include:
  - — IDT MacStation
  - — Desktop units
  - — Deskside units
  - — Departmental servers
  - — R3000 or R4000 based systems
- Cross development platforms include:
  - — Sun-4
  - — DEC Vax

DESCRIPTION

This data sheet contains an overview of some of the tools and support available when developing microprocessor based systems using the MIPS development host platforms. These systems provide an easy-to-use, robust environment for the hardware and software development of today's high-performance RISC based systems, and greatly reduce the time and effort required to bring an application to market.

As in any development environment, ongoing enhancements are made to enrich the tool set. Detailed information on current products and enhancements, new tools, and third-party support products is available from your local IDT sales representative.

MIPS DEVELOPMENT SYSTEMS CHARACTERISTICS

MIPS' Development Systems, available from IDT, provide a large tool box when developing software and designing hardware architectures for any of the MIPS ISA CPUs. Based on the UNIX operating system, RISC/os is SVID compliant, converging BSD and System V. Because RISC/os is a multiuser, multi-tasking operating system, many users can be active on the host at the same time and each user may initiate multiple tasks. These include simple multi-tasking capabilities from print spooling —the ability to queue listings to print while still compiling or editing—to more than 200 users all compiling, editing, linking, etc.

User protection indigenous to UNIX, easily managed by the System Administrator, is a huge asset in developing, testing and maintaining systems software. Configuration Management, the job of software management, is much easier with these user isolation capabilities. For example, each user can belong to a group which is developing a certain section of the project. As a user builds and tests a subprogram, he submits that tested unit to Configuration Management for archive. The librarian can give other users access, but they cannot modify the code. This enforces coding rules as code is reviewed before it is accepted. The style may seem restrictive, but has many benefits: it ensures reliable code in the library, enforces testing procedures, and keeps code stable.

Many features of standard UNIX operating systems ease the burden of program development. VI, the screen editor, (instead of a line editor), is a simple and powerful text editor that can be used for program entry. It has all the standard text editor features, plus an array of advanced capabilities for the experienced programmer. Saving and backing up important files is easily achieved by use of the TAR command. TAR, used for streaming tape backup, lists directories on tapes, can extract files from tapes, compare them, and manipulate them easily. Lastly, the Makefile command helps compile and link many subprograms easily. It is a simple list of all the files you need to compile and then link together. If during the debug process one subprogram is modified, invoking Makefile will find the single subprogram that has to be compiled again (by time/date stamps) and then relink automatically.

The CPU bandwidth required to be efficient at doing multitasking is well beyond the capability of today's medium range PC or Macintosh computers. Many advances in personal computer technology have stretched these single user architectures into multiuser domains, but to reduce the latency when adapting these systems requires more raw MIPS. These MIPS development hosts are thus ideal for the medium to large scale development team required for today's high-performance RISC-based applications.

7

CONNECTIVITY

The MIPS Development Platforms have been designed to easily integrate into existing computer environments. In most cases, these platforms easily integrate and allow the users to access the system through their existing terminals, create source files with existing terminals for download, compile and link, or more extensively use the systems file and printer resources. Solutions to a wide variety of integration goals and computing environments are readily available as parts of the MIPS Development platforms.

RS-232 Connections

The simplest method to interface to the MIPS Development Platform is to attach RS-232 terminals directly. There are typically a number of direct connections, including Comm 0 for the system console (where the system is booted and system administration functions are often performed). These terminal ports allow a number of different RS-232 devices to be connected to the host system, including IBM compatible PCs running terminal emulation software or modem connections for telephone dial-up. BAUD rates, parity, and other communication protocol information are easily configured.

Network Connections and X-Terminals

MIPS development systems are capable of integrating into all common computer networks, including Ethernet and DECnet. If the current environment includes thick or thin wire Ethernet the connection is simple, since MIPS systems support NFS-Network File System. NFS handles file transfers across a network, making all of the file resources of the network appear as if they belong in each system on the network. Since TCP/IP runs on the system, Ethernet file transfer and file sharing is transparent. This allows MIPS systems to easily connect to DECstations, Sun workstations, and any other Ethernet system using these conventions. Using Ethernet, X Terminal support is provided by RISCwindows™. This is a MIPS native implementation of the standard X Window System™ combined with OSF Motif™. Alternately, the RISComm software package can be used to integrate the MIPS host into the DECnet computer network.

PC Compatible Connections

IBM PCs or compatibles can be connected directly through RS-232 or Ethernet. For RS-232 connections, a simple terminal emulator like Procomm Plus works well. The programmer can create source code using DOS applications and then transfer it to the MIPS platform using the Kermit protocol inside of Procomm Plus. Alternatively, the programmer can share files in the PC and the system by using products from Novell. They provide a software tool that runs in both systems allowing the user to compile files that exist on the PC, or run application programs on the PC and use the file system on the MIPS platform transparently. Finally, IDT has produced a cross-compiler, including remote symbolic debug, for direct use on a PC platform.

Macintosh

Several solutions are available to utilize existing Macintosh equipment. uShare™ provides a communication network between the Apple Macintosh and MIPS platforms. Once in place, it provides Mac users with server capabilities, electronic mail, print spooling, data backup, and terminal emulation allowing interactive work. This environment allows programmers to create code on the Mac using standard word processing applications, then transfer the file to the MIPS platform for compile and test. Caymen makes The Gator Box, which provides a gateway or bridge from Apple-Talk to the MIPS platform. Disk sharing and file sharing are capable with this tool as well.

MIPS OPTIMIZING COMPILERS

A very important aspect of performance and development ease is the compiler technology. Fortunately, this is a fundamental strength of MIPS.

The MIPS instruction set and compiler technology were codeveloped before any silicon was architected. Many years were expended developing, tuning, and testing the instruction set and the ability of compiler technology to generate efficient object code from high-level languages. After this rigorous analysis, the silicon trade-offs were made. The result is a chip and compiler toolset designed to work with each other; this is dramatically different from traditional CPU/compiler development, where a chip manufacturer designs a chip and then expects compiler writers to "do their best with it".

MIPS optimizing compiler technology, widely regarded as the best in the industry, is based on mathematical models that work 100% of the time. This is substantially better than the "portable compiler" technology used for many other processors, which frequently uses heuristic rules for optimization that may not result in as robust operation. Today, five levels of compiler optimization are available. Each individual level further optimizes code size or execution speed. Local optimizations include: Optimal Calling Sequences, Branch to Branch Optimizations, Local Common Subexpression, Schedule FP Units, Pipeline Scheduling, Constant Folding, and Code Selection. Global optimizations, which optimize across procedure boundaries include: Moving invariant code out of loops, Strength Reduction, Register Assignment, Global Common Subexpression, Shrinkwrapping, Inter-procedural Register Allocation, and Procedure Inlining.

The structure of the MIPS compilers exemplifies "State of the Art" design; the compiler suite is designed to use a common optimizing structure, called the back end, and multiple language parsers or front ends. This foundation yields many benefits: improvement in the back end improves all languages, and more front ends (languages) can be easily added at any time and obtain the full benefit of MIPS optimizations. Also, the structure allows combinations of languages, including assembly, to be incorporated in a single program. MIPS compiler suite includes C, FORTRAN, Pascal, ADA, COBOL, PL/1, assembly. Languages from third party vendors are available as well.

MIPS C cross compiler is also available for the Sun-4 and DEC VAX environments, allowing this state of the art optimizing compiler to be brought to a cross-development environment.

TOOLS FOR DEVELOPMENT

MIPS development hosts include support for both hardware planning, software development, and software integration. These tools allow application architects to define a system capable of meeting the cost/performance goals of the application, allow the software to be developed quickly and efficiently, and ease the process of integration of the application software onto the final target system.

Many of these tools are now available in either source or binary form, and have been re-hosted to the Sun-4 and DEC VAX environments. In addition, these tools are available in versions to support either R3000 (including IDT R3051 family) or R4000-based CPU development.

Hardware Architecture Evaluation

The quality of an application system is determined by its ability to meet the needs of its marketplace. Good systems are well planned, well thought out, well designed, and are maintainable. Tools for hardware architecture definition help measure how close the final system will actually come to meeting the systems' predefined goal, before time and money are spent on developing prototypes. MIPS tools include the ability to accurately gauge the performance of application software on a given memory architecture, and allow the hardware architect to make cost performance trade-offs in the target system even before schematics are fully developed. These tools are contained in a product called the System Programmer's Package—SPP, and complement many of the software development tools discussed below. For example, Sable, a symbolic debugger/instruction simulator can be used to profile and develop kernel code. Pixie, Pixstats, and Profiler work to provide detailed information about the dynamic behavior of the software in the proposed system including information about cache performance, "hot spots" and dead spots in the code, and the dynamic instruction mix used by that software.

DBX Source-Level Debugger

This standard debugger for UNIX is excellent for testing and finding software problems at the source code level. The debugger works for C, FORTRAN, Pascal, and assembly language. DBX is an easy tool to use; simply compile your code with the -g option (this keeps the symbol table from being stripped) and then invoke the debugger by typing "DBX command_file_name source_file_name". The command_file_name allows a set of DBX commands to run for set up, like setting variables, setting breakpoints, running to a specific point and displaying variables. Simple commands for DBX are: RUN, LIST, DUMP (list data about current procedure), STEP, STOP AT line#, STOP IN procedure_name, UP/DOWN (traverse stack activation levels), etc. Complex commands like "stop VAR in PROCEDURE if EXPRESSION" are also supported. DBX lets you use all the resources within the language except coprocessor zero, which can be debugged using "Sable".

Both the SPP and the IDT System Integration Manager allow the capabilities of DBX to be brought to source level debugging on a remote target system. This provides a familiar environment to the programmer as the task of integrating application software onto the target system is performed.

Program Behavior Analysis Tools

Pixie is a UNIX program that provides statistics about a program's dynamic behavior. One type of data collected shows all the called routines, how many times they were called, how many instructions per call, and the percent of time spent in that call. This information is used to find out where most of the program time is spent, allowing the programmer to focus on those routines which dramatically affect the performance of the application. Another type of data collected shows the locality of the code. This helps to predetermine how much cache would be appropriate for this program. It also goes into detail on floating point usage, integer multiply/divide usage, all possible interlocks, load/branch nops, and more. For it to collect this type of data, it actually instruments your object code; the instrumented code is executed normally, and the output is formatted using the pixstats (pixie statistics) program.

The Profiler is another UNIX tool that further defines code behavior. The user can concentrate in specific areas of program behavior by focusing the profilers attention to those items. Separate lists can be generated covering procedure information. They are: sorted by total time spent in each procedure, sorted by times called, sorted by number of cycles executed, sorted by number of clocks executed, sorted by number of clocks per line inside a procedure, and number of procedures never called. Again, this tool set allows the programmer to tune those areas of the code which will most affect the end system performance, thus increasing programmer efficiency.

The System Programmer's Package

SPP is a toolbox containing programs that help system developers to build, test, and download software to the target hardware. Among the utilities included in the SPP are the following:

- A hardware environment simulator which allows the system architect to evaluate the performance of different types of memory systems
- A software environment simulator which allows symbolic kernel code debug
- A set of tools for downloading into the target machine, and interfacing to DBX to perform remote target source level debugging.
- Common I/O routines and drivers used in many systems.

SPP is provided in source or binary form and is written in C, allowing for easy modification and tailoring.

SUMMARY

MIPS Development platforms provide all the tools necessary for hardware and software system design. UNIX complements the tool set by providing an engineering environment and communication capabilities to support a large or small engineering team. This environment supports the full development cycle required to be successful with and quick to market with applications based on the IDT/MIPS RISC processor family.

ADDITIONAL INFORMATION

Additional information about specific models and capabilities is available from your local IDT sales representative.

Integrated Device Technology, Inc.

TRAINING CLASS
APPLICATIONS DEVELOPMENT WITH THE IDT R3051™/R3081™ FAMILY OF RISControllers™

OVERVIEW

IDT offers a training class intended to provide in-depth knowledge on the use and capabilities of the R3051/R3081 family of processors. The class is intended to provide an accurate basis for device evaluation, as well as to provide a design engineer with the ability to rapidly bring an R3051/81 application to production.

The class is thus intended for engineers who are designing with the processor family, and who wish to minimize time to market. It is also appropriate for customers performing a detailed processor survey prior to device selection.

COURSE CONTENTS

The course provides a detailed discussion, including hands-on workshops, of both the hardware and software considerations appropriate to applications development. While the course does assume basic familiarity with hardware and software development, the course does not assume previous RISC training or experience.

The course prepares the participant to create designs around the R3051 family through detailed lecture and workshops. The programming envirnoment is reviewed, as are the various hardware price-performance tradeoffs available.

A detailed outline of the course is contained on the next page.

COURSE LOCATION AND SCHEDULE

The course is held on three consecutive days at our Santa Clara, California facility. Directions, accomodations, and schedule information is available from your local sales representative.

7

DAY 1

Device Overview
- CPU Integer Unit
- Floating Point Accelerator
- System Control Co-Processor
- On-chip Caches
- System Interface

Instruction Set Architecture
- Overview
- Register Model
- Instruction Set Details
- Co-processor Operations

IDT/sim
- Overview
- Commands

Workshop: Using IDT/sim
- Instruction decoding
- Command Set
- Program Assembly

Cache Architecture
- Cache Architecture
- Operation
- Flushing
- Performance

Memory Management
- Overview
- Virtual to Physical Address Translation
- TLB Operation

Exception Handling
- Precise Exception Model
- Exception Processing
- Software Techniques
- Exception Latency
- Special Techniques

Workshop: IDT R3051 Family Evaluation Board

DAY 2

System Interface
- Operations Priority
- Execution Engine Fundamentals
- Read Interface
- Write Interface

Workshop: Reading and Writing a Memory Mapped Register

DRAM Interface
- Discrete Implementation Techniques
- The R3721 DRAM controller

Workshop: DRAM Control

Reset/Clocking Interface
- Mode selectable options
- Input and output clocks

Workshop: Reset Interface

High-Level Language Program Development
- Compiler overview
- IDT/c multi-host compiler

Workshop: Program Development

DAY 3

7RS385 Evaluation Board Design Review
- Board Overview
- Memory Timing
- I/O Timing

Floating Point Options
- Hardware floating point
- Software Emulation

Workshop: Motor Control

Software Development
- Simulation tools
- IDT/kit
- IDT/sim
- Remote target symbolic debug

Workshop: Software Development

Subsystem Products
- Module Products
- Interface Techniques

Workshop: Hardware and Software Integration

Integrated Device Technology, Inc.

FASTX™ COLOR X-TERMINAL REFERENCE PLATFORM FOR IDT R3051 FAMILY

ADVANCE INFORMATION
IDT79S3901

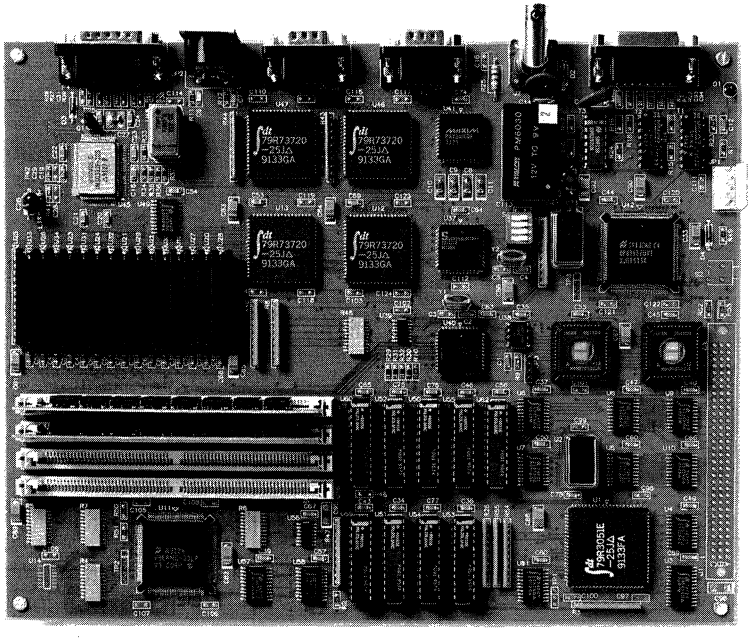
FEATURES:

- IDT79R3051E/3052E/3081E RISController™ CPU
- 2MB, 4MB, 8MB, or 16MB DRAM in up to 4 SIMM modules
- V3 Burst memory DRAM controller
- 2MB Video RAM video buffer
- Up to 1MB ROM or EPROM
- Supports up to 25MHz processor-memory interface
- Programmable resolution up to 1280 x 1024
- 8 bits of color per pixel
- Programmable refresh rate
- Standard PC/AT keyboard
- Two RS-232C serial ports, up to 19.2Kbaud
- IEEE 802.3 10base5 and 10base2 Ethernet interface
- Serial EEPROM stores configuration settings
- On-board speaker driver port
- Expansion/debug connector
- Interval timer for interrupts from 3.9ms to 500ms
- +5VDC, ±12VDC

DESCRIPTION:

IDT's FASTX Reference Platform provides a hardware baseline design, complete with X11 software for evaluation of cost-performance points and different OEM implementation options. The IDT R3051 family offers the widest range of RISController™ cost-performance options based on pin-compatible choices of cache, frequency and floating point options.

FASTX includes a programmable frame buffer supporting resolutions up to 1280 x 1024. Its small size and single processor orientation make it an excellent starting point for low-cost, high-performance designs. Cost-performance points can be easily adjusted by CPU clock frequency, CPU choice (cache size options) and the amount of memory installed.



FASTX Board. Actual Size 10.75" x 8.5" x 1.5"

OCTOBER 1992

Integrated Device Technology, Inc.

IDT R3051™ FAMILY LASER PRINTER CONTROLLER REFERENCE PLATFORM FOR PostScript™ Level 2 SOFTWARE FROM ADOBE®

ADVANCE INFORMATION
IDT79S389

FEATURES

- Software-ready laser printer controller suitable for Adobe OEMs developing PostScript Level 2 products
- IDT/Adobe demonstration platform for PostScript Level 2 software running on IDT's R3051 RISController™ family
- IDT/OEM R3041/R3051/R3081 based prototyping target and reference design (25MHz)
- Uses IDT79R3721 DRAM Controller and IDT73720 Bus Exchangers
- Options for two-way interleaved or non-interleaved (jumpers) DRAM memory system
  - Up to 16MB DRAM (four 72-pin sockets; 1 or 4MB SIMMs)
  - 4 non-interleaved banks or 2 two-way interleaved banks
- Options for two-way interleaved or non-interleaved EPROM/ROM memory system
  - Up to 4MB ROM (8 32-pin sockets; 1, 2 or 4Mb EPROM/ROMs)
  - 2 non-interleaved banks or 1 two-way interleaved bank
- 512 bytes serial EEROM
- Programmable DUART (85C30) with RS232C and AppleTalk® ports
- SCSI Controller (53C80) with one SCSI port (2 connector locations)
- Centronics parallel input port
- Adobe reference front panel interface (based on Canon LBP-8 MARKIIIR 6-button/LCD/LED front panel)
- IDT FIFO-based Canon video interface to LBP-SX/RX engines
- Clock, reset and interrupt generation logic
- Expansion bus connector for:¡
  - Custom engine interfaces (600dpi, color, etc.)
  - Additional I/O (Ethernet, Adobe FAX, etc.)
  - Additional font ROM space
- Shipped with IDT/sim™ initialization and monitor debug software (PostScript EPROMs available from Adobe)
- Executes various Adobe software (provided only under license from Adobe Systems Incorporated), including:
  - Adobe's high-level and low-level monitors
  - Adobe Print Architecture
  - Adobe's PostScript Level 2 Interpreter

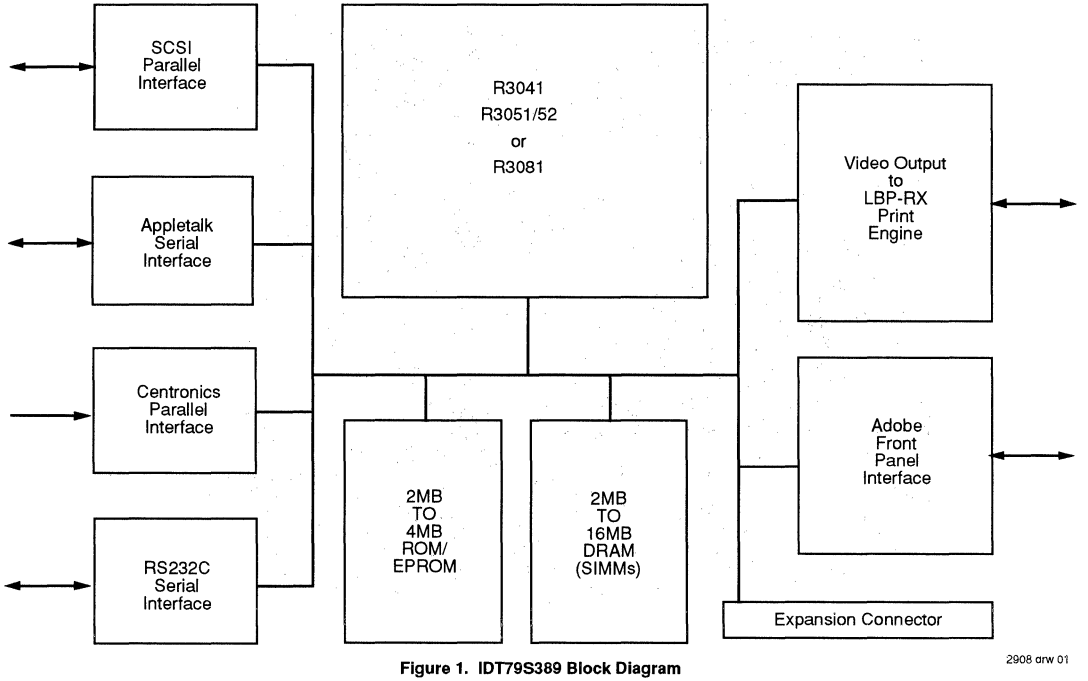


Figure 1. IDT79S389 Block Diagram

OCTOBER 1992

INTRODUCTION

The IDT79S389 provides an R3051 family laser printer controller Reference Platform for rapid adaptation into OEM differentiated products using PostScript Level 2 software from Adobe. "Reference Platform" means that IDT and Adobe engineers have jointly developed both hardware and software modules for the specified configuration. This provides a baseline hardware and software design to accelerate time to market where changes can be limited to one or two areas (form factor, engine interface or I/O options), without having to start at the beginning.

Since the IDT R3051 family includes pin-compatible members with and without floating point accelerator hardware on chip, Adobe software licensees will be able to obtain "core PostScript" binaries in two versions: one compiled with the MIPS C compiler assuming the presence of the FPA (for IDT79R3081), and another version based on IDT's floating point emulation libraries (for IDT79R3041, R3051 and R3052).

The IDT79S389 is completely self contained, and is intended for use either on the desktop, or installed inside a variety of Canon print engines; e.g. Canon OEM engines LBP-SX and LBP-RX, Canon LBP-8 MARKIIIR and HP LaserJet III. The IDT79S389 fits into any of the above engine mounting locations, including the standard power supply and video interface connections. For evaluation on the desktop, a PC-style 4-pin power supply connector is also provided. Figure 1 illustrates the simplified block diagram of the IDT79S389 Reference Platform.

The IDT79S389 Reference Platform is designed around the R3051 RISController family, including the IDT79R3081 and the R3041. All devices in the R3051 family are pin and software compatible. As a consequence, R3041, R3051E, R3052, R3052E, R3081 and R3081E can be substituted for the R3051 throughout this manual. For details on the R3051 family refer to the data sheets and hardware user manuals.

SYSTEM OVERVIEW

Figure 2 illustrates a high-level schematic of the data paths and various subsystems of the board. The User's Manual that ships with the board provides extensive detail on the board, including complete schematics, PAL equations, and theory of operation.

Address and Data Path

The R3051 family uses a time multiplexed address and data bus. The IDT79S389 demultiplexes this bus into an address bus and two data buses. The use of two data buses both minimizes the loading of the buses, and allows either or both of the EPROM and DRAM subsystems to be interleaved.

The address path is constructed using IDT 74FCT162373 16-bit wide transparent latches, and is de-multiplexed off the A/D bus using the processor supplied ALE output signal.

The data paths are provided by a pair of IDT 73720 Bus Exchangers. The 73720 in general is a 3-port, 16-bit wide transceiver, used to multiplex a common CPU port between two data ports (typically found in two way interleaved sys-

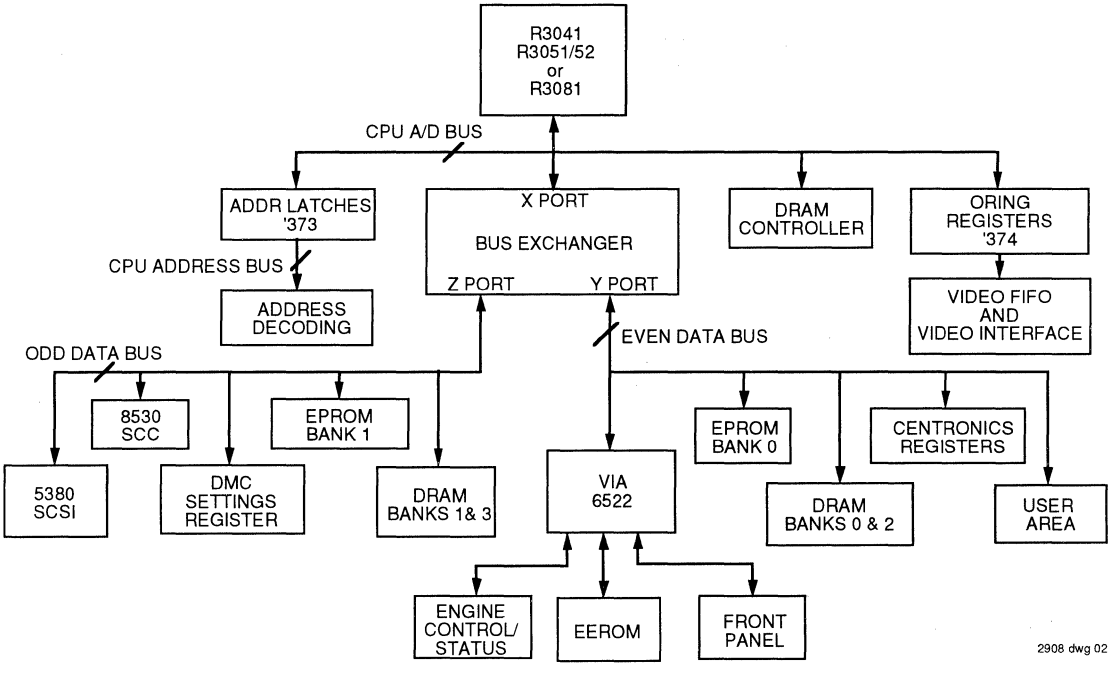


Figure 2. IDT79S389 High Level Schematics

	1MB SIMM non-interleaved	1MB SIMM interleaved	4MB SIMM non-interleaved	4MB SIMM interleaved
Bank 0	0x0080_0000 -> 0x008F_FFFF	0x0080_0000 -> 0x009F_FFFF (even)	0x0080_0000 -> 0x00BF_FFFF	0x0080_0000 -> 0x00FF_FFFF (even)
Bank 1	0x0090_0000 -> 0x009F_FFFF	0x0080_0000 -> 0x009F_FFFF (odd)	0x00C0_0000 -> 0x00FF_FFFF	0x0080_0000 -> 0x00FF_FFFF (odd)
Bank 2	0x00A0_0000 -> 0x00AF_FFFF	0x00A0_0000 -> 0x00AF_FFFF (even)	0x0100_0000 -> 0x013F_FFFF	0x0100_0000 -> 0x017F_FFFF (even)
Bank 3	0x00B0_0000 -> 0x00BF_FFFF	0x00A0_0000 -> 0x00AF_FFFF (odd)	0x0140_0000 -> 0x017F_FFFF	0x0100_0000 -> 0x017F_FFFF (odd)

Table 1. DRAM Memory Map

tems). The control of the 73720 Bus Exchangers is performed by a dedicated PAL, which directs transfers between the CPU and the appropriate data bus, and insures that bus conflicts are avoided.

State Machines

The IDT79S389 uses a distributed state machine structure to implement control of the various peripheral subsystems. In this structure, each peripheral subsystem has dedicated control PALs associated with it. These PALs monitor the start of a transaction, and either ignore the transaction (if intended for other subsystems), or provide the appropriate control responses back to the processor at the appropriate times, according to the latency of the targeted subsystem. A master PAL generates a common "Cycle End" indicator to all state machines, indicating that they can await another transaction.

The advantage of this distributed state machine structure is that memory subsystems can be independently added, removed, or modified, without impacting the rest of the system. This simplifies end user customization and system debug.

The disadvantage of this structure is that the number of PALs required is larger than if the state machines were centralized. It is expected that customers using this as a reference design would customize and/or cost reduce the state machines and I/O subsystems, using interface ASICs, ASSPs, or condensed PALs.

In addition to the distributed state machines, the IDT79S389 contains a number of PALs providing common functions to all state machines. These functions include address decoding, Cycle End generation, data path steering logic, bus timeout, and CPU input/response synchronization.

CPU Subsystem

The IDT79S389 board incorporates the standard R3051 family PLCC footprint. It is targeted to run at 25MHz, although its frequency may be scaled up or down, as appropriate. Note that when scaling frequency, the user should reprogram the wait states associated with the various memory and peripheral subsystems, and may need or choose to use faster or slower control and memory devices. The board and software do not require the use of a TLB.

DRAM Subsystem

The DRAM subsystem of the IDT79S389 board supports the use of 256Kx32 or 1Mx32 72-pin SIMM memories. Up to 4 SIMMs may be used, for a maximum of 16MB of DRAM memory. The memory can be interleaved or non-interleaved, according to a set of DIP switches.

The DRAM system is controlled by the IDT79R3721 DRAM controller. This device features an R3051 family bus interface, and implements direct control of the DRAM devices. The timing and configuration of the DRAMs is programmable in the R3721, according to the settings of an internal mode register.

To maximize user flexibility without requiring PROM changes, the IDT79S389 memory maps a set of DIP switches, called the MSEL switches. At system startup, the value of these switches is read by the CPU and then written to the IDT79R3721 DRAM controller, to configure the system timing model. Thus, in order to change the memory configuration or timing, the user merely needs to set the DIP switches and reset the board.

The DRAM memory is memory mapped to the address space 0x0080_0000 to 0x017F_FFFF, depending on the size of SIMM, number of SIMMs, and interleaving chosen. Table 1 illustrates the address map, depending on configuration. Table 2 illustrates the read and write latency (measured in clock cycles) of the various memory configurations, assuming 80ns SIMMs and a 25MHz system.

The IDT79S389 board is shipped with two 1MB 80ns SIMMs in a non-interleaved configuration. Additional SIMMs can be added by the user, and interleaving can easily be selected.

	Interleaved	Non-Interleaved
First Word of Read	5	5
Adjacent words	1	2
Non-page Write	4	4
Page Write	3	3

Table 2. Number of Clock Cycles for Various DRAM Transfers

	1Mb EPROM	2Mb EPROM	4Mb EPROM
Bank 0 (non-Interleaved)	0x1FC0_0000 -> 0x1FC7_FFFF	0x1FC0_0000 -> 0x1FCF_FFFF	0x1FC0_0000 -> 0x1FDF_FFFF
Bank 1 (non-interleaved)	0x1FC8_0000 -> 0x1FCF_FFFF	0x1FD0_0000 -> 0x1FDF_FFFF	0x1FE0_0000 -> 0x1FFF_FFFF
Bank 0 (Interleaved)	0x1FC0_0000 -> 0x1FCF_FFFF (even)	0x1FC0_0000 -> 0x1FDF_FFFF (even)	0x1FC0_0000 -> 0x1FFF_FFFF (even)
Bank 1 (interleaved)	0x1FC0_0000 -> 0x1FCF_FFFF (odd)	0x1FC0_0000 -> 0x1FDF_FFFF (odd)	0x1FC0_0000 -> 0x1FFF_FFFF (odd)

Table 3. EPROM Address Map

EPROM Subsystem

The EPROM subsystem contains 8 sockets, capable of accepting 1Mb, 2Mb, or 4Mb devices. The sockets accept 8-bit wide EPROMs in the DIP package.

The board can be used with either 4 or 8 EPROM devices; if 8 devices are used, Interleaved or non-interleaved operation can be selected. The density of EPROM, and the interleaving factor, are selected via jumpers and PALs for the board. The board ships with 512KB of 120ns EPROM installed in a single bank; the EPROMs contain the IDT/sim monitor program ported to this board.

The EPROMs reside in the physical address range 0x1FC0_0000 through 0x1FFF_FFFF. This address space includes the system exception vectors, as well as the bootup code, and can be accessed either through or around the on-chip processor cache, according to the virtual address used. Table 3 shows the physical address map for the EPROMs. Table 4 shows the memory latency of the EPROM subsystem, for 120ns EPROMs and a 25MHz system.

SCSI Subsystem

The IDT79S389 board contains a single SCSI channel, implemented using the 53C80 SCSI controller. Although there is only one channel, there are two SCSI connectors on the board, to support the differences in the form factor of the various laser engines supported.

The SCSI device resides in the address range 0x0074_0000 through 0x0074_FFFF.

Serial Channels Subsystem

The IDT79S389 board implements two serial channels. One is a traditional RS-232 channel, and is accessed by a DB-25 connector. The other channel supports AppleTalk, and uses the standard AppleTalk connector. The board includes voltage translators and transceivers to implement the electrical protocols required by these standards.

	Interleaved	Non-Interleaved
First Word of Read	5	5
Adjacent words	4	1.6 (1-3-1)

Table 4. Number of Clock Cycles for Various EPROM Transfers

The serial channels are implemented using a single 85C30 SCC serial controller. The address space for the serial controller is 0x0073_0000 through 0x0073_FFFF.

EEROM Interface

The IDT79S389 board includes a 512B EEROM to store various configuration data. The EEROM is accessed by the 65C22 VIA device, which is memory mapped to 0x0071_0000 through 0x0071_FFFF.

Centronics Interface

The board also includes a unidirectional Centronics port. Centronics data is read from address space 0x0075_0000 through 0x0075_FFFF; Centronics status is written in the address space 0x0076_0000 through 0x0076_FFFF.

Front Panel Interface

The front panel interface corresponds to a Canon LBP-8 Mark IIIR, and uses a series of switches, LEDs, and LCDs to implement front panel control. Front panel is accessed by the 65C22 VIA device, which is memory mapped to 0x0071_0000 through 0x0071_FFFF.

Video Interface

The video interface corresponds to the interface requires for the Canon LBP-8 Mark IIIR, based on the Canon LBP-RX print engine. The video interface is implemented using discrete logic, with status taken from the 65C22.

Video data is sent to the video interface by performing an aliased read of the DRAM memory. If a processor read of the 16MB region starting at 0x0880_0000 is detected, the access will be processed as a DRAM read. However, the read data returned from the DRAM will be captured by the video interface, and later shifted out to the print engine. This technique eliminates overhead by not requiring the processor to explicitly write the data to the video channel.

User Expansion Area

In addition to the memory systems described above, the IDT79S389 board contains a user expansion connector. The user expansion connector allows users to add custom features to the board for software development. Features which could be added might include an Ethernet channel, additional font ROM, or a different engine and front panel interface.

The IDT79S389 board provides a User Chip Select, mapped to address 0x0078_0000 through 0x0078_FFFF, for use with the expansion connector.

Board Form Factor

The form factor and hole placement of the board allows it to be directly mounted into either a Canon LBP-8 Mark IIIR laser printer, the HP LaserJet III, or the Canon OEM print engines LBP-SX or LBP-RX engines. The placement of the video, front panel, and power connectors, are compatible with these form factors.

In addition, the board can be run on a benchtop using a standard PC compatible power supply. If the board is used in this fashion to drive an engine, it is recommended that a common ground between the board and the engine be provided.

Summary: Address Map and Interrupt Assignment

Table 5 is a summary of the address map of the IDT79S389 board. Table 6 shows the interrupt assignments of the CPU.

Memory Subsystem	Start Address	End Address
VIA	0x0071_0000	0x0071_FFFF
SCC	0x0073_0000	0x0073_FFFF
SCSI	0x0074_0000	0x0074_FFFF
Centronics Data	0x0075_0000	0x0075_FFFF
Centronics Status	0x0076_0000	0x0076_FFFF
User Chip Select	0x0078_0000	0x0078_FFFF
MSEL Switches	0x0079_0000	0x0079_FFFF
R3721 Mode Register	0x007A_0000	0x007A_FFFF
DRAM	0x0080_0000	0x017F_FFFF
Aliased Video DRAM	0x0880_0000	0x097F_FFFF
EPROM	0x1FC0_0000	0x1FFF_FFFF

Table 5. IDT79S389 Memory Map Summary

Device	CPU Interrupt
Reserved	Int(0)
R3081 Floating Point	Int(1)
VIA	Int(2)
HFull/Video Reset	Int(3)
SCSI	Int(4)
SCC	Int(5)

Table 6. IDT79S389 Interrupt Assignment

SPECIFICATION SUMMARY

Order Number: IDT79S389

Maximum on board memory capacity:

DRAM — Four 72-pin SIMM sockets for 256Kx32 or 1Mx32 (1 to 16 MB)

EPROM — Eight 32-pin sockets for 128Kx8 to 512Kx8 (to 4 MB)

Serial EEROM — One 8-pin socket for serial EEROM (512 bytes)

Debug Monitor EPROM: IDT/sim Version 4.0 ported to IDT79S389

Serial Ports: Controlled by 85C30 DUART.

Serial — CRT terminal connector or for downloading J3 (25-pin AMP 748133-1,DB25S, right angle female).

Appletalk — AppleTalk connector J2 (8-pin AMP 749179-1, D8 8, right angle female).

Parallel port:

Centronics — 36-pin, female, right angle, standard Centronics parallel connector (R.Nugent RPM-C36SB-SR-TG).

SCSI port: Controlled by 53C80 SCSI controller. SCSI connector J5 or J10 (50-pin, female, right angle, (R.Nugent RPM-C50SB-SR-TG).

Video: Standard 20-pin, male Canon LBP-RX video interface connector (HIROSE PCN-10-20P 2.54DSA).

Front Panel: J7, 34-pin male, right angle connector (AMP 1-103149-7).

Expansion: Four 40-pin male, four wall headers, J11-14 (MOLEX 39-26-7404).

Physical: Compatible with Canon RX, SX engine form factors.

Operating Temp: 0-50ºC.

Power Supply: 5.0V +- 5%, 3 Amps typical (estimate).

PHYSICAL LAYOUT

The physical layout of the IDT79S389 Reference Platform reflects the board's primary objectives:

1. Software delivery vehicle for PostScript Level 2 software from Adobe
   — Memory space appropriate for PostScript Level 2 software typical implementations,
   — Various memory configurations (interleaved vs non-interleaved, code running out of DRAM or out of ROM) to easily evaluate cost and performance alternatives.

2. Cost-Effective design model for IDT79R3051 RISController family
   — NO zero-wait-state memory,
   — Minimum complexity board configuration (6 layers),
   — Fits industry standard Canon LBP-RX print engine.

3. Advanced hardware starting point for rapid evaluation, cost-performance point analysis and development of OEM finished products.

4. Advanced software-ready controller, suitable for immediate development with PostScript Level 2 software from Adobe, and adaptation to other print engines and communications ports (Adobe software available only under license from Adobe Systems Incorporated).

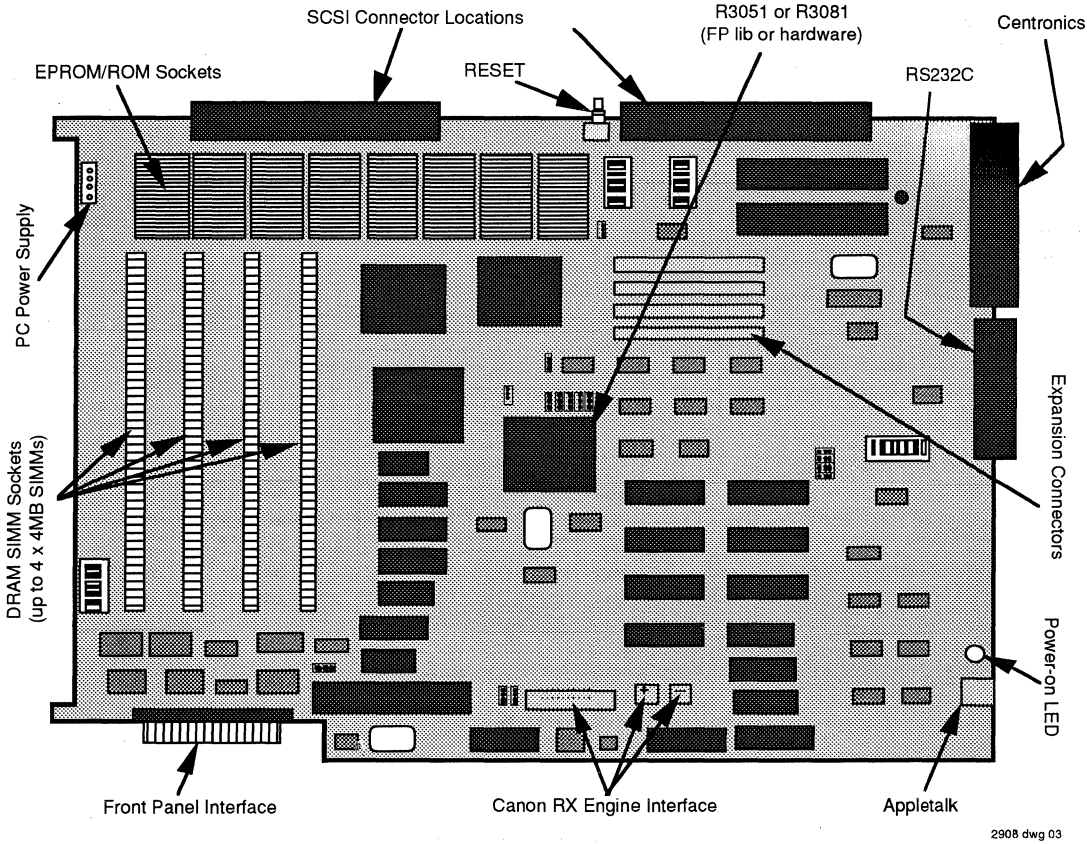


Figure 3. IDT79S389 Board Layout

Integrated Device Technology, Inc.

IDT79R4000 FLEXI-CACHE™ DEVELOPMENT TOOL

PRELIMINARY
IDT7MP6048
IDT7MP6068

FEATURES:

- Hardware Development Tool for implementing various configurations of the secondary cache requirement for the IDT79R4000 CPU
- Configurable in various cache sizes, number of words per line size, and split vs. unified cache operation
- Move from prototype/development to production with no redesign by using pin compatible "production grade" IDT79R4000 secondary cache modules
- Development module operating frequencies to support zero wait-state 50MHz IDT79R4000 operation
- Four identical 80 lead gold-plated SIMMs (Single In-Line Memory Modules) support each IDT79R4000 CPU
- Surface mounted plastic components on a multilayer epoxy laminate (FR-4) substrate
- Multiple ground pins and decoupling capacitors for maximum noise immunity
- TTL compatible I/Os
- Single 5V (±10%) power supply

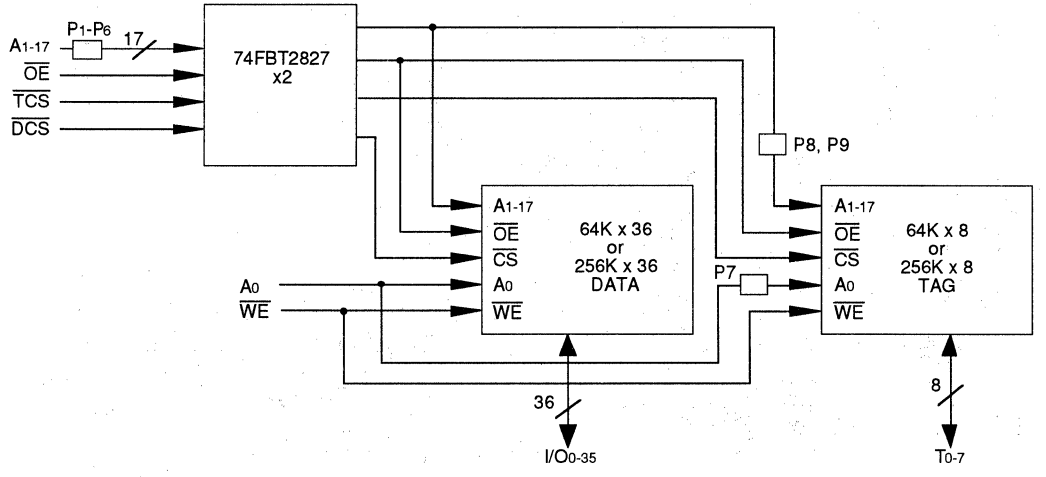
DESCRIPTION:

The IDT7MP6048/7MP6068 is a Hardware Development Tool used for implementing various configurations of the secondary cache requirement for the IDT79R4000 CPU. By changing jumpers on the modules, the designer can easily change certain characteristics (cache size, number of words per line, and split vs. unified operation) of the secondary cache in the lab. By running benchmarks on the actual system using these various cache configurations, the secondary cache which best optimizes system performance can be determined. This development tool gives you cache performance benchmarks which are superior to benchmarks derived via simulation.

Move from development to production without changing the secondary cache footprint by choosing pin compatible "production grade" IDT79R4000 secondary cache modules. These high performance, high density IDT modules are optimized to meet the customers' exact cache requirements required for volume production of the system (please consult the factory for more details).

The IDT7MP6048 is a 1MB secondary cache module block (four identical modules builds a complete cache to support each IDT79R4000 CPU) constructed on a multilayer, epoxy laminate substrate (FR-4) using 11 64K x 4 static RAMs and FBT logic drivers while the IDT7MP6068 is a 4MB secondary cache module block using 11 256K x 4 static RAMs and FBT logic drivers. Extremely high speeds can be achieved using high-performance BiCMOS IDT61B298 or IDT71B028 static RAMs and IDT74FBT2827 drivers. The FBT drivers have

FUNCTIONAL BLOCK DIAGRAM(1)



2841 drw 01

NOTE:

1. The Data and Tag sizes shown on the block diagram are only for the case when the jumpers are in the default positions for the respective modules. These sizes will change according to the jumper connections (see Jumper Connections on page 2).

BiCMOS I/Os and internal 25Ω series output resistors resulting in the fastest propagation times with minimal overshoots and ringing. Multiple GND pins and on-board decoupling capacitors provide maximum noise immunity for this performance critical part of the system. All inputs and outputs of the modules are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refresh for operation of the module.

CACHE CONFIGURATIONS(1)

Memory Size
4MB (7MP6068 default)
2MB
1MB (7MP6048 default)
512KB
256KB
128KB

Words per line
4 (default)
8
16
32

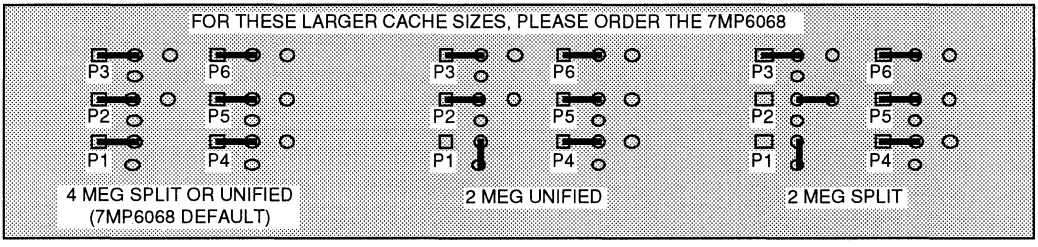
Cache Operation
unified cache (default)
split cache

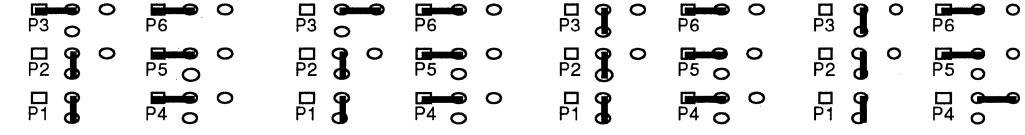
NOTE: 2841 tbl 01

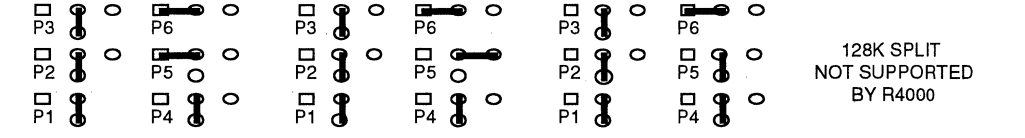
1. Please refer to the Jumper Connections for instructions on how to implement the Cache Configurations shown above.

JUMPER CONNECTIONS:

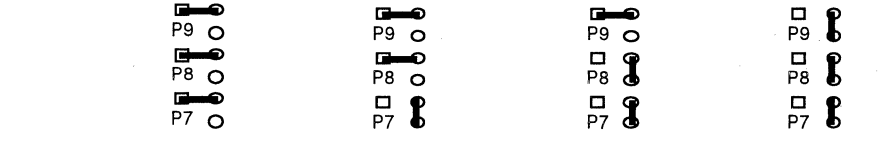
Cache depth and Split vs. Unified Operation are controlled by Jumpers P1-P6 as follows:







Cache line size is controlled by Jumpers P7-P9 as follows:



2841 drw 02

PIN CONFIGURATION[1]

VCC	2	1	GND
I/O1	4	3	I/O0
I/O3	6	5	I/O2
I/O5	8	7	I/O4
GND	10	9	I/O6
I/O8	12	11	I/O7
I/O10	14	13	I/O9
I/O12	16	15	I/O11
I/O14	18	17	I/O13
I/O15	20	19	GND
I/O17	22	21	I/O16
I/O19	24	23	I/O18
I/O21	26	25	I/O20
GND	28	27	I/O22
I/O23	30	29	VCC
I/O25	32	31	I/O24
I/O27	34	33	I/O26
I/O29	36	35	I/O28
I/O30	38	37	GND
I/O32	40	39	I/O31
I/O34	42	41	I/O33
GND	44	43	I/O35
A0	46	45	$\overline{WE}$
A2	48	47	A1
A4	50	49	A3
A6	52	51	A5
VCC	54	53	GND
$\overline{OE}$	56	55	$\overline{DCS}$
A8	58	57	A7
A10	60	59	A9
GND	62	61	A11
A13	64	63	A12
A15	66	65	A14
A17	68	67	A16
T0	70	69	$\overline{TCS}$
T1	72	71	GND
T3	74	73	T2
T5	76	75	T4
T7	78	77	T6
GND	80	79	VCC

2841 drw 03

SIMM
TOP VIEW

NOTE:
1. For proper operation of the module, please refer to the Jumper Connections for proper connections of the module pins.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5V ± 10%

2841 tbl 02

PIN NAMES

I/O0-35	Data Inputs/Outputs
T0-7	Tag Inputs/Outputs
A0-17	Address Inputs
$\overline{DCS}$	Data Chip Select
$\overline{TCS}$	Tag Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground

2841 tbl 03

CAPACITANCE

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN(D)	Input Capacitance (Data)	VIN = 0V	10	pF
CIN(A)	Input Capacitance (A1-15, $\overline{OE}$, $\overline{TCS}$, $\overline{DCS}$)	VIN = 0V	10	pF
CIN(B)	Input Capacitance (A0, $\overline{WE}$)	VIN = 0V	100	pF
COUT	Output Capacitance	VOUT = 0V	10	pF

NOTE: 2841 tbl 04
1. This parameter is guaranteed by design, but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6	V
VIL	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 2841 tbl 05
1. VIL = –1.5V for pulse width less than 10ns.

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating[1]	Value	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	–10 to +85	°C
TSTG	Storage Temperature	–55 to +125	°C
IOUT	DC Output Current	50	mA

NOTE: 2841 tbl 06
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

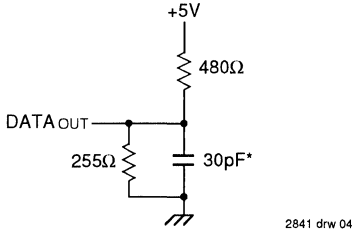
Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI1}\|$	Input Leakage (except A_0, $\overline{WE}$)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LI2}\|$	Input Leakage (A_0, $\overline{WE}$)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	110	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
I_{CC}	Operating Current	$\overline{CS}$ = V_{IL}; V_{CC} = Max., Outputs Open	—	2200	mA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} =–4mA	2.4	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V

2841 tbl 07

AC TEST CONDITIONS

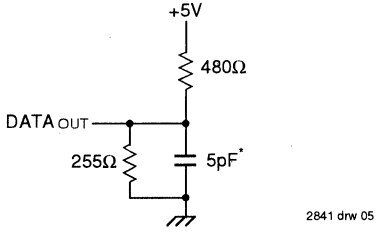
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1—4

2841 tbl 08



2841 drw 04

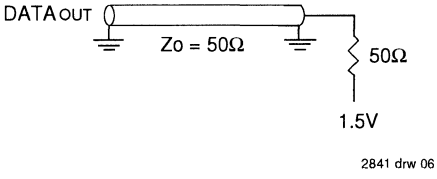
Figure 1. Output Load



2841 drw 05

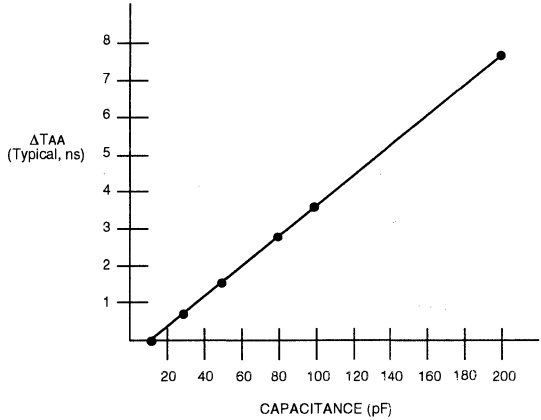
Figure 2. Output Load (for t_{OLZ} and t_{OHZ})

* Including scope and jig.



2841 drw 06

Figure 3. Alternate Output Load



2841 drw 07

Figure 4. Alternate Lumped Capacitive Load, Typical Derating

7

AC ELECTRICAL CHARACTERISTICS

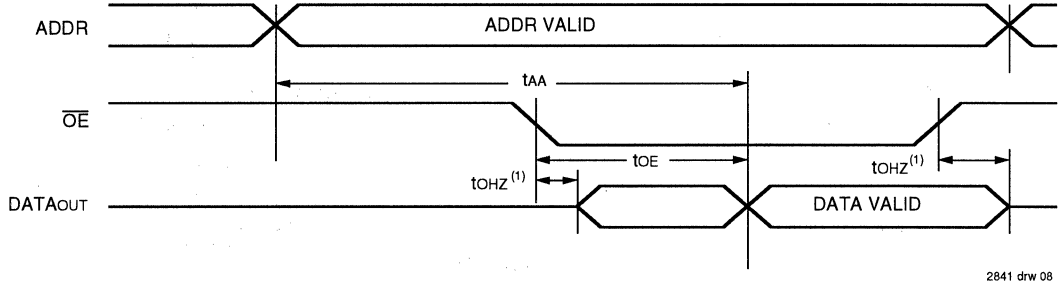
(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MP6048/6068SxxM												Unit
		-12		-15		-17		-20		-25		-30		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE														
t_{AA}	Address Access Time	—	12	—	15	—	17	—	20	—	25	—	30	ns
t_{A0A}	A_0 Access Time	—	10	—	12	—	14	—	16	—	21	—	26	ns
t_{OE}	Output Enable to Output Valid	—	12	—	15	—	17	—	20	—	25	—	30	ns
t_{OHZ}(1)	Output Disable to Output in High-Z	—	10	—	12	—	13	—	15	—	17	—	20	ns
t_{OLZ}(1)	Output Enable to Output in Low-Z	2	—	2	—	2	—	2	—	2	—	2	—	ns
WRITE CYCLE														
t_{AW}	Address Valid to End of Write	12	—	15	—	17	—	20	—	25	—	30	—	ns
t_{A0W}	A_0 Valid to End of Write	10	—	12	—	14	—	16	—	21	—	26	—	ns
t_{WP}	Write Pulse Width	7	—	10	—	12	—	15	—	20	—	25	—	ns
t_{DW}	Data Valid to End of Write	7	—	10	—	12	—	15	—	20	—	25	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design but not tested.

2833 tbl 08

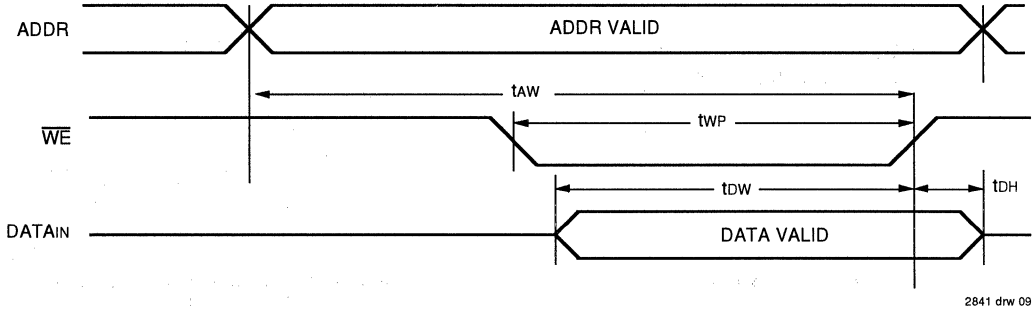
TIMING WAVEFORM OF READ CYCLE(1)



2841 drw 08

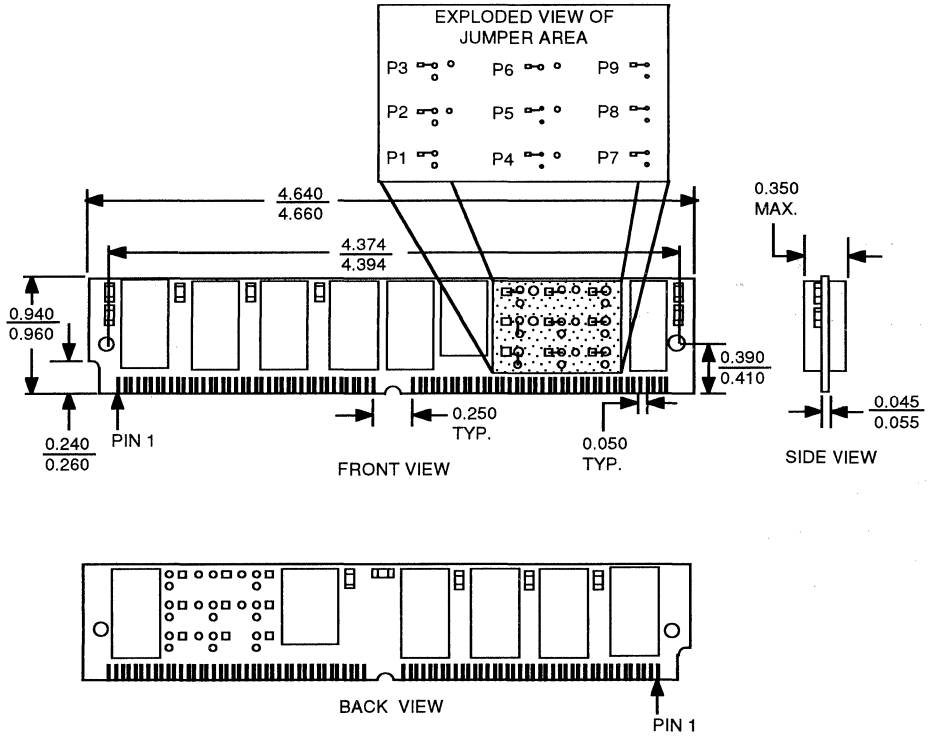
NOTE:
1. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE



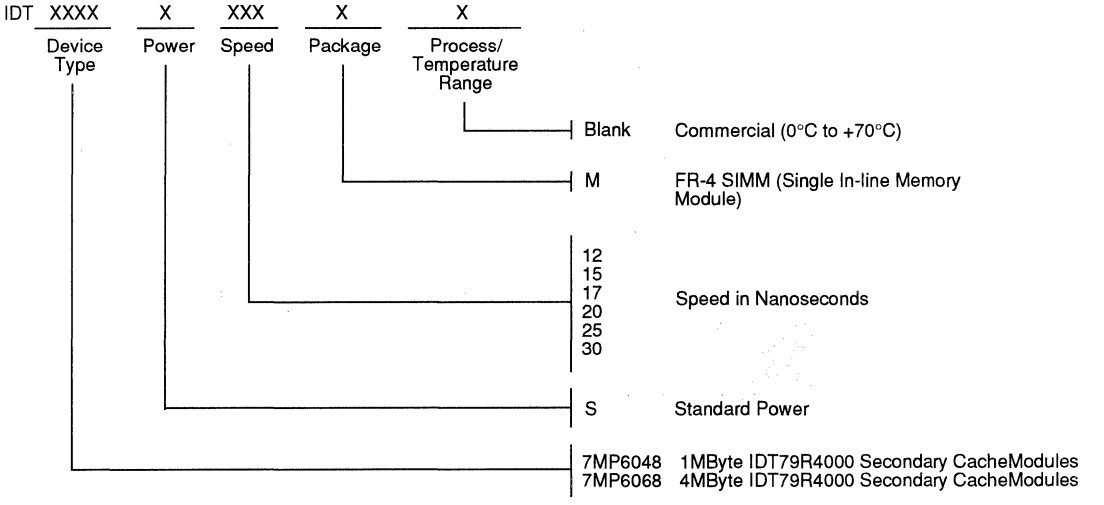
2841 drw 09

PACKAGE DIMENSIONS



2841 drw 10

ORDERING INFORMATION



2841 drw 11

7

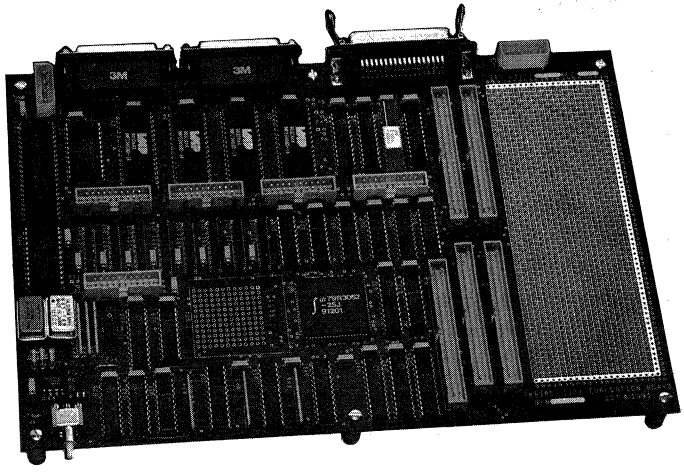
Integrated Device Technology, Inc.

R3051™ FAMILY EVALUATION KIT

IDT79S385A

FEATURES:

- Complete 25MHz RISC System Board
  - — Requires only 5V supply and terminal to operate
  - — Supports R3041, R3051, R3052, or R3081 highly integrated RISC CPUs
  - — Board contains an IDT 79R3052E
  - — 1MB of non-interleaved DRAM, expandable to 4MB
  - — 128KB of EPROM, expandable to 2MB
  - — Serial and Parallel Ports
  - — Connectors provided for easy connection to HP Logic Analyzer
  - — Wire-wrap area on the board
- IDT/c for IBM PC compatibles included in kit
  - — Hardware or software floating point
  - — Remote symbolic debug
- IDT's System Integration Manager included in EPROM
  - — High capability debug monitor
  - — Simplifies software development
- Complete set of documentation included
  - — Supplied with complete set of board schematics
  - — PAL equations supplied on IBM PC 3.5" disks
  - — User's manuals for R3051 family, IDT/sim, and IDT/c
- Utility programs also included
  - — Program utility disk
  - — HP16500A Logic Analyzer disassembly software
- R3081 sample also included for board upgrade



'385 RISC System Board. Actual Size 8.5" x 11"

DESCRIPTION:

The IDT79S385A Evaluation Kit is a complete kit for evaluating the R3051 hardware and software environment. The kit contains a working system, including all schematics and theory of operation, an R3081 sample to allow the user to upgrade the system capabilities, and a complete software development environment, including debug monitor and "C" compiler/assembler toolchain. Finally, the kit is complemented by documentation, logic analyzer software, and utility programs.

COMPLETE SINGLE BOARD COMPUTER

The '385 board is a complete working RISC system intended as a complete design example using the R3051 family of highly integrated RISC CPUs. The board requires only a simple CRT terminal and a 5V power supply for operation. Figure 2 shows a block diagram of the '385 board.

The board is designed around IDT's R3051 family of highly integrated RISC CPUs. An R3052E CPU chip (8KB I-cache and 2KB D-cache, with on-chip TLB) is included in a socket, but any member of the family can be substituted. The 79S385A kit includes a sample of a 25MHz R3081 in a PGA pinout, to allow the user to upgrade the system. A large wire-wrap area is available on the board for adding additional hardware. All the schematics and details of the designs are supplied with the board, including all PAL equations on an IBM format 3.5" disk.

The '385 board is supplied with 1MB of DRAM in socketed 256Kx4 ZIPs; the ZIPs can be replaced with 4 megabit devices to obtain 4MB of DRAM on the board (an applications brief on upgrading memory is included in the kit). Other hardware on board includes a 2681 DUART and an 8254 counter/timer; both these devices are supported with drivers in IDT/sim. A parallel Centronics port is available for higher speed download of code into the board.

The board contains 128KB of EPROM expandable to 2MB by replacing the EPROMs with higher density devices. The EPROMs contain IDT's powerful System Integration Manager (IDT/sim), a debugging monitor that supports download of code from host systems, execution control commands, memory probing, and I/O.

There are two serial ports, a free-running programmable timer, and a parallel Centronics port for high-speed download of software. A set of expansion connectors permits external hardware to be connected to the board, and a wire-wrap area on the board can be used to build additional hardware without using a second board.

The board is designed to be placed on a flat table-top surface. Standoffs are provided for physical support.

The 3051 Bus, along with other control signals, is connected to a set of pins in the center of the board next to the wire wrap area. These signals can be used to connect additional hardware on either the wire-wrap area or on another board via a ribbon cable. DMA control is provided. Table 1 shows the signal description for the expansion connector.

Signal Name	I or O	Description
EA00-EA31	I/O	32-bit buffered address bus
ED00-ED31	I/O	32-bit buffered data bus
SYSOUT	O	Buffered SYSCLK Clock from CPU; used to synchronize data transfers
MRES#	O	Copy of the Reset signal to the CPU
MREQ	O	Memory Request output (handshaking signal for data transfers)
EXACK#	I	Acknowledge input (handshaking for data transfers)
IP4-IP5	I	Auxillary input pin to the 2681 UART
WEA-WED	O	Write Enables for the four bytes of the data word
UCS	O	Chip select signal decoded from the high order address bits for external hardware
INT0:INT5	I	Interrupt inputs to the R3052
RD#	O	Memory Read output signal from the 3052
WR#	O	Memory Write output signal from the 3052
BREQ#	I	Bus Request input to the 3052
BUSGNT#	O	Bus Grant output from the 3052

2885 tbl 01

Table 1. Signals Supplied on Expansion Connector

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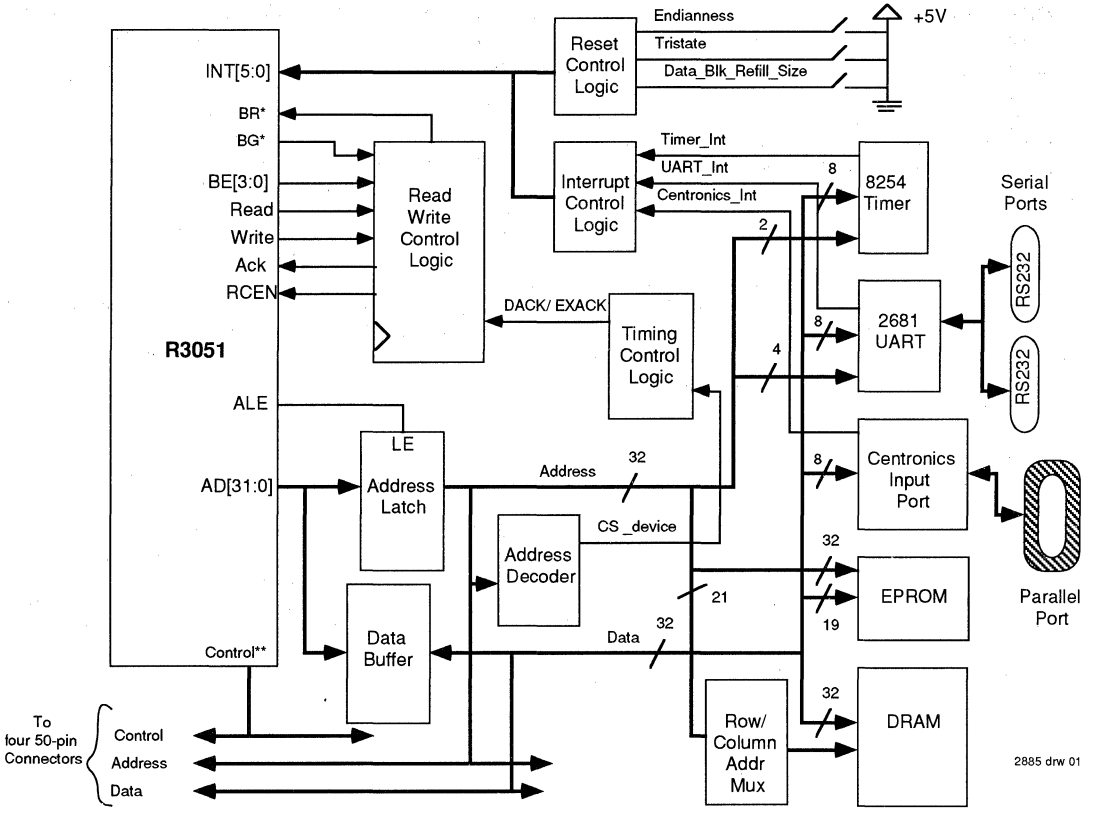


** These control signals include R3051 and the on-board control logic signals as well.

Figure 2. '385 Board Block Diagram

IDT/SIM DEBUG MONITOR SOFTWARE

IDT's System Integration Manager (IDT/sim) is included in EPROMs on the board. This software permits downloading of code from a host system, execution control with breakpoints, in-line assembly and disassembly, and a variety of commands to control main memory, cache memory, and the internal TLB. It provides all the resources needed to bring up new hardware and software.

The evaluation kit also includes a complete set of user documentation for the IDT/sim software tool. The capabilities of IDT/sim are described in a separate data sheet.

IDT/C "C" COMPILER FOR IBM PC COMPATIBLES

In addition, the evaluation kit contains a complete copy of the IDT/c software development toolchain, hosted on IBM PC compatible computers. IDT/c, described in a separate data sheet, includes:

- The ability to generate big- or little-endian code
- Hardware or software floating point support
- "C" library support, including source libraries
- Remote symbolic debug

LOGIC ANALYZER INTERFACE

The 79S385A evaluation kit also includes the ability to simply use an HP16500A logic analyzer for execution trace and software debug. The board includes a set of connectors to easily allow connection of the logic analyzer to the board. Also included is a disk for the HP16500 containing disassembly software, allowing the analyzer to display a disassembled listing of the software executing on the system.

KIT SUMMARY

The IDT 79S385A evaluation kit is a complete low-cost package for evaluation of the R3051 family, especially its software environment. The kit allows the user to develop and execute high-level language programs, to look at a software development toolchain for the IDT R3051 family, and to evaluate a hardware design around the R3051 family.

KIT CONTENTS

'385 RISC Evaluation Board
IDT/c Multi-Host compiler toolchain for IBM PC compatibles
IDT/sim debug monitor included in board EPROMs.
User's Manuals for:

- '385 board
- R3051
- R3081
- IDT/sim
- IDT/c

Applications Guide for R3051 family
Program Utility Disk
Disassembler for HP16500 Logic Analyzer
PAL Equations on IBM PC compatible 3.5" disk format

BOARD SPECIFICATIONS

CPU
25MHz R3052E on board
25MHz R3081 sample included

Cache Ram
8KB I-cache, 2KB D-cache (in 3052 chip)
16KB I-Cache, 4KB D-Cache configurable to
8KB I-Cache, 8KB-DCache (in R3081 chip)

Cacheable Address Space
4GB

DMA Support
Bi-directional tri-stateable buffers can be used to write to DRAM from external logic

Block Refill
4 word instruction block size
1 or 4 word data block size programmable via jumper

Endianness (Byte Ordering)
User programmable via jumper

Read/Write Buffers
Both are 4 words deep (inside 3052 chip)

Interrupts
6 User Interrupts, three synchronized with SYSCLK

I/O characteristics
TTL levels from FCT logic devices, PALs and R3052

Power Supply
2 amps (typical) at 5V, 25°C, at rated speed

Environmental Conditions
Ambient temperature 0°C to +50°C
Relative Humidity 5% to 95%

Clock Frequency
25MHz

Interconnection
Five 50-pin connectors, containing Address, Data, and Control signals and R3052 signals
Five 20-pin plugs for use with HP logic analyzer
Two RS-232 serial ports on DB-25 connectors
One parallel Centronics port for input

User Selectable Options
Endianness, data block refill size

ORDERING INFORMATION

Each unit is shipped with complete schematics and PAL equations. A user's manual includes instructions on downloading code, operating the Software Integration Manager, and providing the correct timing interfaces to additional hardware. Boards are shipped with the 3052E CPU plugged in, but any member of the 3051 family can be used. An additional sample of the R3081 is included to allow user upgrades.

Evaluation Boards

R3051 Family Evaluation Kit 79S385A

EPROM Upgrades

The following part numbers update the evaluation board hardware to the latest version of the IDT/sim monitor.

Evaluation boards 7RS901BGP
Use with 79S385 only

Auxillary Download Programs

For downloading code from a MIPS machine into an evaluation board. This software includes programs to convert MIPS object code into S-records and to download either ASCII or binary S-records to a remote target. This software is only needed if you are running the MIPS C-compiler and do not have SPP. If you are using IDT/c or you have IDT/sim or MIPS SPP you already have these utilities.

MIPS download utility 7RS950BUU
Supplied on QIC-24 TAR tape

Integrated Device Technology, Inc.

IDT/sim™ *NEW! Version 4.0* IDT7RS901
SYSTEM INTEGRATION MANAGER
ROMable DEBUGGING KERNEL
FOR R3000 ISA CPUs

FEATURES:

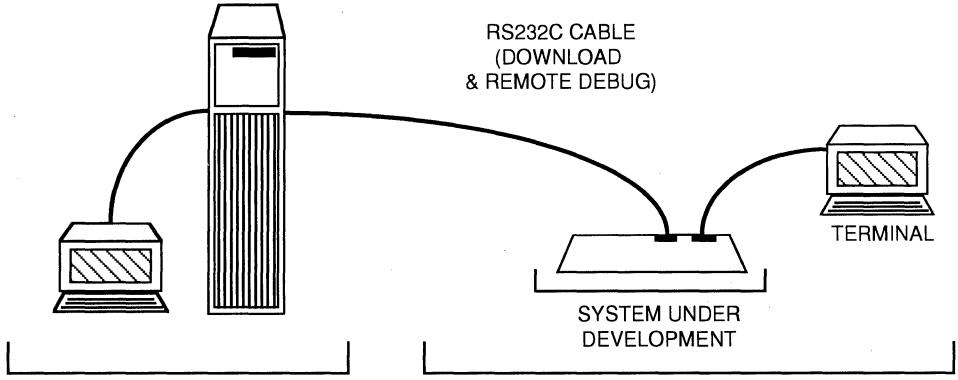
- **Complete Source Code Provided**
- **Robust Debug Monitor**
- **Supports Source Level Debug**
  - **DBX - MIPS Tool Chain**
  - **IDB - IDT/c™ Tool Chain**
- **Remote File Access - Connects Target & Remote Host**
- **Diagnostic Tests for Memory, Cache, MMU, FPU, and System**
- **Adaptable to Systems With or Without Hardware Floating Point Accelerator**
- **Includes Variety of Device Drivers**
- **Easy to Add New Commands and I/O drivers**

POWERFUL TOOL FOR INTEGRATION OF SYSTEMS BASED ON R3000 ISA CPUS:

The IDT7RS901 System Integration Manager (IDT/sim™) is a ROMable software product that permits convenient control and debug of RISC systems built around R3000 ISA CPUs (R3000, R3001, R3500, 3051 Family, 3081 Family). Facilities are included to operate the CPU under controlled conditions, examining and altering the contents of memory, manipulating and controlling R3000 resources (such as cache, TLB and coprocessors), loading programs from host machines, and controlling the path of execution of loaded programs.

IDT/sim source code includes IDT's MicroMonitor, a very simple monitor for performing the initial debugging of new hardware.

IDT/sim requires 115KB of EPROM space for code and data, and 71KB of RAM space for uninitialized variable data and stack.



HOST SYSTEM (MacStation™, MIPS, Sun, or PC)

TARGET WITH IDT/sim in EPROMs System Integration Manager

7

IDT/SIM FEATURES

IDT/sim is a software tool to help system designers debug hardware designs and port software to systems based on one of the R3000 ISA CPUs (R3000, R3001, R3500, 3051 Family, 3081 Family). The software is supplied in EPROMs on most IDT RISC SubSystem Development products, and may be purchased in source code form so it can be compiled and installed on your system.

IDT/sim provides all the basic functions needed to get a new hardware design debugged and to port and debug software on it. Typically, the monitor is compiled and burned into EPROMs that are plugged into the target system. Approximately 115KB of EPROM are needed for the binary code, and 71KB of RAM are needed for storing variables. Once installed, the designer communicates with the monitor via a simple terminal connected to an RS-232 port on the target system. Source code is included to support a variety of UARTs for this port. On start-up, the monitor will determine the cache and main memory sizes automatically.

Diagnostics

The monitor includes a set of diagnostic routines for testing the integrity of the hardware.

Main Memory Test: Finds opens, shorts, and stuck-at faults on data and address lines. A cache memory test runs memory tests on both caches, checks tag memory, and verifies that instructions can be executed from cache.

System Test: Checks the ability to read and store full words, half words, and bytes. Checks cache operation for valid, hit/miss, and invalidation.
MMU Test: Checks operation of TLB inside the R3000.

Floating Point Test: Tests the functionality of the R3010 FPU, including exception interrupts.

Download Support

Object code created on a software development system can be downloaded in either ASCII S-records or binary formats to the target system's memory. The code can be produced with the MIPS development tools or with IDT/c on any of a number of development platforms: MIPs, Sun, IDT's MacStation, and 386/486 PCs under Xenix or DOS.

IDT/sim source code includes utilities to convert object code from the MIPS compiler to S-records, to convert the S-records to a binary format (which is more compressed and downloads faster), and to download the binary records to the target. Similar utilities for use with the IDT/c multi-host C compiler are supplied with IDT/c.

A terminal emulation feature allows the terminal, used as the IDT/sim console, to also be used as a terminal to a software development system accessed through a second serial port. This mode supports remote file download.

Debug Commands

There are a variety of commands included in IDT/sim to support software/hardware debug.

Execution Control: Breakpoint, call, continue, go, gotill, next, step, unbreak.

Memory Commands: Assemble, cache flush, compare,disassemble, dump, dump cache, dump registers, fill, fill registers, move,read/write cache, search and substitute.

TLB Commands: Dump, flush, map, pid and probe.

Remote Debug: Source level debug with DBX on a MIPS RISC/os system and with IDT Cross development 'c' compiler tools.

Communications: Remote file access, terminal emulator and set baud rate.

Run-Time Support

IDT/sim includes over 40 functions that can be called by user's programs to perform common I/O and R3000 control operations. A complete list of the commands is listed later in this document.

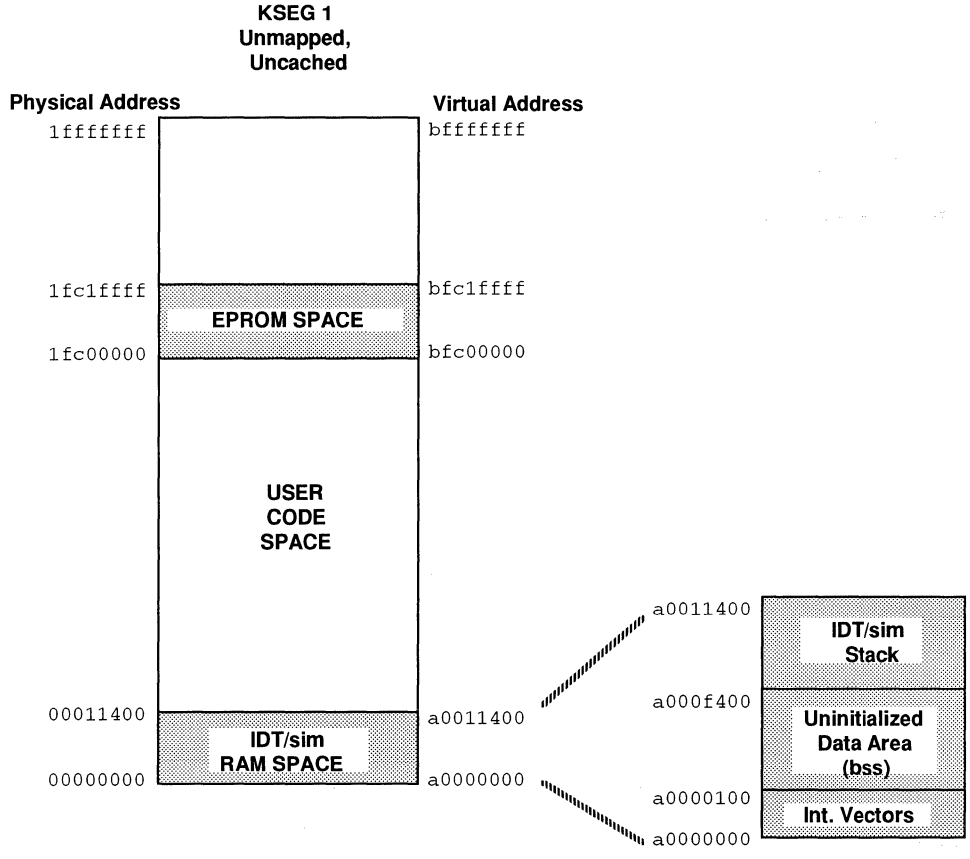
NEW FEATURES IN VERSION 4.0

IDT MicroMonitor: IDT/sim includes IDT's MicroMonitor, a very simple monitor for performing the initial debugging of new hardware. The only hardware which must be functioning to run the MicroMonitor is the CPU, EPROM and a serial port function. This allows for immediate debugging of hardware even when the DRAM memory is not functioning.

Source Level Debug: Supports source level debug using either IDT/c or the MIPS Tool Chain.

Remote File Access: Connects target with remote host file system allowing file transfer between target and host.

Trace Facility: Traces the memory accesses of a user program. Provides for tracing the path of execution reads from and writes to memory. Trace qualifiers allow the tracing of a specific instruction or class of instructions. Also specific memory ranges may be specified. The user may stop tracing on the following conditions: Trace buffer full, hitting a breakpoint, executing a specific instruction or accessing a specific memory range. The trace buffer contents may be displayed using standard R3000 family mnemonics.



IDT/sim Memory Map

The figure above shows the memory utilized by IDT/sim. The EPROM space starts at virtual address bfc00000, which is the R3000's start-up address. The compiled version of IDT/sim with all features included occupies about 115KB of EPROM space, and is normally placed in 128KB of EPROM. IDT/sim uses main memory to store interrupt vectors, variables, and a stack. 71KB of RAM space is reserved for this data.

IDT/SIM COMMANDS

asm <addr> **Examine and change memory interactively using standard assembler mnemonics.**

brk|b [addresslist] Set/display Breakpoints.

cacheflush/cf [-i|-d] Flush I-cache and /or D-cache.

call|ca <address> [arg1 arg2 ... arg8] Call Subroutine with up to 8 arguments.

checksum|cs [start_addr num_bytes] Display the checksums for an address range.

compare|cp [-w|-b|-h] <RANGE> <destination> Compare the block of memory specified by *RANGE* to the block of memory that starts at *destination.*

cont|c Continues execution of the client process from where it last halted execution.

dbgint|di [<-e|-d DEV>] Debug interrupt enable/disable - allows 'break key' to generate external interrupt.

debug|db [DEV] Enter remote debug mode.

dis <RANGE> Disassemble target memory specified by *RANGE.*

disptag|dt [-i] RANGE Displays the instruction or data cache tag values and data contents.

dr [reg#|name\reg_group] Dump the current contents of register(s).

dt Dump the trace buffer.

dump|d [-w|-h] <RANGE> Dump the memory specified by *RANGE* to the display .

enable DEVICE Connect to remote host for file access

fill|f [-w|-h|-b|-l|-r] <RANGE> [value_list] Fills memory specified by range with *value_list.*

fr [-s|-d] <reg#|name> <value> Fill <reg#name> with <value>.

go|g [-n] <address> Start execution at address <address>.

gotill|gt <address> Continue execution until address <address>.

help|? [commandlist] This command will print out a list of the commands available in the monitor. If a command list is supplied, only the syntax for the commands in the list is displayed.

history|h Display last 16 commands entered.

idb [DEVICE] Connect to remote host source level debugger.init|i Initialize prom monitor (warm reset).

load|l [options] DEV Download code to target.

move|m [-w|-b|-h] <RANGE> <destination> Move the block of memory specified by *RANGE* to the address specified by *destination.*

next|n [count] Step over subroutine calls.

rad [-o|-d|-h] Set the default radix to the requested base.

rc [-i] [-w|-b|-h] <RANGE> Isolate and read from cache.

rdfile <filename> <RANGE> Read file from remote host file system.

regsel|rs [-c|-h] Select either the compiler names or the hardware names for registers.

search|sr [-w|-b|-h] <RANGE> <value> [mask] Search area of memory for value.

seg [-0|-1|-2|-u] Set the default segment to the requested k-segment.

setbaud|sb DEV Set the baud rate on a serial channel.

step|s [count] Single step count times.

sub [-w|-h|-b|-l|-r] <address> Examine and change memory interactively.

t {-a/-o/-e/-d/-r RANGE/-w RANGE/-c RANGE/-i INS/-m MSK} Trace command.

tc [-e BPNUM] [-d BPNUM] Trace conditionally command.

te [DEV] Connects the console port straight through to a second serial port.

tex [RANGE] Exclude tracing calls to RANGE.

tlbdump|td [RANGE] Dumps the contents of the TLB.

tlbflush|tf [RANGE] Invalidates the contents of the TLB.

tlbmap|tm [-i index] [-ndgv] <vaddress> <paddress> Virtual to physical mapping of the TLB.

tlbpid|ti [pid] Set/display TLB PID.

tlbptov|tp <physaddr> Probe the TLB.

ts [-b/-f/-o/-r RANGE/-w RANGE/-i INS/-m MSK] Stop trace command.

unbrk|ub <bpnumlist> Clear breakpoints.

wc [-i] [-w|-b|-h] <RANGE> [value_list] Isolate and write to I or D cache.

wtfile <filename> [value_list] Write file to remote host file system.

LIST OF RUN TIME SUPPORT ENTRY POINTS

_exit
atob
clear_cache
cli
close
exc_utlb_code
flush_cache
get_mem_conf
get_range
getchar
gets
install_command
install_immediate_int
install_new_dev
install_normal_int
ioctl
longjmp
open
printf
putchar
puts
rclose*
read*
reinit
reset
restart
rfileinit*
rgets*
rlseek*
ropen*
rprintf*
rread*
rwrite*
set_mem-conf
setjmp
showcar
sprintf*
strcat
strcmp
strcpy
strlen
tokenize
write

* New in Version 4.0

DEVICE DRIVERS (INCLUDED IN SOURCE CODE)

68681/2681 DUART

8530 SCC

SCSI

Centronics Parallel

8254 Timer/Counter

8251 UART

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ORDERING INFORMATION

To upgrade an IDT board level product, see the EPROM order codes below. To order IDT/sim in source code, order the Internal Use License AND order the software on the appropriate source media. You may also order binary distribution rights for the run-time version of the monitor. Ask your IDT sales office for information.

Licenses

Internal Source License 7RS901SLV
Permits purchase of up to six copies of source code (any media combination) and use of source code to develop run-time binaries on up to six machines at a time, but does not permit inclusion of the run time code in an end product. Also purchase one or more of the Source Media listed below.

Limited Binary Distribution Rights 7RS901BLP-L
Extension to Internal Source License to permit inclusion of binary code into end product. Internal Source License must be referenced on order or ordered simultaneously. This license permits up to 100 copies to be distributed royalty-free. For additional copies purchase the Unlimited Binary Distribution Rights .

UnLimited Binary Distribution Rights 7RS901BLU-L
Extension to Limited Binary Distribution Rights to allow unlimited distribution of binary code. Internal Source License and Limited Binary Distribution Rights must be referenced on order or ordered simultaneously.

Maintenance Agreement 7RS901SSY
One year free updates. We supply a direct telephone contact for support.

Source Media

IDT/sim source code can be compiled with either the MIPS C compiler or with IDT/c version 4.1 or later. Earlier versions of IDT/c cannot compile this code. The products listed below are media only and must be purchased with license 7RS901SLV above.

Source for 386/486 PC, MS-DOS 7RS901SBF-L
Compile with IDT/c C-Compiler. Shipped with both 1.2 MB 5.25" and 1.44 MB 3.5" diskettes.

Source for 386/486 PC, SCO Xenix 7RS901SXX-L
Use with IDT/c C-Compiler. Shipped with both 1.2 MB 5.25" and 1.44 MB 3.5" diskettes.

Source for IDT MacStation, on Mac Disc 7RS901SMD-L
Use with MIPS C Compiler supplied with MacStation or with IDT/c.

Source for MIPS / SUN machines, on DC6150 QIC TAR Tape 7RS901SUU-L
Use with MIPS C Compiler or with IDT/c.

EPROM Versions

The following versions of IDT/sim are supplied in EPROMs for the indicated hardware. These versions are for updating the hardware to the latest version of the monitor. No license required. An upgrade is NOT available for the 7RS382 and 7RS383 Evaluation Boards.

For Any 7RS30x, 7RS40x Prototyping System 7RS901BAP
For 7RS388 Real8™ Laser Printer Controller 7RS901BFP
For 7RS385 Evaluation Board 7RS901BGP

Integrated Device Technology, Inc.

IDT/c™ Multi-Host C-Compiler System

IDT7RS903

FEATURES:

- **ANSI C-compiler, Optimizing Scheduler, Assembler, Linker, Librarian, and ANSI Libraries**
- **Efficient Floating Point Emulation Mode for systems without hardware FPU. Includes Transcendentals**
- **Symbolic and assembly level debug support.**
- **Versions available for 80386 machines under MS-DOS™, MIPS machines and MacStation under RISC/os, and Sun SparcStation**
- **Provides control over multiple memory segments**
- **Supports entire IDT family of MIPS ISA Processors (R3000, R3001, R3051/2, R3081, and R3500)**

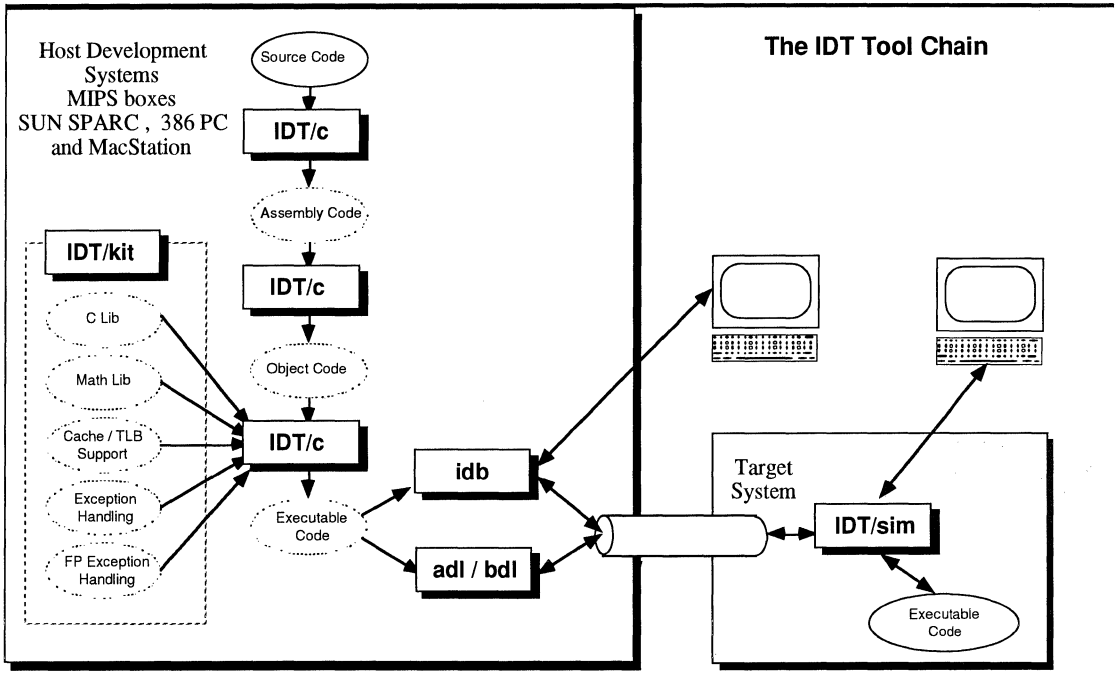
OPTIMIZING C-COMPILER SYSTEM:

IDT/c is C compiler system for the MIPS R3000 and derivatives, specifically designed for developing and debugging code that runs on a remote target. The compiler system includes the GNU C compiler, an assembler with instruction optimization, a linker, a librarian, and a symbolic debugger. A complete floating point emulation library is included also.

The IDT/c package is available for execution on 386 machines under MS-DOS, on the MIPS and SUN workstations, and on IDT's MacStation.

Unique features of IDT/c include the ability to divide code into segments for programming ROMs, the ability to relocate initialized variables into ROM space, extremely efficient floating point emulation (up to ten times faster than other emulation methods), and a programming language in the symbolic debugger to control execution by testing data and addresses in the program.

New features in release 4.1 of IDT/c include the symbolic debug facility, a switch to produce assembly language output for the MIPS tool chain, and a full set of transcendental arithmetic functions.



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OVERVIEW

The IDT/c C-Compiler System is a complete development package for CPUs based on the R3000 architecture. It contains an optimizing cross compiler, optimizing scheduler, assembler, linker, and a downloader. The 'C' compiler is compliant with ANSI 'C' standard and performs the optimizations available in state-o-the-art 'C' compilers. The assembler supports the R3000 machine instructions and architecture described in the book by Gerry Kane, "MIPS RISC Architecture", including both native and synthetic instructions. The complete IDT/c package runs on a variety of host machines and operating systems and is compatible with other IDT development software, such as IDT/sim and IDT/kit.

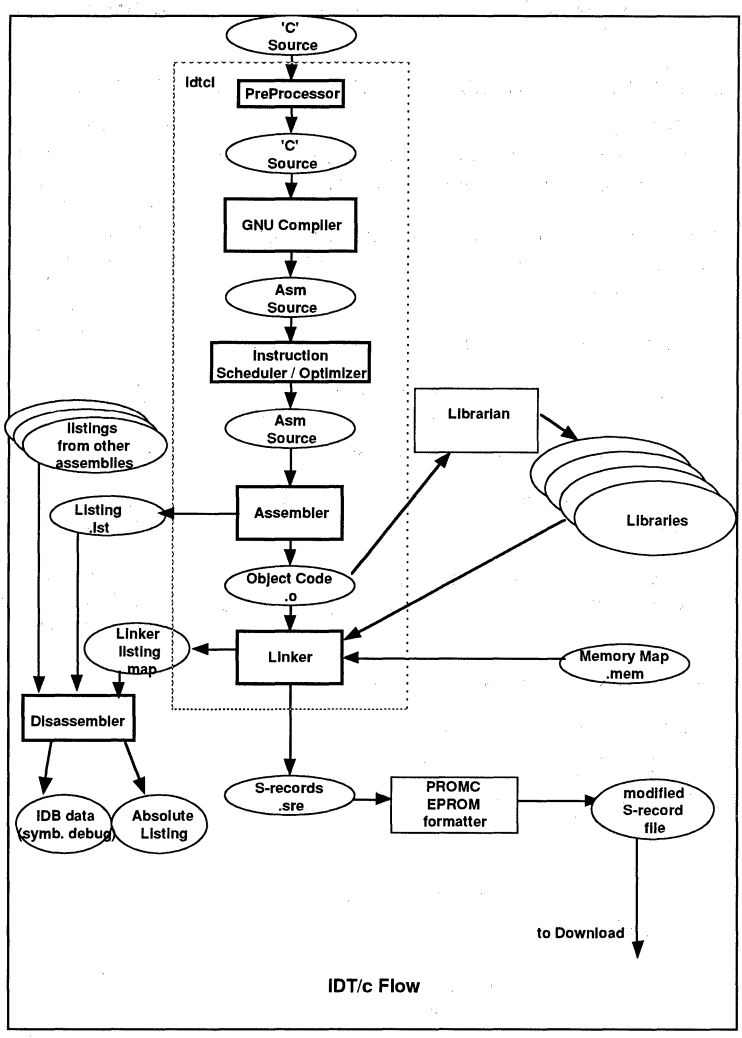
Compiler

The C pre-processor is GNU cpp and the compiler itself is based on GNU C. All C-preprocessing features are supported. The combination of the compiler and assembler included in IDT/c has been tested for compliance to the ANSI C standard using the Plum Hall test suite. The C compiler performs extensive optimization in multiple passes through the code. Switches can be used to fine tune the optimizations.

The output of the compiler is an assembly language file. For the version of IDT/c that runs on the MIPS workstation, a switch selects whether output is for the IDT assembler or for the MIPS assembler. If the MIPS assembler output is chosen, then modules compiled by IDT/c can be assembled and linked in the MIPS environment with modules compiled by the MIPS compiler. IDT/c is far more efficient than MIPS c for floating point emulation. The MIPS compatibility switch makes it possible to use IDT/c only for modules with floating point code, and MIPS c for everything else.

Optimizing Scheduler and Assembler

The IDT assembler implements the R3000 native instruction set as well as the augmented synthetic instructions defined in the "MIPS RISC ARCHITECTURE" book by Gerry Kane. An optimizing scheduler first expands the synthetic instructions into the native instruction set. It then rearranges code to take advantage of R3000 pipeline architecture. The scheduler also analyzes loads of static constants and tries to make use of previously loaded constants. The assembler produces .o files which can be linked together with other files to produce an executable file.



IDT/c Flow

Memory Description File

The memory description file is used to instruct the linker where to place object modules in the R3000 memory map. It tells the linker what address classes are legal, what addresses exist within those classes, and what addresses should be written to output files. The file consists of a sequence of class specifications (CODE, DATA, etc.) and associated address ranges. It is possible to control placement of individual modules.

Linker

The linker combines separately assembled program files into one object module. Command line switches may be used to override the memory description file.

There are three types of output file formats supported: S-Records, Intel hex, and binary image. The S-Record files are useful in down-loading to target boards. The hex format file is useful for EPROM programming because the code can be divided into multiple files under this format. S-Records can be downloaded to a target containing the IDT/sim monitor using a supplied download utility (DOS) or uucp (UNIX). Additionally, the IDB facilities in IDT/sim v 4.0 and IDT/c v 4.1 provide fast, reliable download of S-Records.

Endianess

IDT/c includes a switch so that code may be compiled in either Big-endian or Little-endian format.

Floating Point Library

IDT/c includes a floating point emulation library. A switch in the compiler is set at compile time to determine how the compiler should handle floating point instructions. In the normal mode, it will produce R3010 Floating Point Accelerator instructions in the object code. If the switch is set the other way, the compiler will insert calls to the floating point library instead, and the floating point library must be available at link time. Because the compiler knows about the library during compile time, it can perform optimizations not otherwise possible and minimize the execution penalty for using software instead of hardware.

Librarian

IDT/c supports object code library files. Many compiled routines may stored in a single library file by using the Librarian utility. At link time, the linker extracts only the routines actually used. This technique reduces the number of files that must be dealt with explicitly during program development.

PROM-C

PROM-C is a utility included with IDT/c that permits variables initialized by the program to be moved from their normal locations in the object code into designated memory space destined for EPROM. The user program can execute a simple routine at start-up to move the variables from EPROM back into RAM space at the appropriate locations.

TYPICAL COMPILATION SEQUENCE

Assume 4 C modules, m0.c m1.c m2.c m3.c . m0.c contains 'main' function.

Compile the programs:

```
idtcl -O -c -ZA m0.c m1.c m2.c m3.c
```

(the default compiler mode determined at installation time is used)

Make a library:

```
ilib -c lib.a m1.o m2.o m3.o
```

Link it all :

```
idtcl -o prog -ZT80020000 -ZD80030000 m0.o lib.a
```

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IDB - SYMBOLIC REMOTE DEBUGGER

Remote debugging differs from the 'conventional' in several ways. The control of target program relies on communication line and debugging agent on the target instead of using o/s signals and related services.

Idb was specifically designed to work with IDT/sim to provide full control of the target program. The distinguishing features are: a program mode in which idb executes scripts that contain debugging and flow control commands; and host file services which provide target program with full access to host files. The required physical link between host and target is a single RS232 line capable of 19200 bps.

It is also possible to use direct low-level IDT/sim debugging from an idb session.

Program mode

The script sample on page 6 (last page) illustrates some of capabilities of the program mode.

Remote file services

IDB supports file open, close, read, write, seek; printf; and gets commands in the standard C library format.

FLOATING POINT EMULATION MODE

When floating point and double length variables are used in C programs, compilers usually produce assembly instructions that directly operate on floating point arguments. Most of the time this also requires use of designated register set to hold floating point operands. The C compiler is aware of underlying hardware and attempts to produce optimal code by using all available resources.

The R3000 architecture has the floating point coprocessor in separate chip (R3010). There are numerous floating point instructions that operate on the 32 floating point registers inside the R3010. When floating point hardware is not present — for example, an R3000 without the R3010, or an R3051 or R3052 controller chip — executing programs that use floating point arithmetic requires software that can compensate for the missing hardware. There are two basic solutions to this problem: trapping on the floating point instructions at execution time, and simulating the FPU in software in the trap handler; and modifying the compiler so that it does not produce any instructions for the FPU in its output.

Using the operating environment to trap all attempts to execute instructions on (non-existent) floating point hardware offers the advantage of using a single object code version of the application whether hardware FPU is present or not. The disadvantage is that the complete FPU state machine must be emulated to the last detail since the code produced by the C compiler expects the real hardware to be present. The code that must be executed for each FP instruction is substantial: the trapping overhead for each FP instruction, the maintenance of the FP state machine, and the instructions to execute the required FP operation on integer hardware.

For example, the sequence below requires 3 traps, each of which involves saving all the registers used in the particular trap routine, maintaining the state of the 'virtual' FP register set somewhere in memory, performing the actual FP arithmetic (double addition), and updating the 'virtual' FPU status register bits.

```
lwc1        $f14, ($9)
lwc1        $f15, 4($9)
add.d       $f8, $f14, $f6
```

The solution implemented in IDT/c is to switch the compiler to a different mode for the two environments. In emulation mode, the compiler does not assume presence of any additional hardware, so only R3000 instructions are produced, and FP operations are performed by calls to special routines. The calls are compiler-generated and there is absolutely no difference on the C source level. The same C program that generated the example above would generate the following code in IDT/c emulation mode.

```
lw          $4, ($9)
lw          $5, 4($9)
jal         __adddf3
```

The only overhead is that of performing FP operations on R3000. On floating point intensive applications, IDT/c typically yields execution times four to five times slower than R3010 execution times, but eight to twelve time faster than the FP hardware emulation method described above.

IDT/C PERFORMANCE

The performance of IDT/c has been measured against the MIPS C compiler, which is a well-respected tool chain offering the highest performance on RISC machines.

Floating Point Emulation

Table 1 shows the relative performance of a floating point intensive program under three different floating point options. The hardware in all three cases was the the 7RS388 Laser Printer controller board. This board uses the R3000, the R3010, and 16KB each of Instruction and Data cache. The board was operating at 25MHz.

Bnchmrk	Hardware	Trap Emulation	IDT/c Emulation
add.s	5	1345	25
sub.s	5	1340	25
mul.s	5	1320	25
div.s	10	1830	55
sin.s	55	23490	430
cos.s	55	23650	440
ln.s	40	19045	580
sqrt.s	60	10480	235
add.d	5	2290	35
sub.d	5	2310	40
mul.d	10	2315	50
div.d	10	2485	110
sin.d	55	23295	390
cos.d	55	23535	350
ln.d	45	18930	560
sqrt.d	70	10380	220

Table 1. IDT/c FP Emulation Performance

- The column labeled "Hardware" shows the results of a MIPS C compilation using hardware FPA instructions.
- The column labeled "Trap Emulation" shows the same binary run in the same system with no hardware FPA. The operating system traps on the R3010 instructions, and the trap handler emulates the R3010 hardware in software.
- The last column shows the results for IDT/c Emulation mode. In this test, the code was re-compiled with IDT/c in FP Emulation Mode. Whenever a floating point operation is required, the compiler generates a call to the appropriate library routine to perform the function. There is no trap overhead.

Integer Comparisons

Table 2 illustrates the results of a set of benchmarks compiled by both the IDT/c and MIPS "C" compilers. These benchmarks are commonly referred to as "The Intel Benchmark Suite", since Intel introduced them to measure the performance of various embedded processors began when they announced the i960CA.

Benchmark	MIPS C	IDT/c
Anneal	5200	5340
BubbleSort	448	542
Dhrystone	38,461	35,714
MatMult	1920	2710
PI-500	1140	1540
QuickSort	392	477

Table 2. IDT/c vs. MIPS C on Intel Benchmarks

Table 3 may be more representative of the range of differences, as the Stanford Benchmark suite tends to exercise more of the processor.

Benchmark	MIPS C	IDT/c
Perm	.059	.067
Towers	.061	.066
Queens	.039	.043
IntMatMult	.083	.089
Puzzle	.311	.396
QuickSort	.040	.047
BubbleSort	.044	.054

Table 3. IDT/c vs. MIPS C on Stanford Benchmarks

The results indicate a variety of performance differences between IDT/c and MIPS "C" across these benchmarks. Note, however, that these benchmarks may not be fully representative of either compiler, as they are extremely small programs using only integer arithmetic.

Note that the performance difference between these compilers is different across different hardware platforms. Specifically, the ability of the benchmark to remain cache resident will influence the performance gain of MIPS techniques such as procedure inlining and loop unrolling. Systems with differing cache sizes and/or memory latency may then show different results for integer code.

Mix and Match Strategy

To maximize performance, a system designer could choose to use a "mix and match" strategy in the software toolchain. For example, the bulk of the application could be compiled using the MIPS compiler, while IDT/c is utilized in the floating point intensive portions of the code.

This approach marries the best of both toolchains. The MIPS compiler extracts maximum performance from the majority of the integer only code, while IDT/c does the best job of performing floating point operations in software.

IDT/c facilitates this approach by allowing IDT/c to use the MIPS backend assembler, thus allowing code generated by IDT/c to be directly linked with code generated by the MIPS compiler. Thus, the programmer can use IDT/c (with the MIPS backend assembler) on the floating point intensive code, and the MIPS compiler on the rest of the code.

Table 4 illustrates the performance gain achievable when using such a mix and match strategy. In this table, two of the Stanford Benchmarks are shown with an IDT/c only, and with a mix and match strategy.

Benchmark	IDT/c	Mix and Match
Mn	.277	.267
FFT	.327	.303

Table 4. IDT/c with IDT/c back-end vs. MIPS back-end

7

```
1>bp foo1
2>bp foo2
10>c                                continue
20>if $cb .eq. 1 then 50            if stopped in foo1 just
                                      record the stack pointer
                                      value
30>if $cb .eq. 2 then 60            if in foo2 goto 60
40>stop                             stopped somewhere else (not
                                      in foo1 or foo2)
50>$stack = $29
55>goto 10
60>if $29 .gt. $stack then 10       continue
70>ub 1                             stack is too low. remove
75>ub 2                             bp 1 and bp 2.
80>bp int_handler                   set breakpoint in
                                      int_handler
90>c                                continue
100>if $cb .ne. 1 then 40           not in int_handler
110>if $29 .gt. 0xa0060000 then 90
                                    not dangerously low
120>if $4 .gt. 10 then 200          int_handler should never be
                                      called with the first arg
                                      greater then 10
130>stop
200>ar                              display argument
210>stop
```

Sample Program in IDB Control Language
This example monitors stack depth difference in two routines and if positive starts to trace stack values in the third routine.

ORDERING INFORMATION

The IDT/c C-Compiler is an efficient R3000 C-compiler system based on the popular GNU C and hosted on a variety of computers. The IDT/c system includes the compiler, assembler, scheduler and linker. All PC versions of the software are shipped with both 1.2 MB floppy discs and 1.44MB 3.5" diskettes. A "boxtop" single user license is included with the product. Contact your IDT sales office for multiple user licensing.

Media, with Floating Point Library

The software listed below includes the floating point library.

For 386/486 machine, MS-DOS **7RS903FBBF-N**
This product uses extended memory space on the 386. 4 MB recommended.

For 386/486 machine, SCO Xenix **7RS903FBXX-N**

For MIPS machine RISC/os, on DC6150 QIC TAR Tape **7RS903FBUU-N**

For MacStation, on Macintosh Disc **7RS903FBMD-N**
Runs on MacStation R3000 board under IDT/ux.

For SUN Sparcstation, on DC6150 QIC TAR tape **7RS903FBWU-N**

Integrated Device Technology, Inc.

IDT/kit™ KERNEL INTEGRATION TOOLKIT

IDT7RS909

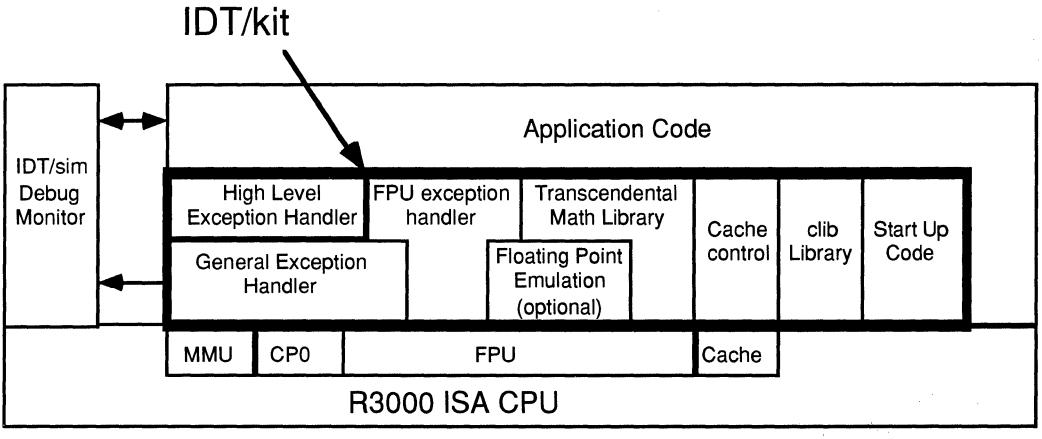
FEATURES:

- **Source code and object code versions of commonly used routines for an R3000 ISA CPU**
- **Start-Up Code to initialize CPU, MMU, and C runtime environment**
- **Cache control code to size, initialize, flush, and clear for DMA**
- **Re-entrant Exception Handler**
- **Floating Point Emulation Library and Transcendental Math Functions**
- **ANSI Standard C Library**
- **Time Support Functions**
- **MicroMonitor for initial hardware debug**
- **Interface Library to IDT/sim™ monitor**

ESSENTIAL CODE FOR R30XX SYSTEMS

IDT/kit (Kernal Integration Toolkit) consists of libraries and routines for important system software operations for R3000-based CPUs. Modules are provided for initializing systems, handling interrupts, servicing floating point exceptions, and many other other common operations. Libraries are included for floating point emulation, transcendental arithmetic routines, and ANSI standard C functions. All IDT/kit libraries are supplied in source code (C and assembly) and in object modules compiled for both little- and big-endian systems and for both hardware and software emulation floating point.

IDT's MicroMonitor is also included in the IDT/kit package. The MicroMonitor is a very simple monitor for initial debug of new hardware. It requires only that the CPU, EPROM, and a serial port be operational. The MicroMonitor can be an invaluable aid for detecting state machine problems in first article hardware.



Schematic Representation of the modules in IDT/kit, showing how they control parts of the R3000 CPU and connect to IDT/sim, IDT's debug monitor.

7

IDT/KIT™ FEATURES

The IDT Kernel Integration Toolkit (IDT/kit) consists of a set of libraries ready to be linked with user developed code. IDT/kit contains functions that would normally be furnished by an operating system like UNIX but without the overhead. Functions are provided for initializing the system, memory management, exception handling and time support; an ANSI standard 'C' library and a math library with transcendental functions are supplied.

This environment can be compiled with IDT/c or MIPS compilers, Big or Little Endian, Cached or Uncached and with an optional Emulation Mode if no Floating Point Accelerator is installed. With IDT/kit, floating point emulation support is transparent to the user application.

IDT/kit typically would co-exist with IDT/sim and become part of a total development and debug environment. On a system where IDT/sim is installed, all the commands, entry points and debugging facilities of IDT/sim are available to the Kernel Integration Toolkit. When using IDT/sim, IDT/kit filters exceptions first. If IDT/kit does not handle an exception, then it is passed to IDT/sim.

Default exception handlers intercept exceptions, save the environment, preserve the Exception Registers for later analysis, restore the environment and return to continue program execution. The default handlers can easily be replaced or extended with more robust handlers written by the user.

IDT/kit relieves the application from the low level tweaking necessary to get started but leaves easy hooks into the system for expansion and polishing as the development progresses. All code is supplied in source code (C and assembly), to allow easy access for modifications needed to tailor the system to specific needs. This allows the programmer to shorten the project development time by the 2 to 3 months required to understand and service the R3000 ISA resources like cache, MMU and exception handling.

IDT/kit includes IDT's MicroMonitor, a very simple monitor for performing the initial debugging of new hardware. The only hardware which must be functioning to run the MicroMonitor is the CPU, EPROM and a serial port function. This allows for immediate debugging of hardware even when the DRAM memory is not functioning.

IDT/KIT COMPONENTS

1. MICROMONITOR:

A small assembly language monitor to aid in debugging the hardware design. The MicroMonitor requires only that three hardware resources are functional: the CPU can execute instructions, the EPROM can provide instructions and the UART can send and receive characters.

2. IDT_CSU.S, THE START UP MODULE

Supplies the initialization and set up code necessary for operation of the system.

- initialize the Status Register
  a) clear parity error bit
  b) set Coprocessor 1 usable bit correctly
  c) clear all IntMasks enabled
  d) set kernel/user mode
- set Cause Register
  a) clear software Interrupts Pending
- clear bss area
- establish temporary uncached user stack
- determine memory and cache sizes
- establish permanent stack at Top of Memory
- flush I and D-Caches
- if there is a Translation Lookaside Buffer invalidate it
- initialize library if IDT's standard C Library is used
- initialize exception handlers
- jmp to users' main()

3. LIBIKIL.A, KERNEL INTEGRATION LIBRARY:

The IDT Kernel Integration Library (libikil.a) is a library which can be linked to user programs to supply functions required to support the environment of the R3000 ISA family. This library is divided into four sections: Memory Handling, General Exception Handling, Floating Point Exception Handling and Time Support Functions.

a. memory handling - the full range of functions necessary to manage main memory, cached memory and the Translate Lookaside Buffers
b. general exception handling - the functions used in enabling and handling any interrupt exceptions, hardware or software, asserted by the CPU
c. floating point exception handling - provides the support for the Floating Point Unit, the R3010, or for Emulation Software for floating point arithmetic , "strongly recommended" by the IEEE Standard 754-1985. It is transparent to the application code calling this interface whether hardware or software emulation is being employed.
d. Time support functions using the 8254 timer as a prototype

4. LIBILNK.A, THE IDT/SIM INTERFACE LIBRARY:

the IDT/sim linking module which interfaces with all the functions available with IDT/sim not defined with IDT/kit or by the user

5. LIBIC.A, ANSI STANDARD C LIBRARY:

The IDT Standard C Library (**libic.a**) is a standard archive library which, when linked with the users' filename.o files, provides the functions defined by the ANSI standard including standard I/O, String and Character functions, Utility functions, and memory allocation functions.

6. LIBIMATH.A, MATHEMATICS LIBRARY:

The IDT Math Library (**libimath.a**) is a standard archive library which, when linked with the users' filename.o files, provides the transcendental functions required for standard math processing. Whether hardware floating point or software emulation is be used is transparent to the application code calling this library.

7. UTILITIES:

Three utilities that execute under MIPS RISC/os are supplied to convert from compiler output from the MIPS coff file format to an S-record format and to downloading the S-records to a target board in either ASCII or binary forms. These utilities are need only for users of the MIPS C-compiler who do not have IDT/sim or MIPS SPP/e.

HOW IDT/KIT IS USED

IDT's Kernel Integration Toolkit includes a robust set of tools for the embedded controller developer. They are "packaged" in accessible, modular containers, the IDT/kit libraries. The four libraries, arranged by function, supply most of the routines required by RISC applications. Only those libraries needed to resolve function calls must be entered on the link command line; the others are never accessed which establishes a fully modular environment.

IDT/kit serves as an envelope for the installation's application code. The source module, idt_csu.S, is linked first, then the development code and, finally, any kit libraries required to support function calls. This allows the developer to concentrate on the application and not waste resources re-developing the support routines. Although the libraries are provided complete and ready to link, source code for all the functions is also distributed to allow easy examination for information or as a template for additional routines. All the necessary Make/Batch files are included to facilitate any changes, additions or corrections. Some examples:

strcpy (or any of the C library routines) - perhaps your installation has developed a super-algorithm. It isn't quite ANSI Standard but does your job better. Simply edit the source in the clib subdirectory (or replace the one that is there), execute the makefile for your configuration (IDT/c or MIPS, Big or Little Endian, REAL or Emulation Mode) and the library, libic.a, now contains your code. Your module could also be placed on the system Link line before the corresponding library and the call would be resolved before the library is searched.

Interrupt Handling - you want the default interrupt handler (it's already there), but you need an additional flag set. Edit the routine in the killib subdirectory, run the Make/batch file for your configuration (IDT/c or MIPS, Big or Little Endian, REAL or Emulation Mode) and the library, libikil.a, now contains "your "default interrupt handler.

These kinds of simple modifications allow the IDT/kit routines to be tailored for a specific system without expending the time to investigate and understand all the routines; only the section applicable to the application need be tweaked and the Make/Batch files provide easy guidelines for doing it.

IDT/kit FUNCTION LIST

CSU_IDT.S: START UP MODULE

start() ---------- Startup routine

LIBIKIL.A: KERNEL INTEGRATION LIBRARY

Programmable interval timer driver

install_timer_driver() install timer driver
i8254init() ---------- timer driver init
i8254open() ---------- opens the device
i8254ioctl() ---------- i/o control function

Assembly level exception handling

disable_int() ---------- clear selected interrupts
enable_int() ---------- set selected interrupts
exc_norm_code() ---- general exception code
exc_utlb_code() ------ UTLB Miss code
exception() ---------- general exception code
init_erc_vecs() -------- init vector code
longjmp() ---------- go to setjmp() point
other_excp() ---------- handles other exception
setjmp() ---------- set setjmp() state

High level exception handling

add_ext_int_func() -- set default exc handler
clr_except_ptr() ------ clears setjmp pointer
config_memory() ----- size of main memory
extern_int() ---------- external interrupt code
exception() ---------- general exception code
get_except_ptr() ----- get execption pointer
init_tlb() ---------- initializes TLB
mem_exc_hdlr() ------ memory exception code
sae_errmsg() ---------- prints msg & exits
set_except_ptr() ------ sets setjmp pointer
spurious_int() --------- unexpected ext interrupt

FPU interface module

fp_defaultHdlr() -------- default handler
fp_disableTrap() ----- clears trap bits in fpcsr
fp_enableTrap() ------ sets trap bits in fpcsr
fp_init() ---------- init floating Point
fp_int() ---------- FP interrupt dispatcher
fp_signal() ---------- user exception handler
fpclr_stickybits() ------ clear sticky bits in fpcsr
fpget_excregs() ------ get Exc Regs
fpget_fpcsr() ---------- get FP Control/Status
fpget_RM() ---------- get rounding mode fpcsr
fpget_stickyBits() ---- get sticky bits fpcsr
fpset_fpcsr() ---------- set FP Control/Status
fpset_RM() ---------- sets rounding mode
fpset_stickyBits() ---- sets sticky bits in fpcsr
fpset_excregs() ------- set Exc Register buffer

Assembly language FPU access

clr_CAUSE() ---------- clears SW bits in CAUSE
get_CAUSE() --------- returns contents of CAUSE
get_fpcsr() ---------- returns FPU csr
get_cp0epc() ---------- gets epc
get_STATUS() -------- status register contents
set_CAUSE() --------- sets CAUSE Register
set_fpcsr() ---------- sets FPU csr

Functions affecting I/D Caches

clear_Dcache() ------- invalidate portion of Dcache
clear_Icache() -------- invalidate portion of Icache
config_Dcache() ----- size of Data cache
config_Icache() ------- size Instruction cache
flush_Dcache() ------- invalidates entire Data cache
flush_Icache() -------- invalidates entire Inst cache
get _mem_conf() ----- gets memory configuration
size_cache() ---------- finds size of cache

Assembly language TLB access

resettlb() ---------- invalidates tlb entry
ret_tlblo() ---------- returns tlb entry lo reg
ret_tlbhi() ---------- returns tlb entry hi reg
ret_tlbpid() ---------- returns tlb process ID field
set_tlbpid() ---------- sets current tlb pid
tlbprobe() ---------- probes tlb
tlbmapping() ---------- maps tlb entry

Time support module

time_cmd_init() ------- starts clock
time_init() ---------- init timer drvr
timer_int ---------- clock interrupt routine
time() ---------- returns timer tics
time_it() ---------- times the selected function

Assm language Write Buff Routine

wbflush() ---------- flushes the write buffer

LIBILNK: IDT/SIM LINK LIBRARY

Cache Routines

clear_cache() --------- clears portion of I and D
flush_cache() --------- flushes entire I and D

Character Routines

getchar() ---------- inputs a character
putchar() ---------- outputs a character
showchar() ---------- makes character visible

Command Line Interpreter

cli() ---------- Command Line Interpreter
get_range() ---------- parses the range spec
tokenize() ---------- parses the command line

Exit and Reenter Routines

_exit() ---------- exit & return to monitor
promexit() ---------- exit & return to monitor
reinit() ---------- reinitializes monitor
reset() ---------- resets prom monitor
restart() ---------- restarts the debug monitor

Help Screen Routine

help() ---------- prints Help Screen

ROUTINES TO EXTEND IDT/SIM

install_commands() - adds user commands
install_immediate_intnstalls user interrupt
install_new_dev() ---- installs new device
install_normal_int() -- installs user interrupt

Routines for low level I/O

close() ---------- closes an open device
open() ---------- opens a device
read() ---------- reads data from device
write() ---------- writes data to an device

I/O Control Function

ioctl() ---------- sets I/O flags / calls drivers

Routines to save /restore context

longjmp() ----------restores setjmp context
setjmp() ----------saves the current context

Memory configuration routines

get_mem_conf() -----returns mem configuration
set_mem_conf()------sets the mem configuration

Formatting print routine

printf() ----------formatting print routine

Dummy routines for libic

_init_file() ----------dummy file routine
_init_sbrk()----------dummy sbrk routine

String routines

atob() ----------Ascii string convert
gets() ----------gets string function
puts() ----------outputs string to I/O
strcat() ----------concatenates two strings
strcmp()----------compares two strings
strcpy()----------copies one string to another
strlen() ----------returns length of string

LIBIC.A: ANSI STANDARD C LIBRARY

abs() ----------absolute value of integer
atof()----------fp value of an Ascii string
atoi() ----------integer value of Ascii str
atol()----------long value of Ascii str
bsearch()----------binary search of a array
div()----------rem & quot of int division
ferror() ----------error during a file operation?
atexit() ----------routines called at exit time
exit()----------Terminate with status
fopen()----------open file/ret file stream ptr.
fclose()----------close a file
fdopen()----------open stream
labs()----------absolute value of long arg
ldiv()----------rem & quotient of division
free()----------free allocated memory
malloc()----------memory allocation
realloc()----------reallocation of memory
fscanf()----------read data from a file
printf()----------display data on the std I/O
qsort()----------quick sort routine
rand()----------generates random number
srand()----------seed for random num genr
sbrk()----------mem allocation bp routine
scanf()----------read data from standard input
sprintf()----------output data into a string
sscanf()----------read data from a string
memcmp()----------compare two memory arrays
memcpy()----------memory array copy
memmove()----------memory array move
memchr()----------ret ptr to first matched char
memset()----------place a char in memory array
strlen()----------return string length
strcmp()----------strings are identical?
strcpy()----------copy string
strncpy()----------copy n characters of a string
strchr()----------ret ptr to first match of a char
strchr()----------ret ptr to last match of a char
strcat()----------concatenate a strings
strncat()----------concatenate strings
strspn()----------len of prefix of str
strcspn()----------len of prefix of str
strpbrk()----------ptr to first occur of any char
strstr()----------string a occurs in string b?
strtok()----------return tokens
strtod()----------convert string to a double
strtol()----------convert string to long int

LIBIMATH.A: TRANSCENDENTAL MATH LIBRARY

acosh()----------inv hyperbolic cosine of x
acos()----------cos -1 (x)
asin()----------sin -1(x)
asinh()----------inverse hyperbolic sine of x
atan()----------tan -1 (x)
atan2()----------tan -1 (x/y)
atan2()----------tan -1 (x/y)
atanh()----------inv hyperbolic tangent of x
cabs()----------complex absolute value
exp()----------exponential function e^x
hypot()----------sqrt (x*x + y*y)
z_abs()----------double-complex absolute
cbrt()----------cube root of x
cosh()----------hyperbolic cosine of x
exp()----------exponential function e^x
expm1()----------exponent (x - 1)
ceil()----------smallest int not < x, double
floor()----------largest int not > x, double
rint()----------nearest x in dir of round
fmod()----------fp remof x/y, sign of x
atan()----------tan -1 (x)
cos()----------cos of x
exp()----------exponential function e^x
log()----------natural logarithm ln(x), x>0
log10()----------base 10 logarithm, x>0
sin()----------sine of x
sqrt()----------square root of x, x>= 0
tan()----------tan of x
xtoi()----------raises x to integer power, i
sim_fpint()----------simulate IEEE standard trap
sim_unint----------sim FP Unimplemented Op
log()----------natural logarithm ln(x), x>0
log10()----------base 10 logarithm, x>0
log1p()----------log (1 + x)
log__L()----------og(1 + x) -2s/s
pow()----------x^y
cos()----------cos of x
sin()----------sine of x
sinh()----------hyperbolic sine of x
copysign()----------returns x with sign of y
drem()----------x - n*y, integer nearest n
finite()----------1 = real x; 0 = INF or NAN x
logb()----------exponent of x^n
scalb()----------x * (2**n) computed for n
sqrt()----------square root of x, x>= 0
tan()----------tan of x
expm1()----------exponent (x - 1)
tanh()----------hyperbolic tangent of x
fabs()----------absolute value of number
frexp()----------returns mantissa;exp in *ptr
isnan()----------tests for floating point NaN
ldexp()----------returns quantity *2^exp
pow()----------x^y

7

ORDERING INFORMATION

To order the IDT/kit Developer's Package, order the Internal Source License AND order the software on the appropriate source media. The License Agreement is available from your local IDT sales office and is also published in IDT's development tools catalog.

LICENSES

Internal Source License 7RS909SLV
Permits purchase of up to six copies of source code (any media combination) and use of source code to develop run-time binaries on up to six machines at a time, but does not permit inclusion of the run time code in an end product.

Limited Binary Distribution Rights 7RS909BLP-L
Extension to Internal Source License to permit inclusion of binary code into end product. Source License must be referenced on order or ordered simultaneously. This license permits up to 100 copies to be distributed royalty-free. Additional copies are subject to the royalty .

UnLimited Binary Distribution Rights 7RS909BLU-L
Extension to Internal Source License to permit distribution of unlimited number of copies of binaries derived from the code.

MAINTENANCE

Maintenance Agreement 7RS909SSY
One year free updates.

SOURCE MEDIA

IDT/kit source code can be compiled with either the MIPS C compiler or with IDT/c version 3.5 or later. Earlier versions of IDT/c cannot compile this code. The products listed below are media only and must be purchased with license 7RS909SLV above.

Source for 386, MS-DOS 7RS909SBF-L
Compile with IDT/c C-Compiler. Shipped with both 1.2 MB 5.25" and 1.44 MB 3.5" diskettes.

Source for 386 PC, SCO Xenix 7RS909SXX-L
Use with IDT/c C-Compiler.

Source for IDT MacStation, on Mac Disc 7RS909SMD-L
Use with MIPS C Compiler supplied with MacStation or with IDT/c.

Source for MIPS or SPARC machine, DC6150 QIC TAR Tape 7RS909SUU-L
Use with MIPS C Compiler or with IDT/c.

Integrated Device Technology, Inc.

MacStation™ 3 RISC WORKSTATION IN A Macintosh®

IDT7RS503

FEATURES:

- **15 or 25 MIPS RISC Computer Add–In Board for Macintosh II Computers**
- **Includes AT&T UNIX® SVR3 Operating System with BSD 4.3, NFS, X11, and Motif**
- **Supplied with MIPS C-Compiler, Assembler, and Symbolic Debugger**
- **Uses all Macintosh peripherals for I/O**
- **Includes Macintosh-independent SCSI and serial I/O ports**
- **Multifinder and System 7 compatible**
- **Available as add–in board or as completely configured systems**

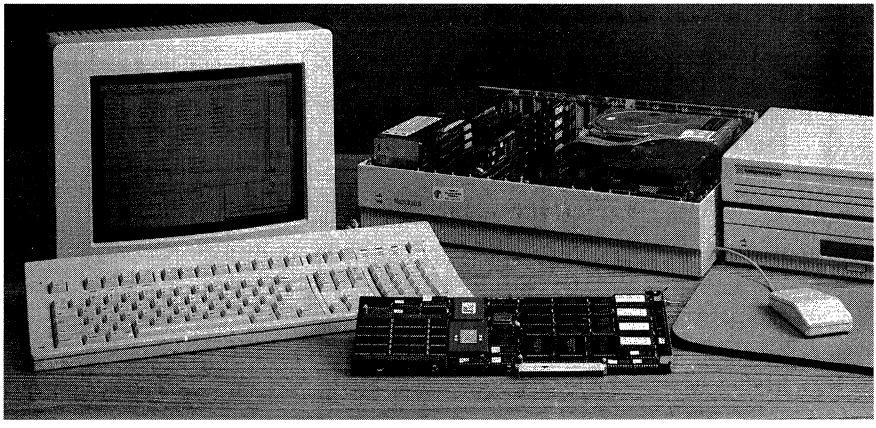
R3000 COMPUTER PLUGS INTO A MACINTOSH II

IDT's MacStation™ 3 is a high performance R3000-based workstation consisting of a MIPS® R3000 RISC CPU board that plugs into a Macintosh II computer, a complete AT&T SVR3 UNIX® operating system, and a collection of Macintosh programs used to communicate between the UNIX and Mac operating systems.

The UNIX software is MIPS RISC/os v 4.5.2, MIPS port of AT&T Unix. It is supplied with TCP/IP, NFS®, X11G3, and Motif. The UNIX software can support multiple user sessions, using either Telnet or X, running one or more Macs or external terminals.

A Macintosh application, IDT/console, is used as a console terminal and I/O handler for the UNIX OS. Opening the application creates a terminal window on the Macintosh from which UNIX can be booted. File I/O commands from UNIX are intercepted by IDT/console, which reads and writes UNIX files encapsulated inside Macintosh files. The encapsulated files can reside on the same disks as Macintosh files without partitioning. With a single command, a file can be moved between the Macintosh and Unix environments. An optionally available package, Intercon's NFS/share™, can be used to mount the Unix files on the Macintosh.

Other Macintosh software includes IDT/envy™, an Extension that provides TCP/IP paths among the Mac, UNIX, and an Ethernet card; NSCS Telnet, a telnet terminal application for the Macintosh; Consulair EDIT, a Macintosh text editing program; and MacTCP.



2891 drw 01

MACSTATION 3 HARDWARE

RISC CPU Card

The MacStation is available with either of two CPU cards. One is approximately 15 MIPS performance, and includes 8MB of local DRAM, 2 serial I/O ports and a SCSI port. The processor on this card runs at 20MHz, and includes 16KB each of Instruction and Data Cache. The other card is approximately 25 MIPS in performance, and includes 16MB of local DRAM, 2 serial I/O ports, and a SCSI port. The processor runs at 25MHz, and includes 64KB each of Instruction and Data Cache.

The SCSI port can be used to connect hard disks with the UNIX file systems on them. This provides higher performance than that available when the Mac's disks are used for the UNIX files.

The serial I/O ports can be used for a separate console terminal or for printers or other common I/O devices. Drivers are included for a number of common devices.

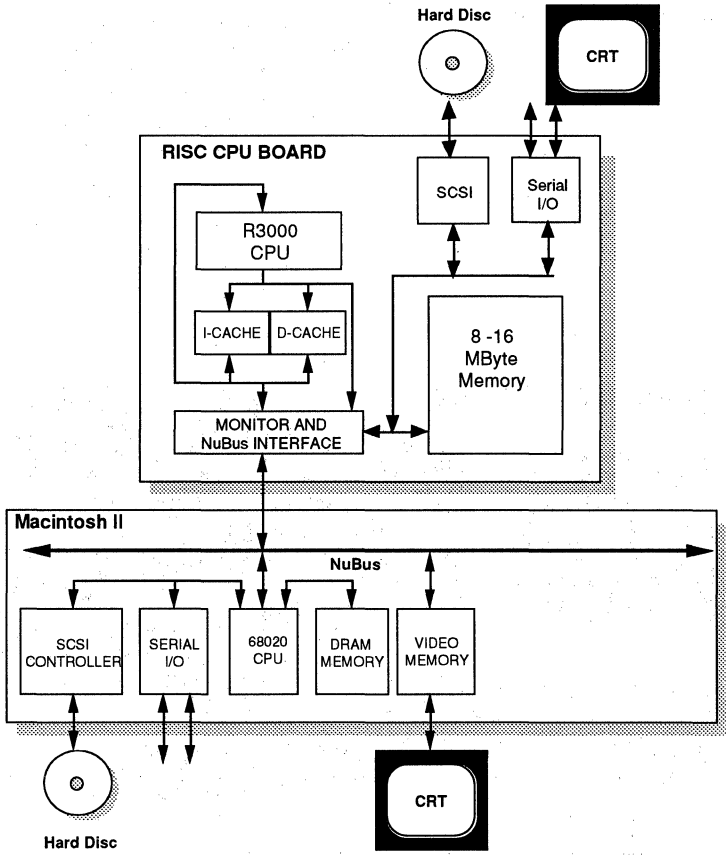
MACSTATION 3 SOFTWARE

UNIX O/S

The UNIX OS is AT&T SVR3 with BSD 4.3 extensions and fast file system. This is a full-featured UNIX, including on-line manuals, SMTP, reconfiguration files, and the MIPS C-compiler. Any application which runs under MIPS RISC/os will run directly on this OS. Ports of other SVR3 applications are easy, but generally require recompiling for the MIPS hardware. The UNIX software includes NFS file sharing services, the X11 library, and Motif (MIPS RISCwindows). The UNIX file systems are encapsulated in Macintosh files and may exist on any number of Mac disks. Swap space is preset to 40 MB, but can be changed easily.

C Compiler

The C compiler included with the MacStation is the MIPS C compiler, noted for extremely efficient optimization of code. A switch in the compiler determines whether K&R or ANSI C is supported.



2891 drw 02

Drivers

Source code is supplied for a number of I/O devices, including terminal, disk, and network. A reconfiguration directory and make files are available to rebuild the kernal with new or modified drivers.

MACINTOSH SOFTWARE

All supplied Macintosh software is compatible with System 6.07 and with System 7.0.

IDT/console

IDT/console is an application that runs on the Macintosh under MultiFinder, and provides a terminal emulation window for the UNIX console, as well as I/O services to UNIX for file systems on Macintosh disks.

MacTCP

This Apple communication tool adds TCP/IP capability to the Macintosh.

IDT/envY

IDT/envY is a Macintosh extension that provides the UNIX and Macintosh sides two different IP addresses, so they can communicate with each other using TCP/IP protocols. This communication takes place over the NuBus, so it is extremely fast and reliable. No Ethernet card is required for the Macintosh-UNIX path. IDT/envY also permits a single Macintosh Ethernet card to serve both CPUs.

Telnet

Telnet is a Macintosh application that opens a terminal window on the Macintosh through which new UNIX sessions can be started. Multiple Telnet windows can be open at once, each running different processes.

EDIT

Consulair EDIT is a Macintosh text editing program, well suited for writing C source code. The text files are easily passed to the Unix side for compilation and debug.

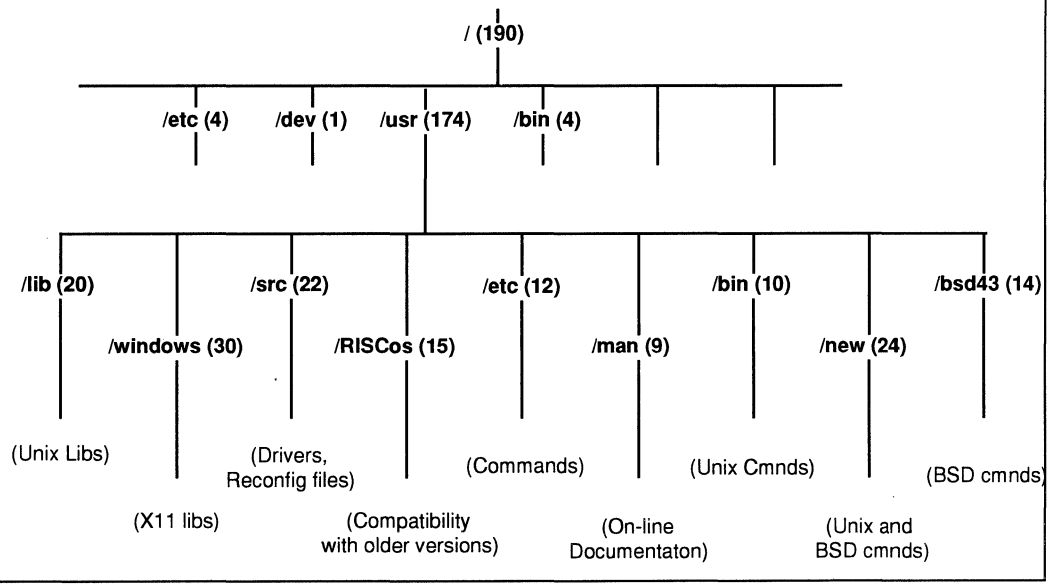
NFS for the Macintosh

NFS communications is included with the UNIX package, so files can be mounted from remote servers. Intercon's NFS/share™ is available as an option on the Macintosh side. NFS/share allows UNIX file systems to be mounted and opened on the Mac like AppleShare volumes.

X–Windows

An X–11 Library and Motif client software is included for the UNIX side. Apple's MacX is available separately for the Macintosh side so that X–windows can be opened on the Macintosh screen.

Major Components of UNIX file systems and approximate size in MBytes.
Swap file (typically 40 MB) not shown



7

Integrated Device Technology, Inc.

CUSTOM AND OFF-THE-SHELF RISC ASSEMBLIES

INTRODUCTION

IDT's RISC Subsystems Division provides design and manufacturing services for subassemblies and complete PC boards using any of the company's RISC CPUs, from the R3051 to the R4000. Several CPU Modules are available as standard off-the-shelf products for either prototype development, for initial software porting, or for use in volume production. Four of IDT's standard R3000-based modules are shown on the following pages.

FOR PROTOTYPE DEVELOPMENT

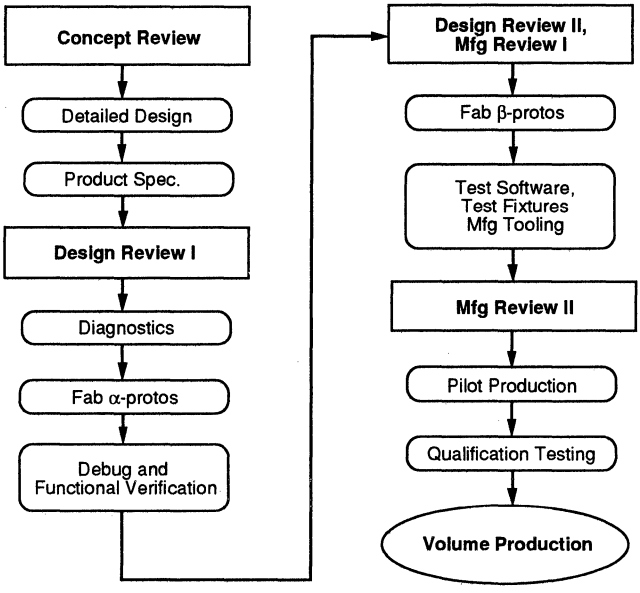
For quick development of systems, use a prototyping platform. There is a completely assembled and tested prototype development platform available for each of IDT's standard CPU modules. These platforms include the module, main memory, EPROM containing IDT/sim debug monitor, serial I/O for control and downloading, and an expansion bus for adding additional hardware to the design. The prototyping platforms require only a 5V supply and a terminal to be operational. Code compiled on the software development system can be downloaded, executed, and debugged.

FOR PRODUCTION

You can design your system around one of the standard CPU modules to save engineering time and simplify manufacturing. The modules are carefully engineered to support the high speeds present around the CPU, and are completely tested and burned-in prior to shipment. To achieve high performance, the modules are typically built using all surface mount components on both sides of an 8 to 14 layer FR-4 PC board. Some modules include ASICs to add features and reduce size. High pin-count and fine-pitch (<20 mil) components are routinely assembled on our production lines. Several different interconnect systems are used to provide reliable connection between the module and the mother board.

CUSTOM MODIFICATION OF STANDARD MODULES

If one of our standard modules isn't exactly what you need, we can make modifications for you. The modifications can be as simple as changing the reset conditions or clock rate, or modifying the on-board state machine behavior. Or we can design a completely new module for to meet your exact specifications. In either case, we will supply you with test hardware and diagnostic software so we can work together to speed your program along.



8

ENGINEERING AND MANUFACTURING SERVICES

Use our Engineering Experience

IDT can design and manufacture board-level products to meet your needs. We have designed and put into production more MIPS-based products than anyone else in the world, ranging from 40 MHz CPU modules to high-volume low-cost embedded controllers based on the 3051.

When you hire IDT to design your board, you take advantage not only of an experienced design team with a fully equipped hardware lab and support staff, but also IDT's extensive software porting and debug experience. Together with your engineers, we will define the optimum architecture, review the detailed design, develop diagnostic tools, and debug the prototype hardware and software. The same team of software engineers that developed IDT's powerful software tools will help get your software running on your own custom hardware.

Production Assembly and Test

Once your design has been completed, IDT will create a complete manufacturing package, and put the product into production in our own PC board assembly plant.

Initial units from the line will be qualified for reliability, manufacturability, and conformance to the product specification. On-going production can then commence with deliveries according to your needs. IDT can manufacture quantities as small as a few hundred per year, or as large as hundreds per week.

Using IDT's manufacturing resources offers the advantages of experienced manufacturing and test personnel, ready access to the development engineers for problem-solving, and close co-ordination with the semiconductor divisions of the company to insure timely delivery of components.

TABLE OF CONTENTS

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Integrated Device Technology, Inc.

R3000 CPU MODULE

IDT7RS109

FEATURES

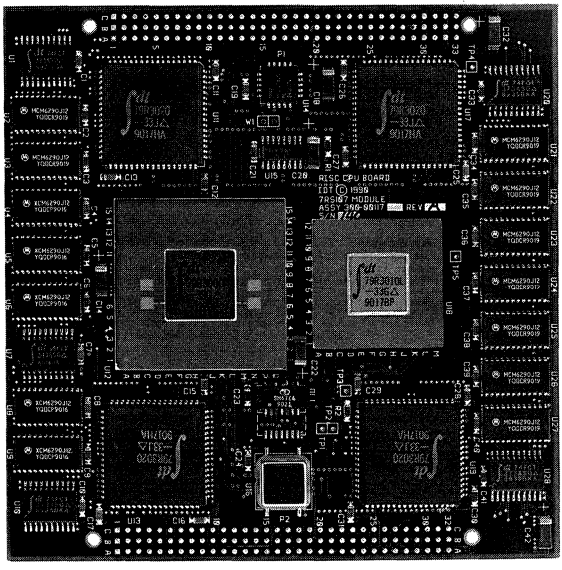
- 64KB each of Instruction and Data Cache
- High Speed: 33MHz
- Includes R3010 Floating Point Accelerator
- 1-word Read Buffer; 4-word Write Buffer
- Supports R3000 Multiprocessor Features
- On-Board Parity Check and Generate
- Four or Eight-word block refills
- On-board oscillator, delay line, and reset circuitry
- 100% burn-in and functional test at rated speed

R3000 MODULE FOR HIGH PERFORMANCE CPUS AND MULTIPROCESSOR SYSTEMS

The IDT7RS109 is a complete reduced instruction set computer (RISC) CPU, based on the MIPS R3000 RISC processor, and supplied on a small fully-tested high-density plug-in module. The module includes the R3000 CPU, the R3010 Floating Point Accelerator, 64kB each of data and instruction cache memory, a single word read buffer and a four-word write buffer. Clock generation, reset, control, parity, and interrupt functions are included on the module to simplify the remainder of the system design.

The 109 module includes a latch to hold an external address for snooping in the D-cache and is designed to support the R3000's multiprocessor features.

The module is constructed using surface mount devices on a 5.2" by 5.2" epoxy laminate board, and is connected to the user's system via 195 pins located in two pin row regions on the board.



7RS109 Module. Actual Size 5.2" x 5.2 "

8

RELATED PRODUCTS

Prototyping System

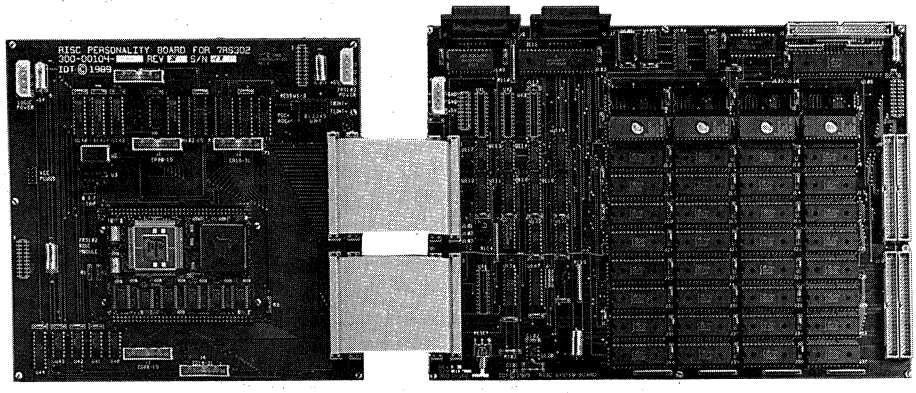
The 7RS109 module can be placed into immediate service using our flexible 7RS409 Prototyping Platform. The system includes a 7RS109 module and two additional boards: a general purpose CPU board, and a personality card that interfaces the module to the CPU board.

The CPU board contains 1MB of main memory, 256kB of EPROM, two RS232 serial ports, an 8254 counter/timer, and an 8-bit parallel port accessible through a dual port RAM. Four 50-pin connectors provide access to all the address, data, and control signals for external connection to additional hardware on, for example, a wire-wrap board.

The system includes IDT's Software Integration Manager, which provides facilities for downloading code, examining memory, and stepping through programs.

The personality card is on a separate board, and provides a bed for the module, necessary control signals, and connectors for an HP16500 Logic Analyzer.

Code for the R3000 can be created on a MIPS development system, on IDT's MacStation™ system, or using IDT's PC-based cross assembler and compiler products. Assembled code can be downloaded into the Prototyping System for execution and debug.



NOTE:
The card on the left is the personality card with a module; the card on the right is the general purpose CPU.

Figure 1. A 7RS409 Prototyping Platform

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Integrated Device Technology, Inc.

R3000 CPU MODULE

IDT7RS110

FEATURES

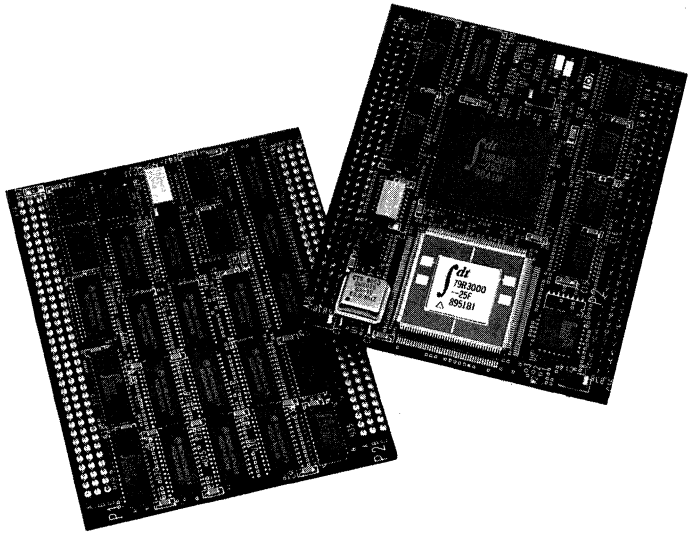
- High Speed: 33MHz
- Small size: 3.3" x 4.1"
- 32KB each of Instruction and Data Cache
- Optional R3010 Floating Point Accelerator
- Single-word Read and Write Buffers
- On-Board Clock, Reset, and Parity Logic
- 100% burn-in and functional test at rated speed

R3000 MODULE FOR GENERAL USE IN SMALL SYSTEMS

The IDT7RS110 is a complete reduced instruction set computer (RISC) SubSystem, based on the MIPS R3000 RISC processor, and supplied on a small fully-tested high-density plug-in module. The size and performance of the 7RS110 make it ideal for embedded aplications such as laser printers and X-terminals. The 7RS110 includes an R3000 Instruction Set CPU, 32kB each of instruction and data cache. a single word read buffer, a single word write buffer and the R3010 Floating Point Accelerator (optional).

Cache misses are handled with single word memory accesses or with eight or sixteen word block refills.

The module is constructed using surface mount devices on a two-sided epoxy laminate board, and is connected to the user's system via six rows of 36 pins each.



7RS110 Module. Actual Size 3.3" x 4.1 "

8

RELATED PRODUCTS

Prototyping System

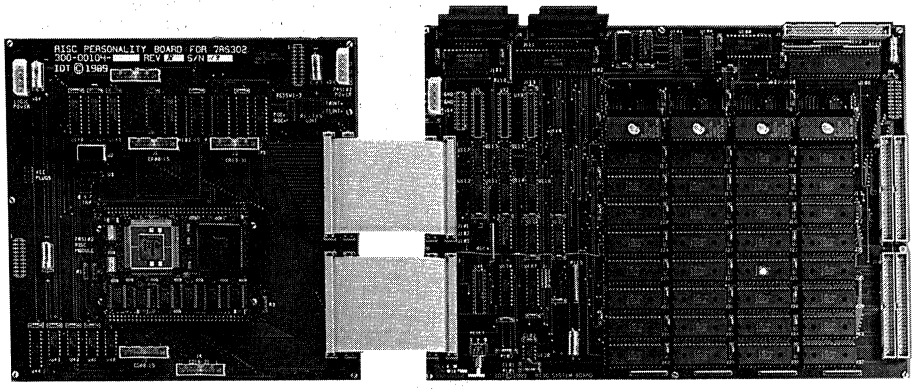
The 7RS110 module can be placed into immediate service using our flexible 7RS410 Prototyping Platform. The system includes a 33MHz 7RS110 module and two additional boards, a general purpose CPU board, and a personality card that interfaces the module to the CPU board.

The CPU board contains 1MB of main memory, 256K of EPROM, two RS232 serial ports, an 8254 counter/timer, and an 8-bit parallel port accessible through a dual port RAM. Four 50-pin connectors provide access to all the address, data, and control signals for external connection to additional hardware on, for example, a wire-wrap board.

The system includes IDT's IDT/sim System Integration Manager, which provides facilities for downloading code, examining memory, and stepping through programs.

The personality card is on a separate board, and provides a bed for the module, necessary control signals, and connectors for an HP16500 Logic Analyzer.

Code for the R3000 can be created on a MIPS development system, on IDT's MacStation™ system, or using IDT/c, IDT's Multi-Host cross compiler product, available for a variety of machines. Assembled code can be downloaded into the Prototyping System for execution and debug.



NOTE:
The card on the left is the personality card with a module; the card on the right is the general purpose CPU.

7RS410 Module Prototyping Platform

ORDERING INFORMATION

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Integrated Device Technology, Inc.

HIGH PERFORMANCE R3000 CPU MODULE

ADVANCE INFORMATION
IDT7RS114

FEATURES

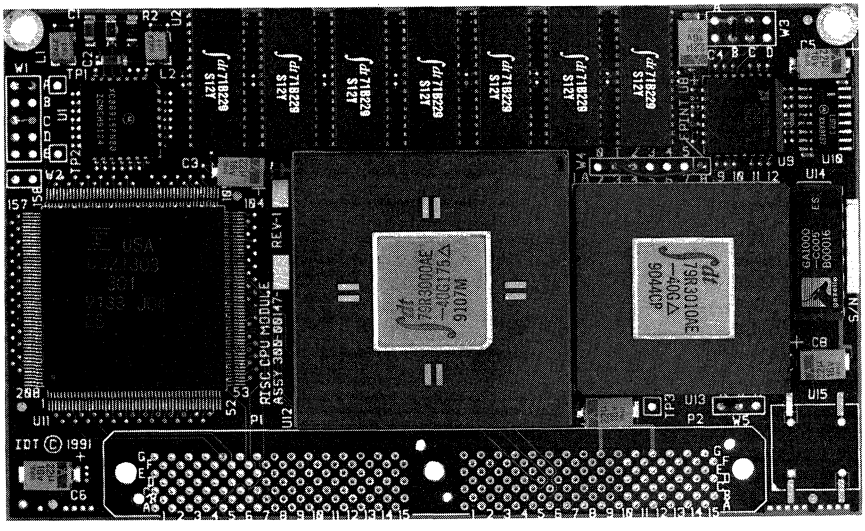
- Cache Size: 64kB Instruction, 64kB Data
- Processor Speeds up to 40MHz
- Includes R3010 Floating Point Accelerator
- 8-word Write Buffer
- Small Size 3.6" x 4.0"
- Block refill option of 1, 4, 8, 16, or 32 words
- On-board oscillator, delay line, and reset circuitry
- 100% burn-in and functional test at rated speed

R3000 MODULE FOR HIGH PERFORMANCE CPUS AND MULTIPROCESSOR SYSTEMS

The IDT7RS114 is a complete reduced instruction set computer (RISC) CPU, based on the MIPS R3000 RISC processor, and supplied on a small fully-tested high-density plug-in module. The module includes the R3000 CPU, the R3010 Floating Point Accelerator, 64kB each of data and instruction cache memory, an eight-word write buffer. Clock generation, reset, control, and interrupt functions are included on the module to simplify the remainder of the system design.

The IDT7RS114 module includes a latch to hold an external address for snooping in the D-cache and is designed to support the R3000's multiprocessor features.

The module is constructed using surface mount devices on a 3.6" by 4.0" epoxy laminate board, and is connected to the user's system via a 210-pin Augat connector.



7RS114 (Actual Size is 3.6" x 4.0")

8

RELATED PRODUCTS

Prototyping System

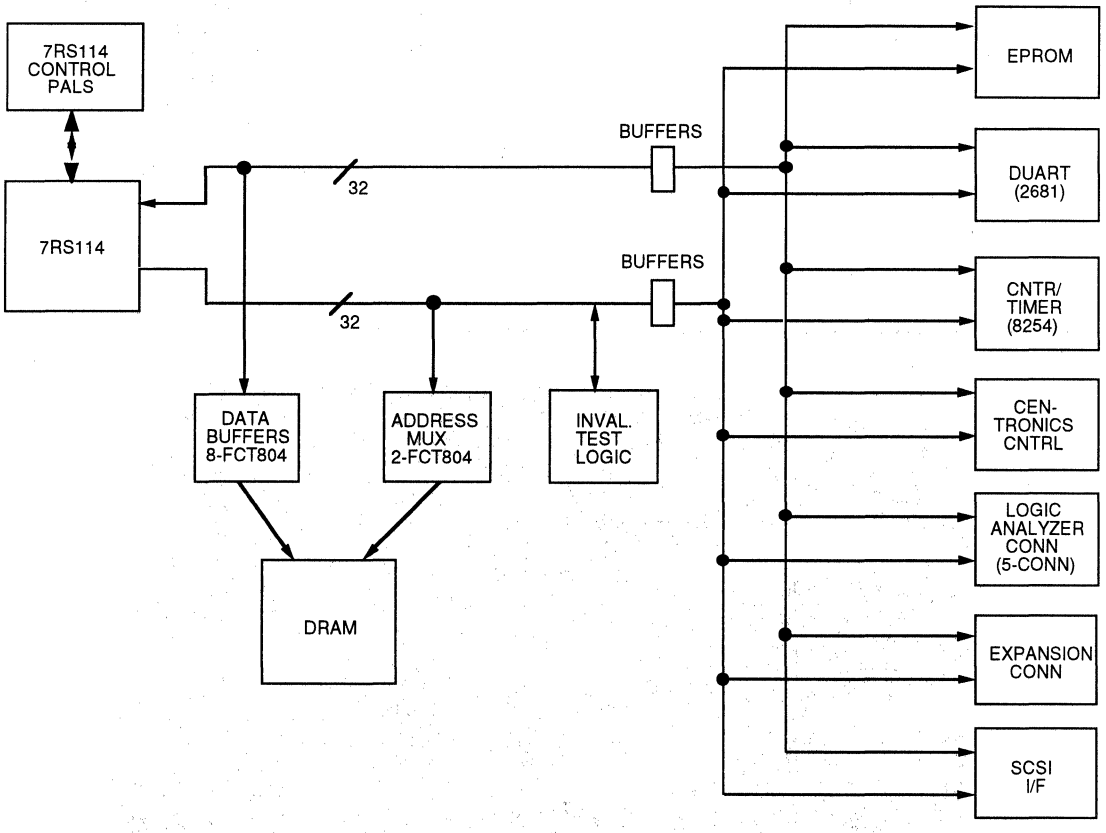
The 7RS114 module can be placed into immediate service using our flexible 7RS414 Prototyping Platform. The system includes a 7RS114 module and a general purpose CPU board that interfaces the module to the CPU board.

The CPU board contains 4MB of main memory, 256K of EPROM, DUART, SCSI interface, Centronics interface, an 8254 counter/timer, and connectors for an HP16500 Logic Analyzer. Four 50-pin connectors provide access to all the address, data, and control signals for external connection to additional hardware on, for example, a wire-wrap board.

The system includes IDT's IDT/sim System Integration Manager, which provides facilities for downloading code, examining memory, and stepping through programs.

Code for the R3000 can be created on a MIPS development system, on IDT's MacStation™ system, or using IDT/c, IDT's Multi-Host cross compiler product, available for a variety of machines. Assembled code can be downloaded into the Prototyping System for execution and debug.

7RS414 BLOCK DIAGRAM



2900 drw 01

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