ANALOG DEVICES

AN-670 APPLICATION NOTE

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A Complete EDFA/Raman Pump and CW Laser Solution

by Troy Murphy

INTRODUCTION

The ADN8820 Evaluation Board is a complete circuit solution for an Erbium-doped fiber amplifier (EDFA), a Raman amplifier, and continuous wave (CW) source laser applications. The demo board comes completely assembled and preconfigured to connect to a laser diode. The board can also be easily reconfigured for a specific application.

This application note is written to complement the ADN8820 data sheet. It assumes a basic understanding of laser diode and optical amplifier operation. Refer to the ADN8820 Data Sheet for its technical specifications and internal block diagrams.

The ADN8820 features a high output current driver, three built-in transimpedance amplifiers (TIAs), and a compensation amplifier that can be adjusted for the fastest loop settling time. The device can be set for one of four operational modes: constant output current (CC), constant output power (COP), constant laser power (CLP), or constant EDFA gain (CG).

Built-in protection prevents laser diode and EDFA damage by setting the maximum laser diode current and voltage, maximum output power, maximum laser diode power, and maximum EDFA gain. The limit thresholds are easily adjustable.

BOARD OVERVIEW

Figure 1 shows an overview map of the demo board. Section numbers are referenced inside parenthesis. The ADN8820 is mounted near the center of the board in Section (1). This area contains the minimum application circuitry needed for the device. The demo board was designed significantly larger to provide maximum flexibility and ease of customer use.

Power supply connections are at the upper-right corner of the board in Section (2). Wires can be soldered onto the board or screwed into the terminal block labeled POWER. The laser diode connects between VOUT and GND on the top center of the board in Section (3). Both solder pads and a terminal block labeled LASER are provided.

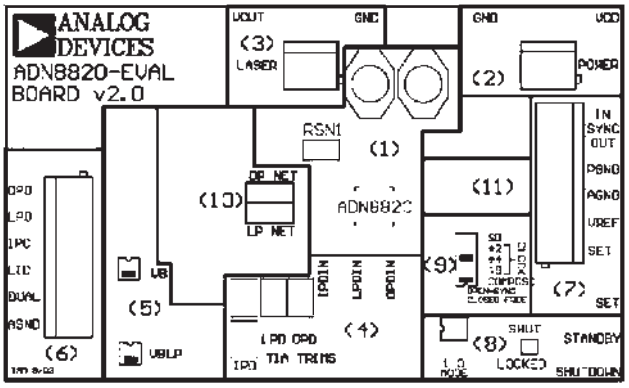

Figure 1. Demo Board Overview Map

Photodiodes connect to solder pads near the center of the board in Section (4). For typical operation, connect the photodiode anodes to ground and the cathodes to their respective inputs. The output photodiode connects to OPDIN, the laser photodiode connects to LPDIN, and the input photodiode (if used) connects to IPDIN.

Section (6) contains the photodiode TIA and current monitor outputs on a terminal block. The labels refer to ADN8820 pin names. EDFA output, laser diode output, and EDFA input TIA monitors are labeled OPO, LPO, and IPO, respectively. Trimming potentiometers at the bottom center of the board in Section (4) adjust the sensitivity of these TIAs.

LIO is the output current monitor. The board is designed for LIO to output 1 V/A. Therefore, 500 mA of output current would produce 0.5 V on LIO. The 50 mΩ output current sense resistor labeled RSN1 is located in Section (1). If an external RSN value is used, the LIO voltage is determined by LIO = 20 × (IOUT × RSN).

Limit voltages for OPLIM, LPLIM, ILIM, IPMIN, and VLIM are set with resistor dividers located in Section (5). In addition, dc bias voltages for the input and laser photodiode are set with the two 2 × 2 headers, labeled VB and VBLP. These headers connect directly to the respective ADN8820 pins. Connect the top row to set the bias at VDD, and connect the bottom row to set to ground. Alternate bias voltages can be set with an external voltage divider, as described in the Setting TIA Bias Voltages section.

SYNCIN and SYNCOUT are available on a terminal block in Section (7) located on the right side of the board. PGND and AGND reference points are also available. A built-in 2.5 V reference from the ADN8820 is at VREF. The SET input controls the output current or gain of the EDFA, depending on which mode the device is in. SET is also connected to a solder pad below the terminal block.

Section (8) contains STANDBY and SHUTDOWN solder pads. These are active-high logic inputs. These pads do not connect directly to the ADN8820. The logic levels are inverted through Q4 and Q5 and connect to SS/$\overline{SB}$ and DSEL/$\overline{SD}$, respectively.

The operating mode of the ADN8820 is set with the MODE switch located in Section (8). Refer to the Modes of Operation section of the ADN8820 Data Sheet for a complete explanation of these modes.

Two LEDs in this Section (8) show the ADN8820 status. Green indicates the loop is locked and stable. Red indicates the ADN8820 is in shutdown.

The 5 × 2 header located in Section (9) can be connected with 2 mm jumpers. The bottom row sets the PWM clock mode. Shorting this row puts the device in free-run mode; open sets it to external sync mode. An external clock must be connected to SYNCIN to leave this row unconnected. See the Setting PWM Clock section for more details.

Place a jumper across the top row to shutdown the ADN8820. The jumper is only one of the ÷2, ÷4, or ÷8 labeled rows to set the PWM free-run clock frequency. The PWM clock is set by ÷2 to 400 kHz, ÷4 to 200 kHz, and ÷8 to 100 kHz.

The on-board surface-mount compensation network is located to the left of the ADN8820 inside Section (1). Different compensation can be set using through-hole components located in Section (11). Solder a jumper-short across OP NET and LP NET to use the external network. Refer to the Adjusting the Compensation Network section for more details.

CONNECTING TO THE BOARD

The ADN8820 Demo Board was designed to run from a single 3.0 V to 5.5 V supply. Supply voltages higher than 5.5 V could damage the ADN8820 and possibly the laser diode. Connect power wires to the board in Section (2) through either the terminal block or solder pads.

The laser diode anode connects to VOUT in Section (3). Connect the laser diode cathode to GND. Screw wires into the terminal block or solder them directly to the solder pads.

Solder photodiode (PD) connections directly to the board in Section (4). The EDFA input PD connects to IPDIN, the laser power PD connects to LPDIN, and the EDFA output PD connects to OPDIN. Most applications require the photodiode cathode to connect to the TIA input with the anode connecting to ground.

Keep photodiode lead lengths to a minimum and avoid twisting input and ground wires together. This helps reduce parasitic input capacitance to the TIA, which, in turn, improves both stability and settling time.

SETTING PHOTODIODE BIAS VOLTAGES

The header labeled VB in Section (5) sets the bias voltage for the EDFA input photodiode. This voltage connects to Pin 2 (VB) on the ADN8820, the noninverting input of the input photodiode TIA. Header VBLP sets the bias voltage for the laser power photodiode TIA. Connecting a 2 mm jumper across the top row forces the bias voltage to VDD, connecting the bottom row sets it to 0 V as shown in Figure 2.

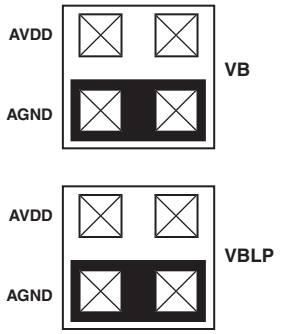

Figure 2. TIA Bias Voltage Header Settings

Alternative bias voltages can be set by removing the jumpers and soldering through-hole resistors according to Equation 1 and Equation 2.

$$VB = \frac{RVB2}{RVB1 + RVB2} \quad (1)$$

$$VBLP = \frac{RVBLP2}{RVBLP1 + RVBLP2} \quad (2)$$

The output photodiode is always biased to 0 V. The noninverting input of the TIA for the output photodiode is internally connected to AGND in the ADN8820 and cannot be adjusted.

Most applications require the photodiode cathode to connect to the TIA input with the anode connecting to ground. In this configuration, set VB and VBLP to 0 V by connecting a 2 mm jumper across the bottom row of the header. The output voltage of the TIA will increase with an increase of light to the photodiode.

LOOP CONTROL MODES

The control loop operating mode of the ADN8820 is set with the MODE switch located in Section (8). Refer to Figure 3 and the ADN8820 data sheet for a complete explanation of these modes.

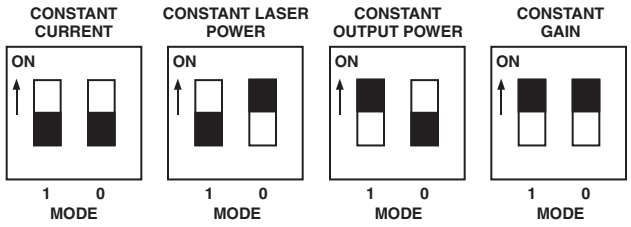

Figure 3. Demo Board Loop Control Modes

CALIBRATING PHOTODIODE TIAS

Multiturn potentiometers for trimming the sensitivity of the photodiode TIAs are located at the bottom of the board in Section (4). These potentiometers are used as feedback resistors around each TIA. Increase resistance by turning the potentiometer screw clockwise. Decrease resistance by turning the potentiometer screw counter clockwise.

The laser and EDFA output TIAs each use a 25 kΩ potentiometer. The input photodiode TIA uses two potentiometers in series: a 1 MΩ potentiometer for course tuning and a 25 kΩ potentiometer for fine tuning. This accommodates a wide dynamic range of EDFA input. The TIA outputs are available on the terminal block in Section (6) at OPO, LPO, and IPO.

A suggested method for calibrating each TIA is outlined below. First, the laser photodiode TIA is adjusted, then the input TIA, and finally the output TIA. All calibration can be done with the ADN8820 in a constant current mode. For CW lasers, stop after Step 3.

1) Place the ADN8820 into constant current mode (00 on the MODE switch).
2) Apply the appropriate voltage to the SET input to set the calibration current. In this mode, the LIO voltage will be forced to equal the SET voltage. For example, 300 mV on the SET input corresponds to 300 mA of output current using R_{SN} = 50 mΩ.
3) Adjust the LPD potentiometer until the desired LPO voltage is achieved.
4) Apply 0 V to SET. This sets the pump laser current to 0 A.
5) Connect an optical source with a known constant power. Most optical amplifiers are specified to a given input power, such as –20 dBm.
6) Adjust the two IPD potentiometers until the desired IPO voltage is achieved.
7) Review the optical amplifier data sheet to find its gain versus pump laser current.
8) Apply appropriate voltage to SET to force the required pump laser current. For example, 300 mA of laser current yields a gain of +20 dB. Therefore, for an input of –20 dBm, an output of 0 dBm can be expected.
9) Adjust the OPD potentiometer until the desired OPO voltage is achieved. For constant gain mode applications, adjust for OPO to equal IPO. Constant gain mode will adjust the pump laser current until OPO equals IPO.

ADJUSTING THE COMPENSATION NETWORK

The ADN8820 uses one of two compensation networks depending on its operating mode. The CC and CLP modes engage the network connected to the EANLP pin, and the COP and CG modes engage the EANOP network.

The on-board EANLP compensation network was designed for the fastest loop settling time response and should not require adjustment. The on-board EANOP network should provide stability for most applications, although it may not offer the fastest settling time.

Components R1, R2, R3, C1, C2, and C3 make up the EANLP network as shown in the demo board schematic in Figure 11. R11, R12, R13, C11, C12, and C13 create the EANOP network. These 0603 surface-mount components can be replaced directly. Use Figure 4 to find their locations on the demo board.

Through-hole network components are also available. RLPx and CLPx components connect to EANLP through the JP4 jumper labeled LP NET; ROPx and COPx components connect to EANOP through the JP5 jumper labeled OP NET (see Figure 11 for their electrical connections). Jumpers JP4 and JP5 must be shorted to connect the through-hole networks.

When using the OP NET through-hole network, remove surface-mount components R11, R12, R13, and C12. This prevents unwanted interaction between the external and on-board networks. Similarly, remove surface-mount components R1, R2, R3, and C2 when using the LP NET through-hole network.

STABILIZING

The on-board compensation network should provide stability for both the CC and CLP modes. The surface-mount network connected to the ADN8820 EANLP pin was designed for the fastest loop settling time in these modes. A PID network connected to the EANOP pin is provided for the COP and CG modes. Depending on the laser diode used, this network may not provide sufficient stability and may require adjustment.

Loop stability and response time can be monitored with an oscilloscope on the demo board output as listed in Table 1.

Table 1. Stability Monitoring Outputs for Different Modes

Control Loop Mode	Stability Monitor
Constant Current (CC)	LIO
Constant Laser Power (CLP)	LPO
Constant Output Power (COP)	OPO
Constant Gain (CG)	OPO

The ADN8820 will force these outputs to equal the SET input voltage in the CC, CLP, and COP modes. In CG mode, the device will force the OPO voltage to equal IPO, keeping the device in a constant gain.

Apply a step voltage to the input and observe the response of the monitor output. Generally speaking, increasing loop gain or bandwidth will improve settling time. Too much will result in excessive overshoot or instability.

An unstable loop appears as a constant sine wave on the monitor output. The oscillation frequency will typically be around 100 kHz to 1 MHz or higher. Some low level switching noise at 1 MHz may be present on the LIO pin, but do not confuse this for instability.

Increase C1 if the output current is not stable in the CC mode by replacing the 0603 component or removing the component and installing the appropriate R-C network to RLP2 and CLP1. If the system is unstable in constant laser power (CLP) mode, users can either reduce the LPD potentiometer resistance or increase C1.

The simplest method for stabilizing the control loop in the COP or CG modes is to reduce the OPD potentiometer resistance. Unfortunately, this may also affect the usable range of the control input. Remember, the device is trying to keep OPO equal to SET in the COP mode or the IPO output in the CG mode.

The EANOP network can also be adjusted to improve loop response for the COP and CG modes. To improve stability, increase C11 (or COP1 if using the external network).

SETTING THE PROTECTION LIMITS

Table 2 shows the limiter voltages for an unmodified demo board.

Table 2. Demo Board Default Protection Limits

Limiter Input	Sets the Maximum:	Default Voltage	Connect Resistors:
VLIM	Laser Diode Voltage	VDD	RVLIM
ILIM	Laser Diode Current	2.6 V	RILIM1, RILIM2
LPLIM	Laser Diode Power	2.6 V	RLPLIM1, RLPLIM2
OPLIM	EDFA Output Power	2.6 V	ROPLIM1, ROPLIM2
IPMIN	EDFA Gain	0 V	RIPMIN

Maximum output voltage will not exceed the voltage at the VLIM pin. To adjust VLIM, add through-hole resistor RVLIM. The value of RVLIM is a function of the supply voltage, VDD.

$$RVLIM = \frac{100\,\text{k}\Omega}{\frac{VDD}{VLIM} - 1} \quad (3)$$

Maximum output current is controlled by ensuring the voltage at LIO never exceeds the ILIM voltage. The demo board comes configured for LIO = 1 V/A. Therefore, the voltage at ILIM corresponds to the maximum output current. For example, ILIM = 2 V sets the maximum output to 2 A. The ILIM voltage is set with RILIM1 and RILIM2 according to Equation 4.

$$ILIM = 2.5\,\text{V} \times \frac{RILIM2}{RILIM1 + RILIM2} \quad (4)$$

Maximum laser power and output power are similarly controlled by comparing LPLIM and OPLIM to outputs LPO and OPO, respectively. Adjust the LPLIM by adding RLPLIM1 and RLPLIM2. Adjust OPLIM with ROPLIM1 and ROPLIM2. Use Equation 4 by replacing the appropriate resistor variable.

It is not necessary to add all of these resistors. ILIM, LPLIM, and OPLIM have a default voltage of 2.6 V if their external resistors are not used.

An additional protection control is provided for constant gain (CG) mode. If the voltage at IPO drops below IPMIN, the pump laser diode current is reduced. This prevents the optical amplifier from trying to increase its gain too high, damaging the pump lasers. Such a condition could occur if the input signal drops out or becomes disconnected.

The demo board comes with the IPMIN voltage pulled to 0 V. The voltage at IPMIN must exceed 200 mV to activate the maximum gain protection. Add resistor *RIPMIN* to set *IPMIN*.

$$RIPMIN = 1\,\text{k}\Omega \times \left(\frac{2.5\,\text{V}}{IPMIN} - 1 \right) \quad (5)$$

You should calculate *RIPMIN* only after calibrating the IPO and OPO TIAs.

STANDBY AND SHUTDOWN MODES

Standby and shutdown modes are activated through the STANDBY and SHUTDOWN input pads on the ADN8820 demo board. Both inputs are active high. These pads connect to the FETs on the demo board which pull down the SS/$\overline{\text{SB}}$ pin for standby mode or DSEL/$\overline{\text{SD}}$ for shutdown. A red LED will turn on when the ADN8820 is in shutdown mode.

Standby mode disables both the linear and PWM output amplifiers, forcing the output current to 0 A and deactivates the PWM clock frequency. The compensation error amplifier and photodiode TIAs remain active. Shutdown disables all amplifier and places the ADN8820 in a low current state.

You can also place the device into shutdown by connecting a jumper across the top row of header JP3, labeled $\overline{SD}$. This jumper overrides any logic level connected to the SHUTDOWN pad. Remove the jumper to resume normal operation.

MODIFYING THE PWM SWITCHING FREQUENCY

The PWM switching clock is divided from the dither frequency. The dither frequency is set with R48. The division factor is 2, 4, or 8, as determined by the jumper setting on header JP3. The demo board comes configured with a PWM clock frequency of 100 kHz. The recommended PWM clock range is 100 kHz to 1 MHz.

The PWM amplifier can operate from its internal clock or it can sync to an external clock applied to SYNCIN. For free-run (internal clock) operation, connect a 2 mm jumper across the row labeled COMPOSC on header JP3. Remove this jumper to operate from an external clock.

If using an external clock, keep the internal PWM clock frequency within 200 kHz of the SYNCIN clock. This ensures the PLL will achieve a stable lock quickly.

The phase of the PWM clock is adjusted through RPHASE1 and RPHASE2. Phase can be adjusted to spread the switching edges of multiple ADN8820 devices over one clock period. This helps reduce power supply ripple to the boards. The phase shift is approximately equal to 360° × (*PHASE*/2.5 V), where *PHASE* is the voltage

$$PHASE = 2.5\,V \times \frac{RPHASE2}{RPHASE1 + RPHASE2} \quad (6)$$

If *RPHASE*1 and *RPHASE*2 are not connected, the *PHASE* voltage defaults to 0.6 V or approximately 86°.

MULTIPUMP OPTICAL AMPLIFIER APPLICATIONS

Multiple demo boards can be easily ganged together for multipump optical amplifier applications. Connect the DUAL output from the first (master) board to the SET input of the second board. For more than two pump lasers, connect the SET input of the subsequent boards to the DUAL of the previous board in a daisy-chain fashion.

The master board can be run in either constant output power (COP) or constant gain (CG) modes. However, the second and subsequent boards should be kept in constant laser power (CLP) mode for best system loop stability.

In COP mode, the control voltage connects to SET on the master board. This sets the optical amplifier optical output power. In CG mode, the master board controls all pump lasers to force its OPO voltage to equal the IPO voltage.

The *DUAL* output voltage follows the equation

$$DUAL = 20 \times (LIO - 0.9 \times ILIM) \quad (7)$$

In the application, the master board will turn up its pump laser diode while leaving all other pumps off. The master board will start to turn on the second pump laser once the first pump reaches about 90% of its maximum current. If still more gain is required, then a third pump turns on once the second pump reaches 90% maximum current. This process continues for all pumps until the required optical gain is achieved.

ADJUSTING OUTPUT CURRENT SENSE RESISTOR

The demo board uses resistor RSN1 to sense the output current. RSN1 and RSN2 are connected in parallel across the CSP and CSN pins on the ADN8820. RSN1 is 50 mΩ, which results in the LIO output moving 1 V per amp of output current.

Connect a through-hole resistor at *RSN2* to change the value of the sense resistor. If *RSN1* is not removed, the combined sense resistance will be the parallel combination of the two.

$$RSN = \frac{RSN1 \times RSN2}{RSN1 + RSN2} \quad (8)$$

Output current is monitored at *LIO* and is

$$LIO = 20 \times IOUT \times RSN \quad (9)$$

A lower value of *RSN* will slightly improve circuit efficiency. A higher value of *RSN* improves *LIO* sensitivity and may be required for maximum output currents of less than 300 mA.

The maximum output current from the demo board is limited by the inductors. Both inductors are rated to a dc current of 4.5 A max.

BOARD LAYOUT

The board uses four layers, including internal ground and power planes. Both ground and power planes are split into two sections: one for high current and digital signals, and one for low noise analog signals. The linear and PWM output amplifiers on the ADN8820 connect to PVDD and PGND. The built-in voltage reference amplifier (VREF), photodiode TIAs, and limiter inputs are referenced to AVDD and AGND.

The laser diode current return path is through AGND. This separates switching noise from the PWM and digital circuitry from the laser diode and sensitive analog TIAs. Refer to the ADN8820 data sheet for more information on split-plane layouts.

Figure 4 shows an enlarged view of the surface-mount components around the ADN8820. The board does not have clear labels due to space restrictions.

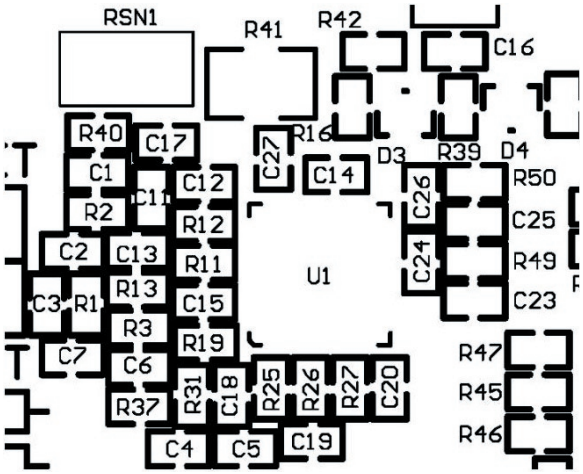

Figure 4. Enlarged View of Surface-Mount Component Labels

Figures 5 to 10 show the layout drawings for the silkscreen, top and bottom layers, ground plane, power plane, and drilling guide. These figures are smaller than actual scale.

The power and ground plane drawings are negative masks. They indicate where the solid copper plane is removed. Vias that connect to these planes will not appear on the mask. Vias that do not connect will show up as a solid circle.

The drill guide shows via and through-hole locations and sizes. The circle represents a 10-mil hole with a 20-mil pad; the "X" symbols indicate a 5-mil hole with a 10-mil pad. Other symbols conform to the through-hole components used.

Figure 11 shows the complete demo board schematic for v2.0.

DEMO BOARD LAYOUT DRAWINGS

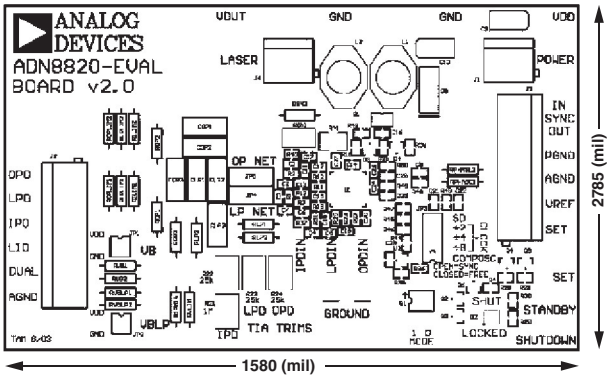

Figure 5. ADN8820-EVAL v2.0 Silkscreen

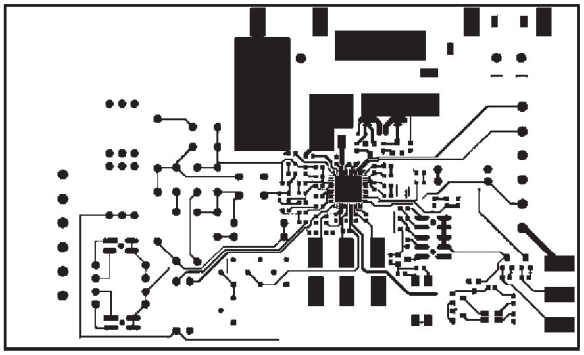

Figure 6. ADN8820-EVAL v2.0 Top Layer

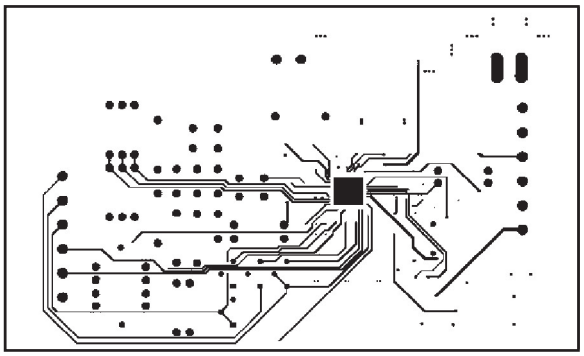

Figure 7. ADN8820-EVAL v2.0 Bottom Layer

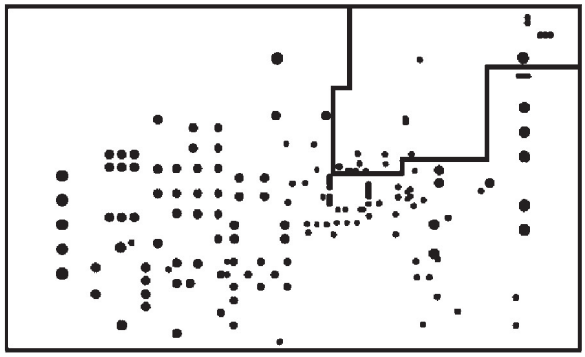

Figure 8. ADN8820-EVAL v2.0 Ground Plane

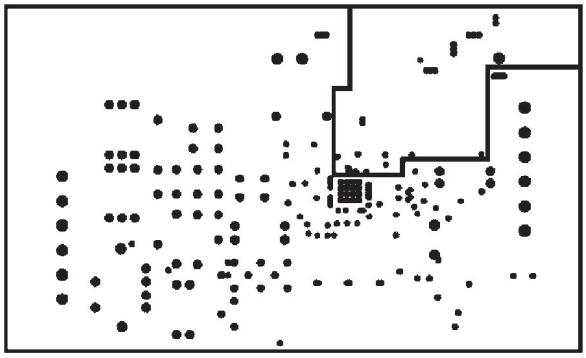

Figure 9. ADN8820-EVAL v2.0 Power Plane

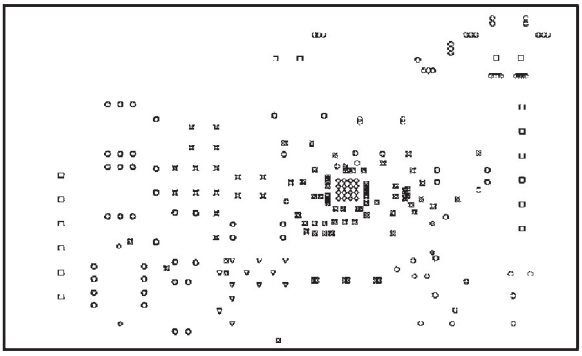

Figure 10. ADN8820-EVAL v2.0 Drill Guide

DEMO BOARD V2.0 SCHEMATIC

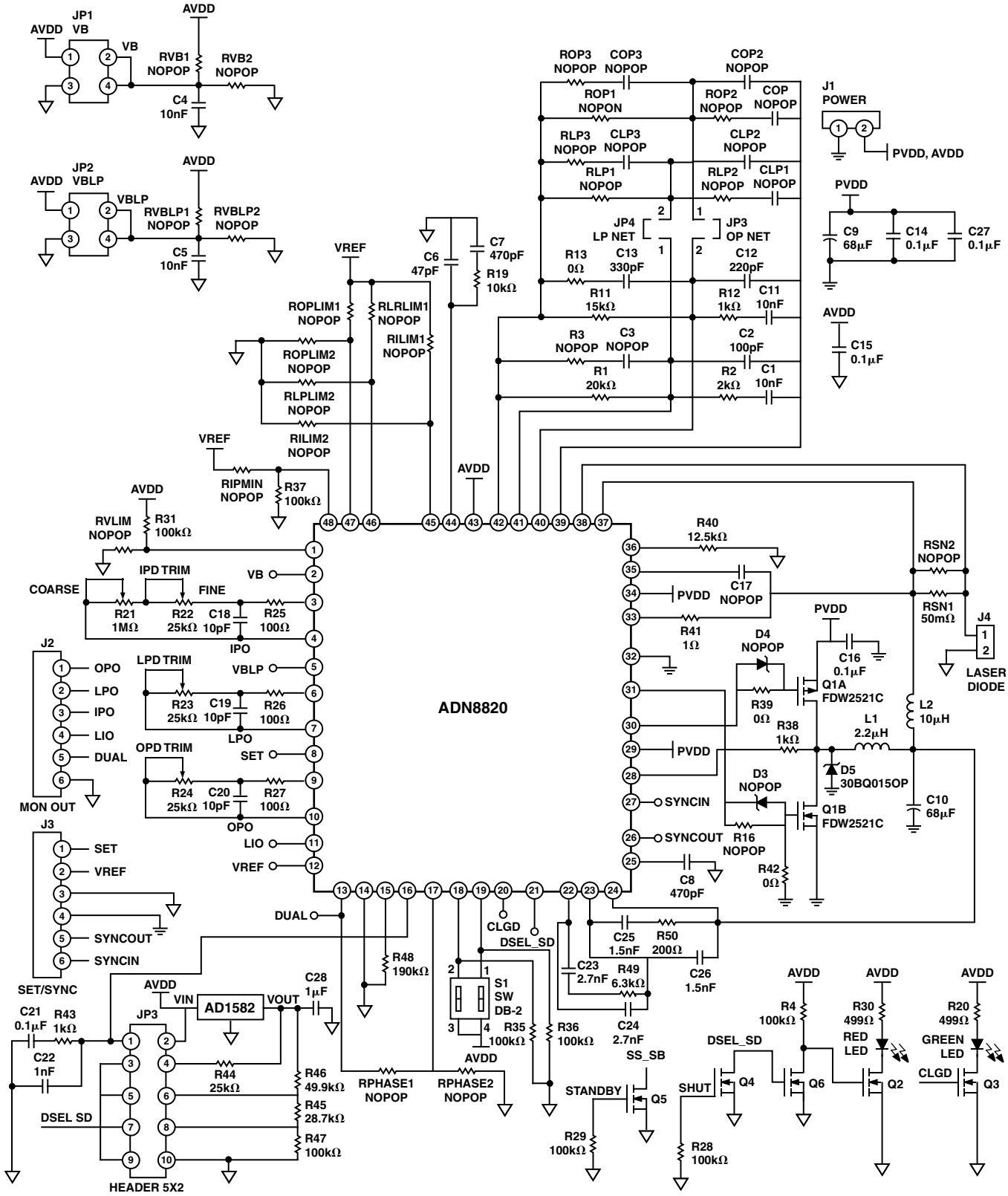

Figure 11. ADN8820-EVAL v2.0 Board Schematic

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