SECTION 2 BBC Microcomputer Model B +

BBC Microcomputer Model B+ Service Manual

Contents

WARNING: THE COMPUTER MUST BE EARTHED

IMPORTANT: The wires in the mains lead for the apparatus are coloured in accordance with the following code:

Green & Yellow	Earth
Blue	Neutral
Brown	Live

The moulded plug must be used with the fuse and fuse carrier firmly in place. The fuse carrier is of the same basic colour (though not necessarily the same shade of that colour) as the coloured insert in the base of the plug. Different manufacturers' plugs and fuse carriers are not interchangeable. In the event of loss of the fuse carrier, the moulded plug MUST NOT be used. Either replace the moulded plug with another conventional plug wired as detailed below, or obtain a replacement fuse carrier from an authorised ACORN dealer. In the event of the fuse blowing it should be replaced, after clearing any faults, with a 3 amp fuse that is ASTA approved to BS1362.

If the socket outlet available is not suitable for the plug supplied, the plug should be cut off and the appropriate plug fitted and wired as previously noted. The moulded plug which was cut off must be disposed of as it would be a potential shock hazard if it were to be plugged in with the cut off end of the mains cord exposed.

As the colours of the wires may not correspond with the coloured markings identifying the terminals in your plug, proceed as follows:

The wire which is coloured green and yellow must be connected to the terminal in the plug which is marked by the letter E, or by the safety earth symbol ± , or coloured either green or green and yellow.

The wire which is coloured blue must be connected to the terminal which is marked with the letter N, or coloured black.

The wire which is coloured brown must be connected to the terminal which is marked with the letter L, or coloured red.

1 Introduction

This manual is intended to provide the information required to diagnose and repair faults on the BBC Microcomputer Model B+ which was designed by ACORN Computers Ltd of Cambridge, England.

The information contained in this manual is aimed at service engineers and ACORN dealers who will be servicing the BBC Microcomputer on behalf of ACORN Computers Ltd.

2 Packaging and installation

The microcomputer is supplied in a two-part moulded polystyrene packing in a cardboard box. Supplied with the microcomputer is a User Guide, an introductory cassette package, a UHF TV lead, and a guarantee registration card. Disc and Econet versions also contain a Disc Filing System User Guide and an Econet User Guide respectively.

The mains supply for UK models is 240V AC 50Hz. The microcomputer is supplied with a moulded 13 amp square pin plug. If this plug is unsuitable then it must be cut off and thrown away. Instructions for fitting a replacement plug are given right at the front of this manual.

The microcomputer is turned on by a switch at the back of the microcomputer next to the mains lead.

Do not use the microcomputer in conditions of extreme heat, cold, humidity or dust or in places subject to vibration. Do not block ventilation under or behind the computer. Ensure that no foreign objects are inserted through any openings in the microcomputer.

3 Specification

3.1 The microcomputer

The microcomputer is contained in a rigid injection moulded thermoplastic case, and provides the following facilities.

73 key full travel QWERTY keyboard including 10 user-definable function keys. Keyboard has two key rollover and auto repeat.

Fully encased internal power supply manufactured to BS 415 Class 1.

Internal loudspeaker driven from a 4-channel sound synthesis circuit with ADSR envelope control.

A colour television signal, for connection to a normal domestic television aerial socket, is available through a phono connector. This signal is 625 line, 50Hz, interlaced, encoded PAL A and is modulated on UHF channel 36.

A BNC connector supplies a composite video output to drive a black and. white or PAL colour monitor.

6-pin DIN connector provides separate RGB and sync outputs at TTL levels. RGB are all high true, and sync is link selectable as high or low true, pulse duration 4.0 microseconds.

A standard audio cassette recorder can be used to record computer programs and data at 300 or 1200 baud using the Computer Users' Tape Standard tones. The cassette recorder is under automatic motor control and is connected to the computer via a 7-pin DIN connector.

An interrupt driven elapsed time clock (user settable). 6512A processor running at 2MHz.

64K of read/write Random Access Memory (RAM), allowing a shadow screen mode, and 12K paged RAM in any mode.

32K Read Only Memory (ROM) integrated circuit containing the Machine Operating System and a fast BASIC interpreter. The interpreter includes a 6502/6512 assembler which enables BASIC statements to be freely mixed with 6502/6512 assembly language. Code generated using the BASIC assembler can be run on a machine with a 6512 microprocessor, or a machine with a 6502 microprocessor.

Up to five 32K sideways ROMs may be plugged into the machine at any time, having the effect of ten 16K ROM slots (eleven including BASIC). These ten 16K ROM slots are paged and may include Pascal, word processing, computer aided design software, disc and ECONET and WINCHESTER filing systems or TELETEXT acquisition software.

The full-colour Teletext display of 40 characters by 25 lines, known as mode 7, has character rounding, with double height, flashing, coloured background and text plus pixel graphics - all to the Teletext standard.

The non-Teletext display nodes (modes 0 to 6) provide user-definable characters in addition to the standard upper and lower case alpha-numeric font. In these modes, graphics may be mixed freely with text.

The following screen modes are available:

Mode 0: 640 x 256 2-colour graphics and 80 x 32 text (20K)
Mode 1: 320 x 256 4-colour graphics and 40 x 32 text (20K)
Mode 2: 160 x 256 16-colour graphics and 20 x 32 text (20K)
Mode 3: 80 x 25 2-colour text only (16K)
Mode 4: 320 x 256 2-colour graphics and 40 x 32 text (10K)
Mode 5: 160 x 256 4-colour graphics and 20 x 32 text (10K)
Mode 6: 40 x 25 2-colour text only (8K)
Mode 7: 40 x 25 Teletext display (1K)
Mode 128: 640 x 256 2-colour graphics and 80 x 32 text (20K)
Mode 129: 320 x 256 4-colour graphics and 40 x 32 text (20K)
Mode 130: 160 x 256 16-colour graphics and 20 x 32 text (20K)
Mode 131: 80 x 25 2-colour text only (16K)
Mode 132: 320 x 256 2-colour graphics and 40 x 32 text (10K)
Mode 133: 160 x 256 4-colour graphics and 20 x 32 text (10K)
Mode 134: 40 x 25 2-colour text only (8K)
Mode 135: 40 x 25 Teletext display (1K)

All graphics access is transparent.

Shadow mode gives 32K BASIC program RAM (less workspace) to the user in any screen mode.

The shadow screen mode offers equivalent display sizes to the standard mode 0 to 7 screens, but using an auxiliary memory area, the "shadow" RAM. In shadow display modes (nudes 128 to 135) BASIC or a user program is free to use all memory between OSHWM (PAGE) and &7FFF, plus the 12K bytes of sideways (paged) RAM.

The 12K paged RAM is available to the user in any screen mode, shadow or non-shadow.

Serial interface to RS423 standard. The new standard has been designed to be inter-operable with RS232C equipment. Baud rates are software selectable between 75 baud and 19200 baud (guaranteed up to 9600 baud) .

An 8-bit input/output port with 2 control bits.

Four analogue input channels. Each channel has an input voltage range of OV to 1.8V. The conversion time for each channel is 10 milliseconds. The resolution of the ADC chip is 10 bits.

1 MHz buffered extension bus for connection to a variety of external hardware such as a TELETEXT acquisition unit, IEEE 488 interface, WINCHESTER disc drive etc.

Buffered interface for connection via the TUBE to a range of second processors.

CENTRONICS compatible printer interface.

The basic model B+ may have added to it a floppy disc interface using either an 8271 or 1770 controller IC.

Also, a low cost network interface, the Acorn ECONET, may be added.

Finally, a speech upgrade is available using the 5220 speech IC to generate predefined words and sounds through the built-in speaker.

3.2 Power supply

Input voltage	240V AC RMS +/-10%
input frequency	47-53Hz
+5V output voltage	+5V DC +/-0.1V
+5V output current	0.1A minimums 3.5A maximum
+12V output voltage	+12V DC +/-10%
+12V output current	1.25A maximum
-5V output voltage	-5V DC +/-10%
-5V output current	0,1A maximum
Total output power	35W

3.3 Display outputs

Modulated output (marked UHF out)

Standard	625-line PAL A UHF colour television signal
Channel	E36
Vision carrier	Nominal 591.25MHz
RF output	1.0 to 2.5mV
6db bandwidth	>= 8MHz
RF output impedance	75 ohms
Connector	phono

Composite video (marked video out)

Output level	Nominal 1V peak to peak
Output impedance	Nominal 75 ohms
Option	Chrominance information (link selectable) allows composite PAL monitors to be used
Connector	BNC

Colour monitor (marked RGB)

RGB signals	TTL type levels
CSYNC signal	TTL type level +ve/-ve going (link selectable)
Connector	6-pin DIN

3.4 RS423

Line length	1200m maximum
Input impedance	> 4k ohms
Baud rate	19200 maximum (guaranteed up to 9600)

3.5 Cassette interface

Output impedance	Less than 1k ohms
Input impedance	Greater than 100k ohms
Output level	Nominal 200mV peak to peak, 70mV RMS
Dynamic input range	Nominal 50mV to 5V peak to peak, -25 to +15dB 0dB = 350mV RMS
Motor control	By miniature relay within computer Contact rating 1A at 24V DC
Baud rate	300 or 1200 baud using standard CUTS tones (1200 and 2400 Hz tones)
Connector	7-pin DIN

3.6 Analogue to digital convertor

Resolution	10 bit
Full scale input voltage	VREF
VREF	1.8V typical
Accuracy (with respect to VREF)	
full scale error	0.5% typical
zero scale error	0.5% typical
Non-linearity	0.1% typical
Temp coefficient	-6mV/degree C typical
Conversion speed	10.0ms per channel typical
Input impedance	> 1M ohms

3.7 ECONET

Line voltages	0.25V and 3V typical into 50 ohms

3.8 CENTRONICS compatible printer interface

Data strobe	4us pulse

3.9 Audio output

Output power	0.5W
Speaker impedance	8 ohms

3.10 Environment

Air temperature

system on	0 to 35 degrees C
system off	-20 to 70 degrees C

Humidity

system on	85% relative humidity at 35 degrees C
system off	95% relative humidity at 35 degrees C

Storage conditions

air temperature	-20 to 70 degrees C
humidity	95% relative humidity at 55 degrees C

3.11 Dimensions

Height 73mm (including feet)
Width 415mm
Depth 345mm

4 Disassembly and assembly

To service the BBC Microcomputer B Plus, first disconnect the power supply plug from the mains and remove all peripheral connections from the computer.

To disassemble

The lid of the microcomputer case may be removed after undoing four fixing screws, two on the rear panel and two underneath. Take care not to lose the two spire clips pushed onto the case lid, into which the rear fixing screws locate. DO NOT remove the lid with the mains power connected.

Inside the microcomputer are three main sub-assemblies:
power supply unit, keyboard and the main printed circuit board.

To remove the keyboard, undo the two screws and nuts holding it to the case bottom, taking care to note the positions of the associated washers. Unplug the 17-way keyboard connector and the 2-way loudspeaker connector from the main printed circuit board, and the 10-way serial-ROM connector, if fitted.

The power supply unit is connected to the main circuit board by seven push-on connectors which may be unplugged. Three screws on the underside of, the case are undone allowing the unit to be removed. On reassembly, ensure that the same type of screw is used (M3x6mm).

The main printed circuit board can be removed after the two wires to SK2 (composite video BNC socket) have been disconnected. Undo the seven fixing screws and remove the circuit board from the case by sliding it forwards and then lifting it from the rear.

To reassemble

Replace the main printed circuit board by putting the front edge (with connector headers) in first and pulling it forwards as far as possible until the back edge drops in. Be careful not to trap the composite video wire to the BNC connector if this was removed. Replace the PCB fixing screws.

Reconnect the composite video and its connector.

Reconnect the power supply, being careful to route the wires neatly, and connect the wires (seven) to the push-on connectors on the PCB, being very careful to get the polarity right.

PCB connectors marked VCC must have a red wire attached(three)
PCB connectors marked OV must have a black wire attached (three)
The connector marked -5V has the purple wire attached (one).

Replace the keyboard and reconnect the loudspeaker to the main PCB. Be careful to reconnect the keyboard ribbon socket so that all the pins are engaged; it is easy to displace the connector one pin to right or left. Replace the 10-way serial-ROM connector if fitted. Replace the nuts and bolts holding the keyboard in place.

Make one final check that all reconnections have been made correctly, especially the power supplies which will short circuit if two are reversed.

Replace the lid and press down at the rear whilst tightening the two rear fixing screws. Finally replace the front two fixing screws.

5 Circuit description

This circuit description has been kept as simple as possible as the detailed fault finding section (section 9) should prove to be of more use for servicing. A detailed description is given of those features of the BBC Microcomputer B + which are new.

5.1 General

The microcomputer uses the 6512 CPU (IC42) which allows more accurate timing of the logic circuitry than did the 6502, see 5.2. The 6512 requires two clock signals at 'MOS' voltage levels, in all other respects it functions in the same way as the 6502.

The computer clocks are derived from a 16MHz crystal controlled oscillator circuit (X1 and half of IC26), and divider circuitry in the video processor ULA (IC53).

The 6512 accesses 31 1/4Kbytes of ROM, 3/4Kbyte of memory mapped input/output, and up to 44Kbytes of RAM. 64Kbytes of RAM are installed on the PCB, the extra 20Kbytes being used for the screen memory in shadow mode, see 3.1.

The memory mapped I/O is located in pages &FC, &FD, and &FE of the CPU address space.

There are five sideways ROM sockets installed on the PCB, each capable of taking an 8, 16, or 32Kbyte ROM or EPROM (ICs 35 44 57 62 68). When used with a 32K ROM, each sideways ROM socket is decoded as two 16K sideways ROM slots. A sixth ROM socket IC71 holds a 32Kbyte ROM which contains the operating system and BASIC. 'The number of the ROM currently in use is held in the ROM select latch (IC45).

64Kbytes of RAM are installed on the board in eight 64K by 1 bit DRAM chips, (ICs 55 56 60 61 64 65 66 67). Of this RAM, 32Kbytes are always accessible to the CPU, 12Kbytes can be paged into the sideways (paged) ROM space, and the remaining 20Kbytes are used as screen memory in shadow mode. Both CPU (IC42) and 6845 cathode ray tube controller (IC78) have access to the RAM. Each can access the RAM at full 2MHz clock speed by. interleaving the accesses on alternate phases of the 2MHz clock. The RAM is thus being accessed at 4MHz. The 6845 accesses the RAM sufficiently to perform the refresh function.

Screen display is provided through the 6845 (IC78), video processor (IC53), and various encoding circuits. Three display outputs are available:

RGB consists of CSYNC and RED GREEN BLUE at TTL voltage levels. Each colour is either on, off, or flashing, giving sixteen displayable colour effects, ie eight static colours and eight flashing colours.

VIDEO output is a summation of RGB to give a grey scale (luminance only). If link S26 is made the chrominance component (colour information) is added to the VIDEO output.

UHF output is obtained by mixing luminance, chrominance and SYNC signals, and then feeding the result to a UHF modulator.

Serial input/output is provided by the cassette port and RS423 port. Both are controlled by the 6850 asynchronous communications interface adapter (IC82) and a ULA called the serial processor (IC85).

Analogue input is fed to the four-channel 10 bit ADC chip (IC84).

A local area network facility is provided by the ECONET circuitry, centred on the 68B54 advanced data-link controller (IC81).

Two build options are available for the floppy disc circuitry. One is based on the 8271 floppy disc controller (IC15) as used on all BBC Microcomputers issues 1 to 7. The second option is based on the 1770 floppy disc controller (IC16). Some components are common to both options. The 1770 operates in either single density (FM) or double density (MFM) mode, and includes a data separator and disc speed decision logic. The 1770 controller interface is therefore simpler than the 8271 controller interface. ICs 1, 2, 3, 4, and 9 are not required with a 1770.

The CENTRONICS compatible printer interface is based on half (the A port) of a 6522 versatile interface adapter (IC10). IC5 buffers data sent to the printer.

The User Port is connected directly to the B port of the same 6522 (IC10).

The 1MHz extension bus is a fully buffered interface to the CPU, operating with lus transfer cycles. The bus appears as a 512 byte address block in the processor I/O space at pages &FC and &FD.

The TUBE interface provides buffered address and data lines for connection to a second processor. The TUBE itself is a fast parallel bidirectional FIFO and is resident in the 2nd processor unit.

The keyboard is read through half (the A port) of a 6522 versatile interface adapter (IC20).

Sound is produced by the 76489 (IC38), a four-channel sound generator chip. Speech may be generated using an optional 5220 speech processor (IC29) and 6100 word PHROM (IC37).

5.2 CPU timing

A 16MHz crystal controlled oscillator (X1 and half of IC26) generates clock pulses which are divided by circuitry within the video processor ULA (IC53). Pins 4, 5, 6, and 7 of the video processor provide 1MHz, 2MHz, 4MHz, and 8MHz outputs respectively. 8MHz, 4MHz and 2MHz are used to generate RAS and CAS for the DRAMs, and 6MHz for the TELETEXT chip IC59. 2MHz is used to generate the main system clock, 2E. 1MHz is used directly by the TELETEXT chip, and also in conjunction with 2MHz to generate the phase shifted 1MHz
system clock, lE from IC25.

The CPU is normally clocked at 2MHz. The 6512 (IC42) requires a two phase non-overlapping clock on inputs phil (pin 3) and phi2 (pin 37), see figure
1.

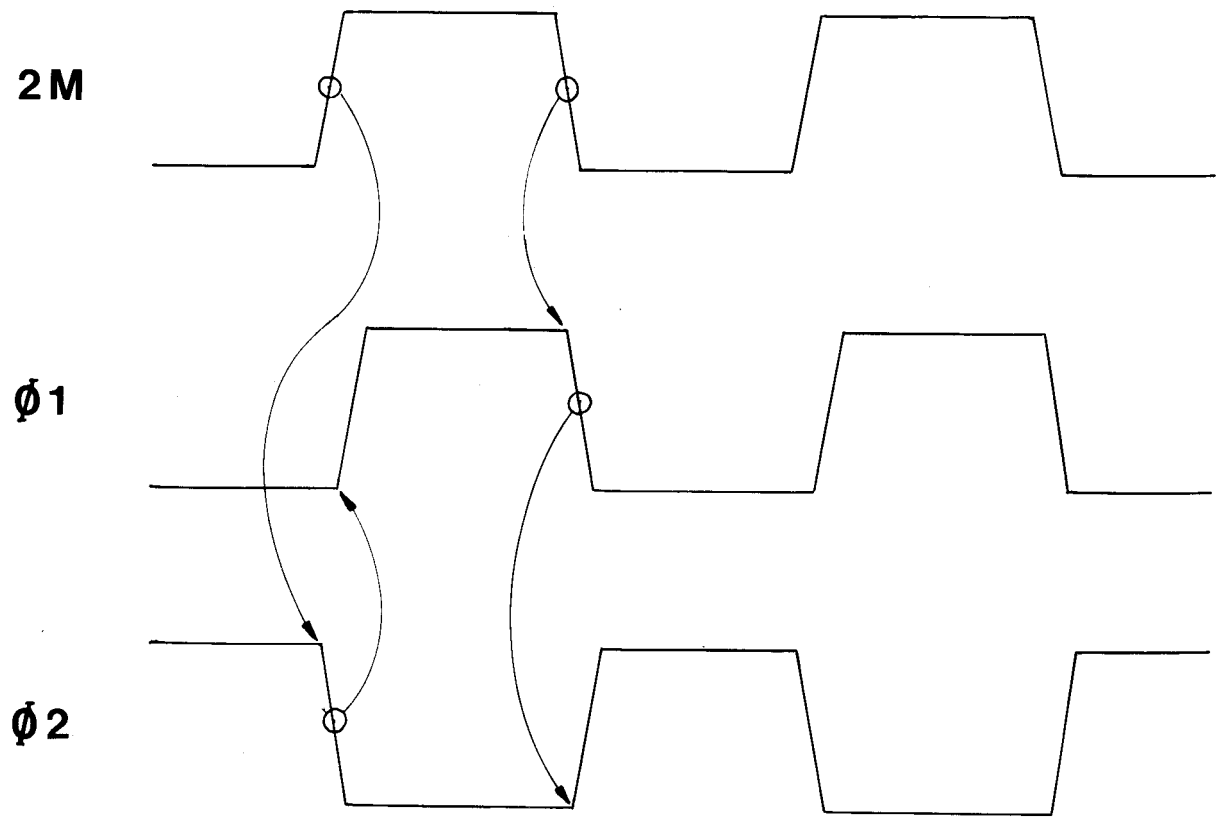


Figure 1 Non-overlapping clock inputs phil and phi2

Phil and phi2 are generated by IC33, two gates of which are used to build an R-S latch. Not2M from IC26 is used to set and reset the R-S latch which toggles at 2MHz unless a third gate from IC33 blocks the not2M signal. During 2MHz operation the phi2 clock corresponds to not2M, the inverse of 2M from the video processor.

When accessing slow devices (1MHz extension bus, ADC, VIAs, 6845, ACIA, and serial processor) the clock is stretched to give a pseudo 1MHz cycle. The system 1MHz clock, E, is generated in half of IC25 from the 1MHz and 2MHz outputs of the video processor. The other half of IC 25 is used to synchronise the transition from 2MHz to 1MHz clocking. Each 1 MHz peripheral select line is connected to an input of NAND gate IC41. If any input of this NAND gate is taken to logic 0 then a 1MHz CPU cycle will occur. For 1MHz cycles phi2 is held at logic 1 until the 1E signal is synchronised. The cycle ends with both phi2 and 1E falling together.

There are two ways in which the transition from 2MHz to 1MHz takes place depending on which phase 1E was on when the request was received from IC41, see figure 2.

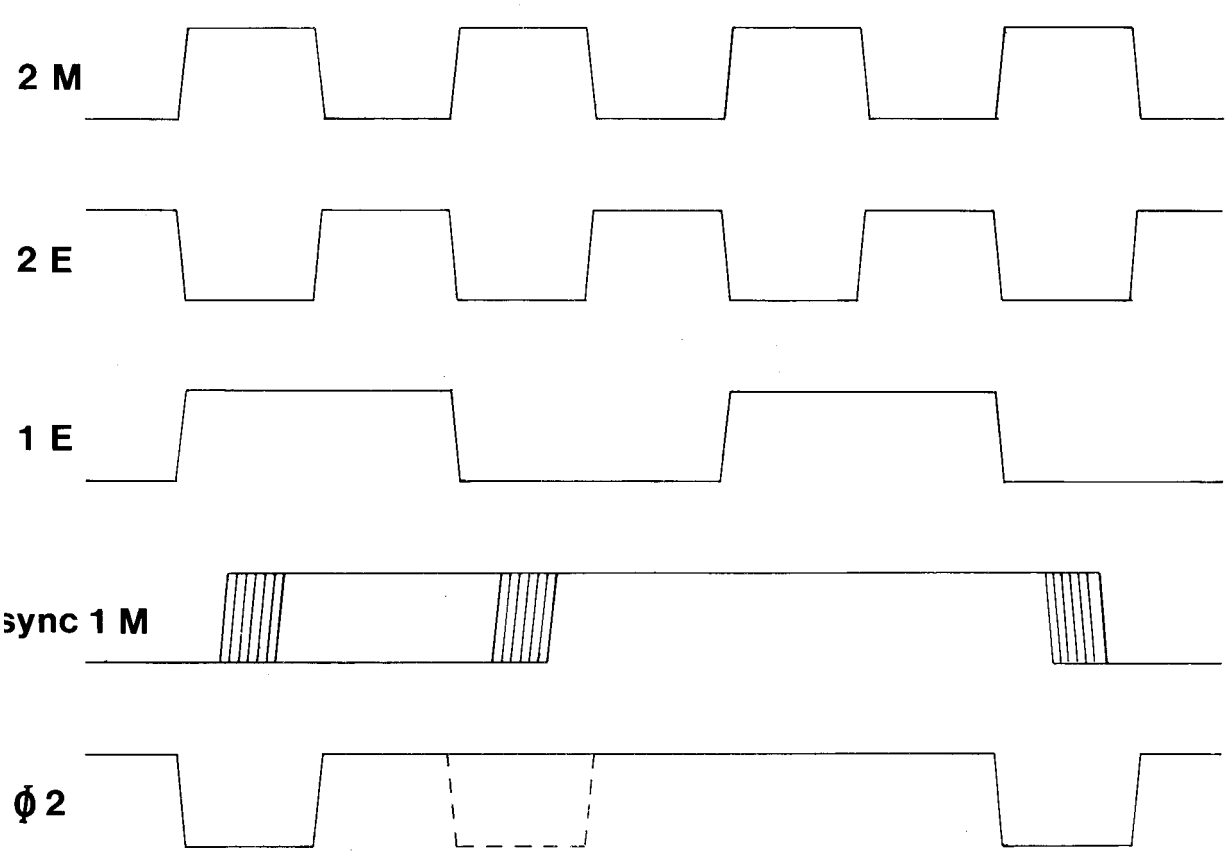


Figure 2 2MHz to 1MHz transition

5.3 Reset circuitry

The system has two reset circuits, one is a general reset from a 555 timer (IC43)., the other is an RC network which just resets the system VIA (IC20) on power-up. This allows the software to detect the difference between a power-on reset and a BREAK key reset. The keyboard BREAK key connects via S10 (a PCB made link) to the 555 timer. The 555 generates reset pulse RS which is inverted to give the CPU notRS signal.

5.4 Address decoding and memory

Figure 3 shows the memory map.

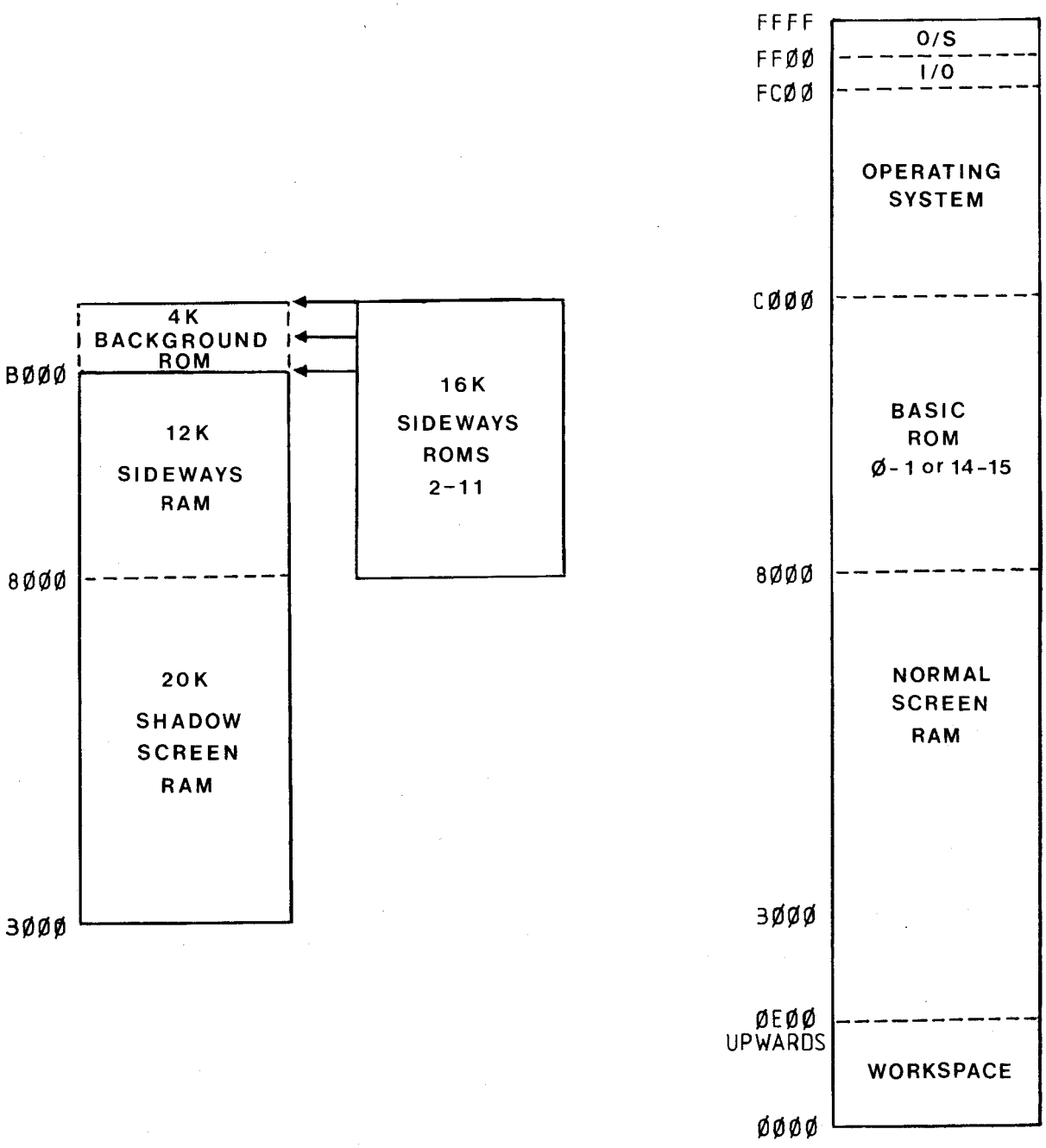


Figure 3 Memory map

At the heart of the memory selection is the programmable array logic (PAL) chip IC36. It selects which screen RAM is in use (normal or shadow); it controls the sideways ROM select latch IC45; it selects the paged RAM.

5.4.1 ROM operation

Any ROM socket on the PCB can either hold an 8K, 16K or 32K BYTE device. 8K or 16K IC's are paged into the memory map from &8000-&9FFF or from &8000-&BFFF respectively, a 32K device provides two 16K banks of memory paged into the memory map from &8000-&BFFF. The extra address line A14 (QA from IC45) required by 32K devices is available to each ROM slot when the appropriate molex link is altered. The ROM socket IC numbers, their corresponding ROM select numbers and their corresponding link numbers are shown in figure 4.

IC No	ROM Nos	Link No	Notes
IC35	2/3	S9	Molex link made W as standard for 8K/16K use
IC44	4/5	S11	" " "
IC57	6/7	S12	" " "
IC62	8/9	S15	" " "
IC68	10/11	S18	" " "
IC71	0/1 or 14/15	S19	PCB cuttable link made E as standard for 32K (16K operating system and I/O and 16K BASIC)

Figure 4 ROM socket IC numbers, ROM numbers, and device selection link numbers

As can be seen from figure 4, ROM numbers range from 0 to 15. ROMs are prioritised, the highest ROM number language and filing system will be selected after a 'hard' reset. 15 has the highest priority, 0 the lowest. So if two or more sideways ROMs are language ROMs, then the computer will start up in the language in the highest number ROM slot. Similarly for filing system ROMS.

IC35, 44, 57, 62, and 68 we shall call "user ROMs". Each user ROM socket is functionally identical and can contain language or service ROMs. IC71 we shall call the "system ROM".

The system ROM contains the operating system. The operating system is always in the memory map from &C000-&FFFF and must always be fitted in IC71. As standard, the computer ones with a 32K ROM for IC71. It contains the operating system and the BASIC language. For this reason link S19 is hard wired East in the 32K position.

The BASIC part of the system ROM occupies one of four sideways ROM numbers. As standard, any call made to ROM 14 or 15 selects BASIC, and any call to ROM 0 or 1 is ignored. Hence BASIC occupies the highest priority ROM slot and the computer will start up in BASIC. If molex link S13 is moved from South to North then any call made to ROM 0 or 1 will select BASIC, and any call to ROM 14 or 15 will be ignored. This allows the user to select an alternative language at power-on (the language entered at start-up will be the one with the highest socket number when more than one language ROM is fitted).

Address decoding is carried out by the PAL (IC36) and this then selects either the operating system (if the address is in the range &C000-&FFFF) or the current sideways ROM (if the address is in the range &8000-&BFFF). Part of IC40 disables the ROM output drivers when an I/O address occurs (&FC00-&FEFF).

The currently selected ROM number (0-15) is held in the ROM select latch IC45. The ROM select latch is mapped into the memory at address &FE30 via the PAL IC36. When writing to this address, the four data lines D0-D3 provide the ROM number which is latched into IC45, see also 5.4.2.

When the PAL decodes an address from &8000-&BFFF, IC36 pin 18 goes low and enables IC46. IC46 is a three line to eight line decoder which selects the particular IC socket allocated to the ROM number, in IC45. The least significant bit held in IC45 is fed to the relevant ROM socket only if the link for that socket is made E for a 32K device. The correct half of the 32K device is then selected to be placed in the memory map.

5.4.2 Paged RAM operation

The 12K paged RAM is selected with a ROM number between 128 and 255 (D7 set). The top bit of the data bus D7 is available to the PAL IC36. Writing to the ROM select latch at address &FE30 as described in 5.4. 1, will save D7 in the PAL. D0-D3 are stored as normal in IC45. If D7 is set (logic 1) then the PAL selects the 12K paged RAM when the CPU address is in the range &8000 to &AFFF. If the ROM selected by D0-D3 is present then the top 4K of that ROM will also appear in the memory map, above the 12K paged RAM, from &B000-&BFFF. As ROM 0 is not allocated as standard (it is BASIC if S13 is changed), writing 128 to the ROM select latch will merely place the 12K paged RAM into the memory map and &B000-&BFFF will be vacant.

5.4.3 RAM access

There is 64K of installed RAM.

RAM access is dependent on whether the computer is in normal mode or shadow mode, and the differences are shown in Figure 5.

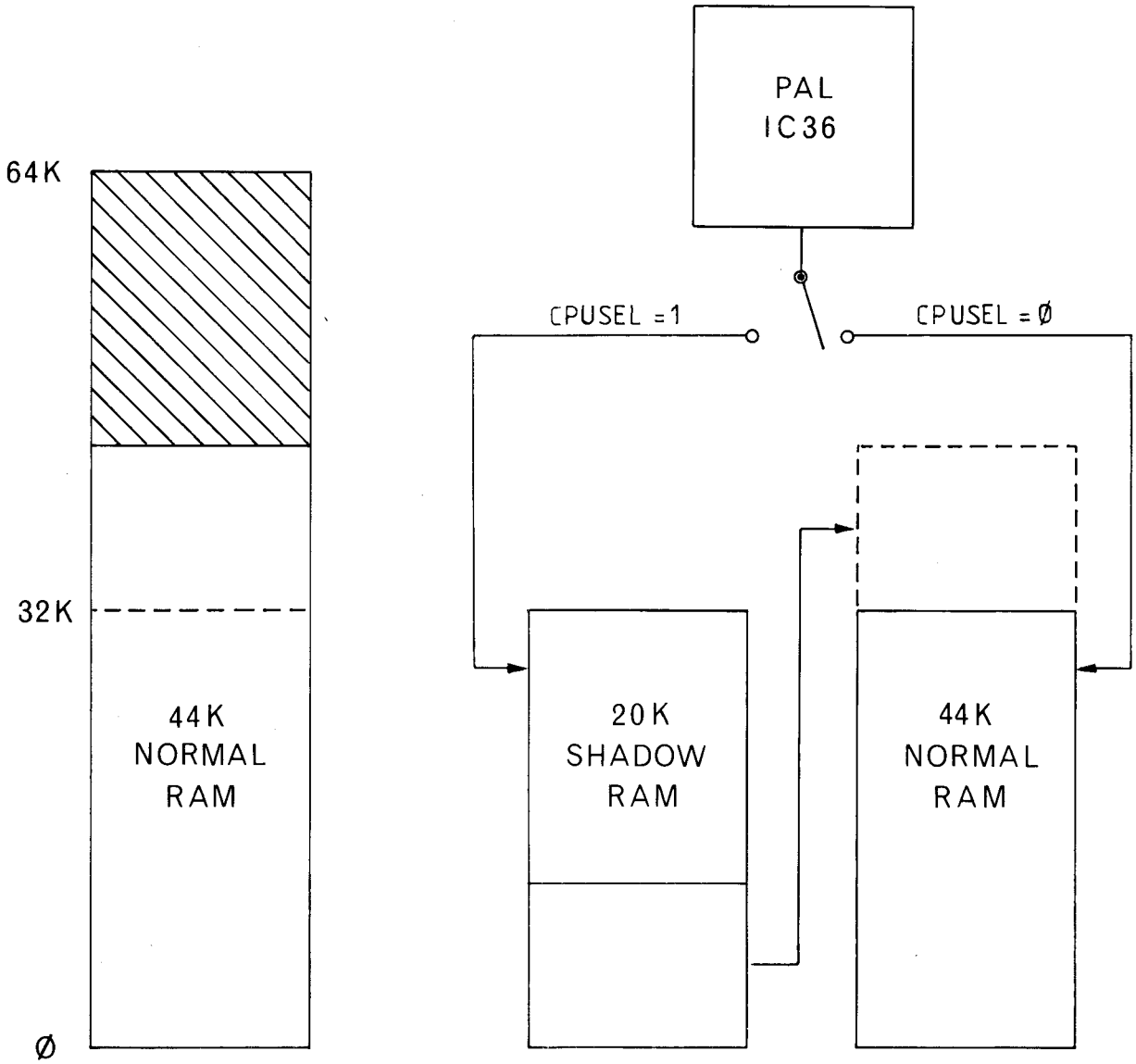


Figure 5 RAM access in normal and shadow modes

In normal mode the RAM can be thought of as 44K from address &0000-&AFFF. The top 12K of this RAM from address &8000-&AFFF is paged into the memory map when required in place of the bottom 12K of the sideways ROM space, see 5.4.2. The remaining 20K of RAM is set aside for the shadow screen memory, while it always exists, it is not available to the system in normal mode. The bank of 44K RAM we shall call "normal RAM". In normal mode, VDUSEL (IC36 pin 17) is always zero.

Any code executing anywhere within normal RAM in normal mode will always access normal RAM, it cannot access shadow RAM.

In shadow mode the RAM can be thought of as 44K from address &0000-&AFFF, plus a parallel bank of 20K RAM from address &3000-&7FFF which we shall call "shadow RAM". As in normal mode, the top 12K of normal RAM is paged into the memory when required. In the address range &3000-&7FFF the PAL (IC36) is able to switch between shadow RAM and normal RAM. It selects access to the shadow memory if a) shadow mode is on b) it detects a VDU driver and c) the operand address is between &3000 and &7FFF, the part of the memory map used by the screen. Otherwise it selects access to normal RAM. The machines logic is set to shadow mode when logic 1 is written to D7 at address &FE34, this causes pin 17 (VDUSEL) to go high. &FE34 is the address of a register in the PAL and when D7 is set any screen access through the VDU drivers will cause the PAL to switch in the shadow memory by making pin 12 (CPUSEL) high. In shadow node, VDUSEL is always set, and CPUSEL is low to access normal RAM and high to access shadow RAM.

When the paged RAM is selected in shadow mode, the top 4K, &A000 to &AFFF, is programmed by the PAL (IC36) to have the attributes of VDU drivers.

Any code executing between &0000-&9FFF in shadow mode will always access normal RAM.

Any code executing from sideways RAM between &A000-&AFFF will access the shadow RAM (if selected) when the operand address is between &3000-&7FFF. This special attribute is not available to any other sideways memory, ROM or RAM.

5.4.4 RAM circuitry

The 64K installed RAM is provided by eight 64K by 1 dynamic memory devices ICs 55, 56, 60, 61, 64, 65, 66, and 67. Figure 6 shows the RAM timing diagram.

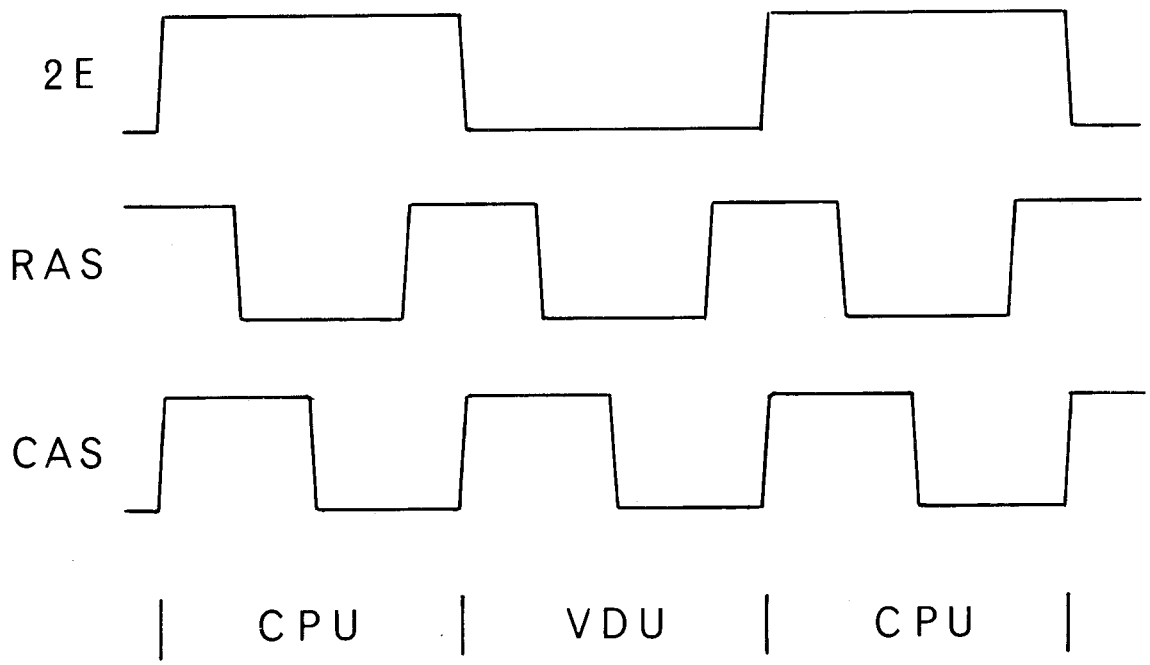


Figure 6 RAM timing diagram

The RAM control circuit is designed to work with either 128 or 256 refresh cycle DRAMs, refresh being provided by the 6845 CRTC (IC78) in conjunction with two ex-OR gates of IC63 and an AND gate of IC34.

The RAM is accessed at 4MHz, the CPU and VDU each having 2MHz access.

The address multiplexers for the VDU cycle are ICs 72, 73, 74, and 75. Various combinations of the inputs of these ICs are used depending on the screen mode in use. In particular, TELETEXT mode 7, with its own character generator (IC59) is markedly different from the other seven bit-mapped modes 0-6.

The address multiplexers for the CPU cycle are ICs 50 and 51.

RAM is working (being addressed and strobed) the whole time, both during CPU and VDU phases, even when not required (except for the purpose of refresh). But data to or from the RAM is only available to the CPU, when the data buffer IC49 is enabled. This occurs when any input to the NAND gate in half of IC40 goes low, that is when A15 is low (address between &0000-&7FFF) or if the paged RAM signal fran IC36 is low (address between &8000-&AFFF and paged RAM selected), or if the video processor (VIDPROC) is enabled (address &FE20). RAM is disabled when the VIDPROC is written to, by holding notCAS at logic 1 (see IC23).

5.5 Disc interface

There are two floppy disc interfaces which can be fitted to the PCB, based on either the 8271 floppy disc controller for FM only, or the 1770 floppy disc controller for FM and MFM.

5.5.1 8271 FDC

Two open collector buffer ICs are used to drive the disc unit. A 7416 (hex inverter, IC8) is used to invert the "true' control signals output by the controller IC15. Two gates from a 7438 (quad NAND gate, IC7) generate the two drive select signals by combining the controller's drive select lines with the load head signal (used as a motor control line).

Each data pulse from the drive triggers/retriggers a monostable pulse generator IC1. The pulse clears an R-S latch formed by two cross-coupled NAND gates (IC9), and clears the bit interval timer formed by two divide by sixteen circuits (IC2) and a NAND gate (IC9). If the bit interval exceeds the time determined by the bit interval timer then the latch will be set (DW=1). The 8271 monitors the latch (the data window) and the read data pulses to decode the serial data stream.

If the latch is reset (DW = 0) when a data pulse occurs, the 8271 interprets the bit value as logic 1; conversely if DW = 1 then the data bit is a logic 0. Logic 0 bits are encoded as 8us between RD pulses, logic is as 4us, and each bit interval is 8us.

The bit interval timer is designed to detect an interval of approx 6. 5us.

Disc speed is measured by timing the interval between index pulses, which are nominally 200ms apart. One interval timer IC4 is used for both RDY0 and RDY1. 16/13 MHz (1.2307MHz) is used to clock a binary counter (IC4). When all drives are off, the MOTOR signal will be high (off). Motor off forces both stages of IC3 to predefined states, IC3 pin 13 is high and IC3 pin 2 (notRDY) is high. A drive is turned on when MOTOR goes law. IC3 can now be clocked by index pulses and so detect the state of the digital timer IC4.
If IC4 pin 11 goes high then the interval between index pulses is greater than 213ms (2^18*812.5ns),and the disc speed is too slow. If IC4 pin 11 is still at logic 0 when an index pulse occurs then the disc speed is taken to be almost right, so that after one additional disc revolution the speed can be assumed within working limits. IC3 pin 13 is clocked low if IC4 pin 11 is low when an index pulse occurs. If IC3 pin 3 is still low at the next index pulse then IC3 pin 2 will go law, indicating that the drive is ready. Diode Dl and resistor R2 OR the MOTOR signal and the state of IC4 pin 11. The OR function means that whenever IC4 pin 11 goes high it will set IC3 pin 13, and the RDY generation sequence is returned to the beginning. Resetting IC3 by IC4 pin 11 avoids a false RDY if the drive is very slow, when IC4 pin 11 might go high then low between two index pulses.

Communication between the 8271 disc controller and the microprocessor occurs at two levels:

Commands to the disc controller are made by normal program controlled accesses to the I/O space between addresses &FE80 and &FE83.

Bytes of data transferred between the disc and the controller are processed using an NMI interrupt routine which demands immediate action from the CPU. The interrupt program code accesses the 8271 at address &FE84; this address is for DACK controlled transfers. When a DACK controlled transfer is required the 8271 generates an interrupt by setting pin 11 high (of IC15). The interrupt request is inverted by IC7, an open collector NAND gate, to become notNMI. NotNMI is a wire NUR signal which passes directly to the CPU notNMI input (IC42 pin 6) via an AND gate (IC34).

Address decoding for the disc controller is done by three ICs.

IC22 pin 8 goes low when the CPU address is greater than &FC00, and so enables the I/O decoding logic. IC21 generates the notFDC signal which is low for address values &FE80 to &FE9F. The final decode is by IC28 which splits the notFDC space into blocks of four using the A2 address. IC28 pin 12 is low for &FE80 to &FE83 which is the notCE address for the 8271 disc controller. NotDACK is low for &FE84 to &FE87. Pin 15 of IC28 is held permanently low (link S7 West) as 8271 interface timing is controlled by not2M through the notR and notW signals (from IC27).

5.5.2 1770 FDC

The 1770 is expected to be the standard disc interface. A 1770 operates in either single density (FM) or double density (MFM) mode, and has data separator and disc speed decision logic built in. A much simpler disc interface results: ICs 1, 2, 3, 4 and 9 are not needed. No drive select logic is incorporated in a 1770 so IC17 is fitted for this function. IC17 also latches two contol signals which are used to select between FM and MFM
operation and to reset the 1770, both under program control.

The control register IC17 is a write only device which occupies the address space &FE80 to &FE83. IC23 gates the decoded address signal with notW (IC27 pin 6) to form the control register clock.

All 1770 registers are addressed in the range &FE84 to &FE87.

It can be seen that the 1770 controller and the 8271 controller address space has been swapped. This is to allow the disc system software to distinguish between the two devices.

Two interrupt signals come from a 1770, pins 27 and 28. The two interrupts are inverted and wire NORed on to the notNMI line by two parts of IC7 (quad NAND gate). Link S8 selects between the single interrupt of an 8271 and dual interrupt of a 1770. When a 1770 is fitted S8 must be made. For the 1770 option link S7 is made East, this incorporates not2M into the chip select signals and so defines the timing of data transfers between the disc controller and the CPU. Link S5 is available to allow program controlled suppression of 1770 disc controller interrupts (IC17 is not present when the 8271 is fitted). The disable function is not used at present so S5 is not fitted.

5.6 Display circuitry

Three display outputs are provided - RGB, composite video, and UHF.

5.6.1 RGB

Red, green and blue signals are produced by the video processor and are then buffered by Q1, Q2, and Q3 to be fed to the DIN socket (SK3) at TTL type levels. The fourth signal required at the RGB output is a composite SYNC (CSYNC) generated from horizontal sync and vertical sync of the 6845. CSYNC polarity can be altered using link S27. The 0V and +5V power supply also appears on SK3.

5.6.2 Composite video

Composite video is a summation of the three primaries (red green and blue) to give a grey scale, mixed with negative CSYNC. The order from darkest to lightest is: black, blue, red, green, magenta, cyan, yellow, white. The grey scale is set by the resistor values 8101, 8104, and 8108. These feed Q8 which produces a 1V peak to peak signal on BNC connector SK2. The chroma component described in 5.6.3 may be added to the composite video by making link S26. The voltage ratio of chroma to luminance is defined by C48.

5.6.3 UHF

Red green and blue are summed by resistors R82, R84, and R93 and fed into Q6 to create a grey scaled luminance (or luma) signal. Diodes D12, D13, and D14 boost the luminance level for colours to compress the grey scale. Resistors R107 and R138 mix the luma and negative CSYNC respectively while 8139 and
R146 trim the DC level of the "video" waveform fed to the UHF modulator. Chroma is added through C49. The modulator generates an amplitude modulated UHF signal on TV channel E36 (591.25MHz).

The chroma signal is an amplitude and phase modulated 4.4336MHz simulated sine wave which is added to the video signal. For neutral colours, white/black/grey, the chroma amplitude is zero. For other colours the phase of the chroma signal determines the colour while the chroma amplitude fixes the colour strength. The chroma phase is measured, in the TV, against a reference set by locking to the (average) colour burst. A 17,734,475Hz (+/-100Hz) oscillator is used to generate the colour subcarrier master clock. VC1 allows adjustment of the clock frequency. Two D type registers form a ring counter which generates two phase shifted 4.4336MHz signals (1C79 pins 6 and 9). All chroma signals are derived by mixing cambinations of the two master chroma signals or their inverse with a bank of ex-OR gates. For PAL (Phase Alternation by Line) the chroma signal reference phase is shifted 90 degrees on alternate lines. An exclusive-OR gate (1083) driven from half of IC69 modifies one of the ring counter outputs to cause the required phase alternation.

For NTSC operation, link S28 can be changed to give a constant reference phase (IC83 pin 13 to 0v) - R92 must be removed for NTSC, and the crystal X2 must be 4 times the colour carrier frequency of the NTSC broadcast standard (eg 14.318MHz for USA).

The chroma waveform phase and amplitude are selected by the red green and blue (RGB) signals from the video processor. RGB controls the six ex-OR gates (IC86 and IC83) to direct the required phase(s) of 4. 4336MHz to the NAND gate array (IC87 and IC90) and to enable the appropriate NAND gates. Resistors R85 to R92 mix the NAND gate outputs to form a single chroma signal, including the colour burst. R86 and R89 are used to match the DC level from the resistor mixing network for all colours, but not the colour burst. A crude low Q tuned circuit formed by Ll and C40 filters the chroma signal before it is buffered with the emitter follower Q9. R114 and R120 bias Q9 and also offer a suitable termination to the filter. Q9 then drives the signal mixing point to form the complete colour video signal used to drive the UHF modulator. The impedance of C49 (at 4.4336MHz) fixes the voltage ratio of chroma to luma in the modulator drive signal. C48 serves the same purpose, when link S26 is made, in mixing chroma into the video waveform available at SK2.

5.7 CENTRONICS compatible printer interface

The computer can drive a centronics compatible printer through IC10, a 6522 VIA. Port A of the VIA is configured as an 8-bit output port which is buffered by IC5 and fed to PL9. Printer strobe pulses are generated by a program sequence which toggles CA2 (IC10 pin 39) high-low-high. Strobe pulses are typically 4us wide.
ACK from the printer is connected to CA1 (IC10 pin 40). ACK is pulsed low for approximately 5us by the printer when it is ready for the next character/byte transfer.

5.8 User port

Port B of IC10 offers eight individually programmable input/output lines, and two programmable control lines, connecting to PL10.

5.9 1MHz extension bus

The 1MHz bus is a fully buffered interface to the CPU via PL11, which operates with lus transfer cycles. IC12 (bidirectional buffer) is enabled when either FRED or JIM is accessed (pages &FC and &FD). These two pages are decoded by IC22 and IC28, with signals notFRED and notJIM appearing on pins 4 and 5 respectively of IC28. When either notFRED or notJIM goes low, the 1MHz bus enable goes low (IC34 pin11), and takes low an input of the NAND gate IC41 thus causing a 1MHz CPU cycle.

NotFRED (IC28 pin 4) and notJIM (IC28 pin 5), along with R/notW (IC24 pin 10) and 1MHz bus enable (IC34 pin 11) are synchronised to the 1MHz system clock (1M) by latching them in IC32. This ensures that no glitches occur on the 1MHz bus interface.

5.10 TUBE interface

The TUBE interface connects to a second processor via PL12. The signals present are the eight data lines, five address lines A0 to A4, R/notW, 2E, notRS and notIRQ. The 'data lines are buffered by IC14, and the address lines, R/notW and 2E are buffered by IC13. The data buffer IC14 is enabled when a TUBE address (&FEE0-&FEFF) is decoded by IC21, this enable signal (notTUBE) being fed also to the TUBE connector, PL12.

Rll is fitted so the computer OS can detect when there is no second processor present (or powered on).

5.11 ECONET

ECONET is based around the 68B54 (IC81) advanced data link controller. IC81 performs the conversions between serial and parallel data, and generates the interrupt requests which are connected to NMI. Each byte transfer between network and CPU is requested by an NMI. Interrupts can be disabled by making pin 4 IC23 low thereby setting the D-type (half of IC69), which is achieved by a read of &FE18. Reading this address returns the station ID number which is set up on the links S23. Interrupts are enabled when pin 2 IC69 goes low (a read of &FE20) , which, when clocked by not2E, resets the D-type.

Transmit data from the 68B54 is fed to a differential line driver circuit IC91, and then through SK7 on to the twisted pair network cable. The differential drive voltages are, typically, 0.25V and 3V. A monostable (half of IC88) is used to time-out the ECONET line driver by taking pin 9 IC91 low after approximately 4.5s (longer than the time required to transmit a maximum length data packet). This is designed to prevent a single computer holding its driver on and thereby bringing the whole network down.

Receive data is decoded by a comparator circuit IC92 and fed into the 68B54. IC93, the collision detect ciruitry, is not fitted because the software protocols should prevent any collision. Before transmission, the line is sampled to see if it is in use. If it is, the transmission is held up until a certain time after the line is first free again. This time is dependent on the station ID and so will be different for every station on the line. When required collision detect may be installed by fitting components as shown on the circuit diagram, and breaking the link S29, a PCB copper link.

5.12 Cassette and RS423 ports

For both the cassette (SK5) and RS423 (SK4) interfaces, a 6850 asynchronous communications interface adaptor (ACIA) IC82 is used to buffer and serialise or deserialise the data. The serial processor IC85 contains two programmable baud rate generators, a cassette data/clock separator, switching to select
either RS423 or cassette operations, and also a circuit to synthesise a sinewave to be fed out to the cassette recorder.

Note that the receive bit rate for cassette operations is derived from the FSK signal not from the serial processor control register bits used when RS423 operation is selected.

IC18 divides the 16MHz clock signal by 13 (1.23 MHz) and this signal is divided further within the serial processor to produce the synthesised 2400/1200Hz cassette record signal, and the bit rate clocks. Automatic motor control of an audio cassette recorder is achieved by using a small relay driven by transistor Q7 from the serial processor.

R66 and C30 provide the necessary timing elements for delay between receiving the high tone run-in signal and asserting the data carrier detect signal to the 6850.

The signal caning from the cassette recorder is buffered, filtered and shaped by three stages of the LM324 amplifier IC89.

The RS423 data in and data out signals and the request to send output RTS and clear to send input CTS signals are interfaced by ICs 94 and 95 which translate between TTL and standard RS423 signal levels +5V and -5V.

RS423 signals are compatible with the RS232 signals common in computer related equipment.

Selection of the cassette or RS423 for input and output is by bit 6 of the serial processor control register, bit 7 is for cassette motor control. Bits 0 to 2 control the transmit bit rate, while bits 3 to 5 set the RS423 receive bit rate.

5.13 Analogue to digital convertor

The A to D circuit is based on a uPD7002 IC84, which can accept upto four analogue inputs, from SK6. The voltage reference is set by three silicon diodes, D9, D10, and D11, which gives a typical full scale voltage of 1.8V. When a conversion is complete, the CPU is interrupted via CB1 of the 6522 (IC20 pin 18) which generates an IRQ (IC20 pin 21) .

5.14 Audio circuitry

IC38 is a four-channel sound generator which can be programmed to vary the frequency and volume of three independent tone generators and the amplitude of a single noise generator. The sound signal is DC " restored" by mixing in a signal derived from the sound envelope. An inverting peak detector (IC47 D4 C15 etc.) derives the inverted sound envelope which is then summed with the sound signal in the ratio of 2: 1. Part of IC47 forms a virtual earth summing amplifier which mixes the sound, its envelope, the external audio input and an optional speech signal into one audio channel. The audio is then filtered through a second order low pass filter (approximately 7kHz bandwidth) and applied to the volume control (optional) before final amplification by IC77 an LM386. IC77 drives the internal keyboard mounted 8 ohm speaker via PL15. Plug S20 allows fitting of a remote volume control, when no volume control is fitted a shunt is required on S20 (south) to enable the audio.

The audio output of the optional speech system is filtered by an operational amplifier second order filter (cut-off frequency of 7kHz) before mixing in with the other audio signals. Speech is generated by an optional TMS5220 with TMS6100 (or equivalent) vocabulary "PHROM".

5.15 Keyboard

The keyboard circuit is given in figure 9.6 of the Appendix. The keyboard connects to the main PCB via PL13.

A 1MHz clock signal 1E is fed to a 74LS163 (IC1 on keyboard) binary counter, the outputs of which are decoded by a 7445 (IC3 on keyboard) decoder driver circuit. These outputs drive the rows of the keyboard matrix, each row being driven in turn. If any key is depressed, an 8 input NAND (IC4 on keyboard) will produce an output when that row is strobed and this will interrupt the CPU through line CA2, pin 39 of IC20 on the main computer board. The interrupt tells the computer to enter the key reading software. In order to discover which key was pressed, the CPU loads directly into the 74LS163 (IC1 on keyboard) the address of a key matrix row, allowing it to interrogate each row in turn. Also, the CPU drives the 74LS251 data selector (IC2 on keyboard) with the 'column address' of a single key on the selected row. In this way, the processor can interrogate each individual key in turn until it discovers which one was depressed and caused the interrupt. Once read, the keyboard assumes its free running mode.

6 Upgrading the PCB

The following section gives instructions for adding extra hardware to upgrade the PCB for disc, ECONET, and speech. Dealers and service centres performing these upgrades must also conform to upgrade procedures and requirements as notified by their supplier, and should refer to any available information updates for latest details.

In the following section, items marked * may already be fitted to the board. All ICs are inserted with their pin 1 facing the back of the computer. 6.1 1770 disc option
FM or MFM 5 1/4 inch floppy disc interface.

i) The following parts are required:

IC7	7438 (must not be 74LS38)
IC8	7416 or 7406
IC16	1770
IC17	74LS174

*R1	150R
*R5	150R
*R6	150R
*R7	150R
*R8	150R
*R14	3k3

The appropriate filing system ROM

ii) Insert the ICs listed above into the sockets which should be provided on the main circuit board. If any sockets are missing then solder in the correct DIL socket for that IC. Note: IC16 uses two 14-pin SIL sockets.

iii) Except on early boards, the resistors listed above will already be in position on the PCB. Check each one, and solder in any which are missing.

iv) Insert the filing system ROM into a vacant sideways ROM socket (IC 35, 44, 57, 62, or 68).

v) Make link S7 East with a shunt (probably already in this position), or tinned copper wire if molex pins not fitted.

vi) Make link S8 with a shunt (probably already in this position), or tinned copper wire if molex pins not fitted.

vii) Test using a PORT tester.

Note: the 1770 disc upgrade is usually carried out without soldering.

6.2 8271 disc option

i) The following parts are required:

IC1	74LS123
IC2	74LS393
IC3	4013B
IC4	4521B
IC7	7438 (must not be 74LS38)
IC8	7416 or 7406
IC15	8271
*R1	150R
*R2	10k
*R3	k
*R5	150R
*R6	150R
*R7	150R
*R8	150R
*R9	3k3
*R10	3k3
*R14	3k3
*C1	1n plate ceramic 2%
*D1	IN4148

*16K ROM (DNFS)

ii) Insert the ICs listed above into the sockets which should be provided on the main circuit board. If any sockets are missing then solder in the correct DIL socket for that IC. Note: 1015 uses two 14-pin SIL sockets.

iii) Except on early boards, the resistors, capacitor arid diode listed above will already be in position on the PCB. Check each one, and solder in any which are missing.

iv) Insert the filing. system ROM (DNFS) into a vacant sideways. ROM socket (IC 35, 44, 57, 62, or 68).

v) Make link S7 West with a shunt, or tinned copper wire if molex pins not fitted.

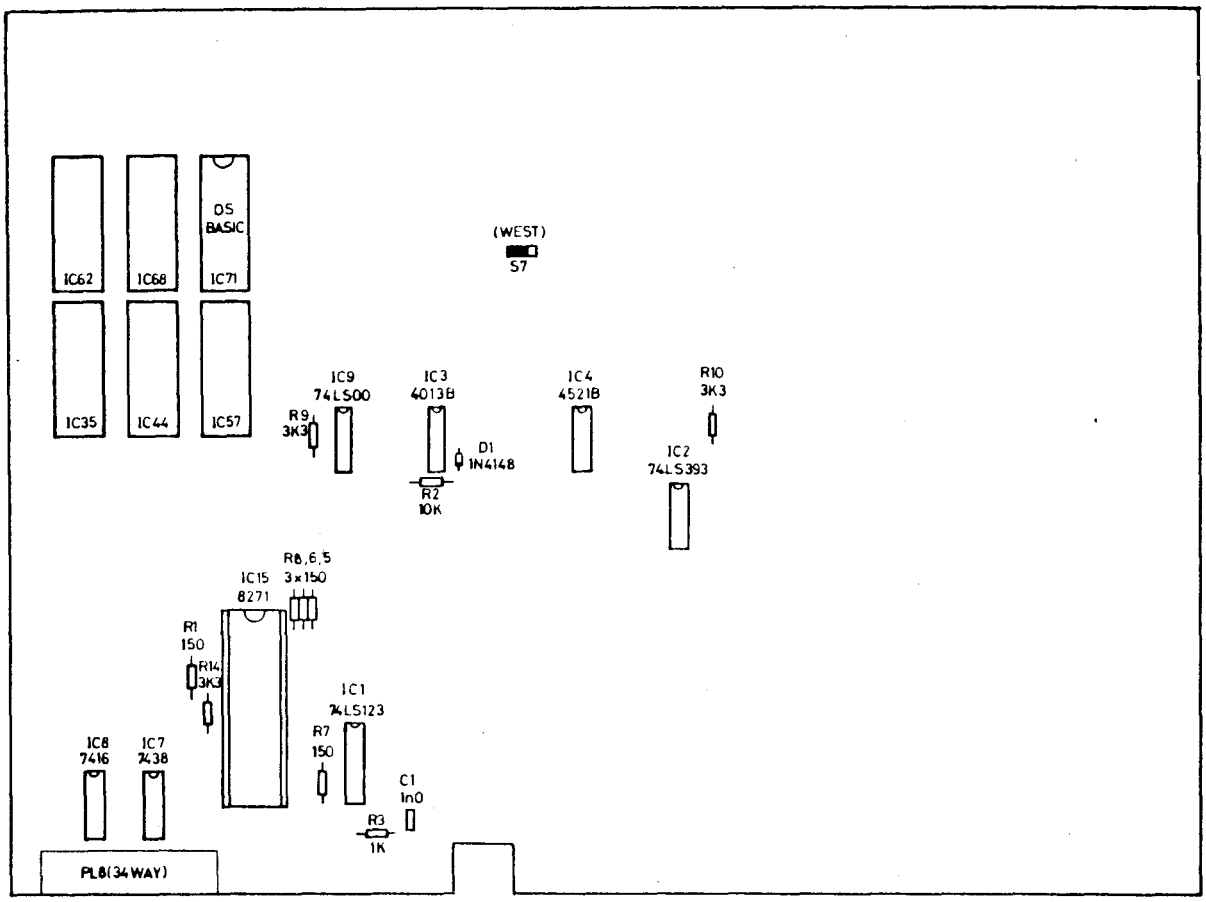
vi) Break link S8 by removing shunt (if fitted).

vii) Test using a PORT tester.

Note: If an 8271 disc interface is being fitted as a replacement for an existing 1770 disc interface, the following items must be removed from the PCB:

IC16	1770
IC17	LS174

Link S8 must be broken.



8271 Disc interface components

6.3 ECONET

Local area network interface

Due to the complexity of this upgrade and the specialised test equipment required, it should only be carried out by ACORN Approved ECONET Service Centres, with the appropriate test equipment. Upgrade procedures and requirements, as notified by suppliers, should also be adhered to and reference should be made to any available information updates for latest details.

i) The following items, from the ECONET Hardware Upgrade Kit, are required to upgrade model B+:

QTY	DESCRIPTION	CIRCUIT REFERENCE
3	RESISTOR 1K0 0.25W 5%	R63,73,148
1	RESISTOR 1K5 0.25W 5%	R147
1	RESISTOR 4K7 0.25W 5%	R59
4	RESISTOR 10K 0.25W 2%	8140,141,142,143
1	RESISTOR 39K 0.25W 5%	R64
4	RESISTOR 100K 0.25W 2%	8106,110,125,134
1	RESISTOR 220K 0.25W 5%	R77
2	RESISTOR 1M5 0.25W 5%	R78,79
1	RESISTOR PACK 8 x 22K	RP2
1	CAPACITOR 10% 6V3 TANT	C57
1	CAPACITOR 47% 10V TANT	C37
1	CAPACITOR 2n2 CER PL 2%	C26
1	IC 68B54	IC81
1	IC 75159	IC91
1	IC 74LS123	IC88
1	IC 74LS132	IC70
1	IC 74LS244	IC80
1	IC LM319	IC92
1	SOCKET DIN 5 PIN 180 DEGREE	SK7
2	CONNECTOR 8 WAY WAFER	S23
7	SHUNT	FOR S23
2	SOCKET 14 PIN DIL	FOR IC91,92
1	SOCKET 28 PINDIL	FOR IC81 (OPTION)
1	CONNECTING LEAD ECONET	
1	Current network filing system ROM (eg DNFS)	

IMPORTANT NOTE: Collision detect circuitry is not included in the model B+ ECONET upgrade. It has been found, following exhaustive tests, that this feature is not required when a BBC Microcomputer is operating within an ACORN ECONET environment. However, it may be required where an ECONET machine is used with equipment which does not include the ACORN NFS software and provision is made for this circuitry to be fitted to the PCB. See below.

ii) If collision detect circuitry is to be fitted, the track link at S29 should be cut before proceeding (see below).

iii) Solder the 14 pin DIL sockets into positions IC91 and 92.

iv) Insert ICs 91 and 92 into their sockets.

v) Solder all the remaining ICs, resistors and capacitors into their correct positions on the PCB. IC81 may be socketed as an option, though this may degrade reliability.

vi) Solder the two 8 way wafer connectors into the PCB in their correct positions and then push the seven shunts onto all but the North-most pins.

vii) Solder the DIN socket into the PCB.

viii) Insert the filing system ROM (eg DNFS) into a vacant sideways ROM socket. Note that, where a B+ machine is already fitted with the 1770 Disc Interface, a DNFS ROM must be fitted in addition to the 1770 DFS ROM already installed.

ix) If collision detect circuitry is required, the additional components given below must be fitted:

QTY	DESCRIPTION	CIRCUIT REFERENCE
1	RESISTOR 1K0 0.25W 5%	R68
4	RESISTOR 56K 0.25W 2%	895,96,98,99
1	RESISTOR 1M5 0.25W 5%	R97
1	CAPACITOR l0nF CER PLT	C28
1	IC LM319	IC93
2	SOCKET 14 PIN DIL	FOR IC93

In addition, the track link at S29 should be cut.

x) In order to complete the ECONET upgrade, the machine must be tested using the approved ACORN ECONET test kit.

6.4 Speech

Speech synthesiser, word PHROM, and serial ROM socket

i) The following parts are required:

IC29 5220
IC37 6100 PHROM

15-way single sided edgecard socket (2 off)

10-way right angle wafer plug

10-way connecting lead with sockets fitted

100n disc ceramic capacitor (2 off)

ROM socket cover

ii) Add components other than ICs listed above to keyboard assembly as shown in figure 7.

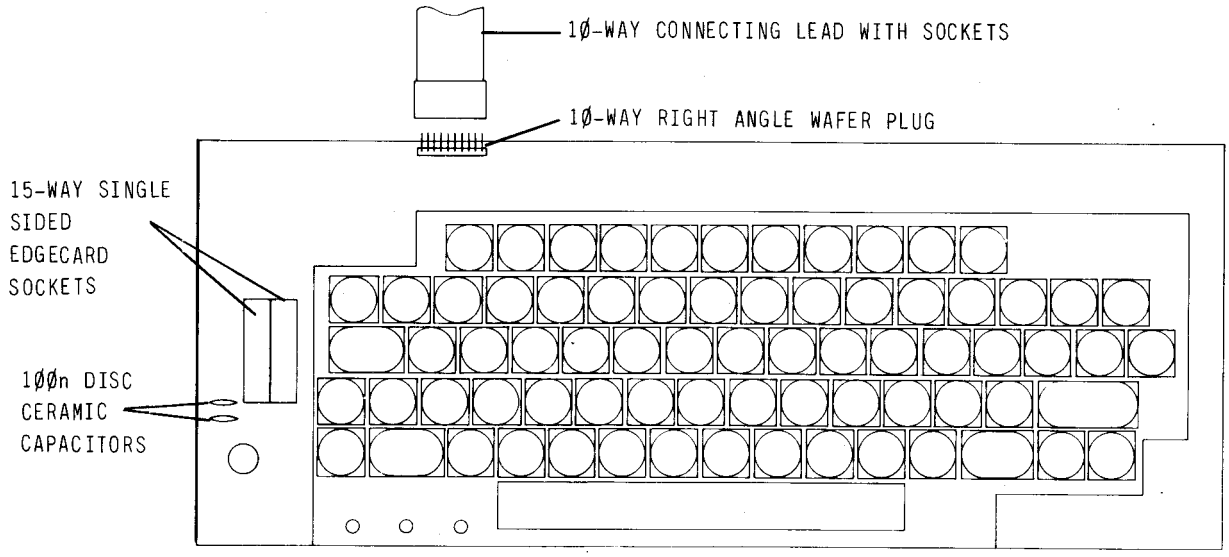


Figure 7 Keyboard assembly

iii) Plug the other end of the ribbon cable into PL14 on the PCB.

iv) Test for continuity between the following points for each edge connector in turn:

Edge connector pin number 6 7 8 9 10 11 12 13 14 15
IC37 pin number 1 3 4 5 6 7 10 11 13 14

Note: on the edge connector pin 1 is nearest the loudspeaker, thus the polarising key is pin 3, and pins 4 and 5 are empty.

Also check that there are no short circuits between any of the edge connector pins.

v) Insert IC29 and IC37 into their sockets on the PCB.

vi) Turn the computer on and type:

```
REPEAT SOUND-1,GET,0,0:UNTIL0
```

and press the RETURN key.
Any key now pressed should cause the system to utter a word or sound.

vii) Adjust VR1 until the speech is at the correct pitch. This can be measured by connecting a frequency meter to pin 3 IC29. Adjust VR1 until the meter reads 160kHz +/-100Hz.

viii) Remove the perforated section from the left of the case lid, fit the ROM socket cover, and reassemble the machine.

ix) Test using a PORT
tester.

7 Selection links

This section describes the function of each of the links on the PCB, the type of link, and its position as standard.

S1 PCB track, made West: West for 5 1/4" disc drive, East for 8".

S2 PCB track, made North: North for 5 1/4" disc drive, South for 8".

S3 PCB track, made South: South for 5 1/4" disc drive, North for 8".

S4 PCB track, made South: South for 5 1/4" disc drive, North for 8".

S5 wire link, not fitted: allows disc filing system to disable NMI. This feature is not supported by current disc software.

S6 PCB track, made South: South for 5 1/4" disc drive, North for 8".

S7 plug, made East: East for 1770 floppy disc controller, West for 8271.

S8 plug, fitted: fitted for 1770 floppy disc controller, removed for 8271.

S9 plug, made West: West for 8K/16K ROM/EPROM in IC35, East for 32K ROM/EPROM in IC35.

S10 PCB track, made East: East enables keyboard BREAK key, West forces permanent reset, broken (neither East nor West) disables BREAK key.

S11 plug, made West: West for 8K/16K ROM/EPROM in IC44, East for 32K ROM/EPROM in IC44.

S12 plug, made West: West for 8K/16K ROM/EPROM in IC57, East for 32K ROM/EPROM in IC57.

S13 plug, made South: South causes BASIC to take high priority ROM numbers 14/15, North causes BASIC to take low priority ROM numbers 0/1.

S14 plug, made North: North gives white on black video, South gives black on white video. Beware monitor performance in the latter configuration.

S15 plug, made West: West for 8K/16K ROM/EPROM in IC62, East for 32K ROM/EPROM in IC62.

S16 - test link not present on issue 2 or later PCB.

S17 PCB track, made North: North configures 1MHz bus audio for input, South for output.

S18 plug, made West: West for 8K/16K ROM/EPROM in IC68, East for 32K ROM/EPROM in IC68.

S19 PCB track, made East: East enables BASIC part of OS/BASIC, West disables BASIC and leaves just the operating system.

S20 plug, made South: South gives full volume on audio. Remove if VR2 fitted.

S21 - optional audio output prior to volume control.

S22 -

S23 eight plugs, seven shunts: ECONET ID number set up as binary number by user. Only fitted if ECONET interface fitted.

S24 wire link, not fitted: optional termination resistor for RS423. Should not be fitted for correct operation of RS423.

S25 wire link, not fitted: optional termination resistor for RS423. Should not be fitted for correct operation of RS423.

S26 wire link, not fitted: made adds chrominance component to composite video output.

S27 plug, made South: South gives negative-going CSYNC for RGB, North gives positive-going CSYNC.

S28 PCB track, made North: North for PAL video circuitry, South for NTSC. Note: for NTSC operation R92 must be cut out. The modulator may need changing for TVs which cannot receive channel 36.

S29 PCB track, made: made for operating ECONET without collision detect hardware. Collisions are detected by software protocols.

S30 PCB link, made: always made for 6512 CPU.

8 Test equipment

A PORT tester is available for the microcomputer. This is an uprated version of the old FIT tester. It will check the DRAMs, and all the I/O ports on the microcomputer: disc, printer, user, 1MHz bus, TUBE, UHF, video, RGB, RS423, cassette, A to D, and ECONET. To use this tester, the microcomputer must at least have the CPU running and the MOS/BASIC ROM working and sane of the
RAM working.

Full operating instructions are supplied with the equipment.

9 Fault finding

This section goes step by step through fault finding in each section of hardware. It should be studied in conjunction with the circuit diagram and block diagram in the Appendix.

If any part of the machine is suspected of being faulty, the following points should always be checked first:

1 no loose connectors and broken cables

2 no broken or shorting tracks

3 ICs plugged into their sockets correctly

4 power supply working and reaching the components concerned

5 all digital signals are at clean TTL logic levels (greater than 2.4V for 1, less than .5V for 0). On timed signals this must be true for the period 150ns before phi2 on read cycles and 300ns before phi2 on write cycles.

The following items of test equipment are required for fault finding:

PORT tester

10A Multimeter

logic probe

20MHz dual beam oscilloscope

TV, composite monitor, colour monitor

cassette player

disc drive

frequency counter

5 ohm 5W resistor

9.1 Switch on

Connect the suspect microcomputer to a UHF TV and an RGB monitor. Connect the mains supply and switch on both the monitors and the computer. One of the following will happen.

a) There is noise on the monitor screens (no signal from computer). There is no power-on beep sound (there may be a continuous noise), and the LEDs do not light, or light incorrectly.

Results: either power supply is dead, or there is a fault in the heart of the microcomputer.

Follow the sequence of checks shown below.

1 If there is no noise on power-up, and no LEDs light up then check the power supply (see 9.2).

2 If a PET tester is available then use it. The PET tester will work on the B+ providing the CPU is running and it can access the ROM, although it may give strange screen output, and some of the tests will fail. Please refer to the information manual supplied to dealers for details of the operation of the PET tester when used with the B+. If PET will not work at all then either the CPU isn't running or it cannot access the ROM.

3 Check HS and VS signals (pin 39 and pin 40 IC78) using an oscilloscope. HS and VS should be clean TTL voltage levels, HS pulsing every 64 us and VS pulsing every 20ms.

Results: if they are stuck or floating then carry on with the checks below. If they are working then the CPU must have programmed the 6845 and so must have gained access to the OS ROM. Check using PET (see information manual supplied to dealers). If the signals are there but are not pulsing at the correct intervals then look for a data line fault to CRTC.

4 Check that the notRS pin of the CPU (pin 40 IC42) is high when the computer is switched on. It should pulse low on power-up and when the BREAK key is pressed. If it is stuck low then look for shorts or damaged components around the 555.

5 Check that there is activity on the SYNC (pin 7 IC42) and the R/notW (pin 34 IC42) lines of the CPU. If SYNC is stuck then the CPU has stalled, and R/notW won't be working anyway. Check for address and data bus short or open circuit, or a complete failure to select the OS ROM (see 9.5).

6 Check the CPU clocks. Phi1 and phi2 should be as shown in figure 1 (see section 5.2). If not then check the 2M circuitry from the video processor IC53. IC33 pin 3 should be low. If not then check SYNC 1M at pin 8 IC41 which should also be low. If SYNC 1M is high then check IC25. If SYNC 1M is stuck high then find which one of the inputs to IC41 is stuck low. The 1MHz device attached to this input must be checked.

7 Check activity on the CPU address lines. If after a BREAK the activity starts and then stops, this suggests that the CPU cannot read the OS ROM. Check the OS ROM by replacing it with a known good one. Check that it is enabled and that all address lines are present. Check following BREAK that notOE pulses low at 2MHz (inverse of phi2), and notCS goes low and stays low for a time.

8 Check all clocks from video processor 8M 4M 2M 1M, see 9.3.

9 After BREAK check CRTC notCS pin pulses low (pin 25 IC78).

If all the above checks pass then the machine should do more than exhibit the symptoms stated in (a).

b) The screen synchronises (no noise) but there is only a flashing cursor in the top left corner.

Results: usually caused by a keyboard fault.

Check that the keyboard is connected correctly, see 9.9.

c) The banner message appears, but is incorrect or incomplete.

d) The correct banner message is:

Acorn OS 64K

<filing system>

<language>

>

For example, with a 1770 FM disc filing system and BASIC language the correct banner message is:

Acorn OS 64K

1770 DFS

BASIC

>

Results: the CPU is running and is accessing the OS. Use a PET tester if available (see information manual supplied to dealers). If the banner message is fragmented then check the CRTC address lines for shorts. If the message gives the prompt

Language?

where BASIC is fitted in the example above check S13 and also check the Pg latch. Language? cannot occur when it is a badly fitted IC since the OS and the BASIC are in the same ROM. A badly fitted OS/ROM would prevent the machine powering up.

e) The machine does a start-up beep, and the caps lock LED comes on, but there is no display, or no display on the UHF monitor.

Results: the video circuitry is faulty, see 9.7.

f) There is no fault on power-up.

Results: most I/O faults will not stop the computer and display from working. Use a PORT tester to find out which I/O circuit is faulty.

9.2 Power supply

With the power supply turned off, unplug the three black OV leads and the three red +5V leads and the single purple -5V lead from the PCB.

Connect a 5 ohm 5W resistor across one pair of red and black leads (a pair that were together on the board) and tape the other leads with insulating tape to stop them shorting. Turn on the power supply and measure the voltage across the resistor using an oscilloscope. The voltage must be in the range 4.9V to 5.1V, with a maximum noise of 50mV peak to peak. WARNING: the resistor will get hot.

Repeat the test with the other two pairs of red and black leads.

Results: if any one pair measures zero or a very low voltage then one of the leads is damaged. If all are out of spec then the power supply unit must be changed.

If the +5V lines are good, leave the resistor in place on the last pair and using the other trace on the oscilloscope measure the -5V voltage. Connect both probes to OV and superimpose the traces in the centre of the CRT. Connect one probe to +5V (across the resistor) and the other to -5V (the purple lead). The two traces should deflect in opposite directions, the -5V being between -4.75V and -5.25V.

When all the voltages are correct, switch off the power supply and reconnect the black leads to the PCB on the connectors marked OV.

Set the multimeter to a 10A DC scale and connect it between one of the connectors on the PCB marked VCC and all three red wires together. Turn on the power supply just long enough to measure the current (any length of time may heat up the PCB tracks excessively). The board should draw from 1.5 to 2.2A, depending on its upgrade state.

Repeat the test, after turning off the power supply, for each of the three +5V connectors on the PCB in turn.

Results: if the current at any one connector is zero or very low then look for a broken lead, connector, or PCB track. If all results are zero then there is either a short circuit and the power supply has cut out (likely) or the whole power network has gone open circuit (unlikely). This can be checked by measuring the +5V voltage across the board. Zero voltage means short circuit, +5V means open circuit.

Replace all the power supply leads in their correct positions, red to VCC, black to OV, and the purple lead to -5V.

As a final check, measure the voltage across the power supply pins of a few ICs around the board and check that it is in spec.

9.3 Oscillator and divider circuitry

Using the oscilloscope, check that 8MHz, 4MHz, 2MHz, and 1MHz are available from pins 7, 6, 5, and 4 respectively of the video processor IC53.

Results: if these signals are not present then check that 16MHz is available at pin 8 IC53. If it is then replace IC53. If not then check the crystal controlled oscillator circuit formed by half of IC26 and Xl.

Check that the CPU has two non-overlapping 2MHz clock inputs on pins 3 (phil) and 37 (phi2) of IC42, as shown in figure 1.

Check that lE is available at pin 6 IC25. This signal should be phase shifted in relation to 1M at pin 4 IC53 as shown in figure 8.

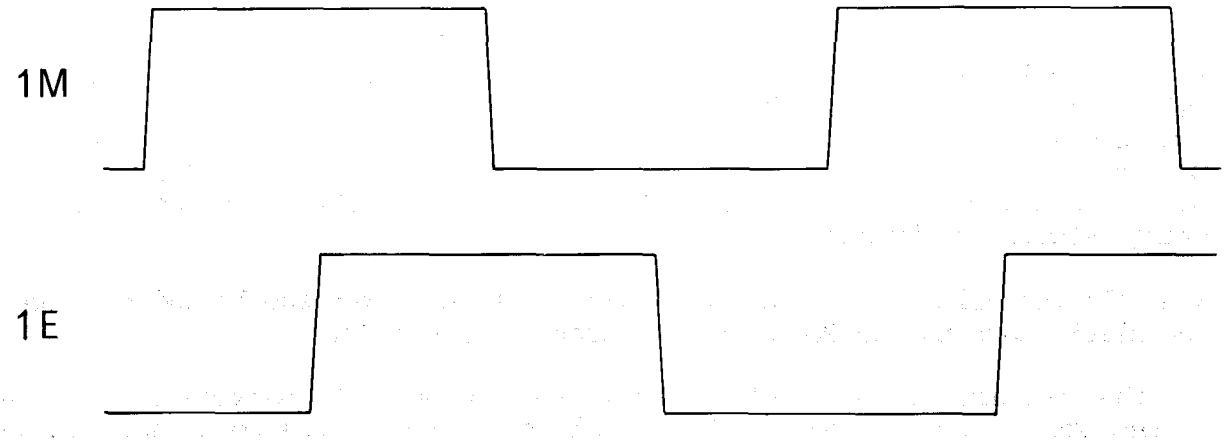


Figure 8 1M/1E

9.4 CPU

Test pin 40 IC42 (reset pin) and check that it is high. Press the BREAK key and make sure that pin 40 goes low for a reset and then high again on release.

-"Results: if pin 40 is stuck low then check for a short circuit on the main PCB, the keyboard, BREAK key, keyboard connectors or the resistors and capacitors of the 555 reset circuitry. If it is stuck high then check the 555 timer circuit (1C43), the keyboard ribbon cable and connectors, and the BREAK key itself.

Check that notIRQ (pin 4) and R/notW (pin 34) are wobbling. If not then test SYNC (pin 7). If SYNC is stuck either high or low then the processor is stalled.

Results: if CPU is stalled then check that ROMs are plugged in their sockets correctly. Check for address and data bus short or open circuit.

9.5 ROM

If ROM circuitry is not functioning then the CPU will not operate. Check that all ROMs are inserted with all the pins correctly in their sockets.

Use a PET tester if available (see information manual supplied to dealers). If this runs then the CPU is functioning correctly.

If the CPU cannot access the OS, 'heck that the OS ROM is enabled and that all address lines are present. Check following BREAK that notOE pulses low at 2MHz (inverse of phi2), and not CS goes low and stays low for a time. Replace the OS/BASIC ROM with a known good one. Make sure that S19 is made East.

If machine works, but sideways ROM selection is faulty, then run the following program to test the ROM select latch.

```
  10 romsel% = &FE30
  20 INPUT romnumber%
  30 DIM P% 100
  40 [
  50 .start%
  60 LDA# romnumber%
  70 STA romsel%
  80 RTS
  90 ]
 100 CALL start%
```

Run the program and type in a number between 0 and 15 (&0 and &F). Check using a logic probe or oscilloscope that the binary representation of this number appears on pins 11 (most significant), 12, 13, and 14 (least significant) of IC45.

Results: if the ROM numbers are not getting through to the ROM latch then alter line 80 of the program to

```
80 JMP start%
```

and re-run the program.

Check with an oscilloscope that notPGLD from pin 13 IC36 is wobbling. If not then check for shorted track. If notPGLD is working then replace IC45.

If ROM latch contains correct ROM number but sideways ROMs still do not work then check decoder IC46.

9.6 DRAMs

Use a PORT tester to carry out a RAM check.

Check that RAS and CAS (pins 4 and 15 respectively of the eight DRAM ICs) are wobbling.

Results: if RAS is stalled low then the DRAM ICs may be destroyed. Check the circuitry for generating RAS and CAS (the video processor IC53 8M, 4M, and 2M, half of IC31, and various gates). Check that RAS and CAS timing is as shown in figure 6.

Check that RAM data lines are wobbling.

Check that the data bus buffer is being enabled, pin 19 IC49.

9.7 Video

Look at the displays from the three monitors (UHF, video, and RGB) and see which of the following, (a), (b), (c), or (d) best describes them.

a) None of the monitors operate.

Results: there are incorrect signals coming from the video processor. Replace the video processor IC53.

Run the following program and check that video processor is being selected (pin 3 IC53 is wobbling).

```
10 vidproc% = &FE20
20 DIM P% 100
30 [
40 .start%
50 STA vidproc%
60 JMP start%
70 ]
80 CALL start%
```

b) The RGB works but the UHF doesn't. Test the UHF modulator input voltage using an oscilloscope. Set the oscilloscope to 50mV per division, 10 microseconds per division, auto trigger, and attach the probe to the wire running through the white plastic boss in the centre of the left side of the modulator.

Press the BREAK key and check that the PAL voltage waveform looks something like figure 9.

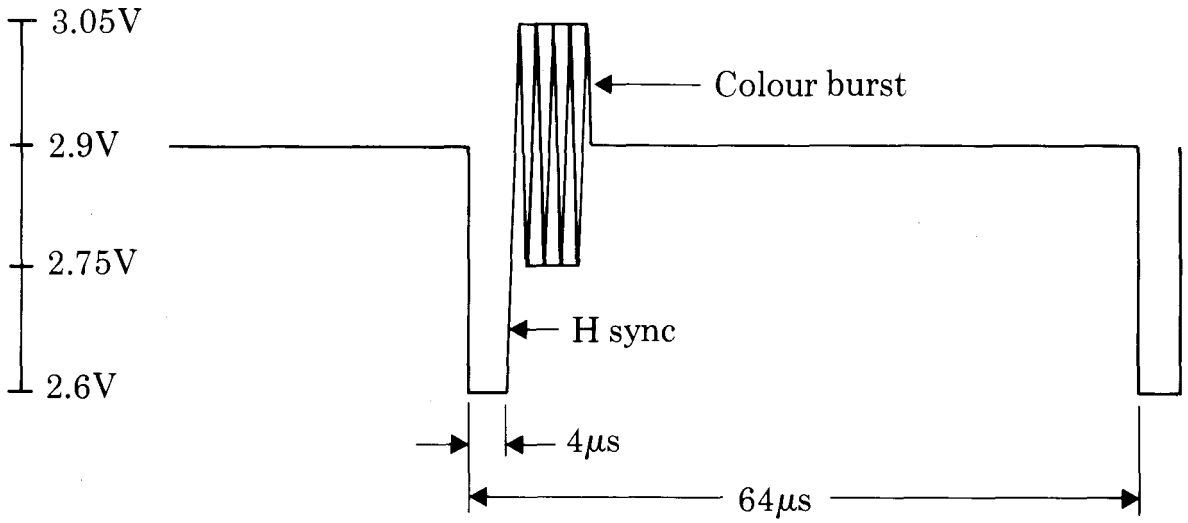


Figure 9 Black PAL voltage waveform

Type in the following:

```
COLOUR 129 : CLS
```

and press RETURN.

The waveform should now look something like figure 10.

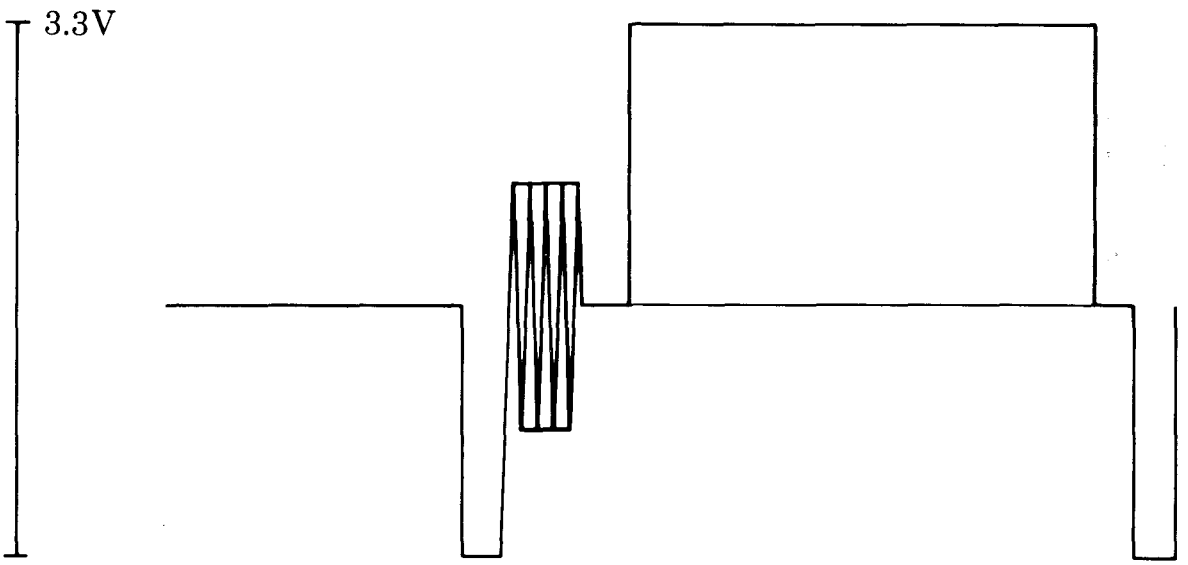


Figure 10 White PAL voltage waveform

Results: if the two waveforms are correct and the UHF monitor does not give a display then the UHF modulator is faulty and should be replaced.

If the colour burst part of the waveforms is missing then the fault lies in the chrominance circuitry, see (c).

If any other part of the waveforms is incorrect, make link S26 temporarily and test the composite video output with an oscilloscope. The waveforms should be similar to those indicated in figures 9 and 10, but of reduced amplitude (1V peak to peak).

If the composite output waveforms are good with link S26 made (including colour burst), but the UHF output does not work, then the fault lies in the UHF luminance circuitry (Q6, D12, D13, D14, C36 and associated resistors). Check that diodes D12, D13, and D14 are inserted the correct way round (the PCB is marked +).

If the video output waveforms are bad then the video luminance circuitry (Q8 and associated resistors) may be faulty, and possibly chrominance circuitry also, see (c).

A composite colour monitor can be used to test the video output with link S26 made. If the composite colour monitor works in black and white only then the chrominance circuitry is faulty, see (c).

c) RGB works; UHF works in black and white only.

Results: the chrominance circuitry is faulty. Test pin 3 of IC87 with a frequency counter. The measured frequency must be 17.7345MHz +/- 400Hz, and can be adjusted using VC1. If there is no signal on pin 3 IC87 then check the oscillator circuit formed by X2, Q10 and associated components.

IC79 is a 74S74. A 74LS74 in this position can cause the circuit to fail. Check that there are signals from pins 9 and 6 of IC79 (4. 4336MHz) and also a signal from pin 9 IC69 (7.7kHz approximately).

Check that Ll has not gone open circuit and that C49 has not failed, and check Q9.

Failing all this check the logic circuit formed by ICs 83, 86, 87, and 90, and resistors R85 to R92.

d) The RGB picture is distorted.

Results: either the DIN plug is incorrectly fitted to the monitor socket, or CSYNC must be inverted by altering S27.

9.8 Cassette interface and RS423

These two interfaces are examined together because they share two major components, the UART or ACIA IC82 and the serial processor or SERPROC IC85.

If both the cassette interface and RS423 fail (shown up by the PORT tester) then it is likely that the fault is with one of the above ICs or its address decoding.

a) Cassette interface

Use a PORT tester to verify that the cassette interface is faulty.

All tests on the cassette interface must be carried out using a known working cassette recorder and tape. The commonest fault is the user's cassette recorder and the azimuth adjustment should be checked. The tape recorder's volume control should be set for an output of 300mV peak to peak.

Test pin 25 IC85 (the serial processor) and check that 16MHz/13 (812ns period) is arriving at that pin. This signal must be stable and accurate. If not, the divide by 13 circuitry formed by IC18 is faulty.

If the cassette fails to LOAD, look at the following pins while attempting to LOAD:

IC89 pin 8 should show high and low tones of equal amplitude, symetrical about OV. If there is a marked displacement then replace IC89.

IC89 pin 14 should be similar to pin 8, with maximum 50mV displacement

IC89 pin 1 should show a 1.4V peak to peak square wave with an even mark/space ratio. Reduce the volume of the cassette recorder until this is so. Maximum 50mV displacement.

Check that pins 2 and 3 of IC82 are wobbling.

Check that both IC82 and IC85 can be selected by running the following program.

```
 10 acia% = &FE08
 20 serproc% = &FE10
 30 DIM P% 100
 40 [
 50 .start%
 60 LDA acia%
 70 LDA serproc%
 80 JMP start%
 90 ]
100 CALL start%
```

Monitor the two chip selects, pin 9 IC82 and pin 9 IC85. These should be wobbling. If one is faulty then check the address decoding IC21 and IC39, and the connections from pin 5 and pin 6 IC39.

If the cassette fails to SAVE, then SAVE a section of ROM and check that there is a synthesised sine-wave signal from IC85 pin 27 of around 1.8V peak to peak. If not then replace IC85. If there is then replace the LM324 IC89.

b) RS423

Use a PORT tester to verify that the RS423 is faulty.

One way of checking the operation of the RS423 is to connect the suspect microcomputer to a known working microcomputer via their RS423 ports. The connections must be made as follows

```
Din to Dout     pin A to pin B
Dout to Din     pin B to pin A
0V to 0V        pin C to pin C
CTS to RTS      pin D to pin E
RTS to CTS      pin E to pin D
```

Once the two machines are connected, switch on the power for both, and configure the known working microcomputer to accept RS423 as input by typing

```
*FX2,2
```

This command will cause the microcomputer to accept input from both the keyboard and RS423, so keyboard commands will still work.

Now type the following BASIC program into the suspect microcomputer

```
10 *FX3,5
20 REPEAT
30 PRINT "U";
40 UNTIL 0
```

This program configures the suspect microcomputer to give output to the RS423 and to the screen. It then prints the character "U", whose ASCII code is &55. &55 is a good number for testing the RS423 because it consists of alternating bits 01010101.

RUN the program.

If the known working microcomputer starts printing etc across the screen then the RS423 is working as a transmitter. If it works then go on to test it as a receiver.

If no output appears then test the suspect RS423 circuit as follows.

Check the Dout line either side of the driver, pins 2 and 15 of IC95. Pin 2 should be oscillating at normal TTL logic levels V/+5V. Pin 15 should be oscillating in phase with pin 2 but at RS423 logic levels -5V/+5V. If pin 2 is active but pin 15 is not then replace the driver IC95.

Check that the SERPROC IC85 is sending the transmit clock TXCK and receiving transmit data TXD from the 6850 IC82. These signals are on pins 26 and 22 respectively of IC85. If these signals are inactive then it is likely that the SERPROC is faulty or cannot be addressed. Use the test program given in the cassette section above to check that the address decoding for the SERPROC and 6850 is working.

Now press CTRL BREAK on each microcomputer and swap the configurations, so that the good computer is the transmitter and the suspect computer is the receiver.

If "U" characters are output on to the monitor by the suspect computer then its RS423 is working as a receiver.

If no output appears then test the suspect RS423 circuit as follows.

Check the Din line either side of the receiver, pins 4 and 7 of IC94. Pin 4 should be oscillating at RS423 logic levels -5V/+5V. Pin 7 should be oscillating in phase with pin 4 but at normal TTL logic levels OV/+5V. If pin 4 is active but pin 7 is not then replace the receiver IC94.

Check that the SERPROC IC85 is sending the receive clock RXCK and receive data RXD to the 6850 IC82. These signals are on pins 26 and 22 respectively of IC85. If these signals are inactive then it is likely that the SERPROC is faulty or cannot be addressed. Use the test program given in the cassette section above to check that the address decoding for the SERPROC and 6850 is working.

The alternative way of testing RS423 without using another microcomputer is to connect RTS to CTS and Dout to Din. Then if the BASIC program above is used to transmit data its path can be followed from the data bus through the 6850, SERPROC, drivers, out through the connector and back again through the receivers, SERPROC and through RXD back to the 6850. This loop allows all the components of the RS423 circuit to be checked as above.

9.9 Keyboard

Keyboard problems either show up as a single key which won't work reliably, or a whole group of keys which refuses to operate.

The single key fault is caused by that particular switch having worn out, or the track becoming broken by excess force. Replace the key or solder the track.

For multiple key problems, the first thing to check is that the connectors are inserted correctly. It is easy to displace either connector of the keyboard ribbon cable one pin to the left or right. If the connections are good then check that one of the wires in the cable itself hasn't been broken where it is held by the connector. Replace the ribbon cable with a good one. Try replacing the whole keyboard assembly with a good one. If it still doesn't work then there is probably a fault in the computer itself. Use a PORT tester.

9.10 Disc interface

8271: check all links are in correct position for 8271 operation:

S1 North (PCB LINK)
S2 North (PCB LINK)
S3 South (PCB LINK)
S4 South (PCB LINK)
S6 South (PCB LINK)
S7 West
S8 open circuit

Check that all ICs and passives are fitted and inserted correctly, see 8271 disc upgrade, section 6.2.

Use a PORT tester to check that the disc interface is the problem.

Check that a disc filing system ROM has been fitted eg DNFS. If the filing system is stored in an EPROM (as opposed to a mask ROM) then make sure that pin 27 is connected to 5V.

Connect a known working dual 80 track disc drive.

Turn the microcomputer on. Check that the start-up message indicates a filing system ROM is present.

Acorn OS 64K

Acorn DFS

BASIC

>

Results: If the message does not report the "Acorn DFS" then check the IC socket by fitting a known good language ROM. Check the DFS (or DNFS) Ram in another machine. If both are OK then check the 8271 (IC15) and the chip select logic, check for correct data, address, RD and WR signals at IC15. Check for 2MHz on pin 3 and for a reset pulse on pin 4 (when break key used) of IC15.

Press SHIFT and BREAK, then release BREAK while holding SHIFT down. Drive 0 should start (the LED on the front of the drive comes on).

Results: if the drive fails to come on then test that pin 38 IC15 is high (pin 10 IC8 low).

Results: if pin 10 IC8 goes low then check the connection from IC8 to PL8. If pin 10 IC8 is high then first check that a DNFS ROM is fitted and is plugged in correctly. Try fitting a good 8271. Then run the following program and check that the 8271 is being selected using an oscillosope on IC15 pin 24.

```
13 fdc% = &FE80
20 DIM P% 100
30 [
40 .start%
50 LDA fdc%
60 JMP start%
70 ]
80 CALL start%
```

If drive does come on with SHIFT BREAK then insert a known good 80 track disc into drive 0. Use a disc which has a number of files on it, and make sure that a write protect tab is fitted. Shut the drive door.

Try *CAT to get a catalogue of the disc. If no catalogue appears then check that S7 is fitted West. Check that notCS pulses low (pin 24 IC15). If not then check decoder IC28.

Check that after a BREAK a pulse occurs on pin 7 IC15. If not then check decoder IC28.

Check that RDY pins 5 and 32 of IC15 are low. If RDY is high then check S2, and for 2MHz at pin 3 IC15. If 2MHz is missing then link S6 is probably open circuit, if 4MHz then S6 set incorrectly. Check that index pulses are reaching IC3 pins 3 and 11. If not then either S4 is wrong or the disc drive is faulty. If index pulses are reaching IC3 but RDY is not going low then the disc may not be reaching speed. Measure the index pulse frequency. It should be 5Hz +/-3%.

Use an oscilloscope to monitor data on the signal end of R7. The data should be negative-going lus pulses with intervals of 4 or 8us between them. If not then check connections to PL8.

1770: check all links are in correct position for 1770 operation:

S3 South (PCB LINK)
S4 South (PCB LINK)
S5 broken
S7 East
S8 made

Check that all ICs and passives are fitted and inserted correctly, see 1770 disc upgrade, section 6.1.

Use a PORT tester to check that the disc interface is the problem.

Check that a disc filing system }Y4 has been fitted, eg 1770 DFS or ADFS. If the filing system is stored in an EPROM, check that pin 27 of the EPROM is connected to 5V. For tests that follow we shall assume the use of the 1770 DFS, so fit this ROM if it is not already in place.

Connect a known working dual 80 track disc drive.

Turn the microcomputer on. Check that the start-up message indicates a filing system ROM is present.

Acorn OS 64K

1770 DFS

BASIC

>

Results: if the message fails to say 1770 DFS then check the ROM socket and the ROM. If the ROM works OK then check that the data, address and control signals are reaching the 1770, IC16. Check for pulses on pin 1 of IC15 after a break. If there are none, check the address decoding logic.

Press SHIFT and BREAK, then release BREAK while holding SHIFT down. Drive 0 should start (the LED on the front of the drive comes on).

Results: if drive doesn't come on then check using an oscilloscope or logic probe that MO (pin 20 IC16) is high, notMOTOR (pin 10 IC8) is law. Check that S0 (pin 7 IC17) is high, notS0 (pin 8 IC7) is low. If the above signals are correct then check the connection from IC7 and IC8 to connector PL8. If the above signals are wrong then try a good 1770 and check IC17. Check that IC17 is reset after a BREAK (all outputs law). Check IC17 function by poking values between 0 and 64 into location &FE80. Check that the correct bit pattern appears on the outputs.

If drive does come on with SHIFT BREAK then insert a known good 80 track disc into drive 0. Use a disc which has a number of files on it, and make sure that a write protect tab is fitted. Shut the drive door.

Try *CAT to get a catalogue of the disc. If no catalogue appears then check that S7 is fitted East. If an incorrect catalogue is obtained then check that S8 is fitted. This fault is unlikely if the disc system has worked before, but likely after an upgrade.

Check that after a BREAK a chip select (notCS) pulse occurs on pin 1 IC16. If not then check decoder IC28.

Use an oscilloscope to monitor read data (notRD) on pin 19 IC16, or the signal end of R7. The data should be negative-going pulses of period 4us or 8us. If not then check connections to PL8. Replace 1770.

9.11 Printer port

Use a PORT tester to check that the printer port is faulty.

Test the VIA (IC10) by writing values to it and testing the outputs. First configure all the data lines as outputs by writing &FF to the data direction register A (DDRA)

?&FE63=&FF

Then write &00 to the output register

?&FE61=&00

All the data lines to the printer connector PL9 should now be low, pins 3 5 7 9 11 13 15 and 17. If they are not all zero then check them at the VIA itself, pins 2 3 4 5 6 7 8 and 9 of IC10. If these are all low then the buffer 105 is faulty. Otherwise check for open circuit tracks on data lines on both the printer side and the CPU side of the VIA.

Now write &FF to the output register

?&FE61=&FF

All the data lines to the printer connector PL9 should now be high, pins 3 5 7 9 11 13 15 and 17. If they are not all 1 then check them at the VIA itself, pins 2 3 4 5 6 7 8 and 9 of IC10. If these are all high then the buffer IC5 is faulty. Otherwise check for short circuit tracks on data lines -on both the printer side and the CPU side of the VIA.

A better test is to use the binary configuration 10101010 on the outputs, and then change it to 01010101. These correspond to the values &AA and &55. This way short circuits are more likely to give the wrong value in the tests.

Connect a known good printer to the microcomputer. Check that the printer strobe output from the VIA pin 39 IC10 gives a 4us negative going pulse when the computer is instructed to print. If it does then check this pulse at pin 14 1C13. If the printer interface is working correctly then there should be regular strobe pulses until the printer buffer is full. If there is only a single pulse then check the printer ACK input pin 40 IC10. These two lines together (strobe and ACK) perform the data control handshake and, on being instructed to print, the two signals ought to alternate until the printer buffer is full. If the computer is sending a strobe pulse but no ACK is coming back from the printer then the connections to the edge connector PL9 are faulty. If the strobe pulse is not being sent then the fault is either a broken track or the VIA chip itself.

9.12 User port

Use a PORT tester to check that the user port is faulty.

Test the VIA (IC10) by writing values to it and testing the outputs. First configure all the data lines as outputs by writing &FF to the data direction register B (DDRB)

```
?&FE62=&FF
```

Then write &00 to the output register

```
?&FE60=&00
```

All the data lines to the user connector PL10 should now be low, pins 6, 8, 10, 12, 14, 16, 18 and 20. If they are not all zero then check for open circuit tracks on data lines on both the printer side and the CPU side of the VIA.

Now write &FF to the output
register ?&FE60=&FF
All the data lines to the user connector PL10 should now be high. If they are not all 1 then check for short circuit tracks on data lines on both the printer side and the CPU side of the VIA.

A better test is to use the binary configuration 10101010 on the outputs, and then change it to 01010101. These correspond to the values &AA and &55. This way short circuits are more likely to give the wrong value in the tests.

9.13 1MHz extension bus

Use a PORT tester. If the 1MHz extension bus is faulty then the PORT tester may show up all kinds of errors, because it is driven through the 1MHz bus.

Use the following program to exercise the FRED and JIM address decoding.

```
10 fred% = &FC00
20 jim% = &FD00
30 DIM P% 100
40 [
50 .start%
60 LDA# &00
70 .loop%
80 STA fred%
90 STA jim%
100 JMP loop%
110 ]
120 CALL start%
```

RUN the program and test pins 4 and 5 IC28 for the FRED and JIM signals, which should be pulsing low for lus or 1.5us (depending on the CPU's synchronisation to 1M). If not then replace IC28. If the signals are good then test them at pins 16 and 14 IC6.

Check that the ROM output enable pin 6 IC40 is high (ROM disabled) when. either FRED or JIM is low.

Check that SYNC 1M pin 8 IC41 is high when either FRED or JIM is low.

Check that the data bus buffer enable pin 19 IC12 is low (enabled) when either FRED or JIM is low.

All the above three signals come indirectly from pin 11 IC34.

Check that the data bus D0-D7 goes low both sides of the buffer at some point after the buffer is enabled (pin 19 IC12 goes low).

9.14 TUBE interface

Use a PORT tester to check that the TUBE interface is faulty. Run the following test program

```
  10 tube% = &FEE0
  20 DIM P% 100
  30 [
  40 .start%
  50 LDA# &00#
  60 .loop%
  70 STA tube%
  80 JMP loop%
  90 ]
 100 CALL start%
```

Test the enable pin 19 IC14 with an oscilloscope and check that the signal is wobbling. If not then check the address decoding performed by IC21 and IC22.

Check that all data lines both sides of the buffer pins 11-18 and pins 9-2 of IC14 (D0-D7) go low at some point after the enable pin 19 IC14 goes low.

Change line 50 of the program to

50 LDA# &FF

and check that all the buffered data lines go high at some point after the enable pin 19 IC14 goes low.

If these tests do not give correct results then check the data bus buffer IC14 and the PCB tracks and connections to PL12.

50 LDA# &AA

and

50 LDA# &55

can also be tried. These correspond to output bit patterns 10101010 and 01010101.

A0-A4, R/notW, and 2E can be looked for on pins 12 9 7 5 3 16 and 18 of IC13. These signals should be the same as the system signals, but delayed by 10-15ns.

9.15 Analogue to digital conversion

Use a PORT tester to verify that the ADC circuit is faulty.

Check VREF by measuring the voltage between pin 8 IC84 and ground. This voltage should be approximately 1.8V. Look for shorted or broken tracks if it is not.

Connect two known working 2-way joysticks to the D-type connector SK6 used for the ADC. Type in and RUN the following program.

```
10 VDU 23,1,0;0;0;0;
20 CLS
30 REPEAT
40 PRINT TAB(0,0); ADVAL(1); SPC(4)
50 PRINT TAB(0,2); ADVAL(2); SPC(4)
60 PRINT TAB(0,4); ADVAL(3); SPC(4)
70 PRINT TAB(0,6); ADVAL(4); SPC(4)
80 UNTIL 0
```

Move the joysticks and see if you can get numbers in the range 0 to 65520 on each of the 4 channels. (In practice it may well not be possible to get near either one or both of the end values, but a good range of numbers on each channel is sufficient to show that the converter is working.)

If this experiment does not work then check that the ADC IC can be accessed by running the following program.

```
10 adc% = &FEC0
20 DIM P% 100
30 [
40 .start%
50 LDA adc%
60 JMP start%
70 ]
80 CALL start%
```

Check that pin 23 IC84 is active. If not then check the address decoding and connections from pin 9 IC21.

Press CTRL BREAK and look at the signal on pin 28 IC84. This line signals the end of a conversion and should be pulsing low approximately once every 10ms. If it is, but there is still a problem with A to D conversion, then check that the EOC signal is reaching pin 18 IC20.

9.16 ECONET

ECONET can only be serviced properly by ECONET service centres, who will have the necessary test equipment to check the system thoroughly. However, there are a few simple things which can be checked without the test equipment.

Check that all the ECONET components are installed and have been fitted correctly, see 6.3.

Check that notNMI on the CPU pin 6 IC42 is not being held low.

If the system will not give a correct ID number then use the shunts S23 to find which track is broken or shorting.

Appendix

Connector pinouts

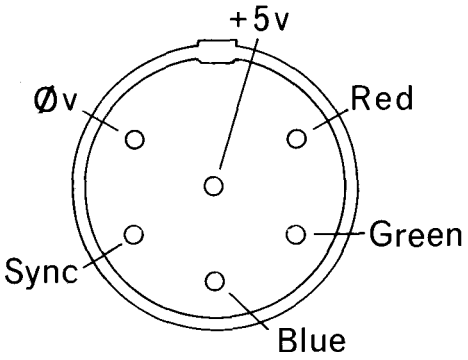
SK1 UHF out
phono

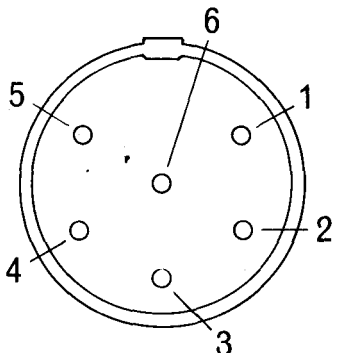
outer: ground
inner: UHF

SK2 video out
BNC

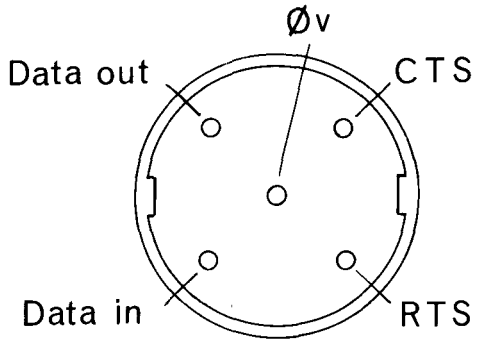
outer: ground
inner: video

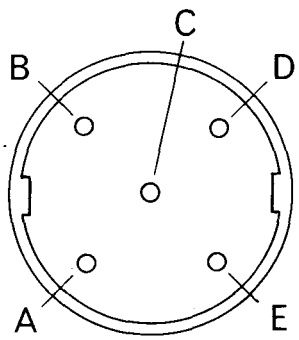
SK3 RGB
6-pin DIN



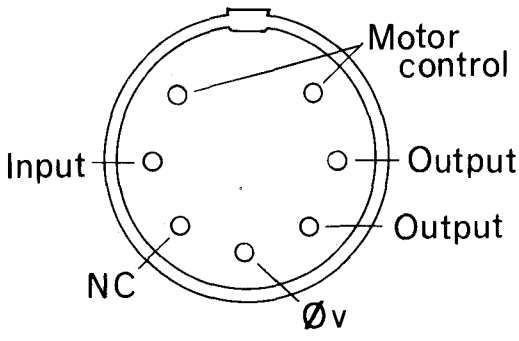


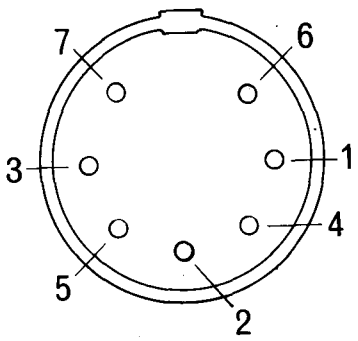
SK4 RS423
5-pin DIN



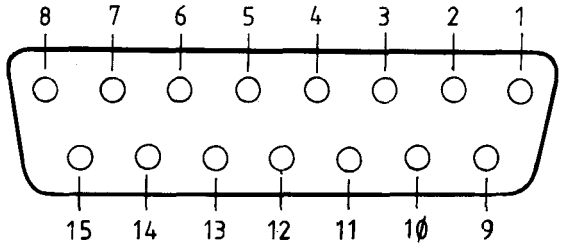


SK5 cassette
7-pin DIN



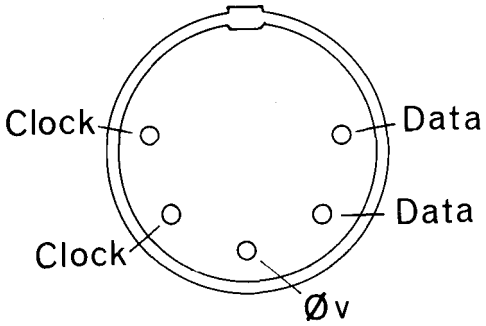


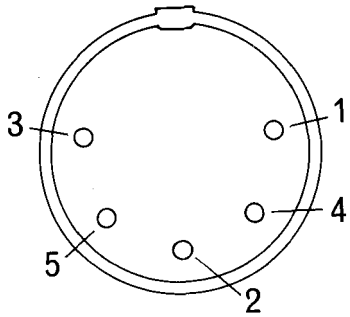
SK6 analogue in
15-way D-type



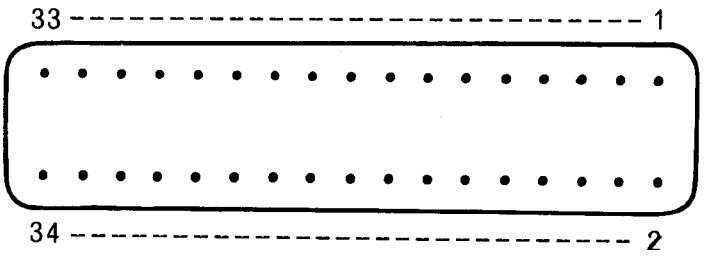
1	+5V	9	light pen strobe (notLPSTB)
2	0V	10	digital switch input (I1)
3	0V	11	voltage reference (VREF)
4	CH3	12	CH2
5	analogue ground	13	digital switch input (I0)
6	0V	14	voltage reference (VREF)
7	CH1	15	CH0
8	analogue ground		

SK7 ECONET
5-pin DIN



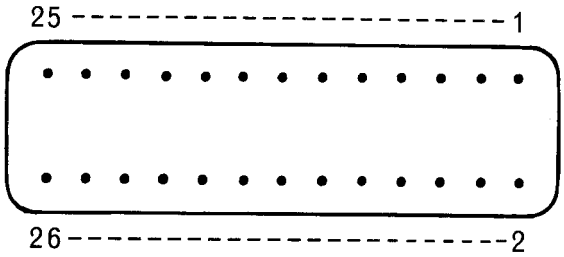


PL8 disc drive
34-way IDC



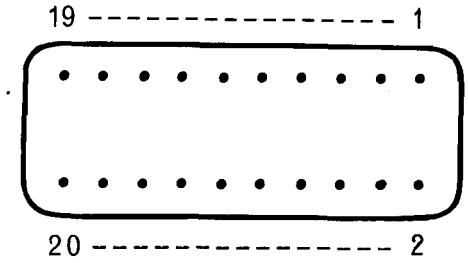
1	0V	2	(notS/SEL 8")
3	0V	4	(notINX 8")
5	0V	6	NC
7	0V	8	notINX 5 1/4"
9	0V	10	notS0
11	0V	12	notS1
13	0V	14	NC
15	0V	16	notMOTOR
17	0V	18	notDIR
19	0V	20	notSTEP
21	0V	22	notW/DATA
23	0V	24	notWR/EN
25	0V	26	notTK0
27	0V	28	notWR PCT
29	0V	30	notR/DATA
31	0V	32	notS/SEL 5 1/4"
33	0V	34	(notRDY 8")

PL9 printer
26-way IDC



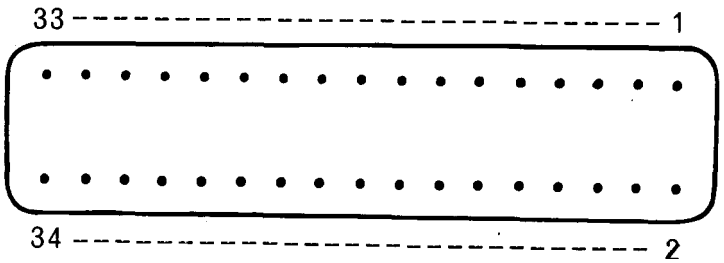
1	STB	2	0V
3	PA0	4	0V
5	PA1	6	0V
7	PA2	8	0V
9	PA3	10	0V
11	PM	12	0V
13	PA5	14	0V
15	PA6	16	0V
17	PA7	18	0V
19	ACK	20	0V
21	NC	22	0V
23	NC	24	0V
25	NC	26	NC

PL10 user port
20-way IDC



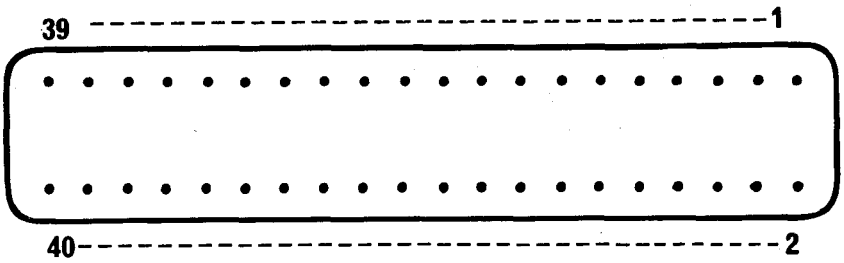
1	+5V	2	CB1
3	+5V	4	CB2
5	0V	6	PB0
7	0V	8	PB1
9	0V	10	PB2
11	0V	12	PB3
13	0V	14	PB4
15	0V	16	PB5
17	0V	18	PB6
19	0V	20	PB7

PL11 1MHz bus
34-way IDC



1	0V	2	R/notW
3	0V	4	1E
5	0V	6	notNMI
7	0V	8	notIRQ
9	0V	10	notPGFC
11	0V	12	notPGFD
13	0V	14	notRS
15	0V	16	audio in/out (see S17)
17	0V	18	D0
19	D1	20	D2
21	D3	22	D4
23	D5	24	D6
25	D7	26	0V
27	A0	28	A1
29	A2	30	A3
31	A4	32	A5
33	A6	34	A7

PL12 TUBE
40-way IDC



1	0V	2	R/notW
3	0V	4	2E
5	0V	6	notIRQ
7	0V	8	notTUBE
9	0V	10	notRS
11	0V	12	D0
13	0V	14	D1
15	0V	16	D2
17	0V	18	D3
19	0V	20	D4
21	0V	22	D5
23	0V	24	D6
25	0V	26	D7
27	0V	28	A0
29	0V	30	Al
31	+5V	32	A2
33	+5V	34	A3
35	+5V	36	A4
37	+5V	38	NC
39	+5V	40	NC

PL13 keyboard
17-pin molex

1	0V
2	BREAK
3	1E
4	keyboard enable
5	SD4
6	SD5
7	SD6
8	SD0
9	SD1
10	SD2
11	SD3
12	SD7
13	cassette LED
14	CA2 (to generate In)
15	+5V
16	shift lock LED
17	caps lock LED

Parts list

NOTE: Items identified by * are normally available as spare parts - please contact your supplier for details of availability.

ITEM	PART NO	DESCRIPTION	QTY	REMARKS
BBC Microcomputer Model B+ PCB Assembly				
1				
2				
3				
4		RESISTOR SOT 0.25W 5%	1	R76 TYP 3k3 to 6k8
5	0502,100	RESISTOR 10R 0.25W 5%	4	R58,121,122,153
6	0502,330	RESISTOR 33R 0.25W 5%	3	R53-55
7	0502,680	RESISTOR 68R 0.25W 5%	6	R94,109,112,128-130
8	0502,820	RESISTOR 82R 0.25W 5%	3	R62,65,67
9	0502,101	RESISTOR 100R 0.25W 5%	6	R31,45-47,57,61
10	0502,151	RESISTOR 150R 0.25W 5%	5	R1,5-8
11	0502,180	RESISTOR 18R 1W 10%	1	R37 FERRANTI IC53 ONLY
12	0502,271	RESISTOR 270R 0.25W 5%	3	R20,21,40
13	0502,331	RESISTOR 330R 0.25W 5%	2	R30,35
14	0502,471	RESISTOR 470R 0.25W 5%	4	R49,75,88,102
15	0502,681	RESISTOR 680R 0.25W 5%	3	R85,91,92
16	0502,821	RESISTOR 820R 0.25W 5%	1	R86
17				
18				
19				
20				
21	0502,102	RESISTOR 1K 0.25W5%	16	R3#,11,16,36,38, R63,68,73,84,104, R105,107,131-133,148
22	0502,122	RESISTOR 1K2 0.25W 5%	1	R89
23	0502,152	RESISTOR 1K5 0.25W 5%	4	R82,146,147,154
24	0502,182	RESISTOR 1K8 0.25W 5%	3	R50-52
25	0502,222	RESISTOR 2K2 0.25W 5%	8	R74,80,87,101,114, R120, 124,149
26	0502,272	RESISTOR 2K7 0.25W 5%	2	R69,138
27	0502,332	RESISTOR 3K3 0.25W 5%	10	R9#,10#,14,18,19, R56,71,90,118,152
28	0502,392	RESISTOR 3K9 0.25W 5%	4	R93,108,139,150
29	0502,472	RESISTOR 4K7 0.25W 5%	7	R4,23,43,48, R59,60,100
30	0502,562	RESISTOR 5K6 0.25W 5%	1	R103
31	0502,822	RESISTOR 8K2 0.25W 5%	2	R123,127
32				
33	0502,103	RESISTOR 10K 0.25W 5%	13	R2#,22,26,27,29, R34,42,44,81, R111,126,144,151
34	0502,123	RESISTOR 12K 0.25W 5%	1	R116
35	0502,153	RESISTOR 15K 0.25W 5%	1	R115
36	0502,223	RESISTOR 22K 0.25W 5%	1	R72

Components marked # are fitted only with 8271 disc interface.

37	0502,393	RESISTOR 39K 0.25W 5%	2	R64,117
38	0502,563	RESISTOR 56K 0.25W 5%	1	R15
39	0502,623	RESISTOR 62K 0.25W 5%	1	R33
40	0502,823	RESISTOR 82K 0.25W 5%	1	R66
41	0502,104	RESISTOR 100K 0.25W 5%	3	R28,41,70
42	0502,154	RESISTOR 150K 0.25W 5%	2	R137,145
43	0502,224	RESISTOR 220K 0.25W 5%	3	R39,77,136
44	0502,274	RESISTOR 270K 0.25W 5%	1	R83
45	0502,824	RESISTOR 820K 0.25W 5%	1	R135
46	0505,103	RESISTOR 10K 0.25W 2%	4	R140-143
47	0505,563	RESISTOR 56K 0.25W 2%	4	R95,96,98,99
48	0505,104	RESISTOR 100K 0.25W 2%	4	R106,110,125,134
49				
50	0502,105	RESISTOR LA0 0.25W 5%	3	R17,24,25
51	0502,155	RESISTOR 1M5 0.25W 5%	3	R78,79,97
52				
53	0520,180	RESISTOR 18R 1W0 10%	1	R37
54	0581,103	POTENTIOMETER 10K 20%	1	VR2
55	0581,104	POTENTIOMETER 100K 20%	1	VR1
56				
57				
58	0590,223	RESISTOR PACK SIL 22Kx8	1	RP2
59	0590,682	RESISTOR PACK SIL 6K8x9	1	RP1
60				
61				
62				
63				
64				
65				
66	0631,010	CAPACITOR 10pF CERAMIC	1	C39
67	0631,033	CAPACITOR 33pF CERAMIC	2	C12,16
68	0631,039	CAPACITOR 39pF CERAMIC	1	C40
69	0631,047	CAPACITOR 47pF CERAMIC	3	C44,45,49
70	0631,068	CAPACITOR 68pF CERAMIC	3	C4,17,18
71	0631,100	CAPACITOR 100pF CERAMIC	3	C20,53,55
72				
73	0631,150	CAPACITOR 150pF CERAMIC	1	C36
74	0631,270	CAPACITOR 270pF CERAMIC	1	C22
75	0630,039	CAPACITOR 390pF CERAMIC	1	C47
76	0630,047	CAPACITOR 470pF CERAMIC	1	C48
77	0630,082	CAPACITOR 820pF CERAMIC	2	C58,59
78				
79				
80	0630,100	CAPACITOR 1n0F CERAMIC	1	C1#
81	0630,150	CAPACITOR 1n5F CERAMIC	1	C11
82	0630,220	CAPACITOR 2n2F CERAMIC	4	C26,31,34,35
83	0630,330	CAPACITOR 3n3F CERAMIC	1	C8
84	0630,470	CAPACITOR 4n7F CERAMIC	5	C19,21,32,42,43
85	0629,010	CAPACITOR 10nF CERAMIC	3	C3,13,28
86	0650,333	CAPACITOR 33pF POLY	1	C29

Components marked # are fitted only with 8271 disc interface.

87	0680,002		CAPACITOR 33/47nF DECUP 64/67		A
88	0640,473		CAPACITOR 47nF CERAMIC	1	C24
89	0640,104		CAPACITOR 100nF CERAMIC	5	C5-7,9,23
90	0651,224		CAPACITOR 220nF CERAMIC	2	C38,41
91					
92	0613,100		CAPACITOR luF TANT	1	C33
93	0635,047		CAPACITOR 4u7F 16V ELEC RADIAL	1	C30
94	0635,100		CAPACITOR 10uF 16V ELEC RADIAL	3	C27,51,52
95	0621,047		CAPACITOR 4u7F 10V ELEC AXIAL	1	C15
96	0610,010		CAPACITOR 10uF 10V TANT	1	C57
97	0621,470		CAPACITOR 47uF 10V ELEC_6 AXIAL		C25,46,50,54,56,60
98	0610,047		CAPACITOR 47uF 10V TANT	1	C37
99	0620,100		CAPACITOR 10uF 6V3 ELEC AXIAL	1	C14
100					
101	0699,003	*	CAPACITOR TRIM 5-65pF	1	VC1
102					
103					
104	0860,005	*	CHOKE 33uH	1	L1
105					
106					
107	0820,160	*	CRYSTAL 16MHZ	1	X1
108	0820,177	*	CRYSTAL 17.734475MHZ	1	X2
109					
110					
111	0810,001	*	RELAY 5V	1	RL1
112					
113					
114	0780,239	*	TRANSISTOR BC239	7	Q1-5,7,9
115	0780,309	*	TRANSISTOR BC309	2	Q6,8
116					
117	0783,906	*	TRANSISTOR 2N3906	1	Q10
118					
119					
120	0794,148	*	DIODE 1N4148	14	D1#,D2-4,8-18
121	0794,001		DIODE IN4001	3	D5-7
122					
123					
124	0740,016	*	IC 7416	1	IC8
	0740.006	*	IC 7406	1	IC8 OPTION
125	0740,038	*	IC 7438	1	IC7
126	0741,000	*	IC 74S00	1	IC52
127	0742,000	*	IC 74LS00	5	1C9#,19,27,87,90
128	0741,002	*	IC 74S02	1	IC33

Components marked # are fitted only with 8271 disc interface:

129	0742,002	*	IC 74LS02	1	IC58
130	0741,004	*	IC 74S04	1	IC26
131	0742,004	*	IC 74LS04	1	IC24
132	0742,008	*	IC 74LS08	1	IC34
133	0742,010	*	IC 74LS10	1	IC48
134	0742,020	*	IC 74LS20	1	IC40
135	0742,030	*	IC 74LS30	2	IC22,41
136	0742,032	*	IC 74LS32	1	IC23
137	0741,074	*	IC 74S74	2	IC31,79
138	0742,074	*	IC 74LS74	1	IC69
139	0742,086	*	IC 74LS86	3	IC63,83,86
140	0742,109	*	IC 74LS109	1	IC25
141	0742,123	*	IC 741S123	2	IC1#,88
142	0742,132	*	IC 74LS132	1	IC70
143	0742,138	*	IC 74LS138	2	IC21,46
144	0742,139	*	IC 74LS139	2	IC28,39
145	0742,163	*	IC 74LS163	2	IC18,45
146	0742,174	*	IC 74LS174	1	IC17 1770 ONLY
147	0742,244	*	IC 7415244	4	IC5,6,13,80
148	0742,245	*	IC 7415245	3	IC12,14,49
149	0742,253	*	IC 74LS253	4	1C72-75
150	0742,257	*	IC 74LS257	2	IC50,51
151	0742,259	*	IC 74LS259	1	IC30
152	0742,273	*	IC 74LS273	1	IC54
153	0742,283	*	IC 7415283	1	IC76
154	0742,374	*	IC 7415374	2	IC11,32
155	0742,393	*	IC 74LS393	1	IC2#
156	0739,120	*	IC DS88LS120N	1	IC94
157	0770,319	*	IC LM319	2	IC92,93
158	0770,324	*	IC LM324	2	IC47,89
159	0770,386	*	IC LM386	1	IC77
160	0733,691	*	IC DS3691N	1	IC95
161	0704,865	*	IC 4164-12	8	IC55,56,60,61,64-67
162	0706,511	*	IC TM4164EK8-12	1	IC96 OPTIONAL
163	0706,522	*	IC 6512A	1	IC42
164	0706,845	*	IC 6522	2	IC10,20
165	0706,850	*	IC 6845	1	IC78
166	0707,002	*	IC 6850	1	IC82
167	0735,159	*	IC uPD7002	1	IC84
168	0706,490	*	IC SN75159N	1	IC91
169	0708,271	*	IC SN76489N	1	IC38
170	0706,854	*	IC 8271	1	IC15#
171	0753,521		IC 68B54	1	IC81
172	0754,013	*	IC HEF 4521B	1	IC4#
173	0705,050	*	IC HEF 4013B	1	IC3#
174	0201,241	*	IC SAA 5050	1	IC59
175	0201,666	*	IC OS/BASIC ROM	1	IC71
			IC DNFS 3.0 ROM	1	IC35#

Conponents marked # are fitted only with 8271 disc interface. IC35 is also fitted for ECONET.

176	2201,113	*	IC 1770 DFS ROM	1	IC57 1770 ONLY
177	0201,274	*	IC ADFS ROM	1	IC44
178					
179					
180	0201,647	*	IC V10 V2 PROC	1	IC53
181	0201,648	*	IC SERPROC	1	IC85
	0201,602		IC 2C199	1	OPTION FOR IC85
182	0770,555		IC LM555	1	IC43
183	0201,880	*	IC PAL 16R4	1	IC36
184	0701,770	*	IC 1770	1	IC16
185					
186					
187					
188					
189					
190					
191	0800,114	*	IC SOCKET DIL 14P		OPTION
192	0800,116	*	IC SOCKET DIL 16P		OPTION
193					
194					
195	0800,128	*	IC SOCKET DIL 28P	9	IC29,35.37,44,53, IC57,62,68,71
196					
197	0800,006	*	CONNECTOR IDC 34 WAY	2	PL8,11
198	0800,007	*	CONNECTOR IDC 40 WAY	1	PL12
199	0800,008	*	CONNECTOR IDC 26 WAY	1	PL9
200	0800,050	*	PLUG 2 WAY	3	PL15,S26
201	0800,051	*	PLUG 3 WAY	4	S13,14,20,27
202	0800,052	*	PLUG 5 WAY	3	SK3/A,S9,11,12,15,18
203	0800,054	*	PLUG 8 WAY	2	S23
204	0800,055	*	PLUG 10 WAY	1	PL14
205	0800,059	*	PLUG 17 WAY	1	PL13
206					
207	0800,009	*	CONNECTOR IDC 20 WAY	1	PL10
208					
209	0800,070	*	SHUNTS	16	S9,11-15,18,20, S23(7off),27
210	0870,420		TINNED COPPER WIRE	A/R	S7,8,16,R12,32
211					
212	0800,200	*	FASTON TABS	7	+5V(3) 0V(3) -5V(1)
213					
214					
215	0800,004	*	SOCKET DIN 5 WAY	1	SK7
216					
217	0800,002	*	SOCKET DIN 6 WAY	1	SK3
218	0800,001	*	SOCKET DIN 5 WAY DOMINO	1	SK4
219	0800,003	*	SOCKET DIN 7 WAY	1	SK5
220	0800,304	*	SOCKET D TYPE 15 WAY	1	SK6
221					

222	0825,000	*	MODULATOR UM 1233 E36	1	SK1
223					
224					
225					
226	0705,220	*	IC TMS 5220 (SPEECH)	1	IC29
227	0201,608	*	IC SPEECH PHROM V1 6100	1	IC37
228					

NOTE: SOT denotes Select On Test and therefore the value of the component will vary from machine to machine.

BBC Microcomputer Model B+ General Assembly

1	0103,001	*	KEYBOARD ISS 2 (INC. SPEAKER)	1
2	0201,233	*	CASE UPPER ISS 5	1
3	0201,232	*	CASE LOWER ISS 4	1
4	0201,098	*	REAR ACCESS LABEL ISS 6	1
5	0201,111	*	BOTTOM ACCESS LABL ISS4	1
6	0201,096	*	KEYBOARD LABEL ISS. 4	1
7	0800,600	*	BNC CONNECTOR 75R	1
8	0890,000	*	'STICK ON' FOOT	4
9	0882,988		4BA INT WASHER	2
10	0882,986		NYLON WASHER 1/D 5	5
11	0882,948		No 8 SPIRE NUT	2
12	0882,914		4BA NUT FULL	2
13	0882,712		No 4x7/16" PAN HD SUPER 2	
14	0882,649		No 8x19 FL HI) POSI	4
15	0882,644		No 8x9.5 FL HD POSI	5
16	0882,343		4BA x 5/8 PAN HD POSI	2
17	0882,122		M3 x 8 PAN HD POSI	3
18	0831,105	*	P.S.U	1

Glossary

ACK	ACKnowledge line on the printer port
ACIA	Asynchronous Communications Interface Adaptor - serial to parallel and parallel to serial converter (6850)
ADC	Analogue to Digital Converter
ADLC	Advanced Data Link Controller - ECONET control IC (68B54)
ADSR	Attack, Decay, Sustain, Release - defining the envelope of a sound
ASCII	American Standard Code for Information Interchange - binary code for representing alphanumeric characters.
BASIC	Beginners All-purpose Symbolic Instruction Code
BBC	British Broadcasting Corporation
BNC	Bayonet-Neill-Concelman - the type of bayonet connector used for the video output
CA1/2	Control lines associated with the PA port on a VIA
CAS	Column Address Strobe - control line for the DRAM
CB1/2	Control lines associated with the PB port on a VIA
CPU	Central Processor Unit (6512)
CR	Capacitor Resistor network
CRT	Cathode Ray Tube
CRTC	Cathode Ray Tube Controller IC (6845)
CSYNC	Composite SYNChronisation pulse train for video/TV display
CTS	Clear To Send - control input on the RS423 port
CUTS	Computer Users Tape Standard
DIN	European standard connector family used for the cassette socket, RGB socket etc
DRAM	Dynamic Random Access Memory
EPROM	Erasable Programmable Read Only Memory
FIT	Final Inspection Tester
FDC	Floppy Disc Controller (1770 or 8271)
IC	Integrated Circuit
ID	IDentity - refers to the unique number of a given ECONET station or paged ROM
IDC	Insulation Displacement Connectors - parallel cable connectors underneath the computer
IFEE488	A parallel interface usually associated with automatically controlled test instruments
I/O	Input Output
IRQ	Interrupt ReQuest - control line on the 6512 processor
MOS/OS	Machine Operating System or OS
MPU	Microprocessor Unit - same as CPU
NMI	Non-Maskable Interrupt - control line on the 6512 processor
PA	Port A - One of the two ports of a VIA
PAL	i) A feature of the British television colour system where colour information phase is varied on alternate lines. Hence Phase Alternate Line
PAL	ii) Abbreviation for a type of logic integrated circuit (IC) which is programmed by fusing microscopic links in the IC. Programmable Array Logic circuits are used to reduce the number of ICs needed on a circuit board
PB	Port B - The other port of a VIA
PCB	Printed Circuit Board.

PET	Test device designed for use with BBC Microcomputer Model B. Will work on the B+ but with different results, see information manual supplied to dealers
PHI1	CPU clock input - non-overlapping with PHI2
PHI2	CPU clock input also called 2E
PL	Header PLug
PORT	Test device for use with BBC Microcomputer Model B+
PSU	Power Supply Unit
Q1 etc	Transistor numbers
QWERTY	Signifies a standard typewriter key layout
RAM	Random Access read/write Memory
RAS	Rae Address Strobe - control line for the DRAM
RC	Resistor Capacitor network
RGB	Red Green Blue - individual colour signals for the VDU
ROM	Read Only Memory
ROMSEL	ROM SELect latch
RS423	An internationally defined convention for serial transmission of data
RTS	Ready To Send - control output on RS423 port
S1-30	PCB links
SK	Socket
TTL	Tranistor Transistor Logic - a standard type of digital IC (74- series)
UHF	Ultra High Frequency - signal for input to a TV aerial socket
ULA	Uncommitted Logic Array - semi-custom IC
VC	Variable Capacitor
VDU	Visual Display Unit
VIA	Versatile Interface Adaptor (6522)
VR	Variable Resistor
1E	A synchronous enable or clock for 65xx/68xx family peripheral ICs. 1E is a continuous 1MHz square wave
1M	1 MegaHertz from video processor
2E	A synchronous enable or clock for 65xx/68xx family peripheral ICs. 2E may have two or three half cycles suppressed to synchronise it to 1E
2M	2 MegaHertz from video processor
4M	4 MegaHertz from video processor
8M	8 MegaHertz from video processor

IC description

IC1 74LS123 Dual monostable (one half used, 8271 FDC only)

Required only by 8271 disc interface. This monostable defines the pulse width of data pulses from the disc drive during disc read operations. Pin 9 receives negative pulses from the disc drive, the monostable triggers on falling edges and generates a negative pulse of about 0.9us on pin 12.

IC2 74LS393 Dual divide by 16 (8271 FDC only)

This IC receives an 8MHz clock. Along with a NAND gate (part of IC9) this chip forms a digital timer/monostable. It is set to about 6.5us and gives the decision point between logic 0 and logic 1 data bits from the disc drive.

IC3 4013 CMOS dual J-K flip-flop (8271 FDC only)

The two J-Ks are used to detect disc speed. When a drive is off, pin 13 is set to logic 1 by the logic 1 notMOTOR signal fed through resistor R2. Pin 2 is held at 1 by the first J-K. Q19 of IC4 (pin 11) has no effect as D1 will always be biased off. When a drive starts, notMDTOR goes low allowing the first J-K to be clocked by index pulses. If an index pulse occurs when Q19 of IC4 is at 1 then the first J-K will stay set, which means the disc is slow. If Q19 is 0 when an index pulse occurs, the J-K will reset and allow the second J-K to be clocked. The next index pulse will set the second J-K (pin 2 goes low) indicating drive ready. This state is inhibited if the disc speed is slow, as the first J-K will be immediately set and so force the second J-K to reset (pin 2 high).

IC4 4521 CMOS 24 stage binary divider (8271 FDC only)

Used as a 2 to the power 18 divider. It counts cycles of 16/13 MHz to time a period of about 213ms (2^18*812ns). The divider is reset by each index pulse, so if Q19 goes high then the disc is slow. If the disc is very slaw, such that Q19 goes law high low between index pulses, the diode D1 ensures that the J-K (IC3) remains set.

IC5 74LS244 Octal buffer

Permanently enabled buffer for the CENTRONICS campatible printer interface data lines.

IC6 74LS244 Octal buffer

Permanently enabled buffer for the 1MHz extension bus. Buffered lines are four address lines LA0 to LA3, notPAGEFD, notPAGEFC, 1MHzE, and RnotW.

IC7 7438 Quad 2 input o/c NAND (either disc interface)

1) o/p pin 6 is drive select 1. Gates motor control and drive select from controller circuitry to form the external drive select. Must be able to drive a 150 ohm pull-up resistor hence cannot be LS TTL.
2) o/p pin 8 is drive select 0 (see above).
3) o/p pin 11 is used to buffer and invert the disc controller interrupt signal on to the wire-NOR notNMI interrupt line.
4) o/p pin 3 gates the 1770 DRQ on to the interrupt line. Used only with 1770 hence link S8 used to select 1770 (made) or 8271 (broken) option.

If IC7 is fitted and the disc controller is not, then IC7 pin 13 or pin 2 (or R14) must be pulled low to avoid notNMI being held low permanently which would stop the ECONET hardware from working.

IC8 7416 Hex o/c inverter

Converts active high signals from disc control circuitry into the active low signals required by the disc drive. Also gives increased signal drive capability.

IC9 74LS00 Quad 2 input NAND (8271 FDC only)

1) o/p pin 11 decodes the 6.5us time counted by IC2.
2) o/p pins 6 and 8 form an R-S latch. This latch generates the data window for the 8271 disc controller. When the interval between data pulses is 8us (logic 0 data) then the data window latch is set (pin 8 high) when the next data pulse is received. The data pulse always resets the latch. If the data pulse interval is 4us (logic 1 data) then the latch stays reset.
3) o/p pin 3 is used as an inverter to form the positive going index pulses needed to reset the CMOS counters used for disc speed timing.

IC10 6522 Printer/user VIA

This is a versatile interface adapter (VIA) IC. Half of it (A) provides a CENTRONICS compatible printer interface buffered via ICS. Handshaking is carried out via CA2 (strobe output buffered in IC13) and CA1 (ACK input). The (B) half is connected directly to PL10 and is called the User Port.

IC11 74LS374 Octal latch

This IC latches the low address signals AO to A7. These are used by 1MHz peripherals. The main function of the latch is to buffer the lines, but it also synchronises the lines so that changes can occur only while 1E is inactive (low). The latch is clocked by 1M, see also IC32.

IC12 74LS245 Octal bi-directional buffer

Used to buffer the 8 data lines from the data bus to the 1MHz expansion bus. Data direction is controlled by the de-glitched R/notW signal.

IC13 74LS244 Octal buffer

Used to buffer five address lines AO-A4, R/notW, and not2M for the TUBE interface. Also buffers the strobe handshake line for the CENTRONICS compatible printer interface.

IC14 74LS245 Octal bi-directional buffer

Used to buffer 8 data lines from the data bus to the TUBE interface. Is enabled only when TUBE is addressed.

IC15 8271 FM floppy disc controller (8271 FDC only)

Driven by the ACORN disc filing system software (FM - single density recording) to control 40 track or 80 track disc drives. Note the disc interface can be changed for 8 inch drive operation.

IC16 1770 FM/MFM floppy disc controller (1770 FDC only)

Driven by either the ACORN 1770 disc filing system software (for FM - single density recording) or by the ACORN advanced disc filing system software (for MFM - double density recording) to control 40 track or 80 track 5.25 inch disc drives (or any compatible alternative). The 1770 disc controller cannot be used in conjunction with 8" disc drives.

IC17 74LS174 Hex D-type (1770 FDC only)

This hex D-type latch is used for the disc control signals not generated by the 1770. Motor on/off, two drive select signals, and one side select signal are held in the latch. Also the disc format mode (single/double density) and a 1770 master reset signal are held in this latch. All these signals are under direct program control. The latch is addressed at &FE80.

IC18 74LS163 Presettable 4-bit counter

Configured as a divide by 13 to give 16MHz/13 clock for cassette and RS423 baud rate generation and disc speed detection.

IC19 74LS00 Quad 2 input NAND

1) o/p pin 11 detects a count of 12 on IC18 and generates a synchronous load pulse so that LC18 divides by 13.
2) o/p pin 8 is used as an inverter to generate notW for the system RAM.
3) o/p pins 3 and 6 are part of the decoder that converts the 2-bit code for display RAM size (from the addressable latch IC30) to the 4-bit code fed to the adder IC76.

IC20 6522 System VIA

This is a versatile interface adapter (VIA) IC. The A data lines are used for communication with the keyboard, speech system, and sound. CA1 is VSYNC from the CRTC, which interrupts the CPU every 2Oms. CA2 generates an interrupt when a key is pressed. PBO-PB3 drive the addressable latch IC30. PB4 and PB5 are inputs from the joystick fire buttons. PB6 and PB7 are inputs from the speech processor. CB1 is the end of conversion signal from the analogue to digital convertor LC84. CB2 is the light pen strobe signal from pin 9 of the 15-way D-type connector (SK6) used for analogue in.

IC21 74LS138 3 to 8 line decoder

This IC is enabled for address values &FE** (page FE), the Sheila L/O space. It is enabled when A8 is low and A9-A15 are high. The Sheila space is decoded into 8 blocks of 16 bytes. Each block is enabled when the corresponding decoder output is low.

LC22 74LS30 8 input NAND

Detects address values of &FC00 and greater. It forms the first stage of the I/O space address decoder logic.

LC23 74LS32 Quad 2 input OR

1) o/p pin 3 gates notW with the notFDC enable (address &FE80) to form the disc control latch clock.
2) o/p pin 6 gates notINTOFF/notSTATID with not2E to give a glitch-free active low preset signal for the ECONET NML control latch.
3) o/p pin 8 gates the 2M clock with notVLDPROC to form CAS enable signal which can only be active (high) during CPU RAM access (phi2 high).
4) o/p pin 11 gates notDEN with the latched D6 RAM data. So "D6" received by the teletext generator chip IC59 will be forced high during display blanking.

IC24 74LS04 Hex inverter

Used for inverting various signals around the board.

IC25 74LS109 Dual J-notK flip-flop

1) o/p pin 6 is a flip-flop clocked at 2M and samples the 1M signal to form the internal 1E and notlE clocks.
2) o/p pin 10 is used as a state machine to process 1 MHz cycle requests. When pin 10 is high it holds phi2 high until phi2 and 1E syncronise.

LC26 74S04 Hex inverter

Three parts are used in a ring of two, plus buffer, 16 MHz oscillator. The remaining three are used where inversion is needed on time critical signals.

IC27 74LS00 Quad NAND

1) o/p pin 3 is used to gate 2M with R/notW to form notR, a syncronous read enable used by the ADC and 8271 disc controller (if fitted).
2) o/p pin 6 is used to gate 2M with notR/W to form notW, a syncronous write signal used by the ADC and the 8271 disc controller (if fitted).
3) o/p pin 8 is used as an inverter to generate notRS, the system master reset.
4) o/p pin 11 is a spare gate. Inputs are tied to +5V.

IC28 74LS139 Dual 2 to 4 line decoder

1) o/p pins 10 and 12 split the FDC address space into two parts. Uses A2 and notFDC so that o/p 10 is low for address values &FE84 to &FE87 and o/p 12 is low for &FE80 to &FE83. The o/p's repeat in blocks of 4 up to address &FE9F. When S7 is East (1770 disc controller) 2M is used to enable the device o/p's so the enable signals are effectively synchronous with phi2.
2) o/p pins 4,5 and 6 decode the I/O pages FRED JIM and SHEILA. The decoder ' uses the I/O enable from IC22 and A8 and A9 to detect the 256 byte I/O blocks.

o/p 4 is FRED &FC**
o/p 5 is JIM &FD**
o/p 6 is SHEILA &FE**

1C29 TMS5220 Speech synthesiser (optional)

1C30 74LS259 Octal addressable latch

This device expands the number of output bits available for system contol functions. It is driven by the operating system through the system VIA (IC20).

IC31 74S74 Dual D-type flip-flop

1) o/p pin 6 disables the addressable latch IC30 during a CPU access of the system VIA, to avoid VIA o/p glitches disturbing the latch (IC30) contents. The function does not need schottky speed.
2) o/p pins 8 and 9 generate timing for RAS, the RAM row address clock. RAS is a delayed 4M clock, the delay being nominally 62.5ns (half period of 8M). This device is schottky to minimise device delay uncertainty.

1C32 74LS374 Octal D-type

This device is used to sychronise and de-glitch the 1MHz device control signals. By using 1M to clock the register, signal changes can only occur while lE is low (inactive).

IC33 74S02 Quad 2 input NOR

1) o/p pins 1,4 and 10 form the CPU clock generator. Outputs 4 and 10 are connected as an R-S flip-flop, which generates a non-overlapping two phase clock. Schottky is used for minimum gate delays and to allow low value pull-up resistors to be used. The pull-ups (R20 and R21) ensure the MOS logic 1 voltages needed by the 6512A CPU.
2) o/p pin 13 inverts the RAS timing signal to form notRAS, the RAM row address clock. The delayed RAS signal (RSL) is used to modify the high/low ratio of notRAS. NotRAS is held low for an extra lOns (approx) to meet the longest known Trsh spec of 120ns DRAMs. RSL controls the ROW/COLUMN address switching. The small delay between notRAS and RSL helps ensure the minimum RAM RAS address hold time is exceeded.

IC34 74LS08 Quad 2 input AND

1) o/p pin 3 combines the operating system enable with the BASIC language enable, so either will select the 32Kbyte ROM IC71. Logic 0 active.
2) o/p pin 6 combines two "NMI" signals (notNMI and notINT) to form the complete notNMI interrupt for the CPU.
3) o/p pin 8 operates with 2 EX-OR gates (IC63) to reduce the refresh address cycle time when in display mode 7.
4) o/p pin 11 combines the JIM and FRED enables. This signal, active law, indicates a 1MHz bus cycle is in progress.

IC35 various 64K, 128K or 256Kbit paged ROM

A 32Kbyte device in this socket appears in sideways ROM slots 2 and 3 (link S9 East). Link S9 West allows 8 or 16Kbyte EPROMs/ROMs to be fitted. IC35 can be any ROM or EPROM with a notCE access time less than 250ns.

IC36 16R4 Programmable array logic (PAL) IC (ACORN no 0201,880)

This device generates 4 enable signals:
1) A14 and A15 are decoded to form notOS, which is low when A14 AND A15 are logic 1.
2) A14 (low) AND A15 (high) are decoded to form notPG, the current sideways ROM enable. If sideways RAM is enabled (SRAM=1) then notPG is forced high while A12 OR A13 is low.
3) [A12 (low) OR A13 (low)] AND A14 (low) AND A15 (high) are decoded. The address decoded is ANDed with the sideways RAM enable bit (SRAM) to form notPGRAM. NotPGRAM will be low (active) if sideways RAM enable (SRAM) is logic 1 and the current address is between &8000 and &AFFF.
4) notPGLD is formed by decoding notROMSEL and A2. NotPGLD is low (active) when notROMSEL is law AND A2 is low.

The PAL contains two addressable 1 bit latches (write only):
1) VDUSEL is addressed at &FE34, and latches the value of D7. VDUSEL is the hardware SHADOW mode switch. Logic 0 is normal mode, which emulates the standard model B microcomputer VDU operation.
2) SRAM is addressed at &FE30. SRAM is an extension to the ROM select latch and holds the value of D7. This bit is the sideways RAM select flag. The signal is labelled "Qh" in the PAL spec (0201,880).

The PAL monitors the state of VDUSEL to determine if a shadow display mode is active. When VDUSEL is high (shadow active), the PAL checks the address of each CPU opcode fetch. If the opcode address is in the VDU driver code space then a temporary 1-bit flag is set (in the PAL). The flag remains set until an opcode outside the VDU driver code space is read. While the flag is set, all CPU access to memory between &3000 and &7FFF is redirected to the shadow RAM. The redirection is achieved by manipulating the "A15" RAM address line. The RAM A15 address is generated by the PAL, and is the signal CPUSEL. Normally CPUSEL is the same as the CPU A15 address signal. When the flag is set, the PAL tests each CPU address and forces CPUSEL high if the address is in the range &3000 to &7FFF. So in shadow mode the CPU will access the shadow screen RAM for VDU operations and normal RAM for all other operations. VDU driver code is identified by its memory address. All code between address &C000 and &DFFF is treated as a VDU driver. Also, code in the paged RAM between &A000 and &AFFF is treated as a VDU driver (but not in paged ROM).

From the above it is apparent that any program code in the VDU code spaces must not address RAM between &3000 and &7FFF unless it intends to write to the shadow RAM (screen).

IC37 TMS6100 Speech PHROM

A serial ROM which contains the speech vocabulary data, used by 1C29.

IC38 SN76489 Sound generator.

This IC contains three sound channels and one noise channel. The sound pitch, attack, sustain, decay, and release are independently programmable from BASIC or machine code. Control is exercised through the system VIA IC20.

IC39 74LS139 Dual 2 to 4 line decoder

1) o/p pins 4,5,6 and 7. This decoder, is enabled by IC21, for I/O address values between &FE00 and &FE1F. The IC uses address lines A3 and A4 to complete the I/O address decoding for the CRTC (&FE00/1), ACIA (&FE08/9), SERPROC (&FE10) and the ECONET control signal notINTOFF/notSTATID (&FE18).
2) o/p pins 9,10,11 and 12 decode address values &FE20 to &FE3F into 2 write only blocks and 2 read only blocks (only one is used). At &FE20 (WR) is the VIDPROC. &FE20 (RD) is INTON, an ECONET control. &FE30 to &FE3F (WR) is "ROMSEL" space, see PAL IC36

1C40 74LS20 Dual 4 input NAND

1) o/p pin 6 controls the paged ROM notOE signal. All paged ROMs are disabled during CPU write cycles by this gate (R/notW i/p). ROMs are also disabled for the I/O address space (FRED, JIM and SHEILA). The not2M clock ensures ROMs can only drive the data bus during phi2 which avoids bus drive conflicts during address changes.
2) o/p pin 8 "ORs" three active low signals to form an active high RAM data request signal. A15 low OR notPGRAM low OR notVIDPROC low will enable the RAM data buffer IC49, see IC48 o/p 12.

IC41 74LS30 8 input NAND

ORs five I/O enable signals to form the active high 1MHz cycle signal SYNC 1M. This signal is used by IC25 to trigger lE and phi2 clock syncronisation. The five input signals correspond to the various I/O devices which operate with 1MHz (1E) interface timing.

IC42 6512A CPU

The 6512A is a member of the NMOS 6500 processor family. This IC is functionally similar to a 6502A, the only significant difference being the clock drive. A 6512A uses MOS level clocks (phil and phi2) and so gives more precise system timing than is possible with the 'TTL "phi in" clock of the 6502A.

THE TWO PROCESSOR TYPES ARE NOT INTERCHANGEABLE.

This microcomputer can use 2,3 or 4 MHz CPU parts (6512A/B/C)

IC43 NE555 Monostable IC

The 555 is used as a monostable for generation of the microprocessor system reset pulse. It is triggered at power-on or by the keyboard BREAK key. A logic 1 active output pulse is generated and part of IC27 inverts RS to form notRS, the CPU reset.

IC44 various 64K,128K or 256Kbit paged ROM

A 32Kbyte device in this socket appears in sideways ROM slots 4 and 5 (link Sll East). Link S11 West allows 8 or 16Kbyte EPROMs/ROMs to be fitted. This device can be any ROM or EPROM with a notCE access time less than 250ns.

IC45 74LS163 Synchronous divide by 16 counter

Used as a 4-bit latch which holds the paged ROM LD. The IC is clocked by not2E. When the latch is addressed, at &FE30, its LD enable is taken low (active) and the write data on the CPU data lines DO to D3 is latched. The load event is effectively when phi2 falls. The QA output (latched DO) is used as a pseudo address line for 32Kbyte ROMs/EPROMs and so splits these devices into two 16Kbyte pages.

IC46 74LS138 3 to 8 line decoder

This decoder is enabled by the notPG signal from the PAL (1C36). When enabled the decoder selects one of the RCM sockets, according to the code held in LC45. Each enable output is active for 2 paged ROM IDs as the decoder uses the latched values of Dl to D3. S13 is used to select the page number for the "language" half of IC71 (normally BASIC II). S13 North selects page 0/1. South selects page 14/15.

IC47 LM324 Quad operational amplifier

The four parts of this IC are used to filter and amplify the speech and sound signals before they reach the volume control.
1) o/p pin 1 is the final filter stage, nominal bandwidth of 7kHz.
2) o/p pin 7 is the speech audio filter stage, approximately 7kHz bandwidth.
3) o/p pin 8 is the summing stage, mixes sound, speech, speech envelope and user audio inputs into one channel.
4) o/p pin 14 extracts the sound channel envelope. The op amp inverts the sound signal and charges C15 through D4. R34 discharges C15 " slowly", so C15 holds the sound envelope voltage (inverted). When the envelope is added to the sound audio, the resulting signal is "AC", that is symmetric about OV.

IC48 74LS10 Triple 3 input NAND

1) o/p pins 6 and 8 are part of the hardware scroll wrap around logic. With parts of IC19 they decode the screen size code, CO and Cl from IC30, to drive the offset adder IC76.
2) o/p pin 12 enables the RAM data bus buffer IC49 and the RAM write signal. The logic 1 request input from IC40 pin 8 is gated with not2M to form notENM, the 0 active RAM enable signal. Not2M is used to ensure the enable is only active during the CPU phase, ie while phi2 is high. This avoids bus conflicts during phil. Also it forces the RAM to be "read only" during VDU cycles. Note the buffer is active for RAM or VLDPROC access. During a VIDPROC write the RAM is disabled by holding notCAS at logic 1 (see IC23 and IC52).

IC49 74LS245 Octal buffer

The RAM and VIDPROC data bus buffer. This IC isolates the RAM data bus from the CPU data bus to allow VDU read cycles to occur without interference from the CPU data bus, particularly during 1MHz device cycles. Another important function of the buffer is to reduce the CPU data bus loading by isolating the RAM and VIDPROC etc.

IC50 and IC51 74LS257 Quad two to one data selector

These two ICs select the RAS and CAS address signals from the CPU address lines. The CPU A15 is not used. The "A15" input is the CPUSEL signal from the PAL IC36. The CPU address is only valid during phi2 high because IC50 and IC51 are disabled (held tristate) while phi2 is law. phi2 low is the VDU RAM access period. 2M is used as an enable to avoid loading the phi clocks.

IC52 74S00 Quad 2 input NAND

1) o/p pins 3 and 6 connected as an R-S flip-flop. The set and reset signals are the inverted and delayed 4M and 8M clocks respectively. The output signal on pin 3 is the precursor of the 6MHz clock used by the TELETEXT display circuit. See IC63 o/p 3.
2) o/p pin 8 is used to drive the RAM notCAS clock. NotCAS is timed from the system 4M clock. notCAS is held high, if the CPU cycle is a VIDPROC write, by a logic low from IC23 pin 8.
3) o/p pin 11 is used to modify the duty cycle of the 16MHz clock to suit the needs of the Ferranti ULA (IC53). Note the passives R36,R37, R38 C14,D5,D6,D7 may also be needed for the Ferranti IC.

IC53 ULA Video processor IC

This component contains a 4-bit divider which generates the 8/4/2 and 1MHz system clocks. It also selects the RGB signals, internal for modes 0 to 6 and external, from LC 59, for mode 7. The RGB can be inverted if link S14 is made South. The main function of the IC is parallel to serial conversion of the display data read from RAM and the logical translation of the pixel code to the 3-bit RGB "code" of each display pixel. The translation process varies with screen resolution (mode). A pixel may be represented in RAM by 1,2 or 4 bits of data.

IC54 74LS273 Octal D-type

This IC latches the RAM data at the end of alternate VDU phases. It is needed to hold the data for the teletext IC which has long data setup and hold times. The latch is clocked 500ns before the SAA5050 IC59, giving equal setup and hold times of 500ns.

IC55,56,60,61,64,65,66,67 4164 64Kx1 bit 120ns access DRAMs

These eight ICs are the system memory. The RAM appears as a 32Kbyte block from &0000 to &7FFF. A further 20Kbytes are used for a "SHADOW" screen memory. The remaining 12Kbytes is PAGED in under program control as a sideways RAM. Note IC96, a DRAM SIL pack, may be supplied instead of these ICs.

IC57 various 64K,128K or 256Kbit paged ROM

A 32Kbyte device in this socket appears in sideways ROM slots 6 and 7 (link S12 East). Link S12 West allows 8 or 16Kbyte EPROMs/ROMs to be fitted. This device can be any ROM or EPROM with a notCE access time less than 250ns.

IC58 74LS02 Quad 2 input NOR

1) o/p pin 1 mixes the video display sync pulses HS and VS to form notCSYNC. The HS pulse is nominally 4us long. VS is nominally 132us (2 TV rasters) long.
2) o/p pin 4 gates the buffered. CPU R/notW with notENM to form the DRAM W signal, which is buffered and inverted by LC19 to form notDW.
3) o/p pin 10 gates notDEN and RA3 (from the CRTC) to form the DIS EN signal. DIS EN high enables the VIDPROC generated RGB signals. It does not affect mode 7. This signal is used to blank the display: notDEN is high for periods outside the display window and so blanks the graphic mode borders. RA3 is only active for the text only "graphic" screen modes (modes 3,6,131 and 134), when the signal causes a 2 raster space between each text row. In modes 3,6,131 and 134 the CRTC RA lines count from 0 to 9. The other modes have only 8 raster lines per character row so the RA lines count from 0 to 7, therefore RA3 only goes high for modes 3,6,131 and 134.
4) o/p pin 13 is part of the colour burst monostable. The o/p signal enables the colour subcarrier during the colour burst interval. R76 and C32 determine the pulse duration which is set at manufacture to be in the range 4 to 6us. D15 is used to discharge C32 quickly during the HS pulse period. The monostable is "triggered" at the end of the HS pulse.

IC59 SAA5050 The Teletext display generator

The SAA5050 contains the character look up ROM, the raster counter and general control logic needed to generate the pixel information for mode 7. The IC receives character data codes from IC54, at a rate of 1MHz. VS is used to reset the IC at the start of each TV field and so maintain display synchronisation, particularly with the internal raster counter. Character rounding is permanently on. The notRA0 line, from the CRTC via IC24, gives the SAA5050 information on the current TV display' field, odd or even, to allow character rounding.

IC62 various 64K,128K or 256Kbit paged ROM

A 32Kbyte device in this socket appears in sideways ROM slots 8 and 9 (link S15 East). Link S15 West allows 8 or 16Kbyte EPROMs/ROMs to be fitted. This device can be any ROM or EPROM with a notCE access time less than 250ns.

IC63 74LS86 Quad 2 input EX OR

1) o/p pin 3 is part of the 6MHz clock circuit.
2) o/p pins 6 and 8 are used to modify the CRTC address during the unused read cycle of mode 7 VDU cycles. Along with IC34 o/p pin 8 these gates form a circuit which reduces the time taken to cycle through the refresh address sequence when in mode 7.
3) o/p pin 11 is a spare gate, inputs tied to +5V.

IC68 various 64K,128K or 256Kbit paged ROM

A 32Kbyte device in this socket appears in sideways ROM slots 10 and 11 (link S18 East). Link S18 West allows 8 or 16Kbyte EPROMs/ROMs to be fitted. This device can be any ROM or EPROM with a notCE access time less than 250ns.

IC69 74LS74 Dual D-type flip-flop

1) o/p pin 6; this flip-flop holds the ECONET NMI enable signal. The flip-flop is used as an R-S latch. When address &FE18 is read/written, the latch is set (o/p 6 low), which disables ECONET NMIs. IC23 o/p 6 gates not2E with the decoded address to give a glitch-free preset pulse. To enable the NMIs, address &FE20 is read. The decoded address signal appears as logic 0 on the D i/p and is clocked through by the rising edge of not2E (eg when phi2 falls). This clears the D-type (pin 6 high) and by the feedback action of Q connected to notCL locks the D-type in the reset state (ie notINTON high will not cause the D-type to became set). Note as notPR (pin 4) acts directly on the Q o/p it can defeat the notCL i/p and set the device.
2) o/p pin 9 generates the alternate line signal which is used by the PAL encoding logic to encode the chroma signal. The D-type is clocked by HS and so changes state at the start of each TV raster line (divides the line frequency by two). Link S28 (made with a PCB track) allows the alternating line signal to be disconnected, for NTSC operation. Note: for NTSC R92 should be removed and an appropriate colour subcarrier crystal fitted. X2 should be four times the colour subcarrier frequency. The RF modulator must also be chosen to suit the destination country.

IC70 74LS132 Quad 2 input schmitt trigger NAND (ECONET only)

Note: when collision detect is not used (IC93 not fitted) IC70 can be the cheaper 74LS00.
1) o/p pin 3 inverts notRTS. If the collision detect circuit is fitted, this gate buffers IC93 to give a true "no collision" signal. Its main purpose is to give clean TTL level signals with normal TTL transition times.
2) o/p pin 6 forms the notCTS signal used by IC81 to check for network collisions. Input 5 ensures the signal is always false if the network clock is not present.
3) o/p pin 8 gates the network NMI enable with the true "INT" signal to form notINT. NotINT is the ECONET notNMI signal which is passed to the CPU via IC34. R56 is only needed on machines built without an ECONET interface.
4) o/p pin 13 inverts notIRQ from IC81 to form IRQ. This signal is treated as an NMI by the system (when enabled by IC69). NotINT is an open drain o/p so R59 is needed as a logic high pull-up.

IC71 OS/BASIC

A 32Kbyte ROM. The top half addressed from &C000 to &FFFF (except for 0.75Kbyte I/O) contains the machine operating system program. The bottom half is a paged ROM containing BBC BASIC II. Link S13 selects the BASIC ROM slot number: South selects slots 14/15 (standard configuration, high priority), North selects slots 0/1 (low priority). Link S19 is permanently made East for CPU address A14 to pin 27 of ROM IC.

IC72,73,74,75 74LS253 Dual 4 to 1 data selector

These four ICs select the DRAM address signals according to the current display mode and RAS/CAS state. Not2M enables the four ICs during the VDU RAM read phase. RSL drives pin 14 to select the RAS or CAS address signals, RSL low selects the row address (notRAS clock). MA13 from the CRTC IC78 selects the node 7 address group when high. MA13 is low during all the "graphics" screen modes. The VDUSEL signal from IC36 is low for normal screen nodes and high for all shadow screen modes.

IC76 74LS283 4-bit adder

The adder is used to modify the natural display address from the CRTC IC78. Take mode 0 as an example. Mode 0 uses 20Kbytes of RAM from &3000 to &7FFF. If the CRTC display is scrolled (in hardware) then the address from the CRTC will be, say, &4000 to &8FFF (assumes a scroll step of &1000). The display memory must still be &3000 to &7FFF. To keep the CRTC address, as seen by the RAM multiplexer, correct, an offset is conditionally added to the actual CRTC address. The offset is 12K. As the address-logic does not generate an address above &8000 there is no use for address line A15 (MA13). Thus when the CRTC scrolls above &8000 it appears to address &0000 upwards. By adding " 12K" the RAM address becomes &3000 upwards. So although the CRTC outputs an address outside the allowed RAM address, the adder causes the true address to remain in the allowed range of &3000 to &7FFF. This principle is used for all graphic screen modes (ie all but mode 7).

There are four different graphic screen sizes, 8/10/16/20Kbytes. The adder therefore needs to "add" an offset of 24K/22K/16K/12K respectively. The operating system gives a 2-bit code labelled C0,C1 which is decoded to give the adder offset for the current screen mode.

C1	C0	Offset	adder input B4	B3	B2	B1
0	0	16K	0	1	1	1
0	1	8K	1	0	1	1
1	0	20K	0	1	0	1
1	1	10K	1	0	1	0

IC77 LM386 Audio power amplifier

This IC is a low-cost amplifier with a fixed voltage gain of about 26db. C24 and R58 are needed to give load independant output stability (freedom from parasitic oscillation).

IC78 6845 CRTC controller

The CRTC is responsible for all VDU address generation. It is a programmable device which, once set up, independantly generates the RAM address sequence for a wide range of display formats. The IC can " scroll" the display by responding to a change in the value of the display start address. A programmable cursor and the horizontal and vertical sync pulses are also generated by this IC. Included in the IC is an address latch which is used with the "light pen" input to save the character address at the time of a trigger event on pin 3 of the IC. The device is accessed at 1MHz by the CPU at &FE00/1. A character clock of 1 or 2MHz is supplied by the VIDPROC, depending on the VDU mode.

IC79 74S74 Dual schottky D-type flip-flop

The two parts of this IC are used in a ring counter which is clocked at four times the colour subcarrier frequency (17.734475MHz). Each D-type generates an output at the colour subcarrier frequency (4. 43361875MHz). The two signals are in phase quadrature (90 degrees apart) and form the master signals for the PAL chroma encoding logic. The signal on pin 8 is set to 4.4336MHz +/-100Hz by adjustment of VC1.

IC80 74LS244 Octal 3-state buffer

The 8 buffers in this IC are used to drive the CPU data bus with the ECONET station ID. The buffers are enabled when the CPU reads address &FE18. A write to &FE18 will result in a data bus drive conflict and should not be attempted. Link S23 sets the station ID. Each link has a binary value with the largest, 128 (decimal), at the North end of the row. A broken link (shunt removed) adds the link value to the station ID eg all links fitted gives 0.

IC81 68B54 Serial data link controller (ECONET only)

This IC is an ADLC (advanced data link controller). It is responsible for transmitting and receiving serial data to and from the ECONET. Each byte of an ECONET transfer is under interrupt control, and is managed by a network filing system. The notRTS signal is controlled by software. It enables the ECONET line driver IC91. NotDCD is driven by a clock detection circuit to allow a program to detect the network clock. NotCTS is tested to check for network data packet collisions, see comments on collision detection under IC93. NotIRQ is used as an NMI interrupt, which is enabled/disabled under program control (see IC69 and IC70). A 4k7 pull-up resistor R59 is fitted when IC81 is present, as notIRQ is an open drain output.

IC82 6850 ACIA (UART)

A UART is a serial asyncronous interface circuit which can both transmit and receive data. The 6850 is used for parallel to serial data conversion for either the cassette interface or the RS423 interface. Three handshake signals are available, notDCD, notRTS, and notCTS. These can be tested by the controlling program to determine interface status. Two clock inputs allow the transmit and receive bit rates to be set independently. The two clocks are generated in the SERPROC IC85.

IC83 74LS86 Quad two input EXOR

1) o/p pin 3 is part of the TV colour (PAL) encoder circuit. One of four EXORs is used to select the phase of the colour subcarrier reference needed to synthesise the colour subcarrier for a particular colour.
2) o/p pin 6 see above (o/p pin 3).
3) o/p pin 8 is used to select the polarity of the CSYNC signal on the RGB connector SK3. With link S27 set North, positve syncs are generated. S27 South (the normal setting) gives negative syncs.
4) o/p pin 11; this gate is driven by the alternate line divider IC69 and shifts one of the master colour subcarrier references by 180 degrees to give the phase alternating line (PAL) subcarrier. PAL can be disabled by making S28 South.

IC84 upD7002 4-channel analogue to digital converter

. Analogue signals input via SK6 are converted (about 10ms per channel) to a 12-bit digital value. The ADC informs the processor of a completed conversion by interrupting it (IRQ). Interrupts are generated by the system VIA IC20 when it receives an active notEOC signal. Three diodes (D9 D10 D11) in series are used for the voltage reference which is typically 1.8 volts with a -6mV per degree C temperature coefficient. Note that the accuracy of the ADC part is equivalent to a resolution of about 8 bits.

IC85 ULA Serial processor IC

The SERPROC handles the RS423 and cassette interface circuits. Built into the IC are programmable clock generators which set the serial bit rate. Signals from the selected interface (RS423 or cassette) are routed to/from the 6850 IC82 by this IC. The replay cassette signals are demodulated in
IC85 and a bit clock signal is recovered. A preamble tone is timed to initialise data reception. When fitted, R66 and C30 are used to time the preamble tone. Motor control of a cassette recorder is managed by the SERPROC. A control bit in the IC controls the relay RL1. The control signal on pin 11 is buffered by Q7 which switches the relay coil (50 ohm).

IC86 74LS86 Quad two input EXOR

1) o/p pin 3 generates a colour subcarrier reference component according to the current display colour.
2) o/p pin 6 is one of three gates which generate control signals to gate the subcarrier component signals into the resistor matrix, by enabling or disabling NAND gates in IC90.
3) o/p pin 8 see o/p pin 6
4) o/p pin 11 see o/p pin 6

IC87 74LS00 Quad two input NAND

1) o/p pin 3 buffers the colour reference oscillator to ensure TTL levels.
2) o/p pin 6 is used as an inverter. It drives the colour burst timing components R76 and C32 with notHS, see IC58 o/p pin 13.
3) o/p pin 8 is one of two gates which drive the colour subcarrier resistor matrix with the colour burst subcarrier components. Input pin 10 receives an enable pulse from the colour burst monostable.
4) o/p pin 11 is the second gate of the colour burst generator.

IC88 74LS123 Dual monostable (ECONET only)

1) o/p pin 5 determines the maximum allowed transmission period for an ECONET data packet. The monostable's duration is set to about 4.5s and is triggered by the inverted ECONET controller notRTS signal (which previously directly enabled the line driver). While triggered the monostable enables the line driver IC91. At the end of a transmission the monostable is cleared. Normally the monostable output (pin 4) appears logically to follow the RTS signal. The real purpose of this circuit is to stop a micro from permanently driving the ECONET line as a result of, say, a user program crash.
2) o/p pins 4,13; this monostable is triggered by the received clock from an ECONET line. While the clock is present the monostable remains triggered, o/p pin 4 low. If the clock is not present or is very slow, then o/p pin 4 will oscillate or stay set. The state of the monostable can be checked directly, by the ECONET filing system testing the 68B54 notDCD signal.

IC89 LM324 Quad operational amplifier

1) o/p pins 1,8,14 give two stages of filtering and one limiting amplifier stage for the received cassette audio signal. When the audio is present, a 1.2 volt (approx.) square wave will be presented to the SERPROC.
2) o/p pin 7 buffers the audio output to the cassette recorder.

IC90 74LS00 Quad two input NAND

o/p pins 3,6,8,11 are four gates which are selectively enabled to drive the colour subcarrier resistor mixing matrix, to generate the colour subcarrier phase for the current display colour. L1, C40 and R113 in parallel with R114 form a simple low Q band pass filter tuned to the colour subcarrier frequency (4.43MHz), which reduces the harmonics of the chroma (colour) signal.

IC91 75159 Dual RS422 line driver (ECONET only)

1) o/p pin 2 used as an inverter. Forms a true RTS signal to trigger/clear the ECONET timer monostable.
2) o/p pins 12,13 drive the ECONET data lines with an RS422 differential signal. An RS422 signal has nominal TTL logic levels; two lines are driven to opposite logic states, to give differential signal transmission. The gate is capable of driving a 50 ohm load tied to 2.5 volts. When the ECONET interface is inactive (not transmitting) the driver is in a high impedance state. A logic 1 on pin 9 enables the driver.

IC92 LM319 Dual analogue comparator (ECONET only)

1) o/p pin 7 senses the ECONET clock signal. R78 introduces a small amount of hysteresis to avoid self-oscillation of the comparator when no signal is present (which would result in permanent clock present indication). R63 is a pull-up, the comparator has an open collector output. The comparator receives an attenuated clock signal which is also positively biased. R125,134,140,141 form an attenuator (approximately 10:1). R147 with R148 sets a bias of about 2 volts so the comparator input signals stay within the supply voltage (5 volts).
2) o/p pin 12; this comparator receives data from the ECONET line. R73 is a pull-up and R79 gives the comparator hysteresis. R106,110,142,143 form an attenuator (approximately 10:1). Again the inputs are biased to nominally 2 volts. The comparator converts the differential ECONET data signal to single ended TTL which is decoded in IC81, the ADLC. The LM319 comparator is sufficiently sensitive to allow high impedance attenuators to be used while still detecting the ECONET idle line state. An idle line has a differential voltage of about 0.6 volts impressed on it by the ECONET line termination networks (not part of the micro).

IC93 LM319 Dual analogue comparator (not normally fitted)

This comparator circuit is not normally fitted. When fitted its purpose is to detect data packet collisions on the ECONET. Collisions are normally avoided by the network filing system protocol, and so are rare. When a collision occurs it will result in data corruption (detected by the filing system error checks when collision detection hardware is not fitted). If collision detection should be required then link S29 should be broken and IC93 and its associated components fitted.

IC94 88LS120 Dual RS423 receiver circuit

1) o/p pin 7 receives the RS423 port data signal. This input is also compatible with RS232 data. To reduce the voltage swing the signal is attenuated by 8124,118. C31 reduces the signal bandwith and so reduces the risk of glitches in the received signal presented to the SERPROC.
2) o/p pin 9 receives the RS423 notCTS control signal. 8149,152 attenuate the voltage levels while C35 "filters" the signal.

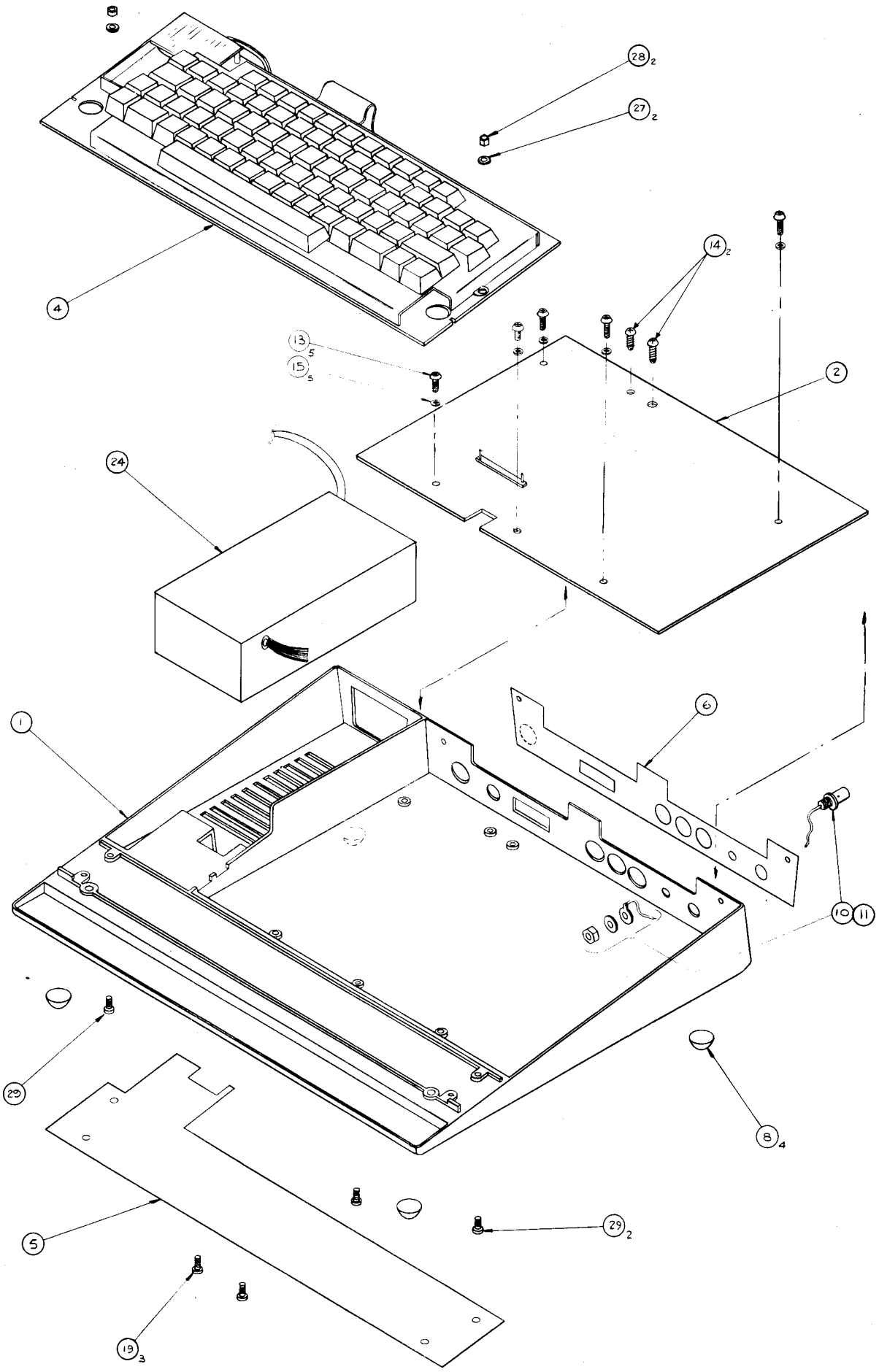
S24 and S25 are optional links which connect internal termination resistors to ground. These links should not be fitted.

IC95 3691 Dual RS423 line driver

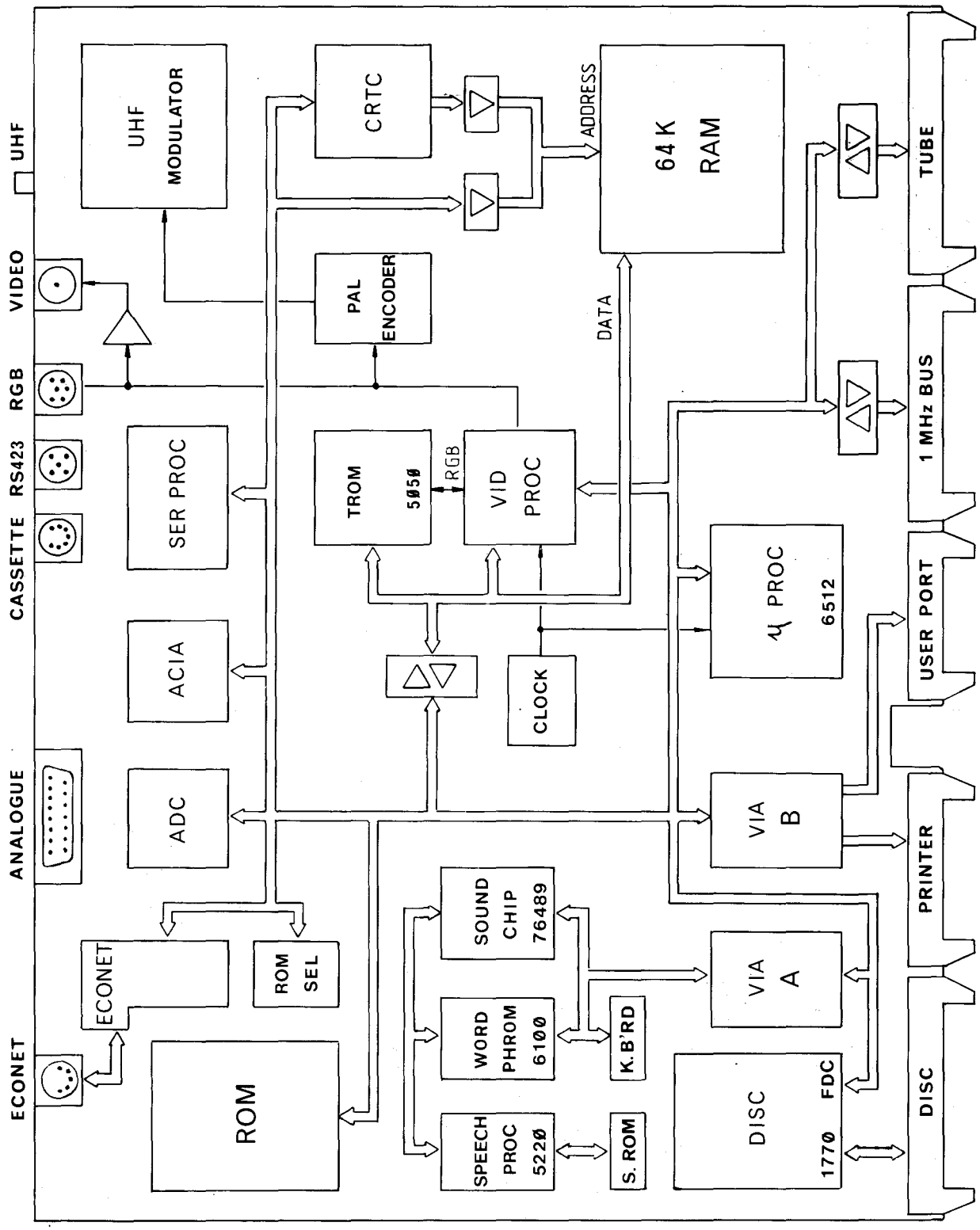
1) o/p pin 10 drives the notRTS control line with an RS423 compatible signal. C45 slew limits the signal to reduce electromagnetic radiation which might cause interference to other equipment. Note in most applications this line can interface to an RS232 device.
2) o/p pin 15 drives the data line of an RS423 interface. C44 slew limits the signal.

IC96 4164EK8 SIL pack 64Kbyte DRAM, 120ns access

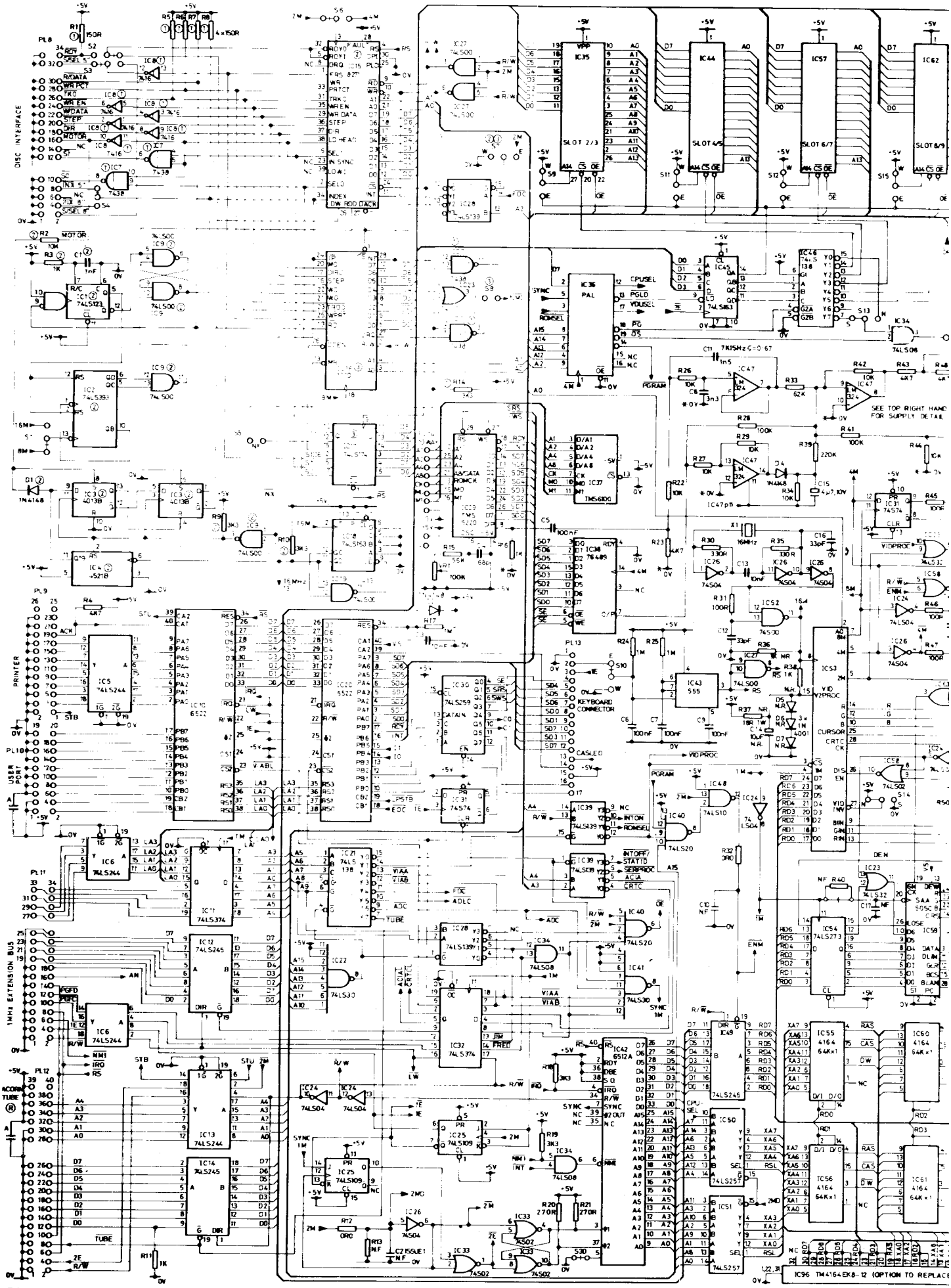
This device can be fitted as an alternative to 8 off 64Kx1 DRAM integrated circuits ICs 55,56,60,61,64,65,66,67.



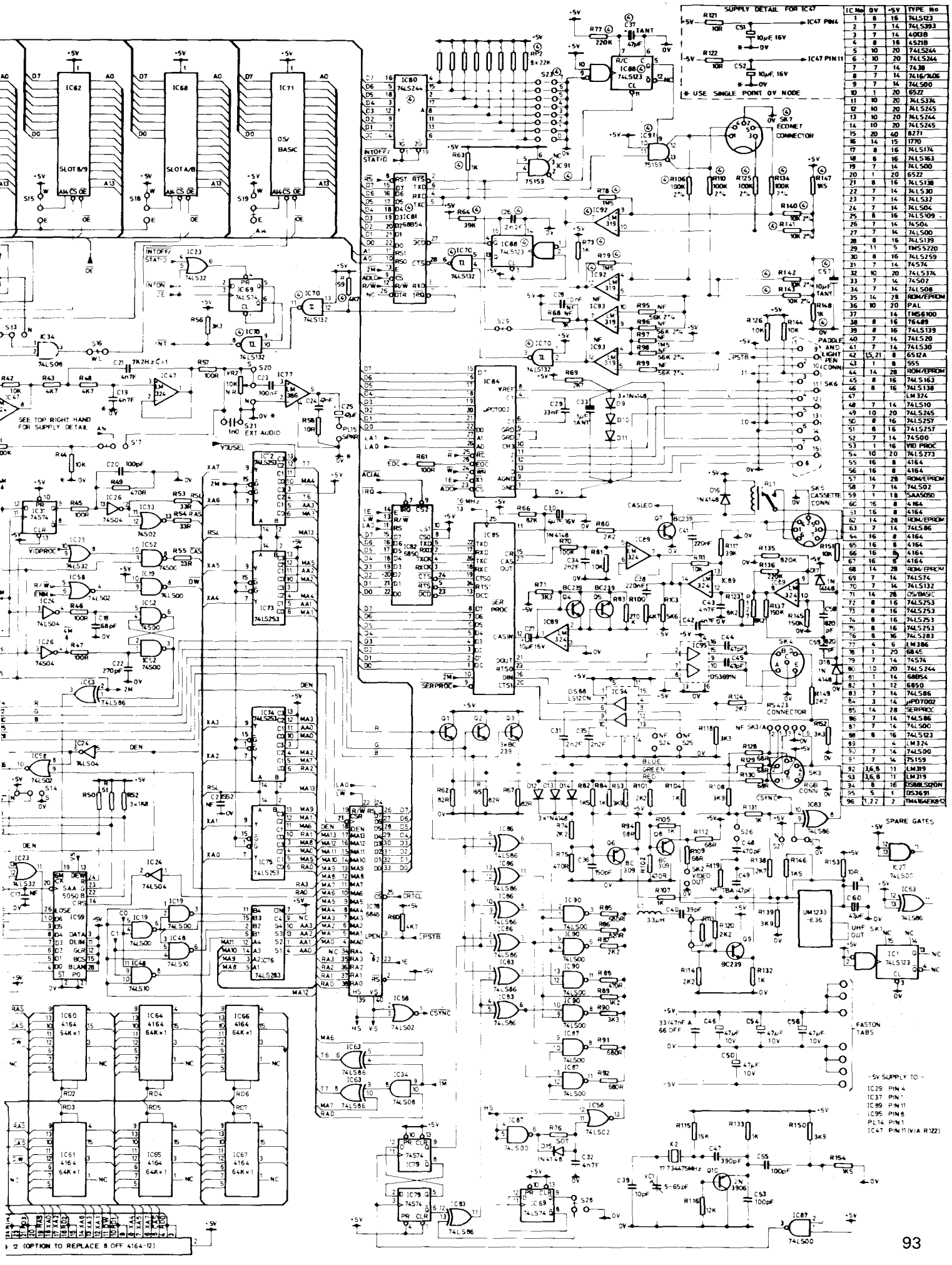
Final assembly



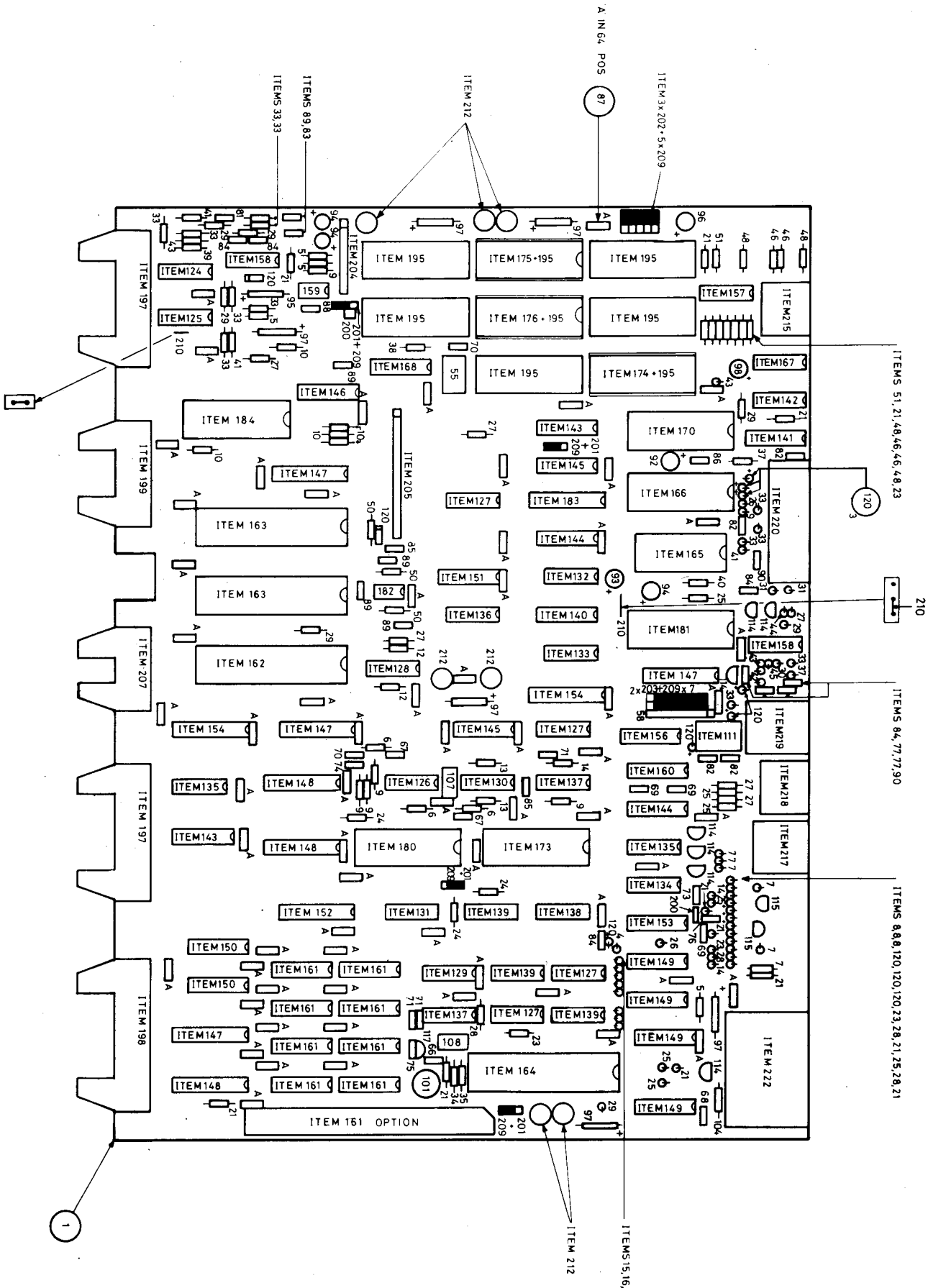
Circuit block diagram



PCB circuit diagram

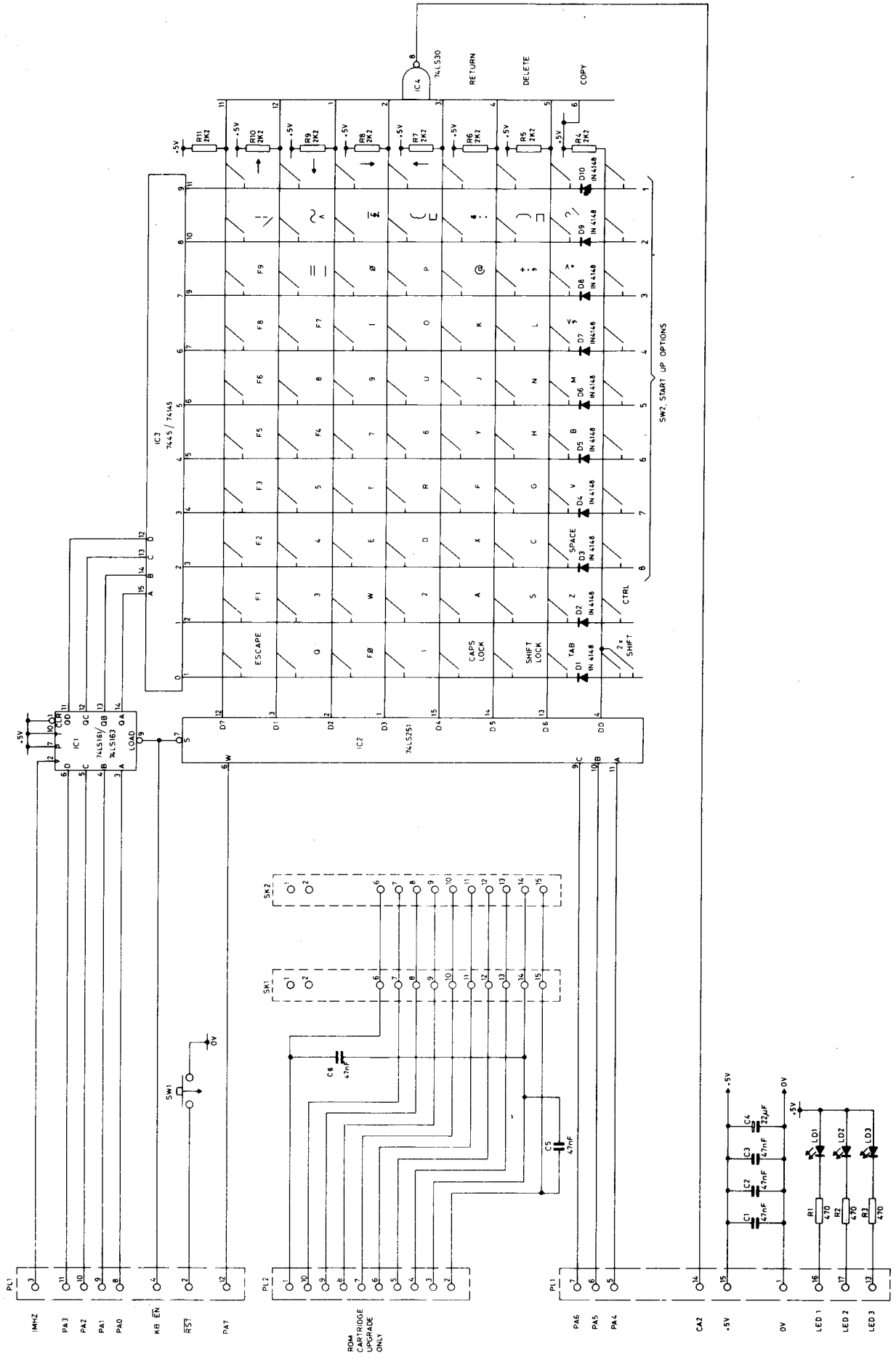


IC No	0V	+5V	TYPE No
1	8	16	74LS123
2	7	14	74LS393
3	7	14	4030B
4	8	16	6521B
5	10	20	74LS244
6	10	20	74LS244
7	7	14	7438
8	7	14	7416/7406
9	7	14	74LS00
10	1	20	6522
11	10	20	74LS374
12	10	20	74LS245
13	10	20	74LS244
14	10	20	74LS245
15	20	40	8271
16	14	15	1770
17	8	16	74LS174
18	8	16	74LS163
19	7	14	74LS00
20	1	20	6522
21	8	16	74LS138
22	7	14	74LS30
23	7	14	74LS32
24	7	14	74LS04
25	8	16	74LS109
26	7	14	74S04
27	7	14	74LS00
28	8	16	74LS139
29	11	5	TMS5220
30	8	16	74LS259
31	7	14	74S74
32	10	20	74LS374
33	7	14	74S07
34	7	14	74LS08
35	14	28	ROM/EPROM
36	10	20	PAL
37	8	14	TMS4100
38	8	16	7640B
39	8	16	74LS139
40	7	14	74LS20
41	7	14	74LS30
42	15,21	8	6512A
43	1	8	555
44	14	28	ROM/EPROM
45	8	16	74LS163
46	8	16	74LS138
47			LM 324
48	7	14	74LS10
49	10	20	74LS245
50	8	16	74LS257
51	8	16	74LS257
52	7	14	74S00
53	1	16	VID PROC
54	10	20	74LS273
55	16	8	4164
56	16	8	4164
57	14	28	ROM/EPROM
58	7	14	74LS02
59	1	18	SAA5050
60	16	8	4164
61	16	8	4164
62	14	28	ROM/EPROM
63	7	14	74LS86
64	16	8	4164
65	16	8	4164
66	16	8	4164
67	16	8	4164
68	14	28	ROM/EPROM
69	7	14	74LS74
70	7	14	74LS132
71	14	28	OS/BASIC
72	8	16	74LS253
73	8	16	74LS253
74	8	16	74LS253
75	8	16	74LS253
76	8	16	74LS283
77	4	6	LM386
78	1	20	6845
79	7	14	74S74
80	10	20	74LS244
81	1	14	68B54
82	1	12	6850
83	7	14	74LS86
84	3	14	μPD7002
85	14	28	SERPROC
86	7	14	74LS86
87	7	14	74LS00
88	8	16	74LS123
89		4	LM324
90	7	14	74LS00
91	7	14	75159
92	3,6,8	11	LM319
93	3,6,8	11	LM319
94	8	16	DS8BLS120N
95	5	1	DS3691
96	1,2,2	2	TMM164EK-12

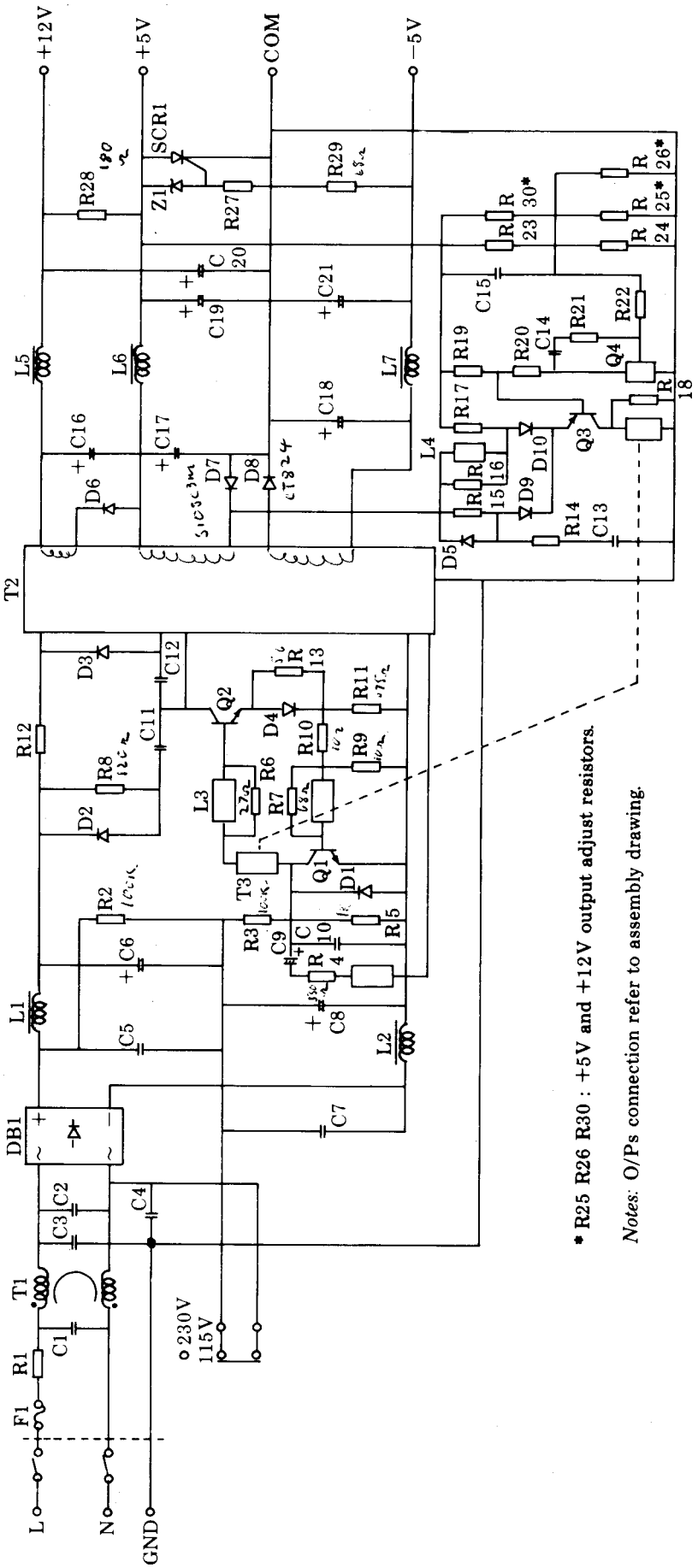


NOTE:-ITEM161-FIT EITHER 8x4164-12 OR 1xTM4164EK8—12 (64K x 8 SIP, 120nS)
(64K x1, 120nS)

PCB layout



Keyboard circuit diagram



Power supply circuit diagram