GW1NZ series of FPGA Products

Package & Pinout User Guide

UG843-1.8.3E,02/02/2024

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Revision History

Date	Version	Description
10/24/2018	1.0E	Initial version published.
01/10/2019	1.1E	Introduction to the I/O BANK updated.
04/03/2019	1.2E	● I/O Bank View updated; ● CS16 package outline updated.
08/23/2019	1.3E	The POD style of CS16 unified.
12/10/2019	1.4E	The QN48 package information added.
07/01/2020	1.5E	The FN32F package information added.
12/18/2020	1.6E	The new device of GW1NZ-2 added.
01/20/2021	1.6.1E	The GW1NZ-2 QN48 and QN48M added.
02/26/2021	1.7E	GW1NZ-2 removed.
11/25/2021	1.7.1E	The QN48 package information updated.
08/18/2023	1.8E	● The units in the package diagrams standardized in millimeters. ● The info. of QN48 and CS100H packages for GW1NZ-2 devices added. ● The recommended PCB layout in chapter 4 “Package Diagrams” added.
09/12/2023	1.8.1E	The info. of FN24 and CG25 packages for GW1NZ-1 devices added.
11/30/2023	1.8.2E	● The info. of CS42 package for GW1NZ-2 devices added. ● The pin quantity of CS100H package in “Table 2-4 Quantity of GW1NZ-2 Pins” updated.
02/02/2024	1.8.3E	● The description of “2.5 Introduction to the I/O BANK” optimized. ● The info. of pitch and size for CS42 package in “Table 2-1 Package and Max. User I/O Information” added. ● The package outline and recommended PCB layout of CS42 package for GW1NZ-2 devices added.

Contents

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1 About This Guide

1.1 Purpose

This manual contains an introduction to the GW1NZ series of FPGA products together with a definition of the pins, list of pin numbers, distribution of pins, and package diagrams.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- DS841, GW1NZ series of FPGA Products Data Sheet
- UG290, Gowin FPGA Products Programming and Configuration User Guide
- UG843, GW1NZ series of FPGA Products Package and Pinout
- UG842, GW1NZ-1 Pinout
- UG847, GW1NZ-2 Pinout

1.3 Abbreviations and Terminology

The abbreviations and terminology used in this manual are as shown in Table 1-1 below.

Table 1-1 Abbreviations and Terminology

Abbreviations and Terminology	Meaning
CG	WLCSP Package
CS	WLCSP Package
FN	QFN Package
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable IO
QN	QFN Package

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

The GW1NZ series of FPGA products are the first generation products in the LittleBee® family. They offer ultra-low power consumption, instant on, low cost, non-volatile, high security, various packages, and flexible usage. They can be widely used in industry control, communication, consumer, video control, etc.

GOWINSEMI provides a new generation of FPGA hardware development environment through market-oriented independent research and development that supports the GW1NZ series of FPGA products and applies to FPGA synthesizing, layout, place and routing, data bitstream generation and download, etc.

2.1 PB-Free Package

The GW1NZ series of FPGA products are PB free in line with the EU ROHS environmental directives. The substances used in the GW1NZ series of FPGA products are in full compliance with the IPC-1752 standards.

2.2 Package and Max. User I/O Information

Table 2-1 Package and Max. User I/O Information

Package	Pitch (mm)	Size (mm)	GW1NZ-1	GW1NZ-2
CG25	0.35	1.8 x 1.8	20	-
CS100H	0.4	4 x 4	-	79 (21)
CS16	0.4	1.8 x 1.8	11	-
CS42	0.4	2.4 x 2.9	-	35 (11)
FN24	0.4	3 x 3	18	-
FN32	0.4	4 x 4	25	-
FN32F	0.4	4 x 4	25	-
QN48	0.4	6 x 6	41	41 (12)

Note!

- In this manual, abbreviations are employed to refer to the package types. See 1.3

Abbreviations and Terminology.

- The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. When mode [2:0] = 001, JTAGSEL_N and the four JTAG pins (TCK, TDI, TDO, and TMS) can be used as GPIO simultaneously.

2.3 Power Pin

Table 2-2 GW1NZ Power Pin

VCC	VCCIO0	VCCIO1	VCCIO2
VCCIO3	VCCIO4	VCCIO5	VCCX
VCCPLL	VCCM	VCCD	VCCIOD

2.4 Pin Quantity

2.4.1 Quantity of GW1NZ-1 Pins

Table 2-3 Quantity of GW1NZ-1 Pins

Pin Type		GW1NZ-1					
		CS16	CG25	FN24	FN32	FN32F	QN48
Single-ended IO/Differential Pair/LVD[1]	BANK0	7/2	8/2	6/1	12/5	12/5	17/8
	BANK1	4/0	12/6	12/6	13/5	13/5	23/11
Max. User I/O[2]		11	20	18	25	25	41
Differential Pair		2	8	7	10	10	19
VCC		1	1	1	1	1	2
VCCX		1	1	1	1	1	1
VCCIO0		1	1	1	1	1	1
VCCIO1		1	1	1	1	1	1
VSS		1	1	2	2	2	2
MODE0		1	1	1	0	0	1
MODE1		0	0	0	0	0	1
MODE2		0	1	1	0	0	0
JTAGSEL_N		0	0	0	1	1	1

Note!

- [1] The number of single-ended/ Differential I/O pins includes CLK pins and download pins.
- [2] The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. When mode [2:0] = 001, JTAGSEL_N and the four JTAG pins (TCK, TDI, TDO, and TMS) can be used as GPIO simultaneously.

2.4.2 Quantity of GW1NZ-2 Pins

Table 2-4 Quantity of GW1NZ-2 Pins

Pin Type		GW1NZ-2		
		CS100H	QN48	CS42
Single-ended IO/Differential Pair/LVDS[1]	BANK0	23/9/4	10/4/1	10/4/2
	BANK1	17/8/7	10/5/5	0/0/0
	BANK2	23/11/7	8/4/1	14/7/4
	BANK3	4/1/0	4/2/2	4/2/2
	BANK4	6/3/1	2/1/1	2/1/1
	BANK5	5/2/2	6/3/2	4/2/2
Max. User I/O[2]		79	41	35
Differential Pair		34	19	16
VCC		0	0	1
VCC/VCCPLL		1	1	0
VCCX		1	0	1
VCCIO0		1	1	1
VCCIO1		1	1	0
VCCIO2		1	0	0
VCCIO3		1	0	0
VCCIO4		1	0	0
VCCIO5		1	0	0
VCCIO1/VCCIO2		0	0	1
VCCIO3/VCCIO4/VCCIO5		0	1	1
VCCX/VCCIO2		0	1	0
VCCD/VCCIOD		1	0	0
VSS		2	2	2
MODE0		1	1	1
MODE1		0	0	0
MODE2		1	0	0
JTAGSEL_N		1	1	1

Note!

- [1] The number of single-ended/Differential I/O pins includes CLK pins and download pins.
- [2] The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. When mode [2:0] = 001, JTAGSEL_N and the four JTAG pins (TCK, TDI, TDO, and TMS) can be used as GPIO simultaneously.

2.5 Introduction to the I/O BANK

GW1NZ-1 includes two I/O banks.

GW1NZ-2 includes six I/O banks.

Please refer to DS841, GW1NZ series of FPGA Products Data Sheet > 2.3 Input/Output Blocks for detailed bank distribution schematic.

This manual provides an overview of the distribution view of the pins in the GW1NZ series of FPGA products. Please refer to 3 View of Pin Distribution for further details. Different IO Banks in the GW1NZ series of FPGA products are marked with different colors.

User I/O, power, and ground are marked with different symbols and colors. The various symbols and colors used for various pins are defined as follows:

- "  " denotes I/Os in BANK0.
- "  " denotes I/Os in BANK1.
- "  " denotes I/Os in BANK2.
- "  " denotes I/Os in BANK3.
- "  " denotes I/Os in BANK4.
- "  " denotes I/Os in BANK5.
- "  " denotes I/Os in BANK6 and DIOs in MIPI.
- "  " denotes VCC, VCCX, and VCCIO. The filling color does not change.
- "  " denotes VCC. The filling color does not change.
- "  " denotes NC.

3 View of Pin Distribution

3.1 View of GW1NZ-1 Pin Distribution

3.1.1 View of CS16 Pin distribution

Figure 3-1 View of GW1NZ-1 CS16 Pin Distribution (Top View)

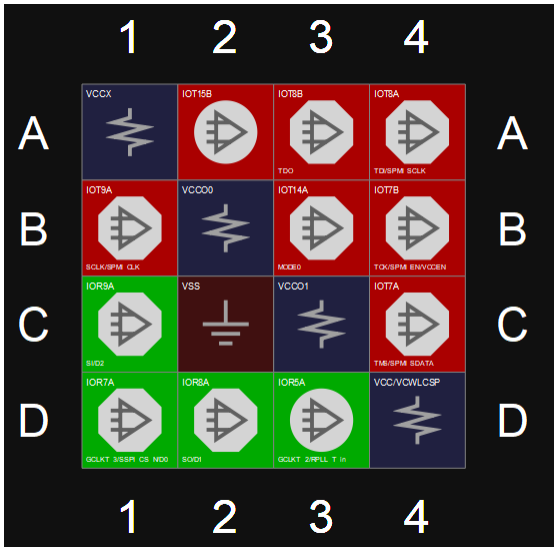


Table 3-1 Other Pins in GW1NZ-1 CS16

VCCIO0	B2
VCCIO1	C3
VCC	D4
VCCX	A1
VSS	C2

3.1.2 View of FN32 Pin Distribution

Figure 3-2 View of GW1NZ-1 FN32 Pin Distribution (Top View)

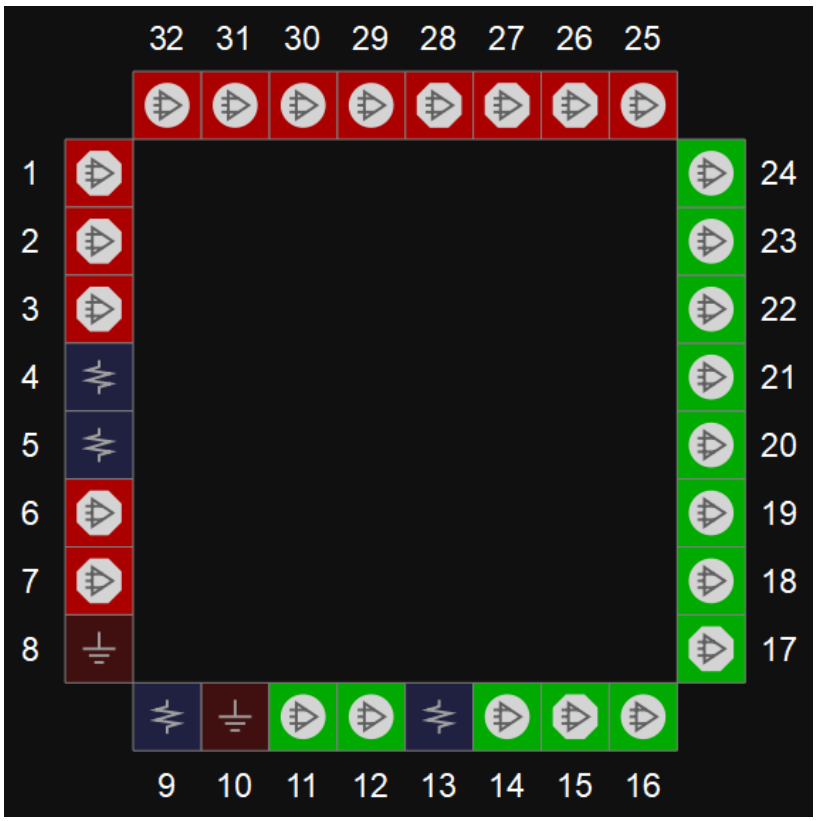


Table 3-2 Other Pins in GW1NZ-1 FN32

VCCIO0	5
VCCIO1	13
VCC	9
VCCX	4
VSS	8, 10

3.1.3 View of FN32F Pin Distribution

Figure 3-3 View of GW1NZ-1 FN32F Pin Distribution (Top View)

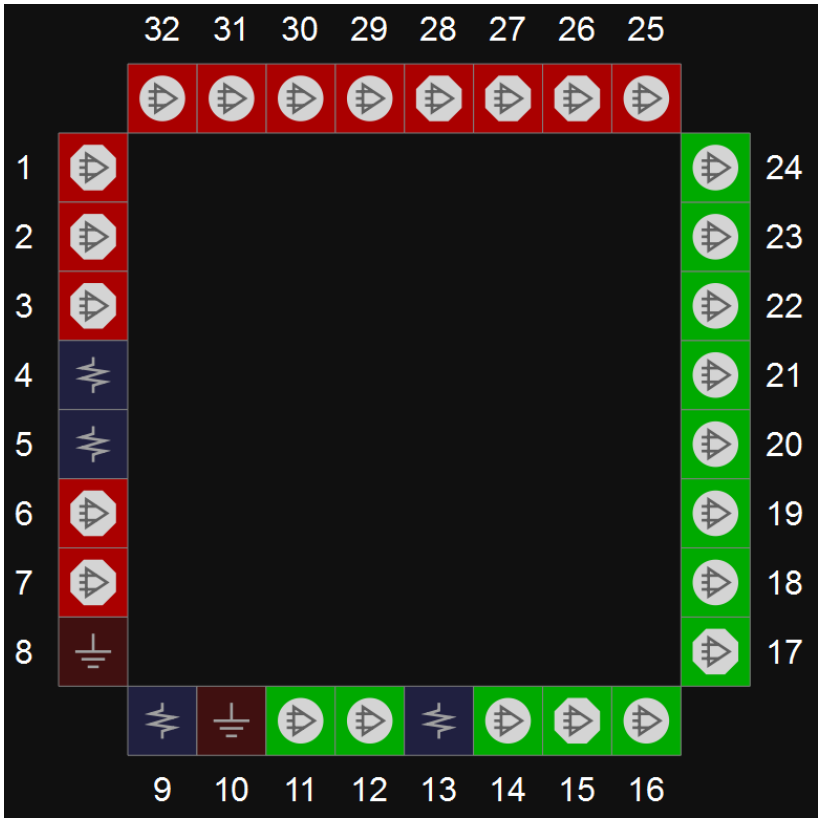


Table 3-3 Other Pins in GW1NZ-1 FN32F

VCCIO0	5
VCCIO1	13
VCC	9
VCCX	4
VSS	8、10

3.1.4 View of QN48 Pin Distribution

Figure 3-4 View of GW1NZ-1 QN48 Pin Distribution (Top View)

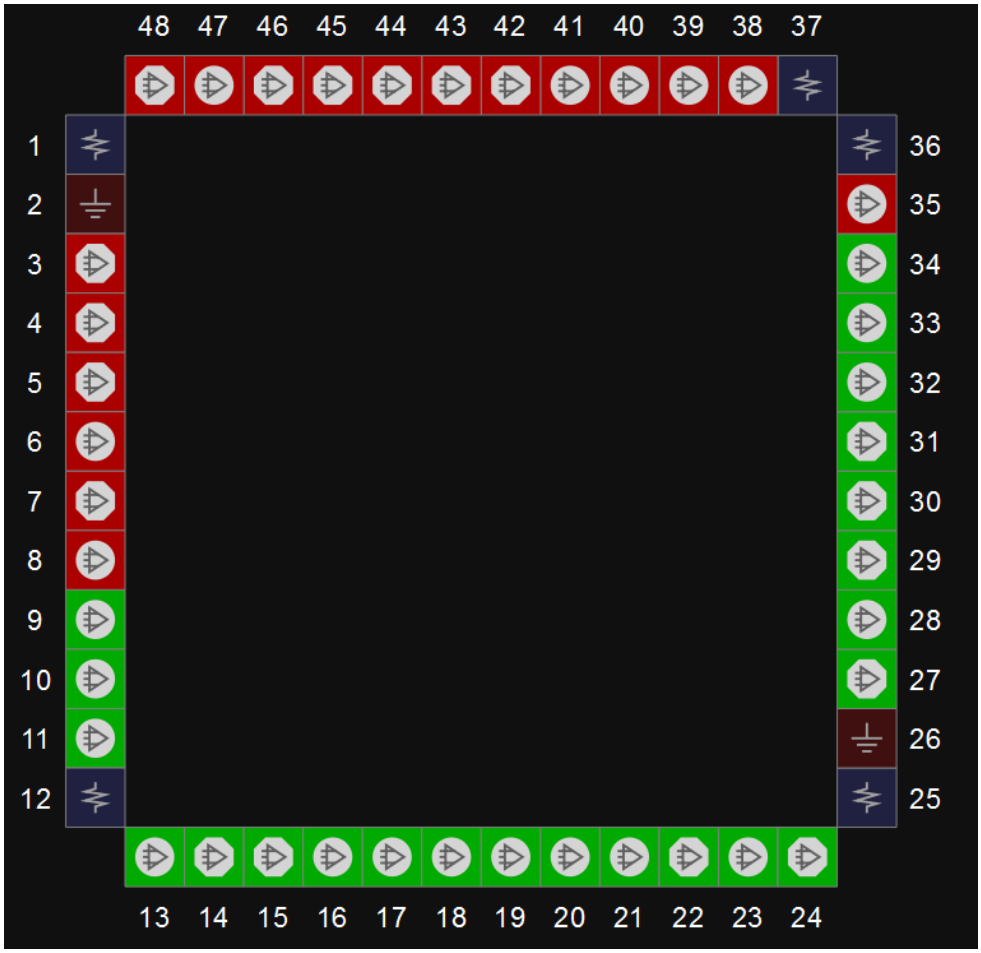


Table 3-4 Other Pins in GW1NZ-1 QN48

VCC	12,37
VCCIO0	1
VCCIO1	25
VCCX	36
VSS	2,26

3.1.5 View of CG25 Pin Distribution

Figure 3-5 View of GW1NZ-1 CG25 Pin Distribution (Top View)

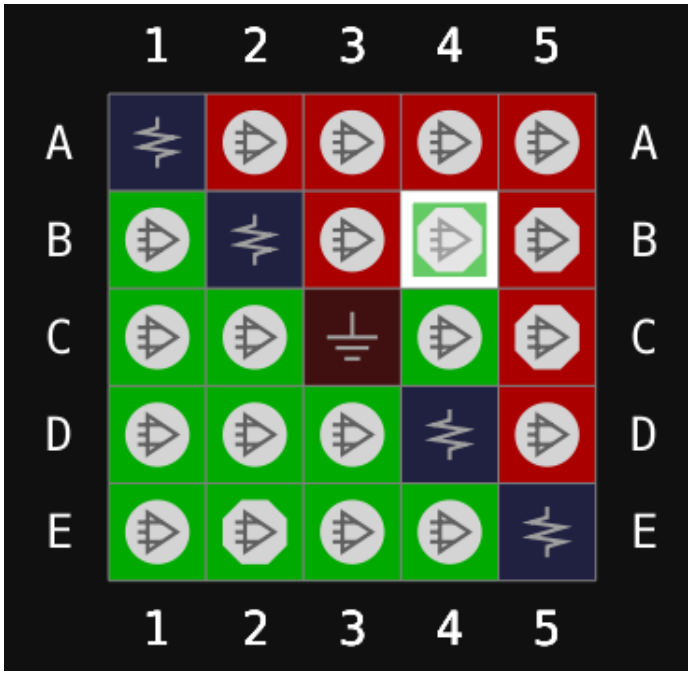


Table 3-5 Other Pins in GW1NZ-1 CG25

VCC	E5
VCCIO0	D4
VCCIO1	B2
VCCX	A1
VSS	C3

3.1.6 View of FN24 Pin Distribution

Figure 3-6 View of GW1NZ-1 FN24 Pin Distribution (Top View)

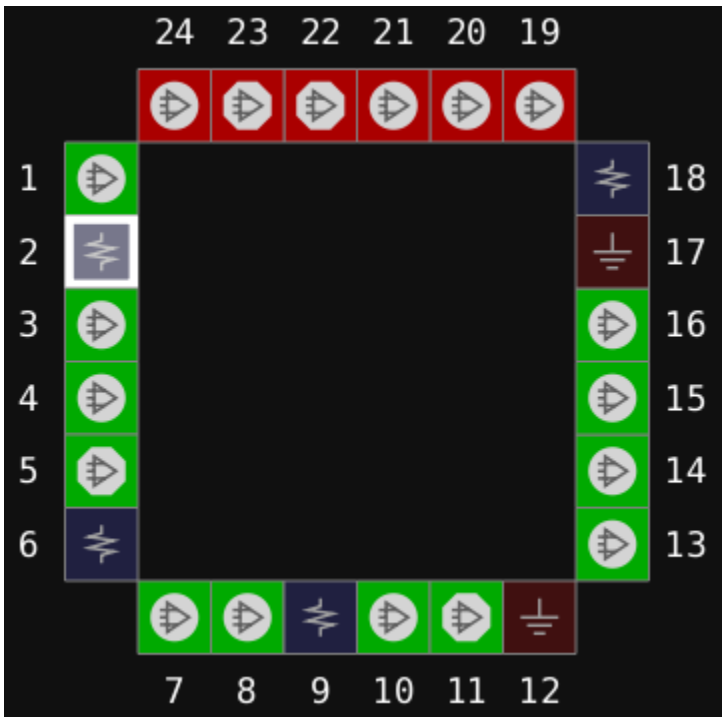


Table 3-6 Other Pins in GW1NZ-1 FN24

VCC	6
VCCIO0	18
VCCIO1	9
VCCX	2
VSS	12,17

3.2 View of GW1NZ-2 Pin Distribution

3.2.1 View of QN48 Pin Distribution

Figure 3-7 View of GW1NZ-2 QN48 Pin Distribution (Top View)

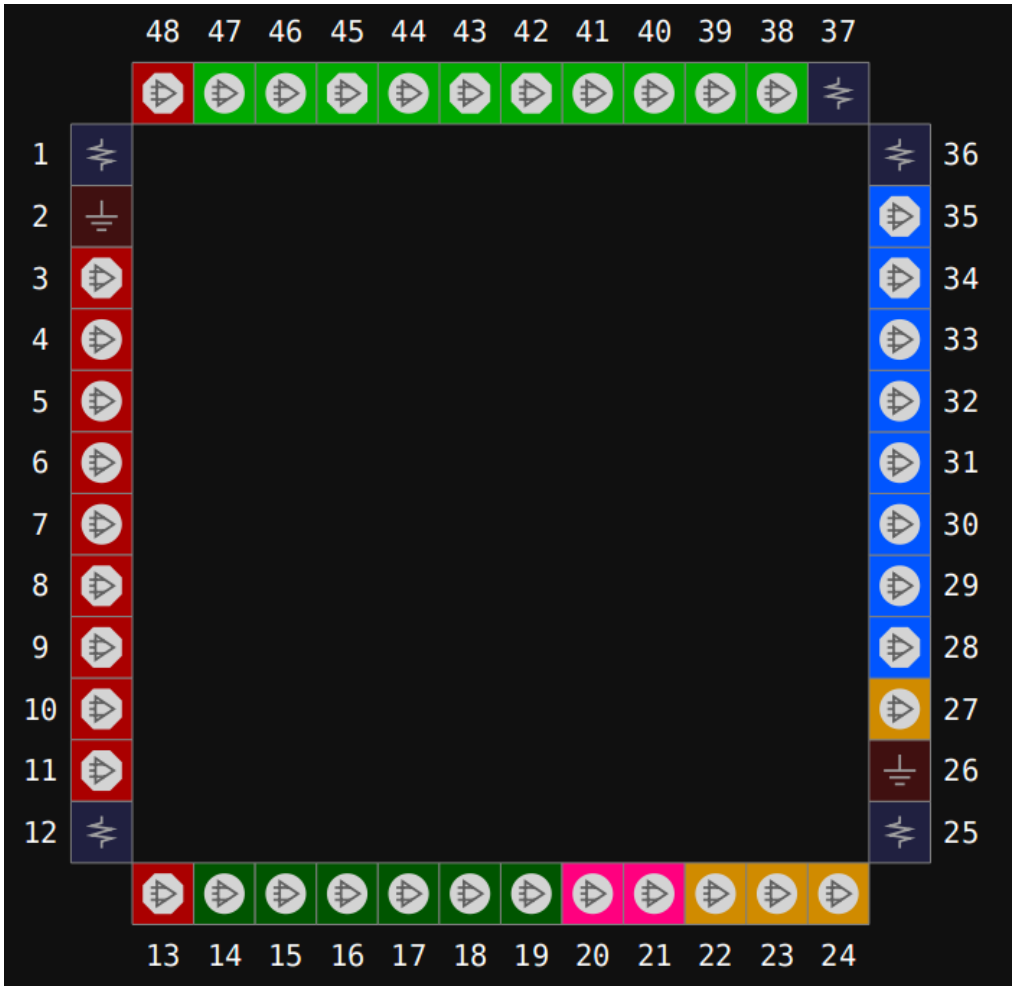


Table 3-7 Other Pins in GW1NZ-2 QN48

VCCIO0	1
VCCIO1	37
VCCIO3/VCCIO4/VCCIO5	25
VCC/VCCPLL	12
VCCX/VCCIO2	36
VSS	26,2

3.2.2 View of CS100H Pin Distribution

Figure 3-8 View of GW1NZ-2 CS100H Pin Distribution (Top View)

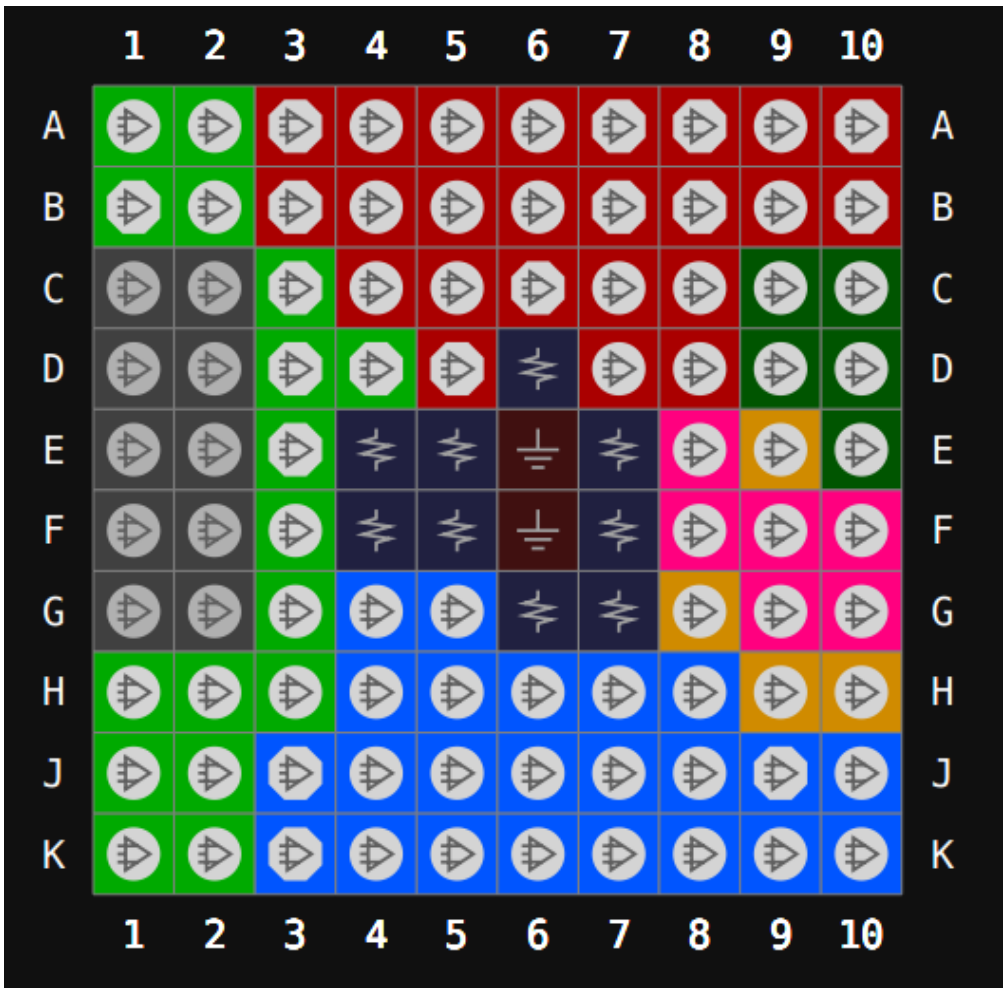


Table 3-8 Other pins in GW1NZ-2 CS100H

VCCIO0	D6
VCCIO1	E4
VCCIO2	G6
VCCIO3	G7
VCCIO4	F7
VCCIO5	E7
VCC/VCCPLL	E5
VCCD/VCCIOD	F4
VCCX	F5
VSS	E6,F6

3.2.3 View of CS42 Pin Distribution

Figure 3-9 View of GW1NZ-2 CS42 Pin Distribution (Top View)

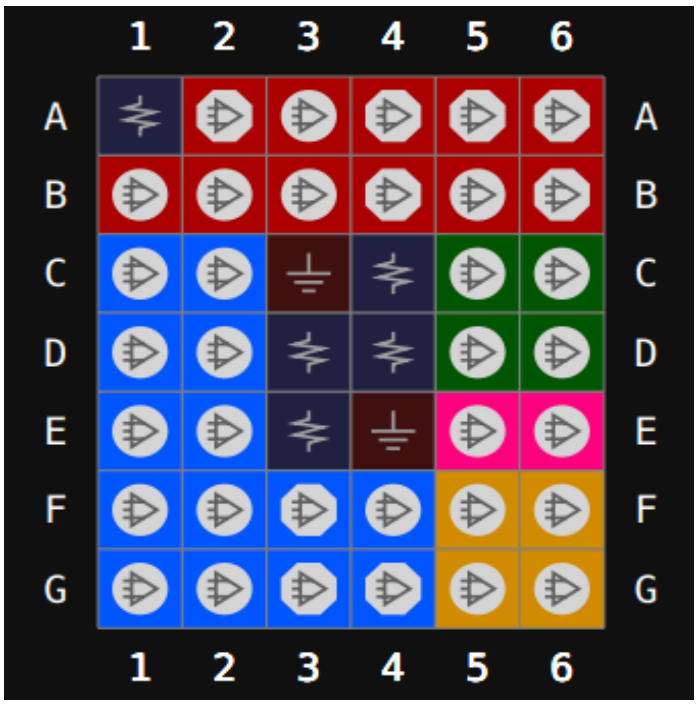


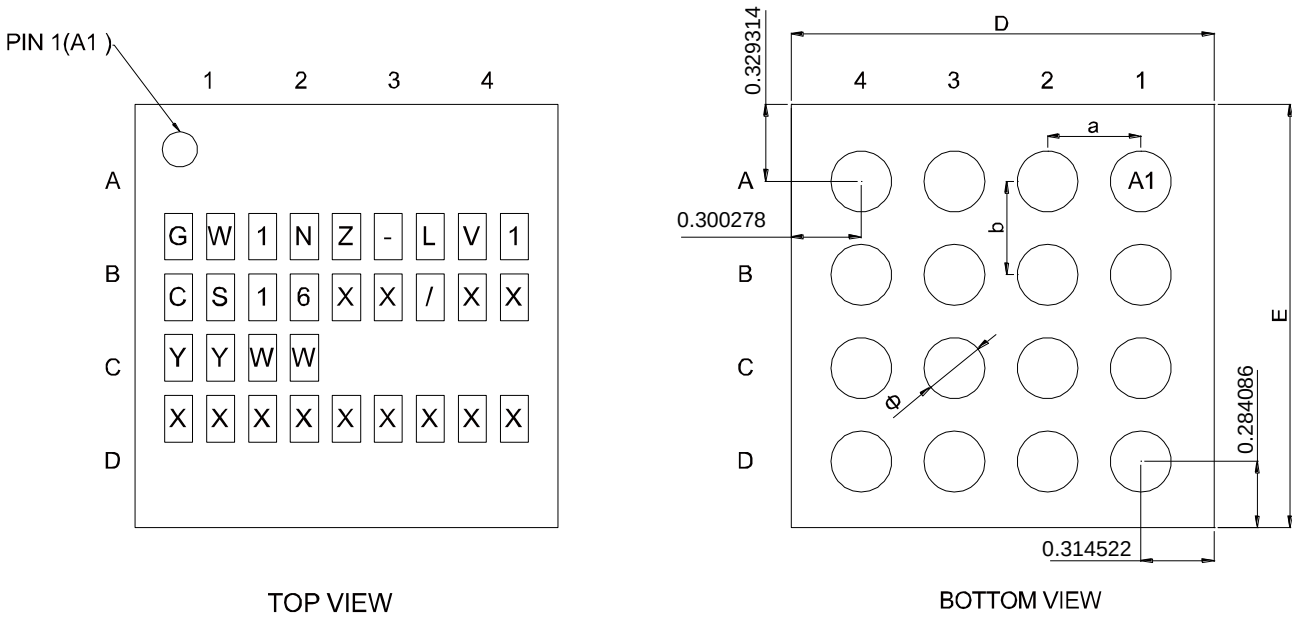
Table 3-9 Other pins in GW1NZ-2 CS100H

VCCIO0	A1
VCCIO1/VCCIO2	D3
VCCIO3/VCCIO4/VCCIO5	C4
VCC	D4
VCCX	E3
VSS	E4,C3

4 Package Diagrams

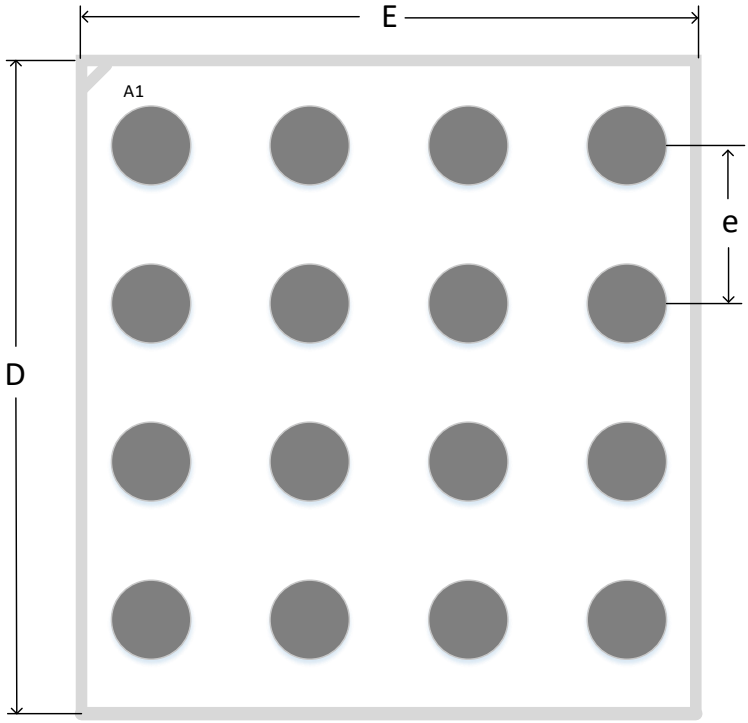
4.1 CS16 Package Outline (1.8mm x 1.8mm)

Figure 4-1 Package Outline CS16

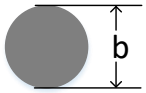


SYMBOL	ITEM	DATA(mm)
D0*E0	PACKAGE SIZE X*Y	1.8148*1.8134±0.025
Φ	BALL DIAMETER	0.26±0.03
a/b	BALL PITCH X/Y	0.4/0.4
N	BALL COUNT	16
H	PACKAGE HEIGHT	0.54±0.05
H1	BALL HEIGHT	0.2±0.025
H2	SI THICKNESS+PI	0.315±0.015
H3	BACK COATING	0.025±0.01

Figure 4-2 Recommended PCB Layout CS16



TOP VIEW

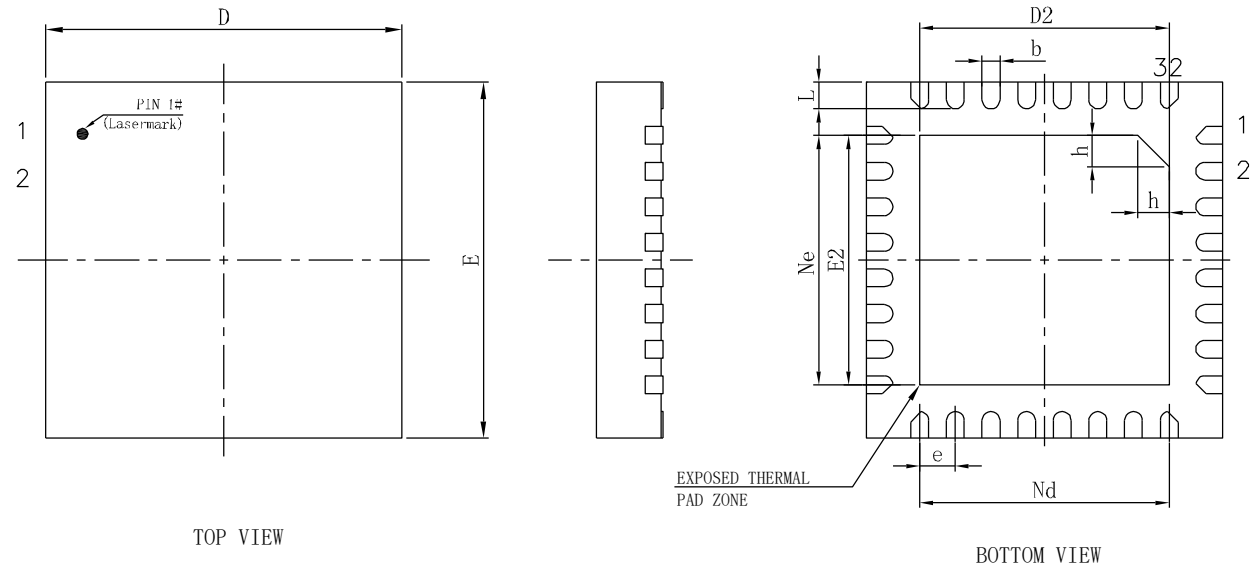


Unit:mm

D	1.81
E	1.82
e	0.40
b	0.20

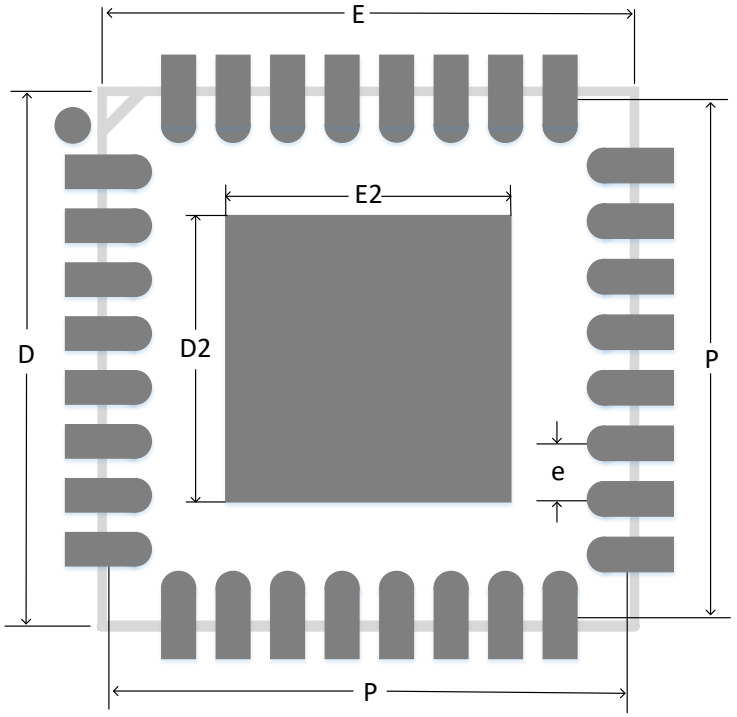
4.2 FN32 Package Outline (4mm x 4mm)

Figure 4-3 Package Outline FN32

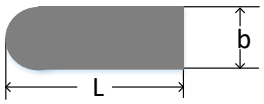


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
e	0.40BSC		
Ne	2.80BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
L	0.25	0.30	0.35
h	0.30	0.35	0.40

Figure 4-4 Recommended PCB Layout FN32



TOP VIEW

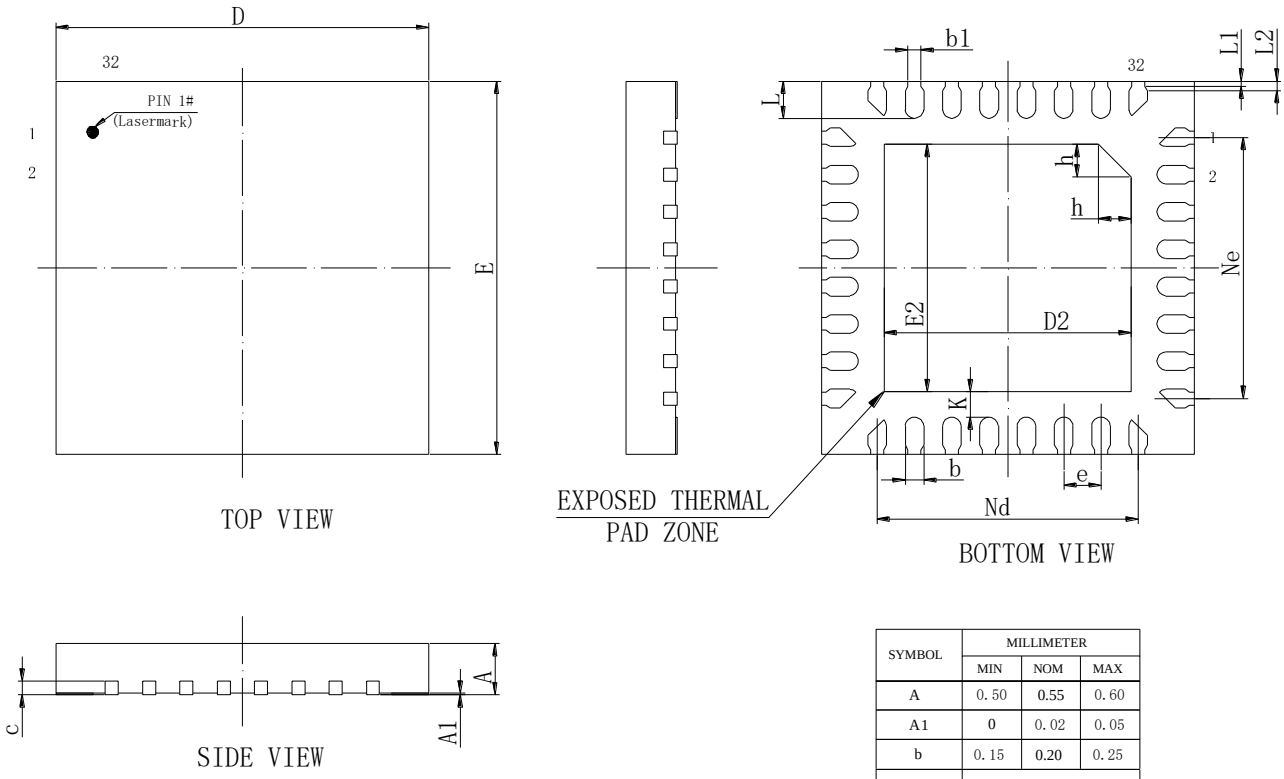


Unit:mm

D	4.00
E	4.00
D2	1.83
E2	1.83
P	4.10
e	0.40
L	0.70
b	0.20

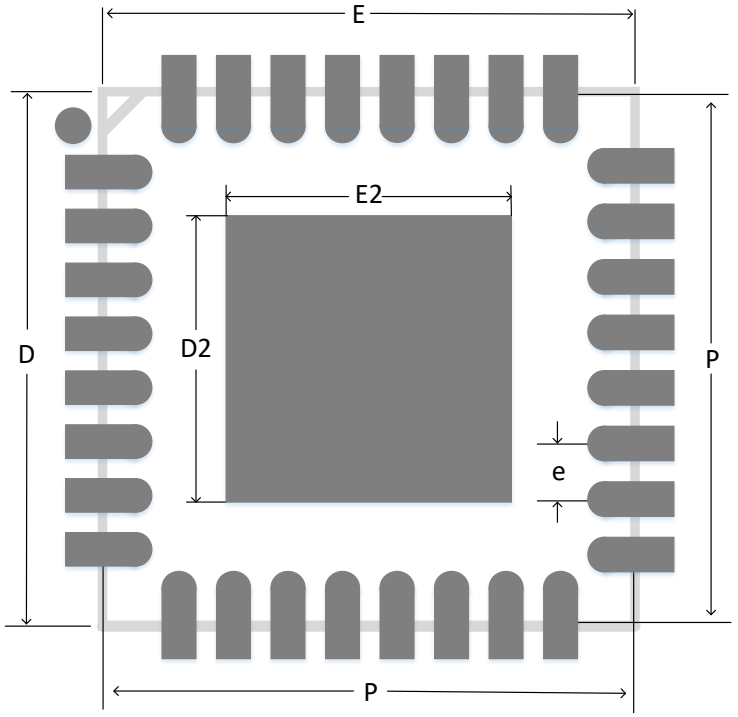
4.3 FN32F Package Outline (4mm x 4mm)

Figure 4-5 Package Outline FN32F



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1	0.14REF		
c	0.10	0.15	0.20
D	3.90	4.00	4.10
D2	2.55	2.65	2.75
e	0.40BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.55	2.65	2.75
Ne	2.80BSC		
L	0.35	0.40	0.45
L1	0	0.05	0.10
L2	0.05	0.10	0.15
h	0.30	0.35	0.40
K	0.20	-	-

Figure 4-6 Recommended PCB Layout FN32F

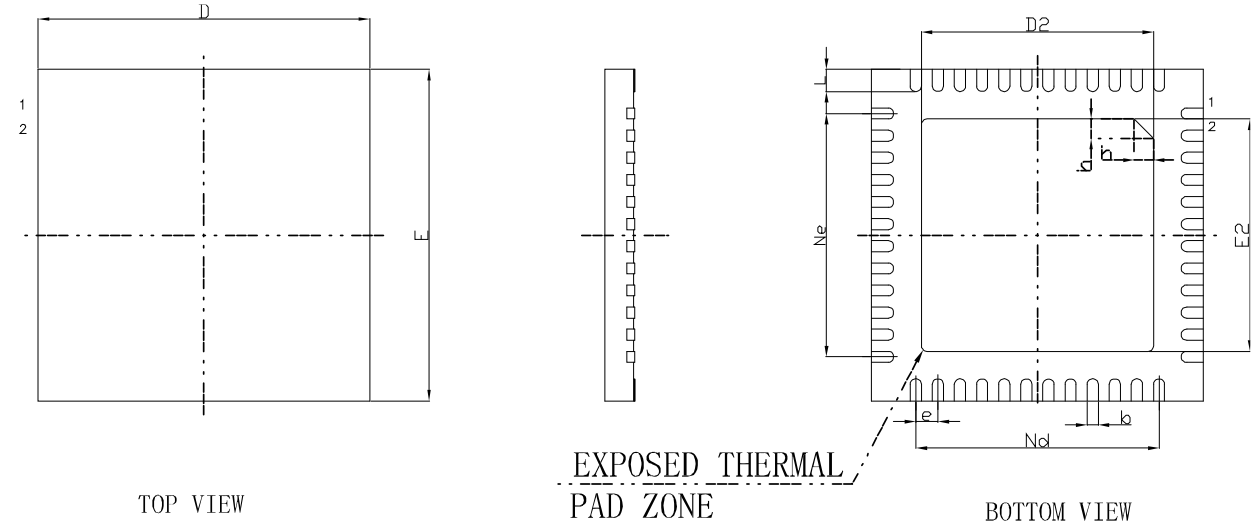


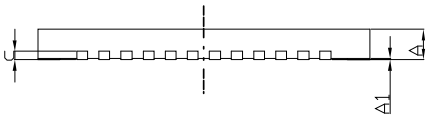
Unit:mm

D	4.00
E	4.00
D2	1.74
E2	1.74
P	4.00
e	0.40
L	0.80
b	0.20

4.4 QN48 Package Outline (6mm x 6mm, GW1NZ-1/2)

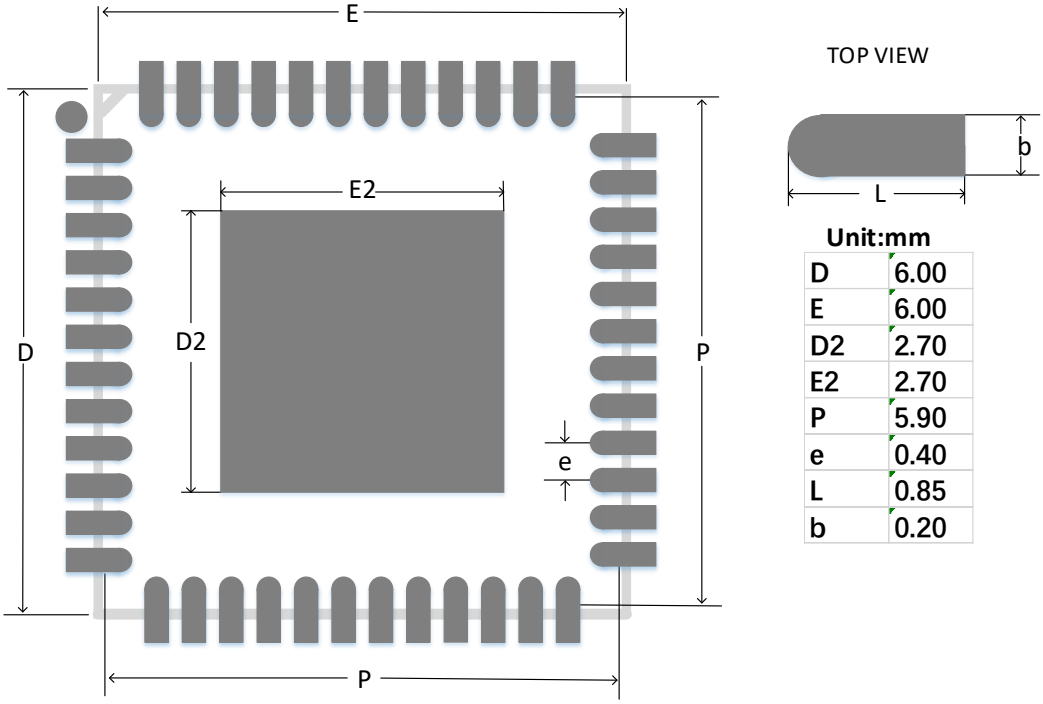
Figure 4-7 Package Outline QN48





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.10	0.15	0.20
D	5.90	6.00	6.10
D2	4.10	4.20	4.30
e	0.40BSC		
Ne	4.40BSC		
Nd	4.40BSC		
E	5.90	6.00	6.10
E2	4.10	4.20	4.30
L	0.35	0.40	0.45
h	0.30	0.35	0.40

Figure 4-8 Recommended PCB Layout QN48

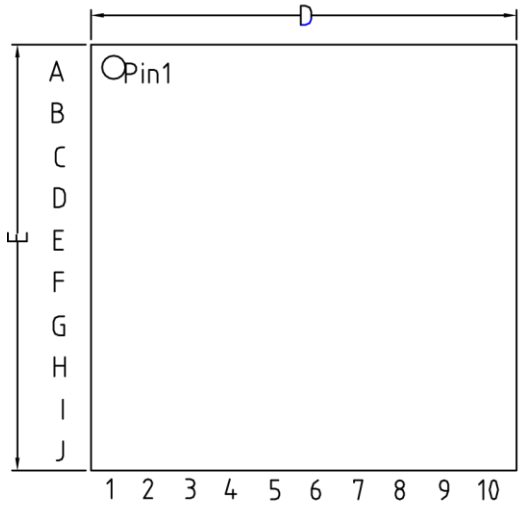


Unit:mm

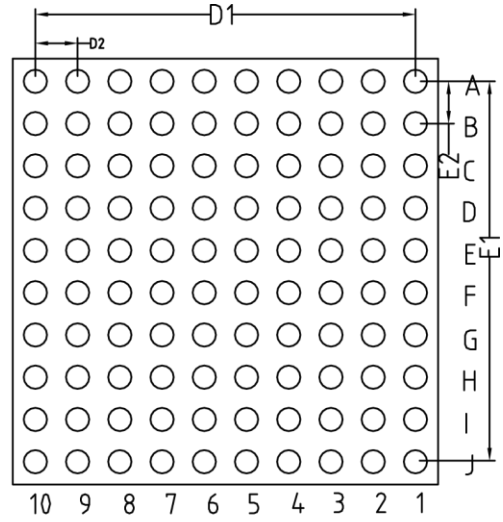
D	6.00
E	6.00
D2	2.70
E2	2.70
P	5.90
e	0.40
L	0.85
b	0.20

4.5 CS100H Package Outline (4mm x 4mm)

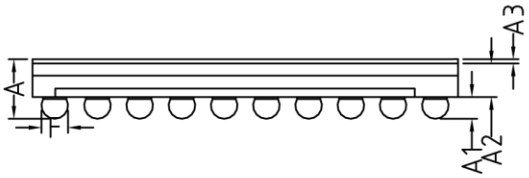
Figure 4-9 Package Outline CS100H



TOP VIEW
Ball Down



BOTTOM VIEW
Ball Up

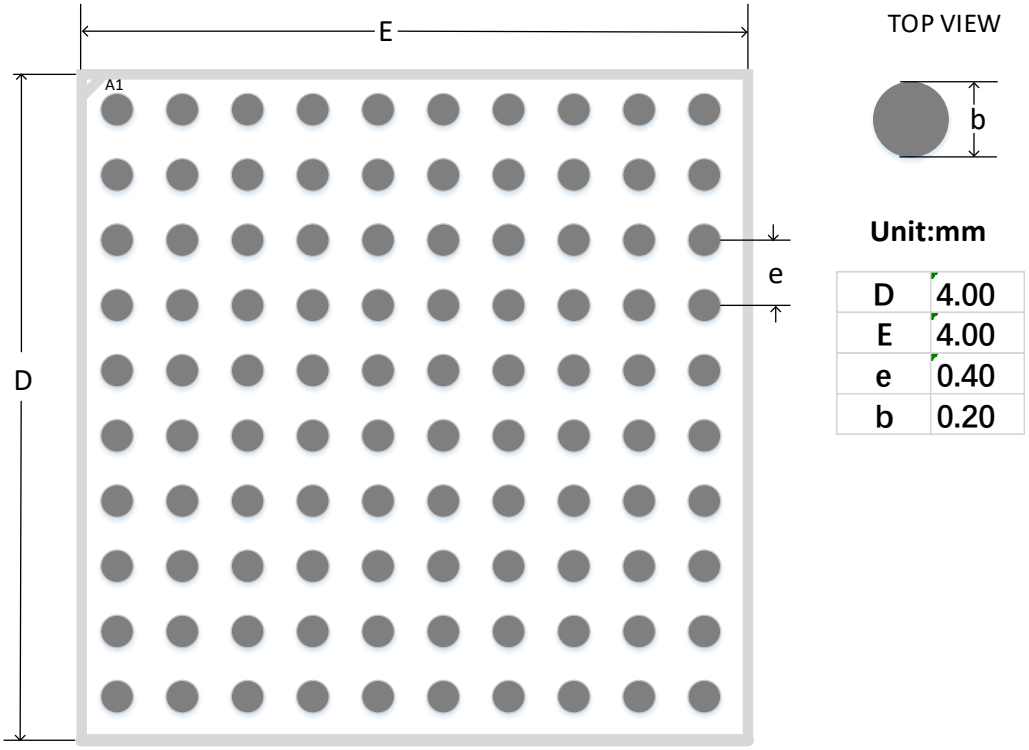


SIDE VIEW

Unit:mm

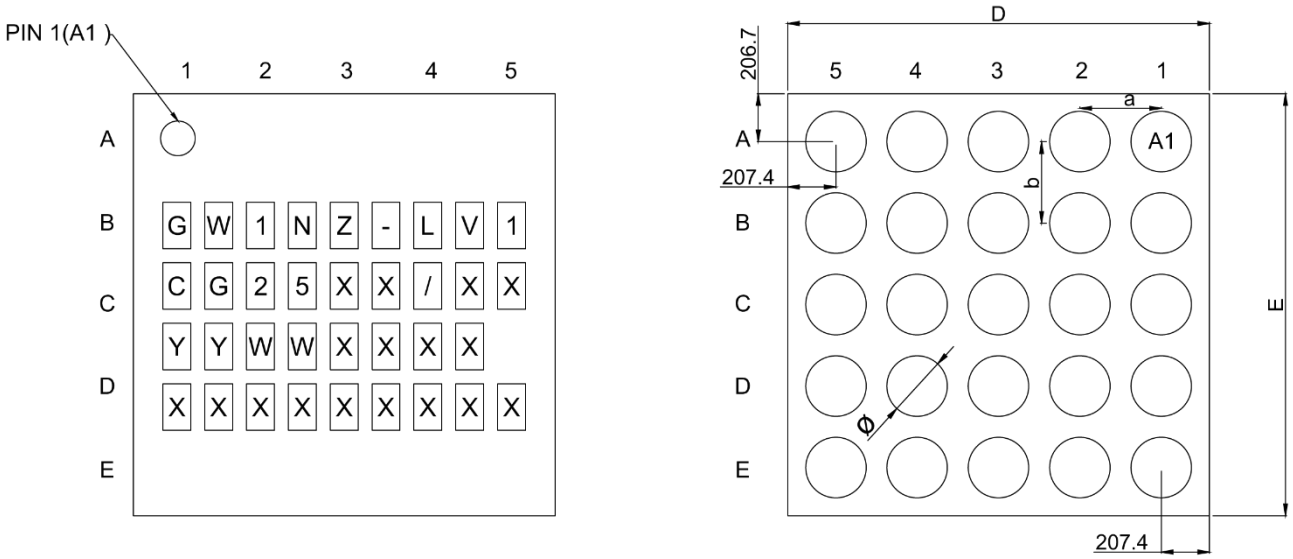
		NO.	Mean	Tolerance
Top Thickness		A	0.54	±0.0405
Ball Height+UBM Thickness		A1	0.2	±0.023
Wafer/Grinding Thickness		A2	0.3	±0.0125
Backside Coating Thickness		A3	0.04	±0.005
Pkg Die Size	X	D	4	±0.025
	Y	E	4	±0.025
Ball Size afer reflow		F	0.262	±0.020
Ball Pitch		D1	3.6	NA
		D2	0.4	NA
		E1	3.6	NA
		E2	0.4	NA

Figure 4-10 Recommended PCB Layout CS100H



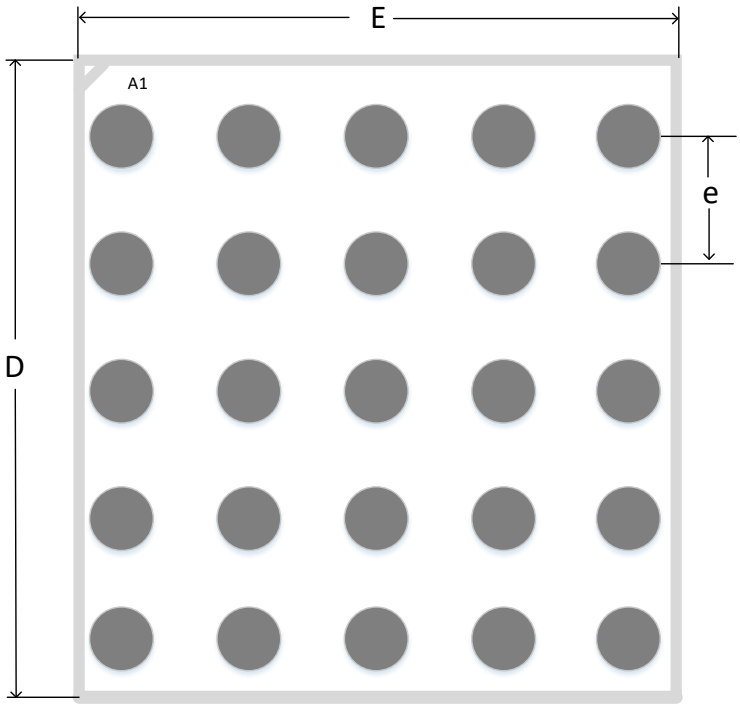
4.6 CG25 Package Outline (1.8mm x 1.8mm)

Figure 4-11 Package Outline CG25



SYMBOL	ITEM	DATA(MM)
D*E	PACKAGE SIZE X*Y	1.8148*1.8134±0.025
Φ	BALL DIAMETER	0.26±0.03
a/b	BALL PITCH X/Y	0.35/0.35
N	BALL COUNT	25
H	PACKAGE HEIGHT	0.54±0.05
H1	BALL HEIGHT	0.2±0.025
H2	SI THICKNESS+PI	0.315±0.015
H3	BACK COATING	0.025±0.01

Figure 4-12 Recommended PCB Layout CG25

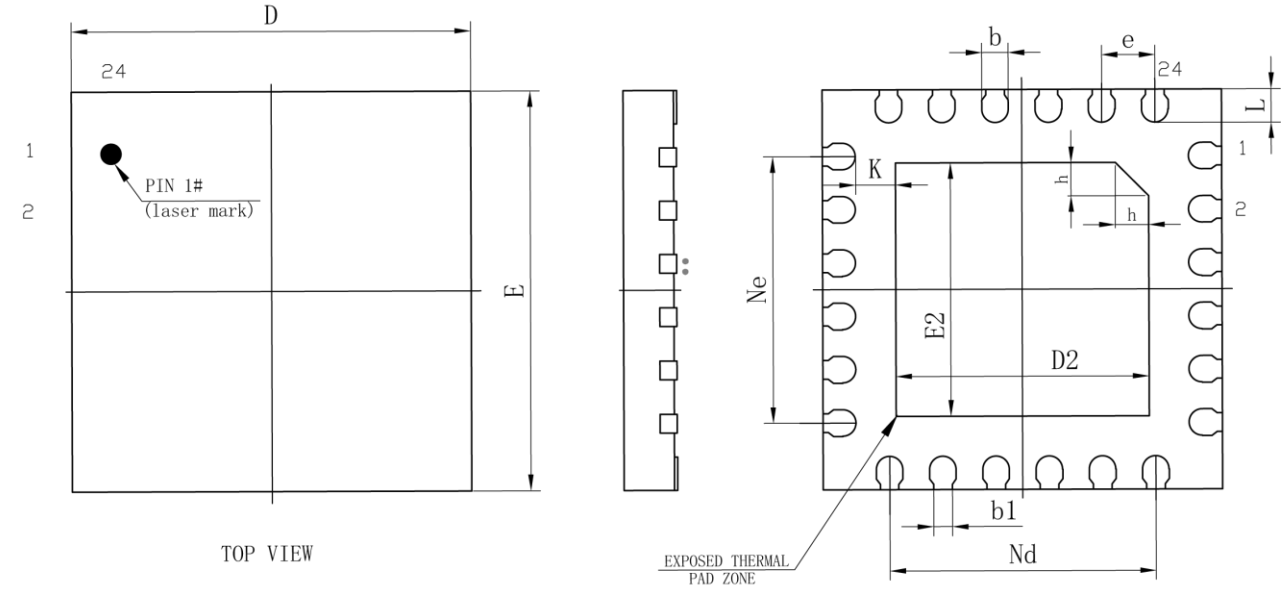


Unit:mm

D	1.815
E	1.815
e	0.35
b	0.15

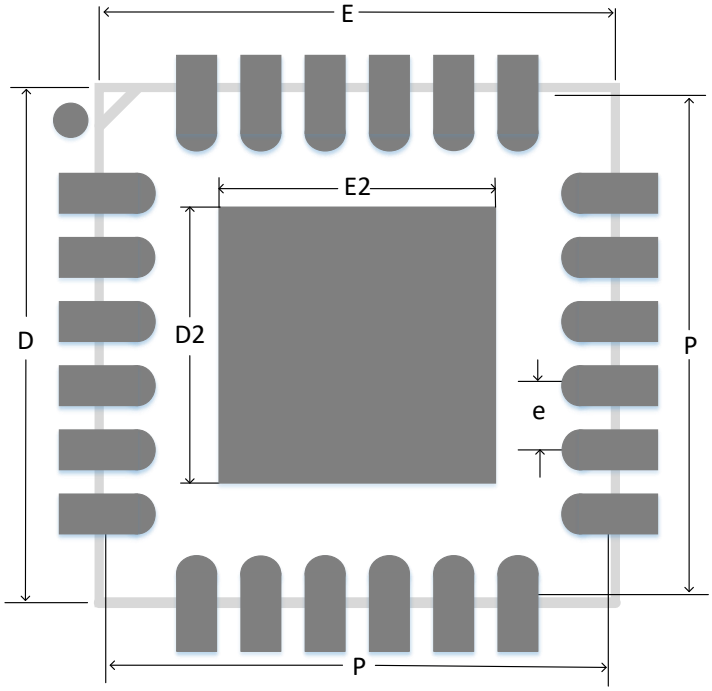
4.7 FN24 Package Outline (3mm x 3mm)

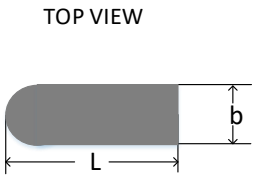
Figure 4-13 Package Outline FN24



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.35	–	0.40
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1	0.14REF		
c	0.127REF		
D	2.90	3.00	3.10
D2	1.80	1.90	2.00
e	0.40BSC		
Ne	2.00BSC		
Nd	2.00BSC		
E	2.90	3.00	3.10
E2	1.80	1.90	2.00
L	0.20	0.25	0.30
h	0.20	0.25	0.30
K	0.25	0.30	0.35

Figure 4-14 Recommended PCB Layout FN24



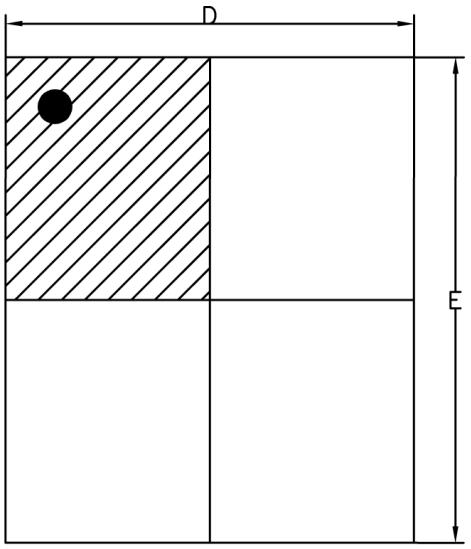


Unit:mm

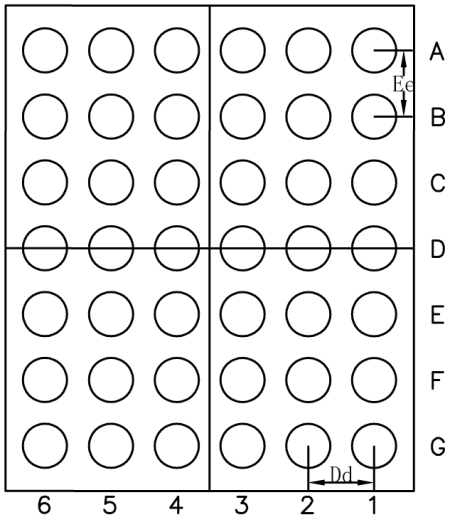
D	3.00
E	3.00
D2	1.30
E2	1.30
P	3.10
e	0.40
L	0.65
b	0.20

4.8 CS42 Package Outline (2.4mm x 2.9mm)

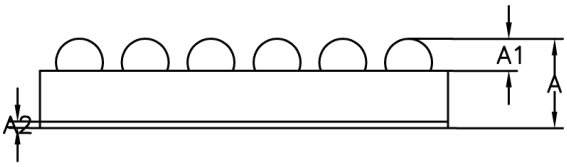
Figure 4-15 Package Outline CS42



Top View



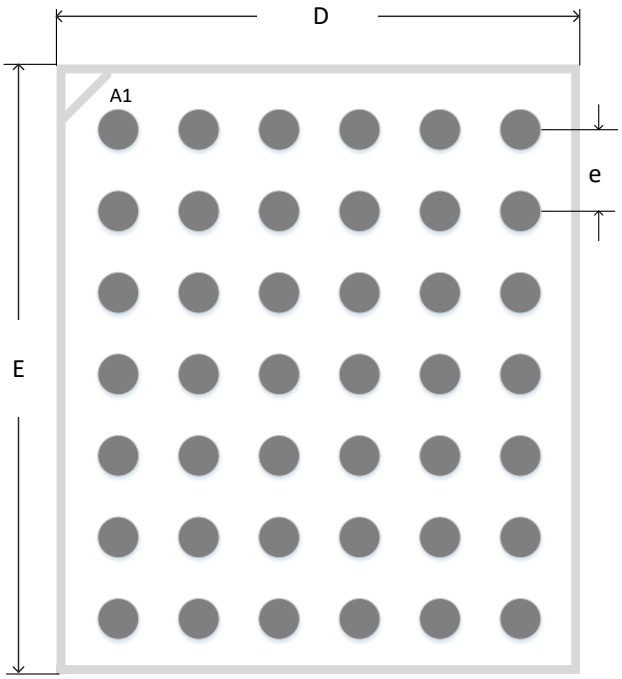
Bottom View



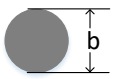
Side View

POD			
参数	尺寸（mm）		
	Min.	Typ.	Max.
D	2.4716	2.4866	2.5016
E	2.936	2.951	2.966
A	0.5095	0.542	0.5745
A1	0.214	0.194	0.174
A2		0.040	
Ee		0.400	
Dd		0.400	

Figure 4-16 Recommended PCB Layout CS42



TOP VIEW



Unit:mm

D	2.49
E	2.95
e	0.40
b	0.27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