GOWIN高云

智慧逻辑 定制未来

GW2AN-18X/9X

Data Sheet

DS971-1.1E, 12/14/2023

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Revision History

Date	Version	Description
09/21/2020	1.0E	Initial version published.
07/16/2021	1.01E	Information on GW2AN-9X optimized.
10/28/2021	1.02E	GW2AN-9X UG256/PG256/UG324 added.
05/25/2022	1.03E	● Recommended I/O operating conditions updated. ● Power supply ramp rates updated.
08/26/2022	1.04E	● The maximum value of the differential input threshold V_{THD} updated. ● Note about DC current limit added. ● 2.9.1 I2C Timing Characteristics added.
09/07/2022	1.05E	● Table 3-3 Power Supply Ramp Rates updated. ● Table 3-8 DC Electrical Characteristics over Recommended Operating Conditions updated. ● Figure 2-1 Architecture Overview updated.
11/11/2022	1.06E	● Table 3-2 Recommended Operating Conditions[1] updated. ● Table 3-5 POR Parameters updated. ● Table 3-8 DC Electrical Characteristics over Recommended Operating Conditions updated. ● Table 3-9 Static Current updated.
02/24/2023	1.07E	● Table 3-1 Absolute Max. Ratings updated. ● Table 3-8 DC Electrical Characteristics over Recommended Operating Conditions updated. ● Description of the on-chip differential termination resistor modified. ● Information on Slew Rate removed.
05/25/2023	1.08E	● Note about the default state of GPIOs modified. ● Information on MIPI IOs added. ● 2.5.2Memory Configuration Modes added.
12/14/2023	1.1E	● Table 1-1 Product Resources updated. ● Note added to Table 3-2 Recommended Operating Conditions[1]. ● Table 3-9 Static Current updated. ● Figure 4-2 Package Marking Examples updated. ● Note about the default state of GPIOs optimized. ● The I/O logic output diagram and the I/O logic input diagram combined into Figure 2-5 I/O Logic Input and Output. ● Note for Table 3-8 DC Electrical Characteristics over Recommended Operating Conditions modified. ● Section 2.4.6 Power up Conditions removed. ● Editorial updates.

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1 General Description

The GW2AN series of FPGA products are the first generation of the Arora family with non-volatile technology, featuring high-speed LVDS interfaces, abundant BSRAM memory resources, and NOR Flash resources. These embedded resources combined with a streamlined FPGA architecture and 55nm process make the GW2AN series of FPGA products an ideal solution for high-speed and low-cost applications.

GOWINSEMI provides a new generation of FPGA hardware development environment that supports FPGA synthesis, placement & routing, bitstream generation and download, etc.

1.1 Features

- Lower power consumption
  - 55nm process
  - LV: Supports 1.0V core voltage
  - EV: Supports 1.2V core voltage
  - UV: Supports 2.5V/3.3V core voltage
  - Supports dynamically turning on/off the clock
- Multiple I/O standards
  - LVCMOS33/25/18/15/12；LVTTL33,SSTL33/25/18 I, II, SSTL15；HSTL18 I, II, HSTL15 I；PCI, LVDS25, RSDS, LVDS25E, BLVDSE, MLVDSE, LVPECLE, RSDSE
  - Input hysteresis options
  - Drive strength options
  - Individual Bus Keeper, Pull-up/Pull-down, and Open Drain options
  - Hot socketing
- GPIOs support MIPI D-PHY RX
  - Bank4/Bank5 of GW2AN-18X/9X support MIPI input by using MIPI IO mode
- Abundant basic logic cells
  - 4-input LUTs (LUT4s)
  - Supports shift registers and shadow SRAMs
- NOR Flash
- Block SRAMs with multiple modes
  - Supports Dual Port mode, Single Port mode, and Semi-Dual Port mode

  - Supports byte-enable
- Flexible PLLs
  - Frequency adjustment (multiplication and division) and phase adjustment
  - Supports global clocks
- Configuration
  - JTAG configuration
  - Five GowinCONFIG configuration modes: AUTO BOOT, SSPI, CPU, I²C, SERIAL
  - Supports I²C/SSPI background upgrade
  - Supports programming the SPI Flash directly in JTAG and SSPI modes; For other modes, you can program the SPI Flash using an IP
  - Supports bitstream file encryption and security bit settings

1.2 Product Resources

Table 1-1 Product Resources

Device	GW2AN-9X	GW2AN-18X
LUT4s	10,368	20,736
Flip-Flops (FFs)	10,368	15,552
Shadow SRAM(SSRAM) Capacity (bits)	40K	40K
Block SRAM(BSRAM) Capacity(bits)	540K	540K
Number of BSRAMs	30	30
NOR Flash(bits)	16M	16M
Maximum PLLs	2	2
Global Clocks	8	8
High-speed Clocks	8	8
LVDS(Mb/s)	1250	1250
MIPI(Mb/s)	1200	1200
I/O Banks	9	9
Maximum GPIOs	389	389
Core Voltage (LV Version)	1.0V	1.0V
Core Voltage (EV Version)	1.2V	1.2V
Core Voltage (UV Version)	2.5V/3.3V	2.5V/3.3V

Table 1-2 GW2AN-18X PLL List

Package	Device	Available PLLs
PG256	GW2AN-18X	PLLL/PLLR
UG256	GW2AN-18X	PLLL/PLLR
UG324	GW2AN-18X	PLLL/PLLR
UG332	GW2AN-18X	PLLL/PLLR
UG400	GW2AN-18X	PLLL/PLLR

Package	Device	Available PLLs
UG484	GW2AN-18X	PLLL/PLLR

Table 1-3 Device-Package Combinations, Maximum User I/Os, and (True LVDS Pairs)

Package	Pitch (mm)	Size (mm)	E-pad Size (mm)	GW2AN-9X	GW2AN-18X
PG256	1.0	17 x 17	–	207(86)	207(86)
PG484	1.0	23 x 23	–	–	381(96)
UG256	0.8	14 x 14	–	207(86)	207(86)
UG324	0.8	15 x 15	–	279(74)	279(74)
UG332	0.8	17 x 17	–	–	279(82)
UG400	0.8	17 x 17	–	335(95)	335(95)
UG484	0.8	19 x 19	–	383(96)	383(96)

Note!

- [1] The package types in this manual are referred to by acronyms, see 4.1 Part Naming for more information.
- JTAGSEL_N and JTAG pins cannot be used as GPIOs simultaneously. The number of maximum user I/Os noted in this table is referred to when the four JTAG pins (TCK, TDI, TDO, and TMS) are used as GPIOs. See *UG973, GW2AN-18X and GW2AN-9X Package and Pinout* for more details.

2 Architecture

2.1 Architecture Overview

Figure 2-1 Architecture Overview

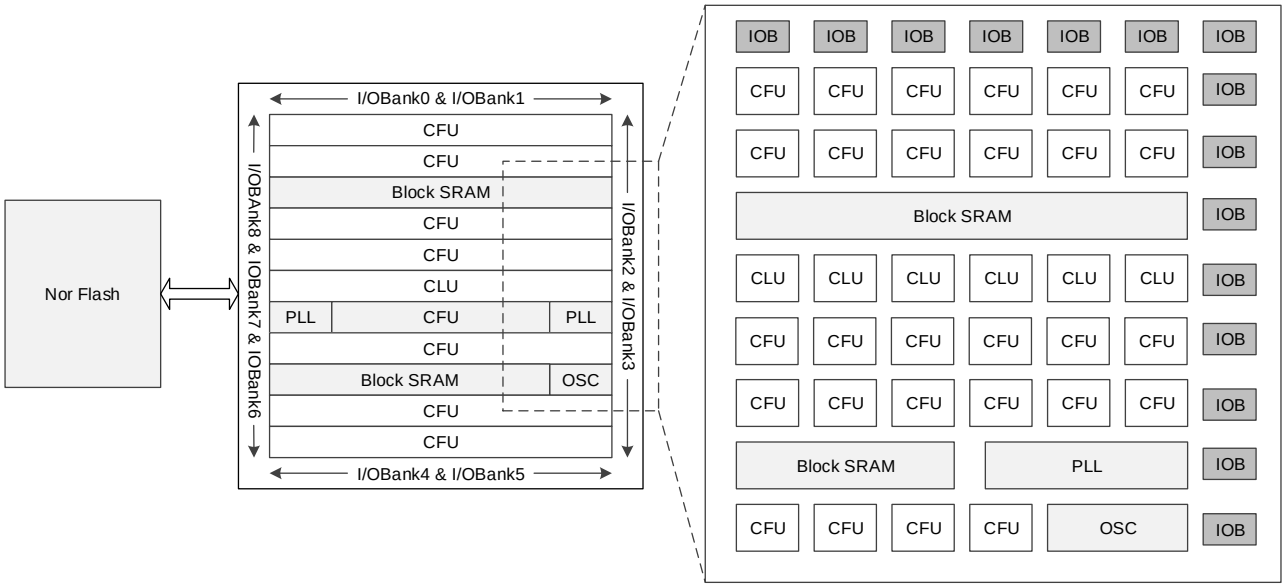


Figure 2-1 shows an overview of the architecture of the GW2AN series of FPGA products integrated with a NOR Flash memory chip. See 2.2 NOR Flash for more information on the NOR Flash.

See Table 1-1 for more information on the resources provided. The core of the FPGA is an array of logic cells surrounded by IO blocks. Besides, BSRAMs, PLLs, and an on-chip oscillator are provided.

The Configurable Function Unit (CFU) and the Configurable Logic Unit (CLU) are the two kinds of basic logic blocks that form the core of GW2AN FPGAs. Devices with different capacities have different numbers of rows and columns of CFUs/CLUs. For more information, see 2.3 Configurable Function Units.

The I/O resources in the GW2AN series of FPGA products are arranged around the periphery of the devices in groups referred to as banks, which are divided into nine banks, including Bank0 - Bank8. The

I/O resources support multiple I/O standards and can be used for regular mode, SDR mode, generic DDR mode, and DDR_MEM mode. For more information, see 2.4 Input/Output Blocks.

BSRAMs are embedded as a row in the GW2AN series of FPGA products. Each BSRAM has a capacity of 18Kbits and supports multiple configuration modes and operation modes. For more information, see 2.5 Block SRAM.

PLLs in the GW2AN series of FPGA products can provide synthesizable clock frequencies. Frequency adjustment (multiplication and division), phase adjustment, and duty cycle adjustment can be achieved by configuring the parameters. These FPGAs have an embedded programmable on-chip clock oscillator that supports clock frequencies ranging from 1.5625 MHz to 100MHz, providing clocking resources for the MSPI mode. For more information, see 2.6 Clocks and 2.10 On-chip Oscillator.

There are also abundant Configurable Routing Units (CRUs) that interconnect all the resources within the FPGA. For example, routing resources distributed in CFUs and IOBs interconnect resources in them. Routing resources can be automatically generated by the Gowin software. In addition, the GW2AN series of FPGA products also provide abundant dedicated clock resources, long wires (LWs), global set/reset (GSR) resources, programming options, etc. For more details, see 2.7 Long Wires and 2.8 Global Set/Reset.

2.2 NOR Flash

The NOR Flash integrated into the GW2AN series of FPGA products encompasses the following features:

Features

- 1.65V to 3.465V supply voltage
- 16M bits of storage, 256 bytes per page
- Supports SPI
- Clock frequency: 100 MHz
- Software/Hardware Write Protection:
  - Entire/partial write protection via software settings
  - Top/bottom block protection
- Minimum 100,000 program/erase cycles
- Fast program/erase operations:
  - Page program time: 1ms
  - Sector erase time: 100ms
  - Block erase time: 0.3s/0.5s
  - Chip erase time: 10s

- Data retention: 20 years

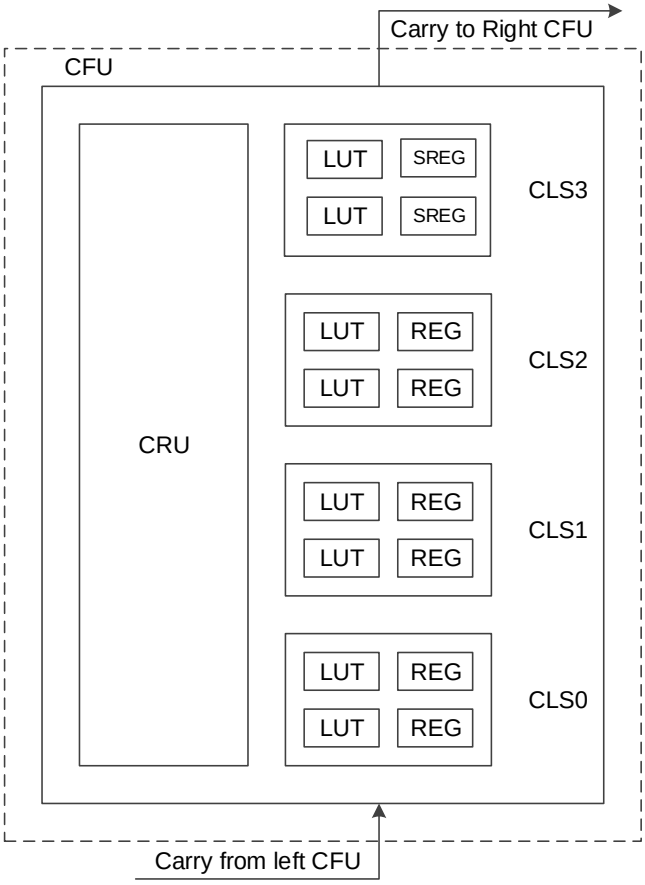
2.3 Configurable Function Units

Configurable Function Units (CFUs) and/or Configurable Logic Units (CLUs) are the basic cells for the core of GOWINSEMI FPGA Products. Each basic cell consists of four Configurable Logic Sections (CLSs) and their routing resource Configurable Routing Units (CRUs). Each of the three CLSs contains two 4-input LUTs and two registers, and the other one only contains two 4-input LUTs, as shown in Figure 2-2 .

The CLSs in the CLUs cannot be configured as SRAMs, but can be configured as basic LUTs, ALUs, and ROMs. The CLSs in the CFUs can be configured as basic LUTs, ALUs, SRAMs, and ROMs according to application scenarios.

For more information on the CFUs, see *UG288, Gowin Configurable Function Unit (CFU) User Guide*.

Figure 2-2 CFU Structure View



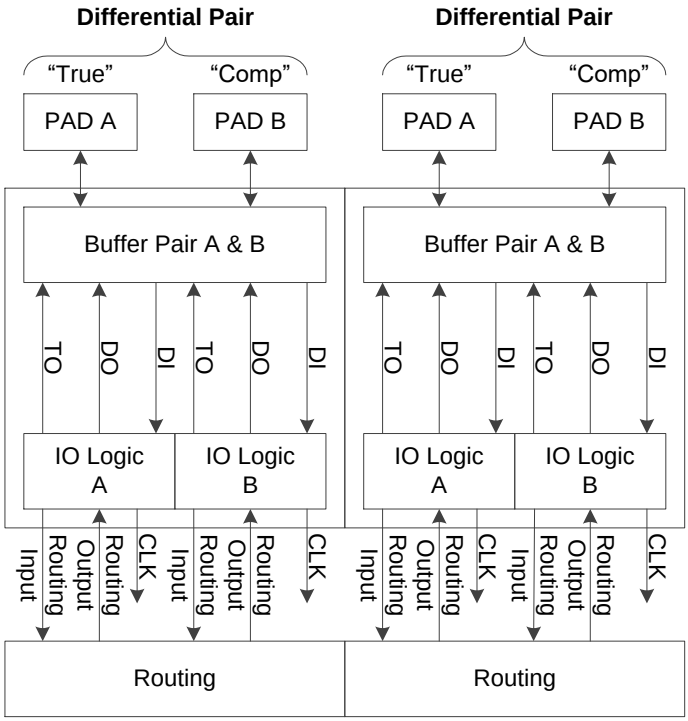
Note!

The SREGs need special patch support. Please contact Gowin's technical support or local office for this patch.

2.4 Input/Output Blocks

The Input/Output Block (IOB) in the GW2AN series of FPGA products consists a buffer pair, IO logic, and corresponding routing units. As shown below, each IOB connects to two pins (marked as A and B), which can be used as a differential pair or as two single-ended inputs/outputs.

Figure 2-3 IOB Structure View



The features of the IOB include:

- V_{CCIO} supplied with Each bank
- LVCMOS, PCI, LVTTL, LVDS, SSTL, HSTL, etc.
- Input hysteresis options
- Drive strength options
- Individual Bus Keeper, Pull-up/Pull-down, and Open Drain options
- Hot socketing
- IO logic supports basic mode, SDR mode, DDR mode, etc.

2.4.1 - 2.4.3 describe I/O standards, I/O logic, and I/O logic modes. For more information about the IOB, please refer to *UG289,Gowin Programmable IO (GPIO) User Guide*.

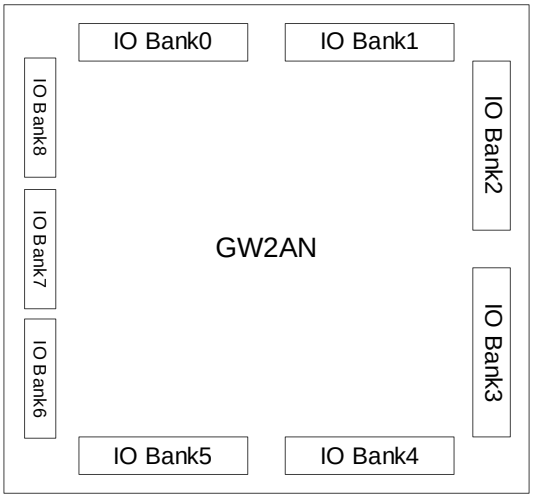
2.4.1 I/O Standards

There are nine I/O banks in the GW2AN series of FPGA products, as shown in Figure 2-4. Each bank has its own I/O power supply V_{CCIO}. V_{CCIO} can be 3.3V, 2.5V, 1.8V, 1.5V, 1.35V, 1.2V, or 1.0V. See Table 3-2 for more information.

To support SSTL, HSTL, etc., Each bank also has one independent voltage source (V_{REF}) as the reference voltage. You can choose to use the internal V_{REF} (0.5 x V_{CCIO}) or the external V_{REF} input via any IO from the

bank.

Figure 2-4 I/O Bank Distribution View of GW2AN



Different banks in the GW2AN series of FPGA Products support different on-die termination settings, including single-ended resistors and differential resistors. Single-ended resistors are set for SSTL/HSTL input/output and are supported in Bank2/3/6/7/8. Differential resistors are set for LVDS input and are only supported in Bank 4/5. For more information, please refer to *UG289, Gowin Programmable IO User Guide*.

Note!

During configuration, all GPIOs of the device are high-impedance with internal weak pull-downs. After the configuration is complete, the I/O states are controlled by user programs and constraints. The states of configuration-related I/Os differ depending on the configuration mode.

The GW2AN series of FPGA products support LV version, EV version, and UV version.

The LV version devices support 1.0V V_{CC}, and the EV version devices support 1.2V V_{CC}, allowing for low power consumption.

V_{CCIO} can be set to 1.0V, 1.2V, 1.5V, 1.8V, 2.5V, or 3.3V as needed.

The UV version devices support 2.5V and 3.3V V_{CC}, and a linear voltage regulator is integrated to facilitate a single power supply.

For the V_{CCIO} requirements of different I/O standards, see Table 2-1 and Table 2-2.

Table 2-1 Output I/O Standards and Configuration Options

I/O standard (output)	Single-ended/Differential	Bank V_{CCIO}(V)	Drive Strength (mA)	Typical Applications
LVTTL33	Single-ended	3.3	4,8,12,16,24	Universal interface
LVCMOS33	Single-ended	3.3	4,8,12,16,24	Universal interface
LVCMOS25	Single-ended	2.5	4,8,12,16	Universal interface
LVCMOS18	Single-ended	1.8	4,8,12	Universal interface
LVCMOS15	Single-ended	1.5	4,8	Universal interface

I/O standard (output)	Single-ended/Differential	Bank V_{CCIO}(V)	Drive Strength (mA)	Typical Applications
LVCMOS12	Single-ended	1.2	4,8	Universal interface
SSTL25_I	Single-ended	2.5	8	Memory interface
SSTL25_II	Single-ended	2.5	8	Memory interface
SSTL33_I	Single-ended	3.3	8	Memory interface
SSTL33_II	Single-ended	3.3	8	Memory interface
SSTL18_I	Single-ended	1.8	8	Memory interface
SSTL18_II	Single-ended	1.8	8	Memory interface
SSTL15	Single-ended	1.5	8	Memory interface
HSTL18_I	Single-ended	1.8	8	Memory interface
HSTL18_II	Single-ended	1.8	8	Memory interface
HSTL15_I	Single-ended	1.5	8	Memory interface
PCI33	Single-ended	3.3	N/A	PC and embedded system
LVPECL33E	Differential	3.3	16	High-speed data transmission
MLVDS25E	Differential	2.5	16	LCD timing driver interface and column driver interface
BLVDS25E	Differential	2.5	16	Multi-point high-speed data transmission
RSDS25E	Differential	2.5	8	High-speed point-to-point data transmission
LVDS25E	Differential	2.5	8	High-speed point-to-point data transmission
LVDS25	Differential(TLVDS)	2.5/3.3	3.5/2.5/2/1.25	High-speed point-to-point data transmission
RSDS	Differential(TLVDS)	2.5/3.3	2	High-speed point-to-point data transmission
MINILVDS	Differential(TLVDS)	2.5/3.3	2	LCD timing driver interface and column driver interface
PPLVDS	Differential(TLVDS)	2.5/3.3	3.5	LCD row/column driver
SSTL15D	Differential	1.5	8	Memory interface
SSTL25D_I	Differential	2.5	8	Memory interface
SSTL25D_II	Differential	2.5	8	Memory interface
SSTL33D_I	Differential	3.3	8	Memory interface
SSTL33D_II	Differential	3.3	8	Memory interface
SSTL18D_I	Differential	1.8	8	Memory interface

I/O standard (output)	Single-ended/Differential	Bank V_{CCIO}(V)	Drive Strength (mA)	Typical Applications
SSTL18D_II	Differential	1.8	8	Memory interface
HSTL18D_I	Differential	1.8	8	Memory interface
HSTL18D_II	Differential	1.8	8	Memory interface
HSTL15D_I	Differential	1.5	8	Memory interface
LVCMOS12D	Differential	1.2	8/4	Universal interface
LVCMOS15D	Differential	1.5	8/4	Universal interface
LVCMOS18D	Differential	1.8	8/12/4	Universal interface
LVCMOS25D	Differential	2.5	8/16/12/4	Universal interface
LVCMOS33D	Differential	3.3	8/24/16/12/4	Universal interface

Table 2-2 Input I/O Standards and Configuration Options Supported by GW2AN

I/O standard (input)	Single-ended/Differential	Bank V_{CCIO}(V)	Supports Hysteresis Options?	Needs V_{REF}?
LVTTL33	Single-ended	1.5/1.8/2.5/3.3	Yes	No
LVCMOS33	Single-ended	1.5/1.8/2.5/3.3	Yes	No
LVCMOS25	Single-ended	1.5/1.8/2.5/3.3	Yes	No
LVCMOS18	Single-ended	1.5/1.8/2.5/3.3	Yes	No
LVCMOS15	Single-ended	1.2/1.5/1.8/2.5/3.3	Yes	No
LVCMOS12	Single-ended	1.2/1.5/1.8/2.5/3.3	Yes	No
SSTL15	Single-ended	1.5/1.8/2.5/3.3	No	Yes
SSTL25_I	Single-ended	2.5/3.3	No	Yes
SSTL25_II	Single-ended	2.5/3.3	No	Yes
SSTL33_I	Single-ended	3.3	No	Yes
SSTL33_II	Single-ended	3.3	No	Yes
SSTL18_I	Single-ended	1.8/2.5/3.3	No	Yes
SSTL18_II	Single-ended	1.8/2.5/3.3	No	Yes
HSTL18_I	Single-ended	1.8/2.5/3.3	No	Yes
HSTL18_II	Single-ended	1.8/2.5/3.3	No	Yes
HSTL15_I	Single-ended	1.5/1.8/2.5/3.3	No	Yes
PCI33	Single-ended	3.3	Yes	No
LVCMOS33OD25	Single-ended	2.5	No	No

I/O standard (input)	Single-ended/Differential	Bank V_{CCIO}(V)	Supports Hysteresis Options?	Needs V_{REF}?
LVCMOS33OD18	Single-ended	1.8	No	No
LVCMOS33OD15	Single-ended	1.5	No	No
LVCMOS25OD18	Single-ended	1.8	No	No
LVCMOS25OD15	Single-ended	1.5	No	No
LVCMOS18OD15	Single-ended	1.5	No	No
LVCMOS15OD12	Single-ended	1.2	No	No
LVCMOS25UD33	Single-ended	3.3	No	No
LVCMOS18UD25	Single-ended	2.5	No	No
LVCMOS18UD33	Single-ended	3.3	No	No
LVCMOS15UD18	Single-ended	1.8	No	No
LVCMOS15UD25	Single-ended	2.5	No	No
LVCMOS15UD33	Single-ended	3.3	No	No
LVCMOS12UD15	Single-ended	1.5	No	No
LVCMOS12UD18	Single-ended	1.8	No	No
LVCMOS12UD25	Single-ended	2.5	No	No
LVCMOS12UD33	Single-ended	3.3	No	No
LVDS25	Differential	2.5/3.3	No	No
RSDS	Differential	2.5/3.3	No	No
MINILVDS	Differential	2.5/3.3	No	No
PPLVDS	Differential	2.5/3.3	No	No
LVDS25E	Differential	2.5/3.3	No	No
MLVDS25E	Differential	2.5/3.3	No	No
BLVDS25E	Differential	2.5/3.3	No	No
RSDS25E	Differential	2.5/3.3	No	No
LVPECL33E	Differential	3.3	No	No
SSTL15D	Differential	1.5/1.8/2.5/3.3	No	No
SSTL25D_I	Differential	2.5/3.3	No	No
SSTL25D_II	Differential	2.5/3.3	No	No
SSTL33D_I	Differential	3.3	No	No
SSTL33D_II	Differential	3.3	No	No
SSTL18D_I	Differential	1.8/2.5/3.3	No	No

I/O standard (input)	Single-ended/Differential	Bank V_{CCIO}(V)	Supports Hysteresis Options?	Needs V_{REF}?
SSTL18D_II	Differential	1.8/2.5/3.3	No	No
HSTL18D_I	Differential	1.8/2.5/3.3	No	No
HSTL18D_II	Differential	1.8/2.5/3.3	No	No
HSTL15D_I	Differential	1.5/1.8/2.5/3.3	No	No
LVCMOS12D	Differential	1.2/1.5/1.8/2.5/3.3	No	No
LVCMOS15D	Differential	1.5/1.8/2.5/3.3	No	No
LVCMOS18D	Differential	1.8/2.5/3.3	No	No
LVCMOS25D	Differential	2.5/3.3	No	No
LVCMOS33D	Differential	3.3	No	No

2.4.2 I/O Logic

Figure 2-5 shows the I/O logic input and output of the GW2AN series of FPGA products.

Figure 2-5 I/O Logic Input and Output

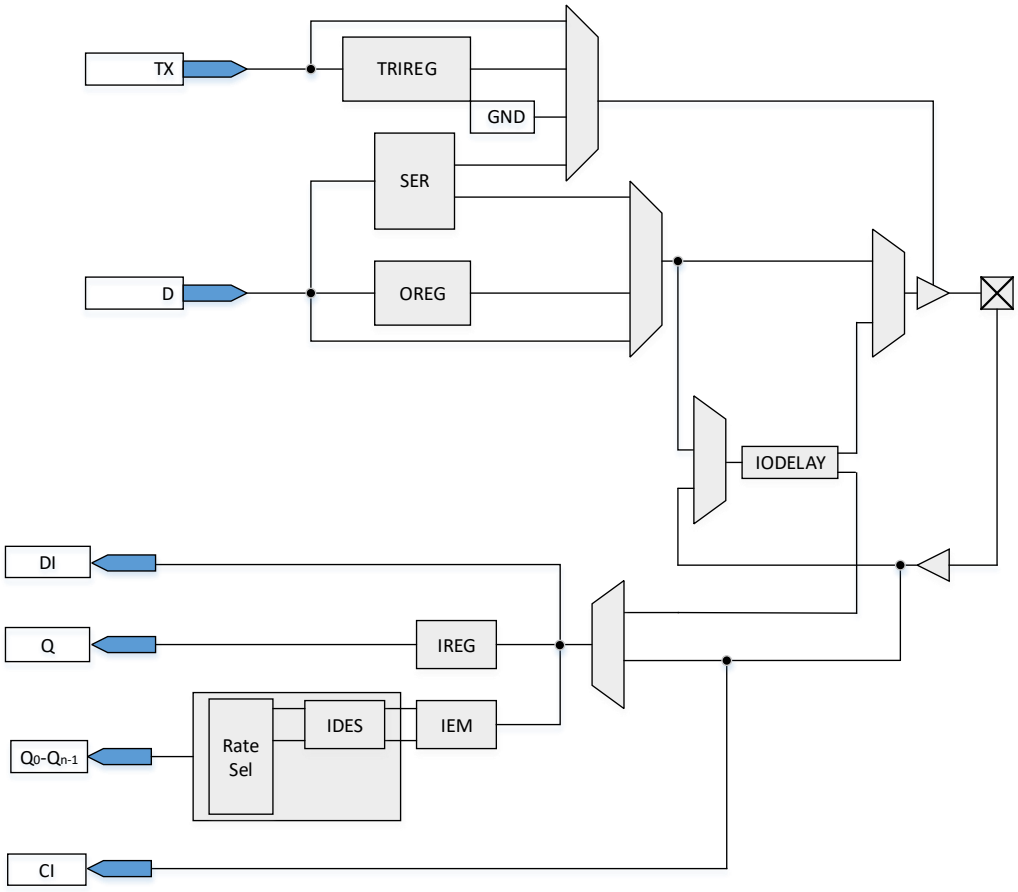


Table 2-3 Port Description

Port	I/O	Description
CI[1]	Input	GCLK input signal. For the number of GCLK input signals, please refer to UG972，GW2AN-18X Pinout and UG978，GW2AN-9X Pinout .
DI	Input	IO port low-speed input signal input into the fabric directly.
Q	Output	IREG output signal in the SDR module.
Q_0-Q_{n-1}	Output	IDES output signal in the DDR module.

Note!

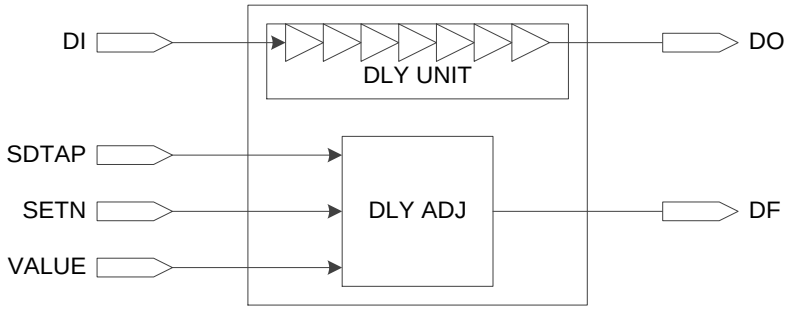
When CI is used as GCLK input, DI, Q, and Q0-Qn-1 cannot be used as I/O input and output.

Descriptions of the I/O logic modules of the GW2AN series of FPGA products are presented below.

IODELAY

See Figure 2-6 for an overview of the IODELAY module. Each I/O of the GW2AN series of FPGA products has an IODELAY module, providing a total of 128(0~127) steps of delay, with one step of delay time being about 18ps.

Figure 2-6 IODELAY Diagram



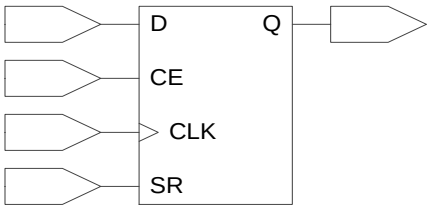
There are two ways to control the delay:

- Static control.
- Dynamic control: can be used with the IEM module to adjust the dynamic sampling window. The IODELAY module cannot be used for both input and output at the same time.

I/O Register

See Figure 2-7 for the I/O register in the GW2AN series of FPGA products. Each I/O provides one input register (IREG), one output register (OREG), and one tristate register (TRIREG).

Figure 2-7 I/O Register Diagram



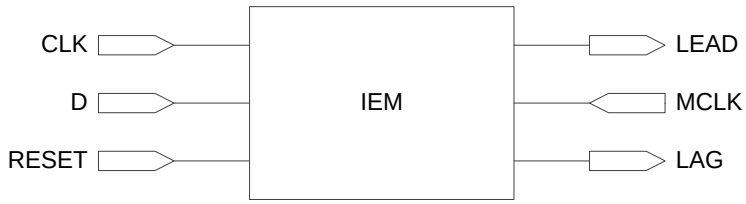
Note!

- CE can be programmed as either active low (0: enable) or active high (1: enable).
- CLK can be programmed as either rising edge triggering or falling edge triggering.
- SR can be programmed as either synchronous/asynchronous SET/RESET or disabled.
- The register can be programmed as a register or a latch.

IEM

The IEM(Input Edge Monitor) module is used to sample data edges and is used in generic DDR mode, as shown in Figure 2-8.

Figure 2-8 IEM Diagram



Deserializer(DES) and Clock Domain Transfer

This series of FPGA products provide a simple deserializer(DES) for input I/O logic to support advanced I/O protocols. The clock domain transfer module of the input clock in DES provides the ability to safely switch the external sampling clock(strobe) domain to the internal continuous running clock domain. There are multiple registers used for data sampling.

The clock domain transfer module offers the following functions:

- The internal continuous clock is used instead of the discontinuous DQS for data sampling. This feature applies to the DDR memory interface.
- For the DDR3 memory interface standard, align the data after read-leveling.
- In generic DDR mode, when DQS.RCLK is used for sampling, the clock domain transfer module is also required.

Each DQS provides WADDR and RADDR signals for the clock domain transfer module in the same group.

SER

This series of FPGA products provide a simple serializer(SER) for output I/O logic to support advanced I/O protocols.

2.4.3 I/O Logic Modes

The I/O Logic of the GW2AN series of FPGA products supports several operation modes. In each operation mode, the I/O (or I/O differential pair) can be configured as output, input, INOUT or tristate output (output signal with tristate control).

2.5 Block SRAM

2.5.1 Introduction

The GW2AN series of FPGA products provide abundant block SRAM resources. These memory resources are distributed as blocks throughout the FPGA array in the form of rows. Therefore, they are called block static random access memories (BSRAMs). The capacity of each BSRAM can be up to 18,432 bits (18K bits). There are five operation modes: Single Port mode, Dual Port mode, Semi-Dual Port mode, ROM mode, and FIFO mode.

The abundant BSRAM resources are available for implementing high-performance designs. The features of BSRAMs include:

- Up to 18,432 bits per BSRAM
- Clock frequency up to 380MHz (230MHz in Read-before-write mode)
- Supports Single Port mode
- Supports Dual Port mode
- Supports Semi-Dual Port mode
- Provides parity bits
- Supports ROM Mode
- Data widths from 1 to 36 bits
- Mixed clock mode
- Mixed data width mode
- Byte Enable function for double-byte and above data
- Normal read and write mode
- Read-before-write mode
- Write-through mode

2.5.2 Memory Configuration Modes

BSRAMs in the GW2AN series of FPGA products support various data widths, see Table 2-4.

Table 2-4 Memory Size Configuration

Single Port Mode	Dual Port Mode	Semi-Dual Port Mode	ROM Mode
16K x 1	16K x 1	16K x 1	16K x 1
8K x 2	8K x 2	8K x 2	8K x 2
4K x 4	4K x 4	4K x 4	4K x 4
2K x 8	2K x 8	2K x 8	2K x 8
1K x 16	1K x 16	1K x 16	1K x 16
512 x 32	-	512 x 32	512 x 32

Single Port Mode	Dual Port Mode	Semi-Dual Port Mode	ROM Mode
2K x 9	2K x 9	2K x 9	2K x 9
1K x 18	1K x 18	1K x 18	1K x 18
512 x 36	-	512 x 36	512 x 36

Single Port Mode

The single port mode supports 2 read modes (bypass mode and pipeline mode) and 3 write modes (normal mode, write-through mode, and read-before-write mode). In single port mode, writing to or reading from one port at one clock edge is supported. During the write operation, the written data will be transferred to the output of the BSRAM. When the output register is bypassed, the new data will show up at the same write clock rising edge.

For more information on single port mode, please refer to *UG285, Gowin BSRAM & SSRAM User Guide*.

Dual Port Mode

The dual port mode supports 2 read modes (Bypass mode and Pipeline mode) and 2 write modes (Normal mode and Write-Through mode). The applicable operations are as follows:

- Two independent read operations
- Two independent write operations
- An independent read operation and an independent write operation

Note!

It is not recommended to perform simultaneous read access from one port and write access from the other port to the same memory address.

For more information on dual port mode, please refer to *UG285, Gowin BSRAM & SSRAM User Guide*.

Semi-Dual Port Mode

The semi-dual port mode supports 2 read modes (bypass mode and pipeline mode) and 1 write mode (normal mode). Semi-dual port mode supports simultaneous read and write operations in the form of writing to port A and reading from port B.

Note!

It is not recommended to perform simultaneous read access from one port and write access from the other port to the same memory address.

For more information on semi-dual port mode, please refer to *UG285, Gowin BSRAM & SSRAM User Guide*.

ROM Mode

BSRAMs can be configured as ROMs. The ROM can be initialized during the device configuration stage, and the ROM data needs to be provided in the initialization file. Initialization is completed during the device power-on process.

Each BSRAM can be configured as one 16Kbits ROM. For more

information on ROM mode, please refer to *UG285, Gowin BSRAM & SSRAM User Guide*.

2.5.3 Mixed Data Width Configuration

The BSRAMs in the GW2AN series of FPGA products support mixed data width operations. In dual port mode and semi-dual port mode, the data widths for read and write can be different, see Table 2-5 and Table 2-6.

Table 2-5 Dual Port Mixed Read/Write Data Width Configuration

Read Port	Write Port						
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	2K x 9	1K x 18
16K x 1	*	*	*	*	*		
8K x 2	*	*	*	*	*		
4K x 4	*	*	*	*	*		
2K x 8	*	*	*	*	*		
1K x 16	*	*	*	*	*		
2K x 9						*	*
1K x 18						*	*

Note!

"*" denotes the modes supported.

Table 2-6Semi-dual Port Mixed Read/Write Data Width Configuration

Read Port	Write Port								
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	512x32	2K x 9	1K x 18	512x36
16K x 1	*	*	*	*	*	*			
8K x 2	*	*	*	*	*	*			
4K x 4	*	*	*	*	*	*			
2K x 8	*	*	*	*	*	*			
1K x 16	*	*	*	*	*	*			
512x32	*	*	*	*	*	*			
2K x 9							*	*	*
1K x 18							*	*	*

Note!

"*" denotes the modes supported.

2.5.4 Byte-enable

BSRAMs support the byte-enable function. For data longer than a byte, the additional bits can be blocked, allowing only the selected portion to be written into the memory. The blocked bits will be retained for future operation. Read/write enable ports (WREA, WREB) and byte-enable parameter options can be used to control the BSRAM write operation.

2.5.5 Parity Bit

There are parity bits in BSRAMs. The 9th bit in each byte can be used as a parity bit to check the correctness of data transmission. It can also be used for data storage.

2.5.6 Synchronous Operation

- All the input registers of BSRAMs support synchronous write.
- The output registers can be used as pipeline registers to improve design performance.
- The output registers are bypass-able.

2.5.7 BSRAM Operation Modes

The BSRAM supports five different operations, including two read modes (Bypass mode and Pipeline mode) and three write modes (Normal mode, Write-Through mode, and Read-before-Write mode).

Read Mode

The following two read modes are supported.

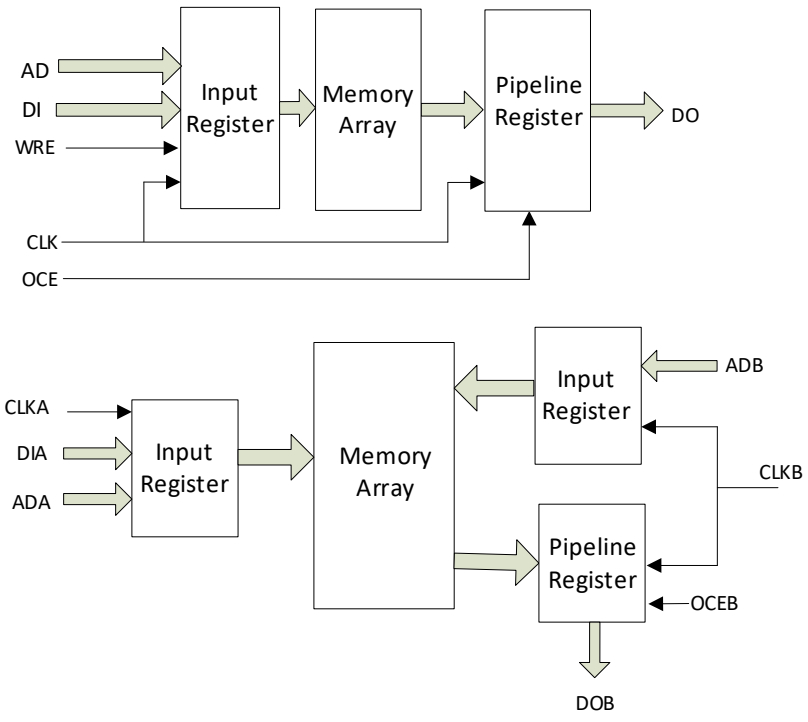
Pipeline Mode

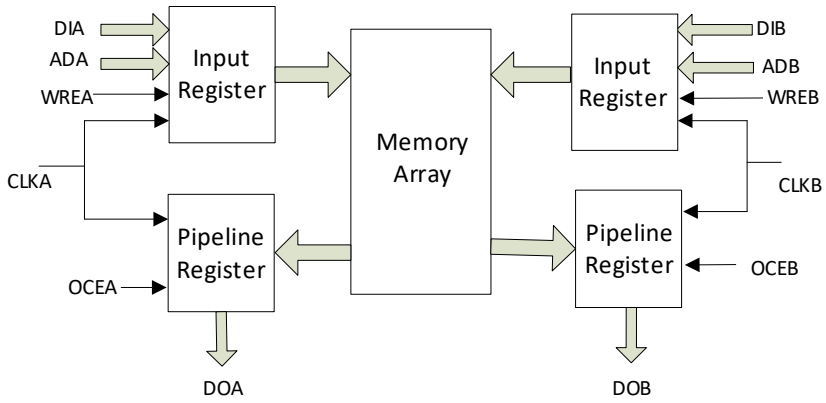
When a synchronous write cycles into a memory array with pipeline registers enabled, the data can be read from pipeline registers in the next clock cycle. The data bus can be up to 36 bits in this mode.

Bypass Mode

When a synchronous write cycles into a memory array with pipeline registers bypassed, the outputs are registered at the memory array.

Figure 2-9 Pipeline Mode in Single Port Mode, Dual Port Mode, and Semi-dual Port Mode





Write Mode

NORMAL MODE

In this mode, when you write data to one port, the output data of this port does not change. The written data will not appear at the read port.

WRITE-THROUGH MODE

In this mode, when you write data to one port, the written data will appear at the output of this port.

READ-BEFORE-WRITE MODE

In this mode, when you write data to one port, the written data will be stored in the memory according to the address, and the original data in this address will appear at the output of this port.

Note!

Read-before-write is not supported in DP mode.

2.5.8 Clock Mode

Table 2-7 lists the clock modes in different BSRAM modes:

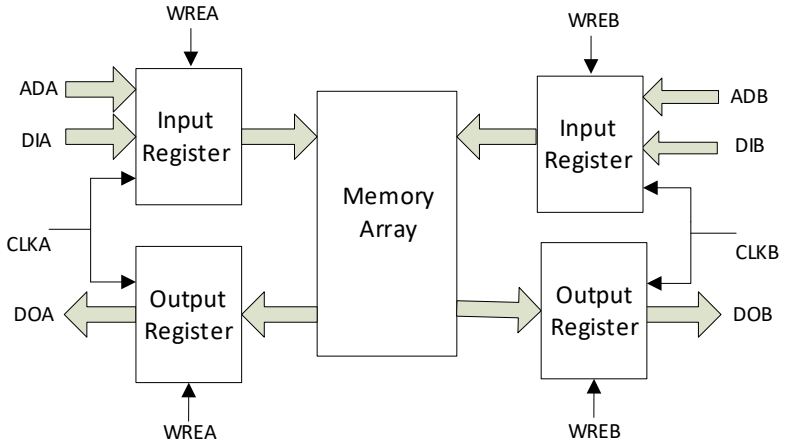
Table 2-7 Clock Modes in Different BSRAM Modes

Clock Mode	Dual Port Mode	Semi-Dual Port Mode	Single Port Mode
Independent Clock Mode	Yes	No	No
Read/Write Clock Mode	Yes	Yes	No
Single Port Clock Mode	No	No	Yes

Independent Clock Mode

Figure 2-10 shows the independent clock operation in dual port mode with one clock at each port. CLKA controls all the registers at Port A; CLKB controls all the registers at Port B.

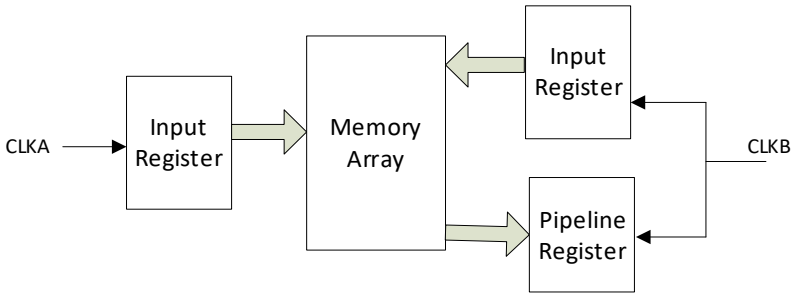
Figure 2-10 Independent Clock Mode



Read/Write Clock Mode

Figure 2-11 shows the read/write clock operation in semi-dual port mode with one clock at each port. The write clock (CLKA) controls data inputs, write addresses and read/write enable signals of Port A. The read clock (CLKB) controls data outputs, read addresses, and read enable signals of Port B.

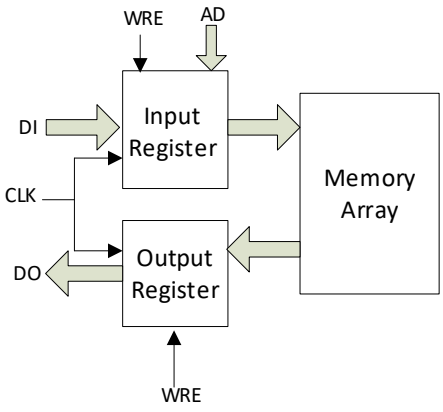
Figure 2-11 Read/Write Clock Mode



Single Port Clock Mode

Figure 2-12 shows the clock operation in single port mode.

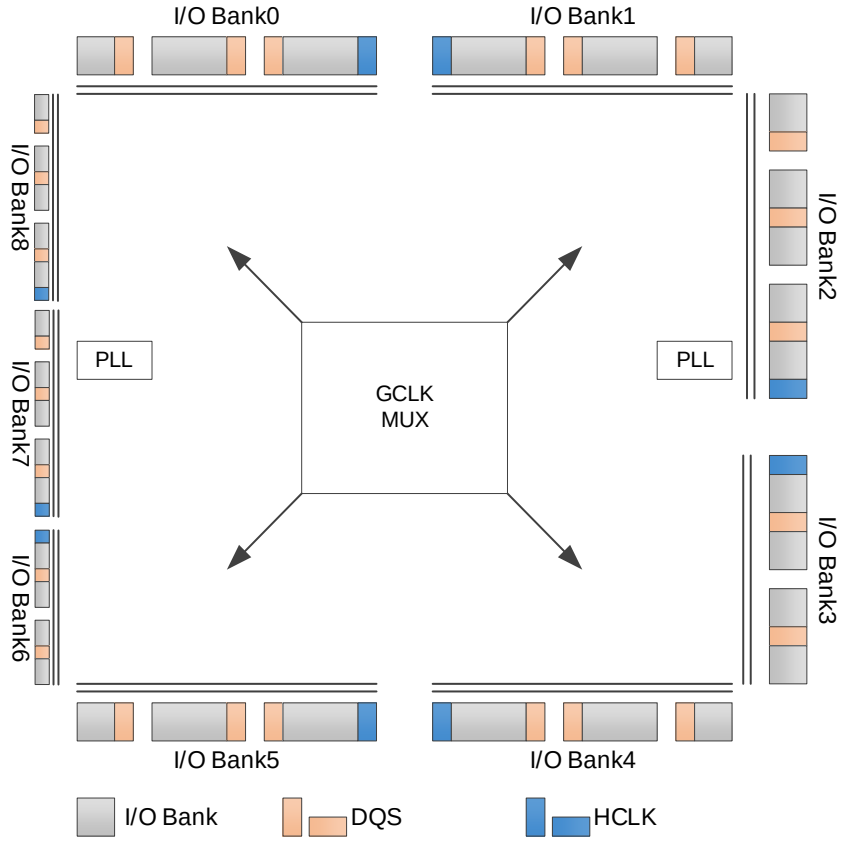
Figure 2-12 Single Port Clock Mode



2.6 Clocks

The clock resources and wiring are critical for high-performance applications in FPGA. The GW2AN series of FPGA products provide global clocks (GCLKs) which connect to all the registers directly. In addition, high-speed clocks (HCLKs), PLLs, DQSs, etc. are provided.

Figure2-13 GW2AN Clock Resources



2.6.1 Global Clocks

The Global Clock(GCLK) resources are distributed in the device as four quadrants. Each quadrant provides eight GCLKs. The clock sources of GCLKs include dedicated clock input pins and CRUs, and better clock performance can be achieved by using the dedicated clock input pins.

2.6.2 PLLs

The PLL (Phase-locked Loop) is one kind of feedback control circuit. The frequency and phase of the internal oscillator signal are controlled by the external input reference clock.

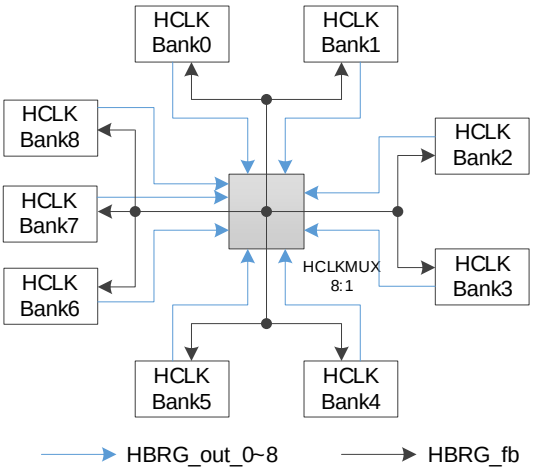
PLLs in the GW2AN series of FPGA products can provide synthesizable clock frequencies. Frequency adjustment (multiplication and division), phase adjustment, and duty cycle adjustment can be achieved by configuring the parameters.

2.6.3 High-speed Clocks

The high-speed clocks (HCLKs) are designed to facilitate high-

performance I/O data transmission and are specifically tailored for source synchronous data transmission protocols, see Figure 2-14.

Figure 2-14 GW2AN HCLK Distribution



As shown in Figure 2-14, there is an 8:1 HCLKMUX module in the middle of the HCLK. HCLKMUX can send the HCLK signal from any bank to another, providing enhanced flexibility in the utilization of HCLK.

The function modules that are available for the HCLK resources include:

- DHCEN: Dynamic enable modules for the high-speed clocks. Its function is similar to that of DQCE. It is used to turn on/off the high-speed clock signal dynamically.
- CLKDIV/CLKDIV2: Frequency division modules for the high-speed clocks. There is one CLKDIV in each bank. It is used to generate a frequency-divided clock with the same phase as the input clock, which is used in the IO logic mode.
- DCS: Dynamic GCLK selectors.
- DLLDLY: Dynamic delay adjustment modules for the clock signals input via the dedicated clock pins.

2.6.4 DDR Memory Interface Clock Management(DQS)

The DQS module of the GW2AN series of FPGA products provides the following features to support the clocking requirements of the DDR memory interface:

- Receives DQS inputs, sorts out waveforms and shifts 1/4 phase
- Provides read/write pointers for the input buffer
- Provides a data valid signal for internal logic
- Provides DDR output clock signals
- Supports DDR3 write voltage control

The DQS module supports three modes for different I/O interfaces.

For more information on the GCLKs, HCLKs, and DQSs, see UG286, Gowin Clock User Guide.

2.7 Long Wires

As a supplement to the CRU, the GW2AN series of FPGA products provide another kind of routing resource - the long wire, which can be used for clock, clock enable, set/reset, or other high fan out signals.

2.8 Global Set/Reset

The GW2AN series of FPGA products offer a dedicated global set/reset (GSR) network that connects directly to the device's internal logic and can be used as asynchronous/synchronous set or asynchronous/synchronous reset, with the registers in the CFUs and I/Os being able to be configured independently.

2.9 Programming & Configuration

The GW2AN series of FPGA products support SRAM configuration, and the configuration data needs to be re-downloaded upon each power-up. You can also store the configuration data in either the internal Flash or an external Flash. In this case, the GW2AN device loads the configuration data from the internal Flash or the external Flash into the SRAM upon power-up.

In addition to JTAG, the GW2AN series of FPGA products also offer support for GOWINSEMI's own GowinCONFIG configuration modes, including SSPI, MSPI, CPU, SERIAL. For more information, please refer to *UG702, GW2AN-18X & 9X Programming and Configuration Guide*.

2.9.1 I²C Timing Characteristics

Note!

- The SDA pin is not open-drain.
- Supports point-to-point applications.
- Supports connecting multiple chips of the same series to the bus at the same time and configuring them through broadcasting.

Figure 2-15 I²C Timing Diagram

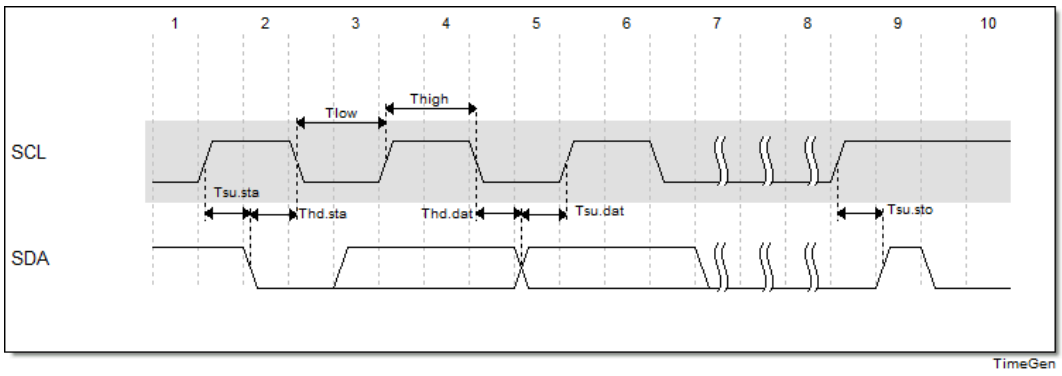


Table 2-8 I²C Timing Requirements for GW2AN-18X and GW2AN-9X

Symbol	Parameter	Min	Max	Unit
F_{SCL}	Clock Frequency	-	400	KHz
T_{low}	LOW period of the SCL	1.3	-	us
T_{high}	HIGH period of the SCL	0.6	-	us
$T_{hd.sta}$	Start Hold Time	0.6	-	us
$T_{su.sta}$	Start Setup Time	0.6	-	us
$T_{hd.dat}$	Data In Hold Time	80[1]	-	ns
$T_{su.dat}$	Data In Setup Time	500[1]	-	ns
$T_{su.sto}$	Stop Setup Time	0.6	-	us

Note!

- [1]: $T_{hd.dat}$ & $T_{su.dat}$ exceed the I²C specification.

2.10 On-chip Oscillator

The GW2AN series of FPGA products have an embedded programmable on-chip clock oscillator which provides a clock source for the MSPI configuration mode. See Table 2-9 for the output frequencies. The on-chip oscillator also provides a clock resource for user designs. Up to 64 clock frequencies can be obtained by setting the parameters. The following formula is used to get the output clock frequency:

f_{out}=200MHz/Param。

Note!

“Param” should be even numbers from 2 to 128.

Table 2-9 Output Frequency Options of the On-chip Oscillator

Mode	Frequency	Mode	Frequency	Mode	Frequency
0	2MHz[1]	8	6.25MHz	16	12.5MHz
1	4.3MHz	9	6.7MHz	17	14.3MHz
2	4.5MHz	10	7.1MHz	18	16.7MHz
3	4.8MHz	11	7.7MHz	19	20MHz
4	5.0MHz	12	8.3MHz	20	25MHz
5	5.3MHz	13	9.1MHz	21	33.3MHz
6	5.6MHz	14	10MHz	22	50MHz
7	5.9MHz	15	11.1MHz	23	100MHz

Note!

[1] The default frequency is 2MHz.

3 AC/DC Characteristics

Note!

Please ensure that you use Gowin's devices within the recommended operating conditions and ranges. Data beyond the working conditions and ranges are for reference only. Gowin does not guarantee that all devices will operate normally beyond the operating conditions and ranges.

3.1 Operating Conditions

3.1.1 Absolute Max. Ratings

Table 3-1 Absolute Max. Ratings

Name	Description	Min.	Max.
V_{CC}	Core voltage(LV version)	-0.5V	1.1V
	Core voltage(EV version)	-0.5V	1.32V
	Core voltage(UV version)	-0.5V	3.75V
V_{CCIO}	I/O Bank voltage	-0.5V	3.75V
V_{CCX}	Auxiliary voltage	-0.5V	3.75V
-	I/O voltage applied[1]	-0.5V	3.75V
Storage Temperature	Storage temperature	-65℃	+150℃
Junction Temperature	Junction temperature	-40℃	+125℃

Note!

- [1] Overshoot and undershoot of -2V to (V_{IHMAX} + 2)V are allowed for a duration of <20 ns.

3.1.2 Recommended Operating Conditions

Table 3-2 Recommended Operating Conditions[1]

Name	Description	Min.	Max.
V_{CC}	Core voltage(LV version)	0.95V	1.05V
	Core voltage(EV version)	1.14V	1.26V
	Core voltage(UV version)	2.375V	3.6V
V_{CCIO}[2]	I/O Bank voltage	1.14V	3.6V
V_{CCX}	Auxiliary voltage	2.7V	3.6V
T_{JCOM}	Junction temperature (commercial operation)	0℃	+85℃
T_{JIND}	Junction temperature (industrial operation)	-40℃	+100℃

Note!

- [1] For more information on the power supplies, please refer to *UG972, GW2AN-18X Pinout* and *UG978, GW2AN-9X Pinout* .
- [2] When the V_{CCIO5} voltage is below 2.0V, the static current of V_{CCIO5} will increase by about 20mA.
- The allowable ripples on V_{CC}, V_{CCIO}, and V_{CCX} are 3%, 5%, and 5% respectively. 1). For devices of which the PLL is powered directly with V_{CC}, the ripple on V_{CC} can affect the jitter characteristics of the PLL output clock; 2). The ripple on V_{CCIO} can eventually be passed on to the output waveform of the IO Buffer.

3.1.3 Power Supply Ramp Rates

Table 3-3 Power Supply Ramp Rates

Name	Description	Min.	Typ.	Max.
Ramp	Power supply ramp rates for all power supplies	0.1mV/μs	-	10mV/μs

Note!

- A monotonic ramp is required for all power supplies.
- All power supplies need to be in the operating range as defined in Table 3-2 before configuration. Power supplies that are not in the operating range need to be adjusted to a faster ramp rate, or you have to delay configuration.

3.1.4 Hot Socketing Specifications

Table 3-4 Hot Socketing Specifications

Name	Description	Condition	I/O Type	Max.
I_{HS}	Input or I/O leakage current	$0<V_{IN}<V_{IH}(MAX)$	I/O	150uA
I_{HS}	Input or I/O leakage current	$0<V_{IN}<V_{IH}(MAX)$	TDI,TDO, TMS,TCK	120uA

3.1.5 POR Specifications

Table 3-5 POR Parameters

Name	Description	Device	Name	Value
V_{POR_UP}	Power on reset ramp up trip point	GW2AN-9X	V_{CC}	TBD
			V_{CCX}	TBD
			V_{CCIO}	TBD

Name	Description	Device	Name	Value
		GW2AN-18X	V_{CC}	0.78V
			V_{CCX}	1.9V
			V_{CCIO}	0.95V
V_{POR_DOWN}	Power on reset ramp down trip point	GW2AN-9X	V_{CC}	TBD
			V_{CCX}	TBD
			V_{CCIO}	TBD
		GW2AN-18X	V_{CC}	0.63V
			V_{CCX}	1.3V
			V_{CCIO}	0.65V

3.2 ESD performance

Table 3-6 GW2AN ESD - HBM

Device	GW2AN-18X	GW2AN-9X
UG256	HBM>1,000V	HBM>1,000V
UG332	HBM>1,000V	–
UG324	HBM>1,000V	HBM>1,000V
UG400	HBM>1,000V	HBM>1,000V
UG484	HBM>1,000V	HBM>1,000V
PG256	HBM>1,000V	HBM>1,000V

Table 3-7 GW2AN ESD - CDM

Device	GW2AN-18X	GW2AN-9X
UG256	CDM>500V	CDM>500V
UG332	CDM>500V	–
UG324	CDM>500V	CDM>500V
UG400	CDM>500V	CDM>500V
UG484	CDM>500V	CDM>500V
PG256	CDM>500V	CDM>500V

3.3 DC Characteristics

3.3.1 DC Electrical Characteristics over Recommended Operating Conditions

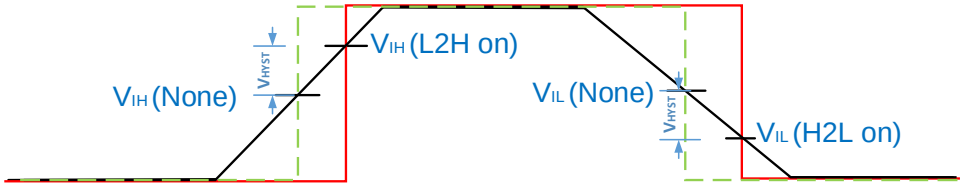
Table 3-8 DC Electrical Characteristics over Recommended Operating Conditions

Name	Description	Condition	Min.	Typ.	Max.
I_{IL},I_{IH}	Input or I/O leakage current	$V_{CCIO}<V_{IN}<V_{IH}$(MAX)	-	-	210μA
		$0<V_{IN}<V_{CCIO}$	-	-	10μA
I_{PU}	I/O Active Pull-up Current	$0<V_{IN}<0.7V_{CCIO}$	-30μA	-	-150μA
I_{PD}	I/O Active Pull-down Current	V_{IL}(MAX)$<V_{IN}<V_{CCIO}$	30μA	-	150μA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN}=V_{IL}$(MAX)	30μA	-	-
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN}=0.7V_{CCIO}$	-30μA	-	-
I_{BHLO}	Bus Hold Low Overdrive Current	$0\le V_{IN}\le V_{CCIO}$	-	-	150μA
I_{BHHO}	Bus Hold High Overdrive Current	$0\le V_{IN}\le V_{CCIO}$	-	-	-150μA
V_{BHT}	Bus Hold Trip Points	-	V_{IL}(MAX)	-	V_{IH}(MIN)
C1	I/O Capacitance	-	-	5pF	8pF
V_{HYST}	Hysteresis for Schmitt Trigger inputs	V_{CCIO}=3.3V, Hysteresis=L2H[1],[2]	-	240mV	-
		V_{CCIO}=2.5V, Hysteresis=L2H	-	140mV	-
		V_{CCIO}=1.8V, Hysteresis=L2H	-	65mV	-
		V_{CCIO}=1.5V, Hysteresis=L2H	-	30mV	-
		V_{CCIO}=3.3V, Hysteresis=H2L[1],[2]	-	200mV	-
		V_{CCIO}=2.5V, Hysteresis=H2L	-	130mV	-
		V_{CCIO}=1.8V, Hysteresis=H2L	-	60mV	-
		V_{CCIO}=1.5V, Hysteresis=H2L	-	40mV	-
		V_{CCIO}=3.3V,Hysteresis=HIGH[1],[2]	-	440mV	-
		V_{CCIO}=2.5V,Hysteresis=HIGH	-	270mV	-
		V_{CCIO}=1.8V,Hysteresis=HIGH	-	125mV	-

Name	Description	Condition	Min.	Typ.	Max.
		V_{CCIO}=1.5V,Hysteresis=HIGH	-	70mV	-

Note!

- [1] Hysteresis="NONE", "L2H", "H2L", "HIGH" indicates the Hysteresis options that can be set when setting I/O Constraints in the FloorPlanner tool of Gowin EDA, for more details, see *SUG935, Gowin Design Physical Constraints User Guide*.
- [2] Enabling the L2H (low to high) option means raising V_{IH} by V_{HYST}; enabling the H2L (high to low) option means lowering V_{IL} by V_{HYST}; enabling the HIGH option means enabling both L2H and H2L options, i.e. V_{HYST}(HIGH) = V_{HYST}(L2H) + V_{HYST}(H2L). The diagram is shown below.



3.3.2 Static Current

Table 3-9 Static Current

Device	Name	Description	Device type	C8/I7	C7/I6
				Typ.	Typ.
GW2AN-LV9X GW2AN-LV18X	I_{CC}	V_{CC} current (V_{CC}=1.0V)	LV	-	30mA
	I_{CCX}	V_{CCX} current (V_{CCX}=3.3V)	LV	-	12mA
	I_{CCIO}[1]	V_{CCIO} current (V_{CCIO}=2.5V)	LV	-	1mA
GW2AN-UV9X GW2AN-UV18X	I_{CC}+I_{CCX}	V_{CCX} current + V_{CC} current(V_{CCX}= V_{CC}=3.3V)	UV	-	46mA
	I_{CCIO}[1]	V_{CCIO} current (V_{CCIO}=2.5V)	UV	-	2mA
GW2AN-EV9X GW2AN-EV18X	I_{CC}	V_{CC} current (V_{CC}=1.2V)	EV	-	34mA
	I_{CCX}	V_{CCX} current (V_{CCX}=3.3V)	EV	-	12mA
	I_{CCIO}[1]	V_{CCIO} current (V_{CCIO}=2.5V)	EV	-	2mA

Note!

[1] When the V_{CCIO5} voltage is below 2.0V, the static current of V_{CCIO5} will increase by about 20mA.

3.3.3 Recommended I/O Operating Conditions

Table 3-10 Recommended I/O Operating Conditions

Name	V_{CCIO} (V) for Output			V_{REF} (V) for Input		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVTTL33	3.135	3.3	3.6	-	-	-
LVCMOS33	3.135	3.3	3.6	-	-	-
LVCMOS25	2.375	2.5	2.625	-	-	-
LVCMOS18	1.71	1.8	1.89	-	-	-
LVCMOS15	1.425	1.5	1.575	-	-	-
LVCMOS12	1.14	1.2	1.26	-	-	-

Name	V_{CCIO} (V) for Output			V_{REF} (V) for Input		
	Min.	Typ.	Max.	Min.	Typ.	Max.
SSTL15	1.425	1.5	1.575	0.68	0.75	0.9
SSTL18_I	1.71	1.8	1.89	0.833	0.9	0.969
SSTL18_II	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I	2.375	2.5	2.645	1.15	1.25	1.35
SSTL25_II	2.375	2.5	2.645	1.15	1.25	1.35
SSTL33_I	3.135	3.3	3.6	1.3	1.5	1.7
SSTL33_II	3.135	3.3	3.6	1.3	1.5	1.7
HSTL18_I	1.71	1.8	1.89	0.816	0.9	1.08
HSTL18_II	1.71	1.8	1.89	0.816	0.9	1.08
HSTL15	1.425	1.5	1.575	0.68	0.75	0.9
PCI33	3.135	3.3	3.6	-	-	-
LVPECL33E	3.135	3.3	3.6	-	-	-
MLVDS25E	2.375	2.5	2.625	-	-	-
BLVDS25E	2.375	2.5	2.625	-	-	-
RSDS25E	2.375	2.5	2.625	-	-	-
LVDS25E[1]	2.375	2.5	2.625	-	-	-
SSTL15D	1.425	1.5	1.575	-	-	-
SSTL18D_I	1.71	1.8	1.89	-	-	-
SSTL18D_II	1.71	1.8	1.89	-	-	-
SSTL25D_I	2.375	2.5	2.625	-	-	-
SSTL25D_II	2.375	2.5	2.625	-	-	-
SSTL33D_I	3.135	3.3	3.6	-	-	-
SSTL33D_II	3.135	3.3	3.6	-	-	-
HSTL15D	1.425	1.575	1.89	-	-	-
HSTL18D_I	1.71	1.8	1.89	-	-	-
HSTL18D_II	1.71	1.8	1.89	-	-	-

Note!

V_{CCIO} of banks using True LVDS is recommended to be set to 2.5V.

3.3.4 Single-ended I/O DC Characteristics

Table 3-11 Single-ended I/O DC Characteristics

Name	V_{IL}		V_{IH}		V_{OL} (Max)	V_{OH} (Min)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min	Max	Min	Max				
LVCMOS33 LVTTL33	-0.3V	0.8V	2.0V	3.6V	0.4V	V_{CCIO}-0.4V	4	-4
							8	-8
							12	-12
							16	-16
							24	-24

Name	V_{IL}		V_{IH}		V_{OL} (Max)	V_{OH} (Min)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min	Max	Min	Max				
					0.2V	V_{CCIO}-0.2V	0.1	-0.1
LVCMOS25	-0.3V	0.7V	1.7V	3.6V	0.4V	V_{CCIO}-0.4V	4	-4
							8	-8
							12	-12
							16	-16
					0.2V	V_{CCIO}-0.2V	0.1	-0.1
LVCMOS18	-0.3V	0.35 x V_{CCIO}	0.65 x V_{CCIO}	3.6V	0.4V	V_{CCIO}-0.4V	4	-4
							8	-8
							12	-12
					0.2V	V_{CCIO}-0.2V	0.1	-0.1
LVCMOS15	-0.3V	0.35 x V_{CCIO}	0.65 x V_{CCIO}	3.6V	0.4V	V_{CCIO}-0.4V	4	-4
							8	-8
					0.2V	V_{CCIO}-0.2V	0.1	-0.1
LVCMOS12	-0.3V	0.35 x V_{CCIO}	0.65 x V_{CCIO}	3.6V	0.4V	V_{CCIO}-0.4V	2	-2
							4	-4
					0.2V	V_{CCIO}-0.2V	0.1	-0.1
PCI33	-0.3V	0.3 x V_{CCIO}	0.5 x V_{CCIO}	3.6V	0.1 x V_{CCIO}	0.9 x V_{CCIO}	1.5	-0.5
SSTL33_I	-0.3V	V_{REF}-0.2V	V_{REF}+0.2V	3.6V	0.7	V_{CCIO}-1.1V	8	-8
SSTL25_I	-0.3V	V_{REF}-0.18V	V_{REF}+0.18V	3.6V	0.54V	V_{CCIO}-0.62V	8	-8
SSTL25_II	-0.3V	V_{REF}-0.18V	V_{REF}+0.18V	3.6V	NA	NA	NA	NA
SSTL18_II	-0.3V	V_{REF}-0.125V	V_{REF}+0.125V	3.6V	NA	NA	NA	NA
SSTL18_I	-0.3V	V_{REF}-0.125V	V_{REF}+0.125V	3.6V	0.40V	V_{CCIO}-0.40V	8	-8
SSTL15	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCIO}-0.40V	8	-8
HSTL18_I	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCIO}-0.40V	8	-8
HSTL18_II	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	NA	NA	NA	NA
HSTL15_I	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCIO}-0.40V	8	-8
HSTL15_II	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	NA	NA	NA	NA

Note!

[1] The total DC current limit(sourced and sunk current) of all IOs in the same bank: the total DC current of all IOs in the same bank shall not be greater than n*8mA, where n represents the number of IOs bonded out from a bank.

3.3.5 Differential I/O DC Characteristics

Table 3-12 Differential I/O DC Characteristics

LVDS

Name	Description	Test conditions	Min.	Typ.	Max.	Unit
V_{INA},V_{INB}	Input Voltage		0	-	2.4	V
V_{CM}	Input Common Mode Voltage	Half the Sum of the Two Inputs	0.05	-	2.35	V
V_{THD}	Differential Input Threshold	Difference Between the Two Inputs	±100	-	±600	mV
I_{IN}	Input Current	Power On or Power Off	-	-	±10	μA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 100Ω	-	-	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 100Ω	0.9	-	-	V
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T = 100Ω	250	350	450	mV
ΔV_{OD}	Change in V_{OD} Between High and Low		-	-	50	mV
V_{OS}	Output Voltage Offset	(V_{OP} + V_{OM})/2, R_T = 100Ω	1.125	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} Between High and Low		-	-	50	mV
I_S	Short-circuit current	V_{OD} = 0V outputs short-circuited	-	-	15	mA

3.4 Switching Characteristics

3.4.1 CFU Switching Characteristics

Table 3-13 CFU Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
t_{LUT4_CFU}	LUT4 delay	-	0.337	ns
t_{LUT5_CFU}	LUT5 delay	-	0.694	ns
t_{LUT6_CFU}	LUT6 delay	-	1.005	ns
t_{LUT7_CFU}	LUT7 delay	-	1.316	ns
t_{LUT8_CFU}	LUT8 delay	-	1.627	ns
t_{SR_CFU}	Set/Reset to Register output	-	0.93	ns
t_{CO_CFU}	Clock to Register output	-	0.38	ns

3.4.2 BSRAM Switching Characteristics

Table 3-14 BSRAM Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
t_{COAD_BSRAM}	Clock to output from read address/data	-	2.55	ns
t_{COOR_BSRAM}	Clock to output from output register	-	0.28	ns

3.4.3 Gearbox Switching Characteristics

Table 3-15 Gearbox Timing Parameters

TBD

3.4.4 Clock and I/O Switching Characteristics

Table 3-16 External Switching Characteristics

Name	Description	Device	C8/I7		C7/I6		Unit
			Min	Max	Min	Max	
Pin-LUT-Pin Delay[1]	Pin(IOxA) to Pin(IOxB) delay	GW2AN-18X	-	3.83	-	4.59	ns
$T_{HCLKdly}$	HCLK tree delay	GW2AN-18X	-	0.82	-	0.98	ns
$T_{GCLKdly}$	GCLK tree delay	GW2AN-18X	-	1.77	-	2.12	ns

Note!

[1] Test conditions：V_{CCIO}=3.3V, V_{CCX}=3.3V, LVCMOS33, 8mA, 15pF load.

3.4.5 On-chip Oscillator Switching Characteristics

Table 3-17 On-chip Oscillator Switching Characteristics

Name	Description	Min.	Typ.	Max.
f_{MAX}	Output Frequency (0 to +85℃)	106.25MHz	125MHz	143.75MHz
	Output Frequency (-40 to +100℃)	100MHz	125MHz	150MHz
t_{DT}	Output Clock Duty Cycle	43%	50%	57%
t_{OPJIT}	Output Clock Period Jitter	0.01UIPP	0.012UIPP	0.02UIPP

3.4.6 PLL Switching Characteristics

Table 3-18 PLL Switching Characteristics

Device	Speed Grade	Name	Min.	Max.
GW2AN-18X	C8/I7	CLKIN	3MHz	500MHz
		PFD	3MHz	500MHz
		VCO	500MHz	1250MHz
		CLKOUT	3.90625MHz	1250MHz
	C7/I6	CLKIN	3MHz	400MHz
		PFD	3MHz	400MHz

Device	Speed Grade	Name	Min.	Max.
		VCO	400MHz	1000MHz
		CLKOUT	3.125MHz	1000MHz
GW2AN-9X	C8/I7	CLKIN	3MHz	500MHz
		PFD	3MHz	500MHz
		VCO	500MHz	1250MHz
		CLKOUT	3.90625MHz	1250MHz
	C7/I6	CLKIN	3MHz	400MHz
		PFD	3MHz	400MHz
		VCO	400MHz	1000MHz
		CLKOUT	3.125MHz	1000MHz

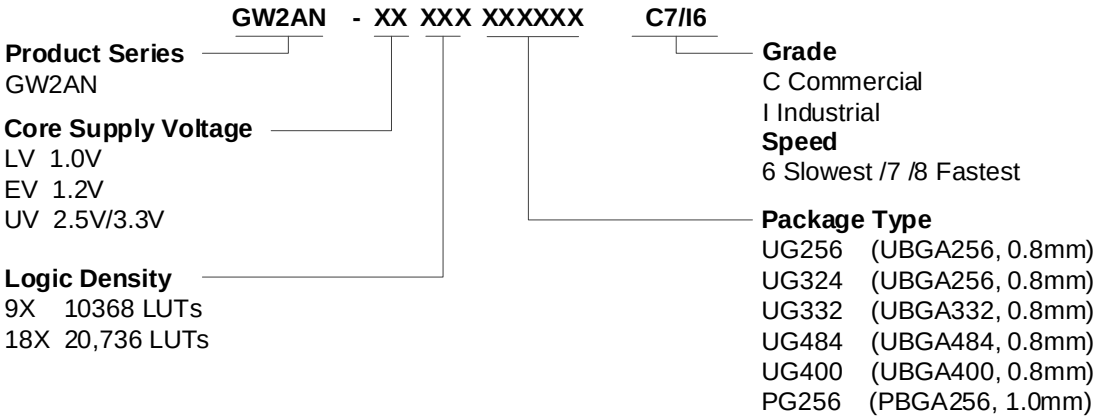
3.5 Configuration Interface Timing Specification

The GW2AN series of FPGA products support multiple GowinCONFIG modes, including MSPI, SSPI, SERIAL, CPU. For more information, please refer to *UG702, GW2AN-18X & 9X Programming and Configuration Guide*.

4 Ordering Information

4.1 Part Naming

Figure 4-1 Part Naming – Production



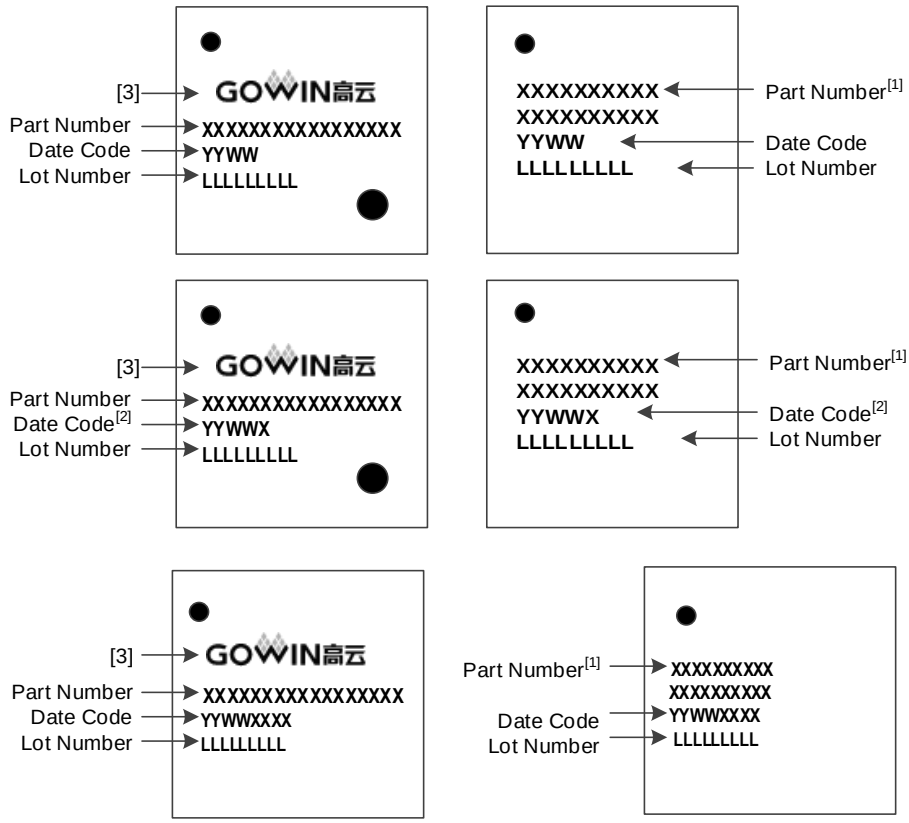
Note!

- For more information about the packages, please refer to 1.2 Product Resources.
- The LittleBee® family devices and Arora family devices of the same speed grade have different speeds.
- Both “C” and “I” are used in Gowin’s part name marking for one device. GOWIN devices are screened using industrial standards, so the same device can be used for both industrial (I) and commercial (C) applications. The maximum temperature of the industrial grade is 100°C, and the maximum temperature of the commercial grade is 85°C. Therefore, if the chip meets speed grade 7 in commercial grade applications, its speed grade will be 6 in industrial grade applications.

4.2 Package Markings

Gowin's devices have markings on the their surfaces, as shown in Figure 4-2.

Figure 4-2 Package Marking Examples



Note!

- [1] The first two lines in the right figure(s) above are both the "Part Number".
- [2] The Date Code followed by an "X" is for X version devices.
- [3] Whether the package marking bears the Gowin Logo or not depends on the package type, package size, and Part Number length. The above figure are only examples of the package markings.

5 About This Guide

5.1 Purpose

This datasheet provides a comprehensive overview of the GW2AN series of FPGA products, including their features, resources, architecture, AC/DC characteristics, and ordering details. It aims to enhance accessibility and facilitate the effective utilization of Gowin's devices.

5.2 Related Documents

The latest documents are available at www.gowinsemi.com.

- UG702, GW2AN-18X & 9X Programming and Configuration Guide
- UG973, GW2AN-18X and GW2AN-9X Package & Pinout User Guide
- UG972, GW2AN-18X Pinout
- UG978, GW2AN-9X Pinout

5.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are shown in Table 5-1.

Table 5-1 Terminology and Abbreviations

Terminology and Abbreviations	Full Name
ALU	Arithmetic Logic Unit
BSRAM	Block Static Random Access Memory
CFU	Configurable Function Unit
CLS	Configurable Logic Section
CRU	Configurable Routing Unit
DCS	Dynamic Clock Selector
DP	True Dual Port 16K BSRAM
DQCE	Dynamic Quadrant Clock Enable
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable IO
IOB	Input/Output Block
LUT4	4-input Look-up Table
LUT5	5-input Look-up Table
LUT6	6-input Look-up Table
LUT7	7-input Look-up Table
LUT8	8-input Look-up Table
PG	PBGA
PLL	Phase-locked Loop
REG	Register
SDP	Semi Dual Port 16K BSRAM
SP	Single Port 16K BSRAM
SSRAM	Shadow Static Random Access Memory
TDM	Time Division Multiplexing
UG	UBGA

5.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail：support@gowinsemi.com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